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Phase I Report

COMPUTER COMPONENTS DEVELOPMENT

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

ABSTRACT

This report represents the work performed under Phase I of the contract. The object of Phase I was to determine a reasonable design philosophy and to conduct preliminary investigations to verify the soundness of the design approach. Under Phase I, studies were limited to techniques and components which could be suitably incorporated into dynamic switching circuits utilizing semiconductor diode logic and vacuum-tube power devices. Conventional transformer designs are being considered to obtain the necessary impedance transformations.

The remainder of this report contains a discussion of the design philosophy which is being followed in the development of high-speed switching components. This is followed by descriptions and results of component tests which have been made. Also included in this report is a description of a promising circuit configuration utilizing diode logic and a cascode power amplifier. The report is concluded with a brief outline of the direction of future effort.

OBJECTIVE

The object of this program is the engineering development of a basic set of switching elements which may be used to fabricate certain specific logical configurations. It is desired that the circuitry developed be capable of operating at switching rates which are an order of magnitude greater than rates presently employed in conventional digital switching circuits. This implies that the circuitry must operate effectively at a switch rate of 10 mc/sec. Another objective of the program is the determination and clarification of basic limitations of the component parts of the circuitry.

DESIGN PHILOSOPHY

It is almost impossible to design high-speed switching circuitry on a hit-or-miss basis. This is due primarily to the inadequacies or limitations of the basic elements. None of the basic elements—diodes, tubes, transformers, etc.—are perfect. The successful circuit design must function correctly in spite of these basic difficulties. The task of the circuit designer is the optimization of the circuit design so that the best possible performance is obtained. In other words, the designer must be acutely aware of the limitations of the basic component, and the design must account for these limitations.

Component limitations are the primary factors governing the specification of the basic design philosophy. Let us then begin the discussion of design philosophy with a short explanation of the component limitations.

Perhaps the worst limitation arises from the capacitance associated with the basic components. All components such as tubes and diodes have shunt capacitance between elements. There also exists additional capacitance in the form of stray capacitance due to wiring. In order to produce a voltage pulse at a given point, it is necessary first to charge the capacitance at that point. An examination of a typical dynamic circuit configuration would reveal that capacitance is charged from three components, diode gates, tubes, or transformers. The gates and the tubes will approximate constant current generators while the output from the transformers approximates a constant voltage generator. With a constant current generator the effect of capacitance is obtained from the following equations:

$$e = 1/C \int_0^t i \, dt$$

$$\text{if} \quad i = 0, \; t < 0$$

$$i = I, \; t \geq 0$$

then

$$\Delta e = I/C \, \Delta t \; .$$

The ratio of $\Delta e/\Delta t$ is determined by the ratio of I/C.

As a base, consider the standard one-megacycle dynamic circuitry used in the SEAC, MIDAC, and various other computers. The goal is to increase the operation speed of this basic circuit by at least a factor of ten. Can the capacitance at the various critical points be decreased by a factor of ten? The answer is obviously no. It is apparent that the capacitance which presently exists cannot be substantially reduced. Some small reduction of capacitance is obtainable if more direct wiring is employed. However, this reduction may be nullified if the tube selected for the power amplifier has greater interelectrode capacitances than the 6AN5.

Next let us consider the effects obtained if the circuit action is speeded up by increasing the available charging current I. If perfect diodes were available, this would be a feasible solution, except from the viewpoint of power dissipation. However, presently available diodes suffer undesirable transient effects during the switching interval. In particular, the transient recovery of diodes from conduction to nonconduction must be given serious study. The diode does not recover instantly, due to the existence of the minority carriers in the diode at the time of switching. The diode is not switched until these carriers have diffused out of the active diode region. The number of carriers found in the diode at the time of switching is proportional to the magnitude of the forward current. Thus, for any given diode the fastest recovery time is obtained with the minimum forward current. The recovery time will roughly increase in proportion to an increase in forward current. Preliminary studies have indicated that back recovery effects are not as serious as might first be expected. Even so, it is still important to obtain fast recovery times. This means that only small increases in charging current can be obtained. The increase in charging current will never approach an order of magnitude.

One consideration remains. If the voltage Δe is reduced, a faster operation can be achieved. This means that a gate designed to give a 10-v pulse at 1 mc/sec should function adequately at 10 mc if the voltage swing is reduced to 1 v. This is the desired low-current gate. The reduction of the gate-voltage swing must be accompanied by a proportional increase in the g_m of the power amplifier tube. In the MIDAC 1 mc/sec circuits the 6AN5 tube has an effective g_m of about 7000 μmhos. A MIDAC gate structure operating at 10 mc/sec requires a pentode-type tube with a g_m of 70,000 μmhos. It is possible with existing tubes to achieve a g_m of 50,000 μmhos.

Let us now examine in somewhat more detail the effects of g_m and gate-voltage changes on the performance of a dynamic switching circuit.

A transformer of optimum design will deliver a secondary current of magnitude

$$I_s = \frac{I_p^2 T}{4E_o C_p} \qquad I_g N = I_s$$

where

I_p is the primary current,

C_p is the capacitance seen at the primary,

E_o is the magnitude of the pulse from the secondary,

T is the rise time desired,

I_g is the current required for one gate drive, and

N is the maximum permissible number of gate drives.

Now

$$I_p = g_m E_g ,$$

where E_g is the grid swing.

The loss occurring in the gating can be accounted for by setting

$$E_g = A E_o \qquad A < 1 .$$

E_g may also be expressed in terms of current and capacitance:

$$E_g = \frac{B I_g T}{C_g} ,$$

where

C_g is the capacitance seen by the output of the gating circuit, and

B is the efficiency of the gating configuration.

Combining the previous formulae yields

$$N = \frac{g_m^2 T^2 AB}{4 C_p C_g}$$

or

$$N = \frac{M^2 T^2 E}{4} ,$$

where

$M = \frac{g_m}{\sqrt{C_p C_g}}$, a figure of merit, and

E = AB, the gate efficiency defined as the product of the gate-structure current and voltage-transfer ratios.

For the purpose of illustration assume

$$T = 10^{-8} \text{ sec},$$

$$E = 1/25, \text{ and}$$

$$M = 5 \times 10^{9} \text{ rad/sec}.$$

For the above values N = 25. It is noted that a rather inefficient gate structure was assumed. Also, the formula does not account for transformer losses which certainly are not negligible at 10 mc/sec. In spite of various losses which have been neglected, the above calculation is important. It indicates that 10-mc dynamic circuitry which will provide an adequate number of gate drives can be achieved.

Little has been said about the transformer design. The ultimate efficiency of a transformer at high frequencies seems to be primarily dependent on the core material. To be sure, different methods of construction produce better transformers, but at high frequencies the core material seems to remain the dominant factor. It appears that the choice of a core material must be a compromise between permeability and core losses. Existing ferrites which have high permeability also have high losses; those with low losses have lower permeabilities. It is impossible at this time to predict the exact behavior of high-frequency core material, for the reduction of permeability is perhaps counterbalanced by the reduced losses, which should tend to increase the time rate of change of flux density B even though ΔB has decreased. Experimentation and study are required to determine the optimum transformer.

In brief, the design philosophy adopted seeks to minimize the gating currents and the gate-voltage swing. The power-amplifier design effort is directed toward a circuit having a very high g_m and an excellent figure of merit. Pentodes and cascoded triodes seem best suited for this application. The type of gate structure to be used or the number of gate drives required is at present an open question. We shall determine the optimum gate structure for high-frequency operation and the maximum number of gate drives available.

INVESTIGATIONS OF VACUUM-TUBE DRIVER CONFIGURATIONS

THEORETICAL COMPARISON OF VACUUM TUBES

As stated earlier in this report, the number of gate drives, N, for serial dynamic circuitry may be expressed as

$$N = \frac{M^2 T^2 E}{4},$$

where

$$M = \frac{g_m}{\sqrt{C_p C_g}}, \text{ rad/sec,}$$

T = pulse rise time, sec, and

E = gate efficiency.

The quantity M may be defined as a vacuum-tube figure of merit for this type of circuitry; in order to obtain the largest number of gate drives at a given repetition rate, M should be as large as possible. Consequently, a survey of available tubes has been conducted with a view toward a maximum M. The results of this survey are presented in Table I.

From Table I it is clear that the best of the conventional tubes is the 436A tetrode. However, some of the triodes available have extremely large transconductances and would have a better figure of merit than the 436A if it were not for the Miller effect capacity. The cascode circuit described in the next section reduces the Miller capacitance and thereby increases the figure of merit.

THE CASCODE CIRCUIT

The cascode circuit of Fig. 1 represents an approach which reduces the input capacitance due to the Miller effect. A high figure of merit is thereby obtained from the very-high-g_m triodes. The Miller effect in this circuit depends on the gain to the plate of tube one, K_1; K_1 is small because the plate load for tube one is the impedance looking into the cathode of tube two, which is a small impendance approximately equal to $1/g_m$.

Thus we may write

$$C_{in} = C_{gk} + (1 - K_1) C_{pg} . \tag{1}$$

In order to determine the input capacitance, one must first determine the impedance R_e looking into the cathode of tube two. R_e may be found from a consideration of the equivalent circuit of Fig. 2. The following equations are written by inspection of the equivalent circuit:

$$I_p = \frac{-\mu (E_g - E_{p1})}{2r_p + R_L} \tag{2}$$

$$E_{p1} = -\mu E_g - I_p r_p . \tag{3}$$

Substituting (3) into (2) and simplifying, one obtains

$$I_p = \frac{-\mu E_g (\mu + 1)}{(\mu+2) r_p + R_L} \tag{4}$$

TABLE I

COMPARISON OF FIGURE OF MERIT OF VACUUM TUBES

	6AN5	6AK5	6AH6	404A	435A	418A	436A	5857	417A	437A	416A
C_{gp} ($\mu\mu f$)	0.075	0.01	0.03	0.05	0.035	0.05	0.07	0.004	1.8	3.5	1.25
C_{in} ($\mu\mu f$)	9.0	3.9	10.0	7.0	7.9	16	15	9.3	9.0	11.5	6.5
C_{out} ($\mu\mu f$)	4.8	2.85	2.0	2.5	2.9	2.7	3.5	2.2	.48	.9	0.7
g_m (ma/volt)	8	5	9	12.5	15.5	25	30	20	24	45	50
$M = \frac{g_m}{\sqrt{C_{in}\, C_{out}}}$ (rad/μsec)	1210	1490	2010	2990	3240	3790	4130	4410 (1)	(2)	(2)	(2)

(1) Secondary emission type.
(2) See section on the cascode circuit.

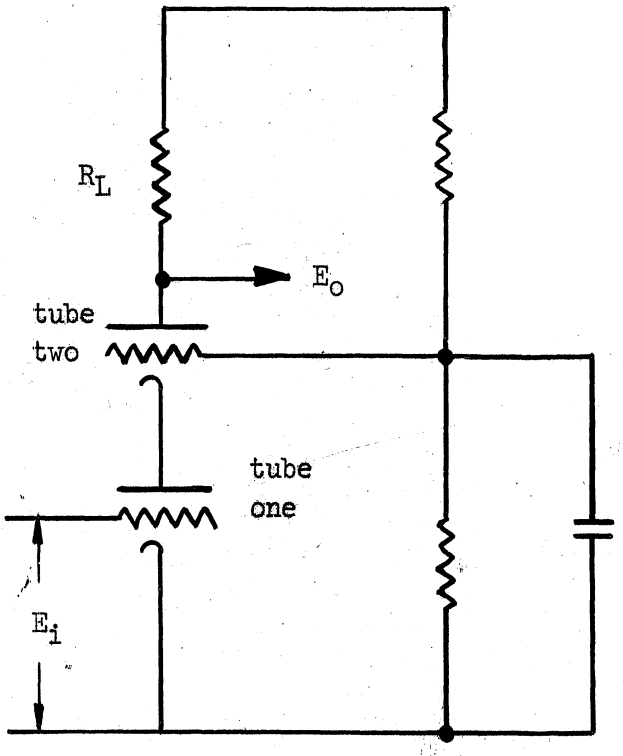


Fig. 1. The cascode circuit.

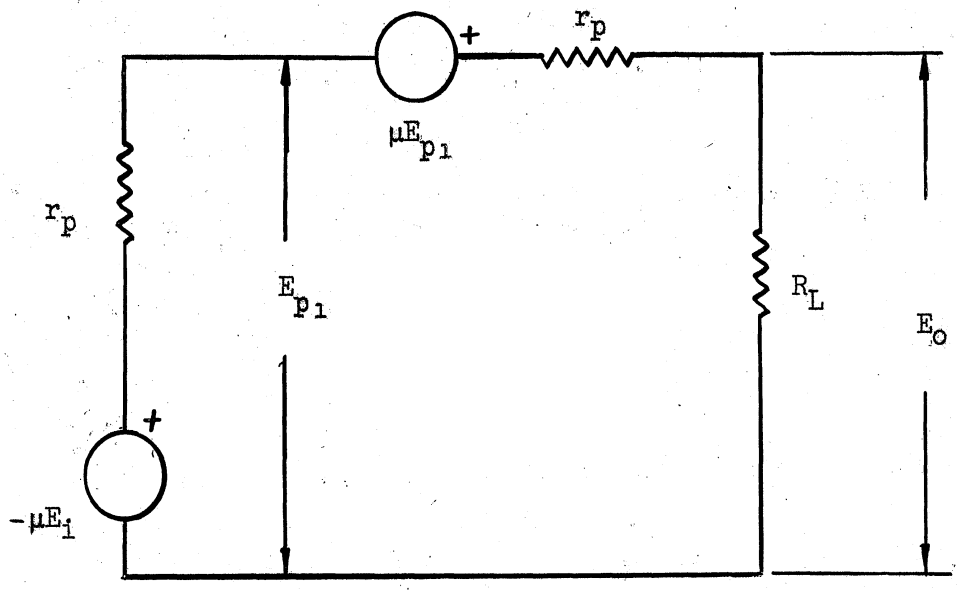


Fig. 2. Cascode equivalent circuit.

Substituting (4) into (3), one has

$$E_{p1} = \mu E_g + \frac{\mu E_g (\mu + 1) r_p}{(\mu + 2) r_p + R_L} \qquad (5)$$

The impedance we desire is evidently the ratio of voltage to current at that point:

$$R_e = \frac{E_{p1}}{I_p} \quad . \tag{6}$$

Substituting (4) and (5) into (6), one has finally

$$R_e = \frac{r_p + R_c}{\mu + 1} \quad . \tag{7}$$

The gain K_1 is that of a triode with plate load R_e:

$$K_1 = \frac{-\mu R_e}{r_p + R_e} \tag{8}$$

$$= \frac{-\mu (r_p + R_L)}{(\mu + 2) r_p + R_L} \quad .$$

Therefore, from (1) the input capacitance is

$$C_i = C_{gk} + \left[\frac{\mu (r_p + R_L)}{(\mu + 2) r_p + R_L} + 1\right] C_{gp} \quad . \tag{9}$$

If $R_L \ll (\mu + 2) r_p$, this may be simplified to

$$C_i \doteq C_{gk} + (2 + R_L/r_p) C_{gp} \quad . \tag{10}$$

The figure of merit of the cascode circuit is also dependent on the output capacitance, which is evidently the capacitance plate-to-grid plus some fraction of the capacitance plate-to-cathode since this latter capacitance does not have the full output voltage impressed. The effect of C_{pk} will be that of a capacitance whose size is C_{pk} multiplied by the ratio of the voltage impressed on C_{pk} to the total output voltage. Thus

$$C_{out} = C_{pg} + \frac{K_2 - K_1}{K_2} C_{pk} \tag{11}$$

where K_2 = overall gain.
The gain K_2 is

$$K_2 = E_o/E_i = (R_L I_p)/E_i \quad . \tag{12}$$

Substituting I_p from (8), one has

$$K_2 = \frac{-\mu (\mu + 1) R_L}{(\mu + 2) r_p + R_L} \quad . \tag{13}$$

If $R_L \ll (\mu + 2) r_p$, this reduces to

$$K_2 \doteq -(\mu/r_p)\, R_L = -g_m R_L \quad . \tag{14}$$

Substituting the values for K_1 and K_2 into the formula for output capacitance, one has

$$C_{out} \doteq C_{pg} + \frac{\mu(\mu+1) R_L - \mu(r_p + R_L)}{\mu(\mu+1) R_L} C_{pk}$$

$$\doteq C_{pg} + (1 - 1/(g_m R_L)\, C_{pk} \quad . \tag{15}$$

The figures of merit for particular tubes in a cascode configuration with an overall gain of 20 are presented in Table II. Of these tubes, the 416A is evidently the best. A test circuit using the 437A triode has been studied experimentally in order to study the feasibility of the cascode circuit.

TABLE II

FIGURE OF MERIT OF CASCODE TRIODES WITH AN OVERALL GAIN OF 20

	417A	437A	416A
C_{in} ($\mu\mu$f)	13.5	20.1	8
C_{out} ($\mu\mu$f)	3.28	4.4	2
g_m (ma/volt)	24	45	50
M (rad/μsec)	3600	4780	12,500

EXPERIMENTAL PERFORMANCE OF THE 436A TETRODE COMPARED WITH CASCODE 437A TRIODES

The theoretical performance of the cascode 437A's is slightly better (approximately 14%) than that of a single 436A. Experimental performance has been observed with a 3:1 transformer matched to a 100-ohm secondary load as the plate load. The transformer was wound on a Ferroxcube 3-C ferrite cup core; this is not the best possible transformer, but it serves to compare vacuum tubes. The grid input consisted of pulses at approximately a 10.6 mc/sec repetition rate with a pulse duration of about 0.03 μsec. The bias, plate supply, and input signal voltages were adjusted for each tube so that the maximum signal output was obtained within the rating of the tube. The results, given in Table III, show that the output current per volt of drive is approximately 16% more for the 437A. Thus the 437A's maintain their theoretical superiority in experiment.

TABLE III

COMPARISON OF THE 436A TETRODE AND CASCODE 437A TRIODES

	B+	Bias	Grid Signal E_g, volts	Output Current I_o, ma	$\frac{I_o}{E_g}$
437A	250	-2.6	5.2	340	69.2
436A	120	-4	4.6	260	56.5

TYPICAL OPERATION OF CASCODE 437A'S

The large grid swing used in the foregoing section for comparing the 437A and 436A tubes would be impractical in a computer circuit because 20-ma gates would be required to produce the 5.2-v grid swing at 10 mc. A more realistic 4-ma gate will deliver 1 v to the grid; with a -0.5-v bias, the cascode circuit will then produce about 100 ma in the 100-ohm load through the 3:1 transformer at 10.6 mc. Again it is emphasized that the transformer core material used in these 10-mc experiments was intended for 1-mc operation; it is anticipated that the use of ferrites designed for high-frequency application will result in a better transformer.

DIRECTION OF FUTURE DEVELOPMENT

Power Amplifier.—Although the difference in performance of the 436A and 437A tubes is perhaps not great enough to justify the use of two tubes in the cascode circuit, the 416A will theoretically perform three times as well as the 436A. Since the cascode configuration has worked well with one tube type, it is reasonable to expect that the theoretical advantage of the 416A will be realized. Hence, future experimental pulse amplifiers will consist of cascode 416A triodes.

Diode Structures.—Preliminary diode investigations have been concerned with the characteristics of various commercial diodes. Future effort is to be directed toward studies of gating configuration using now-ideal diodes.

Transformer Design.—Transformer studies which are just beginning will consist of a study of commercially available core materials and sample transformers. In particular, we seek an optimum transformer design compatible with the cascode power amplifier.

THEORETICAL STUDIES OF DIODE GATING STRUCTURES

INTRODUCTION

The basic MIDAC–SEAC package has, for purpose of analysis, been broken down into three parts: input logic configuration, tube, and transformer. This section deals particularly with the problems associated with the input logic circuit operation at high clock repetition rates.

To date the major portion of the work done on gate design has assumed ideal diodes. However, it was felt at the beginning that considerable attention should be directed toward considering the diodes as nonlinear circuit elements. Thus, a diode testing program was begun to evaluate currently available diodes under conditions more typical of the anticipated gate structure than those conditions specified by the manufacturer.

The point-contact diodes exhibit a sharp reverse current spike when switched from a forward to a reverse bias condition. It is this reverse transient and the associated recovery time which are of major interest in the design of high-speed switching circuits.

The approach taken to this problem has been first to study the factors affecting recovery and second to consider both analytically and experimentally the importance of the non-ideal diode behavior in the overall circuit operation.

Although there is a "best" diode, the conclusion to date is that if forward currents through the diode are limited to 2 ma, any good point-contact diode will work satisfactorily at pulse widths of .04 μsec.

REVERSE TRANSIENT

If some assumptions are made regarding the diode, it is possible to obtain a solution for this reverse current as a function of time.

1. If the cross-sectional dimensions are much greater than the diode thickness, then the problem becomes one dimensional.

2. A point-contact diode can be approximated by a junction diode. Test results show this to be a reasonable assumption.

3. If the concentration of $P \gg N$, then it can be assumed that current flow at the junction is only hole current.

Since the hole current at the junction is equal to the total current, and if an expression is known for the current at the junction, the reverse current at any cross section is completely described.

Current flow is composed of conduction and diffusion components:

$$I = q \mu_p E_p - q D_p \frac{\partial P}{\partial x} , \tag{16}$$

where

q = charge of an electron or hole,

μ_p = hole mobility in the N region,

E_p = magnitude of the electric field in the N region,

D_p = diffusion constant for holes in the N region, and

$\frac{\partial P}{\partial x}$ = hole density gradient in the N region.

At the junction, current flow is by diffusion only:

$$I_r\Big|_{x=0} = - q D_p \frac{\partial P}{\partial x} . \tag{17}$$

Thus, to solve for the reverse current it is then necessary to solve the continuous-flow or one-dimensional diffusion equation (18) for the proper set of boundary conditions associated with the reverse current transient:

$$\frac{\partial P}{\partial t} = \frac{P_{no} - P}{\tau_p} + D_p \frac{\partial^2 P}{\partial^2 x} , \tag{18}$$

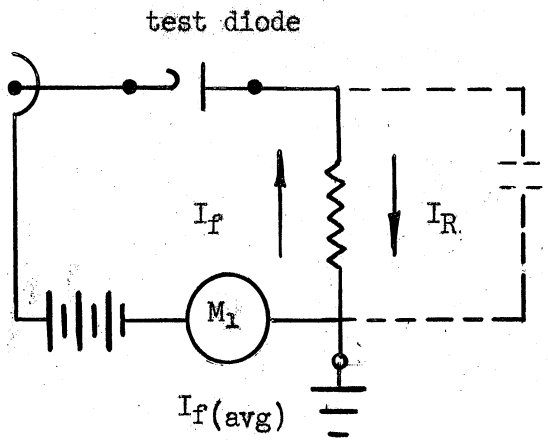
where

P = hole density in N region,

P_{no} = hole concentration in N region under conditions of no externally applied bias, and

τ_p = life-time of holes in N region.

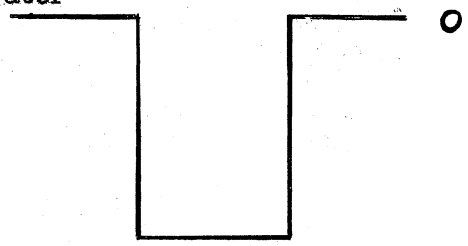
The reverse transient is composed of durations T_1 and T_2. (See Fig. 3.) After a semiconductor diode has been passing current in the forward direction for a period of time sufficient to allow the hole density P to reach its steady-state value, the concentration gradient is as shown in Fig. 4a. When the bias is reversed, the concentration gradient assumes successive conditions at times t_1, t_2, t_3, and t_4.



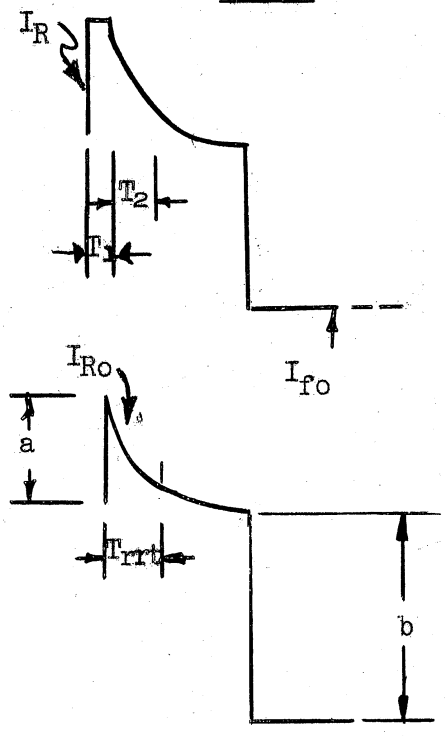
I_f = forward current
I_R = reverse current
E_b = back bias

Input

25-kc square using Tektronix type 105 generator



Output

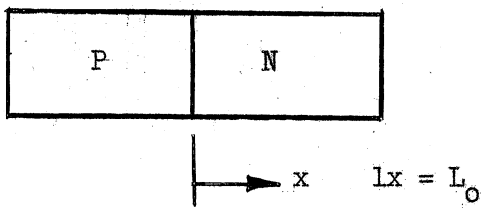


T_{rrt} = reverse recovery time has been defined here to be the time in μsec for $I_r = .33\ I_{Ro}$

$T_{rrt} = T_1 + T_2$ for junction diodes

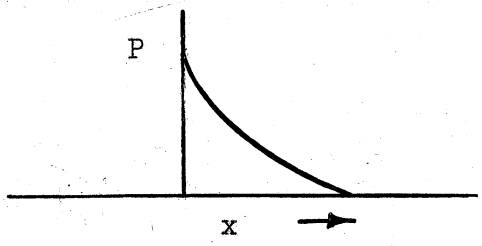
$T_{rrt} = T_2$ for point-contact diodes where $T_1 \ll T_2$

Fig. 3. Reverse transient measurement.



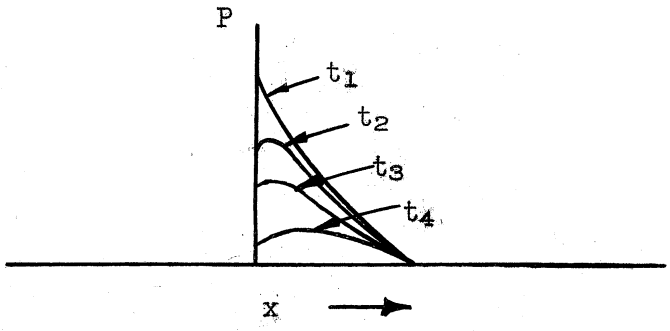
Steady-State Hole Concentration

(a)



Hole Concentration for Reverse Bias Condition During T_1

(b)



Hole Concentration for Reverse Bias Condition During T_2

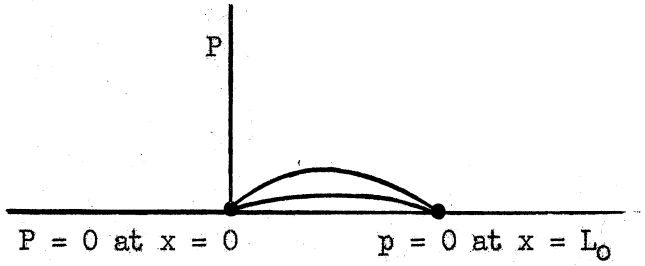


Fig. 4. Theoretical junction diode.

During T_1 the hole diffusion out of the N region is limited by the resistance of the external circuit. Thus T_1 is a function of the external circuit resistance and the previous forward current.*

Reverse recovery time measurements have shown that for point-contact and small junction diodes $T_1 \ll T_2$. One possible reason for this would be the relatively small volume of P and N material used in the construction of the above type diode as compared to the larger volumes used in such junction diodes as the G.E. 1N91, where T_1 does become an important factor.

Since $T_1 \ll T_2$ here, we can limit our interest to the time T_2. Reverse recovery time (T_{rrt}) is equal to T_2 for the diodes considered. (See Fig. 3.)

Thus we are interested in solving the diffusion equation for the following boundary conditions (see Fig. 4): $R = 0$, $x = 0$ and $P = 0$, $x = L_o$ at $t = 0$, to obtain $P = f(x,t)$ $t \geq 0$.

The procedure is to solve Equation 18 for the boundary conditions given and thus evaluate two of the three resulting constants. However, in order to satisfy the third constant it is necessary to require Equation 19 to equal Equation 20 at $t = 0$:

$$P = f(x,t) \quad \text{for } t \geq 0 \tag{19}$$

$$P = f(x,t) \quad \text{for } t < 0 . \tag{20}$$

Equations 19 and 20 both result from the solution of Equation 18, but Equation 20 is the steady-state solution for hole density before switching bias conditions.

The mathematical steps have been omitted as routine methods of solving partial differential equations are used:

$$P = P_{n\,max} \left[\frac{\sin h \frac{L_o - x}{L}}{\sin h \left(L_o/L\right)} \right] \tag{19}$$

$$P_{n\,max} = \sum_{1}^{m} \frac{2}{m\pi} \sin \frac{m\pi x}{L_o} \left[1 + \left(\frac{L_o}{m\pi L} \right)^2 \right]^{-1}$$

$$= x \exp \left[- \frac{t}{\tau_p} \left(1 + \left(\frac{m\pi L}{L_o} \right)^2 \right) \right]. \tag{20}$$

*Sometimes reference is made to holes being swept out of the N region. It is true that those holes adjacent to the junction are "swept out," but the majority of the N region holes "die" as a result of recombination.

Then from Equation 17 at $x = 0$ and $L_o/L \ll 1$,

$$I_r = -2\,q\,P_{n\,max}\,\frac{D_p}{L_o}\exp\left[\left(-\frac{t}{\beta}\right)\right], \tag{21}$$

where

$$\beta = \frac{\tau_p\,L_o^2}{\pi\,L^2}\,.$$

The diffusion constant is related to hole mobility by Einstein's relation

$$D_p = \frac{kT}{q}\,\mu_p \tag{22}$$

$\therefore$

$$\beta = \left(\frac{L_o^2\,q}{\pi^2\,k}\right)\frac{1}{T\mu_p}\,,$$

where

$P_{n\,max}$ = maximum hole concentration on the N side of the junction under steady-state forward bias conditions,

L_o = length of N region,

$L = \sqrt{D_p\tau_p}$,

T = absolute temperature in degrees, and

k = Boltzmann's constant.

Certainly as small β as possible is desired. However, care should be taken in drawing conclusions, especially in regard to temperature effects. The model taken is quite simple, and such considerations as surface recombination have been neglected.

However, there are three conclusions that can be drawn:

1. Since hole mobility (μ_p) is less than electron mobility (μ_e), there would be a gain in recovery time if the current was primarily electron current rather than hole current as assumed here.

2. The hole mobility of silicon (μ_p) is less than the hole mobility for germanium (μ_p). Therefore, diodes made from basic germanium may be superior to silicon diodes of identical construction.

3. Most certainly small dimensions are very important as L_o appears as a squared term.

There are a number of factors that affect reverse recovery time (T_{rrt}).

1. T_{rrt} is a function of the diode physics by Equation 21.

2. T_{rrt} is a function of steady-state forward current (I_f).

Notice in Equation 21 that the term $P_{n\ max}$ appears. By Boltzmann's equation governing diffusion across the junction,

$$P_{n\ max} = P_{no}\, \epsilon^{\frac{q\ E_{ex}}{RT}} . \tag{23}$$

E_{ex} is the external forward bias, and is a function of forward current (I_f)

3. T_{rrt} is a function of pulse rate (prf).

If the pulse rate is such that the forward-current steady-state condition is not reached, then the reverse recovery time is certainly less.

4. Reverse recovery time has been assumed equal to T_2, but if T_1 is not negligible, circuit resistance then becomes much more important.

5. The back bias E_b also affects back recovery time, but to a much lesser extent than would be expected.

Considering all the above,

$$T_{rrt} = f(I_f, \text{prf}, E_b, R_c, C_j) . \tag{24}$$

The junction capacitance (C_j) has been included. The junction between the N and P regions is also referred to in the literature as the depletion layer. This physical capacitance is to be distinguished from an "effective hole-storage capacitance" resulting from the hole storage in the N region.

If a correlation were found between measured capacitance and recovery time, it would indicate the hole-storage effect would be unimportant compared to charge storage of C_j. Recovery time and capacitances have been measured, and it has been found that there is no correlation, as would be expected.

It can be shown that junction capacitance is a function of back bias (E_b). The junction between the two types of crystalline impurities is characterized by a lack of holes and electrons in what is known as the depletion layer. Adjacent to this region there are fixed ions that are not neutralized by the mobile carriers in the respective regions. This situation is then exactly equivalent to the parallel-plate capacitor where

$C = \epsilon A/s$,

ϵ = dielectric constant,

A = cross-sectional area, and

s = distance between plates.

As E_b is increased, the depletion layer widens and the capacitance C_j decreases.

REVERSE TRANSIENT MEASUREMENTS

Equation 24 summarizes the factors affecting reverse recovery time. Figure 5 illustrates the type of data taken on a number of types of point-contact diodes. The HD-2182 diode has been used for illustration because of its relative consistency.

Notice the following:

1. T_{rrt} is independent of circuit resistance.

2. T_{rrt} increases monotonically with increased forward current.

3. The junction capacitance C_j and the reverse recovery time T_{rrt} as functions of E_b are apparently related. However, data from other diodes have shown C_j vs E_b to be essentially constant for all point-contact diodes while T_{rrt} vs E_b curves vary between the dashed limits shown not only for various diode types but within a particular type. Thus, $T_{rrt} \neq f(C_j)$.

4. T_{rrt} increased with reduced E_b, indicating that a large-amplitude input pulse to the "and" gate would be desired if T_{rrt} were critical in the "and" gate structure.

Although exceptions to each of the above have been observed, particularly among the 1N191 and 1N117, the remarks above can be made regarding point-contact diodes in general. The following types have been tested: 1N117, 1N191, French 1N191, H.D. 2109*, H.D. 2182*, and a new silicon-junction diode by Hughes with a very good recovery time. If consistency of characteristic trends can be defined as well behaved, the starred (*) diodes have this characteristic of dependability.

Table IV is included to support the following proposition. That is, good recovery times may be expected among all types of point-contact diodes. Therefore, other properties will probably be the determining factors in picking a good diode.

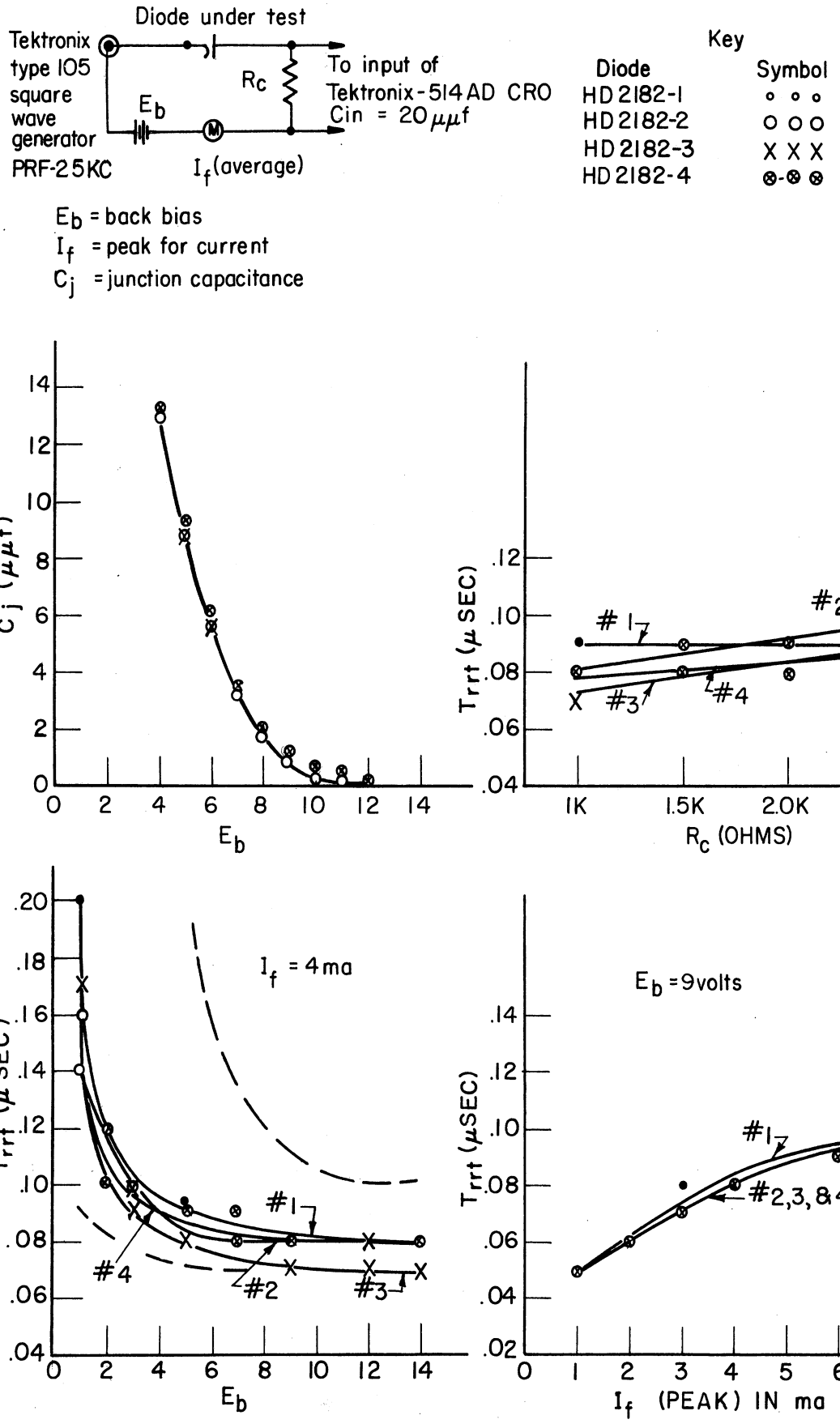


Fig. 5. Reverse transient characteristics.

TABLE IV

DISTRIBUTION OF DIODE TYPES BASED ON RECOVERY TIME MEASUREMENTS

T_{rrt} in μsec	I_f = 2 ma						I_f = 4 ma					
	1N117	1N191	F1N191	150	2109	2182	1N117	1N191	F1N191	150	2109	2182
.00												
.01												
.02												
.03												
.04	x	x										
.05	xxxx	xxx			xx		x					
.06	x		x	x		xxxx	xxxx	x				
.07			x	x			x		x			
.08	x	x					x	x		x	x	xxxx
.09			xx							x	x	
.10	x		x					xx	x			
.11									x			
.12							x	x	x			
.13	x								x			
.14												
.15												
.16												
.17												
.18												
.19												
.20												

E_b = 9 volts in all cases

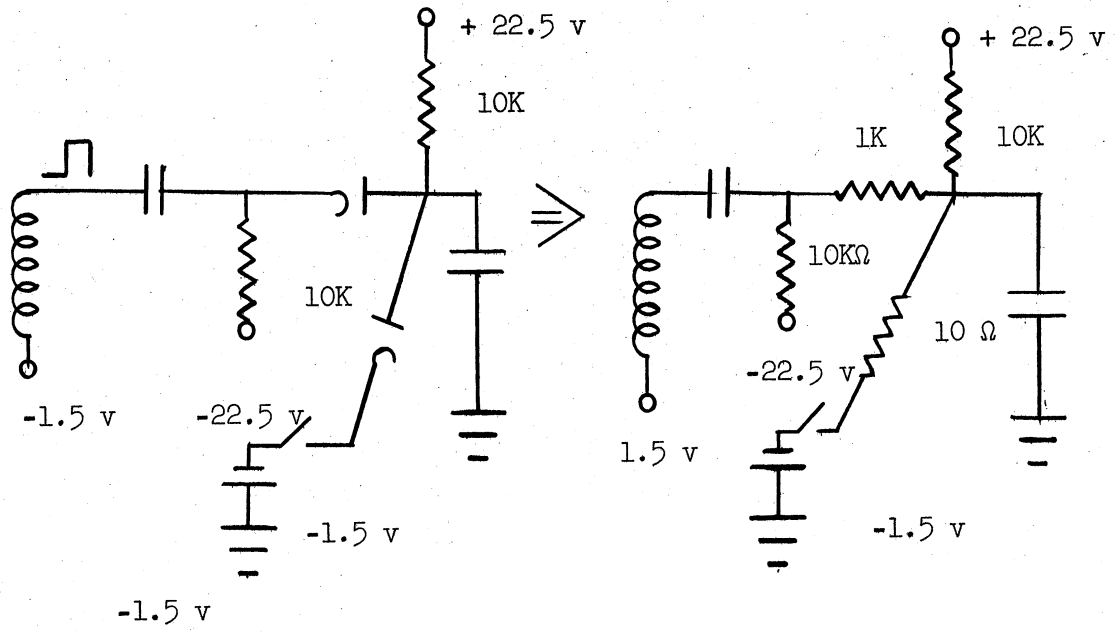
From Fig. 3, $a/b = I_{RO}/I_f$. Let R_{BO} = initial back resistance and R_f = forward steady-state resistance. Then from Fig. 3, if $a/b = 1$, $R_{BO} = R_f$, and if $a/b \ll 1$, $R_{BO} \gg R_f$.

Thus, if the diode in switching from forward to back bias can be assumed to be a nonlinear resistance element of the form $R_{BO}\, e^{\alpha t}$ the importance of $a/b = 1$ is apparent. Two diodes, H.D. 2109 and Hughes Si-Junction, have very desirable a/b ratios (Table V).

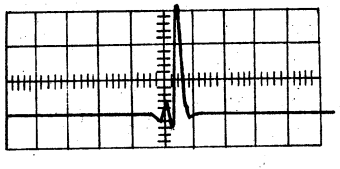
To illustrate the importance of R_{BO} on a simple two-input and gate (truth = 1 = a pulse), the following experiment was tried:

For a good diode, $R_{BO} = 10^3\ \Omega$ is conservative. Therefore let $R_D = R_{BO}\, e^{t/T_{rrt}} = R_{BO}$ during the entire pulse.

Let $R_f = 10\ \Omega$

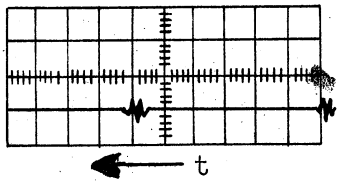


Vertical: 1 volt/cm
Horizontal: .1 μsec/cm



t

10 Ω resistor not pulled down



t

10 Ω resistor pulled down to simulate T = A · B

TABLE V

REVERSE TO FORWARD RESISTANCE RATIO

Diode	a/b Ratio	
	I_f = 2 ma	I_f = 4 ma
IN117 - 6	.6	.4
7	.8	.467
8	1.17	.867
9	.75	.433
IN191 - 4	.3	.183
5	.3	.175
6	.35	.267
F191 - 1	.566	.36
2	.566	.36
3	.67	.44
4	.70	.45
5	.67	.40
150 - 1	.60	.375
2	.95	.65
*HD 2109 - 1	.267	.14
2	.267	.14
HD 2182 - 1	1.13	.867
2	1.13	.90
3	1.07	.83
4	1.11	.83
E_b = 9 volts ⇄		
*Si-J** - 1	.278	.154
2	.972	.513
4	.930	.628

*These diodes have proven to be of superior quality.
**Silicon Junction

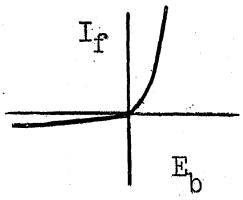
One point in regard to measurement of reverse transients is of particular importance; that is, the magnitude of the scope input capacitance (Fig. 3). Figure 6a data are taken on a 1N191 at high values of forward current under the test conditions indicated. Figure 6b illustrates the effect of increased scope capacitance.

Figure 6c is the Hughes published data for the 1N191, indicating a marked disagreement between these measured values and published data as they differ by a factor of 3. An increase in scope input capacitance could well account for these differences.

PRELIMINARY INVESTIGATION OF LOGICAL CONFIGURATIONS

Consider first the gating structure of Fig. 7a. For optimum design diodes at various points in the circuit require different characteristics.

For diode A it is desired to have the same voltage drop across it for various values of forward current as the purpose of this diode is to clamp point (2) as other gates are pulsed. That is, the slope of the static characteristic curve is large, or $\Delta E/\Delta I \longrightarrow 0$.



At I_f = 20 ma the following data were obtained:

Diode Type	Slope
HD 2182	20
French 1N191	10
HD 2109	6.66
1N117	6.00
1N191	3.5
Hughes Si-Junction	2.8

It is noticed in Table VI that the forward resistances, R_f, at lower values of I_f do not differ by an order of magnitude as indicated here. The change in slope at low value of forward current accounts for this difference.

Notice that diode D of Fig. 7a is also a grid clamp, but here $\Delta E/\Delta I$ is no longer of major concern as this diode, being on the "or" output, is either

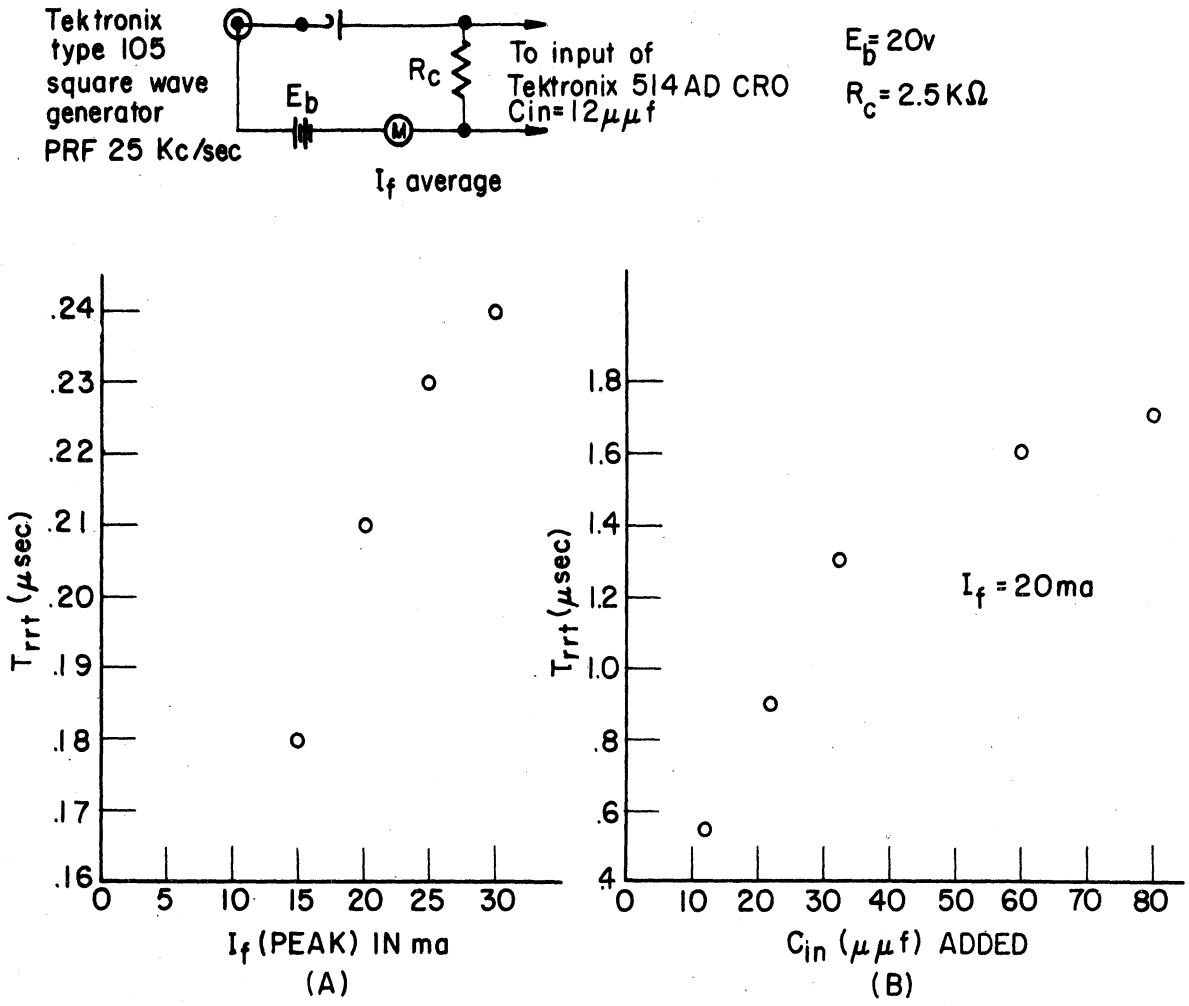


Fig. 6. Reverse transient characteristics of a 1N191.

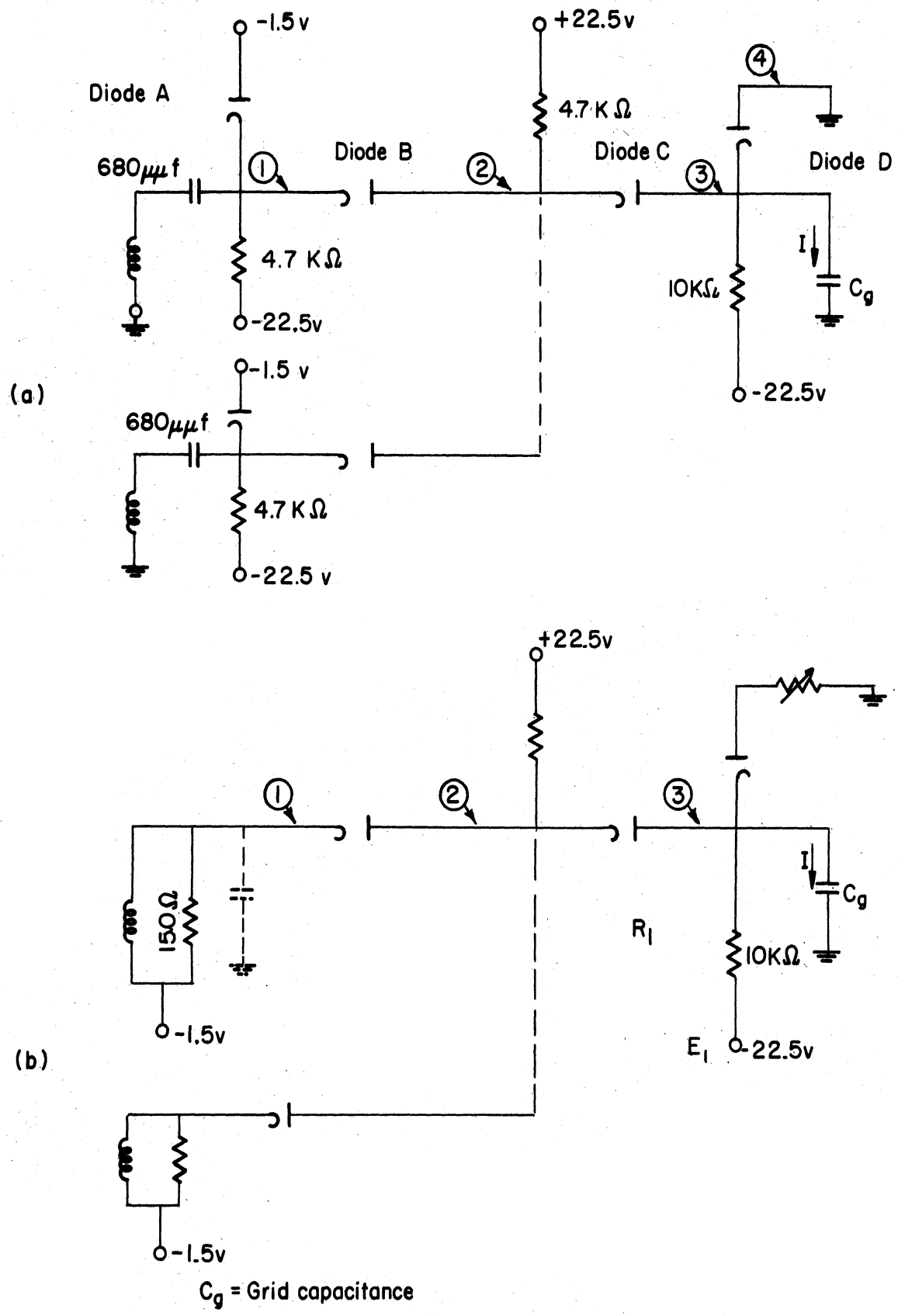


Fig. 7. Logic configuration.

TABLE VI

LOGIC STAGE VOLTAGE EFFICIENCY (A)

Diode*	I_f	D-C Volt Levels			R_f	Pulse Amplitude				A	CKT Condition
		1	2	3		1	2	3	3*		
1N117	2.25	-1.5	-1.05	-.35	156	4	3.4	1.6	1.90	47.5%	No Tube
HD 2109	2.25	-1.5	-1.00	-.30	134	4	3.5	2.1	2.40	60%	No Tube
HD 2182	2.25	-1.5	-1.00	-.30	134	4	3.4	1.6	1.9	47.5%	No Tube
Si-J	2.25	-1.5	-1.00	-.55	244	4	3.4	2.0	2.05	51.3%	No Tube
1N117	2.25	-1.5	-1.00	-.40	178	4	3.4	1.3	1.50	37.5%	With Tube
HD 2109	2.25	-1.5	-1.00	-.30	134	4	3.3	1.5	1.80	45%	With Tube
Si-J	2.25	-1.5	-1.00	-.55	244	4	3.2	1.6	1.65	41.3%	With Tube
1N117	4.5	-1.5	- .90	-.50	111	4	3.4	1.5	1.5	37.5%	No Tube
HD 2109	4.5	-1.5	- .90	-.40	89	4	3.5	1.9	2.0	50%	No Tube
HD 2182	4.5	-1.5	- .90	-.35	77.8	4	3.3	1.3	1.45	36.3%	No Tube
Si-J	4.5	-1.5	- .90	-.80	178	4	3.5	2.3	2.0	50%	No Tube
1N117	4.5										With Tube
HD 2109	4.5										With Tube
Si-J	4.5										With Tube
1N117	6.75	-1.6	- .90	-.50	74	4	3.3	1.3	1.3	37.5%	No Tube
HD 2109	6.75	-1.6	- .90	-.50	74	4	3.5	1.8	1.8	45%	No Tube
HD 2182	6.75	-1.6	- .90	-.40	59.3	4	3.2	0.9	1.0	25%	No Tube
Si-J	6.75	-1.6	- .90	+.40	59.3	4	3.5	1.1	2.0	50%	No Tube
1N117	6.75	-1.6	- .90	-.50	74	4	3.3	1.1	1.1	27.5%	With Tube
HD 2109	6.75	-1.6	- .90	-.50	74	4	3.4	1.4	1.4	35%	With Tube
Si-J	6.75	-1.6	- .85	-.60	88.9	4	3.4	1.6	1.5	37.5%	With Tube

I_f = steady-state forward current through the grid clamp diode.
*All of the above represent the best of the particular diode type.

conducting or it is not. In the work to date, it has been found important when designing for noise clipping to consider the d-c voltage drop across diode D as:

$$\left|E_{(2)d\text{-}c}\right| - \left|E_{(3)d\text{-}c}\right| \neq \left|E_{(2)d\text{-}c}\right| - \left|E_{(4)d\text{-}c}\right|$$

The transient effect of diode B is not critical for two reasons. First, during the transient time $R_{B0}\, e^{\alpha t}$ becomes large after a very short period. Second, when all gates are pulsed, the reverse current tends to charge the grid capacitance.

In both circuits of Fig. 7 it is the output clamp diode that is of major concern, as it is this diode that steals a portion of the charging current I.

In general, the principal problem is to get the grid up. If current I is needed to charge C_g, then R_1 and the pull-down supply E_1 are chosen such as to discharge C_g in the desired time. Therefore, asuuming C_g can be discharged, the forward transients of diodes, A, B, and D and the reverse transient of diode C after the pulse can be neglected.

Using essentially the circuit of Fig. 7a as a one-input "and" gate to determine possible transient effects in the diode B position, it was found that at I_f = 2.5 ma all point-contact diodes performed equally well.

When additional input was added to simulate the logical function $A\bar{B}$, the noise through the gate for a 3-v input pulse of .02-μsec duration was found to be approximately .3 v. If capacitance were put in parallel with the pulsed "and" diode, the following noise outputs were observed at point (2):

$C_{\mu\mu f}$	Noise Voltage
0	.3
10	1
20	1.5

The circuit of Fig. 7b is a simplification of the circuit of Fig. 7a. Since the d-c resistance of the transformer winding is $\doteq$ 0 Ω, the clamp diode may be eliminated by pulling down the secondary to - 1.5 v.

Formerly, the pulse transformer, had to supply $2I + \epsilon$ to raise the potential of point (1). However, in the present circuit, the transformer need put out only the sufficient current to the parallel combination of the damping resistance and wiring capacitance to cut off the "and" diode.

The current efficiency B as defined in the introduction now becomes equal to 1, whereas formerly it was at best equal to 1/2.

Since the grid-clamp diode is of major concern, the data of Table VI have been taken using the circuit in Fig. 7b to determine the voltage efficiency of a single input "and" gate for various types of output clamp diodes:

$$A = \text{voltage efficiency} = \frac{\text{pulse amplitude at point (3)}}{\text{pulse amplitude at point (1)}} .$$

The output column (3) has been corrected for the difference in noise clipping due to voltage drop across the clamp diode. For these tests, .4 v of noise clipping has been taken as standard.

Voltage efficiency decreases with increased forward current through the clamp diode as expected. Since the recovery times are roughly comparable for all point-contact diodes, it is thus substantiated that it is the a/b ratio or large R_{BO} that is the critical diode property.

With the tube included, the voltage efficiency of the circuit decreases by about 10% due to the grid drawing current during a portion of the pulse to obtain the high values of g_m.

In conclusion, the H.D. 2109 offers the best possibilities for the following reasons:

1. Low steady-state-forward resistance compared to the silicon-junction.

2. Small a/b ratio.

3. Good transient properties.

More of these diodes are on order as we originally had only a few samples.

DIRECTION OF FUTURE ANALYSIS

Future effort is to be placed on the realization of efficient high-frequency gating structures. Both experimental and analytical studies are contemplated. An analytical study of an or-and-or gating structure realized with non-ideal diodes has been started but no results are presently available. The effects of capacitance are included in the model under study. The results of this study should yield valuable design data pertaining to high-frequency gating structure using existing non-ideal diodes.