

SiGe/CMOS Millimeter-Wave Integrated Circuits and Wafer-Scale Packaging for Phased Array Systems

by

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To My Parents and Wife

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Chapter 1

Introduction

1.1 Phased Array Systems

Phased array systems have been proposed in the 1950's [1] and are widely used in communication and radar applications (Fig. 1.1). Phased array systems can achieve electronic beam forming and fast beam scanning much faster than mechanical systems [2–4]. For communication applications, phased array systems have been employed on either the transmitter or receiver side, or both.

Fig. 1.2 shows the basic concept of a phased array system with 8 antenna elements. For the receiver side, the radiated signal arrives at each antenna element of the array at a different time depending on the angle of incidence and the spacing between the antennas. The phased array system compensates for the time difference and combines the signals coherently while rejecting the signal from other directions. Similar explanation can be applied to the transmitter side with a spacial

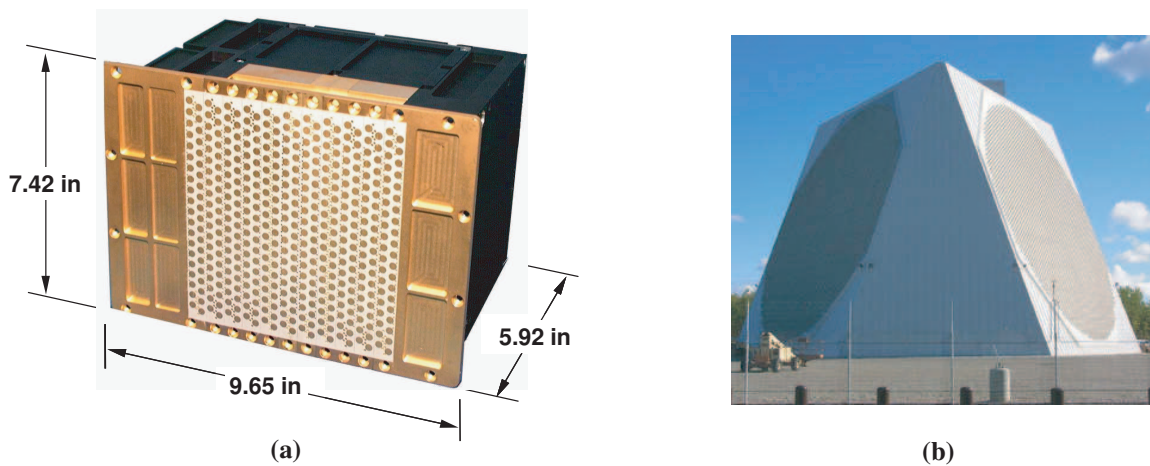


Figure 1.1 (a) NASA's High Data Rate User Phased Array Antenna (HRUPAA) for Ka-band satellite communications [5] and (b) Alaska District's 90-foot diameter phased array radar for missile warning and space surveillance [6].

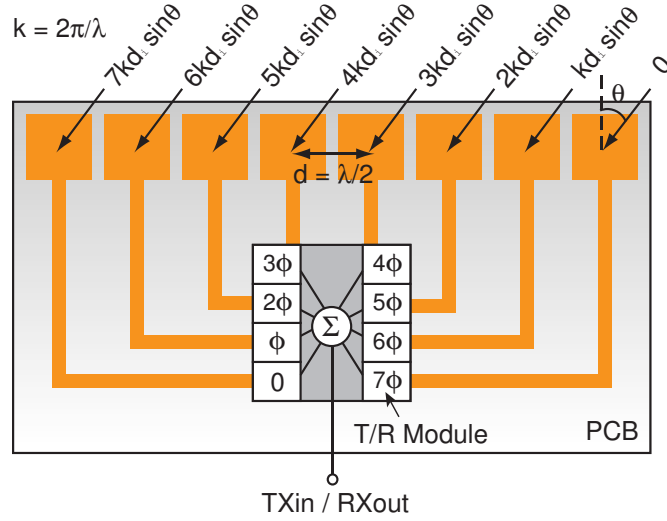


Figure 1.2 Phased array system with 8 antenna elements.

power combining concept.

In the receiver side of phased array systems, strong interferes from different directions can be placed in the nulls of a radiation pattern in order not to interfere with the desired signals [7]. Another fundamental merit of phased-arrays is to improve the effective signal-to-noise ratio (SNR) at the output of the receiver by $10\log(N)$ (dB) because the time-delayed signals from the antenna array add coherently while the noise generated by each receiver chain for the antenna elements adds incoherently, hence increasing a channel capacity [8]. For the transmitter side, phased array systems have higher spacial power efficiency and create less interference to nearby communication system.

To compensate for the time delay between the antenna elements, a phase shifter can be used instead of a variable time delay element for narrow-band applications. Any required time delay can be wrapped around every 360° of signal phase because the carried information changes relatively slowly in the case of narrow-band systems. In a linear array, the phase difference between adjacent antenna elements can be calculated as;

$$\phi_{\Delta} = 2\pi \frac{d \sin(\theta)}{\lambda}, \quad (1.1)$$

where λ is the wavelength, d is the spacing between the antenna elements, and θ is the angle of incidence. When the phase shifters have a progressive phase difference of ϕ , the phased array steers

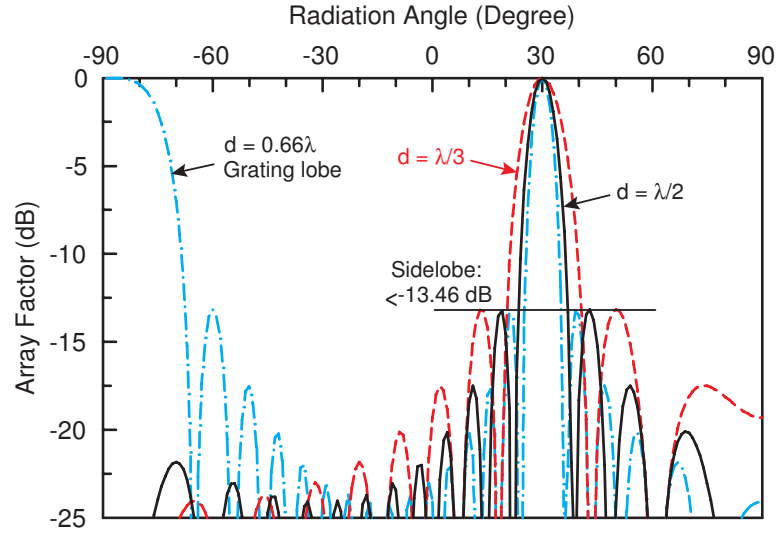


Figure 1.3 Normalized array factor of 16 element phased antenna array with uniform illumination and different antenna spacing when the phased array steers the antenna beam to $\theta = 30^\circ$.

the antenna beam to

$$\theta = \sin^{-1} \left(\frac{\lambda}{2\pi \cdot d} \phi \right). \quad (1.2)$$

Assuming far-field observations, the total field of the antenna array is equal to the field of a single antenna element multiplied by a factor which is widely referred to as the array factor (AF) [9].

The array factor of an N-element linear array is

$$AF = \frac{\sin \left(\frac{N}{2} \frac{2\pi}{\lambda} d \cos(\theta) + \phi \right)}{\sin \left(\frac{1}{2} \frac{2\pi}{\lambda} d \cos(\theta) + \phi \right)}. \quad (1.3)$$

Fig. 1.3 shows the normalized array factor (AF/N) of 16 element phased antenna array with three different antenna spacing when the phased array steers the antenna beam to $\theta = 30^\circ$. The spacing between the antennas is usually chosen to be close to $\lambda/2$ for a high antenna directivity and no grating lobes¹.

¹A lobe, other than the main lobe, produced by array antenna when the antenna spacing is sufficiently large to permit the in-phase addition of radiation fields in more than one direction.

1.2 Phased Array Architectures

To compensate for the time delay between the antenna elements, phase shifting in the RF domain for each array element (*All-RF* phased array architecture) has been dominant since they were developed. Recently, a phased array system based on IF phase shifting architecture [10] and LO phase shifting architecture [11, 12] were realized at 94 GHz and 77 GHz, respectively. Also, the signal for each antenna element can be processed in the digital domain without any phase-shifting method. Fig. 1.4 shows the block diagram of the four different phased array architectures.

The *All-RF* architecture is the most compact architecture among the phased array architectures since only a single mixer is required and the LO signal does not need to be distributed to each receiver path. The IF or LO phase shifting architectures have an advantage of elimination of the RF phase shifters which can be lossy at millimeter-wave frequencies. However, the IF or LO phase shifting architectures require an LO distribution network, and these result in a complex system and layout especially for large arrays with 64–1000 elements. Also, in satellite or defense applications, the required LO phase noise is very low (for example, < -155 dBc/Hz at 10 kHz offset for X-band radar systems and < -123 dBc/Hz at 1 MHz offset for 11-13 GHz direct broadcast satellite systems). This can only be achieved using an external oscillator such as a dielectric resonator oscillator and removes the advantage of integrated silicon-based oscillators.

Another important advantage of the *All-RF* architecture over the other architectures is that the output signal after the RF combiner has a high pattern directivity and can substantially reject an interferer before the following receiver units (Fig. 1.4(a)). This results in reduced linearity requirement for the mixer block and maximizes the value of the phased arrays as a spatial filter. In IF or LO phase shifting architectures, a mixer is connected to antenna with interferences from all directions due to a low pattern directivity, and therefore generates intermodulation products, which can propagate throughout the array. The high linearity requirement of the mixer in the IF and LO phase shifting architectures also applies to the digital beam forming architecture, and also, the analog/digital (A/D) converters need to have a large dynamic range to accommodate all the incoming signals without distortion. Also, the digital beam forming architecture requires the largest number of components including the A/D converters and its power consumption is high due to high speed digital parallel processing of the incoming signal. However, it is the only architecture which can

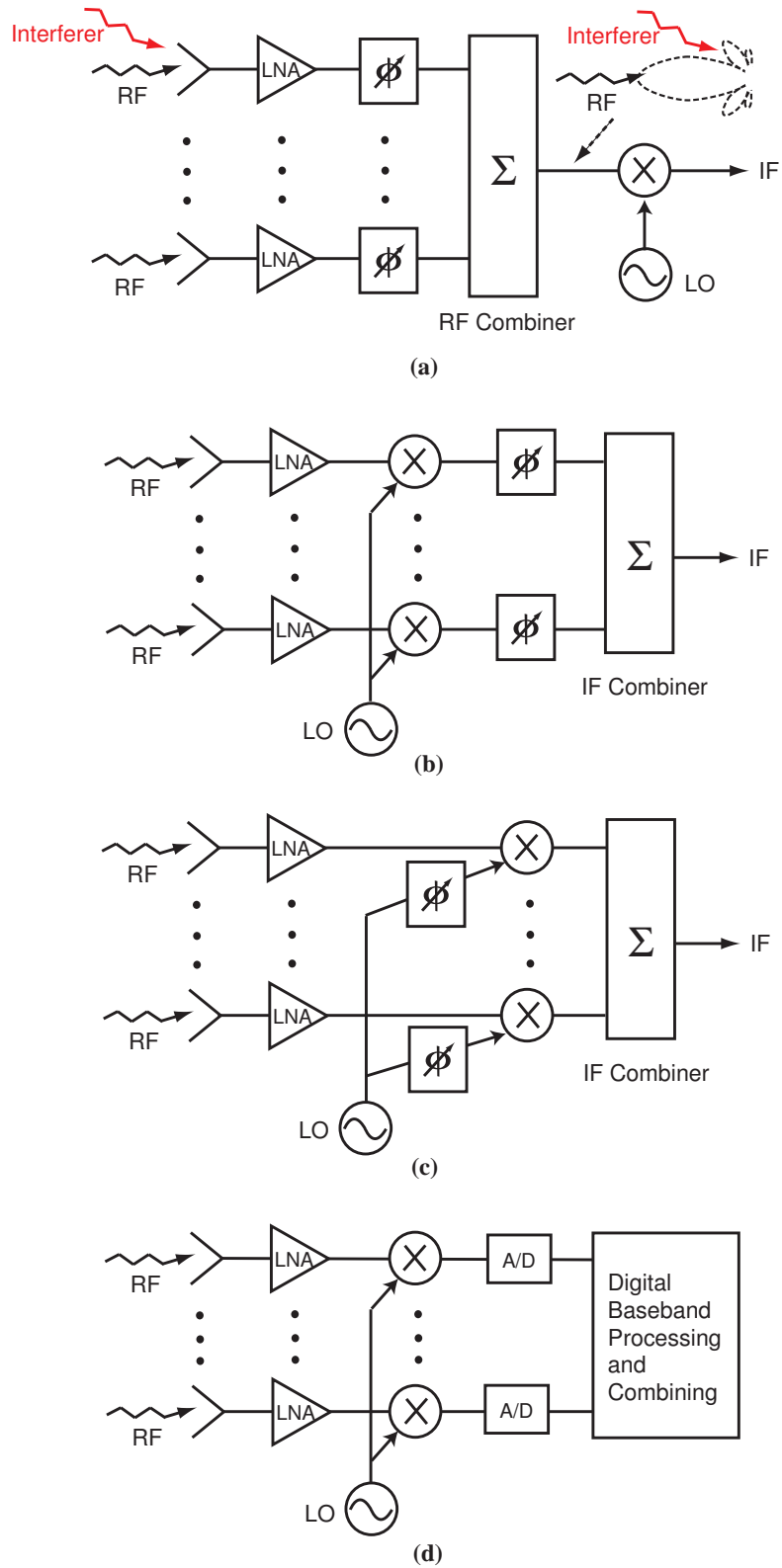


Figure 1.4 Phased array receiver architectures: (a) RF phase shifting, (b) IF phase shifting, (c) LO phase shifting, and (d) digital beam forming.

simultaneously synthesize a very large number of beams, and the number of beams is given only by the processing power in the digital beamformer.

1.3 RF Phase-Shifting Transmit/Receive Module

The performance of phased array systems is mainly driven by the performance of transmit/receive (T/R) modules. The T/R module for the *All-RF* phased array architecture includes low noise amplifier (LNA), phase shifter, variable gain amplifier (VGA) or attenuator, single-pole-double-throw (SPDT) switches and power amplifier (PA). The SPDT switches are required to switch between the transmit and receive modes. The VGA or variable attenuator can change the weight to tailor the beamwidth and sidelobe level and also to compensate for the gain variation of the phase shifter vs. phase state.

Fig. 1.5 shows several different T/R module block diagrams for the *All-RF* phased array architecture. Fig. 1.5(a) is a T/R module with two different transmitting and receiving paths. To reduce the module size, the phase shifter and variable attenuator in the transmitter and the receiver can be shared using SPDT switches (Fig. 1.5(b)). However, this system needs a high gain LNA to compensate for the loss of the consecutive phase shifter and variable attenuator. The high gain LNA requires high isolation SPDT switches to prevent an oscillation due to the LNA, SPDT switches and PA circular loop. Fig. 1.5(c) shares an amplifier as well as the phase shifter and variable attenuator, and therefore the high isolation SPDT switches are not required and the linearity requirement of the LNA can be relaxed.

The phase shifter is the most essential building block in the *All-RF* phased array system. The phase shifter can be either analog-type (continuous phase shift) or digital-type (step phase shift). The digital-type passive phase shifter has advantages of simple control circuits and immunity to noise in the control lines. Also, the digital-type phase shifter can be controlled without power consumption, and therefore it is preferable for a phased array system with a large number of antenna elements.

A 4-bit digital-type phase shifter with 22.5° phase resolution (a maximum phase error of $\pm 11.25^\circ$) is the most specified design for satellite communications and radar systems. This is because, with $\pm 11.25^\circ$ phase delay resolution, the phased arrays can scan the antenna beam almost

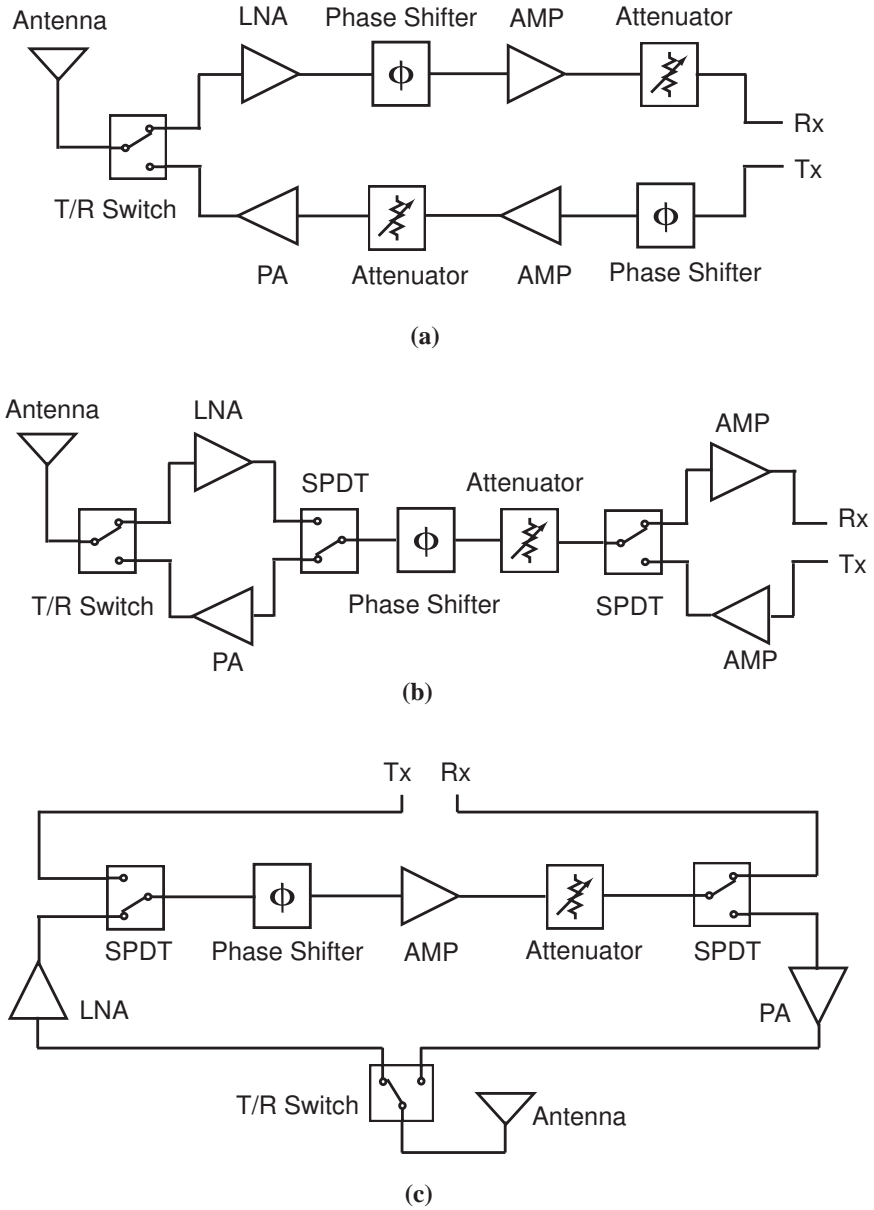


Figure 1.5 Various system architectures of transmitter/receiver modules.

continuously with a negligible decrease of array gain or increase in sidelobe levels. Fig. 1.6 presents the array factor of a linear uniformly excited 16-element phased array with an element-to-element spacing, $d = \lambda/2$ and scanning every 3° with 4-bit phase shifters. The required delay for each element is rounded to the nearest phase delay available in the 4-bit phase shifter. The loss at the scanning direction due to the 4-bit phase resolution is less than 0.1 dB at all continuous scan angles (maximum 0.33 dB loss with 3-bit phase resolution).

Fig. 1.7 shows array factors with two different amplitude weighting for 16-element array an-

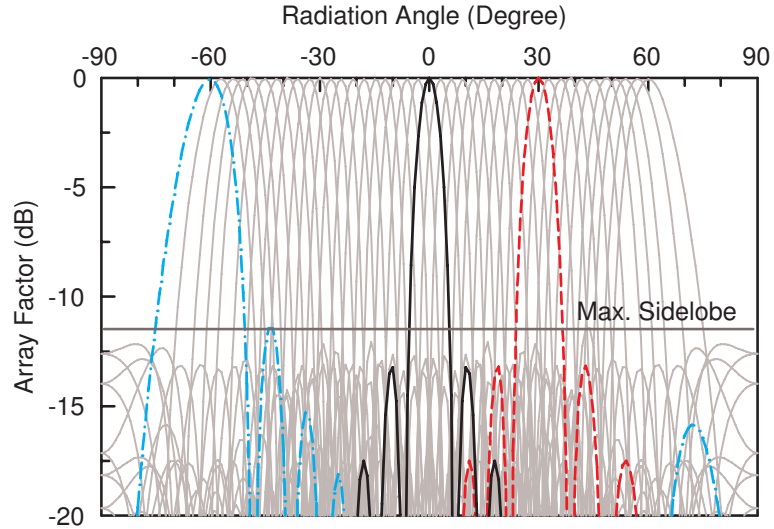


Figure 1.6 Array factor of a 16-element phased array scanning every 3° from -60° to 60° with 4-bit phase shifters ($d = \lambda/2$).

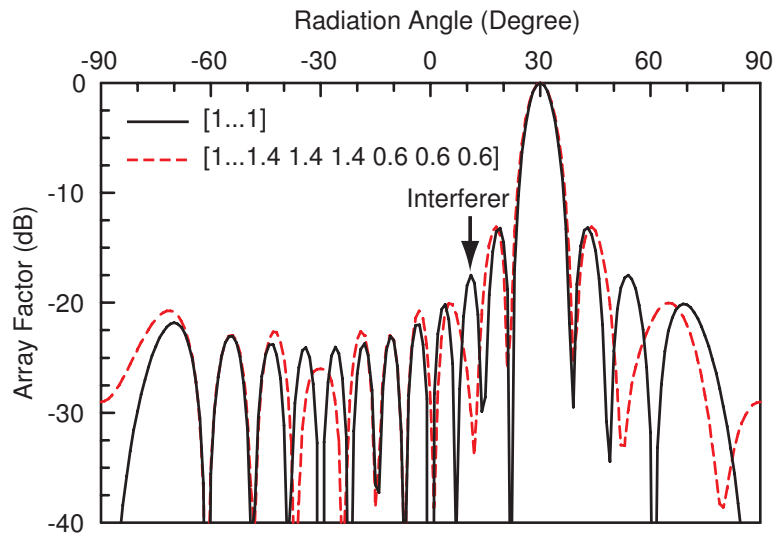


Figure 1.7 Normalized array factor of 16 element phased antenna array with different antenna weighting when the phased array steers the antenna beam to $\theta = 30^\circ$.

tennas using VGAs or variable attenuators. The solid line shows the array factor for a constantly weighted array, while the dashed line represents the array factor with amplitude weighting vector of $[1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1.4 \ 1.4 \ 1.4 \ 0.6 \ 0.6 \ 0.6]$. If a interferer comes from a angle of $\theta = 10^\circ$, amplitude weighting can change the null position and attenuate the interferer drastically. The null position can be more effectively controlled with phase shifting and amplitude weighting, together .

Table 1.1 Relative Performance Comparisons of Different Device Technologies [13] (Excellent: ++ ; Very Good: + ; Good: 0 ; Fair: - ; Poor: --).

Performance Matrix	SiGe HBT	Si BJT	Si CMOS	III-V MESFET	III-V HEMT
Frequency response	+	0	0	+	++
1/f and phase noise	++	+	-	--	--
Broadband noise	+	0	0	+	++
Output conductance	++	+	-	-	-
Transconductance/Area	++	++	--	--	-
CMOS integration	++	++	N/A	--	--
IC cost	0	0	++	-	--

1.4 SiGe BiCMOS Process

With recent developments in SiGe bipolar complementary metal oxide semiconductor (BiCMOS) technologies, it is possible to build Si-based millimeter-wave sub-systems on a single chip. The operation theory of silicon-germanium heterojunction bipolar transistor (SiGe HBT) was established by Kroemer in 1957 [14]. SiGe HBT technologies utilize bandgap engineering and show a dramatically improved performance comparing to a Si bipolar junction transistor (BJT). In SiGe BiCMOS processes, Ge is introduced into the base of the transistor, and bandgap of the base is smaller since the bandgap of Si and Ge are 1.12 eV and 0.66 eV, respectively. This enhances electron injection and produces a higher current gain. In addition, Ge composition is typically graded across the base and this generates an electric field, which accelerates the minority carriers and improves the frequency response of the transistor. Therefore, the SiGe BiCMOS technology provides good performance, and is compared in Table 1.1.

The most remarkable advantage of SiGe BiCMOS technologies over the III-V semiconductor based technologies is its high level of system integration and low cost of production. SiGe HBT technology also maintains strict compatibility with conventional Si CMOS manufacturing, and therefore digital circuits requiring CMOS transistors still can be integrated together. SiGe BiCMOS technologies take all the advantages of the Si IC manufacturing, such as high yield and low die cost, while provide comparable performance with III-V technology. Commercial SiGe process now exists in the leading semiconductor companies around the world, including: IBM, Hitachi,

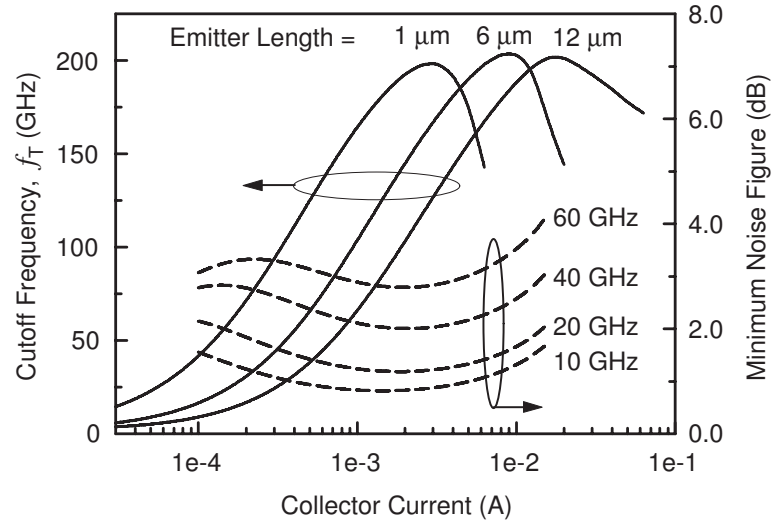


Figure 1.8 Simulated cutoff frequency (f_T) and noise figure minimum of a transistor with a emitter length of $12 \mu\text{m}$ versus collector current.

Conexant, Infineon, Philips, Lucent, Atmel, ST Microelectronics, TSMC...etc.

Fig. 1.8 shows the cutoff frequency (f_T) and the noise figure minimum of a $0.12 \mu\text{m}$ SiGe BiC-MOS process (IBM 8HP) [15]. The peak f_T of a SiGe HBT is about 200 GHz at a collector current density of $12 \text{ mA}/\mu\text{m}^2$, and the minimum noise figure (NF_{min}) of a common-emitter amplifier is about 1.8 dB at 35 GHz with a current density of $1.5 \text{ mA}/\mu\text{m}^2$. Hyper-abrupt junction diodes are also available and can be used as varactors (HAVAR) [16]. Metal-oxide-metal (MIM) capacitors and spiral inductor models are supported in the process design kit. However, their layout provided by the process design kit is not optimal for high density millimeter-wave circuits and these passive components should be designed using a commercial electromagnetic software (Sonnet²) using a full-wave simulation.

1.5 Objective and Contents of Thesis

Phased array systems have been widely used in satellite communication and defense applications. However due to their high cost and large size, their commercial applications have been very limited. The high cost is due to the discrete implementations of the transmit/receive (T/R) module and the whole phased array. Typically in these T/R modules, III-V front-end MMICs (GaAs and/or InP) were assembled together with silicon-based baseband and digital control back-end chipsets,

²Sonnet, ver. 10.53, Sonnet Software Inc., Syracuse, NY, 1986-2005.

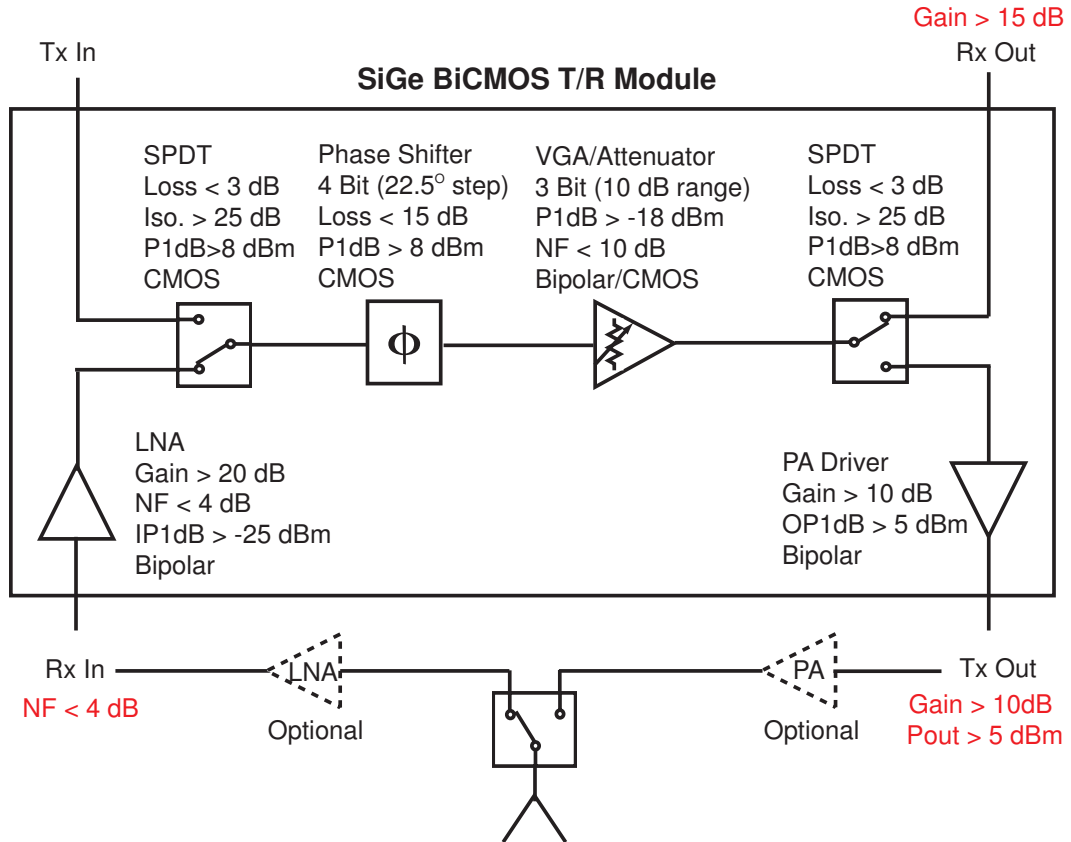


Figure 1.9 System block diagram of the Ka-band phased array T/R module.

resulting in relatively high cost and low integration density. [17–19]. Therefore, the integration of high capability RF blocks with baseband and digital processors on a silicon chip will drastically reduce the cost and size of phased-arrays. A SiGe BiCMOS process can be an excellent candidate for this purpose, and can provide high performance SiGe HBT for RF and analog processes and dense CMOS for digital circuit designs [20]. The SiGe BiCMOS process can enjoy all the advantages of the Si IC manufacturing, such as complexity, high yield and low cost, but also provides comparable performance with III-V technology.

Therefore, the objective of this thesis is to propose a solution to replace III-V components utilizing the SiGe BiCMOS technologies so as to reduce the III-V component count of the phased array system while maintaining high performance. The application areas are in low cost miniature phased-arrays for mobile satellite systems for high data-rate communications and defense systems such as radars and high bandwidth telecommunication links covering the Ka-band frequency range. Fig. 1.9 shows the system block diagram of the proposed Ka-band SiGe BiCMOS phased array T/R

modules with the performance specifications for the each circuit block. In the T/R module system diagram, the signal amplification components such as the LNA, VGA and PA driver amplifier are designed using SiGe HBT, while the phase shifter, SPDT switches and attenuator are based on CMOS transistors.

Chapter 2 covers the theory and design of the Ka-band LNA and VGA. A new design and optimization procedure for simultaneous noise and input power matching is presented considering the base-collector feedback capacitance. The design and implementation of a variable gain low noise amplifier (VG-LNA) with a low insertion phase imbalance is also presented. The low phase imbalance can be achieved using a current steering technique and a novel compensating resistor in the bias network.

Chapter 3 explains the phase shifter design and measurement, and the phase shifter is also integrated with the LNA and VGA for a phased array receiver front-end. The phase shifter is based on CMOS switched delay networks and have 22.5° phase resolution and $<4^\circ$ rms phase error at 35 GHz, and can handle 10 dBm of RF power (P_{1dB}). A differential phase shifter is also designed since the differential phase shifter is essential for high density integration and low on-chip coupling in a multiple-element T/R module.

In Chapter 4, the theory, design and measurement of a low-loss distributed CMOS step attenuator are presented. Twelve nMOS varistors are spaced $\lambda/16$ apart in a $50\text{-}\Omega$ synthetic t-line and control the attenuation. The electrical distance between the varistors is explored to minimize the size of the distributed attenuator, and a method to balance the insertion phase is presented.

Chapter 5 presents the theory and design of the SPDT switches for Ka-band applications. It is found that the substrate resistance (R_{sub}) network of CMOS transistors is a very important factor for millimeter-wave CMOS switch designs. For SPST switches, the shunt topology results in superior performance compared to series designs. However, the series switch isolation and power handling can be improved with the use of a high- R_{sub} design and parallel resonant networks. For the SPDT case, the high- R_{sub} deep n-well switch results in very small chip area and wide-band performances.

Chapter 6 shows the final Ka-band T/R module design and measurement. The SiGe BiCMOS Ka-band T/R module has excellent gain and phase control. The T/R module performance was predicted to within 1–2 dB using a concatenation of separate $50\ \Omega$ design blocks presented in the previous chapters.

Chapter 7 shows a silicon wafer-scale package for millimeter-wave integrated circuits or RF MEMS devices. The sealing technique (gold ring bonding) can result in un-wanted resonance modes. However, a gold-ring grounding technique is proposed to eliminate all package resonances or slot-line modes and improve the group delay flatness. The gold-ring grounding also improves the isolation between the input and output ports because the grounded gold-ring considerably reduces the leakage.

Chapter 8 is the conclusion and future work chapter. A single-chip T/R module design for a multi-element phased array system is proposed.

In Appendix, a new concept of a switchable balun is demonstrated at 5–6 GHz using a 0.13 μm CMOS process. CMOS transistors are placed at the center-taps of the balun for the switching operation. The integrated switchable balun occupies $250 \times 240 \mu\text{m}^2$, and can be used for compact low-power T/R applications with a single-ended antenna and differential low-noise and transmit amplifiers.

Chapter 2

Ka-Band SiGe Variable Gain Low Noise Amplifier

2.1 Introduction

Most communication systems including phased array systems require a low noise amplifier (LNA). The LNA decides the system noise figure and should provide enough gain to overcome the noise of subsequent stages. Recent development of SiGe HBTs allows LNA integration on a single chip for millimeter-wave sub-systems.

The phased array system requires amplitude control of the incoming signal and a variable gain amplifier (VGA) is often used for the signal amplitude control. The VGA can be combined with a low noise amplifier (LNA) to reduce power consumption and chip size for a phased array receiver. In phased array systems, a amplitude control range of about 10 dB, and a linear-in-magnitude gain variation are desirable for amplitude weighting. The VGA with digital control is preferred over an analog design since it simplifies the interface with digital circuits. The VGA must have a low insertion phase variation over the different gain states (phase imbalance) to avoid complex phase/amplitude calibration of the array [3].

In this chapter, a Ka-band single-ended LNA and a Ka-band differential variable gain LNA (VG-LNA) are presented. The LNA is based on a cascode amplifier using $0.12\ \mu\text{m}$ SiGe hetero-junction bipolar transistors (HBT). A new design procedure for simultaneous noise and input power matching is developed considering the collector-base feedback capacitance (C_{μ}). At 33–34 GHz, the single-ended LNA results in a measured gain of 23.5 dB, a return loss of <-20 dB and a noise figure of 2.9 dB. The input return loss is <-10 dB and the noise figure is 2.6–3.2 dB for the entire Ka-band frequency range. The LNA is $300 \times 300\ \mu\text{m}^2$, consuming 6 mA from 1.8 V supply (11 mW). The output 1 dB compression power is -6 dBm. To author's knowledge, these are state-of-the-art results and show the validity of the design technique. The VGA of differential VG-LNA

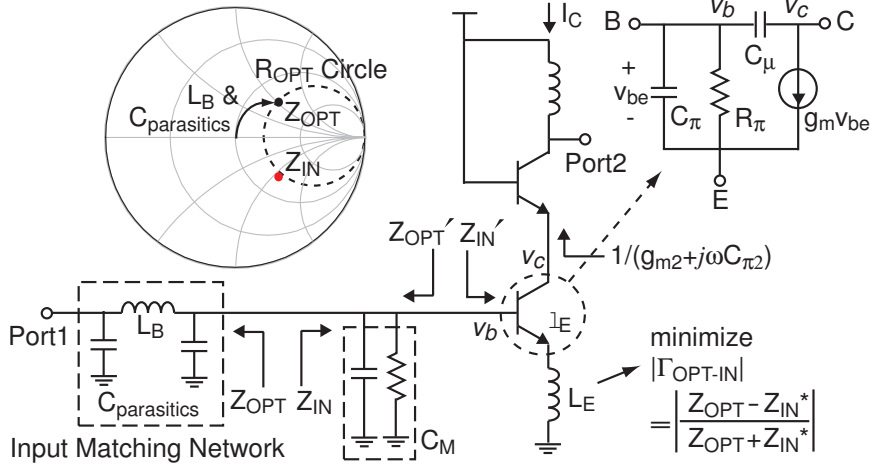


Figure 2.1 Cascode low noise amplifier with a Miller capacitance, C_M replacing C_μ at the base node. $Z_{IN}'=133-j57$ (Ω), $Z_{IN}=76-j45$ (Ω) and $1/j\omega C_M=167-j147$ (Ω) with $\ell_E=8$ μm , $I_C=2.5$ mA and $L_E=105$ pH.

is based on digital current steering technique to minimize the phase imbalance [21]. The measured VG-LNA gain at 32–34 GHz is 9–20 dB with 8 different linear-in-magnitude gain states, and with a noise figure of 3.4–4.3 dB. The measured rms phase imbalance is $<2.5^\circ$ at 26–40 GHz for all gain states and this is achieved using a novel compensating resistor in the bias network. The differential VG-LNA consumes 33 mW (13.5 mA, 2.5 V) and the input 1-dB gain compression point is -27 dBm. The chip size is 0.13 mm² without pads.

2.2 Low Noise Amplifier Design Theory

The common-emitter/source LNA with inductive degeneration has been one of the most preferable LNA topologies [22–25]. The degeneration inductor increases not only the linearity of an amplifier, but also the input resistance for impedance matching. The cascode configuration is also frequently used to increase the reverse isolation and results in less design complexity.

Voinigescu et al. developed a general LNA design procedure using a scalable device model for simultaneous noise and (input) power matching [23] without a constrained power consumption [22, 24]. In this procedure, the transistor size (emitter length, ℓ_E with a given emitter width) is chosen for the optimal noise resistance (R_{OPT}) to be 50 Ω at the optimal current density. Then, the degeneration inductor (L_E) increases the input resistance (R_{IN}) to 50 Ω , and the base inductor (L_B) matches the input reactance (X_{IN}). In this procedure, there are three assumptions; 1) the noise figure

minimum, NF_{min} is not a function of ℓ_E at the optimal current density, 2) L_E does not affect R_{OPT} , and only changes R_{IN} , 3) the magnitudes of the optimal noise reactance and the input reactance are always the same ($X_{OPT} = -X_{IN}$). However, these assumptions do not hold well at millimeter-wave frequencies and this is mostly due to the collector-base feedback capacitance, C_μ . Also, it will be shown that it is better to choose R_{OPT} larger than 50Ω so as to match the input impedance with a single inductor, L_B .

For $R_\pi \gg 1/\omega C_\pi$ or $f \gg f_T/\beta_o$ (cutoff frequency/DC current gain), the input impedance of a degenerated common emitter amplifier, shown in Fig. 2.1, is usually written as (neglecting C_μ),

$$Z_{IN}' = R_{IN}' + jX_{IN}' = \frac{g_m L_E}{C_\pi} + j \left(\omega L_E - \frac{1}{\omega C_\pi} \right). \quad (2.1)$$

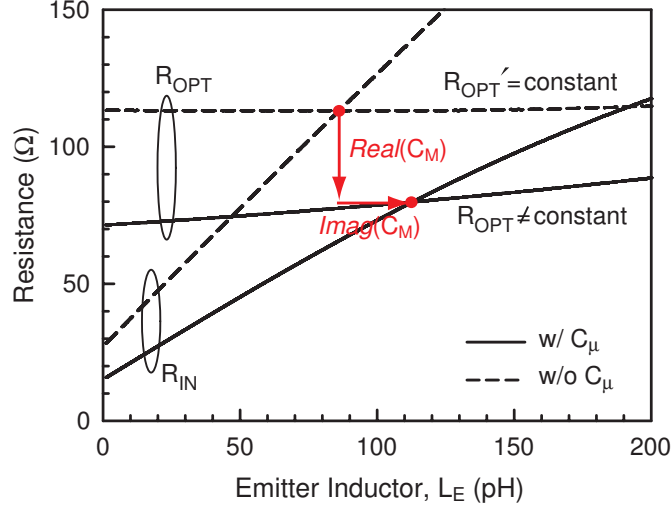
From the series-series feedback theory, one can prove that the emitter inductor, L_E does not affect the optimal source resistance (R_{OPT}') and only affects the optimal source reactance (X_{OPT}') resulting in $X_{OPT}' = -X_{IN}'$ [26]. However, the input impedance (Z_{IN}) and the optimal source impedance (Z_{OPT}) for a millimeter-wave amplifier substantially change when C_μ is considered.

Figure 2.2 clearly shows the effect of C_μ at 35 GHz. The amplifier is biased at its optimal current density for the lowest NF_{min} . Without C_μ , R_{OPT}' is constant and $X_{OPT}' = -X_{IN}'$ for all L_E values. However, these conditions do not hold if C_μ is considered. R_{OPT} changes from 72Ω to 89Ω (Fig. 2.2(a)), and the input reactance, X_{IN} becomes more capacitive rather than inductive (Fig. 2.2(b)), as L_E increases from 0 pH to 200 pH. The C_μ effect can be explained with a shunt capacitance at the base node, C_M , using the Miller-effect theory.

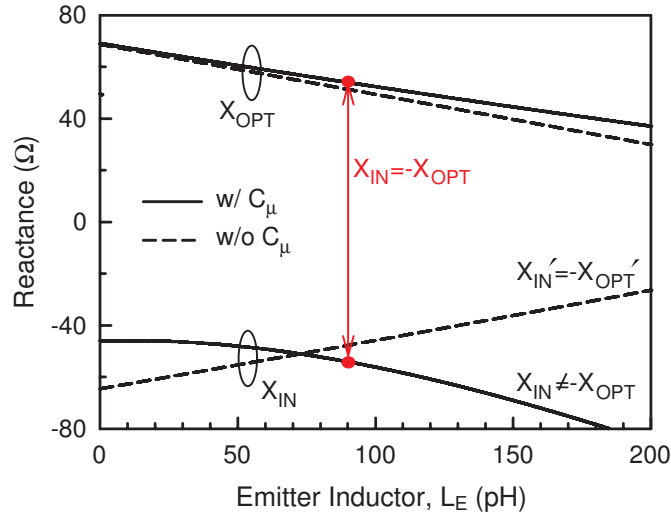
The C_μ of a cascode amplifier can be replaced with C_M as,

$$\begin{aligned} v_c/v_b &= \frac{-g_m v_{be}/(g_{m2} + j\omega C_{\pi 2})}{v_{be} + (j\omega C_\pi \cdot v_{be} + g_m v_{be}) \cdot j\omega L_E} \\ &\approx -1/(1 + j\omega g_m L_E) \end{aligned} \quad (2.2)$$

$$C_M = (1 - v_c/v_b) C_\mu \approx \frac{2 + j\omega g_m L_E}{1 + j\omega g_m L_E} C_\mu \quad (2.3)$$



(a)



(b)

Figure 2.2 Simulated input and optimal noise (a) resistance and (b) reactance with and without C_μ versus L_E , when $\ell_E=8 \mu\text{m}$ and $I_C=2.5 \text{ mA}$. For the simulation without the effect of C_μ , an inductor is connected between the base and collector to resonate out C_μ .

$$j\omega C_M = \frac{\omega^2 g_m L_E C_\mu}{1 + (\omega g_m L_E)^2} + j\omega C_\mu \cdot \frac{2 + (\omega g_m L_E)^2}{1 + (\omega g_m L_E)^2}. \quad (2.4)$$

From the imaginary part of C_M (or the real part of $j\omega C_M$), it is found that L_E and C_μ generate a *noiseless* shunt conductance value, $\omega^2 g_m L_E C_\mu / \{1 + (\omega g_m L_E)^2\}$. This is congruent with the *noiseless* series resistance, $g_m L_E / C_\pi$ in (2.1), due to L_E and C_π . In the case of $L_E=105 \text{ pH}$, $\ell_E=8 \mu\text{m}$ and a collector current (I_C) of 2.5 mA, the impedance $1/j\omega C_M$ is $167 - j147 \text{ } (\Omega)$ at 35 GHz. Even though L_E always increases X_{IN}' in (2.1), L_E with C_μ can eventually decrease X_{IN} since L_E increases

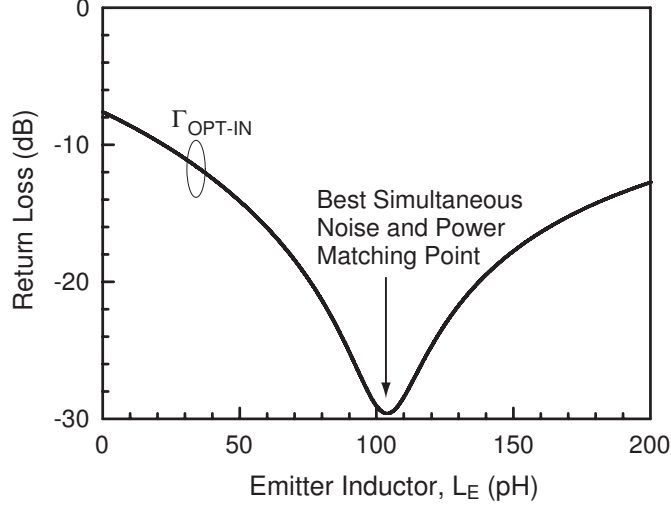


Figure 2.3 Simulated Γ_{OPT-IN} of a cascode amplifier versus L_E , when $\ell_E=8 \mu\text{m}$ and $I_C=2.5 \text{ mA}$.

R_{IN}' and C_M transforms R_{IN}' to $-X_{IN}$.

If C_M is purely capacitive and $Z_{OPT}'=Z_{IN}'^*$ for a specific L_E value, then $Z_{OPT}=Z_{IN}^*$ at the same L_E because C_M can be considered as a part of the lossless input matching network. This means that the L_E values for $R_{OPT}=R_{IN}$ and $X_{OPT}=-X_{IN}$ can be the same only if C_M is purely capacitive. The effects of the real and imaginary parts of C_M can be conceptually illustrated with arrows in Fig. 2.2(a). The resistance shift from point A ($R_{OPT}'=R_{IN}'$) to point B ($R_{OPT}=R_{IN}$) is due to the real part (susceptance) of C_M , and L_E value shift is due to the imaginary part (conductance) of C_M . With C_M composed of real and imaginary values, the L_E needed for $R_{OPT}=R_{IN}$ is different than the L_E needed for $X_{OPT}=-X_{IN}$. Therefore, the L_E corresponding for $R_{OPT}=R_{IN}=50 \Omega$ is not the optimal value anymore for simultaneous noise and power matching since $X_{OPT} \neq -X_{IN}$ at this L_E value. However, the conductance of C_M is noiseless and L_E does not change NF_{min} , and therefore the L_E value for the best simultaneous noise and power matching can be chosen to minimize the reflection coefficient (Fig. 2.3),

$$|\Gamma_{OPT-IN}| = \left| \frac{Z_{OPT} - Z_{IN}^*}{Z_{OPT} + Z_{IN}^*} \right|. \quad (2.5)$$

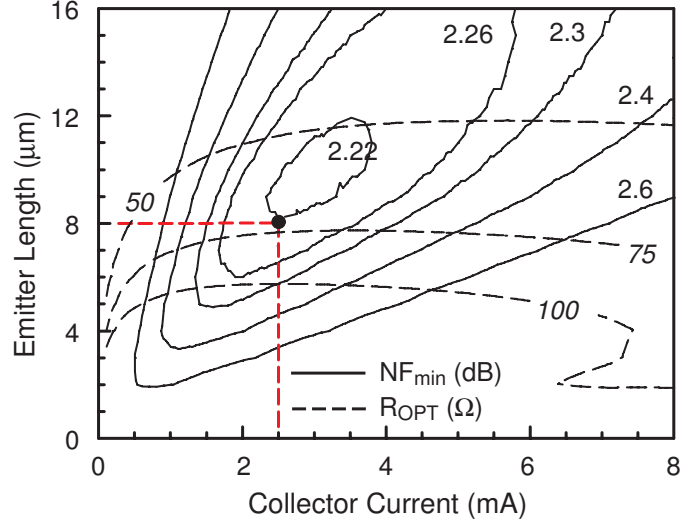


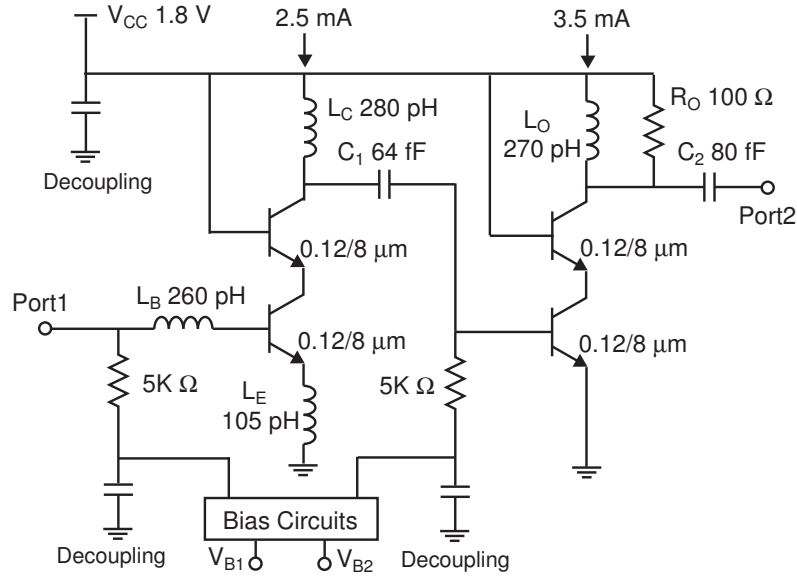
Figure 2.4 Simulated minimum noise figure and optimal noise resistance contour as a function of the emitter length and collector current when $L_E=0$.

2.3 Ka-Band SiGe Low Noise Amplifier

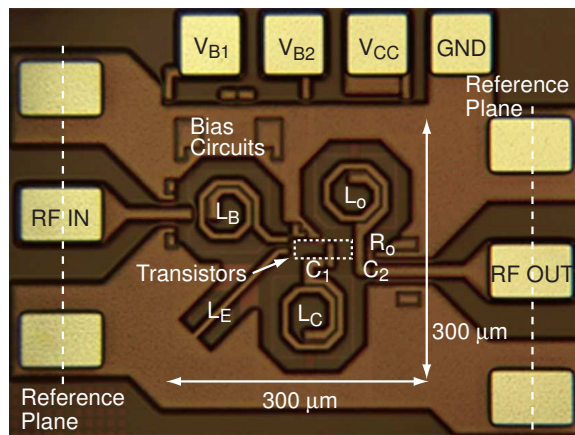
2.3.1 Circuit Design

The LNA is designed using IBM 0.12 μm SiGe BiCMOS process (8HP) with a peak f_T of 200 GHz. The optimal device size and current density are obtained using NF_{min} contours as a function of ℓ_E and I_C [27]. Fig. 2.4 shows the NF_{min} contours at 35 GHz together with R_{OPT} contours when $L_E=0$. The optimal current density is almost constant, but its NF_{min} changes with ℓ_E . The designed LNA has $\ell_E=8 \mu\text{m}$ and $I_C=2.5 \text{ mA}$. The ℓ_E is chosen where $R_{OPT}>50 \Omega$ (also considering the R_{OPT} increase due to L_E), in order to match Z_{OPT} using a single inductor (L_B) because the parasitic capacitances of L_B are not negligible at 35 GHz. The Smith chart in Fig. 2.1 shows the effect of the inductor parasitic capacitances and the matching condition. Fig. 2.4 can be used to trade off the power consumption, noise figure and R_{OPT} (for the input matching network). Any combination of ℓ_E and I_C can be chosen for a noise and power matched LNA as long as Γ_{OPT-IN} in (2.5) is minimized with L_E , and Z_{OPT} is matched using an input matching network.

Figure 2.5 shows the designed two stage LNA. A thin line inductor, $L_E=105 \text{ pH}$, is selected to minimize Γ_{OPT-IN} (Fig. 2.3). A spiral inductor, $L_B=260 \text{ pH}$ and its parasitic capacitance transform the Port1 impedance (50Ω) to $Z_{OPT} (\approx Z_{IN}^*)$. The second amplifier stage is a duplicate of the first stage without L_E for layout simplicity, and is biased at $I_C=3.5 \text{ mA}$ to get an overall gain of 25 dB.



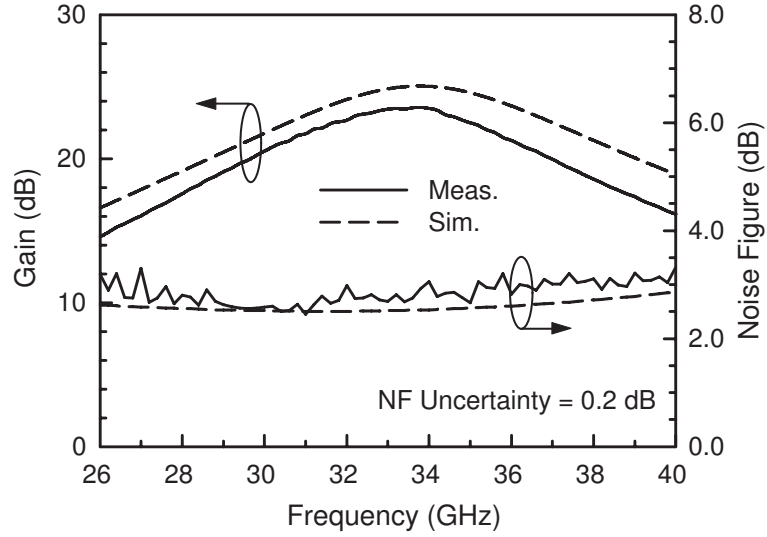
(a)



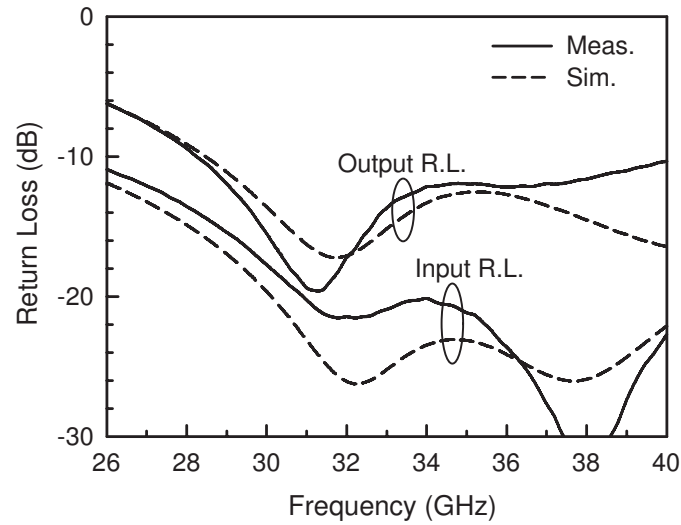
(b)

Figure 2.5 (a) Schematic and (b) photograph of the Ka-band LNA.

The interstage matching is composed of L_C and C_1 , and L_O , R_O and C_2 match the second stage output impedance to 50Ω . The output resistance, R_O increases the matching bandwidth by reducing the impedance transformation ratio. All passive components such as inductors, interconnects, and capacitors are simulated together using a commercial electromagnetic software (Sonnet). The RF pads and their tapered transitions are designed to provide 50Ω input and output impedances. The simulated quality factor of the planar inductors at 35 GHz is 12–15 for 200–300 pH. The total LNA chip area is less than 0.33 mm^2 and 0.1 mm^2 with and without pads, respectively.



(a)



(b)

Figure 2.6 Measured and simulated (a) gain and noise figure, and (b) input and output return loss.

2.3.2 Measured Results

The LNA S-parameters are measured on-chip with an Agilent E8364B network analyzer using SOLT calibration to the probe tips. The LNA draws 6 mA from 1.8 V supply voltage and the power consumption is 11 mW. The measured gain is 23.5 dB at 34 GHz and >15 dB for the Ka-band frequency range (Fig. 2.6(a)). As shown in Fig. 2.6(b), the measured input return loss is <-20 dB around the design frequency and <-10 dB over the entire Ka-band frequency range.

The noise figure of the LNA is measured using an Agilent 346CK01 noise source and a noise

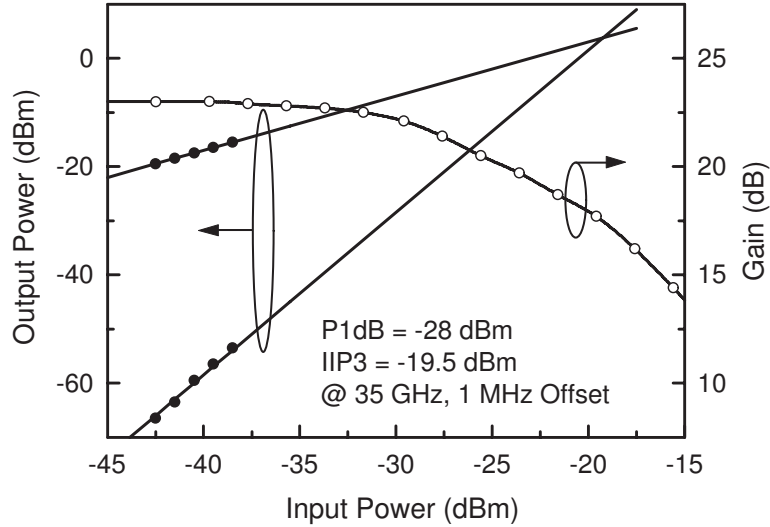


Figure 2.7 Measured power handling capability.

figure measurement personality of an Agilent E4448A spectrum analyzer. Two Ka-band preamplifiers are used in front of the spectrum analyzer and result in 0.2 dB noise figure uncertainty. As shown in Fig. 2.6(a), the measured noise figure is 2.6–3.2 dB at Ka-band and agree very well with simulation.

The measured 1 dB gain compression point (P_{1dB}) at 35 GHz is -28 dBm and -6 dBm for the input and output ports, respectively (Fig. 2.7). The third-order intermodulation products with a offset frequency of 1 MHz is also measured and the extrapolated intermodulation intercept point ($IP3$) is -19.5 dBm and $+4$ dBm at the input and output ports.

2.4 Variable Gain Amplifier Design Theory

Even though the amplifier gain variation can be achieved using various methods, there are three basic VGA types which are not based on a variable attenuation stage (Fig. 2.8). A bias-controlled VGA, where the bias current or collector-emitter voltage are controlled to change the transconductance (g_m), is quite common for RF applications (Fig. 2.8(a)) [28]. The feedback factor can also control the gain of a amplifier (Fig. 2.8(b)) [29]. The input impedance for these VGA topologies depends on the gain level, especially at Ka-band frequencies. Therefore, the insertion phase changes significantly depending on the VGA gain, and results in a high phase imbalance.

Fig. 2.8(c) shows a current splitting VGA topology [30, 31]. The bias current of the input tran-

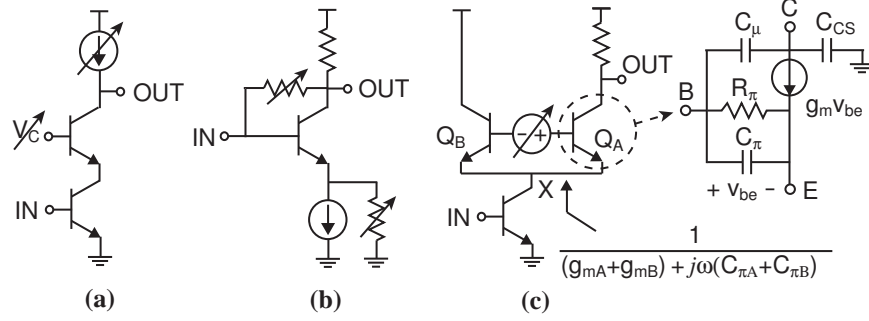


Figure 2.8 Basic types of VGA: (a) bias control, (b) feedback control, and (c) current splitting.

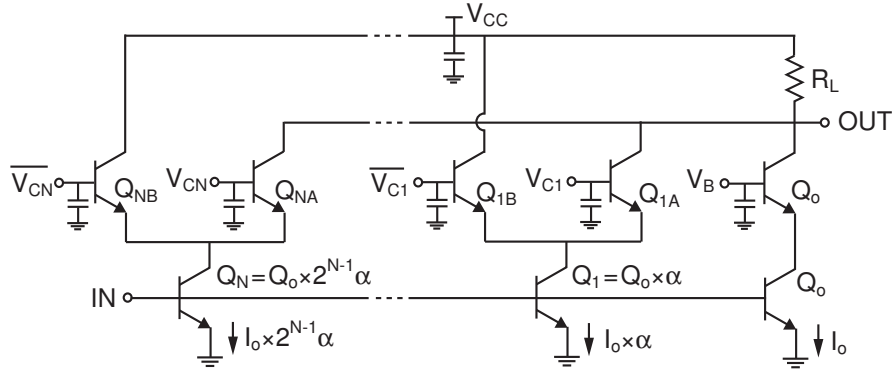


Figure 2.9 Current steering linear-in-magnitude VGA with digital controls.

sistor can be split into two transistors depending on the control voltage, and a variable gain can be achieved. This topology has a constant bias current for the input transistor, and results in a constant input impedance. The bias current variation for the current splitting stage changes the impedance looking into node X , $1/(g_m + j\omega C_\pi)$. However, this does not have much affect on the insertion phase since $g_m \gg j\omega C_\pi$. The output capacitance, $C_\mu + C_{CS}$ (C_{CS} =capacitance between collector and substrate), slightly varies due to the bias voltage variation at the base-collector junction. This effect can be compensated using a resistor as discussed in Section 2.5.1.

Fig. 2.9 presents the digital version of the current splitting VGA. The gain variation is achieved by completely steering the bias current of the input transistor (Q_n , $n = 1 \dots N$) to two transistors (Q_{nA} and Q_{nB}). When the control voltage V_{Cn} is high, the Q_n bias current is steered through Q_{nA} and the base signal of Q_n is amplified to the output. When V_{Cn} is low, the Q_n bias current is steered toward Q_{nB} without amplifying the signal. The transistor sizes of N current steering amplifiers are binary scaled for N -bit operation, and therefore the bias current and g_m are also scaled in the same way. The minimum gain of the VGA is defined by the cascode transistor, Q_o , which is α times smaller

than Q_1 . The VGA voltage gain can be written as:

$$A_v = -g_{m\circ}R_L(1 + \alpha \cdot b_1 + 2\alpha \cdot b_2 + \dots + 2^{N-1}\alpha \cdot b_N) \quad (2.6)$$

where $g_{m\circ}$ is g_m of Q_\circ , and $\{b_1 b_2 \dots b_N\}$ is the binary word for the control voltage (V_{Cn}). Therefore, the maximum gain variation is $20\log\{1 + \alpha(2^N - 1)\}$ (dB).

2.5 Differential Variable Gain Low Noise Amplifier

2.5.1 Circuit Design

A Ka-band differential 3-bit VG-LNA is designed using IBM 0.12 μm SiGe BiCMOS process with a peak f_T of 200 GHz (Fig. 2.10 and Table 2.1). A LNA stage proceeds VGA stage for the low noise figure for all the gain states. The LNA is an inductively degenerated cascode amplifier. The input impedance is matched with L_B and L_E for simultaneous input optimum noise and power matching [23]. The transistor has a emitter size of $0.12 \times 8 \mu\text{m}^2$ and is biased at 1.5 mA close to the optimal current density for the minimum noise figure.

The VGA stage is implemented to achieve a maximum gain variation of ~ 11 dB, resulting in $\alpha = 0.35$. To minimize the current consumption, the smallest transistor Q_1 is selected first to have a small emitter length (ℓ_E) of 0.56 μm . The ℓ_E of Q_\circ , Q_2 , and Q_3 are then scaled, while the emitter width (0.12 μm) is fixed. Since the g_m of the input transistor does not exactly scale with ℓ_E , the ℓ_E ratio between the transistors is slightly modified for accurate linear-in-magnitude gain control. The VGA is biased at a current density for maximum f_T , resulting in a total bias current of 10.5 mA.

The VGA phase imbalance is low by virtue of the constant bias current of the input transistor. However, the insertion phase still varies for each bit since the output capacitance ($C_\mu + C_{CS}$) changes depending on the gain state. The capacitance change is more severe for the larger transistor (the higher order bit). When V_{C3} is switched to low, C_μ decreases due to the increased reverse-bias voltage of the base-collector junction and the VGA insertion phase increases. This phase imbalance can be compensated by using a resistor R_Φ (130 Ω) in the Q_{3B} control line. R_Φ increases the input

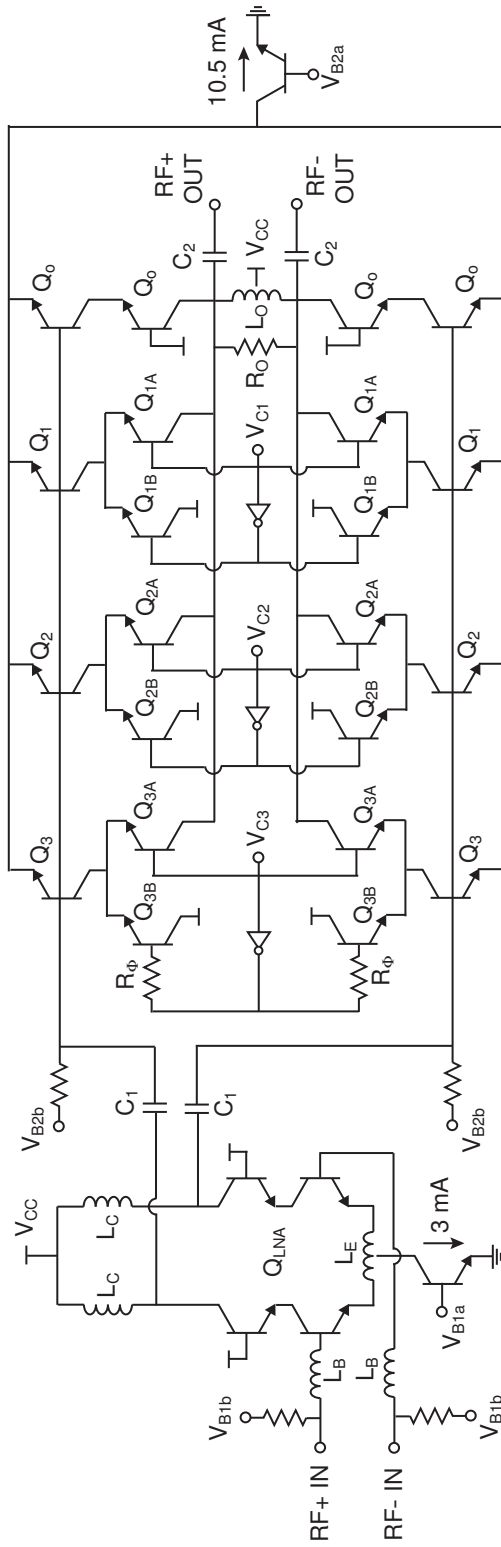


Figure 2.10 Schematic of the designed Ka-band differential VG-LNA.

Table 2.1 Summary of the VG-LNA Design Values.

HBT	Emitter Length	L_B	300 pH
		L_E	220 pH
Q_0	1.5 μm	L_C	310 pH
Q_1	0.56 μm	L_O	460 pH
Q_2	1.0 μm	C_1	90 fF
Q_3	1.9 μm	C_2	110 fF
Q_{LNA}	8.0 μm	R_O	180 Ω
V_{CC}	2.5 V	R_Φ	130 Ω

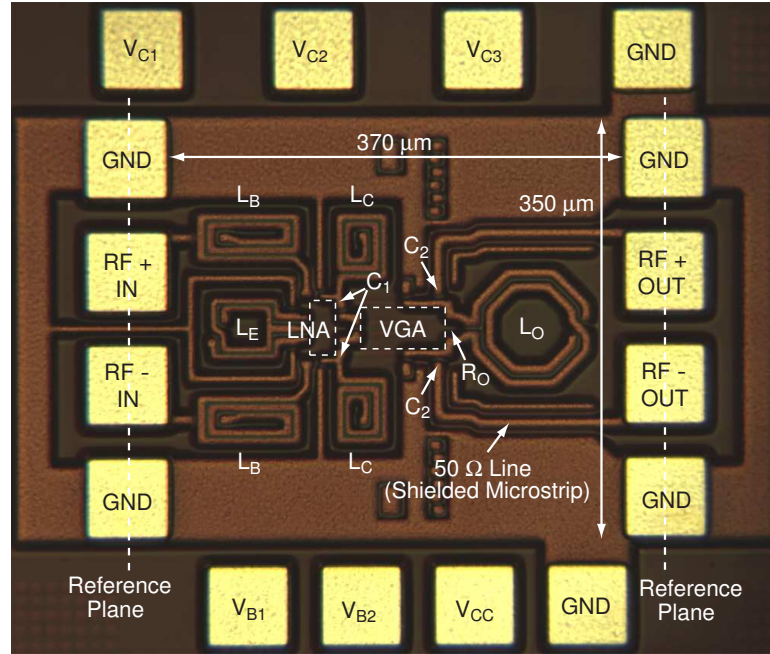


Figure 2.11 Photograph of the designed Ka-band differential VG-LNA.

impedance of Q_{3B} to

$$\frac{j\omega C_{\pi B} R_\Phi + 1}{g_{mB} + j\omega C_{\pi B}}, \quad (2.7)$$

and therefore the magnitude of the Q_3 voltage gain increases. This results in an increase of the Q_3 input capacitance due to the Miller effect, and a decrease in the VGA insertion phase. As a result, the decrease of C_μ at the output is compensated by increasing the effective input capacitance of Q_3 .

Fig. 2.11 shows a photograph of the VG-LNA. The output of the VG-LNA is matched to a differential 100 Ω load using L_O and C_2 . L_C and C_1 are used for interstage matching between the

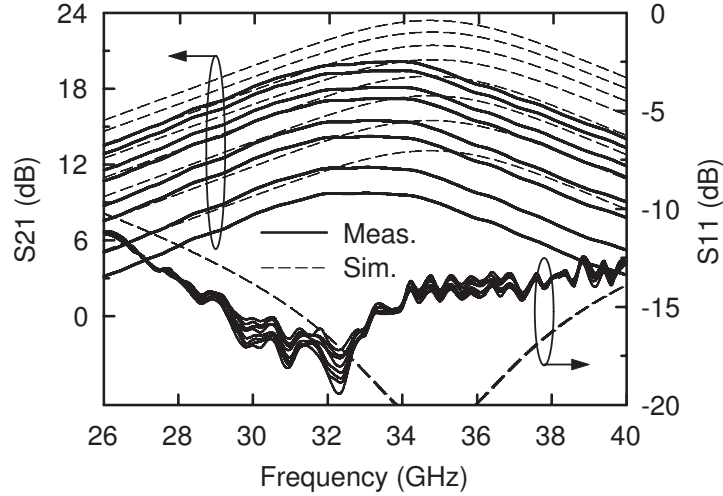


Figure 2.12 Measured and simulated gain and input return loss of the 8 different gain states.

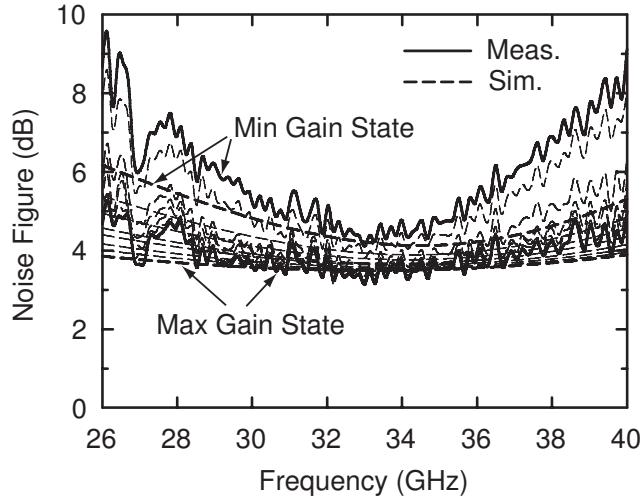


Figure 2.13 Measured and simulated noise figures of the 8 different gain states.

LNA and VGA stages. All passive components such as inductors, interconnects, and capacitors are simulated using a commercial electromagnetic software (Sonnet). The total VG-LNA chip area is $350 \times 370 \mu\text{m}^2$ (0.13 mm^2) without pads.

2.5.2 Measured Results

The differential VG-LNA was measured on-chip using waveguide magic-T baluns for differential to single-ended conversion. The measurement system is calibrated using a differential calibration substrate (Cascade ISS126-109) and the measured results are referenced to the input and

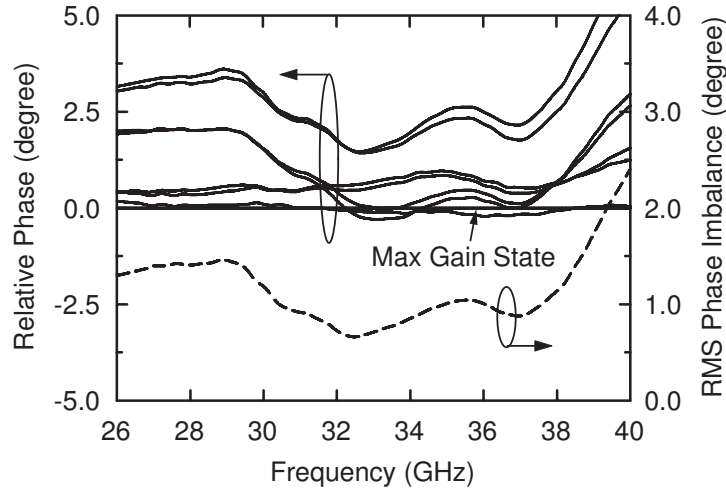


Figure 2.14 Measured relative insertion phase and rms phase imbalance for all gain states.

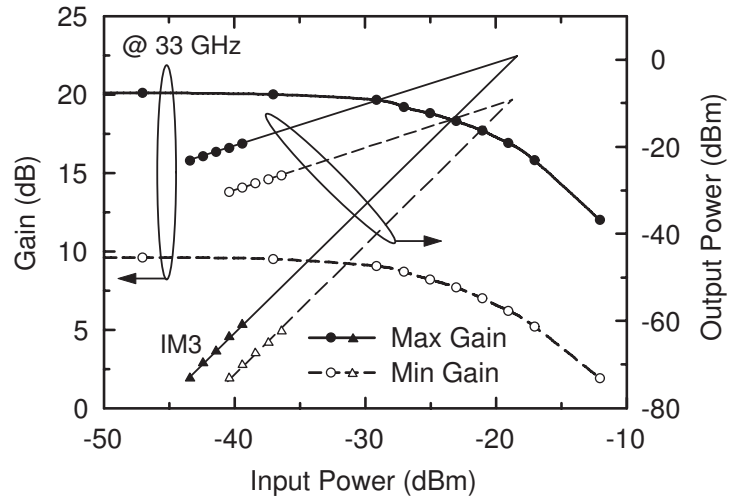


Figure 2.15 Measured output power and gain versus the input power.

output G-S-S-G pads. The measured VG-LNA has a linear-in-magnitude gain control between 20 and 9 dB at 32–34 GHz (Fig. 2.12). At 33 GHz, the 8 different gains are 9.9, 9.1, 7.9, 7.1, 5.9, 5.1, 3.8, and 3.0 in magnitude, resulting in a gain step of 1.0 ± 0.2 and a slightly lower gain step for the least significant bit. The measured center frequency shifted by 1–2 GHz compared to simulations due to un-accounted parasitic capacitances and transistor model/process variations. The measured S_{11} and S_{22} are less than -11 dB and -15 dB for the 8 different gain states, respectively. Even though the output capacitance ($C_{\mu} + C_{CS}$) depends on the gain states, the S_{22} is always well matched since R_o dominates the output impedance.

The noise figure was measured using an Agilent 346CK01 noise source and an E4448A spectrum analyzer. The off-chip balun and G-S-S-G probe loss is subtracted from the measurement. The measured noise figure is 3.4–4.3 dB for the maximum–minimum gain state at 32–34 GHz (Fig. 2.13). The noise figure is slightly worse for the low gain state because the VG-LNA gain is low but the VGA noise current is constant. Fig. 2.14 shows the measured insertion phase of the VG-LNA relative to the maximum gain state, and the rms phase imbalance is $<2.5^\circ$ at 26–40 GHz.

The input 1-dB gain compression point is measured at 33 GHz, resulting in -27 dBm for all the gain states (Fig. 2.15). The third-order intermodulation product with an offset frequency of 1 MHz results in an input intermodulation intercept point of -19 dBm. The input power handling capability of the VG-LNA does not depend on the gain state because the linearity of the VGA stage does not change due to the constant bias current.

2.6 Summary

A Ka-band cascode LNA is implemented using a $0.12\ \mu\text{m}$ SiGe BiCMOS process. A new design and optimization procedure is presented considering the base-collector feedback capacitance. The proposed design procedure results in both a wide band matching (<-10 dB) and a record noise figure (2.6–3.2 dB) over the entire Ka-band frequency range. A differential Ka-band VG-LNA (9–20 dB gain) is implemented using a $0.12\ \mu\text{m}$ SiGe BiCMOS process for phased array systems. A rms phase imbalance of $<2.5^\circ$ is achieved using a digital current steering technique and a novel compensation resistor. To author’s knowledge, this chapter represents the first VG-LNA at Ka-band frequencies with excellent phase balance and noise figure, and the VG-LNA is suitable for Ka-band phased array applications.

Chapter 3

Ka-Band CMOS Phase Shifter and Phased Array Receiver Front-Ends

3.1 Introduction

Phased array systems have been used since the 1950's to achieve electronic beam control and fast beam scanning [3, 4]. They require a receiver front-end per antenna element which includes a low noise amplifier (LNA), a phase shifter, and a variable gain amplifier (VGA). These have been implemented with GaAs- or InP-based discrete modules especially at millimeter-wave frequencies, resulting in relatively high cost and low integration density. However, with recent developments in silicon technologies, it is possible to build Si-based phased array on a single chip [8, 32], and the GaAs component count can be drastically reduced.

Fig. 3.1 shows the block diagram of a phased array receiver front-end. The electronic phase shifters vary the insertion phase of the incoming signal and this results in the antenna beam scanning. The VGA can weight the RF signals to tailor the beamwidth and sidelobe level and also compensate for the gain variation of the phase shifter. As explained in Chapter 1, the RF phase-

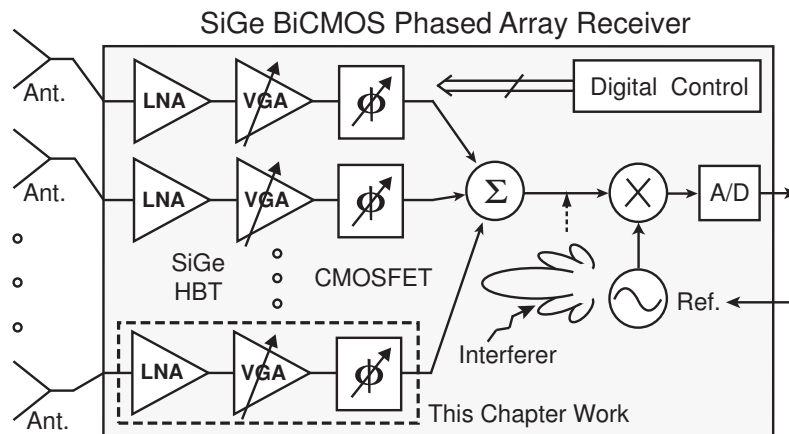


Figure 3.1 Block diagram of a SiGe BiCMOS receiver front-end for an RF phase-shifting phased array system.

shifting architecture has been used since the 1950's and has several advantages over the LO or IF phase-shifting architecture [8]: 1) The possible interferer is canceled before the mixer/receiver, and this greatly relaxes the mixer linearity and overall dynamic range requirement. 2) There is no need to distribute a local oscillator signal over the chip, which is important for large element systems. 3) The power consumption is reduced since only one mixer is needed for the entire array.

The phase shifter is the most essential building block in the phased array system. There are four basic types of phase shifters [33]: switched delay [34–36] loaded reflection [37, 38] loaded line [39, 40] and vector modulation [30, 41], and all can be designed using either distributed or lumped elements, but the lumped element design is preferable on silicon for high integration density. The phase shifter also can be either analog-type (continuous phase shift) or digital-type (step phase shift). The digital-type passive phase shifter has advantages of simple control circuits and immunity to noise in the control lines.

In this chapter, CMOS single-ended and differential versions of 4-bit switched-delay type phase shifter are presented for a 35-GHz phased array receiver system (Fig. 3.1). The phase shifters are based on CMOS switched delay networks and have 22.5° phase resolution and $<4^\circ$ rms phase error at 35 GHz, and can handle 10 dBm of RF power (P_{1dB}). For the single-ended design, a SiGe low noise amplifier (Chapter 2) is placed before the CMOS phase shifter, and the LNA/phase shifter results in 11 ± 1.5 dB gain and <3.4 dB of noise figure. In the core of the differential front-end, a VG-LNA (Chapter 2) is integrated together, and the VG-LNA/phase shifter results in 10 ± 1.3 dB gain and 3.8 dB of noise figure. The gain variation can be reduced to 9.1 ± 0.45 dB with the variable gain function applied. The single-ended and differential front-ends occupy a very small chip area, with a size of $350 \times 800 \mu\text{m}^2$ and $350 \times 950 \mu\text{m}^2$, respectively, excluding pads. These chips are competitive with the GaAs and InP designs, and will pave the way for low-cost millimeter-wave phased array front-ends based on silicon technology.

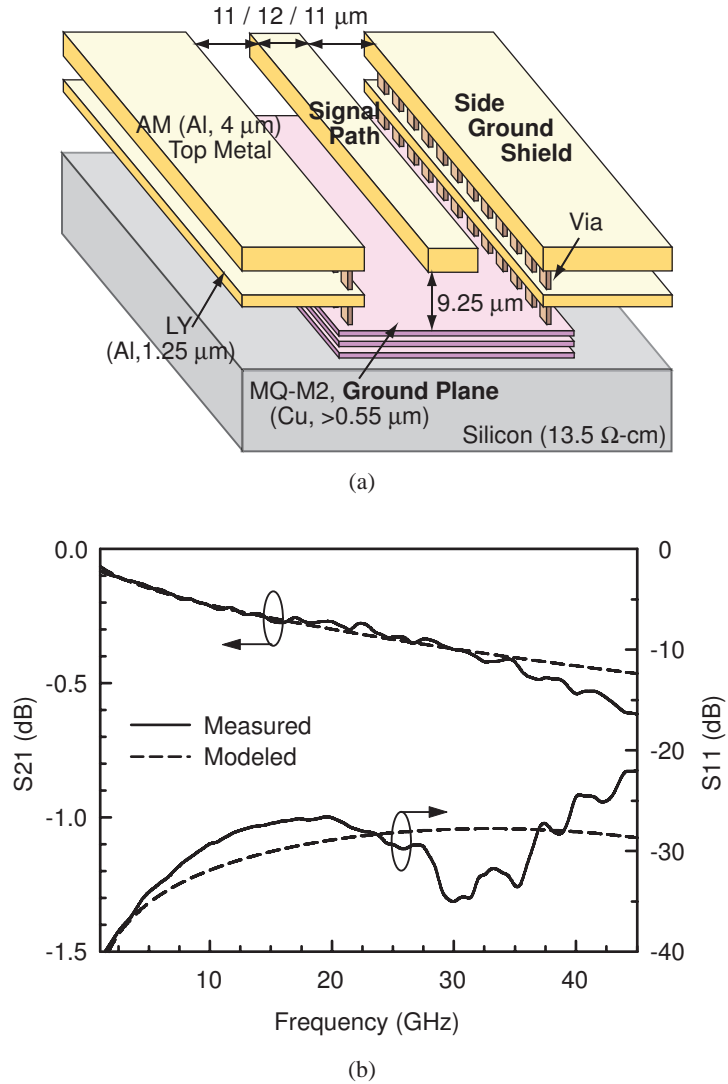


Figure 3.2 (a) Shielded 50 Ω microstrip line structure using the 7 metal-layer profile (IBM 8HP) and (b) measured and modeled S-parameters of the transmission lines ($Z_o = 48.5 \Omega$, $\alpha = 0.4$ dB/mm and $\epsilon_{eff} = 3.9$).

3.2 Phase Shifter Design

3.2.1 Transmission Line and Pad Transition

The IBM 8HP process supports 7 metal layers including top 2 thick metal layers. A 50- Ω transmission line is designed as shown in Fig. 3.2(a). The bottom and side ground plane shield the signal line from the lossy substrate and nearby inductors or transmission lines. The 50 Ω line is measured and results in a impedance (Z_o) of $\sim 48.5 \Omega$, a loss (α) of 0.4 dB/mm, and an effective permittivity (ϵ_{eff}) of 3.9 at 35 GHz (Fig. 3.2(b)). The transition between the transmission line and G-S-G

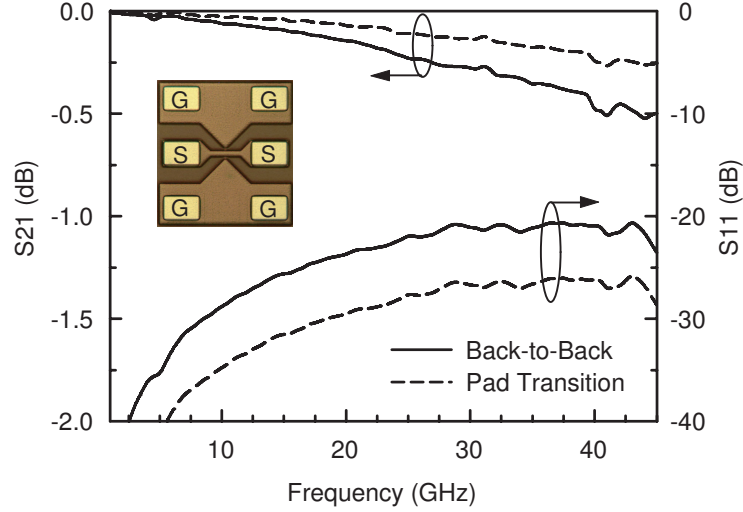


Figure 3.3 Measured S-parameters of the pad transitions.

pad is also designed using Sonnet to provide a $50\text{-}\Omega$ impedance, and is measured in a back-to-back configuration (Fig. 3.3). The performance of a single transition then obtained using a symmetrical ABCD matrix, and result in a return loss of < -25 dB up to 45 GHz, and a insertion loss of 0.2 dB at 35 GHz.

3.2.2 CMOS Switches

The phase shifters are based on $0.12\ \mu\text{m}$ CMOS transistors (Fig. 3.4). The CMOS transistor is a 4-port device with a body node of the substrate contact. The CMOS gate is biased using a large resistor, $R_C = 20\ \text{k}\Omega$, in order to prevent signal leaking and oxide breakdown. Fig. 3.4(b) shows the simplified circuit model of an nMOS series switch, where C_{ds} is the series capacitance between the drain and source and C_j is the drain and source junction capacitance. R_{sub} is the series resistance from the junction to the ground node, and therefore includes the substrate resistance and substrate contact resistance (R_{subc}). R_{sub} highly depends on the size and distance (from the transistor) of substrate contacts, and even the transistor shape [42]. Therefore, large substrate contacts ($35 \times 50\ \mu\text{m}^2$) are placed very closely all around each nMOS transistor to minimize the uncertainty, and R_{sub} is assumed to be $50\ \Omega$ in this design [43]. Minimizing R_{sub} with the large substrate contacts also increases the isolation of the CMOS switch because it reduces the input signal leakage through the junction capacitance to the output port.

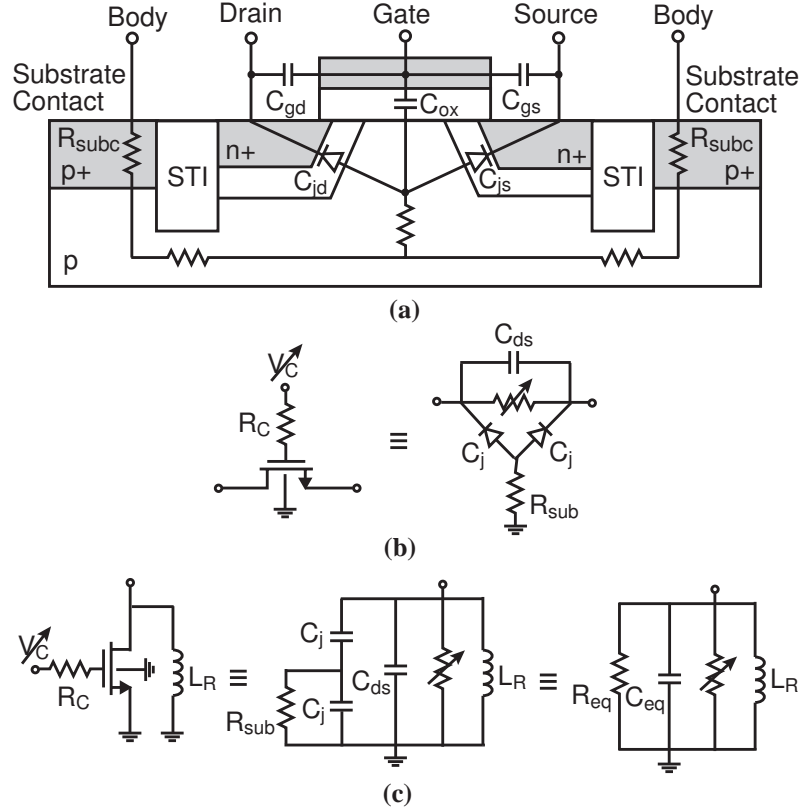


Figure 3.4 a) Cross sectional view of CMOS transistor and simplified circuit models of (b) a series switch and (b) a shunt switch with a parasitic-resonating inductor.

The on-state resistance of CMOS switches can usually be reduced by enlarging the gate width in low frequency application. However, at Ka-band frequencies, capacitive coupling to the substrate due to the junction capacitances C_j results in an increased signal loss. This means that there is an optimum value for the gate width in order to minimize the insertion loss at a given frequency and a specific input/output impedance [44]. Fig. 3.5 shows that the insertion loss is minimized when the gate width is 20–26 μm (optimal $w = 23 \mu\text{m}$). The simplified model values of the switch are also shown for $w = 23 \mu\text{m}$.

The CMOS shunt switch and its equivalent circuit is also shown in Fig. 3.4(c). The gate width of the shunt switch can be larger than the series switch because the junction capacitances do not degrade the on-state switch performance due to the already grounded source. The small on-state resistance is more important for the shunt switch so as to minimize the impedance to the ground. However, the junction capacitances degrade the off-state isolation (to ground) and this limits the transistor size. A shunt inductor ($L_R = 1/\omega^2 C_{eq}$) can be connected in parallel with the shunt switch

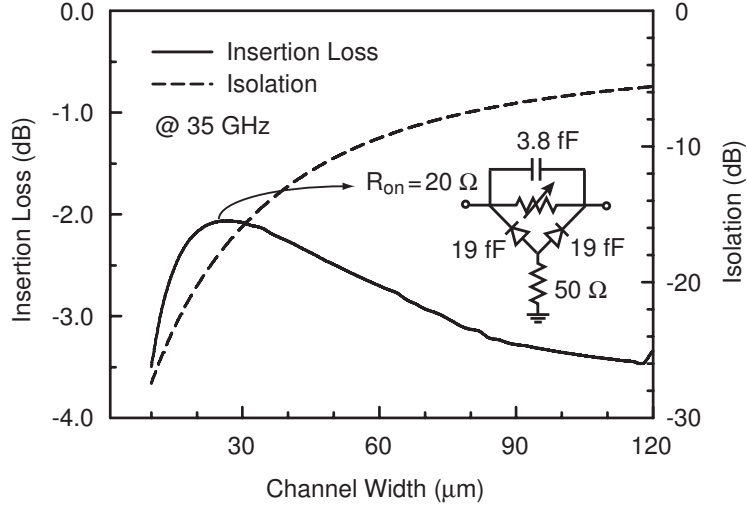


Figure 3.5 Simulated insertion loss and isolation of CMOS series switch at 35 GHz versus channel width. The simplified model of 23 μm wide CMOS switch is also shown.

to resonate out the parasitic capacitance (C_{eq}) at a desired frequency and this allows an increase in the transistor size. In Fig. 3.4(c), C_{eq} and R_{eq} of the equivalent circuit are calculated using:

$$R_{eq} = \frac{4\omega^2 R_{sub}^2 C_j^2 + 1}{\omega^2 R_{sub} C_j^2} > \frac{4}{\omega C_j} \quad (3.1)$$

$$C_{eq} = \frac{C_j + 2\omega^2 R_{sub}^2 C_j^3}{4\omega^2 R_{sub}^2 C_j^2 + 1} + C_{ds}, \quad (3.2)$$

and R_{eq} is usually large ($>1 \text{ k}\Omega$) unless the transistor is extremely large. Therefore the off-state isolation depends mostly on the quality-factor (Q) of L_R . In the phase shifter design, the gate width of the shunt switch is enlarged to 34 μm considering the inductor value and the isolation bandwidth at 35 GHz.

3.2.3 Single-Ended Switched-Delay Phase Shifter

For a switched-delay type phase shifter, low-pass or high-pass Π and T networks provide up to 90° of phase delay or advance while being matched at a desired frequency [34, 40]. The inductor and capacitor values for the low- or high-pass networks are calculated to provide ϕ phase delay or

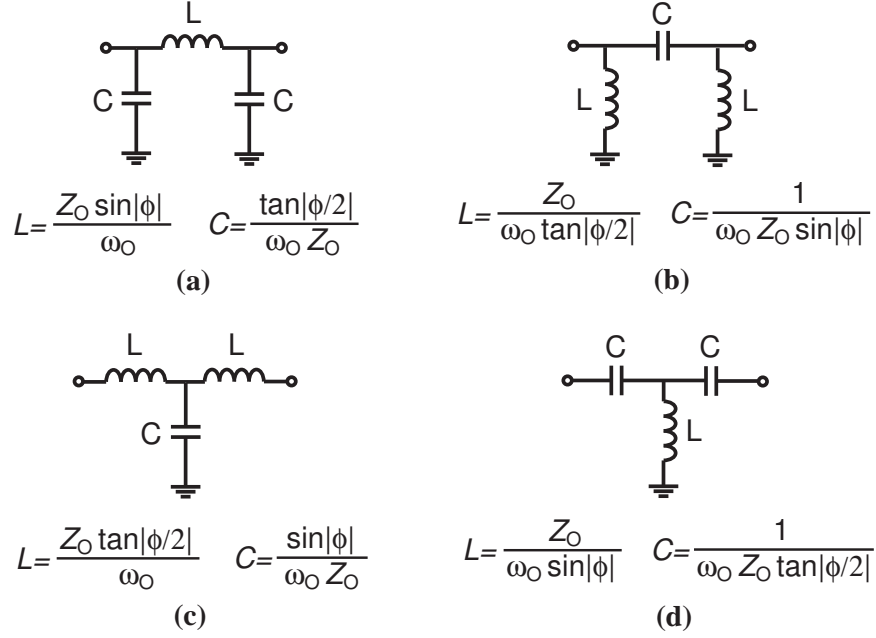


Figure 3.6 (a) Low-pass Π , (b) high-pass Π , (c) low-pass T and (d) high-pass T networks with $|\phi| < 90^\circ$ insertion phase and perfect matching to Z_0 at ω_0 .

advance using:

$$|\angle S_{21}| = |\angle S_{12}| = \phi \quad (3.3)$$

$$S_{11} = S_{22} = 0, \quad (3.4)$$

and are summarized in Fig. 3.6. The low-pass Π network is preferred on silicon since it requires a single and small inductor.

Fig. 3.7 shows the switched-delay phase shifter using CMOS switches and the simplified circuit model of the bypass and phase delay states. With T_1 off and T_2 on, L_S and C_P form a low-pass Π network with a delay given by $\phi = \sin^{-1}(\omega_0 L_S / Z_0)$. When T_1 is on and T_2 is off, L_R resonates with the parasitic capacitance of T_2 , and L_S and $C_P/2$ are in parallel with the on-state resistance (R_{on1}) of T_1 . The total reactance of L_S and $C_P/2$ is

$$X_P = \frac{1}{1/j\omega_0 L_S + j\omega_0 2C_P} \quad (3.5)$$

$$= \frac{Z_0}{1/j \sin|\phi| + j2 \tan|\phi/2|} \quad (3.6)$$

$$= j 2Z_0 \tan|\phi/2|, \quad (3.7)$$

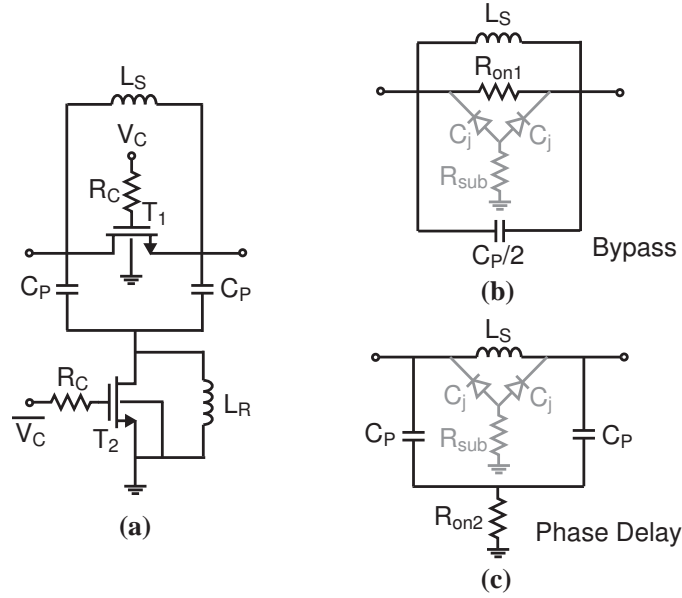


Figure 3.7 (a) Single-ended CMOS 1-bit phase shifter and the simplified circuit model of the (d) bypass and (e) phase delay states.

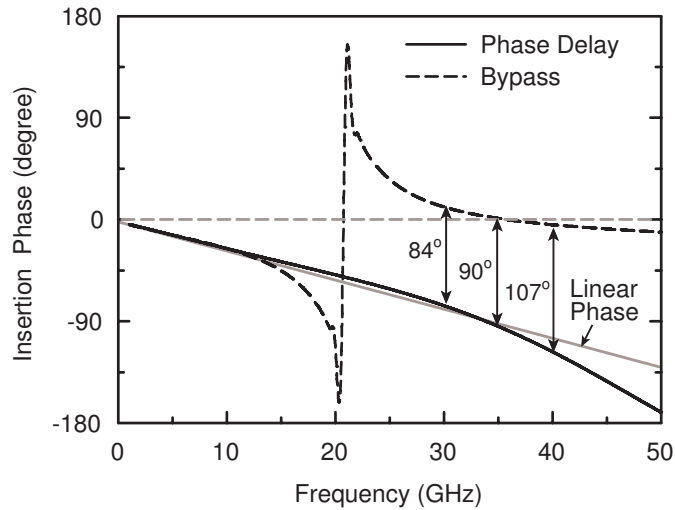
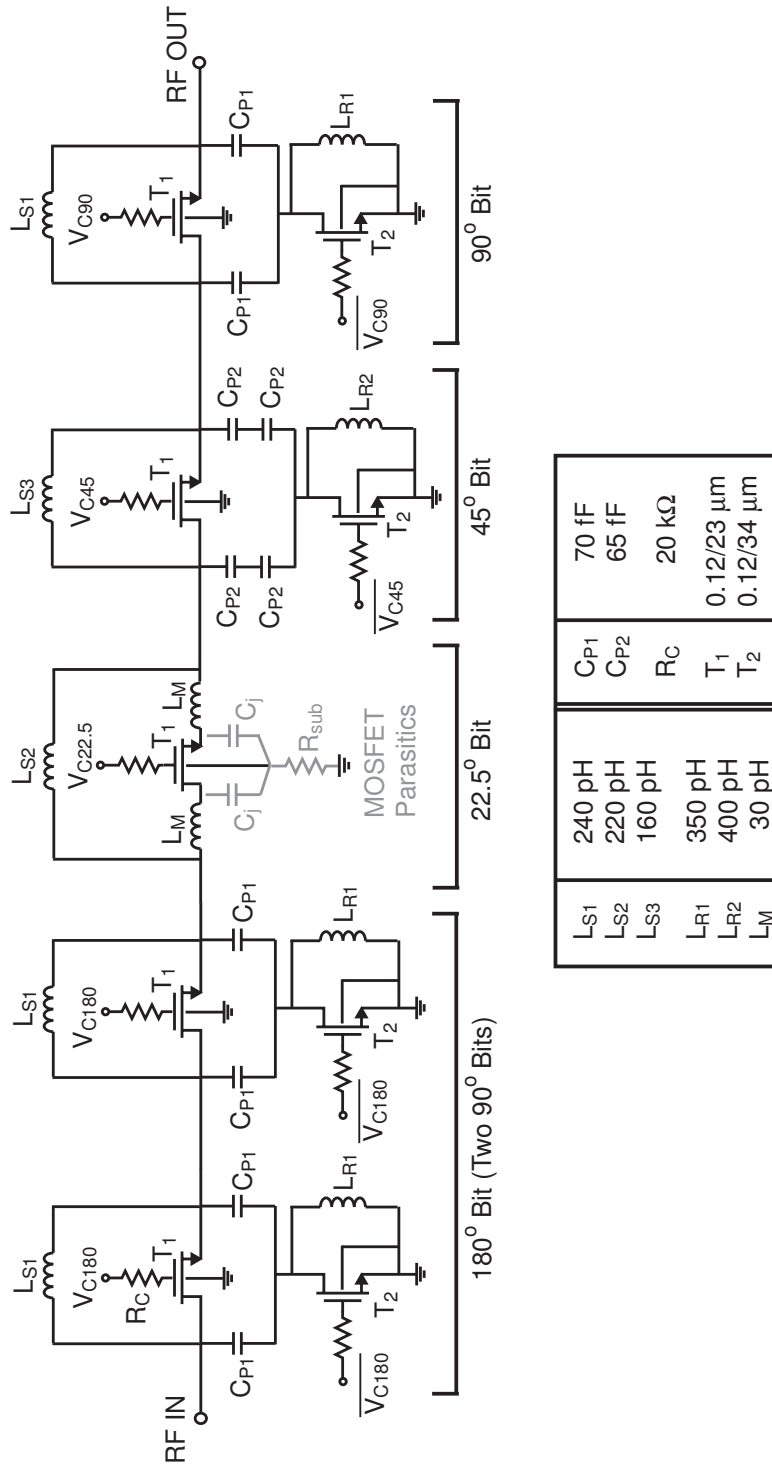


Figure 3.8 Simulated insertion phase of the 1-bit CMOS 90° phase shifter.

and has minimal impact on the insertion phase of the bypass state as long as $X_P \gg R_{on1}$. When X_P is comparable with R_{on1} , the bypass state also results in a small phase delay, but the low-pass network can be designed to provide an extra phase delay so as to achieve the desired phase difference between the bypass and phase-delay states. Fig. 3.8 shows the simulated insertion phase of the 90° CMOS phase shifter. The bypass and phase delay states have 0° and -90° insertion phase at 35 GHz. The insertion phase of the low-pass Π network is linear up to 35 GHz and the bypass state



L_{S1}	C_{P1}	70 fF
L_{S2}	C_{P2}	65 fF
L_{S3}	R_C	$20 \text{ k}\Omega$
L_{R1}	T_1	$0.12/23 \text{ }\mu\text{m}$
L_{R2}	T_2	$0.12/34 \text{ }\mu\text{m}$
L_M		30 pF

Figure 3.9 Schematic of the single-ended Ka-band 4-bit CMOS phase shifter.

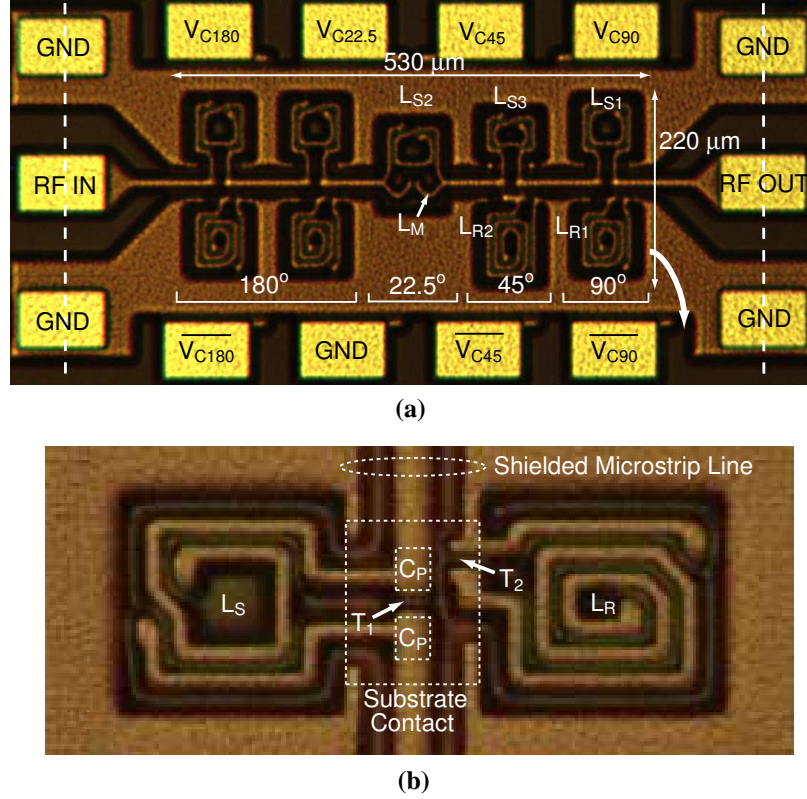


Figure 3.10 Chip photographs of (a) the single-ended Ka-band phased shifter, and (b) a blow-up view of the 90° phase bit.

has a parasitic resonant frequency at $\omega = 1/\sqrt{L_R(C_{eq} + 2C_P)} = \omega_o/\sqrt{2C_P/C_{eq} + 1}$ due to C_P . Still, one can achieve good performance at 28–40 GHz.

The 4-bit phase shifter is designed using 5 stages of switched-delay networks (Fig. 3.9). The first two stages are 90° phase shifters and tied together to become the 180° bit. The 22.5° , 45° and 90° phase bits are cascaded in series afterwards using $50\ \Omega$ lines. Each stage can operate in either a bypass or low-pass (delay) mode. The values of the spiral inductors (L_S and L_R) and MIM capacitors (C_P) are optimized using full-wave electromagnetic simulations and take into account the parasitics of T_1 and T_2 . The 45° phase bit is designed with two shunt capacitors (C_{P2}) in series due to the minimum available MIM capacitor value. In the case of the 22.5° phase shifter bit, the parasitic capacitances of L_{S2} and T_1 are large enough to effectively become the shunt capacitor of the low-pass network, and L_M matches the junction capacitance for the bypass states. The L and C values are summarized in the table of Fig. 3.9.

The chip photograph of the single-ended phased shifter is shown in Fig. 3.10. A tapered transi-

tion from G-S-G pads to the microstrip line provides a $50\ \Omega$ input and output impedance. Inductors are surrounded closely by ground planes to reduce their distance and cross-coupling, and the parasitics are taken into account. The chip size is $530 \times 220\ \mu\text{m}^2$ ($< 0.12\ \text{mm}^2$) without pads. The CMOS phase shifter does not consume any static power, and results in a simulated average insertion loss of 12 dB at 35 GHz.

3.2.4 Differential 4-Bit Phase Shifter

The differential phase shifter is also designed using the low-pass Π networks. Fig. 3.11(a) presents a single bit and its differential series switch model. Since the switches operate differentially, the RF virtual ground of the substrate nodes are formed inside the substrate. This decreases R_{sub} of the differential switch compared to the single-ended switch since the substrate contact resistance (R_{subc}) can be ignored and also the substrate resistance itself is decreased by a factor of 2. For the differential shunt switch, R_{sub} can be completely ignored in the design due to the virtual ground at the junction. The equivalent circuit models for the bypass and phase delay states are shown in Fig. 3.11(b) and (c), where C_{ds} is ignored since it is small.

Because R_{sub} for the differential switch is small, the junction capacitances (C_j) of the series and shunt switches can be matched with input and output inductors, L_M , and therefore the gate width of the CMOS transistor can be enlarged. Also, the differential shunt switch can be designed without the resonating inductor. Fig. 3.11(b) and (c) also shows the simplified differential half-circuit models for the bypass and phase delay states, and explain how the inductor and capacitor values are calculated. L_M is first designed to match the two junction capacitances of the series switch and series combination (C_x) of $2C_P$ and C_j (of the shunt switch). C_x is almost C_j if $2C_P$ is large enough. Then, L_M and $1.5C_j$ can be considered as an impedance transformer between Z_o and Z_X , where $Z_X = Z_o(1 + Q^2) = Z_o + \omega^2 L_M^2 / Z_o$. Therefore, L_S and C_P of the low-pass Π network are calculated using the equations in Fig. 3.6 with Z_X instead of Z_o . In this case, the loss due to R_{on} becomes smaller because Z_X is larger than Z_o .

The 4-bit differential phase shifter is shown in Fig. 3.12. The 90° and 45° phase bit are based on the switched-delay networks using differential CMOS switches. The 180° phase bit is based on a differential CMOS quad switch with input and output matching inductors. The 180° phase bit is

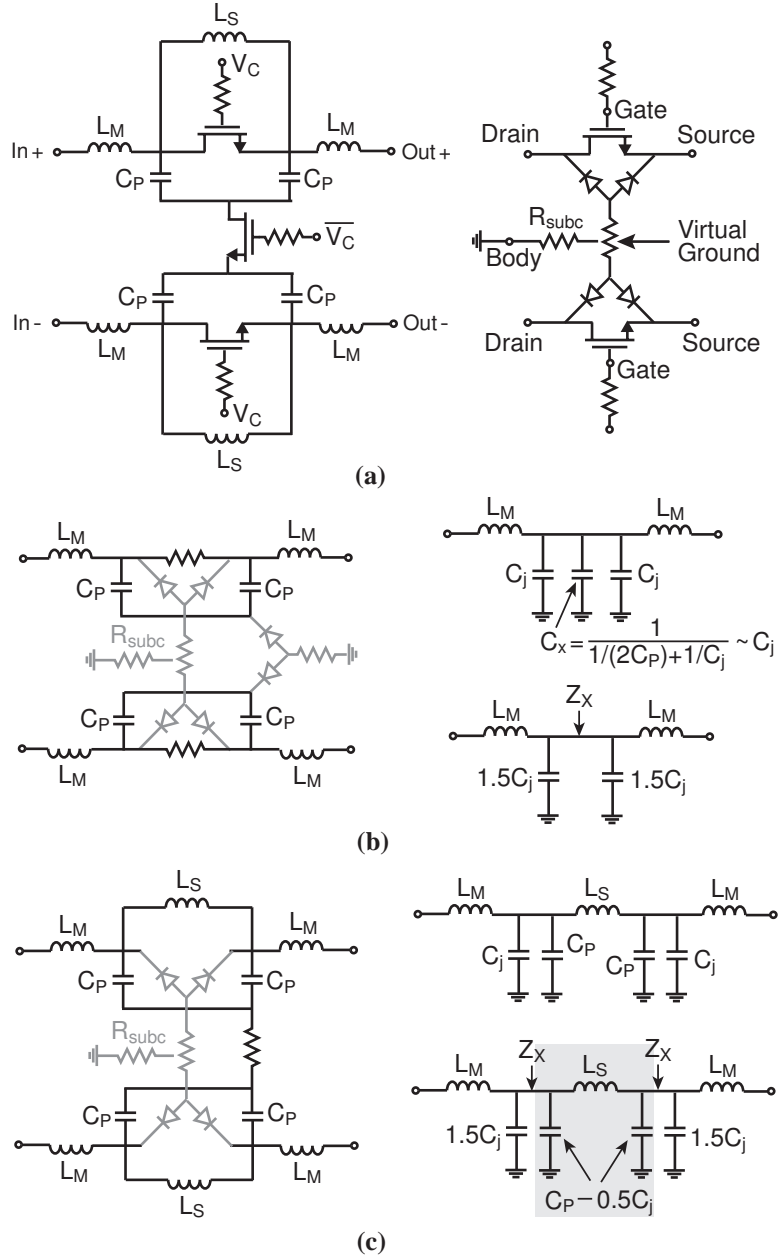


Figure 3.11 (a) Differential CMOS 1-bit phase shifter with the differential CMOS switch, and the equivalent circuit and simplified half-circuit of (b) bypass and (c) phase delay states.

placed between the 90° and 45° phase bit and their input and output matching inductors are combined together. The matching inductors, L_M for the differential paths are reversely coupled to each other so as to take advantage of the mutual coupling. The 22.5° phase bit is a loaded-line phase shifter using varactor diodes (HVAR) [45]. The loaded line is composed of L_D and C_D , and has an impedance of 60Ω for $C_D = 10 \text{ fF}$ ($V_{C22.5} = 2.5 \text{ V}$) and 40Ω for $C_D = 35 \text{ fF}$ ($V_{C22.5} = 0 \text{ V}$) considering all the parasitics. The diode is operated in the digital mode ($V_{C22.5} = 0/2.5 \text{ V}$) resulting

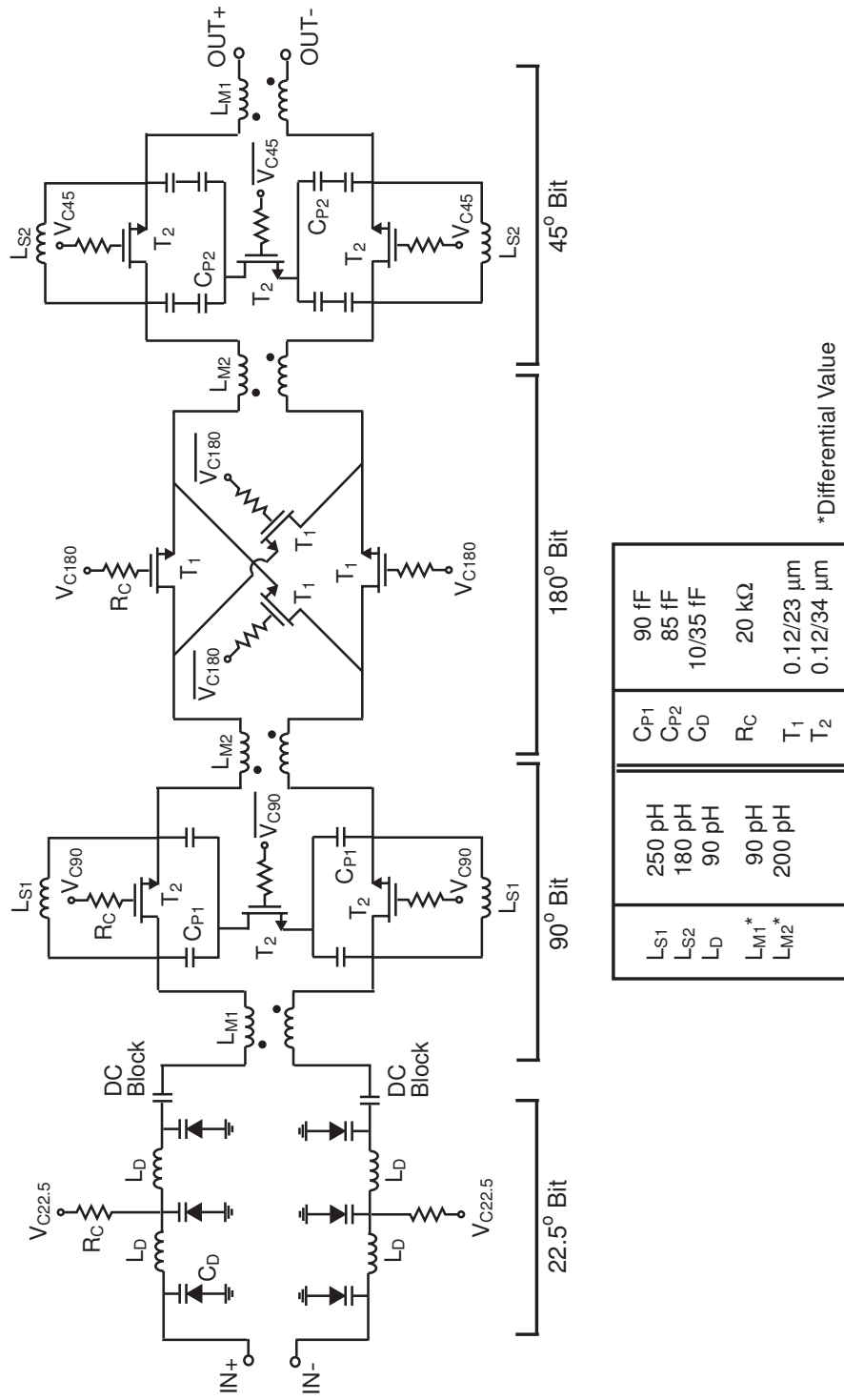
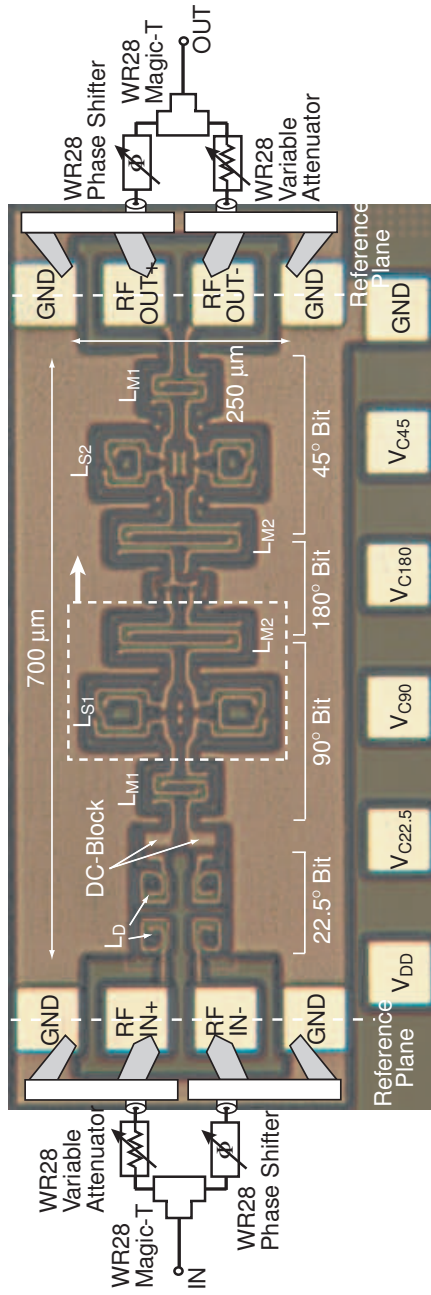
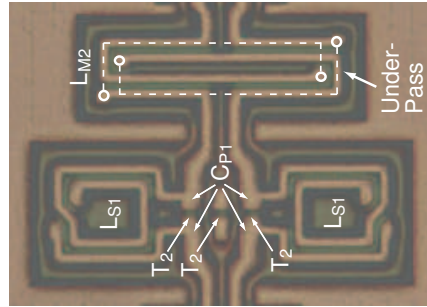


Figure 3.12 Schematic of the differential Ka-band 4-bit CMOS phase shifter.



(a)



(b)

Figure 3.13 Chip photograph of (a) the differential Ka-band phased shifter, and (b) the blow-up view of the 90° phase bit and L_{M2} . The Ka-band differential measurement setup is also shown together.

in 22.5° phase difference. The junction area of the diode is $4 \times 4 \mu\text{m}^2$, and the quality-factor is 4–11 for the reverse bias voltage of 0–2.5 V. The final L and C values of the differential phase shifter are obtained using full-wave simulation and summarized in the table of Fig. 3.12.

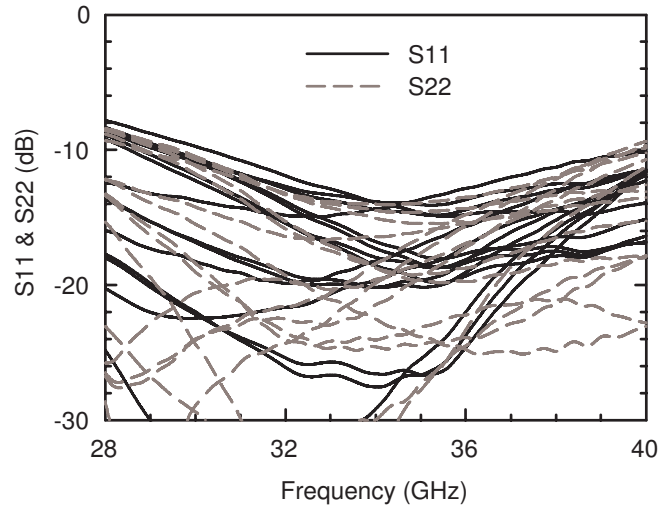
Fig. 3.13 presents the chip photograph of the differential phased shifter. Inductors are also surrounded closely by ground planes, and all parasitics are taken into account using full-wave simulation. The differential matching inductors (L_M) are designed using two top metal layers to maximize the mutual coupling and the under-pass of the inductors is shown in Fig. 3.13(b). The CMOS switches are placed very close to each other to take the advantage of the differential switch topology by reducing the substrate resistance between the transistors. The chip size is $700 \times 250 \mu\text{m}^2$ ($< 0.18 \text{ mm}^2$) without pads. The Ka-band 4-bit differential phase shifter also does not consume any static power, and results in an average insertion loss of 10 dB at 35 GHz.

3.3 Phase Shifter Measurements

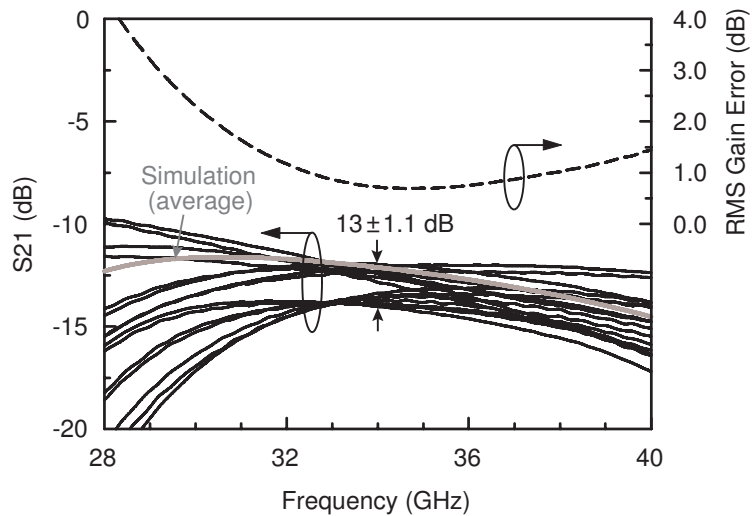
3.3.1 Single-Ended 4-Bit Phase Shifter

The single-ended phase shifter was measured on-chip using an Agilent E8364B network analyzer using SOLT calibration to the probe tips. Fig. 3.14 presents the measured S-parameters for the 16 different phase states. A input/output match of < -10 dB is obtained from 30–40 GHz. The combined input and output losses for the pad transitions (0.35–0.45 dB from 30 to 40 GHz) are not taken out of the measurements. The measured loss is 13 ± 1.1 dB at 34 GHz (12.6 ± 1.1 dB without pad losses), and agrees well with simulations. The rms gain error of the 16 different phase states is about 1 dB at the design frequency (35 GHz).

Fig. 3.15 presents the measured absolute phase performance of the single-ended phase shifter. The phase shifter is designed based on true time-delay networks, and therefore the phase steps increase with frequency. However, the phase steps are relatively constant around the designed frequency because of the negative phase slope of the bypass state (resulting from the resonance of T_2 and L_R). The rms phase error ($\Delta_{rms}\phi$) is calculated from a standard deviation of $\Delta\phi_n = \angle S_{21,n} - 22.5^\circ \times n$, and the rms phase error at 35 GHz is 4° . The rms phase error at 28–38 GHz is still less than 11.25° , which is the 5th significant bit and has virtually no effect on the phased array.



(a)



(b)

Figure 3.14 Single-ended phase shifter: Measured (a) input and output return loss, and (b) insertion loss of 16 different phase states and the rms gain error.

Fig. 3.16 presents the insertion loss of each bit of the phase shifter versus the input power (measured separately). The power handling capability of the phase shifter is limited by the junction diode of the CMOS switch since this diode is forward biased when the peak signal voltage is higher than 0.7 V in the negative swing. The power 1-dB compression point (P_{1dB}) of the 90° phase bit is 10 dBm, and this sets the power handling limit. The 45° and 22.5° phase bit have a higher P1dB since they are not as resonant as the 90° phase bit. Measurements on a CMOS series switch (bypass state) show an input third-order intermodulation intercept power (P_{IP3}) of 26 dBm at 35 GHz.

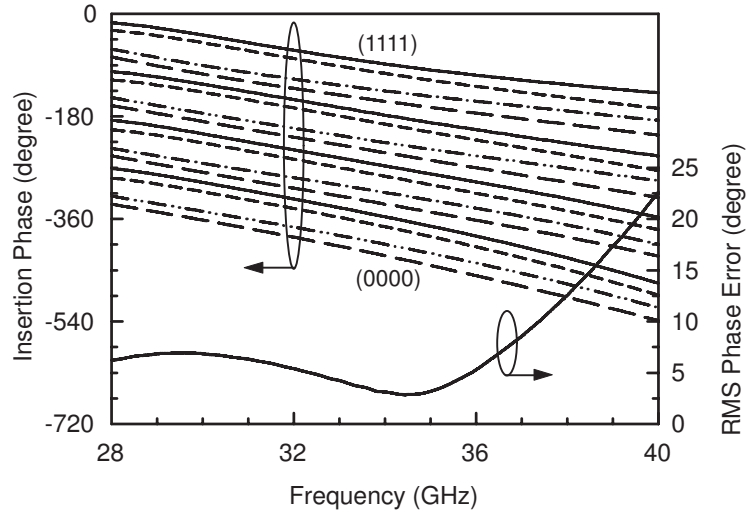


Figure 3.15 Single-ended phase shifter: Measured insertion phase of 16 different phase states and the rms phase error.

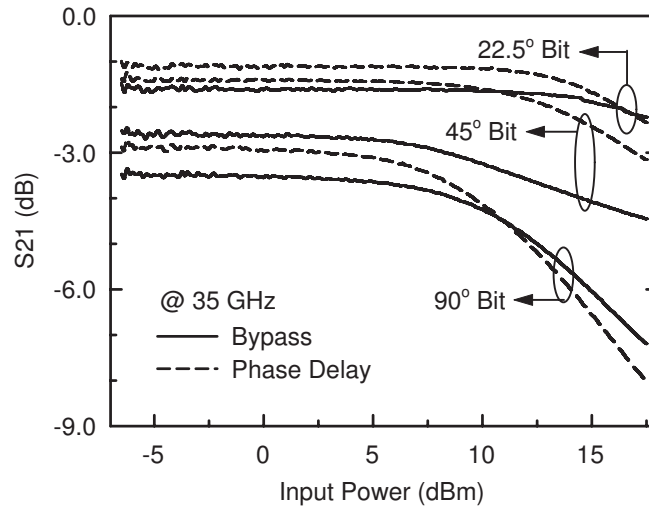
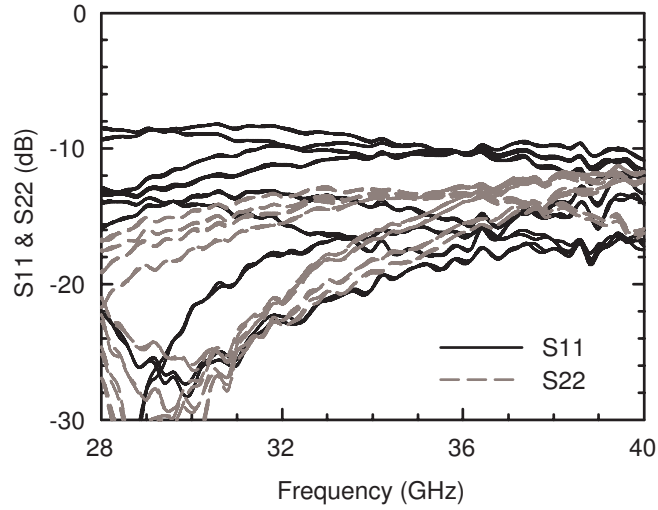


Figure 3.16 Single-ended phase shifter: Measured insertion loss of the each phase bit versus input power. The input and output pad transitions are de-embedded.

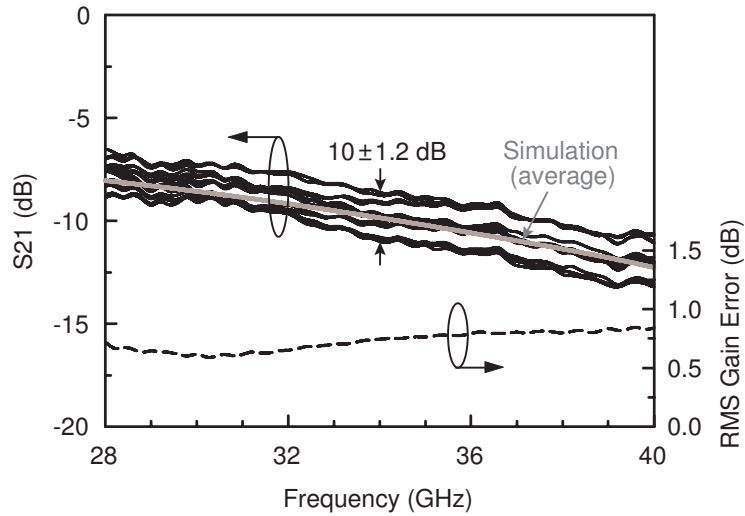
3.3.2 Differential 4-Bit Phase Shifter

The differential phase shifter was measured on-chip using an Agilent E8364B network analyzer using off-chip baluns (Fig. 3.13(a)). A waveguide magic-T is used for the single-to-differential conversion, and a waveguide phase shifter and variable attenuator are also used for fine tuning the phase and amplitude imbalance. The system is then calibrated using a differential calibration substrate and the measured results are referenced to the input and output G-S-S-G pads.

The measured S-parameters for the 16 different phase states are shown in Fig. 3.17. The input



(a)



(b)

Figure 3.17 Differential phase shifter: Measured (a) input and output return loss, and (b) insertion loss of 16 different phase states and the rms gain error.

return loss is less than -8 dB and the output return loss is less than -12 dB at 28–34 GHz. The input return loss is a bit high since the loaded-line phase shifter (22.5° phase bit) is not a perfectly matched phase shifter. The measured loss is 10 ± 1.2 dB at 34 GHz and is less than the single-ended phase shifter since the 180° phase bit is much more compact and contains a single series switch in each path. The rms gain error is less than 1 dB at 28–40 GHz (Fig. 3.17(b)). This is smaller and more constant versus frequency than the single-ended phase shifter because the differential design minimizes the effect of R_{sub} (due to the virtual ground) and series matching inductors are used

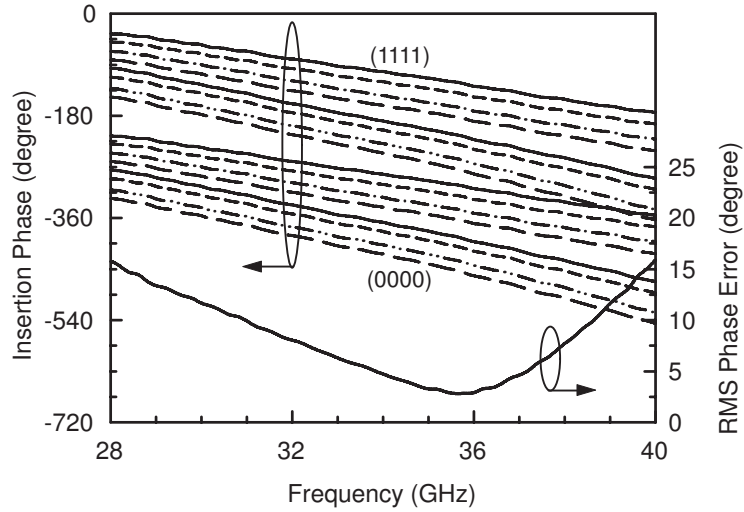


Figure 3.18 Differential phase shifter: Measured insertion phase of 16 different phase states and the rms phase error.

instead of shunt resonant inductors.

Fig. 3.18 presents the measured absolute phase performance of the differential phase shifter and the rms phase error. The 90° , 45° and 22.5° phase bits of the phase shifter are designed based on true time-delay networks, but the $0/180^\circ$ phase bit is a constant phase shifter design. This results in a larger phase step at 28 GHz, and a slight phase overlap at 40 GHz. However, the phase steps are still relatively constant around the design frequency of 35 GHz, and the rms phase error is still less than 15° over the 28–40 GHz range and only 4° at 35 GHz.

3.4 Receiver Front-End Measurements

The single-ended and differential phase shifters result in excellent performance, but have a loss of 10–13 dB. Therefore, it is important to build an LNA to improve the phased array gain and noise figure. The phase shifters can handle a high input power ($P_{1dB} = 10$ dBm), and therefore the total system linearity is not limited by the phase shifter even with a high gain LNA.

3.4.1 Single-Ended LNA/Phase Shifter

The single-ended receiver is shown in Fig. 3.19. The matching inductor L_M of the 22.5° phase bit is increased a bit ($L_M = 70$ pH) for the better input and output matching. The total chip size

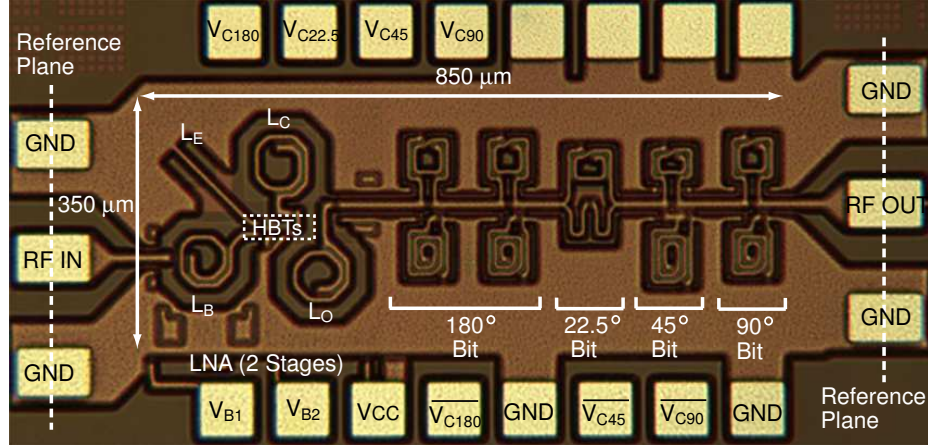


Figure 3.19 Chip photograph of the single-ended Ka-band phased array BiCMOS receiver.

$850 \times 350 \mu\text{m}^2$ and is less than 0.3 mm^2 . The gain and phase of the receiver were also measured on-chip using SOLT calibration to the probe tips. The noise figure was measured using an Agilent 346CK01 noise source and a noise figure measurement personality of the Agilent E4448A spectrum analyzer. Two Ka-band preamplifiers are used in front of the spectrum analyzer and result in a 0.2 dB noise figure uncertainty.

The measured gain and noise figure for all 16 different phase states are shown in Fig. 3.20(a). The single-ended receiver results in 11 ± 1.5 dB of gain at 34 GHz with an associated noise figure of < 3.4 dB. The input return loss for all 16 different phase states is very close to the LNA input characteristics due to the high reverse isolation of the LNA ($S_{11} < -15$ dB at 30–40 GHz). The output return loss of the single-ended receiver is similar to the results of single-ended phase shifter ($S_{22} < -10$ dB at 30–40 GHz, see Fig. 3.14(a)). These results agree very well with simulations. The measured input P_{1dB} and P_{IP3} at 35 GHz are -28 dBm and -22 dBm, respectively. The P_{1dB} and P_{IP3} of the receiver are limited by the LNA rather than the phase shifter.

Fig. 3.20(b) presents the measured absolute phase performance and rms phase error of the single-ended receiver. Two different rms phase errors are calculated using a constant-phase phase shifter and a true time-delay (TTD) phase shifter assumption. The phases step of the true time-delay phase shifter increase linearly versus frequency and the rms error ($\Delta_{TTD.rms}\phi$) is a standard deviation of $\Delta\phi_{TTD.n} = \angle S_{21.n} - f/f_o \cdot 22.5^\circ \times n$. It is seen that the single-ended receiver results in $< 12.5^\circ$ of rms phase error at 28–40 GHz for either model ($\Delta_{rms}\phi$ and $\Delta_{TTD.rms}\phi$).

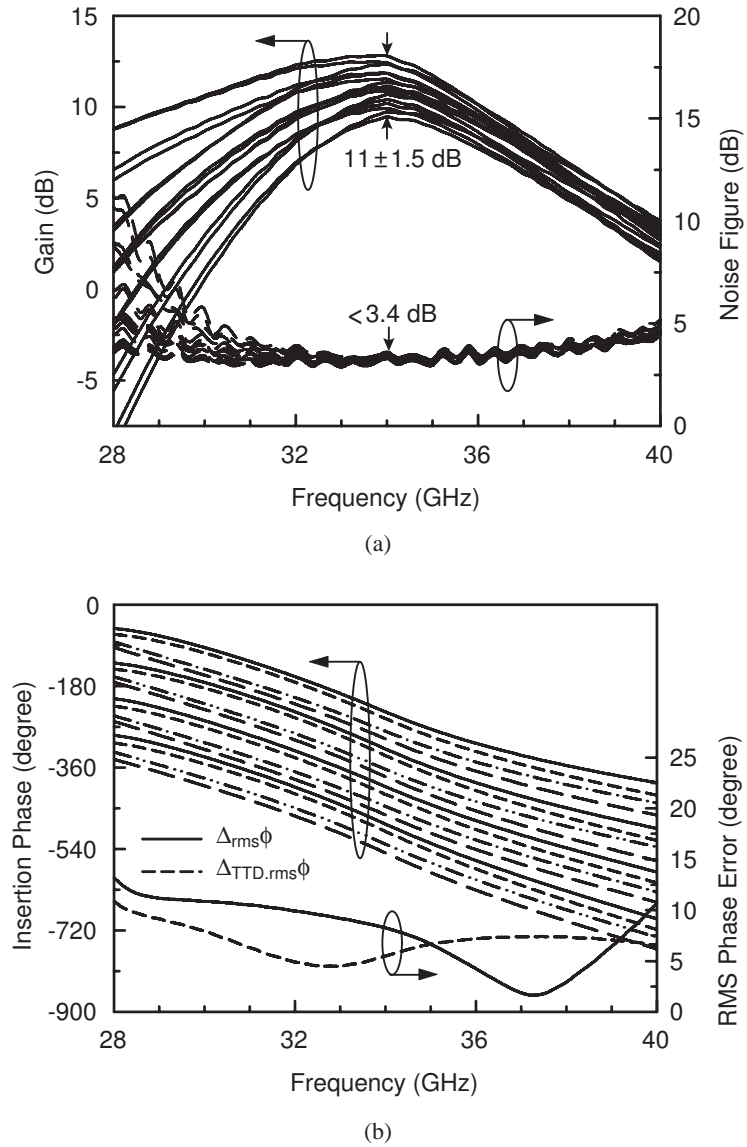


Figure 3.20 Single-ended receiver: Measured (a) gain and noise figure, and (b) insertion phase and rms phase error of 16 different phase states.

3.4.2 Differential VG-LNA/Phase Shifter

The chip photograph of the differential receiver is shown in Fig. 3.21. The total chip size is $950 \times 350 \mu\text{m}^2$ and less than 0.34 mm^2 . The gain and phase of the receiver was measured on-chip using the same method for the differential phase shifter (see Fig. 3.13). The noise figure was also measured using Agilent 346CK01 noise source and a noise figure measurement personality of Agilent E4448A spectrum analyzer with two Ka-band preamplifiers. The loss of the off chip-balun and G-S-S-G probes are measured using the back-to-back configuration and subtracted from the

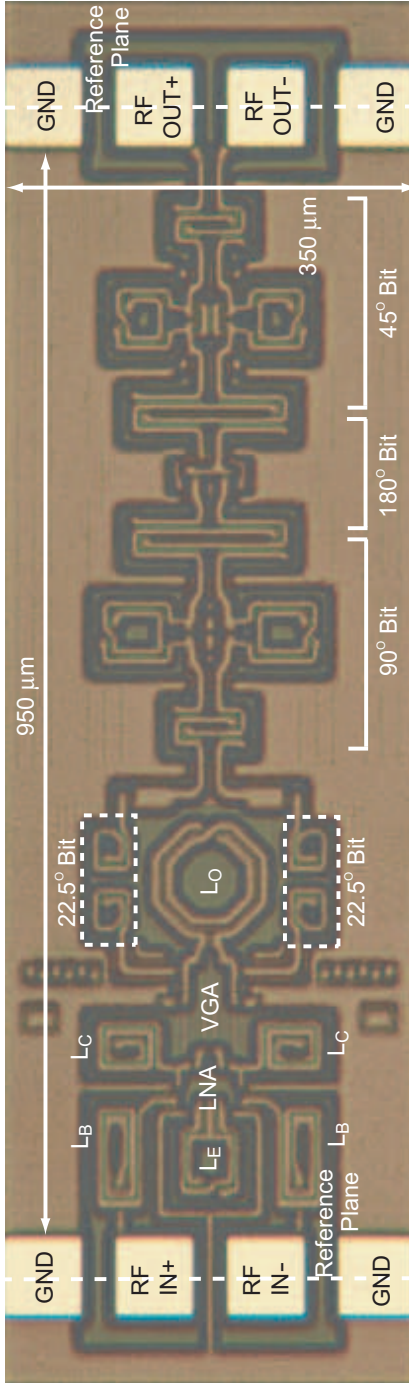
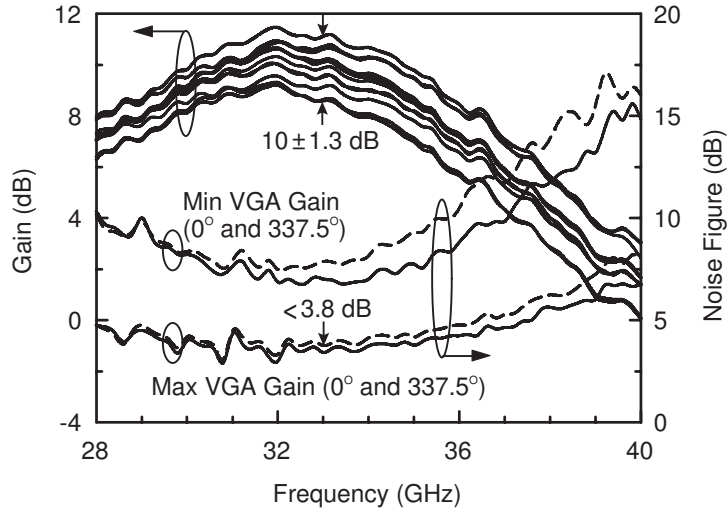
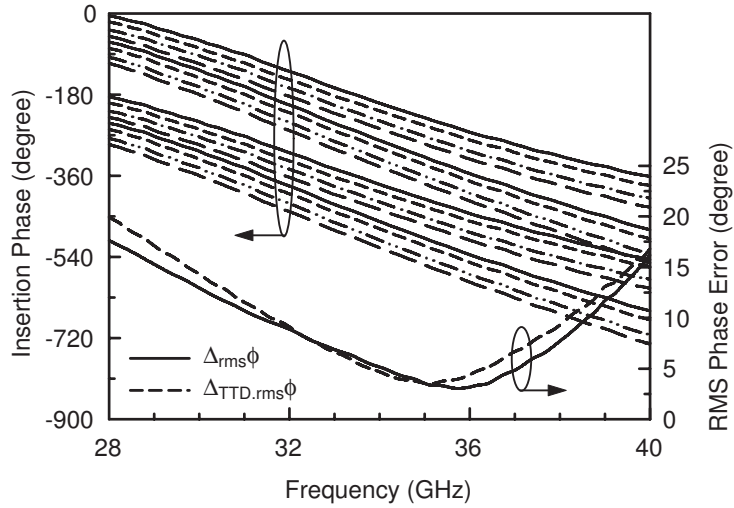


Figure 3.21 Chip photograph of the differential Ka-band phased array BiCMOS receiver (Bias pads are not shown).



(a)



(b)

Figure 3.22 Differential Receiver: Measured (a) gain and noise figure, and (b) insertion phase and rms phase error of 16 different phase states.

measurement.

Fig. 3.22(a) presents the total gain and noise figure of the differential receiver. The gain is 10 ± 1.3 dB at 33 GHz for the maximum gain state of the VG-LNA. The noise figure is measured for the 0° and 337.5° phase states because these represent the highest and lowest loss states of the differential phase shifter. The noise figure is less than 3.8 dB for the maximum gain state of the VG-LNA.

Fig. 3.22(b) presents the measured absolute phase performance and rms phase error of the dif-

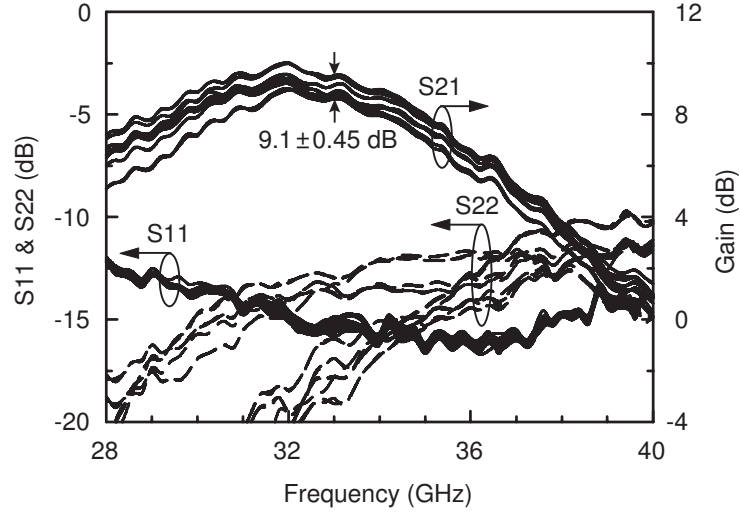


Figure 3.23 Differential Receiver: Measured gain and return loss of 16 different phase states with gain-error compensation using the VGA.

ferential receiver. Both $\Delta_{rms}\phi$ and $\Delta_{TTD.rms}\phi$ are 4° at 35 GHz, and less than 20° at 28–40 GHz. $\Delta_{rms}\phi$ and $\Delta_{TTD.rms}\phi$ of the differential receiver are very similar since the phase shifter is composed of both a true-time delay phase bit (90° , 45° and 22.5°) and a constant phase bit (180°). All the measurements agree very well with simulations.

The gain variation of the VG-LNA is 20–9 dB with a constant gain step in magnitude, and the rms phase imbalance of the VG-LNA is less than 2.5° at 28–40 GHz and only 0.7° at 32–34 GHz. Therefore, the gain imbalance of the phase shifter can be compensated without increasing the phase error. Fig. 3.23 presents the differential receiver gain with gain-error compensation, and the compensated gain is 9.1 ± 0.45 dB at 33 GHz (rms gain error of < 0.35 dB). This is sufficient for phased arrays with low side lobe levels. Fig. 3.23 also shows the input and output return loss of the differential receiver over all phase states. The input return loss is set by the VG-LNA and less than -13 dB and the output return loss is less than -10 dB. The measured input P_{1dB} is -28 dBm at 35 GHz for all 8 different gain states and measured input P_{IP3} at 35 GHz is -20 dBm. Again, P_{1dB} and P_{IP3} are mostly limited by the VG-LNA and not by the phase shifter.

3.5 Summary

This chapter shows that it is possible to obtain state-of-the-art LNA/phase shifters at Ka-band frequency range using a standard silicon BiCMOS technology. The phased array front-end has also

been implemented in a differential design, which is essential for high density (multiple-element) integration and low on-chip coupling. This was not possible with GaAs and InP technologies due to the lack of accurate device matching with millimeter-wave transistors. The silicon front-ends occupy a very small area, and can be arrayed in 4-16 elements on a single silicon chip for compact Ka-band phased-array modules. The silicon modules will not replace the GaAs/InP power amplifier and very low noise amplifier (noise figure of 1–1.5 dB at 35 GHz) but can significantly reduce the cost of the back-end (phase shifters, VGA, combiner, etc.) in defense-based applications.

Chapter 4

10–50 GHz CMOS Distributed Step Attenuator

4.1 Introduction

Modern communication systems require variable attenuators and variable gain amplifiers for amplitude control in a variety of applications such as automatic level control loops, modulators, and phased array systems. Variable attenuators are more suitable for applications which require high linearity, low power consumption and low temperature dependency which cannot be achieved with variable amplifiers [46, 47].

In phased array systems, the beamwidth and sidelobe level of an array are tailored by applying amplitude weighting with gain control circuits. Phased array systems usually have demanding requirements in terms of the power consumption, because each antenna path needs a separate gain control in the transmit/receive module. Therefore, variable attenuators have been used extensively in these systems. A step attenuator is preferred over an analog design since it removes the need of digital-to-analog converters in the control path. A phased array requires precise amplitude control with 1-dB steps and a maximum attenuation of 8–10 dB. However, the step attenuator must have a very low insertion phase variation over the different attenuation states (phase imbalance) to avoid tracking error and complex phase/amplitude calibration [48–50].

Most step attenuators rely on three basic types of topologies shown in Fig. 4.1: the Π -attenuator, the T-attenuator, and the bridged-T attenuator [51–55]. These designs relay a signal through either a bypass line or an attenuation cell with RF switches. These types of attenuators highly depend on the switch performance, and are mostly used in circuits based on III-V semiconductor devices such as GaAs HEMT where high performance transistors are readily available. This is not possible in a CMOS process due the relatively poor transistor performance as a switch at microwave frequencies. Analog type CMOS attenuators are also available and do not require high performance

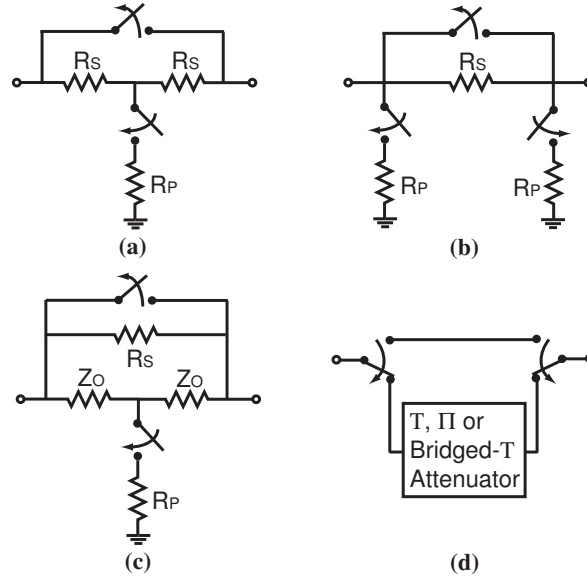


Figure 4.1 Conventional one-bit attenuator networks: (a) T-attenuator, (b) Π -attenuator and (c) bridged-T attenuator using SPST (single-pole-single-throw) switches and (d) using SPDT (single-pole-double-throw) switches.

switches [46, 47, 56], but analog attenuators need a digital-to-analog convertor and consume static power.

In this chapter, a 10–50-GHz CMOS step attenuator using a distributed attenuator topology are presented [57, 58]. The topology is optimized for integration using a CMOS process. The phase imbalance is minimized for applications such as phased array systems. After the limitation of conventional attenuator topologies, as well as the distributed attenuator, is discussed, the circuit implementation and the measured results are presented. The attenuator is controlled by 12 nMOS varistors, and the nMOS parasitics are absorbed in a synthetic transmission line to result in a wide bandwidth. The electrical distance between the varistors is explored to minimize the size of the distributed attenuator, and a method to balance the insertion phase is presented. At 33–37 GHz, the minimum attenuation state loss is 2.1 dB, and the maximum attenuation state loss is 13.0 dB. The attenuator has a maximum attenuation range of 11 dB with 0.9-dB steps (13 states). The rms phase imbalance is less than 3° at DC–50 GHz for all attenuation states. The attenuator does not consume any static power and the input 1-dB compression point is 5 dBm (defined as the 1-dB drop in the maximum attenuation range) at 25 GHz. The total chip size excluding pads is $200 \times 750 \mu\text{m}^2$ (0.15 mm^2).

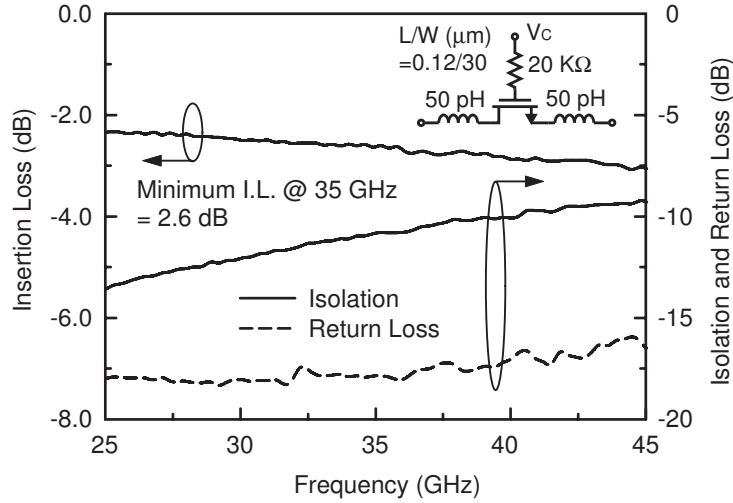


Figure 4.2 Measured response of the nMOS SPST switch optimized for minimum loss at 35 GHz.

4.2 Design Theory

4.2.1 Conventional Design Limitations

Even with rapid gate-length scaling in CMOS processes, CMOS switches are still difficult to realize with a low insertion loss and high isolation at frequencies above 20 GHz. To improve the insertion loss, the channel resistance of CMOS transistor is usually reduced by enlarging the gate width even though the isolation is degraded. However, capacitive coupling with the substrate due to the junction capacitances results in an increased signal loss to the substrate. This means that there is an optimum value for the gate width in order to minimize the insertion loss at a given frequency [44]. Fig. 4.2 shows the measured insertion loss and isolation of a 0.12- μm CMOS series switch with a gate length optimized for 30–40-GHz operation. The available minimum insertion loss at 35 GHz is 2.6 dB with an isolation of -13 dB. Therefore, the minimum loss per attenuator bit is 2.6 dB for the topologies of Fig. 4.1(a)-(c) and 5.2 dB for the topologies of Fig. 4.1(d).

Even with ideal switches, the resistors in the conventional topologies are another design issue in a CMOS process. The ratio of the shunt resistor (R_P) and the series resistor (R_S) for 1-dB attenuation is 150:1 for the Π -attenuator and the T-attenuator and 67:1 for the bridged-T attenuator [59]. Also, R_S values are as low as a few ohms in 50- Ω systems. These results in a layout concern because of the limited sheet-resistance value available in CMOS processes. If one uses two different materi-

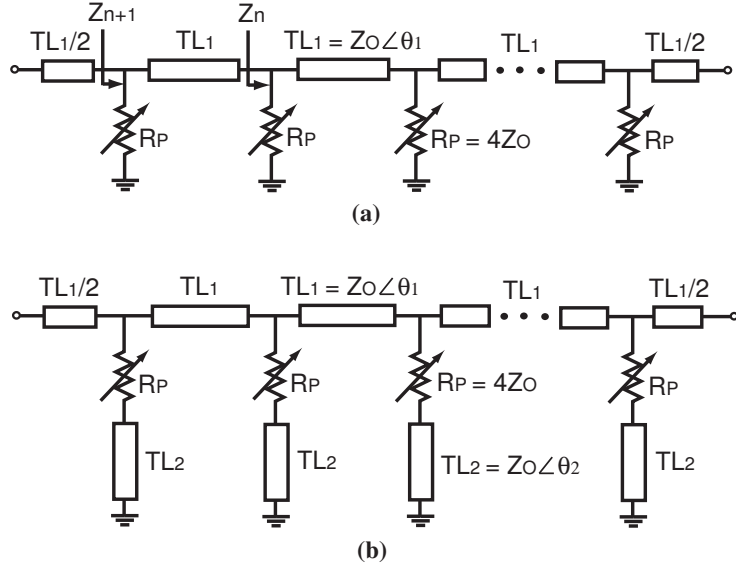


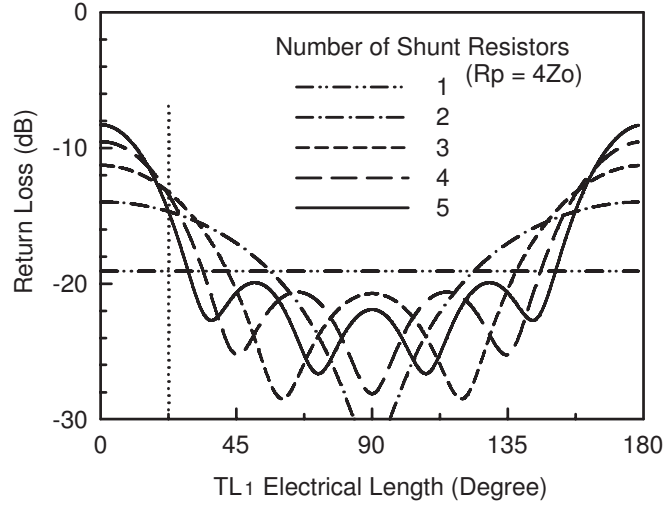
Figure 4.3 (a) Distributed step attenuator and (b) phase-balanced distributed step attenuator with a shorter electrical distance between the shunt varistors.

als for the resistors, the attenuator suffers from mismatch and high temperature dependency. Also, very small value resistors are susceptible to process variations and parasitics (shunt capacitance and series inductance).

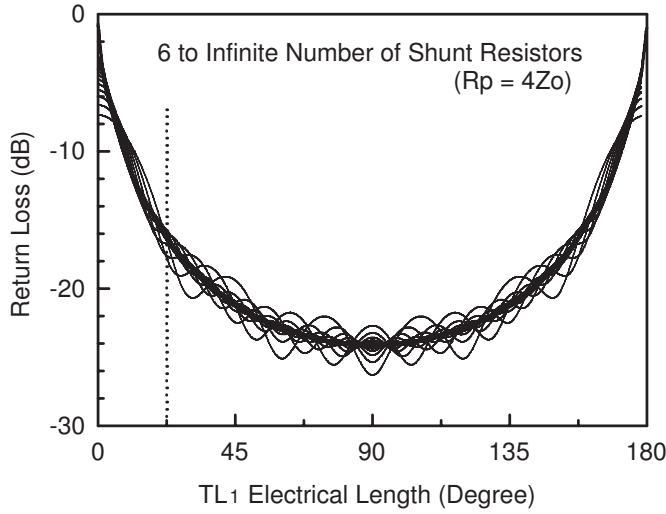
4.2.2 Distributed Attenuator Concept

Distributed attenuators have been used in microwave circuits for several decades [57]. In these designs, shunt PIN diodes are used as a switch or varistor and spaced a quarter wavelength apart. The quarter wavelength transmission lines (t-lines) are used as impedance inverters to match the input and output impedance of the shunt diodes. By changing the number of the actuated (forward biased) diodes, the distributed attenuator can be used as a step attenuator. The distributed attenuator topology is compatible with a CMOS process due to the absence of series switches, but many quarter wavelength t-lines are not practical in a CMOS process. Therefore, the effects of the electrical distance between the shunt elements are explored in this section.

Fig. 4.3(a) shows a distributed step attenuator network. Shunt varistors are periodically placed in a t-line (Z_0) with a electrical distance of θ_1 between two adjacent elements. The input and output impedance of the attenuator with only one shunt resistor (R_P) is $R_P \parallel Z_0$. When $R_P = 4Z_0$, the insertion loss is about 1 dB and the return loss is less than -19 dB. Fig. 4.4(a) and Fig. 4.4(b) present the



(a)



(b)

Figure 4.4 Return loss of distributed attenuators with (a) 1 to 5 shunt resistors and (b) 6 to infinite number of shunt resistors as a function of electrical distance between the shunt resistors

return loss of the distributed attenuator with 1 to 5 shunt resistors, and 6 to infinite number of shunt resistors as a function of θ_1 , respectively. As the number of shunt resistors increases, the return loss converges to a value, RL_∞ . RL_∞ can be calculated from the relation between Z_{n+1} and Z_n (shown in Fig. 4.3(a)) as:

$$\frac{1}{Z_{n+1}} = \frac{1}{R_P} + \frac{1}{Z_o \left(\frac{Z_n + jZ_o \tan \theta_1}{Z_o + jZ_n \tan \theta_1} \right)} \quad (4.1)$$

Table 4.1 On/Off Selection of 12 Shunt Varistors Spaced 22.5° Apart and The Electrical Distance Between The Actuated Varistors (\ominus :ON (Actuated), $-$:OFF with $R_P = 4Z_o$).

Attenuation (dB)	0	1	2	3	4	5	6	12
R_{P1}	-	-	-	-	-	-	-	\ominus
R_{P2}	-	-	-	-	-	\ominus	-	\ominus
R_{P3}	-	-	-	\ominus	\ominus	-	-	\ominus
R_{P4}	-	-	\ominus	-	-	\ominus	\ominus	\ominus
R_{P5}	-	-	-	-	\ominus	-	\ominus	\ominus
R_{P6}	-	\ominus	-	\ominus	-	\ominus	\ominus	\ominus
R_{P7}	-	-	-	-	\ominus	-	\ominus	\ominus
R_{P8}	-	-	\ominus	-	-	\ominus	\ominus	\ominus
R_{P9}	-	-	-	\ominus	\ominus	-	\ominus	\ominus
R_{P10}	-	-	-	-	-	\ominus	-	\ominus
R_{P11}	-	-	-	-	-	-	-	\ominus
R_{P12}	-	-	-	-	-	-	-	\ominus
Elec. Distance ($^\circ$)	n/a	n/a	90	67	45	45	22	22

$$\frac{Z_\infty}{Z_o} = \frac{\sqrt{j4k \tan \theta_1 - (4k^2 + 1) \tan^2 \theta_1} - j \tan \theta_1}{2(1 + jk \tan \theta_1)} \quad (4.2)$$

$$RL_\infty = 20 \log \left| \frac{Z_\infty/Z_o - 1}{Z_\infty/Z_o + 1} \right| \text{ (dB)}, \quad (4.3)$$

where $k = R_P/Z_o$. As expected from the quarter wavelength distributed attenuator, the return loss, RL_∞ is minimized when θ_1 is 90° ($\lambda/4$) as shown in Fig. 4.4(b). Fig. 4.4(b) also shows that the return loss is still low enough (-17 dB) with a much shorter electrical distance such as $\theta_1 = 22.5^\circ$ ($\lambda/16$). In a distributed step attenuator with many shunt varistors, the shunt resistors can be selected from the shunt varistors so as to be a desired θ_1 apart and to result in a good impedance match over all attenuation states. Table 4.1 shows the selection method for 12 distributed shunt varistors with an electrical distance of $\theta_1 = 22.5^\circ$. If 2, 3, 4 or 5 varistors are selected, one can ensure an electrical separation of 90° , 67.5° , 45° , or 45° , respectively, and therefore an impedance match better than -20 dB (Fig. 4.4(a)). For a higher number of selected varistors, the electrical separation is 22.5° , and results in a -17 -dB impedance match (Fig. 4.4(b)).

The insertion loss of the distributed attenuator with 1 to 12 shunt resistors ($R_P = 4Z_o$) is shown

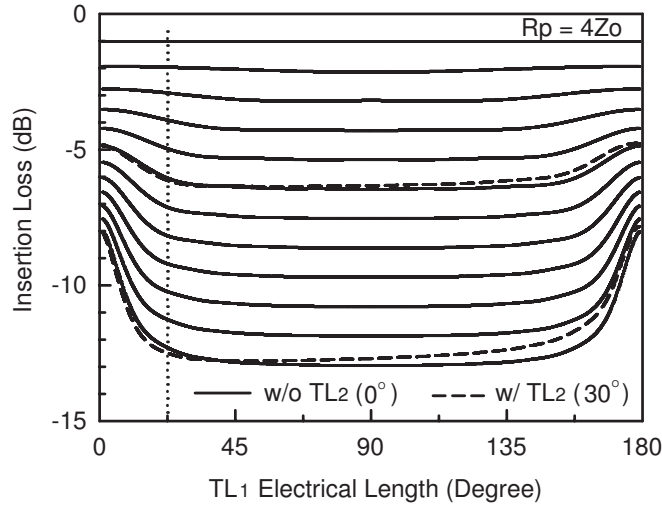


Figure 4.5 Simulated insertion loss of 1 to 12 distributed resistors as a function of the electrical length of TL_1 . Also shown is the insertion loss of 6 and 12 distributed resistors with $TL_2 = 30^\circ$.

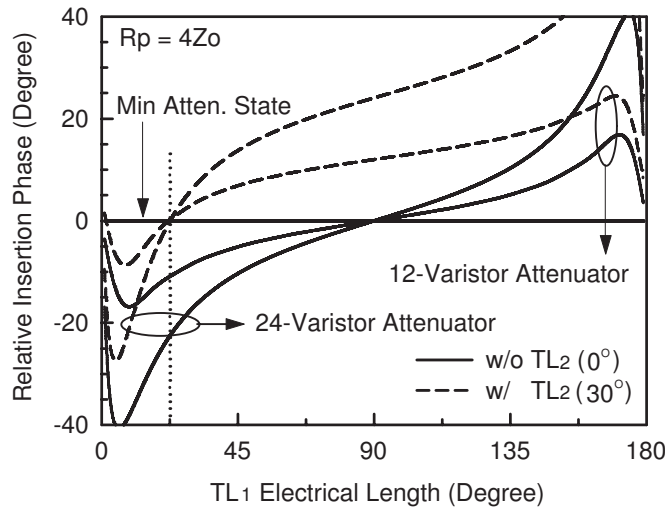


Figure 4.6 Simulated insertion phase of maximum attenuation state relative to minimum attenuation state as a function of TL_1 electrical length of the distributed step attenuators with 12 and 24 varistors when $TL_2 = 0^\circ$ and 30° . With $TL_2 = 30^\circ$, TL_1 electrical length for zero phase imbalance is shifted down from 90° to 22.5° for both cases with 12 and 24 varistors.

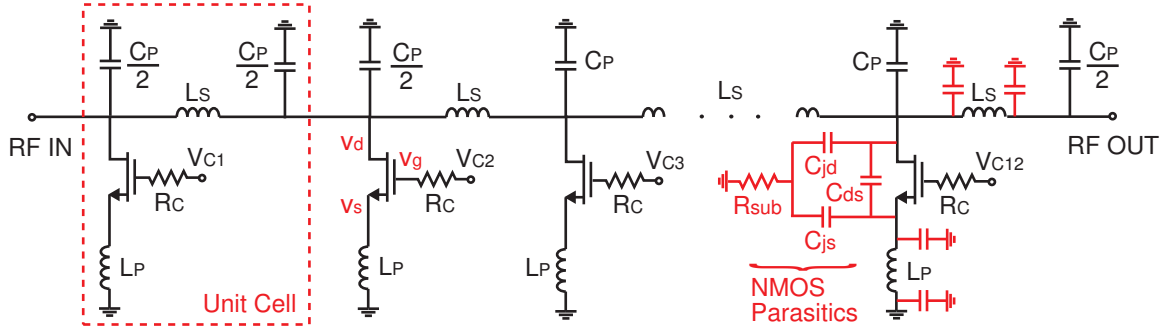
in Fig. 4.5. The attenuation increases monotonically even when θ_1 is as small as 22.5° . However, the insertion phase is not constant for $\theta_1 \neq 90^\circ$ (Fig. 4.6). When $\theta_1 = 22.5^\circ$, the phase difference between the maximum and minimum loss states is more than 11° – 22° for the distributed step attenuator with 12–24 varistors. For a perfect phase balance, another short t-line (TL_2) is introduced in each varistor as shown in Fig. 4.3(b). TL_2 increases the insertion phase of the distributed attenuator because the shunt impedance due to TL_2 is larger at higher frequencies. However, TL_2 does not

affect the phase when the shunt varistors are not actuated. For $TL_2 = 30^\circ$, one can achieve a zero phase difference between the maximum and minimum loss states at $\theta_1 = 22.5^\circ$ as shown in Fig. 4.6. For the low attenuation states (1–5 dB) of the step attenuator, the electrical separation between the actuated varistors is not 22.5° as shown in Table 4.1. However, the phase imbalance is still low, because the phase difference (between the maximum and minimum loss states) of the distributed step attenuator with 1–5 varistors is low at an electrical separation of 22.5° – 90° for $TL_2 = 30^\circ$. Therefore, the total phase imbalance of the distributed step attenuator is always very low ($< 3^\circ$) for all attenuation states.

4.3 Circuit Design and Layout

4.3.1 NMOS Varistors

A distributed step attenuator with 12 varistors is designed using the IBM 8HP 0.12- μm BiC-MOS process (Fig. 4.7). NMOS transistors with a channel width of 2.1 μm are used as varistors in a t-line impedance of $Z_o = 50 \Omega$. The size of the nMOS transistor is designed for a channel resistance of 200 Ω when the gate is biased at the control voltage, $V_C = 1.2 \text{ V}$. This voltage is chosen since it is compatible with (future) on-chip digital logic circuits. Biasing is done using a large resistor, R_C , to prevent the RF signal from leaking through the bias line. The input signal voltage of the attenuator is limited by the drain junction diode of the nMOS transistor, because the junction diode is forward biased when the peak signal voltage ($v_{d,peak}$) is higher than 0.7 V in the negative swing. Because R_C keeps the gate node floating at RF voltages, the gate voltage (V_g) is bootstrapped by the source and drain voltages, and $V_g \approx V_C + (v_d + v_s)/2 \approx V_C + v_d/2$. When the varistor is not actuated ($V_C = 0 \text{ V}$), $|V_{gs}|$ and $|V_{gd}|$ are less than $v_{d,peak}/2$, and this voltage should be below the threshold voltage not to self-bias the varistor. When the varistor is actuated ($V_C = 1.2 \text{ V}$), V_{gs} and V_{gd} change between $1.2 \pm v_{d,peak}/2$. For $v_{d,peak} = 0.7 \text{ V}$, the maximum voltage (1.55 V) is still less than the oxide breakdown voltage (1.65 V) given in the device model parameters. However, the changing values of V_{gs} and V_{gd} , as well as v_d modulate the channel resistance and change the attenuation level of the actuated varistor depending on the input power level. This limits the power handling capability of the actuated varistor and the attenuator (Section 4.4.2).



V _c	0/1.2 V
NMOS length	0.12 μm
NMOS width	2.1 μm
C _p	30 fF
L _s	90 pH
L _p	130 pH
R _c	20 KΩ

Figure 4.7 Schematic of the distributed 10–50-GHz step attenuator with the parasitics of the nMOS varistor.

The parasitics of the nMOS varistor are also shown in Fig. 4.7. The series capacitance, $C_{ds} < 0.5$ fF consists of the gate-drain, gate-source and drain-source parasitic capacitances and is negligible up to 50 GHz. The source and drain junction capacitances (C_{jd} and C_{js}) are about 4 fF. The t-lines of the distributed step attenuator is designed to absorb C_{jd} and C_{js} as shown in the next section. Each nMOS device is closely surrounded by a large substrate contact to reduce the substrate coupling between the devices and minimize the resistance from the source/drain junctions to ground (R_{sub}). This result in an increase in the source/drain isolation and a decrease in the t-line loss by adding capacitive (drain) parasitics to the t-line, rather than resistive parasitics.

4.3.2 Synthetic Transmission Lines

TL_1 and TL_2 t-lines are synthesized using lumped inductors and capacitors at 35 GHz (f_o) to have electrical lengths of $\theta_1 = 22.5^\circ$ and $\theta_2 = 30^\circ$, respectively. TL_1 is synthesized using L_s , C_p and C_{jd} , and their values are calculated using the impedance and electrical length, as:

$$\sqrt{\frac{L_s}{C_p + C_{jd}} \left(1 + j \frac{\pi f_o C_{jd}^2 R_{sub}}{C_p + C_{jd}} \right)} \approx \sqrt{\frac{L_s}{C_p + C_{jd}}} = Z_o \quad (4.4)$$

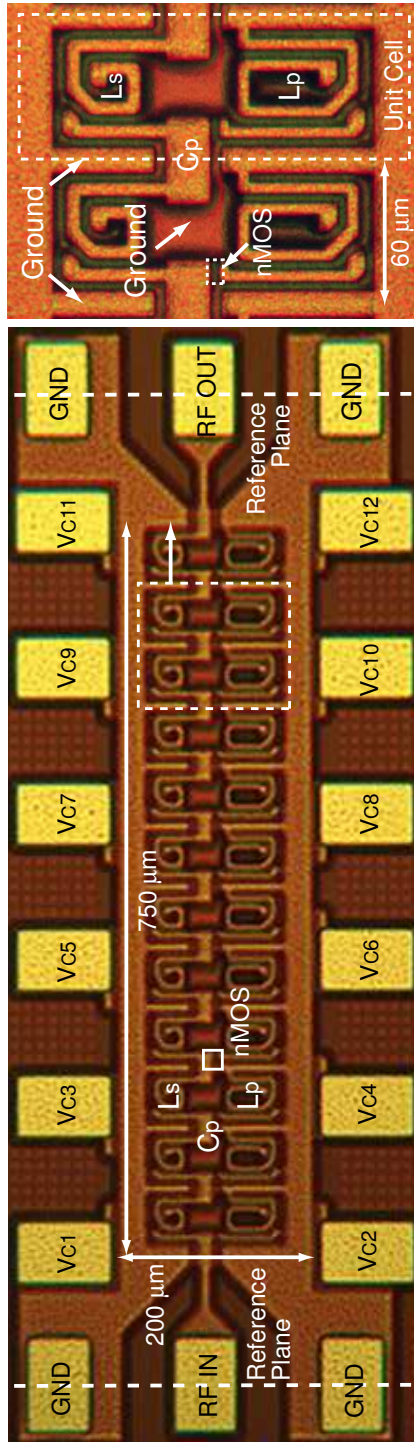


Figure 4.8 Microphotograph of the distributed 10–50-GHz step attenuator (left) and an enhanced picture of two cells (right).

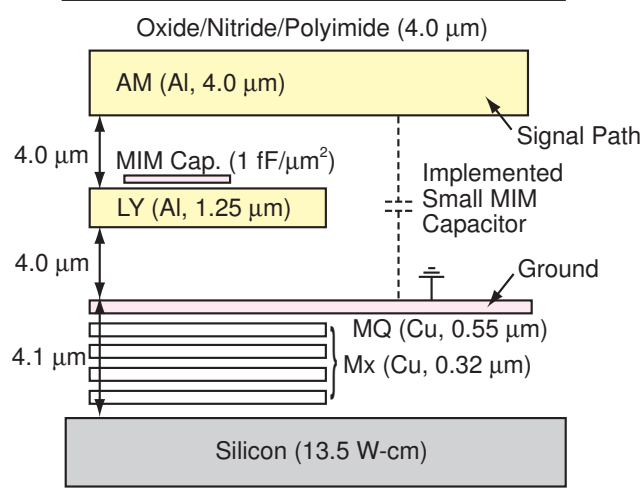


Figure 4.9 Metal layer stack of the IBM 8HP process

$$2\pi f_o \sqrt{L_S(C_P + C_{jd})} = \theta_1 . \quad (4.5)$$

Because the electrical length of synthetic TL_1 is designed to be 22.5° , its Bragg frequency is $16/\pi$ times higher than f_o [60], and TL_1 can be very accurately synthesized using a single LC section. TL_2 is a short t-line with one of its terminals shorted to ground, and can be replaced with a single inductor, L_P , using:

$$\frac{j2\pi f_o L_P}{1 - (2\pi f_o)^2 L_P C_{js}} = jZ_o \tan \theta_2 , \quad (4.6)$$

and L_P compensates for the source parasitic C_{js} .

To reduce the chip size, L_S and L_P are laid very closely to each other with ground planes between them (Fig. 4.8). The parasitic shunt capacitances of L_S and L_P are about 4 fF and 6 fF, and are taken into account together with C_{jd} and C_{js} , respectively. The third metal layer (MQ) is used as a ground plane throughout the chip except under the inductors (Fig. 4.9). C_P is a very small capacitor (30 fF) and is implemented using the capacitance between the top metal (AM) layer and the ground layer (MQ). The unit cells of L_S , L_P and C_P are optimized using full-wave electromagnetic simulations (Sonnet) and the results are cascaded in Agilent ADS¹ for the whole circuit simulation. The transitions of G-S-G pads are designed to provide matched 50-Ω input and output impedance. The total chip size is $200 \times 750 \mu\text{m}^2$ (0.15 mm^2) excluding the pads.

¹ADS, ver. 2005A, Agilent Technologies, Palo Alto, CA, 1983-2005.

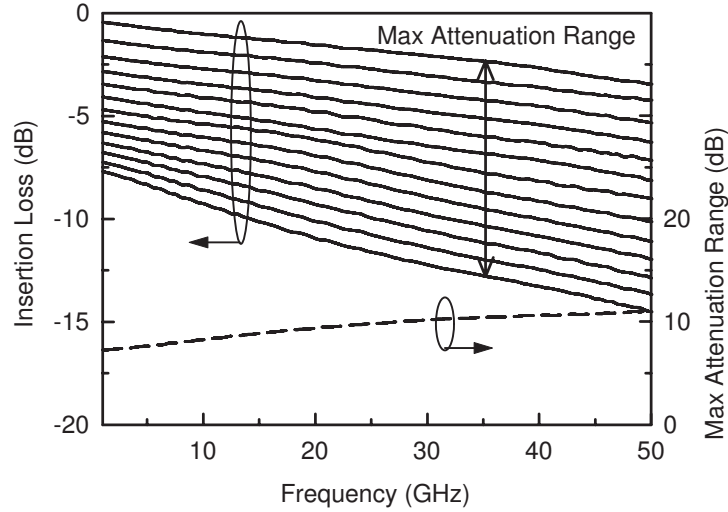


Figure 4.10 Measured attenuation of 13 different states of the distributed step attenuator.

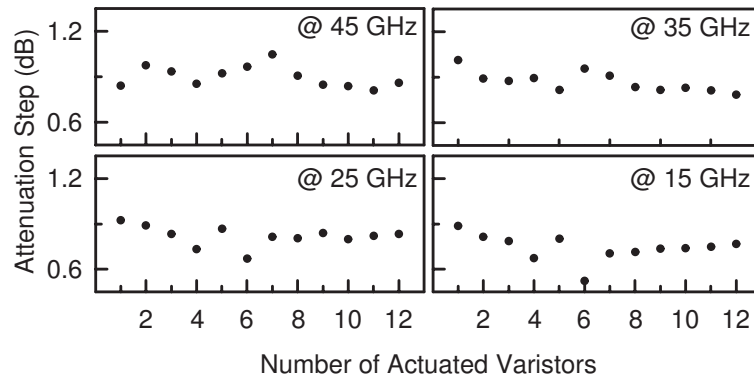


Figure 4.11 Measured attenuation step as a function of actuated varistors. At 35 GHz, the attenuation step is 0.9 ± 0.1 over all attenuation states.

4.4 Simulation and Measurement

4.4.1 Attenuation and Phase Balance

The S-parameters of the distributed step attenuator are measured on-chip using an Agilent E8364B network analyzer and an SOLT calibration to the probe tips. Twelve digital controls are biased using Table 4.1. Fig. 4.10 shows the measured insertion loss of all attenuation states. The maximum attenuation range is the insertion loss difference between the smallest and largest attenuation states. The input and output pad transitions together add about 0.4-dB insertion loss at 35 GHz and are included in the measurement. The attenuator has an insertion loss (of the minimum attenuation state) of 2.1 dB at 35 GHz which is less than the loss of a single nMOS SPST switch at 35 GHz

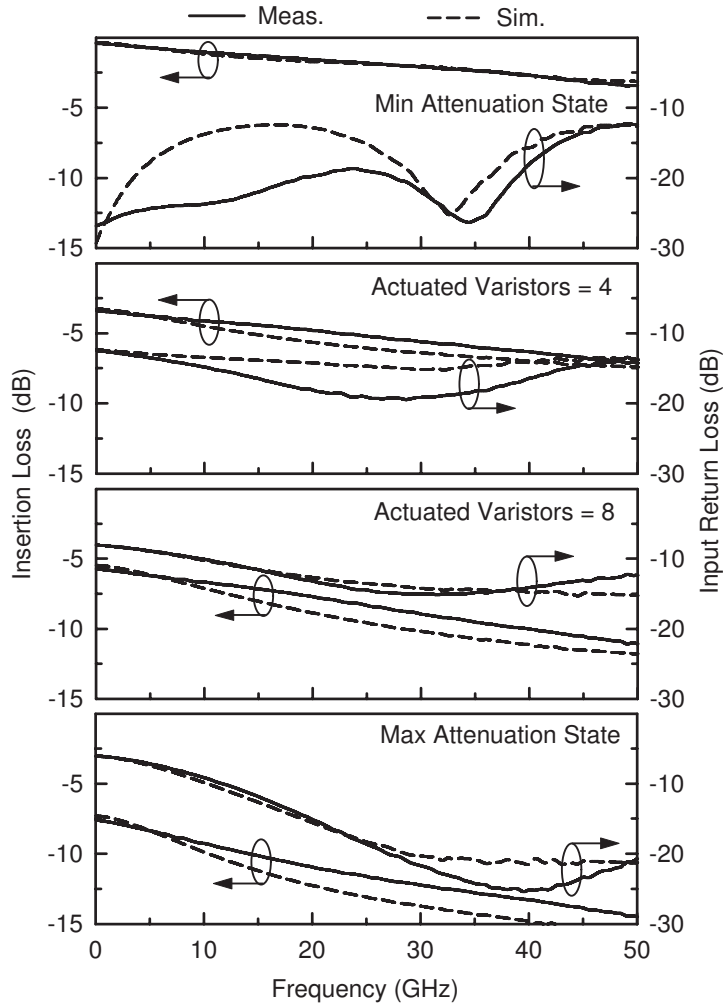


Figure 4.12 Measured and simulated insertion loss and return loss when 0, 4, 8 and 12 varistors are actuated.

(Fig. 4.2). The attenuation steps are 0.9 ± 0.25 dB and are shown in Fig. 4.11 at four different frequencies. The maximum attenuation range and the attenuation steps decrease at lower frequency because the electrical distance between the nMOS varistors becomes shorter.

Fig. 4.12 presents the measured and simulated responses of 4 different attenuation states when 0, 4, 8 and 12 varistors are actuated. The minimum loss state has a low return loss, so the synthetic t-line (TL_1) has a impedance very close to 50Ω . The measured input and output return loss of all attenuation states are shown in Fig. 4.13. The return loss is less than -13.6 dB at the designed frequency, 35 GHz, and less than -9.1 dB at 10–50 GHz. At frequencies close to DC, the varistors have zero electrical distance and the attenuator has a return loss of -6 dB when all the varistors are actuated. This is expected since the circuit becomes equivalent to 12 parallel resistors each with

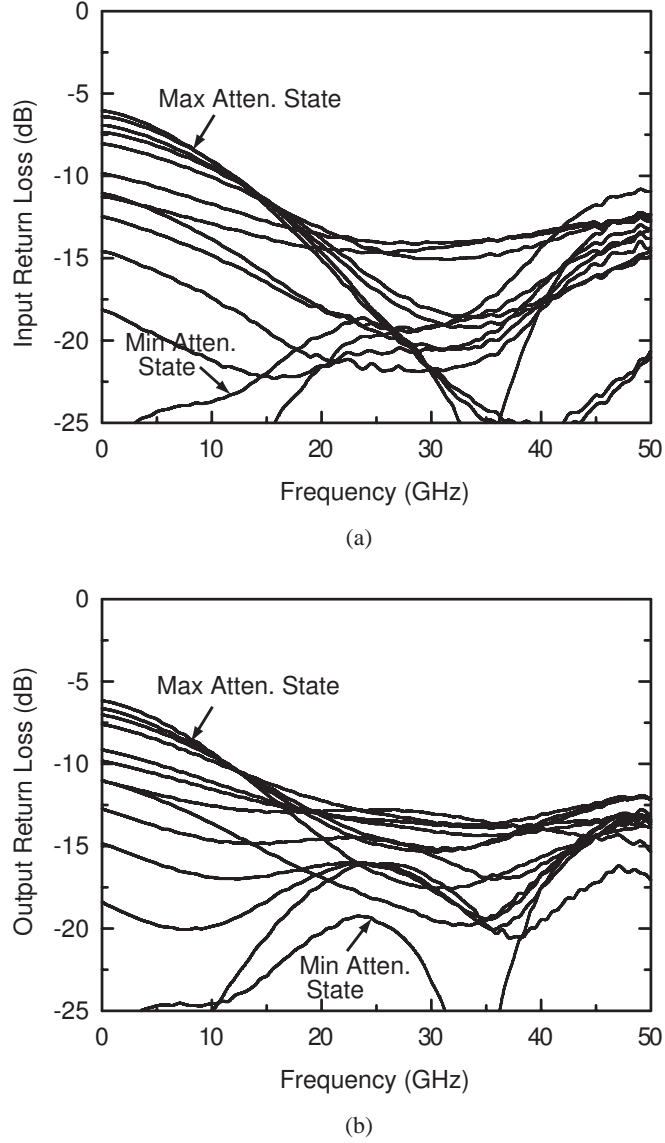


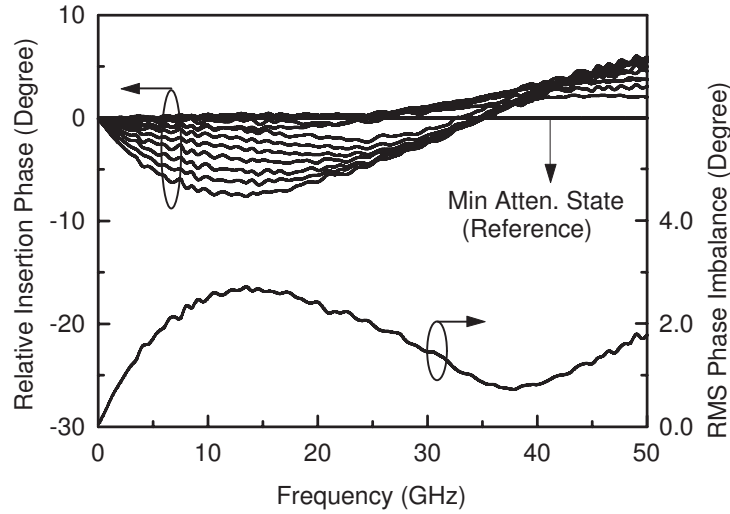
Figure 4.13 Measured (a) input and (b) output return loss of 13 different states of the distributed step attenuator.

$$R_P = 4Z_o (Z_L = Z_o/3).$$

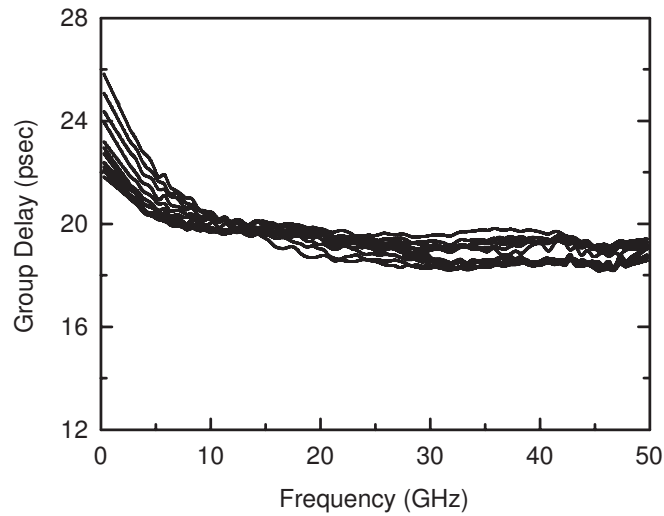
Fig. 4.14(a) shows the measured insertion phase relative to the phase of the minimum attenuation state. The maximum phase imbalance is less than 7° over the entire DC–50-GHz frequency range. The rms imbalance is calculated using the standard deviation of the insertion phase as:

$$\Delta_{rms}\Phi = \sqrt{\frac{1}{13} \sum_{i=0}^{12} \{S_{21ph,i} - \overline{S_{21ph}}\}^2}, \quad (4.7)$$

where $S_{21ph,i}$ is the insertion phase of i^{th} attenuation state and $\overline{S_{21ph}}$ is the mean of all the insertion



(a)



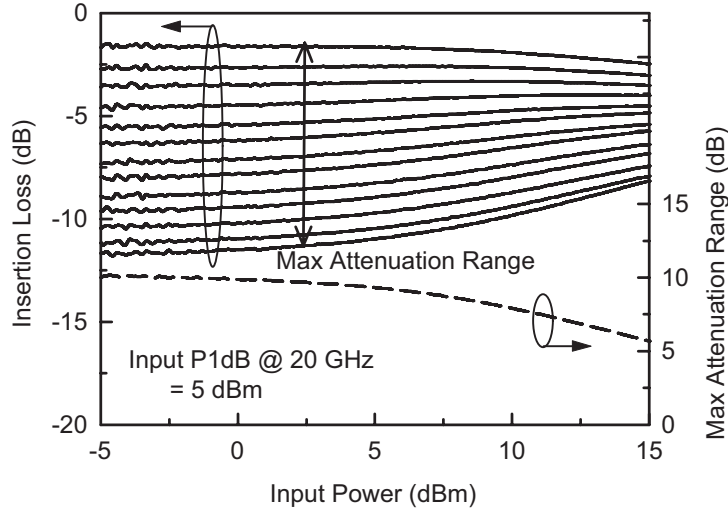
(b)

Figure 4.14 Measured (a) relative insertion phase and rms imbalance, and (b) group delay of 13 different states of the distributed step attenuator.

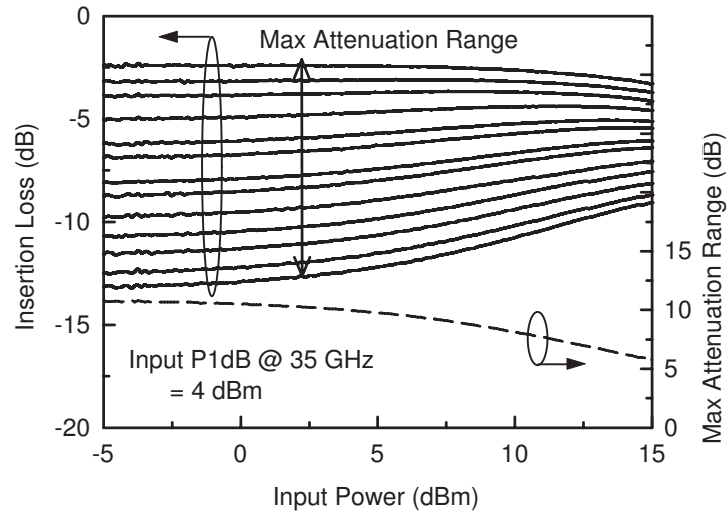
phases. The rms phase imbalance is less than 1° at 33–42 GHz, and less than 3° over the DC–50-GHz frequency range. Fig. 4.14(b) presents the group delay of all attenuation states. The group delay is about 19 ± 0.6 psec at 10–50 GHz for all attenuation states.

4.4.2 Power Handling

Fig. 4.15 shows the measured attenuation versus input power at 20 GHz and 35 GHz. As the input power increases, the attenuation increases at low attenuation states (gain compression) and



(a)

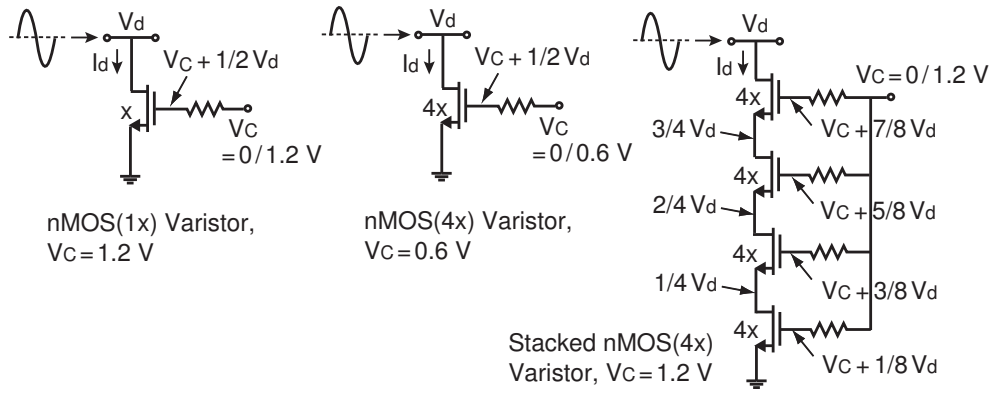


(b)

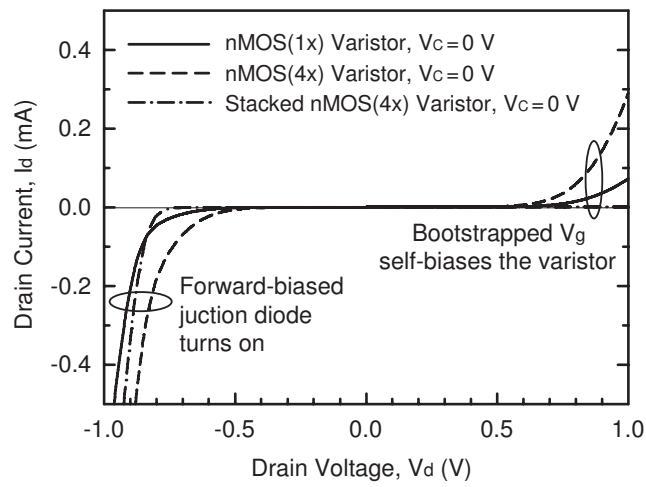
Figure 4.15 Measured power handling of the distributed attenuator at (a) 20 GHz and (b) 35 GHz.

decreases at high attenuation states (gain expansion). Because the gain expansion and compression occur based on the attenuation states, the 1-dB compression point (P_{1dB}) of the attenuator is defined as the 1-dB drop in the maximum attenuation range. The input P_{1dB} is about 5 dBm at 20 GHz, and 4 dBm at 35 GHz. The measured P_{1dB} is limited by the gain expansion of the high attenuation states (before the gain compression of the low attenuation states).

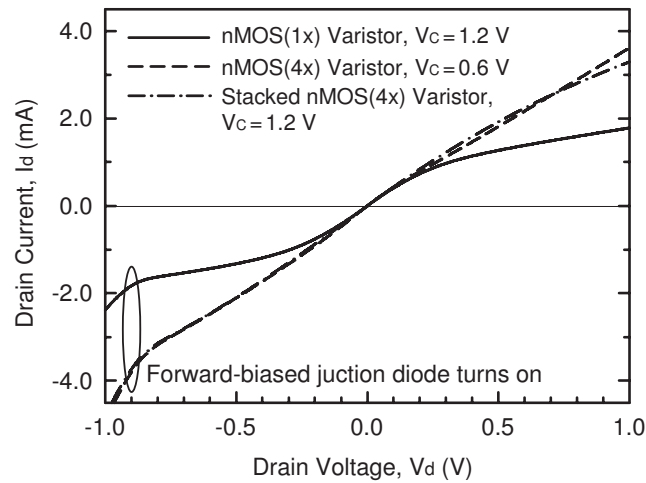
Fig. 4.16 depicts the DC-simulated drain current of the nMOS varistors as a function of the drain voltage. The drain current is obtained considering the gate node being bootstrapped by the drain voltage. The bootstrapped gate voltage levels are shown in Fig. 4.16(a). The drain junction diode



(a)



(b)



(c)

Figure 4.16 (a) NMOS varistors with the bootstrapped gate voltage, the simulated drain current for the (b) off-state and (c) actuated varistors considering the bootstrapped gate voltage.

of the nMOS transistor is forward biased and turns on when the signal voltage level is high in the negative swing ($V_d < -0.7$ V). This decreases the effective shunt resistance of the off-state varistor and results in gain compression at the low attenuation states. Also, the bootstrapped gate voltage self-biases the off-state varistor when the signal voltage level is high ($V_d > 0.8$ V) in Fig. 4.16(b). Therefore, the gain for the low attenuation states of the attenuator starts compressing at 7 dBm, which corresponds to $v_{d,peak} = 0.7$ V in a 50- Ω system.

Fig. 4.16(c) shows the drain current of the actuated nMOS varistors versus the drain voltage, and shows a possible solution to improve power handling capability. The drain current in Fig. 4.16(c) does not saturate as in the standard I_{ds} versus V_{ds} curves of a nMOS transistor since the bootstrapped gate voltage is considered. For a single nMOS(1 \times) varistor with $V_C = 1.2$ V, the channel resistance increases as V_d increases, resulting in a gain expansion for a high input power level. To increase the P_{1dB} of the attenuator, a nMOS(4 \times) varistor with $V_C = 0.6$ V can be used. For this case, the bootstrapped gate voltage compensates for the I_d saturation by increasing V_{gs} or V_{gd} , resulting in a linear I_d versus V_d characteristic. Also, a stacked nMOS(4 \times) varistor with $V_C = 1.2$ V can improve the P_{1dB} . The stacked nMOS transistor equally divides the signal voltage (Fig. 4.16(a)), and the varistor shows a linear I_d versus V_d characteristic.

Using these linearity-improved varistors, the P_{1dB} of the distributed step attenuator can be increased up to the RF power level where the gain of the minimum attenuation state is compressed by 1 dB due to the forward biased junction diode. However, the nMOS transistors of these varistors are 4 \times larger for the same total shunt resistance (200 Ω), and have 4 \times higher parasitic capacitances. This results in a larger insertion loss for the minimum attenuation state of the attenuator since the drain junction capacitance cannot be completely absorbed in the synthetic t-line due to the substrate resistance (R_{sub} in Fig. 4.7). Therefore, the linearity-improved varistors should be used only in the front cells of the distributed step attenuator where the actuated varistor needs to handle more power, and the standard nMOS(1 \times) varistors should be used in the later cells.

4.5 Summary

The theory, design and measurement of a low-loss distributed CMOS step attenuator are presented. Twelve nMOS varistors are spaced $\lambda/16$ apart in a 50- Ω synthetic t-line. The attenuation is

controlled by the nMOS varistors and the nMOS parasitics are absorbed in the synthetic t-line. The maximum attenuation range is 11 dB at 35 GHz with a minimum/maximum attenuation state loss of 2.1/13.0 dB at 35 GHz. The return loss is less than -9 dB at 10–50 GHz. The phase imbalance is minimized with shunt inductors and the rms phase imbalance is less than 3° for the entire operating bandwidth. The total chip size is 0.15 mm^2 excluding pads and the input P_{1dB} of the maximum attenuation range is 4 dBm at 35 GHz. The power handling can be improved using stacked nMOS varistors.

Chapter 5

Ka-Band Low-Loss and High-Isolation Switch in 0.13- μm CMOS

5.1 Introduction

Switches are one of the important building blocks in RF/millimeter-wave systems. Single-pole-single-throw (SPST) and single-pole-double-throw (SPDT) switches can be used for various applications such as transmit/receive modules, variable attenuators and phase shifters, wide-band pulse generators, and multi-standard communication systems. The switches are commonly designed using III-V semiconductor-based transistors or diodes. However, as CMOS technology is scaled down and adopted for many RF integrated systems, CMOS transistor-based switches has become great candidates for low loss designs at DC–5 GHz [61–65]. CMOS switch design above 10 GHz is still challenging due to a high insertion loss and low isolation, as well as relatively low power handling capability [66–69]. Therefore, CMOS switches for millimeter-wave frequencies are not reported much even though CMOS integrated circuits have been developed for millimeter-wave systems [70, 71].

The main limitation of CMOS transistors when used as a switch is the junction diode between the source/drain node, and the substrate (Fig. 5.1). The junction diodes increase the signal loss and also limit the signal voltage swing. Since the impedance of the junction capacitance is very low at millimeter-wave frequencies, the substrate resistance network (R_{sub}) from the junction to the substrate ground is also an important issue [72].

This chapter presents designs and measurements of Ka-band single-pole-single-throw (SPST) and single-pole-double-throw (SPDT) 0.13- μm CMOS switches with careful consideration to the substrate resistance network. Designs based on series and shunt switches on low and high substrate resistance networks are presented. It is found that the shunt switch and the series switch with a high substrate resistance network have a lower insertion loss than a standard designs. The shunt SPST

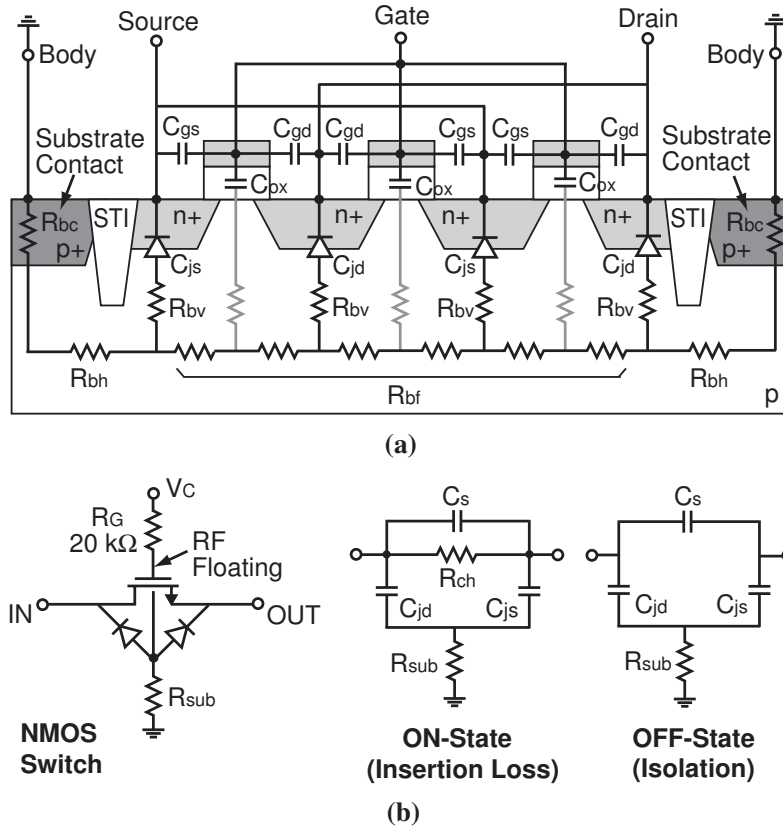


Figure 5.1 (a) Cross sectional view and equivalent circuit model of nMOS transistor and (b) schematic of a nMOS switch and its simplified small-signal circuit model of on and off states.

switch shows an insertion loss of 1.0 dB and an isolation of 26 dB at 35 GHz. The series SPDT switch with a high substrate resistance network shows excellent performance with 2.2-dB insertion loss and >32-dB isolation at 35 GHz, and this is achieved using two parallel resonant networks. The series-shunt SPDT switch using deep n-well nMOS transistors for a high substrate resistance network results in an insertion loss and isolation of 2.6 dB and 27 dB, respectively at 35 GHz. For series switches, the input 1-dB compression point (IP_{1dB}) can be significantly increased to ~ 23 dBm with the use of a high substrate resistance design. In contrast, IP_{1dB} of shunt switches is limited by the self-biasing effect to 12 dBm independent of the substrate resistance network. The chapter shows that, with good design, several 0.13- μm CMOS design can be used for state-of-the-art switches at 26–40 GHz.

5.2 CMOS Switches

5.2.1 CMOS Transistor and Substrate Network

Fig. 5.1(a) shows a simplified equivalent circuit of a nMOS transistor with three gate fingers. The nMOS transistor is a 4-port device with a body node connected to the substrate contact, as well as the gate, source, and drain nodes. C_{js} and C_{jd} are junction capacitances of the source and drain junction diodes, and C_{gs} and C_{gd} are the parasitic capacitance between the gate, and the source and drain. There are substrate-related resistances between the source/drain junction, and the body node. This substrate resistance networks include the vertical and horizontal resistances (R_{bv} and R_{bh}), the resistance between the junctions of gate fingers (R_{bf}), and the substrate contact resistance (R_{bc}).

The substrate resistance network significantly affects the transistor characteristics at millimeter-wave frequencies, and depends on many factors such as size and distance of substrate contacts, transistor size, number of gate fingers, and even nearby circuit elements [42, 73]. Because these factors are related to a specific circuit layout, the substrate resistance network is not usually modeled in a CMOS process. Recent transistor models provide simplified model parameters for the substrate resistance networks and the parameters can be used for modeling a transistor pre-laid out with substrate contacts [74]. However, the simplified model can be inaccurate and cannot take into account nearby circuit elements. Computing a distributed network of the substrate resistance networks has been tried, but takes a long simulation time or is limited to simple layouts [75–77]. Therefore, one way of minimizing the uncertainty in the substrate resistance network is to design circuits with either a very low (minimizing) or very high (maximizing) substrate resistance network.

5.2.2 CMOS Switch Model

A nMOS transistor can be used as a switch by controlling the gate voltage, and a gate resistor, $R_G = 20 \text{ k}\Omega$, is required in order to prevent signal leaking and oxide breakdown. The simplified equivalent circuit of the nMOS switch is shown in Fig. 5.1(b). C_s is the series capacitance due to C_{gs} and C_{gd} , and R_{ch} is the on-state channel resistance. R_{sub} is the resistance due to R_{bv} , R_{bh} , R_{bf} and R_{bc} . This single resistor model for substrate resistance network has been shown to be accurate up to 10 GHz. Three or five resistor models can represent the substrate resistance network more

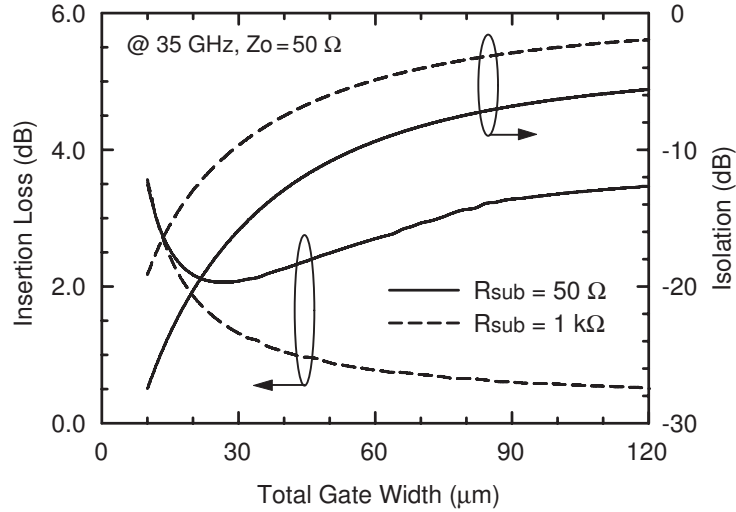


Figure 5.2 Simulated insertion loss and isolation of an intrinsic nMOS switch at 35 GHz versus the gate width with a referenced port impedance of 50Ω .

accurately [78–80], but the resistance values of these models depend on the layout and cannot be provided in a transistor model.

To improve the insertion loss of a nMOS switch, R_{ch} of the nMOS transistor is usually reduced by enlarging the gate width even though the isolation is sacrificed. However, the enlarged junction capacitances (C_{js} and C_{jd}) also increase the capacitive coupling to the substrate, resulting in an increase of the signal loss, especially above 10 GHz. This means that there is an optimum value for the gate width in order to minimize the insertion loss at a given frequency and port impedance [44]. Fig. 5.2 shows that, in the case of $R_{sub} = 50 \Omega$, the insertion loss at 35 GHz is minimized when the gate width is 20–26 μm . When R_{sub} is much higher than the port impedance ($R_{sub} = 1 \text{ k}\Omega$, $Z_o = 50 \Omega$), the insertion loss keeps decreasing as the gate width is enlarged even to $>120 \mu\text{m}$. This is because the common node of C_{js} and C_{jd} is floating, and C_{js} and C_{jd} couple the RF signal between the input (drain) and output (source) without leaking to the substrate. However, for the same reasons, the off-state isolation is significantly worse than that of the nMOS switch with a low R_{sub} .

5.3 SPST and SPDT Switch Design

Various SPST and SPDT switches are designed using a $0.13\text{-}\mu\text{m}$ BiCMOS process (IBM 8HP) for Ka-band frequencies ($f_o = 35 \text{ GHz}$). For the CMOS transistors, the BSIM4v2 model is provided

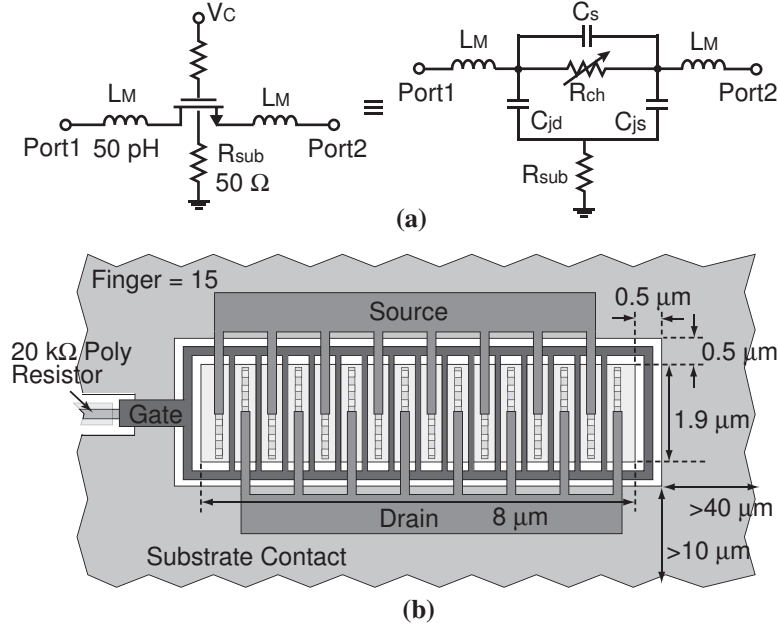


Figure 5.3 (a) Schematics of the low- R_{sub} series SPST switch and (b) nMOS transistor layout for the switch.

by the design kit. However, the substrate resistance network is not modeled, and the single resistor model (R_{sub}) is left to be defined by the user [43]. At Ka-band frequencies, this R_{sub} value has to be considered carefully for a low-loss switch design because of the low impedance of the junction capacitance (C_{js} and C_{jd}).

5.3.1 Low- R_{sub} Series SPST Switch

To reduce the signal loss due to C_{js} and C_{jd} , inductors (L_M) can be placed at the input and output of a nMOS switch as a matching circuit (Fig. 5.3(a)). If $R_{sub} \approx 0$, one can increase the gate width higher than the optimum value of Fig. 5.2, and match C_{js} and C_{jd} using series inductors. However, R_{sub} is roughly estimated to be 30–100 Ω even with a very large substrate contact, and therefore a lossless matching network is not possible due to the low circuit quality factor ($Q = 1/\omega R_{sub} C_{js}$). With an estimation of $R_{sub} \approx 50 \Omega$, L_M and the gate width for minimum insertion loss are found to be 50 pH and 28 μm ($N_f = 15$, $w = 1.9 \mu\text{m}$), respectively. For $R_{sub} \approx 50 \Omega$, the transistor is entirely surrounded by a large substrate contact ($90 \times 25 \mu\text{m}^2$) placed very closely to the transistor (Fig. 5.3(b)). The simulated insertion loss and isolation are 2.6 dB and 10 dB, respectively. The isolation of the series SPST switch is lower than the isolation of intrinsic nMOS switch of Fig. 5.2

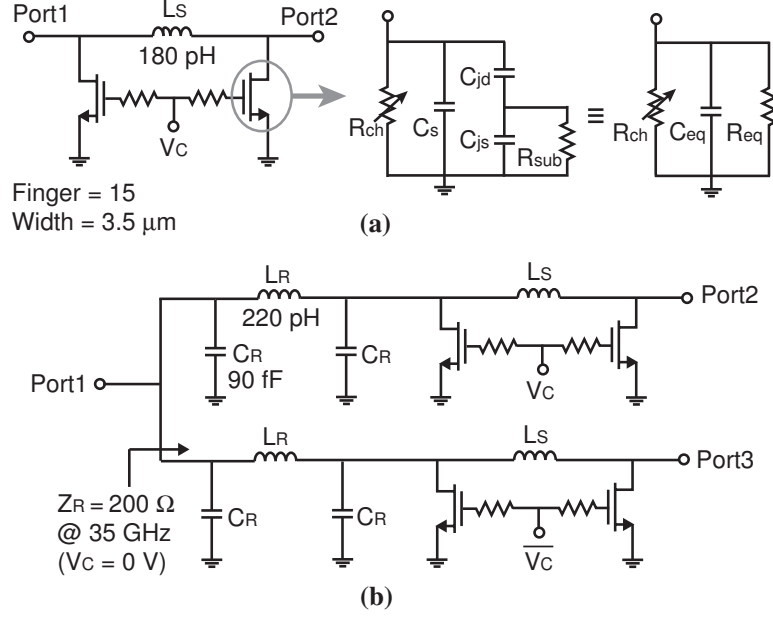


Figure 5.4 Schematics of the low- R_{sub} shunt (a) SPST and (b) SPDT switches.

since L_M matches C_{js} and C_{jd} also in the off-state. To increase the switch isolation, a shunt switch is often used together with a series switch, especially for a SPDT switch. However, the insertion loss of the series-shunt switch cannot be lower than that of the series SPST switch.

5.3.2 Low- R_{sub} Shunt SPST and SPDT Switches

NMOS switches can be used as shunt elements for a low-loss SPST switch, and the circuit is shown in Fig. 5.4(a). C_{eq} and R_{eq} of the equivalent circuit are calculated using:

$$R_{eq} = \frac{4\omega^2 R_{sub}^2 C_j^2 + 1}{\omega^2 R_{sub} C_j^2} > \frac{4}{\omega C_j} \quad (5.1)$$

$$C_{eq} = \frac{C_j + 2\omega^2 R_{sub}^2 C_j^3}{4\omega^2 R_{sub}^2 C_j^2 + 1} + C_s, \quad (5.2)$$

where $C_j = C_{js} = C_{jd}$. R_{eq} is usually large ($>500 \Omega$) unless the transistor is very wide. Therefore, the gate width of the shunt switch can be chosen to be larger than that of the series switch, and the shunt capacitance, C_{eq} can be matched using inductors. Π -type matching with two shunt switches and a series inductor (L_S) is preferred than T-type matching with one shunt switch since it requires only one inductor and provides a higher isolation. The isolation of Π -type matching with two nMOS ($1 \times$)

switches is higher by ~ 10 dB at 35 GHz than that of T-type matching with a twice wider nMOS($2\times$) switch due to the impedance transformation of the Π -network (L_S and C_{eq} 's). In this shunt switch design, R_{sub} is estimated to be 50Ω , and the gate width of $52.5 \mu\text{m}$ ($N_f = 15$, $w = 3.5 \mu\text{m}$) is chosen to provide >25 dB isolation at 35 GHz.

Fig. 5.4(b) shows a SPDT switch design using two shunt SPST switches. C_R - L_R - C_R Π -network acts as a $\lambda/4$ transmission line and transforms the low impedance of the off-state SPST switch to a high impedance ($Z_R \approx 200 \Omega$) at the common node of the SPDT switch. The impedance, Z_R is limited by the input impedance of the off-state SPST switch. The simulated loss of the Π -network is <0.5 dB and is lower than the loss of the low- R_{sub} series switches. Therefore, at millimeter-wave frequencies, it is better to use $\lambda/4$ -based designs for relatively narrow-band applications rather than a traditional low- R_{sub} series-shunt SPDT design.

5.3.3 High- R_{sub} Series SPST and SPDT Switches

Even if the capacitive coupling due to the junction capacitances of the nMOS switch can be minimized by increasing R_{sub} , it was shown in Section 5.2.2 that the high- R_{sub} design significantly decreases the series switch isolation (see Fig. 5.2). In this case, the isolation can be greatly improved by adding an inductor between the source and drain nodes which resonates with the total series capacitance, C_t (see Fig. 5.1)

$$C_t = \frac{C_{js} \times C_{jd}}{C_{js} + C_{jd}} + C_s \quad (5.3)$$

at a desired frequency [72, 81].

Fig. 5.5(a)(b) presents the high- R_{sub} series SPST switch at 35 GHz. In order to increase R_{sub} , the substrate contact resistance (R_{bc}) of Fig. 5.1(a) is increased by adopting a very small substrate contact ($0.28 \times 5 \mu\text{m}^2$) close to the nMOS transistor. The SPST switch consist of two series nMOS transistors with a large gate width of $100 \mu\text{m}$ ($N_f = 21$, $w = 4.8 \mu\text{m}$). The resonant inductors ($L_1 = 380$ pH, $L_2 = 340$ pH) are connected between the source and drain to increase the isolation. L_1 and L_2 have different sizes, and resonate with the series capacitances at two different frequencies (34 GHz and 36 GHz) to increase the total isolation bandwidth. For the same insertion loss, two large nMOS($2\times=100 \mu\text{m}$) switches in series are preferred than one small nMOS($1\times=50 \mu\text{m}$)

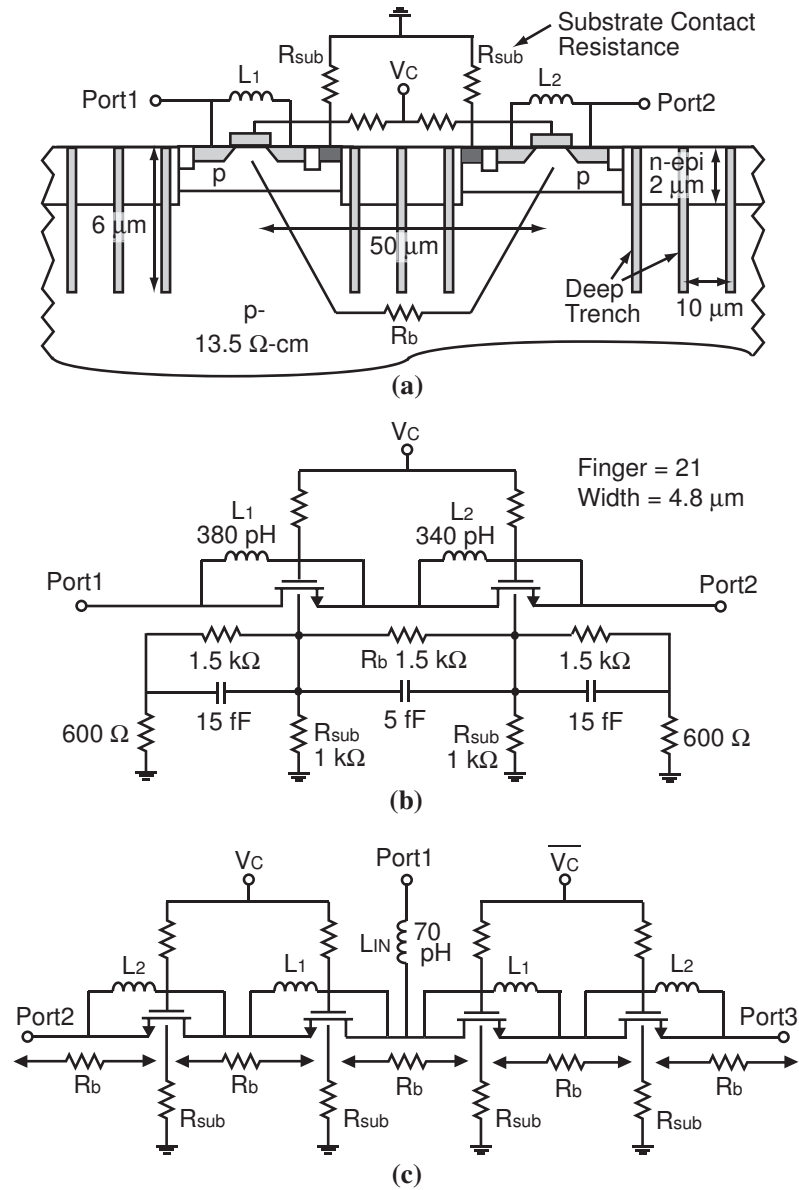


Figure 5.5 (a) Cross sectional view and (b) schematic of the high- R_{sub} series SPST switch, and (c) schematic of the high- R_{sub} series SPDT switch.

switch since L_1 and L_2 values are more reasonable and the total isolation bandwidth is wider.

The nMOS transistors are separated $50\ \mu\text{m}$ away for high isolation between the junctions (Fig. 5.5(a)). Because R_{sub} is very high, the substrate resistance, R_b between the junctions of the two nMOS transistors also has to be as high as possible. To increase R_b , the nMOS transistors are surrounded by an isolation moat (n-type epitaxial layer) and deep trenches. The isolation moat and deep trench have a thickness of $2\ \mu\text{m}$ and $6\ \mu\text{m}$, respectively, and also prevent the nMOS transistors from latch-up and coupling with other circuits around the switch. The simulated insertion loss and

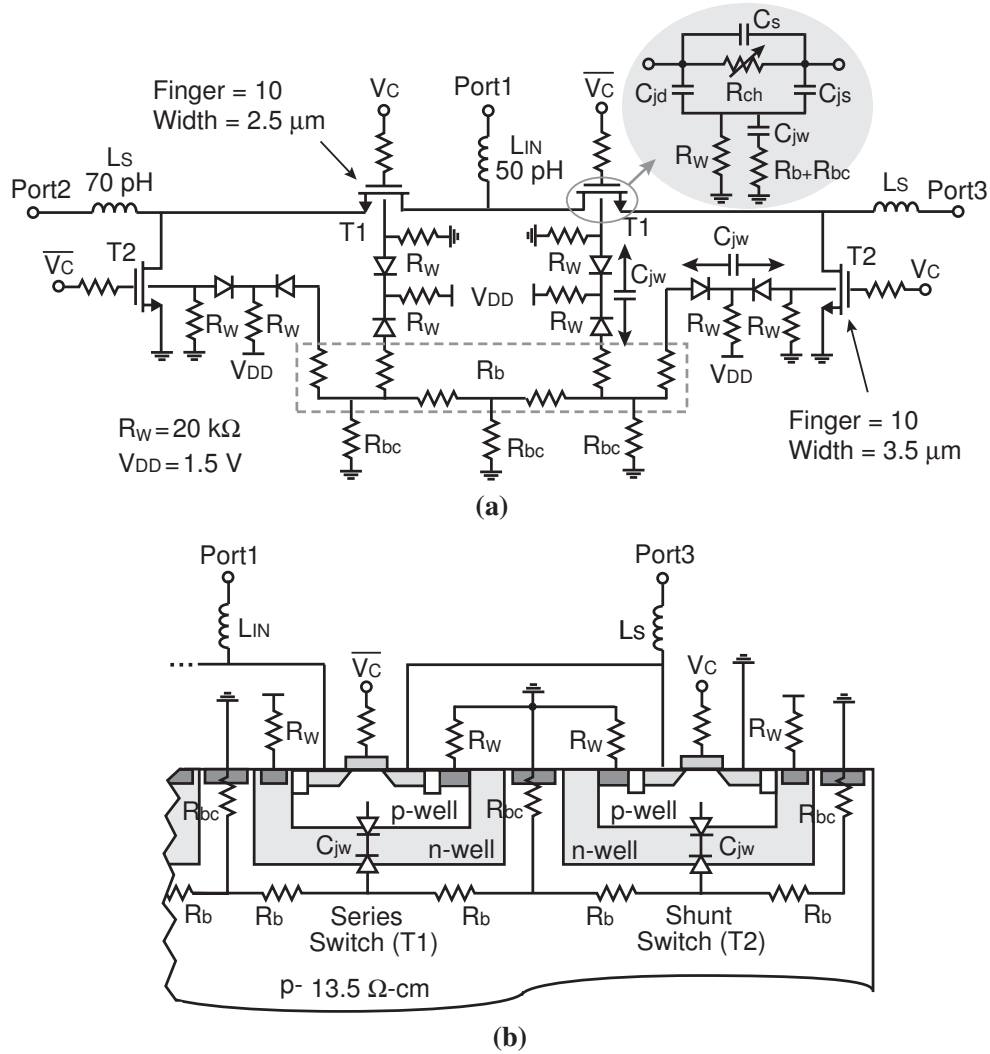


Figure 5.6 (a) Schematic and (b) cross sectional view of the series-shunt SPDT switch using deep n-well nMOS transistors (half-circuit is shown).

isolation at 35 GHz are 1.9 dB and >30 dB with the assumption of $R_b = 1$ k Ω . The high- R_{sub} series SPDT switch is also implemented using two SPST switches (Fig. 5.5(c)). The shunt capacitance of the capacitive T-junction is matched using a meander line inductor, $L_{IN} = 70$ pH.

5.3.4 High- R_{sub} Deep N-Well Series-Shunt SPDT Switch

Another way to obtain a high R_{sub} is with the use of a deep n-well nMOS transistor (Fig. 5.6) [65, 68]. The isolated p-well and the deep n-well are biased with large resistors ($R_W = 20$ k Ω) to 0 V and 1.5 V, respectively, to establish a reverse bias junction without decreasing R_{sub} . To increase the low isolation of the high- R_{sub} series switch, a shunt switch is also required

resulting in a series-shunt design. The SPDT switch are designed to achieve a isolation of ~ 30 dB at 35 GHz, and the series and shunt transistor sizes ($T1$ and $T2$) are optimized for the lowest insertion loss. The capacitive T-junction and the capacitance of shunt switches are matched by inductors, L_{IN} and L_S , respectively.

Even though the R_{sub} value of the deep n-well series-shunt switch is increased using R_W , the effective impedance from the source and drain junctions to ground is lower than R_W due to the junction capacitances of the deep n-well (C_{jw}). C_{jw} depends on the deep n-well area and the bias voltages, and the C_{jw} of $T1$ is about 45 fF ($j100 \Omega$ at 35 GHz) for an applied voltage of 0 V and 1.5 V for the p-well and n-well, respectively. (C_{jw} can be reduced with higher reverse bias voltages, but this requires special voltage levels.) Therefore, the effective R_{sub} value using deep n-well process is limited by C_{jw} at millimeter-wave frequencies. The effective R_{sub} value can be increased with a high R_b and R_{bc} , but the nMOS transistors and nearby circuits have to be well separated as in the case of the high- R_{sub} series switch, resulting in a relatively large chip area. To achieve a small chip area in this design, relatively good substrate contacts ($3 \times 11 \mu\text{m}^2$) are placed at both sides of the transistors for a device isolation, even though the effective R_{sub} value is lowered to $\sim 300\text{--}500 \Omega$.

5.4 Simulated and Measured Results

All inductors and interconnecting lines were simulated using full-wave EM software (Sonnet¹), and the CMOS model provided by the IBM 8HP design kit was used. The CMOS switches were measured on-chip with Agilent E8364B network analyzer using SOLT calibration to the probe tips. The pad transitions are deembedded using measured back-to-back transitions (0.18-dB loss at 35 GHz per pad transition), and the reference planes are shown in Fig. 5.7 together with the locations of nMOS transistors and the chip sizes.

5.4.1 SPST Switches

Fig. 5.8 presents the measured and simulated insertion loss and return loss of the 3 different SPST switches. Since there is no deterministic way to calculate the substrate resistance networks, R_{sub} is assumed to be 50Ω in the simulation of the low- R_{sub} series and shunt SPST switches. For the

¹Sonnet, ver. 10.53, Sonnet Software Inc., Syracuse, NY, 1986-2005.

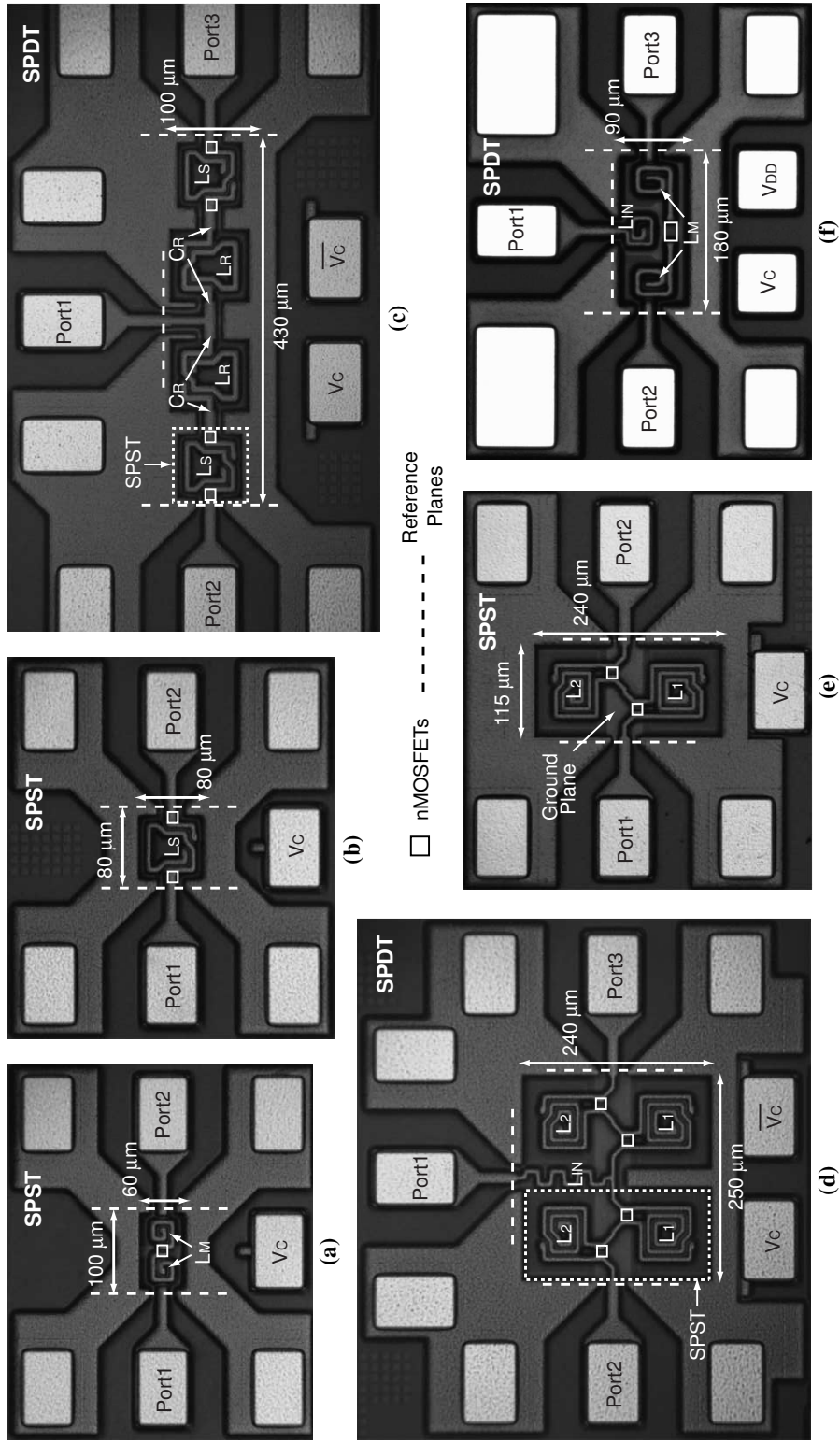
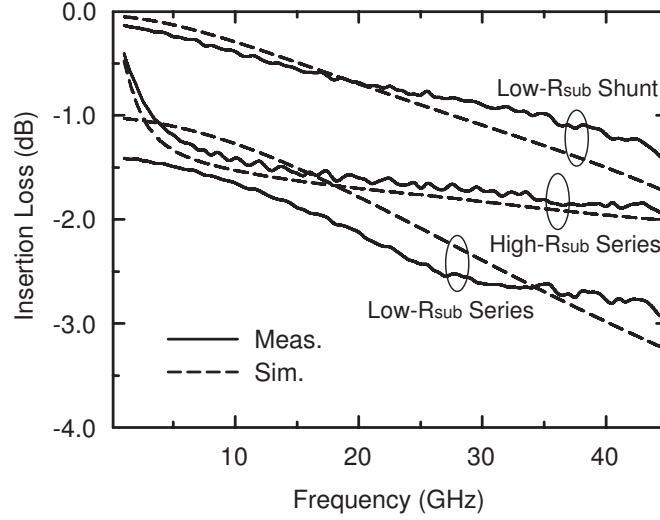
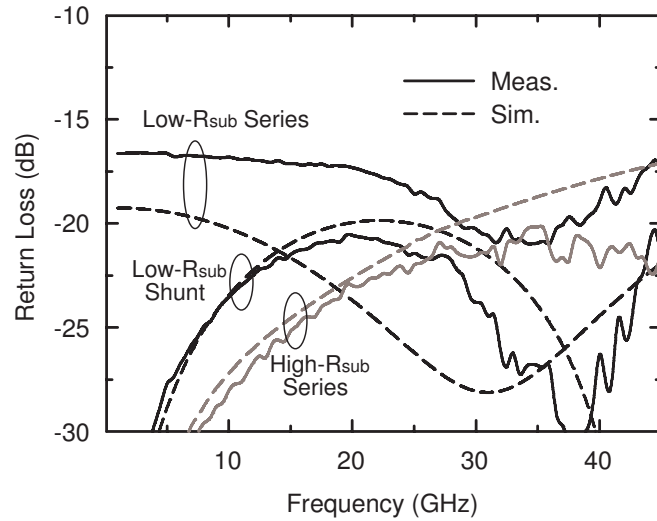


Figure 5.7 Micro-photograph of the (a) low- R_{sub} series SPST, (b) low- R_{sub} shunt SPST, (c) low- R_{sub} series SPDT, (d) high- R_{sub} series SPDT, (e) high- R_{sub} shunt SPDT, and (f) deep n-well series-shunt SPDT switches.



(a)



(b)

Figure 5.8 Measured and simulated (a) insertion loss and (b) return loss of the SPST switches.

case of the high- R_{sub} series switch, the modeled substrate resistance network is shown in Fig. 5.5(b), where the capacitance due to the deep trenches are also considered.

The measured insertion loss of the low- R_{sub} series switch is 2.6 dB at 35 GHz with a isolation of 10 dB (Fig. 5.9). The low- R_{sub} Π -shunt switch has only 1.0-dB insertion loss and 26-dB isolation at 35 GHz, and shows the state-of-the-art performance. The measured insertion loss of the high- R_{sub} series switch is 1.8 dB at 35 GHz, and each nMOS transistor switch accounts for 0.9-dB loss. The associated isolation shows the tuned resonances and is >25 dB at 34–42 GHz. This proves that the substrate resistance between the transistors is very high ($R_b \approx 1.5$ k Ω). All the SPST switches have

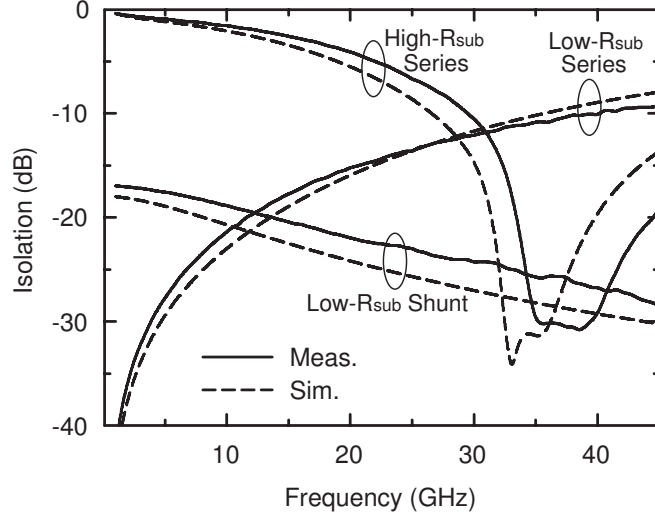


Figure 5.9 Measured and simulated isolation of the SPST switches.

a return loss < -18 dB at 35 GHz. Among the different SPST switch configurations, the low- R_{sub} Π -shunt switch has the best overall performance. As discussed in Section 5.3.2, R_{eq} of (5.1) is relatively high for the low- R_{sub} Π -shunt switch, but can be increased even higher with a high- R_{sub} design, resulting in a lower insertion loss. Simulations indicate that the high- R_{sub} Π -shunt switch results in a insertion loss improvement of 0.5 dB at 35 GHz without a degradation in isolation.

5.4.2 SPDT Switches

The measured insertion loss and return loss of the low- R_{sub} shunt SPDT switch are shown in Fig. 5.10(a). The insertion loss and return loss are 2.4 dB and -15 dB, respectively, at 35 GHz with an isolation of 31 dB (Fig. 5.12). The insertion loss of this design is a little higher than the shunt SPST switch due to the relatively low impedance of the off-state SPST switch at the T-junction ($Z_R = 200 \Omega$, see Fig. 5.4(b)). Simulations of the high- R_{sub} shunt SPDT switch also show that the insertion loss can be improved by 0.5 dB without a degradation in isolation.

The high- R_{sub} series SPDT switch with parallel resonant network has a measured insertion loss of 2.2 dB and a return loss of -21 dB, respectively, at 35 GHz (Fig. 5.10(b)). The measured isolation is >30 dB at 34–39 GHz and >25 dB at 33–43 GHz, and shows relatively narrow band performance. The measured insertion loss and return loss of the deep n-well series-shunt SPDT switch are also shown in Fig. 5.11. The insertion loss and return loss are 2.6 dB and -19 dB,

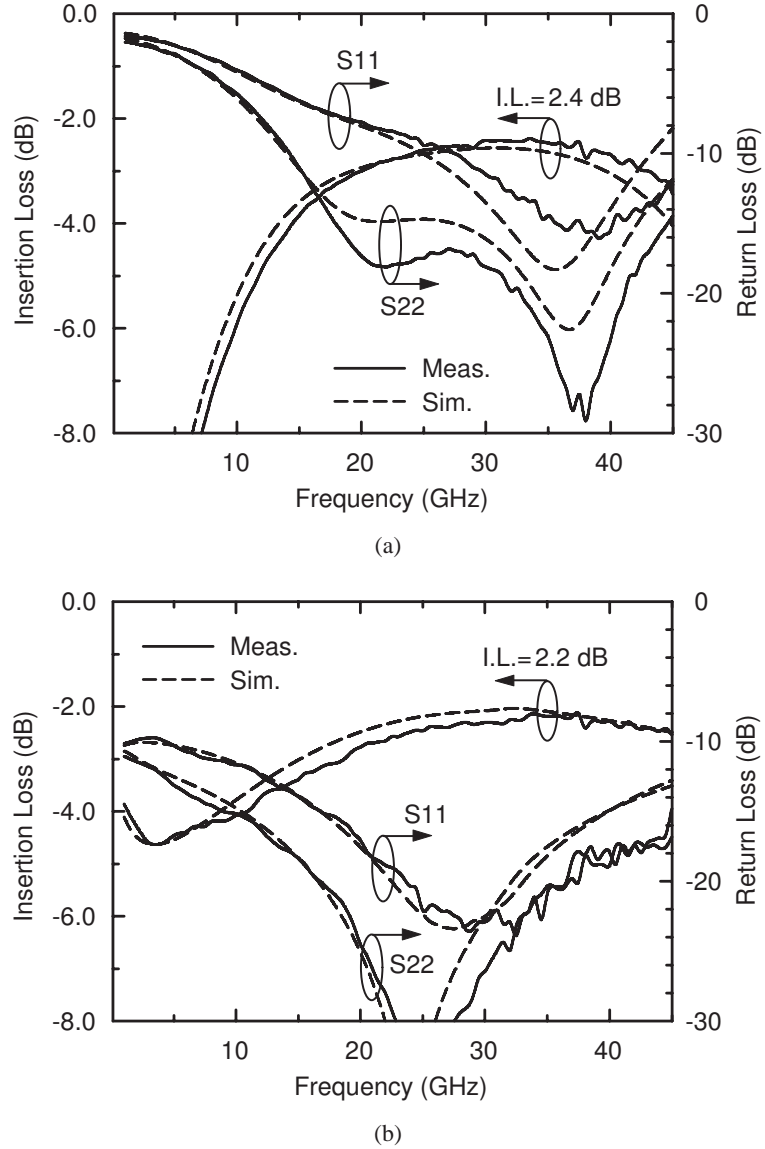


Figure 5.10 Measured and simulated insertion loss and return loss of the (a) low- R_{sub} shunt SPDT, (b) high- R_{sub} series SPDT

respectively, at 35 GHz with an isolation of 27 dB (Fig. 5.12).

The low- R_{sub} shunt and high- R_{sub} series SPDT switches have excellent insertion loss and isolation at 35 GHz, but show tuned responses, either due to the $C_R-L_R-C_R$ Π -network or the parallel resonant networks. However, the deep n-well series-shunt SPDT switch shows very wide-band performance and occupies smaller chip area ($180 \times 90 \mu\text{m}^2$). Also, the deep n-well series-shunt SPDT switch does not require isolation moats and deep trenches for the isolation with other circuits.

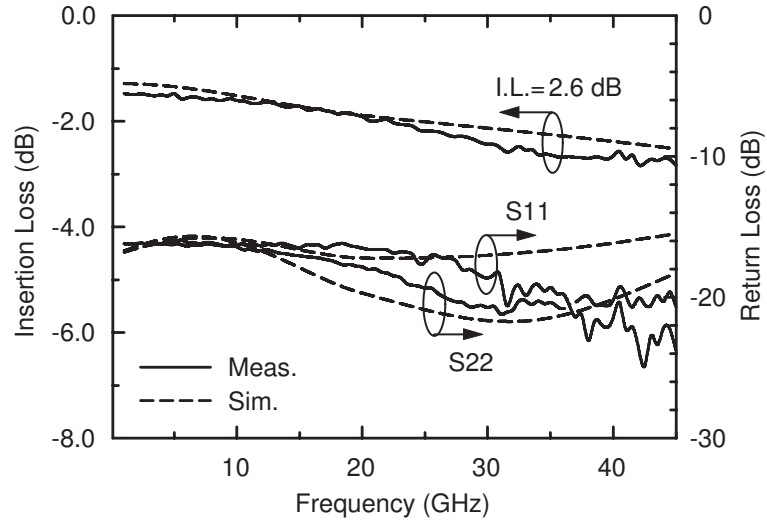


Figure 5.11 Measured and simulated insertion loss and return loss of the deep n-well series-shunt SPDT switches.

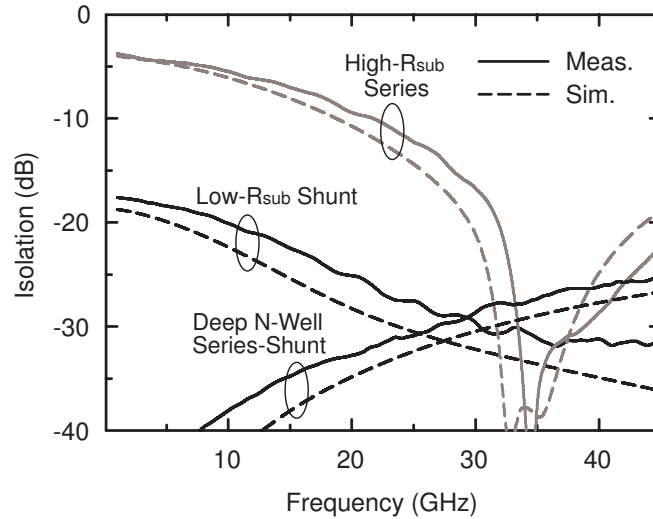
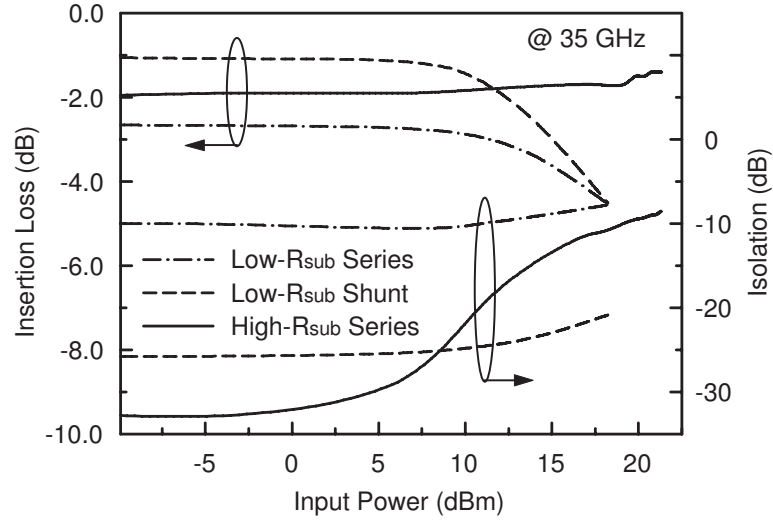


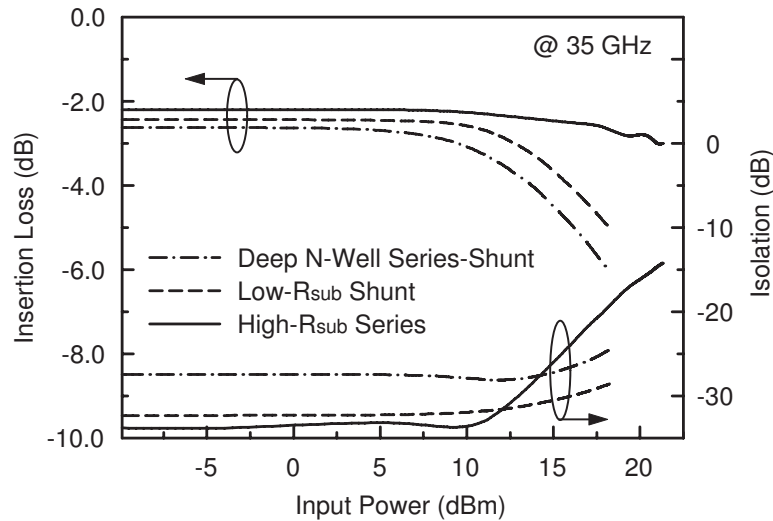
Figure 5.12 Measured and simulated isolation of the SPDT switches.

5.4.3 Power Handling and Linearity

The main limitation of the power handling capability is the junction diodes of the nMOS switches, which is forward biased when the peak signal voltage is higher than 0.7 V in the negative swing. In order to increase the power handling capability of nMOS switches, a high R_{sub} is often used and reduces the effective voltage across the junction diode [63–65]. In the case of the shunt switch, a self-biasing effect can also limit the power handling capability. The gate voltage of a nMOS switch is bootstrapped by the source and drain voltage due to the gate resistor (R_G), and



(a)



(b)

Figure 5.13 Measured insertion loss and isolation versus input power of the (a) SPST and (b) SPDT switches.

therefore the gate voltage of the shunt switch is the half of the input (drain) voltage because the source is grounded. Therefore, the shunt switch is self-biased when the input voltage is higher than twice of the threshold voltage of the nMOS transistor.

Fig. 5.13(a) shows the measured insertion loss and isolation of the SPST switches versus the input power at 35 GHz. The input 1-dB compression point (IP_{1dB}) of the low- R_{sub} series and Π -shunt SPST switches are 15 dBm and 12 dBm, respectively. The shunt SPST switch has a lower IP_{1dB} , and the gain compresses little faster due to the self-biasing effect. The gain (insertion loss) of the

Table 5.1 Performance Summary of The Ka-Band CMOS Switches.

	@ 35 GHz	I.L. (dB)	R.L. (dB)	Isol. (dB)	IP1dB (dBm)	P25dB* (dBm)	IIP3 [†] (dBm)
S P S T	Low- R_{sub} Series	2.6	-21	10	15	n/a	26
	High- R_{sub} Series	1.8	-20	32	>22	8	31
	Low- R_{sub} Shunt	1.0	-27	26	12	9	31
S P D T	High- R_{sub} Series	2.2	-21	>32	~23	16	32
	Low- R_{sub} Shunt	2.4	-15	31	14	>19	31
	Deep N-Well Series-Shunt	2.6	-19	27	12	18	26

* Maximum input power for a isolation of >25 dB.

† Measured with a input power of <-3 dBm.

high- R_{sub} series SPST switch does not compress up to 22-dBm of input power due to the high- R_{sub} value. However, the off-state gain (isolation) of the high- R_{sub} series SPST switch expands as the input power is increased. This is explained by the high isolation of this switch, which results in a large voltage between the drain (input) and source (output) of the off-state switch at an input power of >5 dBm, and the self-biasing effect.

Fig. 5.13(b) shows the measured insertion loss and isolation of the SPDT switches versus the input power at 35 GHz. The IP_{1dB} of the Π -shunt SPDT switch is 14 dBm. The IP_{1dB} of the high- R_{sub} series SPDT is about 23 dBm. The gain (insertion loss) of the high- R_{sub} SPDT switch compresses because the isolation of the off-state SPST switch decreases when the input power is increased. The gain (isolation) expansion of the high- R_{sub} series SPDT switch occurs at a higher input power than the SPST switch. This is because the SPDT switch always has a 50 Ω input impedance, but the SPST switch has a high input impedance when the switch is off. For the high- R_{sub} SPDT switch, the isolation is better than 25 dB up to an input power of 16 dBm. The deep n-well series-shunt switch has a IP_{1dB} of 12 dBm, and change little in isolation versus input power.

The input 3rd-order intermodulation intercept points ($IIP3$) are also measured at 35 GHz with a offset frequency of 1 MHz, and all the results are summarized in Table 5.1.

5.5 Summary

This chapter presents several 0.13 μm CMOS SPST and SPDT switches operating for Ka-band applications. It is found that the substrate resistance network of CMOS transistors is a very important factor for millimeter-wave CMOS switch designs. For SPST switches, the shunt topology (low and high R_{sub}) results in superior performance compared to series designs. However, the series switch isolation and power handling can be improved with the use of a high- R_{sub} design and parallel resonant networks, but at the expense of isolation bandwidth. For the SPDT case, the high- R_{sub} deep n-well switch results in very small chip area and wide-band performances. If a high power handling desired, the high- R_{sub} series SPDT switch is recommended, but results in narrow isolation bandwidth. The design procedure can be extended to 60–100 GHz using 90-nm or 65-nm CMOS transistors.

Chapter 6

A Ka-Band BiCMOS T/R Module for Phased Array Applications

6.1 Introduction

Recent developments in SiGe and CMOS mm-wave circuits have shown receiver front-ends up to 100 GHz [70, 71], a 6-18 GHz 8-element phased array receiver [32], and mm-wave transmit or receive phased arrays [12] to name a few. The phased array work has been implemented solely in either transmit or receive modes, which is acceptable for applications requiring separate transmit or receive antennas. However, many systems require full-duplex communications from the same aperture and this can be achieved with a compact T/R module. The T/R module should provide accurate gain control (0–10 dB) and phase shift (4-bit) so as to allow precise setting of the phased array main-lobe and side-lobes.

A well known T/R module topology uses a single phase shifter for both the transmit and receive paths and has been previously implemented using GaAs MMICs [82] (Fig. 6.1). The use of a single phase shifter ensures that the transmit and receive beams point to the same direction with minimal calibration. This topology allows a standard connection to an optional high-power and ultra low-noise transmit/receive III-V MMIC before connecting to the antenna.

This chapter presents a Ka-Band BiCMOS transmit/receive (T/R) module with amplitude and phase control. In the receive mode, the T/R module results in a controllable gain of 9–19 dB at 33–35 GHz, with a NF of 4 – 5 dB and an input P_{1dB} of –29 dBm. In the transmit mode, the maximum gain and output P_{1dB} are 10 dB and +5.5 dBm, respectively, and can be controlled over a 10 dB range (output P_{sat} is +8 dBm). The measured rms gain and phase error are < 0.6 dB and $< 7^\circ$, respectively, in both the transmit and receive modes using 1-bit gain compensation in the on-chip VGA. The chip is only 0.93×1.33 mm² and consumes 58 mW and 29 mW in the transmit and receive modes, respectively. To author’s knowledge, this is the first Ka-Band BiCMOS T/R module

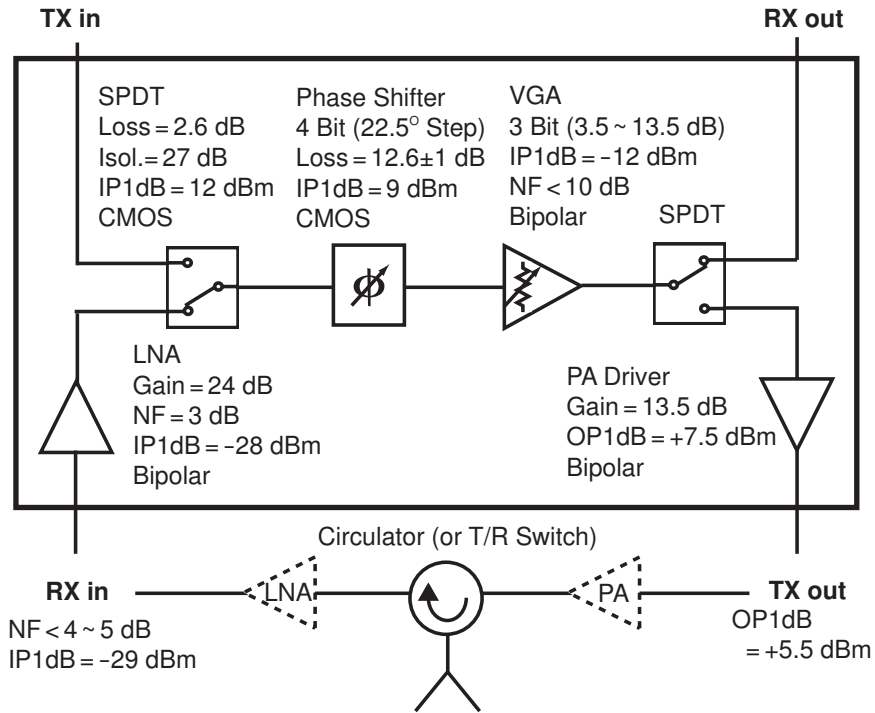


Figure 6.1 Block diagram of the BiCMOS T/R module. Values inside the T/R module box are measured separately, while values outside the T/R module are based on full chip measurements.

to-date, and with applications in satellite communications and defense systems.

6.2 Design and Implementation

The T/R module is a concatenation of individual 50Ω blocks as shown in Fig. 6.1. All amplifiers are implemented using the $0.12 \mu\text{m}$ SiGe transistors available in the IBM 8HP process, while the switches and phase shifters are implemented using the $0.12 \mu\text{m}$ CMOS transistors in the same process. The 2-stage cascode LNA is shown in Chapter 1, and has a measured gain of 24 dB without pad losses and a NF of 2.9 dB at 34–35 GHz [83]. The VGA is based on a current-steering design with a measured gain of 3.5–13.5 dB using 8 steps (3-bits), with a current consumption of 10 mA and an input P_{1dB} of -12 dBm at the maximum gain state (a differential version is presented in Chapter 2 [84]). The power amplifier driver is a two-stage class-A common-emitter design with LC matching networks (Fig. 6.2) and results in 13.5 dB gain at 34–35 GHz, and an output P_{1dB} of $+7.5$ dBm for a power consumption of 40 mW (power added efficiency of 13%), and occupies $< 0.1 \text{ mm}^2$ of space.

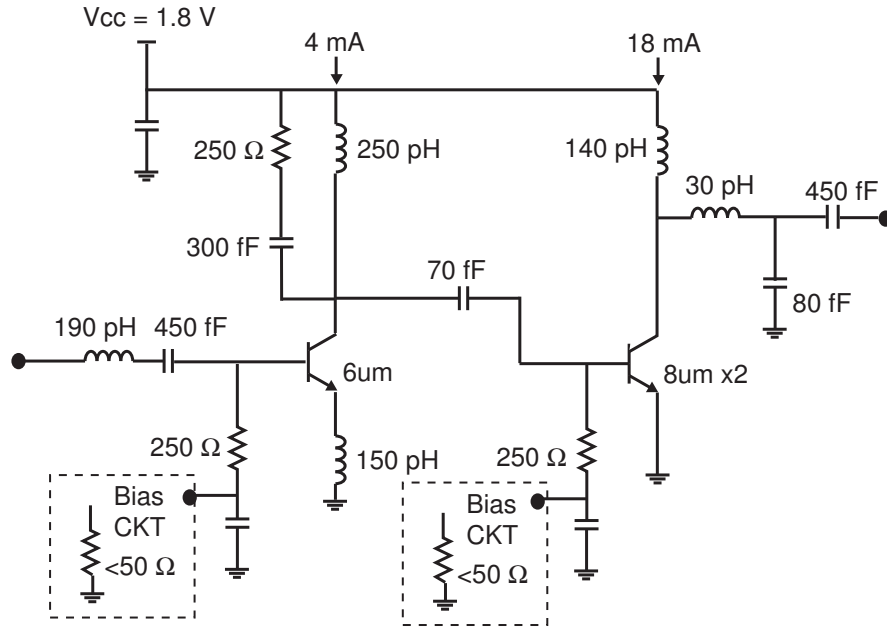


Figure 6.2 Schematic of PA driver for the fully integrated phased array T/R module.

The 4-bit phase shifter is based on switched LC networks with an insertion loss of 11.5–13.5 dB at 34–35 GHz depending on the phase state (Chapter 3), a P_{1dB} of 9–10 dBm and nano-second switching speeds [36]. The deep n-well series/shunt single-pole double-throw switches in Chapter 5 show excellent performance at 35 GHz with an insertion loss of 2.6 dB, an isolation of 27 dB and an input P_{1dB} of 12 dBm ($IIP3$ of 26 dBm). The connecting CPW transmission-lines are shielded 50 Ω G-S-G implemented in the top metal layers [36], and all input and output ports have compensated CPW pad transitions and an estimated insertion loss and reflection coefficient of 0.4–0.5 dB and < -20 dB at 30–40 GHz, respectively.

Fig. 6.3 presents the T/R module as tested. The components are placed very close to each other, and full electromagnetic simulations indicate virtually no coupling between the different element inductors (< -30 dB between the VGA and the SPDT switch, < -30 dB between the LNA and the SPDT switch and phase shifter, etc.). Also, the simulated electromagnetic coupling between the input and output ports (for example, RXin to TXout) is < -50 dB at 30–40 GHz. The simulated module gain in the transmit and receive modes are 8.8 ± 1 dB and 19.3 ± 1 dB, respectively, depending on the phase state. Both transmit and receive mode gains can be controlled over a 10 dB

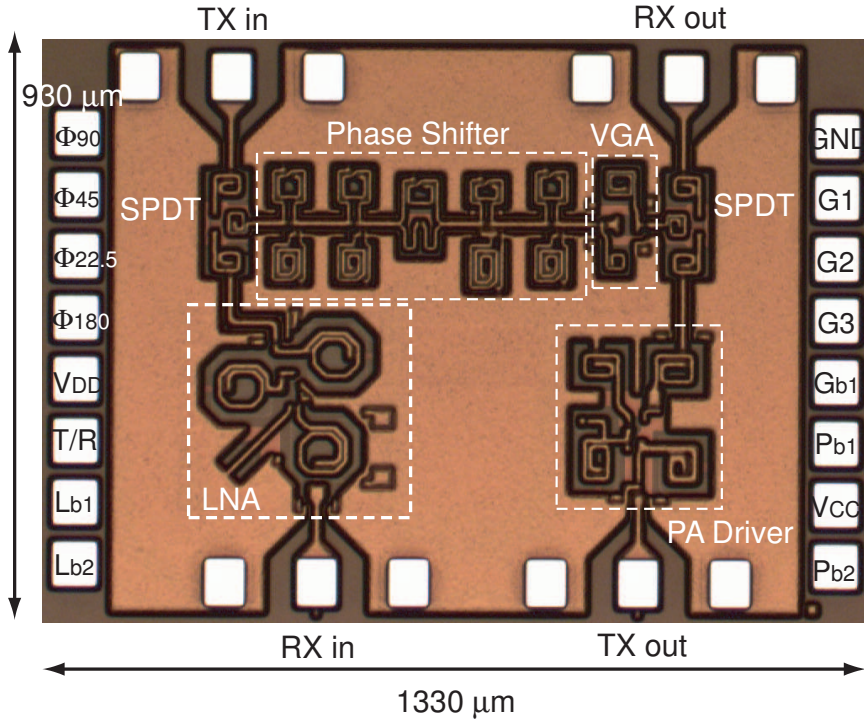


Figure 6.3 Microphotograph of the silicon BiCMOS T/R module using the IBM 8HP process.

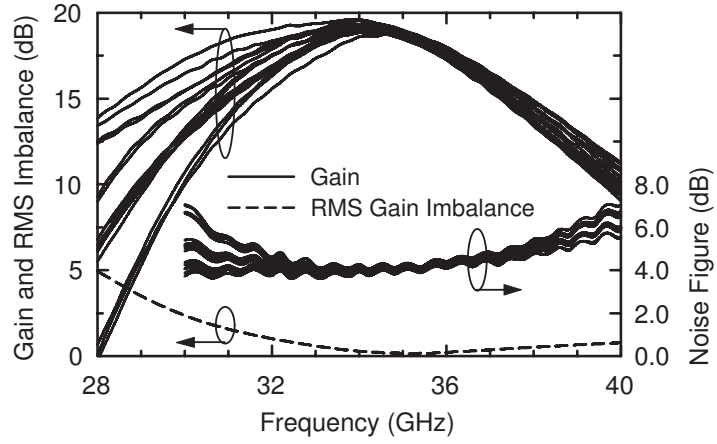
range.

$$RX = 24 - 2.6 - 12.6 + 13.5 - 2.6 - 0.4 \text{ (pads)} = 19.3 \text{ (dB)}$$

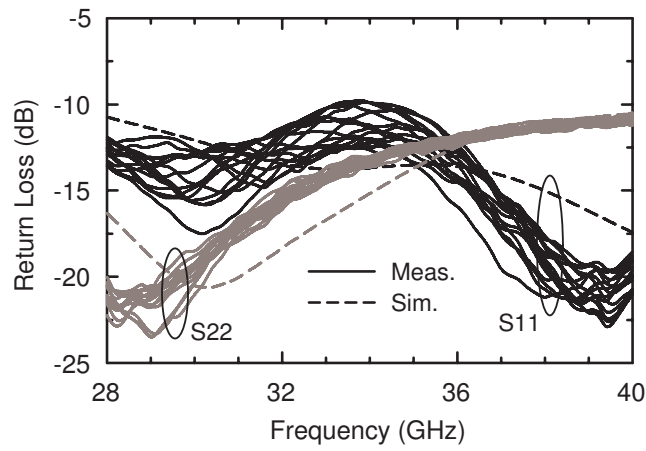
$$TX = -2.6 - 12.6 + 13.5 - 2.6 + 13.5 - 0.4 \text{ (pads)} = 8.8 \text{ (dB)}$$

6.3 Measurements

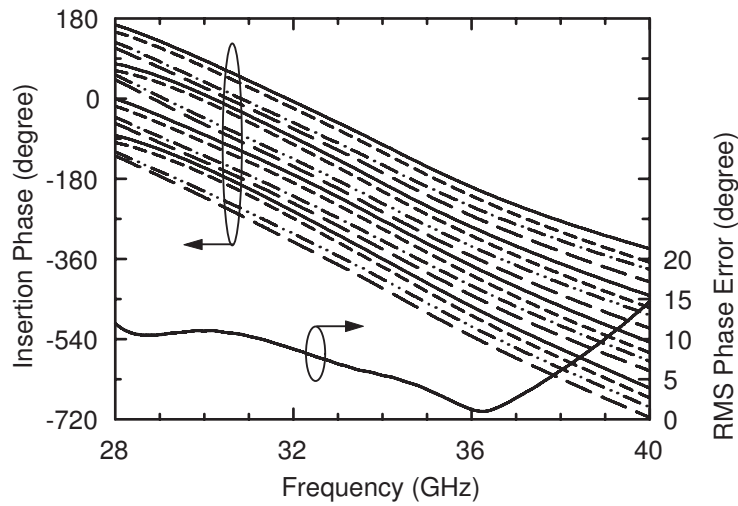
Fig. 6.4 presents the measured receive-mode S-parameters. It is seen that the T/R module results in excellent performance with a maximum small-signal receive gain of 19 ± 0.4 dB, a noise figure of < 4.3 dB at 33–35 GHz and excellent 4-bit phase response. The measured rms gain and phase error are < 0.6 dB and $< 7^\circ$ at 33–38 GHz (< 0.3 dB and $< 5^\circ$ at 34–36 GHz) with 1-bit gain compensation (that is, the VGA gain was toggled between two gain states in order to achieve a near constant gain vs. phase state). The receive gain can also be lowered by 10 dB in 8 separate steps (3-bit control) with a penalty of only 1 dB in the NF ($NF < 5$ dB at 33–35 GHz) and with virtually no change in the phase state (rms phase imbalance of $< 2^\circ$ at 30–40 GHz for a 10 dB amplitude



(a)



(b)



(c)

Figure 6.4 Measured S-parameters in the receive mode: (a) Gain and NF with VGA equalization, (b) 4-bit phase response and (c) input and output match for all phase states.

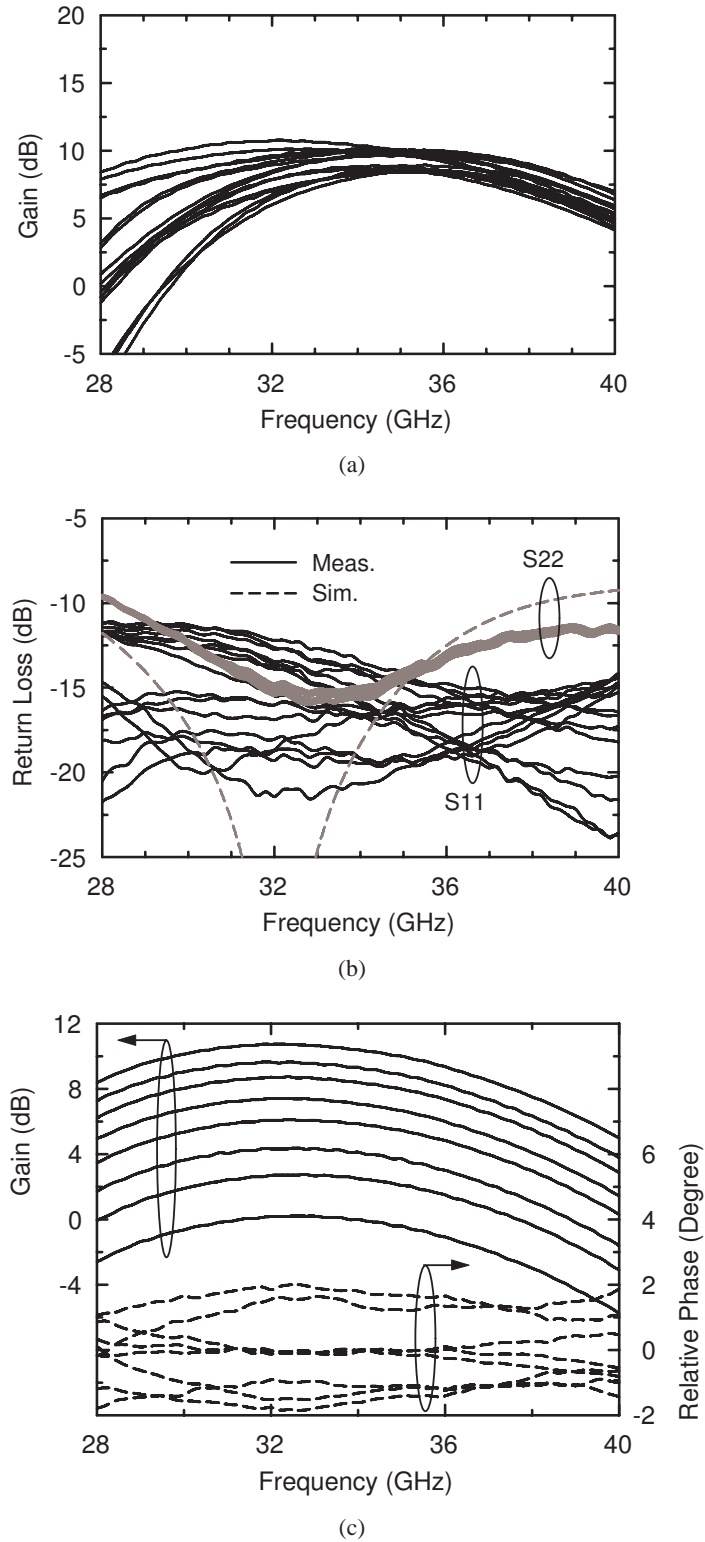


Figure 6.5 Measured S-parameters in the transmit mode: (a) Gain for the 4-bit states without VGA equalization. The peak-to-peak gain variation can be reduced to < 1 dB with the use of the VGA. (b) Input and output reflection coefficients. (c) Gain and insertion phase of 8 different gain states.

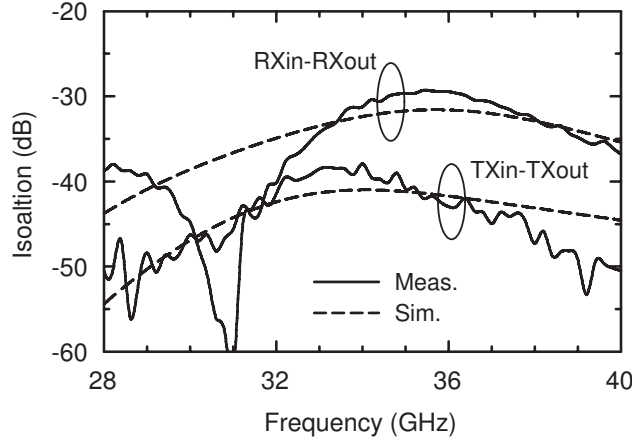


Figure 6.6 Measured isolation of the receive and transmit modes.

control). The measured RXin and RXout reflection coefficients remain < -10 dB over all gain and phase settings. The power consumption in the receive mode is only 16 mA from a 1.8 V supply (29 mW).

Fig. 6.5 presents the measured transmit-mode S-parameters. In this case, the power consumption is 32 mA from a 1.8 V supply (58 mW). The maximum small-signal gain at 33–35 GHz is 10 dB for a peak VGA setting. The transmit gain vs. phase state can also be compensated using the VGA to result in an rms gain and phase response which are identical to the receive mode (see Fig. 6.4(a)(b)). The measured output P_{1dB} is +5.5 dBm for an input of -3.5 dBm and is below the expected value of +7.5 dBm (measured on a stand-alone PA driver). It is believed that this is due to a premature saturation of the VGA output due to the slightly inductive SPDT switch input impedance. The transmit output power can be controlled over a 10 dB range using the VGA (-5 dBm to +5 dBm for a -5 dBm input) with an rms phase imbalance of $< 2^\circ$ at 30–40 GHz. The measured TXin and TXout reflection coefficients remain < -10 dB over all gain and phase settings.

The LNA and the PA driver can be turned off using external controls, and therefore, the isolation between the TXin and TXout port is > 70 dB in the receive mode. In the transmit mode, the isolation between RXin and RXout is also > 70 dB. The measured TXin/TXout and RXin/RXout isolation become -40 dB and -30 dB (max. VGA setting) for the receive and transmit modes, respectively, when the LNA and PA are both kept on irrespective of the transmit or receive mode status (Fig. 6.6). The isolation is high enough and ensures that the noise arising from the TXin port and reflected at the antenna port (with a reflection coefficient of -10 dB) will not affect the system NF. Still, it is

best to turn off the on-chip PA in the receive mode. The simulated switching speed of the SPDT switch and phase shifter (between two states) is 1–2 ns for an RF power of –10 dBm to 0 dBm, and the switching speed of the on-chip LNA and PA driver are < 200 and < 400 ns, respectively, for an output power of -10 dBm and +5 dBm. This is fast enough for most T/R applications.

6.4 Summary

This chapter presents a state-of-the-art BiCMOS Ka-band T/R module capable of excellent gain and phase control. The T/R module performance was predicted to within 1–2 dB using a concatenation of separate 50 Ω design blocks. Some of these design blocks were built one year in advance on different IBM 8HP process runs, and is an indirect indication of the IBM 8HP maturity. The LNA linearity is enough for satellite applications, but can be improved by at least 15 dB using a larger bias current and less gain, albeit at a slight reduction (0.5 dB) in the LNA noise figure.

Chapter 7

Low-Loss Silicon-on-Silicon DC–110 GHz Resonance-Free Package

7.1 Introduction

Numerous microwave and millimeter-wave circuits using MMIC and RF MEMS technologies have been demonstrated with outstanding RF performance for various defense and commercial RF applications. High performance devices, especially RF MEMS devices, should be encapsulated in a hermetic environment to provide protection to the internal circuits from the surrounding elements (humidity, contaminants) [85, 86]. These packages are required to exhibit minimum insertion loss, excellent match, good isolation between the ports, as well as no parasitic resonance in the package. Furthermore, these packages should be manufacturable at a reasonable cost since packaging is usually the most expensive step in the production process.

High performance wafer-scale packaging has been studied by many research groups. Several wafer bonding techniques, such as polymer bonding [87], glass frit bonding [88, 89], solder bonding [90], and gold thermo-compression bonding [91–94] have been used to achieve hermetic or near-hermetic sealing. Schbel et al. used glass-frit bonding with 0.25–0.5 dB insertion loss of a CPW feed-through at 77 GHz [88]. Radant MEMS also presented a DC–40 GHz packaged RF MEMS switch with a return loss of less than -20 dB using glass-frit bonding [89]. Packages using non-conducting sealing material such as polymer and glass-frit are well established and very low cost. However, the polymer bonding does not provide a true hermetic seal, and the glass-frit bonding has potential limitations due to its very high bonding temperature (450–550°C). Muldavin et al. [91] and Margomenos et al. [92] used gold thermo-compression bonding with low insertion loss of a hermetic via-hole transition. But the hermetic via-hole technique requires a very thin substrate at millimeter-wave frequency. At lower frequencies, Jourdain et al. reported 0.1–0.15 dB insertion loss at 2 GHz with solder (SnPb) bonding using CPW feed-throughs [90]. Both the sol-

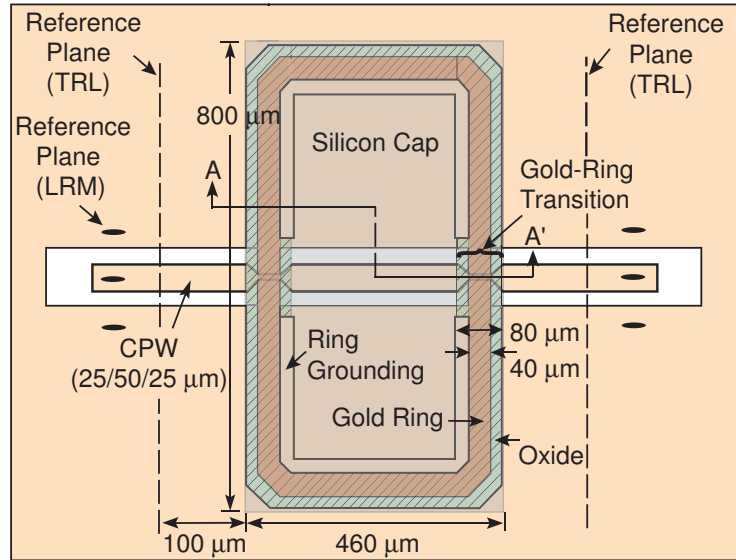
der and thermo-compression bonding use metallic seals with a bonding temperature of 220–360°C depending on the process. Min and Rebeiz also have demonstrated a wafer-scale package using thermo-compression bonding with low insertion loss transitions for CPW feed-throughs [93, 94].

In this chapter, the previous CPW-based approach are applied to a hermetic-compatible wafer-scale DC–110 GHz package. Coplanar waveguide (CPW) lines on a high resistivity silicon wafer are covered with another silicon wafer using gold-to-gold thermo-compression bonding. Oxide is used as a dielectric inter-layer for CPW feed-throughs underneath the gold sealing ring. A 130 μm high cavity is etched in the cap wafer to remove an impact of capping wafer on CPW lines or RF devices. The designed feed-through has an insertion loss of 0.05–0.26 dB at DC–110 GHz with a return loss of < -20 dB (per transition). The gold sealing ring is connected to the CPW ground to eliminate any parasitic resonance and leakage of the package. The whole packaged CPW line has a measured insertion loss of 0.2–0.7 dB and return loss of < -20 dB at DC–110 GHz. It is shown that grounding of the metal sealing ring is essential for obtaining a resonance-free package. Also, the grounding results in very low RF leakage between the input and output port transitions achieving high isolation in the case of a series switch (in the open-state position).

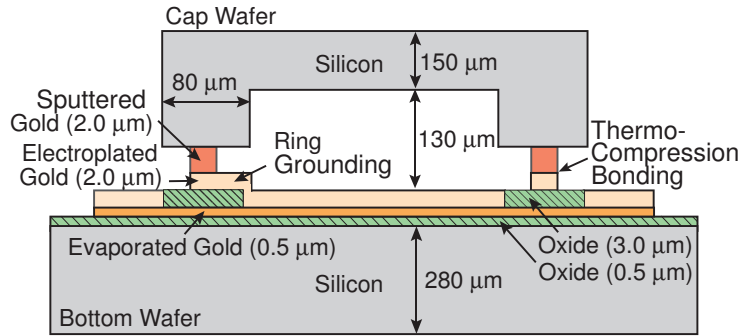
7.2 Package Design

The DC-110 GHz package is based on a gold-to-gold thermo-compression bonding technique of two silicon wafers (Fig. 7.1). A 25/50/25 μm CPW line is used on the bottom wafer to achieve a 50 Ω transmission line. The CPW dimension of 100 μm is selected to be less than $\lambda_g/10$ at 110 GHz to ensure single mode operation. High resistivity silicon wafers (1000 $\Omega\text{-cm}$) are used for the bottom and cap wafers to decrease the CPW line loss. A 130 μm cavity is etched in the cap wafer to remove the impact of placing a silicon wafer in the near proximity of the CPW lines or RF components. Therefore, the CPW lines or RF components do not need to be re-designed for use inside the package.

A gold ring over an oxide inter-layer provides sealing for the hermetic package. The oxide inter-layer protects the CPW center conductor from being connected to the ground plane. The gold ring needs to be wide enough to achieve a hermetic seal, and a 40 μm gold ring is used in this design [95].



(a)



(b)

Figure 7.1 Top view (a) and AA' cross section (b) of the DC-110 GHz package based on CPW transmission lines.

7.2.1 Package Transition

The width of the CPW center conductor underneath the gold ring is narrowed down to $10\ \mu\text{m}$ to compensate for the capacitive loading of the gold ring and to keep a constant impedance throughout the transition (Fig. 7.2(a)). The narrow capacitive line with a length of $w = 40\ \mu\text{m}$ has an impedance of $32\ \Omega$ (for an oxide inter-layer of $3\ \mu\text{m}$) and is matched by the inductive tapering in the CPW line. The simulated return loss and insertion loss of the transition using Sonnet¹ is lower than $-20\ \text{dB}$ and $0.19\ \text{dB}$, respectively, at $110\ \text{GHz}$ (Fig. 7.2(b)). The relatively high insertion loss at $110\ \text{GHz}$ is due to the thin ($t = 0.5\ \mu\text{m}$) and narrow ($w = 10\ \mu\text{m}$) CPW center conductor underneath the gold ring. If the oxide layer is increased to $6\ \mu\text{m}$, the CPW center conductor becomes $20\ \mu\text{m}$ and the

¹Sonnet, ver. 9.52, Sonnet Software Inc., Syracuse, NY, 1986-2003.

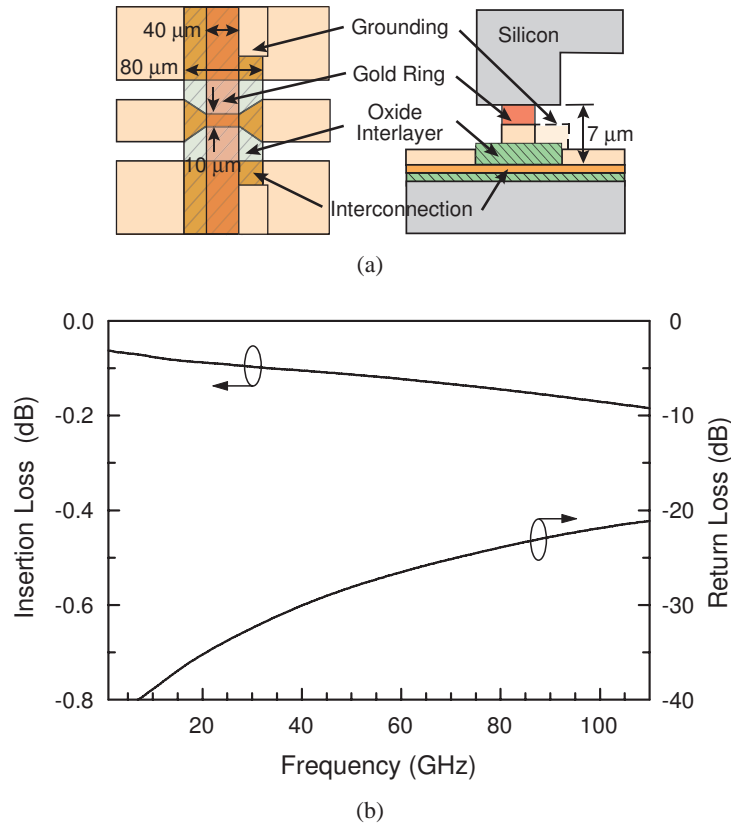


Figure 7.2 Top and side view (a) and simulated insertion and return loss (b) of the gold-ring transition.

insertion loss reduces to 0.12 dB at 110 GHz. This can be achieved with glass-frit bonding, but is hard to do with PECVD oxide without stress and cracking issues and potential loss of the hermetic seal.

7.2.2 Gold-Ring Grounding

The gold sealing ring is connected to the CPW ground all around the package except at the input/output CPW lines. Without grounding, the gold ring is floating over the oxide inter-layer, and results in package resonances at the frequencies where the package circumference equals to multiples of wavelength. The gold-ring grounding also increases the isolation between the input and output ports in the case of an open series switch. The gold-ring grounding removes any slotline modes when the package is not symmetric with respect to the CPW center conductor and the ground-plane widths inside the package are unequal (see Fig. 7.4(a)). The reason is that the gold-ring grounding acts as an air bridge and equalizes the potential of the ground planes above and below the CPW

center conductor [96].

7.3 Fabrication

7.3.1 Fabrication Flow

The fabrication process is shown in Fig. 7.3. The CPW line is fabricated on a 280 μm -thick silicon substrate. The substrate is passivated with a 5000 \AA thick PECVD oxide layer. The first step is a lift-off process of Ti/Au/Ti 300/4400/300 \AA which patterns the CPW line and the thin feed-through layer (Fig. 7.3(a)). This feed-through must be thin to make a relatively planar bonding surface. The next step is a PECVD deposition of 3 μm oxide (SiO_2), which is patterned using an RIE process (Fig. 7.3(b)). This oxide layer provides the dielectric inter-layer between the CPW line and the gold sealing ring. During the RIE process, the oxide passivation layer in the CPW slots is also removed everywhere except under the gold-ring transition. The reason is that the oxide passivation layer increases the loss of CPW line due to charge trapping on the Si/ SiO_2 interface [97]. Then, a 300/1000/300 \AA Ti/Au/Ti seed layer is sputtered and the CPW line and the bottom part of the sealing ring are electroplated to 2 μm (Fig. 7.3(c)).

On a separate 280 μm -thick cap wafer, a 2 μm Au layer is sputtered first, and the top part of the sealing ring is patterned with wet etching. The next step is a lift-off process of align keys on the backside of the cap wafer for the future bonding process (Fig. 7.3(a)). Then, a 1000 \AA of Al layer is sputtered and patterned to provide a DRIE mask of the 130 μm high package cavity (Fig. 7.3(b)). Before this cavity is etched, opening holes for the CPW probes are etched first using a photoresist mask (Fig. 7.3(c)). The 280 μm silicon cap wafer is then completely etched through, and these openings can be used for stud bump interconnects or probe measurement. If via-holes are placed outside of the package for a standard surface-mount package, the 160 μm DRIE step for the opening holes can be removed from the process.

7.3.2 Gold-to-Gold Thermo-Compression Bonding

The final step is the gold-to-gold thermo-compression bonding of the two silicon wafers (Fig. 7.3(d)). The wafers are heated to 360°C and a pressure of 7 MPa is applied for an hour using

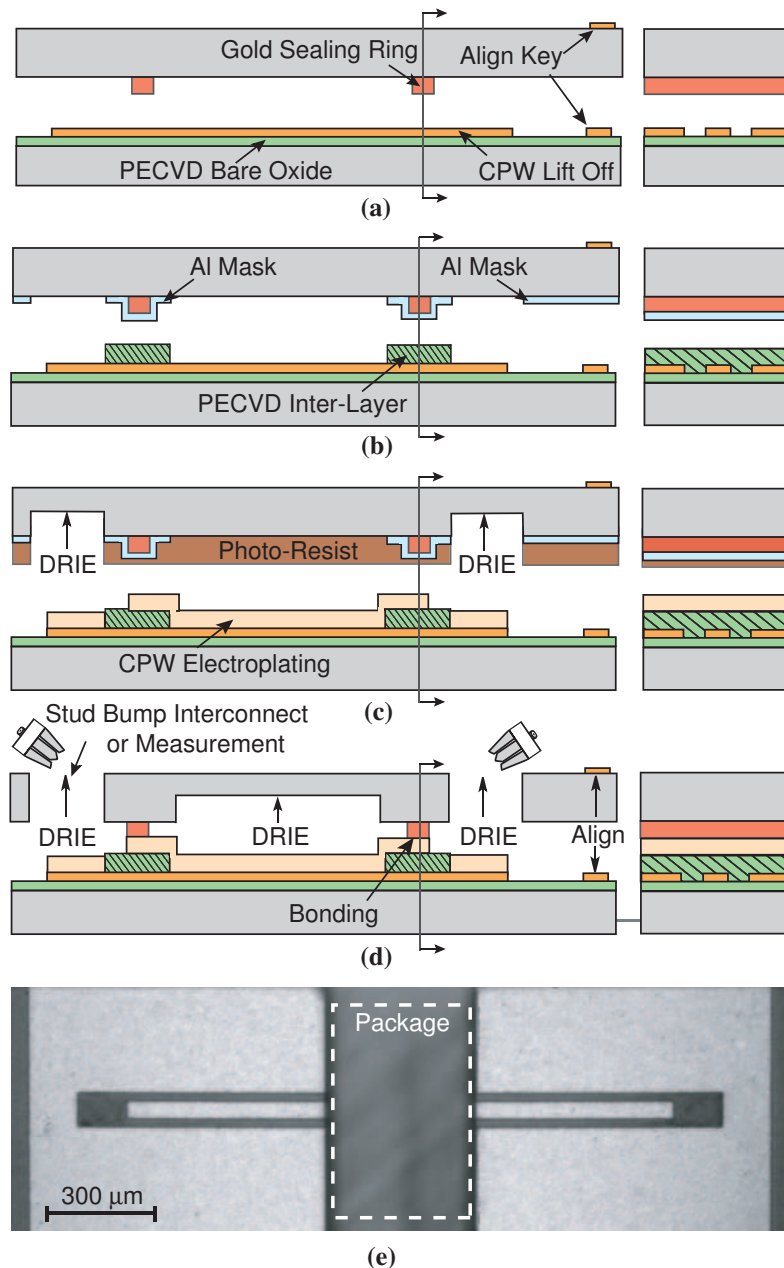


Figure 7.3 Fabrication flow (a)-(d) and a picture of a complete package (e).

the EV 501² bonder. The bonding temperature and pressure are very critical for the CPW lines, as well as the bonding process itself. If the bonding temperature is over 380°C for an hour, the electroplated gold is deformed and the CPW line shows very high loss. This thermo-compression bonding technique has shown proven high reliability hermetic sealing [92, 95]. Notice from the gold-ring and silicon remnants in Fig. 7.4(b) and (c), that the gold-ring and silicon materials of the

²EV 501s, EV Group, Schaerding, Austria

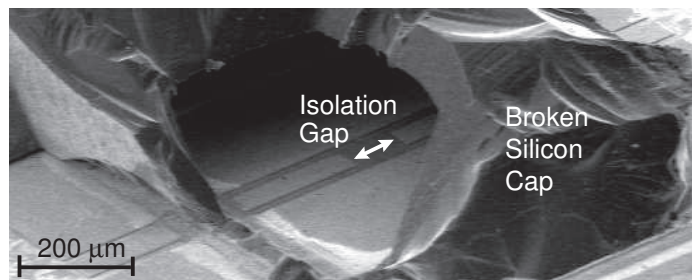
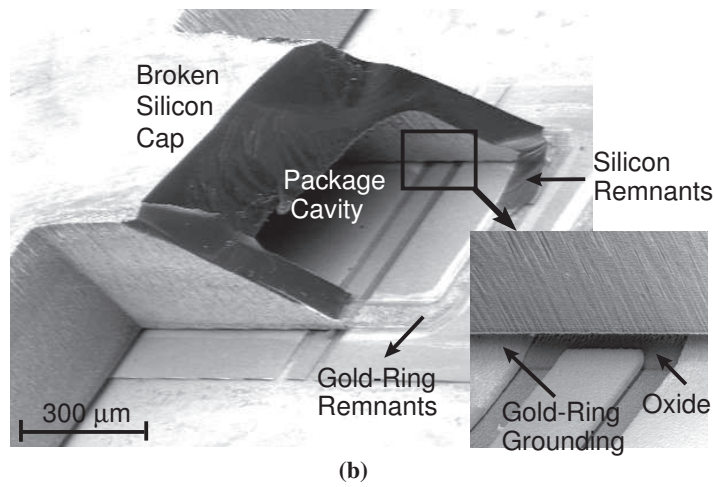
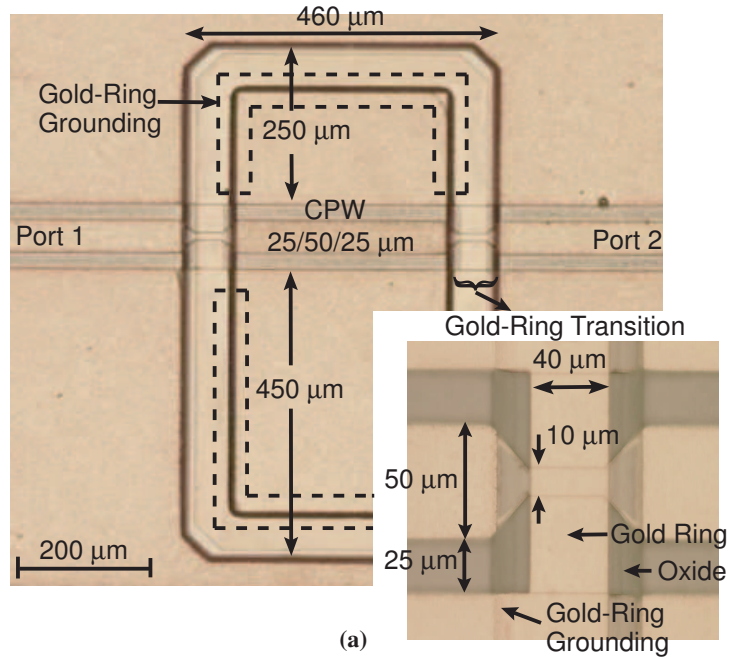


Figure 7.4 Microphotograph of a bottom wafer (a) before bonding, and the SEM photograph of an asymmetric package (b) and a symmetric package (c) with $60\ \mu\text{m}$ gap in the CPW line after the cap is removed over a portion of the package.

Table 7.1 Summary of Measured and Simulated Characteristics of CPW Line and Gold-Ring Transition.

	Freq.	Sim./Meas.	Characteristics
CPW w/ & w/o Si Cap	90 GHz	Sim.*	$Z_0=50 \Omega$, $\alpha=230$ dB/m, $\epsilon_{\text{eff}}=6.0$
		Meas.	$Z_0=49 \Omega$, $\alpha=210$ dB/m, $\epsilon_{\text{eff}}=5.6$
Gold-Ring Transition Loss	20 GHz	Sim.*	Insertion Loss = 0.09 dB
		Meas.	Insertion Loss = 0.13 dB
	40 GHz	Sim.*	Insertion Loss = 0.11 dB
		Meas.	Insertion Loss = 0.16 dB
	75 GHz	Sim.*	Insertion Loss = 0.14 dB
		Meas.	Insertion Loss = 0.20 dB
	110 GHz	Sim.*	Insertion Loss = 0.18 dB
		Meas.	Insertion Loss = 0.26 dB

* $\epsilon_{\text{si}} = 11.9$, $\sigma_{\text{si}} = 0.1$ S/m, $\tan\delta_{\text{si}} = 0.003$, $\epsilon_{\text{oxide}} = 3.8$, and $\sigma_{\text{gold}} = 3 \times 10^7$ S/m

cap wafer remain bonded to the bottom wafer even after the silicon cap is removed. The hermeticity of the packages have not been tested, and this is why this package is referred to hermetic-compatible package.

7.4 Simulation and Measurement

7.4.1 Transition Loss

Table 7.1 summarizes the simulated and measured RF characteristics of the CPW line and the gold-ring transition. S-parameters of the CPW lines are measured on an HP 8510XF network analyzer, using a TRL calibration method to de-embed the probe-to-wafer transition and establish the reference planes shown in Fig. 7.1. The LRM calibration method is also used below 40 GHz and is referenced to the CPW probe tips. The CPW characteristics are measured using many 1,000 μm and 2,000 μm long CPW lines with and without the silicon cap. The silicon cap, with a 130 μm high cavity, has no apparent impact on the CPW characteristics. The measured insertion loss of packaged and un-packaged CPW lines are shown in Fig. 7.5. The loss due to the gold-ring transitions can be estimated by their difference, and is summarized in Table 7.1 at 20, 40, 75, and 110 GHz per transition. The measured packaged line loss is 0.04–0.06 dB higher than the Sonnet simulation

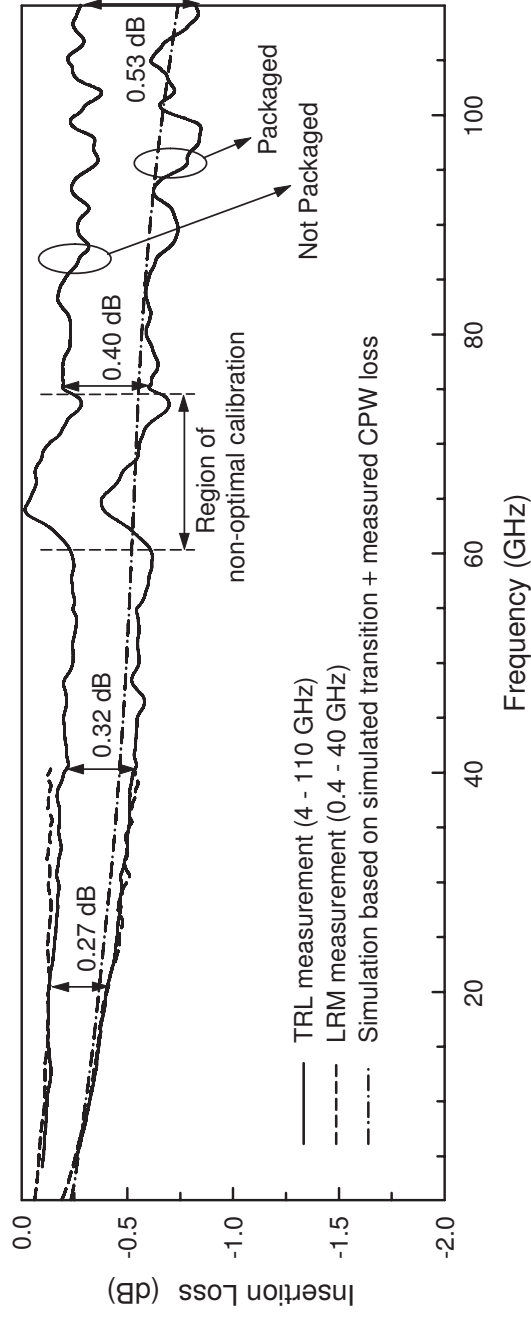
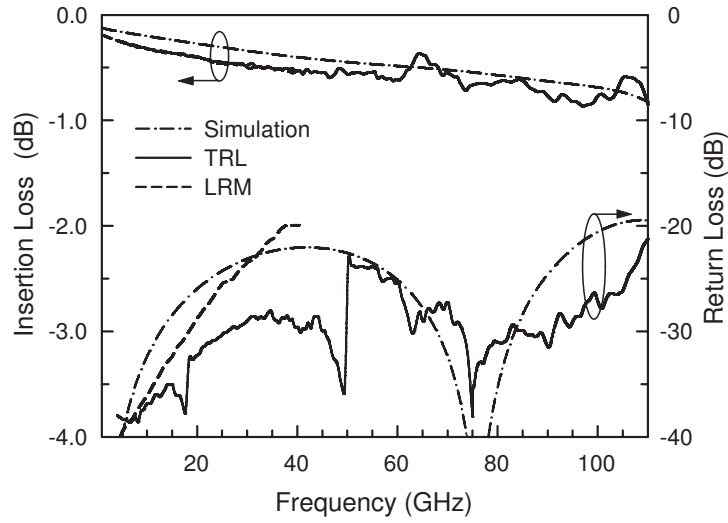
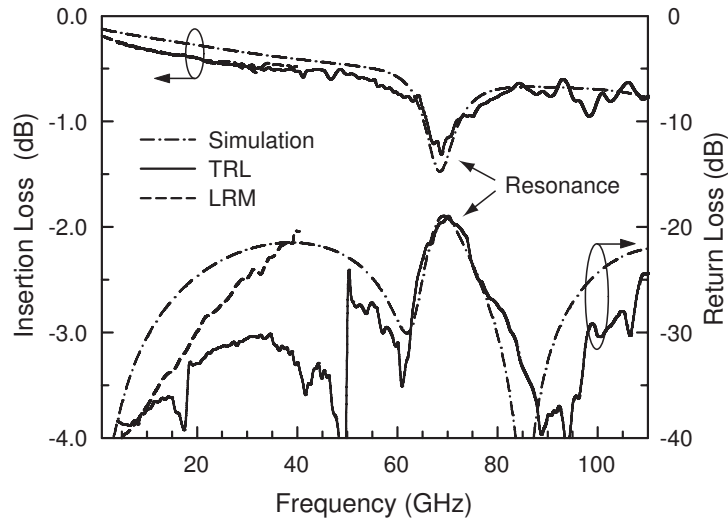


Figure 7.5 Measured and simulated insertion loss of the CPW line and the packaged CPW line. The added loss between two lines includes the effects of two gold-ring transitions.



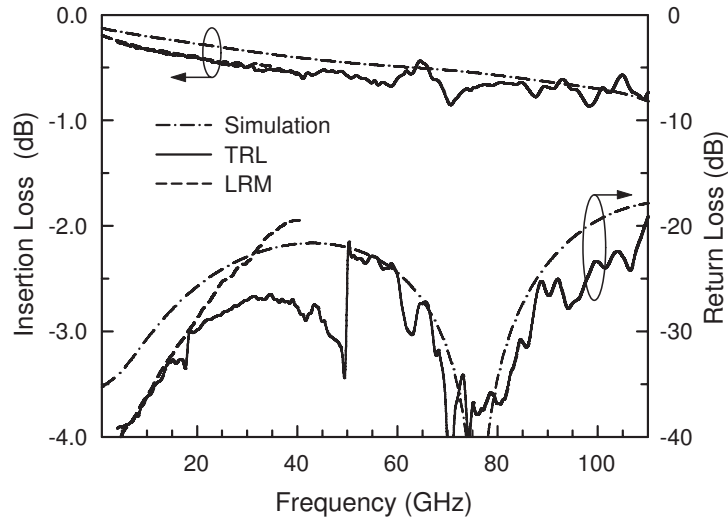
(a)



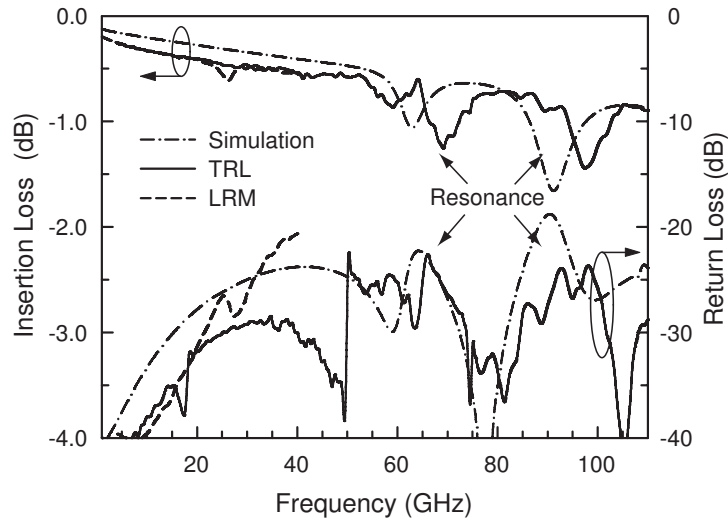
(b)

Figure 7.6 Measured and simulated (HFSS) insertion loss and return loss of a symmetric package with (a) and without (b) gold-ring grounding.

and is possibly due to the oxide passivation layer which is charged under the CPW line. This oxide layer attracts minority carriers of the semiconductor and results in a localized low resistivity inversion layer at the silicon surface [97]. The return loss of the package is mainly determined by the gold-ring transition and is better than -20 dB at DC–110 GHz for a symmetric layout (Fig. 7.1(a), Fig. 7.6(a)) and an asymmetric layout (Fig. 7.4(a), Fig. 7.7(a)).



(a)



(b)

Figure 7.7 Measured and simulated (HFSS) insertion loss and return loss of an asymmetric package with (a) and without (b) gold-ring grounding.

7.4.2 Package Resonance and Group Velocity

Fig. 7.6 presents the HFSS³ simulated and measured insertion loss and return loss of the packaged CPW line. In Fig. 7.6(a), the gold ring is connected to the CPW ground, but in Fig. 7.6(b), the gold ring is floating on the oxide inter-layer. The results demonstrate the effect of the gold-ring grounding to the CPW ground: Without grounding, there is a resonance frequency around 66 GHz

³HFSS, ver. 9.2, Ansoft Corporation, Pittsburgh, PA, 1984-2004.

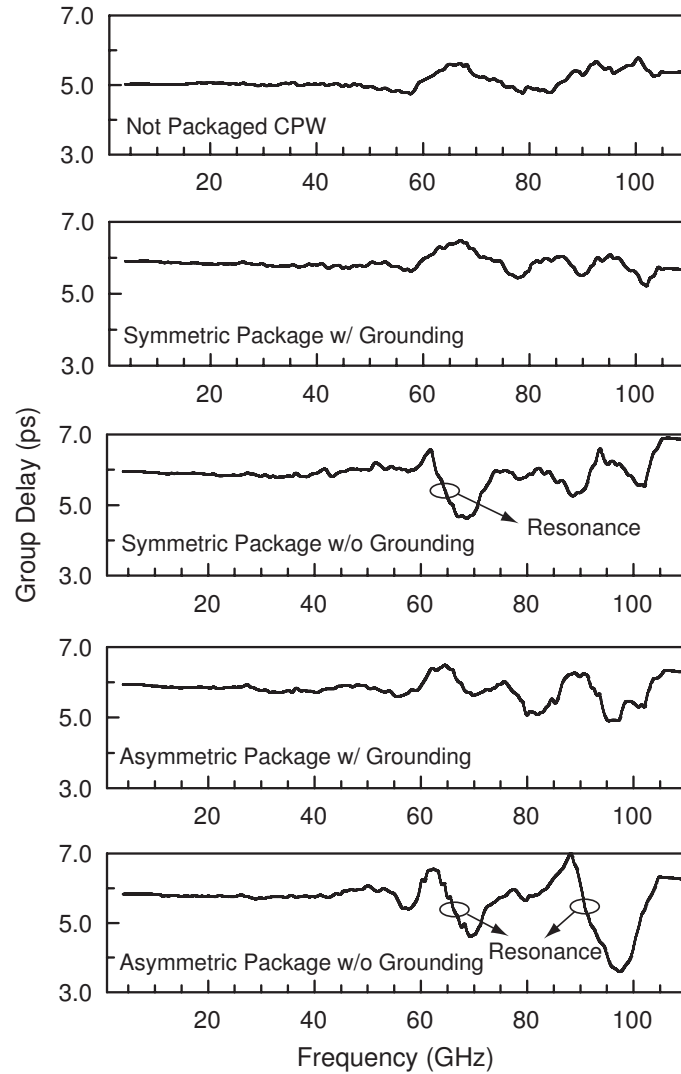


Figure 7.8 Measured group delay of the CPW line and the packaged CPW line with and without gold-ring grounding.

where the circumference of the gold ring equals one guided wavelength ($\lambda_g = \lambda_o / \sqrt{\epsilon_{eff}} = 2.5$ mm). Fig. 7.7 also presents the simulated and measured insertion loss and return loss of an asymmetric packaged CPW line, where the CPW center conductor is not placed in the middle of the package (Fig. 7.4(a)). Fig. 7.7(b) shows two resonances: The first one at 65 GHz is due to the gold-ring resonance, and the second one at 95 GHz is due to undesired slotline mode propagation within the CPW line, which arises from the different size of the CPW ground planes above and below the center conductor [96]. This resonant frequency depends on the size and the asymmetry of the package. As seen in Fig. 7.7(a), the gold-ring grounding removes these undesired resonances.

The effect of the gold-ring grounding can be also shown in the group delay of the measured

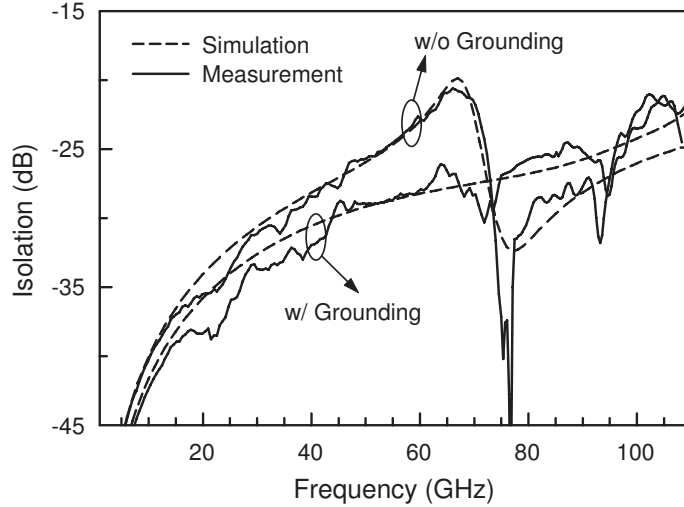


Figure 7.9 Measured and simulated (HFSS) isolation of a symmetric package with and without gold-ring grounding.

CPW line (Fig. 7.8). The packaged CPW line (symmetric or asymmetric) with gold-ring grounding has a relatively flat group delay as in the case of the un-packaged CPW line. However, packaged CPW lines without gold-ring grounding have much more variation in the group delay due to the package resonances. The small ripples in the group delay at 60–110 GHz are due to the non-optimal calibration.

7.4.3 Isolation and Leakage

Fig. 7.9 presents the input/output isolation of a symmetric packaged CPW line with a $60 \mu\text{m}$ -long gap in the center conductor (Fig. 7.4(c)). This represents the case of a series switch in the open-state position. With grounding, the isolation improves up to 8 dB at 65 GHz. The reason is that gold-ring grounding greatly reduces any leakage between the input/output transitions.

Fig. 7.10(a) shows a simple intuitive circuit model of the package without gold-ring grounding. The parasitic capacitance of input/output transitions and gold ring is modeled as $C = 20 \text{ fF}$ and a microstrip line with a characteristic impedance of 15Ω , respectively. One can see that there are two paths between the input and output ports: The direct path (CPW with gap) and the leakage path through the gold ring. At around 65 GHz the leakage path resonates and change phase by 180° . At 80 GHz, the two paths add to zero (destructively interfere) in the S_{21} response (Fig. 7.10(b)). This agrees quite well with the measurement of Fig. 7.9.

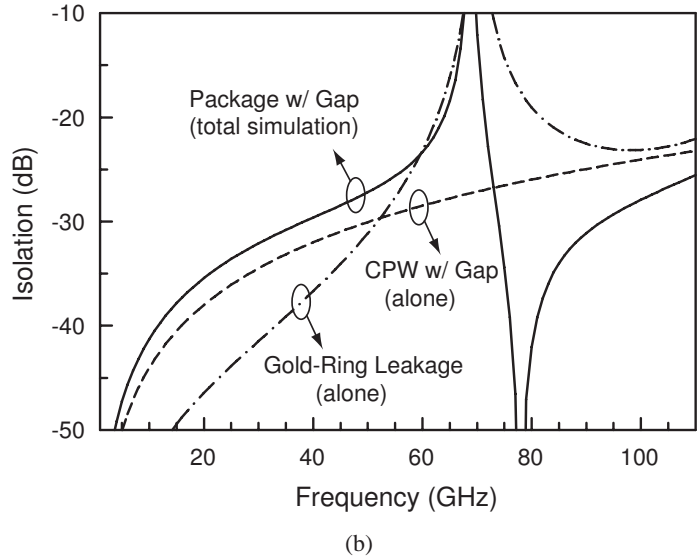
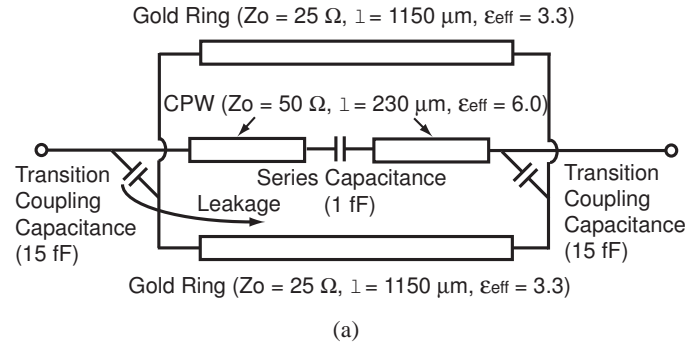


Figure 7.10 Circuit model of a package with the leakage path of the gold ring (a) and the simulated isolation of the paths (b) without gold-ring grounding

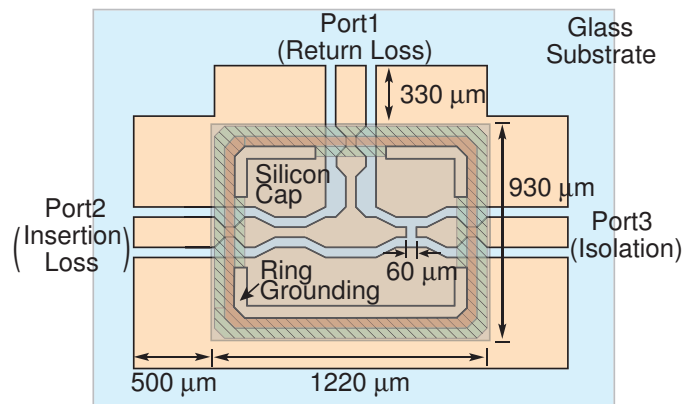
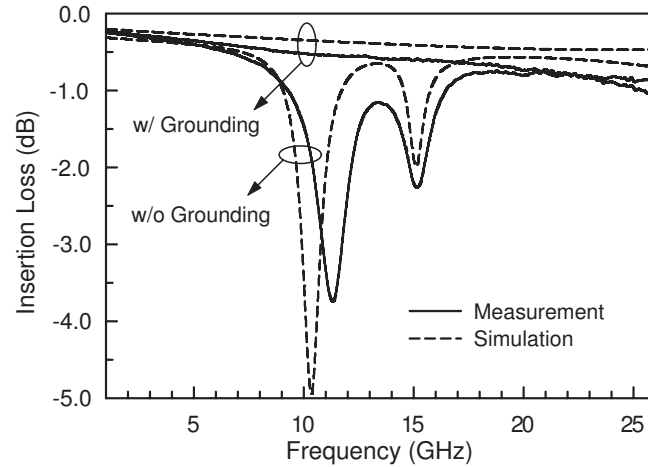
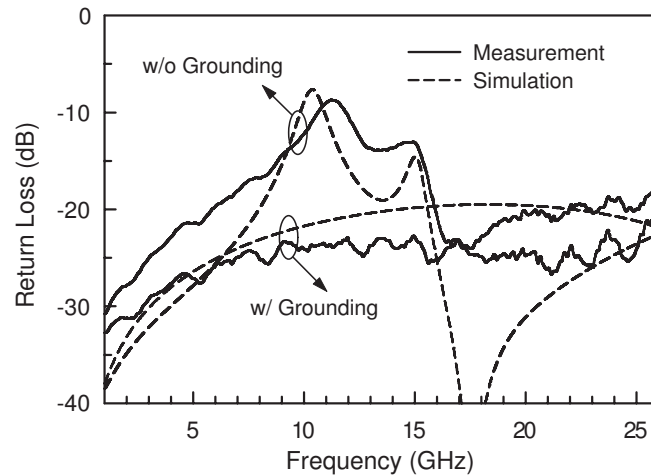


Figure 7.11 Top view of a SP2T package for a DC–26 GHz application.



(a)



(b)

Figure 7.12 Measured and simulated insertion loss (a) and return loss (b) of a SP2T package with and without gold-ring grounding.

7.5 Extension to a Resonance-Free SPNT Switches

Many SPNT switch topologies require large packages for many switches, and as seen above, this may result in unwanted resonance modes. The CPW packaging technique is hereby applied to single-pole-two-throw (SP2T) switches on a glass substrate for a DC–26 GHz application. Fig. 7.11 shows the top view of SP2T switches where port1 is the input port, and port2 and port3 are the outputs ports. The simulated and measured insertion loss S_{21} in Fig. 7.12 clearly shows package resonances at 11 and 15 GHz for the case without gold-ring grounding. With gold-ring grounding, the insertion loss and return loss are less than 1 dB and -20 dB, respectively, and no resonance is

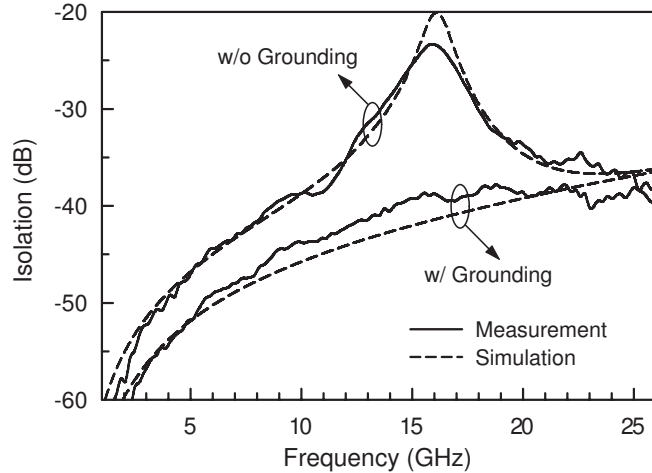


Figure 7.13 Measured and simulated isolation of a SP2T package with and without gold-ring grounding.

present. As shown in Fig. 7.13, the isolation S_{31} improves by up to 15 dB with gold-ring grounding. The leakage in the un-grounded gold ring is quite high due to the large currents on the gold-ring around the 15 GHz resonance frequency. These currents couple to the output port through the transition coupling capacitance and result in an isolation of only -23 dB (instead of -39 dB).

7.6 Summary

This chapter demonstrates the design and fabrication of a wafer-scale package for DC–110 GHz applications. The sealing technique used a gold-to-gold thermo-compression bonding ring which can result in un-wanted resonance modes. The gold-ring grounding to the CPW ground plane eliminates all package resonances or slot-line modes and improves the group delay flatness. The gold-ring grounding also improves the isolation because the grounded gold-ring considerably reduces the leakage between the input and output ports. A packaged CPW line has an additional insertion loss of 0.05–0.26 dB at DC–110 GHz (per transition), with a return loss better than -20 dB for the entire structure. This technique was also applied to SP2T switches at DC–26 GHz and was shown to prevent the formation of resonance modes in large packages.

Chapter 8

Conclusion and Future Work

8.1 Summary and Conclusion

Phased array systems have been used since the 1950's to achieve electronic beam control and fast beam scanning. In the RF-phase shifting architecture, transmit/receive (T/R) modules are required for each antenna element, and these have been traditionally developed using GaAs or InP technology. This thesis demonstrates that state-of-the-art Ka-band (35 GHz) T/R modules can also be developed using the IBM 8HP SiGe BiCMOS technology. The designed circuit blocks for a T/R module include a low noise amplifier (LNA), a 4-bit phase shifter, a variable gain amplifier/attenuator, SPDT switches and a power amplifier (PA) driver.

The 26–40 GHz phase shifters are designed based on CMOS switch and miniature low-pass networks for a single-ended and differential applications, and result in 3° rms phase error at 35 GHz with an average loss at 11–12 dB. The SiGe LNA result in a peak gain of 24 dB and a noise figure of 2.9–3.1 dB at 26–40 GHz for a power consumption of only 11 mW. The variable step attenuator, based on CMOS switches, has 12 dB attenuation range (1 dB step) with very low loss and phase imbalance, and operates at 10–50 GHz. A variable gain LNA is also demonstrated at 30–40 GHz for the differential phased array receiver, and has 20 dB gain and $<1^\circ$ rms phase imbalance between the 8 different gain states and 10 dB gain control. All of these circuits show state-of-the-art performance, and the phase shifter, distributed attenuator and VGA are also first-time demonstrations at Ka-band frequencies.

In the receive mode, the fully integrated T/R module results in a controllable gain of 9–19 dB at 33–35 GHz, with a NF of 4–5 dB and an input P_{1dB} of -29 dBm. In the transmit mode, the maximum gain and output P_{1dB} are 10 dB and $+5.5$ dBm, respectively, and can be controlled over a 10 dB range (output P_{sat} is $+8$ dBm). The measured rms gain and phase error are <0.6 dB and

$< 7^\circ$, respectively, in both the transmit and receive modes using 1-bit gain compensation in the on-chip VGA. The chip is only $0.93 \times 1.33 \text{ mm}^2$ and consumes 58 mW and 29 mW in the transmit and receive modes, respectively. This T/R module is suitable for low cost applications in satellite communications. The silicon T/R modules will not replace the GaAs/InP power amplifier and very low noise amplifier (noise figure of 1–1.5 dB at 35 GHz) but can significantly reduce the cost of the back-end (phase shifters, VGA, combiner, etc.) in defense-based applications.

Finally, a DC–110 GHz Si wafer-scale packaging technique has been developed using gold-to-gold thermo-compression bonding and is suitable for Ka-band and even W-band T/R modules. The package transition has an insertion loss of 0.1–0.26 dB at 30–110 GHz, and the package resonances and leakage were drastically reduced by grounding the sealing ring. This is the first demonstration of a wideband resonance-free (DC–110 GHz) package using silicon technology.

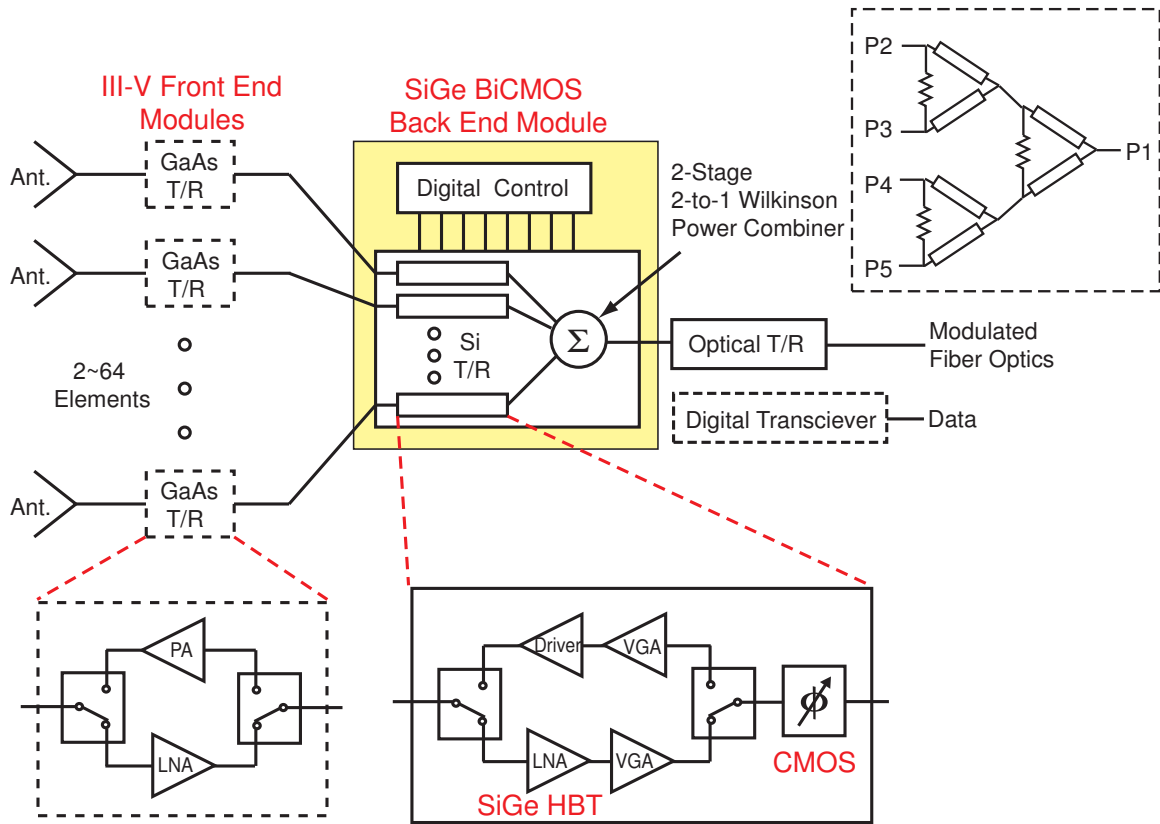


Figure 8.1 System diagram of multi-element phased array T/R module.

8.2 Future Work

8.2.1 Multi-Element Phased Array T/R Module

At the moment, the T/R module for a single antenna element has been completed and shows an excellent performance using SiGe BiCMOS process. Therefore, T/R modules can be integrated together on a single Si chip for multi antenna elements. Fig. 8.1 shows the possible block diagram of the multi-element phased array T/R module. Because the designed phase shifter in Chapter 3 is bi-directional, multi-elements T/R modules can share the phase shifter for the receive and transmit modes using the series-shunt SPDT switches (Chapter 5). To prevent the LNA and PA driver from oscillation, the isolation of the SPDT switches is very important, otherwise the LNA and the PA driver should be turned off or powered down for the transmit and receiver mode, respectively. The LNA, VGA (Chapter 2) and PA driver (Chapter 6) can be reused in this new multi-element T/R module with simple layout modifications. Fig. 8.2 shows the layout of a single module for the

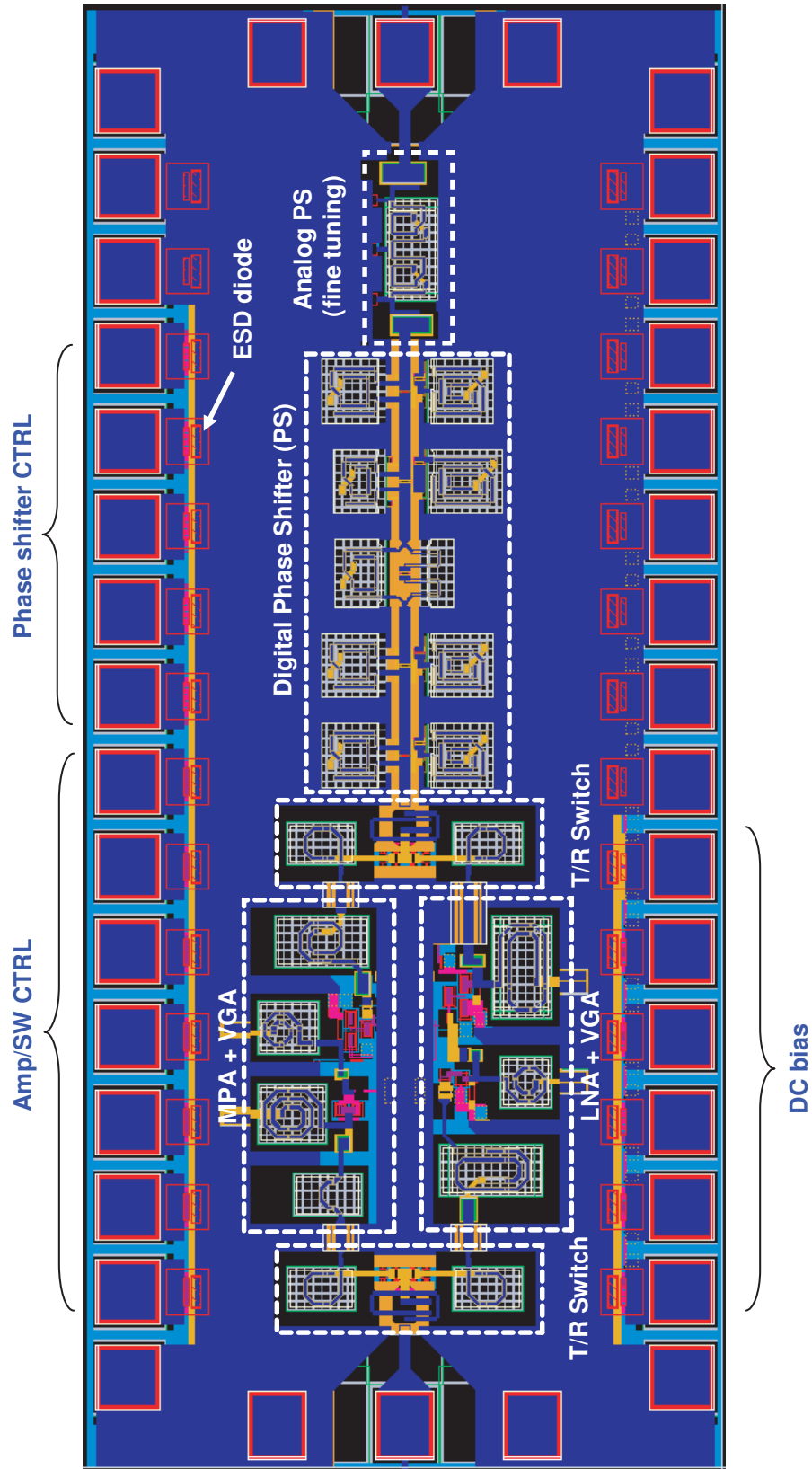


Figure 8.2 Layout of the integrated Ka-band phased array T/R module for a single antenna element.

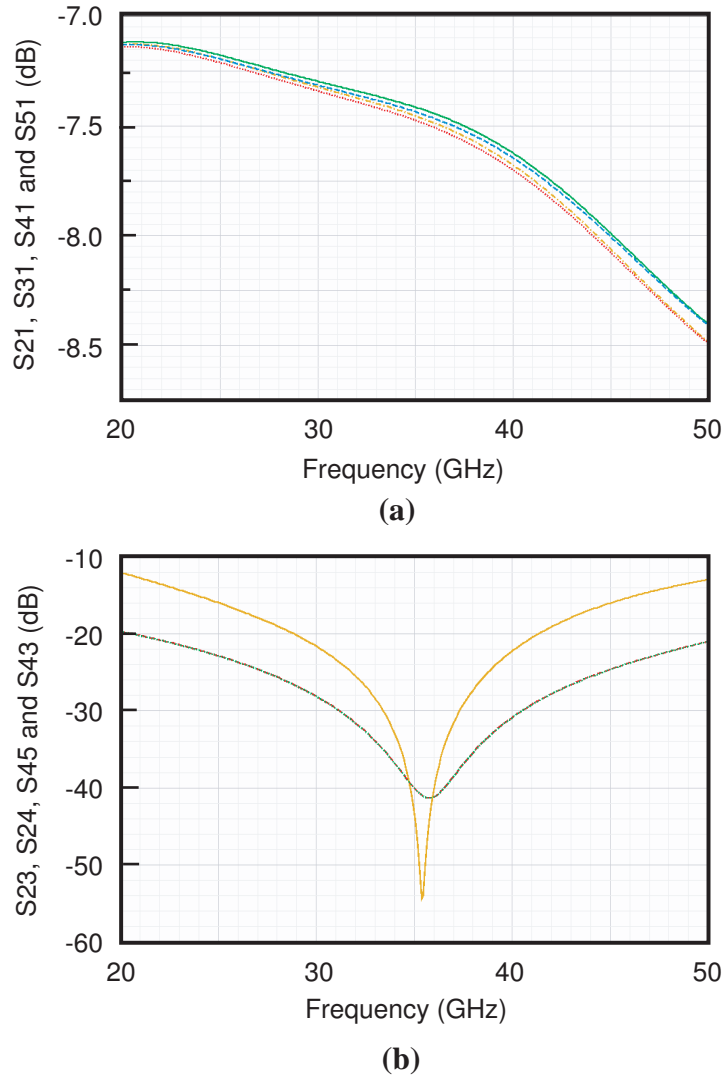


Figure 8.3 Simulated S-parameters of the 2-stage Wilkinson power combiner: (a) insertion loss and (b) isolation.

multi-element T/R module, and one could notice that an analog phase shifter based on HA varactor diodes is added after the 4-bit phase shifter for a continuous phase control (>4-bit phase control).

The multi-element T/R module requires a power combiner/divider on-chip. For bi-directional operation, the power combiner/divider can be designed using a Wilkinson power combiner. In the case of the 4-element T/R module, two Wilkinson combiners can be cascaded together to create 4:1 network. Fig. 8.3 shows the simulated result of the 2-stage Wilkinson power combiner using a full wave EM simulator (Sonnet). The simulated S_{21} is >-7.7 dB up to 40 GHz, and therefore the insertion loss is < 1.7 dB (6 dB is the natural 1:4 divider loss). The simulated isolation between input ports of the 2-stage Wilkinson power combiner is >20 dB at 30–40 GHz. The isolation be-

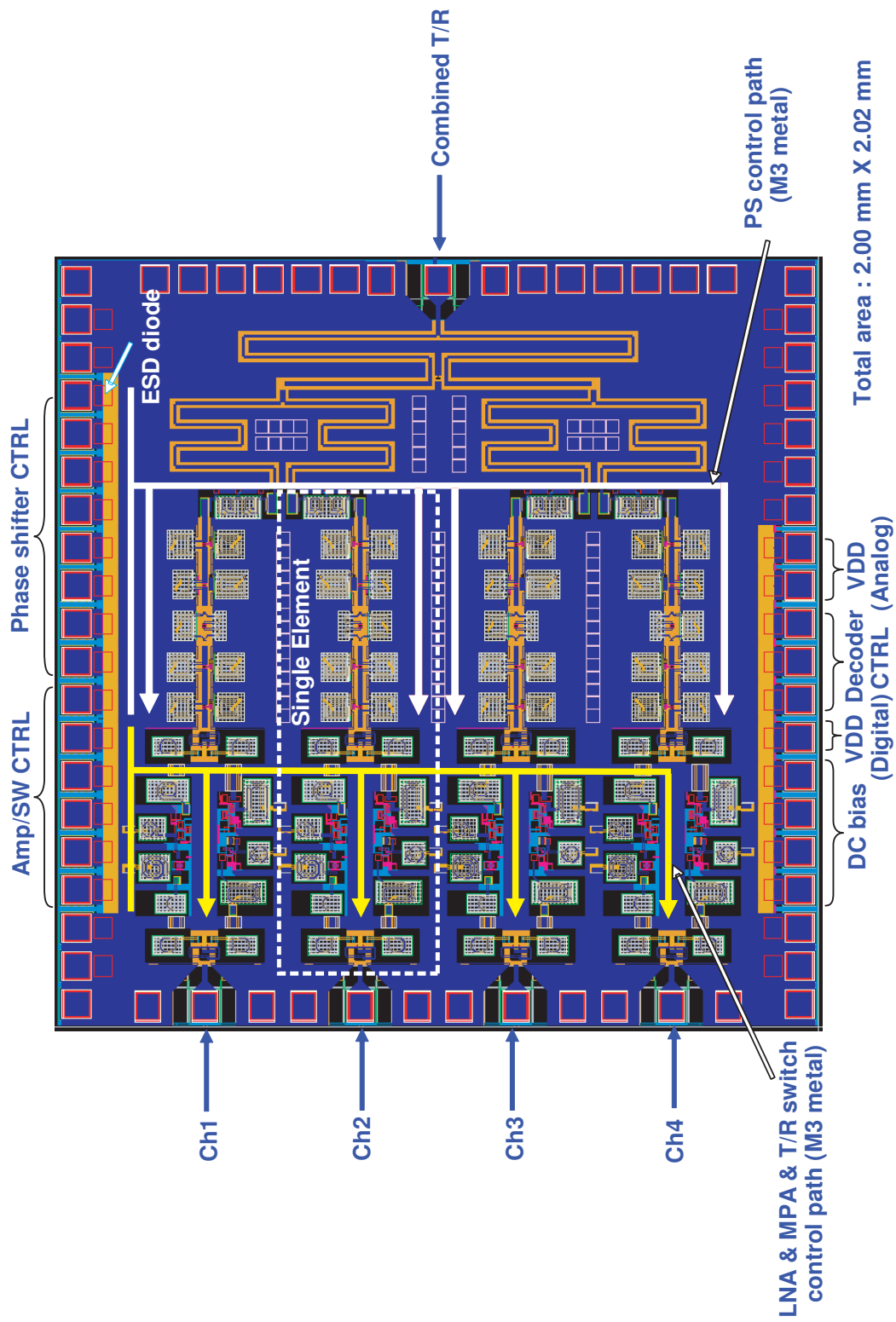


Figure 8.4 Layout of the fully integrated Ka-band phased array T/R module for 4 antenna elements.

tween port 2 and port 3 is lower than the isolation between port port 2 and port 4 due to the 2-stage design. Fig. 8.4 presents the layout of the fully integrated Ka-band phased array T/R module for 4 antenna elements, including the 2-stage Wilkinson power combiner/divider. For the multi-element T/R module, the isolation between the array paths is very important for the accurate phase array operation. Therefore, substrate coupling between devices and circuit blocks is important issue and should be prevented using guard-rings and deep trenches for each array path. Previous work done in Prof. Rebeiz group showed that one can maintain an isolation of > 40 dB at 40 GHz using these designs.

8.2.2 SiGe BiCMOS Process for Millimeter-Wave Applications

The high $f_T > 200$ GHz of a SiGe HBT indicates that the SiGe BiCMOS process is suitable for millimeter-wave RF front-ends, and the whole radar system can be built on a single Si chip. System on a chip (SOC) solution enables high-yield and high-volume manufacturing and thus reduces the price of the radar system drastically. This low-cost radar system can find the market in the 77 GHz automotive radar application since it requires low transmit powers (1–10 mW). Also, one of the advantages of a millimeter-wave frequencies is the higher bandwidth, and therefore SiGe BiCMOS process has drawn lots of attention in this several years for the 60 GHz personal area network (PAN) application with 3–6 Gbps data transfer rates. SiGe/CMOS is also suitable for other applications such as T/R modules for radars at 94 GHz, point-to-point communication system at 80 GHz, and imaging arrays at 94 GHz. There is no doubt that SiGe/CMOS will dominate all commercial and defense applications up to 100 GHz, except for very low noise figure transistors or high power amplifiers. Also, most of the Ka-band demonstration circuits shown in this thesis can be readily scaled to 100 GHz and will allow future miniature phased arrays on a single chip.

Appendix

Appendix A

5–6 GHz SPDT Switchable Balun Using CMOS Transistors

A.1 Introduction

Transformer baluns and SPDT (single-pole-double-throw) RF switches are essential building blocks of RF communication circuits. The transformer baluns and RF switches are usually implemented as off-chip individual components. However, to integrate a whole transceiver on a single silicon chip, the transformer baluns have to be integrated on silicon, and RF switches should be designed based on CMOS transistors [62, 65, 98].

The transformer baluns are mostly used for conversion between single-ended and differential signals. The SPDT RF switches are often used as a transmit/receive (T/R) switch or a switch for multi-standard communication systems. Therefore, the transformer baluns and the SPDT switches are usually the first or second building blocks of an RF communication system. Therefore, it is advantageous to combine the transformer balun and SPDT switch together in one unit since one can reduce the total loss and on-chip routing area (Fig. A.1(a)).

In this appendix, a new concept of a switchable balun is demonstrated at 5–6 GHz using a 0.13 μm CMOS process. The top two metal layers of a CMOS process are used for the primary and secondary inductors of the transformer. The secondary inductor is symmetrically wound, and the CMOS transistors are placed at the center-taps for the switching operation. The transformer is doubly tuned using the transistor parasitic capacitances and an integrated capacitor to overcome the limited coupling factor ($k = 0.76$).

The measured insertion loss of the switchable balun is 1.6–1.7 dB at 5–6 GHz for both ports with excellent input and output match, and the input 1-dB power compression point is 12 dBm. The integrated switchable balun occupies $250 \times 240 \mu\text{m}^2$, and can be used for compact low-power T/R applications with a single-ended antenna and differential low-noise and transmit amplifiers. To

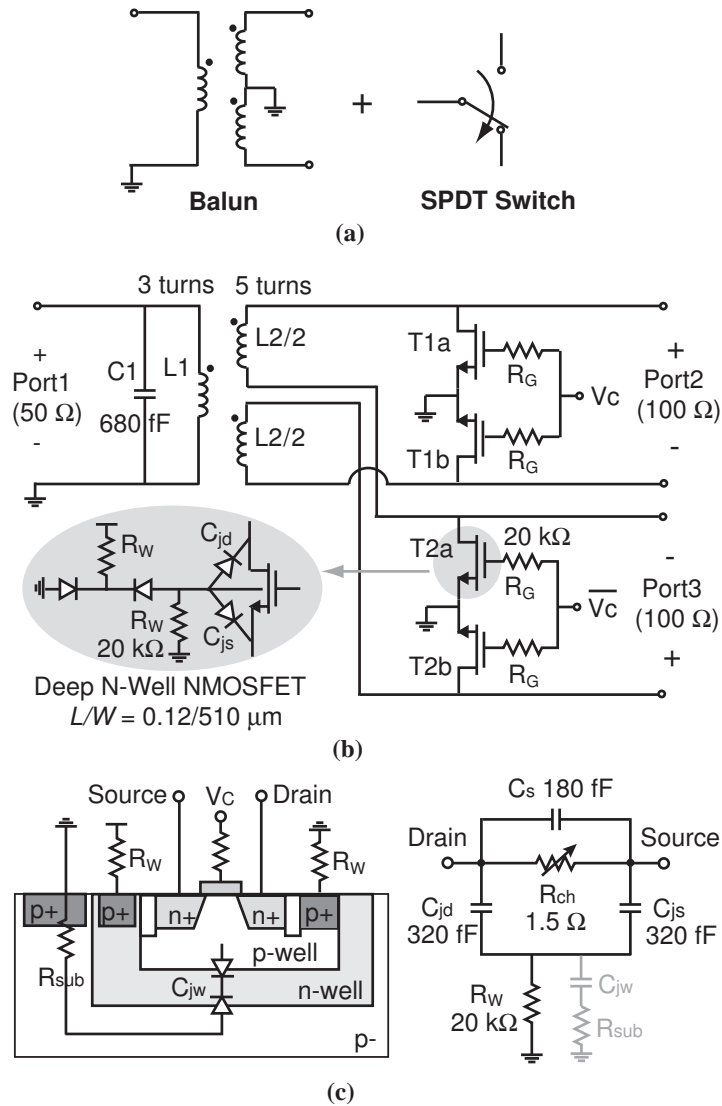


Figure A.1 (a) Concept and (b) schematic of the SPDT switchable balun, and (c) the cross sectional view and equivalent circuit model of the deep n-well nMOSFET.

author's knowledge, this is the first implementation of a switchable transformer balun.

A.2 Design

Fig. A.1(b) shows the schematic of the designed switchable balun. Port1 of the primary inductor is single-ended and Port2 and Port3 of the secondary inductor are differential. Port2 can be considered as the center-tap for the differential signal of Port3, and vice versa. The center-tap of the secondary inductor is usually grounded to achieve good amplitude and phase balance of the differential signal. For the switchable balun, CMOS switches are placed at the center-taps, and can switch

the differential signal between Port2 and Port3 by grounding the center-taps. The single-ended signal port (Port1) is designed to have a $50\ \Omega$ port impedance, and the differential signal ports (Port2 and Port3) have a port impedance of $100\ \Omega$ differential.

A.2.1 Balun Transformer

The balun transformer is designed using the top four metal layers of the IBM 8RF CMOS process (Fig. A.2(a)). The $4\ \mu\text{m}$ thick top metal layer (MA) is wound 3 times in a rectangular shape for the primary inductor ($L1$). The secondary inductor ($L2$) has total 5 turns and results in a higher inductance for the impedance transformation between $50\ \Omega$ and $100\ \Omega$. The secondary inductor is wound with the second metal layer (E1) to have the center-tap in the outer winding (Fig. A.2(b)). Therefore, Port2 and Port3 of the switchable balun, are symmetrical with respect to each other. The underpass for the primary inductor is designed using the fourth metal layer (MG), and the underpass for the secondary inductor is done using LY.

The transformer balun was simulated using full-wave EM software (Sonnet¹) and fitted to a lumped-element model (Fig. A.2(c)) where the leakage inductance of secondary winding is shifted to the primary winding [98]. The simulated coupling factor (k) of the transformer balun is 0.76, and the ratio between $L1$ and $L2$ is about 2.1. The limited k factor of the on-chip transformer result in a decreased bandwidth, and this can be overcome with tuned circuits using capacitors in shunt with the primary and secondary inductors [99]. In this design, the parasitic capacitance of the off-state CMOS switches is used as a tuning capacitance for the secondary inductor and a metal-insulator-metal (MIM) capacitor, $C1$ is used for the primary inductor (see Fig. A.1(b)). The parasitic capacitances of the transformer (C_P and C_S) are also taken into account, and the total shunt capacitance acts as a matching circuit for each port.

A.2.2 CMOS Switch

A nMOS transistor can be used as a switch by controlling the gate voltage through a gate resistor (Fig. A.1(b)). The gate resistor, $R_G = 20\ \text{k}\Omega$, is required in order to prevent signal leaking and oxide breakdown. For conventional SPDT switch designs using nMOS transistors, a series-shunt

¹Sonnet, ver. 10.53, Sonnet Software Inc., Syracuse, NY, 1986-2005.

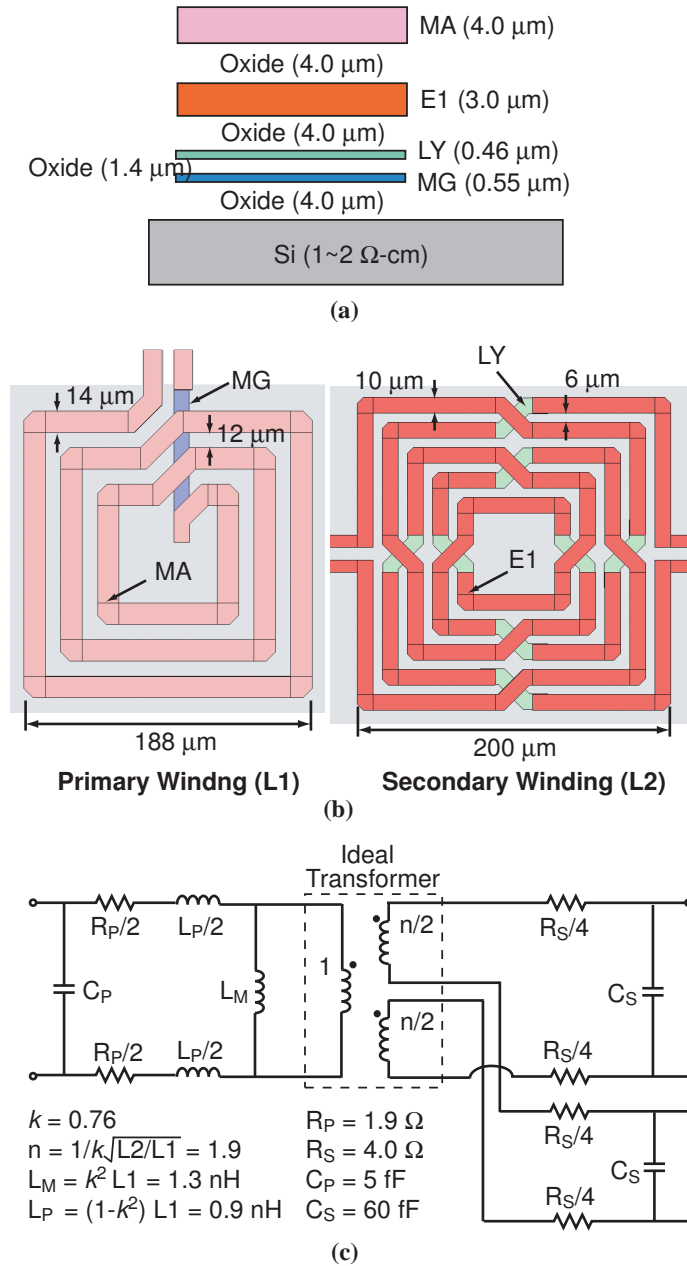


Figure A.2 (a) Metal stack-up of the CMOS process, and (b) layout and (c) model of the balun.

switch configuration is required, and the insertion loss is relatively high due to the series nMOS transistor [65]. However, for the switchable balun, only shunt nMOS switches are required, and the insertion loss can be significantly reduced .

Deep n-well nMOS transistors are used for the nMOS switches, and their simplified circuit model is shown in Fig. A.1(c). The isolated p-well and the deep n-well are biased through large resistors ($R_W = 20 \text{ k}\Omega$) to 0 V and 1.5 V, respectively. Due to the isolated p-well, the body node of

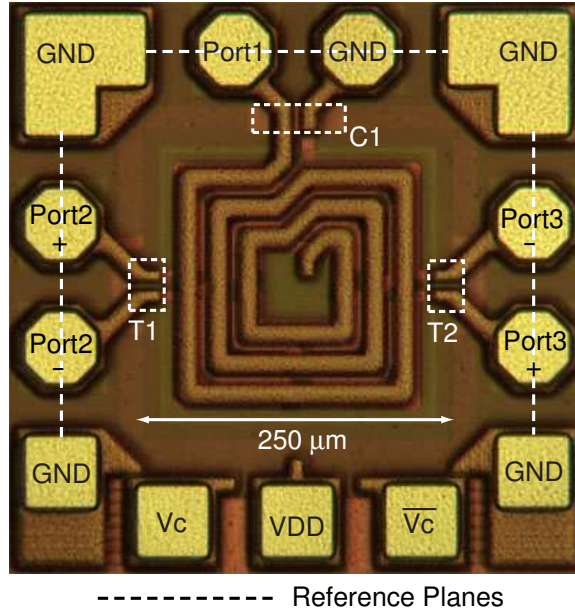


Figure A.3 Micro-photograph of the switchable balun.

nMOS transistor is RF floating, and therefore the junction capacitances ($C_{jd} = C_{js} \approx 320$ fF) couple the source and drain directly and act as the tuning capacitance of the transformer balun. The on-state channel resistance (R_{ch}) of the nMOS switch is very small (1.5Ω). The micro-photograph of the switchable balun is shown in Fig. A.3, and the total chip size is $250 \times 240 \mu\text{m}^2$ (0.06 mm^2) without pads. The chip does not consume DC power other than the leakage gate current.

A.3 Measured Results

A.3.1 Insertion Loss and Isolation

The switchable balun was measured on-chip with external 180° hybrid couplers for differential to single-ended conversion at Port2 and Port3. A 2-port network analyzer (Agilent E8364B) is used, and the 3rd port was always matched to its respective impedance. To measure the insertion loss of the switchable balun, a two-port SOLT calibration is used and this places the reference planes at the GSSG probe tips. The measured insertion loss of the switchable balun is 1.6 dB at 5.5 GHz and < 1.7 dB from 5–6 GHz. Note that the measured insertion loss for Port2 and Port3 are almost identical showing the symmetry of the design (Fig. A.4). The measured amplitude and phase differences between S_{21} and S_{31} are < 0.1 dB and $< 1.5^\circ$, respectively. The measured return loss of Port2 and

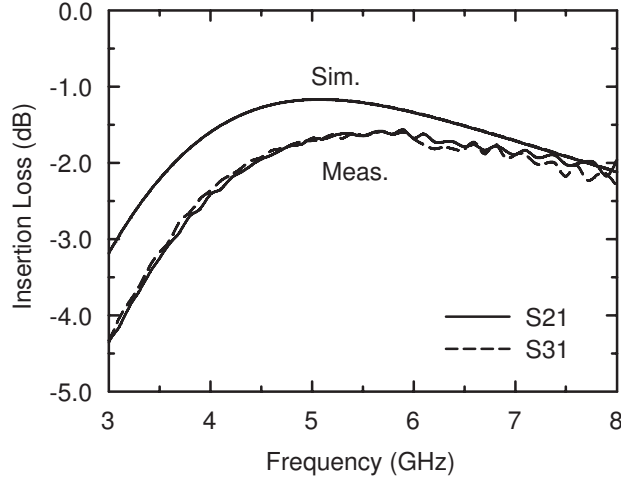


Figure A.4 Measured and simulated insertion loss of the switchable balun.

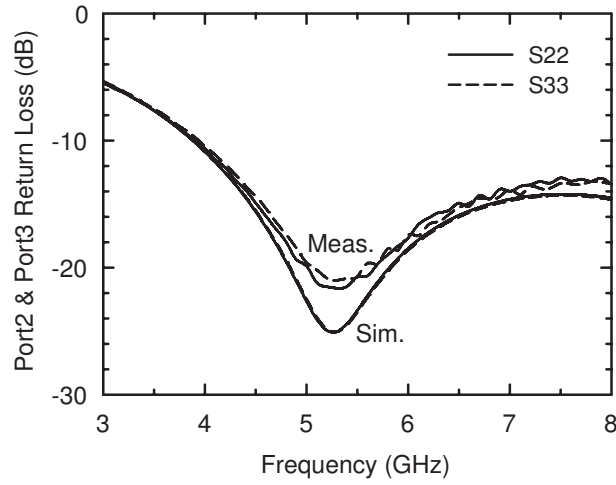


Figure A.5 Measured and simulated return loss of Port2 and Port3.

Port3 is < -18 dB at 5–6 GHz (Fig. A.5) and was done for $T1/T2$ biased OFF/ON ($V_C = 0$ V) and ON/OFF ($V_C = 1.5$ V), respectively.

The return loss of Port1 and the isolation of the switchable balun were measured with a two-port SOLT calibration at the coaxial connector. Port1 is connected through a GSG probe, and Port2 and Port3 are connected through a GSSG probe and a hybrid coupler so as to measure the switchable balun in a single-ended to differential measurement setup. The measured return loss of Port1 is < -15 dB at 5–6 GHz (Fig. A.6). Fig. A.7 shows the measured isolation of the switchable balun, where the probe and hybrid coupler losses (~ 2 dB) are deimbedded out of the measurement. The isolation between Port1 and Port2/Port3 is > 27 dB up to 8 GHz. In this case, S_{21} and S_{31} are

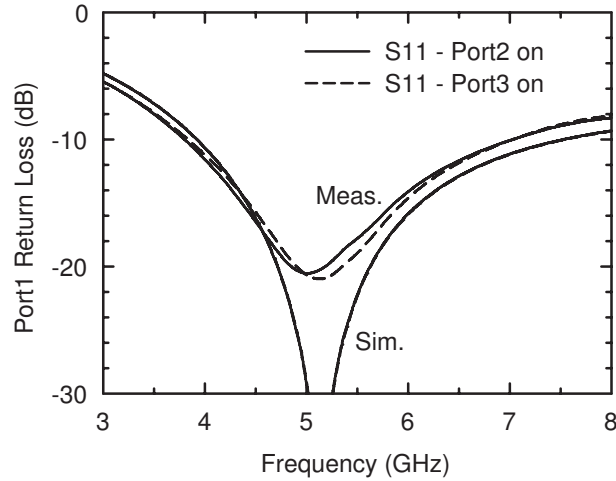


Figure A.6 Measured and simulated return loss of Port1.

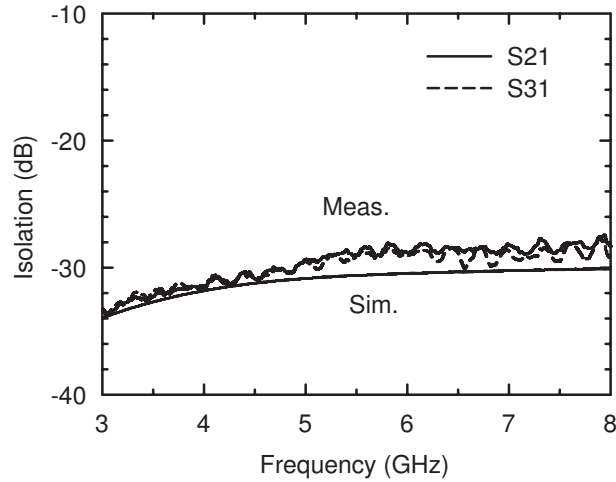


Figure A.7 Measured and simulated isolation of the switchable balun.

measured when the transformer balun is switched to Port3 and Port2, respectively.

A.3.2 Amplitude/Phase Balance and Power Handling

One way to check the operation of the Balun is to measure the amplitude and phase difference between the +/- terminals at the differential ports (Port2 and Port3) for a single-ended input at Port1. Ideally, this difference should be 0 dB and 180°, resulting in a true differential signal. Therefore, S-parameters were measured between Port1 with a single-ended input and the + (or -) terminal of Port2 while the other Port2 terminal was terminated with a 50 Ω load (Fig. A.8). The measured amplitude and phase difference (imbalance) between S_{2+1} (S_{3+1}) and S_{2-1} (S_{3-1}) was <0.3 dB and

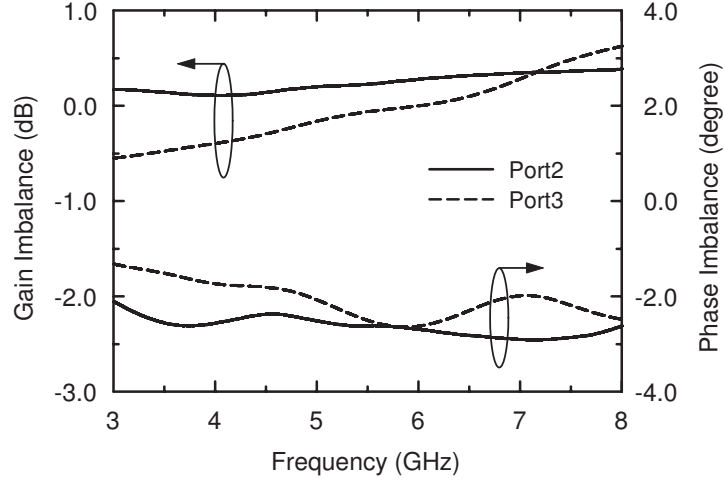


Figure A.8 Phase and amplitude imbalances of the Port2 and Port3

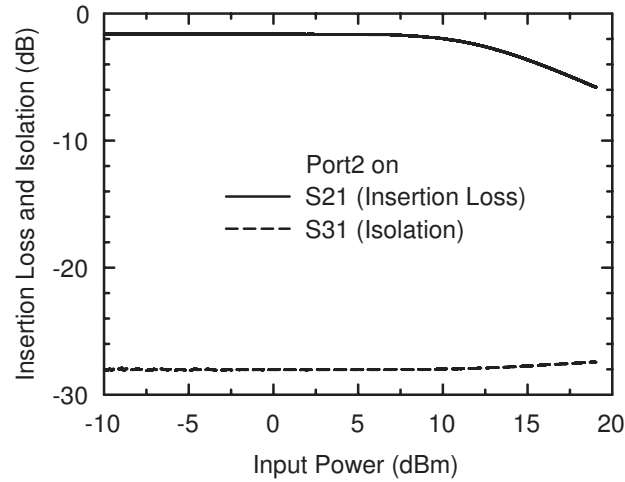


Figure A.9 Measured insertion loss (S_{21}) and isolation (S_{31}) versus input (Port1) power.

$<2.7^\circ$ at 5–6 GHz showing excellent balun operation.

Fig. A.9 shows the measured insertion loss and isolation of the switchable balun versus input power at 5.5 GHz. The main limitation of the power handling capability is a self-biasing effect in the nMOS transistors. Since the gate voltage of a nMOS switch is bootstrapped by the source and drain voltage due to the gate resistor (R_G), the off-state shunt switch is self-biased when the signal voltage is increased. The measured 1-dB compression point (P_{1dB}) of insertion loss (S_{21} with $V_C=0$ V) is 12 dBm when the input signal is Port1. The isolation of the switchable balun (S_{31} with $V_C=0$ V) remains better than 27 dB up to an input power of 20 dBm. To increase the power handling capability for a high power T/R switch, one can stack nMOS switches at the transmit port [100].

The stacked nMOS transistors equally divides the signal voltage, and the self-biasing effect occurs at a higher input power.

A.4 Summary

A new design concept of a switchable balun suitable for 5–6 GHz applications is presented. A transformer balun and an SPDT switch are integrated together using a commercial CMOS process. A differential spiral inductor is designed in order to have the center-tap at the outer winding for the second differential port, and nMOS shunt switches are used to select the differential port. The parasitic capacitances of the nMOS switches and an MIM capacitor are used to match the port impedances, resulting in a tuned transformer response. The measured insertion loss and isolation of the switchable balun are 1.6 dB and 28 dB, respectively at 5.5 GHz. The measured amplitude and phase imbalance are <0.3 dB and 2.7° , respectively, at 5–6 GHz, and the measured P_{1dB} is 12 dBm.

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