

**DESIGN TECHNIQUES FOR ON-CHIP GLOBAL SIGNALING OVER LOSSY
TRANSMISSION LINES**

by

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To Mom and Dad

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Abstract

This thesis describes techniques for global high-speed signaling over long (~10mm) lossy chip-serial transmission lines. With the increase in clock frequencies to multi-GHz rates, it has become impossible to move data across a die in a single clock cycle using conventional parallel bus-based communication. There are also reliability problems due to timing errors, skew, and jitter in fully synchronous systems. Noise, coupling, and inductive effects become significant for both intermediate length and global routing.

A new on-chip lossy transmission line technique is developed and new driver and receiver circuitry for on-chip serial links are described. High-speed long-range serial signaling is best done over transmission lines. However, because of the relatively high sheet resistance of metal interconnect layers, on-chip transmission lines tend to be lossy. Matched termination with resistors and the proper selection of the characteristic impedance of the transmission line structure can effectively suppress ISI. Fast digital CMOS technology allows pulsed mode data drivers to operate at multi-GHz rates. A phase-tuned receiver samples and de-serializes the received signal. Since the sampling instant is tuned to match the received signal eye, there is no requirement to match the clock and signal routing or clock and signal delays. A complete self-testing on-chip transceiver communicating over a 5.8mm on-chip transmission line is implemented in 0.13 μm CMOS and tested. The measured BER at 9Gbps is less than 10^{-10} .

Interleaving is usually necessary in high serial data rate serializer and de-serializer circuits. Multi-stage LC oscillators can be used to generate low phase noise multi-phases clocks required for interleaving. Conventional coupling between oscillators introduces out of phase currents, and this out of phase current causes a lower effective quality factor for each oscillator stage. However, capacitive coupling, a new technique, introduces in phase coupling between stages. Increased coupling with a ring of capacitors decreases phase spacing error dramatically and, in addition, the phase noise of multi-stages is also decreased thanks to in-phase coupling.

Chapter I

Introduction

The current globally synchronous clocking and signaling paradigm will fail as the number of transistors on an IC reaches the 1 billion mark. Although transistor feature size is expected to continue to scale for at least the next decade, power consumption, global signaling, and clocking have become critical problems that now prevent improvements in system performance, efficiency, and integration. The globally asynchronous locally synchronous (GALS) scheme within a *network-on-chip* paradigm is one of the long-term solutions, but this communications-centric methodology can only succeed with a fundamentally new approach to on-chip signaling.

According to the International Technology Roadmap for Semiconductors (ITRS), the rising integration levels and corresponding system complexity lead to “fundamental walls of performance, power consumption and heat dissipation” [1]. The current globally-synchronous signaling and clocking paradigm is largely responsible for an ever increasing portion of the total power consumption. The power consumed by synchronous global clocking has continually grown as integration levels increase and in some applications clocking alone already consumes 33-70% of the total power [2-4]. With multi-GHz clock frequencies, it has become impossible to move data across the die in a single cycle. In addition to these problems, there are also reliability problems due to timing errors, skew, and jitter in fully synchronous systems. Noise, coupling, and

inductive effects become significant for both intermediate and global routing. Buses are taking too much area, yet interconnect is reverse scaling [5] while the required communication bandwidth on an IC is growing exponentially.

The modular [6] or network-on-chip [7-9] approach advocated by the ITRS and others as a long term solution, is the one of the real alternatives. However, the ITRS also concedes that this *communications-centric* approach requires a significant change in communication architecture. In contrast to the traditional globally synchronous approach, the system is divided in GALS functional blocks or modules. The problems of global clocking are eliminated. Since the IC is now comprised of standalone modules, design complexity is reduced and IP reuse is facilitated. Substantial power savings can be achieved by independently setting (and adjusting) the power supply voltage and clock frequency to the modules. Despite these advantages, the modular approach places a far greater burden on communication. Robust communication between asynchronous network components is difficult using present techniques. Modern techniques will also be stretched to their limits to provide adequate local communication.

This chapter summarizes some of the work that has been done by others to mitigate the problems of on-chip signaling. Much of the research in this area has been focused on the analysis and design of on-chip wires. Differential signaling structures are an attractive solution at high frequency. Work has been done to minimize the area and maximize the bandwidth of differential structures. It has been shown that resistive termination extends the bandwidth to three times that compared to the case with capacitive termination. Pre-emphasis is another way to increase the bandwidth of on-chip wires.

A recently proposed architectural approach that uses modulation techniques for on-chip data transmission is described. Skewed pulsed buses and the use of dual VDD buffers, introduced to save power in conventional bus based links, are presented.

1.1. On-chip wires

On-chip wires can be modeled as distributed RC or RLC networks depending on the operating frequency, or as distributed LC networks at high frequency[10] if the wires are constructed with low resistivity, thick top metal. Since differential signaling is noise insensitive and shows better performance than conventional single-ended signaling, as the sensitivity of the receiver becomes smaller[11], differential signaling is attractive for long distance high frequency data transmission. Even though most long distance, on-chip, communication schemes employ differential signaling, the physical structure of differential wires varies greatly, depending on the operating frequency and the mode of operation.

The structure in Figure 1.1(a) [12] was designed based on an RLC model to transmit data at 3Gbps signals, over a 10mm long link. Both pre-emphasis and resistive termination are employed. Both the width, w , and the space, s , between lines are $0.4\mu\text{m}$, the bandwidth achieved for the cross section area is at it's maximum(t is the thickness of the signal lines, tt is the space between signal lines and thick top metal, and tb is the space between signal lines and bottom plane). An on-chip transmission line structure, Figure 1.1(b) [10] based on an LC model allows transmission of a 7.5GHz signal over a 20mm long link. The line width is $16\mu\text{m}$ and the space between lines is $2.1\mu\text{m}$. The characteristic impedance, Z_0 , of the transmission line in Figure 1.1(b) is proportional to

the $(L/C)^{0.5}$, and for a given distance between two lines, increasing the width of the lines decreases the characteristic impedance while, on the other hand, increasing the space between two lines with fixed metal width increases the characteristic impedance. Due to the low inductance and high capacitance of on-chip wires the characteristic impedance tends to be far less than 50 ohm.

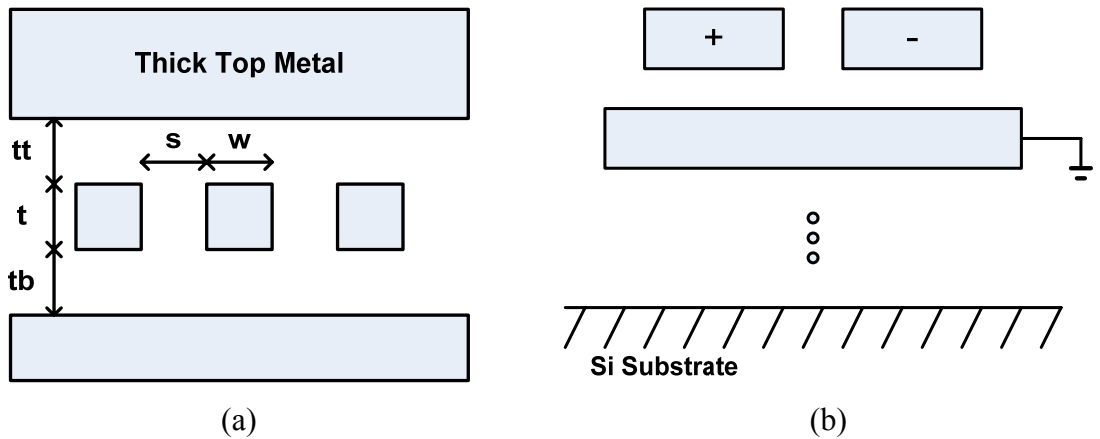


Figure 1.1: Physical structure of wires; (a) is designed based on the RLC model[12] (s is the space between signal lines and w and t are width and thickness of the signal lines respectively.) (b) is designed based on the LC model[10].

In a bus structure similar to that shown Figure 1.1(a) where the space between lines is not large, twists can be inserted in the differential links to cancel neighbor-to-neighbor crosstalk as shown in Figure 1.2. However, this scheme has the disadvantage of having extra series resistance because of the via connections, and the resistive loss can be problematic for data transmission at very high frequencies.

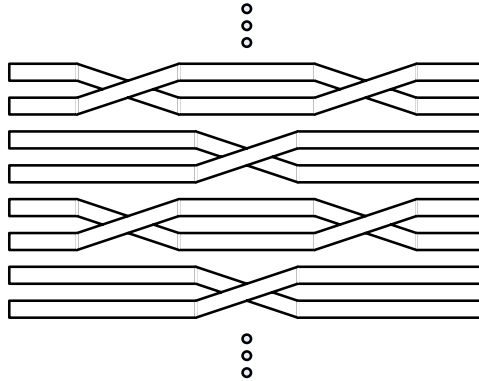


Figure 1.2: Twisted differential bus; This is effective to cancel neighbor-to-neighbor crosstalk.

With differential signaling, latency can be reduced by a factor of 2 by pre-equalizing the differential wires as shown in Figure 1.3 [13]. When clock is high, the charge on differential lines recycles between them, and when clock is low, the transmitter can send data to the receiver. Even though pre-equalizing the lines can save some time for the signal flight, the transmitter can only send data during half the period of the clock cycle, and pre-equalizing can also cause significant clock loading.

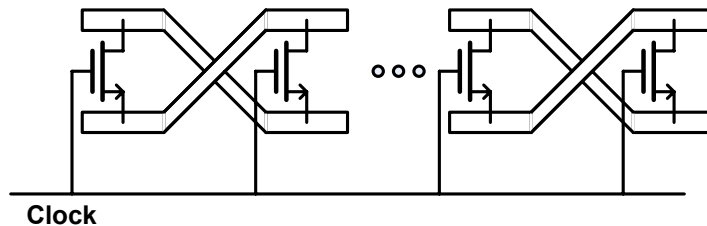


Figure 1.3: Differential line with distributed equalization[13]; When clock signal is high, both lines are set to same voltage (pre-equalizing), so data can be sent only during half the period of the clock cycle.

1.2. Termination

Since the effect of inductance is negligible for long and narrow interconnects, the transfer function can approximate with a first-order RC model, and with low ohmic

termination instead of conventional capacitive termination, three times more bandwidth is achieved[12].

The characteristic impedance of the differential line is:

$$Z_{diff} = 2\sqrt{\frac{L - L_m}{C + C_m}}, \quad (1.1)$$

where L , C , L_m , and C_m are the inductance, capacitance, mutual inductance, and mutual capacitance per unit length, respectively. Z_{diff} is exactly twice the characteristic impedance of a single line, Z_0 , if there are no mutual inductance and mutual capacitance. Figure 1.4 [14] shows a simple configuration for the driver and termination. A resistively loaded transmitter drives a long line which has characteristic impedance Z_{diff} , and there is a termination resistor connecting the two ends of the differential line. In order not to have reflection at both transmitter and receiver, the resistors should meet the following conditions.

$$Z_{diff} = R_L = 2Z_0 \quad (1.2)$$

If two resistors are used for termination at the receiver (one port of the resistor is connected to the end of the line and the other port is connected to the ground), the resistor value for each should be half of Z_{diff} , and this is the same value which is used for the load resistors at the transmitter. If there is a mismatch at the receiver, the reflected signal can be observed at the transmitter requiring source matching. However when the attenuation of interconnect is large, a large resistance can be used to improve output gain at the driver.

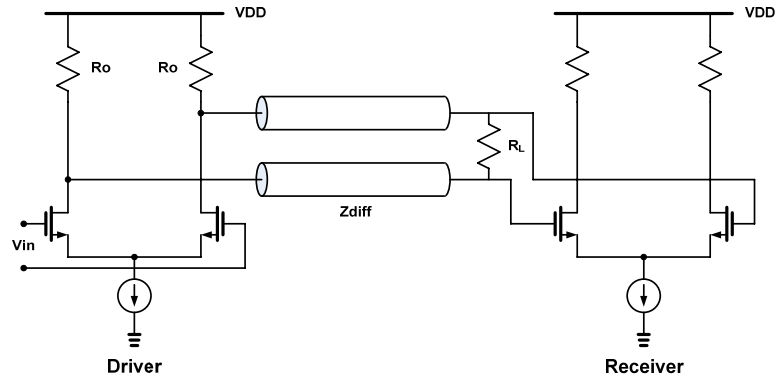


Figure 1.4: A simple configuration for the driving and termination[14]; Since the input differential pair in the data driver is operating at either off or saturation region, the output impedance of the data driver is approximately equal to the impedance of the load resistors. Therefore, same impedance for R_o and Z_{diff} allows impedance matching at the data driver.

1.3. Pre-emphasis and pulse shaping

Pre-emphasis can be used to extend the bandwidth of the wire and reduce inter symbol interference (ISI). Figure 1.5 shows two schemes, overdrive buffering [13] and pulse-width pre-emphasis[12]. The signal with overdrive buffering has a faster pulse rise time allowing higher data transfer rates to the receiver, while pulse-width pre-emphasis uses negative amplitude to reduce ISI. Both methods require extra circuitry for pulse shaping. Schematics of the two pre-emphasis schemes are shown in Figure 1.6. Figure 1.6(a)[13] was designed to generate low swing signals at the output and uses NMOS transistor for the pull-up to take advantage of faster speed compared to the case with a PMOS transistor pull-up. By using the high supply voltage for the logic circuits right before the drivers, the overdrive signals are generated. Figure 1.6(b)[12] is a circuit for the pulse width pre-emphasis signal generation. Sampling clocks, where the duty cycle can be controlled with bias current, generate a pulse width pre-emphasis signal by

sampling data and half period delayed inverted data at rising and falling edges alternatively.

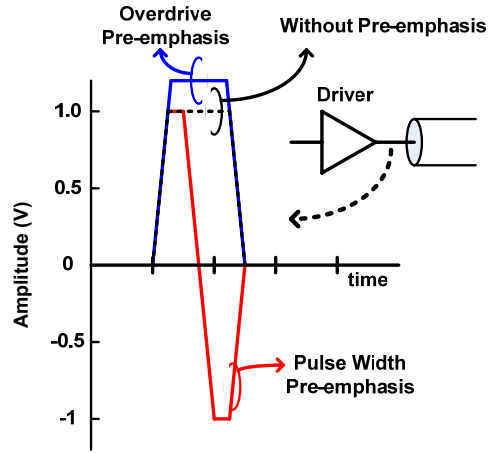


Figure 1.5: Pre-emphasis at the transmitter; overdrive buffering[13] and pulse-width pre-emphasis[12]

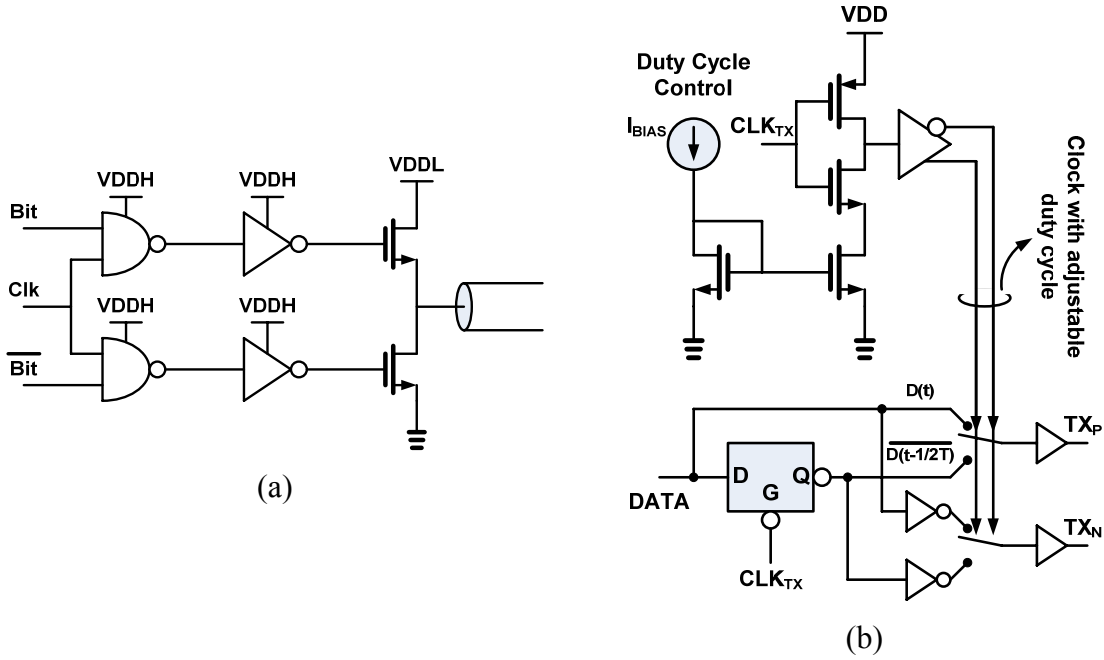


Figure 1.6: Pre-emphasis circuits; (a) Overdrive pre-emphasis[13] and (b) pulse width pre-emphasis[12]

1.4. Modulation

Modulation techniques [10] can be employed to send high speed data along the line. With conventional signaling a digital pulse at the end of a line has the power spectrum similar to that shown in Figure 1.7(a). Most of the signal power is concentrated at low frequency. However, because of the RC characteristic of a long line low frequency components travel slowly and the signal experiences frequency dispersion. At high frequency, the inductance of the wire dominates over the resistance, and the wire behaves like a waveguide (which can be modeled as distributed LC structure) allowing electromagnetic wave propagation. The wire velocity in Figure 1.7(a) and (b) increases with increasing frequency. Although conventional digital data has the spectrum power at all frequencies, the signal power can be restricted in a certain frequency range by using modulation and signals can take advantage of fast wire velocity and limited dispersion at high frequency.

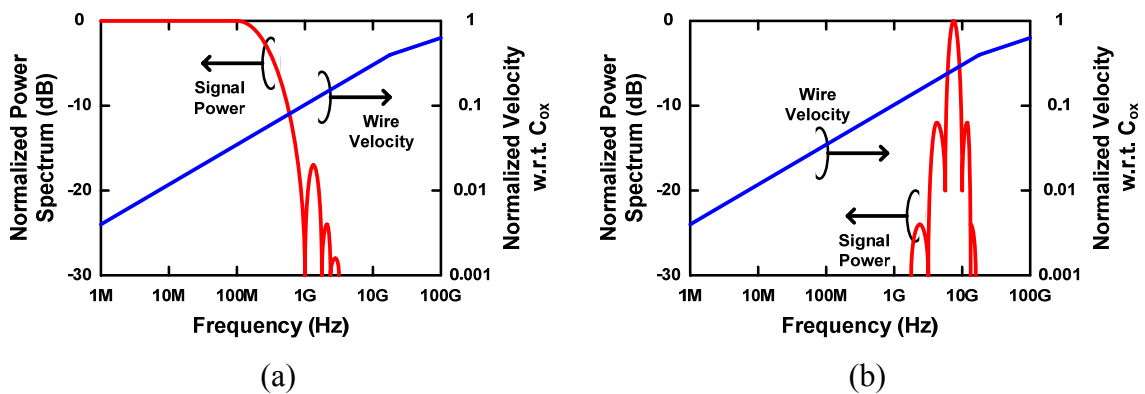


Figure 1.7: Frequency characteristics of conventional digital pulse (a) and modulated pulse (b) [10]

Figure 1.8 shows a simplified block diagram for a transceiver employing direct conversion. A differential input data signal is mixed with the local oscillator signal, and

the up-converted differential signal is driven onto the on-chip transmission line. There is another mixer at the receiver, to down-convert to the original input signal. 1GHz data were transmitted and received using a 7.5GHz local oscillator over 20mm long on-chip transmission line[10]. In this case, the speed for the data transmit was limited by the local oscillator frequency. Analog circuits such as mixers and LC oscillators can cause reliability problem in the presence of substrate and supply noise from digital circuitry.

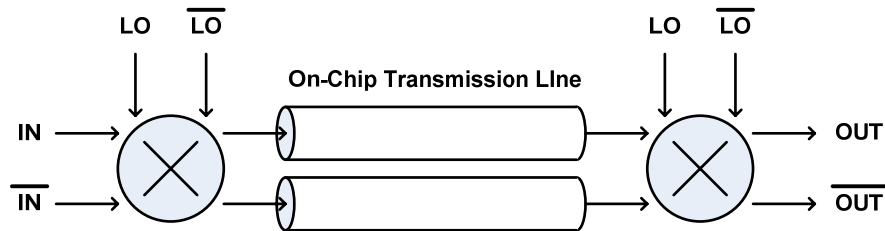


Figure 1.8: Simplified block diagram for the transceiver with direct conversion[10]; The transceiver has two mixers, one at the transmitter for the frequency up conversion and the other at the receiver for the frequency down conversion.

1.5. Skewed Pulsed Buses

Skewed pulsed buses[15] are designed to lower standby and active mode leakage power without any performance degradation. Non-critical paths in a circuit module are suited to this method. By using the high threshold (HVT) and low threshold (LVT) devices alternately and properly encoding the data pulses, the circuit can be designed to pass rising edges with fast LVT devices. During standby mode, leakage is only through HVT devices. As shown in Figure 1.9, a skewed pulse generator makes rising pulses for each input transition at the output of the XOR gates, and the rising pulses only follows fast LVT devices. During standby mode, the output of the XOR remains high, reducing the standby leakage power of the repeater chain since the leakage is only through HVT

devices. Simulations of a 2GHz, 8mm long, 8bit data bus, implemented in partially-depleted SOI 90nm technology with repeaters every 0.5mm, show the skewed pulsed bus has 20% less active mode leakage and 85% less standby mode leakage compared to a traditional bus structure.

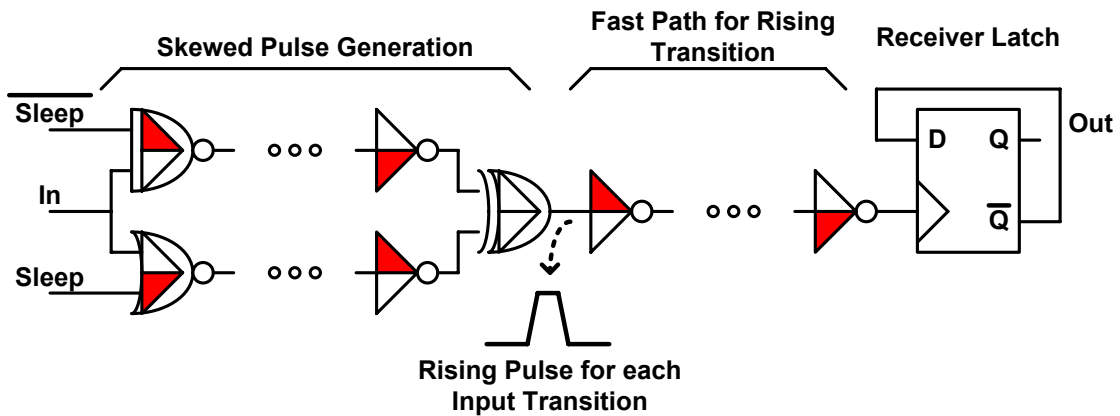


Figure 1.9: Skewed pulsed buses[15]

1.6. Dual VDD buffer

In dual VDD digital circuits, the repeaters in non-critical paths are designed with low VDD, which sometimes requires a large repeater size in order to meet the delay requirement. If the power consumption of a path is excessive due to the large size of the repeaters, it is better to use high VDD repeaters than to increase the size of the repeaters. Figure 1.10 [15] shows a low VDD buffer which has control circuits generating short pulses at the rising edge at the output port to help small sized PMOS, MP_{LO} , pull up. With a control circuit which has only two high VDD transistors, dual VDD buffers can use less area and less power than low VDD only buffers. With the same delay for both

the dual VDD buffer and low VDD buffer, the dual VDD scheme consume 16% less power, and the size of the dual VDD is 56% smaller than low VDD buffer.

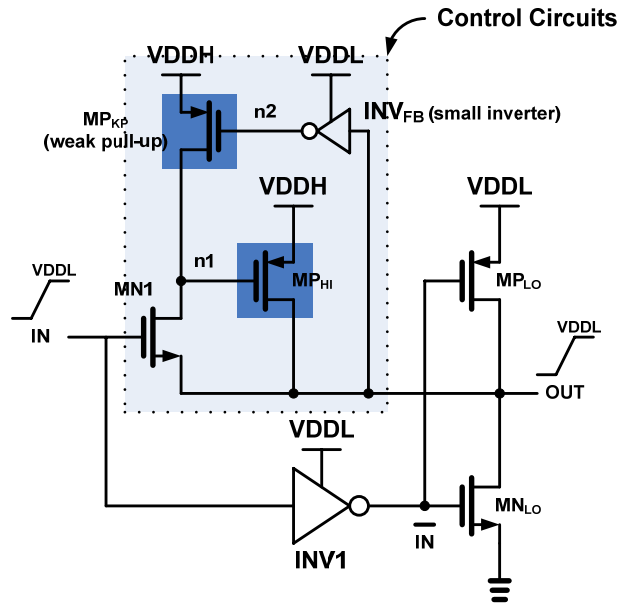


Figure 1.10: Dual-VDD buffer[15]

1.7. Dissertation outline

Some of the techniques suggested by others to improve the performance of on chip global links have been introduced. In the next chapter new techniques to increase the bandwidth of on-chip transmission lines are introduced. Techniques to generate multiple clock phases with low phase noise and low phase-spacing error are presented in Chapter III respectively. The design of an LC oscillator based PLL is explained in chapter IV. In chapter V the building blocks of a 9Gbps on chip transceiver are covered in detail. The design of a 20Gbps on-chip serial link is also presented. The thesis concludes in chapter VI with a summary and suggestions for future works.

Chapter II

On-chip parallel and serial links

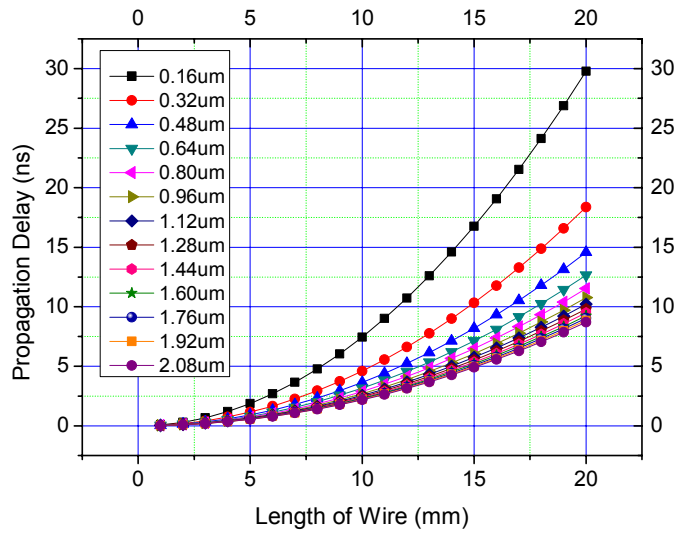
Metal resistivity in conventional CMOS, poses significant challenges to implementing transmission lines for long range (~ 1 cm), on-chip, digital communication. Series resistance causes dispersion, leading to considerable inter-symbol interference (ISI). Dispersion is caused by differing propagation velocities for the low frequency slow-wave (i.e. RC) propagation mode and higher frequency TEM mode [16]. For an on-chip 1cm link, the breakpoint between these two modes can be as high as several GHz. Others have avoided this problem by up-converting to a limited frequency band within the high frequency TEM region [17]. Significant dispersion is avoided by utilizing only a narrow band at high frequency; however, this approach adds complexity to the link and utilizes only a fraction of the potential bandwidth. Another solution is to use very thick, non-standard, metal interconnect lines. In [18], a 50 GHz bandwidth is achieved over a 20 mm link implemented as a coplanar transmission line, formed with a very thick ($5 \mu\text{m}$) non-standard metal layer. We compare a standard parallel-bus design scheme for a conventional 130nm CMOS process and an on-chip transmission line scheme. With same throughput, parallel and serial links are compared in terms of area and power.

2.1. Bus bases global link

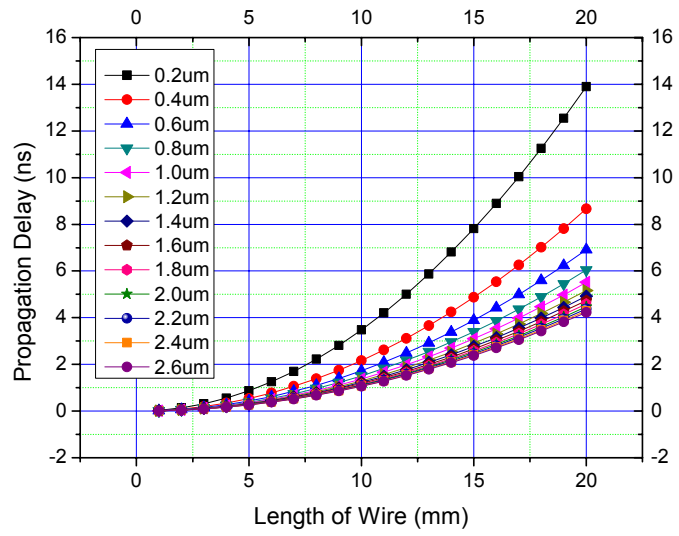
2.1.1 Propagation delay, t_p

The propagation delay, t_p , for a step response is defined as the time for the voltage to rise from 0 to 50% of the final level. Depending on the model used for the RC network, the delay is $0.69RC$ with a lumped RC model and $0.38RC$ for a distributed RC model, where R and C are total resistance and capacitance respectively[19].

The resistance, r , per micron length of a minimum width wire M1 in $0.13\mu\text{m}$ CMOS is $\sim 3\Omega/\mu\text{m}$, while the capacitance, c per micron length, of the same metal is $60\text{aF}/\mu\text{m}$. The propagation delay of the wire is $t_p=0.38RC=0.38rcL^2$ and is proportional to the square of the length. Figure 2.1(a) shows the propagation delay of M1 metal for different lengths and widths. For the minimum width, the propagation delay is about 30ns for a 20mm long line. For a line of twice the minimum width, the delay falls to 16ns for the same length. Figure 2.1(b) shows the propagation delay of over M2 metal lines for different line lengths and widths. For the minimum M2 line width, $0.20\mu\text{m}$, the propagation delay is about 14ns for a 20mm long line. This delay is approximately the same as the delay for an M1 line with a width of $0.48\mu\text{m}$. Using top metal layers has advantage of reducing the propagation delay dramatically, but without using large area since top metal has low resistance due to its increased thickness and lower capacitance due to the increased distance between metal layer and the substrate. However the resistance of vias should be considered when higher metal layers are used..



(a)



(b)

Figure 2.1: Propagation delay for different M1 wire widths versus length in (a) and M2 wire widths versus length in (b)

2.1.2 Optimum number of repeaters, m_{opt} , and minimum propagation time, $t_{p, min}$

From Spice simulation, the intrinsic delay of a minimum sized inverter, t_{p0} , is 21ps. If R_d and C_d , are the equivalent on-resistance and input capacitance of a minimum sized repeater, then the optimum number of repeaters to achieve minimum delay, and minimum propagation time is given by the following equations[19]:

$$m_{opt} = L \sqrt{\frac{0.38rc}{0.69R_d C_d (\gamma + 1)}} = \sqrt{\frac{t_{pwire(unbuffered)}}{t_{p1}}} \quad (2.1)$$

$$t_{p, min} = (1.38 + 1.02\sqrt{1 + \gamma})L\sqrt{R_d C_d rc} \quad (2.2)$$

where L is the length of the wire, r is the resistance per micron, and c is the capacitance per micron. $t_{p1} = 0.69R_d C_d (\gamma + 1) = t_{p0}(1 + 1/\gamma)$ represents the delay of an inverter for a fan-out of 1 and γ is the ratio of intrinsic output capacitance and input gate capacitance of the inverters, C_{int}/C_g (≈ 1).

With $\gamma = 1$, t_{p1} becomes $2t_{p0}$, 42.5ps, and $t_{p, min}$ becomes

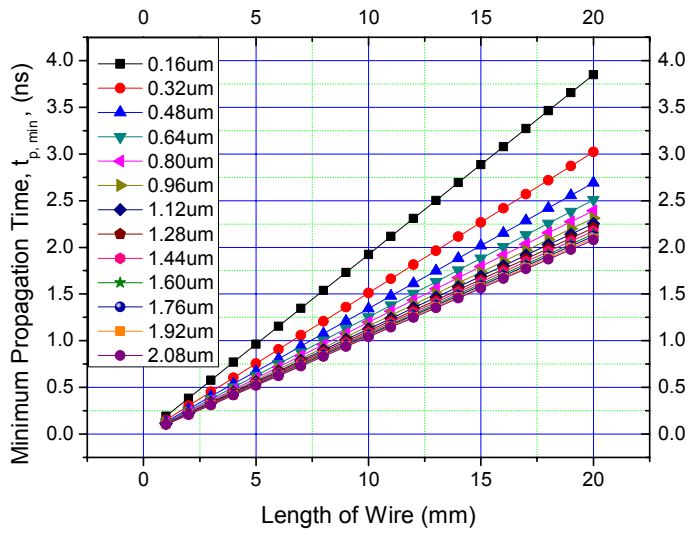
$$t_{p, min} = 3.42L\sqrt{R_d C_d rc} \approx 3.42\sqrt{t_{pwire(unbuffered)}t_{p0}} \quad (2.3)$$

The minimum propagation time, $t_{p, min}$, in (2.3) with the 21ps of the intrinsic delay of a minimum sized inverter, t_{p0} , from Spice simulation and with the unbuffered propagation delay time, $t_{pwire(unbuffered)}$ in Figure 2.1(a) and (b) are shown in Figure 2.2(a) and (b) respectively.

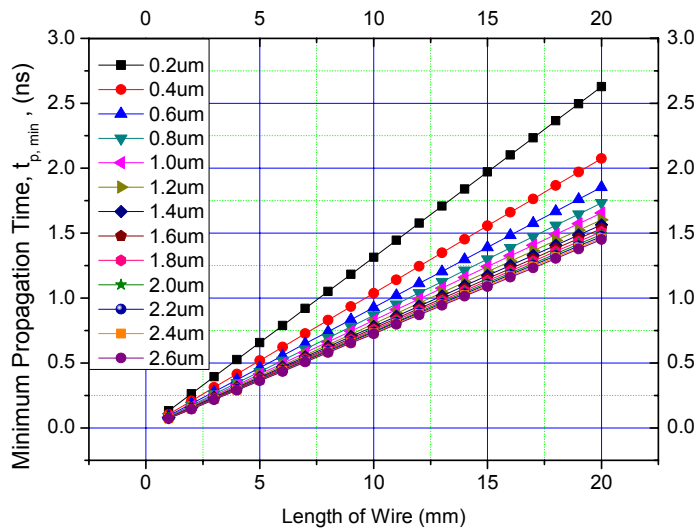
The minimum propagation time for an M1 wire with an optimum number of inverters and with a minimum width, $0.16\mu\text{m}$, is about 4ns in Figure 2.2(a), while the original propagation time for the same line without inverters is about 30ns (Figure 2.1(a)). As shown in Figure 2.2(b) the minimum propagation time for an M2 wire with an

optimum number of inverters and with a minimum width, $0.2\mu\text{m}$, is about 2.7ns , while the original propagation time for the same line without inverters is about 14ns (Figure 2.1(b)).

The number of repeaters for the minimum propagation time with $0.16\mu\text{m}$ M1 wire and $0.2\mu\text{m}$ M2 wire are 27 and 18 respectively from (2.1) as shown in Figure 2.3(a) and (b). Since the number of repeaters with $0.48\mu\text{m}$ M1 wire is 18 in Figure 2.3(a) which is equivalent to the number of repeaters with $0.2\mu\text{m}$ M2 wire, using a higher metal is more efficient in terms of area and power.

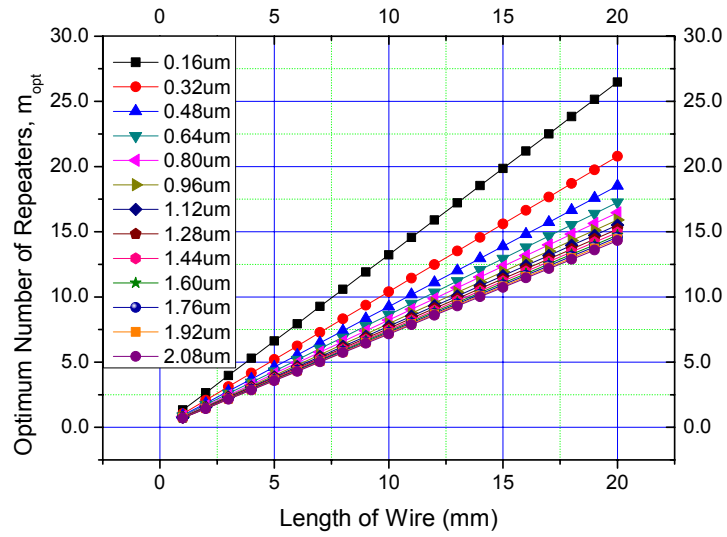


(a)

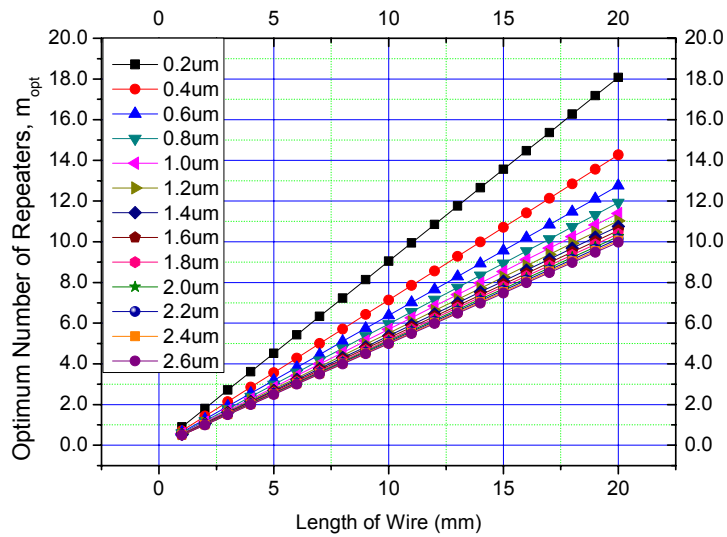


(b)

Figure 2.2: Minimum propagation time for different lengths, with smallest inverter from standard cell library, and metal wire, M1 in (a) and M2 in (b)



(a)



(b)

Figure 2.3: Optimum number of minimum-sized standard-cells repeaters for different widths metal wire M1 versus length in (a) and for different widths metal wire M2 versus length in (b).

2.1.3 Sizing

Sizing the repeaters is essential to reduce the delay. The optimum repeater sizing factor, S_{opt} , is defined as [19]

$$S_{opt} = \sqrt{\frac{R_d c}{C_d r}}. \quad (2.4)$$

For an M1 wire 0.16 μm wide, r is 3.2 $\Omega/\mu\text{m}$ and c is 60aF/ μm . Since the input capacitance of minimum inverter, C_d , is 1.4fF, the equivalent on resistance of the minimum sized inverter, R_d , can be derived from $t_{p0} = 0.69R_d C_d$ and becomes 22kOhm. Therefore, the sizing factor, S_{opt} , is 17.14, and inserting 27 of these sized inverters achieves the minimum delay for the 20mm M1 link.

2.2. Serial global link

2.2.1 Skin depth

At high frequencies the effective resistance of metal wires becomes frequency dependent due to the skin effect. The skin depth, δ , is defined as the depth where the current density falls to a value of e^{-1} of its nominal value, and is given by

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \quad (2.5)$$

where f is the frequency of the signal, and μ is the permeability of the surrounding dielectric. Due to the small thickness of on-chip metal wires, the skin effect is an issue only for wider, thicker wires. Also better conductors such as copper tend to suffer from the skin effect at lower frequencies. Figure 2.4 shows the frequency of each metal wire

where the skin effect starts to appear. In a 130nm CMOS technology two copper wires such as E1 and MA show skin depth transition points of only 507MHz and 443MHz respectively.

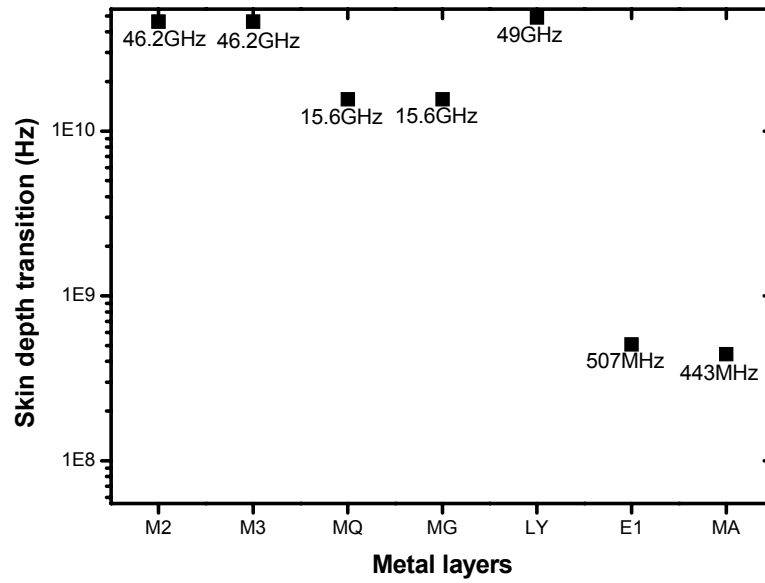


Figure 2.4: Skin depth transition

2.2.2 Characteristic impedance

The characteristic impedance of a transmission line [20] is

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (2.6)$$

$$\approx \sqrt{\frac{L}{C}} \quad (2.7)$$

$$\approx \sqrt{\frac{R + j\omega L}{j\omega C}} \quad (2.8)$$

where R , L , G , C are series resistance, series inductance, parallel conductance, and parallel capacitance per unit length respectively. If the line is low-loss we can assume that $R \ll \omega L$ and $G \ll \omega C$, and the characteristic impedance is given by the equation (2.7) approximately. In the case of a lossy on-chip transmission line, equation (2.8) is more appropriate for the characteristic impedance, since R is comparable or even larger than ωL , but often equation (2.7) is still used for simplicity. The differential on-chip transmission line structure used in this investigation is shown in Figure 2.5. A strip-line rather than a coplanar structure gives better isolation from crosstalk. Figure 2.6 shows the characteristic impedance for various configurations of transmission line - the signal line is implemented on the MG layer and the ground plane is implemented with the M1, M2, M3, and MQ layers. The characteristic impedance is given for different line widths and line spacings and ranges from 10Ω to 70Ω . Implementing the ground plane with the M1 layer tends to give the largest characteristic impedance due to the reduced capacitance between signal lines and ground plane. Either decreasing the width of signal lines or increasing the space between signal lines increases the characteristic impedance, but decreasing the width of signal lines also increases the resistance of the metal wires.

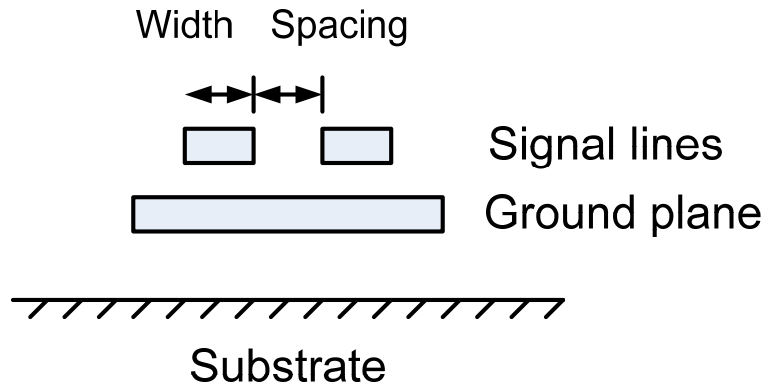


Figure 2.5: On chip transmission line structure

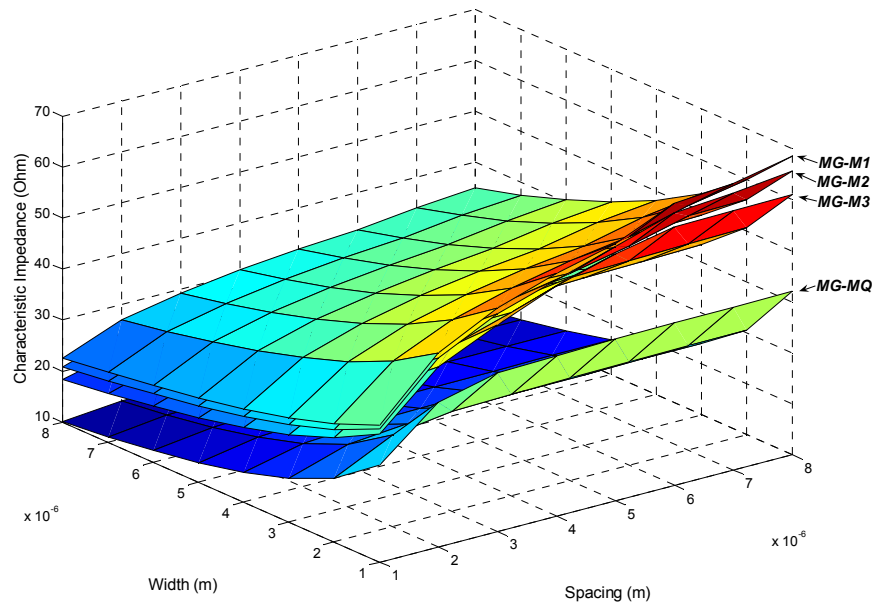


Figure 2.6: Characteristic impedance for MG transmission line with different line widths and line spacing

2.2.3 Length of the transmission Line with matched termination

Due to resistive losses, the response of a lossy transmission line shows both wave propagation and diffusion. A step input propagates as a wave through the line, and the

amplitude of this traveling wave is attenuated along the line with a value at x given by:
[19]

$$V_{step}(x) = V_{step}(0)e^{-\frac{r}{2Z_0}x} \quad (2.9)$$

The arrival of the wave is followed by a diffusive relaxation to the steady-state value at point x : [21, 22]

$$V_{steady-state}(x) = \frac{Z_0}{rx + Z_0} \quad (2.10)$$

Figure 2.7 shows the point where the initial step voltage is same as the steady-state voltage. Increasing the characteristic impedance by widening the space between signal lines allows a longer transmission line due to the decreased total line resistance, but on the other hand increasing the characteristic impedance by reducing the width of signal lines (this is a way to increase total line resistance) reduces the length of transmission line.

Figure 2.8 shows the step response of two lossy transmission lines where *outA* is the output of short transmission line, while *outB* is the output of a very long transmission line. The amplitude of the step due to the wave propagation in Figure 2.8 decreases exponentially along the line, and so that the effect of wave propagation cannot be observed with the very long lossy transmission line. *outA* shows step due to wave propagation followed by a diffusion component, but *outB* shows only a diffusion component since the wave propagation is not apparent due to the large resistance of the line. A transmission line only can be used properly if it shows wave propagation. Since a serial link using a transmission line takes advantage of wave propagation, the maximum

allowable length of transmission line is where the voltage level of the wave propagation equals the minimum allowable voltage level at the receiver.

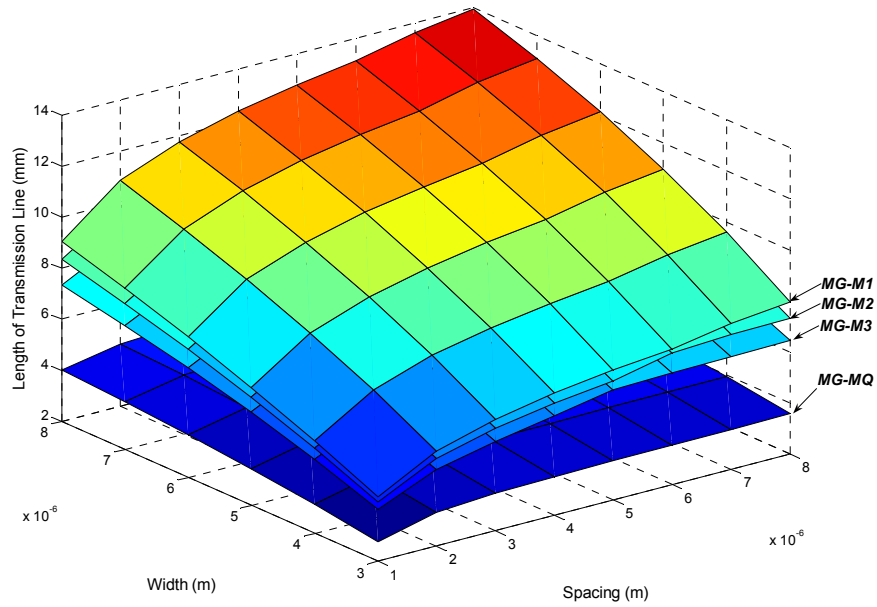


Figure 2.7: Length of transmission line at different widths and spacing with signal line MG (M5)

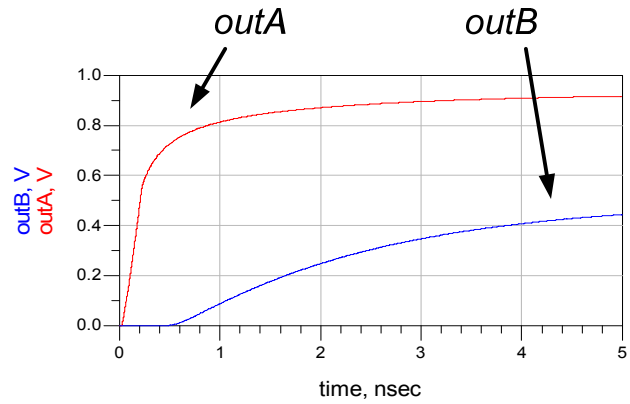


Figure 2.8: Step response of a lossy transmission line; *outA* is output at the end of a short transmission line and *outB* is output at the end of a long transmission line

2.2.4 Area

Using a lower metal layer as a ground plane increases the characteristic impedance due to the reduced self capacitance. However, the increased space between signal lines and ground planes requires a wider ground plane in order to contain electric fields; therefore, the widths of both the transmission line and the ground plane becomes larger. Figure 2.9 shows the overall width of the transmission line for different line widths and spacings.

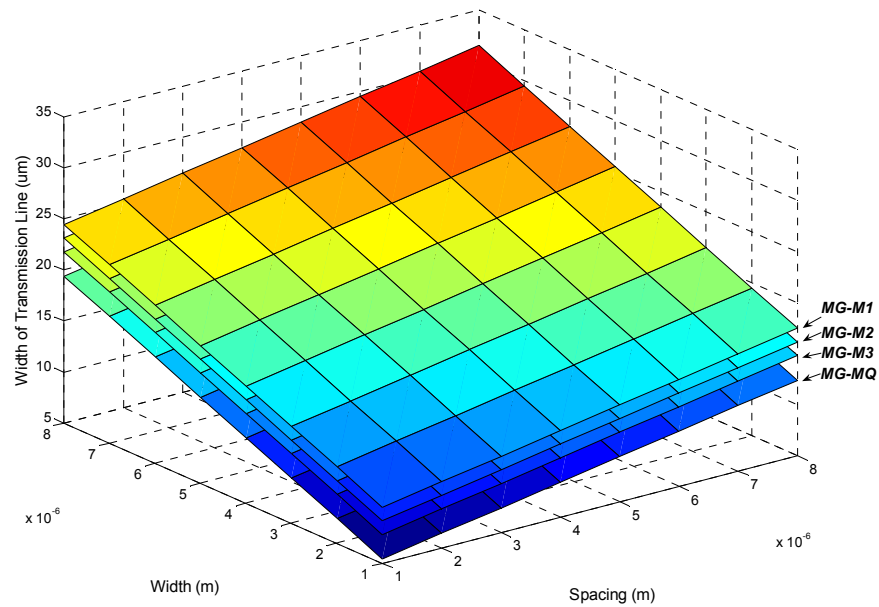


Figure 2.9: Width of transmission line for different widths and spacing with signal line MG (M5)

2.3. 20mm link design example

2.3.1 Parallel bus design

For simplicity, a 20mm long M1 bus with minimum width wires ($0.16\mu\text{m}$) is used in the parallel bus design. The propagation delay without repeaters is about 30ns as shown in Figure 2.1, but with 27 repeaters the total delay is reduced to 4ns as shown in Figure 2.2 and Figure 2.3. For a 1.25GHz operating frequency the signal cannot reach the end of the line in one clock cycle. Therefore flip-flops are required to retime the signal. Considering the setup time and the internal time delay of the flip-flops we can allow 650ps of propagation time between flip-flops. 6 clock cycles are required for the signal to travel the entire length of the line. Two designs are shown in Figure 2.10. Four inverters are inserted between flip-flops in Figure 2.10(a), and three inverters are inserted in Figure 2.10(b). Since the length of line between flip-flops is same for both designs, the inverters in Figure 2.10(a) and Figure 2.10(b) drive $667\mu\text{m}$ and $834\mu\text{m}$ long lines respectively. Spice simulation results of the design of Figure 2.10 are shown in Figure 2.11. Figure 2.11 shows the clock signal, the output of first flip-flop, and the input to the second flip-flop for each case. In the case of 3 inverters (Figure 2.11(a)) the internal delays from the flip-flop are 125.4ps and 134.4ps for the rising and falling output signals respectively, and the average propagation time between flip-flops is 498.45ps $((485.5\text{ps} + 511.4\text{ps})/2)$.

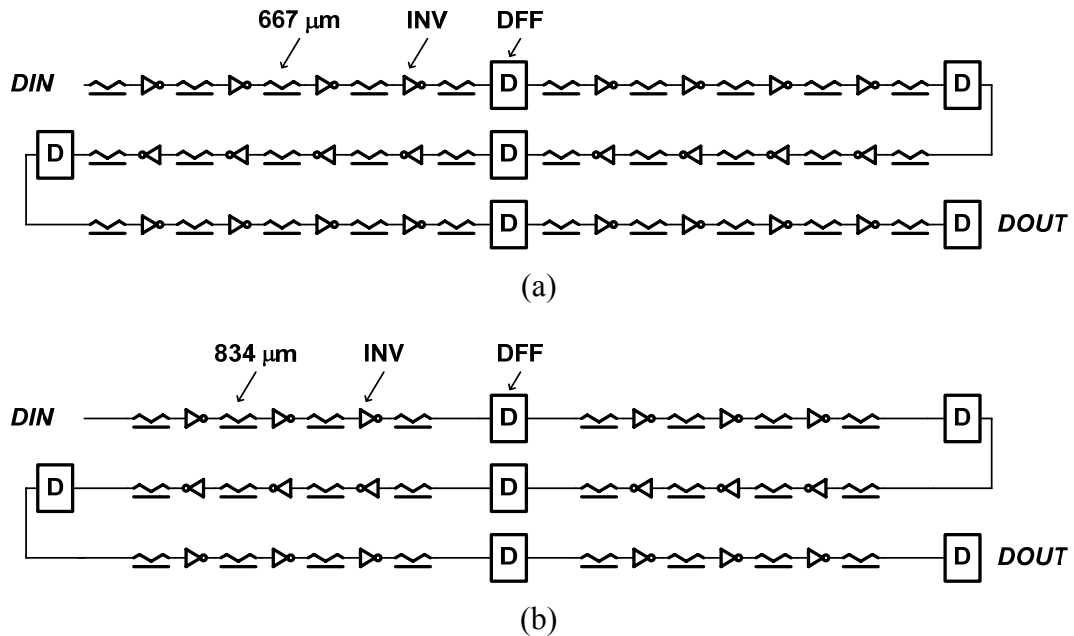
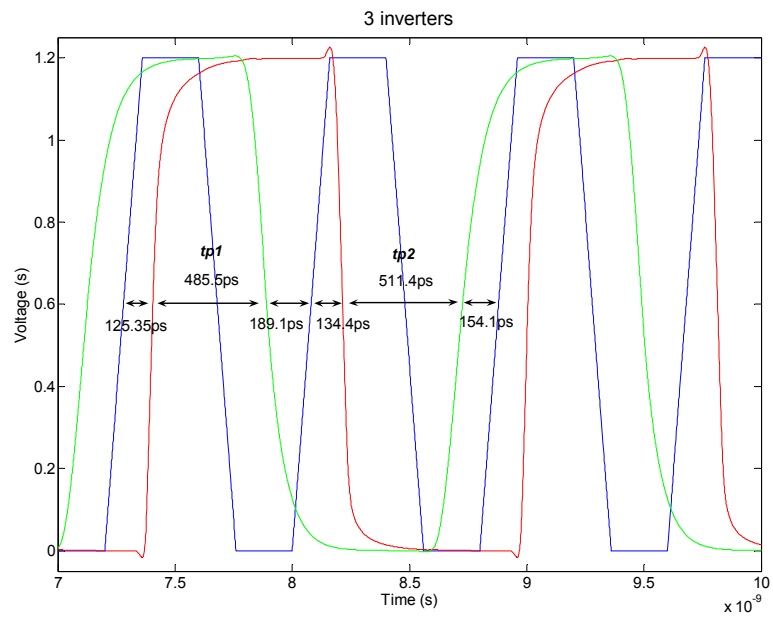
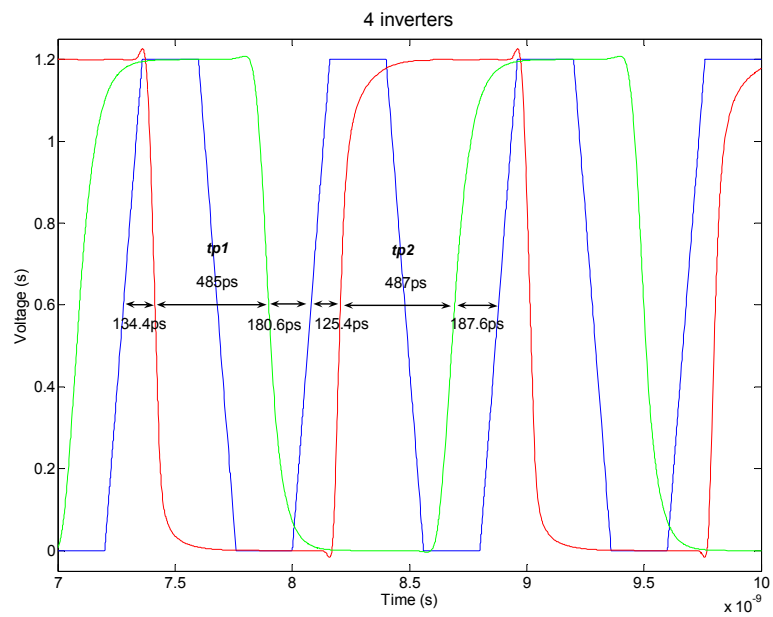


Figure 2.10: Parallel bus designs;(a) 4 inverters and (b) 3 inverters between flip-flops

Table 2.1 summarizes the average propagation delay time and total current for the 8bit parallel bus. A range of currents is given for no bus activity to full activity. Although there is not much difference in the delay time with different numbers of inverters between flip-flops, the minimum average propagation time is achieved with 5 inverters between the sets of flip-flops. Calculations show the optimum number of repeaters for the minimum delay is 27, or just over 4 inverters between flip-flops. As the numbers of inverters between the flip-flops grows, the total current also increases accordingly. However, the current for zero activity is almost the same for all designs since in this case most of the current is consumed by the flip-flops which are still active at every clock edges (each design has the same number of flip-flops).



(a)



(b)

Figure 2.11: Spice simulations with (a) 3, (b) 4 inverters between flip-flops

Table 2.1 Propagation delay and total current of parallel buses

Number of inverters	Average propagation delay time between flip flips; $(tp1+tp2)/2$	Total current of 8 bit parallel buses (VDD=1.2V, F=1.25G)
3	498.45ps	1.587mA ~ 13.778mA
4	486ps	1.599mA ~ 14.622mA
5	484.3ps	1.581mA ~ 15.458mA
6	488.75ps	1.600mA ~ 16.292mA

2.3.2 20mm serial link design

In order to minimize the skin effect and to save area, the MG layer is selected as signal line. For the transmission line the bottom metal layer M1 is selected as ground plane. With a 6 μ m line width and 3 μ m space between signal lines, the initial step voltage due to wave propagation is same amplitude as the steady-state voltage around 10mm from the transmitter. However, actual signal can propagate much further than that point. A 20mm long transmission line is terminated with 33 Ω resistors as shown in Figure 2.12(a). A pulsed mode transmitter in chapter V is used to transmit 10 Gbps signals, and the eye diagram at the end of the transmission line is shown in Figure 2.12(b).

Using a characteristic impedance of 33.4 Ω and 1.2 V signaling, the upper limit of the power delivered to each half line is given by (2.11):

$$P_{in} = \frac{1}{2} \frac{V_{S,rms}^2}{Z_o} = \frac{1}{2} \frac{0.849^2}{33.4} = 10.79mW \quad (2.11)$$

And the lower limit of the power is given by (2.12):

$$P_{in} = \frac{1}{2} \frac{V_{S,rms}^2}{R_{line,total} + R_L} = \frac{1}{2} \frac{0.849^2}{167.4 + 33.4} = 1.795mW \quad (2.12)$$

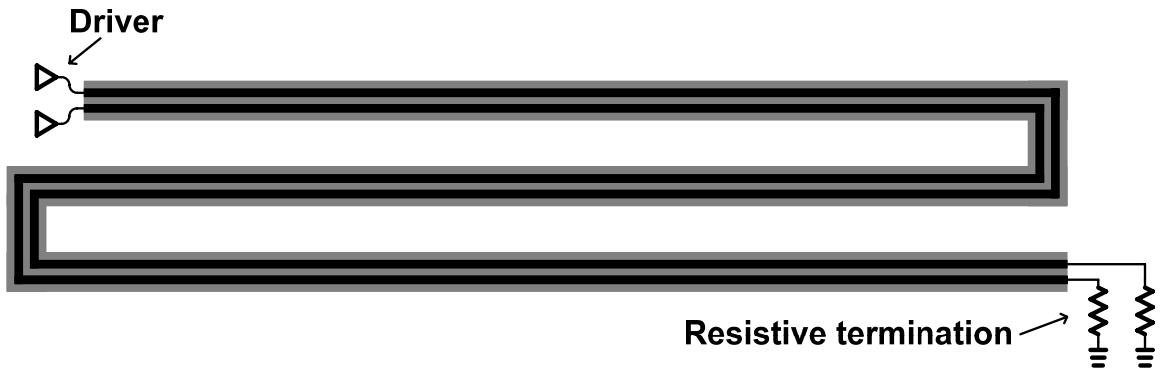
The total supply current consumption of the serial line driver and the current delivered to the transmission line are summarized in the Table 2.2. All three line drivers

are pulsed mode type, and drive 20mm transmission lines. The drivers at 10Gbps and 20Gbps have extra circuitry to generate 10Gbps and 20Gbps pulses respectively since the original data generated at 1.25GHz can only be serialized up to the 5Gbps with standard digital cells. The total current is 6.239mA, 18.45mA, and 48.556mA for the 5Gbps, 10Gbps, and 20Gbps serial links, respectively. Compared to the increase of the current on the transmission line at high frequencies, the current increase for the driver is extremely large since it requires additional circuitry to generate high frequency pulses.

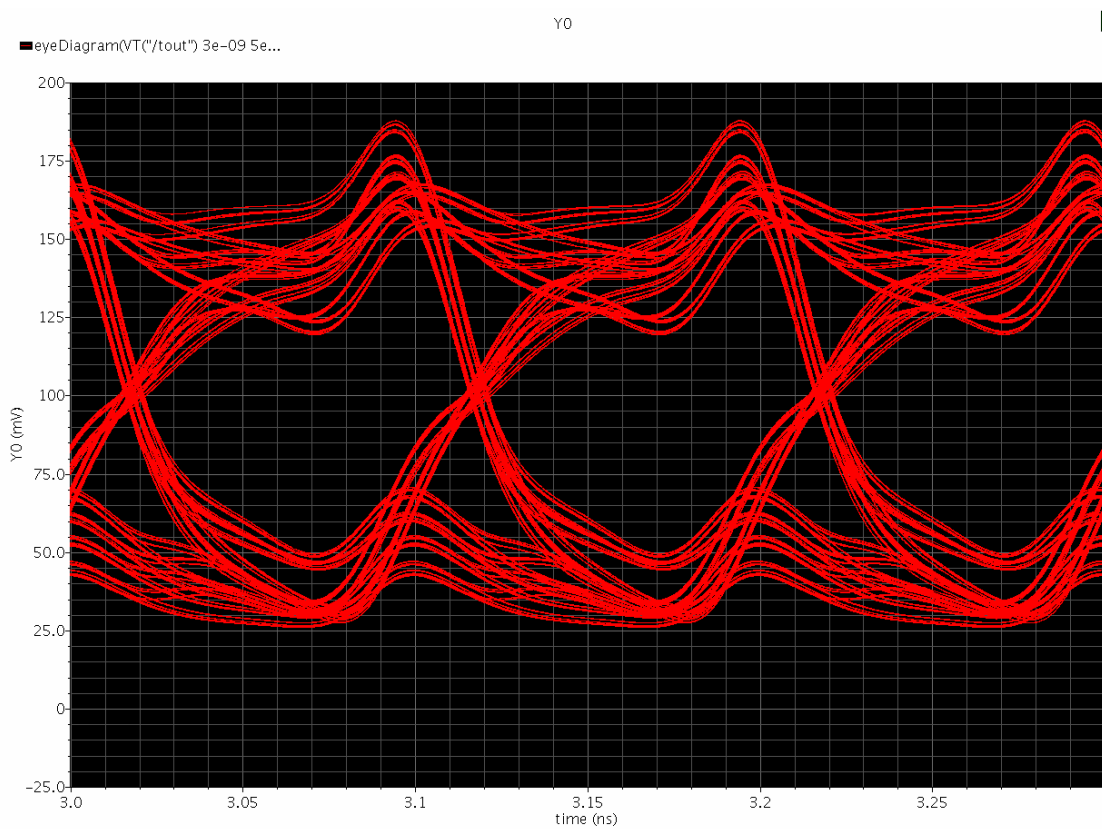
The simulated power consumption of the transmission line lies between the upper and lower boundary values in (2.11) and (2.12).

Table 2.2 Current on the serial link

Serial link	Total current	Current delivered to the transmission line
5Gbps	6.239mA	2.092mA
10Gbps	18.45mA	5.514mA
20Gbps	48.556mA	7.499mA



(a)



(b)

Figure 2.12: Serial link; (a) schematic, (b) eye diagram at the end of 20mm transmission line.

2.3.3 Comparison

Table 2.3 compares a 10Gbps serial link and an equivalent 8-bit-wide parallel bus. The area of the parallel bus, based on the size of standard cells, is 0.688mm^2 . The area of the serial link at 0.449mm^2 , is about 0.24mm^2 smaller than that of the parallel link.

For the power consumption comparison, both a parallel link with three inverters between each set of retiming flip-flops and serial link are driven by same 8bit PRBS generator. Since an N-bit PRBS generator generates a 2^N-1 long data sequence, the 8bit PRBS generator generates a repeating 255 bit data pattern. One of the eight bit outputs is shown in Figure 2.13. The average data transition rate is 4.016 bits out of 8 bits, corresponding to a 50.2 % activation rate.

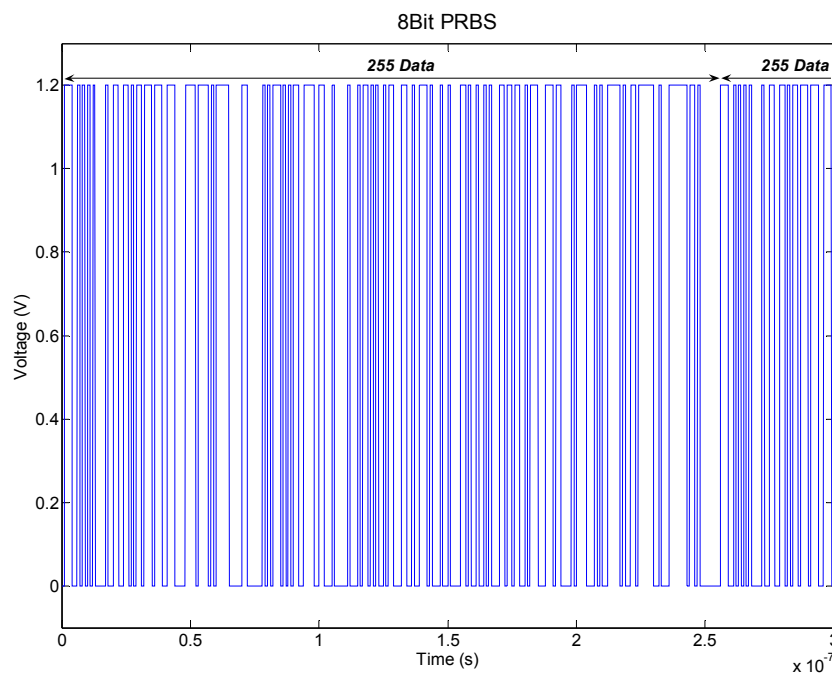


Figure 2.13: One of outputs of 8bit PRBS generator

The total supply current for the serial link is 18.45mA at 1.2V, with only 5.514mA used for the data transmission while the remaining current is for the serialization of two 5GHz data patterns to a single 10GHz data pattern.

The supply current for the parallel link is 6.806mA with the same PRBS input as used to test the serial link. The supply total current ranges from 1.587mA with a zero activation to 13.778mA with full data activity for the link with three inverters between flip flops. The relatively high current for a static input is due to the power consumption of the retiming flip-flops, which are continuously clocked.

With the serial link taking advantage of wave propagation, data can reach the end of the 20mm line only in 150.7ps, compared to 6 clock cycles (4.8ns) for the parallel link. The clock driver for the parallel link is not considered in this comparison. For the serial link the current consumption of the serializer (i.e. total current) is also given in the table.

Table 2.3 Compare serial and parallel links.

	Serial link (10Gbps)	Parallel bus (8bit 1.25Gbps)
Link Area	22.48 μ m X 20mm	34.4 μ m X 20mm
Current	Total Current : 18.45mA @ 1.2V Current on the transmission line : 5.514mA @ 1.2V	3 Inverters between DFFs : 6.806mA @ 1.2V (1.587mA ~ 13.778mA @1.2V)
Time delay for 20mm link	150.7ps	4.8ns 6 clock cycles (800ps X 6)

2.3.4 Conclusion

This chapter compares the power consumption, area and delay of an on-chip transmission line based serial link with that of a conventional, parallel bus link. Prototype 20mm 10Gbps links are designed with both approaches for 130nm CMOS.

The serial link requires a lower signaling power than the parallel bus except at low data activation rates. However, serialization adds considerably to the power required for serial signaling. Figure 2.14 compares the power required for a parallel and serial links designed for data rates of 5Gbps, 10Gbps, and 20Gbps. When the extra power required for serialization is considered the power consumptions are similar at 10Gbps. At 5Gbps the serial approach is more energy efficient, indicating a breakpoint somewhere between 5Gbps and 10Gbps. We expect this breakpoint to be larger in more advanced technology nodes since serialization becomes much more efficient in faster CMOS technology.

This study is not exhaustive since there are still some additional factors that might be considered. A parallel link using a wider or higher metal layer would most likely be more energy efficient. The current consumption required for a 20mm data transmission with the different M1 metal wire widths are shown in Figure 2.15. The widths of M1 are multiples of $0.16\mu\text{m}$. The current decreases from 6.8mA at the minimum width to 3.8mA with the $0.64\mu\text{m}$ wide metal wire. However, increasing wire width also increases capacitance, limiting the improvement in power consumption.

The use of higher level minimum width M5(MG)metal wires decreases current consumption to 2mA as shown in Figure 2.16. The use of higher metal layers decreases not only resistance but also capacitance because of the increased distance between the

metal layer to the substrate. However, on the other hand the clock power dissipation for the parallel link was not considered in those figures. Furthermore, the use of a pseudo-differential serial signaling scheme could significantly reduce the power required for serial signaling.

Since a serial link takes advantage of wave propagation, a serial link has a much shorter propagation delay than an optimally designed parallel bus. Our simulations show that the propagation delay for the serial link is more than an order of magnitude lower than that of the parallel link. This could be a key advantage in high performance applications, such as microprocessors and graphics processors. The area required for a serial link is slightly less than for an equivalent parallel link.

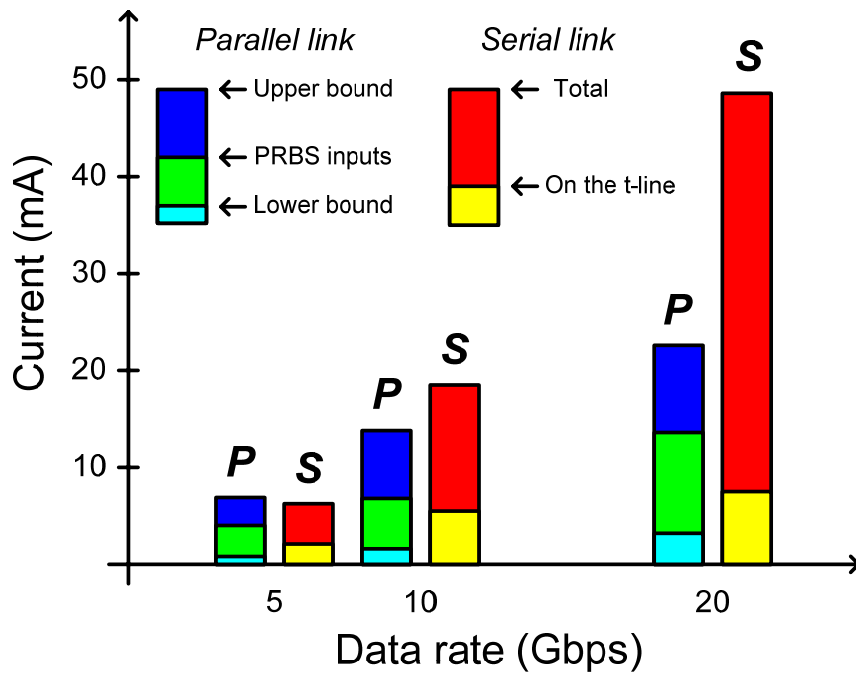


Figure 2.14: Current at the parallel and serial links at 5, 10, and 20Gbps

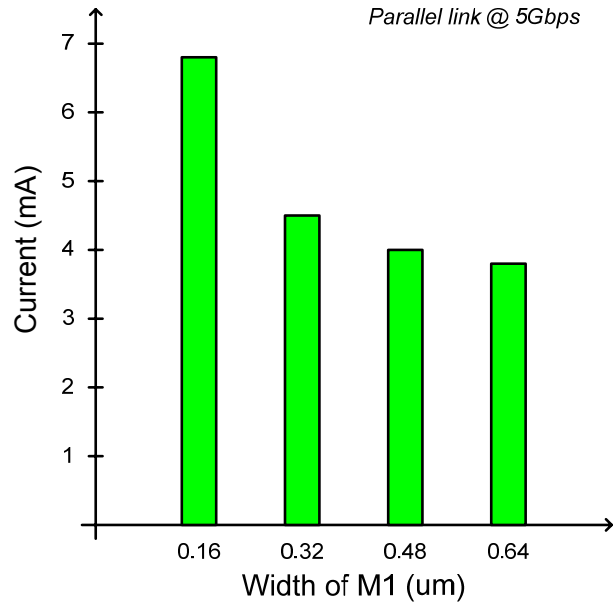


Figure 2.15: Current consumption of a parallel links for different widths of M1 with 5Gbps PRBS data

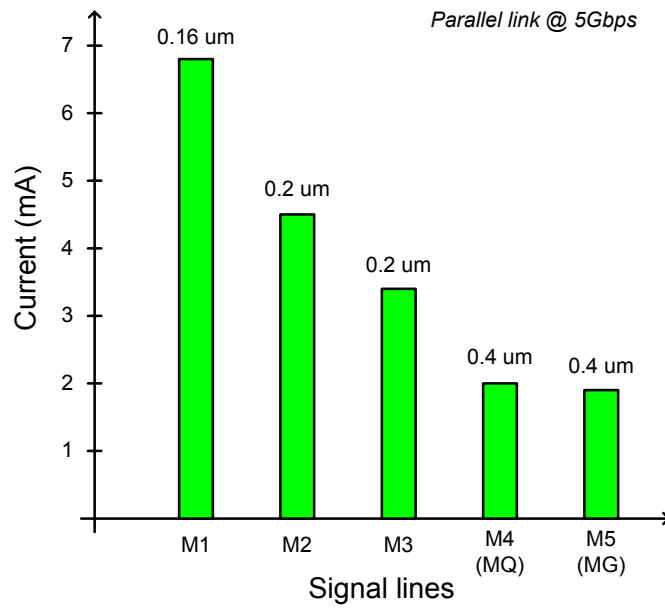


Figure 2.16: Current consumption of parallel links with different layer signal lines.

Chapter III

Multi-stage LC oscillators with capacitive coupling

Multi-stage oscillators[23] not only provide multiple phases, but also generate low phase noise clock signals, since the overall phase noise in a multi-stage oscillator is inversely proportional to the number of stages[24, 25]. Therefore, as the number of stages increases we can get lower noise, but at the expense of large area and power. Much research has been done to decrease the phase noise without further increasing the number of stages[25, 26]. Capacitive coupling for multi-stage LC oscillators, introduced here, is an efficient and simple method to decrease phase noise in multi-phase oscillators since unlike other forms of coupling it does not introduce an out-of-phase coupling current which can decrease phase noise, yet capacitively coupling is very effective in reducing phase spacing error [27]. The phasor diagram in multi-stage oscillators is first presented to explain the variation of the quality factor in multi-stages. Capacitive coupling is explained in detail.

3.1. Phasor diagram

3.1.1 Single stage LC oscillator

The voltage and current phase relationship for a single stage LC oscillator oscillating in steady-state is shown in Figure 3.1[28, 29]. Once oscillation starts, it takes some transient time to reach steady-state, and for the voltage and current phases in LC

tank to become in-phase as shown in Figure 3.1(b). The steady-state phase relationship also can be explained from an open loop model. The open loop model in the case of a single stage LC oscillator is shown in Figure 3.2(a). One of the oscillation conditions is a zero phase shift (or equivalently 360 degree phase shift) in the loop which includes the LC tank. Since LC tank is the only component contributing the phase in the loop, the total phase is same as the phase of the LC tank. Therefore, in order to achieve zero total phase in the loop the phase of the LC tank should be zero. From the amplitude and phase response of the transfer function of the LC tank in Figure 3.2(b) the operating point which satisfies zero phase in the loop can be decided. So, for a single stage LC oscillator, the steady-state oscillation stays at the point of zero phase with the oscillation frequency of $\omega_0, 1/(LC)^{0.5}$.

The LC tank achieves its maximum effective quality factor in case of single stage LC oscillator, since the effective quality factor is proportional to the slope of the phase and the operating point of zero phase is where the derivative of the phase over the frequency is maximum.

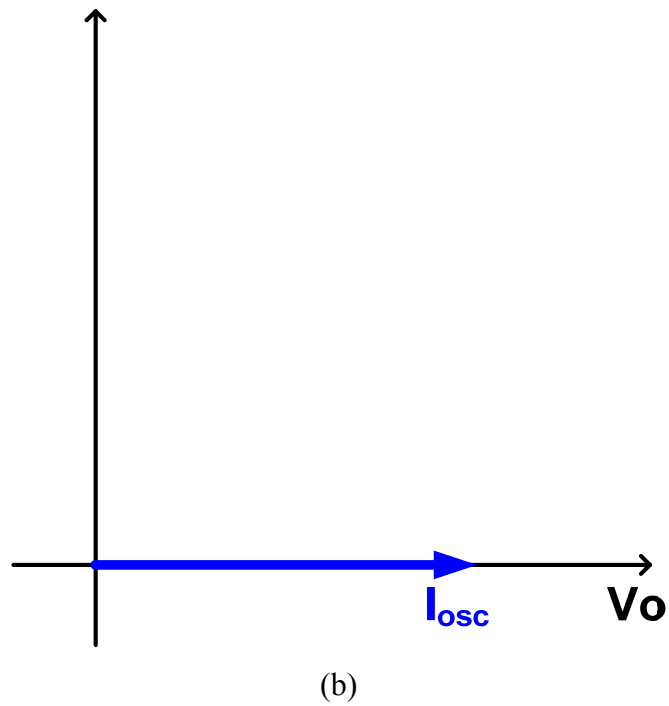
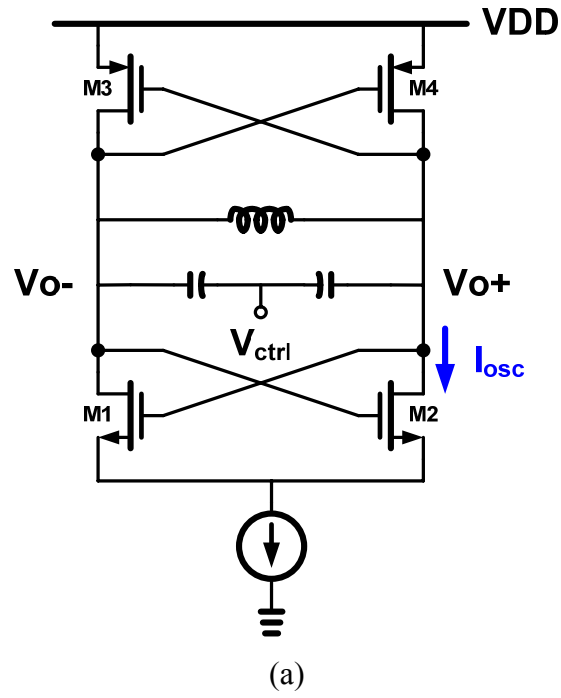
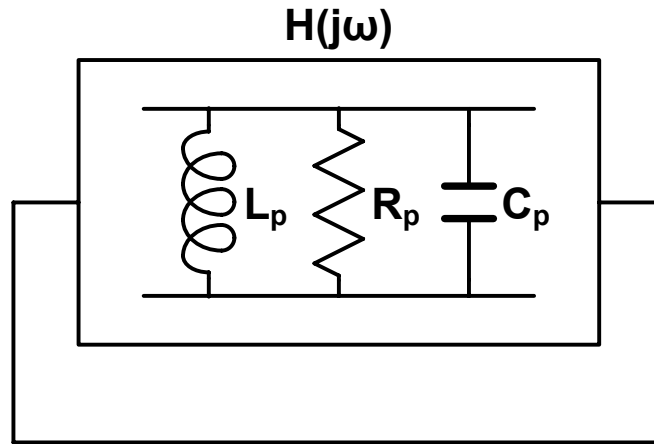
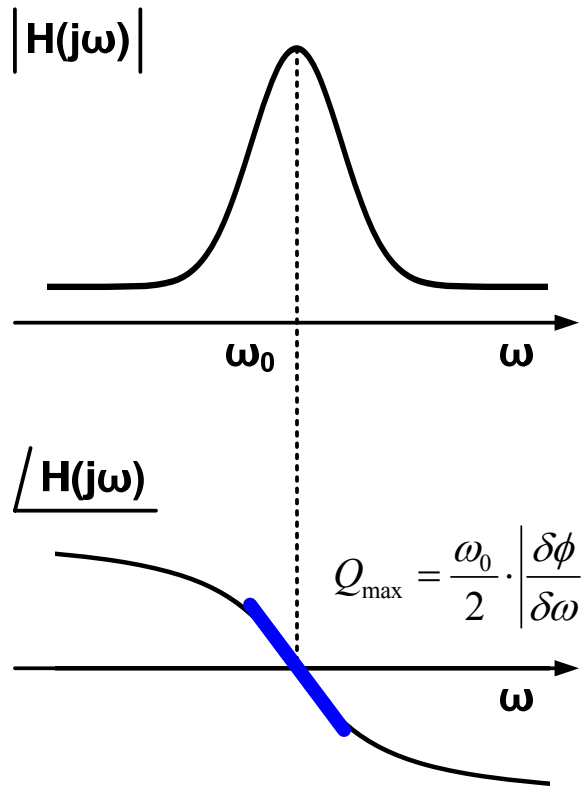


Figure 3.1: (a) Single stage LC oscillator
 (b) Phase relationship; Voltage, V_o , and current, I_{osc} , are in phase.



(a)



(b)

Figure 3.2: Open loop characteristic for a single stage; Transfer function in (a) and magnitude and phase response in (b); Operating point is where the slope of phase is maximum, so the single stage oscillator achieves maximum quality factor.

3.1.2 Three stage coupled LC oscillator

Multi-stage coupled oscillators are usually designed with the basic cell shown in Figure 3.3(a), which is exactly same as the basic cell for the single stage LC oscillator, but with two more transistors, M5 and M6, for coupling with other oscillator stages. Unlike a single-stage LC oscillator, multi-stage oscillators have an additional current component in each basic cell due to the coupling between oscillators. Transistors M5 and M6 in Figure 3.3(a) introduce a coupling current between each stage. The phasor diagram with this coupling current is shown in Figure 3.3(b). Assuming that the magnitude of the coupling current, I_{cou} , is same as that of the oscillation current, I_{osc} , then in case of three stage LC oscillators we have a 60 degree phase difference, Φ , between the coupling current and the oscillation current. For a given stage, the introduced coupling current from an adjacent stage alters the total current which has phase difference of Φ_{osc} with the voltage at the LC tank. Since the zero-phase between the voltage and the current in the LC tank is the oscillation condition at the steady-state as shown in Figure 3.1(b), this requirement forces the LC tank to have $-\Phi_{osc}$ phase with changing the operating frequency slightly. This can be understood more easily from the open loop model in Figure 3.4. In multi-stage coupled oscillators phase shifting is introduced in the loop due to the out of phase coupling current. In order for the sum of phases around the loop to be zero, the LC tank should have same phase but with opposite polarity. This is the steady state condition for oscillation in multi-stage coupled oscillators. Due to the introduced phase component in the LC tank the oscillators do not operate at the same frequency as the single stage oscillator.

The operating frequency can be estimated from the magnitude and phase response

of the transfer function of the tank in Figure 3.4(b). At the operating frequency of the multi-stage oscillator, the derivative of the phase is not the maximum value we get from the single stage oscillator. Therefore, the effective quality factor of the tank is smaller in this type of coupled multi-stage oscillator. As the introduced phase due to increased coupling gets bigger, the effective capacitance of the tank becomes smaller.

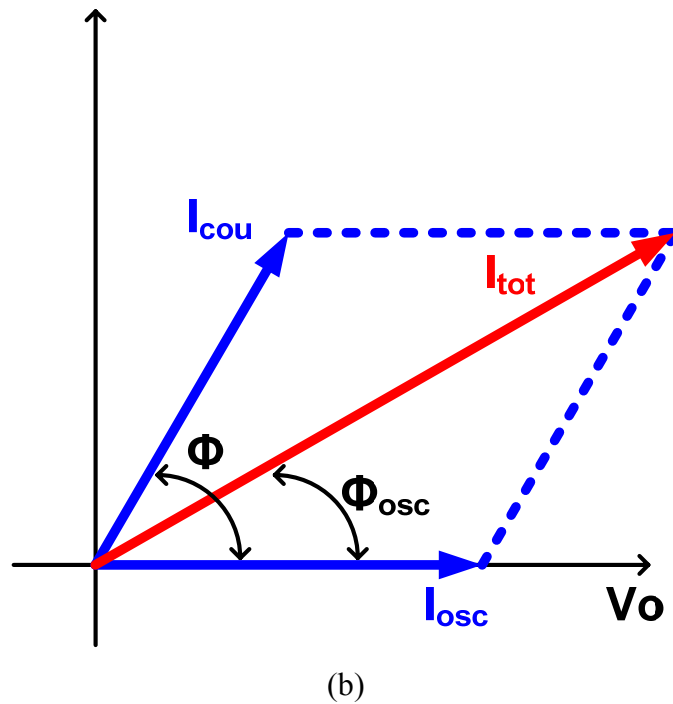
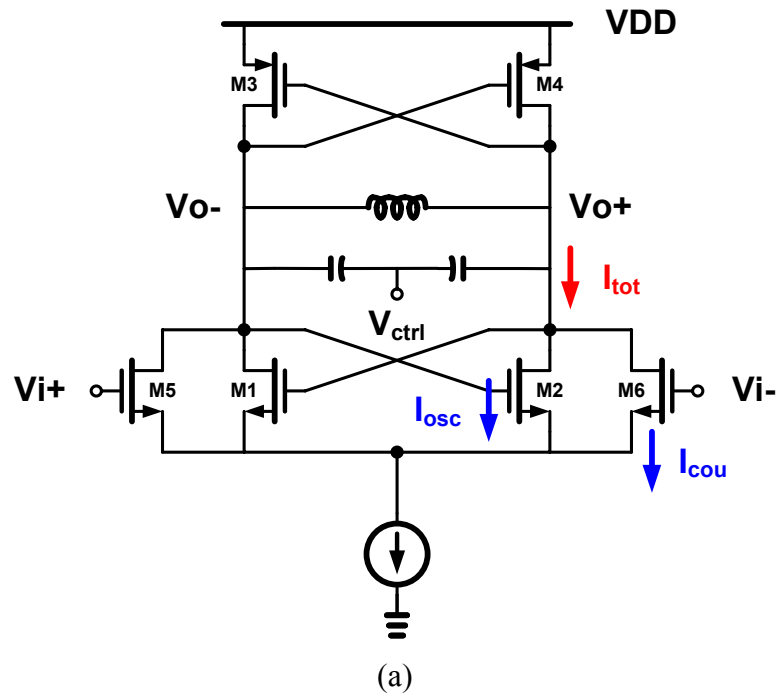
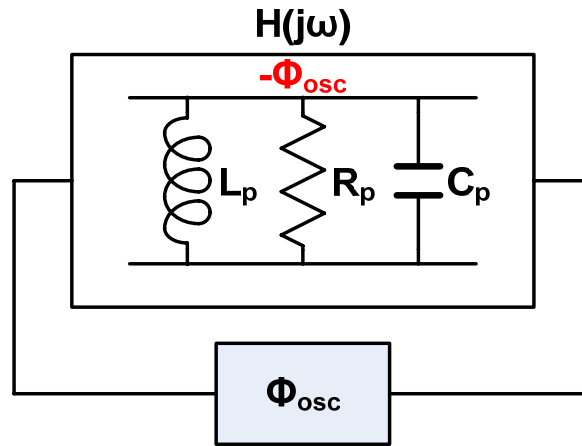
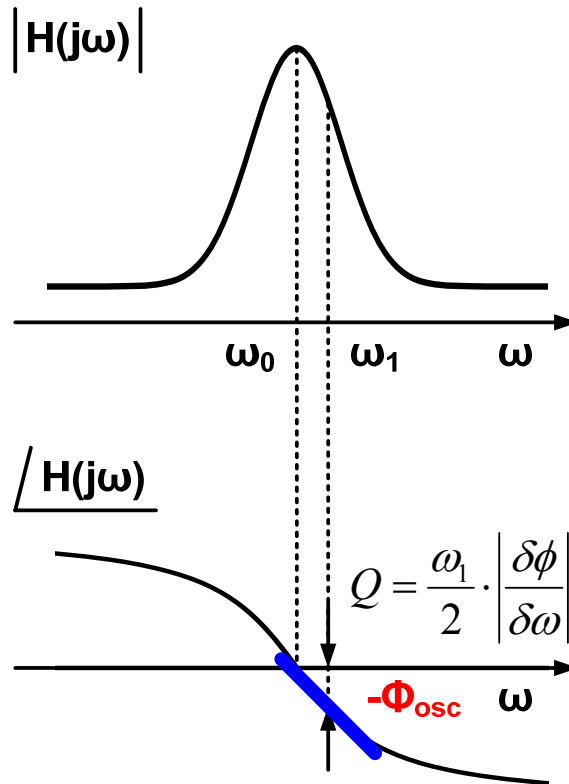


Figure 3.3: (a) Basic cell of three stage LC oscillator (note that there are coupling transistors, M5 and M6, in this case) and (b) Phase relationship; coupling current, I_{cou} , is out of phase with the oscillation current, I_{osc} , and the total current, I_{tot} , has Φ_{osc} phase difference with the voltage, V_o .



(a)

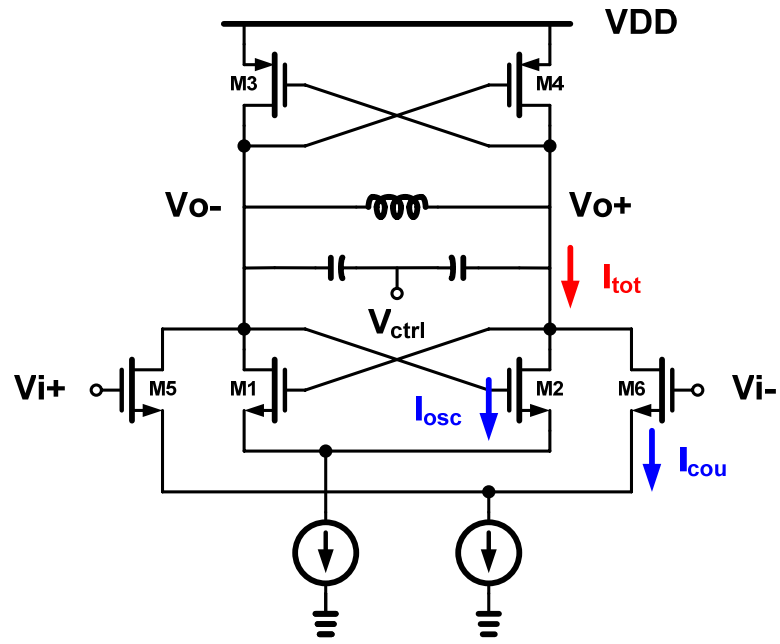


(b)

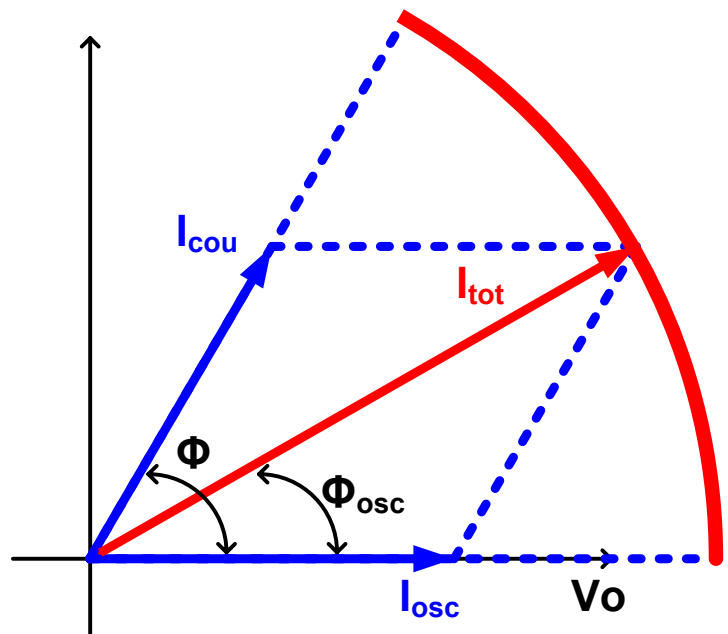
Figure 3.4: Open loop characteristic for the three stage multi-phase oscillator; Transfer function (a) and magnitude and phase response (b); The multi stage oscillator is no longer operate at the point of maximum slope and maximum quality factor

3.1.3 Three stage coupled LC oscillator with separate current sources

In the case of a three-stage LC oscillator, built with the basic stage shown in Figure 3.5(a), there are separate current sources for the coupling transistors and for the cross-connected regenerative transistors. For a fixed total current, increasing the coupling current moves the phase of the total current closer to that of the coupling current, I_{cou} , in Figure 3.5(b). With stronger coupling, the phase accuracy of the multiple phases is improved, but there is also increasing the phase difference, Φ_{osc} , between total current I_{tot} and I_{osc} . Because of the phase difference Φ_{osc} , the effective quality factor of the each stage is degraded and, thus, the oscillator phase noise increases. On the other hand, increasing the current to the cross coupled transistors, I_{osc} , and decreasing the coupling current, I_{cou} , reduces the phase difference, Φ_{osc} , and decreases the phase noise but also increasing the phase spacing error. Therefore, with the separate current sources we can increase the current for coupling between oscillators or increase the current for the cross coupled transistors. In other words, we cannot decrease the phase spacing error and phase noise at the same time.



(a)



(b)

Figure 3.5: (a) Oscillator stage with separate current sources for coupling and cross-coupled transistors (b) Phase relationship; With changing coupling current, I_{cou} , and oscillation current, I_{osc} , we can have different phase difference, Φ_{osc} , between total current, I_{tot} , and the voltage, V_o .

3.2. Capacitive coupling

Introducing capacitive coupling to a conventional multi-stage oscillator is a simple method to reduce both phase-spacing-error and phase noise. Unlike conventional coupling with coupling transistors, capacitive coupling introduces an in-phase coupling current whose phase is same as that of the oscillation current and the coupling strength is much larger than the coupling power with a conventional coupling connection. Another benefit is that the in-phase coupling power increases with the operating frequency.

3.2.1 Architecture

Capacitive coupling can be used along with the conventional coupling with the coupling transistors. It cannot be used as a stand alone coupling method, since capacitive coupling alone cannot define the oscillation direction properly. Capacitive coupling can be accomplished with a ring of capacitors as shown in Figure 3.6. It also shows the phase relationship for a 3 stage LC oscillator ring. The connections of the coupling capacitors are shown with a dashed line. The capacitors connect the oscillator nodes in the order of the phases (i.e. 0° , 60° , and 120° and so on) forming a ring.

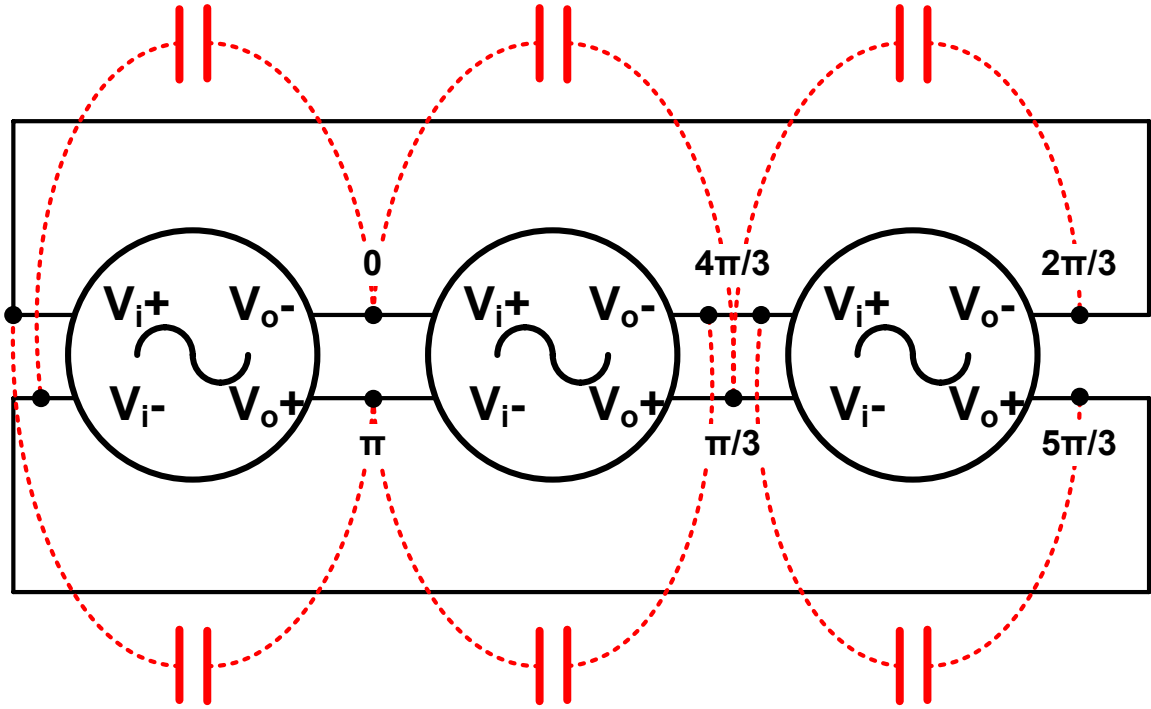


Figure 3.6: Phase relationship in a 3 stage LC oscillator ring. Coupling capacitors are shown with dashed line (coupling capacitors form a ring of capacitors)

3.2.2 Phasor diagram

A phasor diagram of a three-stage LC oscillator ring with capacitive coupling is shown in Figure 3.7. There are three current components at each oscillator node. For example, at node V_{o1} there is the regeneration current, I_{osc1} , and there are two coupling currents; one is a conventional coupling current produced by transistors, I_{c_tr3b} , and the other is coupling current introduced by coupling capacitors, I_{c_cap1} . Since each node has two capacitors, in the case of three-stage LC oscillator, one capacitor connects to a node 60 degree fast and the other to the node 60 degree slow. The coupling current with capacitors for node V_{o1} is sum of two components, I_{c_13b} and I_{c_12} . The phase of total coupling current through the capacitors is same as the phase of regeneration current, I_{osc} ,

because it is the sum of two coupling currents, one from a node that is 60 degree fast and the other from a node 60 degree slow node. The magnitude of the capacitor coupling current is usually much larger than I_{osc} since the current through the capacitor is proportional to the operating frequency, the capacitance, and the phase difference between voltages across the capacitor. As an example, the RMS value of the coupling current is around 10mA in a 4GHz 3 stage LC oscillator ring with 1pF coupling capacitors. As shown in Fig. 9, due to the high in-phase coupling current from the capacitors the magnitude of the total current, I_{tot_cap} , is larger than that of the conventional coupling with transistors, I_{tot_con} , resulting improved phase accuracy, and the phase difference between I_{tot_cap} and I_{osc1} is smaller than that between I_{tot_con} and I_{osc1} resulting reduced phase noise. Even though the RMS current at each capacitor is large, the ring of capacitors does not require extra power since sum of the current in the ring is always zero.

The coupling power with the ring of capacitors grows as the operating frequency goes up since the current through the capacitors is proportional to the operating frequency.

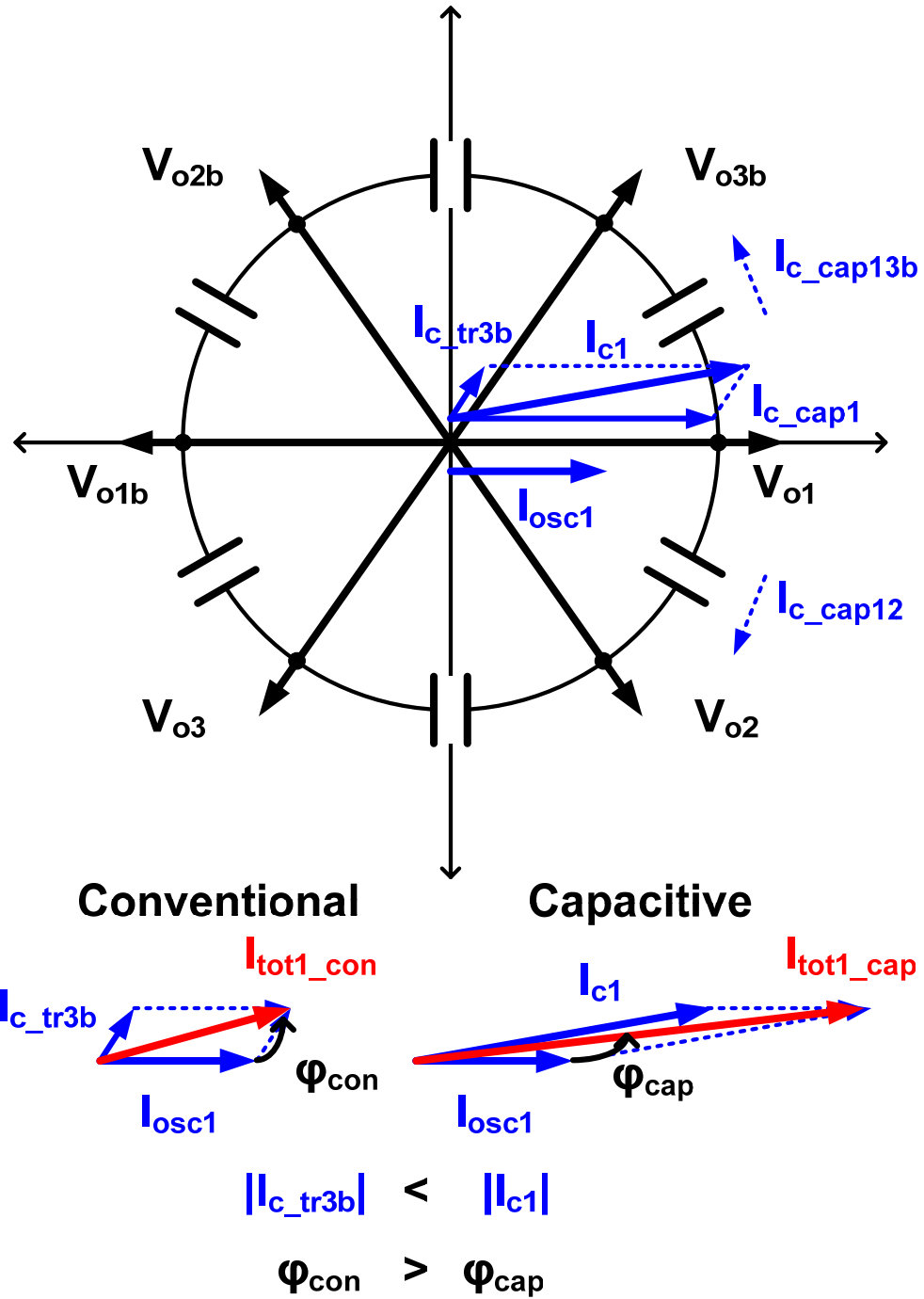


Figure 3.7: Phasor diagram of 3 stage LC oscillator ring with capacitive coupling; With the capacitive coupling there is another path for the current flowing from the ring of capacitors. The coupling current with the ring of capacitors introduces in-phase coupling current, therefore, the coupling strength is much bigger but with much smaller phase difference between total current, I_{tot1_cap} , and the oscillation current, I_{osc1} .

3.2.3 Capacitive loading

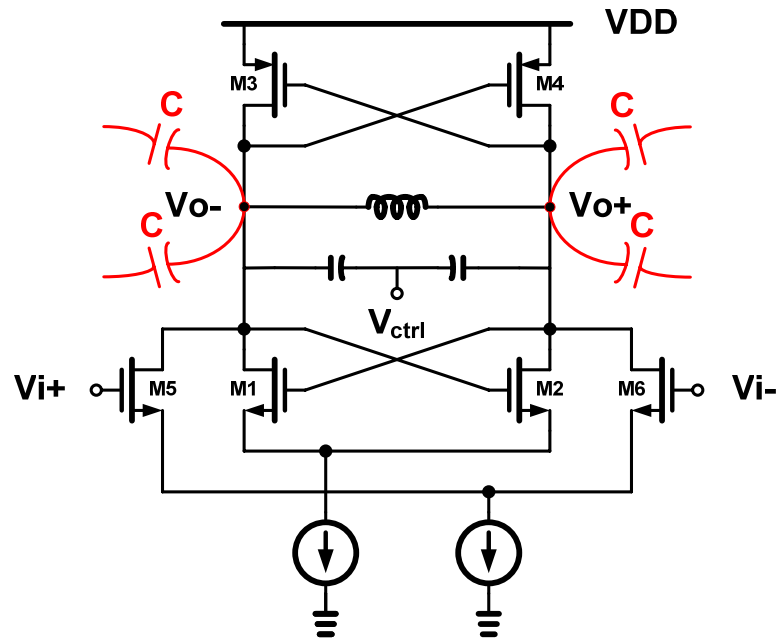
The phase difference, θ , of the voltages across the coupling capacitors generates current flow and causes capacitive loading at each output nodes of the oscillators. The current can be simplified with the use of effective capacitance in (3.1). The original schematic of Figure 3.8(a) has same capacitive loading with the modified schematic in Figure 3.8(b) with grounded capacitors.

$$\begin{aligned}
 i &= C \frac{d(V \cdot e^{j\theta} - V \cdot e^{-j\theta})}{dt} \\
 &= (e^{j\theta} - e^{-j\theta}) \cdot C \frac{dV \cdot e^{j\theta}}{dt} \\
 &= C_{eff} \cdot C \frac{dV \cdot e^{j\theta}}{dt}.
 \end{aligned} \tag{3.1}$$

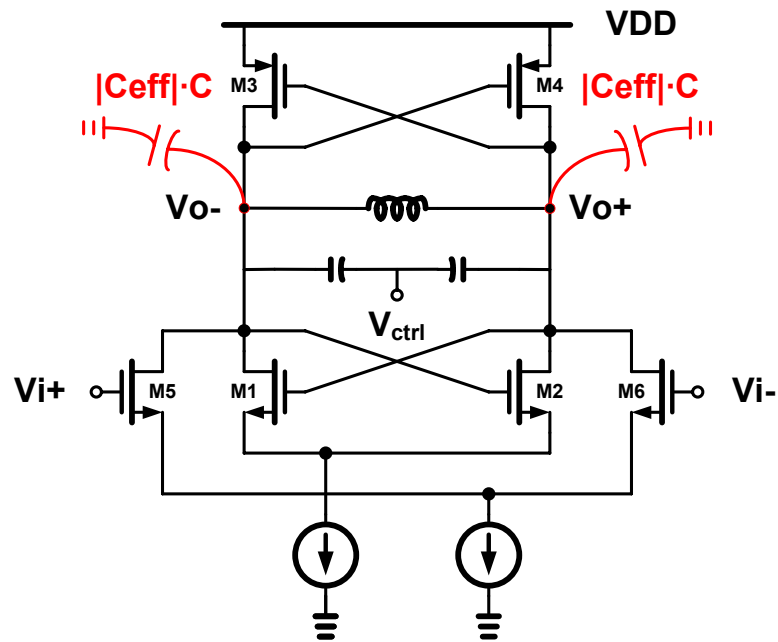
Even though the equivalent model in Figure 3.8(b) can properly explain the change of the operating frequency with the capacitive coupling, it does not explain strength the capacitors coupling between oscillator stages. Capacitive coupling introduces capacitive loading at each node with a value of $|C_{eff}| \cdot C$, and the operating frequency becomes:

$$\omega = \frac{1}{\sqrt{L \cdot \left(C_{tank} + \frac{|C_{eff}| \cdot C}{2} \right)}}. \tag{3.2}$$

Since the ring of capacitors acts as the fixed capacitance at each node, the tuning range of the LC tank decreases.



(a)



(b)

Figure 3.8: Three stage LC oscillator ring (a) with capacitive coupling (b) without capacitive coupling but with same capacitive loading; Both oscillators are operating at the same frequency, but the oscillator with capacitive coupling has capacitive coupling effect, so there is in-phase coupling current.

The effective capacitances for different numbers of stages are summarized in Table 3.1.

Table 3.1 Effective capacitance

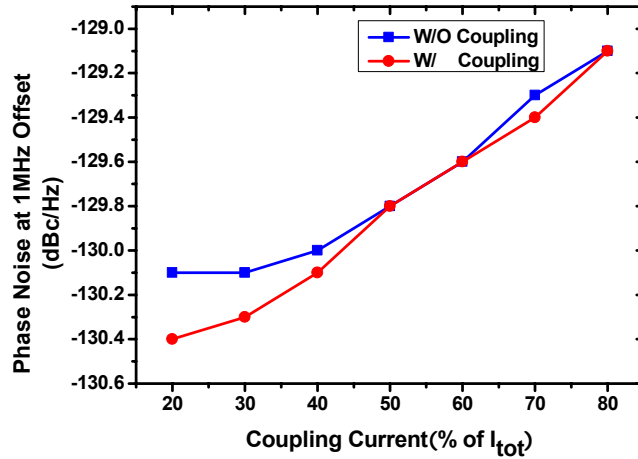
$\theta(\text{degree})$	C_{eff}		C_{load} ($2 \cdot \text{Re}$)
	$\text{Re} + j \text{Im}$	$ C_{eff} \angle C_{eff}$	
45	$\left(1 - \frac{1}{\sqrt{2}}\right) - j \frac{1}{\sqrt{2}}$	$(2 - \sqrt{2})^{0.5} \angle 45^\circ$	$2 \cdot \left(1 - \frac{1}{\sqrt{2}}\right)$
60	$\frac{1}{2} - j \frac{\sqrt{3}}{2}$	$1 \angle 60^\circ$	1
90	$1 - j$	$\sqrt{2} \angle 45^\circ$	2

3.2.4 Comparison: without capacitive coupling and with capacitive coupling

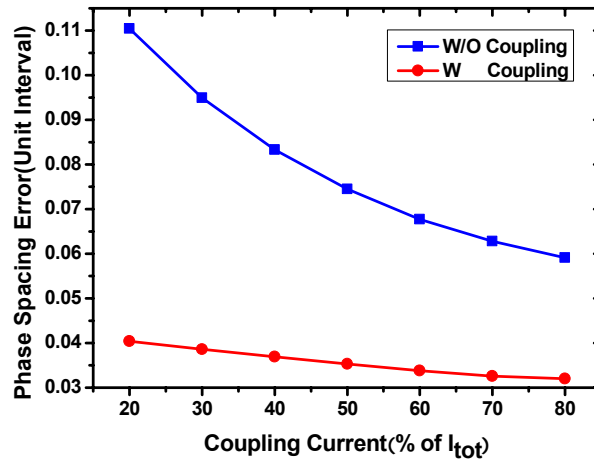
In this comparison, two coupled oscillators with stages shown in Figure 3.8(a) and (b), are designed to have the same oscillation frequency, but only the one with the basic stage in Figure 3.8(a) has capacitive coupling. In order to understand the reduction in phase noise and phase spacing error, two simple three-stage coupled oscillators with the different basic stage were simulated.

With a deliberate mismatch (i.e. $50fF$ extra capacitance in one of the six output nodes which corresponds to about 1.3% capacitance error) added to both three stage oscillators, phase noise and phase spacing error were compared. The phase noise and phase spacing error for different transistor coupling current settings (expressed as a percentage of I_{tot}) are plotted in Figure 3.9(a) and (b) respectively. Even though the two oscillators oscillate at the same frequency, the oscillator with capacitive coupling shows less phase noise and substantially less phase spacing error. In the case of capacitive

coupling a small phase spacing error can be achieved with weak transistor coupling between stages.



(a)



(b)

Figure 3.9: Comparison with/without capacitive coupling (a) Phase noise (b) phase spacing error; the oscillator with capacitive coupling shows slightly better phase noise performance over all, but when we look at the phase spacing error, the oscillator with capacitive coupling shows much better phase spacing error performance.

3.3 Two stage oscillator with capacitive coupling

Capacitive coupling is not effective for two stage oscillators. From the phasor diagram of a two-stage coupled oscillators with capacitive coupling in Figure 3.10 even though there are still coupling currents, I_{c_cap12b} and I_{c_cap12} for node V_{o1} , from the ring of capacitors, the sum of those current is zero since their phase difference is 180 degree for the two-stage oscillators. Therefore, capacitive coupling in two-stage coupled oscillators does not increase the coupling or introduce an in-phase coupling, unlike the case with three or four-stage coupled oscillators with capacitive coupling.

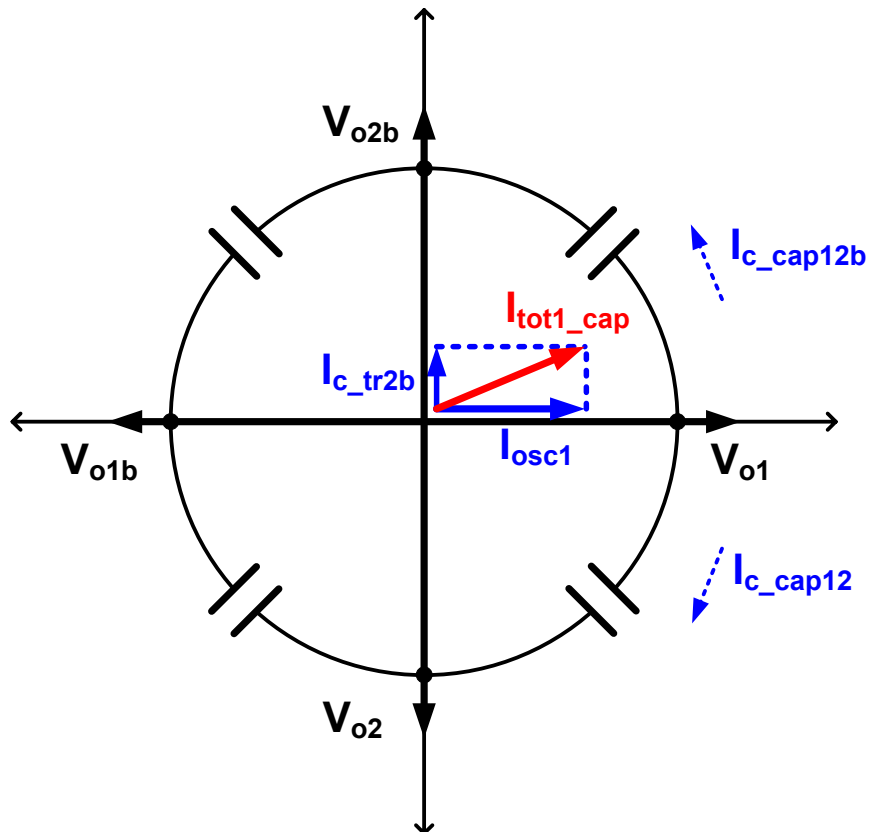


Figure 3.10: Phasor diagram of 2 stage LC oscillator ring with capacitive coupling; in case of two stage LC oscillator the sum of two coupling currents, I_{c_cap12b} and I_{c_cap12} , is zero, so there is no contribution from the capacitive coupling in this case

3.4 Prototype circuits

Three three-stage LC oscillators were fabricated in $0.18\mu\text{m}$ CMOS as shown in Figure 3.11, and the RMS and the pk-pk jitter of each oscillator is shown in Figure 3.12. The jitter for a conventional cell is shown in Figure 3.12(a), and jitter for the cell with separate current sources and cell with coupling capacitors are shown in Figure 3.12(b) and (c) respectively. Jitter was measured with 6mA of total current (i.e. 5mA of regeneration current and 1mA of transistor coupling current). Since the power planes for each oscillator were designed relatively narrower than they had to be, the circuits experienced huge resistance on the power line. That is why the oscillators show poor jitter performance overall. Even though increased current for regeneration reduces the jitter a little in Figure 3.12(b) (compared to the conventional in Figure 3.12(a)), as shown in Figure 3.12(c) capacitive coupling is far more effective in reducing jitter.

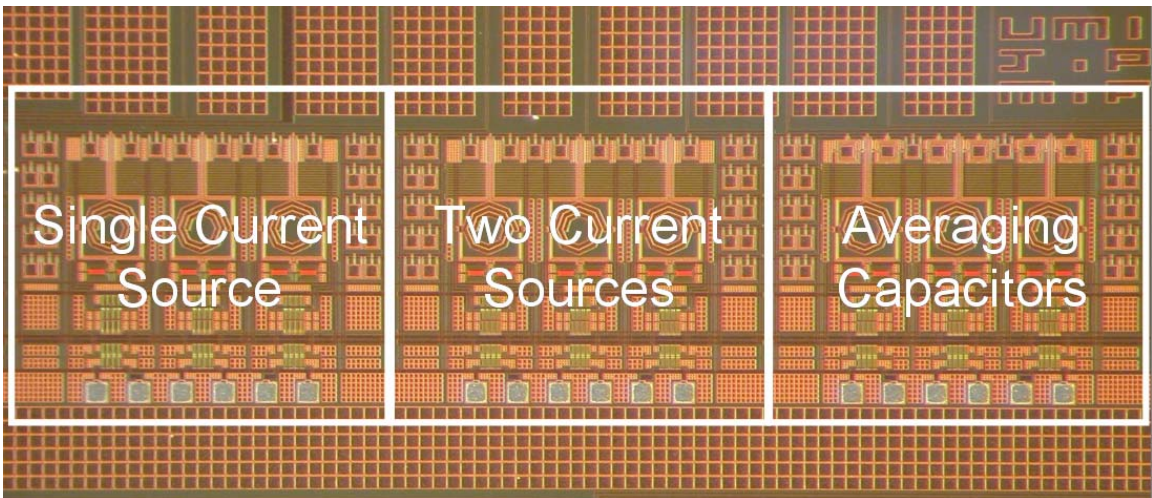
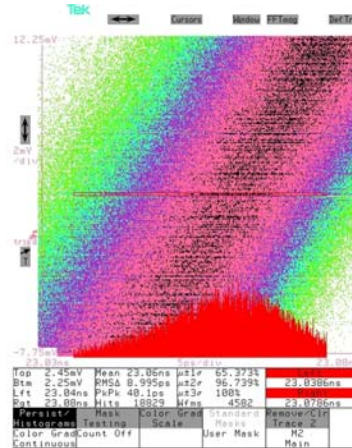
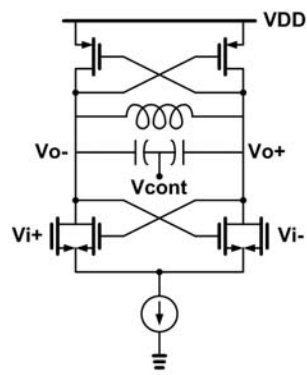
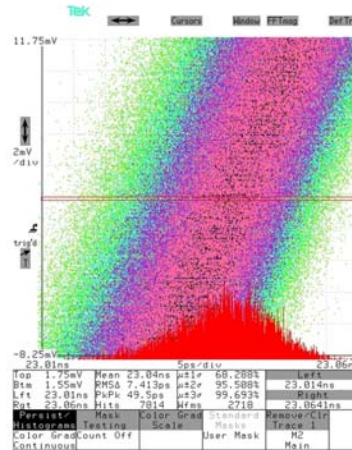
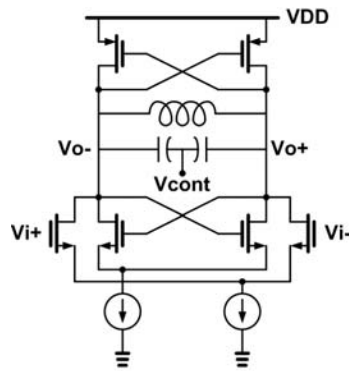


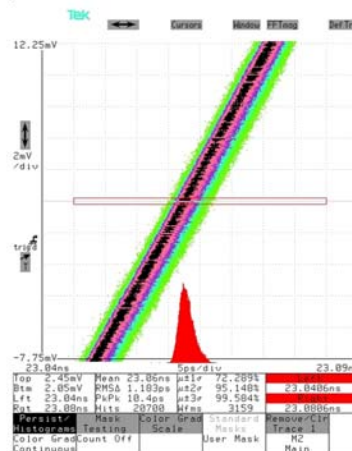
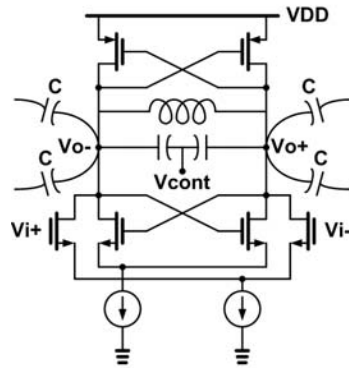
Figure 3.11: Die photograph of the 3 oscillator rings; all three oscillators take same power and same area.



(a)



(b)



(c)

Figure 3.12: RMS and pk-pk jitter of three three-stage LC oscillators
 (a) Conventional Cell; RMS 8.995ps, pk-pk 40.1ps @ 4.537GHz
 (b) With separate current sources; RMS 7.413ps, pk-pk 49.5ps @ 4.588GHz
 (c) With Capacitive Coupling; RMS 1.183ps, pk-pk 10.4ps @ 4.011GHz

3.5 Conclusion

Capacitive coupling in multi-stage LC oscillators introduces a large in-phase coupling current which reduces both phase noise and phase spacing error at the same time. The change of tuning range and operating frequency due to the capacitive coupling can be explained with the aid of the effective capacitance. The ring of capacitors can be replaced with the equivalent capacitors one port of which is grounded, simplifying the analysis of a capacitively coupled oscillator.

Three three-stage coupled LC oscillators were fabricated and jitter of each oscillator was measured. Three stage LC oscillators with capacitive coupling shows 1.183ps RMS jitter and 10.4ps pk-pk jitter at 4.01GHz, and capacitive coupling is far more effective in reducing jitter than conventional coupling with transistors.

With the simple addition of the ring of capacitors both phase noise and phase spacing error can be reduced and this capacitive coupling can be easily extended to any number of stages. The scheme provides accurate finely spaces clocks for clock-and-data recovery and other applications.

Chapter IV

High-speed clock generation with a low-jitter PLL with capacitive coupling

A PLL is a common functional block for generating system clocks in integrated circuits. Since a PLL is a negative feedback system, loop stability is the main issue in design stages. Designing PLL with capacitively coupled oscillators only changes the noise characteristics of the multi-stage LC oscillators. Therefore, we can still follow the standard design procedure of the PLL. Basic functional blocks and loop characteristics of the PLL[30, 31] will be presented in this chapter.

4.1. PLL Fundamentals

A PLL is a functional block operating on changes in frequency or phases of input signals. Mathematical expressions for this operation will be presented shortly.

A periodic signal $x(t)$ can be expressed as

$$x(t) = A \cos \omega_c t \quad (4.1)$$

where A is the amplitude and ω_c is the frequency. For the narrowband phase modulated signal $x(t)$ is expressed as

$$x(t) = A \cos(\omega_c t + \phi_n(t)) \quad (4.2)$$

The total phase of this signal is

$$\phi_{total}(t) = \omega_c t + \phi_n(t) \quad (4.3)$$

and the total frequency can be acquired from the derivative of the total phase.

$$\Omega_{total}(t) = \frac{d\phi_{total}(t)}{dt} = \omega_c + \frac{d\phi_n(t)}{dt} \quad (4.4)$$

A phase-locked loop (PLL) operates on excess components of $\Phi_{total}(t)$ and $\Omega_{total}(t)$ such as $\Phi_n(t)$ and $d\Phi_n(t)/dt$, respectively.

4.1.1 Voltage controlled oscillator (VCO)

The voltage controlled oscillator (VCO) in Figure 4.1 changes its frequency output signal, depending on the input control voltage, V_{cont} , and the frequency of the output signal, it can be expressed as:

$$\omega_{out} = \omega_{FR} + K_v V_{cont} \quad (4.5)$$

Then the phase becomes

$$\phi_{out}(t) = \int (\omega_{FR} + K_v V_{cont}) dt \quad (4.6)$$

and the output voltage waveform can be expressed as

$$V_{out}(t) = A \cos(\omega_{RF} t + K_v \int_{-\infty}^t V_{cont} dt) \quad (4.7)$$

Since a PLL works on the excess component of the $\Phi_{total}(t)$, the transfer function of the VCO can be expressed as

$$\phi_{excess}(t) = K_v \int_{-\infty}^t V_{cont} dt \quad (4.8)$$

The Laplace transform of (4.8) becomes

$$\phi_{excess}(s) = \frac{K_v}{s} V_{cont}(s) \quad (4.9)$$

In this way the transfer function of the VCO in the frequency domain ($\Phi_{total}(t)/V_{cont}(s)$) is K_v/s .

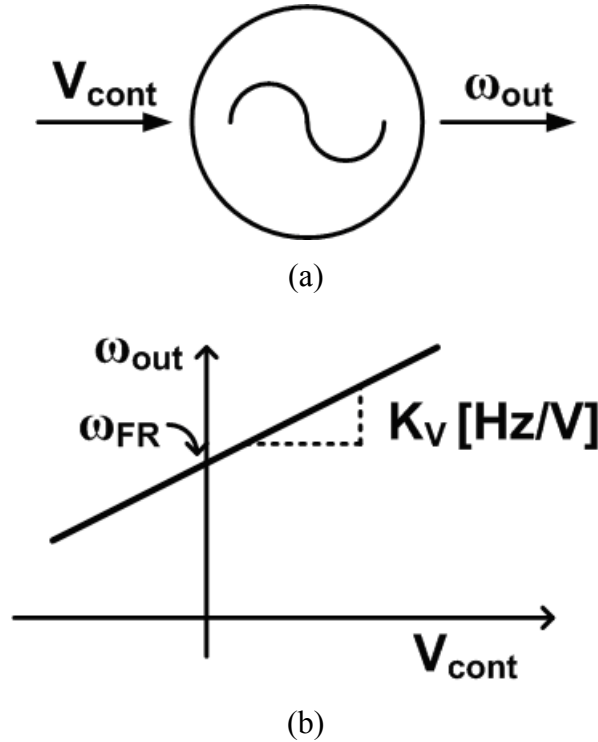


Figure 4.1: Voltage controlled oscillator (VCO); (a) input and output of VCO and the relationship between phase and frequency in (b)

4.1.2 Phase detector (PD)

The phase detector (PD) in Figure 4.2 produces a current or voltage which is proportional to the phase difference or frequency difference of the two input signals. When the phase detector can detect both phase and frequency differences of the input signals, then the phase detector is better called a phase frequency detector (PFD). The transfer function of the PD is expressed as the ratio between the averaged output voltage or current and the input phase difference, as shown in Figure 4.2(b).

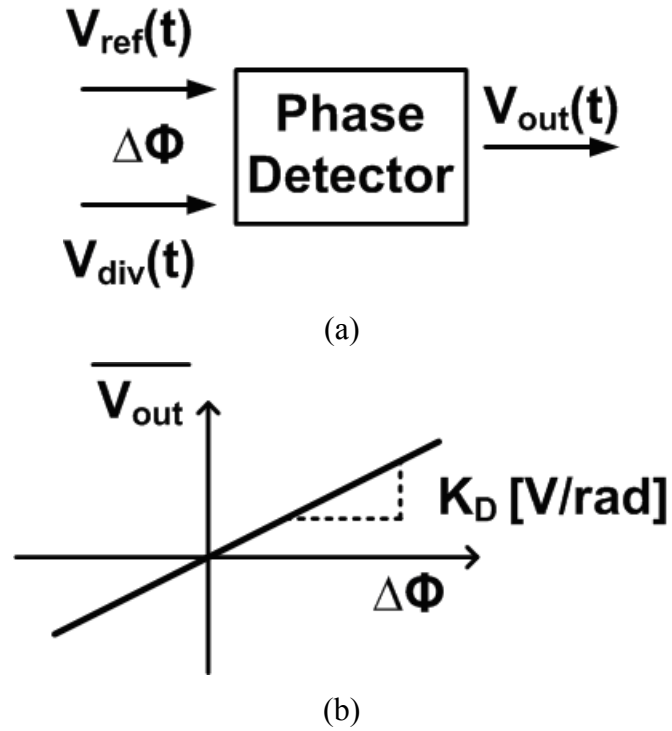


Figure 4.2: Phase detector; (a) input and output of PD and their relationship in (b)

For example, when an XOR gate is used as a PD in Figure 4.3(a), the input and output voltages are shown in Figure 4.3(b). The PD produces an output signal proportional to the phase difference and the averaged voltage is meaningful for the circuit operation.

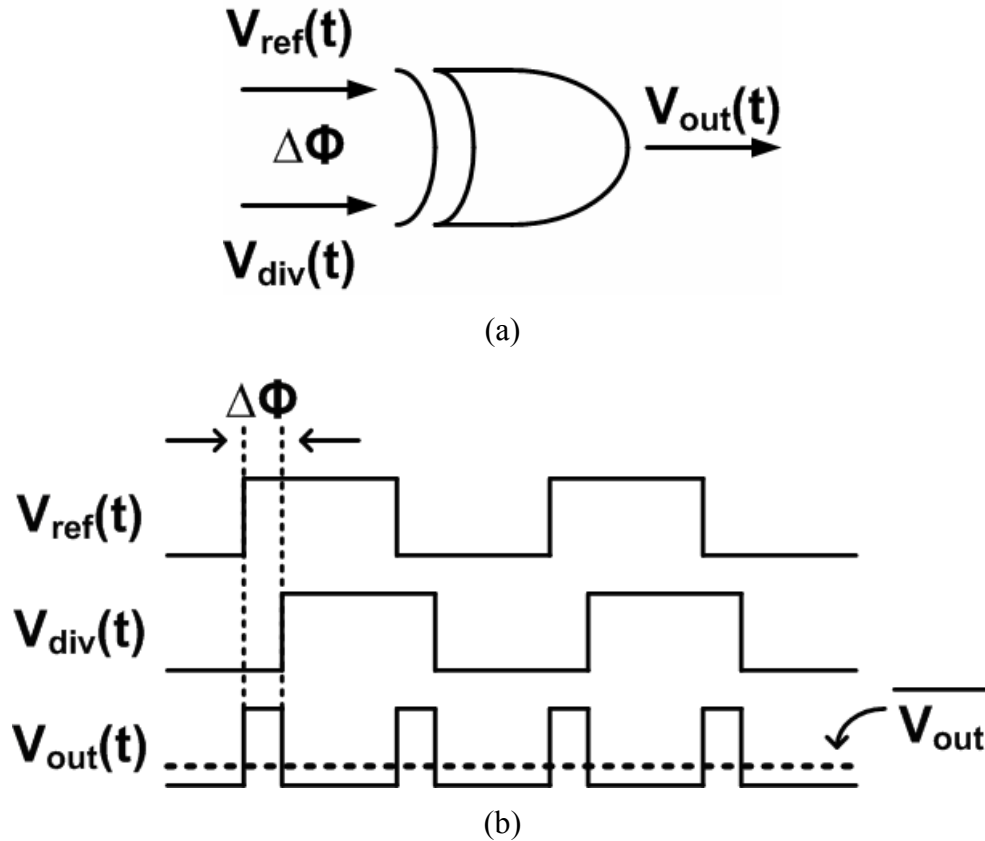


Figure 4.3: XOR as a PD; (a) input and output of PD and waveforms (b)

4.1.3 Phase frequency detector (PFD)

A phase frequency detector (PFD) can detect frequency difference as well as phase difference. In general, a PFD employs edge-triggered flip-flops in order not to become sensitive to the duty cycle of input signals and in this way, a PFD is only sensitive to rising or falling edges. Figure 4.4(a) shows the symbol for a PFD. Based on frequency or phase difference, a PFD generates either *UP* or *DN* signals. The waveforms, in the case of a frequency difference, are shown in Figure 4.4(b). In the example, the frequency of the reference signal is faster than the output signal of the divider.

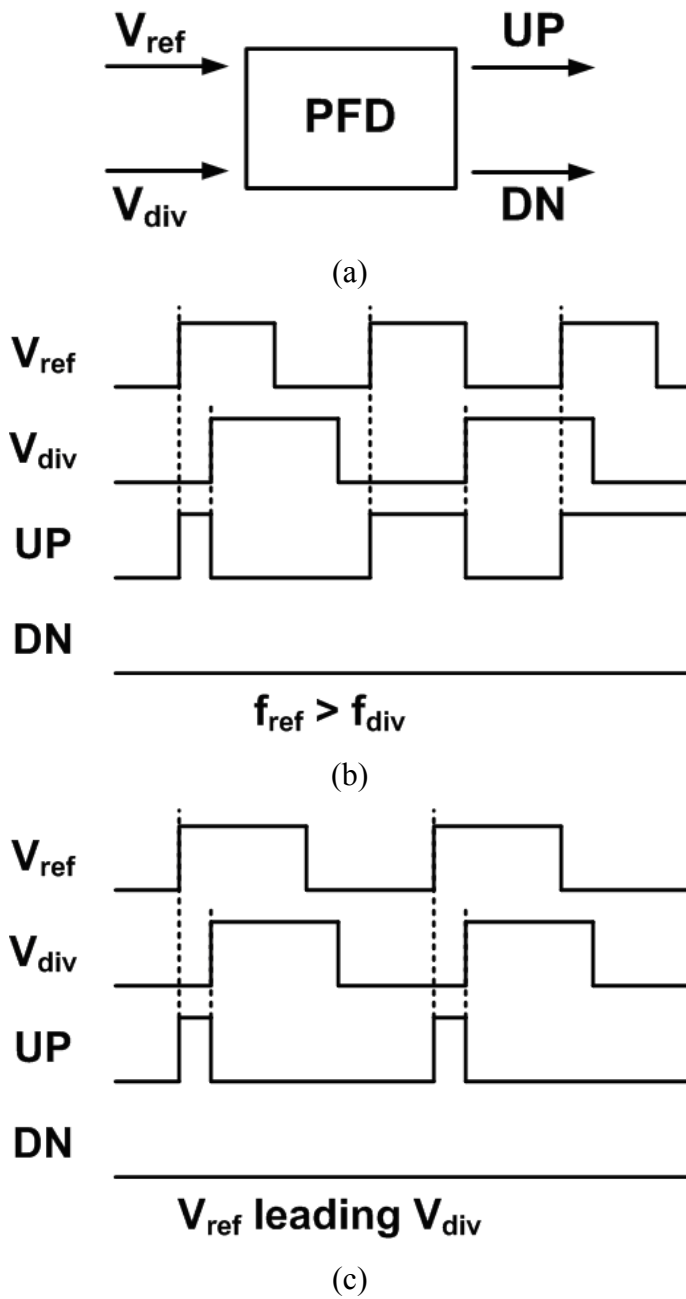


Figure 4.4: (a) Symbol of a PFD, (b) UP and DN signals when the input frequencies are different, and (c) input phases are different.

4.1.4 PFD and charge pump

A switched-current source (charge pump) is a good choice for the PFD output stage since it is fast and has a low noise due to tri-state operation[32]. In addition, the high output impedance of the charge pump insures a loop filter pole at zero frequency. The PFD generates an UP or DN signal during the phase mismatch of the input signals.

$$\theta_e = \theta_{ref} - \theta_{div} \quad (4.10)$$

Then the on-time of either UP or DN becomes $t_p(=\Theta_e/\omega_r)$ for each period($2\pi/\omega_r$) of the reference signal, and the average error current over a cycle becomes

$$\bar{i}_D = \frac{t_p}{2\pi/\omega_r} I_d = \frac{|\theta_e|}{\omega_r} \frac{\omega_r}{2\pi} I_d = \frac{I_d}{2\pi} |\theta_e| \quad (4.11)$$

Therefore, the transfer function of the average current output from the phase difference of input signals becomes

$$\frac{\bar{i}_D}{|\theta_e|} = \frac{I_d}{2\pi} \quad (4.12)$$

and this is the gain, K_D , of the phase frequency detector with a charge pump.

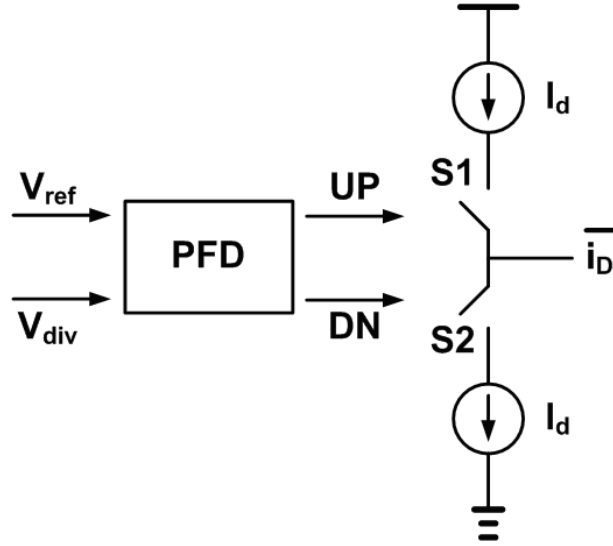


Figure 4.5: PFD and charge pump

4.1.5 Simple PLL

A block diagram of a simple PLL is shown in Figure 4.6(a). The PLL is composed of a VCO, a PD, and a low pass filter (LPF). The PLL is a negative feedback system which uses the PD as an error amplifier. It can be said that the PLL is locked when the phase difference between input and output is constant with time. This can be expressed as:

$$\phi_{out} - \phi_{in} = k. \quad (4.13)$$

and constant phase difference means the frequencies of input and output are the same.

$$\frac{d(\phi_{out} - \phi_{in})}{dt} = \omega_{out} - \omega_{in} = 0 \quad (4.14)$$

The PLL can be modeled as in Figure 4.6(b). The open loop transfer function is :

$$A(s) = \frac{K_D K_V F(s)}{s} \quad (4.15)$$

and the closed loop gain of the negative feedback system is

$$A_f(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{A(s)}{1 + A(s)} = \frac{K_D K_V F(s)}{s + K_D K_V F(s)}. \quad (4.16)$$

Since $A_f(s)$ is 1 at zero frequency (i.e. $s=0$), $A_f(s)$ has a low-pass characteristic which means output phase follows variations of the input in in-band. The transfer function for the error phase, Φ_e , from the input can be expressed as

$$E(s) = \frac{\phi_e(s)}{\phi_{in}(s)} = \frac{1}{1 + A(s)} = \frac{s}{s + K_D K_V F(s)}. \quad (4.17)$$

Since $E(s)$ is 0 at zero frequency ($s=0$) and 1 at infinity ($s=\infty$), this is a high-pass characteristic.

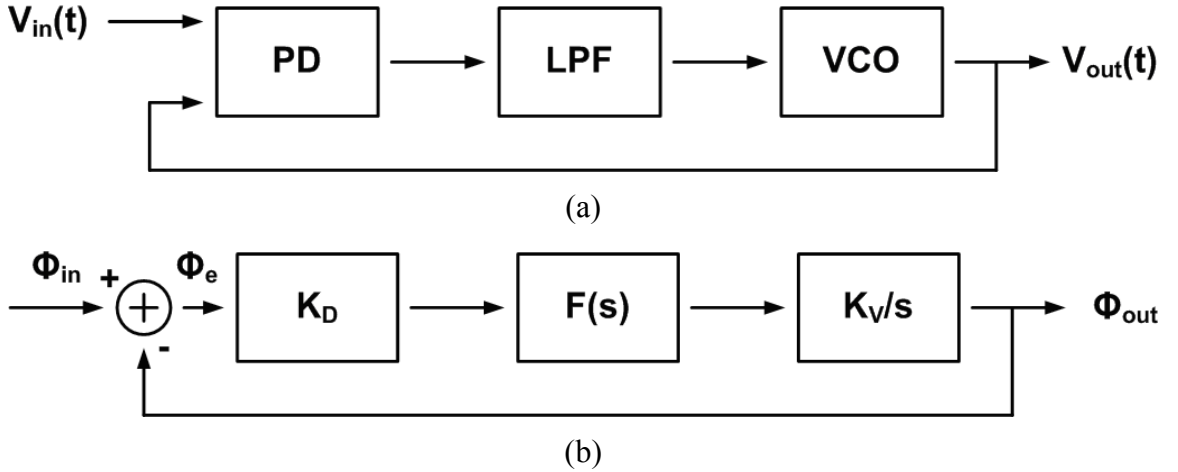


Figure 4.6: Block diagram of PLL in (a) and the model of PLL in (b)

4.1.6 Tracking (steady-state phase error)

Even when there is an abrupt change in phase or frequency of the input signal, we want $E(s)$ to become zero at steady-state. We can use Laplace final value theorem to determine the steady-state phase error,

$$\phi_e(t \rightarrow \infty) = \lim_{s \rightarrow 0} s \phi_e(s) = \lim_{s \rightarrow 0} s E(s) \phi_{in}(s) = \lim_{s \rightarrow 0} \frac{s^2}{s + K_D K_V F(s)} \phi_{in}(s) \quad (4.18)$$

For a step phase input

$$\begin{aligned}\phi_{in}(t) &= \Delta\phi \cdot u(t) \\ \phi_{in}(s) &= \frac{\Delta\phi}{s}\end{aligned}\quad (4.19)$$

the steady-state phase error becomes

$$\phi_e(t \rightarrow \infty) = \lim_{s \rightarrow 0} \frac{s^2}{s + K_D K_V F(s)} \frac{\Delta\phi}{s} = 0 \quad (4.20)$$

if $F(0)$ is not zero.

For a step frequency input described by:

$$\omega_{in}(t) = \omega_o + \Delta\omega \cdot u(t) \quad (4.21)$$

the total input phase becomes

$$\phi_{total}(t) = \int \omega_{in}(t) dt = \omega_o t + \Delta\omega t. \quad (4.22)$$

Then the excess phase is

$$\begin{aligned}\phi_{in}(t) &= \phi_{excess}(t) = \Delta\omega t \\ \phi_{in}(s) &= \frac{\Delta\omega}{s^2}\end{aligned}\quad (4.23)$$

and the steady-state phase error becomes

$$\phi_e(t \rightarrow \infty) = \lim_{s \rightarrow 0} \frac{s^2}{s + K_D K_V F(s)} \frac{\Delta\omega}{s^2} = \frac{\Delta\omega}{K_D K_V F(0)} \quad (4.24)$$

In order to get zero steady-state phase error, $F(s)$ should be infinity at zero frequency. In other words, $F(s)$ should have at least one pole at zero frequency.

For a ramp frequency input

$$\omega_{in}(t) = \omega_o + \frac{d\Delta\omega}{dt} t = \omega_o + \Delta\dot{\omega} t \quad (4.25)$$

total input phase becomes

$$\phi_{total}(t) = \int \omega_{in}(t) dt = \omega_o t + \Delta\dot{\omega} \frac{t^2}{2}. \quad (4.26)$$

Then the excess phase is

$$\begin{aligned} \phi_{in}(t) &= \phi_{excess}(t) = \Delta\dot{\omega} \frac{t^2}{2} \\ \phi_{in}(s) &= \frac{\Delta\dot{\omega}}{s^3} \end{aligned} \quad (4.27)$$

and the steady-state phase error becomes

$$\phi_e(t \rightarrow \infty) = \lim_{s \rightarrow 0} \frac{s^2}{s + K_D K_V F(s)} \frac{\Delta\dot{\omega}}{s^3} = \lim_{s \rightarrow 0} \frac{\Delta\dot{\omega}}{s(s + K_D K_V F(s))} \quad (4.28)$$

In order for this value to be zero, $F(s)$ should have two poles at zero frequency. Then the PLL becomes at least a third order system. But for most applications, the inputs to the PLL are phase- or frequency-step inputs. Therefore, (4.20) and (4.24) become the minimum requirements for the filter design.

4.1.7 Loop filter

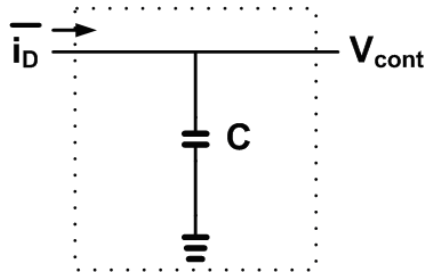
The loop filter rejects high frequency components of the current from the charge pump. Figure 4.7 shows three possible filters and we will evaluate the loop behavior with each filter in the loop. The transfer function ($=V_{cont}/i_D$) of the filters, Figure 4.7(a), (b), and (c), becomes

$$F(s) = \frac{1}{sC} \quad (4.29)$$

$$F(s) = \frac{1+sRC}{sC} \quad (4.30)$$

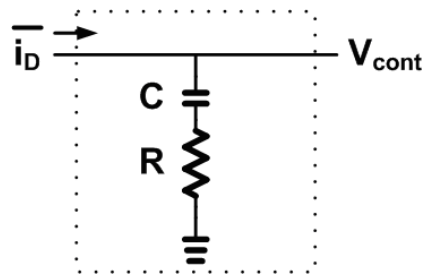
$$F(s) = \frac{1 + s\tau_2}{s(C_1 + C_2)(1 + s\tau_1)} \quad (4.31)$$

where $\tau_1 = R \frac{C_1 C_2}{C_1 + C_2}$ and $\tau_2 = RC_1$ respectively.



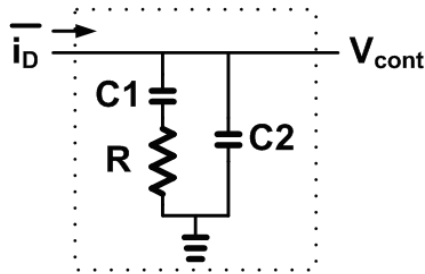
(a)

$$F(s) = \frac{1}{sC}$$



(b)

$$F(s) = \frac{1 + sRC}{sC}$$



(c)

$$F(s) = \frac{1 + s\tau_2}{s(C_1 + C_2)(1 + s\tau_1)}$$

$$\tau_1 = R \frac{C_1 C_2}{C_1 + C_2}$$

$$\tau_2 = RC_1$$

Figure 4.7: Filters in PLL; (a) single pole filter, (b) single pole and single zero filter, (c) two poles and one zero filter

Since the loop shows different characteristics, depending on the filter used, more details are given for each case. With the filter of Figure 4.7(a), the open-loop transfer function becomes

$$A(s) = \frac{K_D K_V F(s)}{s} = \frac{I_d}{2\pi} \frac{K_V}{s} \frac{1}{sC} \quad (4.32)$$

Since $A(s)$ has two poles at zero frequency, the phase margin at unity gain frequency becomes zero and the loop is unstable. It is obvious when we look at closed-loop transfer function:

$$A_f(s) = \frac{\frac{I_d}{2\pi} \frac{K_V}{C}}{s^2 + \frac{I_d}{2\pi} \frac{K_V}{C}} \quad (4.33)$$

Since $A_f(s)$ has two imaginary poles, the loop can never be stabilized. The open loop transfer function of the filter in Figure 4.7(b) is:

$$A(s) = \frac{K_D K_V F(s)}{s} = \frac{I_d}{2\pi} \frac{K_V}{s} \frac{1+sRC}{sC} \quad (4.34)$$

Even though this transfer function also has two poles at zero frequency, it has a zero at $1/RC$. The amplitude decreases by 40dB/dec from zero frequency and with a -180 degree phase, but after the zero frequency the amplitude decreases by 20dB/dec. Therefore, proper selection of R and C , allows placement of zero frequency below the unity gain frequency. The amplitude response of (4.34) with changing R , C , and I_d are shown in Figure 4.8(a), (b), and (c), respectively. Varying R changes only the zero frequency, while varying C changes the amplitude as well as the zero frequency. Varying I_d does not change the zero frequency, but it changes overall amplitude.

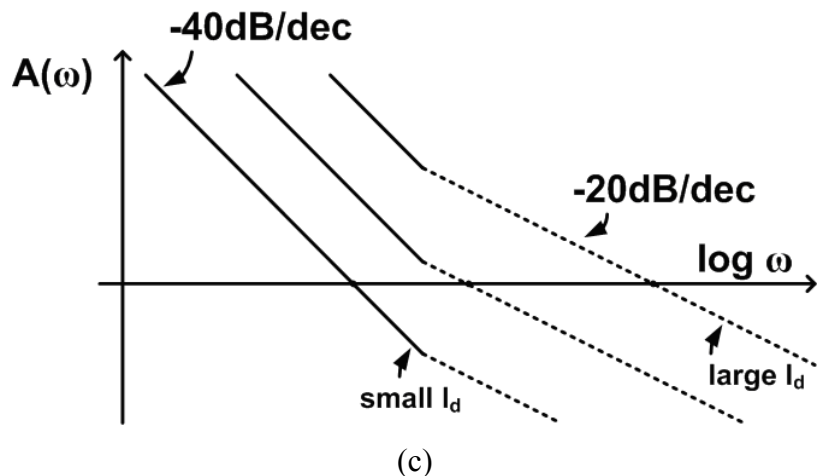
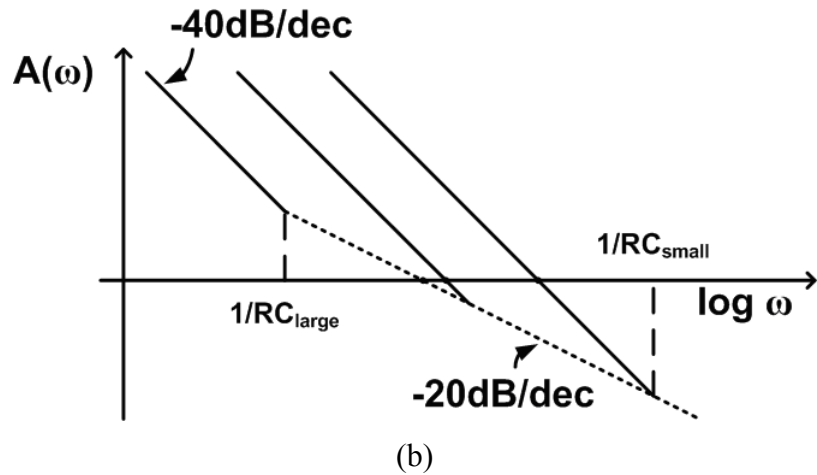
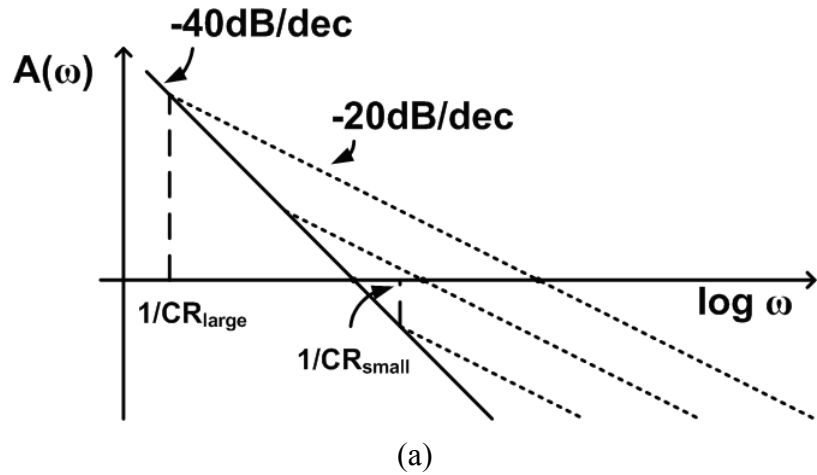


Figure 4.8: Amplitude response of (4.34): (a) changing R , (b) changing C , and (c) changing I_d

The problem with the filter of Figure 4.7(b) is that the control voltage, V_{cont} , changes abruptly for the current input, which causes sideband spurs at the reference frequency[32]. The filter in Figure 4.7(c) is a modified version of the filter in Figure 4.7(b) and has a capacitor to ground, which prevents abrupt voltage changes since the voltage across the capacitor cannot change abruptly. The open-loop transfer function with the filter in Figure 4.7(c) is

$$A(s) = \frac{K_D K_V F(s)}{s} = \frac{I_d K_V}{2\pi s} \frac{1 + s\tau_2}{s(C_1 + C_2)(1 + s\tau_1)} \quad (4.35)$$

and its amplitude response is shown in Figure 4.9. The amplitude initially decreases by 40dB/dec at zero frequency. After the zero frequency ($1/\tau_2$), the slope becomes -20dB/dec and -40dB/dec again after the second pole ($1/\tau_1$). The addition of the C2 capacitor in the loop filter allows increased rejection of high frequency components as compared to the filter in Figure 4.7(c). In order for the closed loop to be stable, the unity gain frequency of the open loop should be located somewhere between the zero frequency and the second pole frequency, where the slope of amplitude is -20dB/dec. The design procedure for deciding physical parameters follows.

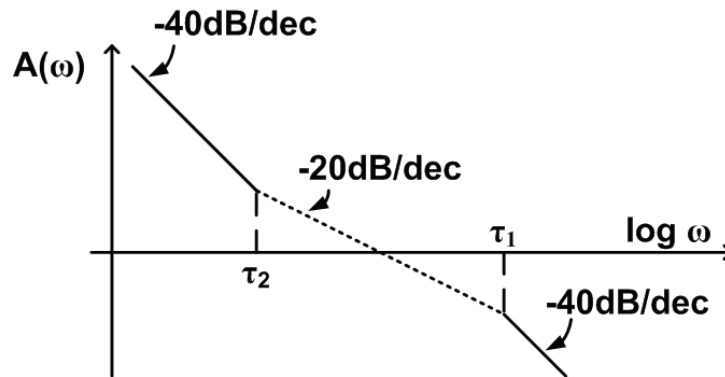


Figure 4.9: Amplitude response of (4.35)

4.1.8 Loop filter design

A complete block diagram of the PLL and a model are presented in Figure 4.10(a) and (b), respectively. The only difference with the simple PLL of Figure 4.6 is that the PLL in Figure 4.10 has a divider in the feedback loop. Therefore, the open loop transfer function is still the same as that of a simple PLL, but closed loop transfer differs:

$$A_f(s) = \frac{A(s)}{1 + H(s)A(s)} = \frac{\frac{K_D K_V F(s)}{s}}{1 + \frac{1}{N} \frac{K_D K_V F(s)}{s}} \quad (4.36)$$

$H(s)$ of the simple PLL is 1, and that, with a frequency divider is $1/N$. To determine loop stability, we look at the frequency response of the loop gain $T(s)$ which is $H(s)A(s)$.

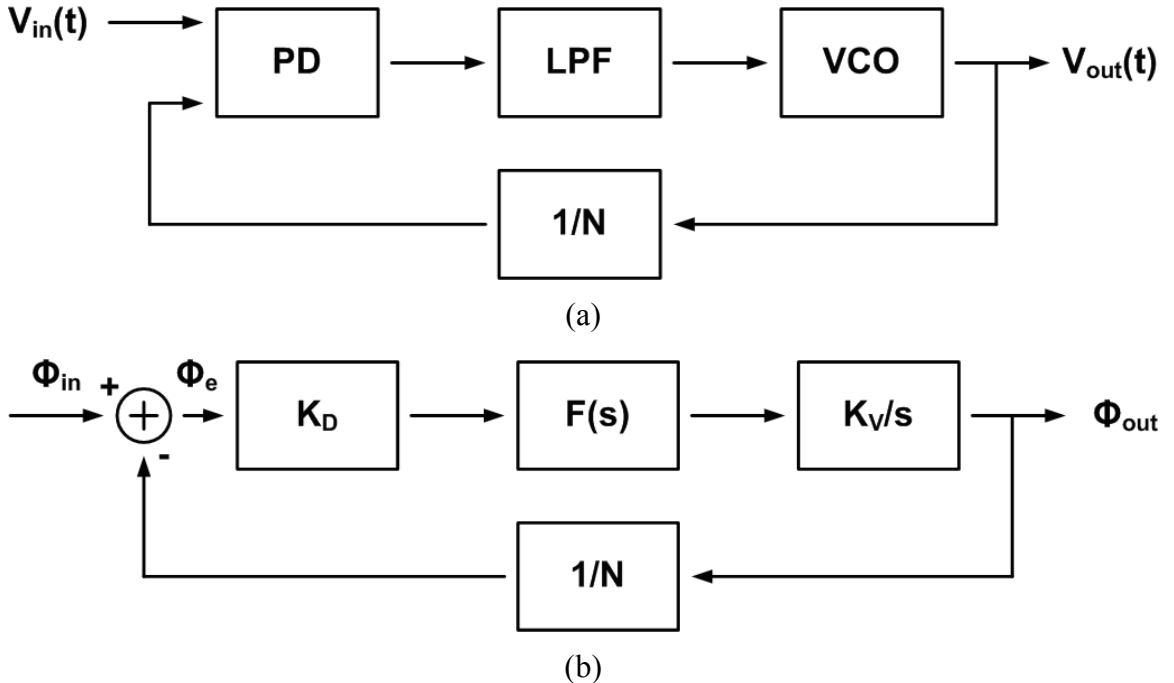


Figure 4.10: (a) Complete block diagram of the PLL and (b) model

The design goal for the loop filter of Figure 4.7(c) is to have the maximum phase margin at the unity gain frequency ω_c , as shown in Figure 4.11. The design procedure to decide

physical parameters to achieve this goal will be explained.

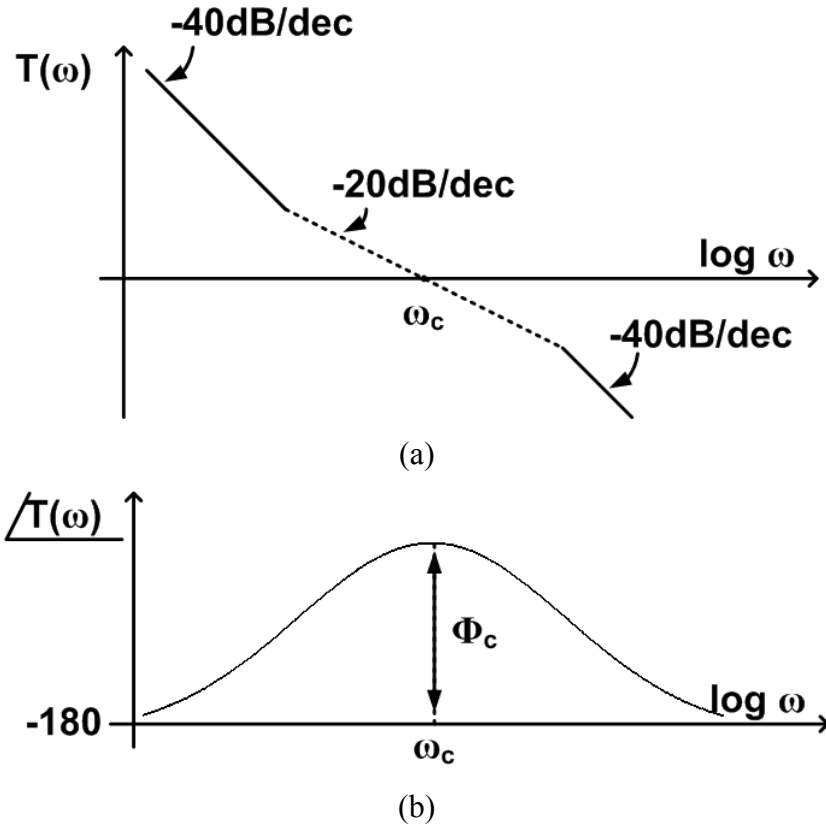


Figure 4.11: Design goal of loop filter is to have the maximum phase margin at the unit gain frequency.; (a) amplitude response and (b) phase response of loop gain $T(\omega)$

The loop gain $T(s)$ with the filter in Figure 4.7(c) is

$$T(s) = \frac{K_D K_V}{N(C_1 + C_2)} \cdot \frac{1 + s\tau_2}{s^2(1 + s\tau_1)} \quad (4.37)$$

Since there are two poles at zero frequency, the PLL is a type 2 PLL. The physical parameters of the filter are chosen to achieve maximum phase margin at the unity gain frequency of the loop gain transfer function $T(s)$. Substituting s with $j\omega$ in (4.37) becomes:

$$T(j\omega) = \frac{-K_D K_V}{\omega^2 N(C_1 + C_2)} \cdot \frac{(1 + j\omega\tau_2)}{(1 + j\omega\tau_1)} \quad (4.38)$$

and the phase of $T(j\omega)$ is

$$\angle T(j\omega) = -180 + \tan^{-1}(\omega\tau_2) - \tan^{-1}(\omega\tau_1). \quad (4.39)$$

Then the phase margin is

$$\phi(\omega) = \angle T(j\omega) + 180 = \tan^{-1}(\omega\tau_2) - \tan^{-1}(\omega\tau_1). \quad (4.40)$$

The frequency at maximum phase margin (ω_c) is where the derivative of (4.40) becomes zero:

$$\frac{d\phi}{d\omega} = \frac{\tau_2}{1+(\omega\tau_2)^2} - \frac{\tau_1}{1+(\omega\tau_1)^2} = 0 \quad (4.41)$$

and unit gain frequency ω_c becomes

$$\omega_c = \frac{1}{\sqrt{\tau_1\tau_2}} = \sqrt{\omega_p\omega_z} \quad (4.42)$$

since ω_p and ω_z are $1/\tau_1$ and $1/\tau_2$, respectively. At unit gain frequency ω_c , τ_1 is equal to $1/\omega_c \tau_2$. Then the phase margin at unit gain frequency becomes

$$\phi(\omega_c) = \tan^{-1}\left(\frac{1}{\omega_c\tau_1}\right) - \tan^{-1}(\omega_c\tau_1). \quad (4.43)$$

In order to organize the phase margin in terms of τ_1 , take the tangent in both sides of (4.43).

$$\tan(\phi(\omega_c)) = \tan\left[\tan^{-1}\left(\frac{1}{\omega_c\tau_1}\right) - \tan^{-1}(\omega_c\tau_1)\right]. \quad (4.44)$$

and use the following relationship for (4.44).

$$\tan(A \pm B) = \frac{\tan A \pm \tan B}{1 \mp \tan A \cdot \tan B}. \quad (4.45)$$

Then (4.44) becomes

$$\tan(\phi(\omega_c)) = \frac{\tan\left(\tan^{-1}\left(\frac{1}{\omega_c\tau_1}\right)\right) - \tan\left(\tan^{-1}(\omega_c\tau_1)\right)}{1 + \tan\left(\tan^{-1}\left(\frac{1}{\omega_c\tau_1}\right)\right) \cdot \tan\left(\tan^{-1}(\omega_c\tau_1)\right)} = \frac{1}{2}\left(\frac{1}{\omega_c\tau_1} - \omega_c\tau_1\right). \quad (4.46)$$

Solving (4.46) gives

$$\begin{aligned} (\omega_c\tau_1)^2 + (\omega_c\tau_1)2\tan(\phi(\omega_c)) - 1 &= 0 \\ \tau_1 &= \frac{\sec\phi(\omega_c) - \tan\phi(\omega_c)}{\omega_c} \end{aligned} \quad (4.47)$$

The time constant τ_1 is given by the desired loop bandwidth and phase margin. Then we can get τ_2 from (4.42)

$$\tau_2 = \frac{1}{\omega_c^2\tau_1} \quad (4.48)$$

C_1 , C_2 , and R can be calculated from these two time constants in (4.47) and (4.48). Then from the requirement that the magnitude of $T(j\omega)$ is 1 at ω_c . in (4.38)

$$C_{tot} = C_1 + C_2 = \frac{K_D K_V}{\omega_c^2 N} \cdot \sqrt{\frac{1 + (\omega_c\tau_2)^2}{1 + (\omega_c\tau_1)^2}} \quad (4.49)$$

and original physical definition of time constants:

$$\begin{aligned} \tau_1 &= R \frac{C_1 C_2}{C_1 + C_2} \\ \tau_2 &= RC_1 \end{aligned} \quad (4.50)$$

Therefore, each physical parameter becomes

$$C_2 = C_{tot} \frac{\tau_1}{\tau_2} \quad (4.51)$$

$$C_1 = C_{tot} - C_2 \quad (4.52)$$

$$R_2 = \frac{\tau_2}{C_1} \quad (4.53)$$

4.1.9 Output noise power of PLL

A simplified noise model of the PLL in Figure 4.10 is presented in Figure 4.12. Noise of each block is represented as output-referred noise. The reference noise is the noise of reference input, while the PFD noise, the LPF noise, the VCO noise, and the divider noise represent the noise from each functional block in PLL. Since each noise source is uncorrelated, the total output noise power is simply the sum of individual output noise powers. The total output noise power is

$$\phi_{no}^2 = N^2(\phi_{nr}^2 + \phi_{neq}^2) \left(\frac{T(s)}{1+T(s)} \right)^2 + \phi_{nv}^2 \left(\frac{1}{1+T(s)} \right)^2 \quad (4.54)$$

where $T(s) = A(s)H(s) = \frac{K_D K_V F(s)}{sN}$ and $\phi_{neq}^2 = \frac{1}{K_D^2} \phi_{np}^2 + \frac{1}{K_D^2 F(s)^2} \phi_{nl}^2 + \phi_{nd}^2$. An

interesting observation is that the noise from VCO to the output has a high-pass transfer function and the other noise sources have a low-pass transfer function from their noise sources to the output. Therefore, from the oscillation frequency of the VCO, ω_{out} , up to the bandwidth of the PLL, $\omega_{out} + \omega_c$, the output noise follows the noise from reference signal, PFD, LPF, and Divider, and after the bandwidth frequency the output noise follows the noise of the VCO. So, there exists a tradeoff in deciding the bandwidth of the PLL. If the noise from the VCO is low compared to the sum of other noises, then a narrow bandwidth is better for achieving low output noise. But, on the other hand, a narrow bandwidth requires a longer time to follow the changes in input frequency or phase.

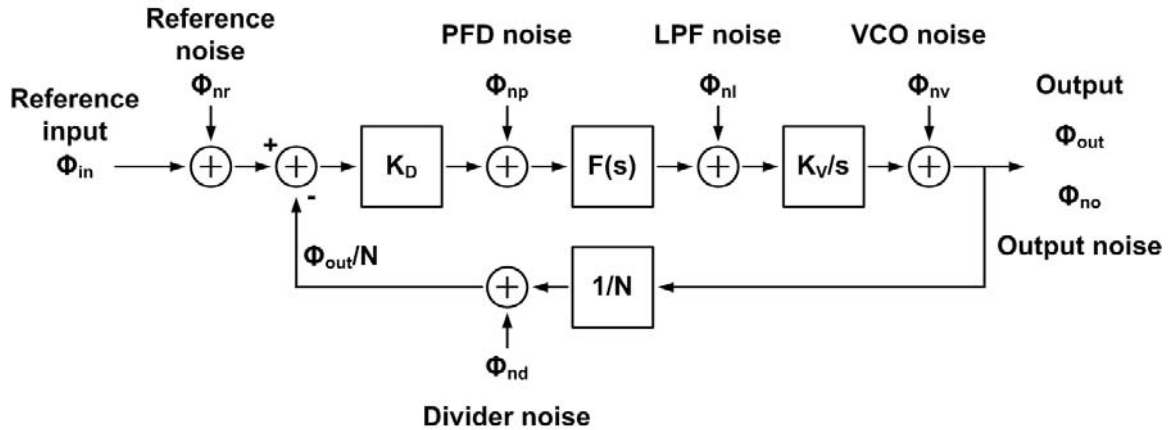


Figure 4.12: PLL with output-referred noise for each block

4.2. A low-jitter PLL with capacitive coupling

Figure 4.13 shows a block diagram of the charge pump PLL with capacitive coupling[33]. The mathematical model developed for the PLL of Figure 4.10 can be used for this PLL without modification. Even though the VCO is now a four stage-coupled oscillator, the same transfer function, K_V/s , can still be used. The only difference for a multi-stage oscillator is that the noise characteristic of the VCO is changed. Since the noise from the VCO only affects the out-of-band noise of the PLL, we can use a low bandwidth PLL in order to take advantage of low phase noise characteristics of the multi-stage coupled oscillators. The four LC oscillator stages in Figure 4.13 are coupled both with transistors and with capacitors, in order to take advantage of in-phase coupling. Separate current sources are used to supply current for the cross-coupled transistors that generate negative resistance (i.e. the regeneration current) and for the coupling transistors. The frequency of one of the eight CMOS signals from the oscillator is divided by 32 and

compared with the reference clock, and the output signal of the charge pump controls the operating frequency.

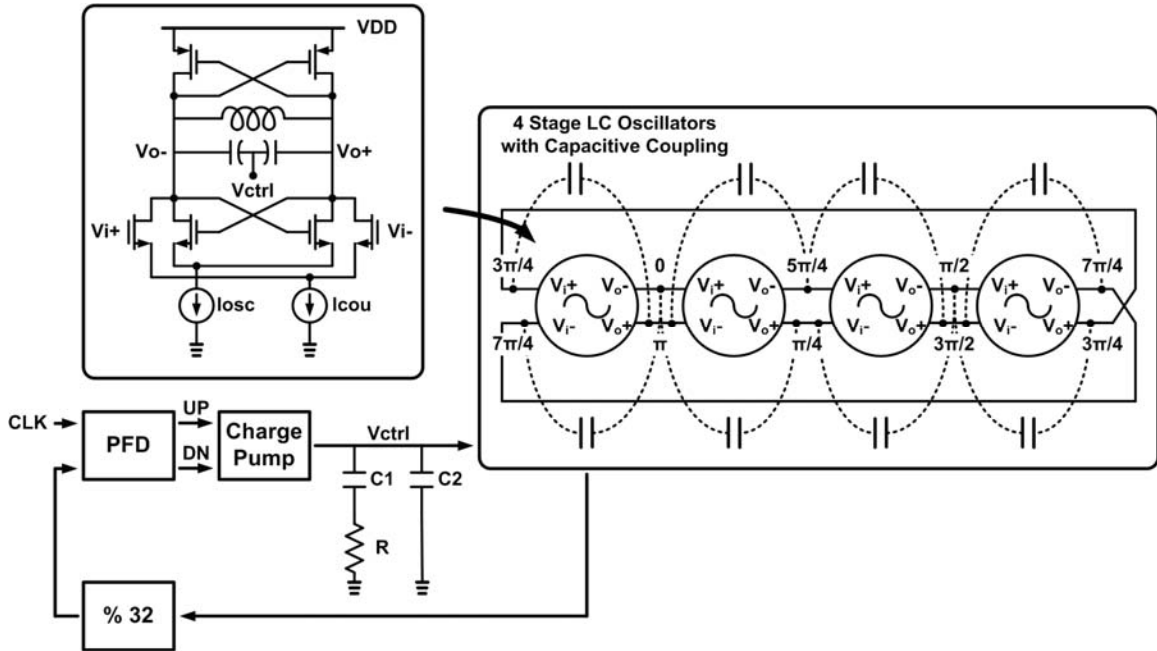


Figure 4.13: PLL with capacitive coupling

The functional blocks are now described in detail.

4.2.1 Phase frequency detector (PFD)

The phase frequency detector in Figure 4.14 generates the control voltages, *up* and *dn*, based on the phase difference and frequency difference between the reference clock and the output signal of the divider. The PFD generates more *up* signals when the frequency of the reference clock is higher than the signal from the divider, or the phase of the reference clock is ahead of the phase of the signal from the divider. On the other hand, the PFD generates more *dn* signals when the frequency of the divider output is higher or the phase of the divided output is leading the phase of the reference clock. When the frequency or the phases of the two inputs are the same, the widths of the control signals,

up and dn , are the same. The width of these two signals represents the timing delay from the two outputs of the PFD to the reset port, RN . When these pulse widths are too narrow for the charge pump to respond properly, it is said that the PLL has dead-zone. Therefore, adding more delay cells in the feedback path from the outputs of the PFD to the reset port results in a wider width for those control signals and eliminates the dead-zone problem[28].

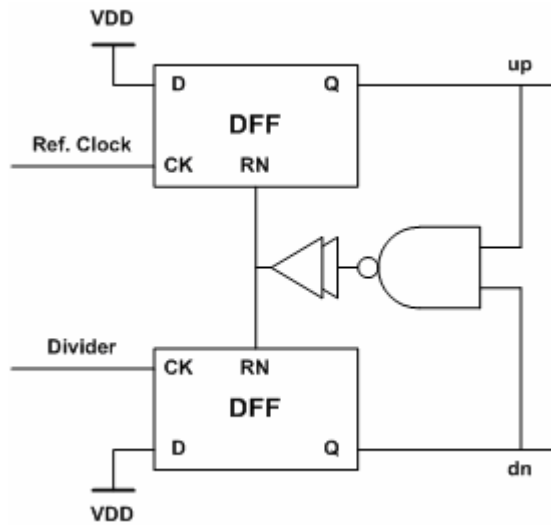


Figure 4.14: Phase frequency detector(PFD)

4.2.2 Charge pump and loop filter

The charge pump and loop filter in Figure 4.15[34] set up the control voltage for the oscillator. When more up signals come from the PFD, the charge pump increases the voltage at the $vctrl$ node and increases the VCO operating frequency. On the other hand, when there are more dn signals, the charge pump decreases the voltage at the $vctrl$ node, reducing operating frequency of the oscillator. The charge pump consists of two current sources and four current steering switches to improve switching time.

With a VCO gain of 500MHz/V, a 100uA charge pump current, a 1MHz loop bandwidth, and an 85-degree phase margin, the physical parameters of C_1 , C_2 , and R can be calculated from (4.47) to (4.53). The values of C_1 , C_2 , and R are 144pF, 0.275pF, and 25.3k Ω , respectively. This is equivalent to a zero frequency of 4.4kHz and the pole frequency of 22.9MHz. Therefore, only the frequency range from 4.4 kHz to 22.9MHz shows an amplitude slope of -20dB/dec. The narrow frequency span of the -20dB/dec region results from the assumption that the unity gain frequency of the loop gain $T(s)$ is the geometric mean of zero and pole frequencies in (4.42). When we consider process variations of the passive components, a wide frequency span for the -20dB/dec region guarantees a stable loop performance. Therefore, in reality, the pole frequency is located far from the unit gain frequency of the loop gain. The values of passive components used for the PLL are 60pF, 4pF, and 108k Ω for C_1 , C_2 , and R , respectively. The zero frequency with these values is 24.6kHz, and the pole frequency is 393kHz. The phase margin is 88 degrees from (4.40).

The size of the LPF is highly dependent on the loop bandwidth (ω_p) of the PLL. Achieving a narrow loop bandwidth requires large capacitors. For example, to achieve 1kHz bandwidth with this PLL, we need capacitance close to 1uF for C_1 . Therefore, usually the physical area of the filter decides the bandwidth of the filter in practice.

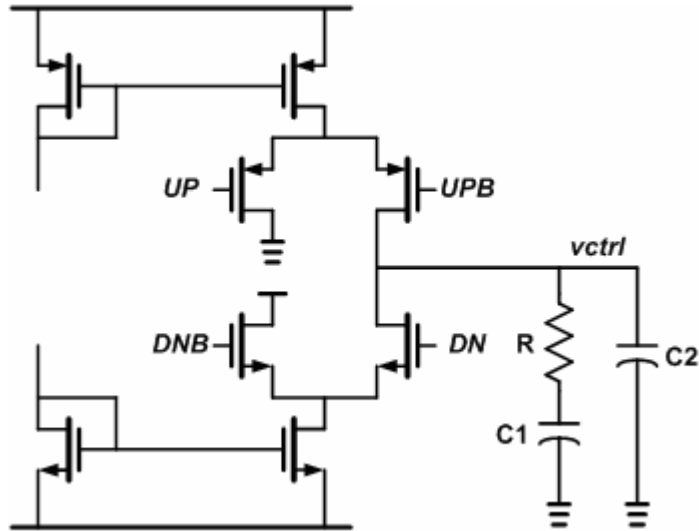


Figure 4.15: Charge pump and filter

4.2.3 Edge match circuit

For proper operation of the charge pump, two control signals from the PFD, up and dn , and their complements, upb and dnb , are required. Inverters can be used to make complementary signals, but the unit inverter delay between up or dn and their complements would cause timing errors in the charge pump. In order to decrease the timing difference due to the inverters, the edge match circuit in Figure 4.16 is used to align the control signals for the charge pump. The buffer in Figure 4.16 is a single CMOS stage where an NMOS transistor takes the place of the PMOS transistor, and a PMOS transistor takes the place of the NMOS transistor in a standard CMOS inverter. Summing two output signals, one from the inverter and buffer and the other from a buffer pair, results in a new averaged signal. Because of averaging the timing difference between output edges is greatly reduced.

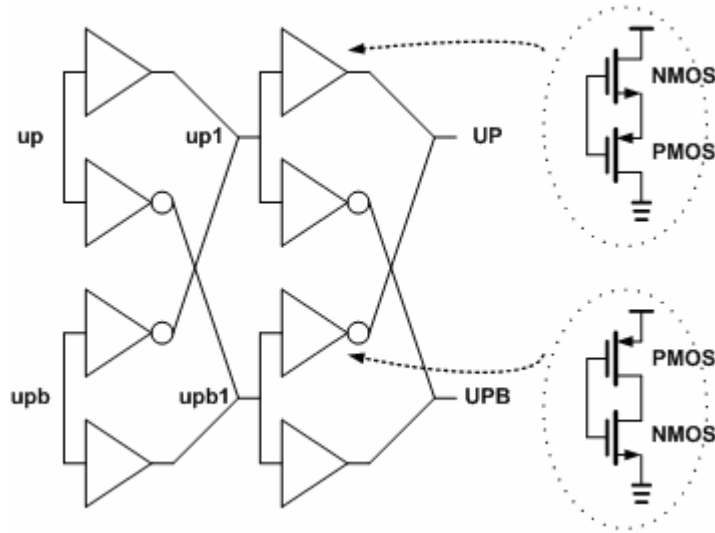


Figure 4.16: Edge match circuit

4.3. Image rejection ratio(IRR)

4.3.1 Basic theory

Figure 4.17 shows the schematic of the Hartley image-reject transmitter[28].

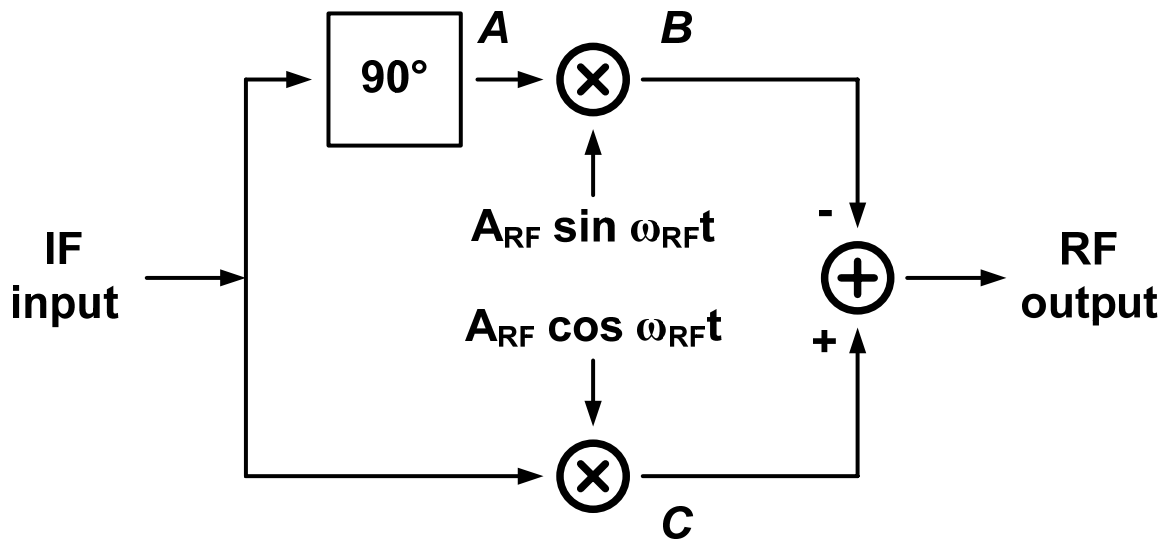


Figure 4.17: Hartley image-reject transmitter

Suppose that the IF input signal is

$$x(t) = A_{IF} \cos \omega_{IF} t, \quad (4.55)$$

then the signal after 90 degree phase shifter at A in Figure 4.17 becomes

$$x_A(t) = A_{IF} \sin \omega_{IF} t. \quad (4.56)$$

Multiplying those IF signals with RF signals gives

$$\begin{aligned} x_B(t) &= A_{IF} \sin \omega_{IF} t \cdot A_{RF} \sin \omega_{RF} t \\ &= \frac{A_{IF} A_{RF}}{2} [-\cos(\omega_{RF} + \omega_{IF})t + \cos(\omega_{RF} - \omega_{IF})t] \end{aligned} \quad (4.57)$$

$$\begin{aligned} x_C(t) &= A_{IF} \cos \omega_{IF} t \cdot A_{RF} \cos \omega_{RF} t \\ &= \frac{A_{IF} A_{RF}}{2} [\cos(\omega_{RF} + \omega_{IF})t + \cos(\omega_{RF} - \omega_{IF})t] \end{aligned} \quad (4.58)$$

at B and C respectively.

The RF output signal is the sum of those two signals in (4.57) and (4.58) and becomes

$$x_{signal}(t) = A_{IF} A_{RF} \cos(\omega_{RF} + \omega_{IF})t. \quad (4.59)$$

The image signals at $\omega_{RF}-\omega_{IF}$ are suppressed perfectly. However, when there is a phase or amplitude mismatches between two RF signals, image signals are not suppressed. The case with mismatches in RF signals can be derived in the same manner.

Suppose the two signals from the oscillator are $A_{RF} \sin \omega_{RF} t$ and $(A_{RF} + \varepsilon) \cos(\omega_{RF} t + \theta)$ where ε and θ are amplitude and phase mismatch respectively.

Multiplying those IF signals with RF signals gives

$$\begin{aligned} x_B(t) &= A_{IF} \sin \omega_{IF} t \cdot A_{RF} \sin \omega_{RF} t \\ &= \frac{A_{IF} A_{RF}}{2} [-\cos(\omega_{RF} + \omega_{IF})t + \cos(\omega_{RF} - \omega_{IF})t] \end{aligned} \quad (4.60)$$

$$\begin{aligned}
x_C(t) &= A_{IF} \cos \omega_{IF} t \cdot (A_{RF} + \varepsilon) \cos(\omega_{RF} t + \theta) \\
&= \frac{A_{IF}(A_{RF} + \varepsilon)}{2} [\cos((\omega_{RF} + \omega_{IF})t + \theta) + \cos((\omega_{RF} - \omega_{IF})t + \theta)]
\end{aligned} \tag{4.61}$$

at B and C respectively.

The sum has an image component at $\omega_{RF}-\omega_{IF}$ along with the desired signal at $\omega_{RF}+\omega_{IF}$.

The desired signal is

$$x_{signal}(t) = \frac{A_{IF}(A_{RF} + \varepsilon)}{2} \cos((\omega_{RF} + \omega_{IF})t + \theta) + \frac{A_{IF}A_{RF}}{2} \cos(\omega_{RF} + \omega_{IF})t, \tag{4.62}$$

and the image signal becomes

$$x_{image}(t) = \frac{A_{IF}(A_{RF} + \varepsilon)}{2} \cos((\omega_{RF} - \omega_{IF})t + \theta) - \frac{A_{IF}A_{RF}}{2} \cos(\omega_{RF} - \omega_{IF})t \tag{4.63}$$

The average power of $x_{signal}(t)$ is

$$\begin{aligned}
P_{signal} &= \frac{1}{T} \int_0^T x_{signal}^2(t) dt \\
&= \frac{A_{IF}^2}{4} \left[\frac{(A_{RF} + \varepsilon)^2}{2} + \frac{A_{RF}^2}{2} + A_{RF}(A_{RF} + \varepsilon) \cos \theta \right],
\end{aligned} \tag{4.64}$$

and the power of the image signal becomes

$$\begin{aligned}
P_{image} &= \frac{1}{T} \int_0^T x_{image}^2(t) dt \\
&= \frac{A_{IF}^2}{4} \left[\frac{(A_{RF} + \varepsilon)^2}{2} + \frac{A_{RF}^2}{2} - A_{RF}(A_{RF} + \varepsilon) \cos \theta \right]
\end{aligned} \tag{4.65}$$

The image to signal ratio becomes

$$\frac{P_{image}}{P_{signal}} = \frac{(A_{RF} + \varepsilon)^2 + A_{RF}^2 - 2A_{RF}(A_{RF} + \varepsilon) \cos \theta}{(A_{RF} + \varepsilon)^2 + A_{RF}^2 + 2A_{RF}(A_{RF} + \varepsilon) \cos \theta} \tag{4.66}$$

Figure 4.18 shows the image to signal ratio on a dB scale with different amplitude and phase mismatches. With zero amplitude and zero phase errors the image to signal ratio is

approximately -80 dB, but degrades to approximately -30 dB with only 3 degree phase error. With 0.1 percent amplitude mismatch the signal to noise ratio is approximately -35 dB and -30 dB with 0 and 3 degree phase errors respectively.

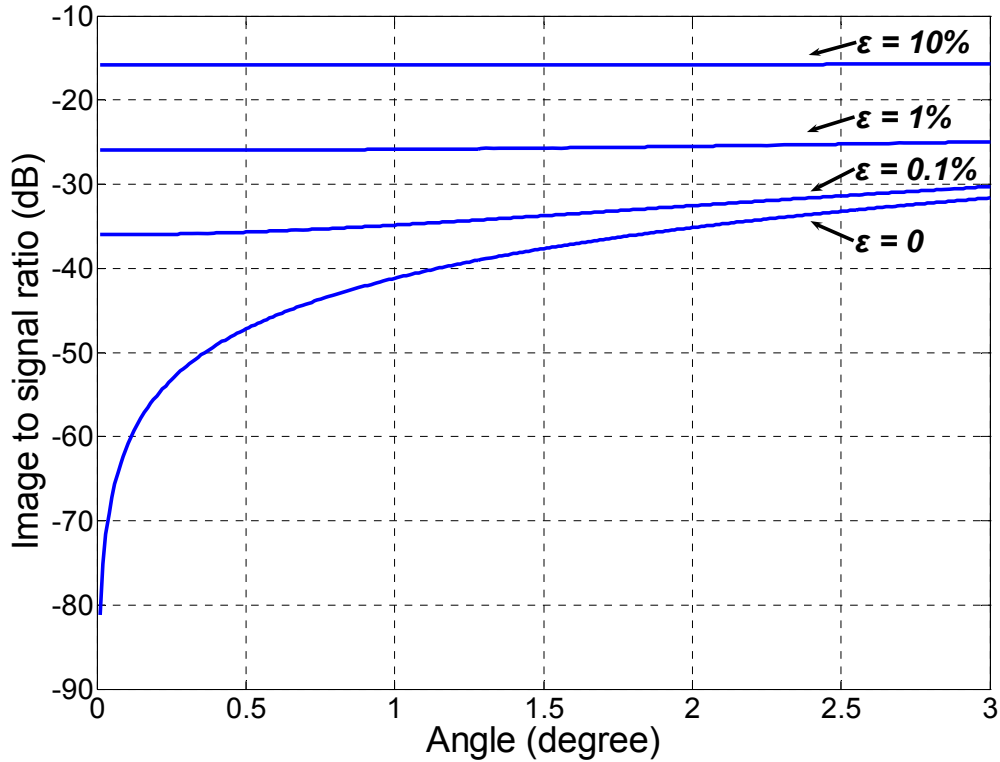


Figure 4.18: Image to signal ratio with amplitude and phase mismatches

4.3.2 Four stage oscillator with capacitive coupling

For the four stage oscillator with capacitive coupling, the phase spacing error can be estimated by using IRR. The schematic to measure the IRR is shown in Figure 4.19. Two four-stage oscillators, one with capacitive coupling and the other has capacitive loading, are compared with the deliberate mismatch (50fF capacitor is connected to one of the output nodes). Since the two coupled oscillators have same capacitive loading, they operate at almost the same frequency (there is approximately a 20MHz frequency

difference) so that we can estimate how much capacitive coupling reduces phase noise and phase spacing error. Figure 4.20 shows the phase noise of both oscillators. With the capacitive coupling the phase noise at 1MHz offset is only 0.2dBc/Hz lower than the phase noise of the oscillator without capacitive coupling.

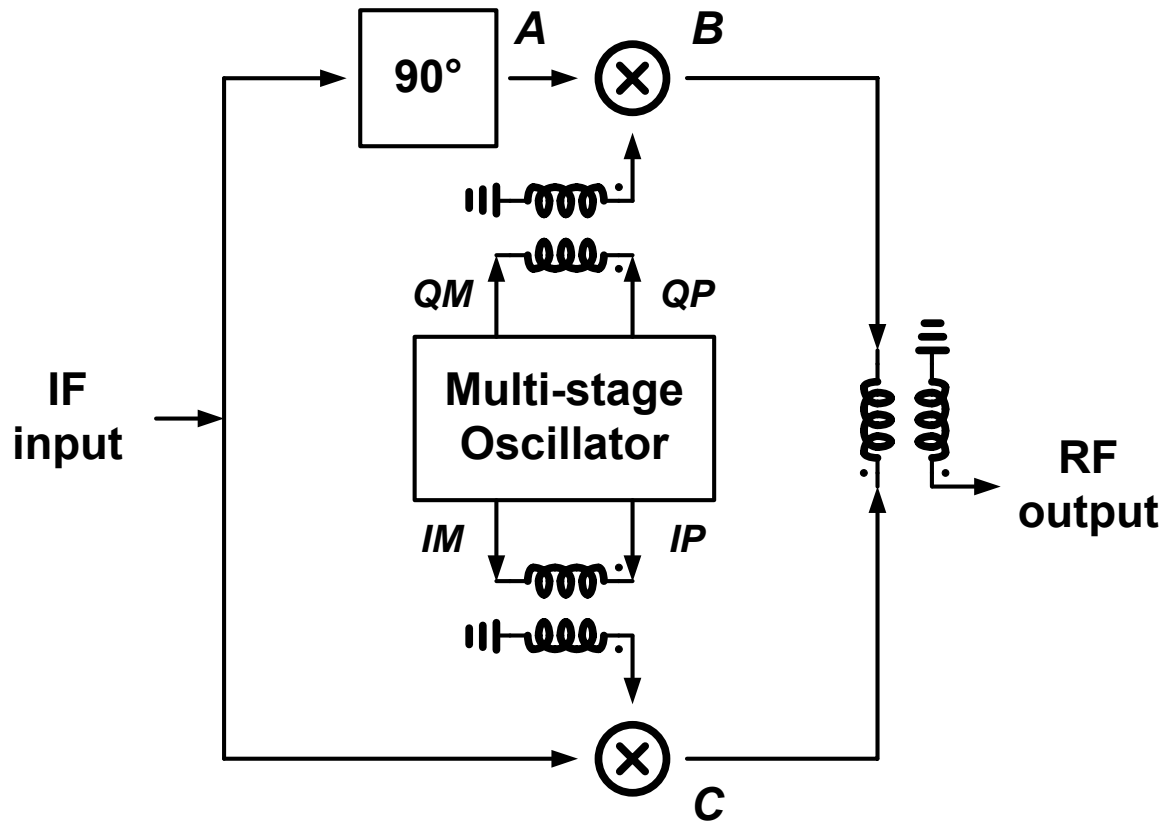


Figure 4.19: Schematic to measure the image rejection ratio

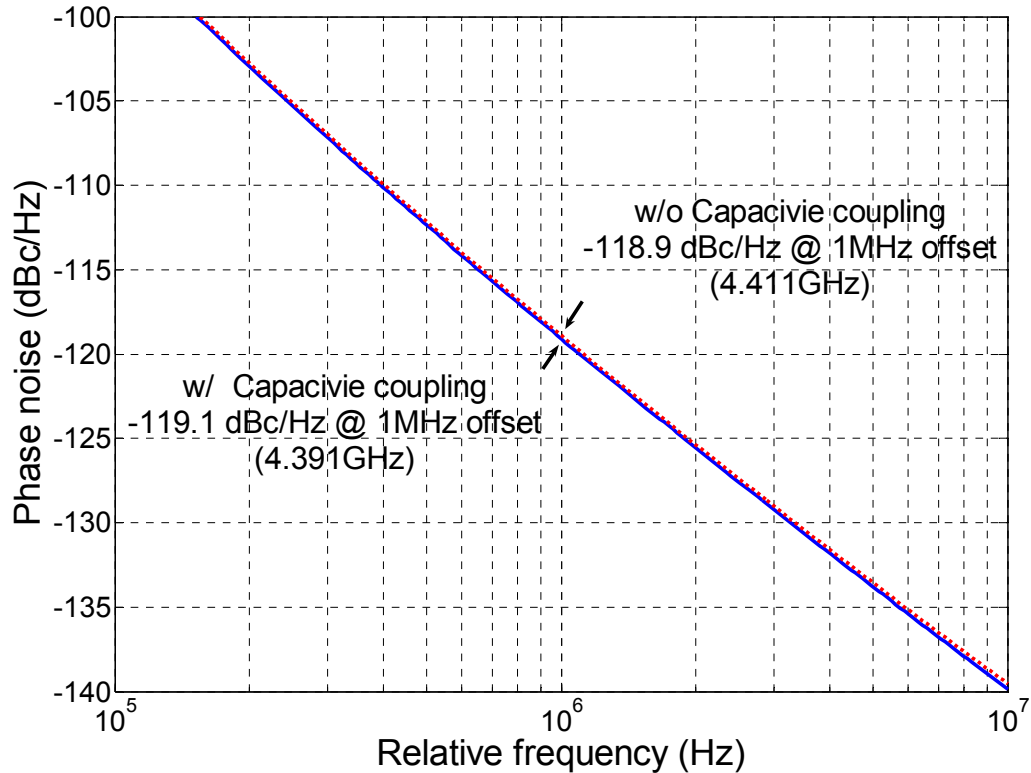
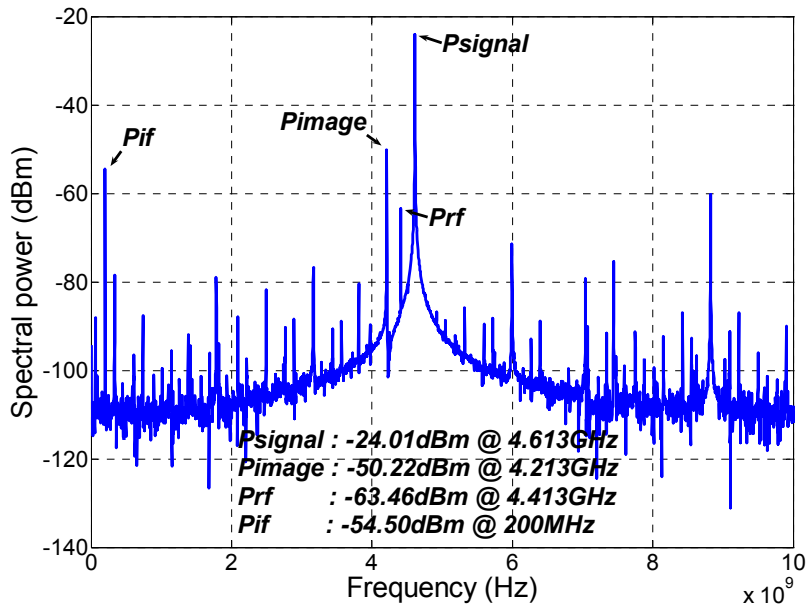
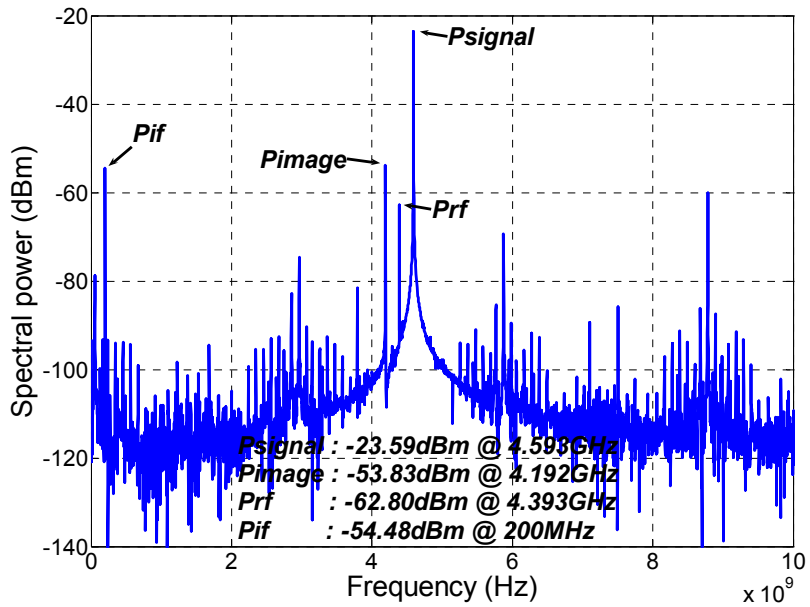


Figure 4.20: Phase noise of the four stage coupled oscillators with deliberate mismatch; w/ capacitive coupling shows -119.1 dBc/Hz at 1MHz offset and w/o capacitive coupling shows -118.9 dBc/Hz at the same offset.

However, when we look at the IRR of both oscillators (Figure 4.21 (a) and (b) respectively), the oscillator with capacitive coupling shows 5 dB more IRR than the oscillator without capacitive coupling. Therefore, we can say that the capacitive coupling is far more effective in decreasing the phase spacing error which is due to the increased coupling power between oscillators. The IRR which is the difference between the spectral power of the signal (P_{signal}) and the image (P_{image}) is 26.21dB without capacitive coupling and 30.24dB with capacitive coupling.



(a)



(b)

Figure 4.21: IRR of the four stage oscillator with deliberate mismatch; (a) IIR of 26.21dB with capacitive loading (b) IIR of 30.24dB with capacitive coupling

4.4. Measurement

A prototype PLL, die photo shown in Figure 4.22, was fabricated in $0.13\ \mu\text{m}$ CMOS. The PLL with $1\ \text{pF}$ coupling capacitors, $2\ \text{mA}$ regeneration current, and $1\ \text{mA}$ transistor coupling current has a measured tuning range of $403\ \text{MHz}$, from $3.066\ \text{GHz}$ to $3.469\ \text{GHz}$. When locked to a $108.4\ \text{MHz}$ reference clock, and measured over a period of 25 minutes, the PLL achieves a long-term RMS jitter of $1.61\ \text{ps}$ at $3.469\ \text{GHz}$, as shown in Figure 4.23. The measured RMS and pk-pk jitter versus frequency is shown in Figure 4.24(a) and (b) respectively. The total power consumption, including the power dissipated by the output buffer, is $32.5\ \text{mW}$, and total active area is $0.49\ \text{mm}^2$.

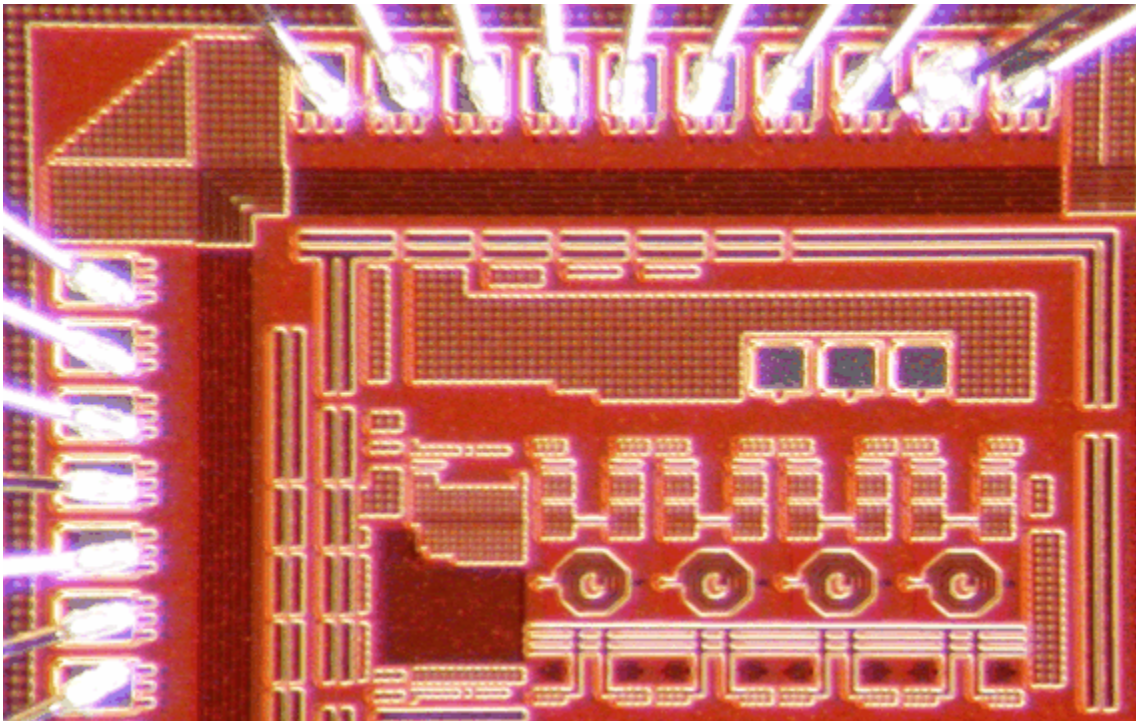


Figure 4.22: Chip microphotograph of PLL

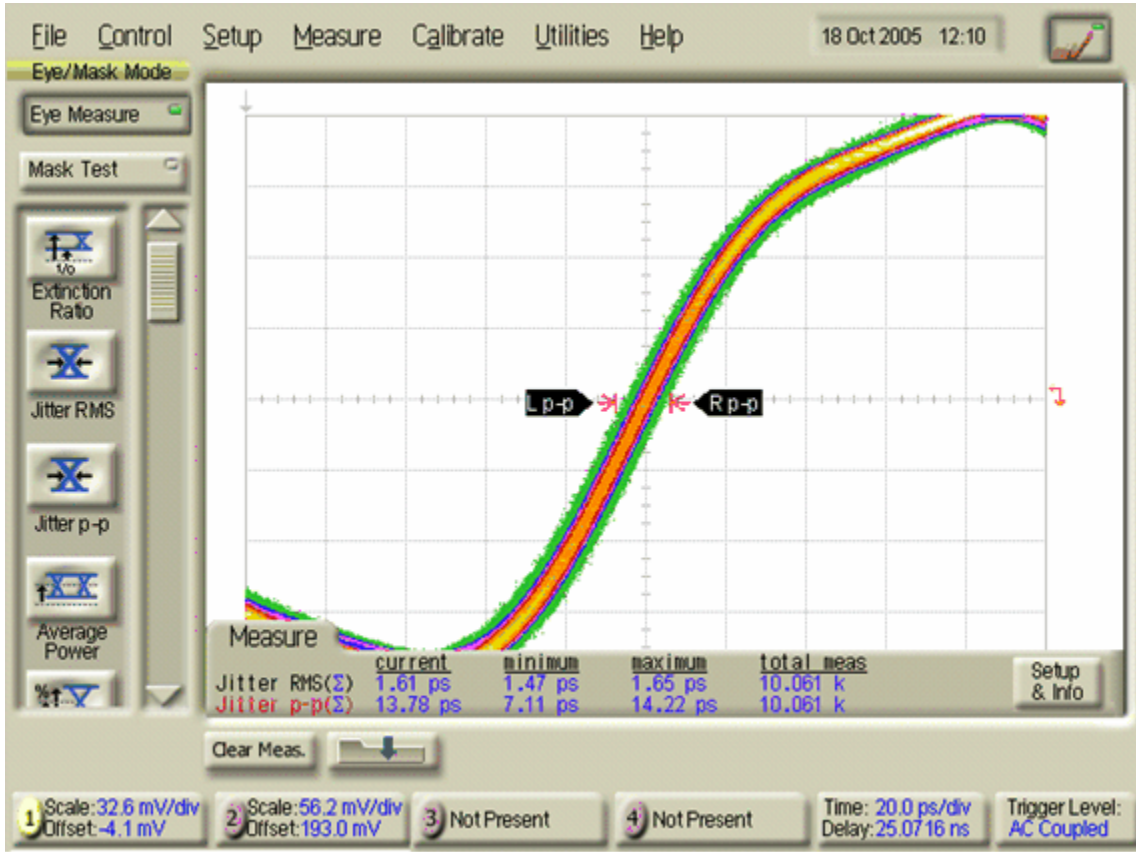
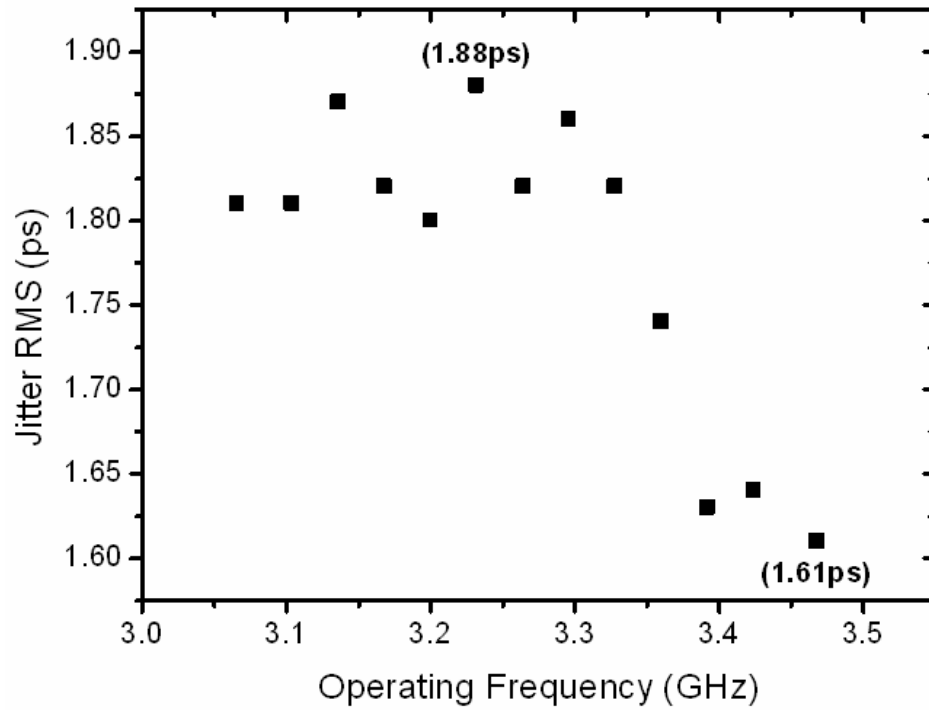
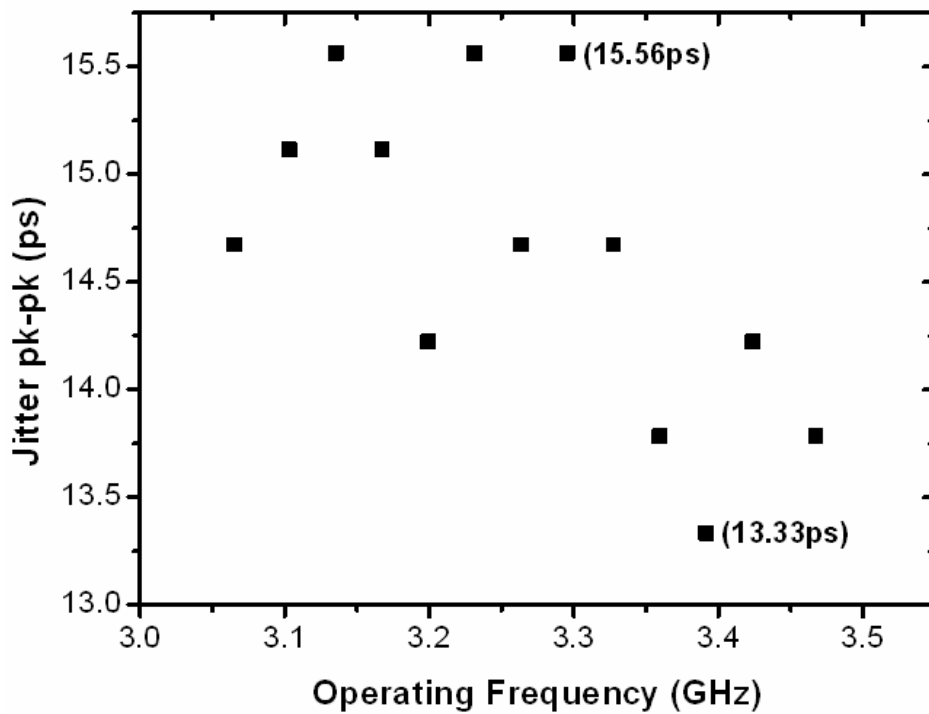


Figure 4.23: 1.61 ps RMS jitter and 13.78 ps pk-pk jitter of the digital output of the PLL at 3.47 GHz



(a)



(b)

Figure 4.24: (a) Measured RMS jitter and (b) measured pk-pk jitter

Figure 4.25 compares the jitter and power dissipation of recently published CMOS LC PLLs[35-38] and this work. [35-37] measure RMS jitter by integrating the measured phase noise, from 10 kHz to 40 MHz, from 1 kHz to 10 MHz, and from 50 kHz to 80 MHz respectively.

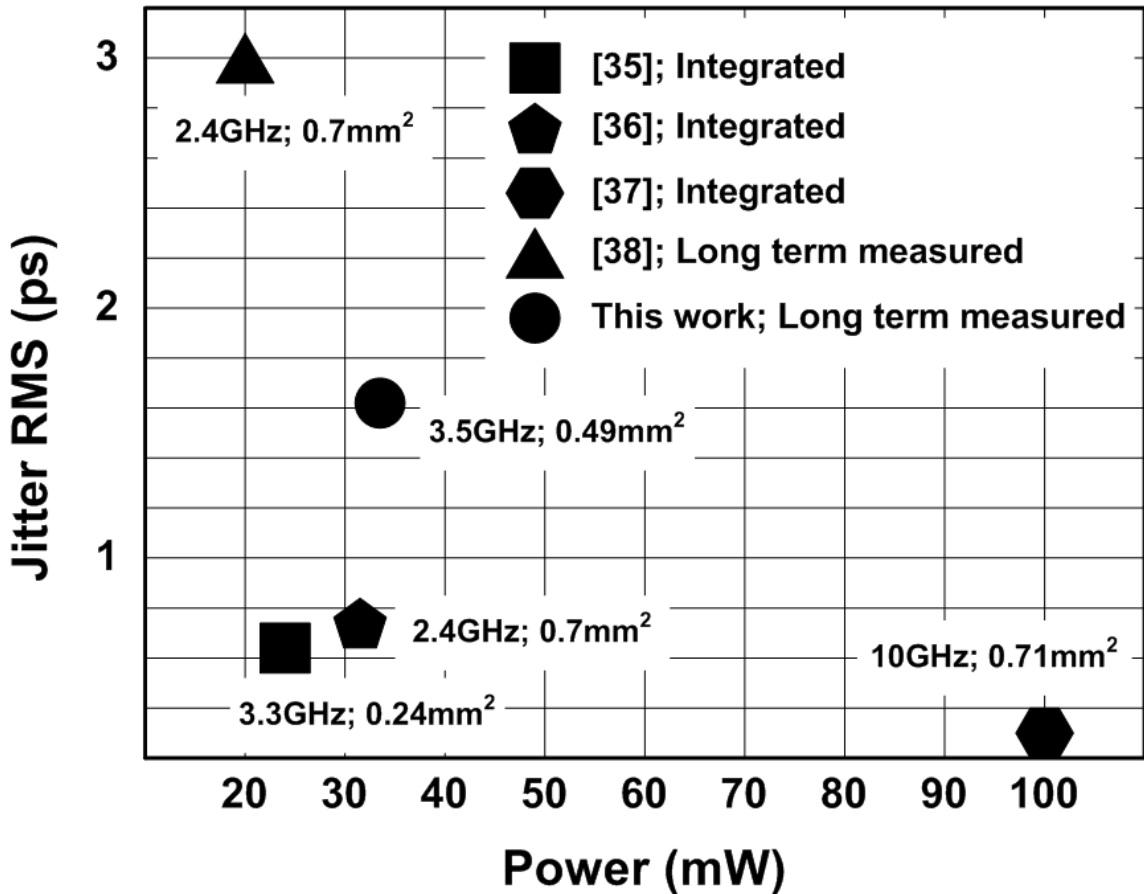


Figure 4.25: Jitter and power dissipation of published CMOS LC-PLLs and this work; [35-37] got their RMS jitter from the phase noise measurement, and [38] and this work got the RMS jitter from the long term measurement with the oscilloscope.

4.5. Conclusion

The noise from VCO to the PLL output has a high-pass transfer function, while the other noise sources have a low-pass transfer function to the output. Within the bandwidth of the PLL from the oscillation frequency, $\omega_{out} \pm \omega_e$, the output noise follows the noise from reference signal, PFD, LPF, and Divider, and beyond this bandwidth the output noise follows the noise of the VCO. In this way there exists a tradeoff in the bandwidth of the PLL. If the noise from the VCO is low compared to the sum of the other noises, then a narrow bandwidth is better for achieving low output noise. But, on the other hand, a narrow bandwidth requires a longer time to follow the changes in the reference input frequency or phase. Since capacitively coupled oscillators have lower phase noise than conventional coupled oscillators, it makes possible to have narrow bandwidth and minimize the overall PLL output noise.

Chapter V

On-chip serial signaling

This chapter presents circuit techniques which enable 9Gbps serial data communication over long (i.e., >5mm) on-chip transmission lines in 0.13 μ m CMOS. A serial link makes the data transmission possible with only one line or two lines (in case of differential signaling). Assuming that the link replaces an 8-bit wide, the signaling rate on the serial link should be 8 times higher, and the data period of the serialized data should be one-eighth of the period of the original parallel data. Figure 5.1 shows the main functional blocks for the serial data transmission. These are a serializer, line drivers, a transmission line, and comparators.

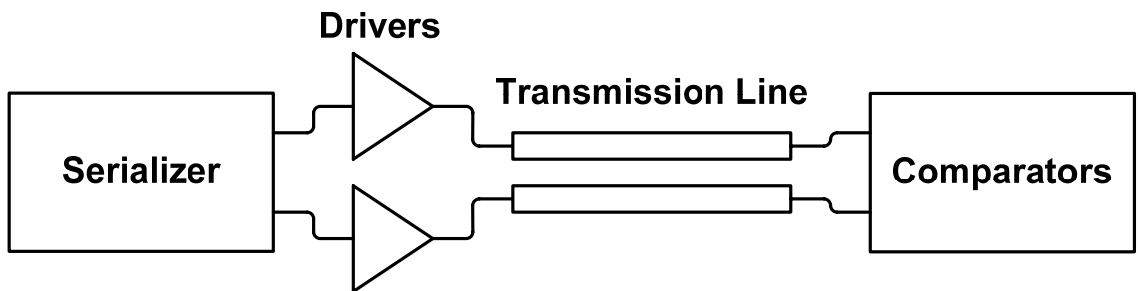


Figure 5.1: Main functional blocks for serial data communication; serializer, data driver, on-chip transmission line, and comparators.

A significant challenge in implementing a serial link is the high clock rate needed. In the example above, we need a clock rate eight times faster than the original parallel bus clock rate for serialization. An even faster clock rate might be required to oversample data in the receiver. An interleaved implementation employing two or more

transmit-and- receive blocks allows us to instead use multiple phases of a slower clock. In this chapter, we describe circuitry to implement a 9Gbps on-chip link. Two interleaved transmit blocks working off 4.5GHz clock phases generate the 9Gbps transmit signal. The receiver is also based on sampling blocks running off phases of a 4.5GHz clock.

The circuit techniques developed for the on-chip serial link are discussed in detail in the following sections, and prototype design along with measurement results are presented in section 5.5.

5.1. Overall block diagram

A block diagram of the on-chip serial link scheme is shown in Figure 5.2. Along with the four main functional blocks-- the serializer, line drivers, on-chip transmission line, and comparators--there is also a PLL, two clock generators, a pre-defined data generator, a de-serializer at receiver, and an error-check block. The pre-defined data generator and error check block are included to measure the performance of the experimental prototype link and are not required in practice.

A single master clock, generated by the PLL, is distributed to both the receiver and transmitter; however no attempt is made to align clock edge distributed to the receiver and transmitter. Even though there is only master clock at 4.5GHz, the whole system operates with two different clock domains--one for the transmitter and the other for the receiver. The transmitter and error checking blocks operate in the same clock domain.

The 1.125GHz 8-bit data words generated by pre-defined data block are serialized to 9Gbps and travel down the long transmission line [20, 39-41] to arrive at the

receiver (RX). Since both the transmitter and receiver share a common master clock, they operate at the same frequency. However these clocks are not in phase and there is also a delay associated with propagation of the signal along the chip transmission line. Since data crosses different clock domains for comparison in the Error Check, synchronization is required to test the operation and reliability of the link.

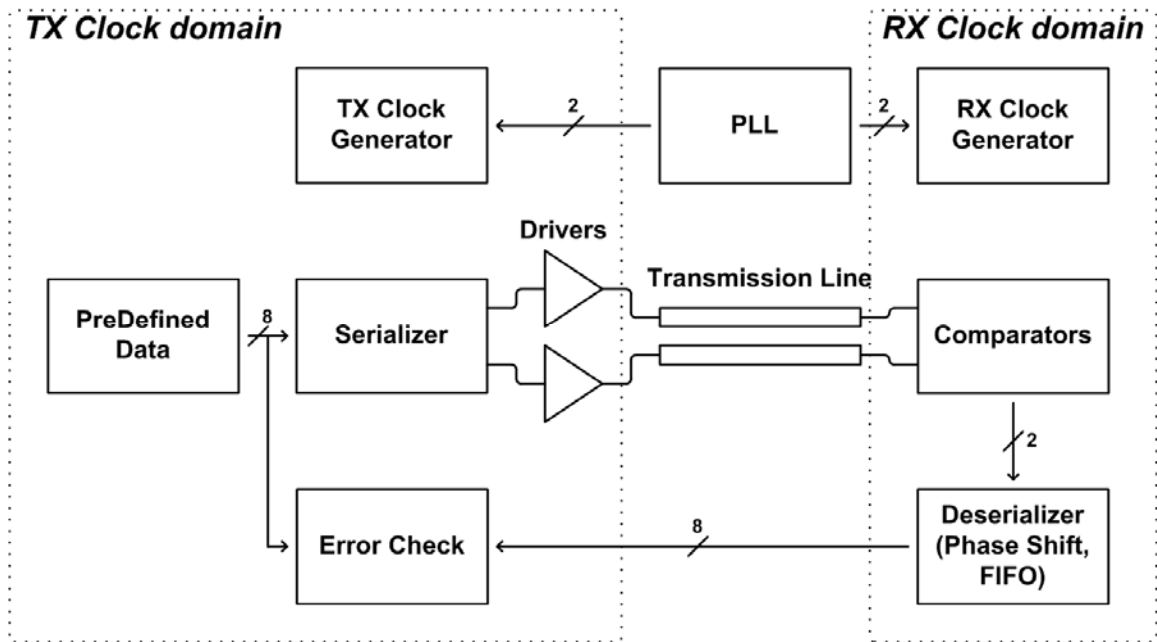


Figure 5.2: Block diagram of on-chip serial link; Serial link consists of two clock domains, TX and RX clock domains. Since both TX and RX share single PLL, their operating frequency is same, but their clock phases are different in order to compensate the delay from the long on-chip transmission line.

5.2. TX (transmitter)

Along with the serializer and transmission-line drivers, the transmitter in Figure 5.3 employs a pre-defined data generator for generation of test data, and a Clock Generator to distribute 1.125GHz, 2.25GHz, and 4.5GHz clock signals from 4.5GHz output of the PLL. Two differential 4.5GHz signals, *inp* and *inn*, from the LC oscillator

of the PLL drive the clock generator which then distributes 4.5GHz, 2.25GHz, and 1.125GHz clock signals to the other blocks. 8-bit differential data at 1.125GHz is generated by the pre-defined data generator and is serialized to a 2-bit differential data signal at 4.5GHz by the serializer. In order to serialize to 9Gbps, two 4.5GHz clock phases are used in the line driver. The phase difference between these two differential clocks is equivalent to the period of the 9Gbps data.

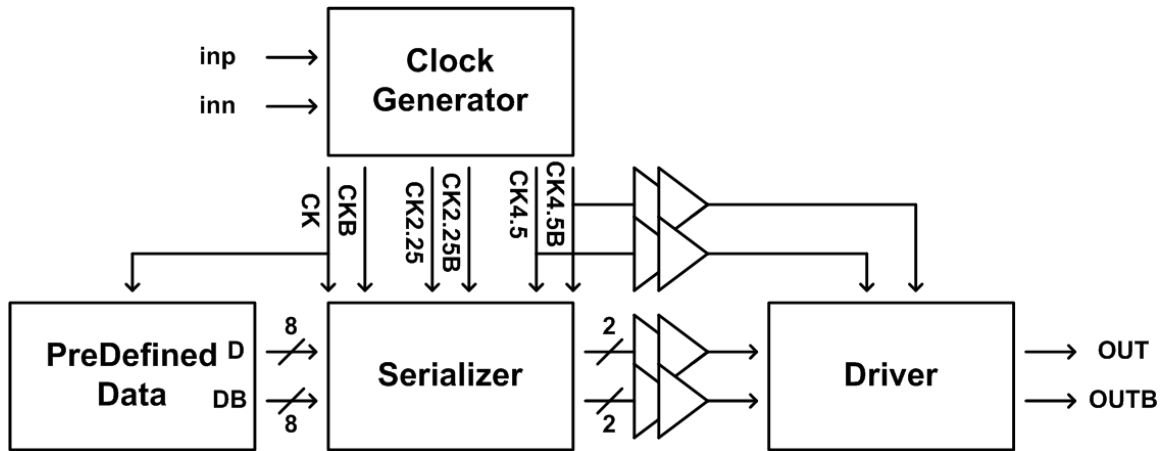


Figure 5.3: Block diagram of the TX (transmitter); transmitter serializes pre-defined data, 8bit 1.125GHz, to 9Gbps and drives long transmission line.

5.2.1 Clock generator

In order to serialize and transmit data, different clock frequencies and phases are required. The clock generator receives two 4.5GHz differential outputs from the PLL, and generates complementary 1.125GHz (CK and CKB), 2.25GHz ($CK2.25$ and $CK2.25B$), and 4.5GHz ($CK4.5$ and $CK4.5B$) clock signals. Usually a divide-by-2 circuit utilizing the complementary outputs of the DFF, Q and QB , can be used to generate half-frequency signals, and in this way two divide-by-2 circuits in series might generate both the 2.25GHz and 1.125GHz clock signals from a 4.5GHz input. However, the series connection of two divide-by-2 circuits does not guarantee that the rising and falling edges

of the 2.25GHz and 1.125GHz clocks are aligned. Instead, the modified clock generator in Figure 5.4 is used to generate correctly aligned clock signals at different frequencies.

In this circuit, DFF *D1* generates a half-frequency signal and *D3* generates a clock that is one-quarter of the frequency of one the 4.5GHz input phases, *inn*. The divided-down clock signals are re-sampled by the other 4.5GHz differential frequency phase, *inp*, by DFFs *D4* and *D5*. In this way, the divided down clock signals, *CK2.25*, *CK2.25B*, *CK*, and *CKB*, are aligned. The edge-match circuit of Figure 4.16 is used at the final stage to reduce delay difference between each clock signal and its complement. Having the edges of the divided clocks aligned makes it easier to control the delays of the signal paths, however, the delay between the original 4.5GHz signal and the divided clock 2.25GHz and 1.125GHz signals still changes with operating frequency.

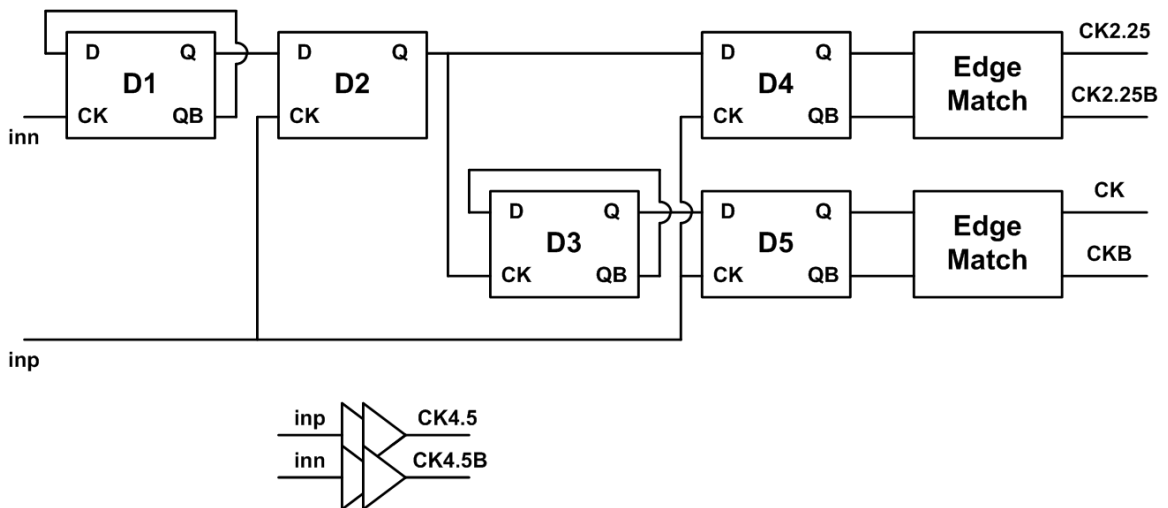


Figure 5.4: Clock generator; *inn* is divided by two and divided by two again at *D1* and *D3* respectively. The divided signals are clocked by the other 4.5GHz signal, *inp*, and aligned.

5.2.2 Serializer

Since we employ two interleaved 4.5GHz transmit blocks, two interleaved parallel streams of 4-bit data at 1.125GHz are serialized to 4.5Gbps. The final 9Gbps serialization is achieved using interleaved line drivers. Figure 5.5 shows one of the two identical 4-bit serializers[42]. In order to properly serialize the data, the original parallel data at 1.125GHz should be properly distributed to both modules in the correct data sequence. $D1$, $D3$, $D5$, and $D7$ are the inputs to one of the modules (Figure 5.5), and $D2$, $D4$, $D6$, and $D8$ are the inputs to the other identical module. To ensure correct sampling at 2.25GHz ($CK_{2.25}$), $D5$ and $D7$ are phase-shifted by a half-period at 1.125GHz by re-sampling with the CKB clock. Similarly, for correct sampling at 4.5GHz, the data path for $D3$ and $D7$ is delayed by a half clock period at 2.25GHz by re-sampling with the $CK_{2.25B}$ clock. Four data paths at 1.125GHz are switched by 1.125GHz differential clocks (CK and CKB), and each data path is available for a half-period of the 1.125GHz clock (i.e. same period as one clock cycle of the 2.25GHz clock) for the flip-flops which re-sample the 1.125GHz data with 2.25GHz clocks. The 2.25GHz data is then sampled by a 4.5GHz clock ($CK_{4.5}$) in the same way with switches operating at 2.25GHz under control of differential clocks, $CK_{2.25}$ and $CK_{2.25B}$.

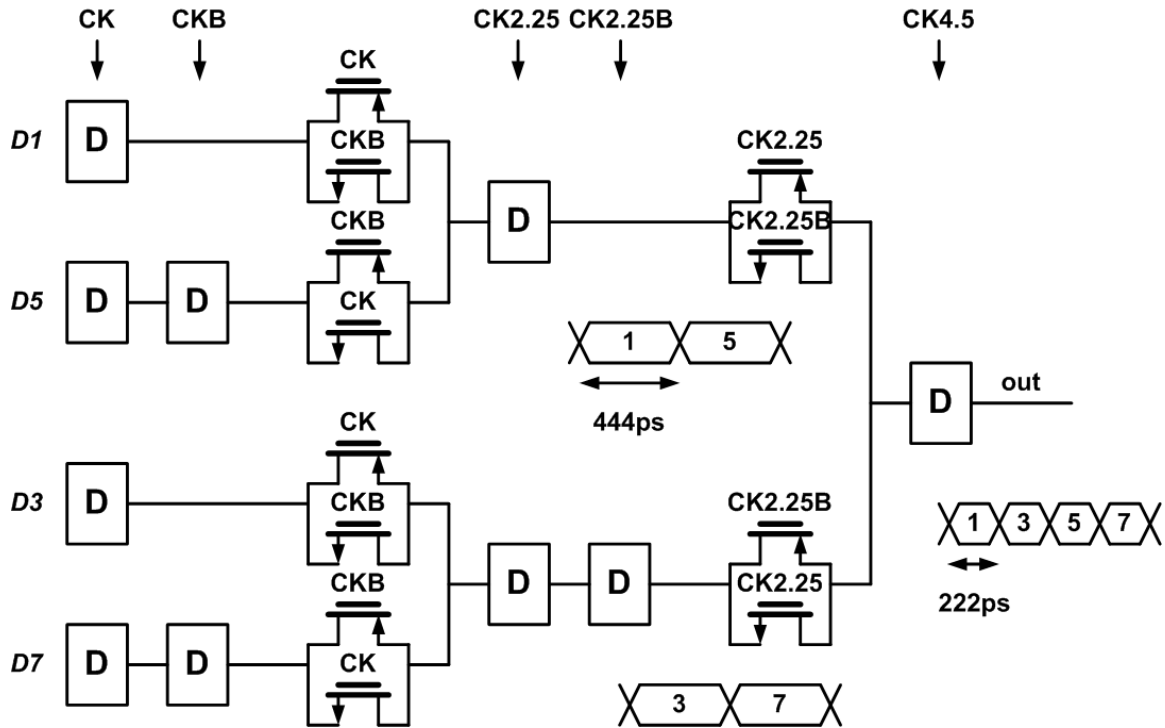


Figure 5.5: A 4-bit serializer[42]; serialization is accomplished by sampling original data at low frequency with high frequency clock signals

5.2.3 Line driver

The final 9Gbps serialization from two 1-bit 4.5Gbps serialized data streams is performed at the driver[43] with the help of two differential 4.5GHz clock phases, $CK4.5$ and $CK4.5B$. Two 1-bit data patterns drive $D1$ and $D2$, and only one half of the driver is active during each half-cycle of a 4.5GHz clock, facilitating 9Gbps serialization at OUT .

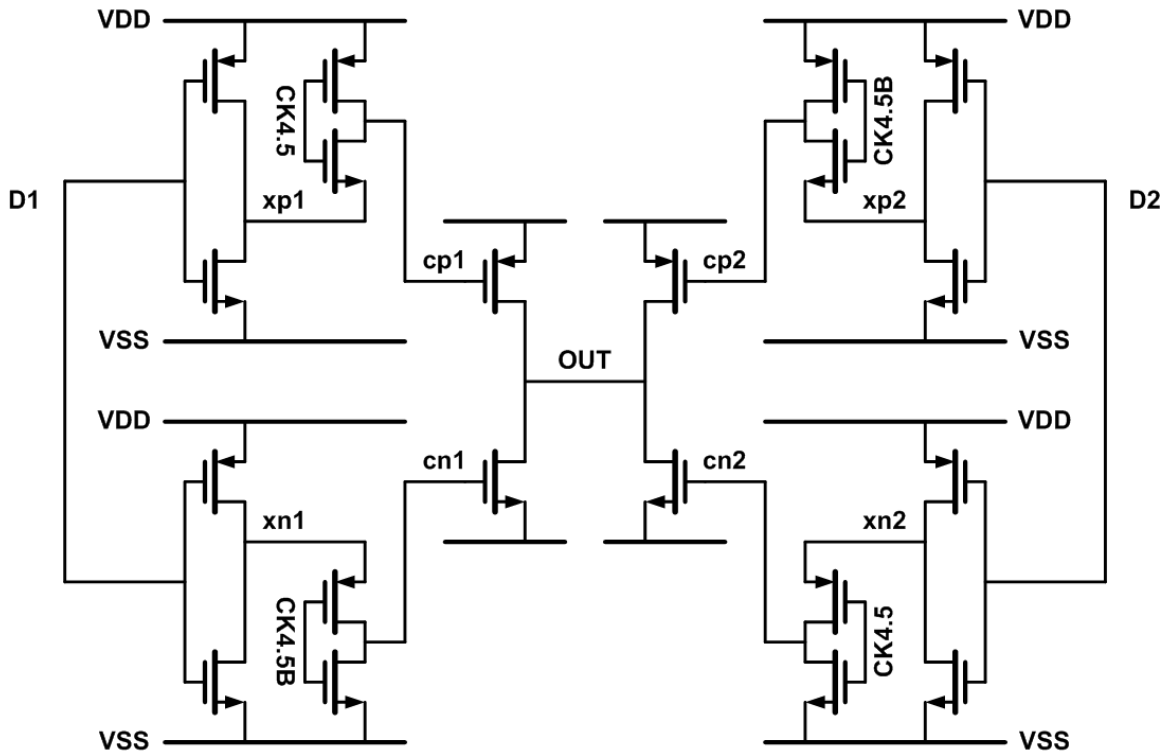


Figure 5.6: Line driver[43]; two identical circuits only one of which is active at a time during half period of 4.5GHz clock signal generates 9Gbps serialized data.

A pulsed signaling driver (Figure 5.6) eliminates DC power dissipation. The line driver is composed of two identical circuits and the outputs of both circuits are connected in-parallel to drive the transmission line. Four pre-drivers drive the four FETs in the two halves of the driver. Only half of each driver is active during each half of the 4.5GHz clock period. Data arrives at the pre-drivers ahead of the clock signals and presets the voltages at internal nodes ($xp1$, $xn1$, $xp2$, and $xn2$). If $D1$ is 0, both $xn1$ and $xp1$ become 1. On the other hand, if the $D1$ is 1, both $xn1$ and $xp1$ become 0. The differential clocks, $CK4.5$ and $CK4.5B$, arrive at the line driver, right after the input data presets the voltages at the internal nodes, and then generates short pulses at nodes, $cp1$ or $cn1$, based on the preset data at nodes $xp1$ and $xn1$. At most only one $cp1$ and $cn1$ activates, either the NMOS or PMOS driver device at any time. Assuming the clock signals maintain a 50

percent duty cycle, the left half-circuit generates the output signal during $CK4.5$ high while the right half-circuit generates the output signal during $CK4.5B$ high. As an example in Figure 5.7, if $D1$ is 1 during the high of $CK4.5$, which sets 0 at both $xp1$ and $xn1$, then only the $cp1$ node changes its value from 1 to 0. cp changes back to 1 at the falling edge of $CK4.5$ and the $cn1$ node still stays at 0.

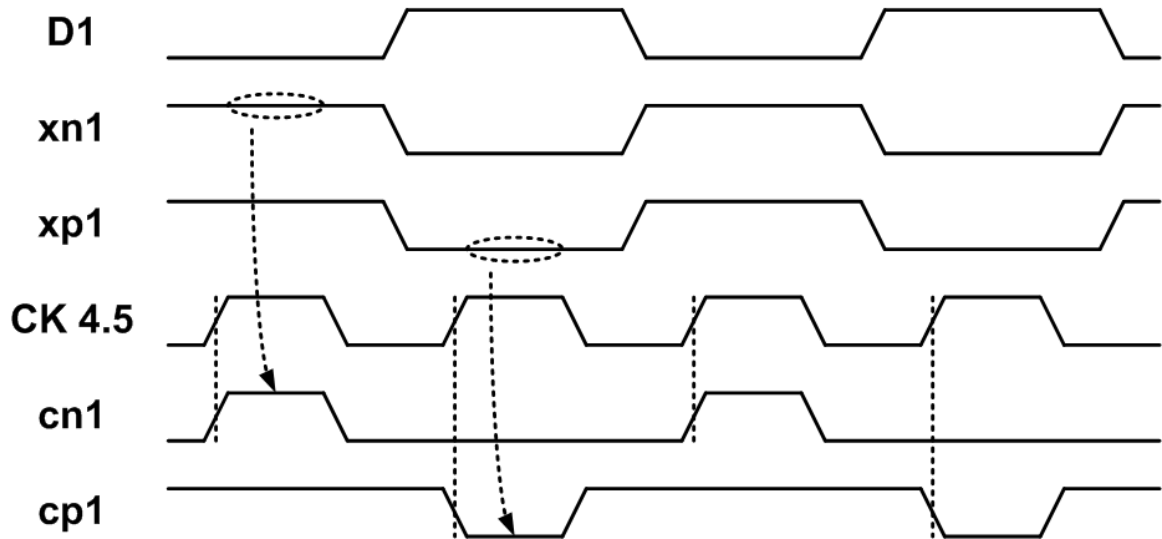


Figure 5.7: Example waveforms for the line driver; input data $D1$, sets up voltages at internal nodes, $xn1$ and $xp1$, and clock signal, $CK4.5$, makes short pulses on $cn1$ and $cp1$ nodes based on the voltage at $xn1$ and $xp1$.

5.3. RX (receiver)

The receiver samples the received signal with interleaved samplers operating at 4.5GHz (the same frequency as the transmitter). The sampled data is de-serialized and then sampled down to 1.125GHz. Due to the delay over the long transmission-line, the phase of the clock signals is tuned for proper data recovery. With appropriate phase control, we can employ only two comparators sampling at 4.5GHz. The comparator clock phases are adjusted to sample the input data at the center of data eye.

The RC-CR filter and phase interpolator blocks in Figure 5.8 allow control of the sampling phase. The outputs of the LC oscillator, *inp* and *inn*, are the inputs to the RC-CR filter, which generates four equally-spaced signals. The phase interpolator takes these four signals and generates another four output signals whose phases are digitally controlled. Since two comparators are used for the data sampling, only two complementary outputs, *rxCK4.5* and *rxCK4.5B*, from the phase interpolator block are used as the clock signals for the comparators. The phase-shift-block aligns the phases of the comparator outputs before de-serialization at the FIFO. Sampling with lower speed clocks de-serializes the high-frequency data down to 2.25GHz and finally to 1.125GHz.

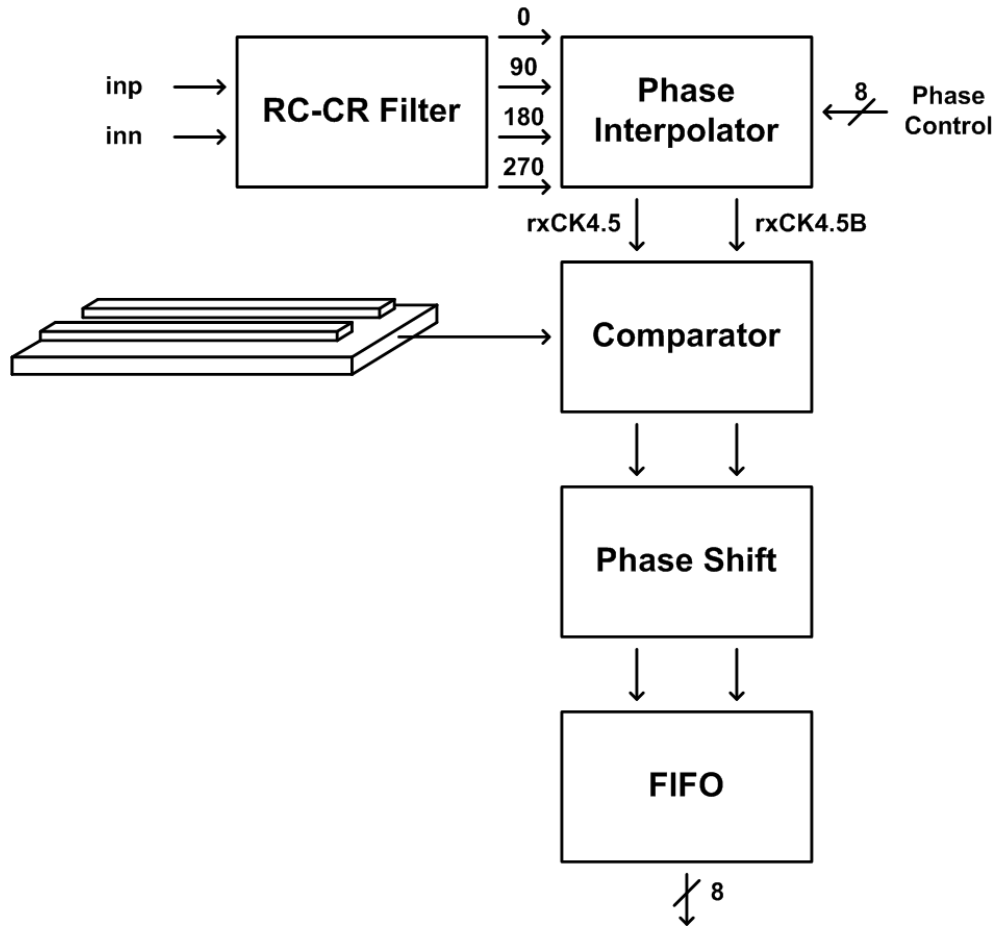


Figure 5.8: Block diagram of the RX; receiver samples the serialized data, 9Gbps, and de-serializes down to 8bit 1.125GHz. It requires clock phase tuning to compensate the delay from the long transmission line.

5.3.1 RC-CR Filter

The differential signals from the LC oscillator, *inp* and *inn*, differ in phase by 180 degrees. In Figure 5.9, a pair of RC-CR filters, one for for each of *inp* and *inn*, generates two differential signals which differ in phase by 90-degrees. The four phases from the two RC-CR filters are separated in phase by 90-degrees. The value of R and C is decided by the operating frequency, and it is recommended that C be at least five times larger than the load capacitance[28]. Even though two signals from a RC-CR filter have a 90-degree phase difference at all frequencies, the magnitude of those two signals is only the

same at $1/(RC)^{1/2}$. Therefore, gain stages follow the RC-CR filters to compensate for amplitude mismatches.

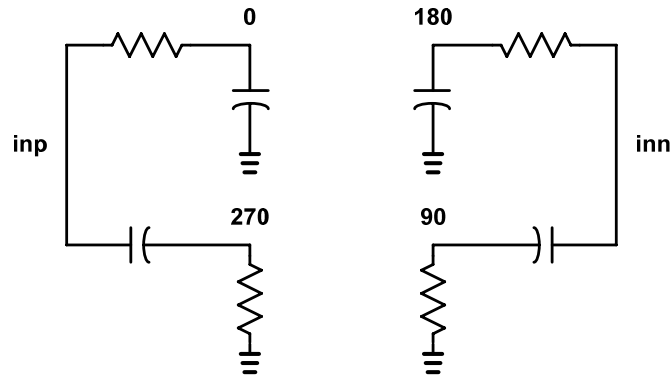


Figure 5.9: A RC-CR filter[28]; four phases, 0 , 90 , 180 , and 270 , are generated from the original two phases, inp and inn .

5.3.2 Interpolator

Although the clock frequency of the RX is same as that of the TX, due to the time delay of the long transmission line and time differences in clock distribution, the RX clock is phase-tuned in order to correctly sample the received signal. The phase of the output signals of the interpolator shown in Figure 5.10 is changed by controlling the bias currents. Two sets of differential clock signals (or four phases) with a phase difference of 90-degrees, i.e. 56ps at 4.5GHz, drive the inputs. Since there are eight differential control-switches, turning one switch *on* or *off* causes approximately 7ps of advancement or delay, respectively. The gain of the interpolator suppresses amplitude mismatch of the signals from the RC-CR filters.

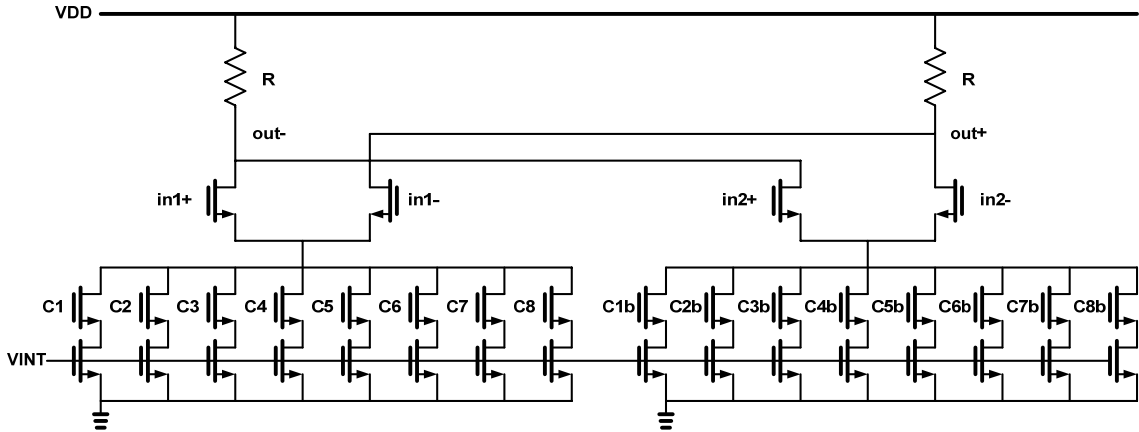


Figure 5.10: Interpolator; the output phases, $out+$ and $out-$, from the two input differential pairs can be modulated by changing the amount of the current in each side.

5.3.3 Comparator

One of the challenges in the design of a serial link is correct data-recovery at the receiver. Usually comparators are used at the first stage of the receiver to sample the received signal and convert a small input signal to CMOS voltage levels.

Most high-speed comparators consist of a preamplifier followed by a regenerative latching stage, with each stage driven by complementary clock signals. While on, the preamplifier operates as a differential amplifier. The latching stage, in turn, amplifies the signal, producing exponential gain over time:

$$V(t) = V_{initial} e^{t/\tau_{regen}} \quad (5.1)$$

where $V_{initial}$ is the voltage difference of the two outputs of the preamplifier (when the latching stage turns on), and τ_{regen} is the regenerative time constant. For a regenerative stage with cross coupled inverters, the time constant τ_{regen} is a function of the parasitic capacitance, C , and the trans-conductance of cross-coupled transistors, g_m

$$\tau_{regen} = \frac{C}{g_m} \quad (5.2)$$

Since the unity gain frequency, f_T , which is equivalent to g_m/C , depends on process technology, it is difficult to achieve improvement of the regenerative time constant for a given latch structure.

If the output voltage level of the latching stage does not reach a voltage corresponding to a digital 1 or 0, then the digital circuits cannot correctly process the comparator output. When the output voltage fails to reach robust digital voltage levels, the comparator output is said to be metastable. The voltage signal level at the long end of the lossy transmission line (from the transmitter) can be as small as 200mV, due to the voltage drop along the transmission line. Since the data rate is fast (9Gbps), the comparator is formed with a cascade of two pairs of preamps and latching stages in order to have sufficient gain to avoid a metastability.

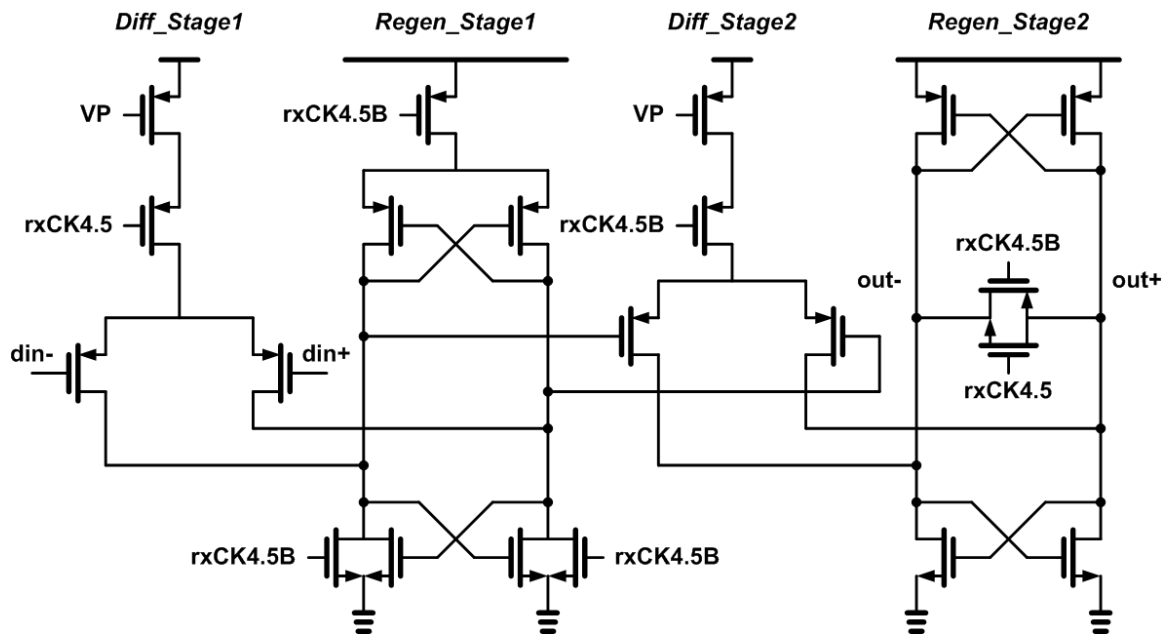


Figure 5.11: Comparator; it samples the difference of input signals, *din+* and *din-*, and regenerates the small voltage difference to the CMOS voltage level.

Figure 5.11 shows a schematic of the comparator. The input signal is sampled by the two comparators each operating at 4.5GS/s and the sampling instants are shifted in phase by 180-degrees. Each comparator has two differential stages (i.e. *Diff_Stage1* and *Diff_Stage2*) and two regeneration stages (i.e. *Regen_Stage1* and *Regen_Stage2*). The first differential stage is operated while the clock, *rxCK4.5*, is low and the second differential stage operates while the clock, *rxCK4.5*, is high (i.e. *rxCK4.5B* is low). When the clock (*rxCK4.5*) is low, the first regeneration stage is reset by turning off the tail current source, and when the clock (*rxCK4.5*) is high, the second regeneration stage is reset by shorting the two differential outputs. At the rising edge of the clock, the outputs of the first differential stage are sampled by the first regeneration stage. The voltage difference of those two outputs continues to grow, with the help of cross connected NMOS and PMOS transistors, until the falling edge of the clock signal. During the time between the falling edge and the next rising edge of the clock signal, the second regeneration stage helps to increase the voltage difference to a voltage level large enough to be compatible with CMOS digital levels.

5.3.4 Comparator output phase alignment

Since the two data-bits generated by the two comparators are aligned to different phases (i.e. with a 180 phase difference), they need to be synchronized to a one clock phase for subsequent digital processing. Since the period of the 4.5GHz clock is close to the clock-to-Q delay of static flip-flops in 0.13 μ m CMOS, it is not easy to meet timing requirements, such as rise and hold time. Therefore, unlike phase-shifting at low frequencies (such as 2.25GHz and 1.125GHz) gradual phase adjustment is required. In this way, it takes four steps to synchronize to a single clock phase at 4.5GHz, as shown in

Figure 5.12, and approximately 45-degree of phase change is achieved at each step. The first column of D flip-flops samples the outputs of the comparators, and then the sampled data is phase shifted through the following three columns.

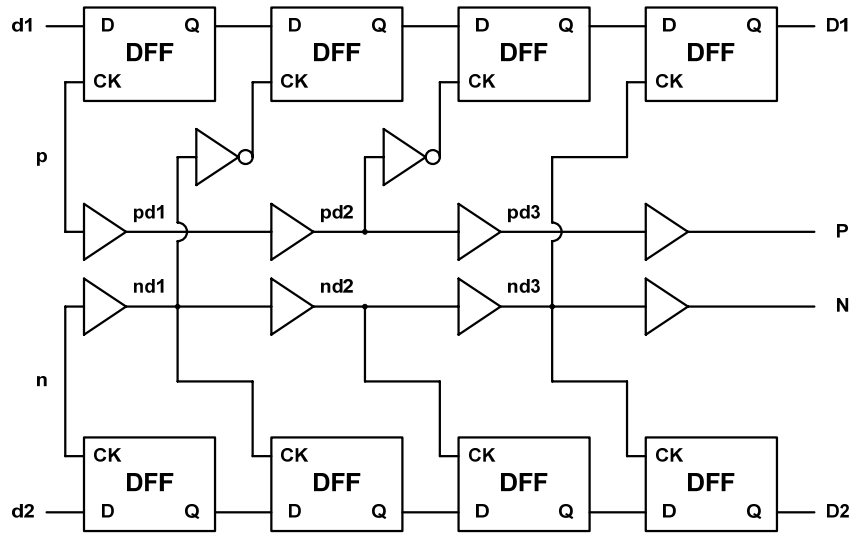


Figure 5.12: Comparator output phase alignment at 4.5GHz; since the outputs of the comparators, $d1$ and $d2$, are out of phase, they need to be aligned to single clock phase ($D1$ and $D2$) for the further digital processing.

5.3.5 FIFO

The FIFO (shown in Figure 5.13) follows the phase shifter and parallelizes the sampled data at 4.5GHz, first, to 2.25GHz, then finally to 1.125GHz. Two data streams at 4.5GHz, $d1$ and $d2$, are sampled by differential 2.25GHz clocks, CK2.25 and CK2.25B, so there is phase difference between the outputs of flip-flops D1 and D2 and the outputs of flip-flops D3 and D4 at 2.25GHz. The out-of-phase 2.25GHz data is synchronized to a single clock phase at the outputs of flip-flops D5~D8, before being re-sampled by the differential 1.125GHz clocks. The 1.125GHz data is in two phase domains (D9~D16) and again needs to be resynchronized (at flip-flops D17~D24) for further digital processing.

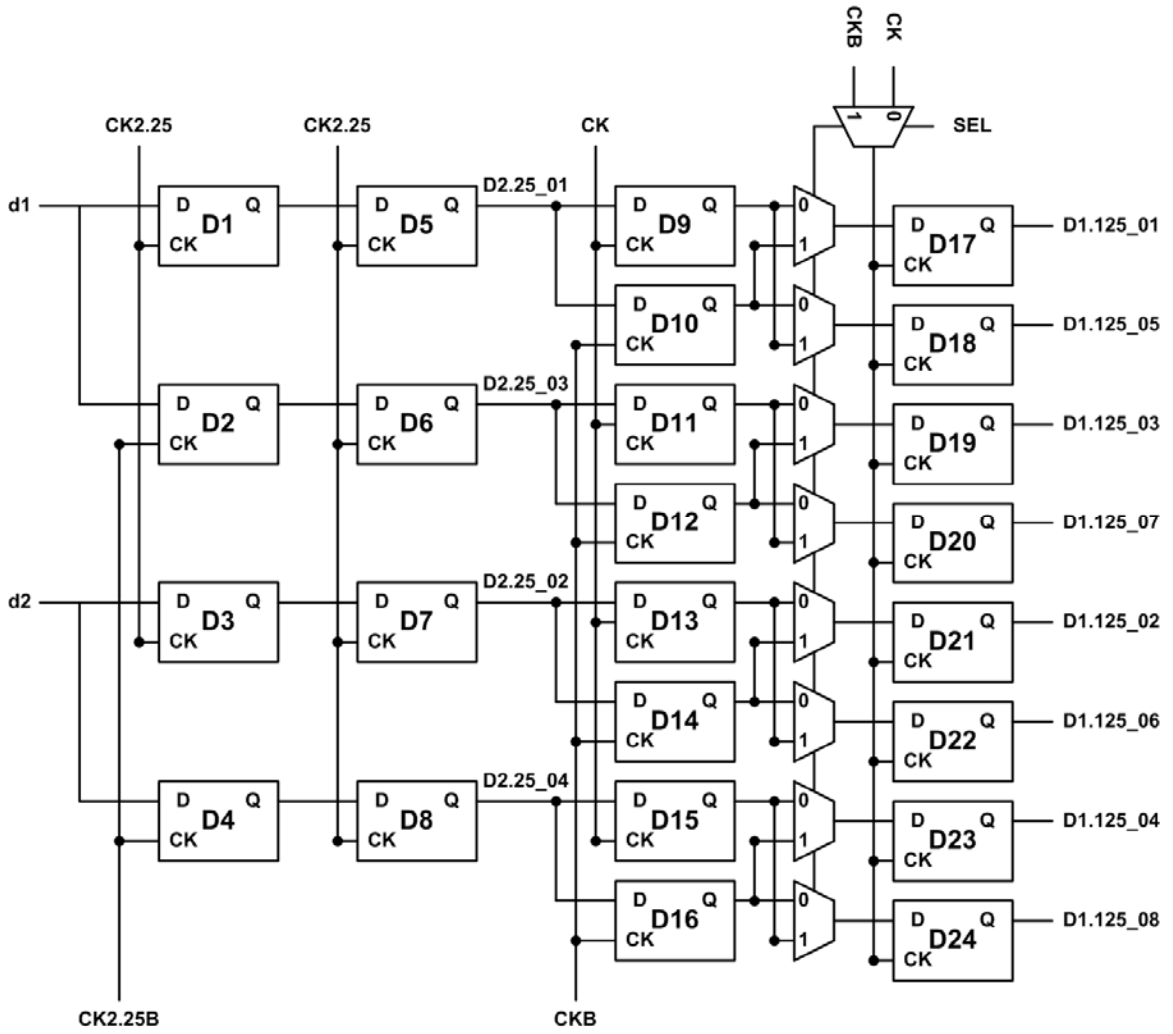


Figure 5.13: FIFO; sampling data at high frequency with clock signals at low frequency allows de-serialization from 2bit 4.5GHz to 4bit 2.25GHz and then to 8bit 1.125GHz.

5.4. Error-check

An error-check block compares data patterns from the transmitter and from the receiver, and generates an error signal when there is a mismatch. The error counter receives and compares two 8-bit data words every 1.125GHz clock cycle. As shown in Figure 5.14, the original 8-bit data sent to the transmitter is stored in registers in the *Fixed Delay* and *Variable Delay* blocks until the serialized data is sampled and recovered at the receiver, and sent to the *CHECK* block. In order to decide whether the recovered data is same as the original data sent by the transmitter, the data from the RX is transferred to the clock domain of the transmitter. The clock synchronization block performs clock domain alignment, and a *WINDOW SELECT* block stores recovered data for two 1.125GHz clock cycles and selects an 8-bit window from the 16 stored data-bits for comparison. The error counter receives and compares two 8-bit data words every clock cycle.

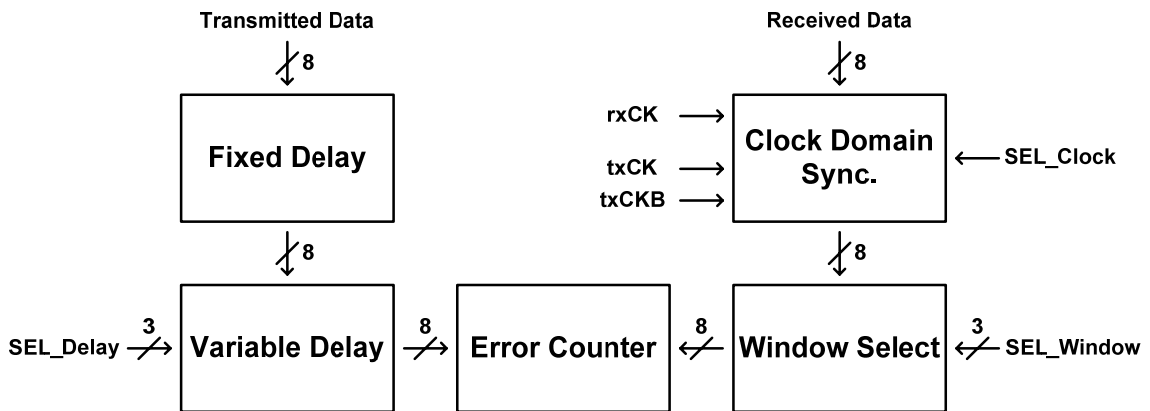


Figure 5.14: Block diagram of the error-check block; error-check block compares two data patterns, transmitted data and received data, and counts the number of errors when there is a discrepancy.

5.4.1 Clock domain synchronization

The clock phases in the receiver are not aligned with the clocks in the transmitter. In order to compare the recovered data with the original data, both data patterns should be in the same clock domain. Figure 5.15 shows a block diagram of the clock domain synchronization scheme[43]. This block aligns the data recovered by the receiver to the data in the transmitter clock domain. In principle, a clock domain change can be achieved by re-sampling the data with the clock signal to which the input data should be synchronized, however care must be taken to ensure sufficient setup-and-hold time. The input data, *DATA_IN*, is sampled by two flip-flops, with complimentary enables signals, at half of the *rxCK* clock frequency. Therefore, the re-sampled data, *DATA0* and *DATA1*, is available for two clock cycles of the *rxCK* clock, enabling correct re-sampling with the transmitter clock. The transmitter clock, *txCK*, is at the same frequency as the receiver clock, *rxCK*, though the phases of these two clock signals are different and unknown. Even though the increased data-bit periods makes re-sampling with transmitter clock much easier, there is still a possibility that the data does not satisfy the setup-and-hold-time for the sampling flip-flops working with clocks from TX. Therefore, synchronization is designed so that both differential clock signals from the TX are available. Even though the *txCKB* clock signal is used for synchronization, the data sampled with *txCKB* is re-sampled to the *txCK* clock domain.

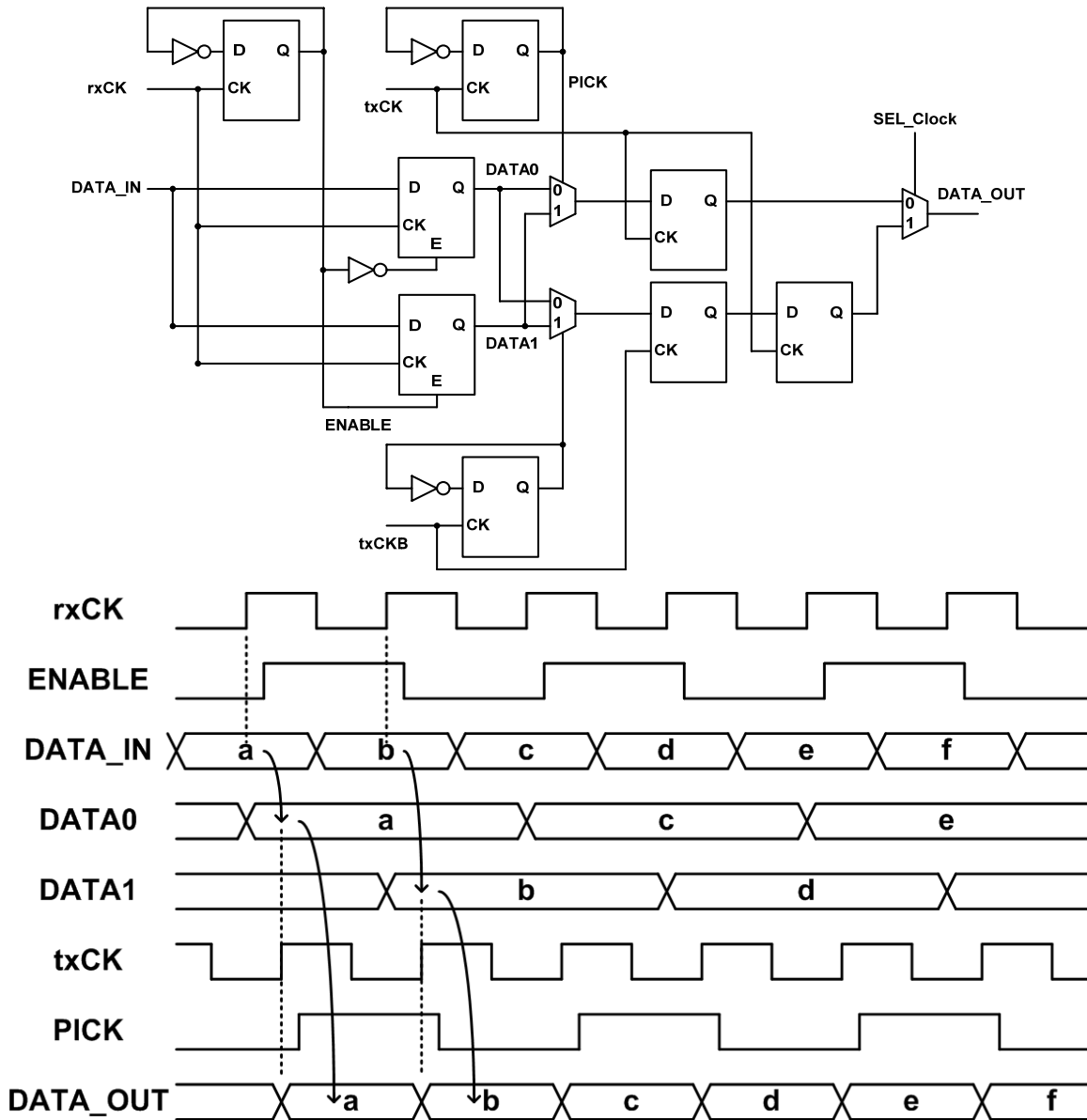


Figure 5.15: Clock domain synchronization[43]; since the recovered data are at the clock domain of the receiver, they need to change their clock domain to that of the transmitter in order to be compared with the original data at the transmitter.

5.4.2 Window selection

Although the recovered data is phase shifted to match the clock domain of the transmit data, for long transmission lines the delay may be comparable to one more or more bit periods, requiring additional alignment. A *WINDOW SELECT* block, shown in

Figure 5.16, performs this function. This block stores 8-bit synchronized data for two clock cycles. By changing the *SEL Window* signal, any 8-bit sequence can be selected from the stored 16-bit word. The selected 8-bit word is compared with the original data by the error-check block.

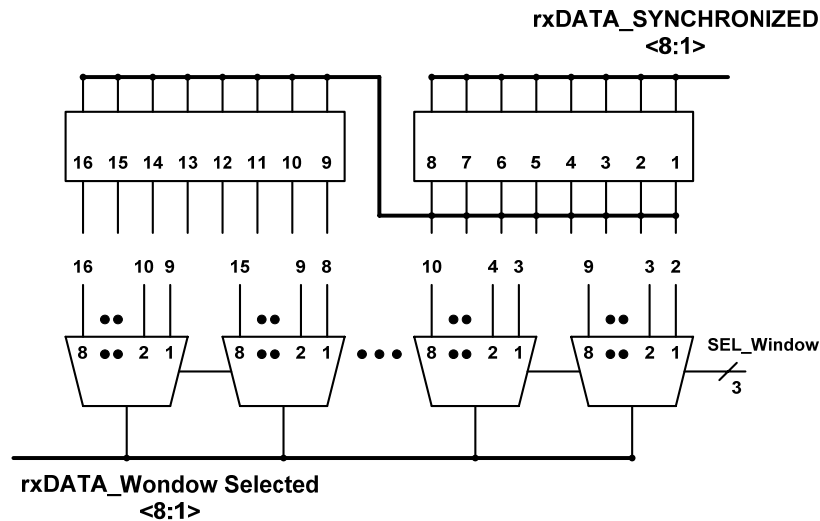


Figure 5.16: Data window selection; it stores 8 bit recovered data for two clock cycles and allows 16 bit data for the final 8 bit data selection.

5.4.3 Error counter

Every clock cycle, the error counter shown in Figure 5.17 compares two the 8-bit input data patterns and increments the error count when a mismatch is found. By performing a bit-wise XOR of the two 8-bit data words and ORing the result, an *ENABLE* signal is generated whenever a mismatch is found. While the enable signal is high, the counter is increased by one for each clock cycle. Since the counter is an 8-bit counter, the maximum number it can count to is 11111111 (=255). By resetting to 00000000 after the maximum value is reached, the counter can continue to monitor the transmission errors.

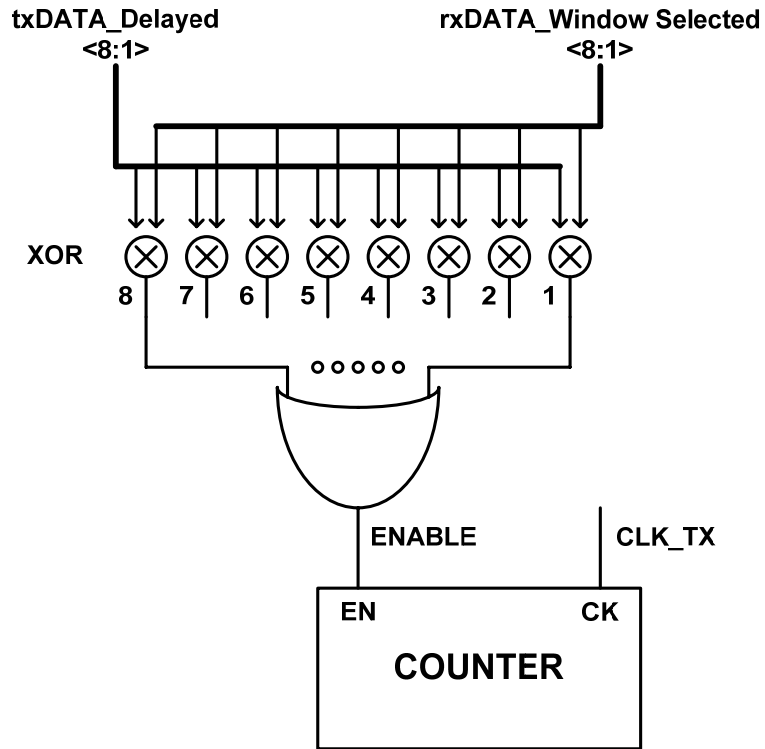


Figure 5.17: Error counter; It receives two data patterns, original data and recovered data, and XORing those two patterns and then ORing the outputs of XORs becomes ENABLE signal. It becomes high and allows counting the number of errors at every clock cycle when there is a discrepancy between two input patterns.

5.5. Measurements of Prototype

The prototype is fabricated in a $0.13\mu\text{m}$ 8M CMOS process, and measures $1.7\text{mm} \times 2.1\text{mm}$ including pads. The transmitter and receiver occupy $0.5\text{mm} \times 0.3\text{mm}$ and $1.4\text{mm} \times 0.4\text{mm}$ respectively. The chip micrograph is shown in Figure 5.18. The 5.8mm transmission line is routed from the transmitter to the receiver outside of the pads. The shielded coplanar transmission line is formed with two $6\mu\text{m}$ wide metal-5(MG) wires separated by $3\mu\text{m}$, over a $21\mu\text{m}$ wide metal-2 ground plane. The simulated characteristic impedance is 30.6Ω and the line is terminated at the receiver with a 30.6Ω poly-silicon resistor.

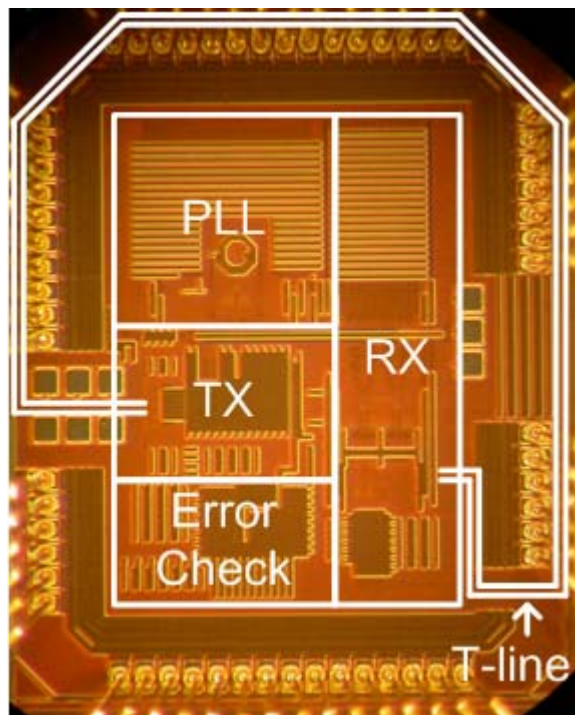


Figure 5.18: Chip micrograph; transmission lines are laid out outside of the bonding pads.

Measured data are shown in Figure 5.19 and Figure 5.20. Figure 5.19 shows the pre-defined serialized patterns, 10101010, 11001100, 11110000, and 01001110,¹ at the output of the drivers, along with the 4.5GHz PLL clock, all of which are measured directly using a GSG probe on a probe station.

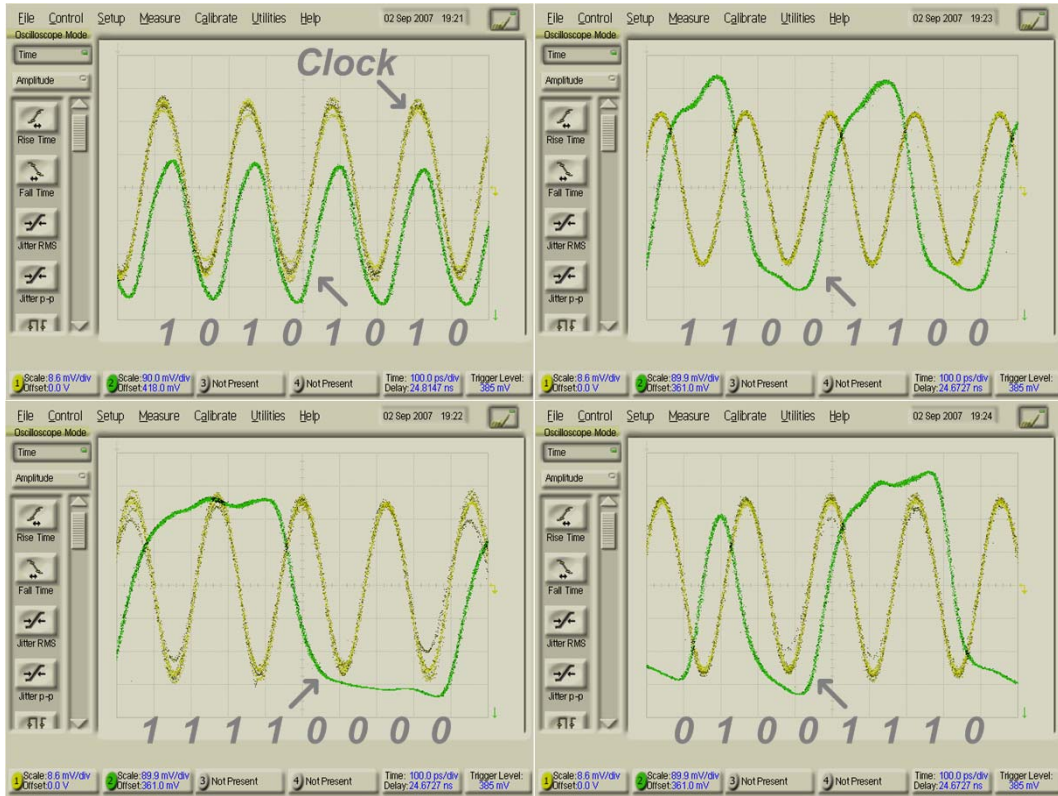


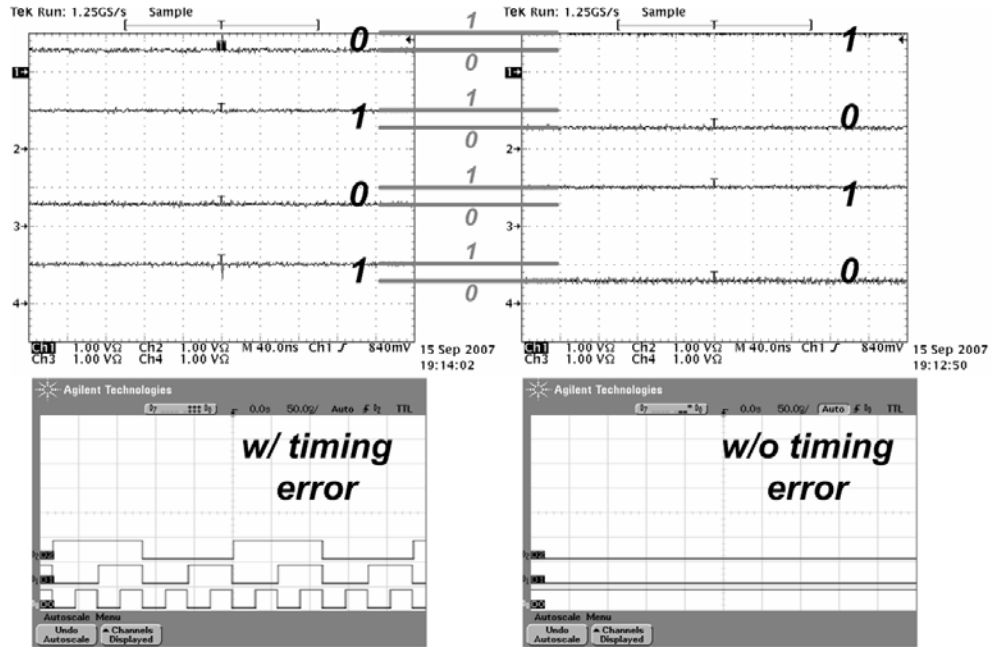
Figure 5.19: Measured clock and serialized data at the output of the driver for the 10101010, 11001100, 11110000, 01001110 patterns

The received de-serialized data are monitored by the on-chip error checking logic and the error count output is recorded with a mixed-signal oscilloscope. When a deliberate mismatch is introduced between transmitted and recovered data through a deliberate timing error, the error counter accumulates as shown on the left side of Figure 5.20. When the receiver correctly recovers data, the error counter stops increasing as shown on the right side of Figure 5.20. The first four bits of the recovered data and three

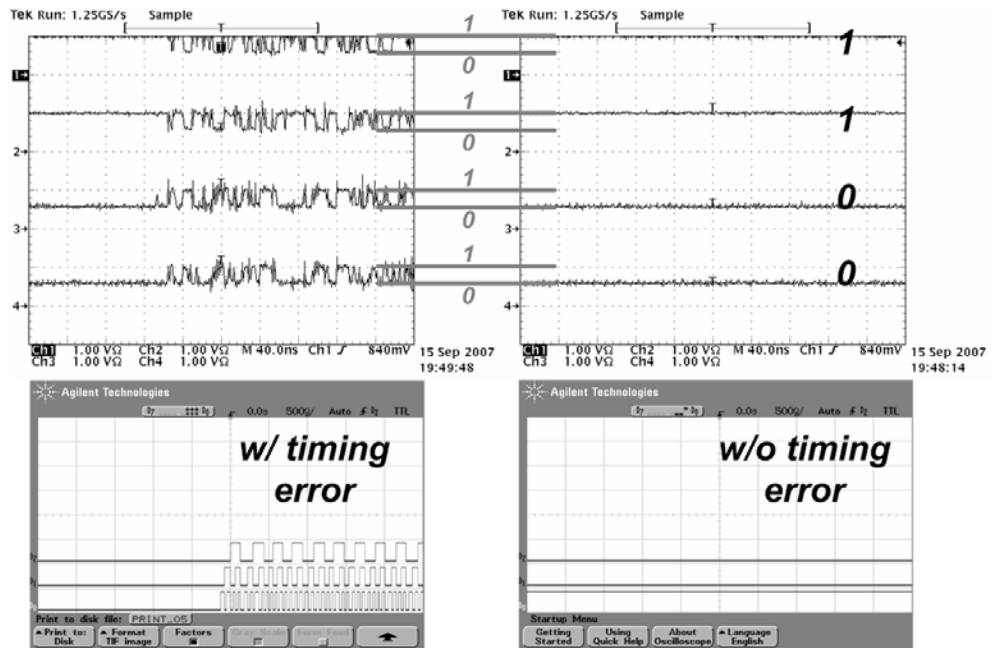
¹ A PRBS generator was also implemented on-chip for the self test. However because of a design flaw the outputs of the PRBS generator are stuck low. One of the 8 bit original data can be observed directly off the chip verifying this problem.

MSBs of the error counter for the 10101010, 11001100, 11110000, 01001110 patterns are shown in Figure 5.20 (a), (b), (c), and (d) respectively. The measured BER is less than 10^{-12} with 10101010, 11001100, and 11110000 patterns, and is less than 10^{-10} with a 01001110 pattern.

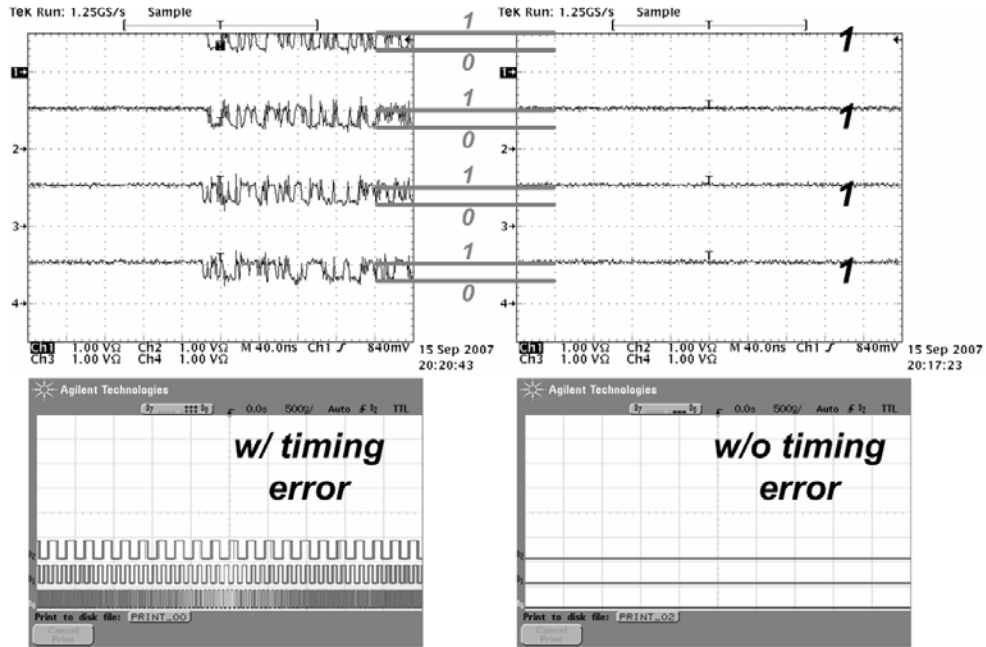
The prototype operates with a 1.5V supply and the total power-supply currents for the analog circuits (i.e. charge pump and LC oscillator in the PLL, comparator, phase interpolator), transmitter, receiver, and error checking logic are 70mA, 280mA, 120mA, and 160mA, respectively.



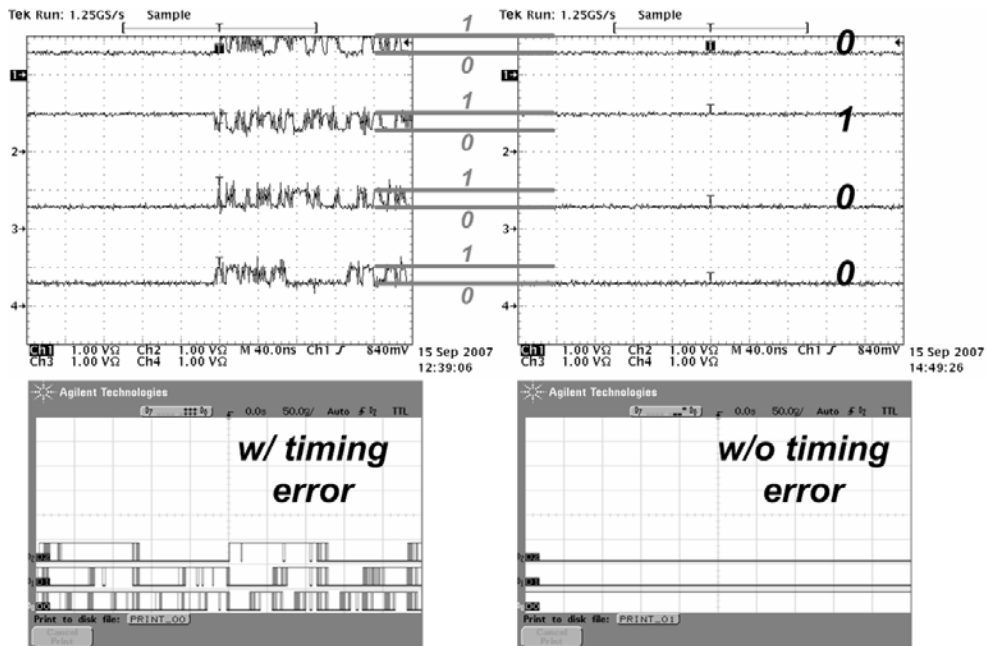
(a)



(b)



(c)



(d)

Figure 5.20: Output of the self checking logic with (left) and without (right) deliberate timing error for the (a) 10101010, (b) 11001100, (c) 11110000, and (d) 01001110 patterns; when there are mismatches between the original data and the recovered data, error counter increases the number of errors at every clock cycles, but when those two data patterns are perfectly matched, the output of the error counter stays at the same value.

Figure 5.21 shows the test setup to measure the serialized data and the recovered data. Since the frequency of the main PLL is high at 4.5GHz, a Cascade ACP40 GSG probe is used for direct measurement. Another GSG probe is used at the same time to record serialized data at the output of the transmitter. A Tektronix TDS 694C digital real-time oscilloscope is used for the measurement of the recovered data, and three MSB outputs of eight bit error counter bits are monitored with the Agilent 54641D mixed signal oscilloscope (The 8 bit the recovered data words are static when there is no timing error).

Printed circuit boards on the probe station and the photo of the measured clock signal and its spectrum are shown in Figure 5.22 and Figure 5.23 respectively. The device was packaged in a low-cost ceramic LCC package, soldered to a custom designed four-layer FR4 PCB. The Cascade probes are only used to monitor high frequency transmission line and clock nodes. A signaling, biasing and supplies are fed though the LCC package.

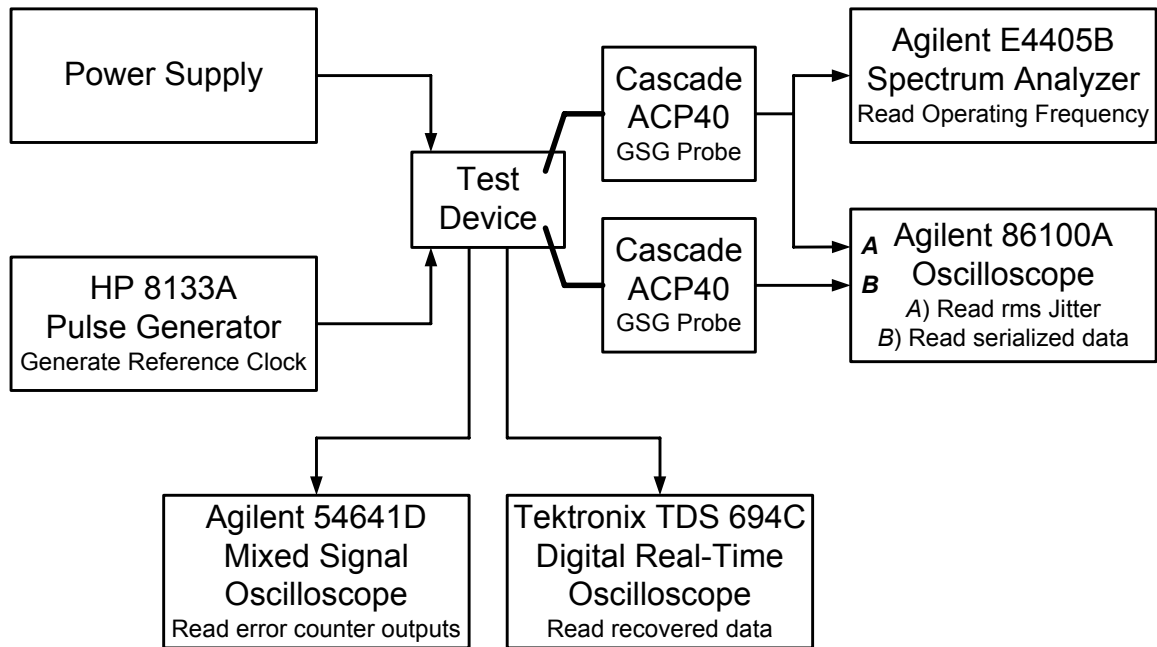


Figure 5.21: Measurement setup; Cascade GSG probes are used to measure the operating frequency, RMS jitter, and the serialized data.

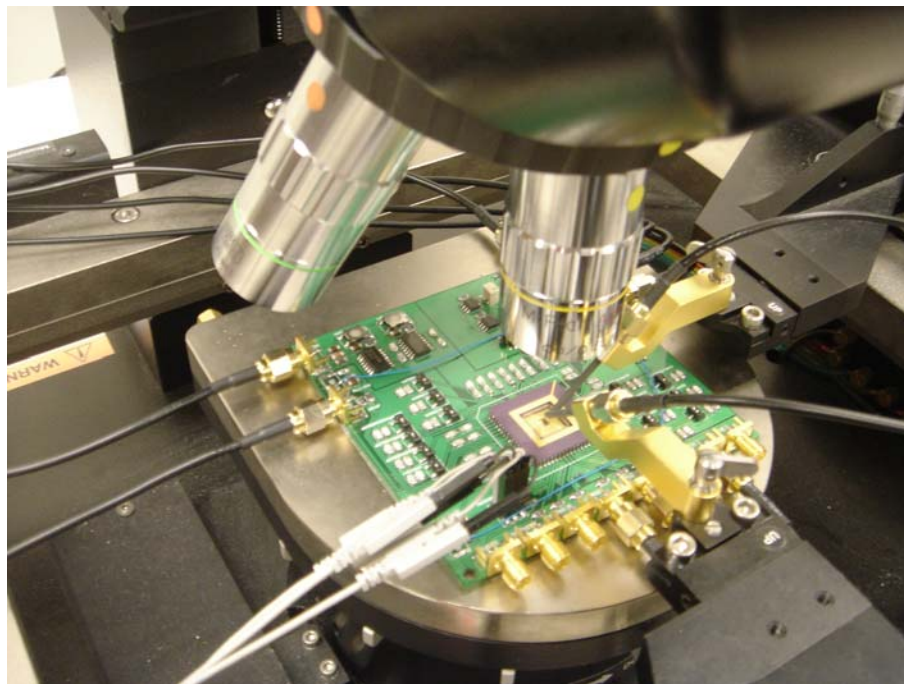


Figure 5.22: Printed circuit board on the probe station.

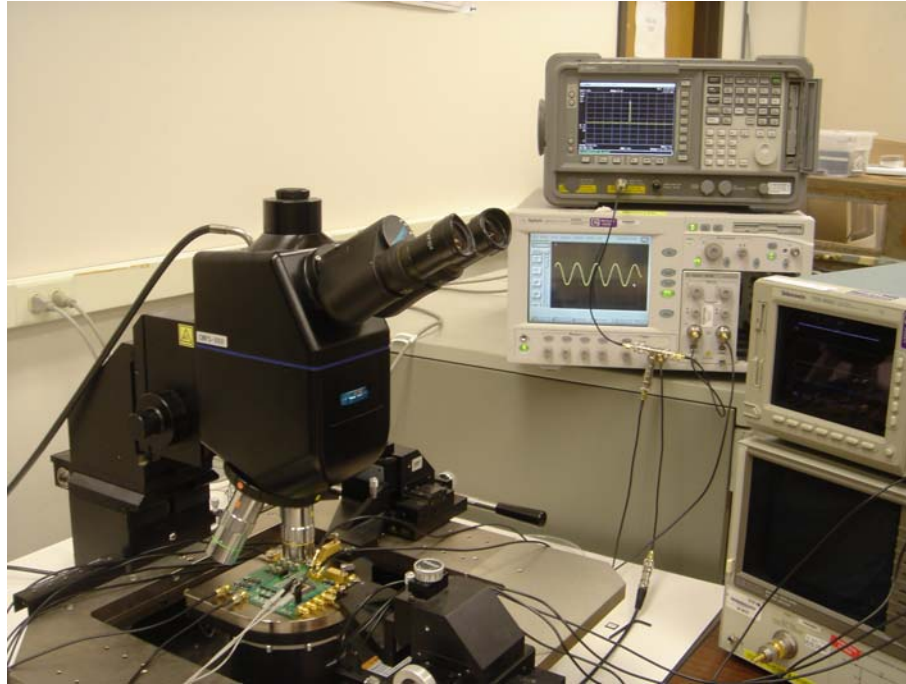


Figure 5.23: Test setup to measure the clock signal and its frequency.

5.6. 20Gbps On-chip Serial Signaling

The circuit design techniques in previous sections can be extended to the design of 20Gbps on-chip serial link in the same technology, 0.13 μ m CMOS. Since operating frequency, and in particular that of the serializer circuitry, is highly constrained by the technology, it is challenging if not impossible to make those circuits work beyond 5 or 6GHz in 130nm CMOS. Therefore, serialization to 20Gbps is best accomplished at the same operating frequency as the circuitry in previous sections but with more interleaving and more clock phases. Multiple phases can be generated using the multi-stage oscillators, with capacitive coupling, providing low phase spacing error and low phase noise, described in detail in chapter III and IV,. Since 20Gbps is equivalent to 16 bit wide parallel data at 1.25GHz, the complexity of the digital circuits is also doubled. This section outlines circuitry for 20Gbps on-chip serial data transmission, and presents simulations of link circuitry operation.

Figure 5.24 shows the block diagram of the TX. In order to transmit 20Gbps serial data with 5GHz clocks, four clock phase are used for the transmitter, and the phase difference between adjacent clocks is 50ps at 5GHz. Only one of the four transmitters is active at any time, during each quarter of the clock period. In order to serialize the data properly, the original test data generated should be equally distributed to all four modules with the proper data sequence. The retiming block distributes the data from the PRBS to the four identical modules in sequence. For proper sampling with 2.5GHz clocks, D9 and D13 in module1 are phase shifted by half a clock cycle at 1.25GHz, and similarly for proper sampling at 5GHz the data path for the 5th and 13th data signals is delayed by half

a clock period at 2.5GHz. Each module has four data streams serialized at 5GHz but at the same phase, therefore in order to serialize four 5GHz data streams to 20GHz, each of the four 5GHz data streams is phase shifted appropriately.

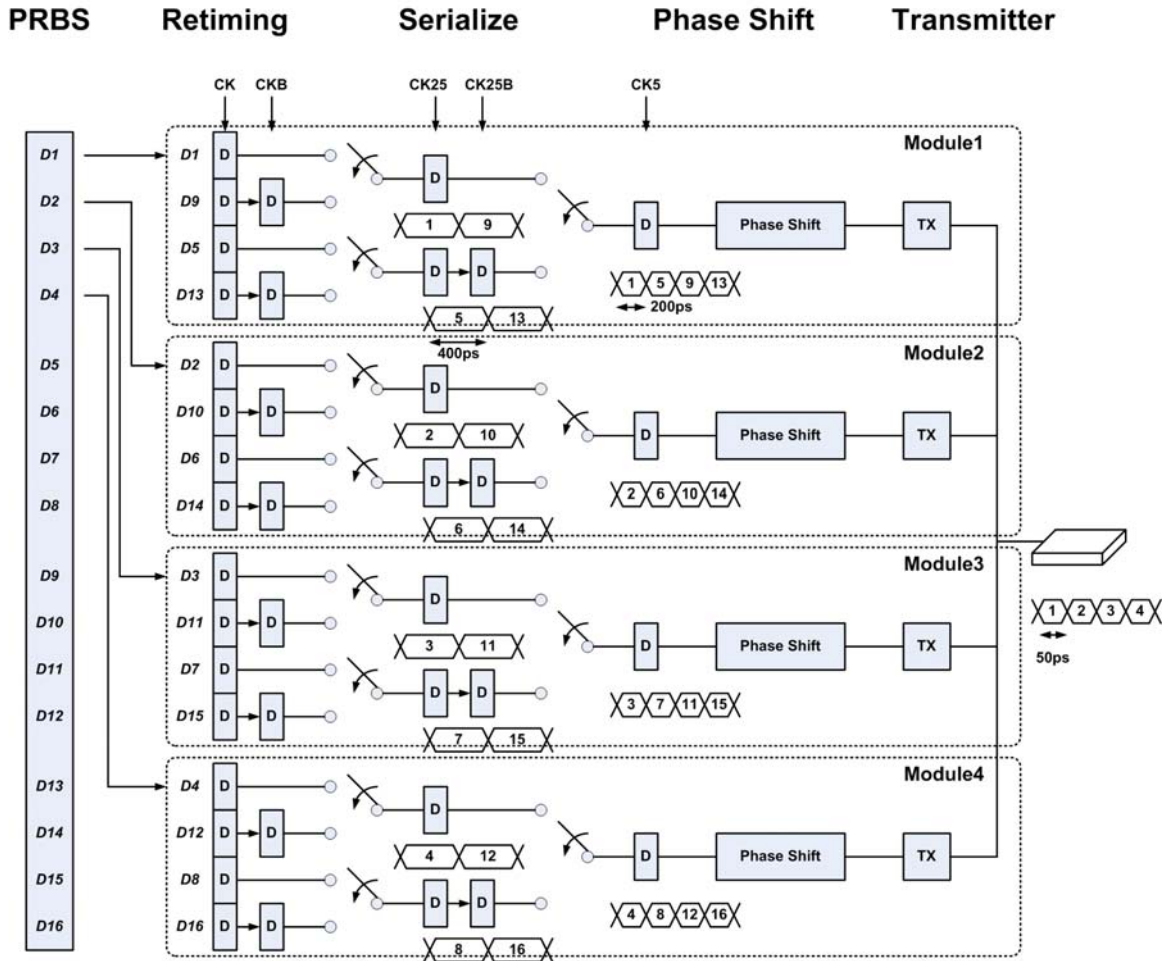


Figure 5.24: System diagram of the transmitter(TX); TX consists of four identical functional blocks. Each block receives original data from the PRBS and does retiming for the proper sampling, serialization to the high frequencies, and phase shifting to guarantee timing requirement for the following data driver.

Figure 5.25 shows the driver to generate 20Gbps serialized output signal. The driver is composed of four identical circuits, and the outputs of each circuit are connected together to drive the transmission line. Only one output of the four circuits is active at any time during each quarter of the clock period, and the combination of the four

independent outputs results in continuous output signal. Unlike the driver used to generate 9Gbps serialized data in chapter V, the driver in Figure 5.25 employs four clock phases and their complements. Data arrives at the transmitter before the clock signals, and sets the voltages at the drain of MN3 and MN2. If the input data is 0, the drain of MP2 becomes VDD and if the input data is 1, the drain of MN3 becomes GND. Out of eight clocks (i.e. in the order of phases CLK1, CLK2, CLK3, CLK4, CLK1B, CLK2B, CLK3B, and CLK4B) four clocks such as CLK1, CLK3, CLK1B, and CLK3B are used for the whole transmitter, and the phase space and the overlap between any consecutive clocks are one fourth of the clock period (assuming the clock signals maintain 50 percent duty cycle). For module 1, CLK1 and CLK1B arrive one fourth of a clock period before CLK3 and CLK3B and set voltages at nodes V1 and V2 to GND and VDD respectively. The subsequent clocks, such as CLK3 and CLK3B, make pulses at the nodes V1 and V2 depending on the input data and generate the voltages at the drain of MP2 and MN3. If Data1 is 1, there is a pulse on the node V1 right after clock CLK3B and if the Data1 is 0, a pulse is generated on the node V2 right after clock CLK3. These pulses drive second stage transistors such as MN5 and MP5, but only one of those transistors is active at a time and setting the voltage on the transmission line.

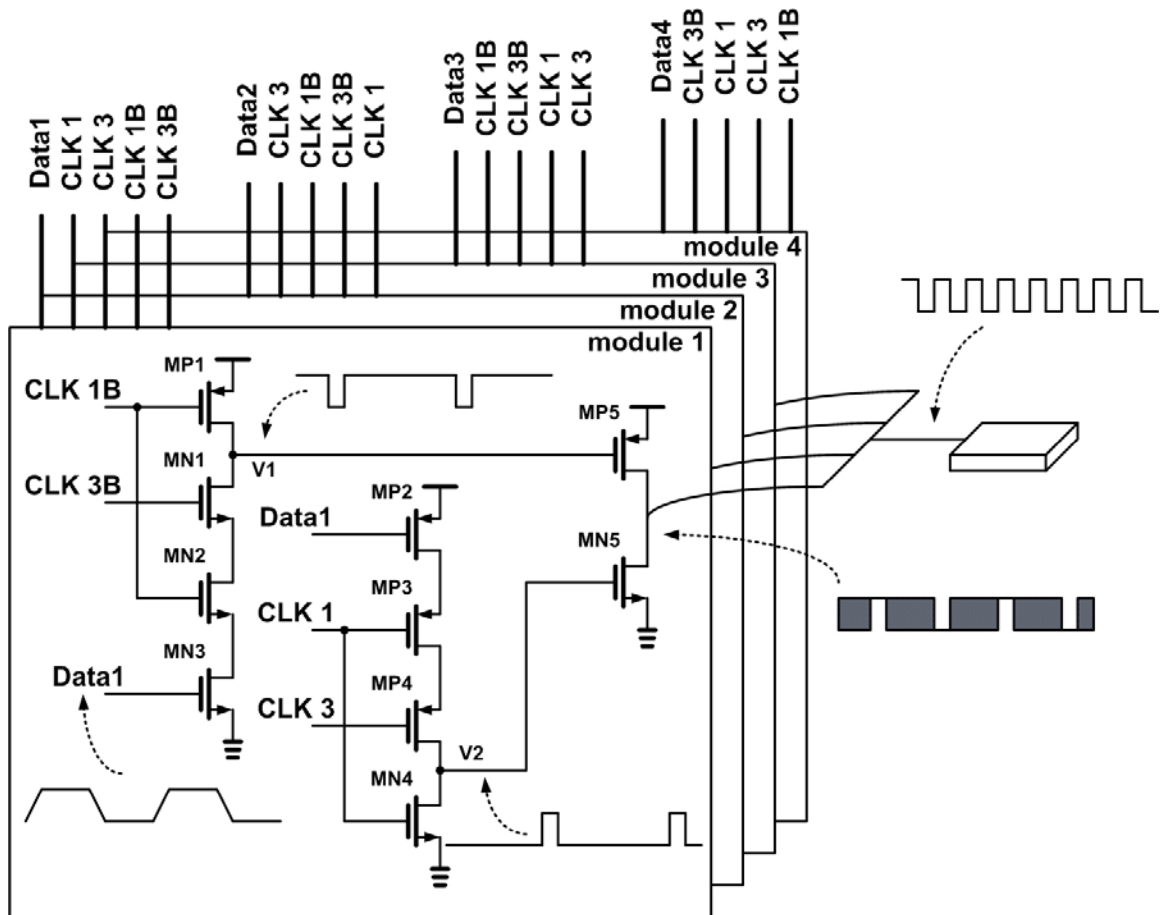


Figure 5.25: Driver for 20Gbps serialization; it consists of four identical modules, and only one module is active at a time. Therefore, the outputs of the driver are the serialized data of the original data in four modules.

The other functional blocks such as de-serializer at the receiver and error check block in previous sections can be used in the same way but with more complexity, for example, with fixed phase tuning, four comparators are required at the receiver.

Figure 5.26 shows the simulated output of the 20Gbps transmitter, recorded at the driver output. Without being loaded by a transmission line, the differential outputs (shown top in Figure 5.26) show a full rail-to-rail voltage swing. The sampling clocks and transmit data pattern for one of the four driver modules is also shown in Figure 5.26. During the overlap of the two clock signals, data is sampled and transmitted.

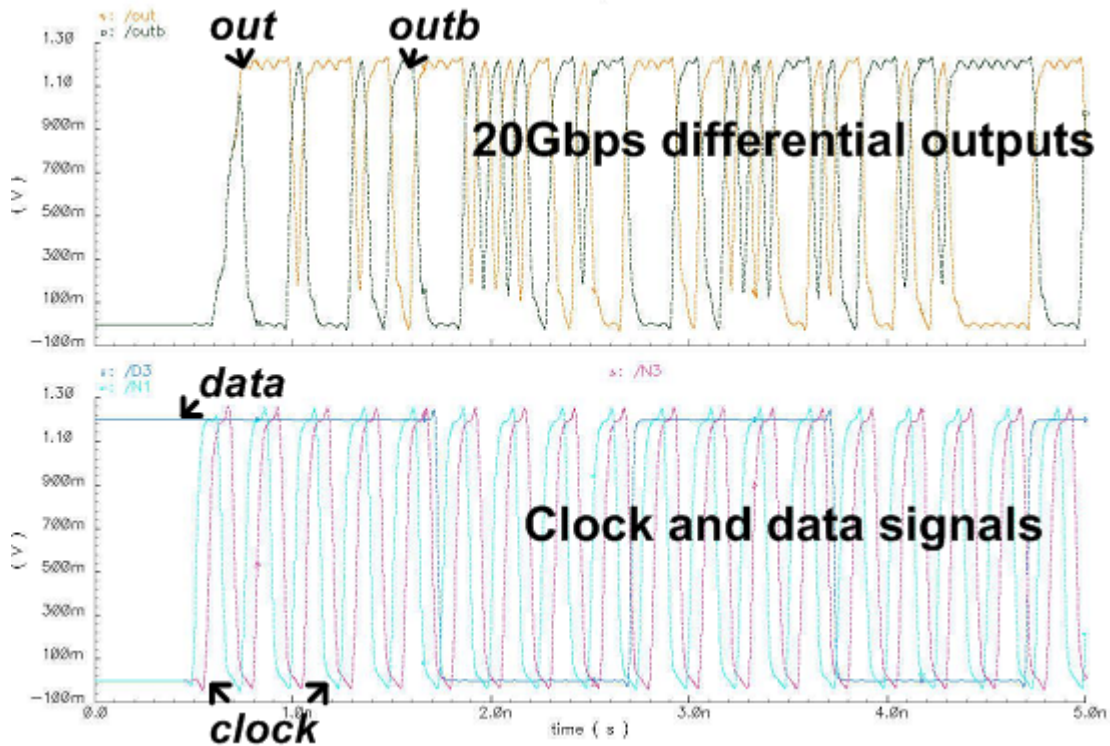


Figure 5.26: 20Gbps serialized data at the output of an unloaded driver is shown at top and clock and data signals for the driver are shown at bottom

Figure 5.27 shows the transmitted and recovered, data patterns, and outputs of the error counter (i.e. the 2nd to the 5th waveforms from the top.) The recovered data is exactly same as the original transmitted data, and error counter indicates no errors.

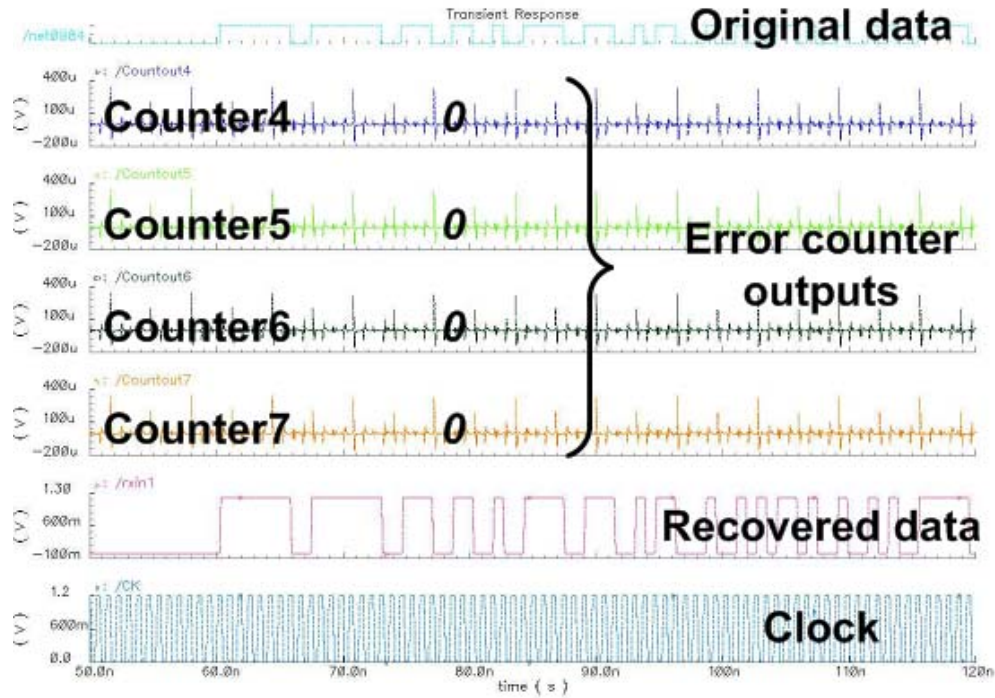


Figure 5.27: Input and output signals of the error check block; Since the recovered data perfectly match with the original data, the outputs of the error counter stay at zero.

5.7. Conclusion

A complete transceiver communicating over a 5.8mm on-chip transmission line was designed and tested. The functionality of the chip was demonstrated with four predefined 8bit patterns (10101010, 11001100, 11110000, and 01001110). The measured BER is less than 10^{-12} with the symmetric patterns such as 10101010, 11001100, and 11110000, and is less than 10^{-10} with a 01001110 input pattern. Functionality was verified in a low cost LCC-packaged device mounted on a FR4 PCB. Although the on-chip signaling frequency is high, there are no requirements for special packaging or special PCB materials. We showed with simulation that a 20Gbps link is also feasible in 0.13 μ m CMOS.

Chapter VI

Summary and Future Work

6.1. Summary

This thesis describes design techniques for the high speed on-chip serial signaling over long(~10mm) lossy transmission lines. With the increase in clock frequencies to multi-GHz rates, it has become impossible to move data across a die in a single clock cycle using conventional parallel bus-based communication. There are also reliability problems due to timing errors, skew, and jitter in fully synchronous systems. Noise, coupling, and inductive effects become significant for both intermediate length and global routing. Techniques for global serial signaling over lossy on-chip transmission lines are demonstrated.

High-speed long-range serial signaling is best done over transmission lines. However, because of the relatively high sheet resistance of metal interconnect layers, on-chip transmission lines tend to be lossy. Because of the different modes of propagation present in a lossy transmission line, low frequency components of digital signals travel slower than high frequency components. This difference in velocities causes significant inter symbol interferences (ISI) for on-chip wires. Matched termination with resistors and the proper selection of the characteristic impedance of the transmission line structure can

effectively suppress ISI. Tradeoffs in the design of lossy transmission lines are also discussed.

Multi-stage LC oscillators are used extensively to generate multi-phases at high frequencies due to their low phase noise. Conventional coupling between oscillators introduces out of phase currents, and this out of phase current causes a lower effective quality factor for each oscillator stage. However, a new technique, capacitive coupling introduces in phase coupling between stages. Increased coupling with a ring of capacitors decreases phase spacing error dramatically and, in addition, the phase noise of multi-stages is also decreased thanks to in-phase coupling. A three-stage capacitively coupled oscillator was designed and tested. The oscillator with capacitive coupling shows 1.18ps measured RMS jitter at 4GHz, while an oscillator without capacitive coupling shows 8ps RMS jitter at 4.5GHz. The frequency difference comes from the capacitive loading of the ring of capacitors. A PLL with a four stage oscillator and with capacitive coupling was also designed and tested. It exhibits measured RMS jitter ranging from 1.61ps RMS jitter and 1.88ps over a 400MHz tuning range from 3.3GHz to 3.8GHz.

A full transceiver communicating over a 5.8mm on-chip transmission line was designed and tested. The prototype device consists of a PLL, a transmitter, a receiver, as well as error checking logic for self test. The LC oscillator based PLL generates a 4.5GHz differential clock signal, which is routed to both the transmitter and the receiver. The transmitter serializes 8b wide 1.125Gbyte/s parallel data and drives the serialized data down the lossy on-chip transmission line. A phase-tuned receiver samples and de-serializes the received signal. Since the sampling instant is tuned to match the received signal eye, there is no requirement to match the clock and signal routing or clock and

signal delays. The 4.5GHz PLL output clock is divided by two (2.25GHz) and four (1.125GHz) for use in serializing the parallel 8b 1.125Gbyte/s data at the transmitter and de-serializing the serial 9Gbit/s data at the receiver, respectively. An error checking block verifies the recovered and de-serialized data from the receiver against the original data and counts the number of discrepancies. The measured BER is less than 10^{-12} with a 10101010 input pattern, and is less than 10^{-10} with a 01001110 input pattern.

6.2. Future work

In principle, signaling rates of over lossy on-chip lines can be very high. Spice simulation shows that a 10mm transmission line structure in 130 nm CMOS designed according to the design method in chapter II can achieve 40Gbps with the ideal $2^{32}-1$ PRBS data (Figure 6.1). In practice, signaling rates are limited by transistor speed, and in particular by the limited speed of the digital serialization circuitry. It is expected that we can achieve much higher data rates with the more advanced CMOS technology.

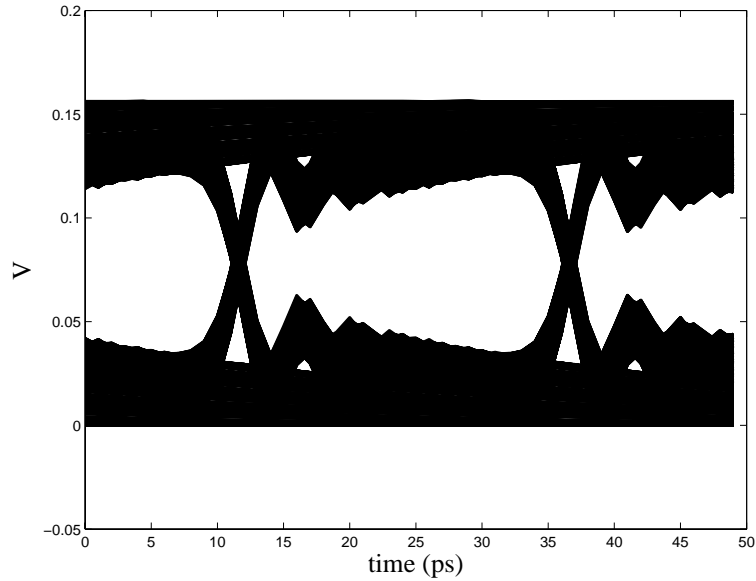


Figure 6.1: Simulated eye diagram of 1 cm link with 40 Gb/s PRBS ($2^{32}-1$) data.

Table 6.1 shows the FO4 delays of an inverter cell in three different CMOS technologies. The 9Gbps 130nm CMOS on-chip link, presented in this work, achieves a bit period equivalent to about 2 FO4 delays. Since the link data rate is determined by digital circuit speed, a comparison of FO4 delays indicates that 25Gbps could be achieved 65nm CMOS.

The on-chip serial link methodology developed in this work could also be applied global communication in 3D integrated systems. Since high-speed signaling works well over lossy lines, transmission lines could connect across die and between die through interdie vias. This would require some study of matching, reflections and loss at the vias. Similar to the work described here a lower frequency clock could be distributed to the transmitter and receiver.

Table 6.1 FO4 delay of an inverter

Technology	130nm	90nm	65nm
FO4 delay	53.6ps	45ps	21.3ps

A problem with measuring the phase spacing error in multi-phase oscillators is that the timing difference between signals is hard to measure accurately with an oscilloscope, since the frequency of the signals is so high that a small difference in the length of the cables dramatically changes the timing difference. The scheme proposed to measure image rejection ratio described in chapter IV can be implemented. A limitation of this approach is that only the phase-spacing-error of a two stage or four stage oscillator can be measured properly.

Capacitive coupling is an effective coupling method especially in high frequency applications. Although capacitive coupling is implemented here for multi-stage LC oscillators, no research has been done on capacitor coupling in inverter-based ring oscillators. Even though the noise performance of an LC oscillator is much better than that of a ring oscillator, a ring oscillator requires far less area and power.

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