Simultaneous Switching Noise in Printed Circuit Boards

LINDA P.B. KATEHI and KAREM A. SAKALLAH

A first-year project status
report prepared for INTEL
Corporation

INTRODUCTION

The research effort during the first year accomplished two important goals; (a) the understanding of the problem of switching noise as it is viewed by the printed circuit board designer and (b) the development of a comprehensive plan of study. A brief discussion of the conclusions drawn from the first part of the study and a detailed description of the developed plan of study with the up to date accomplishments will be given below. This report will be concluded with a discussion of next years proposed effort.

SWITCHING NOISE - OVERVIEW OF RELEVANT WORK

Ground bounce or simultaneous switching noise (SSN) are names used by the circuit designer to indicate the same noise mechanism. This noise is observed at the output terminals of switching drivers as a substantial potential(voltage) variation which is due to the uncontrolled parasitic inductances between the chips and the board [1],[2], [12]. This noise can effectively propagate through the circuit interconnects to the quiet drivers and can be augmented due to local reflections to lead into substantial input level shifts which in turn can cause a loss of stored data (see Figures 1 and 3). In the literature, the switching noise seen at a chip output is expressed as the product of

$$\Delta V = L_{eff} \times N \times \frac{dI}{dt}$$

the number of drivers N, the effective inductance L_{eff} seen at the chip output and the rate of change of the current dI/dt (see Figure 2).

The effective inductance shown in the above equation has the following characteristics:

- It incorporates the effects of the chip-package inductance, the chip lead inductance and the mutual inductances between the chip and the printed circuit board.

- It varies from chip to chip and pin to pin even if the chips are identical and connected to the same printed circuit board.

- It depends on the number of drivers and their relative position on the board.

As a result of the above observations, the effective inductance seen by a single chip at the ground leads can be given by the following equation:

$$L_{eff} = L_{g,lead} + L_{PCB} + M_{chip,package} + M_{chip,PCB}$$

where

$L_{g,lead}$ = inductance of ground lead

L_{PCB} = effective inductance of printed circuit board

$M_{chip,package}$ = mutual inductance between the ground lead and the rest of the chip leads.

$M_{chip,PCB}$ = mutual inductance between ground lead and printed circuit board.

Depending on the application some inductance terms may be more important than others. For example, for specific PCB designs, the inductance of the printed circuit board may have secondary effects as compared to the inductance of the chip ground lead. As a result, the second and fourth term in the above equation can be ignored. In the most general case, however, all of the above terms need to be kept and evaluated with sufficient accuracy.

Another important issue in the evaluation of switching noise is the level of system hierarchy at which this noise needs to be investigated. The need to study switching noise effects at a system level has led historically to a **macroscopic** treatment of the problem. However, the in-depth understanding of the sources which generate this noise calls for more precise, **microscopic**, treatment. A discussion about these two treatments is given in the following section.

MACROSCOPIC VS. MICROSCOPIC

Most of the work performed in the literature has been performed at the chip level with the major assumption that the PCB inductance plays a secondary role. As a result, the fine structure of the board was ignored and the chip pin inductance was considered as the prime source. Furthermore, the geometrical shapes of the power and ground chip pins were not considered important in determining noise levels but it was the number and relative location of the pins that played the most important role [7], [13]. The treatment of switching noise at that level of hierarchy has given a lot of qualitative understanding but has led to unnecessarily conservative and expensive solutions without providing suppression of the noise to desired levels.

On the contrary, very little work has been performed on PCBs or Chips at a microscopic level. In the case of SSN on printed circuit boards, simple cases of two- and three-plane

combinations have been considered which have led to inconclusive results [4], [10]. In these studies, the effects of specific ground geometries on the noise levels were studied but the results were never extended to higher levels of hierarchy thus leaving a rather vague understanding of the importance of these effects on the overall noise level. In the case of SSN on the chip level, the size of the chip pins has been extensively considered and the pin inductance has been evaluated both statically as well as dynamically in the frequency and time domains. However, as with the microscopic analyses discussed earlier, these findings were never implemented into a study of noise as seen at higher system levels and the effort was never extended beyond the level of an academic exercise.

Despite the existing research effort the problem of simultaneous switching noise is still as incomprehensible as it has ever been. The macroscopic as well a microscopic treatments never really converged to the same point thus making the coordination between the two approaches a very much needed effort and necessary for the realistic treatment of the problem.

It is the coordination between the two efforts that we emphasize in our design methodology as it will be described in the next section.

DESIGN METHODOLY: PARASITIC EXTRACTION

Figure 4 shows the major steps of a design methodology necessary for the characterization of the switching noise. This design methodology starts with the layout of the printed circuit board and splits the effort into three different directions: (a) The package modeling, (b) the power/ground plane modeling and (c) the chip driver modeling. These three efforts are then combined to provide an equivalent circuit for the entire printed circuit board which will then be analyzed with an asymptotic waveform approximation to provide a characterization of the existing noise (see Figure 4). Then given this noise signature, an appropriate noise analysis will be performed to specify the appropriate positions and values for the decoupling capacitors. This new circuit arrangements will then be analyzed to verify the effectiveness in noise suppression (see Figures 5,6).

DESCRIPTION OF EFFORT PERFORMED DURING THE FIRST YEAR

During the first year our effort concentrated on the package modeling which involved the exact characterization of specific pin and via geometries and the derivation of equivalent circuits. Through this process we developed a static and dynamic finite element code which can evaluate the field distribution for any open or shielded geometry. With this field distribution known, scattering parameters and equivalent circuits as functions of a number of parameters can be computed. Via inductances in a variety of environments were computed and compared to Finite Difference Time Domain data for validation purposes. Up to now this work has resulted into two symposia presentations (see **Publ.1** and **2**) and into one journal paper (see **Publ.3**). Details of the results from this effort are given in Appendix A.

Also during the first year, the problem of potential variations on the ground was addressed and results were generated for some geometries. This effort has led to the following two interesting observations:

- The computational intensity of the analysis, either static or dynamic, results from the application of the finite elements approach and the discretization of the structure. Such an analysis, though necessary for an accurate microscopic treatment, can only treat small to medium size geometries.

- As a result of the above, an extension of the static or dynamic microscopic treatments to more complex printed circuit board geometries with hundreds of vias and chip pins connecting to multiple power and ground planes is considered as practically impossible.

In view of the above, a tile approach described in the next section is strongly proposed for development during the next phase of this study.

2nd YEAR'S PROPOSED EFFORT-TILE APPROACH

This year's effort will be centered around the previously mentioned **Tile Approach**. This approach is briefly described in the following few steps:

- The original printed circuit board geometry will be divided into tiles corresponding to basic primitive structures.

- The finite element method will then be applied to provide appropriate equivalent circuits which will include all the underlying electromagnetic effects, such as propagation and electromagnetic interference.

- These equivalent circuits will be included in a library of primitive components in order to be used at later stages for the analysis of the whole printed circuit board.

- For a given printed circuit board geometry, the appropriate equivalent circuits for the various primitive geometries will be retrieved from the library and will be interconnected to create an appropriate SPICE/RICE circuit which will be analyzed by asymptotic waveform approximation techniques.

Some example primitive structures with their equivalent circuits are given on Figures (7)-(11).

DELIVERABLES FOR YEAR 2

The deliverables for the second year are outlined below:

- A library of equivalent circuit generators for primitive structures using the codes developed during the first year of this effort.
    * Chip Leads
    * P/G Tiles
- Perform PCB-wide electrical simulation using RICE.
    * Aurora-II daughter board
    * Intel test board
    *Switching configurations assumptions

* Interactive decoupling capacitance insertion.

PUBLICATIONS

1. J-G Yook and L.P.B. Katehi, "Capacitance and Inductance Evaluation of Vertical Inter-connects Using the Finite Element Method," 1993 International URSI Symposium, Ann Arbor, Michigan, June 1993, pp.33.

2. J. Yook, M. Kurk, N. Dib, L. Katehi and T. Arabi, "Evaluation of Ground Inductance in Printed Circuit Boards," to be presented in the 2nd Topical Meeting on Electrical Performance of Electronic Packaging, Monterey, California, October 1993.

3. J-G Yook, M. Kurk, N.I. Dib and L.P.B. Katehi, "Characterization of Planar Circuit Interconnections Using FDTD and FEM Techniques," submitted to the IEEE Transactions on Microwave Theory and Techniques, Special Issue on Interconnects and Packaging.

REFERENCES

4. D. Shear, "EDN's Advanced CMOS Logic Ground-Bounce Tests," EDN, March 1989, pp. 88-114.

5. D. Shear, "Ground-Bounce Tests; Revisited," EDN, April 1993, pp. 120-151.

6. J. Bond, "High-Speed Logic Demands Careful Design," Computer Design, October 1987, pp.23-30.

7. M.A. Schmitt et.al., "Current Distribution in Power and Ground Planes of a Multilayer PIN Grid Array Package," 8th Annual International Electronics Packaging (IEPS) Conference, Dallas, Texas, Nov. 7-10, 1988, pp. 467-475.

8. P.A. Sandborn, H. Hashemi and B. Weigler, "Switching Noise in a Medium Film Copper/Polyamide Multichip Module," SPIE, Vol.1389, International Conference on Advances in Interconnections and Packaging, 1990, pp. 177-186.

9. A.I. Rainal, "Computing Inductive Noise of Chip Packages," AT&T Bell Laboratories Technical Journal, Vol. 63, No. 1, Jan. 1984, pp. 177-195.

10. R. Sonthinathan and J.L. Prince, "Simultaneous Switching Ground Noise," IEEE Journal of Solid State Circuits, Vol. 26, No. 11, Nov. 1991, pp.1724-1728.

11. E.E. Davidson, "Electrical Design of a High Speed Computer Package," IBM J. Res. Develop., Vol. 26, No. 3, May 1982, pp.349-361.

12. C. Dike, "Equivalent Circuit Model Subtle Traits of Advanced CMOS, ICs," EDN, April 1988, pp. 189-195.

13. O. Pederson, B-E. Flaten and T. Gleditsch, "Modeling of Power and Ground Planes," Proceedings of the IEPS International Electronics Packaging Conference, San Diego, September 1991, pp. 654-663.

14. P.A. Brennan, N. Rower, A.E. Ruehli, "Three-Dimensional Inductance Computations with Partial Element Equivalent Circuits," IBM J. Res., Develop., Vol. 23, No. 6, Nov. 1979, pp. 661-667.

15. G. A. Katopis, "Delta-I Noise Specification for a High-Performance Computing Machine," Proceedings of the IEEE, Vol. 73, No. 9, Sept. 1985, pp. 1405-1415.

16. R. Sorrentino, F. Alessandri, M. Mongiardo, G. Avitabile and L. Roselli, "Full-Wave Modeling of Via-Hole Grounds in Microstrip by Three-Dimensional Mode Matching Technique," IEEE Trans. on Microwave Theory and Techniques, Vol. 40, No. 12, Dec. 1992, pp. 2228-2233.

17. W. D. Becker, P.H. Harms and R. Mittra, "Time-Domain Electromagnetic Analysis of Interconnects in a Computer Chip Package," IEEE Trans. on Microwave Theory and Techniques, Vol. 41, No. 1, Jan. 1993, pp. 153-156.

18. R.C. Douglas, G.W. Bull and D.J. Doyle, "Multilayer Microwave Boards: Manufacturing and Design," Microwave Journal, April 1993, pp. 87-98.

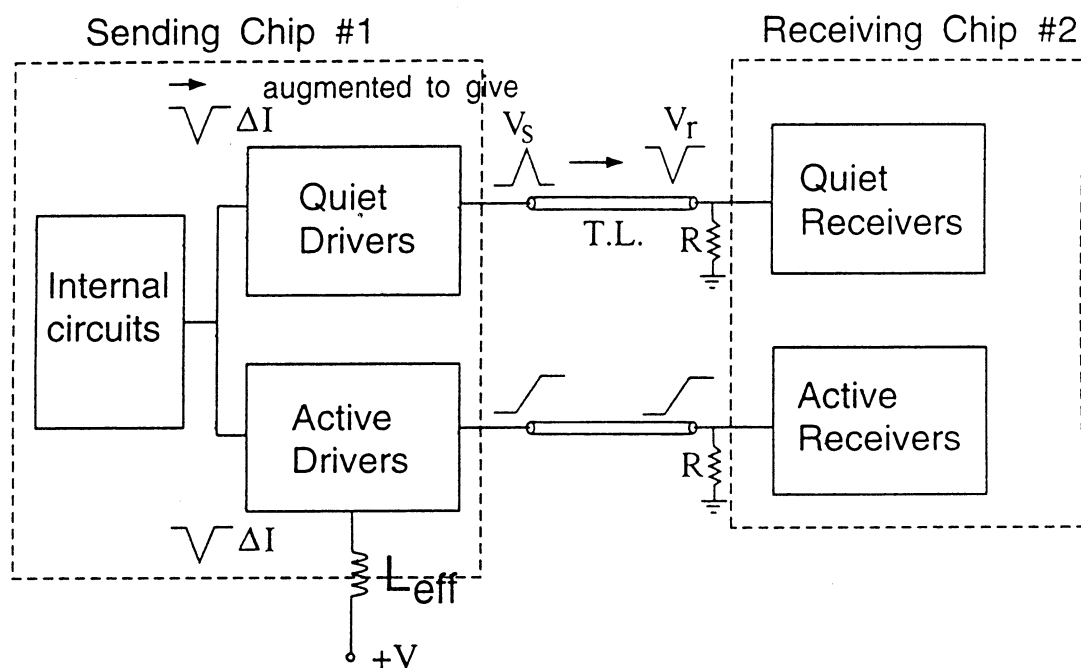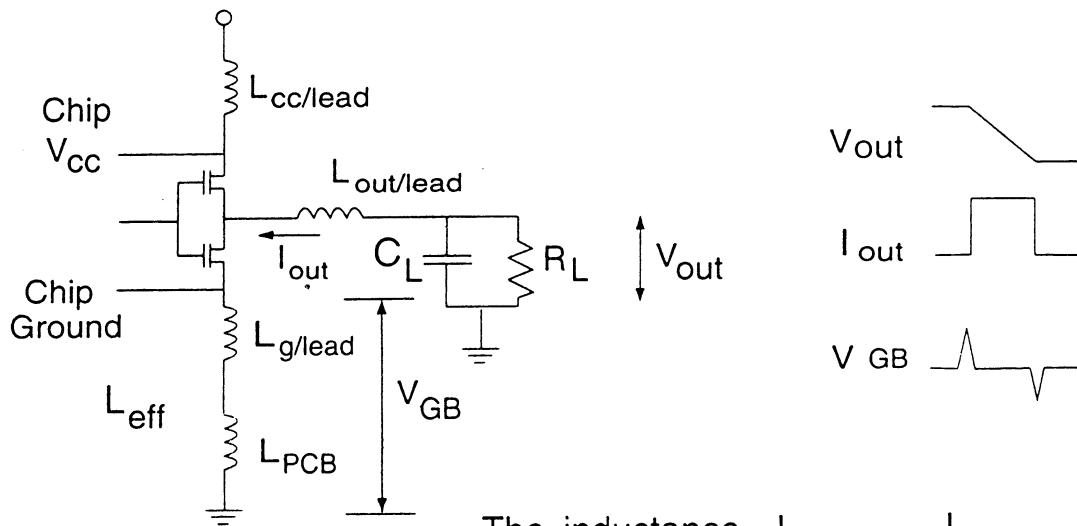**FIGURE 1. A Representation of Simultaneous Switching Noise**

FIGURE 2. Ground Bounce as Seen from the Chip's Side

The inductance L_{eff} = $L_{g/lead}$ + L_{PCB} between the chip ground and the system ground is the major contibutor to ground bounce.

FIGURE 3. The Effects of Ground Bounce on Output Voltages

FIGURE 3. The Effects of Ground Bounce on Output Voltages
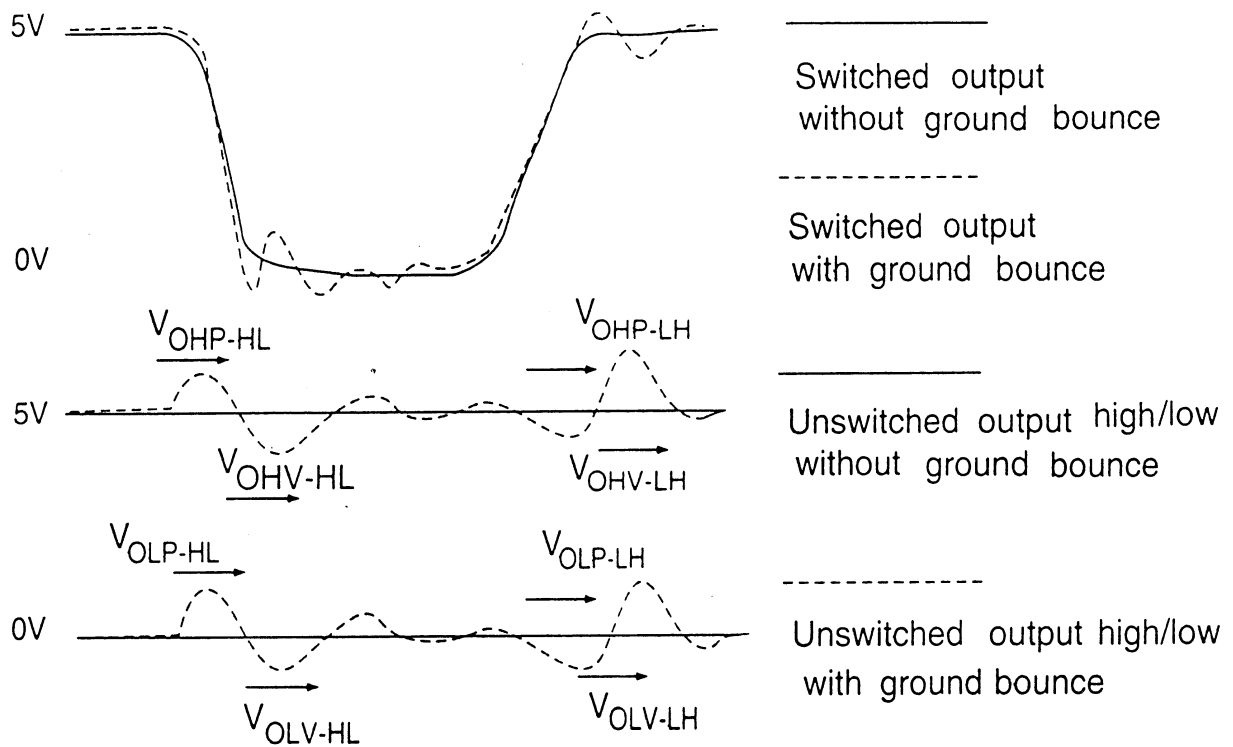
FIGURE 4. Design Methodology:Parasitic Extraction

SSN In PCBs
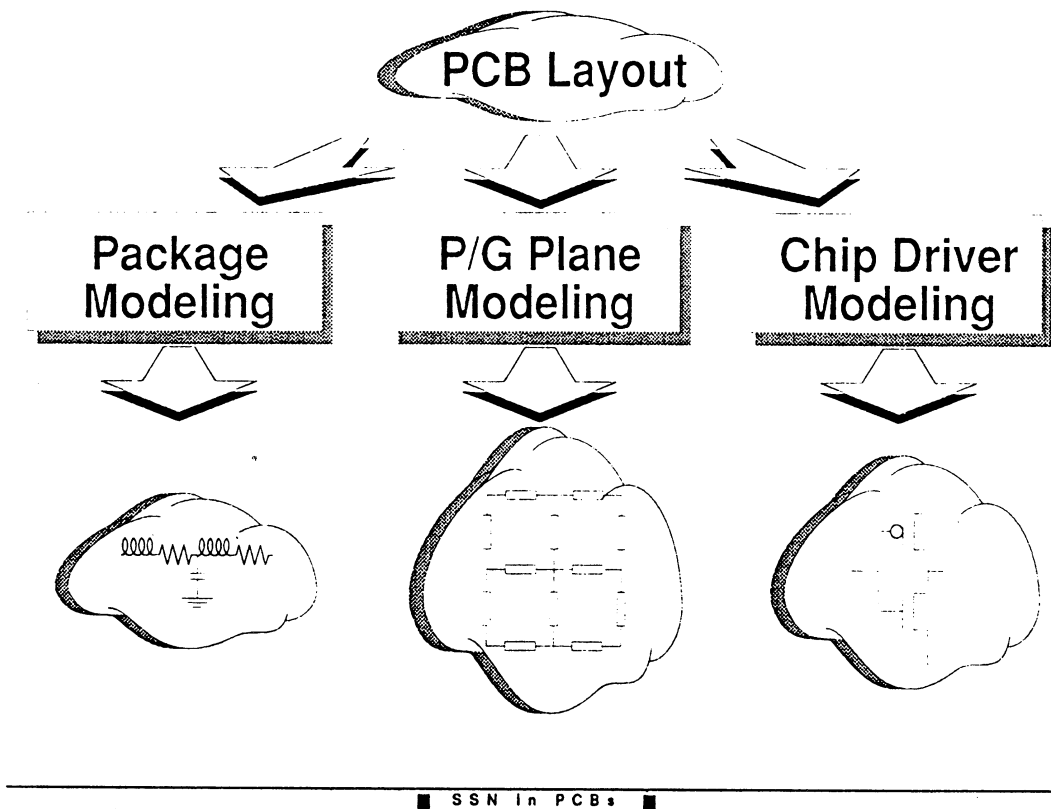
FIGURE 5. Design Methodology: Noise Containment

User Input 〉 Noise Analysis 〉 Done

Excessive

User Input 〉 Decoupling Cap Insertion

Repeat
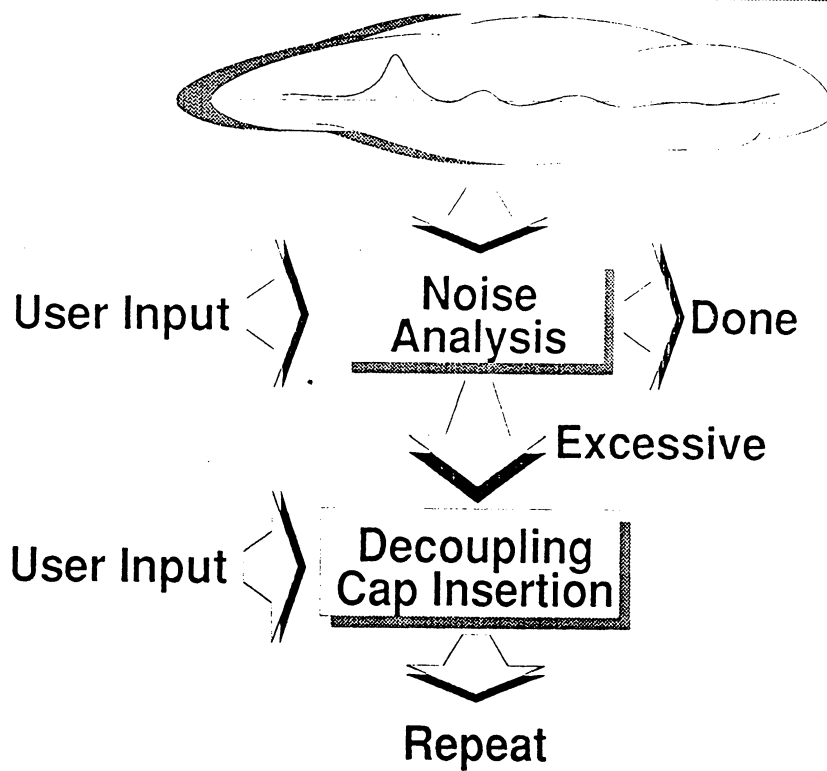
FIGURE 6. Design Methodology: Electrical Simulation

P/G Equivalent Circuit

Asymptotic Waveform Simulation
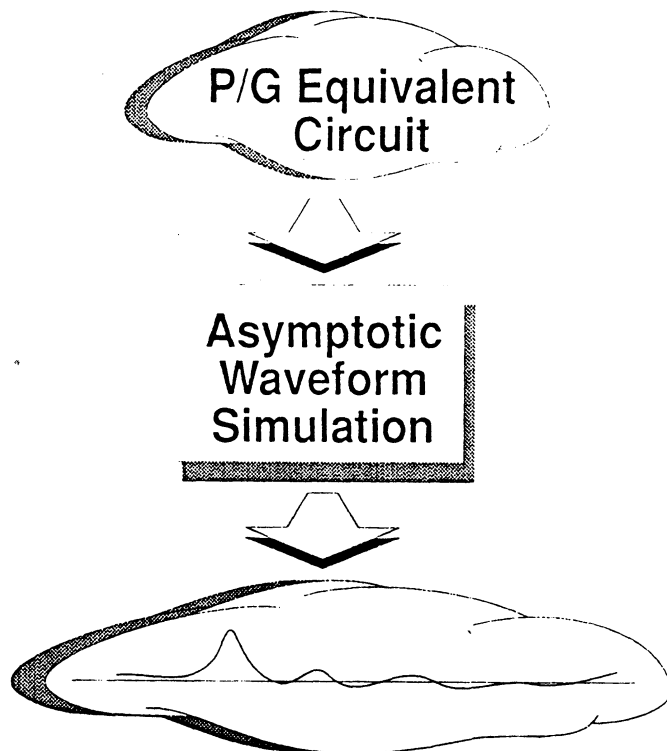
FIGURE 7. Equivalent Circuits: Power/Ground Configuration

(a)
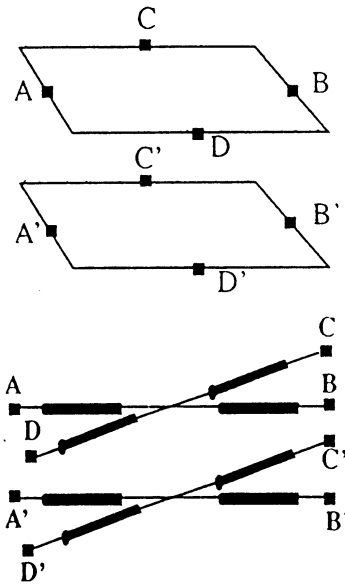
(b)
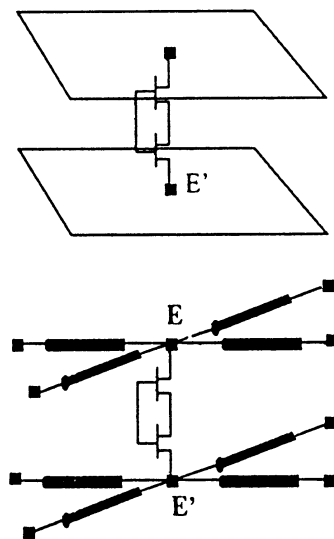
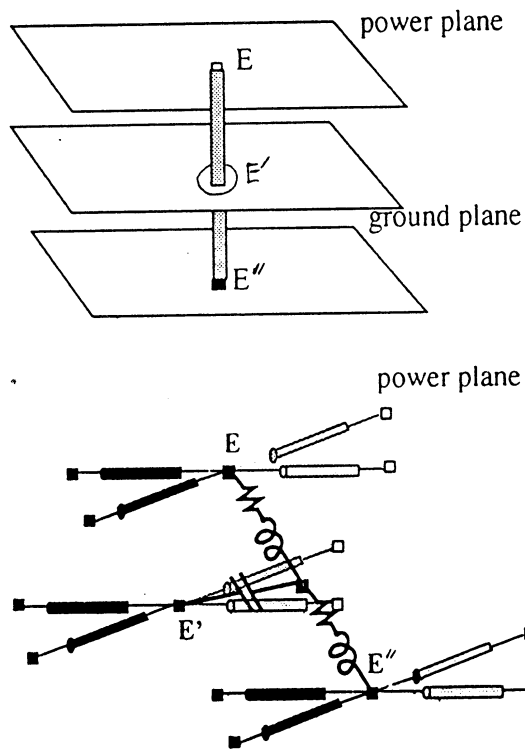FIGURE 8. Equivalent Circuits: P/G/P Configuration with a PTH

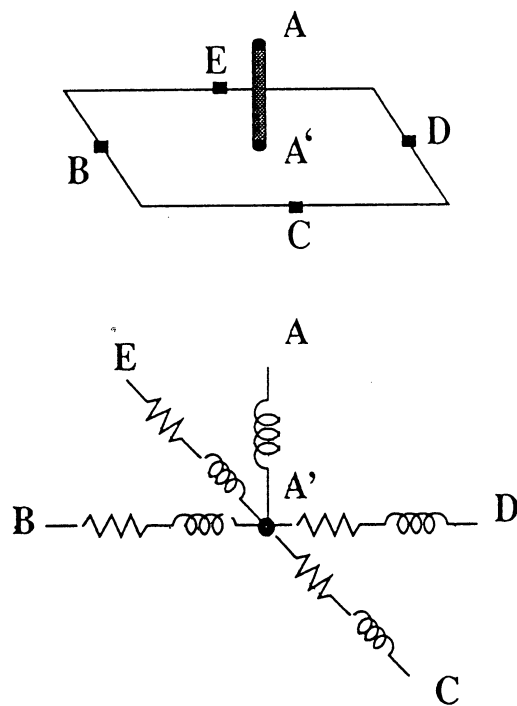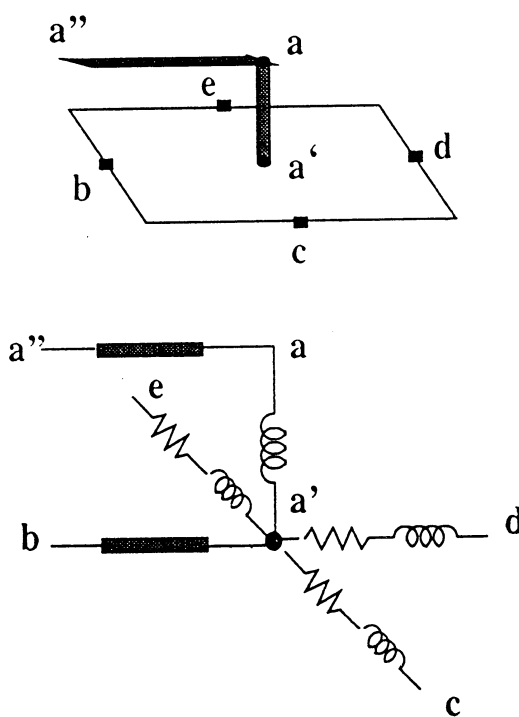FIGURE 9. Equivalent Circuits: Via/Ground Configuration

FIGURE 10. Equivalent Circuits: Interconnect/Via/Ground Configuration.

APPENDIX A

Formulation of the Finite Element Method

Static Problem

Start from Maxwell's equation with electric and magnetic potentials, one can derive following functionals :

$$L\{\phi\} = \int_V \frac{\epsilon}{2}[\nabla\phi \cdot \nabla\phi]dV - \iint_S \rho\phi \, dS$$

$$L\{\bar{A}\} = \int_V \frac{1}{2\mu}[\nabla \times \bar{A} \cdot \nabla \times \bar{A}]dV - \iint_S \bar{J}_s \cdot \bar{A} \, dS.$$

To find appropriate solution of the equations, one need to minimize the functionals with proper basis functions. For electrostatic problem, the node based FEM may be a good candidate. However, for magnetostatic problem, we need to introduce vector based FEM in which vector edge basis function can be used to guarantee spurious-free solution.

Dynamic Problem

From source free vector wave equations, one can derive the following matrix equations after applying Galerkin's method and some vector identities.

$$\{[P^e] - k^2 [Q^e]\} [H^e] = [R^e]$$
$$\{[P^e] - k^2 [Q^e]\} [E^e] = [S^e]$$

where

$$P_{ij}^e = \int_{V_e} (\nabla \times \bar{W}_j^e) \cdot (\nabla \times \bar{W}_i^e)\, dV$$
$$Q_{ij}^e = \int_{V_e} \bar{W}_i^e \cdot \bar{W}_j^e\, dV$$
$$R_i^e = j\omega\mu \oint_{S_e} \bar{W}_i^e \cdot (\hat{n} \times \bar{H})\, dS$$
$$S_i^e = -j\omega\epsilon \oint_{S_e} \bar{W}_i^e \cdot (\hat{n} \times \bar{E})\, dS.$$

In the above equation, k is the only frequency dependent term. For a static problem, $k = 0$. But for a dynamic problem, $k \neq 0$. Moreverover, the overall system equation is complex symmetric and positive semi-definite.

Boundary Conditions

- PEC : $E_{tan} = 0$ $\Rightarrow$ Enforce zero tangential electric field.

- PMC : E_{tan} is continuous $\Rightarrow$ Natural boundary condition. The edge based vector basis function automatically satisfy *pmc* boundary condition for E field formulation.

- ABC : Absorbing Boundary Condition(1st and 2nd order ABC). To truncate a computational domain one needs to introduce artificial boundaries which can simulate infinite space or look like transparent for outgoing waves. In this study we tried to implement vector ABC for 3-dimensional vector wave equations.

Scattering parameter

- *One Port Network :*

  Reflection Coefficient, Normalized Input Impedance

$$\Gamma(x) = \frac{SWR - 1}{SWR + 1} e^{-j2\beta_g(x_{max} - x)}$$

$$SWR = \frac{|I_{max}|}{|I_{min}|},$$

$$z(x) = \frac{1 + \Gamma(x)}{1 - \Gamma(x)}$$

Note. Lossless network $\Rightarrow |\Gamma| = 1$.

Circuit Parameter Extraction

Inductance of via hole and ground plane

- *Method 1 :*

$$L = \frac{\Phi}{I} \qquad [Henry]$$

$$\Phi = \int \int_S \bar{B} \cdot d\bar{S} \qquad [Wb/m^2]$$

$$= \int \int_S \mu_0 \mu_r \bar{H} \cdot d\bar{S}$$

$$I = \oint \bar{H} \cdot d\bar{l} \qquad [Ampere]$$

- *Method 2 :*
  From the S-parameter data, find an equivalent circuit and values of inductance and capacitance. This method depends upon frequency range and reference plane. And it includes the overall effect after the reference plane.

- *Symmetric Two Port Network :*

1. Even and odd mode excitation

2. Even and odd mode input impedances

3. Impedance parameter evaluation

4. S parameter evaluation

$$z_{11} = \frac{z_{in}^e + z_{in}^o}{2}, \quad z_{12} = \frac{z_{in}^e - z_{in}^o}{2}$$

$$\Downarrow$$

$$S_{11} = S_{22} = \frac{z_{11}^2 - 1 - z_{12}^2}{z_{11}^2 + 2z_{11} - z_{12}^2 + 1}$$

$$S_{12} = S_{21} = \frac{2z_{12}}{z_{11}^2 + 2z_{11} - z_{12}^2 + 1}$$

Potential distribution on the ground plane

Under actual conditions a ground plane is not an ideal ground. Moreover, in high frequency circuit the potential on the ground plane is varying due to many factors. To find potential distribution at high frequency range we use the finite element method. After we found electric and magnetic field distribution in a given computational domain, we extracted potentail distribution on the ground plane with rectangular inductance grid model.

$$\bar{E} = -\nabla\phi$$

From this relation the potential difference between any two points can be found as follows:

$$\phi_{AB} = -\int_A^B \bar{E} \cdot d\bar{l}$$
$$= j\omega L_{AB} I_{AB}$$

where L_{AB} and I_{AB} are inductance and current between any arbitrary two points A and B.

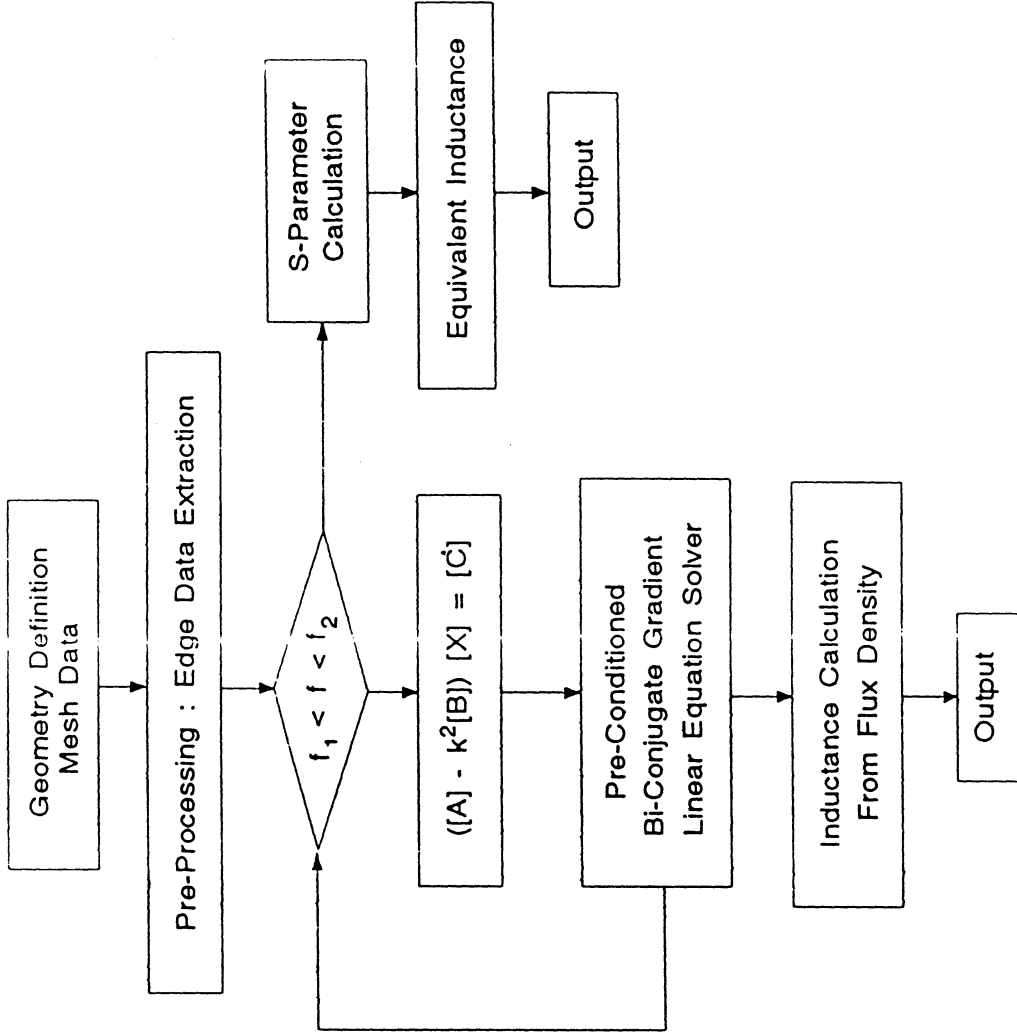Geometry Definition Mesh Data

Pre-Processing : Edge Data Extraction

$f_1 < f < f_2$

$([A] - \kappa^2[B]) \, [X] = [C]$

Pre-Conditioned Bi-Conjugate Gradient Linear Equation Solver

Inductance Calculation From Flux Density

Output

S-Parameter Calculation

Equivalent Inductance

Output

Figure 1 :   Flow chart for computation of S-parameters and via and ground inductances.
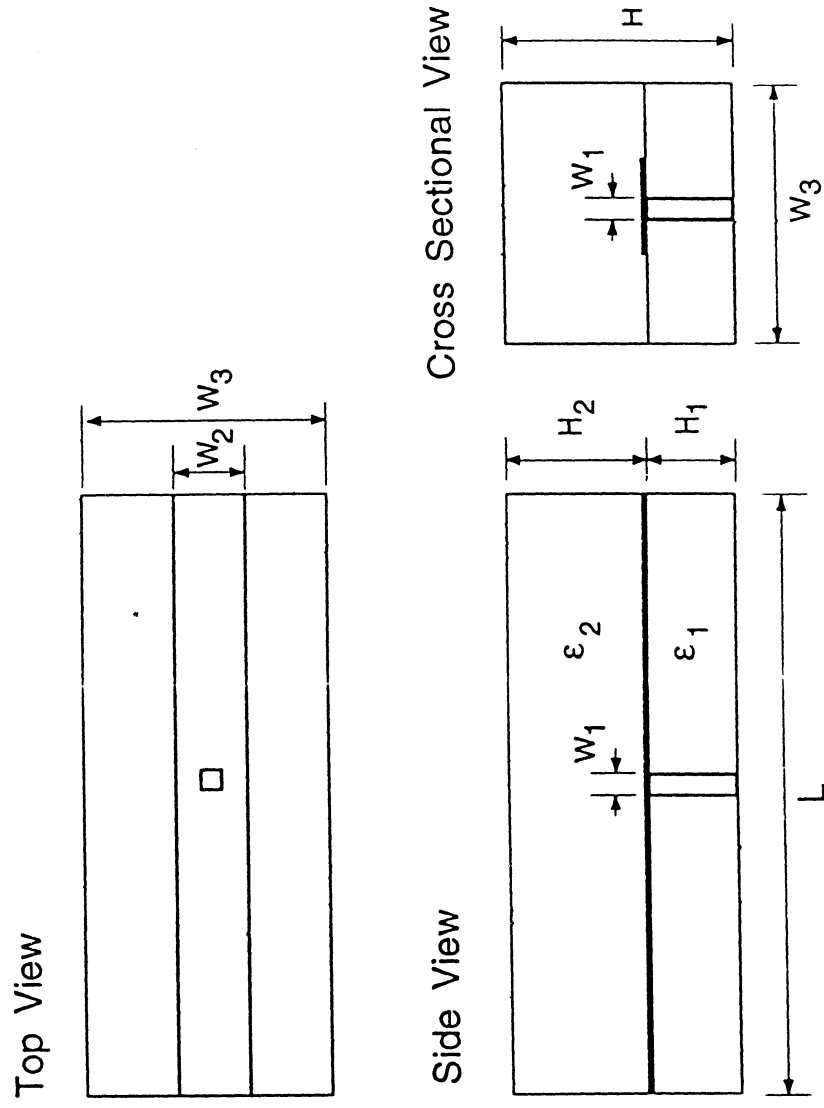
Numerical results

2-port Via Hole

Top View

Side View

Cross Sectional View

Figure 2 :   Geometry of two port via hole.
$W_1 = 0.085mm$, $W_2 = 0.6mm$, $W_3 = 1.785mm$,
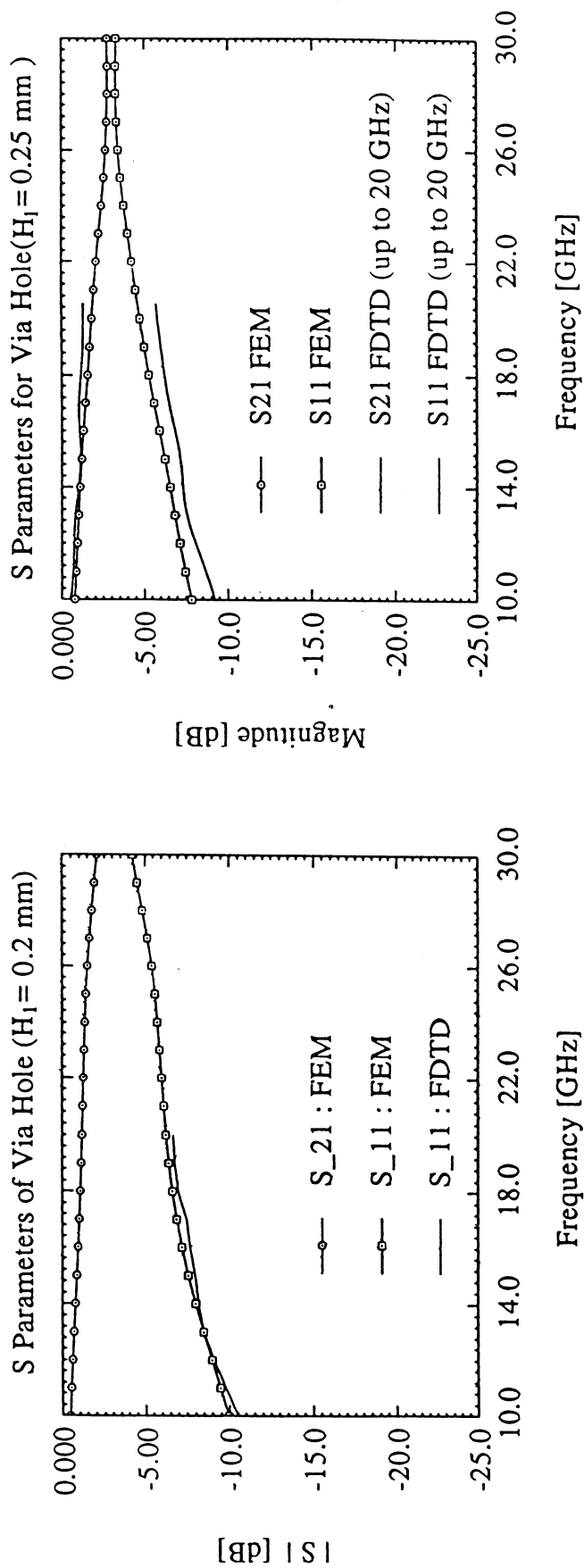$H_1 = 0.2mm$, $H_2 = 0.5mm$, $\epsilon_1 = 12.9$, $\epsilon_2 = 1$

S Parameters for Via Hole(H_1 = 0.25 mm)

Magnitude [dB]

0.000
-5.00
-10.0
-15.0
-20.0
-25.0

10.0 14.0 18.0 22.0 26.0 30.0

Frequency [GHz]

— ⊙ — S21 FEM
— ⊡ — S11 FEM
——— S21 FDTD (up to 20 GHz)
——— S11 FDTD (up to 20 GHz)

S Parameters of Via Hole (H_1 = 0.2 mm)

| S | [dB]

0.000
-5.00
-10.0
-15.0
-20.0
-25.0

10.0 14.0 18.0 22.0 26.0 30.0

Frequency [GHz]

— ⊙ — S_21 : FEM
— ⊡ — S_11 : FEM
——— S_11 : FDTD

Figure 3 : Scattering Parameters of Via Hole As a Function of Frequency : W_1 = 0.085mm, W_2 = 0.6mm, W_3 = 1.785mm, ϵ_1 = 12.9, ϵ_2 = 1 (a) H_1 = 0.20mm,(b) H_1 = 0.25mm

The University of Michigan / Finite Element Method

Inductance of Via Hole and Ground Plane

—◦—	Via Inductance : FEM (f=10 GHz)
··◦··	Ground Inductance : FEM (f=10 GHz)
----	Via Inductance : FDTD (.1 - 20 GHz Fit)
······	Via Inductance : FDTD (.1 - 2 GHz Fit)

Inductance [pH]: 200. 180. 160. 140. 120. 100. 80.0 60.0 40.0 20.0 0.000

Height [um]: 0.0 50.0 100.0 150.0 200.0 250.0 300.0 350.0 400.0 450.0 500.0
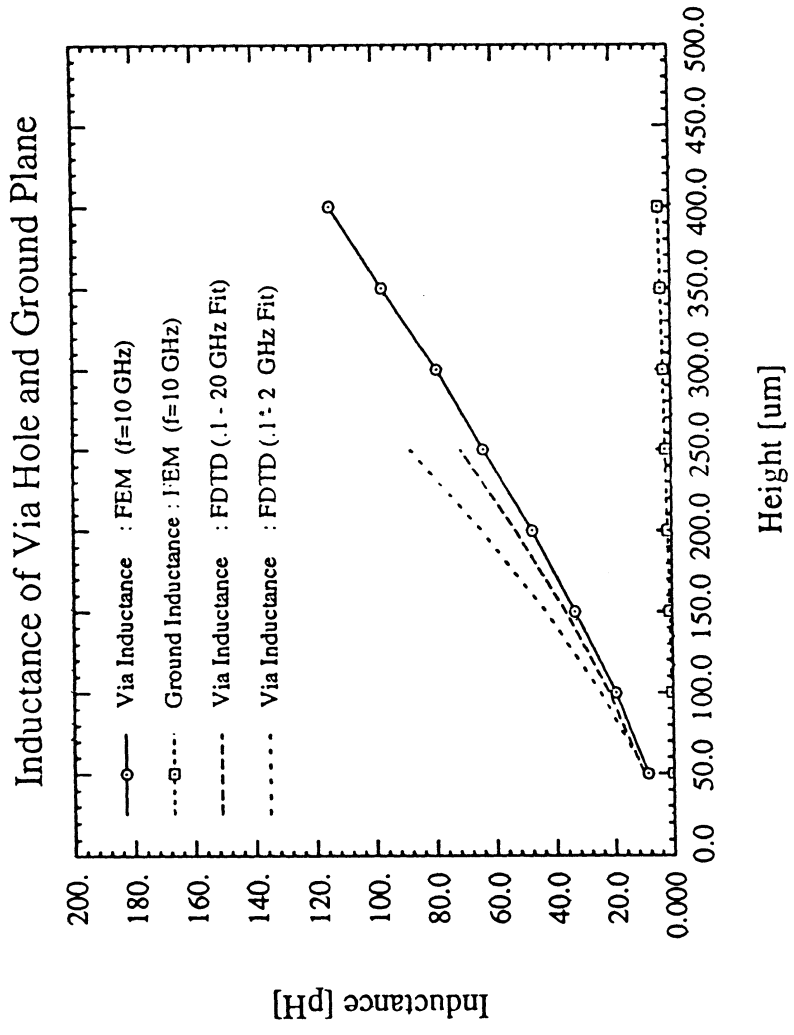
Figure 4 : Via Hole and Ground Inductance As a Function of Via Hole Height at 10 GHz. $W_1 = 0.085mm$, $W_2 = 0.6mm$, $W_3 = 1.785mm$, $\epsilon_1 = 12.9$, $\epsilon_2 = 1$

1-port Via Hole

Top View

Side View

ϵ_2

ϵ_1

W_0

W_2

W_2

W_1

W_1

H_2

H_1
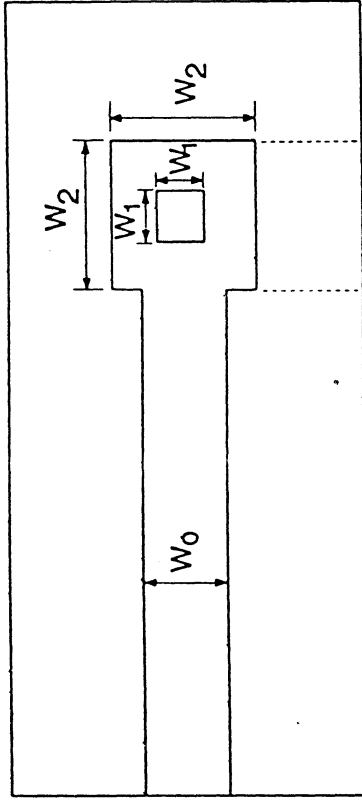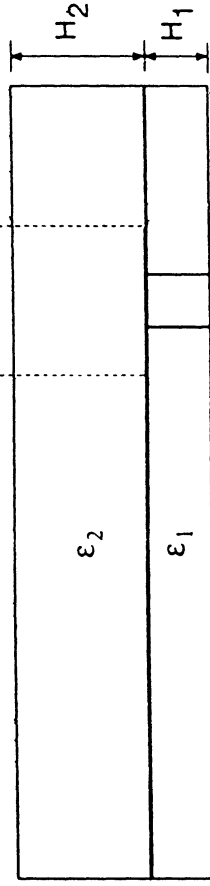
Figure 5 : Geometry of one port via hole. $W_0 = 2.3\text{mm}$, $W_1 = 1.15\text{mm}$, $W_2 = 2.875\text{mm}$, $H_1 = 1.0\text{mm}$, $H_2 = 2.0\text{mm}$, $\epsilon_1 = 3.4$, $\epsilon_2 = 1$.
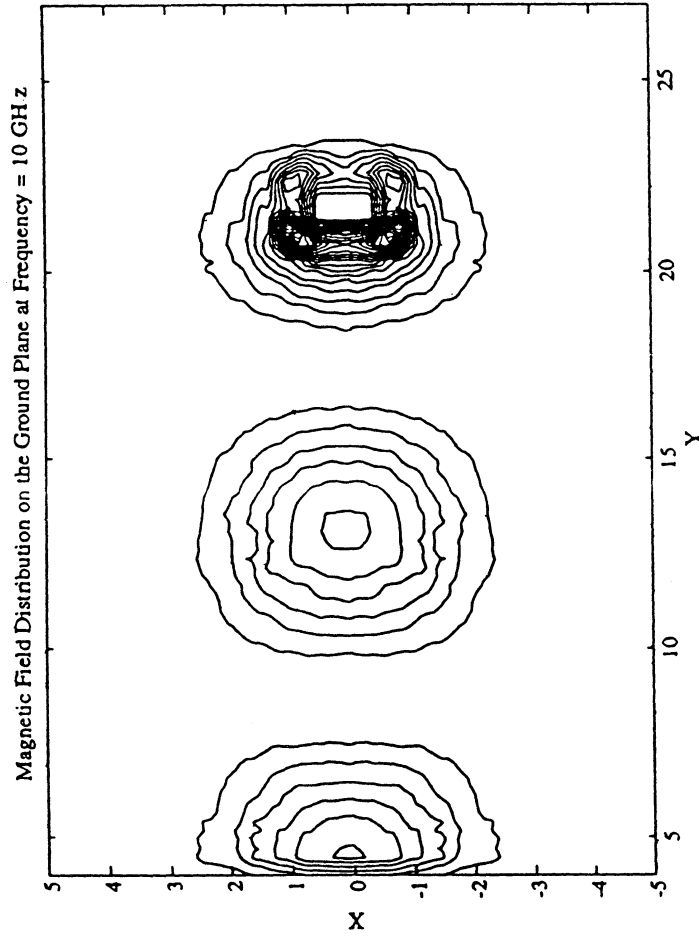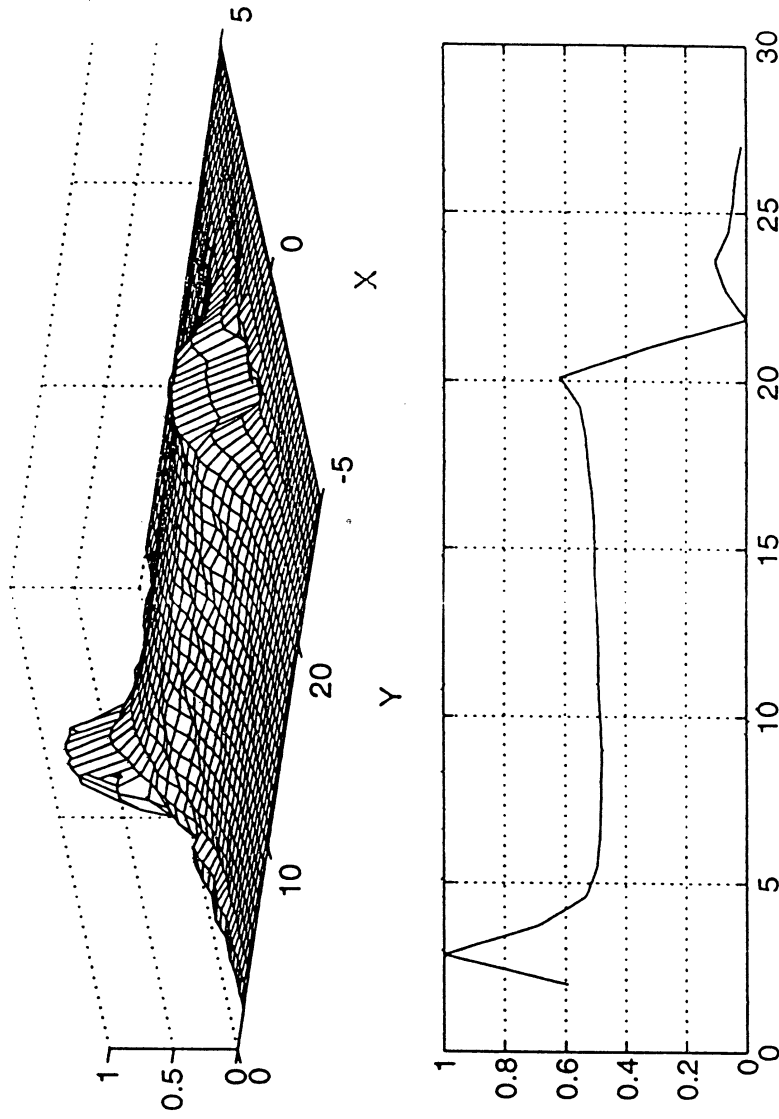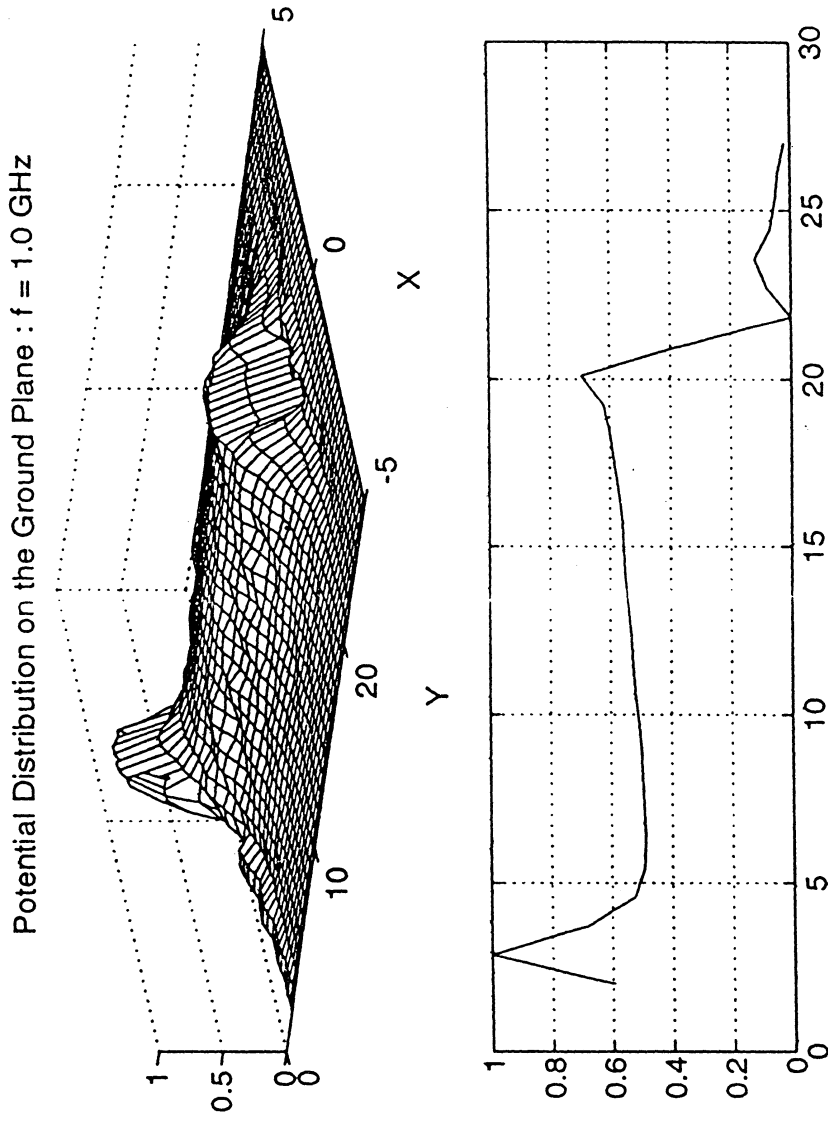
Figure 6 :   Current Distribution on the Ground Plane Around Via Hole at 10 GHz.
$W_0 = 2.3mm$, $W_1 = 1.15mm$, $W_2 = 2.875mm$, $H_1 = 1.0mm$, $H_2 = 2.0mm$, $\epsilon_1 = 3.4$, $\epsilon_2 = 1$

Potential Distribution on the Ground Plane : f = 0.5 GHz

Figure 7 :   Potential Distribution on the Ground Plane Around Via Hole at 0.5 GHz. The maximum correspond to 3.7×10^{-3} V. $W_0 = 2.3mm$, $W_1 = 1.15mm$, $W_2 = 2.875mm$, $H_1 = 1.0mm$, $H_2 = 2.0mm$, $\epsilon_1 = 3.4$, $\epsilon_2 = 1$
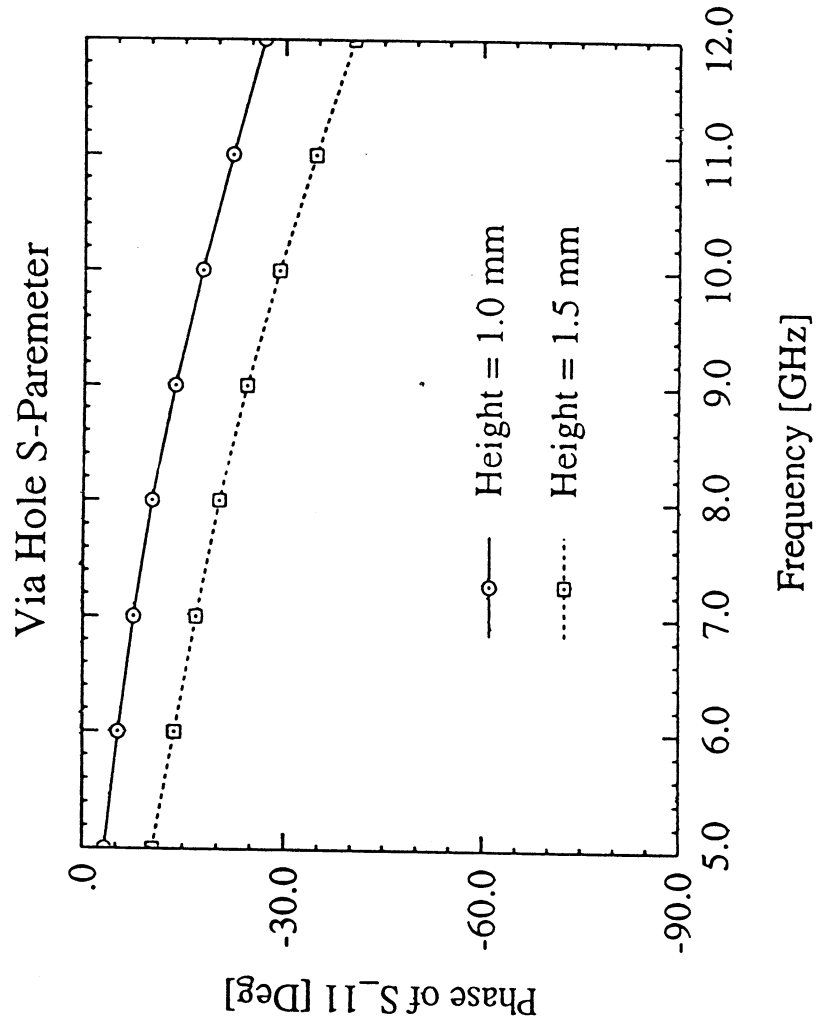
The University of Michigan / Finite Element Method

Potential Distribution on the Ground Plane : f = 1.0 GHz

Figure 8 : Potential Distribution on the Ground Plane Around Via Hole at 1.0 GHz. The maximum correspond to 3.7×10^{-3}V. $W_0 = 2.3$mm, $W_1 = 1.15$mm, $W_2 = 2.875$mm, $H_1 = 1.0$mm, $H_2 = 2.0$mm, $\epsilon_1 = 3.4$, $\epsilon_2 = 1$

Via Hole S-Paremeter

Figure 9 : Scattering Parameters of a Via Hole As a Function of Frequency. $W_0 = 2.3mm$, $W_1 = 1.15mm$, $W_2 = 2.875mm$, $\epsilon_1 = 3.4$, $\epsilon_2 = 1$.
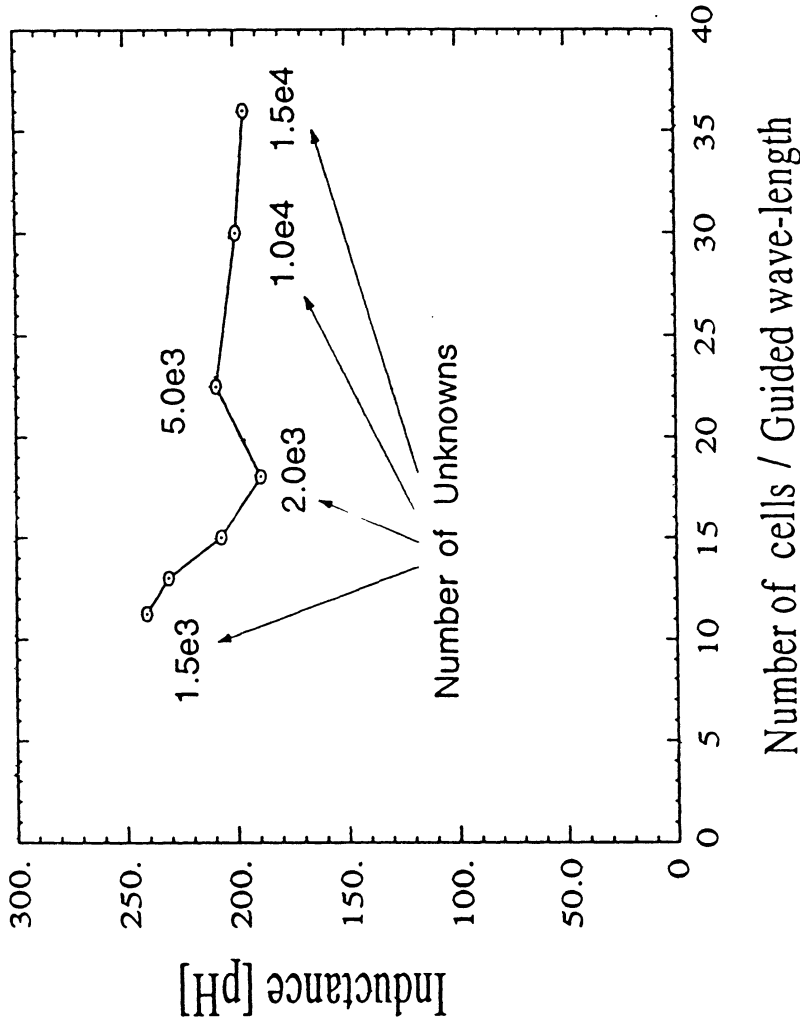
Via Inductance Convergence Test

Figure 10 :   Convergence of via hole inductance as a function of number of meshes per guided wavelength in dense medium. Frequency = 10 GHz, Height = 1.0 mm, W_0 = 2.3mm, W_1 = 1.15mm, W_2 = 2.875mm, ϵ_1 = 3.4, ϵ_2 = 1.
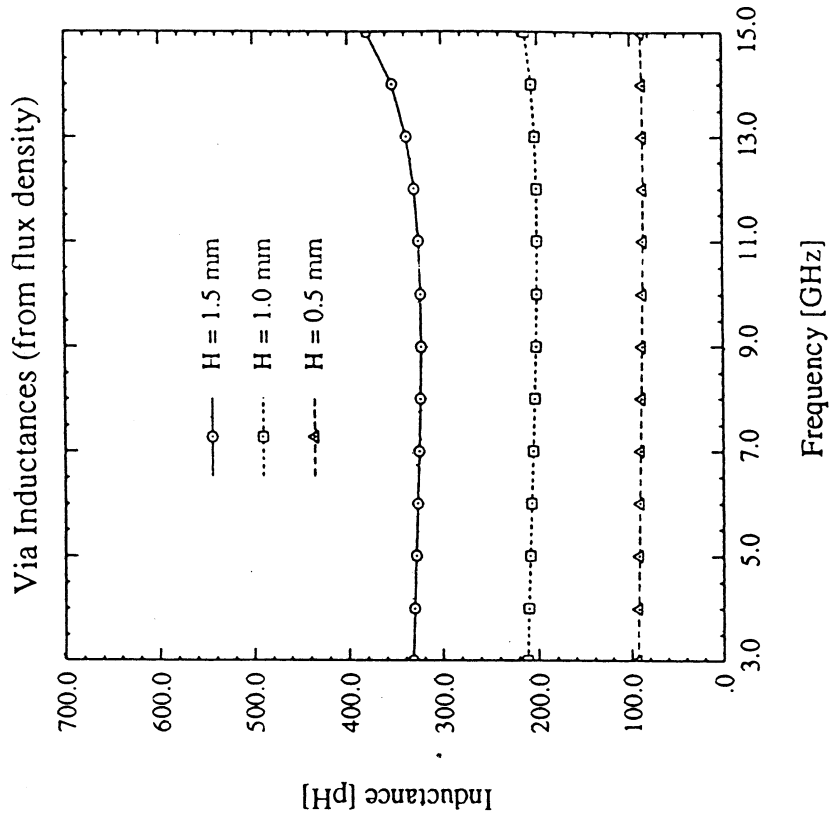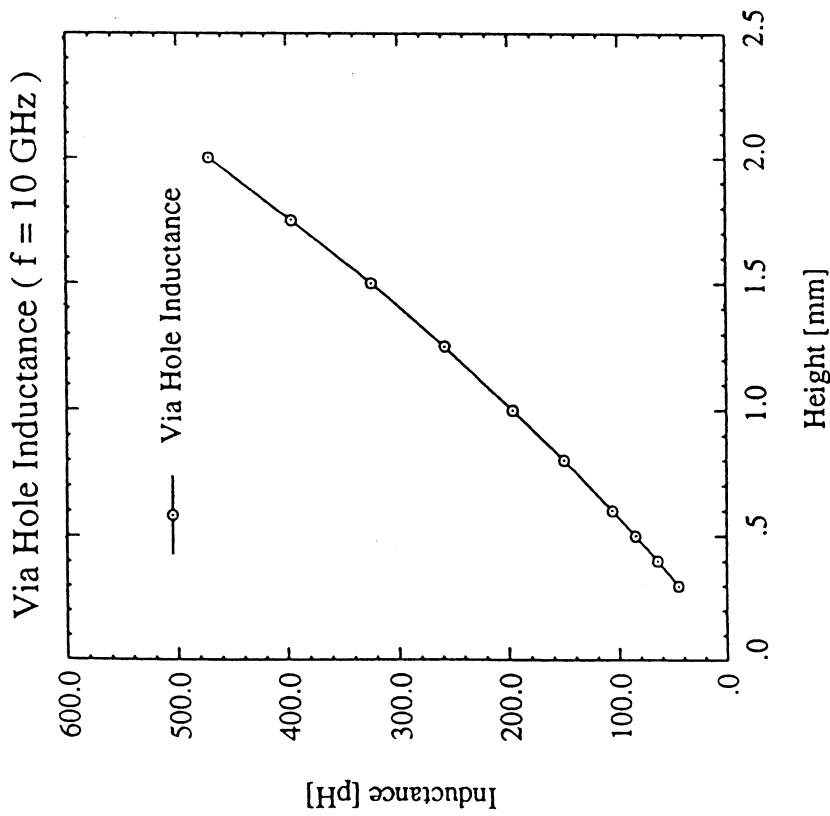
Figure 11 : $W_0 = 2.3$mm, $W_1 = 1.15$mm, $W_2 = 2.875$mm, $\epsilon_1 = 3.4$, $\epsilon_2 = 1$. (a)Inductance of a Via Hole As a Function of Via Hole Height at 10 GHz. (b)Inductance of a Via Hole As a Function of Frequency and Height.

Brief Summary

1. We reduced the number of unknowns using the topological symmetry.

2. The FEM results agree well with FDTD's.

3. Frequency dependent characterizations:

   - Phase of the reflection coefficient changes as frequency changes.

   - $|S_{11}|$ of 2-port via increases as frequency increases.

   - Via inductance depends upon frequency and geometrical factors. Actually, via hole inductance increases as height increase.

4. True ground position is different from the geometrical center of via hole

5. Capacitance of via hole considered in this study is negligibly small.