

**A SUBHARMONIC MIXING
ANTENNA FOR MILLIMETER-WAVE
RECEIVERS AND OSCILLATING
SLOT ANTENNAS FOR
QUASI-OPTICAL POWER
COMBINING**

by

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TO MY PARENTS

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When I began to look for a place to do experimental work in electromagnetics I was told that it was a dead area in this country and I should consider going to the Soviet Union. I would like to thank my advisor Gabriel M. Rebeiz who, for no apparent reason, decided to create a millimeter-wave group and has been remarkably successful.

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PREFACE

The thesis deals with two separate areas in millimeter-wave technology. First the design and characterization of a wideband subharmonic millimeter wave mixing antenna using back-to-back Schottky diodes is discussed. The mixing antenna results in state of the art performance as a subharmonic mixer at 90 GHz and 180 GHz. The mixing antenna is also used as a wideband $2N$ 'th harmonic mixer providing continuous coverage of the 26-260 GHz frequency range in a single low cost fixed tuned unit.

Next, a new transistor oscillator configuration directly coupled to a coplanar waveguide (CPW) fed slot antenna is introduced. This oscillator is particularly well suited to planar fabrication and high frequency operation. The high frequency capability of the oscillator is demonstrated with results for 155 GHz and 215 GHz monolithic oscillators using a sub $0.1 \mu\text{m}$ InP based high electron mobility transistor (HEMT). To our knowledge, these are the highest frequency three terminal millimeter-wave oscillators to date. The use of slot oscillators in quasi-optical power combining arrays is also demonstrated.

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CHAPTER I

INTRODUCTION

In the design of radio frequency equipment at higher and higher frequencies in the millimeter and submillimeter-wave region it becomes increasingly difficult to rely on traditional approaches. Microstrip or coplanar waveguide (CPW) transmission lines suffer from ohmic and dielectric losses [1, 2]. Waveguides with the small dimensions required above 100 GHz are difficult to machine and expensive. For this reason it is advantageous to examine the design of receiver front end mixers and transmitters that eliminate the need to propagate millimeter-wave signals through transmission lines or waveguides. This is done by placing a mixing or oscillating element directly on an efficient planar antenna [3].

1.1 Quasi-Optical Receivers

The only mixing element that can operate well into the terahertz region is the Schottky diode. Fundamental diode mixers require a certain amount of local oscillator (LO) power which may be difficult to generate at millimeter-wave frequencies. To simplify this problem it is possible to design harmonic mixers which use an LO signal at a frequency which is a submultiple of the radio frequency (RF) signal being downconverted. In general the mixing process becomes less efficient as the harmonic

number increases. If two diodes are used in an antiparallel (or back-to-back) configuration, there are two switching cycles per cycle of the LO signal. This effectively doubles the LO frequency [4, 5]. A subharmonic mixer with two back-to-back diodes can be designed with a conversion efficiency comparable to that of a single diode mixer operating in the fundamental mode. The LO source is easier to design because its frequency is lower, and the isolation between the RF and LO inputs becomes easier with the greater frequency separation. There is also some LO noise suppression in a subharmonic design as explained in [6].

The conventional approach to mixer design in the millimeter-wave region has been to mount a whisker contacted diode in a waveguide mixer block. Adjustable waveguide tuners are used to match the effective impedance of a reduced height waveguide to that of the diode and its whisker contact [7]. A subharmonic mixer at 205 GHz in waveguide with two whisker contacted diodes has been constructed by Carlson [8]. This resulted in a single sideband (SSB) receiver noise temperature of 1800 K. A 180 GHz mixer using two antiparallel whisker contacted diodes has also been reported by Mann [9] and a 140 GHz subharmonic mixer using a pair of beam lead diodes has been investigated [10] but these resulted in poorer performance than reported by Carlson.

Recently the University of Virginia developed a planar back-to-back diode chip suitable for millimeter wave applications. The diodes are well matched and exhibit a reduced parasitic capacitance due to the surface channel fabrication procedure [11]. A waveguide subharmonic mixer using this type of diode has been constructed at 210 GHz [12] resulting in a SSB receiver noise temperature of 1600 K. This represents the best room temperature subharmonic mixer ever built at this frequency. Unfortunately the mixer is complicated to build using two waveguides with different dimensions, 2

E-plane tuners, two backshorts, and a suspended stripline circuit. These types of waveguide designs become increasingly difficult to implement at higher frequencies.

Millimeter-wave antennas with mixing elements placed directly at the terminals can be designed without the need for a complex waveguide system and result in receivers with very small dimensions [13, 14, 15, 16, 17, 18, 19]. Mixing antennas of this type can be designed to work into the terahertz region without mechanical limits. A receiver based on this type of mixer can no longer have its conversion loss and noise temperature measured at a bounded wave input as in a waveguide or microstrip-line based mixer. The antenna and its radiation pattern into free space or its coupling to a gaussian beam quasi-optical system must be considered in the mixer characterization.

The first part of this thesis deals with the design construction and characterization of a high efficiency broadband subharmonic mixing antenna using a back-to-back Schottky diode chip fabricated by the University of Virginia. The mixing antenna operated in the subharmonic mode with quasi-optical injection of RF and LO has a double side band (DSB) conversion loss and noise temperature of 6.7 dB and 1080 K at 90 GHz, and 8.5 dB and 1820 K at 180 GHz. The mixing antenna was also built into a $2N^{\text{th}}$ harmonic mixer with a coaxial LO input at even submultiples of the RF. This resulted in a compact economical fixed tuned receiver capable of operation from 26-260 GHz.

1.2 Quasi-Optical Oscillators

All electron devices used to generate radio frequency power suffer from the effects of capacitance between their electrodes. As frequency increases the devices must be made smaller to reduce this interelectrode capacitance. This reduction in size also reduces the power handling capability for an individual device. Systems which combine

the output power from several devices are often used. In the millimeter and sub-millimeter wave range it has been recognized [20] that free space power combining from radiating elements can result in greater efficiency than waveguide or transmission line systems because of the high losses and mechanical difficulties encountered with these media at millimeter-wave frequencies. Quasi-optical oscillators consisting of active devices placed directly on radiating antenna elements have been demonstrated. These units are relatively easy to build and can be placed in arrays for power combining and beam shaping. Like quasi-optical receivers, oscillators that are directly coupled to antennas must be characterized with consideration of the antenna radiation pattern. Many research groups are actively involved in the development of quasi-optical power combining arrays of devices synchronized by either strong coupling or weak coupling between individual elements [21, 22, 23, 24, 25]. Active elements directly coupled to radiating structures have also been used to create quasi-optical phase shifters, multipliers, amplifiers, modulators, and switches [25, 26, 27, 28].

This thesis presents a new quasi-optical transistor CPW-fed slot-antenna oscillator that is particularly well suited for planar fabrication and high frequency operation. Two 20 GHz oscillators and a wideband 7 GHz voltage controlled oscillator (VCO) using commercially available devices are presented. A 37 GHz oscillator using a pseudomorphic heterojunction FET (HFET) developed at Chalmers University of Technology, Sweden is also presented. The high frequency capability of the design is demonstrated with the construction of monolithic 155 GHz and 215 GHz oscillators using a sub 0.1 μm InP based high electron mobility transistor (HEMT) developed by Hughes Malibu Research Laboratory. To our knowledge, these are the highest fundamental frequency oscillators achieved to date for a three terminal device. The use of the oscillating element in extendable power combining arrays is also demonstrated

with a two element array at 5.4 GHz and with a four element array at 20 GHz.

CHAPTER II

SUBHARMONIC MIXER RECEIVER

Millimeter-wave mixer receivers with quasi-optical RF and LO inputs can be built by integrating a mixing element directly at the terminals of a planar antenna. This results in a design which is much simpler than the corresponding waveguide implementation. This chapter describes the development of a subharmonic mixing antenna using an antiparallel (back-to-back) diode pair. Subharmonic mixers have several important advantages at millimeter-wave frequencies (see Chapter 1). To our knowledge, the first room temperature subharmonic mixing antenna has been described by Stephan et al. [13]. This receiver uses a bow-tie antenna on a thin dielectric substrate. We have improved the receiver design by combining a planar $1.3\mu\text{m}$ anode diameter back-to-back Schottky diode chip with a wideband log periodic antenna integrated on a high resistivity silicon wafer. The diode chip was fabricated at the University of Virginia. The log periodic antenna is placed at the back of a silicon lens to eliminate power loss to substrate modes and to render the pattern unidirectional. A polyethylene ($\epsilon_r = 2.3$) quarter-wave matching layer is used at the silicon-air interface to reduce the air-dielectric reflection loss [29]. The LO signal is injected quasi-optically, and the log-periodic antenna catches both the RF and LO signals. An optional matching network can be integrated at the antenna apex for better RF

power transfer into the diode pair [30]. The design can be easily implemented with a spiral antenna if a circular polarization is desired. The upper frequency is only limited by the diode design and not the RF coupling (i.e. antenna, and matching networks), and the University of Virginia and the University of Michigan are currently fabricating high quality planar $0.5\mu\text{m}$ diodes for 600-800 GHz applications. The planar subharmonic receiver is compatible with the fabrication procedure of the back-to-back diode making this approach fully monolithic. This results in an inexpensive receiver suitable for submillimeter-wave imaging arrays.

2.1 Antenna-Lens Design and Measurement

The antenna is a planar self-complementary log-periodic antenna [31] with $\sigma = 0.707$ and $\tau = 0.5$ designed to cover the 26 to 260 GHz band (Fig. 2.1). The

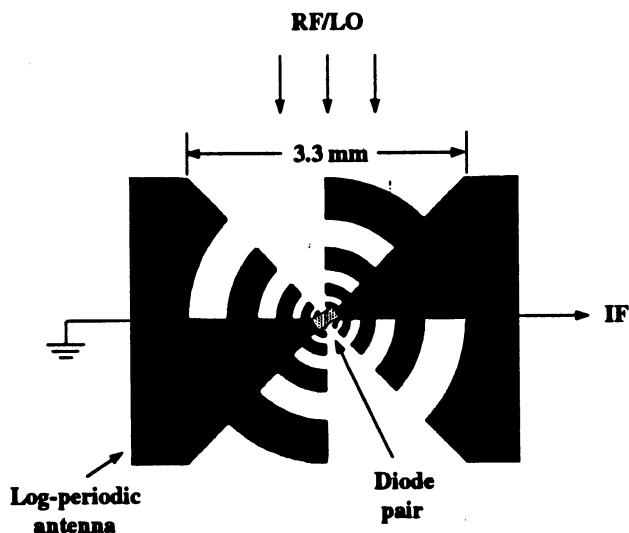


Figure 2.1: 26-260 GHz planar log-periodic antenna with $\sigma = 0.707$ and $\tau = 0.5$.

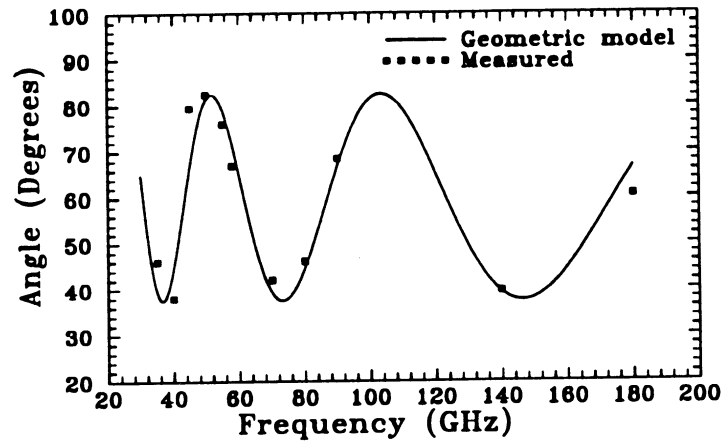
values of σ, τ yield a wideband antenna that maps onto itself every octave. This is advantageous since the LO and RF frequencies are approximately one octave apart. The log-periodic antenna is placed on the back of a silicon lens to eliminate power loss to substrate modes [32]. The dielectric lens also enhances the pattern in the direction

of the dielectric and increases the gain. The antenna input impedance is independent of frequency, and is related to the dielectric constant by:

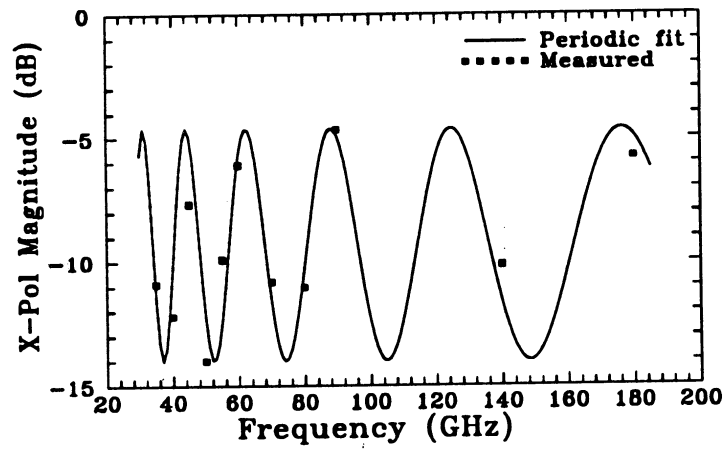
$$Z_{ant} = \frac{189\Omega}{\sqrt{0.5(1 + \epsilon_r)}} \quad (2.1)$$

where 189Ω is the impedance of any self-complementary structure in free-space, and ϵ_r is the relative dielectric constant of Silicon. This yields an impedance of 74Ω for a log-periodic antenna on a Silicon lens ($\epsilon_r = 11.7$). As will be seen later, this impedance does not introduce a large mismatch between the antenna and the back-to-back Schottky-diodes. The log-periodic antenna is linearly polarized but shows a considerable cross-polarization component in the E-and H-planes ranging from -5dB to -14dB depending on the frequency. The polarization direction of the log-periodic antenna was measured from 35 GHz to 180 GHz and found to vary by $\pm 22.5^\circ$ with the period given by the teeth geometry (Fig. 2.2). The measured polarization direction fits the model that the strongest radiation results from the portion of the teeth that is $\lambda_m/4$ long, where λ_m is the wavelength calculated using the mean dielectric constant between silicon and air ($\epsilon_m = (1 + \epsilon_r)/2$). The radiation mechanism alternates between the left and right teeth resulting in the $\pm 22.5^\circ$ polarization-direction change. The cross-polarization magnitude measurements also support this model, being low (-14dB) when the log-periodic antenna is radiating from the center of a tooth and high (-5dB) when the log periodic antenna is radiating from both left and right teeth during the transition which occurs just past the $\lambda_m/4$ center frequency for a tooth (Fig. 2.2).

It is also possible to use a self-complementary logarithmic spiral antenna [33] to yield a circularly polarized pattern. In this case, the cross-polarized component is very low (≤ -20 dB) at all frequencies of operation [30]. However, the spiral antenna will exhibit a 3 dB polarization mismatch loss when coupling to a linearly polarized



(a)



(b)

Figure 2.2: Measured polarization angle (a) and cross-pol magnitude (b) versus frequency for the log-periodic antenna on the substrate lens.

wave.

The log-periodic antenna is placed on an extended hemispherical silicon lens shown in Fig. 2.3. More precisely, the log-periodic antenna is $2220\mu\text{m}$ behind the center of a 0.68cm -radius hemispherical silicon lens. The spacing wafers with a total thickness of $1070\mu\text{m}$ consist of high resistivity silicon substrates ($> 2000\Omega - \text{cm}$). This

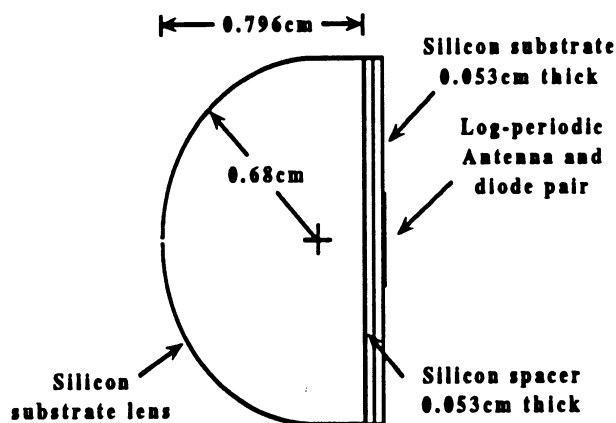


Figure 2.3: The extended hemispherical substrate lens.

configuration was chosen after a ray-optics based calculation by Filipovic et al. on the gaussian-coupling and directivity properties of hyperhemispherical and extended hyperhemispherical lenses [34]. The calculations were performed for double-slot and double-dipole antennas with symmetric patterns and it was found that a position between 2200 and $2400\mu\text{m}$ yields good high gain patterns and good gaussian coupling efficiencies (90%) in the frequency range from 100 to 500GHz . It is important to note that the hyperhemispherical position of $2000\mu\text{m}$ yields an even higher theoretical coupling efficiency (97%) but at the expense of lower gain and therefore lower f-number imaging systems. The position of $2220\mu\text{m}$ is seen as a compromise between high gain patterns needed for large f-number quasi-optical systems and a small reduction in the gaussian-coupling efficiency. The log-periodic antenna was, of course, not analyzed in [34]. However, a $2220\mu\text{m}$ position is chosen for the subharmonic mixer and, as will

be seen later, resulted in good patterns and gaussian-coupling efficiencies.

Figure 2.4 shows the measured E and H-plane patterns of the log-periodic antenna at 40 GHz, 90 GHz, 180 GHz and 250 GHz placed at the $2220\mu\text{m}$ position. The 45° -plane patterns are very similar to the E-plane patterns and are not shown. The cross-polarization pattern is very similar to the co-polarized pattern but with a -5dB to -14dB peak depending on the frequency. Only a small amount of power radiates from the back side of the substrate lens. The back side patterns (not shown) are wider with a peak power about 20dB lower than the front side patterns. The matching gaussian beams at 90 GHz and 180 GHz are discussed in the mixer measurement section. If the log-periodic antenna is placed at a position of $2750\mu\text{m}$ behind the hemispherical center, an elliptical lens is closely approximated. Patterns with lower sidelobes are achieved at 180 GHz and 250 GHz in this position (see Chapter 3) but at the expense of lower gaussian coupling efficiency (see [34]). It is important to note that the log-periodic antenna pattern inside the dielectric substrate lens is frequency independent but the lens acts as a circular aperture of approximately constant dimension resulting in a narrowing of the far-field patterns as frequency increases.

2.2 Diode Characteristics and RF Measurements

The GaAs anti-parallel Schottky-diode chip, shown in Fig. 2.5, is an SR2T1 type developed and fabricated at the University of Virginia. The chip is $250\mu\text{m}$ long and $125\mu\text{m}$ wide. The anode and cathode contact pads are $100\mu\text{m}$ long and $125\mu\text{m}$ wide. The finger length is $50\mu\text{m}$ with a thickness of $2\mu\text{m}$ and width of $3.5\mu\text{m}$. A surface channel technology has been used to eliminate the conducting path between the anode and cathode pads [35] and to reduce the parasitic capacitance between the anode and cathode. The parasitic capacitance is further minimized by thinning the GaAs wafer

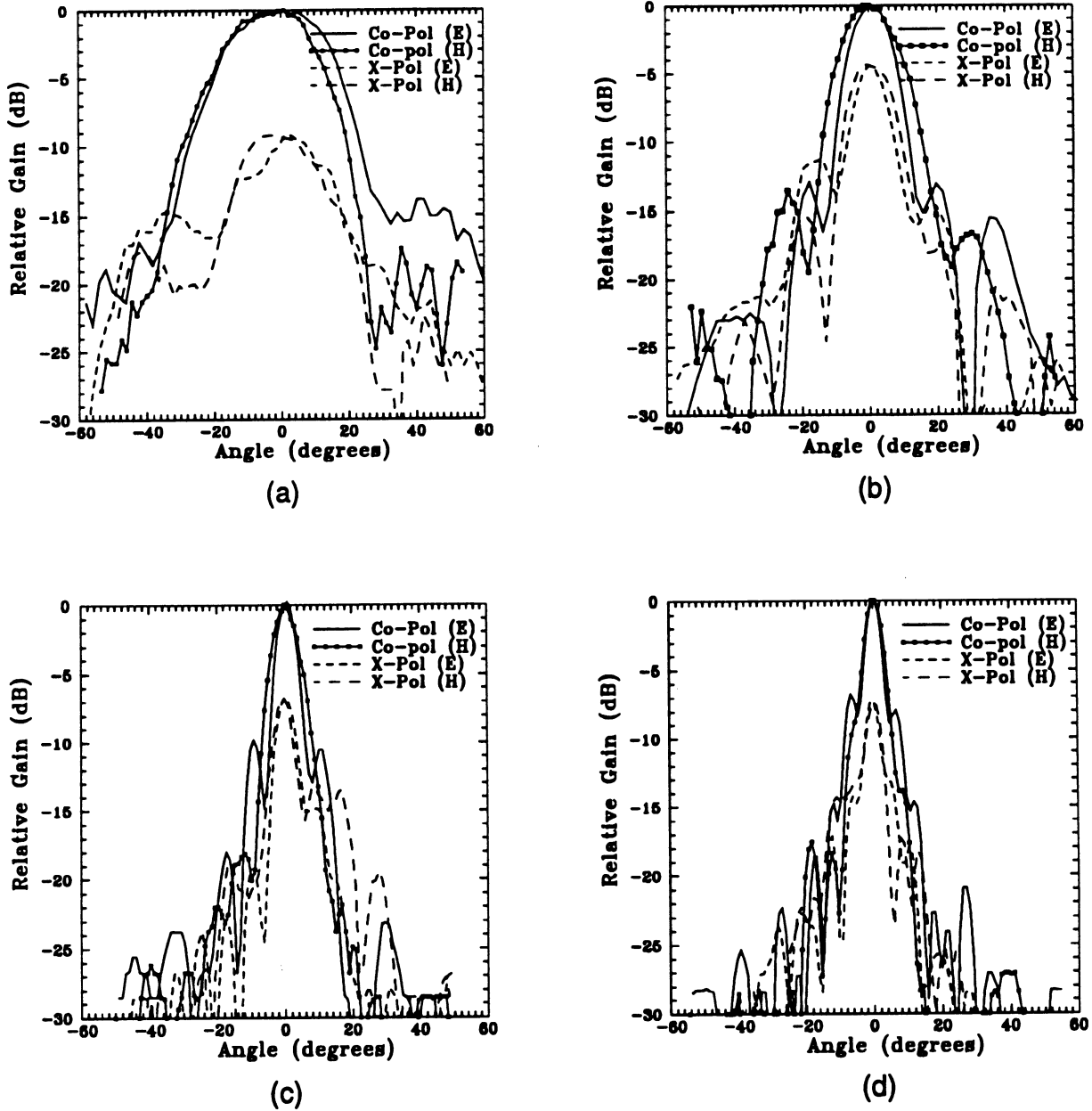


Figure 2.4: Measured radiation patterns for the log-periodic antenna on the extended hemispherical substrate lens (2220 μ m position) at 40 GHz (a), 90 GHz (b), 180 GHz (b), and 250 GHz (d).

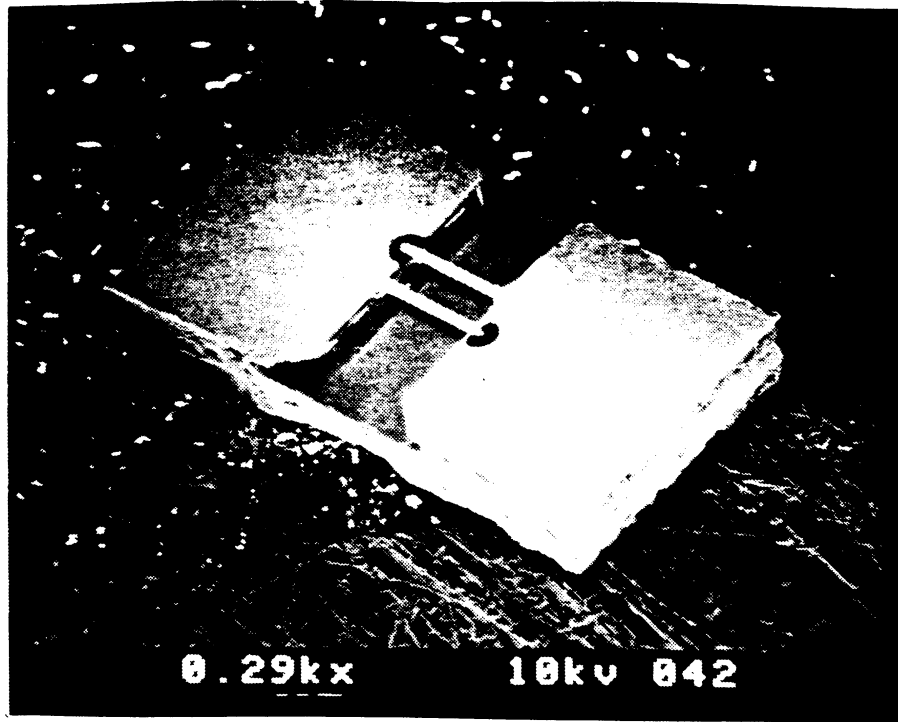


Figure 2.5: SEM picture of the surface channel back-to-back diode chip before GaAs substrate thinning.

to $7\mu\text{m}$ and placing it on a quartz substrate for mechanical rigidity considerations. Details of the fabrication procedure and the substrate thinning technique are presented in [36]. The diode chip is then bonded to the antenna apex using EPO-TEK H20-E silver epoxy [37] (see Fig. 2.6). The quartz substrate can be removed after the chip is bonded in place by simply dissolving the adhesive [36] between the GaAs chip and the quartz substrate. However, in this work, the quartz substrate was kept attached to the diode. The diodes consist of 900\AA n^- layer doped at $2 \times 10^{17}/\text{cm}^3$ backed by a $5\mu\text{m}$ n^+ layer doped at $3 \times 10^{18}/\text{cm}^3$. The diodes have an average anode diameter of $1.3\mu\text{m}$, a measured DC series resistance of 11Ω and a zero-bias junction capacitance of 4fF . The diodes are very similar with an ideality factor $n = 1.2$, a barrier height of 0.85V and a turn on voltage of 0.7V at $1\mu\text{A}$ (see Table 2.1). The total parasitic capacitance for the quartz-supported diode is estimated at $3\text{-}4\text{fF}$, thereby yielding a figure-of-merit cutoff frequency of approximately 2 THz .



Figure 2.6: Photograph of the diode chip bonded to the apex of the planar log-periodic antenna.

Diode SR2T1	Anod dia. (μm)	C_{j0} (fF)	C_p (fF)	I_s (Amps)	Ideality factor	R_s (Ω)	ϕ_{bi} (Volts)
Junction 1	1.3	4	3	8.9×10^{-17}	1.20	10.8	0.84
Junction 2	1.3	4	3	1.9×10^{-17}	1.14	11.4	0.88

Table 2.1: Measured capacitance and DC parameters for both junctions on the back-to-back diode chip.

Video detection measurements were done at 90 GHz and 180 GHz by applying a DC voltage to forward bias one of the diode junctions while reverse biasing the other. A plane wave with a known power density is shined on the log-periodic substrate-lens antenna and the output detected voltage in a $106\text{ K}\Omega$ load is measured with a lock-in amplifier. An additional spacer wafer was used in this measurement to synthesize an approximately elliptical substrate lens ($2750\ \mu\text{m}$ position) to increase the directivity and improve the coupling to a plane wave (see Chapter 3). The RF plane-wave is calibrated to $\pm 5\%$ using an Anritsu power meter at 90 GHz and a large-area bolometer at 180 GHz [38]. The video responsivity is defined here as the ratio of the detected low-frequency voltage across a $106\text{ K}\Omega$ load divided by the RF power available at the *terminals* of the log-periodic antenna. This definition eliminates the effect of the planar antenna and results in an RF source with a constant impedance of 74Ω at 90 GHz and 180 GHz. The available power, P_{av} , at the antenna terminals is given by:

$$P_{av} = SA_e\Gamma_l\alpha_s \quad (2.2)$$

where S is the incident power density, Γ_l is the loss at the silicon-air interface calculated using simple transmission-line analysis to be 1.5 dB and α_s is the dielectric loss in the $1000\ \Omega\text{-cm}$ silicon lens estimated to be 0.5 dB [39]. A_e is the effective aperture of the log-periodic substrate-lens antenna calculated from the measured directivity,

D_a , using the formula [40] $A_e = (\lambda^2/4\pi)D_a$ where:

$$D_a = \frac{4\pi U_{max}}{\iint_{\Omega} U(\theta, \phi) d\Omega} \quad (2.3)$$

and U is the radiation intensity (W/unit solid angle). The directivity is calculated from full-two dimensional measurements of the co-polarized and cross-polarized patterns with a signal-to-noise ratio of better than 40 dB. The measured power radiated to the back side of the lens is about 20 dB below the front side peak. The resulting co-polarized directivity values (in the 2750 μ m position) are 20.6 dB at 90 GHz and 25.2 dB at 180 GHz. The aperture efficiency is given by $\eta_{ap} = A_e/A_{phys}$ where A_{phys} is the physical area of the 0.68 cm radius silicon lens. The corresponding values are 70% at 90 GHz and 51% at 180 GHz.

The measured and theoretical video responsivity [14, 41] at 90 and 180 GHz are shown in Fig. 2.7. The peak diode signal voltages in the experiment were 5.0 mV at 90 GHz and 2.6 mV at 180 GHz. This is in the unsaturated square law operating region with detected voltage directly proportional to input power. The diode parameters used in the theoretical model are a series resistance of 11 Ω , a zero-bias junction capacitance of 4fF, an ideality factor of 1.2 and a barrier height of 0.85V. The model has one free parameter, the parasitic capacitance, chosen to be 3fF. The anode finger inductance is estimated to be small enough to neglect. The peak video responsivity referenced to a 75 Ω source is 2600 V/W at 90 GHz and 1100 V/W at 180 GHz and is competitive with whisker diodes at these frequencies. The model fits the measurements at 90 GHz and 180 GHz without changing any of the diode parameters between the two frequencies. Since the absolute power density is known to $\pm 5\%$ and the estimated error in the antenna directivity is $\pm 5\%$, the parasitic capacitance estimate from video responsivity measurements is accurate to about $2fF$. The results are in approximate agreement with the total diode capacitance measurements made

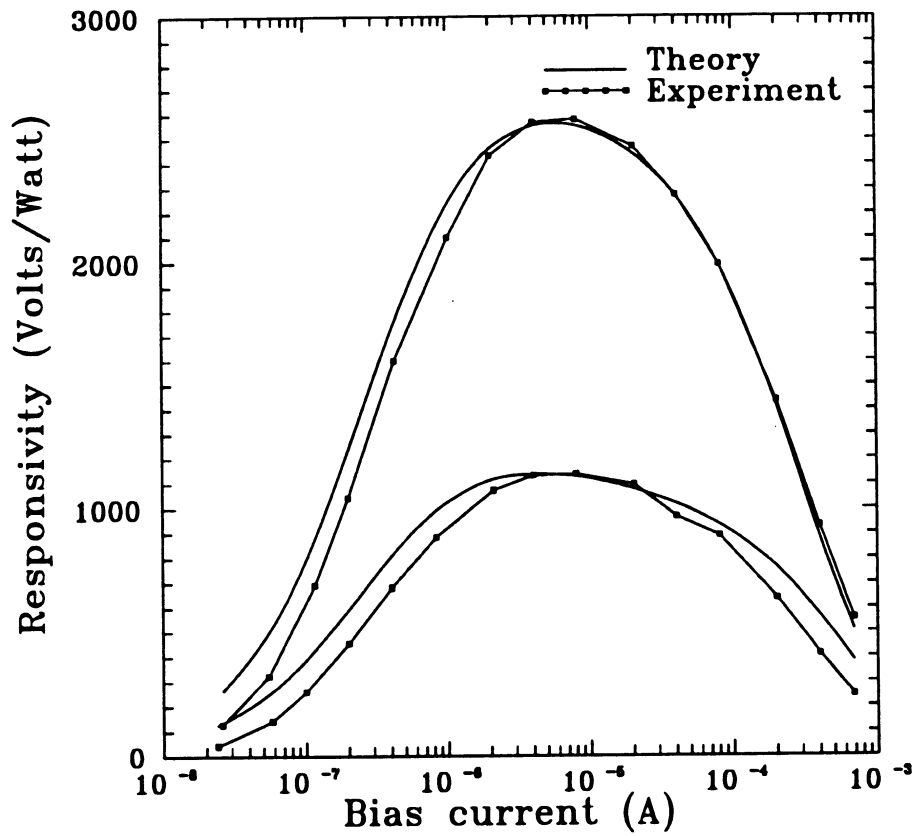


Figure 2.7: Measured video responsivity versus bias current for the diodes at 90 GHz (2600V/W peak) and 180 GHz (1100V/W peak).

with an LCR meter at the University of Virginia and confirm that the substrate thinning procedure has resulted in a lower parasitic capacitance.

The system video responsivity of the diode defined as the detected voltage per unit plane wave power incident on the entire lens area can be expressed as:

$$R_{sys} = R_{75\Omega} \Gamma_1 \alpha_s \eta_{ap} \quad (2.4)$$

where $R_{75\Omega}$ is the video responsivity given above for a 75Ω source. The values of R_{sys} are 1150 V/W at 90 GHz and 350 V/W at 180 GHz.

2.3 Mixer Modeling and Measurements

2.3.1 Nonlinear Analysis

A subharmonic mixer consisting of two antiparallel (or back-to-back) diodes effectively doubles the LO frequency. This configuration has several advantages at millimeter wave frequencies and the conversion efficiency is comparable to that of a single diode mixer operating in the fundamental mode (Chapter 1). A program was written for the nonlinear analysis of subharmonic mixers (see Appendix A). The program is based on the reflection algorithm developed by Kerr et al. [42] and takes into account the asymmetrical I-V curve of the back-to-back diodes. This is done by splitting the antiparallel diodes into two equivalent single diodes with LO terminating impedances set to zero for even harmonics and DC [43]. The higher order terminating impedances at $3f_{LO}$, $5f_{LO}$ and $7f_{LO}$ are taken to be the wideband antenna impedance of 74Ω in parallel with the 3fF parasitic capacitance of the diode. All impedances at higher harmonics are assumed to be short-circuited. The analysis was done for the conversion loss only and the results for a 90 GHz RF and a 182 GHz RF are summarized in Table 2.2.

F_{LO} (GHz)	F_{RF} (GHz)	Available LO power (mW)	RF Impedance (Ω)	LO Impedance (Ω)	IF Impedance (Ω)	Conversion Loss (SSB) (dB)
45	90	5.0	42 - j71	72 - j284	154	8.0
-	-	6.6	44 - j48	91 - j226	98	7.6
-	-	8.0	44 - j35	93 - j193	75	8.3
91	182	6.0	17 - j40	20 - j142	140	10.3
-	-	7.6	18 - j37	24 - j133	108	9.6
-	-	9.0	21 - j34	27 - j123	84	9.8

Table 2.2: Results from non-linear analysis for the subharmonic mixer (LO and RF embedding impedances are 74Ω in parallel with the $3fF$ parasitic capacitance, IF load impedance is 110Ω).

The analysis indicates that a single-sideband (SSB) conversion loss of 7.6 dB and 9.6 dB are attainable at 90 GHz and 182 GHz, respectively, without an RF matching network. The available LO power required at the antenna apex is 6.6 mW at 45 GHz and 7.6 mW at 91 GHz. Forward bias cannot be applied to both diodes simultaneously in this design so zero bias operation is required. This results in the relatively high LO power requirement. The corresponding RF, LO and IF impedances are shown in Table 2.2 and result in an LO mismatch of 1.6 dB at 45 GHz and 2.8 dB at 91 GHz. It is possible to improve the conversion loss by 1 dB at 90 GHz or 2.7 dB at 182 GHz with an RF matching network at the apex of the antenna at a penalty of reduction in bandwidth.

2.3.2 Quasi-Optical System and Receiver Setup

The double side band (DSB) conversion loss and noise temperature were measured with the hot-cold load (Y-factor) technique. The quasi-optical measurement setup is shown in Fig. 2.8.

A dichroic plate was not available for this experiment and a Martin-Pupplet diplexer [44] was used to inject the local oscillator to the subharmonic mixer. The

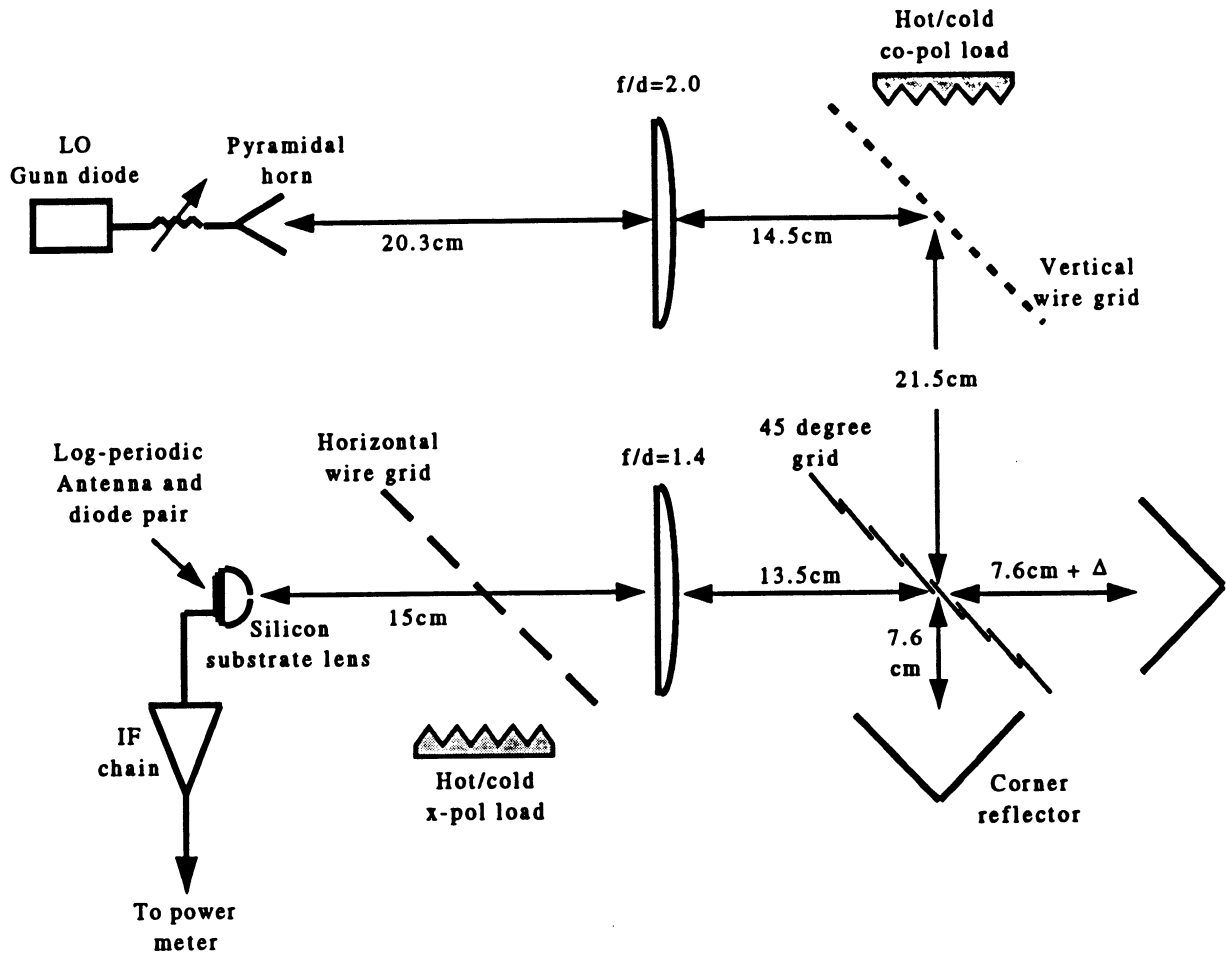
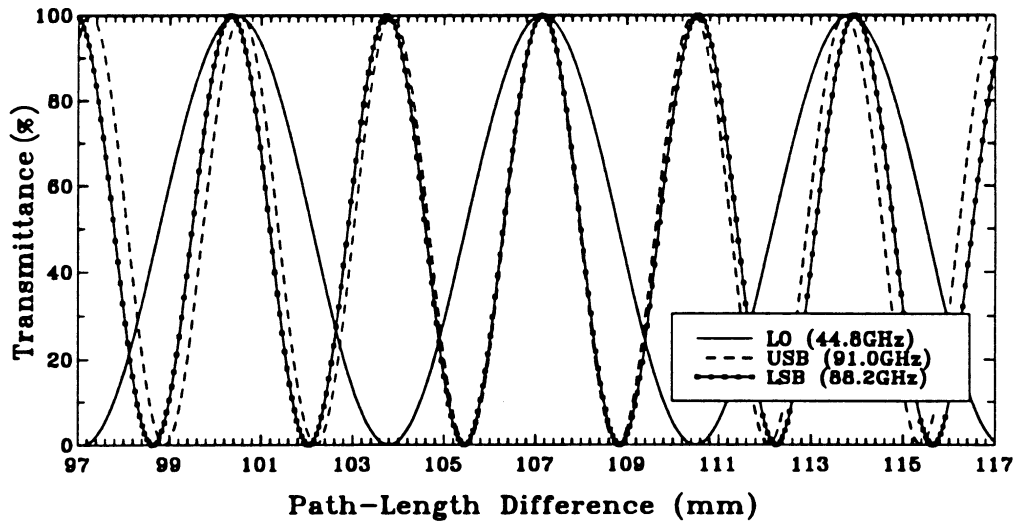


Figure 2.8: Quasi-optical setup for measuring DSB conversion loss and noise temperature.

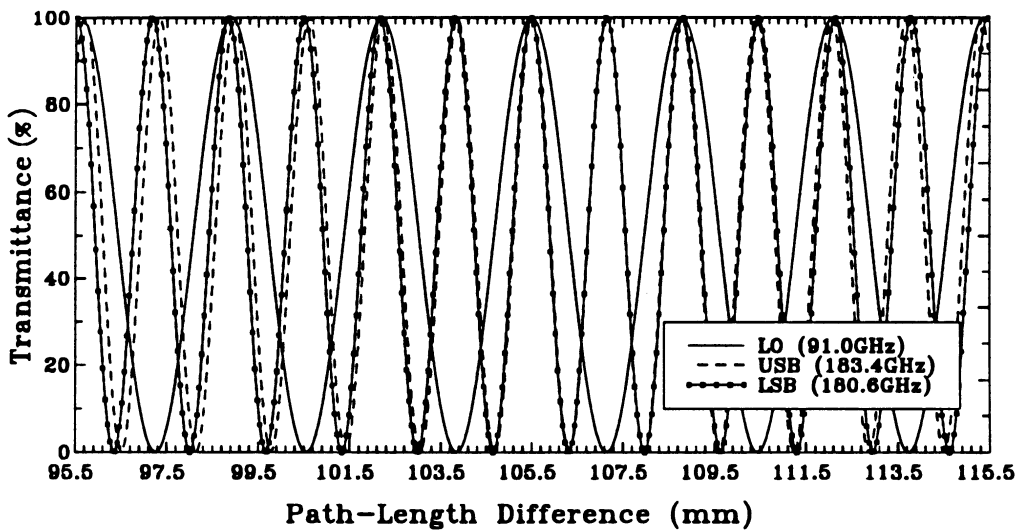
Martin-Pupplett uses polarization grids and its response is therefore independent of frequency. It can be configured to pass the LO signals from the LO port and the upper and lower sideband RF signals at approximately twice the LO frequency from the RF port (Fig. 2.9). At the optimum path length difference (2Δ) of 107.14 mm at 90 GHz and 105.4945 mm at 180 GHz, the RF bandwidth for a maximum insertion loss of 0.2 dB at the upper and lower sidebands is 380 MHz. The Martin-Pupplett also passes the upper and lower sidebands of the LO signal from the RF port. Therefore, one must be careful that fundamental mixing is not occurring at the diode terminals. This is achieved by using well balanced back-to-back diodes that inherently eliminate the fundamental mixing mechanism. The back-to-back diode DC current in the outside loop was around $80 \mu\text{A}$ for an estimated available 45 GHz LO power of 9 mW at the diode terminals. This is about 20-30 times smaller than what is expected from a single diode at comparable available LO power and is an indication that the back-to-back diodes are well balanced and suppressing fundamental mixing.

The quasi-optical measurement setup provides a two lens system for coupling the LO signal from the Gunn source to the mixer. The RF signal is coupled to the hot-cold load through only the f-number 1.4 objective lens. The two lens system optimizes power transfer for the LO signal at 91 GHz. This is done by transforming the gaussian beamwaist radius (W_0) of the pyramidal LO horn to match the gaussian parameters of the log-periodic substrate-lens antenna. LO coupling at 45 GHz is less of a concern since there is an excess of available power from the source. The minimum beamwaist radius (W_0) for any given antenna can be estimated from the asymptotic beam radius growth angle (Θ_{W_0}) which is given by one half of the -8.7 dB beamwidth of the far field pattern:

$$\Theta_{W_0} = \lambda/\pi W_0 \quad (2.5)$$



(a)



(b)

Figure 2.9: Theoretical power transfer function for the Martin-Pupplet polarization rotating diplexer at 90 GHz (a) and 180 GHz (b). Path length difference = 2Δ (107.14 mm optimum at 90 GHz, 105.4945 mm optimum at 180 GHz).

For an aperture limited pyramidal horn with symmetric E and H plane patterns, The beamwaist is given approximately by:

$$W_0 = (\lambda/2\pi)10^{G(dB)/20} \quad (2.6)$$

where

$$G(dB) = 10\log 4.45 A_{E\lambda} A_{H\lambda} \quad (2.7)$$

and $A_{E\lambda}$, $A_{H\lambda}$ are the E- and H-plane aperture dimensions in wavelengths [44]. The 91 GHz LO horn has an approximate beamwaist radius of 8.3 mm at its phase center. The beamwaist calculated from the measured pattern of the log-periodic substrate-lens antenna at 90 GHz in the $2220\mu\text{m}$ position is 5.13 mm. There is also a radius of constant phase curvature (R) for antennas on non-elliptical substrate lenses. Filipovic [34] calculates the value of this radius to be -65 mm for double slot antennas at the $2200\mu\text{m}$ position. The two lens system transforms the gaussian parameters of the pyramidal LO horn to those of the log-periodic substrate-lens antenna. The pertinent dimensions in the quasi-optical system are indicated in Fig. 2.8. These dimensions, however, also reflect the results of some empirical adjustment and mechanical limits imposed by the large physical size of the diplexer. The system in Fig. 2.8 also guarantees that the fundamental gaussian beams for the log-periodic substrate-lens antenna at the RF frequencies are coupled without attenuation to the hot/cold load.

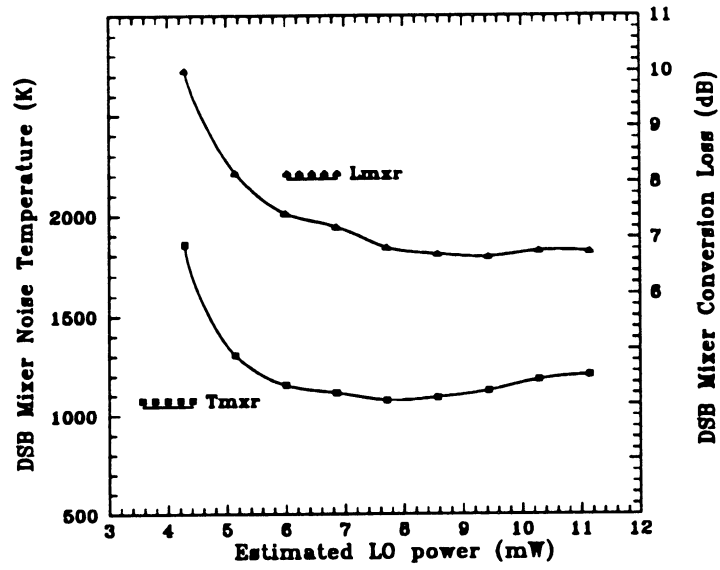
The diffraction loss in the Martin-Pupplett diplexer is estimated to be 0.2 dB. The lenses are 10 cm diameter Rexolite with estimated total reflection and dielectric losses of 0.6 dB at 90 GHz and 0.8 dB at 182 GHz. These are taken out of the measurements for the noise figure and conversion loss. A horizontal polarization grid is placed at 45° in front of the log-periodic/silicon lens antenna to reflect the cross-polarization component into a hot-cold load. In this configuration, both the co-polarized and

cross-polarized components contribute to the RF signal. This measurement method simulates a dichroic plate which can be designed to pass both RF polarizations. The hot-cold load is an Eccosorb AN-72 and the cold temperature is estimated to be 85 K at millimeter-wave frequencies [17]. Quarter wavelength polyethylene matching cap layers ($\epsilon_r = 2.33$) were used at 90 GHz RF and 182 GHz RF and improved the noise temperature and conversion loss by 0.6 dB. This was lower than the expected value of 1.2 dB due to the difficulties encountered in molding the thin spherical plastic lens covers.

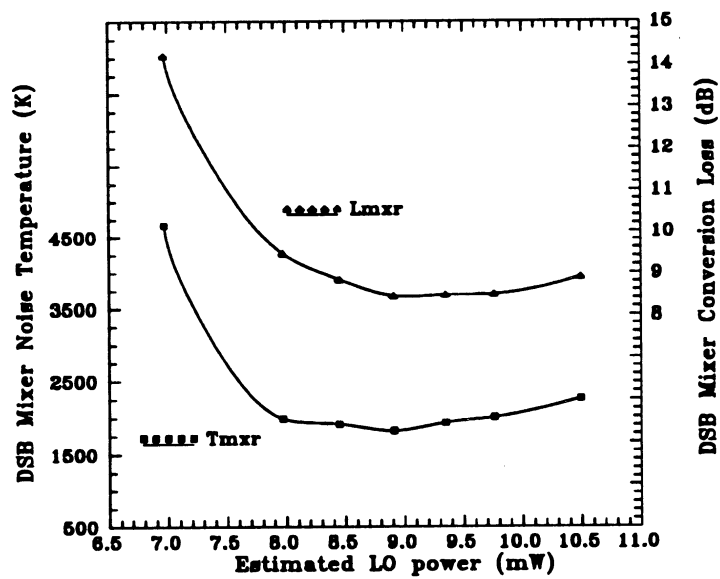
The available LO power at the diode terminals is estimated by measuring the total radiated power at 45 GHz and 91 GHz and then normalizing out the dielectric reflection and absorption loss in the two lens system, the dielectric reflection and absorption loss in the silicon lens and the gaussian coupling efficiency of the pyramidal LO horn (estimated to be 60%) and the gaussian coupling efficiency of the log-periodic antenna on the silicon lens (estimated to be 60% including the cross-pol. loss which affects the LO path). The IF chain consists of a 10 dB coupler, a bias-T to measure the outside DC current, a circulator, a low-noise amplifier chain, a 100 MHz bandpass filter centered at 1.4 GHz and a calibrated IF power meter. The 10 dB coupler is used to measure the IF reflection coefficient and is removed for standard receiver measurements. The IF chain has a gain of 98.5 dB and a 96 K noise temperature without the 10 dB coupler.

2.3.3 90 GHz and 182 GHz Measurements

The measured double-sideband conversion loss and noise temperature at 90 GHz and 182 GHz versus available LO power at the diode terminals are shown in Figure 2.10. The conversion loss and noise temperature are referenced to a hypothetical plane



(a)



(b)

Figure 2.10: Measured conversion loss and noise temperature at 90 GHz (a) and 182 GHz (b) versus estimated LO power available at the antenna terminals.

in front of the log-periodic/silicon lens antenna and include the gaussian coupling efficiency (estimated to be around -0.7 dB), the residual reflection loss at the silicon lens surface (-0.9 dB), absorption loss in the silicon lens (-0.5 dB), the diode intrinsic conversion loss, the mismatch between the log-periodic antenna and the back-to-back diodes and the IF mismatch at 1.4 GHz. The gaussian coupling efficiency includes the power lost to side lobes and back side radiation. Cross-polarized components do not affect the gaussian coupling efficiency in the RF path since they are reflected directly to a hot-cold absorber which couples to all possible modes. A minimum DSB conversion loss of 6.7 dB at 90 GHz and 8.5 dB at 182 GHz is attained at an available LO power of about 9 mW (Fig. 2.10). The measured DSB conversion loss can be related to the SSB nonlinear analysis by increasing the measured results by 3 dB and subtracting the total loss associated with the antenna gaussian coupling efficiency (0.7 dB) and the silicon lens reflection and absorption (1.4 dB). The effective SSB equivalent of the measured conversion loss in a 74Ω system would be 7.7 dB at 90 GHz and 9.4 dB at 180 GHz. These are in close agreement with the theoretical values of 7.6 dB and 9.6 dB (Table 2.2). At 182 GHz the minimum DSB noise temperature of 1820 K is attained simultaneously with the minimum conversion loss. At 90 GHz a minimum DSB noise temperature of 1070 K is measured experimentally at a lower LO power of 8 mW. At both frequencies the IF impedance is experimentally determined to be about 110Ω using an IF power reflection measurement. A microstrip matching network is used to reduce the IF reflection coefficient to less than 0.1 dB for minimum noise-temperature measurements. The noise temperature and conversion loss were about 2 dB higher if the cross-polarization component was not cooled, but terminated in a room temperature absorber. This shows that a significant fraction of the power is in the cross-polarized component and that it should not be ignored

when using a log-periodic antenna on a dielectric lens for receiver measurements.

The same back-to-back diode chip has been used by Siegel [12] in a waveguide system with an E-plane tuner and adjustable backshort to provide some impedance matching. At 205 GHz this system exhibited the best room temperature performance to date resulting in a SSB noise temperature of 1600 K and a conversion loss of 8.7 dB. Our effective SSB conversion loss in a 74Ω system at 180 GHz (9.4 dB) compares well with the result from the waveguide system since the theoretical RF impedance of the diode indicates that the mismatch to the 74Ω antenna may be as high as 2.7 dB.

CHAPTER III

26-260 GHz 2N'th HARMONIC MIXER RECEIVER

A wideband millimeter-wave harmonic mixer-receiver has been developed using a the log-periodic antenna and back-to-back Schottky-diode chip described in Chapter 2 and microwave circuit design. The receiver is planar, fixed tuned, very simple to build and yields excellent performance from 26-260 GHz. The harmonic mixer consists of a back-to-back Schottky diode chip placed at the apex of a wideband log-periodic antenna (Fig. 3.1). The harmonic mixer is quasi-optical and the RF energy is coupled via an integrated antenna on a substrate lens and not through a guided transmission-line structure.

Most millimeter-wave harmonic mixers consist of a Schottky-diode mounted in an E-plane waveguide circuit with an associated LO/IF diplexer. They have limited bandwidth covering only a single waveguide band, and are expensive to build for frequencies above 110 GHz. Also, their conversion loss figures are high for frequencies above 60 GHz because they use a single diode for harmonic mixing. The harmonic mixer presented here has better conversion loss and broader bandwidth than any available waveguide mixer. The back-to-back diode configuration allows efficient even-subharmonic (2N'th harmonic) mixing of the RF signal and results in much lower

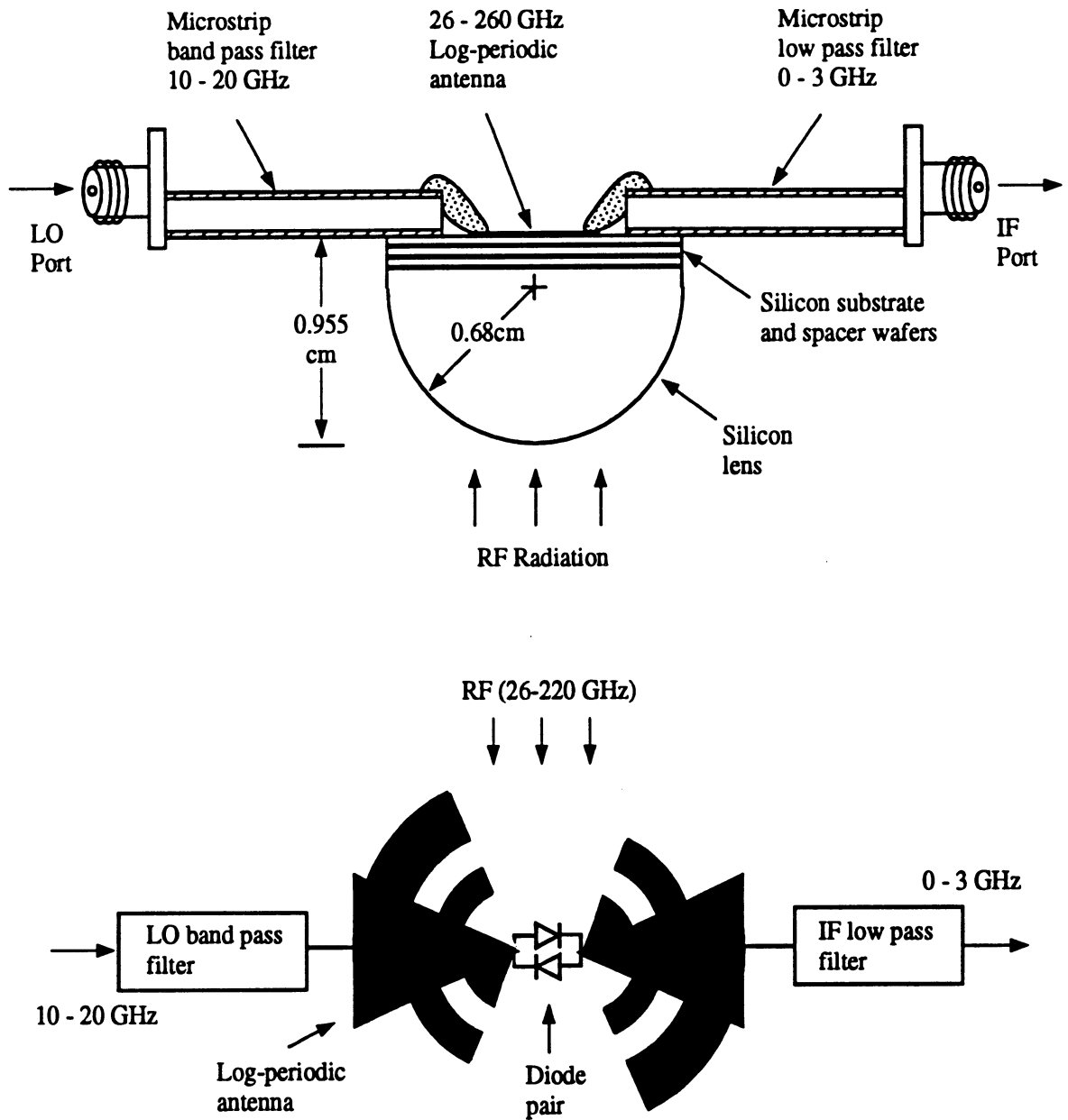
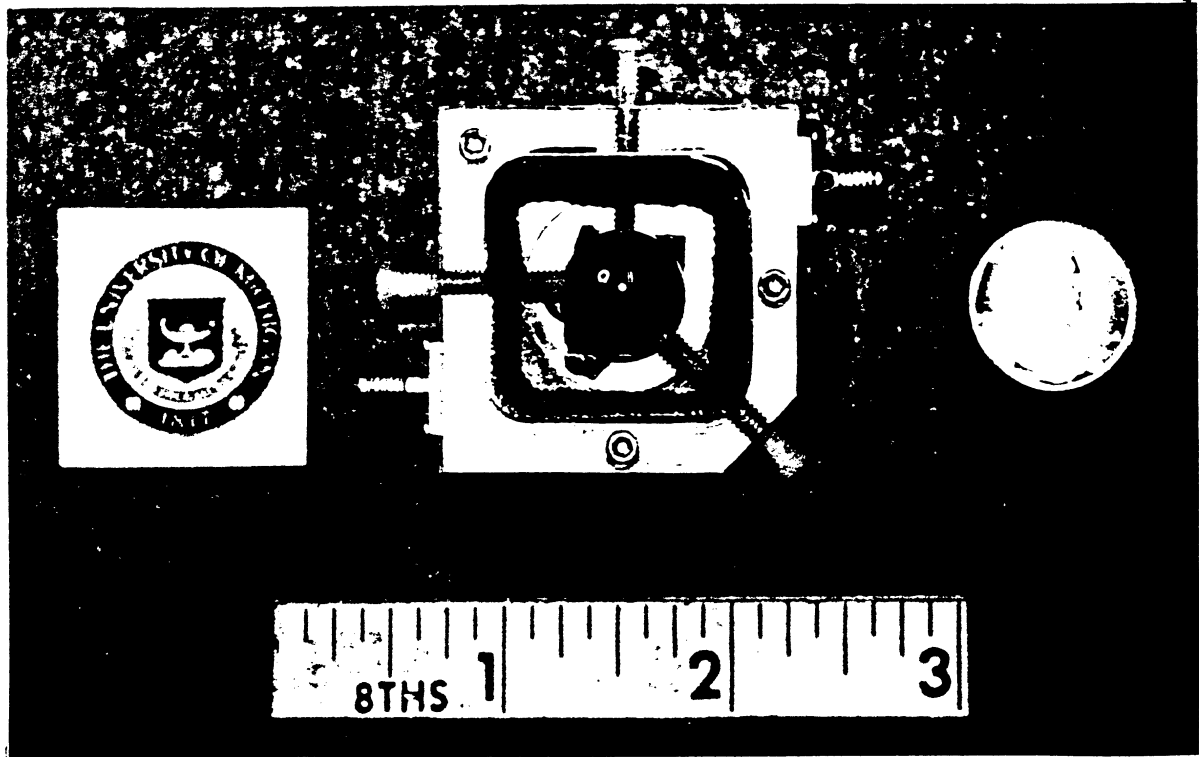
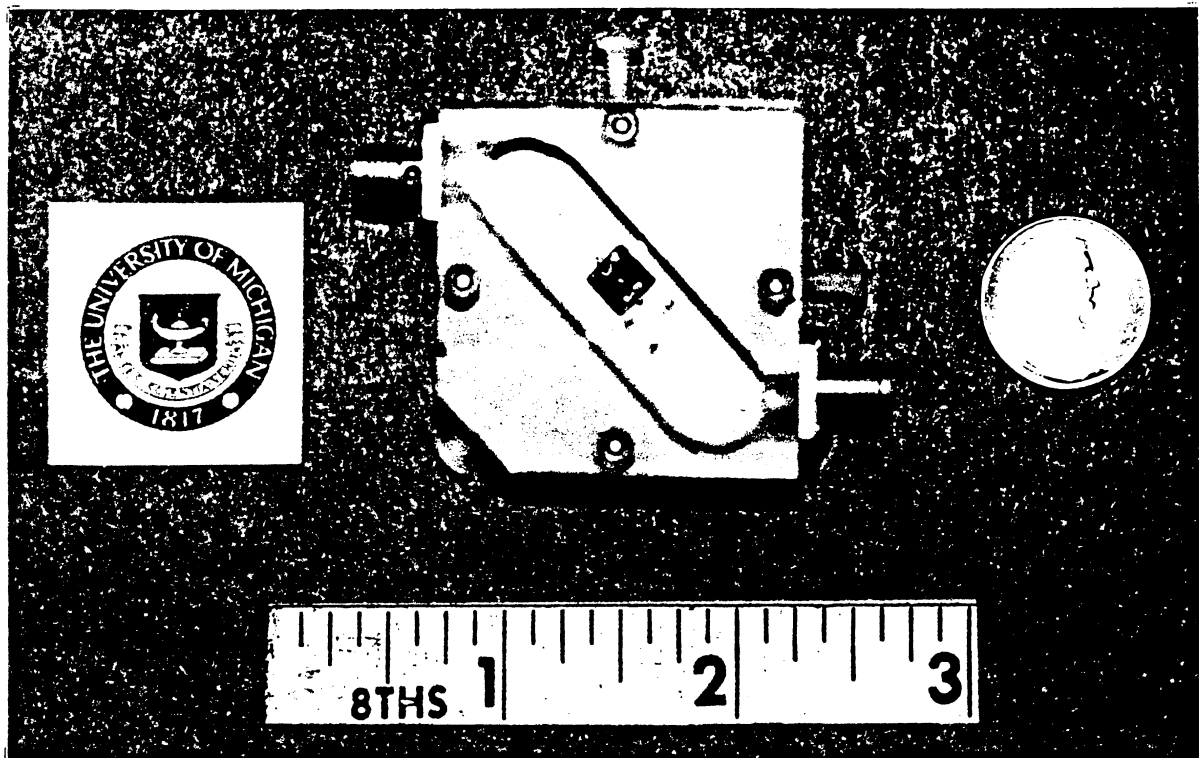


Figure 3.1: Cross sectional view of the $2N$ 'th harmonic mixer-receiver and its equivalent circuit.



(a)



(b)

Figure 3.2: Photographs showing the front side (a) and back side (b) of the quasi-optical 26-260 GHz 2N'th harmonic mixer receiver block.

conversion loss than a single diode. The quasi-optical RF input makes use of the full frequency range of the log-periodic antenna covering more than 5 waveguide bands in a single design (26.5-40, 40-60, 60-90, 90-140, 140-220, 220+ GHz). The lowest and highest frequency of operation are given by the largest and smallest teeth defined in the log-periodic antenna structure. However, in a hybrid design, the diode chip seriously affects the radiation from the smallest teeth and limits the highest frequency of operation to about 300 GHz. The IF and LO channels are diplexed using planar microstrip filters placed just outside the antenna terminals. The receiver can be easily built for submillimeter-wave frequencies (≥ 300 GHz – 1000 GHz) by monolithically integrating the log-periodic antenna with a low-capacitance diode pair.

Application areas for the $2N$ 'th harmonic mixer include wideband early warning systems, wideband search and rescue systems and extending the range of spectrum analyzers and power meters to the millimeter-wave region. Spectrum analyzer frequency range can be extended by connecting the IF output of the mixer to the RF input of the spectrum analyzer and using the LO output of the spectrum analyzer to derive an LO input for the harmonic mixer.

3.1 Antenna-Lens Design and Measurement

The antenna is the same planar self-complementary log-periodic antenna described in chapter 1 with $\sigma = 0.707$ and $\tau = 0.5$ designed to cover the 26 to 260 GHz band. The log-periodic antenna is again placed on the back of a silicon substrate lens to eliminate power loss to substrate mode, enhance the pattern in the direction of the dielectric and increase the gain. The antenna is placed $2750 \mu\text{m}$ behind the center of a 0.68 cm hemispherical lens which closely approximates an elliptical lens [34]. This differs from the $2220 \mu\text{m}$ position used in Chapter 2 which was selected to increase

the gaussian coupling efficiency in a quasi-optical system. An elliptical lens provides a uniform phase front across the aperture plane [47] resulting in the highest gain patterns without any additional optics. When the log-periodic antenna is placed at the elliptical position, the patterns are diffraction limited by the substrate-lens area. The effective aperture (RF collecting area of the antenna) is theoretically independent of frequency and equal to the physical area of the lens multiplied by a constant aperture efficiency. In practice, the aperture efficiency varies from 50-80% due to the variations in cross-pol magnitude discussed in Chapter 2 and other effects due to the small size of the lens relative to the long wavelengths encountered at lower frequencies. Figure 3.3 shows the measured radiation patterns of the log-periodic antenna at 40 GHz, 90 GHz, 180 GHz and 250 GHz. It should be noted that although the log-periodic antenna is frequency independent, the lens area remains constant causing a gain increase approximately proportional to f^2 . The 1.36cm elliptical lens results in very sharp patterns for frequencies above 150 GHz.

3.2 Mixer Design

The anti-parallel diode chip is the same University of Virginia SR2T1 type used in chapter 2. The anode diameter is 1.3 μm and the measured parameters are a series resistance of 11 Ω , a zero bias junction capacitance of 4 fF, an ideality factor of 1.2, a built in potential of 0.85 V, and a parasitic capacitance of 3 fF (see Section 2.2). The non-linear mixing program described in Chapter 2 can be used to calculate the performance of the back-to-back diodes for RF frequencies at two and four times the LO frequency. Table 3.1 shows the calculated diode RF impedance and the associated conversion loss at 34 GHz, 60 GHz and 90 GHz. Although the program does not calculate the diode impedance when used in the higher order sub-

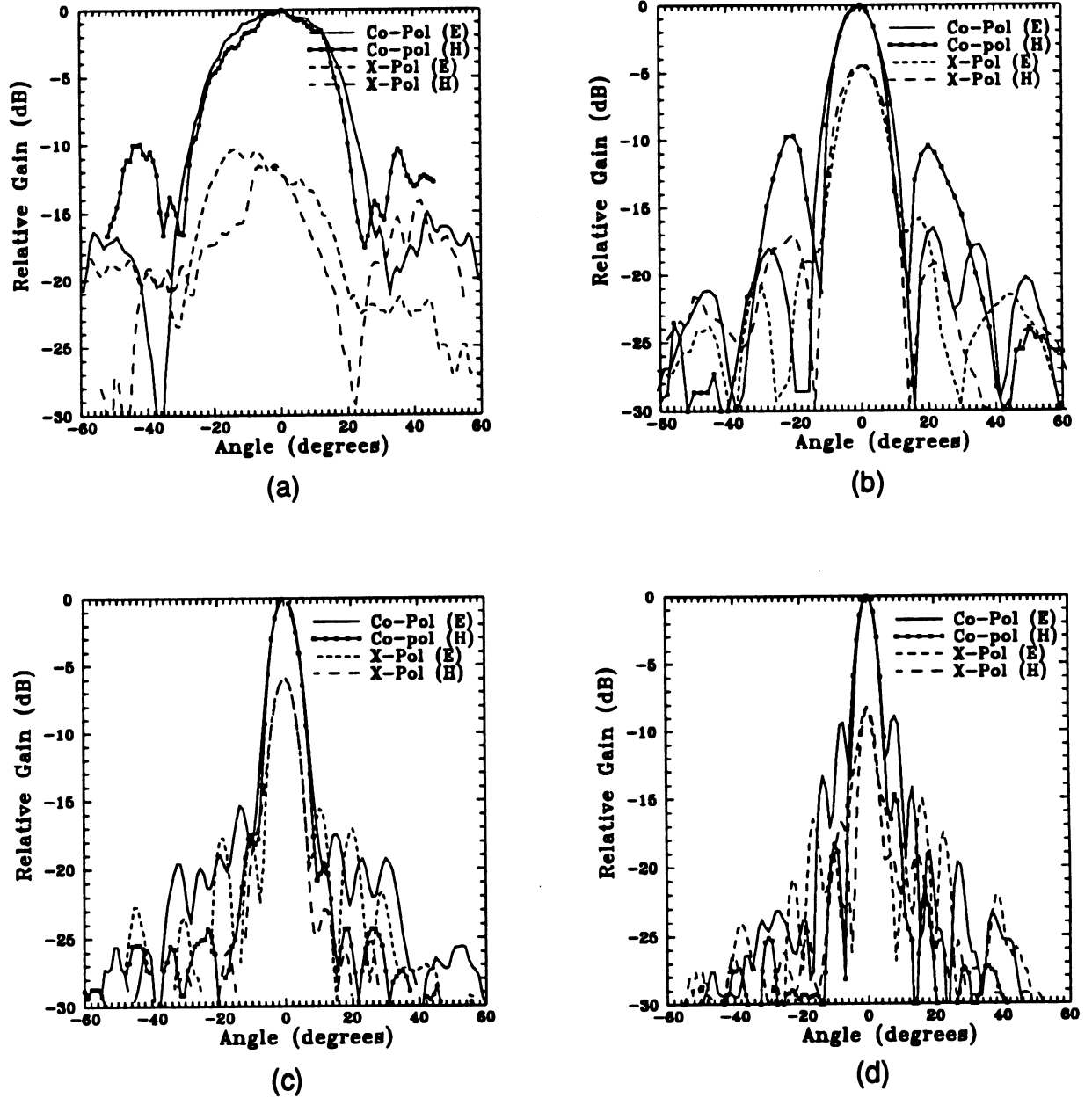


Figure 3.3: Measured radiation patterns for the log-periodic antenna on the approximately elliptical substrate lens (2750 μm position) at 40 GHz (a), 90 GHz (b), 180 GHz (b), and 250 GHz (d).

RF (GHz)	LO (GHz)	Harmonic Number	RF Impedance (Ω)	LO Impedance (Ω)	IF Impedance (Ω)	Conversion Loss (SSB) (dB)
34	17.70	2x	64 - j22	310 - j249	85	7.2
60	15.35	4x	27 - j6	270 - j141	58	15.3
90	22.85	4x	27 - j10	221 - j190	64	15.5

Table 3.1: Mixer program results for 2Nth harmonic mixer, conversion loss is for a 75 Ω RF source and a 50 Ω IF load.

harmonic modes (x6, x8, x10), it does give an indication that the small capacitance of the diode structure results in a high RF impedance throughout the 30-200 GHz band. The mismatch between the antenna and the diode is small, estimated to be less than 2.5 dB over the entire frequency range, and no RF matching network is used between the antenna and the diode chip. The corresponding IF impedance is around 70 Ω and therefore no IF matching network is used. The absence of matching networks in the RF and IF circuits makes the harmonic mixer a truly wideband design.

3.3 LO/IF Diplexer Design

As stated earlier, a microstrip diplexer is integrated at the edge of the log-periodic antenna. The LO signal is fed from the left terminal of the log-periodic antenna and the IF signal is taken from the right terminal (Fig. 3.1.). The antenna is very small electrically at the IF and LO frequencies and therefore behaves as a short conical transmission line. The antenna does not radiate the 10-20 GHz LO since its largest tooth resonates at 30 GHz. The IF filter is designed to be a combination of two separate low pass filters, a low frequency filter with a corner frequency of 3 GHz and a higher frequency filter with a corner frequency of 5 GHz. This results in an overall filter response that is not periodic with frequency and exhibits a very low impedance above 10 GHz providing the return path for the LO signal. The LO filter

is a bandpass filter covering the 10-20 GHz band. A bandpass filter containing only open and short circuit stubs is designed using Kuroda's identities [45] (see Fig. 3.4). The short circuited stubs also provide a simple DC path to ground and therefore are

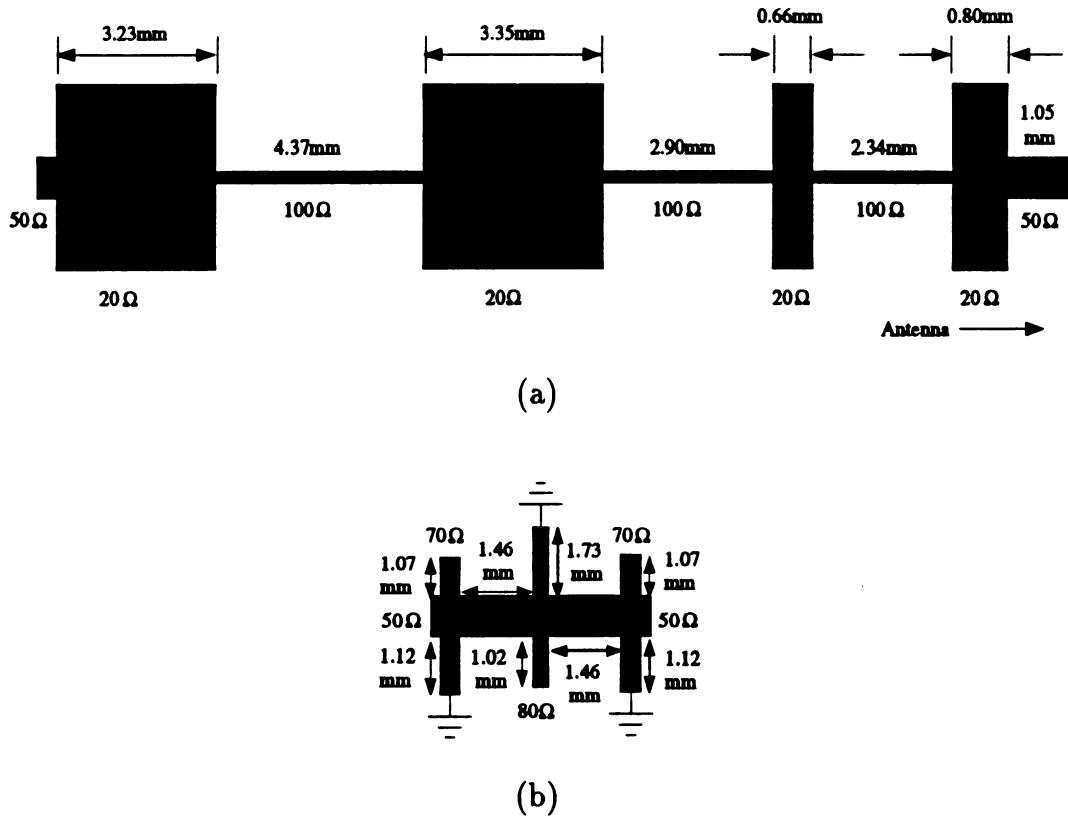
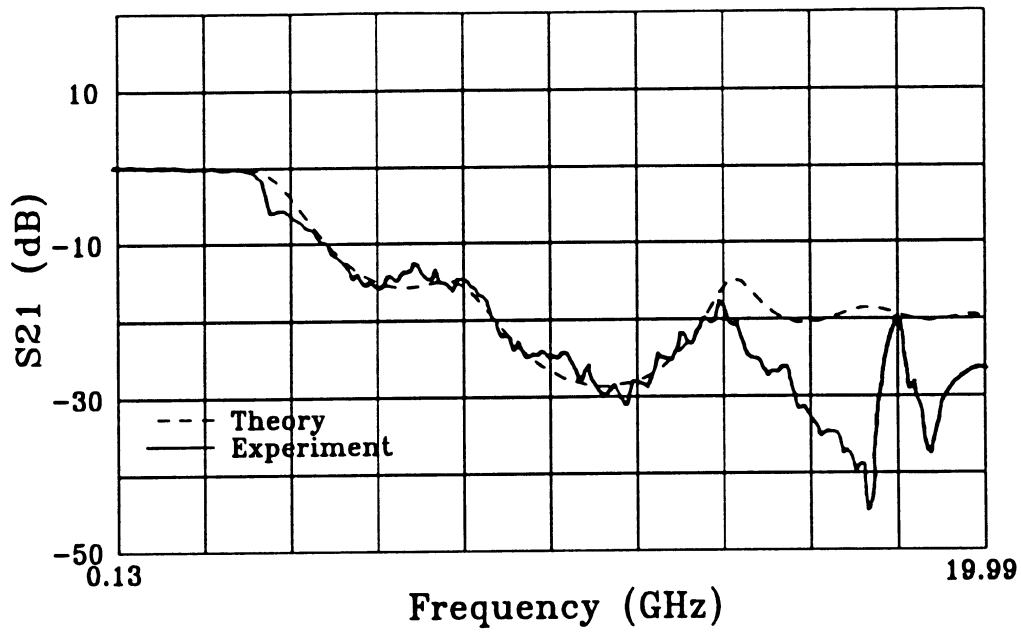
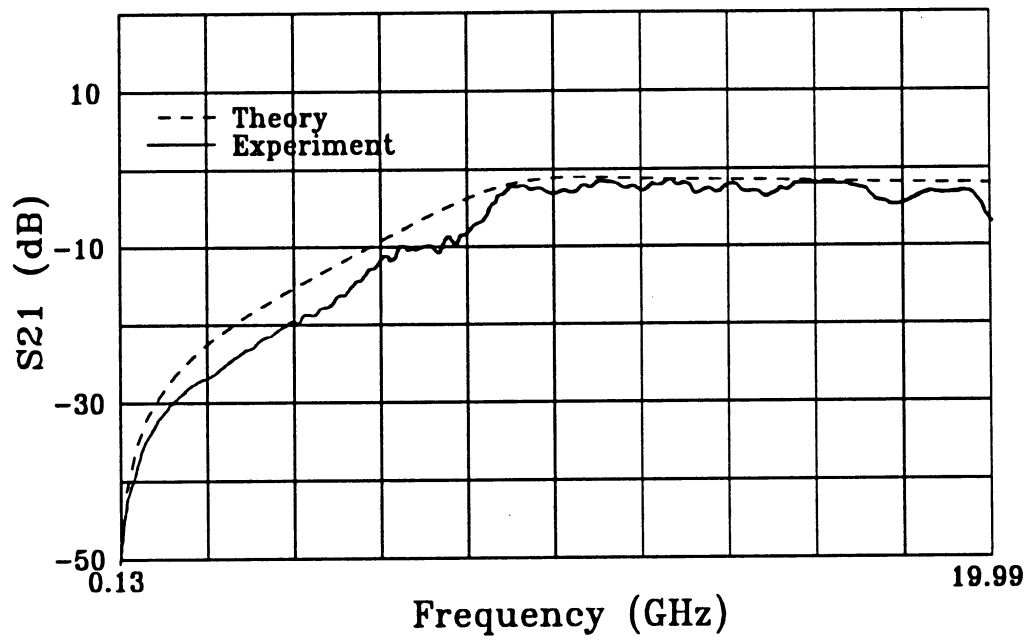


Figure 3.4: Layouts of the microstrip lowpass filter (a) and bandpass filter (b) for the diplexer.

useful for DC testing of the diodes and video detection experiments. The bandpass filter exhibits a low impedance in the IF band (0-3 GHz). A wideband local oscillator is needed in order to achieve full frequency coverage for second harmonic mixing (x2: RF 20-40 GHz) and fourth harmonic mixing, (x4: RF 40-80 GHz). For higher frequencies, the local oscillator range necessary for complete coverage is between 10 and 15 GHz (for example: x6: RF 60-90 GHz, x8: RF 80-120 GHz). Both filters were constructed on 0.635 mm thick Duroid RT/6006 ($\epsilon_r = 6.15$), see [46], and the measured filter responses agree well with theory (Fig. 3.5). The IF filter loss is less



(a)



(b)

Figure 3.5: Measured and theoretical S_{21} of the microstrip lowpass (a) and bandpass (b) filters in the diplexer.

than 0.3 dB up to 3 GHz and the LO bandpass filter loss is around 1.5 dB in the 10-16 GHz range.

3.4 Millimeter-wave Measurements

The harmonic mixer is part of the quasi-optical family of receivers and therefore its conversion loss can be defined and measured in a variety of ways. In this work, the conversion loss is defined as the power delivered to a 50Ω IF load divided by the total plane-wave power incident on the lens aperture (area = 1.26cm^2). This is a “systems” definition and includes all loss components in the harmonic receiver. It is a term that lets the user relate the measured IF power to the total RF power (or plane-wave RF power density) incident on the lens. The total conversion loss includes the following loss components (summarized in Table 3.2):

- 1- The coupling efficiency of the log-periodic antenna on an elliptical lens to a plane wave. As discussed before, the effective aperture is 50% to 80% of the physical area of the lens (around 2 dB loss). The mismatch due to the changing polarization angle is negligible since the antenna is always oriented for maximum response. If the antenna orientation is held constant across the operating frequency range of the receiver an additional loss from the changing polarization direction will be encountered. The maximum value of this additional loss will be 3 dB (see Fig. 2.2 for the polarization properties of the log-periodic antenna on a substrate lens).
- 2- The mismatch between the plane wave and the silicon lens. This is due to the high index of refraction of the lens ($\epsilon_r = 11.7$) and results in a 1.5 dB reflection loss. (No anti-reflection layer is used so as to result in the widest possible bandwidth).
- 3- The loss in the high-resistivity ($\geq 1,000\Omega\text{-cm}$ silicon lens. This is estimated to be 0.4 dB at 100 GHz [39]).

Aperture Efficiency (dB)	Lens Reflection (dB)	Lens Absorption (dB)	IF Filter Loss (dB)
1.5 → 3.0	1.5	0 → 0.4	0 → 0.2

Table 3.2: Summary of system losses that contribute to the measured SSB mixer conversion loss of the $2N$ 'th harmonic mixer

4- The RF mismatch between the antenna impedance (74Ω) and the diode RF impedance. This is calculated to be less than 2.0 dB for most frequencies.

5- The intrinsic back-to-back diode conversion loss. This varies with frequency and harmonic mixing number.

6- The IF mismatch between the diode and the IF load. Since the back-to-back diode is inherently well matched to a 50Ω load, this loss is less than 0.3 dB for all frequencies and mixing orders.

7- The IF filter ohmic loss which is measured to be 0.2 dB at 1.4 GHz.

The RF power was generated using an HP8350B sweeper and harmonic multipliers up to 100 GHz, and Gunn diodes with waveguide doublers for frequencies above 100 GHz. The power density at the location of the lens was measured using an Anritsu power meter with a calibrated standard-gain horn antenna. The local oscillator was generated using an HP83624A synthesized sweeper. The measured conversion loss did not vary for IF frequencies between 0.1-3 GHz and 1.4 GHz was chosen for IF power measurements. The back-to-back diodes require a local oscillator power of 30-50 mW for optimal operation. The upper and lower sideband conversion loss was very similar due to the wideband nature of the antenna and the local oscillator band-pass filter. The measured conversion loss is shown in Fig. 3.6 and summarized in Table 3.3. It exhibits a 9.2 dB single sideband (SSB) conversion loss at 34 GHz, and a

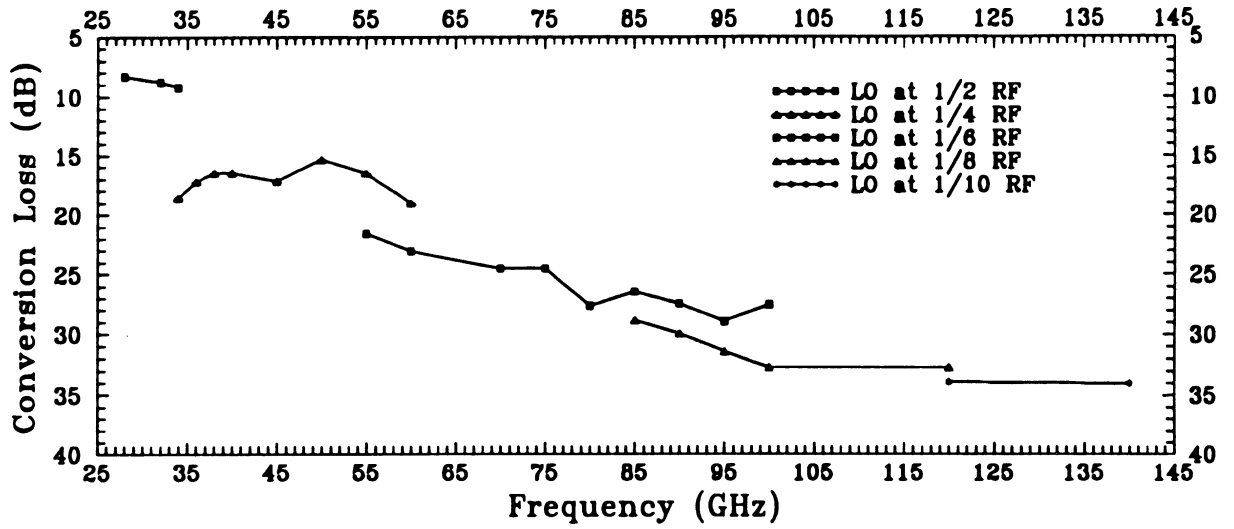


Figure 3.6: Measured SSB system conversion loss (see text) for the $2N$ 'th harmonic mixer.

RF Frequency (GHz)	LO Frequency (GHz)	Conversion Loss Measured (dB) (Calculated (dB))
34	17.70 (x2)	9.2 (9.9)
60	15.35 (x4)	19.0 (18.9)
90	15.23 (x6)	27.4
120	15.18 (x8)	32.7
140	14.14 (x10)	34

Table 3.3: Measured SSB system conversion loss (see text) for the $2N$ 'th harmonic mixer

34 dB SSB conversion loss at 140 GHz. The results at 140 GHz are 10 to 20 dB better than available commercial devices due to the excellent diode chip used and the subharmonic mixing advantage. The measured conversion loss at 34 GHz and 60 GHz agree well with the predicted values when all loss components are taken into account. From the measured antenna patterns, it is possible to use this harmonic receiver up to at least 260 GHz, but since the diode chip was accidentally damaged, no calibrated conversion-loss measurements were made above 140 GHz. This receiver has been extensively used with Tektronics and HP spectrum analyzers for 180 GHz power and frequency measurements. Also, it would be very easy to monolithically integrate a scaled mixer on a high-resistivity GaAs wafer for operation in the submillimeter-wave region (300 GHz - 1000 GHz).

CHAPTER IV

CPW-FED SLOT ANTENNA TRANSISTOR OSCILLATORS

In this chapter a novel active transmitter suitable for low-cost millimeter-wave applications is introduced. The transmitter consists of a coplanar-waveguide (CPW)-fed slot antenna (or dual slot antenna) and a three-terminal device (millimeter-wave HEMT). The transmitter combines microwave oscillator design with theoretical and experimental characterization of planar antennas to build an active slot antenna oscillator suitable for use in quasi-optical power combining arrays.

CPW transmission lines have several advantages at millimeter-wave frequencies. They have lower radiation loss and less dispersion than microstrip lines [48]. Furthermore, the characteristic impedance and phase velocity of CPW lines are less dependent on the substrate height and more dependent on the dimensions in the plane of the conducting surface. Also, the CPW-feed and antenna are on the same side of the substrate thereby facilitating the connection of shunt lumped elements and active devices, and eliminating the need for via holes. The slot-oscillator is therefore compatible with planar HEMT fabrication processes and can be easily scaled to higher frequencies. The CPW-fed oscillator is designed for use on a dielectric substrate lens. The substrate lens eliminates the excitation of substrate modes and the

associated power loss in these modes. It also enhances the pattern in the direction of the dielectric and increases the gain of the planar antenna (see Chapter 1 for more detail).

Two slot-oscillators at 20 GHz, a 37 GHz slot-oscillator, and a 7 GHz voltage controlled slot-oscillator (VCO) are presented in this chapter. The high frequency capability of the design is demonstrated in the following chapter with monolithic slot-oscillators at 155 GHz and 215 GHz. The use of slot-oscillators in quasi-optical power combining arrays is demonstrated in Chapter 6.

4.1 CPW-fed Slot Antenna Impedance

Accurate knowledge of the CPW-fed slot antenna impedance is important because it is used as a parameter in the oscillator design. This results in circuit simplification and an overall reduction in size. The small dimensions of the circuit (much less than a wavelength) allow the design of power combining arrays without triggering grating lobes. When a slot antenna is placed on a substrate lens the electromagnetic environment is approximately equivalent to an infinite dielectric half space. The geometry of a CPW fed slot antenna is shown in Figure 4.1. The impedance of the slot antenna on a dielectric half space can be calculated with the Space Domain Integral Equation (SDIE) technique, a full wave method of moments approach. This technique has been developed at the University of Michigan and has shown excellent versatility in the study of a wide range of planar elements [49, 50, 51, 52, 53]. The SDIE technique is not presented in this thesis but a complete treatment is given by Harokopus [54].

A theoretical calculation of slot-antenna impedance on an $\epsilon_r = 12$ half-space as a function of frequency is presented in figure 4.2 for two W_A/l_A ratios. The impedance

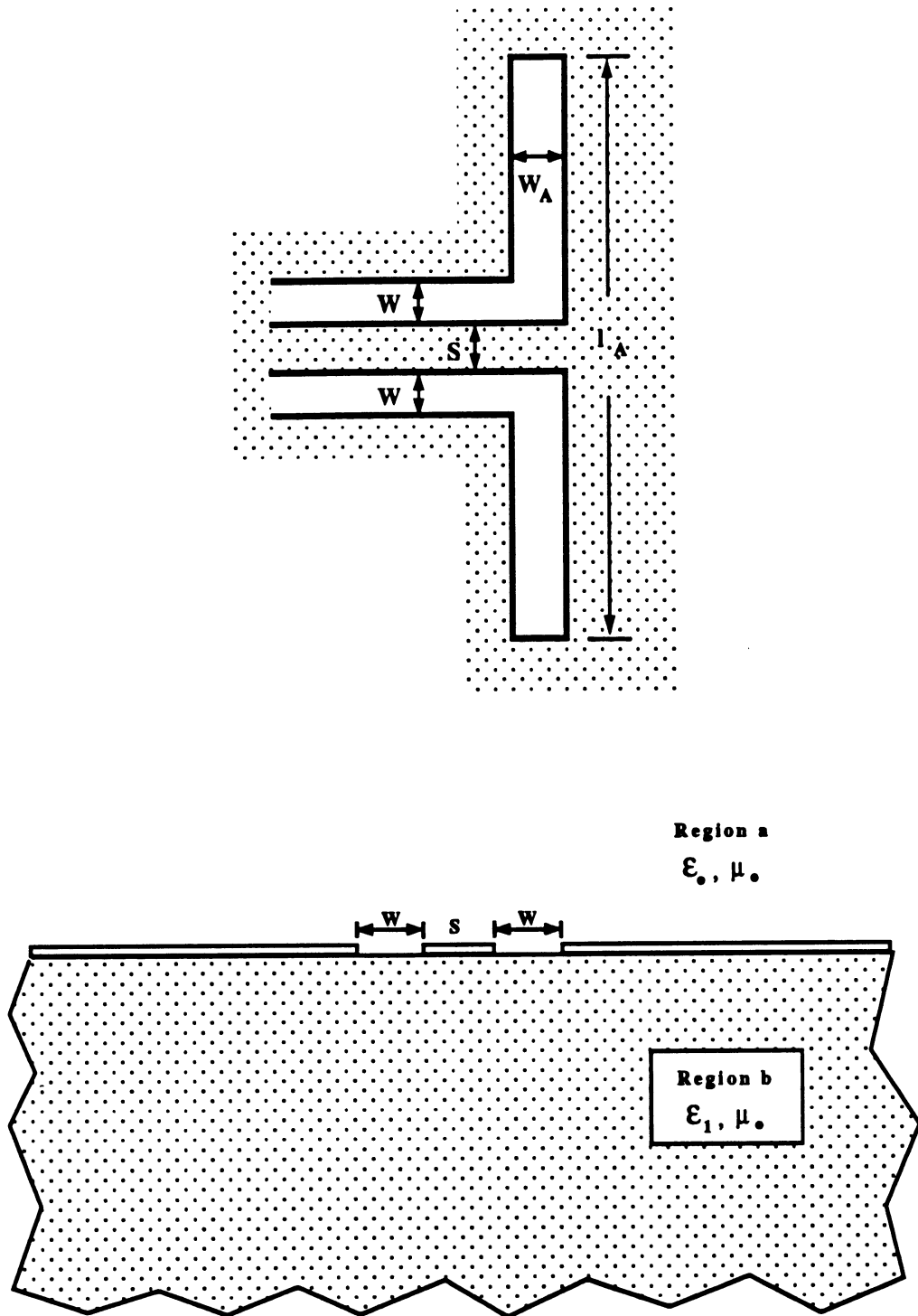


Figure 4.1: Geometry of a CPW-fed slot antenna on an infinite dielectric half space.

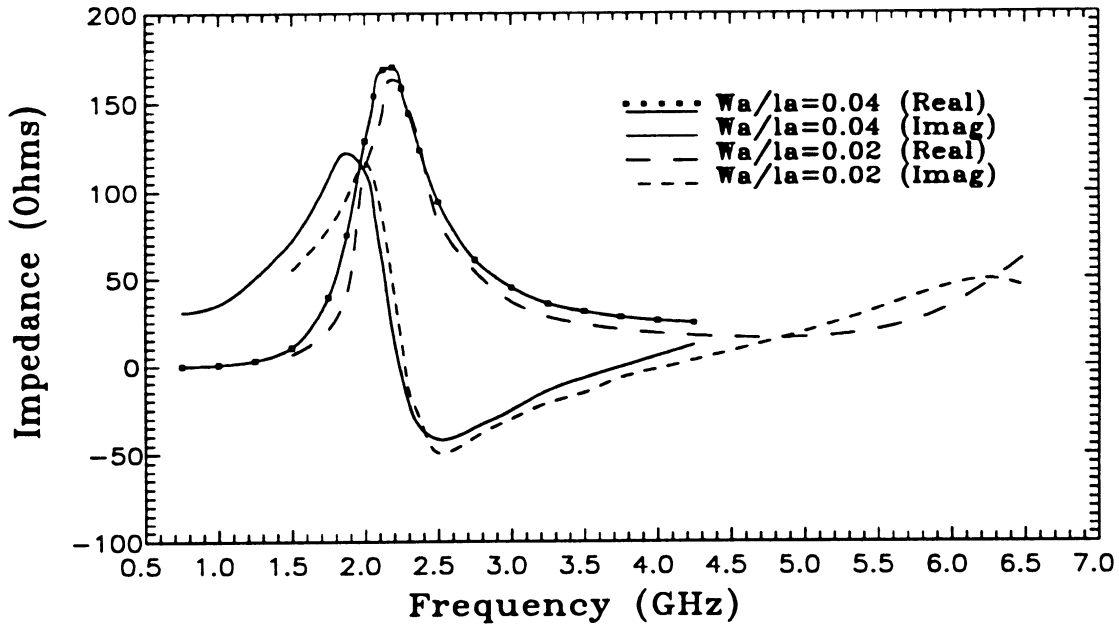
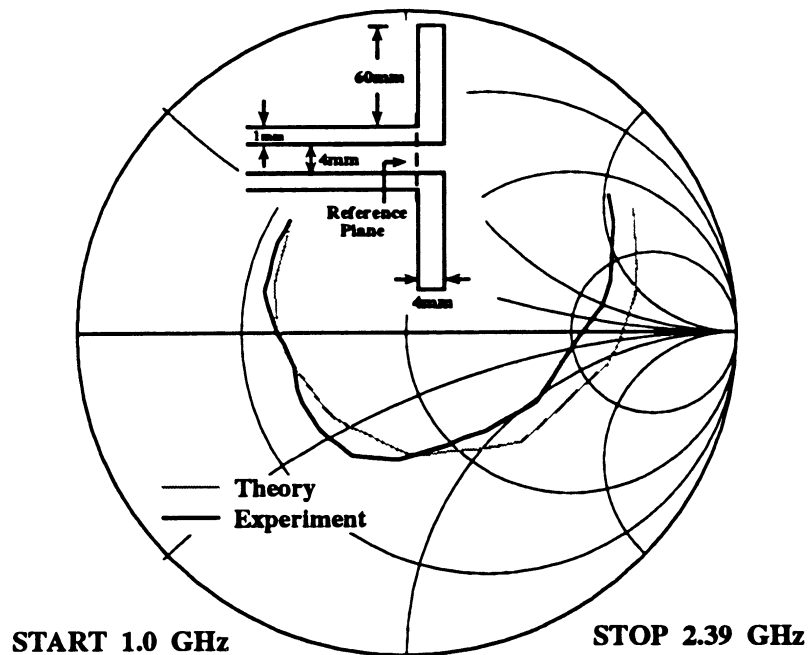


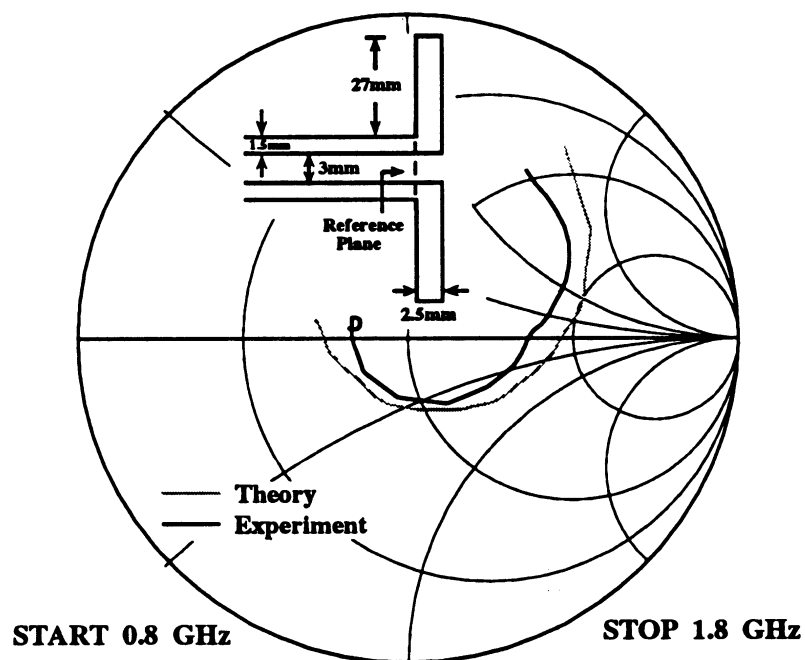
Figure 4.2: Theoretical calculation of slot antenna impedance as a function of frequency for $W_A/l_A = 0.02$ and $W_A/l_A = 0.04$ ($W = 0.5\text{mm}$, $S = 1\text{mm}$, $W_A = 0.5\text{mm}$ or 1mm , $l_A = 27\text{mm}$).

moves through a wide range from a near short circuit at low frequencies, to a high impedance near 160Ω at the first resonance, to a low impedance value (20Ω) with negligible reactance at a second wideband resonance. With appropriate frequency scaling, impedances throughout the range are available for oscillator design.

The accuracy of the theory has been verified by building microwave models of slot-antennas and measuring their impedance with a vector network analyzer. A slot antenna in free space and a slot antenna on a stycastr [55] substrate with $\epsilon_r = 12$ have been measured. The infinite extent of the substrate is simulated by using a large block of material with absorber on the sides not covered by the ground plane. The CPW-fed slot-antennas are attached to a coaxial line using a broadband coax-to-CPW transition which is normalized out of the measurements. The transition equalizes the ground planes at the start of the CPW feed reducing higher order modes on the line. The feed lines are short, about $\lambda_{eff}/4$ to $\lambda_{eff}/2$, and we have not seen any benefit



(a)



(b)

Figure 4.3: Theoretical and measured impedances for CPW-fed slot antennas in free space (a) and on a dielectric half space with $\epsilon_r = 12$ (b).

from additional ground equalization using air bridges along the line. The geometries of the microwave models are shown in Figure 4.3 with the theoretical and experimental impedances. The reference plane is set at the input of the slot. Agreement between the measurements and the theory is generally good in both cases. The variation is due to difficulties encountered in building the infinite substrates and ground planes and the ideal excitation of the CPW which the theory assumes.

4.2 Slot Oscillator Design

The oscillator design is based on the small signal S-parameters of the microwave transistor using the reflection amplifier approach. This approach allows several important oscillator parameters including overall loop gain and frequency stability to be graphically visualized over a wide frequency range [56, 57].

The microwave transistors used are typically in chip form and the manufacturer supplied S-parameters include the effects of the bond wires used to connect the device to the circuit. An indefinite scattering matrix is employed so that short circuited lengths of CPW transmission-line may be placed at the gate and source terminals. Typically a CPW center conductor width to gap ratio of 2 is used to provide an approximately 50Ω transmission line on a silicon ($\epsilon_r = 11.7$), GaAs ($\epsilon_r = 13.1$), or alumina ($\epsilon_r = 9.8$) substrate. The exact characteristic impedances and effective dielectric constants for the CPW lines on a semi-infinite dielectric half space are calculated with the quasi-static analysis available on Linecalc [58] by increasing the substrate thickness until it no longer affects the results.

Computer optimization using Touchstone/Libra [58] is applied to the lengths of the CPW transmission-line at the source and gate to maximize the reflection coefficient at the drain of the device (S_{11}). In this way a reflection magnitude greater than one

is obtained at the design frequency. A slot antenna is designed so that its reflection coefficient through a length of CPW line has a phase angle opposite in sign to S_{11} at the drain of the device. The magnitude of the slot antenna reflection coefficient is made larger than the inverse of S_{11} . This situation allows any noise signal at the design frequency to coherently increase in amplitude resulting in oscillator startup. Nonlinear modeling of oscillator startup and operation is presented in Appendix B. The slot oscillator is a series connected topology and no shunt elements are directly connected between transistor terminal pairs. This eliminates problems that might be encountered with equalizing the potential of enclosed regions in the CPW ground plane.

The source connections (2 of them) are DC short-circuited to the ground plane and a metal-insulator-metal capacitor is integrated at the gate end for applying the gate bias voltage. The drain bias is applied by DC isolating the region of the ground plane near the slot antenna from the region of the ground plane near the source terminals with thin ($30 \mu\text{m}$) capacitively bypassed slits in the metallization. The total capacitance of the overlaid slits should be several hundred pico Farads to prevent the circuit from oscillating at lower frequencies. The large capacitance values insure that the transistor is embedded in an uninterrupted ground plane at the RF design frequency. The equivalent impedances seen by the source, gate and drain ports at lower frequencies are zero (short-circuited) due to the short lengths of CPW line used. The design therefore eliminates the need of additional resonant structures or RF chokes and results in a compact circuit for power combining applications.

The slot oscillator design procedure described above provides high loop gain for the given topology because the magnitude of S_{11} is typically very large. This results in a high probability of successful operation at the design frequency but does not guarantee

the highest possible power output. Maximum oscillator output power may be obtained using different embedding network topologies which come closer to providing the effective feedback required for maximum power added efficiency [59]. This technique is described in Appendix C.

4.3 20 GHz Slot Antenna Oscillators

Two slot-oscillators were designed and built at 20GHz using commercially available hetero-junction FETs (see Appendix D). The first design is based on the NEC NE32100, a low noise small signal device with a gate length of $0.3\mu\text{m}$ and an estimated maximum oscillation frequency (f_{max}) of 65 GHz. To obtain more output power, a second design was based on the Fujitsu FLR016XV, a K-band power transistor (estimated $f_{max} = 54$ GHz). Smith chart plots of $1/S_{11}$ and the slot antenna reflection coefficient through the matching length of CPW are shown in Figs. 4.4 and 4.5 along with the equivalent circuits for the oscillators. At the design frequency the phase angle of $1/S_{11}$ and the antenna reflection coefficient (Γ) are equal and the magnitude of Γ is larger than the magnitude of $1/S_{11}$ providing the loop gain for oscillator startup. This point is indicated on the smith chart plots. The antenna reflection coefficient (Γ) and $1/S_{11}$ move in opposite directions on the smith chart providing stable single frequency operation [57]. The circuit layouts are shown in Fig. 4.6 with ground equalizing bond wire air bridges installed around the gate, drain, and the two source terminals to insure that only the odd mode is excited on the CPW lines. The circuits are realized with $1.5\mu\text{m}$ of evaporated gold on high resistivity silicon substrates. The insulating layers for the capacitive bypassing consists of a $2\mu\text{m}$ thick film of Probimide 408 polyimide [60].

The circuits oscillated when placed at the focus of an elliptical silicon substrate

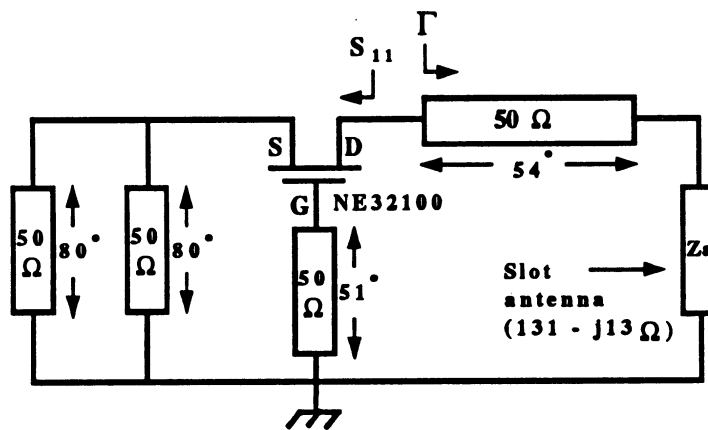
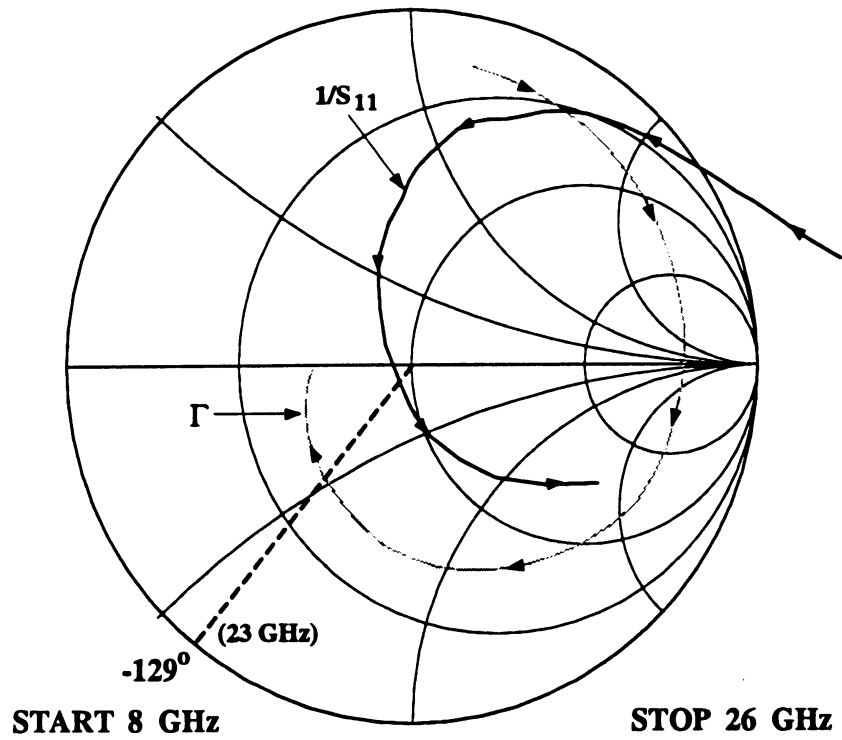


Figure 4.4: Smith chart plot and equivalent circuit of the first 20 GHz CPW fed slot oscillator design.

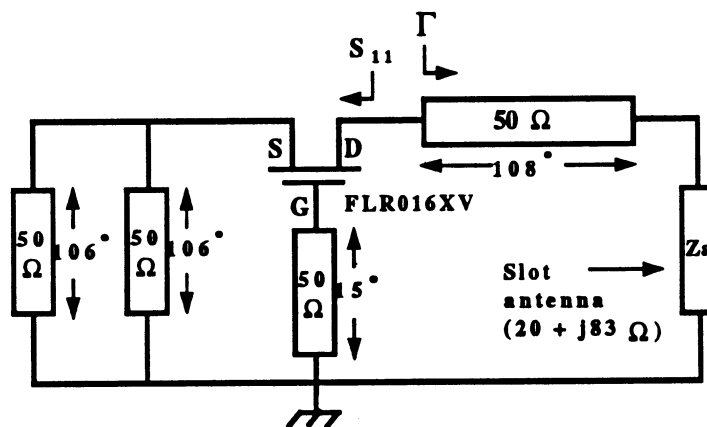
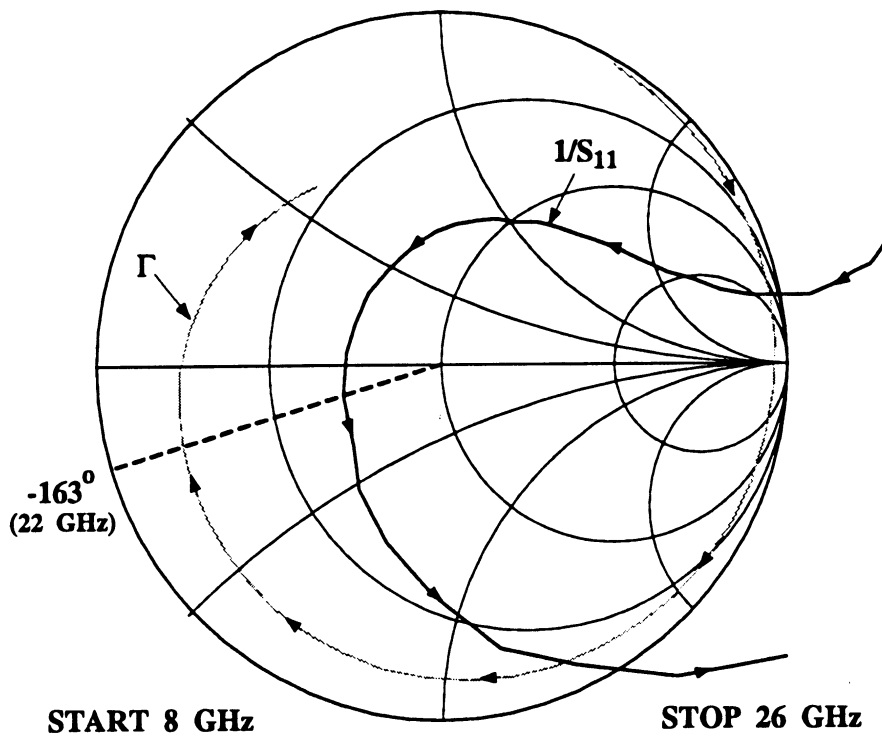


Figure 4.5: Smith chart plot and equivalent circuit of the second higher power 20 GHz oscillator design.

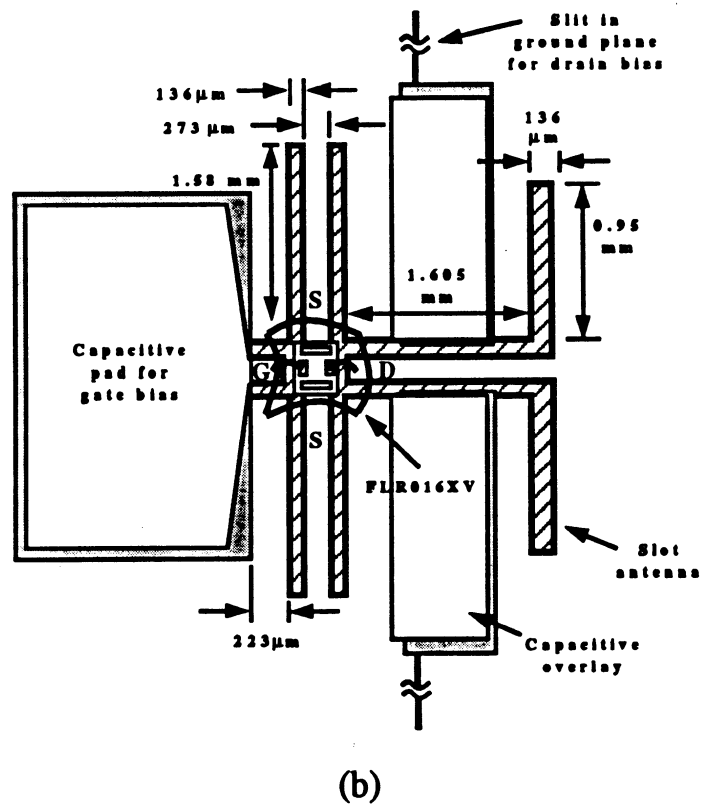
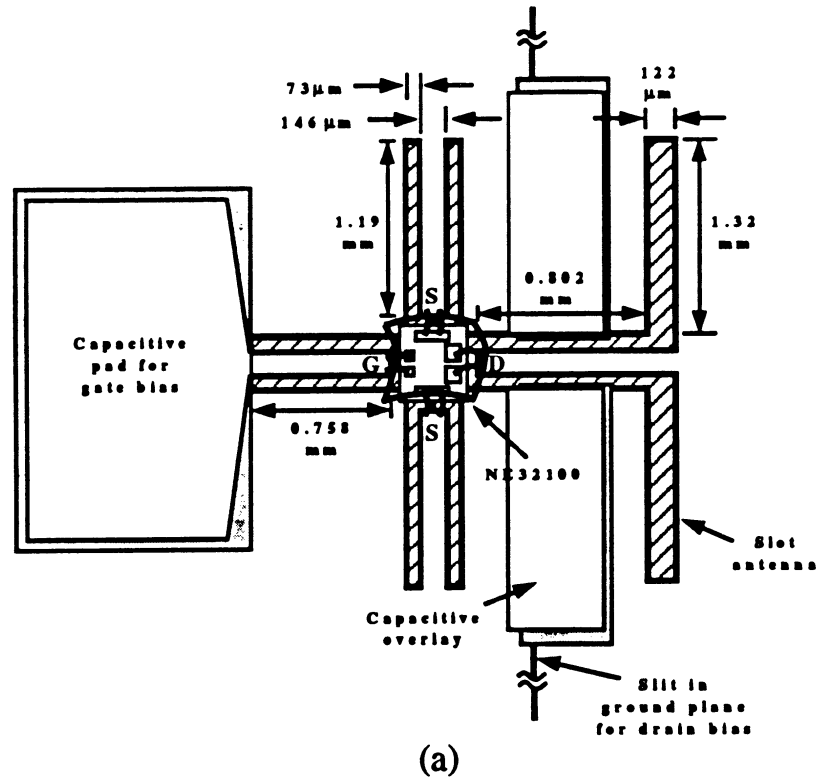


Figure 4.6: CPW circuit layouts for the 20 GHz oscillators showing capacitive bypassing to allow application of DC bias. First design (a), second higher power design (b).

lens with a diameter of 2.6cm. The measured operating frequencies are 5-10% less than the small signal design frequencies due to changes in the S-parameters as large signal conditions are reached. The elliptical lens acts as an infinite dielectric medium and collimates the radiation pattern from the slot antenna (see Chapter 3). The slot-antenna provides a uniform E-plane feed pattern that is transformed by the elliptical lens to a narrow diffraction limited pattern with high sidelobes. On the other hand the final H-plane pattern is wider and with very low sidelobes due to the tapered (nearly $\sin^2\theta$) H-plane pattern of the slot antenna. It is possible to obtain symmetric E- and H-plane patterns with the use of double slot-antenna designs [18]. A functioning 4 GHz single transistor oscillator with a dual slot antenna operating in free space without a substrate lens has been constructed to verify the application of this technique to oscillator design (not published).

The measured radiation patterns for a 20 GHz single slot-oscillator on an elliptical substrate lens are shown in Fig. 4.7. The radiation patterns for both 20 GHz oscillators are very similar. The pattern directivity is estimated from a geometric mean of the front side E-plane, H-plane, and 45-degree plane patterns. The value of the front side directivity is reduced as shown below due to the power radiated to the back side and lost to cross-polarized components.

$$D_o = \frac{4\pi(\text{Front side peak power})}{\iint(\text{Front Co-pol})d\Omega + \iint(\text{Front X-pol})d\Omega + \iint(\text{Back Co-pol})d\Omega} \quad (4.1)$$

Measured back side patterns indicate that about 10% of the power is going into the air behind the lens. This differs from the expected 2% back side power loss given by the $\epsilon_r^{3/2}$ rule [32] since there is no matching layer on the lens front surface to eliminate multiple reflections. The resulting directivity for a 20 GHz single slot oscillator on a 2.6 cm diameter silicon lens is found to be about 13.22 dB. The corresponding aperture efficiency is 71%.

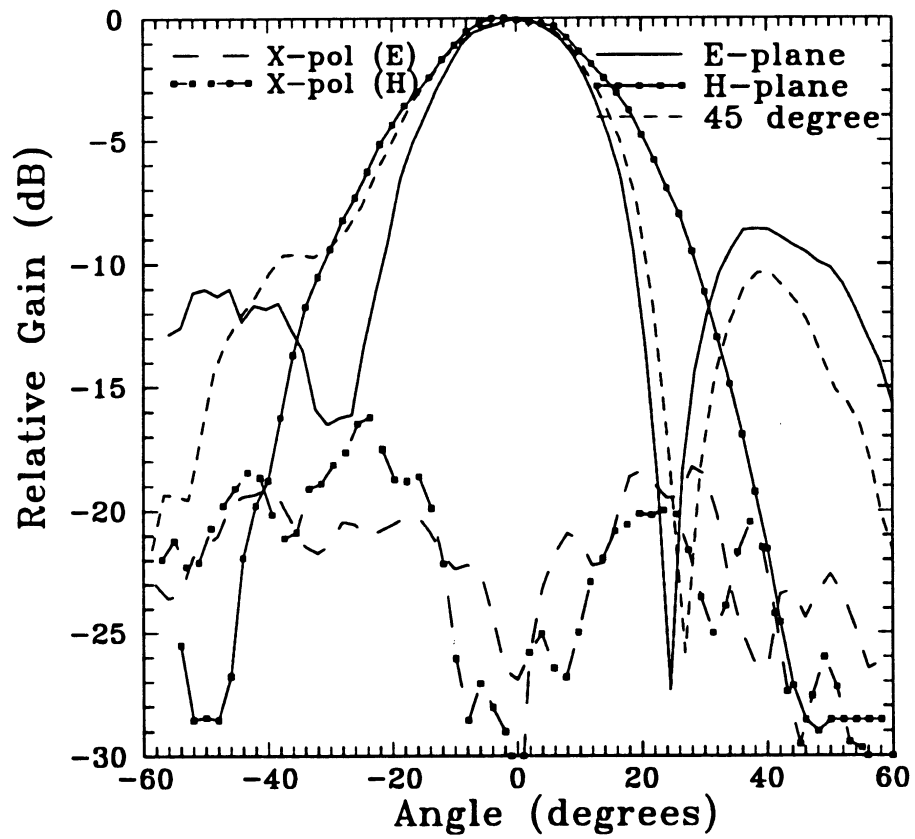


Figure 4.7: Measured radiation patterns of a 20 GHz slot-oscillator on a 2.6 cm diameter silicon substrate lens.

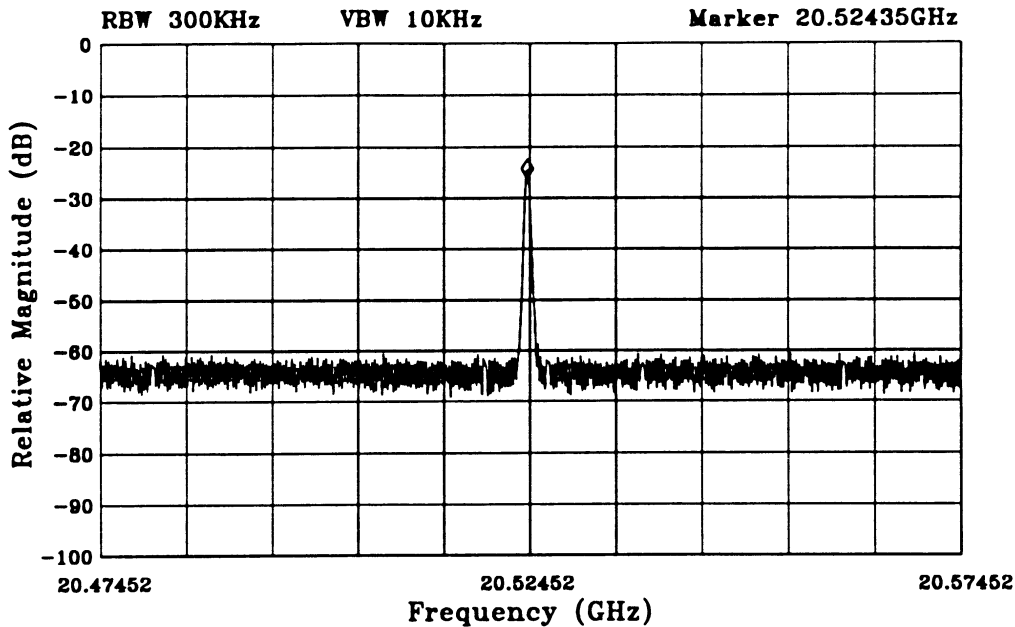


Figure 4.8: Spectrum of the 20 GHz slot antenna oscillator using the Fujitsu FLR016XV.

The total oscillator power is calculated from the absolute power received by a standard gain horn at the pattern peak, the Friis transmission equation [61], and the measured pattern directivity (explained above). Power output depends on the DC bias of the transistor and slight frequency shifts also occur with changes in the DC conditions due to S parameter variations. For the first design, the highest measured total power is 3 mW at 22.45 GHz with a drain current (I_d) of 20 mA and a drain to source voltage (V_{ds}) of 4 V. The second design based on the power transistor has a highest power output of 17 mW at 20.07 GHz ($I_d = 27$ mA, $V_{ds} = 4.5$ V). The DC to RF efficiencies are 3.8% and 14% respectively. These power measurements are accurate to about $\pm 5\%$ with most of the error due to uncertainty in the estimation of the pattern directivity. The theoretical maximum output power for the FLR016XV power transistor used in the second design is estimated to be 45-50 mW using the relationships given by Johnson [62]. The theoretical maximum DC to RF efficiency [63] for this device is about 30%. This indicates that it is possible to increase the

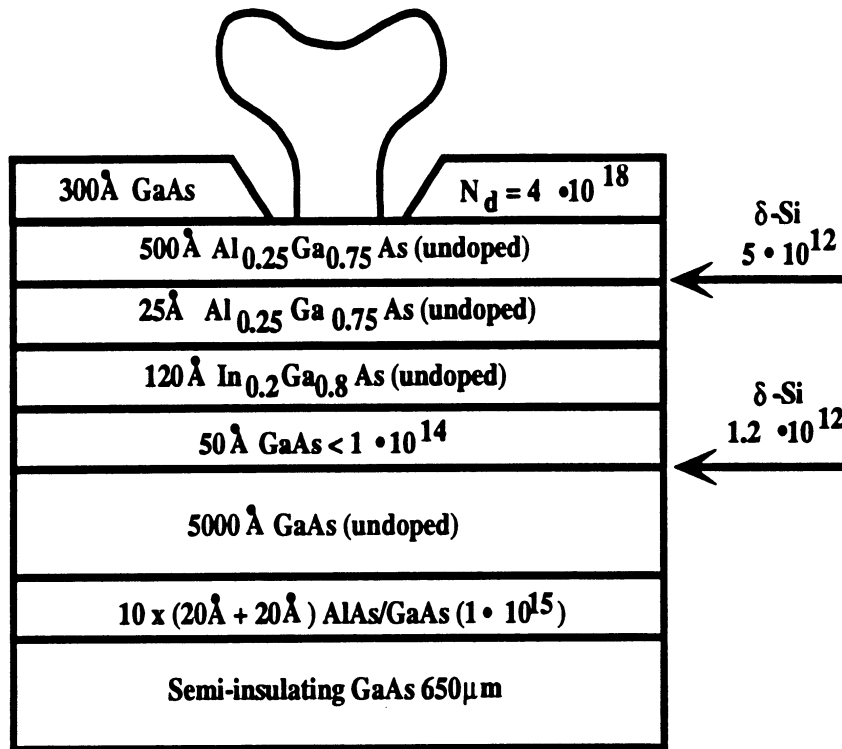
output power and efficiency of the slot oscillators by adjusting the effective feedback in the system (Appendix C).

The spectrum of the higher power 20 GHz oscillator using the Fujitsu FLR016XV is shown in Fig. 4.8.

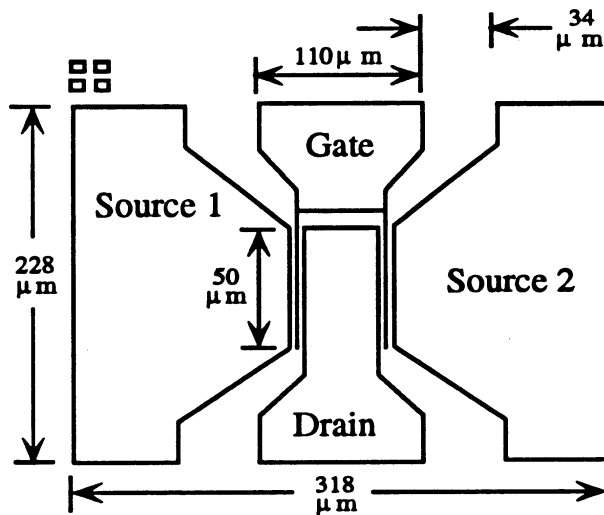
4.4 37 GHz Slot Antenna Oscillator

The 37 GHz slot antenna oscillator is a hybrid circuit using a flip chip transistor to eliminate bond wire parasitics and enable higher frequency operation. The transistor is a pseudomorphic double delta-doped AlGaAs-InGaAs-GaAs type heterojunction FET (HFET) fabricated by Dr. Herbert Zirath at Chalmers University of Technology, Sweden. The material was grown by Quantum Epitaxial Designs, Inc. (QED). The gates were defined by a tri-layer resist electron beam lithography process to obtain a mushroom shaped gate cross section. The gate length is approximately $0.2 \mu\text{m}$ and the effective gate width is $100 \mu\text{m}$. The gates are formed by evaporation of Ti/Pt/Au. The device doping profile and contact pad layout are shown in Fig. 4.9. The small signal device model (Fig. 4.10) was derived at Chalmers from on wafer two-port S parameter measurements to 62.5 GHz by using methods described in [64, 65]. From extrapolation with the experimentally obtained model, the device shows a unity current gain transition frequency (f_t) of 46 GHz and a maximum oscillation frequency (f_{max}) of 84 GHz given by the unilateral gain transition. The relatively large gate and drain pads for flip chip mounting decrease f_t somewhat. The intrinsic f_t , i.e. the f_t when the influences from the pad parasitics are removed is 60 GHz.

The slot oscillator design follows the procedure used in the previous two sections. Since designs based on small signal S parameters show an approximate 10% reduction in the actual operating frequency due to changes in the S parameters as large signal



(a)



(b)

Figure 4.9: The doping profile (a) and contact pad layout (b) of the pseudomorphic HFET developed at Chalmers University of Technology, Sweden.

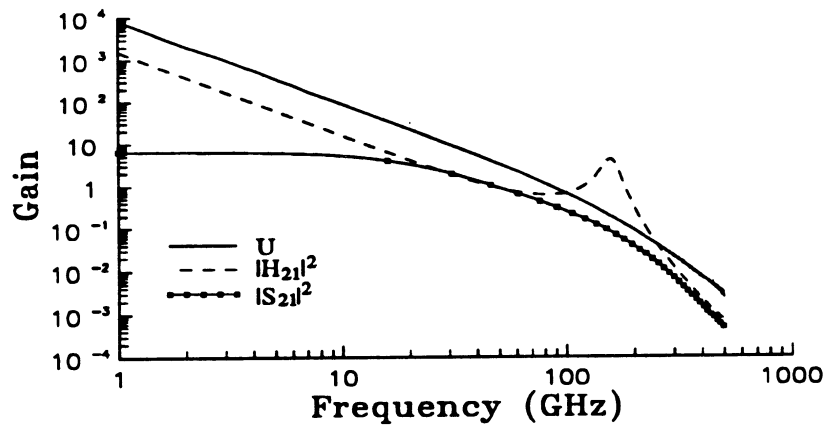
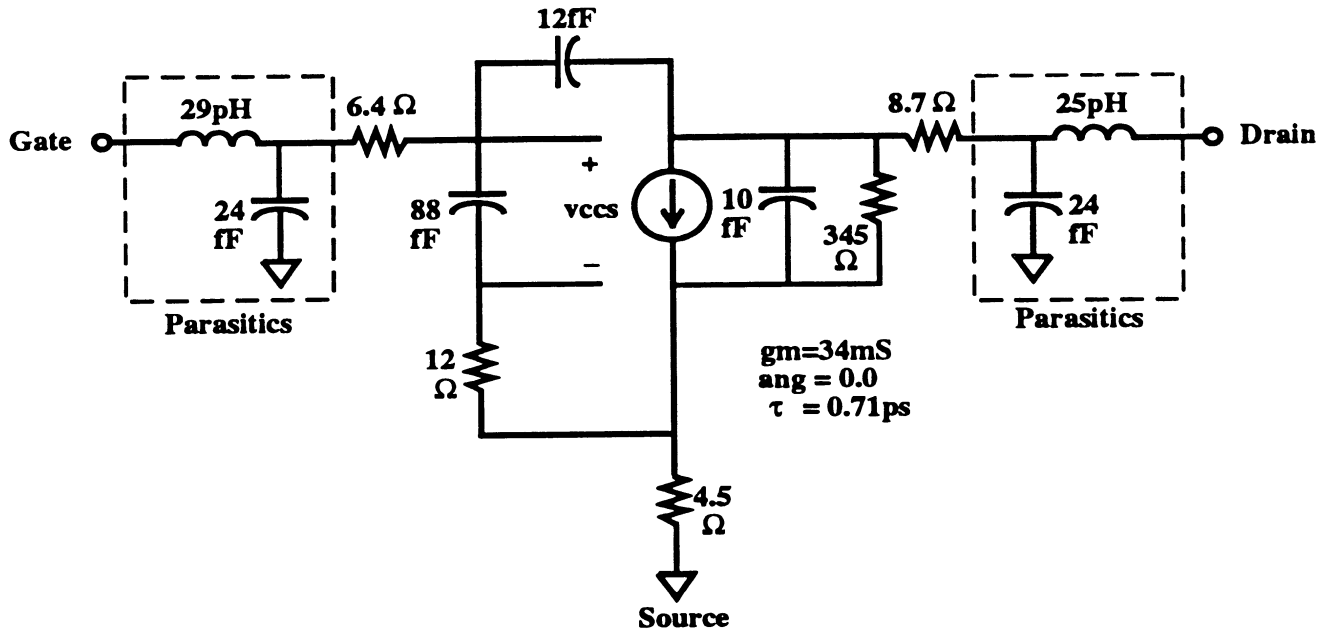


Figure 4.10: Small signal model and simulated gain versus frequency characteristic for the delta-doped HFET ($f_t = 46 \text{ GHz}$, $f_{max} = 84 \text{ GHz}$).

F (GHz)	Power (mW)	I _d (mA)	V _d (Volts)	V _g (Volts)	DC-RF efficiency (%)
37.134	0.135	19.45	2.022	-0.540	0.3
36.884	2.148	34.36	3.860	-0.606	1.62
36.815	2.20	36.33	4.145	-0.583	1.46

Table 4.1: Frequency and power output of the 37 GHz slot antenna oscillator for different DC bias conditions.

conditions are reached, the small signal design of the oscillator was carried out at 44 GHz giving an expected output frequency of 40 GHz. The circuit is fabricated on an alumina substrate ($\epsilon_r = 9.80$) using a 1.5 μm layer of evaporated gold. The insulating layers for capacitive bypassing are made with a 2 μm polyimide film as described before. The CPW transmission line widths are scaled to fit the contact pads of the flip chip and the gap dimensions are chosen to provide a characteristic impedance of 50 Ω . The CPW layout and equivalent circuit are shown in figure 4.11. The transistor was hybrid mounted on the planar CPW circuit with silver epoxy. The oscillator was positioned on a 4.9 cm diameter hyper-hemispherical alumina substrate lens for testing. The oscillator frequency was accurately measured and its spectrum (Fig. 4.12) was observed by downconverting the signal to 1.4 GHz with a harmonic mixer using a synthesized sweeper as an LO source.

The total oscillator power is calculated from the absolute power received by a standard gain horn at the pattern peak, the Friis transmission equation, and the measured pattern directivity as described before. The performance of the oscillator at different DC bias points is given by the following data: highest frequency of 37.134 GHz with a total bias tuning range of 318 MHz, highest power of 2.2 ± 0.2 mW at 36.815 GHz and 1.5% efficiency, and a highest efficiency of 1.6% at 2.1 ± 0.2 mW and 36.884 GHz. These results are summarized in Table 4.1.

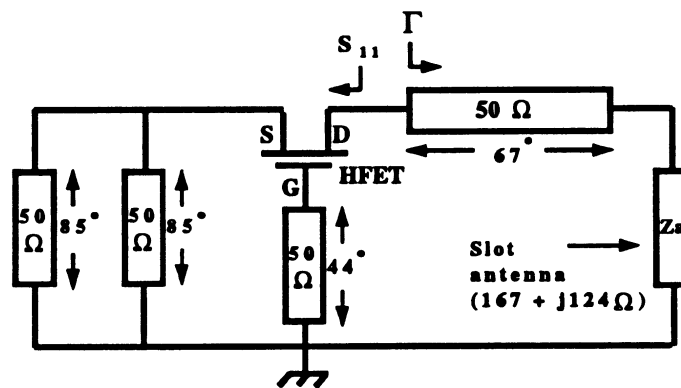
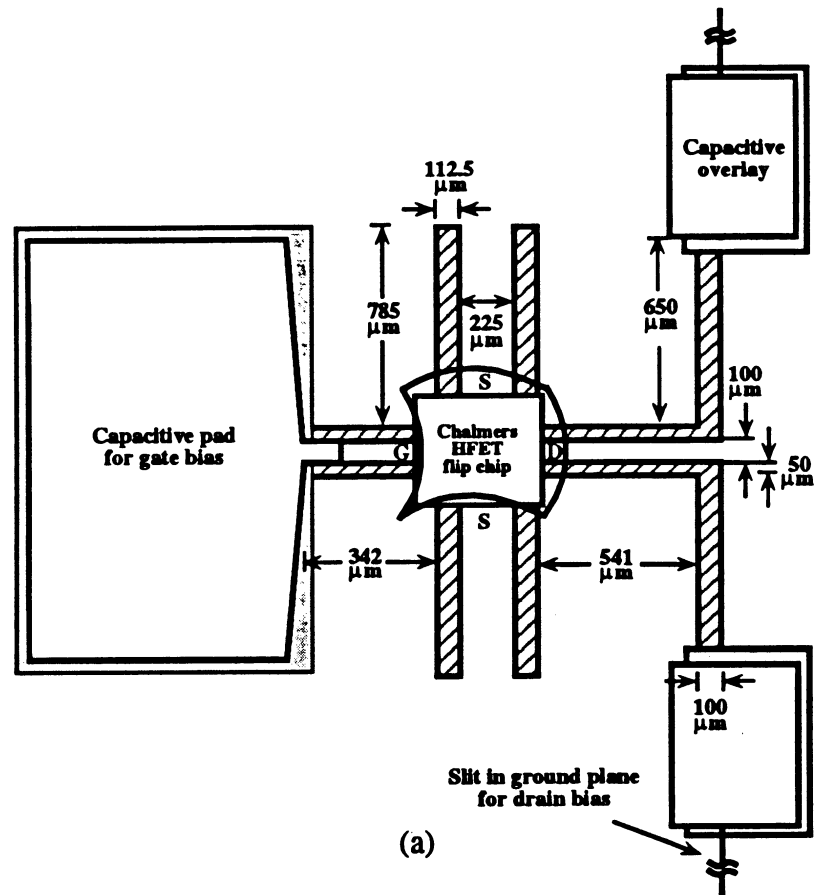


Figure 4.11: CPW layout (a) and 40 GHz equivalent circuit (b) for the slot oscillator using the pseudomorphic HFET.

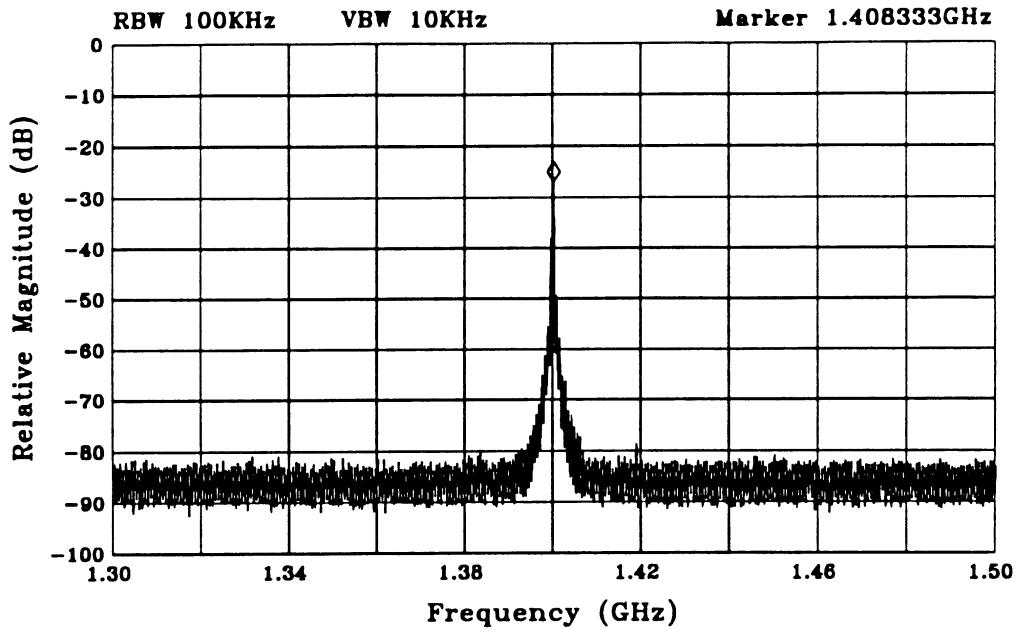


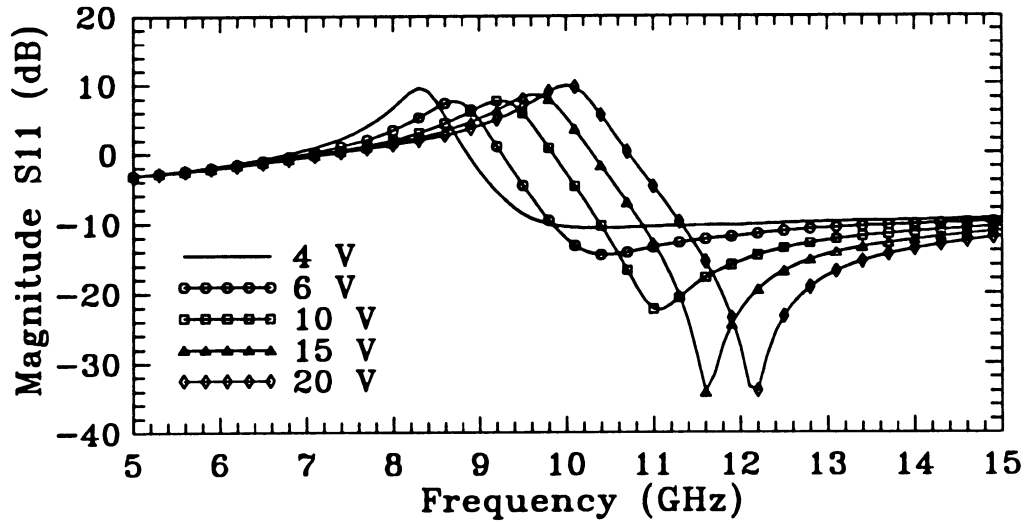
Figure 4.12: Downconverted spectrum of the 37 GHz slot antenna oscillator.

The measured frequencies are lower than the expected value of 40 GHz since the originally expected device was unavailable and the HFET described and modeled above was used as a substitute. The original device had a higher transconductance and better high frequency performance ($f_t=160$ GHz, $f_{max}=114$ GHz). There are also additional parasitics introduced in the hybrid mounting of the device. This 37 GHz oscillator represents the highest frequency achieved to date for a quasi-optical oscillator using a hybrid mounted three terminal device.

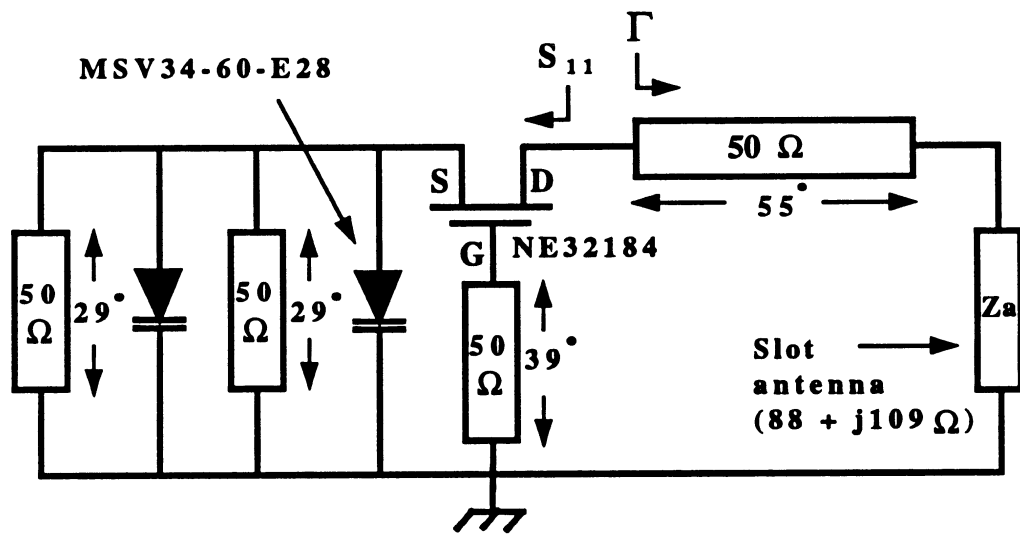
4.5 Voltage Controlled Slot Antenna Oscillator

A VCO (Fig. 4.13,vcopic2) was also designed using the previously described method with the incorporation of varactor diodes (Metelics MSV34-60-E28, see Appendix D.) at the source terminals of the FET. The actual operating frequency of the oscillator near 7 GHz is more than 10% less than the small signal design frequency of 9 GHz due to capacitive parasitics associated with the mounting of the varactors.

The FET is an NE32100 in a plastic package (NE32184). The oscillator was



(a)



(b)

Figure 4.13: Magnitude of S_{11} for different values of control voltage (a) and equivalent circuit (b) for the VCO.

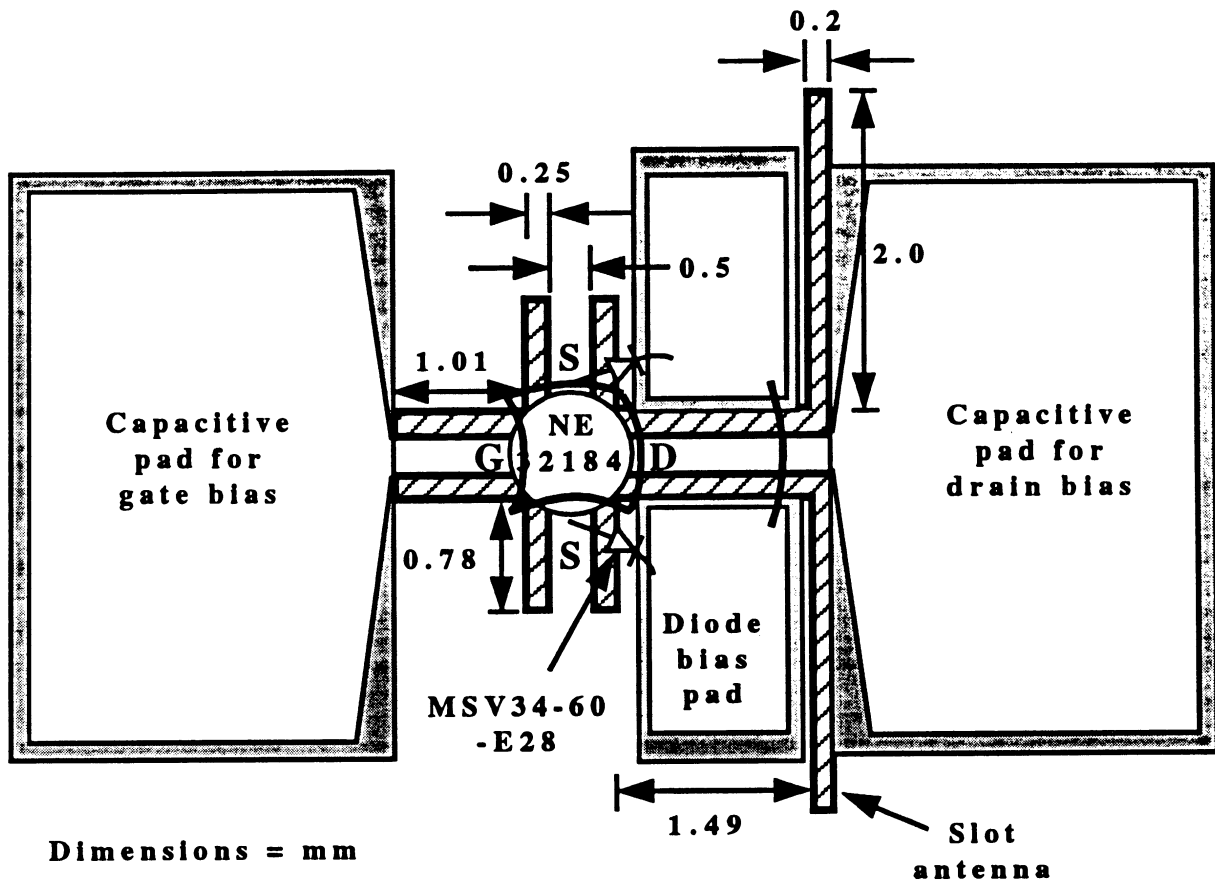


Figure 4.14: CPW layout for the 7 GHz VCO.

placed on a large styrcast block ($\epsilon_r = 12$) for operation because no lens with the large dimensions required at this frequency was available in our laboratory. Since pattern measurements were not possible, the output power was sampled with a standard gain horn pointed at the back (air side) of the antenna. This provides a good measure of the relative output power of the oscillator as it is tuned electronically since the radiation pattern of the slot antenna does not change much over the operating frequency range. There is less than 2 dB variation in output power over a 400 MHz range from 6.85 GHz to 7.25 GHz (Fig. 4.15). This shows that electronically tunable slot-oscillators are

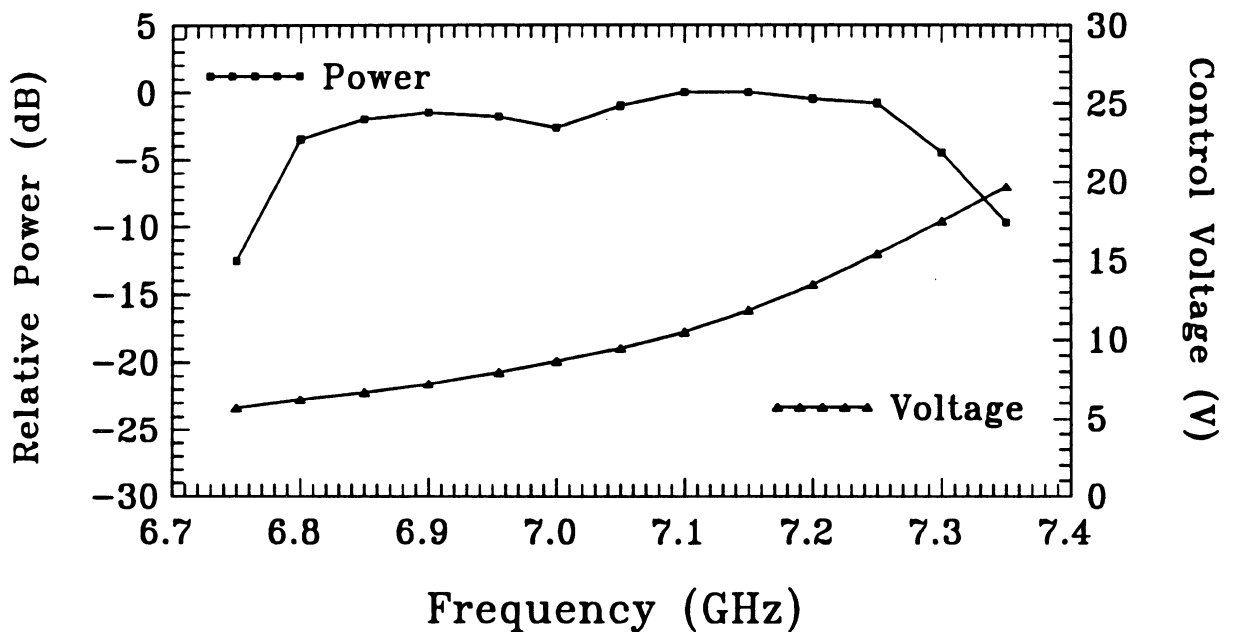


Figure 4.15: Relative power and control voltage vs. frequency with less than 2 dB power variation over a 400 MHz range.

possible for phase locked loops or other applications. The actual operating frequency of the oscillator near 7 GHz is more than 10% less than the small signal design frequency of 9 GHz due to capacitive parasitics associated with the mounting of the varactors. The tuning range is less than what is predicted by linear small signal modeling due to differences encountered as large signal conditions are reached.

4.6 Quasi-Optical Oscillators as Self Oscillating Mixers

Due to the nonlinear nature of oscillating devices, quasi-optical oscillators also act as self oscillating mixers [66, 67]. These can then be used as very low cost Doppler speed sensors or motion detectors which combine transmitter, and receiver in a single device coupled to an antenna. The slot-antenna oscillator presented in this work has demonstrated the ability to function as a Doppler speed sensor. The two element power combining array presented in Chapter 6 has also been used as a Doppler vector receiver due to the phase difference between the two elements. Thus it becomes possible to detect the relative speed of a moving target and indicate if it is approaching or retreating with a simple and inexpensive system.

CHAPTER V

MONOLITHIC 155 GHz AND 215 GHz SLOT ANTENNA TRANSISTOR OSCILLATORS

In this chapter the high frequency capability of the CPW-fed slot antenna oscillator [71, 72] described in Chapter 4 is demonstrated with the construction of monolithic quasi-optical oscillators at 155 GHz and 215 GHz. These oscillators verify the high frequency capability of an InP based high electron mobility transistor (HEMT) developed by Hughes Malibu Research Laboratory, and are suitable for spatial power combining arrays which will be discussed in the next chapter. The output signals were detected with an interferometer in front of an InSb hot electron bolometer [68] and accurate frequency measurements were obtained by heterodyne detection using a wideband quasi-optical harmonic mixer-receiver. These circuits represent the highest frequency oscillators achieved to date for a fundamental source using a three terminal device.

5.1 Design

The quasi-optical oscillator design (Chapter 4) uses a slot antenna fed by a coplanar waveguide (CPW) transmission line. The resulting uniplanar circuit requires no via holes and is compatible with the integration of high speed transistors. Parasitics from bond wires or other mounting techniques are completely eliminated when the

transistor and circuit are fabricated monolithically on the same chip. This allows oscillators to be designed to the highest frequency limit of the device. The oscillator is placed on a dielectric substrate lens for proper operation. The substrate lens simulates an infinite dielectric medium, eliminates power loss to substrate modes, and results in a unidirectional pattern (Chapter 1). The antenna impedance in this environment is accurately calculated using the space domain integral equation technique, a full wave method of moments approach (Chapter 4). The antenna impedance is used as a parameter in the oscillator design resulting in a reduction in the size of the oscillator and overall circuit simplification.

The transistor used is an AlInAs-GaInAs InP based HEMT fabricated at Hughes Malibu Research Laboratory [69]. The device employs a self aligned T-gate defined by an electron beam process. The gate length is $0.05 \mu\text{m}$ and the gate width is $10 \mu\text{m}$. During the oscillator design process, no $10 \mu\text{m}$ gate width device had been tested at microwave frequencies. A larger device with a $50 \mu\text{m}$ gatewidth had been fabricated and tested to 40 GHz. An equivalent circuit was extracted at Hughes using the technique described in [70] and the results were mathematically scaled for the smaller $10 \mu\text{m}$ device. The scaled device model and the simulated gain versus frequency for the $10 \mu\text{m}$ device is shown in Fig. 5.1. The device has a simulated unity current gain transition frequency (f_t) of 300 GHz, a unity voltage gain transition of 544 GHz, and a maximum oscillation frequency (f_{max}) of 738 GHz. The gain calculations show some peaking before the transitions through unity which indicates that there may be problems with using the equivalent circuit close to f_{max} . Since it was derived from measurements on a $50 \mu\text{m}$ device, a large uncertainty exists in the $10 \mu\text{m}$ device model parameters. The parasitic elements L_g , L_d , L_s , C_{pgs} , C_{pgd} , and C_{pds} associated with the extrinsic contact metallizations are known to about $\pm 5\text{pH}$ or fF which is greater than

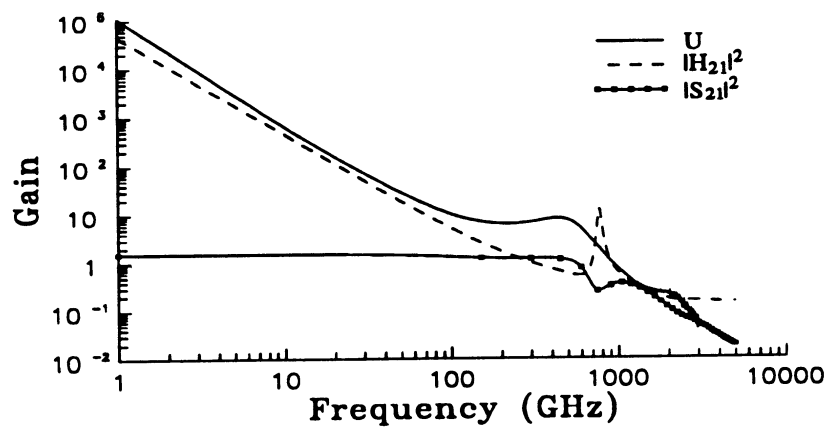
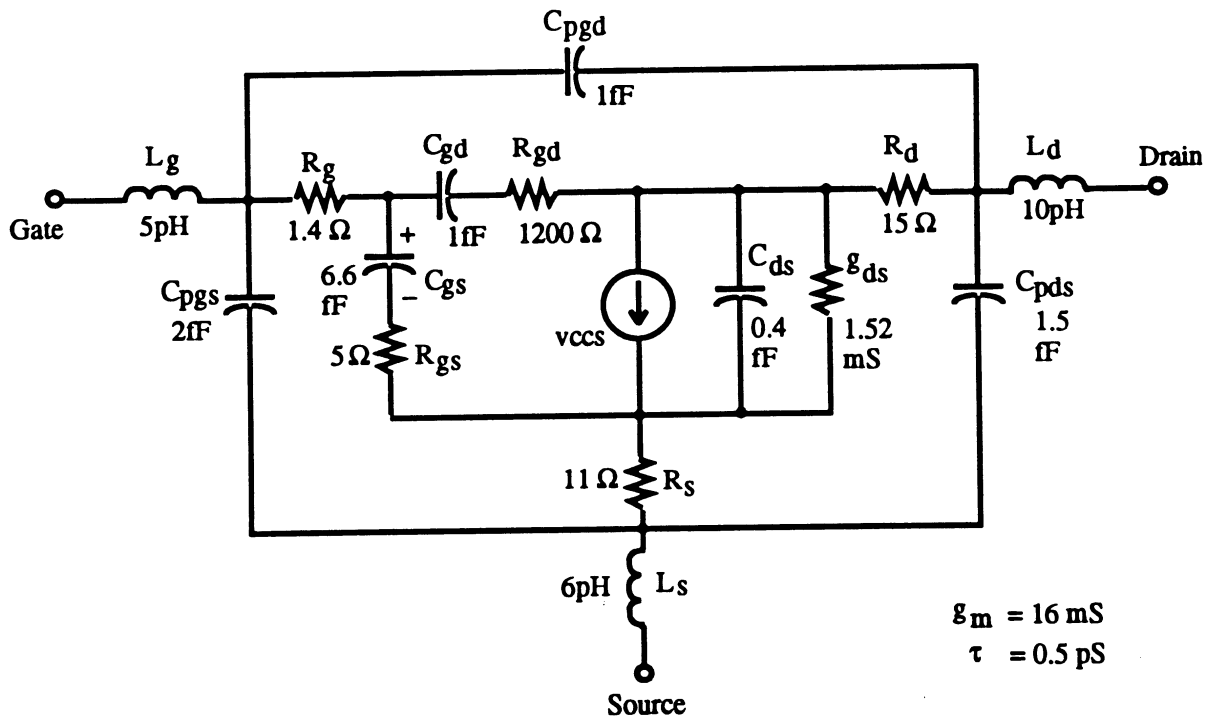


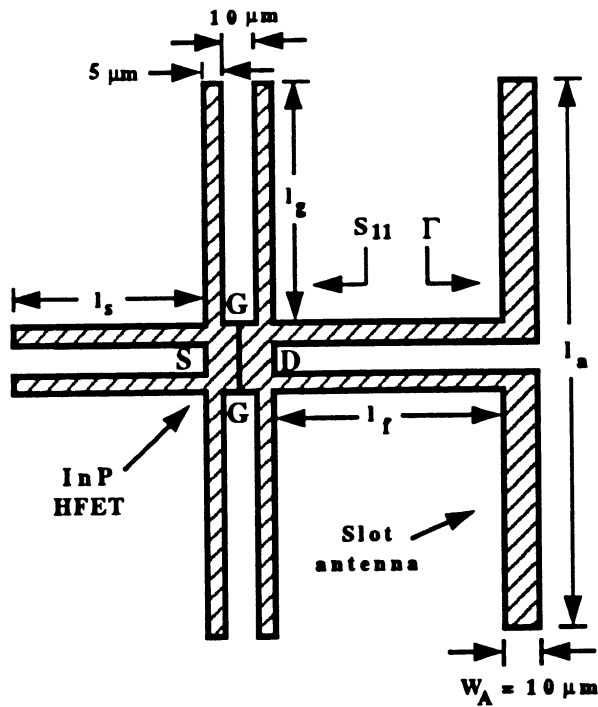
Figure 5.1: Small signal equivalent circuit and simulated gain versus frequency characteristic for the InP based HEMT with $0.05\mu\text{m}$ gate length and $10\mu\text{m}$ gate width.

100% in most cases. Values of the intrinsic elements R_{gs} , C_{gs} , R_{gd} , C_{gd} , g_m , τ , C_{ds} , and g_{ds} are thought to be accurate to $\pm 20\%$. However, DC measurements of the smaller devices indicate that the transconductance is closer to 10 mS than the scaled value of 16 mS (see Fig. 5.1).

The oscillators were designed using the reflection amplifier approach described in Chapter 4. In this case, however, there are two gate terminals with symmetric lengths of CPW transmission line and a single source terminal. The slot antenna is still matched to the drain of the device. Oscillator designs were carried out at frequencies from 150 GHz to 550 GHz. The loss in the CPW lines becomes more significant at these frequencies and was taken into account in the design procedure. All of the CPW lines have a center conductor width of 10 μm and 5 μm giving an impedance of approximately 50 Ω and an effective dielectric constant of 6.7 on an Indium Phosphide substrate. The loss in the lines was estimated by extrapolating data presented in [1, 2]. A conservative value of 0.67 dB/mm at 60 GHz scaled with the square root of frequency was used. Due to the uncertainty existing in the device model, several designs were done at each frequency. The cases considered were with parasitics at their nominal values shown in Fig. 5.1 (low parasitics) and at twice these values (high parasitics). The transconductance was also taken to be either 16mS or 10mS. The simulated figures of merit for the device model under these varying assumptions are summarized in Table 5.1.

Varying the frequency and the model parameters as described above resulted in 28 significant design cases of which 16 were selected by Hughes for fabrication. The CPW layout for the oscillator circuit and the important dimensions for the 16 different designs selected for fabrication are shown in Fig. 5.2.

The transistors were integrated simultaneously with the CPW circuits at Hughes.



F (GHz)	Lp,Cp	g_m (mS)	l_s (μm)	l_g (μm)	l_f (μm)	l_a (μm)	$1/S_{11}$ (mag,ang)	Γ (mag,ang)
150	Low	10	221	177	187.5	390	0.002, -176	0.500, -176
150	Low	16	205.5	183	183.5	390	0.007, -172.6	0.501, -172.6
150	High	10	239	164.5	230.5	360	0.188, 164.4	0.595, 164
150	High	16	291	155.5	112.5	390	0.010, -106	0.514, -106
200	Low	10	176	126	169	270	0.131, 171	0.606, 171
200	Low	16	223	118	132	300	0.010, -168	0.495, -168
200	High	16	194	109	195.5	300	0.010, 112.5	0.486, 112.5
300	Low	16	111.5	76.5	93.5	200	0.022, -172	0.517, -172
400	High	16	9	119.5	89	160	0.098, 133.3	0.477, 133
450	Low	16	29	120	132	70	0.192, 75	0.894, 75
450	High	16	127	99.5	71.5	130	0.157, 173	0.594, 173
500	Low	16	14	111	64.5	160	0.040, 103	0.249, 103
500	Low	16	11	0	79	130	0.074, 111	0.493, 110.5
500	High	16	107	86.5	71	70	0.323, -147	0.897, -146.5
550	Low	16	1.5	0	89.5	60	0.283, 132	0.895, 132
550	Low	16	20.5	74.5	46	120	0.004, -162	0.500, -162

Figure 5.2: CPW circuit layout and oscillator design summary for the monolithic quasi-optical oscillators. Lp,Cp represent the high or low values taken for the extrinsic parasitic inductances and capacitances (L_g , L_d , L_s , C_{pgs} , C_{pgd} , and C_{pds}).

g_m (mS)	Parasitics	$ S_{21} = 1$ (GHz)	f_t $ H_{21} = 1$ (GHz)	f_{max} $G_{max} = 1$ (GHz)	f_{max} $U = 1$ (GHz)
16	low	544	300	738	912
10	low	DC	162	625	672
16	high	388	455	445	906
10	high	DC	135	403	672

Table 5.1: Figures of merit for the InP based HEMT calculated from the equivalent circuit under the different assumptions used in the oscillator designs.

Oscillators were fabricated on each of two InP quarter wafers. Each quarter wafer contains approximately 20 fields and each field contains all 16 selected designs. An additional etch was performed to remove conductive material which exists in the region of the slot antenna and in the gap between the CPW metallizations. Ground plane equalization across the CPW lines is accomplished with an air bridge process. DC biasing of the transistor is made possible by slits in the ground plane which isolate the gate, drain and source. These slits are capacitively bypassed to create an uninterrupted ground plane for the RF circuit. The insulating layer employed in the monolithic circuits is 0.22 μm of silicon monoxide.

5.2 Measurements

The oscillators were positioned on a 2.54 cm diameter approximately elliptical silicon substrate lens for testing. Operational checks and rough frequency measurements were obtained by aligning the oscillators in front of an InSb hot electron bolometer with an interferometer and mechanical chopper in the beam path. The liquid helium cooled InSb bolometer simultaneously provides high sensitivity and wide bandwidth (37.5 GHz-1.5 THz). Two of the designs were found to oscillate at room temperature with about 50% yield. The 150 GHz design case assuming high parasitics and 10 mS

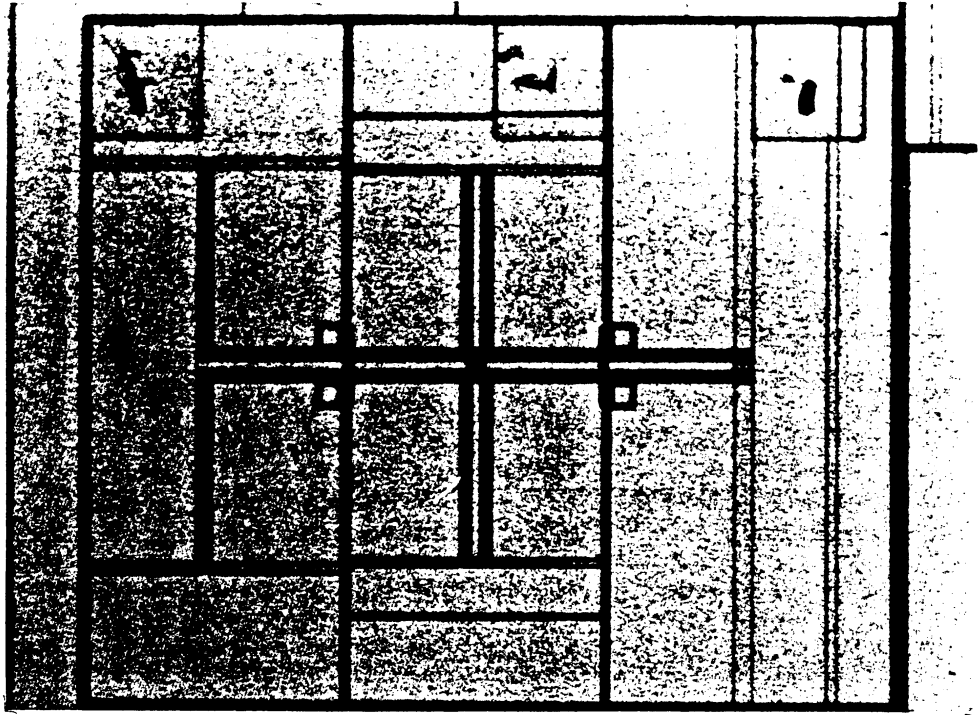
transconductance (150H10) oscillated near its design frequency generating an output signal at 155 GHz. The 500 GHz case assuming high parasitics and 16 mS transconductance (500H16) generated an output at an unexpected frequency near 215 GHz. The other 14 cases generated no output. This situation is not surprising considering the large uncertainty which exists in the device model. The test results for all the successful oscillators are summarized in Table 5.2. Photographs of the 155 GHz and 215 GHz monolithic oscillators are shown in Fig. 5.3.

The oscillator frequencies were accurately measured and their spectrums were observed using harmonic mixers to downconvert the signals. A commercial D-band (110-170 GHz) mixer [73] with a WR-06 rectangular horn was used at 155 GHz (11th and 12th harmonic mixing) but the conversion loss out of band was too high to detect the 215 GHz signal. Both 155 GHz and 213 GHz signals were detected with a wideband quasi-optical harmonic mixer [74, 75] (see Chapters 2,3) using a single forward biased diode for 3rd and 4th harmonic mixing. The setup is shown in Fig. 5.4. A 45 degree wire grid beam splitter is used as a diplexer. Although this introduces a 3 dB loss in the RF and LO paths, it has a wide bandwidth and there is still enough power to detect the signals. The LO frequency was varied to observe both upper and lower sidebands and different IF frequencies were used to insure that the harmonic numbers and RF frequencies are correctly determined. The results of all the heterodyne measurements are summarized in Table 5.3. Downconverted spectrums of a 155 GHz and 215 GHz oscillator are shown in Fig. 5.5. To be certain that the observed signal corresponds to the fundamental oscillation frequency, the LO was adjusted to search for any signals at $1/2$ and $1/3$ of the oscillator frequency and no signals were observed.

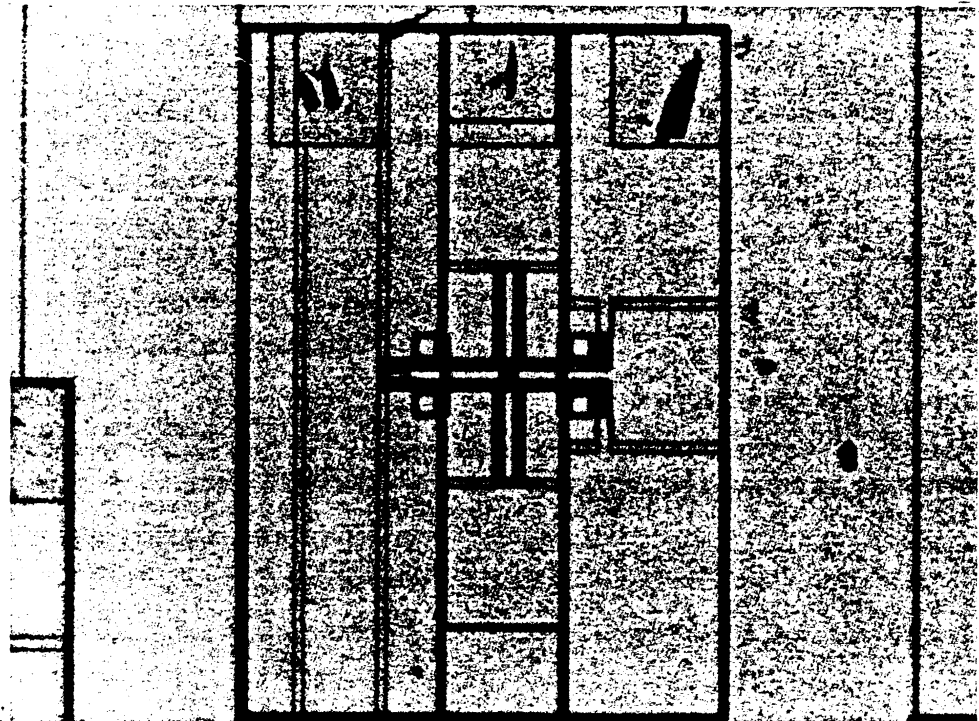
The oscillator output power was estimated with a quasi-optical setup using waveg-

Design	Field	Frequency (GHz)	Bias during oscillation		
			Vg	Vd	Id(mA)
First Wafer					
150H10	4945	153.8	-0.0	0.89	4.3
	4946	152.8	-0.0	0.94	6.5
	4948	152.7	-0.3	1.00	8.7
	4947*	154.0	-0.1	0.98	8.9
	5045	153.4	-0.0	1.00	5.3
	5046	153.5	-0.0	1.00	5.4
	5047*	153.5	-0.2	0.89	6.1
	5146	154.8	-0.0	0.83	5.0
	5147	153.7	-0.0	1.00	7.1
5148	155.0	-0.2	0.93	6.9	
500H16	4947	219.6	-0.1	0.90	7.6
	4948*	209.4	-0.3	1.00	9.0
	5047*	unknown	-0.2	unknown	
	5048*	213.4	-0.4	1.10	7.0
	5147	212.8	-0.3	1.17	5.4
	5146	osc begins		but dies out	
Second Wafer					
150H10	4946	152.4	-0.0	0.89	5.2
	5045	152.0	-0.2	1.00	6.0
	5046	152.0	-0.0	0.92	7.5
	5047	153.2	-0.0	1.00	4.5
	5145	155.9	-0.0	1.00	9.3
	5146	152.4	-0.0	0.87	5.6
	5246	153.0	-0.0	1.00	3.7
500H16	4946	210.1	-0.2	1.00	2.4
	5044	209.2	-0.4	1.10	7.8
	5046	211.6	-0.0	1.0	7.4
	5047	215.5	-0.03	1.10	3.0
	5143	210.0	-0.3	1.06	6.9
	5144	212.6	-0.3	1.07	9.9
	5145	212.2	-0.1	1.10	7.8
	5146	213.4	-0.1	1.10	4.9
	5245	203.0	-0.2	1.10	7.3
5246	208.6	-0.0	1.10	4.4	

Table 5.2: RF test results for all the successful monolithic oscillators using the InSb hot electron bolometer (* indicates a device which ultimately failed during testing).



(a)



(b)

Figure 5.3: Photographs of the successful monolithic oscillator designs, 150H10 operating at 155 GHz (a) and 500H16 operating at 215 GHz (b).

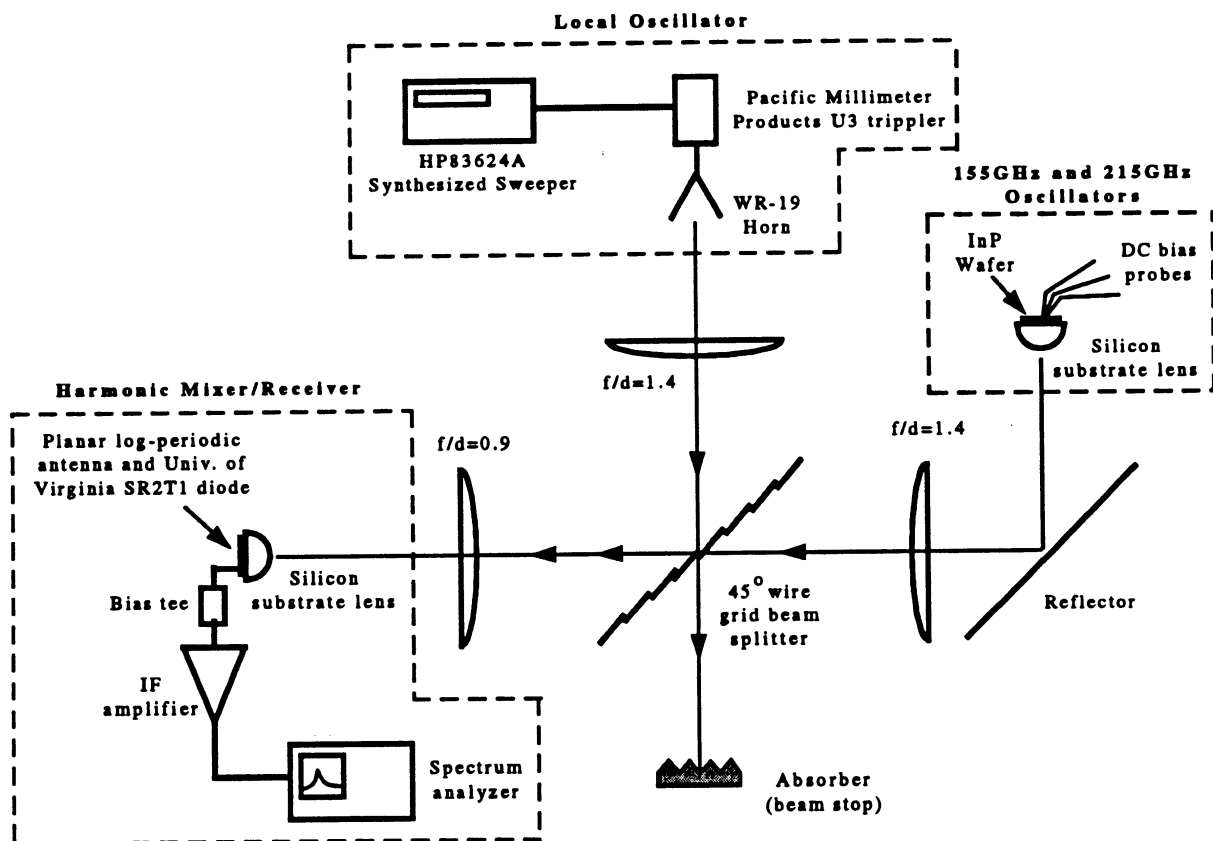
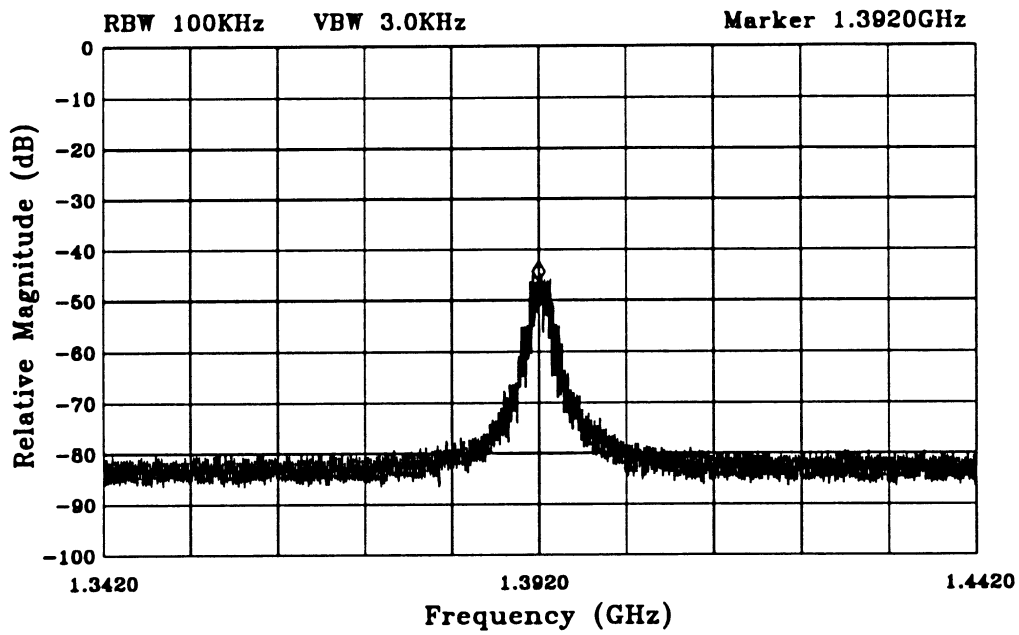


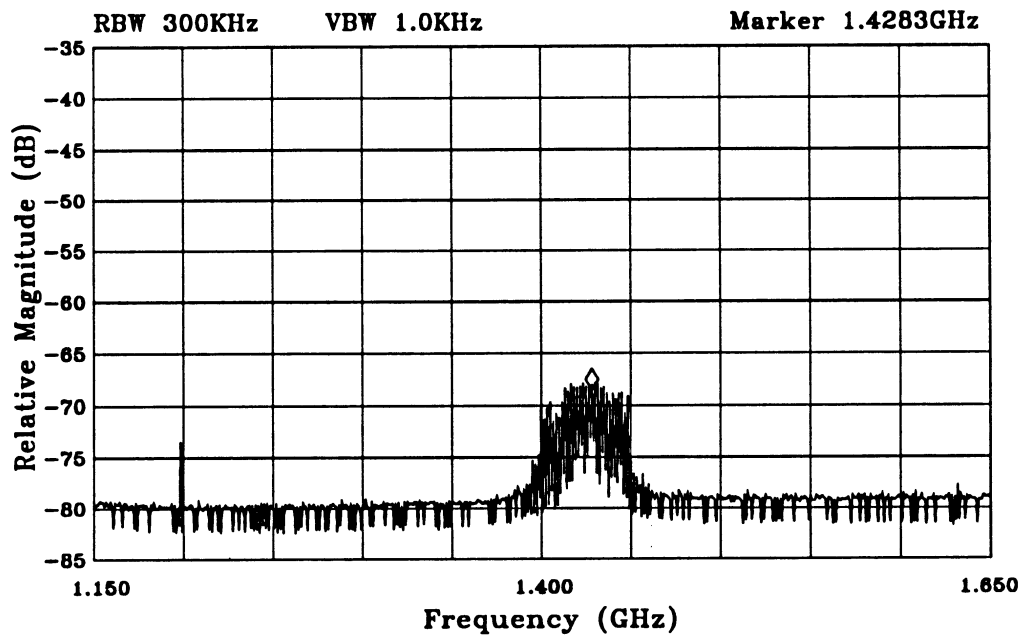
Figure 5.4: Wideband quasi-optical harmonic mixer setup for heterodyne detection of signals from the monolithic slot oscillators.

Oscillator (field)	F_{LO} (GHz)	Harmonic number	F_{IF} (GHz)	RF Sideband	F_{RF} (GHz)
150H10 (4948) wafer 1	51.0517	3	1.393	upper	154.548
	51.9817	3	1.395	lower	154.550
	50.8297	3	2.063	upper	154.552
	52.2050	3	2.068	lower	154.547
150H10 (5047) wafer 1	14.00	11	1.386	upper	155.386
	14.252	11	1.386	lower	155.386
	14.036	11	0.995	upper	155.391
	14.217	11	0.995	lower	155.392
	12.830	12	1.427	upper	155.387
	13.068	12	1.427	lower	155.389
500H16 (4947) wafer 1	52.4715	4	2.4117	upper	212.298
	53.6772	4	2.4117	lower	212.297
	52.6740	4	1.607	upper	212.303
	53.5011	4	1.687	lower	212.317
500H16 (5048*) wafer 1	52.9280	4	1.4117	upper	213.124
	53.6310	4	1.4117	lower	213.112
	52.9766	4	1.2067	upper	213.113
	53.5887	4	1.2233	lower	213.131

Table 5.3: RF test results using heterodyne detection for the two successful monolithic oscillator designs.



(a)



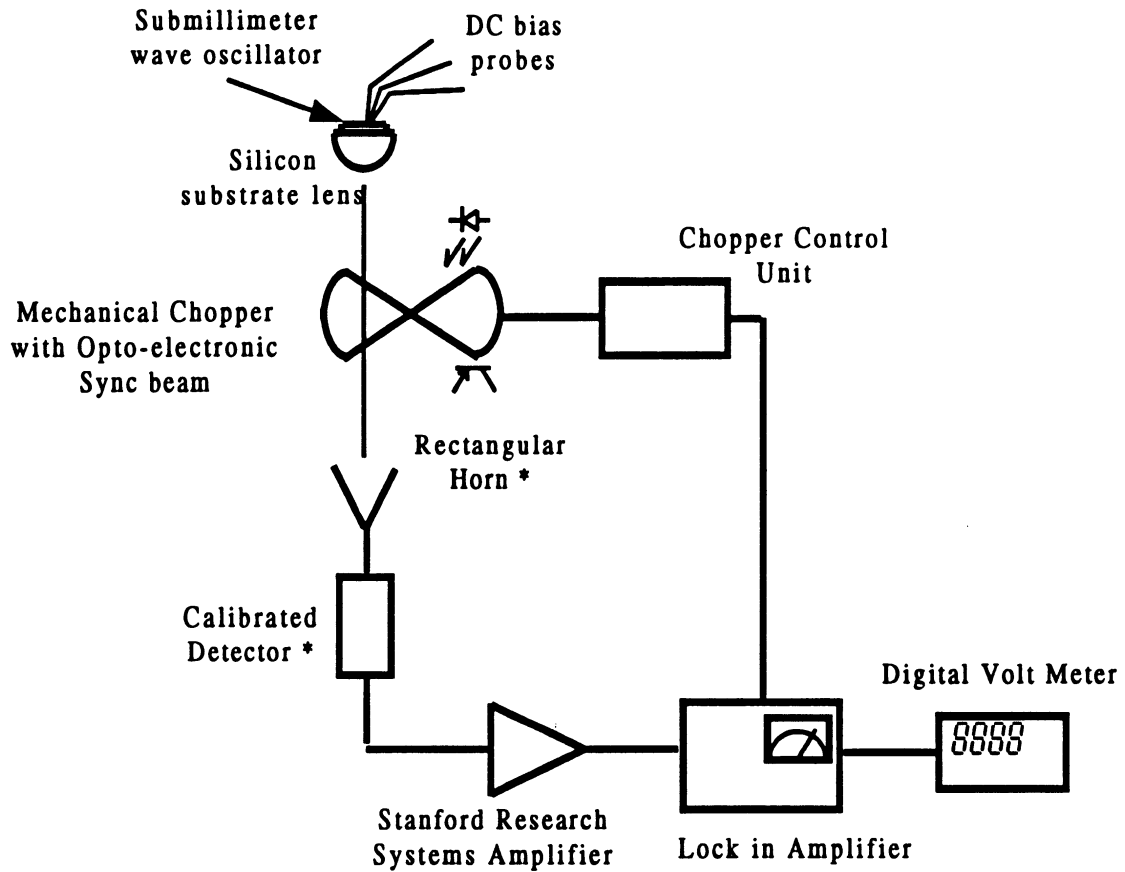
(b)

Figure 5.5: Downconverted spectrums of 155 GHz (a) and 215 GHz (b) monolithic slot antenna oscillators.

uide diode detectors and a lock-in amplifier (Fig 5.6). The waveguide detectors were accurately calibrated using 155 GHz and 215 GHz sources with known output power (Millitech diode multipliers [76]). The slot-oscillator power is determined from the amplitude of the signal at the calibrated detector and the Friis transmission equation. It is not practical to measure the pattern of the oscillator on the substrate lens and therefore its directivity must be estimated. A conservative estimate is made by taking the maximum directivity for an aperture the size of the substrate lens and assuming an aperture efficiency of 40% which includes the electric field taper on the lens surface and the power lost to back side radiation and cross-polarized components (see Chapter 4). Using these estimates, the total output power is found to be no less than $10 \mu\text{W}$ for the 155 GHz oscillator and no less than $1 \mu\text{W}$ for the 215 GHz oscillator. These power estimates are probably running low since the aperture efficiency may be less than 40% and the test system did not allow for mechanical movement of the substrate lens relative to the oscillator during operation to eliminate alignment errors. The corresponding (minimum) DC to RF efficiencies are 0.13% at 155 GHz and 0.014% at 215 GHz. The power measurements are consistent with the fact that the transistor is very small with only a $10 \mu\text{m}$ gate width and the oscillators are operating very close to f_{max} . The circuits were optimized for high loop gain not maximum power (see Chapter 4) and there is a lot of uncertainty in the device model.

5.3 Conclusion

This chapter presents the highest frequencies achieved to-date for quasi-optical oscillators using three terminal devices. A large number of these devices could be used in quasi-optical power combining designs at millimeter wave frequencies to generate milliwatt power levels. The successful development of these monolithic oscilla-



* At 155GHz horn is WR-06 and waveguide detector is Millitech DXP-08
 At 210GHz horn is WR-03 and waveguide detector is Millitech DXW-03

Figure 5.6: Experimental setup for power measurements of the monolithic slot oscillators.

tors demonstrates the high frequency capabilities of the sub-micron gate InP based HEMT which should also find applications as a small signal millimeter-wave and submillimeter-wave amplifier.

CHAPTER VI

POWER COMBINING SLOT ANTENNA OSCILLATOR ARRAYS

All electron devices have capacitance between their electrodes. To operate at higher frequencies, the interelectrode capacitance is reduced by building smaller devices. This reduces the power handling capability. High frequency systems which combine the output power of many individual devices are often used. It has been recognized [20] that free space quasi-optical power combining becomes practical and efficient at millimeter-wave frequencies. Many research groups have achieved successful results with arrays of strongly coupled elements and with arrays of weakly coupled elements [21, 22, 23, 24, 25].

This chapter describes the application of CPW-fed slot antenna oscillators [71, 72] (Chapter 4) in quasi-optical arrays for free space power combining. Small size and compatibility with simultaneous transistor integration [77] (Chapter 5) make the slot antenna oscillator a good candidate for millimeter-wave arrays. The array design follows the approach given by York for weakly coupled oscillators [21]. Two power combining arrays synchronized by mutual coupling between the slot antennas are discussed. The first is a simple two element array consisting of 5.4 GHz slot oscillators operating in free space. The second is a 20 GHz four element array (2x2) placed on

a substrate lens [32] (Chapters 2,3,4,5).

6.1 5.4 GHz Two-Element Array

The two element array presented here demonstrates several important concepts in oscillator array design with a simple system. The frequency of operation in arrays synchronized by weak mutual coupling is determined by the design of the individual elements. The slot oscillators are designed according to the reflection amplifier approach [57, 56] (Chapter 4). The transistors used are NEC 72084 general purpose GaAs MESFETs in plastic packages (see Appendix D). Two identical slot antenna oscillators were fabricated on a very thin printed circuit board substrate to approximate a free space condition. The oscillators share a common CPW line between the inside source terminals to aid in DC biasing but chip capacitors are used to provide an RF short in the middle of the line (Fig 6.1). The slot antenna self impedance and mutual impedance can be calculated in this environment using Booker's relation and standard equations for the equivalent dipole array [40]. The phase of the signal coupled from one oscillator to another is given by the scattering parameter S_{21} which is determined from the impedance matrix ($[Z]$) with standard conversion tables [78]. The voltage coupling (S_{21}) for the slot antennas in the two element array is 0.09 $\angle 47^\circ$. The operating phase difference between the two antennas should be approximately given by the phase of the signal path between them since the oscillators are closely spaced in frequency and have relatively low Q-factors.

The oscillator array exhibited stable operation at a single frequency of 5.4 GHz indicating that the magnitude of the mutual coupling was large enough for synchronization. The measured radiation patterns (Figure 6.2) are consistent with the theoretical pattern for two slot antenna elements operating with a phase difference of 47

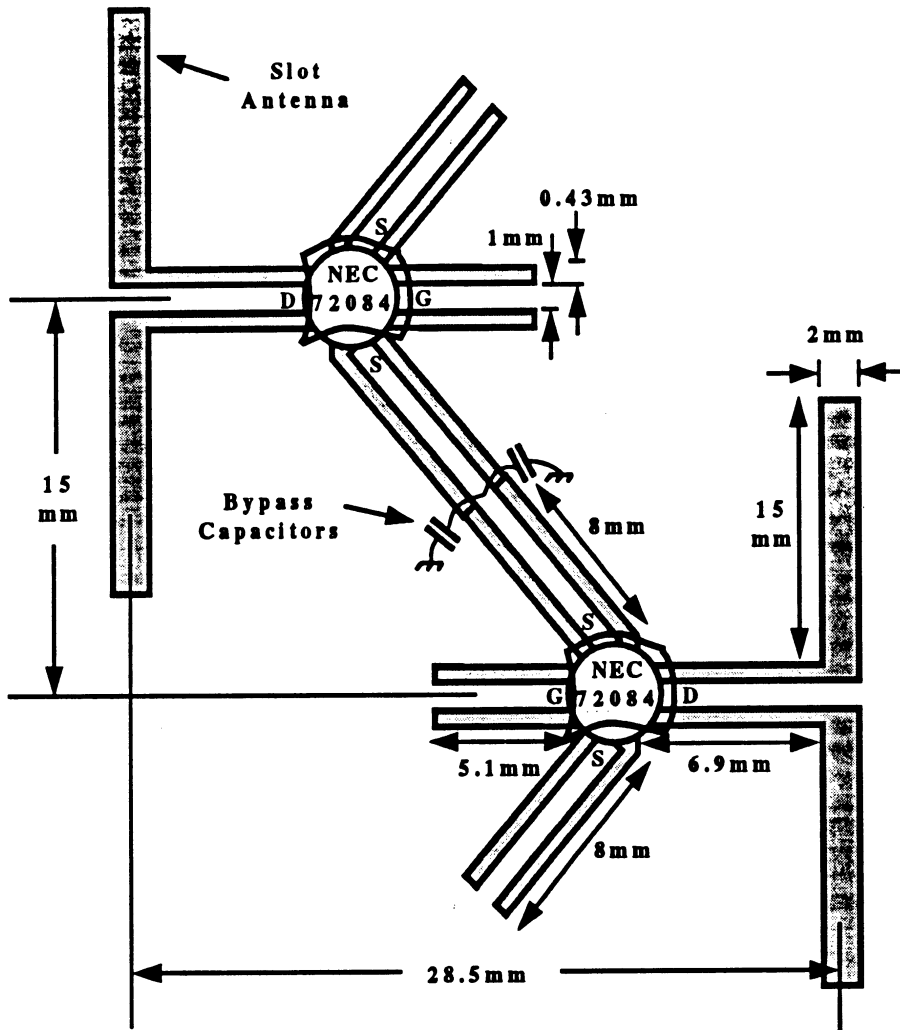
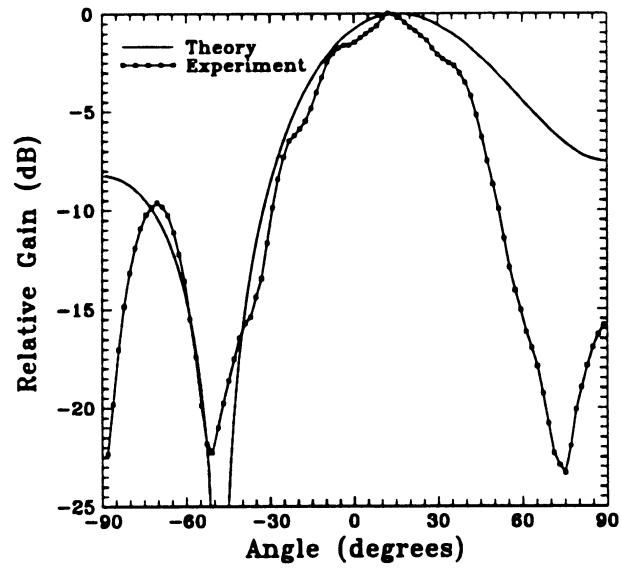
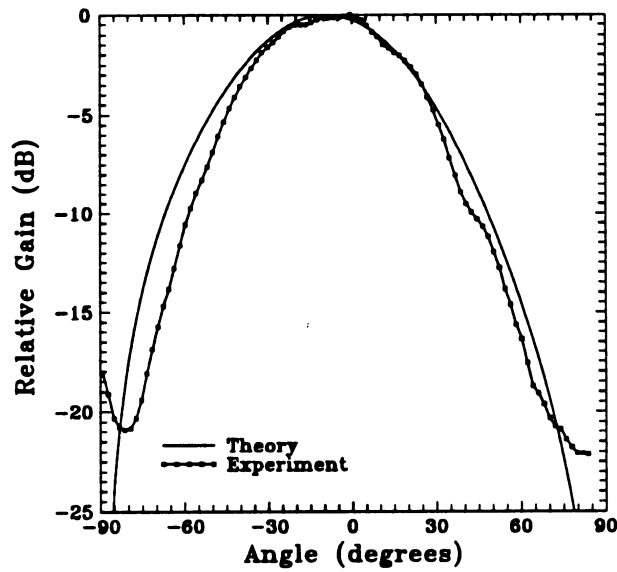


Figure 6.1: 5.4 GHz two element power combining slot oscillator array.



(a)



(b)

Figure 6.2: Measured and theoretical E-plane (a) and H-plane (b) radiation patterns for the two element array.

degrees and a spacing given by the arrangement of the array. The measured E-plane pattern also has false nulls at the pattern edges created by blockage from the mount. The output power is calculated from the measured power at the pattern peak, the theoretical directivity, and the Friis transmission equation [61]. The total radiated power is about 34mW with a DC to RF efficiency of 19%. The array demonstrates a high power combining efficiency of 91% with 18.7 mW radiated by a single oscillator. These values are accurate to about $\pm 5\%$.

Quasi-optical oscillators can be used as self oscillating mixers that combine transmitter and receiver in a low cost Doppler speed sensor. The operating phase difference between the two elements in this array allows it to function as a Doppler vector receiver. By comparing the phase of the two Doppler IF signals it is possible to determine if an object is approaching or retreating. This has been done by observing the trace generated by the two signals on an oscilloscope in X-Y mode and taking note of the rotating direction of the resulting elliptical trace.

6.2 20 GHz Four-Element Array

A four element (2x2) power combining array of quasi-optical slot antenna oscillators has been constructed at 20 GHz. The array elements are identical to the higher power 20 GHz oscillator presented in Chapter 4 except they are redesigned for an alumina substrate ($\epsilon_r = 9.8$) rather than a silicon substrate. The array is placed on an alumina substrate lens for operation. The substrate lens approach provides a planar design that eliminates substrate mode problems and therefore is easily scaled to millimeter-wave frequencies. The substrate lens also increases the directivity providing a high effective isotropic radiated power (EIRP) with a small number of elements. The array delivers a total power output of 68mW with an effective isotropic radiated

power of 4.4W. The DC to RF efficiency of the array is 12%.

6.2.1 Design and Construction

The oscillator element design follows the reflection amplifier approach previously described. The antenna impedance is used as a parameter in the design resulting in a reduction in circuit size and overall simplification. The individual oscillating elements are designed with consideration of the slot antenna self impedance only and mutual coupling in the array is ignored. The circuit is fabricated with 1.5 μm layers of evaporated gold and 2 μm polyimide insulating layers. The transistors used are commercially available microwave power devices (Fujitsu FLR016XV). The transistors are hybrid mounted in the CPW oscillator circuits. Electrical connection to the transistors and the air bridges for ground plane equalization are made with wire bonds. Small slits in the ground plane isolate the gate and drain terminals of the individual transistors in the array so that the DC bias may be applied. The slits in the ground plane are thin (30 μm) and capacitively overlaid to provide an uninterrupted ground plane for the RF circuit.

The array design follows the approach given for weakly coupled oscillators [21]. The coupling parameters between slot antenna elements on a semi-infinite dielectric half space can be calculated using the techniques described by Kominami and Eleftheriades [79, 80]. However, it has been shown [21] that the coupling phases that results in stable modes and in phase power combining for large arrays are $0, 2\pi, 4\pi, \dots$. This would require the oscillators to be placed far apart resulting in grating lobes in the radiation pattern and a low density of radiating elements. In practice, a reflector can be used to adjust the phase of the coupling between an array of closely spaced oscillators. The reflector sets up a cavity mode which equalizes the phase of the elements.

The four element array presented here (Figs. 6.3,6.4) consists of slot antenna oscillators placed as close as possible to each other on an elliptical substrate lens with a movable metal reflector at the back side of the lens. The arrangement of the elements can be extended in two dimensions thus increasing the total number of oscillators. The movable reflector enables the phase of the mutual coupling between the elements to be adjusted creating a free parameter in the locking mechanism. An elliptical alumina substrate lens with a diameter of 5.1 cm ($3.4\lambda_{air}$ at 20 GHz) is used for the array. No antireflection layer or matching cap is used with the substrate lens.

6.2.2 Measurements

The DC bias condition for all of the devices in the array is the same ($V_{gs} = -1V$, $V_{ds} = 6.6V$, and $I_d = 22$ mA per element). With proper alignment of the elliptical substrate lens and reflector, the four oscillators lock to each other and demonstrate single frequency operation at 20.454 GHz. The oscillator array is centered at the back of the substrate lens and the reflector is placed 1.5 mm (about $0.1\lambda_{air}$) behind the active circuit. The array is linearly polarized as given by the orientation of the slot antennas but a small amount of cross-pol does appear due to the lens shape and radiation from the CPW lines. The measured radiation patterns for the array are shown in Figure 6.5. The output power for the array is calculated from the absolute power received by a standard gain horn at the pattern peak, the Friis transmission equation and the directivity. The directivity is calculated from measured patterns (Chapter 4). The value of the front side directivity is reduced by the measured power radiated to the back side (6%) and lost to cross-polarized components (11%). The resulting front side directivity for the array is 18.1 ± 0.2 dB. The total output power for the array is 68 ± 3.4 mW. The corresponding EIRP is 4.4 ± 0.2 W. The measured

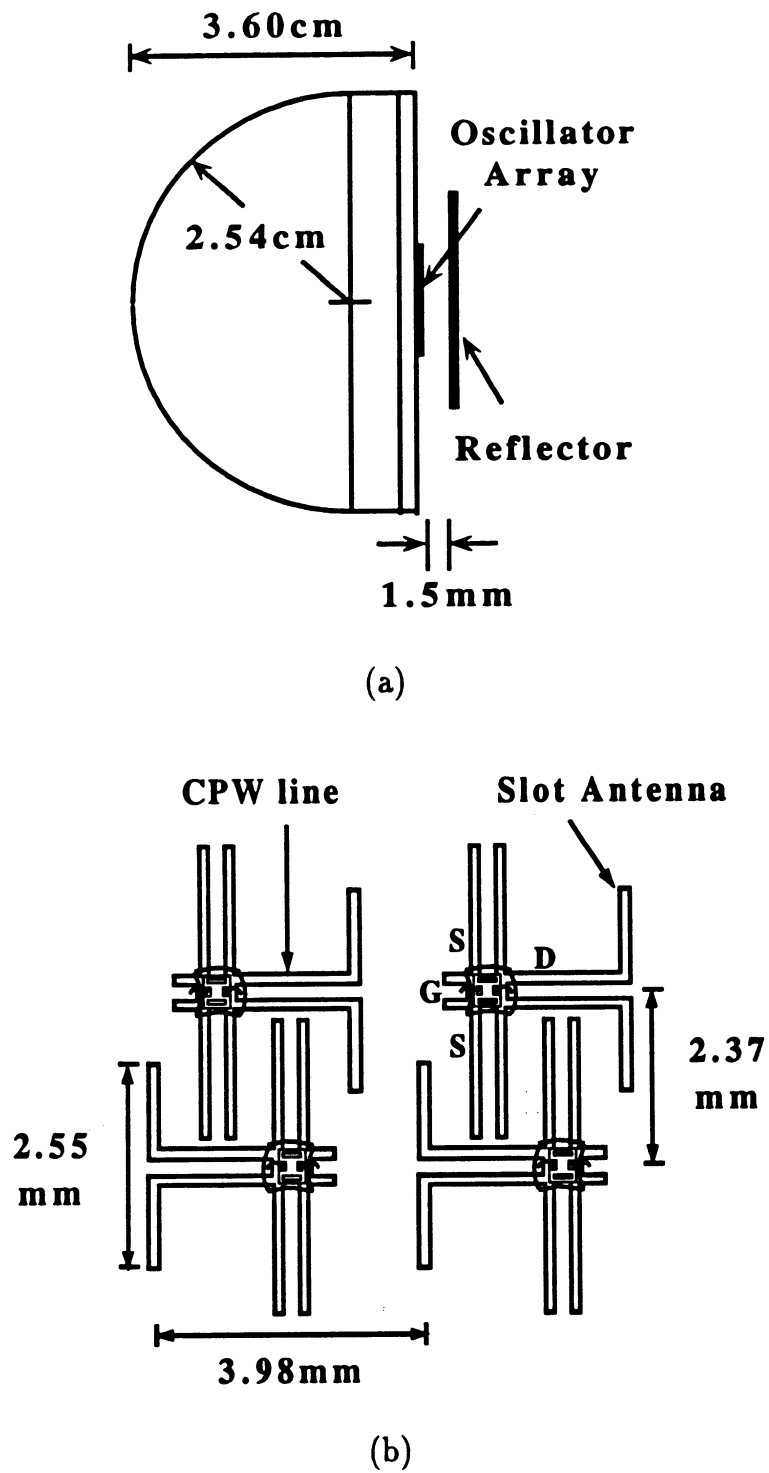


Figure 6.3: Alumina substrate lens (a) and the extendable arrangement of slot oscillators (b) for the four element power combining array.

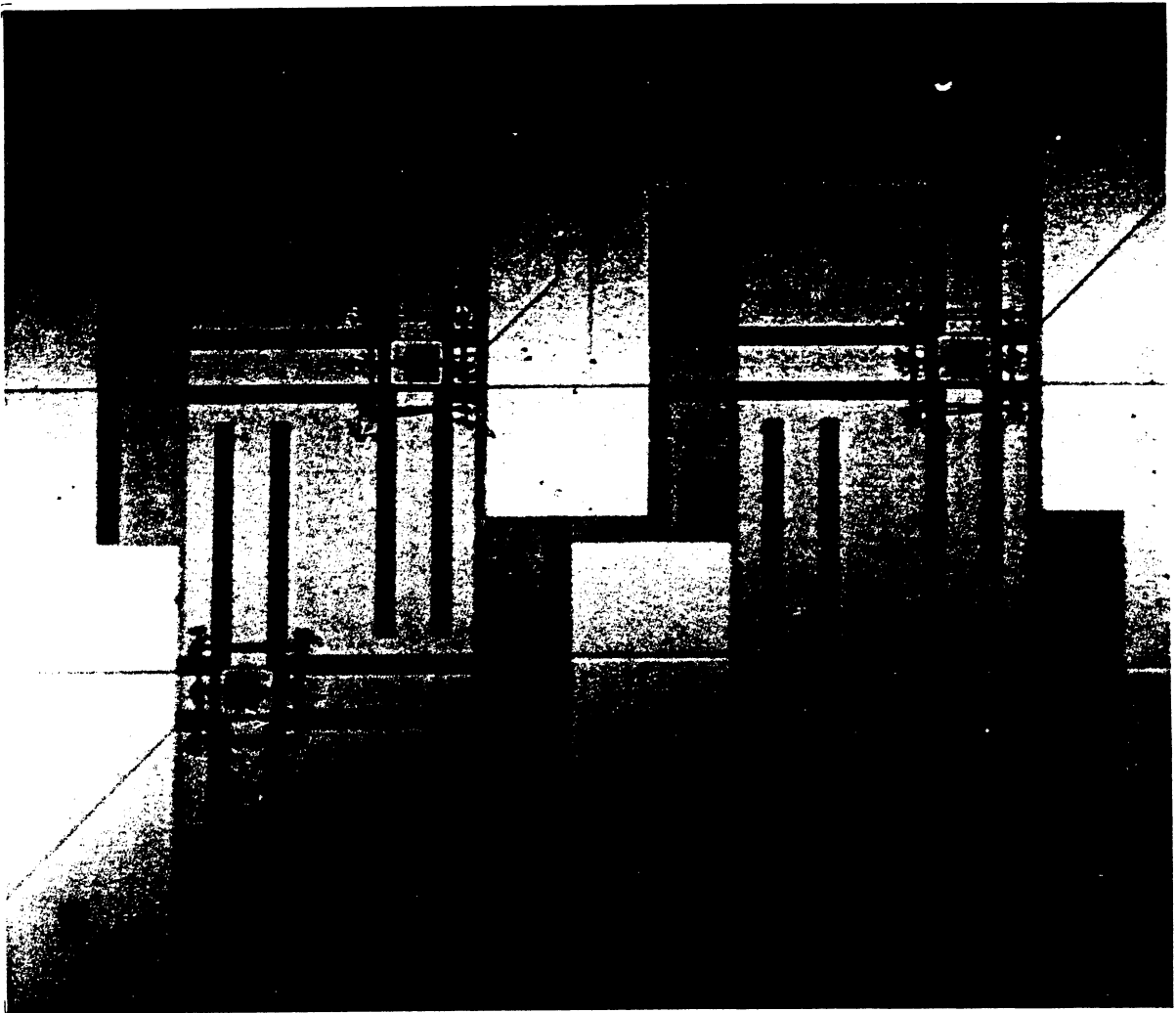
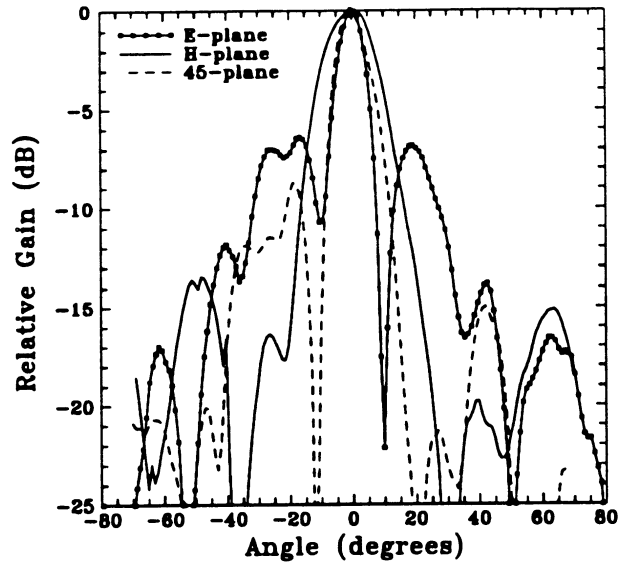
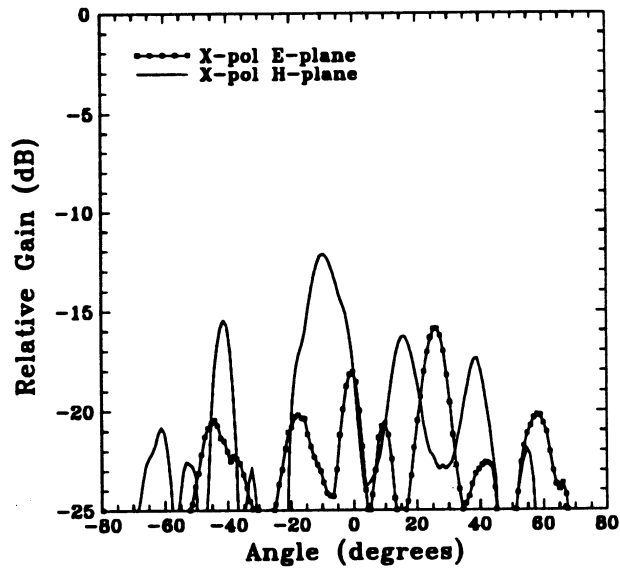


Figure 6.4: Photograph of the 20 GHz four element power combining array of slot antenna oscillators.



(a)



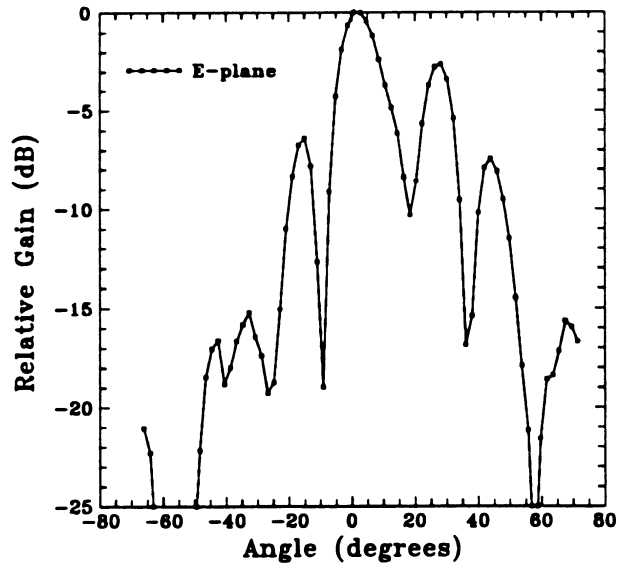
(b)

Figure 6.5: Measured front side co-pol (a) and cross-pol (b) radiation patterns for the four element power combining array.

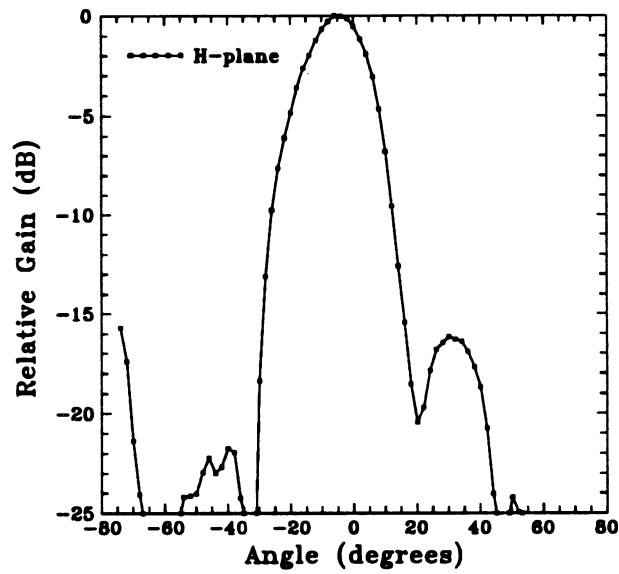
DC to RF efficiency is about 12%. The measured power for a single oscillator of this type is about 17 ± 1 mW [72] (Chapter 4) indicating that the power combining efficiency of the array is near 100%. The theoretical maximum oscillator power for this device is estimated to be about 45-50 mW using the relationships given by Johnson [62]. The theoretical maximum DC to RF efficiency [63] is about 30%. This indicates that it is possible to increase the output power and efficiency by adjusting the effective feedback in the circuit design (see Appendix C).

An indication that the elements are operating in phase is given by the measured patterns for a single oscillator in the array with the antenna on the outside edge (Fig. 6.6). In this case the patterns peaks at an angle away from boresight due to the placement of the antenna away from the lens center. When all four elements are activated and locked together, the measured pattern peaks at boresight indicating that there is no constant phase shift across the array. The array can be operated on hyperhemispherical or extended lenses rather than the elliptical lens. When this is done the rear reflector position must be adjusted and the frequency of operation generally shifts a bit. This indicates that there are weak multiple reflections within the lens which influence the mutual coupling between the elements.

The phase noise of the signal at 100 KHz from the carrier measured with a spectrum analyzer is about -77 dBc/Hz. This value is typical for cavity coupled quasi-optical oscillators and oscillator arrays [24, 21]. The array can be injection locked by introducing a signal quasi-optically into the pattern main beam or by replacing the back side reflector with the flange of an open ended waveguide through which the locking signal can be introduced. With injection locking the phase noise has been reduced to -85 dBc/Hz at 100 KHz from the carrier. The locking bandwidth for the array is 3.2 MHz with an injected power level of $28 \mu\text{W}$ indicating that the external



(a)



(b)

Figure 6.6: Measured E-plane (a) and H-plane (b) radiation patterns for a single element in the array with the antenna on the outside edge.

Q factor is about 130. The free running spectrum and the spectrum under injection locking are shown in Figure 6.7.

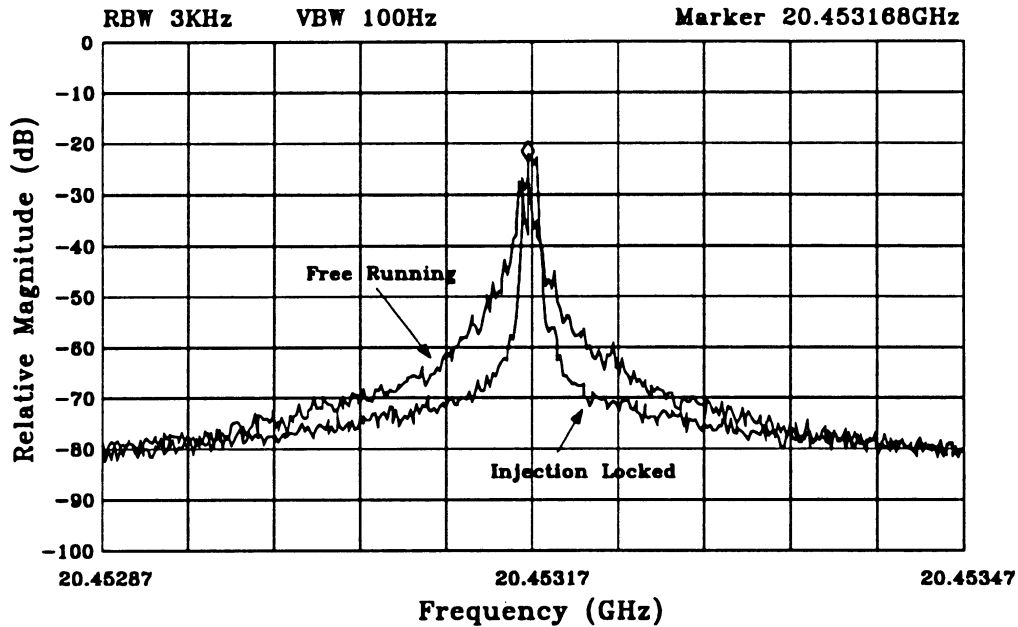


Figure 6.7: Free running and injection locked spectrum of the 4 element power combining array.

6.3 Conclusion

A four element power combining array at 20 GHz has been developed using slot oscillators backed by a substrate lens. The substrate lens approach eliminates power loss to substrate modes and results in a radiation pattern with high directivity (18.1 dB at 20 GHz). The CPW circuit is uniplanar and eliminates the need for via holes and a backing ground plane. Therefore, the design is suitable for medium sized arrays with a high EIRP operating at millimeter-wave frequencies.

CHAPTER VII

CONCLUSIONS AND FUTURE WORK

Practical millimeter-wave receiving and transmitting systems based on active devices directly coupled to antennas have been presented. The systems are planar and suitable for monolithic integration. The designs are free of the mechanical limits imposed by waveguide implementations and are thus suitable for operation into the terahertz region.

7.1 Subharmonic and $2N$ 'th Harmonic Mixer Receivers

The subharmonic and $2N$ 'th harmonic mixer receivers demonstrate the low conversion loss, wide bandwidth and high frequency capability of the planar log-periodic mixing antenna on a substrate lens.

Problems that exist in the system are the variable polarization direction and relatively high cross-pol magnitude of the antenna, the high LO power requirement of the unbiased back-to-back diode pair, and the impedance mismatch between the antenna and the diode pair. Some applications in total power radiometry can tolerate the polarization properties of the antenna used in this work, but subharmonic mixers using different antenna structures need to be investigated if different polarization properties are desired. The high LO power requirement can be reduced by providing

a means of separately biasing the two diodes in the pair. This has been achieved by Lee [81] in a subharmonic log-periodic mixing antenna which shows similar conversion loss with a substantial reduction in required LO power. The impedance mismatch can be reduced by integrating a matching network directly at the antenna terminals. This technique has been successfully demonstrated by Buttgenbach [30] for a log-periodic spiral mixing antenna with SIS detectors.

Future work might include monolithic realizations of the mixing antenna for operation into the terahertz region. This has been demonstrated by Gearhart [19] with a planar log-periodic antenna and a single diode mixer operating at 760 GHz.

7.2 CPW-Fed Slot Antenna Transistor Oscillators

The CPW-fed slot antenna oscillator demonstrates an alternative planar transistor oscillator capable of high frequency operation. Monolithic implementations of the oscillator have been demonstrated and the use of the oscillator in power combining arrays has also been shown.

The main problem with the oscillators presented in this work is the relatively low DC to RF efficiency. This is a consequence of the circuit design and the desire to operate close to the maximum oscillation frequency (f_{max}) for a given device [63]. The circuit design issues of optimum embedding networks and large signal voltage and current limits are addressed in Appendices B and C.

Future work might include the design of slot antenna oscillators which achieve maximum power output for a given device and the construction of larger oscillator arrays. Practical systems which make use of the slot antenna oscillator as a Doppler speed sensor or motion detector might be developed.

APPENDICES

APPENDIX A

Subharmonic Mixer Nonlinear Analysis

This appendix gives a complete listing of the program written to perform the nonlinear analysis of a subharmonic mixer using a back-to-back diode pair. The program is based on a single diode program written by Maas [7] but it is modified to use the symmetry proposed by Kerr [43] for extending the multiple reflection algorithm to a two diode case. The modifications consist of multiplying the LO embedding impedances by two for odd harmonics and setting the LO impedances to zero for even harmonics and DC. The analysis is then conducted for each diode with a 180° phase shift in the LO signal between the two. The frequency conversion matrices for each diode are then combined to create an overall matrix for the diode pair. Two additional parasitic parameters not included in the program written by Maas (parasitic capacitance and inductance) have been added. Modified sections of the program are marked with the # character.

Input to the program is by a text file identical to that of Maas but the two additional parasitics are specified on the first line. An example input file is shown below:

DIODE	6E-17	1.17	4E-15	0.86	0.50	11	295.0	0.0E-9	3.0E-15
VOLTS	1.5	0.0							
FREQS	90E9	1.4E9							
MISCL	100.0	0.025							
ZSIG1	74.0	0.0	74.0	0.0	74.0	0.0	74.0	0.0	
ZSIG2	110.0	0.0	74.0	0.0	74.0	0.0	74.0	0.0	74.0 0.0
ZELO1	100.0	0.0	74.0	0.0	74.0	0.0	74.0	0.0	
ZELO2	74.0	0.0	74.0	0.0	74.0	0.0	74.0	0.0	74.0 0.0

This input file may be used as a test case for the program. The file describes a 180 GHz subharmonic mixer with a SSB conversion loss of 9.56 dB, reverse loss 7.25 dB, LO input impedance of $24.32 - j132.48 \Omega$, RF input impedance of $18.05 - j37.15 \Omega$, and IF output impedance of $108.06 - j1.94 \Omega$. The input and output frequency indices for subharmonic mixing are 2,0.

The program is written in Turbo Pascal, version 5.0 [91] and can be run on an IBM compatible personal computer.

```

#####
## DIODEM6 is a modified version of DIODEM by S.A. Maas as ##
## described below. The modifications cause the program to analyze ##
## a mixer with an antiparallel diode pair using the technique ##
## described by : ##
## ##
## A.R. Kerr "Noise and Loss in Balanced and Subharmonically ##
## Pumped Mixers:Part II-Application" IEEE transactions ##
## Microwave theory and techniques, Vol MTT-27, No.12 Dec 1979 ##
## ##
## Two additional parameters Lp and Cp respectively are added to ##
## the first line of the data file to allow modeling of parasitic ##
## inductance and capacitance. Cp should be the total package C for ##
## both diodes. Cp is appended to the LO embedding impedances ##
## and the LO voltage adjusted downward to maintain Norton ##
## equivalence. The parameter Ls is the whisker or finger ##
## inductance for a single diode which is handled according to the ##
## demands of the symmetry exploited for evaluation in the back to ##
## back case. Both of these parasitics are eventually combined into ##
## the diagonal of the resulting conversion matrix. ##
## In addition Conversion Loss attributable to RF and IF mismatch ##
## are calculated and these are reported along with the intrinsic ##
## conversion loss which may change as ##
## embedding impedances are changed to reduce mismatch losses. ##
## The numeric coprocessor is turned on and the extended type ##
## is used instead of real. ##
#####}

```

{DIODEM: Diode mixer analysis program. Ref: Chapter 4, Microwave Mixers, by S.A. Maas. DIODEM calculates conversion loss and input/output impedance for a single-diode mixer, taking into account embedding impedances at all mixing frequencies and LO harmonics. DIODEM can analyze upconverters, SHP mixers, and modulators as well as conventional downconverters. There are no limitations on range of IF, RF, or LO frequencies.

Data must be entered via a separate file, with the filename extension ".TXT". Input data consists of diode parameters, LO level and bias voltage, frequencies, and embedding impedances. The format is as follows:

```

DIODE IO, eta, Cj0, phi, gamma, Rs, temp(K)
VOLTS peak LO source voltage, Bias voltage
FREQS LO freq, IF freq
MISCL Zc, exit tolerance
ZSIG1 Z-4, Z-3, Z-2, Z-1 (real, im)
ZSIG2 Z0, Z1, Z2, Z3, Z4
ZELO1 Z0, Z1, Z2, Z3
ZELO2 Z4, Z5, Z6, Z7, Z8

```

The first word in each line (DIODE, MISC, etc.) must be written explicitly. phi is the potential and gamma is the exponent for the diode junction capacitance. IF freq is the lowest mixing frequency, whether or not it is the output. Zc is the characteristic impedance of the imaginary transmission line in the reflection algorithm; exit tolerance is the value of the RMS error at which the large-signal algorithm ends. The values following ZSIG1, ZSIG2 are small-signal embedding impedances, in real/imag format. The values following ZELO1,2 are the LO embedding impedances in the same format; a zero must be entered for the imag part of Z0, the DC value.}

```
{$N+} {### Numeric coprocessor on ###}
```

```
CONST
pi = 3.1415926535898 ;
```

```
TYPE
complex = ARRAY [1..2] OF extended ;
waveform = ARRAY [0..127] OF extended ;
short_waveform = ARRAY [0..31] OF extended ; {used in FFT}
freqvector = ARRAY [0..16] OF extended ; {used in FFT}
cmplx_mtx = ARRAY [-4..4, -4..4] OF complex ;
```

{used for conversion matrices}

```

VAR
  vlosource,vbias,L0freq,IFfreq,pwrdis,Idc,Vdc,pavail,pc,L0eff,tolerance,
    conv_loss,rev_loss,x,Input_dBm,Input_power,IM_power : extended ;
  ij,vj,id,vd,c : waveform ;
  j,j8,k,inpfreq,outfreq : integer ;
  Zinsig,Zoutsig,Zin,one,zero,jimag,cmplx,cmplx1,cmplx2,inpzemb,outzemb :
    complex ;
  infile,outfile,vjijfile : text ;
  datafilename,filename,lgsgfilename : STRING [20] ;
  ch1,ch2,ch3,yes_or_no,calc_or_file : char ;
  word : PACKED ARRAY [1..3] OF char ;
  JYconv,jZconv,Yconv,Zconv : cmplx_mtx ;
  skip_lgsg,wants_IM3,save_output : boolean ;
  diode : extended ; {##### diode flag = 1 or -1 #####}
  Ls : extended ; {##### Series inductance #####}
  Cp : extended ; {##### Package or parasitic capacitance #####}
  RFmismatch,IFmismatch,conv_loss_int : extended ; {#####}
  D2pwrdis,D2Vlo,Vdiv,phasemain : extended ; {#####}
  D2Zin : complex ;

{ Global Variables }
IO,dt,temp,eta,phi,cj0,zc,rs,gamma,delta : extended ;
zemblo : ARRAY [0..8] OF complex ;
zembsig : ARRAY [- 4..4] OF complex ;

{$I SCIFUNC5.PAS}      {contains scientific function subroutines}
{$I CMPLXOP5.PAS}     {contains complex arithmetic subroutines}
{$I FFT5.PAS}         {FFT procedure}
{$I CINVERT5.PAS}    {complex matrix inversion procedure}

{*****LARGE-SIGNAL ANALYSIS PROCEDURES*****}

FUNCTION idj(v:extended) : extended ;      {calculates diode I/V}
  BEGIN
    IF v <= 0 THEN
      idj := 0.0
    ELSE IF (v > 0) AND (v < phi) THEN
      idj := IO * (exp(delta * v) - 1.0)
    ELSE IF (v > phi) THEN
      idj := (delta * (v - phi) + 1.0) * IO * exp(delta * phi) ;
      {linear extrapolation}
    END ;
    {prevents convergence problems}

FUNCTION cj(v:extended) : extended ;      {calculates junction capacitance}
  VAR
    denom : extended ;
  BEGIN
    IF v < 0.99 * phi THEN
      BEGIN
        denom := x_tothe_y(1.0 - v / phi,gamma) ;
        cj := cj0 / denom ;
      END
    ELSE
      cj := 10.0 * cj0 ;      {prevents SQRT errors in case v>phi}
    END ;

PROCEDURE Integrate_Diode_Equations(vi:waveform ;
  VAR vr,vd,vj,id,ij,c:waveform) ;
  VAR
    j,j8,jplus1 : integer ;
    vjsav,vjlow,vjhigh,vjest,func,vjint,cint,ijint,dvjint : extended ;
    dvjdt : waveform ;
    outfile : text ;
  BEGIN
    { Estimate and set initial junction voltage }

```



```

IF vi[0] > 0.0 THEN
  BEGIN
    vjlow := 0.0 ;
    vjhigh := 2.0 * vi[0] ;
    vjest := vi[0] ;
    REPEAT
      vj[0] := vjest ;
      func := 2.0 * vi[0] - (rs + zc) * idj(vjest) - vjest ;
      IF func < 0 THEN {vjest is too larg }
        BEGIN
          vjhigh := vjest ;
          vjest := (vjhigh + vjlow) / 2.0 ;
        END
      ELSE IF func > 0 THEN {vjest is too small }
        BEGIN
          vjlow := vjest ;
          vjest := (vjlow + vjhigh) / 2.0 ;
        END
      ELSE
        vj[0] := vjest ;
      UNTIL abs(vjest - vj[0]) < 0.005 ; {#### tol change ##}
      vj[0] := vjest ;
    END
  ELSE
    vj[0] := 2.0 * vi[0] ; { vi[0]<0
{ Integrate diode equations over an LO cycle }
REPEAT
  FOR j := 0 to 127 DO
    BEGIN
      c[j] := cj(vj[j]) ;
      ij[j] := idj(vj[j]) ;
      dvjdt[j] := (2.0 * vi[j] - vj[j] - (rs + zc) * ij[j]) / ((rs + zc)
        * c[j]) ;
      jplus1 := j + 1 ;
      IF j = 127 THEN
        BEGIN
          jplus1 := 0 ;
          vjsav := vj[0] ;
        END ;
      IF ij[j] <= 0.01 * c[j] / dt THEN
        vj[jplus1] := vj[j] + dt * dvjdt[j]
      ELSE { If ij is large, halve the interval }
        BEGIN { gives better numerical stability }
          vjint := vj[j] + 0.5 * dt * dvjdt[j] ;
          ijint := idj(vjint) ;
          cint := cj(vjint) ;
          dvjint := (vi[j] + vi[jplus1] - vjint - (rs + zc) * ijint) /
            ((rs + zc) * cint) ;
          vj[jplus1] := vjint + 0.5 * dt * dvjint ;
        END ;
      END ;
      writeln('Iteration complete in diode eqn subroutine ') ;
      UNTIL abs(vj[0] - vjsav) < 0.005 ; {##### tol #####}
      {Bail out when steady state is reached}
    { Form reverse wave }
    FOR j := 0 to 127 DO
      BEGIN
        id[j] := ij[j] + c[j] * dvjdt[j] ;
        vd[j] := vj[j] + rs * id[j] ;
        vr[j] := vi[j] - id[j] * zc ;
      END ;
      writeln( 'exit integrate_diode_equations' ) ;
    END ;
PROCEDURE LARGE_SIG(vlosource,vbias,tolerance:extended ;
  VAR vd,vj,id,ij,c:waveform) ;
VAR
  err,errchange,ersav,phase : extended ;
  cmplx,cmplx1,cmplx2,vref_freq,new_vinc_freq : complex ;

```

```

prev_vinc,vinc_initial,vinc,vref : waveform ;
coscomp,sincomp : freqvector ;
vref_interp,vinc_interp : short_waveform ;
rho : ARRAY [0..8] OF complex ;
itnum,j1,j,k : integer ;
converged : boolean ;

BEGIN
writeln('entered lgsg') ;
itnum := 0 ;
err := 0.0 ;
ersav := 0.0 ;
converged := false ;

{ Form reflection coefficients, rho[j] }
cmplx[1] := zc ;
cmplx[2] := 0.0 ;
FOR j := 0 to 8 DO
  BEGIN
    csub(zemblo[j],cmplx,cmplx1) ;
    cadd(zemblo[j],cmplx,cmplx2) ;
    cdiv(cmplx1,cmplx2,rho[j]) ;
  END ;

{Calculate initial voltage wave }
cmplx := zemblo[0] ;
cmplx1 := zemblo[1] ;
phase := atan2(cmplx1[2],cmplx1[1] + zc) ;
FOR j := 0 to 127 DO
  BEGIN
    vinc_initial[j] := vbias * zc / (zc + cmplx[1]) + vlosource * zc *
      sin(2.0 * pi * j / 127 - phase) / sqrt(sqrt(zc + cmplx1[1]) + sqrt
        (cmplx1[2])) ;
    {#####}
    vinc_initial[j] := diode * vinc_initial[j] ; {## polarity ##}
    {#####}
    vinc[j] := vinc_initial[j] ;
    prev_vinc[j] := 0.0 ;
  END ;

{ Begin iterative procedure }
REPEAT
  itnum := itnum + 1 ;
  writeln('large-signal iteration no: ',itnum) ;

  { Save old incident wave to use later, in determining convergence}
  FOR j := 0 to 127 DO
    BEGIN
      prev_vinc[j] := vinc[j] ;
    END ;

  { calculate reflected wave, vref }
  integrate_diode_equations(vinc,vref,vd,vj,id,ij,c) ;

  { Test port for large-signal routine: used only in case of problems }
  {Assign(outfile,'trash1.txt');
  rewrite(outfile) ;
  for j:=0 to 31 do
    begin
      j1:=4*j;
      writeln(outfile,vinc[j1]:10:6,vref[j1]:10:6,vd[j1]:10:6,
        ij[j1]:10:6,id[j1]:10:6);
    end;
  close(outfile);}

  { Interpolate reflected wave to minimize FFT time }
  FOR j := 0 to 31 DO
    BEGIN
      k := j * 4 ;
      vref_interp[j] := vref[k] ;
    END ;

```

```

{ FFT to get freq-domain reflected wave }
FFT(vref_interp,coscomp,sincomp,32,5,1) ; {FFT to freq domain}
writeln('thru FFT') ;

{ Multiply by reflection coefficients, rho, to get new freq domain
incident wave }
FOR j:= 0 to 8 DO
  BEGIN
    vref_freq[1] := coscomp[j] ;
    vref_freq[2] := sincomp[j] ;
    cmult(rho[j],vref_freq,new_vinc_freq) ;
    coscomp[j] := new_vinc_freq[1] ;
    sincomp[j] := new_vinc_freq[2] ; {new inc wave in freq domain}
  END ;

{ FFT to get time representation }
FFT(vinc_interp,coscomp,sincomp,32,5,2) ; { FFT to time domain }
writeln('thru inverse FFT') ;

{ Interpolate new time domain waveform
to get a full 128-point waveform }
FOR j := 0 to 31 DO
  BEGIN
    j1 := j + 1 ;
    IF j = 31 THEN
      j1 := 0 ;
    FOR k := 0 TO 3 DO
      BEGIN
        vinc[j * 4 + k] := vinc_interp[j] + (vinc_interp[j1] -
          vinc_interp[j]) * k / 4.0 ;
      END ;
    END ;

{ Add new waveform to original }
FOR j := 0 to 127 DO
  BEGIN
    vinc[j] := vinc[j] + vinc_initial[j] ;
  END ;

{ calculate error function }
ersav := err ;
err := 0.0 ;
FOR j := 0 TO 127 DO
  BEGIN
    err := err + sqr(prev_vinc[j] - vinc[j]) ;
  END ;
err := sqrt(err / 128.0) ;
errchange := abs(ersav - err) ;
writeln('RMS error= ',err:10:6,' Previous RMS error= ',
  ersav:10:6) ;
writeln ;
converged := (abs(ersav - err) < 0.001) OR (err < tolerance) ;
UNTIL converged ; {##### tol #####}
END ;

PROCEDURE LO_prams(vd,id:waveform ;
  VAR Zin:complex ;
  VAR pwrdis,Idc,Vdc:extended) ;

VAR
  cmplx,cmplx1 : complex ;
  vd_interp,id_interp : short_waveform ;
  realv,imagv,reali,imagi : freqvector ;
  j,k : integer ;

BEGIN
  { Calculate diode power dissipation }
  pwrdis := 0.0 ;
  FOR j := 0 to 127 DO
    BEGIN
      pwrdis := pwrdis + vd[j] * id[j] ;
    END ;
  END ;

```

```

    END ;
    pwrdis := pwrdis / 128.0 ;
    { Calculate Zin }
    { Sample vd(t), id(t) in preparation to FFT }
    FOR j := 0 to 31 DO
        BEGIN
            k := j * 4 ;
            vd_interp[j] := vd[k] ;
            id_interp[j] := id[k] ;
        END ;

    { FFT sampled vd & id }
    FFT(vd_interp,realv,imagv,32,5,1) ;
    FFT(id_interp,reali,imagi,32,5,1) ;

    { Form Zin }
    cmplx[1] := realv[1] ;
    cmplx[2] := imagv[1] ;
    cmplx1[1] := reali[1] ;
    cmplx1[2] := imagi[1] ;
    cdiv(cmplx,cmplx1,Zin) ;

    { Get DC current & voltage }
    Vdc := realv[0] * 0.5 ;
    Idc := reali[0] * 0.5 ;
    END ;

    { ***** SMALL-SIGNAL ANALYSIS PROCEDURES ***** }
    PROCEDURE Small_sig(c,ij:waveform ;
        LOfreq,IFfreq:extended ;
        VAR JYconv,JZconv,Yconv,Zconv:cmplx_mtx) ;

    VAR
        j,k,i : integer ;
        cmplx,cmplx1,cmplx2 : complex ;
        csampl,gjsampl : short_waveform ;
        cfreal,cfimag,gjfreal,gjfig : freqvector ;
        omega : ARRAY [ - 4..4 ] OF complex ;
        cfreq,gjfreq : ARRAY [ - 8..8 ] OF complex ;

    BEGIN
        writeln ;
        writeln('Begin small-signal analysis: takes about 15 seconds ') ;
        writeln ;

        { Sample c(t) and ij(t) and form g(t) waveform }
        FOR j := 0 to 31 DO
            BEGIN
                k := j * 4 ;
                csampl[j] := c[k] ;
                gjsampl[j] := delta * ij[k] ;
            END ;

        { FFT c(t) and gj(t) to get frequency components }
        FFT(csampl,cfreal,cfimag,32,5,1) ;
        FFT(gjsampl,gjfreal,gjfig,32,5,1) ;

        { Form complex Fourier coefs of freq-domain junction
            conductance and capacitance. Store as vectors [0..8]
            and throw away higher harmonics }
        cmplx[1] := 0.5 * cfreal[0] ;
        cmplx[2] := 0.0 ;
        cfreq[0] := cmplx ;
        cmplx[1] := 0.5 * gjfreal[0] ;
        cmplx[2] := 0.0 ;
        gjfreq[0] := cmplx ;
        FOR j:= 1 to 8 DO
            BEGIN
                cmplx[1] := 0.5 * cfreal[j] ;

```

```

    cmplx[2] := 0.5 * cfimag[j] ;
    cfreq[j] := cmplx ;
    cmplx[2] := - cmplx [2] ;
    cfreq[ - j] := cmplx ;
    cmplx[1] := 0.5 * gjfreal[j] ;
    cmplx[2] := 0.5 * gjfimag[j] ;
    gjfreq[j] := cmplx ;
    cmplx[2] := - cmplx[2] ;
    gjfreq[ - j] := cmplx ;
  END ;

{ Form omega, the vector of mixing frequencies }
{ omega is complex to aid in multiplications, later }
{ Note that LSB values of omega are negative }
FOR j := - 4 TO 4 DO
  BEGIN
    cmplx[1] := 0.0 ;
    cmplx[2] := 2.0 * pi * (IFfreq + j * LOfreq) ;
    omega[j] := cmplx ;
  END ;

{ Form Zconv, the diode conversion matrix }
{ note that it is [-4..4,-4..4] to match to mixing freq terms }
FOR j := 0 to 8 DO      { row number }
  BEGIN
    FOR k := 0 to 8 DO
      BEGIN
        cmult(cfreq[j - k],omega[j - 4],cmplx) ;
        cadd(cmplx,gjfreq[j - k],Yconv[j - 4,k - 4]) ;
      END ;
    END ;
  cinvert(Yconv,Zconv) ;      {#####}
  writeln ;                  {#####}
  writeln('add Z of Rs and Ls to conversion matrix ') ;
  writeln('prior to combining Y ') ; writeln;
  cmplx[1] := Rs ;          {#####}
  FOR j := -4 to 4 DO      {### add in Rs and Z of Ls   ###}
    BEGIN                  {### prior to inversion to [Y]   ###}
      cmplx[2] := 2.0 * pi * (IFfreq + j * LOfreq) * Ls ;
      cadd(cmplx,zconv[j,j],zconv[j,j])
    END ;
  cinvert(Zconv,Yconv) ;
  IF diode = 1 THEN        {#####}
    BEGIN                  {#####}
      JYconv := Yconv ;    { save the non - augmented matrices }
      JZconv := Zconv ;    { for possible use later }
    END ;
  IF diode = -1 THEN
    BEGIN
      writeln ;
      writeln('2nd time is the charm, Add both diode Y matrices ');
      writeln('                and add in Y of Cp ');
      FOR j := -4 TO 4 DO
        BEGIN
          FOR k := -4 TO 4 DO
            BEGIN
              cadd(JYconv[j,k],Yconv[j,k],cmplx) ;
              Yconv[j,k] := cmplx ;
            END ;
          END ;
        cmplx[1] := 0.0 ;      {#### Y of Cp      #####}
        FOR j := -4 to 4 DO  {#####}
          BEGIN
            cmplx[2] := 2.0 * pi * (IFfreq + j*LOfreq) * Cp ;
            cadd(cmplx,yconv[j,j],yconv[j,j]) ;
          END ;
        END ;
      { Augment with Ze ## }

```

```

        writeln ;
        writeln(' 2nd time , augment total matrix with zembsig ' ) ;
        writeln ;
        cinvert(Yconv,Zconv) ;
        FOR j := -4 TO 4 DO
            BEGIN
                cadd(zembsig[j],Zconv[j,j],zconv[j,j]) ;
            END ;
        { Finally invert to get Yconv, the augmented admittance matrix }
        cinvert(Zconv,Yconv) ;
    END ;
END ;

PROCEDURE SSPrms(inpfreq,outfreq:integer ;
                Yconv:cmplx_mtx ;
                VAR Zinsig,Zoutsig:complex ;
                VAR conv_loss,rev_loss:extended) ;

VAR
    cmplx,cmplx1,cmplx2 : complex ;
    j,k,i : integer ;
    mag,phase,Rload,Rsource : extended ;

BEGIN
    { Calc. conversion loss }
    { Get magnitude of Yconv component }
    com_to_polar(Yconv[outfreq,inpfreq],mag,phase) ;

    { Get real parts of source and load Z }
    cmplx := zembsig[inpfreq] ;
    Rsource := cmplx[1] ;
    cmplx := zembsig[outfreq] ;
    Rload := cmplx[1] ;

    { Calc. conv_loss in DB }
    conv_loss := - 10.0 * ln(4.0 * mag * mag * Rsource * Rload) / ln(10.0) ;

    { Calc. reverse conversion loss the same way }
    com_to_polar(Yconv[inpfreq,outfreq],mag,phase) ;
    rev_loss := - 10.0 * ln(4.0 * mag * mag * Rsource * Rload) / ln(10.0) ;

    { Calc. input impedance }
    cdiv(one,Yconv[inpfreq,inpfreq],cmplx) ;
    csub(cmplx,zembsig[inpfreq],Zinsig) ;
    IF inpfreq < 0 THEN
        Zinsig[2] := - Zinsig[2] ;

    { Calc. output impedance }
    cdiv(one,Yconv[outfreq,outfreq],cmplx) ;
    csub(cmplx,zembsig[outfreq],Zoutsig) ;
    IF outfreq < 0 THEN
        Zoutsig[2] := - Zoutsig[2] ;
    END ;

    { ***** Main Program ***** }

BEGIN
    { Set complex constants }
    zero[1] := 0.0 ;
    zero[2] := 0.0 ;
    one[1] := 1.0 ;
    one[2] := 0.0 ;
    jimag[1] := 0.0 ;
    jimag[2] := 1.0 ;

    { initialize constants }
    save_output := false ;
    skip_lgsg := false ;

    { write header }
    writeln ;

```



```

IF Cp > 0.0 THEN
  BEGIN
    cmplx := Zemblo[1] ; {#### set equivalent Vlo ####}
    cmplx[2] := cmplx[2] - {#####}
      (1/(2*pi*LOfreq*Cp)) ; {#####}
    vlosource := vlosource*(1/(2*pi*LOfreq*Cp))/
      (sqrt(cmplx[1]*cmplx[1] + cmplx[2]*cmplx[2]));
  END
ELSE
  vlosource := vlosource ;

cmplx[1] := 1.0 ; cmplx[2] := 0.0 ; {#### add in Y of Cp to ####}
FOR k := 0 to 3 DO {#### zemblo for odd ####}
  BEGIN {#### harmonics ####}
    cdiv(cmplx,Zemblo[2*k+1],cmplx1) ;
    cmplx1[2] := cmplx1[2]
      + ((2*k+1)*LOfreq)*2*pi*Cp ;
    cdiv(cmplx,cmplx1,zemblo[2*k+1]) ;
  END ;

cmplx[1] := 2.0 ; {##### multiply zemblo by two #####}
cmplx[2] := 0.0 ; {##### for odd harmonics #####}
cmplx2[1] := 0.0 ; {##### and add in Z of Ls #####}
FOR k := 0 to 3 DO {#####}
  BEGIN {#####}
    cmult(zemblo[2*k+1],cmplx,cmplx1) ; {#####}
    zemblo[2*k+1] := cmplx1 ; {#####}
    cmplx2[2] := 2.0 * PI * LOfreq * (2*k+1) * Ls ; {#####}
    cadd(zemblo[2*k+1],cmplx2,zemblo[2*k+1]) ; {#####}
  END ;

FOR k := 0 to 4 DO {#### set zemblo = Z of Ls ####}
  BEGIN {#### for even harmonics ####}
    cmplx[1] := 0.0 ; {## true zero (sign of a man) #}
    cmplx[2] := 2.0 * pi * LOfreq * 2.0 * k * Ls ;
    zemblo[2*k] := cmplx ; {#####}
  END ;

{ Read large-signal data from file if desired }
writeln ;
write('Large-signal data calculated or from file? c/f: ') ;
readln(calc_or_file) ;
writeln ;
writeln ;
IF (calc_or_file = 'f') OR (calc_or_file = 'F') THEN
  BEGIN
    skip_lgsg := true ;
    write('File name: ') ;
    readln(lgsgfilename) ;
    IF (pos('.txt',lgsgfilename) = 0) AND (pos('.TXT',lgsgfilename) = 0)
      THEN
        lgsgfilename := concat(lgsgfilename,'.TXT') ;
    Assign(vjijfile,lgsgfilename) ;
    Reset(vjijfile) ;
    readln(vjijfile) ; { skip the line with the column labels}
    FOR j := 0 TO 127 DO
      BEGIN
        readln(vjijfile,ij[j],id[j],vj[j],vd[j],c[j]) ;
        c[j] := c[j] * 1.0e-12 ;
      END ;
    close(vjijfile) ;
  END ;

{ Do large signal analysis }
{ First calculate the remaining two global constants, dt & delta}
dt := 1.0 / (128 * LOfreq) ;

```



```

delta := 1.1744526e04 / (eta * temp) ;
IF NOT skip_lgsg THEN
    {##### set diode flag 1st diode #####}
    diode := 1 ; {#####}
    large_sig(vsource,vbias,tolerance,vd,vj,id,ij,c) ;

{ Calculate LO parameters }
LO_prams(vd,id,Zin,pwrdis,Idc,Vdc) ;
writeln ; writeln('LO parameters for first diode ') ;
writeln('Zin: Real part= ',Zin[1]:7:2,'      Imag parts= ',Zin[2]:7:2) ;
writeln('Idc (mA) =',1000.0*Idc:8:4,'      Vdc=',Vdc:6:3) ;
cplx := zemblo[1] ;
pavail := sqr(vsource) / (8.0 * cplx[1]) ;
pdc := Vdc * Idc ;
LOeff := (pwrdis - pdc) / pavail ;
writeln('Diode RF power dissipation (mW)=' ,1000.0*(pwrdis - pdc):7:3) ;
writeln('Diode DC power dissipation (mW)=' ,1000.0*pdc:7:3) ;
writeln('Available RF LO power (mW)=' ,1000.0*pavail:7:3,
        'LO Efficiency=' ,LOeff:7:4) ;
{#####}
D2pwrdis := pwrdis ; {### save to create overall ###}
D2Zin := Zin ; {### LO parameters ###}

{ save large-signal results if desired }
{ and set flags for saving small-sig results }
writeln ;
write('Want to write results to a file ? y/n: ') ;
readln(yes_or_no) ;
writeln ;
IF ((yes_or_no = 'y') OR (yes_or_no = 'Y')) THEN
    BEGIN
        save_output:=true;
        write('file name: ') ;
        readln(filename) ;
        IF (pos('.txt',filename) = 0) AND (pos('.TXT',filename) = 0) THEN
            filename := concat(filename, '.TXT') ;
        Assign(outfile,filename) ;
        Rewrite(outfile) ;
    END ;
IF (save_output AND (NOT skip_lgsg)) THEN
    BEGIN
        writeln(outfile,' ij id vj vd c (pf)') ;
        FOR j := 0 TO 127 DO
            BEGIN
                x := c[j] * 1.0e12 ;
                writeln(outfile,ij[j]:9:5,id[j]:10:5,vj[j]:9:4,vd[j]:9:4,
                        x:10:6) ;
            END ;
        writeln(outfile) ;
        writeln(outfile,'Zin: Real parts=',Zin[1]:7:2,'      Imag part=',
                Zin[2]:7:2) ;
        writeln(outfile,'Idc (mA)=' ,1000.0*Idc:8:4,'      Vdc=',Vdc:6:3) ;
        writeln(outfile,'Diode RF power dissipation (mW)=' ,
                1000.0*(pwrdis - pdc):7:3) ;
        writeln(outfile,'Diode DC power dissipation (mW)=' ,1000.0*pdc:7:3) ;
        writeln(outfile,'Available RF LO power (mW)=' ,1000.0*pavail:7:4,
                'LO Efficiency=' ,LOeff:7:4) ;
    END ;

{ Small-signal analysis; generate conv. matrices }
Small_sig(c,ij,LOfreq,IFfreq,JYconv,JZconv,Yconv,Zconv) ;

diode := -1 ; {##### 2nd diode #####}
large_sig(vsource,vbias,tolerance,vd,vj,id,ij,c) ; {#####}
LO_prams(vd,id,Zin,pwrdis,Idc,Vdc) ;
writeln ; writeln('LO parameters for second diode' ) ;
writeln('Zin: Real part = ',Zin[1]:7:2,'      Imag part= ',Zin[2]:7:2);

```

```

writeln('Idc(mA) = ',1000*Idc:8:4,' Vdc= ',Vdc:6:3) ;
cplx := zemblo[1] ;
pavail := sqrt(vlosource)/(8.0 * cplx[1]) ;
pdc := Vdc * Idc ;
LOeff := (pwrdis -pdc) /pavail ;
writeln('Diode RF power dissipation (mW)',1000.0*(pwrdis - pdc):7:3) ;
writeln('Diode DC power dissipation (mW)',1000.0*pdc:7:3) ;
writeln('Available RF LO power (mW) =',1000.0*pavail:7:3,
        'LO Efficiency= ',LOeff:7:4) ;
writeln ;

writeln('LO parameters for both diodes in parallel ') ;
writeln('under 1st harmonic approximation');
D2pwrdis := D2pwrdis + pwrdis ;
cplx[1] := 1.0 ; cplx[2] := 0.0 ;
cdiv(cplx,Zin,cplx1) ; cdiv(cplx,D2Zin,cplx2) ;
cadd(cplx1,cplx2,Zin); cdiv(cplx,Zin,D2Zin) ;
cdiv(cplx,D2Zin,cplx2) ;
cplx[1] := 2.0 ; cplx[2] := 0.0 ;
cdiv(Zemblo[1],cplx,cplx1) ; cadd(cplx1,D2Zin,cplx) ;
cdiv(D2Zin,cplx,cplx1) ; com_to_polar(cplx1,Vdiv,phasemain) ;
D2Vlo := sqrt(abs(D2pwrdis*2/(Vdiv*Vdiv*cplx2[1]))) ;

writeln('Zin: Real part = ',D2Zin[1]:7:2,' Imag part = ',D2Zin[2]:7:2);
writeln('Equivalent LO voltage this system = ',D2Vlo:6:2) ;

writeln('Continue ? (y or n)') ;
readln(yes_or_no);

Small_sig(c,ij,LOfreq,IFfreq,JYconv,JZconv,Yconv,Zconv) ; {#####}

{ Generate performance data }
REPEAT
  writeln ;
  write('Enter input and output frequency indices: ') ;
  readln(j,k) ;
  inpfreq := j ;
  outfreq := k ;
  inpzemb := zembsig[j] ;
  IF j < 0 THEN inpzemb[2] := - inpzemb[2] ;
  writeln('Source impedance: Real part=',inpzemb[1]:6:2,' Imag part=',
          inpzemb[2]:6:2) ;
  outzemb := zembsig[k] ;
  IF k < 0 THEN outzemb[2] := - outzemb[2] ;
  writeln('Load impedance : Real part=',outzemb[1]:6:2,' Imag part=',
          outzemb[2]:6:2) ;
  SSprams(inpfreq,outfreq,Yconv,Zinsig,Zoutsig,conv_loss,rev_loss) ;

  {write small-sig results }
  writeln ;
  writeln('Zin: Real part=',Zinsig[1]:7:2,' Imag part=',
          Zinsig[2]:7:2) ;
  writeln('Zout: Real part=',Zoutsig[1]:7:2,' Imag part=',
          Zoutsig[2]:7:2) ;
  writeln('Conversion loss: ',conv_loss:6:2,' dB') ;
  writeln(' Reverse loss: ',rev_loss:6:2,' dB') ;
  writeln ;
  {#####}
  cplx[1] := 1.0 ; cplx[2] := 0.0 ; {###}
  cdiv(cplx,outzemb,cplx1) ; {###}
  cadd(outzemb,Zoutsig,cplx) ; {###}
  IFmismatch := (outzemb[1]*outzemb[1] + outzemb[2]*outzemb[2])
                * cplx1[1] * 4 * Zoutsig[1] / {###}
                (cplx[1] *cplx[1] + cplx[2]*cplx[2]) ; {###}

```

```

IFmismatch := -10*ln(IFmismatch)/ln(10) ;           {###}
                                                    {###}
cplx[1] := 1.0 ; cplx[2] := 0.0 ;                 {###}
cdiv(cplx,Zinsig,cplx1) ;                          {###}
cadd(Zinsig,inpzemb,cplx) ;                         {###}
RFmismatch := (Zinsig[1]*Zinsig[1] + Zinsig[2]*Zinsig[2]) {###}
              * cplx1[1] * 4 * inpzemb[1] /         {###}
              (cplx[1] * cplx[1] + cplx[2] * cplx[2]) ; {###}
RFmismatch := -10 * ln(RFmismatch)/ln(10) ;         {###}
                                                    {###}
conv_loss_int := conv_loss - RFmismatch - IFmismatch ; {###}
                                                    {###}
writeln('Intrinsic Conversion Loss : ',conv_loss_int:6:2,' dB') ;
writeln('Loss due to RF mismatch : ',RFmismatch:6:2,' dB') ;
writeln('Loss due to IF mismatch : ',IFmismatch:6:2,' dB') ;

IF save_output THEN
BEGIN
  writeln(outfile) ;
  writeln(outfile,'Small-sig results for (',inpfreq,' ',outfreq,')') ;
  writeln(outfile) ;
  writeln(outfile,'Zin: Real part=',Zinsig[1]:7:2,'      Imag part=',
              Zinsig[2]:7:2) ;
  writeln(outfile,'Conversion loss: ',conv_loss:6:2,' dB') ;
  writeln(outfile,'  Reverse loss: ',rev_loss:6:2,' dB') ;
  writeln(outfile) ;
  {#####}
  writeln(outfile,'Intrinsic Conv. Loss : ',conv_loss_int:6:2,' dB') ;
  writeln(outfile,'Loss due to RF mismatch : ',RFmismatch:6:2,' dB') ;
  writeln(outfile,'Loss due to IF mismatch : ',IFmismatch:6:2,' dB') ;
  {#####}
END ;
writeln;
write('Want another small-signal run? y/n: ') ;
readln(yes_or_no) ;
UNTIL (yes_or_no <> 'y') AND (yes_or_no <> 'Y') ;
IF save_output THEN
  close(outfile) ;
  close(infile) ;
END.

```

```
{SCIENTIFIC SUBROUTINES FOR TURBO}
{MUST BE SAVED ON THE ROOT DIRECTORY AS "SCIFUNC5.PAS"}
```

```
FUNCTION X_tothe_Y(x,y:extended) : extended ;
  VAR
    j,k : integer ;
  BEGIN
    IF x = 0.0 THEN
      x_tothe_y := 0.0
    ELSE
      x_tothe_y := exp(y * ln(x)) ;
    END ;
  FUNCTION ATAN2(y,x:extended) : extended ;
    BEGIN
      IF x > 0 THEN
        atan2 := arctan(y / x)
      ELSE IF x < 0 THEN
        atan2 := arctan(y / x) + 3.1415926535898
      ELSE IF (x = 0) AND (y > 0) THEN
        atan2 := 1.5707963267949
      ELSE IF (x = 0) AND (y < 0) THEN
        atan2 := - 1.5707963267949
      ELSE IF (x = 0) AND (y = 0) THEN
        atan2 := 0.0
      END ;
    FUNCTION ASIN(x:extended) : extended ;
      BEGIN
        asin := atan2(x,sqrt(1.0 - sqr(x))) ;
      END ;
    FUNCTION ACOS(x:extended) : extended ;
      BEGIN
        acos := atan2(sqrt(1.0 - sqr(x)),x) ;
      END ;
    FUNCTION TAN(x:extended) : extended ;
      BEGIN
        tan := sin(x) / cos(x) ;
      END ;
    FUNCTION SINH(x:extended) : extended ;
      BEGIN
        sinh := (exp(x) - exp(- x)) / 2.0 ;
      END ;
    FUNCTION COSH(x:extended) : extended ;
      BEGIN
        cosh := (exp(x) + exp(- x)) / 2.0 ;
      END ;
    FUNCTION TANH(x:extended) : extended ;
      BEGIN
        tanh := (exp(x) - exp(- x)) / (exp(x) + exp(- x)) ;
      END ;
```

```
{COMPLEX ARITHMETIC SUBROUTINES}
{MUST BE SAVED ON THE ROOT DIRECTORY AS "CMPLXOPS5.PAS"}
```

```
PROCEDURE CADD(a,b:complex ;
              VAR c:complex) ;

  BEGIN
    c[1] := a[1] + b[1] ;
    c[2] := a[2] + b[2] ;
  END ;

PROCEDURE CSUB(a,b:complex ;
              VAR c:complex) ;

  BEGIN
    c[1] := a[1] - b[1] ;
    c[2] := a[2] - b[2] ;
  END ;

PROCEDURE CMULT(a,b:complex ;
              VAR c:complex) ;

  BEGIN
    c[1] := a[1] * b[1] - a[2] * b[2] ;
    c[2] := a[2] * b[1] + a[1] * b[2] ;
  END ;

PROCEDURE CDIV(a,b:complex ;
              VAR c:complex) ;

  VAR
    denom : real ;
  BEGIN
    denom := sqr(b[1]) + sqr(b[2]) ;
    c[1] := (a[1] * b[1] + a[2] * b[2]) / denom ;
    c[2] := (a[2] * b[1] - a[1] * b[2]) / denom ;
  END ;

PROCEDURE CTAN(x:complex ;
              VAR tangent:complex) ;

  VAR
    num,denom : complex ;
  BEGIN
    num[1] := tan(x[1]) ;
    num[2] := tanh(x[2]) ;
    denom[1] := 1.0 ;
    denom[2] := - tan(x[1]) * tanh(x[2]) ;
    cdiv(num,denom,tangent) ;
  END ;

PROCEDURE COM_TO_POLAR(x:complex ;
                      VAR mag,phase:real) ;

  BEGIN
    mag := sqrt(sqr(x[1]) + sqr(x[2])) ;
    phase := atan2(x[2],x[1]) ;
  END ;

PROCEDURE POLAR_TO_COM(mag,phase:real ;
                      VAR x:complex) ;

  BEGIN
    x[1] := mag * cos(phase) ;
    x[2] := mag * sin(phase) ;
  END ;

PROCEDURE CSQRT(x:complex ;
              VAR y:complex) ;

  VAR
    mag,phase : real ;
  BEGIN
    com_to_polar(x,mag,phase) ;
    y[1] := sqrt(mag) * cos(0.5 * phase) ;
    y[2] := sqrt(mag) * sin(0.5 * phase) ;
  END ;
```

```

PROCEDURE FFT(VAR tvct:short_waveform ;
              VAR fvctr,fvcti:freqvector ;
              n,nu,kflag:integer) ;
{MUST BE SAVED ON THE ROOT DIRECTORY AS "FFT5.PAS" }
{ Sin/Cos FFT subroutine based on Ch. 10 " The Fast Fourier Transform"
  by E. Oran Brigham (Prentice-Hall, 1974). Used with permission.

  fvctr is the cosine (a) coefficient: fvcti is the sin (b) coefficient.
  Form of the series is

  f(t)=a0/2 + a1*cos(wt) - b1*sin(wt) + a2*cos(2wt) -b2*sin(2wt) + ...

  and fvctr(0)=DC component, fvctr(n)=nth harmonic, etc. Components must
  be entered with these sign conventions and twice the DC value for a0, as
  implied above. kflag=1 implies time to freq conversion; kflag<>1 implies
  freq to time conversion. Short_waveform is array[0..31] of extended;
  freqvector is array[0..16] of extended.

  n is the number of points in the time waveform (32,max) and must be a
  power of 2. nu=log2(n). kflag=1 for time to frequency transformation;
  anything else gives frequency to time transformation. }

VAR
  m,n2,n2p1,nu1,jj,jk,k,p,k1,k1n2,l,i,loop : integer ;
  treal,timag,c,s,coef,arg : extended ;
  xreal,ximag : ARRAY [1..32] OF extended ;
FUNCTION j_to_the_k(j,k:integer) : integer ;

  VAR
    x,i : integer ;

  BEGIN
    x := 1 ;
    FOR i := 1 TO k DO
      BEGIN
        x := x * j ;
      END ;
    j_to_the_k := x ;
  END ;

FUNCTION ibitr(j,nu:integer) : integer ;

  VAR
    j1,j2,i,x : integer ;

  BEGIN
    j1 := j ;
    x := 0 ;
    FOR i := 1 TO nu DO
      BEGIN
        j2 := j1 DIV 2 ;
        x := x * 2 + (j1 - 2 * j2) ;
        j1 := j2 ;
      END ;
    ibitr := x ;
  END ;

BEGIN
  n2 := n DIV 2 ;
  n2p1 := n2 + 1 ;
  IF kflag = 1 THEN
    BEGIN
      FOR jj := 1 TO n DO
        BEGIN
          xreal[jj] := tvct[jj - 1] ;
          ximag[jj] := 0.0 ;
        END ;
      END
    ELSE
      BEGIN
        FOR jj := 1 TO n2 DO
          BEGIN
            jk := n - jj + 1 ;

```

```

        xreal[jj] := 0.5 * fvctr[jj - 1] ;
        xreal[jk] := 0.5 * fvctr[jj] ;
        ximag[jj] := - 0.5 * fvcti[jj - 1] ;
        ximag[jk] := 0.5 * fvcti[jj] ;
    END ;
    ximag[1] := 0.0 ;
    ximag[n2p1] := 0.0 ;
END ;
nu1 := nu - 1 ;
k := 0 ;
FOR l := 1 TO nu DO
    BEGIN
        REPEAT
            FOR i := 1 TO n2 DO
                BEGIN
                    m := j_to_the_k(2,nu1) ;
                    p := ibitr(k DIV m,nu) ;
                    arg := (p * 6.283185307) / n ;
                    c := cos(arg) ;
                    s := sin(arg) ;
                    k1 := k + 1 ;
                    k1n2 := k1 + n2 ;
                    treal := xreal[k1n2] * c + ximag[k1n2] * s ;
                    timag := ximag[k1n2] * c - xreal[k1n2] * s ;
                    xreal[k1n2] := xreal[k1] - treal ;
                    ximag[k1n2] := ximag[k1] - timag ;
                    xreal[k1] := xreal[k1] + treal ;
                    ximag[k1] := ximag[k1] + timag ;
                    k := k + 1 ;
                END ;
            k := k + n2 ;
        UNTIL k >= n ;
        k := 0 ;
        nu1 := nu1 - 1 ;
        n2 := n2 DIV 2 ;
    END ;
FOR k := 1 TO n DO
    BEGIN
        i := ibitr(k - 1,nu) + 1 ;
        IF i > k THEN
            BEGIN
                treal := xreal[k] ;
                timag := ximag[k] ;
                xreal[k] := xreal[i] ;
                ximag[k] := ximag[i] ;
                xreal[i] := treal ;
                ximag[i] := timag ;
            END ;
        END ;
    IF kflag = 1 THEN
        BEGIN
            coef := 2.0 / n ;
            FOR loop := 1 TO n2p1 DO
                BEGIN
                    fvctr[loop - 1] := xreal[loop] * coef ;
                    fvcti[loop - 1] := ximag[loop] * coef ;
                END ;
            fvcti[n2p1 - 1] := - fvcti[n2p1 - 1] ;
        END
    ELSE
        BEGIN
            FOR loop := 1 TO n DO
                BEGIN
                    tvct[loop - 1] := xreal[loop] ;
                END ;
            END ;
        END ;
    END ;
END ;

```

```

PROCEDURE Cinvert(a:cmplx_mtx ;
                 VAR b:cmplx_mtx) ;

{ MUST BE SAVED ON THE ROOT DIRECTORY AS "CINVERT5.PAS"}

{ Complex matrix inversion program for use with diode_mixer
  Gauss-Jordan reduction without pivoting

  type cmplx_mtx=array[-4..4,-4..4] of complex
  uses scifunc, cmplxops *)
  uses no global variables from the main program
  a is the input matrix; b is the output
  a must be nonsingular and have no zero entries on the main diagonal

  WARNING: this subroutine may not work well in other applications }

VAR
  j,k,i : integer ;
  one,zero,cmplx,cmplx1 : complex ;

BEGIN
  { define constants }
  one[1] := 1.0 ;
  one[2] := 0.0 ;
  zero[1] := 0.0 ;
  zero[2] := 0.0 ;

  { initialize b; complex identity matrix }
  FOR j := - 4 TO 4 DO
    BEGIN
      FOR k := -4 TO 4 DO
        BEGIN
          b[j,k] := zero ;
        END ;
        b[j,j] := one ;
      END ;
      FOR i := - 4 TO 4 DO
        BEGIN
          FOR j := - 4 TO 4 DO
            BEGIN
              { determine multiplying factor }
              IF j <> i THEN
                BEGIN
                  cdiv(a[j,i],a[i,i],cmplx) ;
                  csub(zero,cmplx,cmplx) ;

                  { multiply row and add to all other rows }
                  FOR k := - 4 TO 4 DO
                    BEGIN
                      cmult(cmplx,a[i,k],cmplx1) ;
                      cadd(cmplx1,a[j,k],a[j,k]) ;
                      cmult(cmplx,b[i,k],cmplx1) ;
                      cadd(cmplx1,b[j,k],b[j,k]) ;
                    END ;
                  END ;
                END ;
              END ;
            END ;
          END ;
        END ;
      END ;

  { a is now a diagonal ; normalize it }
  { and do the same to b }
  FOR j := - 4 TO 4 DO
    BEGIN
      FOR k := - 4 TO 4 DO
        BEGIN
          cdiv(b[j,k],a[j,j],b[j,k]) ;
        END ;
      END ;
    END ;
  END ;

```


APPENDIX B

Nonlinear Oscillator Analysis

Nonlinear analysis of the 20 GHz slot antenna oscillator using the FLR016XV K-band power transistor presented in chapter 4 has been carried out with the harmonic balance analysis available in Touchstone/Libra and with Microwave Spice (MWspice) [58]. The Curtice cubic model was used in both simulations [82]. The DC parameters for the model are obtained from curve fitting to the manufacturer supplied DC data. The other model parameters are determined with the following technique. The manufacturer supplied small signal S parameters are modeled with an equivalent circuit like the one described in Chapter 5, however, R_{gd} is not included to remain consistent with the Curtice model. The resistances and capacitances in the intrinsic Curtice model are inferred directly from the corresponding intrinsic element values in the small signal equivalent circuit. The other extrinsic capacitances and inductances from the linear modeling are included as separate circuit elements in the large signal simulations. This technique results in a good approximate model that is useful in simulating oscillator startup and operation (see Fig. B.1).

B.1 Slot Oscillator Simulation with Touchstone/Libra

The harmonic balance analysis available in Touchstone/Libra does not have a transient analysis capability, however, oscillator startup at 20 GHz can be observed

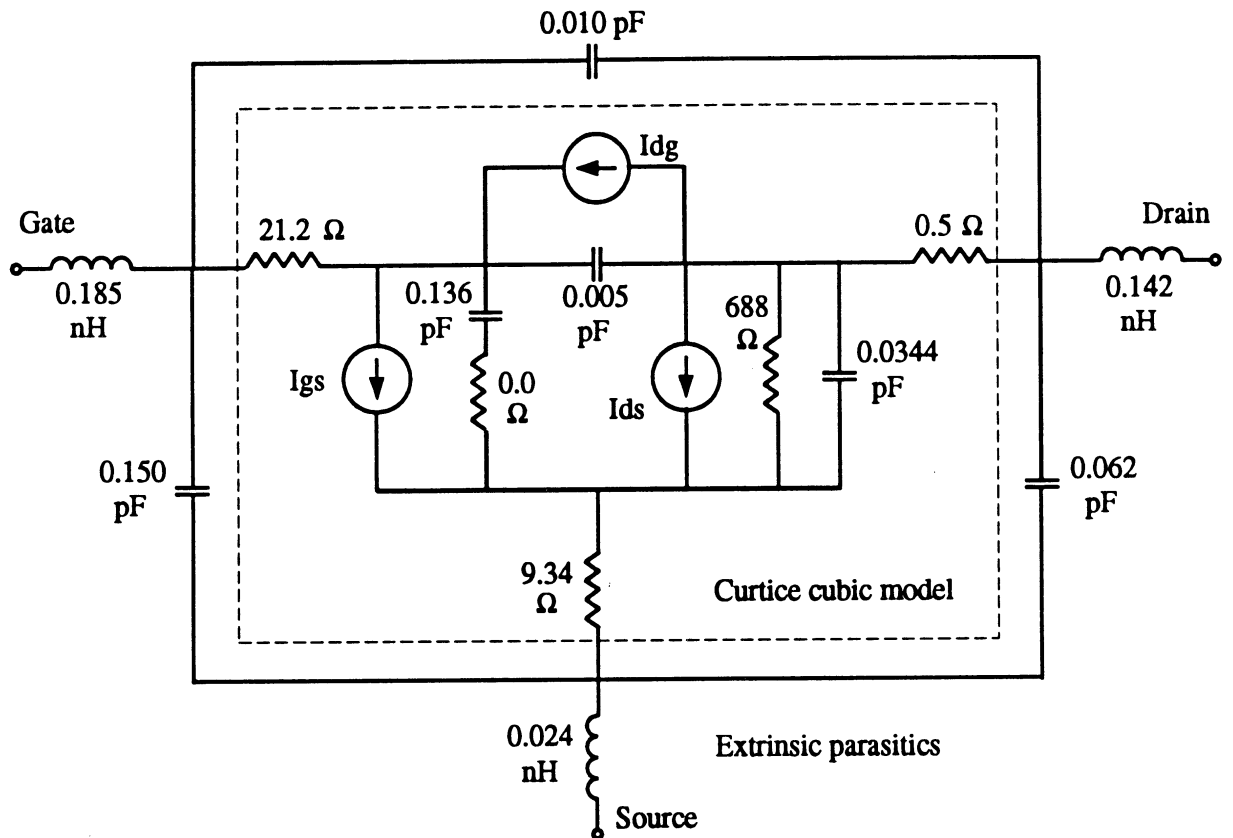


Figure B.1: Nonlinear Curtice cubic model of the Fujitsu FLR016XV (element values determined from S parameters at $V_{ds}=8V$, $I_{ds}=42mA$, DC coefficients $A_0=0.07$, $A_1=0.0486$, $A_2=0.0302$, $A_3=0.0116$, $\beta=0.009$, $\gamma=1.28$ evaluated at $V_{ds}=2V$).

in the slot oscillator circuit by applying a series excitation to the transistor gate with a large magnitude low frequency (500 MHz) voltage source and running the analysis for 50 harmonics. An instability associated with oscillator startup at about 24 GHz is observed around the time when the gate voltage excitation is equal to the value required for normal operation (-1.0 V). A startup frequency of 22 GHz is expected from the original oscillator design based on small signal S parameters. The simulation results are shown in Figure B.2.

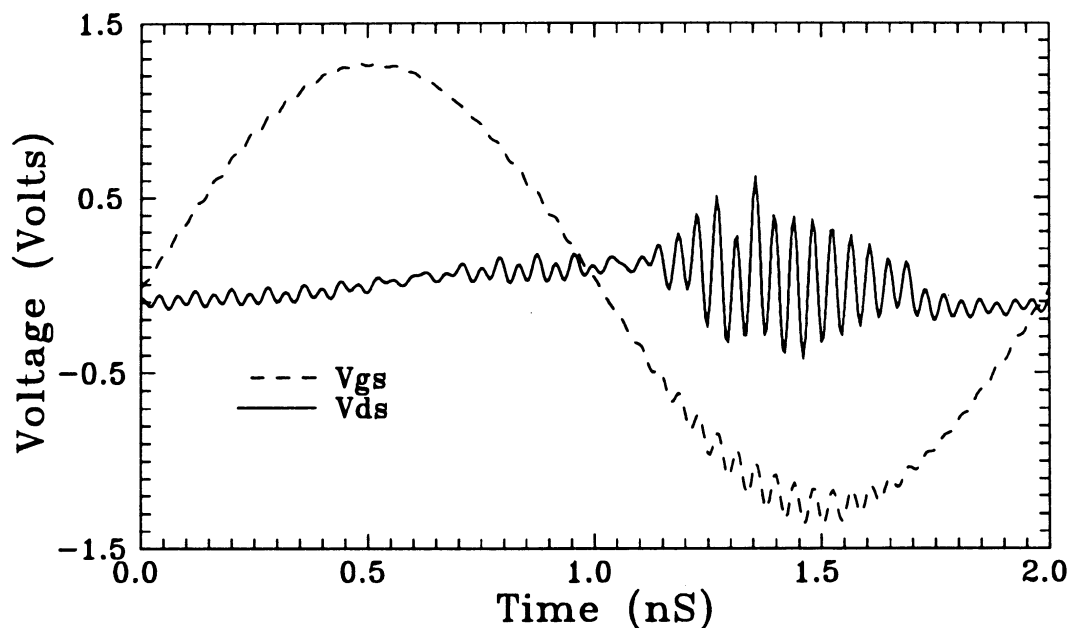


Figure B.2: Simulation of 20 GHz oscillator startup with Touchstone/Libra (AC component of voltages from gate to source and drain to source).

B.2 Slot Oscillator Simulation with Microwave Spice

Microwave Spice has a transient analysis capability and oscillator startup and operation can be simulated directly by providing a current pulse in parallel with the transmission lines at the source terminal of the device in the oscillator circuit

(Chapter 4). Unfortunately Microwave Spice cannot perform the transient analysis when circuit elements are described by external parameter files. This means that a lumped element equivalent to model the slot antenna all the way down to DC must be derived. The equivalent circuit shown in Figure B.3 has been successfully used. The element values in the equivalent antenna circuit are fitted to the one port S

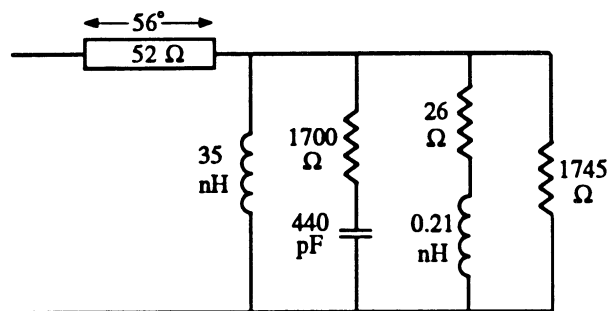


Figure B.3: Slot antenna equivalent circuit used for transient analysis.

parameter data from the full wave SDIE analysis (Chapter 4) using the optimizer in Touchstone/Libra. The Microwave Spice time domain simulation of oscillator startup and operation are shown in Figure B.4. The startup and operating frequency are both about 21.5 GHz. The steady state magnitude of the voltage in the circuit corresponds to a radiated power output of 23 mW. This is close to the experimentally measured value of 17 mW knowing that the simulation does not include losses of any kind.

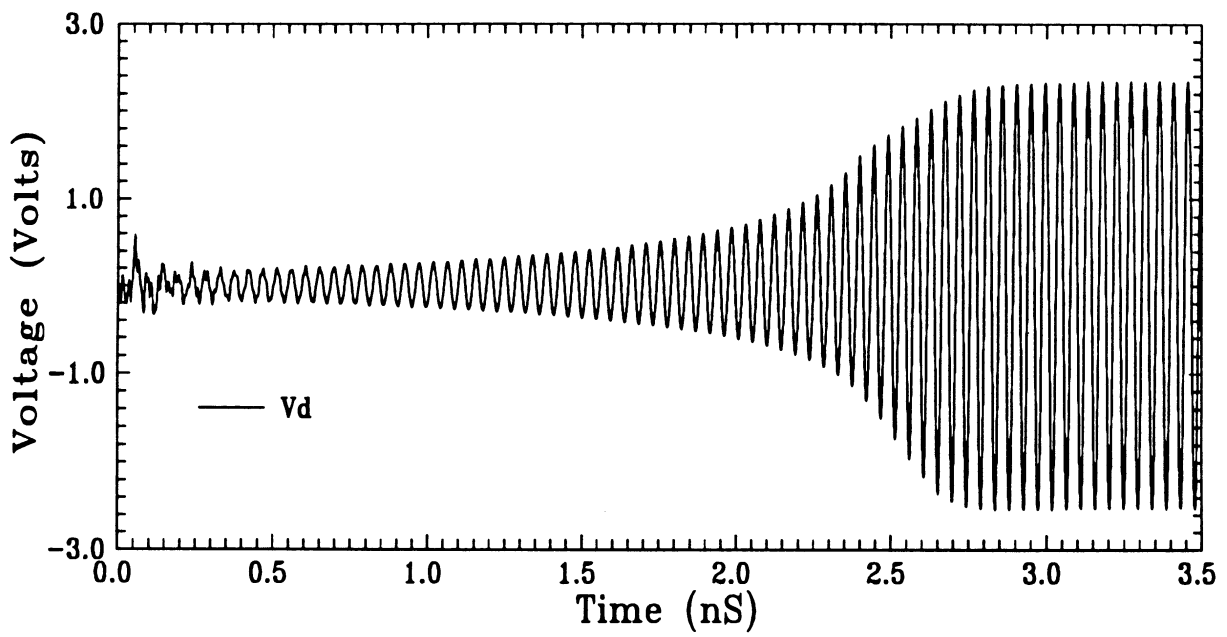


Figure B.4: Simulation of 20GHz oscillator startup and operation with Microwave Spice (AC component of voltage from drain to ground).

APPENDIX C

Oscillator Design for Maximum Power Added Efficiency

This appendix describes a linearized technique for the determination of embedding networks which maximize the added power in a two port oscillator design. The embedding networks are similar to the optimum networks presented by Kotzebue [83] but they are determined here without the assumption of a constant voltage at the input port of the active device. The method presented here will result in a more accurate determination of the embedding networks for maximum power output from a device with a given set of two port parameters.

C.1 The Generalized Oscillator Problem

In the generalized problem of oscillator design using a two-port active device (Fig. C.1), it has been shown [84, 85] that the embedding networks for oscillating systems are those which result in net power flow out of the active device. The total power delivered to the device is given by:

$$P = \frac{1}{2} \text{Re}(\mathbf{V}_1^* \mathbf{I}_1 + \mathbf{V}_2^* \mathbf{I}_2) \quad (\text{C.1})$$

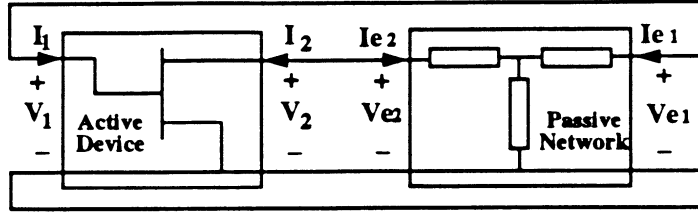


Figure C.1: Equivalent circuit for a generalized two port oscillator design.

where P is negative for net power flow out of the device. The complex ratio of the port 2 voltage (V_2) and the port 1 voltage (V_1) is defined as:

$$\mathbf{A} = A_r + jA_i = V_2/V_1 \quad (\text{C.2})$$

The active device is described by a Y-parameter matrix:

$$\begin{bmatrix} \mathbf{I}_1 \\ \mathbf{I}_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} \mathbf{V}_1 \\ \mathbf{V}_2 \end{bmatrix} \quad (\text{C.3})$$

The total power delivered to the active device can be expressed in terms of V_1 , A_r , A_i and the Y-parameters:

$$P = [g_{11} + g_{22}(A_r^2 + A_i^2) + (g_{12} + g_{21})A_r - (b_{12} - b_{21})A_i] \cdot |V_1|^2 \quad (\text{C.4})$$

where g_{ij} and b_{ij} are the real and imaginary parts respectively of y_{ij} . When $|V_1|$ is assumed to be a constant, the values of the real and imaginary parts of \mathbf{A} which result in the negative minimum of P correspond to the maximum power output from the device. The value of \mathbf{A} which corresponds to this optimum point can be found from the partial derivatives of equation C.1 with respect to A_r and A_i . This value is given by [84, 85]:

$$\mathbf{A}_{opt} = -\frac{y_{21} + y_{12}^*}{2g_{22}} \quad (\text{C.5})$$

When the value of \mathbf{A} is chosen, an embedding network may be synthesized in any one of three series or three shunt configurations given by Kotzebue [83] and shown in Fig.

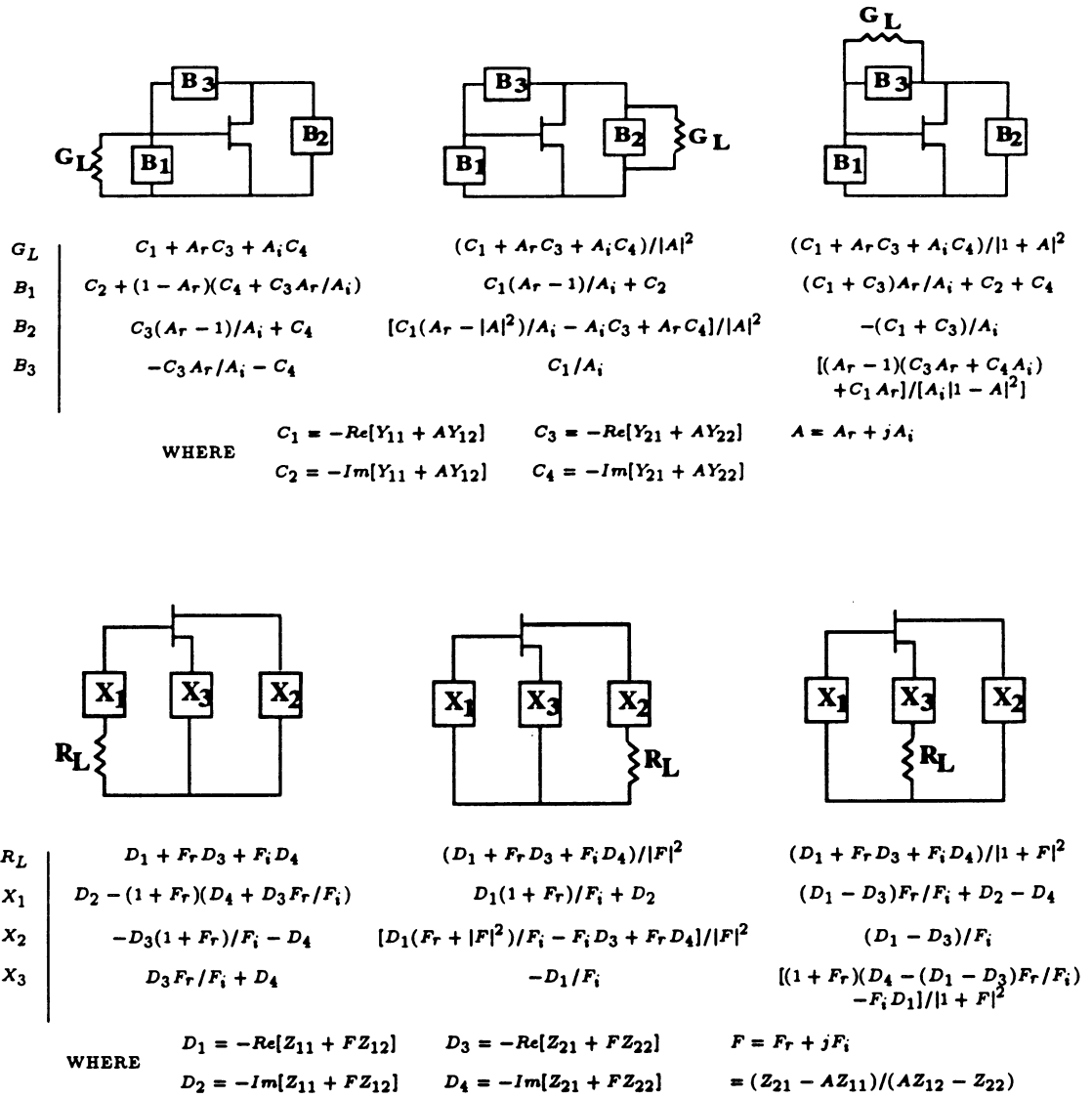


Figure C.2: Three shunt and three series topologies for realizing the optimum embedding networks in an oscillator design.

C.2. The values of the elements are determined with the knowledge that an oscillator at steady state will have the following relationships between the voltages and currents of the active device and the voltages and currents of the embedding network:

$$\begin{aligned} \mathbf{V}_1 &= \mathbf{V}_{e1} & \mathbf{V}_2 &= \mathbf{V}_{e2} \\ \mathbf{I}_1 &= -\mathbf{I}_{e1} & \mathbf{I}_2 &= -\mathbf{I}_{e2} \end{aligned} \quad (\text{C.6})$$

Johnson [62] has indicated that a good starting point for designing the embedding network for an oscillator is to use the Y-parameters of the active device at the gain compression point corresponding to the maximum oscillator power. This value of gain is given by:

$$G_{ME}(\text{max oscillator power}) = \frac{G_o - 1}{\ln G_o} \quad (\text{C.7})$$

where G_o and G_{ME} are the small signal uncompressed, and large signal compressed values, respectively, of the maximum efficient gain defined by Kotzebue [86]. The Y-parameters at this point can be estimated by reducing the transconductance in the equivalent circuit of the active device, or by simply reducing the magnitude of the S-parameter S_{21} until the desired value of gain is obtained [62].

C.2 Maximum Power Added Efficiency

Unfortunately, it is not clear that the magnitude of the port 1 voltage (V_1) will remain constant for all values of \mathbf{A} . A better way to maximize the output power is to determine the value of \mathbf{A} which gives the maximum two-port added power (Eq. C.8) for the oscillating system. The two-port added power is defined as:

$$\text{Added Power} = P_{out} - P_{in} \quad (\text{C.8})$$

The added power in a two-port oscillator design can be maximized by the method described below:

The power delivered to port 2 ($P_2 = -P_{out}$) is taken to be any arbitrary negative constant (power is going out) and the power delivered to port 1 ($P_1 = P_{in}$) which is positive (power is going in) is minimized. Since the phase in the oscillating system is arbitrary, we can select the phase angle of \mathbf{V}_2 to be zero ($\mathbf{V}_2 = V_{2r}$). This establishes a relationship between the real part of \mathbf{I}_2 (denoted by I_{2r}), V_{2r} , and the negative power delivered to port 2, (P_2).

$$P_2 = \frac{1}{2} \text{Re}(\mathbf{V}_2^* \mathbf{I}_2) = \frac{1}{2} V_{2r} I_{2r} \quad \text{and} \quad I_{2r} = 2P_2/V_{2r} \quad (\text{C.9})$$

The imaginary part of \mathbf{I}_2 (denoted by I_{2i}) and V_{2r} are taken as independent variables. The real part of \mathbf{I}_2 is a function of P_2 and V_{2r} given by Eq. C.9. The imaginary part of V_2 has been set to zero. The current and voltage at port 1 (\mathbf{V}_1 , \mathbf{I}_1) are functions of the port 2 variables as determined from the Y-parameter matrix (Eq. C.3). The power delivered to port 1 is given by:

$$P_1 = \frac{1}{2} \text{Re}(\mathbf{V}_1^* \mathbf{I}_1) \quad (\text{C.10})$$

where

$$\mathbf{V}_1 = \frac{\mathbf{I}_2 - \mathbf{y}_{22} \mathbf{V}_2}{\mathbf{y}_{21}} \quad \mathbf{I}_1 = \mathbf{y}_{11} \left(\frac{\mathbf{I}_2 - \mathbf{y}_{22} \mathbf{V}_2}{\mathbf{y}_{21}} \right) + \mathbf{y}_{12} \mathbf{V}_2 \quad (\text{C.11})$$

The input power can be minimized by taking the partial derivatives of P_1 in terms of V_{2r} and I_{2i} and setting them equal to zero. The corresponding values of the independent port 2 variables for maximum added power are:

$$I_{2i} = -\frac{V_2(g_{12}b_{21} + g_{21}b_{12} - 2g_{11}b_{22})}{2g_{11}}$$

$$V_{2r} = 2 \cdot \sqrt{\frac{P_2^2 g_{11}^2}{N}} \quad (\text{C.12})$$

where:

$$N = 4g_{11}g_{22}(g_{11}g_{22} + b_{12}b_{21} - g_{12}g_{21}) - (g_{12}b_{21} + g_{21}b_{12})^2$$

The port 1 variables ($\mathbf{V}_1, \mathbf{I}_1$) can be calculated from these optimum port 2 variables through the Y-parameters (Eq. C.11). The value of \mathbf{A}_{opt} is given by $\mathbf{V}_2/\mathbf{V}_1$:

$$\mathbf{A}_{opt} = \frac{-2g_{11}Y_{21}}{\sqrt{N} + 2g_{11}g_{22} + j \cdot (g_{12}b_{21} + g_{21}b_{12})} \quad (\text{C.13})$$

The embedding networks may then be synthesized as before. The ratio of the arbitrary constant $P_2 = -P_{out}$ and the minimum input power at port 1 (P_1) is equal to the maximum power gain of the active device. This optimization of \mathbf{A} is equivalent to simultaneously matching the input and output ports for maximum added power in the feedback loop.

The gain-compressed Y-parameters for maximum oscillator power described by Johnson [62] should be used in the calculation of \mathbf{A}_{opt} . Oscillator startup should be carefully checked since there may be a phase shift between the small signal Y-parameters and the large signal (gain compressed) Y-parameters. In general, the uncompressed power gain of the device will be higher at oscillator startup and the amplitude of the signal in the system will increase until the power gain compresses to the point given by the Y-parameters used in deriving the embedding network. Gain compression beyond this point will be impossible because the power feedback through the embedding network will be insufficient for operation at any lower gain value. Thus maximum oscillator power will be delivered to the load because the minimized port 1 input power (P_1) will insure operation at the gain compression value for maximum oscillator power (Eq. C.7) and any power not fed back to the input must be dissipated in the embedding network which includes the load.

Numerical examples (Table C.1) using the 20 GHz gain-compressed Y-parameters of two GaAs MESFETs (described in chapter 4) show that the values of \mathbf{A}_{opt} determined with this new optimization method are different from those determined from Eq. C.5. The differences are not extremely large which accounts for the experi-

mental success of oscillators constructed under the assumption that $|V_1|$ is constant [63, 83, 85, 62]. This new method, however, is expected to result in more accurate determination of the embedding networks for maximum output power.

At a constant DC bias point, with a given set of two port parameters, the point of maximum output power is also the point of maximum DC-RF efficiency [63]. For a given device under varying DC bias, however, the point of maximum power and maximum DC-RF efficiency are likely to be different. The magnitude of the port 2 RF voltage (V_2) and current (I_2) for the device in the optimum embedding network should be iteratively calculated to determine if voltage or current limits set by the DC bias conditions [85] will prevent the oscillator from reaching its maximum power output. If this occurs, it may be helpful to choose a different value for A or appeal to a simple load line analysis [87].

Device	G_{ME} (at max osc. power)	A_{opt} (constant $ V_1 $)	A_{opt} (max added power)
FLR016XV (Fujitsu)	5.5 dB	$2.28 + j 13.05$	$3.19 + j 10.73$
NE32100 (NEC)	6.3 dB	$-1.00 + j 1.26$	$-1.10 + j 0.478$

Table C.1: Values of A_{opt} calculated at G_{ME} (max oscillator power) for two GaAs MESFETs at 20 GHz. The FLR016XV is a medium power device. The NE32100 is designed for small signal low noise applications.

APPENDIX D

Manufacturers Data

This appendix gives some of the data for the commercial devices manufactured by NEC [88], Fujitsu [89] and Metelics [90] that were used in Chapters 4 and 6. Electrical characteristics and S parameter data are given.

D.1 NEC NE32100 Ultra Low Noise K-band Heterojunction FET

Symbols	Characteristics	Units	Min	Typ	Max
I_{GSO}	Gate to Source Leak Current, $V_{GS} = -3V$	μA		1	10
I_{DSS}	Saturated Drain Current, $V_{DS} = 2V, V_{GS} = 0$	mA	12	30	60
$V_{GS(off)}$	Gate to Source Cutoff Voltage $V_{DS} = 2V, I_D = 100\mu A$	V	-2.0	-1.0	-0.2
g_m	Transconductance, $V_{DS} = 2V, I_D = 10mA$	mS	30	40	
NF_{opt}	Optimum Noise Figure, $f=12$ GHz $V_{DS} = 2V, I_{DS} = 10mA$	dB		1.0	1.2
G_A	Associated Gain, $f=12$ GHz, $V_{DS} = 2V, I_{DS} = 10mA$	dB	9.5	10.5	
P_{1dB}	Output Power at 1dB Gain Compression $V_{DS} = 2.0V, I_{DS} = 10mA, f = 12GHz$ $V_{DS} = 2.0V, I_{DS} = 20mA, f = 12GHz$	dBm dBm		9.0 10.5	
R_{th}	Thermal Resistance (Channel to Ambient)	$^{\circ}C/W$			380
P_t	Total Power Dissipation	mW			200

```

! NE32100 S-parameters for Vds=2V Ids=20mA
! S-Parameters include bond wires:
! Gate: Total 2 wires 0.0126in. (321 micron) long each wire.
! Drain: Total 2 wires 0.0115in. (292 micron) long each wire.
! Source: Total 4 wires 0.0076in. (194 micron) long each wire.
! Wire: 0.0007in. (17.8 micron) dia. gold.
! f      S11      S21      S12      S22
0.1  0.999  -1.0  4.24  178  0.002  88  0.57  -1
0.2  0.999  -2.0  4.24  178  0.004  87  0.57  -2
0.5  0.999  -6.0  4.23  175  0.007  84  0.57  -4
1.0  0.996  -12.0  4.20  170  0.015  81  0.57  -9
2.0  0.984  -23.0  4.07  160  0.029  75  0.57  -15
3.0  0.971  -33.0  3.94  152  0.042  70  0.56  -21
4.0  0.948  -42.0  3.78  144  0.054  64  0.55  -27
5.0  0.931  -51.0  3.64  136  0.064  60  0.55  -31
6.0  0.914  -59.0  3.52  130  0.074  54  0.54  -36
7.0  0.897  -67.0  3.46  123  0.083  50  0.54  -42
8.0  0.886  -75.0  3.42  116  0.092  47  0.53  -47
9.0  0.861  -85.0  3.35  108  0.102  42  0.52  -53
10.0 0.835  -94.0  3.24  101  0.111  37  0.50  -60
11.0 0.813 -103.0  3.13  94  0.116  32  0.48  -66
12.0 0.795 -112.0  2.99  87  0.123  27  0.46  -72
13.0 0.779 -119.0  2.84  81  0.128  22  0.45  -78
14.0 0.767 -125.0  2.73  76  0.128  18  0.44  -82
15.0 0.759 -129.0  2.59  70  0.130  15  0.43  -86
16.0 0.752 -134.0  2.52  65  0.130  12  0.43  -89
17.0 0.737 -138.0  2.41  61  0.132  10  0.42  -91
18.0 0.725 -143.0  2.35  56  0.129  7  0.42  -91
19.0 0.703 -148.0  2.29  51  0.127  7  0.42  -91
20.0 0.679 -153.0  2.26  47  0.130  9  0.43  -91
21.0 0.673 -158.0  2.20  41  0.141  9  0.43  -94
22.0 0.670 -165.0  2.18  37  0.144  9  0.45  -99
23.0 0.662 -173.0  2.15  30  0.156  5  0.44  -106
24.0 0.647 179.0  2.04  26  0.155  0  0.41  -113
25.0 0.638 174.0  1.94  23  0.154 -1  0.39  -116
26.0 0.655 171.0  2.01  18  0.162 -1  0.39  -121

```

```

! Noise parameters (Vds=2.0V Ids=10mA)
! f      Fmin (dB)      Gamma opt.      rn (normalized)
1        0.35          0.83  10          0.75
2        0.37          0.82  23          0.65
4        0.40          0.80  40          0.57
6        0.50          0.77  53          0.50
8        0.65          0.73  68          0.45
10       0.82          0.67  84          0.42
12       1.00          0.60  103         0.38
14       1.20          0.55  116         0.32
16       1.35          0.52  126         0.25
18       1.55          0.49  137         0.20
20       1.75          0.47  146         0.16
22       1.90          0.45  158         0.12
24       2.10          0.44  170         0.10
26       2.35          0.43 -176         0.09
28       2.60          0.44 -164         0.08
30       2.82          0.45 -153         0.08

```

D.2 Fujitsu FLR016XV K-band Power GaAs FET Chip

Symbols	Characteristics	Units	Min	Typ	Max
I_{DSS}	Drain Current, $V_{DS} = 5V$, $V_{GS} = 0$	mA		70	
V_p	Gate to Source Pinch-off Voltage $V_{DS} = 5V$, $I_{DS} = 3mA$	V	-1.0	-2.0	-3.5
g_m	Transconductance, $V_{DS} = 5V$, $I_{DS} = 40mA$	mS		30	
V_{GSO}	Gate-Source Breakdown Voltage $I_{GS} = 3\mu A$	V	-3		
P_{1dB}	Output Power at 1dB Gain Compression	dBm	19	20	
G_{1dB}	Power Gain at 1dB Gain Compression	dB	8.0	9.0	
N_{add}	$V_{DS} = 2.0V$, $I_{DS} = 20mA$, $f = 12GHz$ ($V_{DS} = 8V$, $I_{DS} = 0.6I_{DSS}(Typ)$, $f = 18GHz$)	%		26	
R_{th}	Thermal Resistance (Channel to Ambient)	$^{\circ}C/W$			130

```

! FLR016XV.S2P 5/92
! FLR016XV
! @8V-42mA
! .5GHZ 26.5GHZ 53
! S-parameters include bonding wires:
! gate : total 1 wire, 1 per bond pad, 0.2mm long each wire
! drain : total 1 wire, 1 per bond pad, 0.2mm long each wire
! source: no bond wire, gold plated via hole to backside of chip
! wire : 25 micron diameter, gold
# GHZ S MA R 50
0.50000 1.000 -5.950 2.168 174.000 0.008 84.060 0.836 -1.520
1.00000 0.986 -10.560 2.170 169.610 0.009 81.000 0.842 -4.390
1.50000 0.990 -16.130 2.145 164.730 0.015 79.770 0.838 -5.990
2.00000 0.980 -21.390 2.140 160.000 0.016 87.320 0.846 -8.330
2.50000 0.956 -27.660 2.135 155.270 0.017 70.980 0.860 -9.150
3.00000 0.972 -34.770 2.246 148.910 0.021 68.900 0.815 -13.020
3.50000 0.975 -39.180 2.188 144.630 0.027 70.040 0.809 -15.480
4.00000 0.953 -45.190 2.143 139.530 0.029 64.510 0.817 -16.770
4.50000 0.936 -49.690 2.114 135.030 0.029 61.090 0.816 -19.630
5.00000 0.937 -53.930 2.077 130.700 0.033 59.160 0.813 -22.870
5.50000 0.930 -59.050 2.044 126.670 0.037 56.610 0.805 -24.330
6.00000 0.919 -63.970 2.010 122.340 0.038 61.030 0.814 -26.660
6.50000 0.913 -67.800 1.955 118.130 0.034 52.300 0.810 -28.980
7.00000 0.905 -71.990 1.915 113.860 0.038 49.400 0.807 -31.370
7.50000 0.900 -75.920 1.879 110.670 0.038 48.600 0.808 -33.210
8.00000 0.887 -79.950 1.839 106.370 0.037 49.480 0.803 -35.290
8.50000 0.877 -84.430 1.799 102.190 0.038 47.900 0.808 -37.110
9.00000 0.869 -87.990 1.754 98.400 0.039 50.450 0.802 -39.150
9.50000 0.864 -92.480 1.735 94.270 0.040 44.040 0.814 -41.620
10.00000 0.856 -96.460 1.697 90.680 0.040 44.150 0.818 -43.460
10.50000 0.855 -100.300 1.659 87.250 0.039 40.940 0.810 -45.150
11.00000 0.844 -104.600 1.620 83.370 0.041 40.410 0.807 -47.060
11.50000 0.841 -108.400 1.599 79.770 0.040 37.770 0.815 -48.850
12.00000 0.834 -112.400 1.574 75.940 0.038 39.360 0.815 -50.800
12.50000 0.828 -116.400 1.549 72.410 0.042 39.840 0.813 -52.840
13.00000 0.822 -120.000 1.513 68.640 0.038 37.740 0.817 -55.120
13.50000 0.817 -123.600 1.487 65.040 0.039 38.880 0.819 -57.030
14.00000 0.817 -127.400 1.459 61.570 0.041 35.430 0.819 -59.460
14.50000 0.814 -131.200 1.434 58.010 0.039 38.090 0.815 -61.770
15.00000 0.808 -135.000 1.415 53.990 0.044 31.350 0.817 -64.000
15.50000 0.812 -138.500 1.385 50.690 0.046 32.620 0.822 -66.590
16.00000 0.803 -142.200 1.355 46.910 0.043 28.170 0.818 -68.990
16.50000 0.800 -144.900 1.335 42.730 0.043 29.660 0.822 -71.480
17.00000 0.801 -149.500 1.304 39.550 0.046 27.020 0.823 -73.440
17.50000 0.799 -152.800 1.286 36.250 0.044 18.830 0.819 -75.230
18.00000 0.794 -156.400 1.257 32.350 0.046 20.100 0.823 -78.270

```

18.5000	0.792	-159.300	1.232	28.930	0.047	21.210	0.824	-80.860
19.0000	0.792	-163.400	1.211	25.410	0.046	17.060	0.824	-82.820
19.5000	0.780	-166.800	1.196	22.130	0.049	15.740	0.834	-84.720
20.0000	0.790	-170.700	1.169	18.620	0.054	14.320	0.827	-86.200
20.5000	0.781	-174.400	1.136	15.200	0.056	11.290	0.827	-87.610
21.0000	0.785	-178.000	1.129	11.040	0.060	12.360	0.823	-90.020
21.5000	0.789	179.010	1.101	7.860	0.062	3.840	0.825	-91.530
22.0000	0.790	175.130	1.082	4.130	0.058	4.300	0.830	-93.960
22.5000	0.788	171.860	1.075	0.170	0.069	0.480	0.843	-97.920
23.0000	0.788	168.410	1.018	-2.280	0.067	-1.940	0.816	-99.710
23.5000	0.784	166.540	1.014	-6.030	0.066	-4.950	0.834	-101.500
24.0000	0.786	163.800	0.992	-9.770	0.072	-5.680	0.848	-103.800
24.5000	0.780	160.540	0.958	-13.130	0.062	-3.700	0.849	-107.500
25.0000	0.791	159.230	0.941	-15.540	0.068	-6.810	0.841	-109.000
25.5000	0.789	157.090	0.900	-19.700	0.069	-8.580	0.839	-113.000
26.0000	0.788	155.650	0.865	-22.590	0.067	-8.850	0.856	-115.500
26.5000	0.782	152.360	0.849	-23.770	0.061	-11.210	0.848	-116.500

D.3 NEC NE72084 General Purpose GaAs MESFET

Symbols	Characteristics	Units	Min	Typ	Max
I_{GSO}	Gate to Source Leak Current, $V_{GS} = -5V$	μA		1	10
I_{DSS}	Saturated Drain Current, $V_{DS} = 3V, V_{GS} = 0$	mA	30	60	150
V_P	Pinch-off Voltage, $V_{DS} = 3V, I_D = 100\mu A$	V	-0.8	-2.0	-4.0
g_m	Transconductance, $V_{DS} = 3V, I_D = 10mA$	mS	20	40	60
f_{MAX}	Maximum Frequency of Oscillation ($V_{DS} = 3V, I_D = 30mA$)	GHz		60	
MAG	Maximum Available Gain at $V_{DS} = 3V, I_D = 30mA$ f = 2 GHz f = 4 GHz f = 8 GHz f = 12 GHz	dB dB dB dB		17.5 15.0 12.0 8.0	
NF_{opt}	Optimum Noise Figure, $V_{DS} = 3V, I_{DS} = 10mA$ f = 2 GHz f = 4 GHz f = 8 GHz	dB dB dB		0.6 0.8 2.0	1.4
G_A	Associated Gain at NF, $V_{DS} = 3V, I_{DS} = 10mA$ f = 2 GHz f = 4 GHz f = 8 GHz	dB dB dB		15.0 12.0 8.5	
P_{1dB}	Output Power at 1dB Gain Compression $V_{DS} = 4.0V, I_{DS} = 30mA, f = 4GHz$	dBm		15	
R_{th}	Thermal Resistance (Channel to Ambient)	$^{\circ}C/W$			400
P_t	Total Power Dissipation	mW			300

! NE72084 S-parameters for Vds=3V Ids=30mA

```
! f      S11      S21      S12      S22
0.13 0.987 -2.1 3.40 179.7 0.0028 178.3 0.664 0.3
0.2 0.985 -3.3 3.51 -179.6 0.01 44.6 0.658 -0.4
0.3 0.999 -6.7 3.58 178.1 0.0046 125.0 0.655 -2.8
0.4 0.982 -9.0 3.56 178.2 0.0235 95.4 0.644 -4.5
0.5 0.972 -12.1 3.56 176.4 0.0206 97.6 0.637 -6.8
0.6 0.955 -15.6 3.52 175.3 0.0269 88.6 0.630 -8.2
0.7 0.935 -19.1 3.53 174.0 0.0280 95.4 0.620 -10.7
0.8 0.906 -21.7 3.44 173.6 0.0328 98.9 0.602 -12.6
0.9 0.881 -24.4 3.35 172.8 0.0345 98.1 0.587 -14.7
1 0.868 -26.7 3.26 173.1 0.0400 100.3 0.586 -16.8
1.5 0.859 -36.5 3.24 172.5 0.0515 107.4 0.565 -23.9
2 0.91 -59 3.53 127 0.07 54 0.60 -37
4 0.76 -110 2.87 83 0.10 26 0.52 -69
6 0.65 -151 2.45 46 0.12 8 0.46 -97
8 0.52 171 2.02 14 0.13 -4 0.42 -122
10 0.49 124 1.82 -18 0.15 -16 0.38 -155
12 0.52 79 1.55 -50 0.17 -31 0.41 166
14 0.57 41 1.30 -82 0.19 -51 0.46 132
16 0.65 9 1.08 -114 0.20 -74 0.56 98
18 0.70 -10 0.86 -136 0.20 -91 0.62 77
```

! Noise parameters for Vds=3V Ids=10mA

```
! f      Fmin (dB)      Gamma opt.      rn (normalized)
2      0.6      0.81 38      0.49
4      1.0      0.74 59      0.39
6      1.3      0.66 102      0.30
8      1.7      0.49 130      0.24
```

D.4 Metelics MSV-34-060-E28 Silicon Varactor Diode

Symbols	Characteristics	Units	
V_{BR}	Reverse Breakdown voltage, $10\mu\text{A}$	V	30
C_J	Junction Capacitance $\pm 10\%$, -4V	pF	0.4
C_{J0}/C_{J30}	Junction Capacitance Ratio		3.4
Q_{-4}	Quality Factor, -4V , ($f = 50\text{MHz}$)		6300
R_s	Series Resistance ($f = 1\text{GHz}$)	Ω	1.3
F_{C4}	Cut-off Frequency $F_{C4} = 1/(2\pi R_s C_{J-4})$	GHz	315
C_p	Parasitic Capacitance (E28 package)	pF	0.1
L_p	Parasitic Inductance (E28 package)	nH	0.5

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