A Fully Integrated CMOS Receiver

by

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to my mom, dad, my sister and my wife…

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ABSTRACT

The rapidly growing wireless communication market is creating an increasing demand for low-cost highly-integrated radio frequency (RF) communication systems. This dissertation focuses on techniques to enable fully-integrated, wireless receivers incorporating all passive components, including the antenna, and also incorporating baseband synchronization on-chip. Not only is the receiver small in size and requires very low power, but it also delivers synchronized demodulated data. This research targets applications such as implantable neuroprosthetic devices and environmental wireless sensors, which need short range, low data-rate wireless communications but a long lifetime. To achieve these goals, the super-regenerative architecture is used, since power consumption with this architecture is low due to the simplified receiver architecture.

This dissertation presents a 5GHz single chip receiver incorporating a compact on-chip 5 GHz slot antenna (50 times smaller than traditional dipole antennas) and a digital received data synchronization. A compact capacitively-loaded 5 GHz standing-wave resonator is used to improve the energy efficiency. An all-digital PLL timing scheme synchronizes the received data clock. A new type of low-power envelope detector is incorporated to increase the data rate and efficiency. The receiver achieves a data rate up to 1.2 Mb/s, dissipates 6.6 mW from a 1.5 V supply.

The novel on-chip capacitively-loaded, transmission-line-standing-wave resonator is employed instead of a conventional low-Q on-chip inductor. The simulated quality

factor of the resonator is very high (35), and is verified by phase-noise measurements of a prototype 5GHz Voltage Control Oscillator (VCO) incorporating this resonator. The prototype VCO, implemented in 0.13 μm CMOS, dissipates 3 mW from a 1.2 V supply, and achieves a measured phase noise of -117 dBc/Hz at a 1 MHz offset.

In the on-chip antenna an efficient shielding technique is used to shield the antenna from the low-resistivity substrate underneath. Two standalone on-chip slot antenna prototypes were designed and fabricated in 0.13 μm CMOS. The 9 GHz prototype occupies a die area of only 0.3 mm^2, has an active gain of -4.4 dBi and an efficiency of 9%. The second prototype occupies a die area of 0.47 mm^2, and achieves a passive gain of approximately -17.0 dBi at 5 GHz.

Two fully integrated 5 GHz receiver prototypes have been designed using super-regenerative architecture in the IBM 0.13 μm CMOS process. The first prototype was fabricated and demonstrated. This receiver draws 6.6 mW, which corresponds to 5.5 nJ per bit at the date rate of 1.2 Mb/s, and occupies a die area of 2.4 mm^2. The second prototype utilizes an inductorless LNA replacing the inductor-based LNA. This inductorless LNA eliminates the problem of electromagnetic signal interference by on-chip inductors in the inductor-based LNA, and greatly shrinks the system die area. The total die area is only 1.4 mm^2. In simulations, same performance is achieved with similar power consumption as that of the first prototype.

CHAPTER I

INTRODUCTION

The rapidly growing wireless communication market is creating an ever-increasing demand for radio frequency (RF) receivers. These include devices used in mobile wireless communication, broadcast television, aircraft radar, hand-held GPS, RFID and wireless sensors in various scientific and industrial fields. To satisfy the ever increasing capacity requirement for more users and higher data rate, radio access has been migrating to higher frequencies and wider channel bandwidths. On the other hand, to minimize the system physical size and cost, more and more RF bands and standards, or even entire RF receivers, are integrated into one chip. This low-cost and higher-level integration becomes possible with advancements in modern CMOS technology, which allows the implementation of RF or microwave components, analog circuits and complex digital schemes all in one single-chip design. This research focuses on developing a wireless solution which is highly integrated, small and requires very low power. This chapter first outlines the motivation of this work and discusses the target applications. Then, different kinds of receiver architectures are compared. Next, the mechanism and development of super-regenerative technology are presented. Then, several state of the art receivers/transceivers are presented and compared. Finally this chapter outlines the organization of the thesis.

1.1 Motivation

Successful wireless products demand low cost, low-power and high-volume techniques. In the baseband section of wireless systems, the silicon real estate required for processors, memories and interfaces has shrunk due to the development of CMOS technology. In contrast to this situation, improvement in passive components, in particular on-chip inductors, has been much less dramatic. To achieve optimum performance of RF transceivers, current commercial approaches usually utilize multiple technologies and high quality discrete components. The use of discrete components (e.g. Surface Acoustic Wave (SAW) filters, resonators based on Micro-Electro-Mechanical Systems (MEMS) technology) enables very good performance, but they are generally very expensive, and not easy to integrate with CMOS. It is estimated that 90 percent of components in a single-mode telephone are passive components [1]. Each discrete component can cost from $0.05 to $5. The high count of components takes up significant board area, complicates the assembly process and increases the cost of the entire wireless system. This is especially true for multi-band receivers where multiple signal paths significantly add to the cost. Since the external component count depends on the receiver architecture, there is a strong drive to adopt highly-integrated architectures that rely less on the external components. Another direct approach to reduce the passive component content is to integrate the passive components directly onto the silicon substrate. The ultimate goal is a single-chip system, where the resonating tank of the VCO, the band select filter, and even the antenna are integrated on chip. Power consumption is another major engineering concern in the design of wireless devices. There is a trade-off between power consumption and system performance. To achieve good performance (such as high data rate and wide coverage area) in general, more power is consumed in many wireless

communication standards such as IEEE 802.11 a/b/g, etc. However, there are many applications which need short range and low data rate, but long battery lifetime. These include wireless systems in implantable neuroprosthetic devices, environmental wireless sensors, RFID, etc. Systems involving wireless sensors are increasingly used in various applications. The goal of this thesis is to develop a highly integrated system with sufficient data rate but low power consumption, low cost and small physical size.

1.2 Receiver Architectures

Wireless communications have been developed for more than a century; it has evolved from all discrete-component implementation to highly integrated system. There are several classical receiver architectures such as super-heterodyne, direct-conversion and super-regeneration. Usually different receiver architectures match different applications depending on the system complexity, power consumption, external component count and system cost.

The super-heterodyne architecture is one of the most popular architecture in modern radio products. It was first proposed by Armstrong in early 1918 [2]. A super-heterodyne receiver downconverts the received RF signal to an intermediate frequency (IF) in two or more steps (as shown in Figure 1.1). Therefore good frequency isolation between RF signal and local oscillator (LO) is achieved, and the radiation from the local oscillator is minimized. Furthermore, amplification is distributed across several frequency stages which relaxes the gain and stability requirement in each stage and increases the total possible gain. Also different RF channels are selected by tuning the local oscillator frequency. Filters in different frequency stages ensure good channel selection and lower interference from neighboring channels and blockers. Generally a

super-heterodyne receiver provides good frequency selectivity and high sensitivity. But it has several drawbacks. In this architecture several filters are required for band selection, image rejection and channel selection. And the filters are usually bulky, expensive SAW filters, which can not be integrated on chip, and greatly increase the physical size and cost of the system. Secondly, impedance matching with the external components (usually with impedance of 50 Ω), increases the complexity and power dissipation of the system. These problems get even worse for multi-band applications.

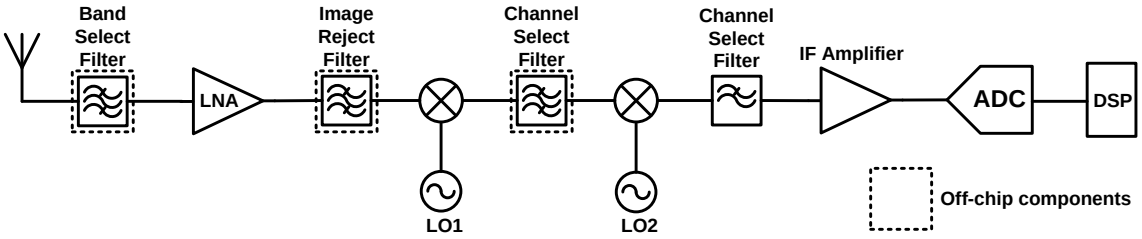


Figure 1.1: Block diagram of a two-stage super-heterodyne receiver.

The direct-conversion architecture is another popular architecture in modern wireless receivers. Due to its high level of integration, this architecture has been found in more applications recently, especially in multi-standards wireless communications. In a direct-conversion receiver, the received RF signal is downconverted to DC or low IF (as shown in Figure 1.2). The image signal is at the desired signal frequency, so no image-rejection filters are required. Usually only a band-select filter is used at the front of the LNA. Thus direct-conversion receiver is suited to on-chip integration. But there are several drawbacks, which make it inferior to super-heterodyne receivers in the past. DC offset is probably the most serious problem. Since in a direct-conversion architecture the downconverted band extends to zero frequency, DC offset voltages can corrupt the signal

and saturate the following stages. The DC offset is caused by LO leakage and interferer induced self-mixing. On the other hand, the flicker noise of CMOS devices also substantially corrupts the downconverted zero frequency signal. There are other disadvantages such as I/Q mismatch in quadrature mixing and even order distortion [3]. To overcome these problems, periodic calibration and offset cancellation techniques are used [4, 5]. But these increase circuit complexity and system power dissipation.

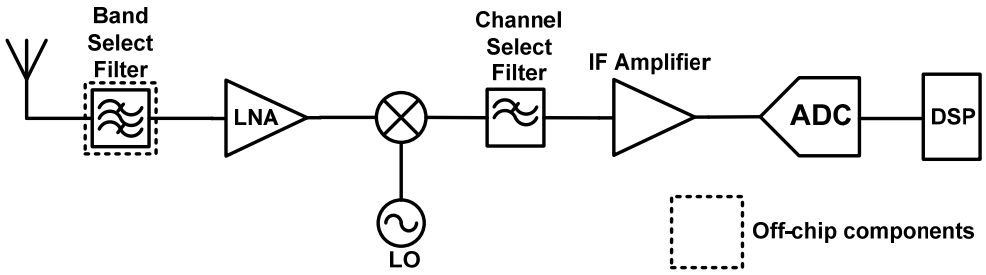


Figure 1.2: Block diagram of a direct-conversion receiver.

The super-regenerative architecture is based on the super-regeneration principle invented by Armstrong in 1922 [6]. This technology was usually used in vacuum tube circuits, but recently there has been a renewal of interest in this architecture. The principle of super-regeneration is based on the variation of the start-up time of the oscillator. Normally oscillation starts from thermal noise in the circuit, which is a relatively slow process. When there is an injected external RF signal, such as a carrier at the resonance frequency, the startup becomes much faster. A basic block diagram of the super-regenerative receiver is presented in Figure 1.3. The oscillator is enabled by a quench signal, so it is periodically driven into the critical oscillating condition, or oscillation start-up state. OOK (On/Off Keying) modulation, or 100% amplitude modulation, is easily detected with this architecture.

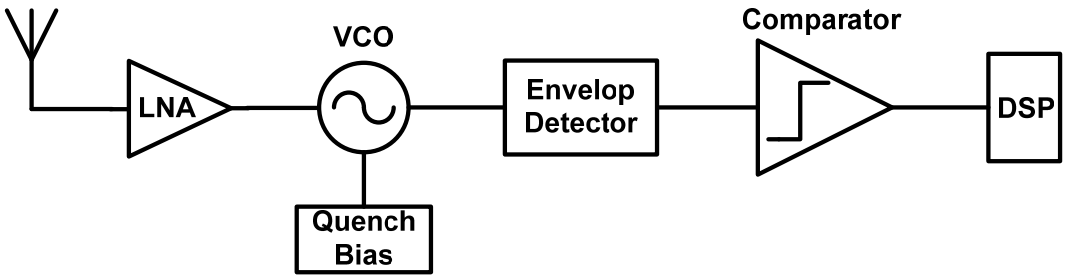


Figure 1.3: Block diagram of a super-regenerative receiver.

Figure 1.4 represents the main signals. The OOK RF signal is coupled to the input of the receiver. When no input signal is applied, the build-up of oscillation is slower than when the RF signal is present. In other words, the oscillation envelop changes with the input RF signal level. Compared with the other two architectures, a super-regenerative receiver has simplified receiver architecture and relaxed design constraints and therefore it is easy in principle to integrate into one chip. However poor sensitivity and selectivity are the major disadvantages of this architecture. On the other hand, component variation due to changes in environment and process makes the receiver performance unstable.

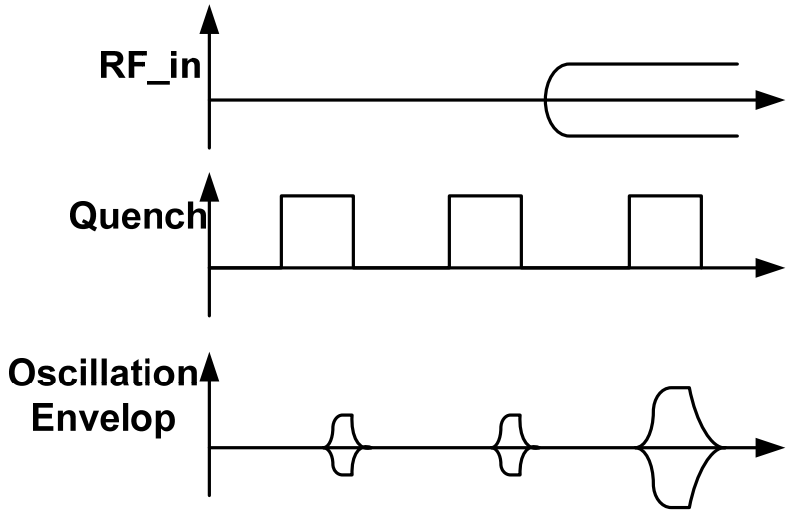


Figure 1.4: Main signals in the super-regenerative receiver.

Each architecture has its merits and drawbacks. Table 1.1 summarizes the pros, cons and applications for each architecture. Both super-heterodyne and direct-conversion offer good frequency selectivity, and high sensitivity, and they can be used to demodulate different types of modulations. These architectures are selected for applications such as cellular wireless communications, wireless LAN applications, etc., where the selectivity and sensitivity are critical. But there are many short-range and low-data-rate applications where low power consumption is more important. The super-regenerative receiver provides large signal gain using only an oscillator as an amplifier with positive feedback, and no separate VCO is needed, which leads to lower power consumption. For this reason super-regenerative architecture is chosen in our design.

Table 1.1: Comparison of different receiver architectures.

Architecture	Pros	Cons	Applications
Super-heterodyne	High performance Reliable	Low level of integration Large physical size High power High cost	Cellular communication, radar, GPS, WLAN
Direct-conversion	High level of integration than super-heterodyne Low power Low cost	DC offset Flick noise Even order distortion I/Q mismatch	Multi-band cellular communication, radar, GPS, WLAN
Super-regenerative	Simple Small physical size Low power High level of integration	Poor selectivity and sensitivity	Short-range, low data rate

1.3 Super-regenerative Receiver Architecture

The super-regenerative technique was widely used in vacuum-tube circuits [7]. In the 1930s, radio amateurs first used super-regenerative circuits in ultra-short-wave communication receivers due to the economy associated with the architecture. During World War II, the super-regenerative circuit came into widespread use by the U.S. army. Walkie-talkie communication receivers and radar pulse responders using this architecture were mass produced in the U.S.A. Then, this technique was progressively replaced by super-heterodyne receiver, due to the better selectivity of the super-heterodyne approach.

Nowadays super-regenerative receivers are still used in many low cost applications like toys.

The advance of modern CMOS/BiCMOS techniques makes it possible to improve the limits of super-regenerative receivers. In the late 1990s, the first integrated CMOS super-regenerative receiver was reported [8][1]. After that several CMOS super-regenerative receivers were developed [9-11]. To achieve higher data rates and broaden the application field, research on super-regeneration has been pushing the operating frequency to higher bands, such as the 2.4 GHz industrial scientific medical (ISM) bands [12-14], or even millimeter wave frequency (e.g. a 7.5 GHz super-regenerative detector reported by Buchanan et al.[15]). In general, a super-regenerative receiver is suitable for OOK modulation detection, since super-regenerative oscillator (SRO) start up depends on the injected RF signal. Recently direct-sequence-spread-spectrum (DSSS) signal detection using a super-regenerative receiver was demonstrated [16], which shows low power spectral density signal transmission and good resistance to interference. Ayers et al. [17] presented the demodulation of Binary Frequency Shift Keying (BFSK) in a super-regenerative transceiver. Poor frequency selectivity is another problem that needs to be overcome for super-regenerative receivers. A super-regenerative receiver was reported recently [18], where Bulk Acoustic Wave (BAW) devices are used as high-Q frequency reference to increase the selectivity. On the other hand Q-enhancement techniques [12, 19] can also be applied to improve the frequency performance.

[1] In this receiver an off-chip resonator is used in the oscillator.

This dissertation presents a 5GHz single chip receiver incorporating a compact on-chip 5 GHz slot antenna and a capacitively-loaded 5 GHz standing-wave resonator. The key contributions of this work are:

- We demonstrated a prototype single chip receiver, incorporating antenna and baseband processing, with a power dissipation of 6.6mW and a die area of 2.4mm^2.
- A novel 5GHz on-chip resonator with a Q of 35 is utilized replacing on-chip inductors improving the receiver efficiency.
- The smallest on-chip slot antenna is integrated into the receiver greatly reducing the system volume.
- Unlike other reported super-regenerative receivers this receiver includes a receive symbol synchronization.
- A new type of envelope detector is employed in this receiver.
- The receiver works at 5GHz with 8 tunable channels a frequency range higher than of the previous design by Jia-Yi Chen [14].

1.4 State of the Art Receiver/Transceivers

The architectures discussed in the last two sections are used in numerous receivers/transceivers. In this section we discuss some state of the art receiver or transceiver designs.

Receiver chip MAX1473 from Maxim [20] is a low-power CMOS super-heterodyne receiver. It is ideal for receiving amplitude-shift-keyed (ASK) data in the 315 MHz or 433 MHz ISM band, with a highest data rate of 100 kps. It achieves a low supply current of 5.2 mA at 3.3 V. This receiver includes a build-in RF image rejection filter,

and is fully integrated. It can be used in system with few external components, and is ideal for cost- and power-sensitive applications.

Broadcom recently released a fully integrated multiple-input and multiple-output (MIMO) multiband direct-conversion CMOS transceiver for WLAN applications (802.11n) [5]. The transceiver provides communication data up to 270 Mbps in 2.4 GHz and 5 GHz ISM and UNII bands. Self-contained and/or DSP-assisted auto-calibration circuitry is extensively utilized to alleviate the DC offset and other problems in direct-conversion architecture discussed in section 1.2. This circuitry adds a lot of overhead to the system in terms of power and physical size. In receiving mode, the total power consumption is 485 mW. But because of its very high data rate, the corresponding energy per bit is very low, which is only 1.8 nJ/bit.

There is still no integrated commercial super-regenerative receiver/transceiver available. Three super-regenerative receivers reported in the literature are presented here. The first system is a low-power and low-voltage super-regenerative receiver operating at 1 GHz and implemented in a 0.35 μm CMOS process [11]. The receiver can demodulate OOK signals with a data rate up to 100 kps. The power consumption is less than 1.2 mW with a 1.5 V power supply, the corresponding energy per bit is 12 nJ/bit. The receiver has a low lever of integration, since an off-chip inductor is used in the VCO resonate tank. The second system is a 1.9 GHz super-regenerative transceiver with a BAW resonator [18]. The BAW device is used to reduce the power consumption and increase the selectivity. But this device is not compatible with CMOS processes, and is expensive to integrate with CMOS. In this receiver, the receiving path only includes an isolation amplifier, a super-regenerative oscillator, a non-linear filter, and an OOK detector. This

simplified topology leads to lower power consumption with a value of 400 μW. The highest data rate is 5kps with energy per bit of 80nJ/bit. The last is a receiver designed by Jia-Yi Chen [12] in our group. This is a fully integrated receive in a 0.13 μm CMOS process. The receiver operates in the 2.4 GHz ISM band, with data rate up to 1Mbps. It achieves a power consumption less than 3mW. Digital calibration and a Q-enhanced filtering are employed to improve the selectivity and sensitivity of the super-regeneration. The prototype has energy per bit of 5.6 nJ/bit, the lowest of these three super-regenerative receivers. Several design methodologies developed for this receiver are adopted in this research.

Another system we select is a 1 Mbps 916.5 MHz OOK transceiver for short-range wireless sensor applications [21]. The receiver uses envelope detection based architecture with a simplified and scalable RF front-end. This receiver only incorporates a SAW filter, an RF gain stage, an envelope detector, and the base band circuitry. It achieves the lowest power consumption (0.5 mW) and lowest energy per bit (0.5 nJ/bit) among the six receivers/transceivers discussed here. But because of the use of SAW filter, it is not easy to integrate into CMOS processes.

Table 1.2 summarizes the performance of the receivers/transceivers. We focus the comparison on the properties such as energy per bit, physical size, and integration level. Both super-heterodyne and direct-conversion architectures can be fully integrated. But they generally have highest power consumption and physical area. On the other hand, super-regenerative receivers provide lower data rate, but consume much lower power and occupy less die area. The super-regenerative receiver can also be fully integrated onto the chip.

Table 1.2: Comparison of different receiver/transceivers.

Receiver Architecture	**Super-Regenerative**			**Envelope Detection Based**	**Direct-Conversion**	**Super-heterodyne**
Reference	Vouilloz [11]	Otis [18]	Chen [12]	Daly [21]	Behzad [5]	Maxim MAX1473 [20]
Operating Frequency	1 GHz	1.9 GHz	2.4 GHz	916.5 MHz	2.4 GHz/5 GHz	315 MHz/433 MHz
Data rate	100 kbps	5 kbps	500 kps	1 Mbps	270 Mbps	100 kps
Power Consumption	1.2 mW	400 µW	2.8 mW	0.5 mW	495 mW	17.2 mW
Energy per bit	12 nJ/bit	80 nJ/bit	5.6 nJ/bit	0.5 nJ/bit	1.8 nJ/bit	172 nJ/bit
Die Area	0.25 mm^2	1.9 mm^2	1 mm^2	1.82 mm^2	18 mm^2	-
Integration Level	Low, Uses Discrete inductor	Low, Use BAW resonator	Fully Integrated	Low, Use SAW Filter	High, Fully Integrated	High, Fully Integrated
Technology	0.35 µm CMOS	CMOS	0.13 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	CMOS

1.5 Dissertation Overview

This research focuses on the design of a single chip super-regenerative receiver. This receiver incorporates an on-chip slot antenna and digital received data synchronization. A capacitively-loaded 5 GHz standing-wave resonator is used in the oscillator to improve energy efficiency. Chapter 2 is an overview of the fully integrated CMOS super-regenerative receiver. In chapter 3, the technical details of key circuit blocks (VCO, LNA, PLL, etc.) are introduced. Two super-regenerative prototypes are designed, based on the circuit blocks, and these are described in chapter 4. Both prototypes are fabricated in the IBM 0.13 μm CMOS RF/mixed-signal process. The test setup and measurement results of some circuit blocks and the prototype receiver are discussed in chapter 5. Lastly we summarize the contributions of this thesis and suggest some future research in chapter 6.

CHAPTER II

SYSTEM ARCHITECTURE

Successful receiver design begins with good choice of system architecture. In Chapter 1 we compared several receiver architectures, and discussed the merits and drawbacks of each architecture. In this chapter, we turn our attention to the super-regenerative architecture which will permit the maximum level of integration, minimize power dissipation, and reduce cost and physical size. We begin with an overview of the system architecture and modes of operation. Then some design concerns and system specifications are presented.

2.1 Overview

A super-regenerative receiver prototype was designed and demonstrated by Jia-Yi Chen [14] in our group. The receiver achieves a 500 kbps-1Mbps data rate at 2.4-2.483 GHz, a sensitivity of -90 dBm, with <3 mW power consumption. Based on this design, we implement a fully integrated 5 GHz super-regenerative receiver with enhanced performance. In this receiver, we integrate a VCO RF resonator and an antenna onto the chip, instead of using high-quality off-chip components or low-quality on-chip LC tanks as in many super-regenerative receivers reported [8, 14, 18]. The physical size of on-chip components is inversely proportional to the working frequency. At a higher frequency, on-chip components are miniaturized, and less lossy. This also enhances the possible detectable RF signal data rate. But a super-regenerative receiver has better performance at lower frequency. As a compromise between these, the receiver is designed in the 5

GHz frequency band. Unlike other work, this receiver also includes an all-digital PLL synchronizer scheme, which synchronizes the received data clock with the transmitter

Figure 2.1 shows the system block diagram of this receiver. The complete RF/analog signal path incorporates an on-chip antenna, a LNA, a VCO, a DAC current source which provides the quench bias current of the VCO, an envelope detector, an offset-cancelled amplifier, and a comparator. In the baseband, a data synchronizer is implemented to control the received data sampling position, and a digital controller is added to control the timing of the whole system. Additionally the VCO is also implemented as part of an on-chip PLL. This PLL comprises the VCO, a phase detector, a charge pump, a loop filter, and a programmable divider. Some circuit blocks in the 2.4 GHz receiver [14] are reused in this design. These include the DAC current source, the offset-cancelled amplifier, the comparator, and the digital controller. The design methodologies of the other circuit blocks are discussed in the next chapter.

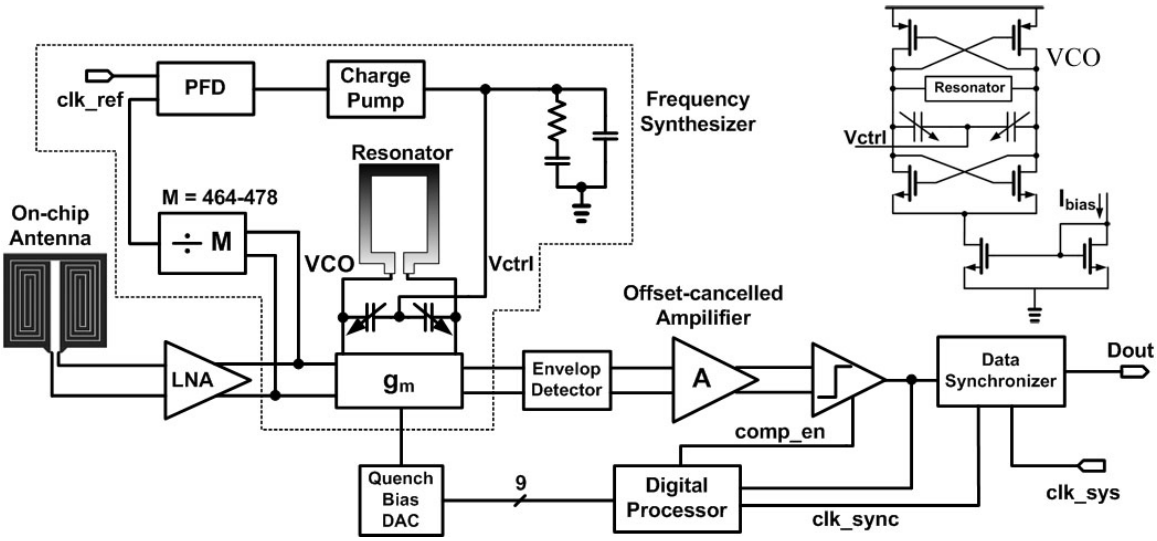


Figure 2.1: Block diagram of the receiver.

In this receiver the incoming RF signal is received by the on-chip slot antenna, amplified by a differential LNA and injected onto the oscillatory nodes of the VCO. The

output of the antenna and input of the LNA are 50 Ω impedance matched at 5 GHz. The LNA also isolates the VCO from the antenna, so no energy is re-radiated by the antenna. The higher Q of a compact capacitively-loaded, standing-wave resonator (demonstrated by this research in [22], and discussed in detail in chapter 3) reduces the power consumption in the regenerative core from 3.2 mW (simulated with a conventional LC resonator) to a measured value of 2.1 mW. The quench bias current, which controls super-regenerative oscillator operating mode, is generated by an on-chip 9b DAC. Similar to [12], a successive approximation register (SAR) search algorithm is employed during initial calibration to estimate the critical bias current (I_{crit}), this is the value at which the active devices in the super-regenerative oscillator exactly compensate for the parasitic loss in the resonator tank. Also during the initial calibration, a frequency synthesizer tunes the receiver to one of eight possible frequency channels. An all-digital PLL controls the quench waveform generation timing so that the phase and frequency of the receiver tracks that of the transmitted data. The envelope detector senses oscillation amplitude on the super-regenerative oscillator and feeds an offset-cancelling preamplifier and a comparator. The overall output of the receiver is demodulated data along with a data clock signal.

2.2 Modes of Operation

Similar to the 2.4 GHz super-regenerative receiver, there are four working modes of the receiver. These are coarse I_{crit} search mode, frequency tuning mode, fine I_{crit} search mode, and signal detection mode. The Q of the resonator, and the parasitic loss in the tank, change with process, environmental temperature and humidity. So an exact value for I_{crit} is very hard to determine. Hence an auto-calibration scheme [12] is employed before each detection period. The calibration takes place in three steps. A coarse I_{crit}

search initially determines an approximate bias current for the VCO. Next, the oscillator is reconfigured as part of a frequency synthesizer tuning the VCO varactors. After frequency tuning, a fine SAR algorithm search determines an accurate value for I_{crit}. Repeated detection periods follow the initial critical current search and frequency tuning. The working modes of the receiver and corresponding DAC bias current waveform are illustrated in Figure 2.2.

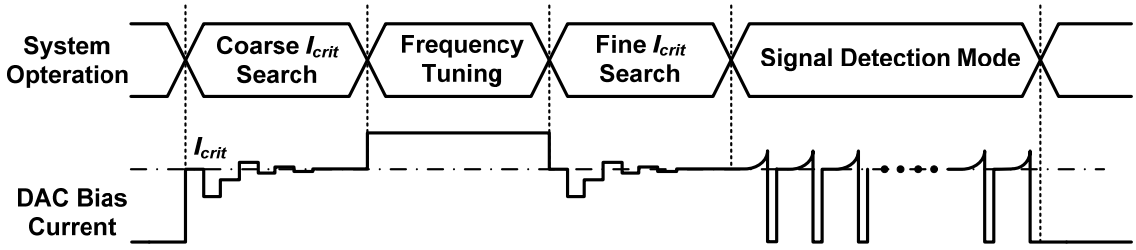


Figure 2.2: Working modes in the receiver and corresponding DAC bias current waveform.

In the frequency tuning mode, the VCO is biased with the highest possible DAC bias current (as shown in Figure 2.2), and configured as part of the PLL. The dividing ratio of the programmable divider in the PLL is changed, which adjusts the VCO control voltage (V_{ctrl} in Figure 2.1), tuning the oscillation frequency. At the end of each frequency tuning mode, the frequency synthesizer is disabled, the VCO control voltage is held on the large capacitors in the PLL loop filter. Since this tuning voltage is subject to charge leakage, frequency tuning needs to be performed periodically to recharge the capacitance in the loop filter. Because of this operation frequency drift problem, the duty cycle of each signal detection mode is short (for this design this mode lasts 10 cycles), and frequency tuning needs to be performed before each signal detection mode.

In the coarse I_{crit} search and fine I_{crit} search modes, a SAR algorithm is used to determine the value of I_{crit}. The 9-bit DAC bias current generator first sets the bias current to midscale value and checks the comparator output to determine if this current value is larger than I_{crit}. Then the binary search continues to find the rest of 9-bit bias values which are closest to, but below, I_{crit}. At the end of the fine I_{crit} search mode, the 9-bit I_{crit} values are stored for the use in the signal detection mode.

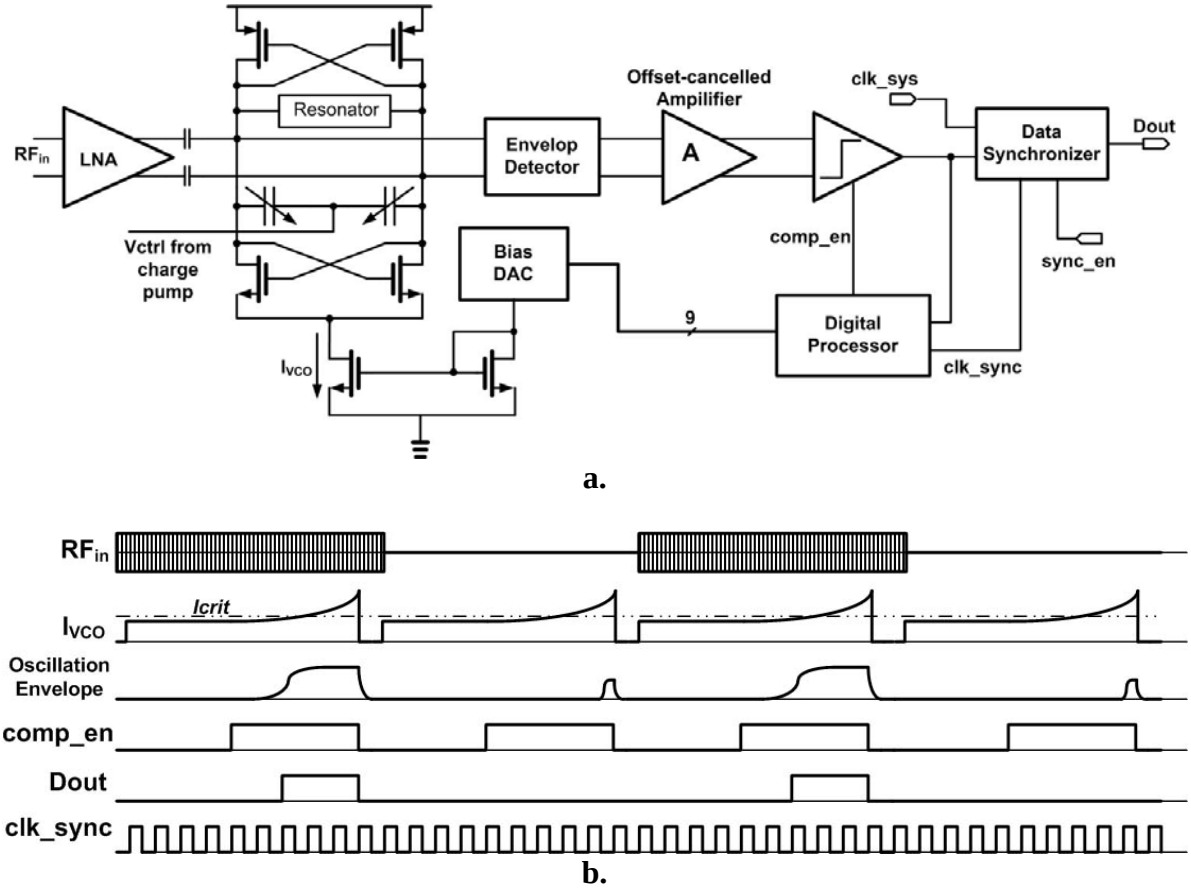


Figure 2.3: System in signal detection mode. a. Block diagram of the system in detection mode. b. Timing diagram of the system in detection mode.

Each signal detection mode lasts 10 cycles of the synchronized clock (*clk_sync* in Figure 2.3). During the first 4 cycles, the oscillator bias is set slightly below I_{crit}, so that some of the parasitic loss in the resonator is cancelled and Q is greatly increased, hence the oscillator operates as a Q-enhanced filter. This is illustrated in Figure 2.4. The tank bandwidth is inversely proportional to the Q factor. So if Q is increased, the band pass filter bandwidth is greatly reduced [12]. In this Q-enhancement period, the receiver channel selectivity is highly improved [12]. During the next 5 cycles the oscillator bias exponentially increases above I_{crit}, the oscillator envelope is detected and the comparator is enabled, so that the receiver senses the RF amplitude; and finally during the last cycle the oscillator bias is quenched, so no residual oscillation interferes with the next detection period. The variation of quench VCO bias current is shown in Figure 2.2.

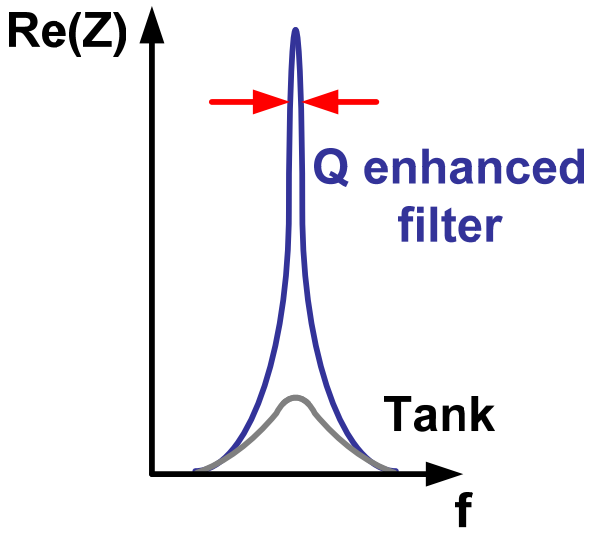


Figure 2.4: Real part of tank impedance vs. frequency with and without Q-enhancement.

2.3 Receiver Design Plan

Improving sensitivity is one of the important design concerns for super-regenerative receiver, especially when the antenna is integrated on the chip. The sensitivity of a receiver is defined as the minimum signal level that the system can detect with acceptable signal-to-noise ratio. At room temperature this is described as [3]

$$P_{in,\min} = -174\,dBm/Hz + NF_{total} + 10 \cdot \log B + SNR_{\min}, \tag{2.1}$$

where $P_{in,min}$ is the minimum detectable signal level, NF_{total} is the total noise figure of the system, B is the channel bandwidth, SNR_{min} is the minimum signal-to-noise ratio at the output. SNR_{min} depends on the data modulation method and bit-error rate (BER). For OOK modulated coherent data with BER=10^{-3}, SNR_{min} is around 7 dB [23]. The effect of channel bandwidth on the BER was studied using Matlab simulink. An OOK modulated 5 GHz digital data stream is fed through a channel with different bandwidth. The BER is calculated by comparing the data stream before and after the channel using simulink's "Error Rate Calculation" function block. The results show that to achieve a BER lower than 10^{-3}, the channel bandwidth need to be at least 3 MHz for 1 Mb/s data (5 GHz carrier frequency) and 13 MHz for 5 Mb/s data. So it is safe to suppose that the channel bandwidth of 5 MHz is big enough to correctly receive 1-2 Mb/s data with a 5 GHz carrier frequency. By substituting the values of B and SNR_{min} into Equation 2.1, we see that to achieve a sensitivity of -90 dBm the total noise figure is at most around 10 dB. For the architecture of Figure 2.1, the total noise figure of the system mostly depends on the first two stages (LNA and VCO). This is described by the Friis equation [24], where the cascaded NF of an n-stage system can be expressed as

$$NF_n = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \cdots + \frac{NF_n - 1}{G_1 G_2 \cdots G_{n-1}}, \tag{2.2}$$

where NF_i is the noise figure of the stage i and G_i is the available power gain of the stage i.

Signal distortion or IIP3 is another aspect which needs to be considered for normal RF receiver design. But for super-regenerative receiver, IIP3 is not critical, since the gain of the system mainly comes from the super-regenerative oscillator in its start-up stage. The oscillator oscillation amplitude determines the output demodulated data. The oscillation amplitude, or the envelope, is not affected by the signal distortion.

Another design consideration is the operation frequency. Since on-chip antennas are less lossy at high frequency, while super-regenerative receivers have better performance at low frequency, an RF frequency for the prototype of 5 GHz is chosen, as a compromise between antenna efficiency and receiver power consumption. The frequency plan of the system is to have 8 channels around 5 GHz with channel spacing of 20 MHz, which is wide enough to select 5 GHz 1-2 Mb/s data.

Based on the design concerns we discussed and the performance of previous super-regenerative receivers, the target sensitivity is set to be around -90 dBm, and the target power dissipation is set to be less than 10 mW. Our aim in this research is to implement a fully integrated CMOS receiver which demonstrates the possibility of integrating the RF resonator and the antenna onto the chip. We chose the IBM 0.13 μm CMOS RF/mixed-signal process, which provides the benefits of good RF/microwave performance and reliable analog/digital performance. The specifications of the proposed super-regenerative receiver are summarized in Table 2-1. Besides this prototype receiver design, we also designed a super-regenerative receiver with inductorless LNA which reduces the possible signal interference due to the RF signal reception by large inductors in normal inductor-based LNA, and hence improves the performance. This is discussed in chapter 4.

Table 2.1: Summary of the receiver target specifications

Center Frequency	5 GHz
Frequency Plan	8 channels with 20 MHz spacing
Power Consumption	< 10 mW
Data Rate	1-2 Mb/s
Sensitivity	-90 dBm
BER	10^{-3}
Technology	0.13 μm RF/mixed-signal CMOS

This chapter introduces the super-regenerative receiver and the design targets. In the next chapter, we turn our attention to the detailed design of several circuit blocks.

CHAPTER III

CIRCUIT BLOCKS

In this chapter, we discuss the design of several circuit blocks and components (such as VCO, LNA, and on-chip antenna) of the receiver. The testing results of some of the prototype components will be presented in the next chapter.

3.1 VCO with a Compact 5GHz Standing-Wave Resonator

A VCO is the most critical component in a super-regenerative receiver. It provides most of the signal gain in the receiver, and it sets the power consumption of the whole system [12]. The phase noise of integrated oscillators is limited by the low quality factor of on-chip inductors. At 5 GHz, inductor Q typically ranges from 5 to 15. Transmission-line-based standing-wave resonators have been used as an alternative to inductor-based resonant tanks, but this approach has been limited to very high oscillation frequencies (i.e. >15 GHz). Furthermore, these oscillators tend to be large because the transmission line must measure an integer multiple of a quarter wavelength [25].

To achieve a compact 5 GHz standing-wave VCO, in this work two techniques are proposed to significantly reduce resonator length so that a transmission line, measuring just $0.04\lambda_0$, achieves a simulated resonator quality factor of 35. The predicted resonator Q is confirmed by phase noise measurements of a prototype standalone VCO. Periodic capacitive-loading reduces wave velocity and wavelength; while capacitive termination reduces the required length of the transmission line to a fraction of the already reduced wavelength. A high Q is achieved because a short transmission line has

low substrate and ohmic losses. Furthermore, the oscillator operates at the frequency of peak resonator Q, not at the resonator self-resonant frequency.

3.1.1 Resonator Design

A single-ended standing-wave oscillator can be formed with a quarter-wavelength transmission line, connected at one end to AC ground, and at the other end to a negative resistance. A differential standing-wave oscillator is formed by connecting a half-wavelength transmission line to a differential negative resistance. In this work, the length of the transmission line is shortened to below a half wavelength by terminating the differential transmission line with capacitors. The amplitude of a standing wave along a transmission line is position-dependent and the current distribution along a linear transmission line resonator can be expressed as:

$$I(z) = I_0 \cos\left(\frac{2\pi}{\lambda} z\right), \tag{3.1}$$

where λ is the wavelength in the transmission line, and z is the position, normalized to λ. This distribution along $|z|<\lambda/4$ is shown in Figure 3.1. The current density falls to 0 at the ends of the transmission line, where the voltage amplitude is maximum, whereas, the current density is maximum at the center of the line, where the voltage amplitude is 0.

A shorter transmission line can be used to achieve the same resonance frequency if the ends of the shorter transmission line are terminated with capacitance. Figure 3.1 shows that the current density at any point along the length of the modified transmission line is maintained the same as in the same section of the original line. The current distribution along the shorter line is identical to that in the corresponding portion of the original transmission line, and thus the same resonance frequency is achieved.

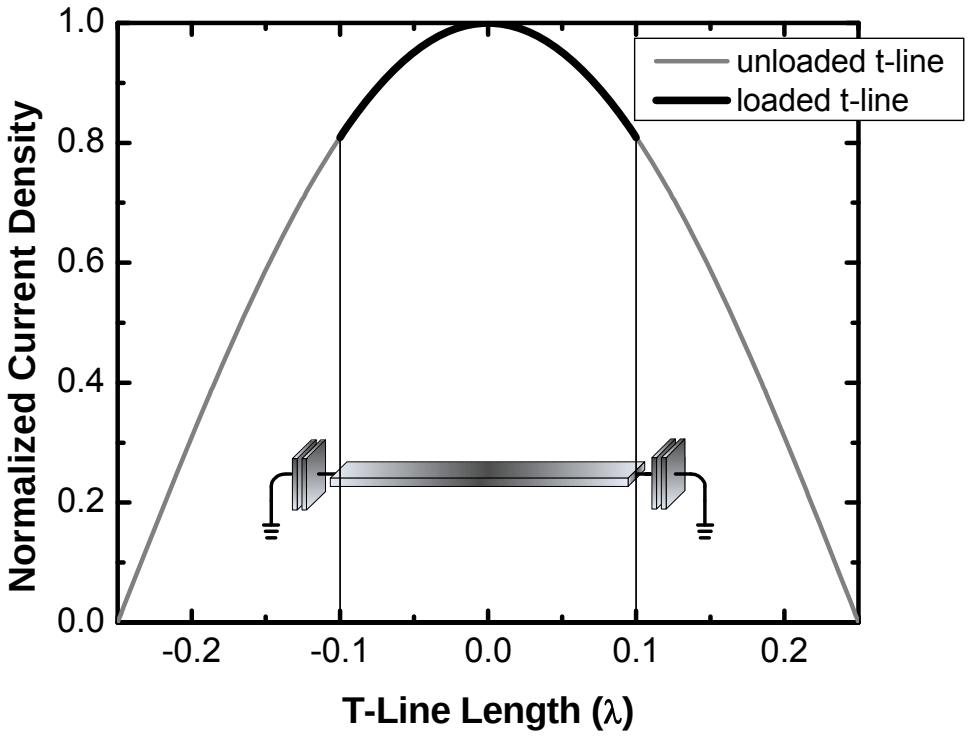
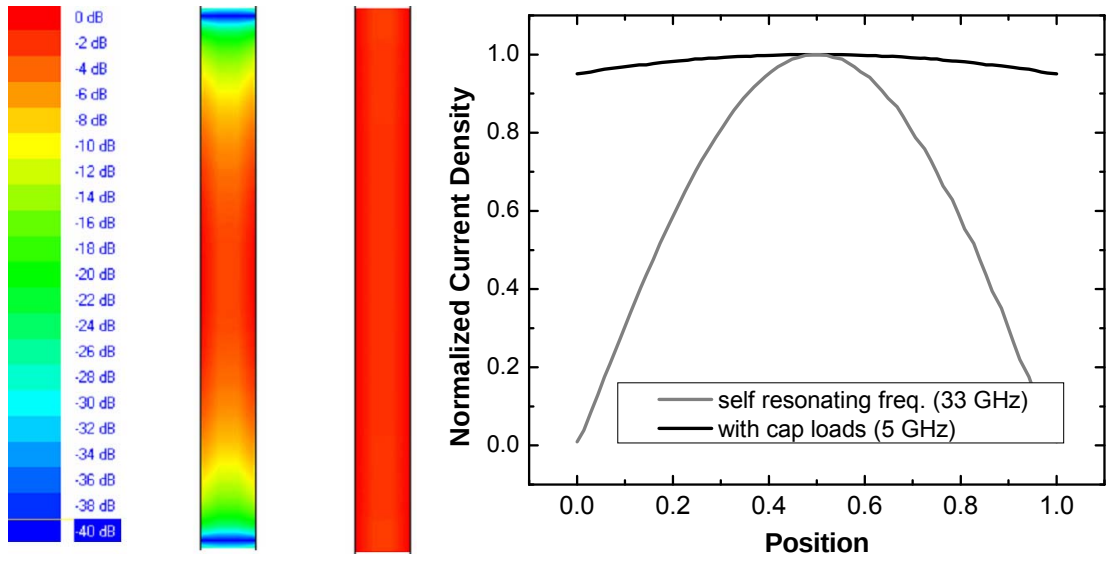


Figure 3.1: Current distributions on a half-wavelength and on a capacitively loaded transmission line.

A 3D EM simulator (Zeland IE3D) is used to compare the current density along a transmission line under two different conditions. Without capacitive loading at the ends of the transmission line, *λ/2* becomes equal to the length of the line, and the resonance frequency is 32 GHz. With the addition of capacitive loading at the ends of the line, *λ/2* becomes much larger than the length of the transmission line and the resonance frequency falls to 5 GHz (Figure 3.2b and 3.2c).

At the lower frequency, since the standing wave mimics that part of the standing wave in the central portion of a much longer transmission line, the current distribution is much more uniform. This is advantageous since because of the uniform distribution tapering [25] is not required and a transmission line with a uniform width can be used.



(a) (b) (c)

Figure 3.2: Simulated current distribution along a shortened transmission line; (a) at the self resonating frequency (32 GHz), (b) with capacitive loads at the ends of the line (at 5 GHz), and (c) simulated normalized current density along the transmission line for both cases

Figure 3.3 shows the equivalence between capacitor loaded transmission line resonator and unloaded transmission line resonator. The relationship between loading capacitor and reduced transmission line length is determine by

$$C = \frac{\tan\theta_2}{Z\omega}, \tag{3.2}$$

where θ_2 is the effective reduction in electrical length (a multiple or submultiple of the wavelength), ω is the resonant frequency, and Z is the impedance [24].

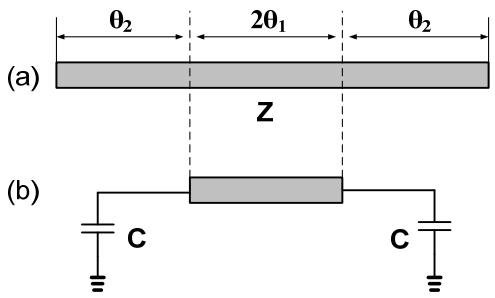


Figure 3.3: (a) Unloaded transmission line resonator. (b) Loaded transmission line resonator.

In this work, we trade off transmission line length and termination capacitance, to achieve an optimum total resonator Q at a given frequency. This tradeoff is introduced qualitatively in Figures 3.4 and 3.5. Figure 3.4 shows the variation in quality factor versus loading capacitance C_p. (It should be noted that since the line length is fixed the resonance frequency also changes with loading capacitance.) There are two distinct regions in the curve: a high capacitance (low frequency) region on the right side of line B, where metal resistance mainly determines the Q; and low capacitance (high frequency) region on the left, where the skin effect and energy coupling to the lossy substrate introduce more losses and the Q ceases to increase with frequency. To achieve best performance, the resonator should be loaded with capacitance to resonate around line B and achieve the peak quality factor.

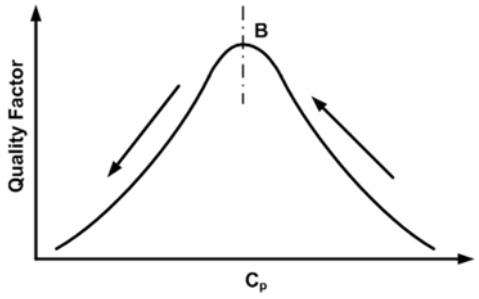


Figure 3.4: Qualitative variation in Q with load capacitance for a given transmission line length

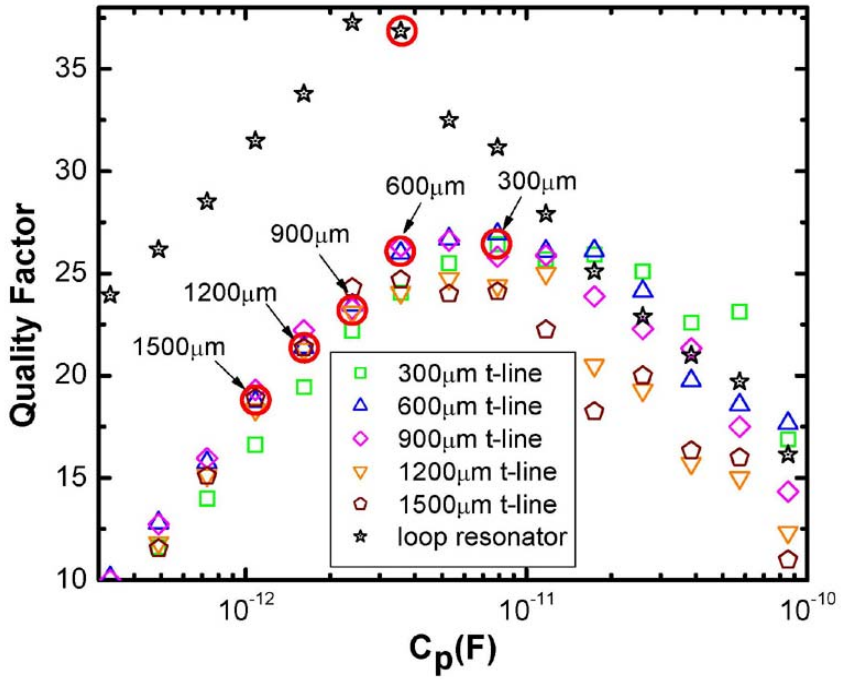


Figure 3.5: Simulated quality factor versus loading capacitance for various transmission line lengths. The circles identify the capacitance values that achieve a 5 GHz resonance frequency for each line length.

To achieve an optimum Q for a given resonance frequency, the tradeoff between line length and capacitance is examined. Five straight transmission line resonators, ranging in length from 300 μm to 1500 μm, and with various capacitive loadings are simulated. The simulation results are shown Figure 3.5, and for each line length a circle identifies the capacitance loading value that achieves a 5 GHz resonant frequency. The characteristic described in Figure 3.4 is apparent.

As shown in Figure 3.6a, the prototype resonator consists of a thick metal rectangular loop over a thin floating metal shield. To reduce ohmic losses, the metal conductor of the resonator is formed with the top three metal layers, connected in parallel. The floating metal shield is formed with floating metal strips, with each strip

formed with the lower five metal layers connected in parallel. This use of parallel strips not only helps reduce the strip resistance but also helps meet the stringent metal fill requirements of the 0.13 μm process. The strip structure also breaks induced eddy currents. When the resonator is differentially connected, the floating metal shield is a virtual ground, which provides a better shield to the lossy substrate. Unlike the case with a conventional inductor, the top of the floating metal shield is relatively close to the conductor (only 1.4μm away), so that the shield deliberately loads the resonator with capacitances. The transmission line with a close by metal shield can be modeled as an LC ladder (Figure 3.6b), where L is series inductance per unit length and C is shunt capacitance per unit length). Capacitors C_p model the capacitance between transmission line and shielding layers. The new equivalent capacitance is $C+C_p$ and the phase velocity is:

$$v_p = \frac{1}{\sqrt{(C + C_p)L}}, \tag{3.3}$$

which is smaller than without metal shielding. Periodic capacitive loading introduces the slow-wave effect [26, 27]. The slow wave effect was demonstrated by H.M. Barlow [28], by placing an array of uniformly spaced parallel wires along a rectangular waveguide. Since the wave-velocity and wavelength are reduced, the slow wave effect allows size to be reduced, and the quality factor to be increased. (The predicted Q versus capacitive loading is over-laid on Figure 3.6b) The combination of the slow-wave-effect and capacitive loading at the ends reduces the length of the transmission line to only $0.04\lambda_0$ (λ_0 is the wavelength in free space).

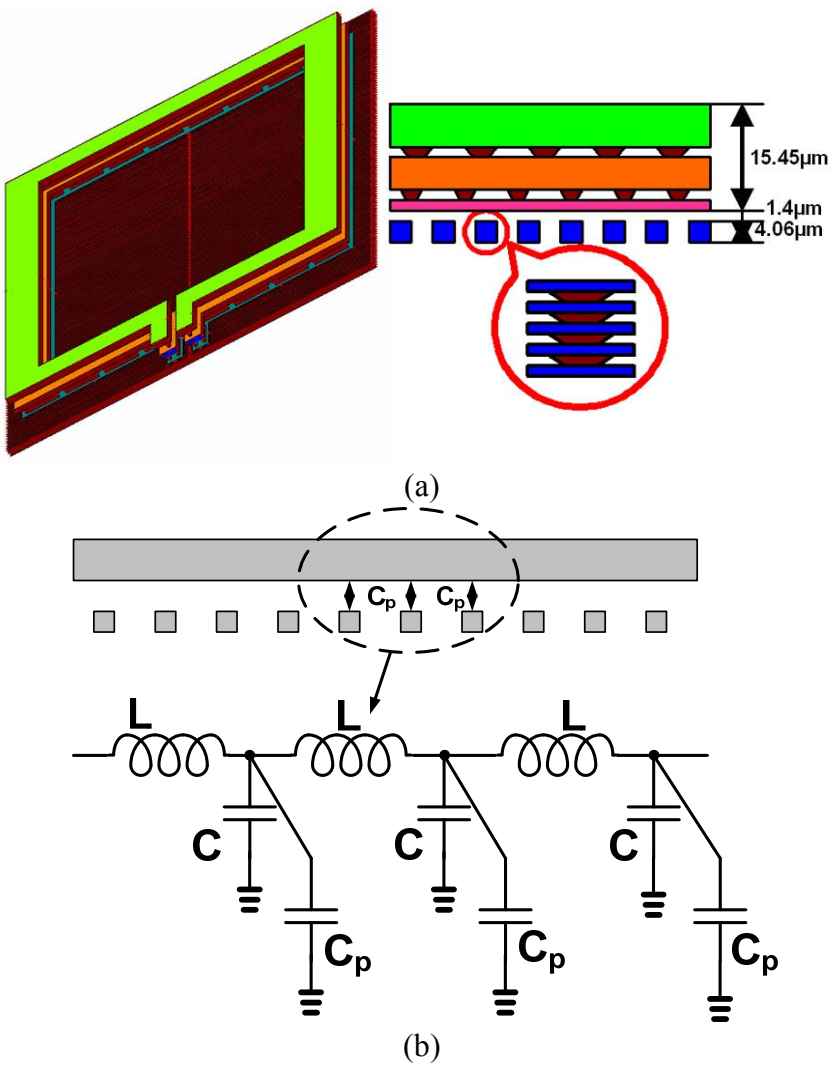


Figure 3.6: (a) Capacitively-loaded slow-wave transmission line resonator. (b) Transmission line with metal shields and the corresponding equivalent circuit.

3.1.2 Prototype Oscillator

Based on this resonator a 5 GHz VCO is designed. A schematic of the prototype oscillator is shown in Figure 3.7. As in most LC oscillators, cross-coupled FETs introduce negative resistance. Current reuse due to the use of NMOS and PMOS cross coupled FETs improves power efficiency. Two 0.83 pF capacitances are connected at the ends to the transmission line. Varactors are used to achieve 22% tuning range. Two common-source output buffers drive 50 Ω loads.

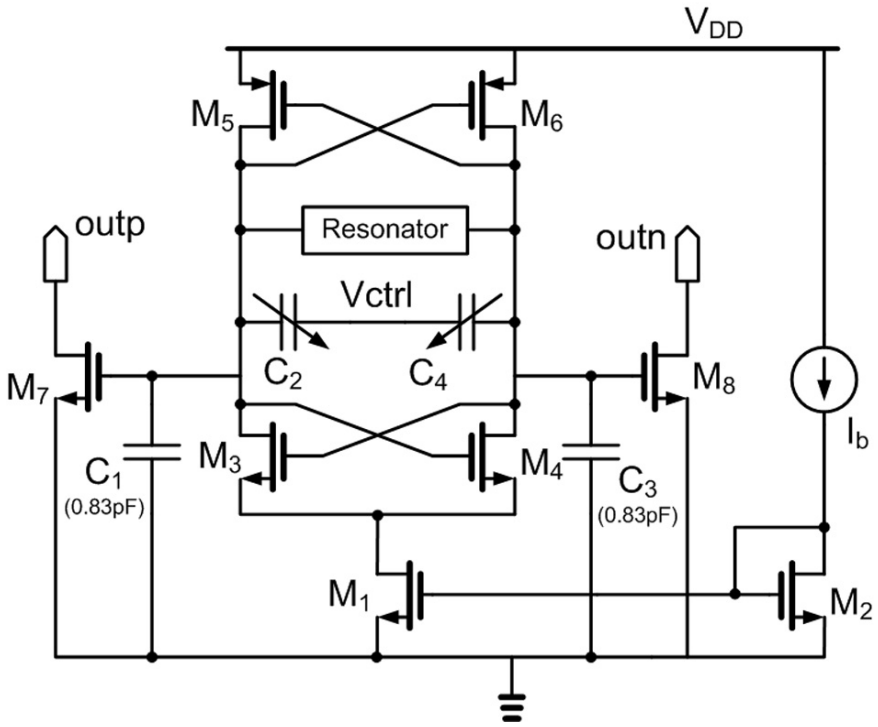


Figure 3.7: VCO schematic.

To compare with an inductor based VCO, the resonator in the VCO is replaced with an inductor (L=0.5 nH, physical size 200 μm×200 μm). To do the comparison, in the simulation, the same bias current is supplied to both VCOs. The simulated phase noise of both is shown in Figure 3.8. There is about a 6.8 dBc/Hz phase noise improvement at 1 MHz offset with the resonator based VCO.

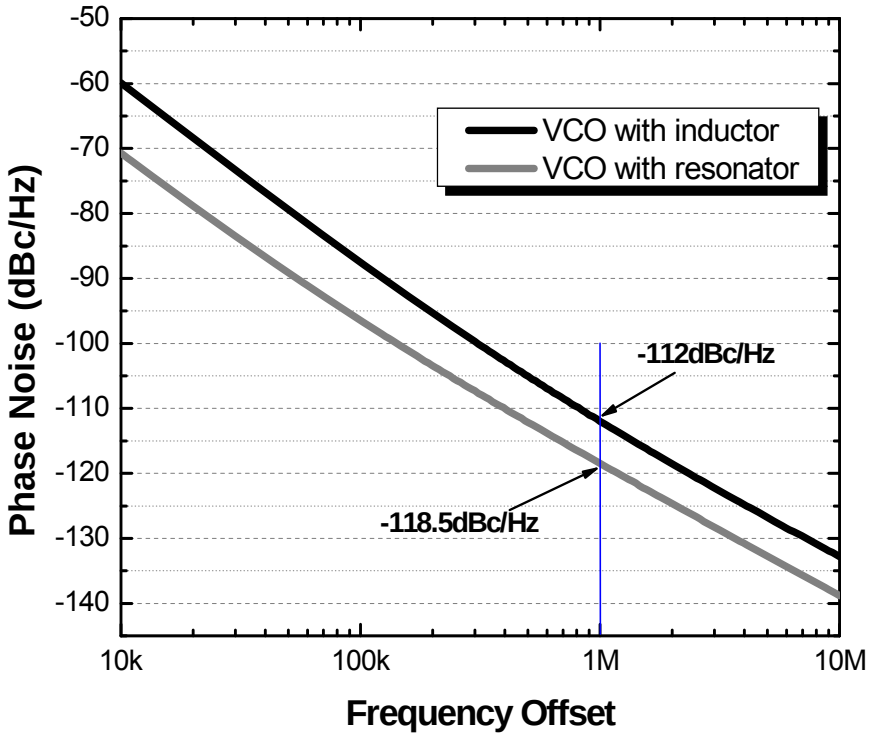


Figure 3.8: Phase noise comparison between resonator VCO and inductor VCO.

The methodology of on-chip resonator design is also used to design a 5 GHz on-chip band pass filter. This is discussed in Appendix A.

In the super-regenerative receiver, the VCO serves as an amplification device and provides most of the gain. The VCO works mostly in oscillation startup period, rather than a stable oscillation state. The phase noise is not critical, but the amplitude noise during startup is more important [12]. This amplitude noise affects the oscillation startup and hence the minimum detectable input single level (i.e. the sensitivity).

In this VCO, we employ a resonator with a higher Q to reduce the power consumption. Because a larger Q means the "Barkhausen criteria" for oscillation can be satisfied with smaller transconductance from transistors (M_3-M_5 in Figure 3.7), the VCO current can be reduced [29].

3.2 On-chip Antenna[2]

Integration of an antenna with the rest of a receiver on a single IC is perhaps the last barrier to achieving a totally integrated single-chip wireless system. Over the past few years, a number of researchers have attempted to address this increasingly important problem [30-33]. These studies report on using basic dipole-type on-chip antennas operating in frequency bands ranging from 7.4 GHz to 77 GHz. In all of these studies, the on-chip antennas are fabricated in a standard CMOS processes but they demonstrate very low radiation efficiencies. This is mainly a consequence of the close proximity of the antenna to the lossy silicon substrate underneath it. This excessive loss significantly deteriorates the gain and radiation efficiency of these antennas. In this section, we present two miniaturized, on-chip slot antenna prototypes working at around 9GHz and 5GHz, respectively. The 9 GHz prototype antenna, also described in [34], has a much higher gain and efficiency compared to state-of-the-art on-chip antennas operating in a similar frequency range. Two main factors contribute to this enhanced performance: the choice of a slot-type antenna (as opposed to a dipole-type antenna) and the effective shielding of the antenna from the low resistivity silicon substrate.

Slot antennas can be considered to be dual of dipole- or wire-type antennas. For the same occupied area, slot antennas have a much larger metal area compared to wire-type antennas, since everywhere, except the antenna aperture, is covered with metal. In this way, the radiating currents are distributed over a larger metallic area and hence, the ohmic losses in a slot antenna are significantly smaller than those in dipole or other wire-type antenna. In miniaturized antennas, where the radiation resistances are usually very small, even small changes in ohmic losses have major implications on the radiation

[2] This part is done with the collaboration with Nader Behdad and Wonbin Hong from The University of Michigan Radiation Lab.

efficiency of the antenna. Therefore, by using a miniaturized slot topology, the radiation efficiency of small on-chip antennas can be significantly enhanced.

The topology of the proposed 9 GHz on-chip slot antenna is shown in Figure 3.9. Figure 3.10 shows the top view of the slot antenna. The antenna is composed of a straight slot section connected to two balanced spirals at its end. The antenna is designed such that its overall electrical length, from the feed point to the end of each balanced spiral, is about a quarter of a wavelength ($\lambda/4$) at the center frequency of operation. This way, this structure acts as a resonant monopole slot antenna and occupies a significantly smaller area compared to traditional dipole or slot antennas. The two feed terminals of the antenna are located at its center, as shown in Figure 3.10. In the current design, these two terminals are connected to the input of the LNA using vias. The antenna occupies a die area of only 0.3 mm^2 and operates in the frequency range of 9-10 GHz. The electrical dimensions of the antenna are $0.017\lambda_0 \times 0.017\lambda_0$, making it 30 times smaller than traditional dipole or slot antennas operating at the same frequency band.

To shield the antenna from the low-resistivity silicon substrate below it, a composite ground plane is used underneath the antenna. This low-resistivity ground plane significantly reduces the adverse affects of the lossy substrate on the performance of the antenna. Presence of the ground plane prevents the fields from penetrating deep into the lossy silicon substrate and reduces the field density in the lossy regions near the antenna. This prevents the substrate from dissipating the power that would otherwise have been radiated, hence increasing the radiation efficiency of the antenna.

The slot antenna is fabricated on the highest of the metal layers available in the CMOS process. The 4 μm thick aluminum top layer has the lowest surface resistivity. The lower metal layers that are used to implement the shielding ground plane are much thinner (0.6 μm) and have a much higher surface resistivity. In order to circumvent the adverse affects of the high resistivity of these metal layers on the efficiency of the on-chip antenna, the shielding ground plane is composed of two floating individual ground

planes placed on two lower metal layers. These layers, each 0.6 μm thick, are separated by a 0.6 μm oxide layer. This way, the capacitance between the two metal layers is large enough that they act as a single ground plane with a much lower surface resistivity and there is no need to physically connect the two floating metallic layers with multiple vias. The antenna layout fully meets the stringent metal fill and density requirements of the 0.13 μm process.

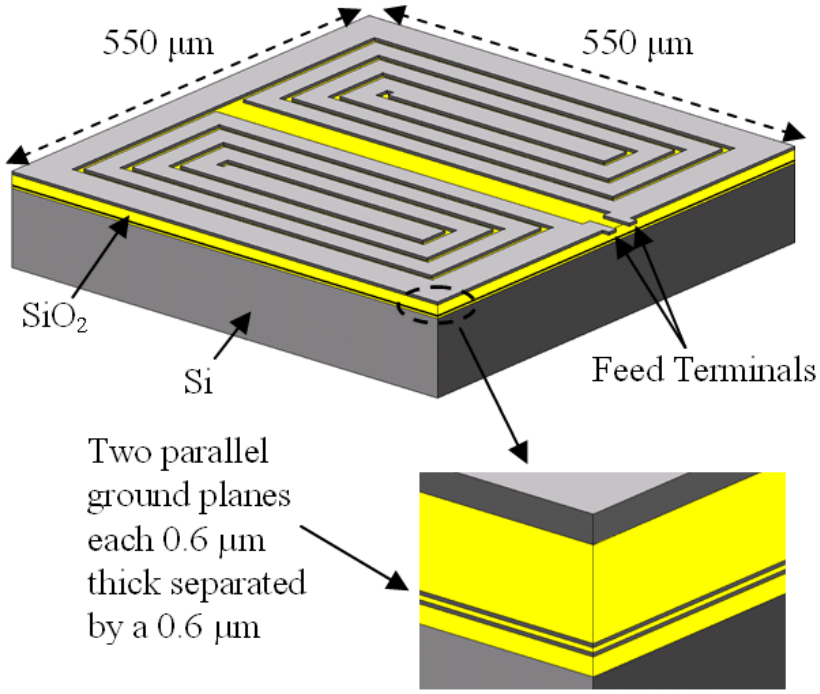


Figure 3.9: Topology of the proposed miniaturized on-chip slot antenna. The antenna and shielding are implemented with standard RF interconnect layers (figure courtesy of our collaborator, Nader Behdad [34]).

Using the same technology, a 5 GHz on-chip is designed for the super-regenerative receiver. The on-chip 5 GHz antenna occupies a die area of only 0.47 mm^2. The electrical dimensions of the antenna are $0.010\lambda_0 \times 0.011\lambda_0$, making it 50 times smaller than traditional dipole antennas operating in the same frequency band.

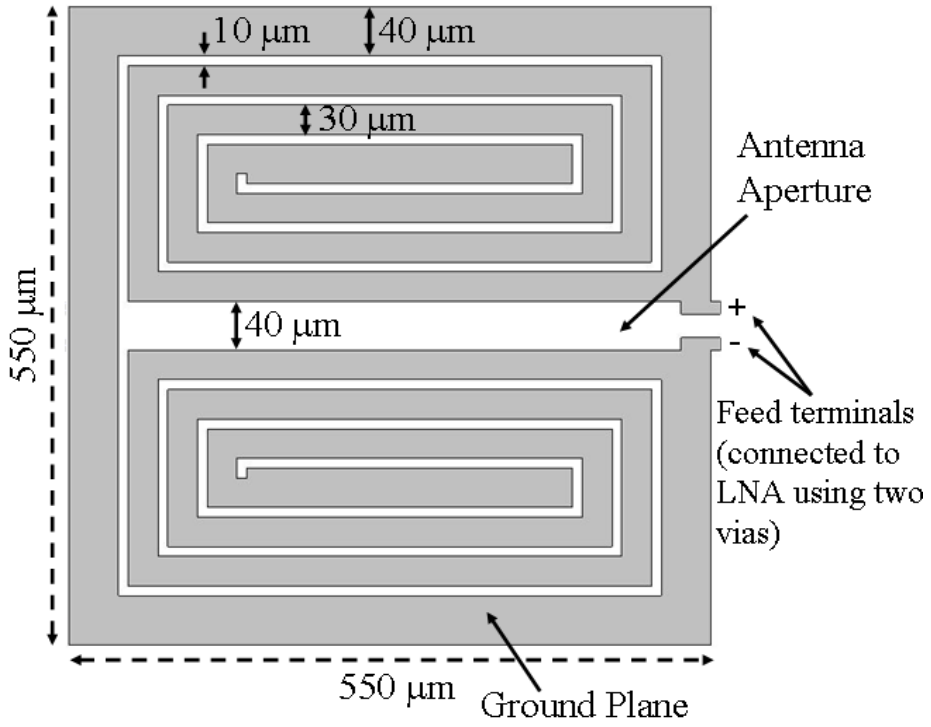


Figure 3.10: Top view of the miniaturized 9 GHz on-chip slot antenna. The feed terminals are located at the center of the antenna and are connected to the LNA using two vias (figure courtesy of our collaborator, Nader Behdad [34]).

3.3 CMOS LNA

The LNA is the first block in the receiver chain and is used to amplify the weak RF received signal. It provides signal amplification without degrading the signal-to-noise ratio too much. As discussed in chapter 2, it together with super-regenerative oscillator determines the noise figure of the whole system. For a super-regenerative receiver, the LNA also prevents the oscillator signal radiating back to the on-chip antenna. There are several LNA topologies. A common-source LNA with inductive degeneration and an inductorless LNA are discussed in this section.

3.3.1 Common-Source LNA with Inductive Degeneration

Common-source LNA with inductive degeneration is widely used in many designs. It achieves noise matching and power matching using passive components. This topology is shown in Figure 3.11 [6, 35]. The input impedance is

$$Z_{in} = \frac{1}{j\omega C_{gs}} + j\omega(L_g + L_s) + \frac{g_m L_s}{C_{gs}} + r_{g,NQS}, \tag{3.4}$$

where the last term originates from the Non-Quasi Static (NQS) Effects. When the transistor operates at a very high frequency, the charge induced in the channel takes some time to drift to the drain. The channel acts as a lossy transmission line, which introduces transit delay. This delay causes the gate resistance $r_{g,NQS}$. Usually the impedance is matched to 50 Ω source load. But as discussed by J. Janssens and M. Steyaert [35], the minimum noise figure is achieved for a source load of about 100 Ω when the NQS effect is considered. We choose an 80 Ω impedance for the LNA designed for a 9 GHz prototype on-chip antenna. To achieve the matching, L_g and L_s must be tuned to cancel out the impedance of the gate capacitance C_{gs}, i.e. $L_g + L_s = 1/\omega^2 C_{gs}$.

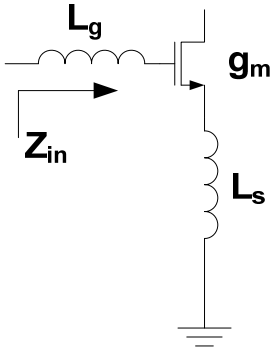


Figure 3.11: Common-source LNA with inductive degeneration.

The schematic of a single-ended LNA is shown in Figure 3.12. The LNA input is matched to the previous stage (e.g. output of an antenna). Transistor M_5 with resistors R_1 and R_3 provides a DC bias for the LNA input and the output buffers. To allow for simulation inaccuracy and process variation, a feedback network consisting of C_f and R_f is employed to widen the bandwidth of the LNA. DC blocks are used at the input, the output and between the LNA core and the buffer to achieve proper bias conditions.

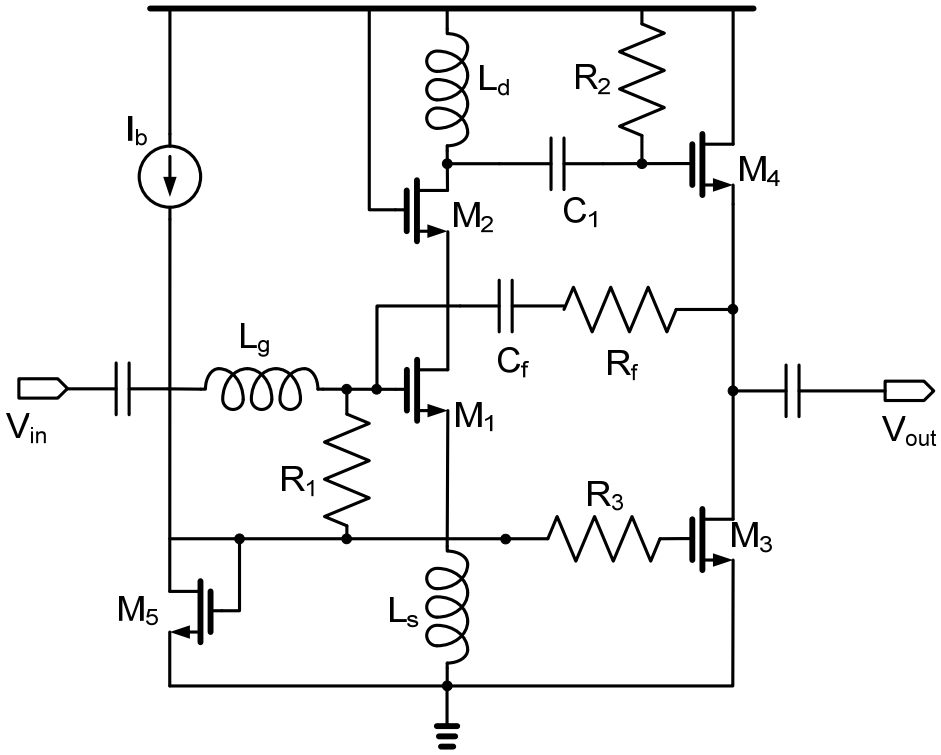


Figure 3.12: The schematic of a single-ended LNA.

3.3.2 Inductorless LNA

Common source topology with inductive degeneration has the best reported noise figure, but its bandwidth is narrow. So in multi-standard or Ultra Wide Band (UWB) receivers, more than one LNA using this topology are required to cover the whole

bandwidth. Moreover, high quality on-chip inductors normally occupy large chip area, and they are not available in a digital CMOS process. Hence, a broadband and inductorless LNA is normally used in multi-standard or wideband application. Many broadband LNAs [36-38] employ resistive feedback to broaden the frequency response bandwidth. But there is a tradeoff between bandwidth, noise figure, gain performance and power consumption in this topology. To improve the noise performance, Bruccoleri et al. [39, 40] exploited feed forward thermal noise canceling techniques in wideband LNA design, where thermal noise from the input stage is sensed and canceled by the noise from the feed-forward network. In this part, we present a wideband LNA with a topology where both resistive feedback and thermal noise canceling techniques are used. In the super-regenerative receiver a wide band LNA can be used because with the on-chip antenna, the bandwidth requirement of LNA is relaxed since the antenna has a limited pass band. Furthermore the VCO can work as a channel-select Q-enhanced filter during Q-enhancement mode. So wideband LNA can be used in the receiver.

Figure 3.13 is the schematic of an inductorless LNA with resistive feedback and noise cancelation. The first stage in the feed-forward path in the LNA is a cascode common source amplifier, which includes the common source transistor M_1, the cascade transistor M_2 and the load resistor R_3. The cascode transistor is used to increase the output impedance and the reverse isolation. The second stage is a noise canceling stage. An RC feedback network (R_f and C_f in Figure 3.12) is used to increase the bandwidth. Capacitor C_3 compensates for the parasitic capacitance (at the drain node of M_2 and the gate node of M_4) and also widens the bandwidth [36]. Resistors R_1 and R_4 provide DC bias. The input impedance at moderate frequencies is set as

$$Z_{in} = \frac{R_f}{1 + A_v} \approx \frac{R_f}{A_v}. \tag{3.5}$$

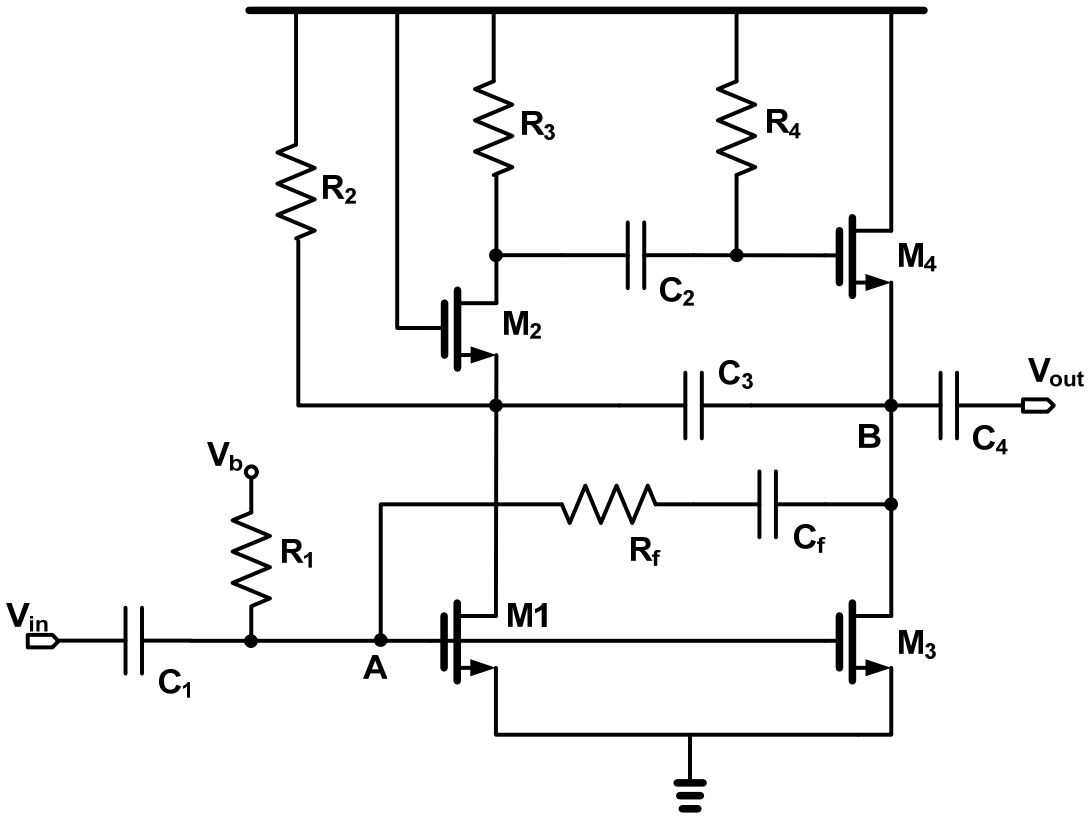


Figure 3.13: The schematic of a single-ended inductorless LNA.

Figure 3.14 explains the mechanism of noise canceling in the circuit. The noise signal due to transistor M_1 at node A flows out of the node A through feedback path (R_f, where C_f is omitted for simplicity) and common source transistor M_3, leading to two opposite-signed noise voltages at the output node B. These two noise signals cancel each other. By carefully designing the circuit parameters, the total output noise is reduced. The cancellation condition is

$$A_{v,2} = 1 + \frac{R_f}{R_s}, \tag{3.6}$$

where R_s is the source impedance, $A_{v,2}$ is the gain of the second stage [39].

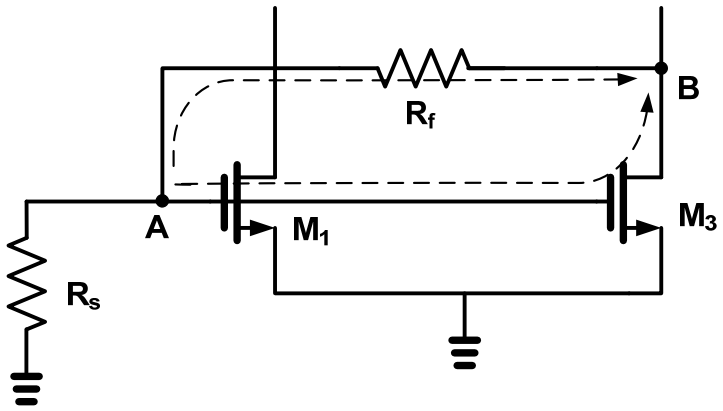


Figure 3.14: LNA noise cancelling mechanism.

3.3 Frequency Synthesizer

Another critical block in the receiver is the frequency synthesizer which is implemented as a phase locked loop (PLL). This is used to tune the VCO frequency to the channel of interest. This frequency synthesizer is a third order type-II integer-N charge pump PLL. The architecture is depicted in Figure 3.15. We employ a charge pump PLL, because its pull-in range is limited only by the VCO tuning range and the charge pump output voltage range [41]. The 5 GHz VCO with on-chip resonator described in section 3.1 is utilized in this PLL. The oscillation output from the VCO is sensed by the feedback divider in the loop. The divider ratio varies from 464 to 478 depending on the digital channel-select input. This divider generates frequency step of 10.5 MHz, which is compared with reference clock *clk_ref*. This step is half the channel spacing (21 MHz), so that the reference spurs fall at the edge of each channel rather than the center of adjacent channel, which allows higher spur magnitude in the PLL synthesizer output signal [42].

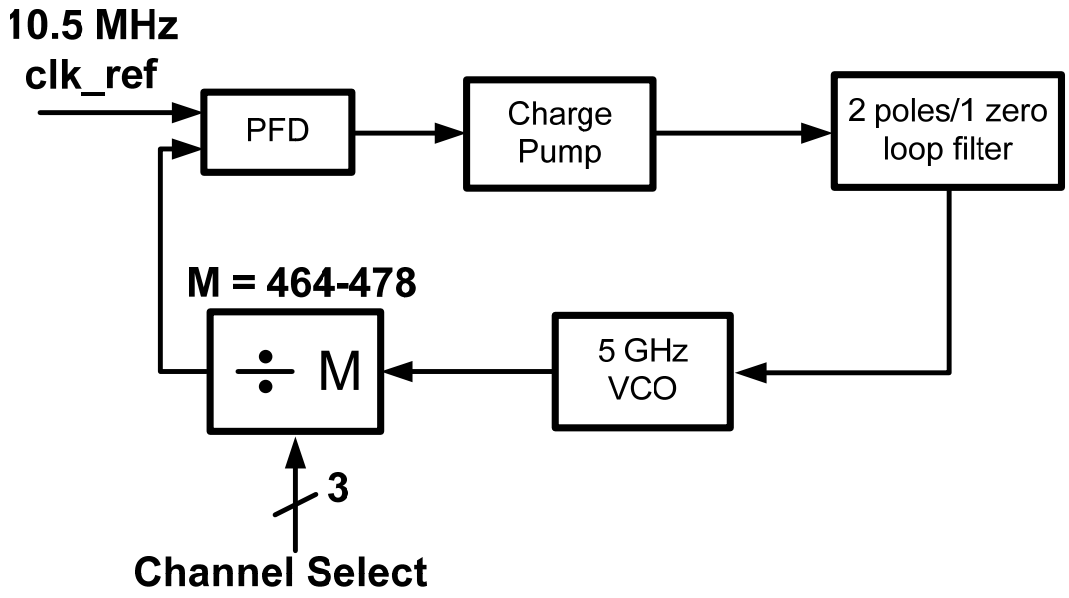


Figure 3.15: Block diagram of the frequency synthesizer.

3.3.1 Differential to Full Swing Converter

A differential to full swing converter (not shown in Figure 3.15) used between oscillation nodes of the VCO and input of the divider is shown in Figure 3.16. It is required since the divider input is single-ended. The converter consists of an opamp style circuit which converts the differential input to a single-ended output. A chain of inverters with feedback resistors amplifies the singled-end signal to the full swing level. The resistor feedback changes the inverter threshold voltage and makes the circuit robust against DC offset [43]. The inverter size increases along the chain, so that the converter can drive a larger load from the input of the following divider.

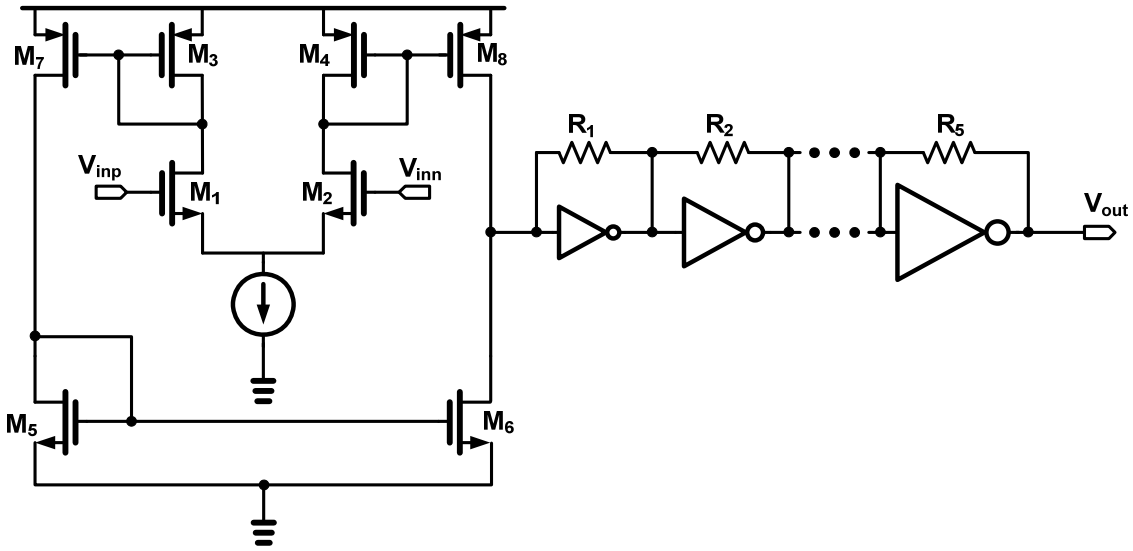


Figure 3.16: Schematic of differential to full swing converter.

3.3.2 Programmable Divider

The divider is based on the pulse-swallow technique. This technique was first used by J. Nichols and C. Shinn [44] in a PLL to minimize the use of high-speed logic and hence lower the power consumption. Figure 3.17 is a block diagram of a conventional pulse-swallow divider, which consists of a two-modulo prescaler (divide by *N+1* or *N*), a fixed-ratio program counter, and a programmable swallow counter. The modulus control bit (*mc*) controls the ratio of the prescaler. Initially, the prescaler divides input signal f_{in} by *N+1*. When the swallow counter is full, it feeds back a control signal to the prescaler and changes the ratio to N. So the total dividing ratio of the divider is

$$N_T = (N+1)\cdot S + N\cdot(P-S) = NP + S\,, \tag{3.7}$$

where P is the ratio of program counter, and N is the ratio of swallow counter which is determined by the channel select. The output signal frequency is

$$f_{out} = \frac{f_{in}}{NP + S}. \tag{3.7}$$

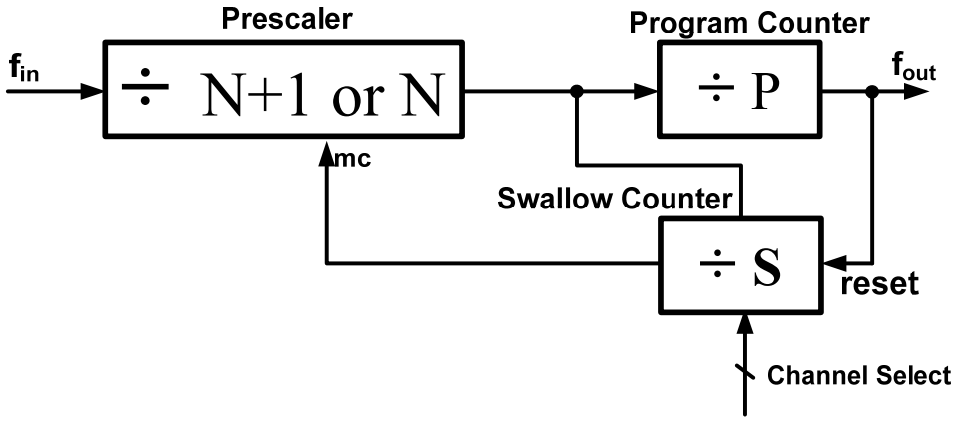


Figure 3.17: Block diagram of conventional divider.

The pulse-swallow divider used in this PLL is shown in Figure 3.18. To achieve faster operation and lower power consumption, a True Single Phase Clock (TSPC) D-flip-flop [45] shown in Figure 3.19 is used in the first stage. A block diagram of the prescaler is illustrated in Figure 3.20. A modular structure consisting of a chain of 2/3 divider cells is employed in the prescaler [46, 47]. There are several advantages to using this modular structure. First, gated latches are utilized in each divider cell to pass synchronized control signal to the previous stage, so synchronization is done locally between neighboring stages. Second, the power dissipation can easily be optimized. Faster but higher-power latches are used only in the divider cells at the head of the divider chain, while at the chain end slower but lower-power latches are employed. Another advantage is that the layout is facilitated since a modular structure is used.

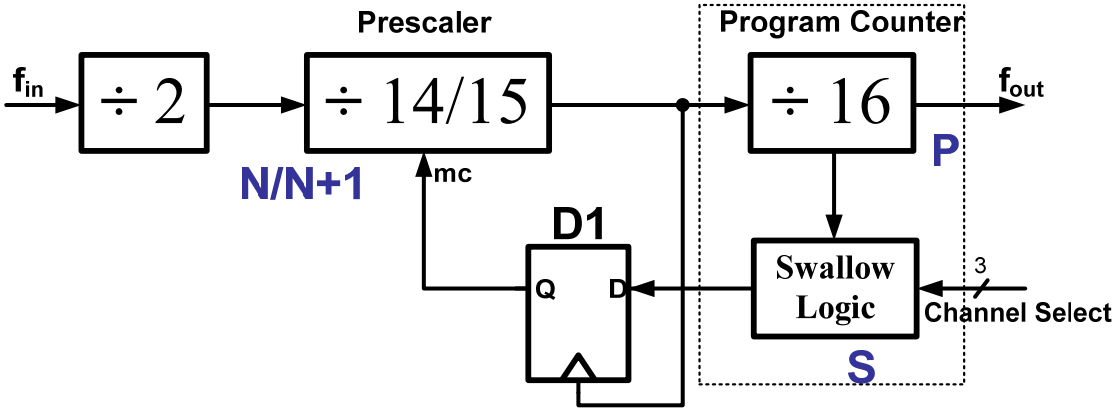


Figure 3.18: Block diagram of the pulse-swallow divider.

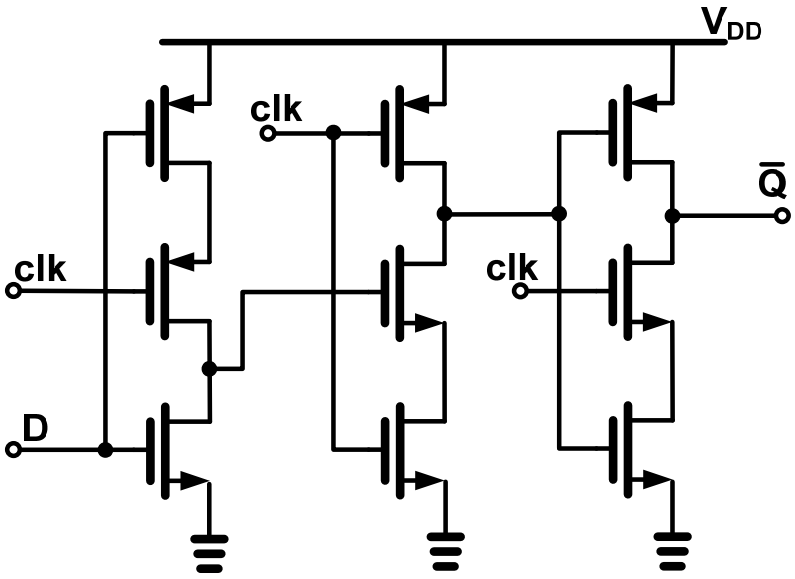


Figure 3.19: Schematic of TSPC D-flip-flop.

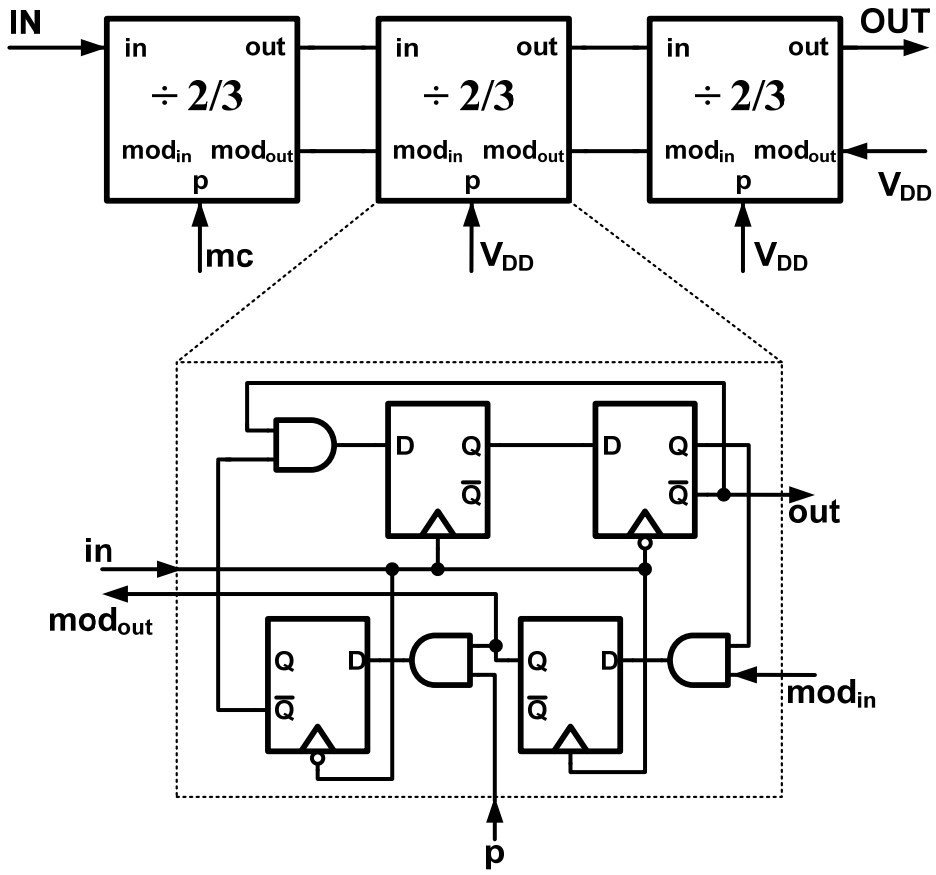


Figure 3.20: Block diagram of modular prescaler.

To simplify the circuit, a single ripple counter is used for the program counter and pulse-swallow counter [48]. This is shown in Figure 3.21 which is a combination of the program counter and swallow logic in Figure 3.18. Compared with the conventional pulse-swallow divider in Figure 3.17, the prescaler modulus control signal is pipelined by an extra D flip-flop (D1 in Figure 3.18) [42], which increases the overall divide ratio to

$$N_T = (N+1)\cdot\left(S+\frac{P}{2}\right)+N\cdot\left(\frac{P}{2}-S\right)=NP+S+\frac{P}{2}. \tag{3.8}$$

Compared with equation 3.7, this is larger by *P/2*. So the output signal frequency is

$$f_{out} = \frac{f_{in}}{NP + S + P/2}. \tag{3.9}$$

Hence a *P/2* higher divide ratio is achieved with the same divide ratio of program divider (*P*) and swallow divider (*S*) as in conventional swallow divider.

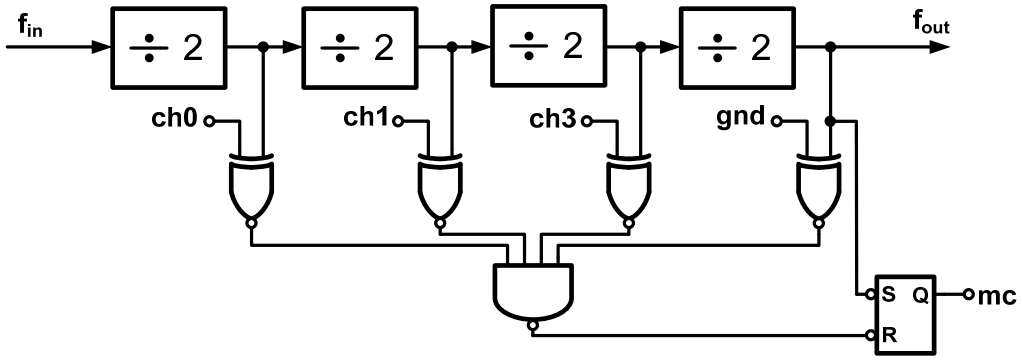


Figure 3.21: Block diagram of program counter with swallow logic.

3.3.3 Phase Frequency Detector (PFD)

A PFD is a circuit block which detects both phase and frequency difference between the input signal and reference signal. A schematic of the PFD used in the frequency synthesizer is shown in Figure 3.22 [29]. This is a tri-state sequential PFD which generates two non-complementary outputs. It consists of two edge-triggered, resettable D flip-flops with the D inputs connected to logical *HIGH*. The two D flip-flops are driven by reference signal (V_{ref}) and converted single-ended VCO signal (V_{in}), respectively. The PFD works as follows. If the phase of signal V_{ref} is less than that of signal V_{in}, then a positive pulse is generated in signal "*up"*, while signal *"down"* remains at zero. If the phase of V_{ref} is higher than that of V_{in}, then a positive pulse appears in *"down"* and *"up"* remains zero. If the phases are equal, then both *"up"* and *"down"*

signals remain zero. So the circuit changes between three logical states: *up*=*down*=0; *up*=0, *down*=1; and *up*=1, *down*=0. This happens only on the rising transitions of V_{ref} and V_{in}. But this PFD may potentially suffer from a "dead zone", which happens when the phase difference between the two signals approaches zero [29, 41]. A delay buffer is added in the reset path in the PFD, which creates simultaneous pulses in "*up*" and "*down*". And this eliminates the dead zone problem.

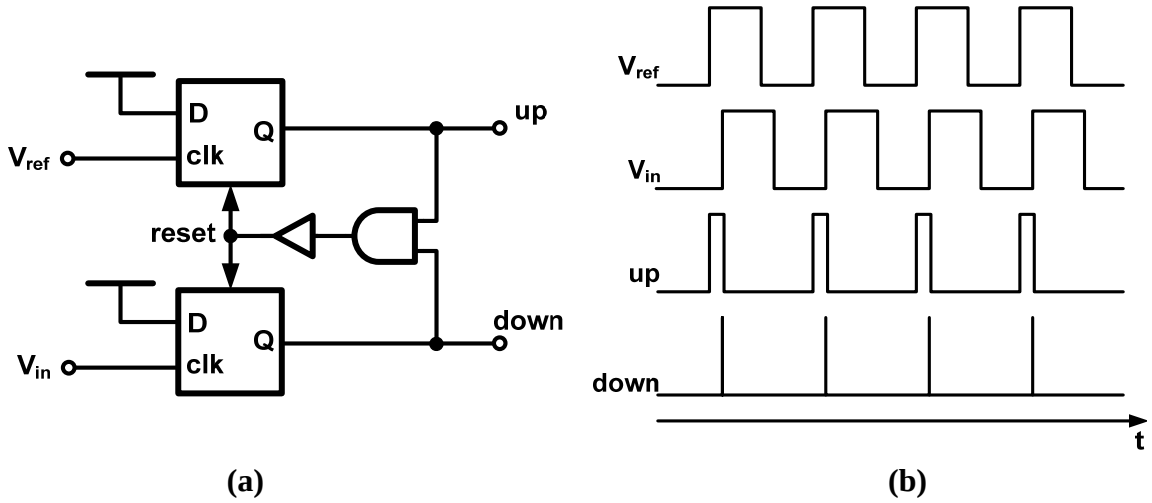


Figure 3.22: Block diagram of PFD and corresponding timing diagram.

3.3.4 Charge Pump and Loop Filter

The "*up*" and "*down*" signals from the PFD drive the charge pump. A schematic of the charge pump and loop filter is shown in Figure 3.23[42]. In order to alleviate the problem of transistor charge injection and clock feedthrough, M_1 and M_4, rather than M_2 and M_3, operate as switches. Since switching transistors M_1 and M_4 are isolated from the output node by M_2 and M_3, the channel charge changes in the switches does not affect the output voltage level. However, in the locked state ripples may exist on the control voltage due to the mismatch between the up and down currents produced by the charge pump. This mismatch can come from the transistor size mismatch in the current mirrors,

transistor switch (M_1 and M_2) turn-on duration mismatch or low output impedance of M_3 and M_4 [42]. This low output impedance leads to additional mismatch between the up and down currents as a function of V_{ctrl}, especially when V_{ctrl} reaches a small value. The ripples on the control voltage potentially lead to large reference sidebands and spurious signals in output of the synthesizer [49]. To reduce the size of the ripple, the second capacitor (C_2) is used in the loop filter. The loop filter provides the current-to-voltage conversion from the output current of charge pump to the VCO control voltage. The effect of C_2 on the ripple and the design method of loop filter in third-order PLLs is presented in reference [50].

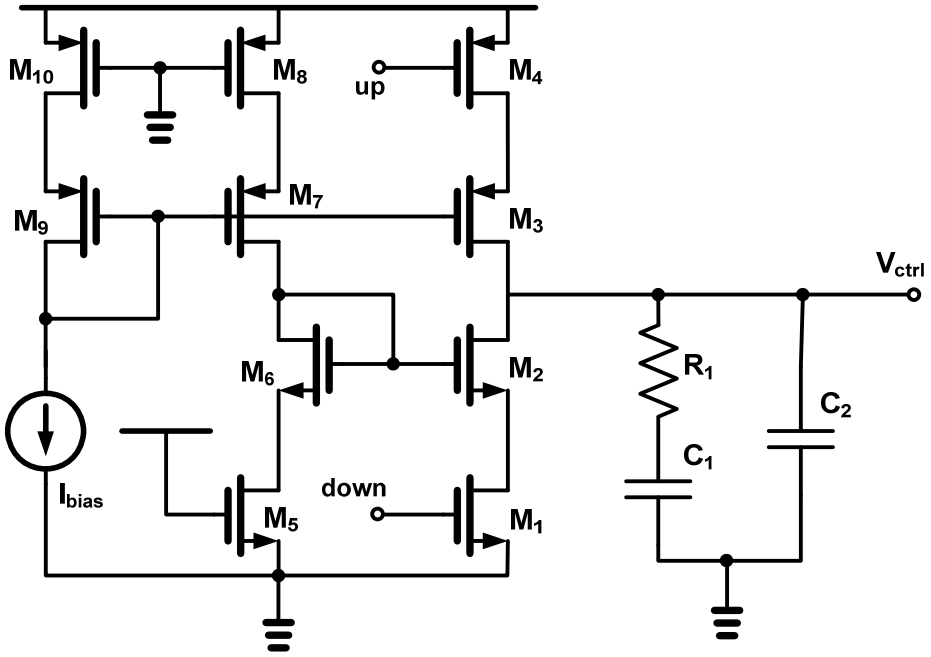


Figure 3.23: Schematic of charge pump with loop filter.

A PLL is a simple negative feedback system. A linear frequency domain or *s* domain model of the PLL is illustrated in Figure 3.24. This model consists of transfer functions of several blocks: PFD/CP, the loop filter, VCO and the divider. So the open loop transfer function of the system is [29, 49]

$$G(s) = \frac{I_{CP}}{2\pi} \cdot Z_f(s) \cdot \frac{2\pi \cdot K_{VCO}}{s} \cdot \frac{1}{M}, \tag{3.10}$$

where $\frac{I_{CP}}{2\pi}$ is the gain of PFD/CP, $\frac{2\pi \cdot K_{VCO}}{s}$ is the gain of VCO, and $Z_f(s)$ is the transfer function of the loop filter, which is

$$Z_f(s) = \frac{1 + sR_1C_1}{s(C_1 + C_2)\left(1 + sR_1\frac{C_1C_2}{C_1 + C_2}\right)}. \tag{3.11}$$

R_1, C_1 and C_2 in the equation are the passive component values of the loop filter illustrated in Figure 3.21.

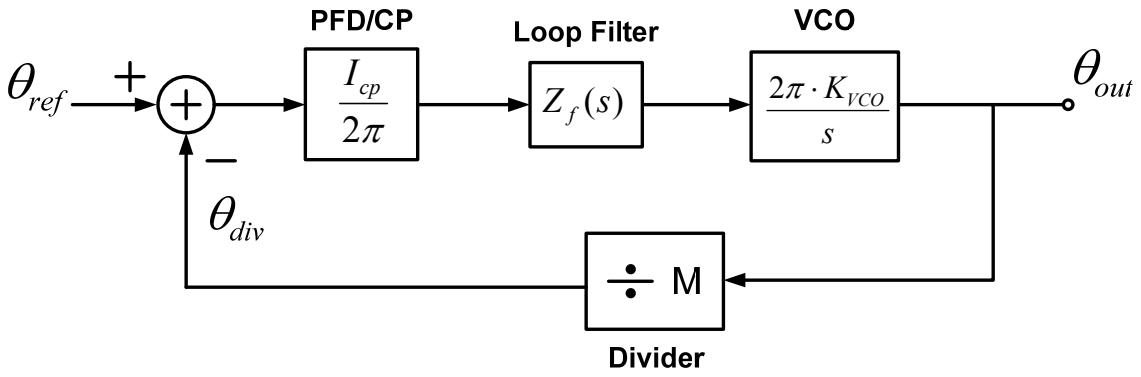


Figure 3.24: PLL linear model.

Substituting equation 3.11 into equation 3.10, we have the open loop transfer function of the system:

$$G(s) = \frac{I_{CP} \cdot K_{VCO} \cdot (1 + sR_1C_1)}{s^2M(C_1 + C_2)\left(1 + sR_1\frac{C_1C_2}{C_1 + C_2}\right)}. \tag{3.12}$$

So there are one zero $\left(s_z = -\frac{1}{R_1 C_1} \right)$ and three poles $\left(s_{p1} = s_{p2} = 0, s_{p3} = -\frac{C_1 + C_2}{R_1 C_1 C_2} \right)$. The corresponding Bode plot is shown in Figure 3.25, where ω_c is the open-loop bandwidth, or the 0 dB cross-over frequency, and φ_m is the corresponding phase margin. These two quantities depend on the positions of the zero and the third pole, which determine the stability of the PLL. This effect can be simulated with the help of PLL Design Assistant [51].

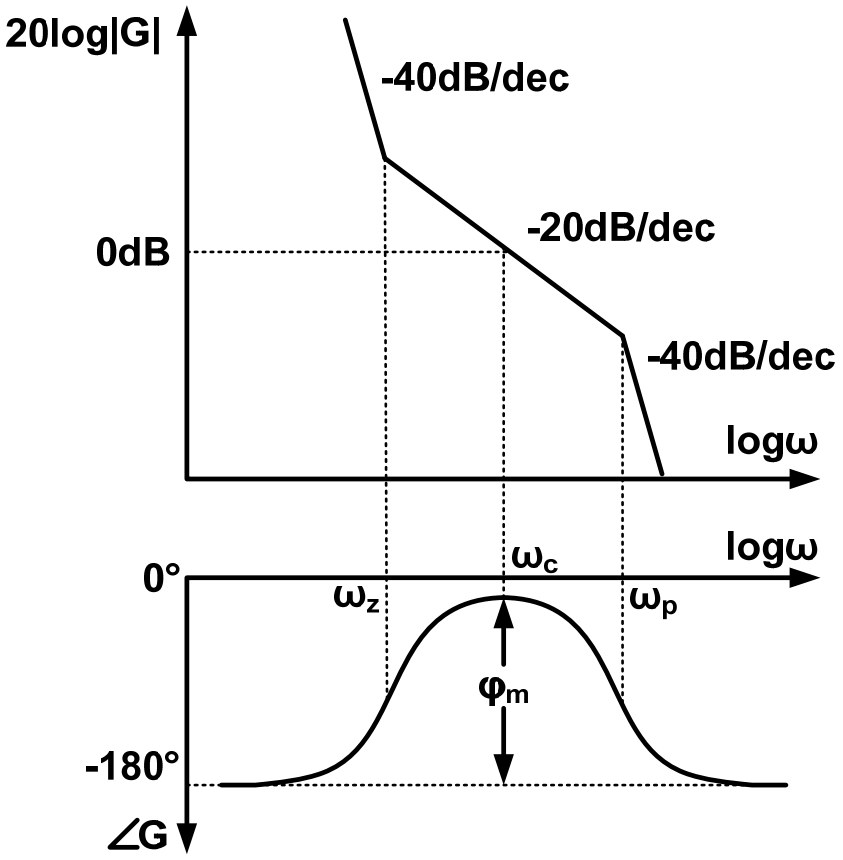


Figure 3.25: PLL Bode plot

3.5 Envelope Detector

In a super-regenerative receiver, an envelope detector is employed to measure the oscillation envelope of the VCO. The performance of the envelope detector determines the maximum signal data rate that the receiver can demodulate. Figure 3.26 shows the schematic of the envelope detector (with a power consumption of 0.12 mW). In detection mode, the super-regenerative oscillator periodically turns on and off. For this VCO, the VCO output common-mode level changes with time. To avoid this problem, a differential to signal-ended converter (the schematic is similar as the one in Figure 3.16) is used. All the N-type transistors (M_1 and M_3) in the circuit are weak inversion biased [52]. In the weak inversion mode, the drain current in transistors M_1 and M_3 is [52, 53]

$$I_D = \frac{W}{L} \cdot I_t \cdot \exp\left(\frac{V_{GS} + U \sin \omega t - V_T}{n V_T} \right) \cdot \left(1 - \exp\left(-\frac{V_{DS}}{V_T} \right) \right), \tag{3.12}$$

where W and L is the transistor channel width and length, I_t is the characteristic current, n is a slope factor, $V_T=kT/q$, and $U \sin \omega t$ represents the input sine wave with amplitude of U. So as the amplitude of the input signal (U) increases, to keep the average drain current (of M_1 and M_3) constant, the gate voltages (V_{GS}) of transistor M_1 and M_3 decrease, and the drain voltages (V_{DS}) increase correspondingly. RC filters (R_2, C_3, and R_4, C_6) remove the AC component of the input signal. Hence the output voltage V_{outp} follows the input signal amplitude level. A replica circuit (on the right) is used to generate a pseudo-differential signal envelope. Simulation results show that the detector can follow an input signal with a data rate up to 10 Mb/s at 5 GHz.

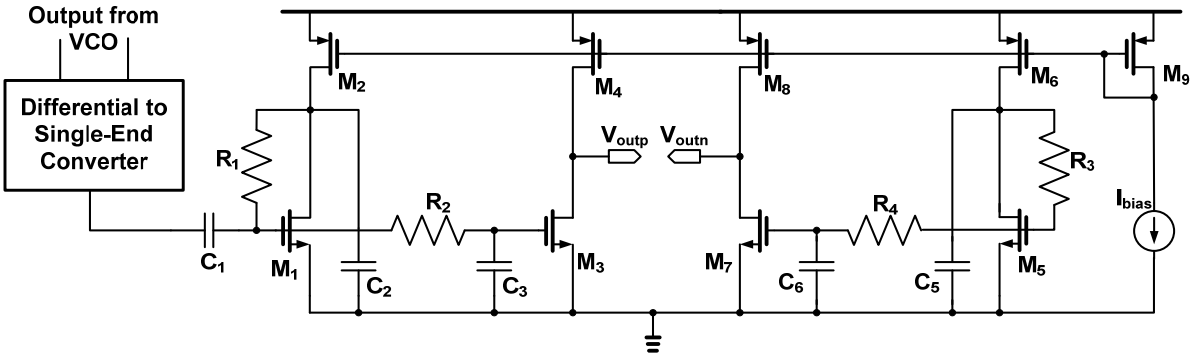


Figure 3.26: Schematic of the envelope detector**.**

3.6 Synchronizer

This super-regenerative receiver employs a synchronizer to synchronize the received data clock with the transmitter. The synchronizer, shown in Figure 3.27, works as an all-digital PLL, where the divide ratio changes depending on early/late detection logic. The demodulated data from the super-regenerative VCO (output of the envelope detection comparator) feeds two sets of flip-flops D1, D2 and D3, D4, where D2, D3, D4 are triggered by CLK (half of *clk_sync* frequency) and D1 is triggered by $\overline{CLK}$ [54]. *a*, *b, c* represent consecutive data samples with *a* and *b* coming from one super-regeneration detection period and *c* coming from the next. If correctly synchronized, *a* and *c* should sample at the center of the data eye. The detection logic decides if the sampling clock is correct depending on the values of *a*, *b* and *c*, and controls the divide ratio of the multi-mode divider (10, 12 or 14). The sampling position moves up (divide ratio = 10), down (divide ratio = 14) or does not change (divide ratio = 12), depending on the result from the early/late detection logic.

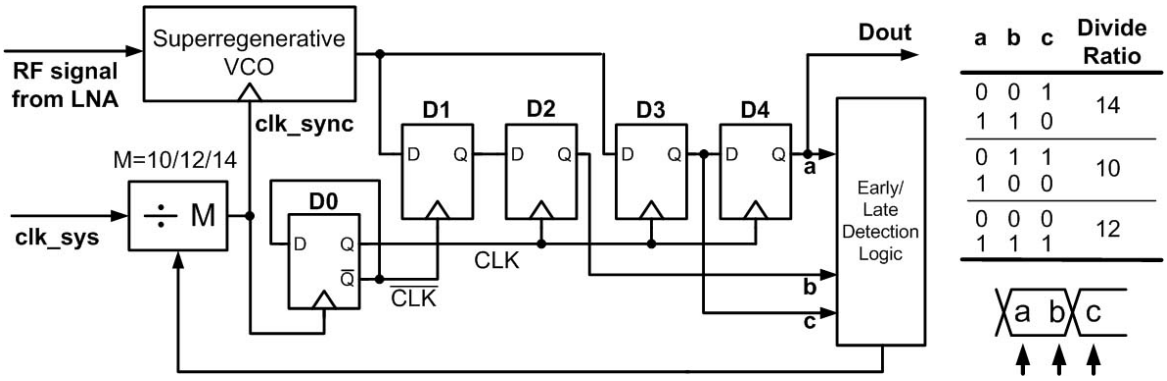


Figure 3.27: Block diagram of the all digital multi-mode divider based synchronizer.

Examples for three different sampling positions are shown in Figure 3.28. The received data is over-sampled. There are two sampling positions (*a* and *b,* data at *a* is used for the synchronizer) in each data eye. In case a, sampled data at position *a* and *b* are always equal, so the sampling position is too early. In case b, sampled data at position *a* and *b* are always opposite near data transition point, so the sampling position is too late. In case c, sampling position is at the center of the data eye, which is the ideal case.

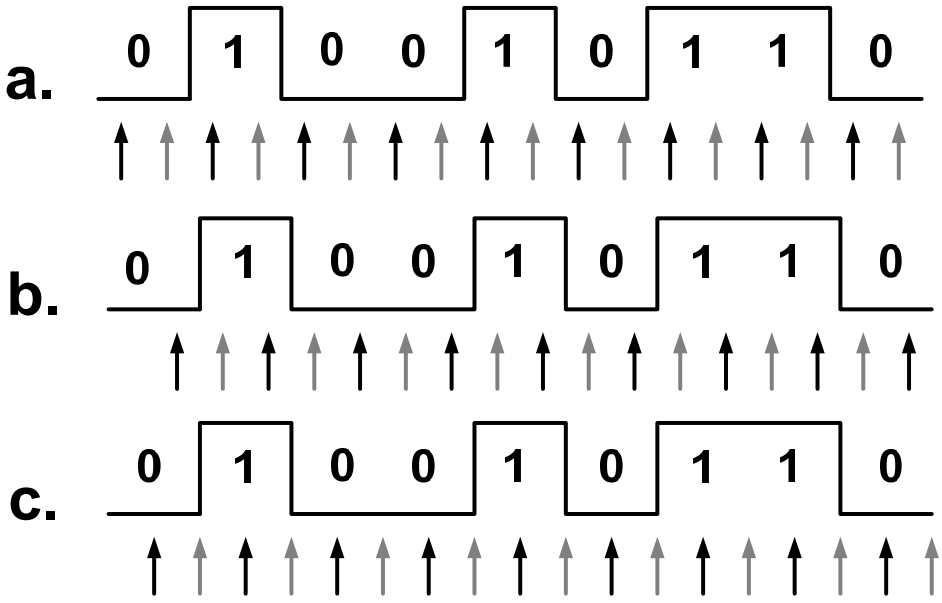


Figure 3.28: Examples of received data stream and different sampling positions (black arrows corresponds to position *a*, grey arrows correspond to position *b*).

In this chapter, the design methodologies used in several circuit blocks are presented. Prototypes of the building blocks are presented in the next chapter.. The test setup and experimental results are also described.

CHAPTER IV

BUILDING BLOCK PROTOTYPES AND TEST RESULTS

The previous chapter discusses design methodologies for some building blocks in the CMOS receiver. To put these methodologies into practice, we have implemented prototypes of several critical building blocks: a 5 GHz VCO with standing wave resonator, a 9 GHz on-chip slot antenna with LNA, a 5 GHz on-chip slot antenna and a 5 GHz on-chip resonator-based filter. In this chapter, we explore the implementation and testing of each building block.

4.1 A 5GHz VCO with Standing-Wave Resonator

Based on the methodology described in section 3.1, a 5 GHz standing wave resonator is designed, and employed in the VCO prototype (Figure 3.7). The prototype is fabricated in an 8-level-metal 0.13 μm CMOS process with a 4 μm thick top aluminum layer. A die micrograph is shown in Figure 4.1. The VCO occupies 0.11 mm^2 and the total die area including pads is 0.29 mm^2.

A PCB board, which provides the bias voltage and tunable bias current for the VCO, is designed for testing. The IC is wire-bonded onto the board. Figure 4.2 illustrates the setup on the probe station. A GSG probe is used to detect the VCO oscillation. The detected signal then is collected using a spectrum analyzer (Agilent E4405B). The whole testing setup is shown in Figure 4.3. Two bias tees provide the DC bias for the output buffer which is 50 Ω matched to the instrument. The spectrum analyzer is employed to measure the oscillator spectrum and phase noise performance of the VCO.

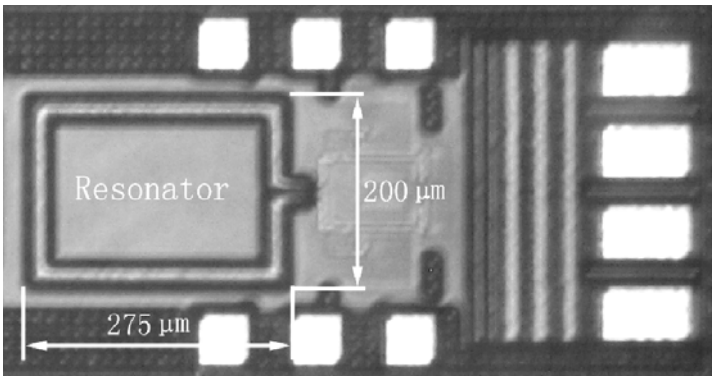


Figure 4.1: VCO die micrograph.

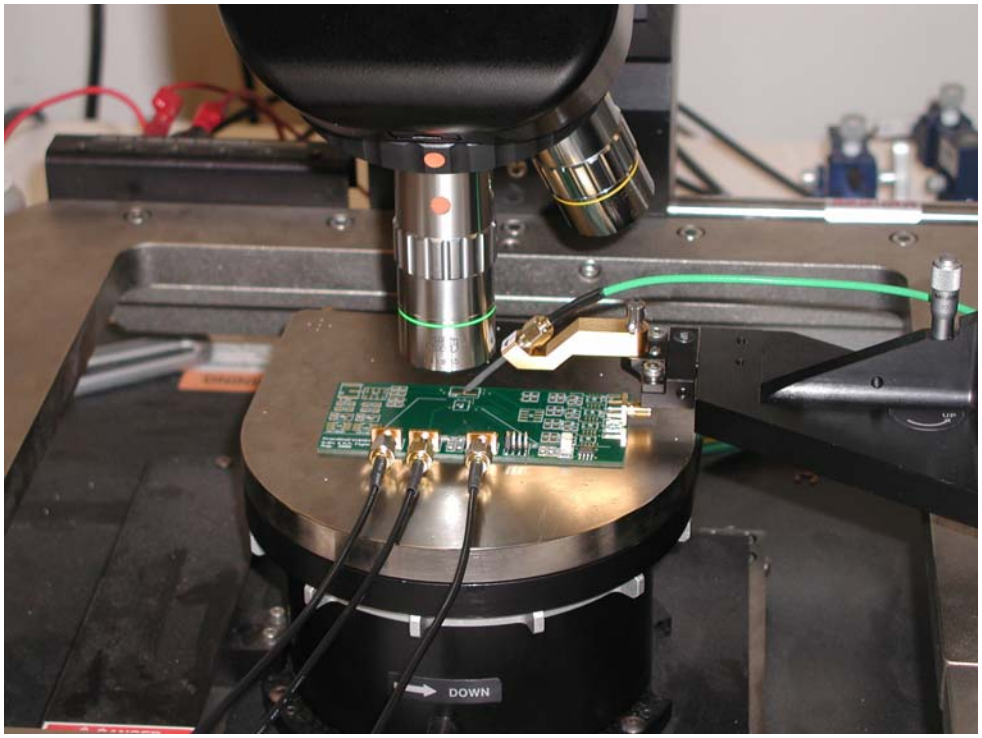


Figure 4.2: The IC is wirebonded to a custom PCB. The PCB supplies DC bias to the IC. A GSG probe is used to probe the output of the oscillator. A bias-tee provides bias to the output buffer.

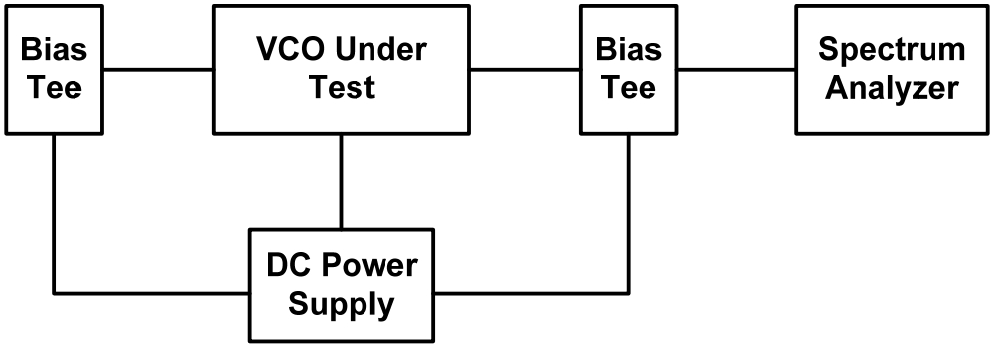


Figure 4.3: VCO measurement setup.

Figure 4.4 shows the measured phase noise performance of the oscillator. A phase noise of -117 dBc/Hz at a 1MHz offset is achieved. Over a 10% tuning range the phase noise at a 1 MHz offset is less than -106 dBc/Hz. Figure 4.5 illustrates the oscillation frequency and output power level over the whole tuning range. The VCO core draws 2.5 mA from a 1.2 V supply. The performance of the VCO is summarized in Table 4.1. To compare the performance of our design with other published work, the figure of merit[55]:

$$FOM = L(f_0) + 10 \cdot \log\left(\frac{P_{DC}}{1mW}\right) - 20 \cdot \log\left(\frac{f_0}{f_{offset}}\right), \tag{4.1}$$

is used. This prototype is compared with other recently published VCOs that operate in the 5 GHz frequency range in Table 4.2. In summary, this prototype on-chip resonator based outperforms most recently published CMOS VCOs in terms of phase noise, tuning range and die area.

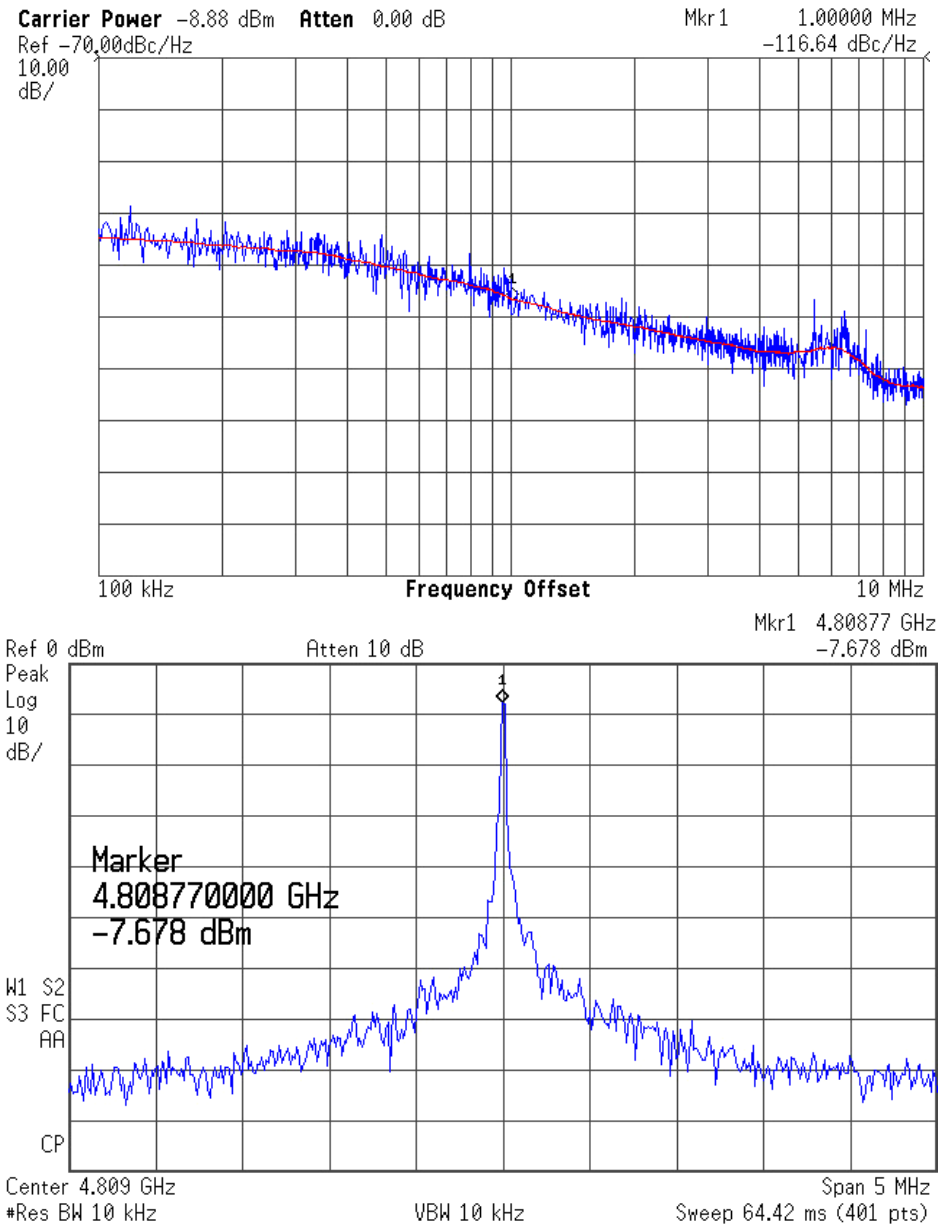


Figure 4.4: Measured phase noise and output spectrum of the VCO.

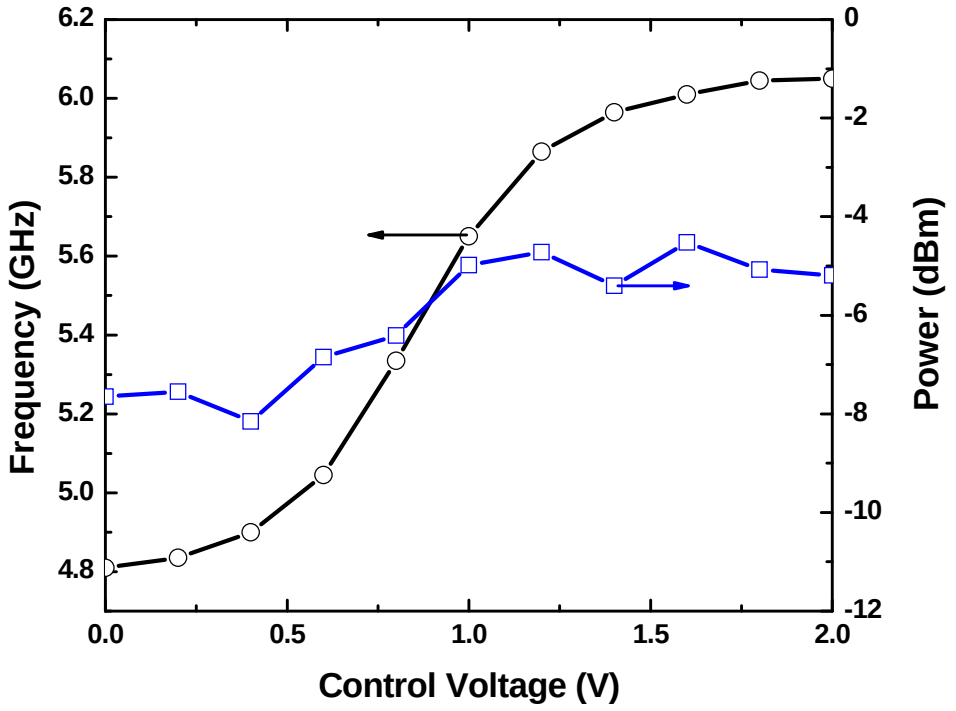


Figure 4.5: Measured oscillation frequency and output power versus control voltage.

Table 4.1 VCO performance summary

Phase Noise	-117 dBc/Hz at a 1 MHz offset
Figure of Merit	-186 dBc/Hz
Operating Frequency	4.81 GHz
Frequency Tuning Range	22%
Supply Voltage	1.2 V
Power Consumption	3 mW
Die Area	0.11 mm^2

Table 4.2: VCO FOM Comparison.

Reference	Technology	f_0 (GHz)	Power Supply (V)	P_{DC} (mW)	PN (dBc/Hz at 1MHz)	Die area (mm^2)	Tuning (%)	FOM (dBc/Hz)
This work	CMOS 0.13 µm	4.81	1.1 to 1.3	3	-117	0.11	22	-186
[56]	BiCMOS SiGe 0.18 µm	5.67	1.5	2.4	-119	0.49	15	-191
[55]	BiCMOS SiGe 0.35 µm	5.6	2.7	13.5	-117	0.20	10	-180
[57]	CMOS 0.18 µm	5.5	1.8	3.6	-115	0.84	20	-184

4.2 Prototype On-chip Slot Antenna[3]

To test the design methodology described in section 3.2, a 9 GHz on-chip antenna with LNA is first designed. The on-chip antenna and its integrated LNA are fabricated in a 0.13 μm RF CMOS process. Figure 4.6 shows a photomicrograph of the prototype I.C., including the 9 GHz miniaturized antenna and the LNA. The IC is die-bonded to a custom PCB which supplies power and DC bias. In order to assess the performance of the antenna, the measurement setup shown in Figure 4.7 is used. A reference horn antenna operating at X-band is mounted on a rotating robotic arm. Both the antenna and LNA outputs are probed with high frequency GSG probes. A Vector Network Analyzer (VNA) is used to feed the horn antenna and the power received from the on-chip antenna is measured using a spectrum analyzer, as shown in Figure 4.7. The distance between the reference horn antenna and the robotic arm is such that the two antennas are in the far fields of one another. The antenna, without the LNA, has a measured gain of -10dBi at 9 GHz. The directivity of this electrically small antenna is almost identical to the directivity of an electrically small dipole (Hertzian dipole) antenna, which is about 1.76 dBi. Therefore, using the relationship, η = Gain/Directivity, the radiation efficiency of this antenna is measured to be 9%. The LNA is designed to provide its maximum gain of 10 dB at 9.5 GHz. The maximum gain of the antenna-LNA combination is measured to be -4.4dBi. The measured gain of the active antenna and the antenna without LNA are both shown in Fig. 4.8. As is seen, the active antenna shows a higher measured gain in the 9-10 GHz frequency band of operation.

[3] This part is done with the collaboration with Nader Behdad,Wonbin Hong and Kamal Sarabandi from The University of Michigan Radiation Lab.

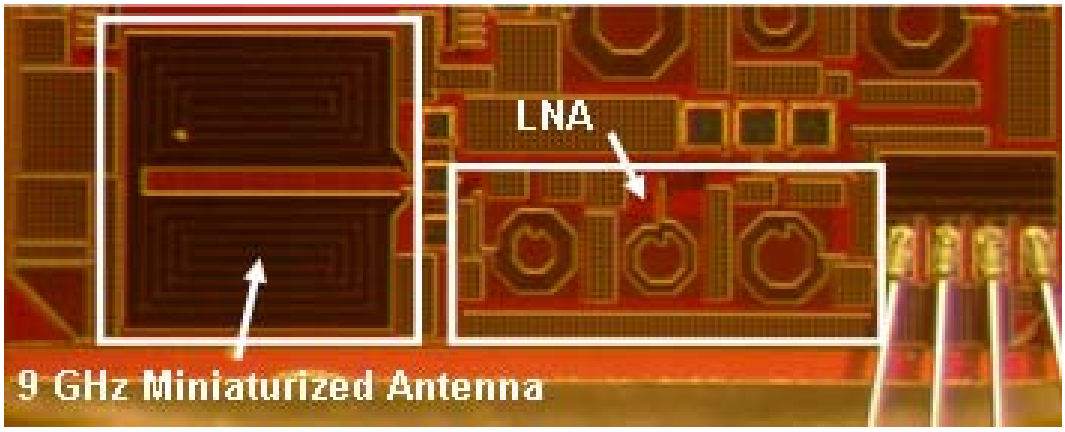


Figure 4.6: Microphotograph of the 9GHz on-chip antenna and the integrated LNA.

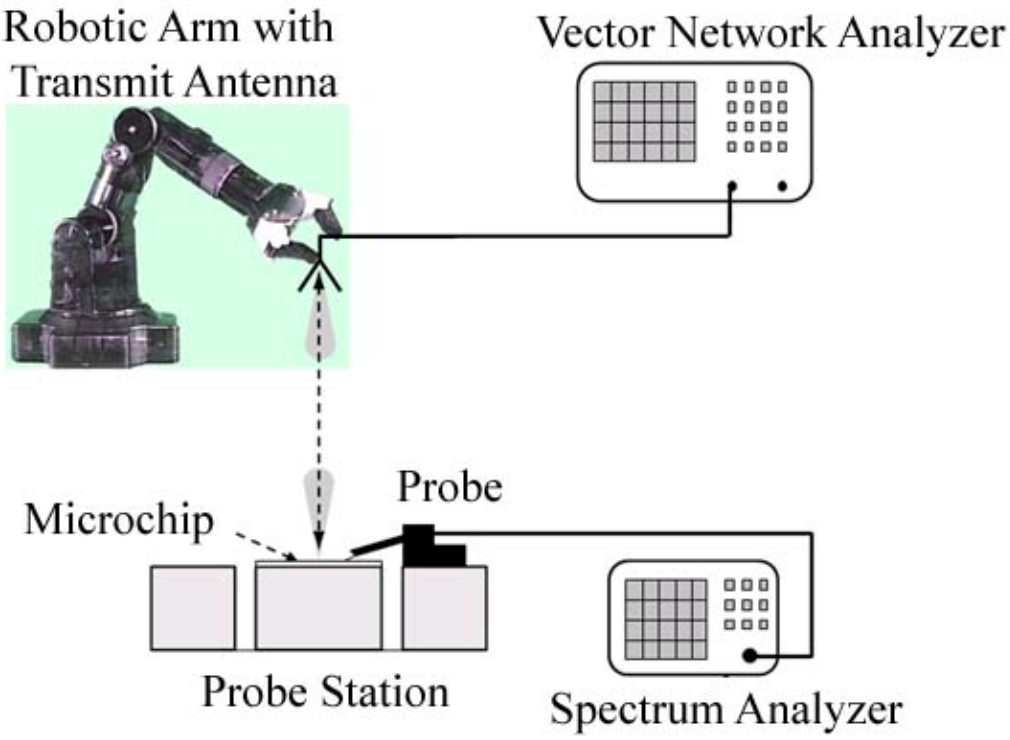


Figure 4.7: On-wafer measurement setup of the on-chip slot antenna.

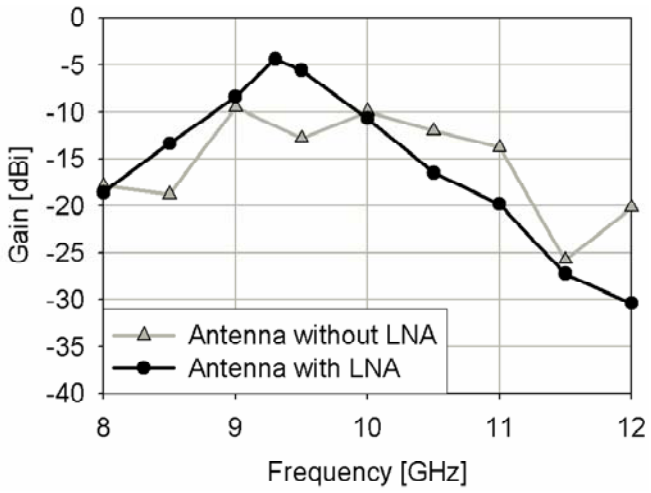


Figure 4.8: Measured gain of the 9GHz on-chip antenna with and without LNA (figure courtesy of our collaborator, Nader Behdad [34]).

Since the 9 GHz on-chip antenna has good performance, another 5 GHz on-chip antenna is designed and fabricated using the same technology. This 5 GHz on-chip antenna is designed for the 5 GHz super-regenerative receiver. The on-chip 5 GHz antenna occupies a die area of only 0.47 mm^2 (Figure 4.9). The electrical dimensions of the antenna are $0.010\lambda_0 \times 0.011\lambda_0$, making it 50 times smaller than traditional dipole antennas operating in the same frequency band. The setup in Figure 4.7 is used to measure the gain of the antenna, which is approximately -17.0 dBi at 5 GHz as shown in Figure 4.10.

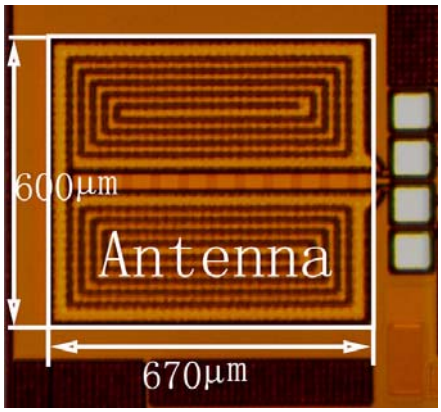


Figure 4.9: Microphotograph of the 5GHz on-chip antenna.

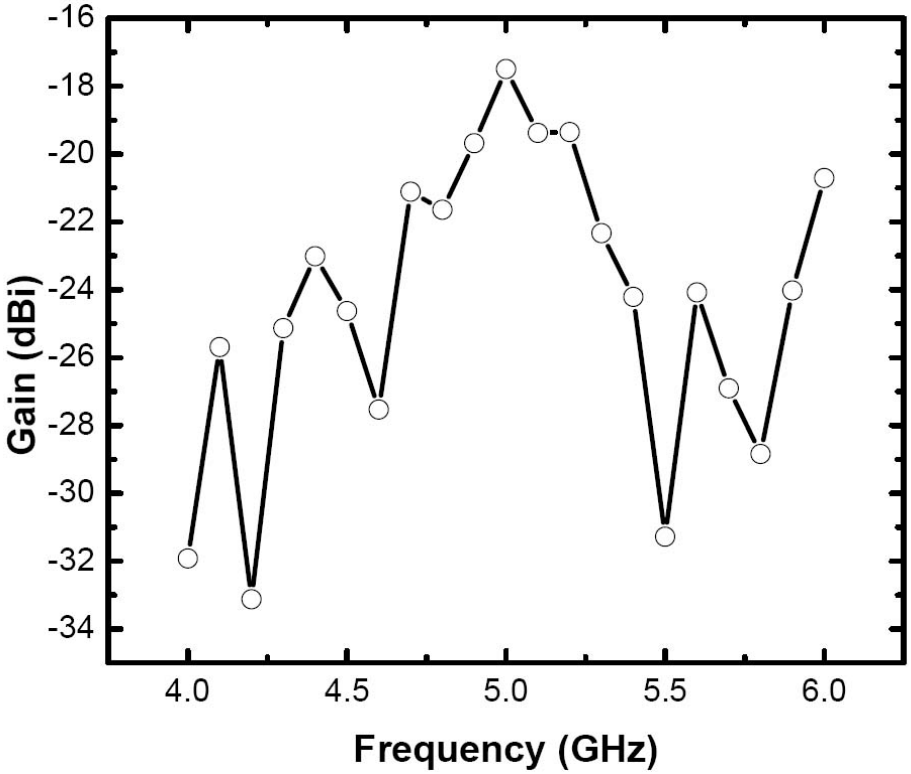


Figure 4.10: Measured gain of the 5GHz on-chip antenna versus frequency[4].

To compare the performance of the current on-chip antenna with other state-of-the-art on-chip antennas reported in literature, one must keep in mind that a fair comparison is only possible when the frequency of operation and the maximum linear dimensions of the antennas are identical. For a fixed frequency, as the maximum linear dimension decreases, the gain of the antenna also decreases [58, 59]. Nevertheless, we attempt to make a fair comparison between the current design and those presented in [30] and [31]. To do this, we use the associated gain definition, defined in [31] and used in [30, 31] to extract the actual gain of the on-chip antennas presented in [30, 31]. In doing so, we also consider the effect of mismatches between the antenna input impedance and

[4] This measurement is done with the collaboration with Nader Behdad, Wonbin Hong and Kamal Sarabandi from The University of Michigan Radiation Lab.

the feeding source, since these effects have real implications in the performance of the antenna. This comparison is performed in Table 4.3. As indicated by Chu, reducing the maximum linear dimension of any antenna significantly reduces its gain and radiation efficiency [58]. However, in spite of the smaller linear dimension of the on-chip antenna presented in this work, it demonstrates a much higher measured radiation efficiency and higher gain compared to those of the antennas presented in [30, 31]. This can be attributed to the effective shielding of the antenna from the lossy silicon substrate, as well as the use of a slot topology instead of a wire-based approach such as the dipoles used in [30, 31].

Table 4.3: Comparison between the current work and other reported on-chip antennas.

Antenna Type	Gain [dBi]	f_r [GHz]	Max. Linear Dimension
9 GHz Prototype	-10.0	9.0	780 μm
5 GHz Prototype	-17.0	5.0	900 μm
Dipole Ant. [30]	-31.2	7.4	2000 μm
Zig Zag Ant. [31]	-17.0	15.0	2000 μm

In this chapter, the test results of several circuit block prototypes are discussed. In the following chapter, we will present the final implementation of the fully integrated receiver. As we will show the receiver outperform super-regenerative receivers reported in term of integration level.

CHAPTER V

AN EXPERIMENTAL CMOS RECEIVER

In the previous chapter we present the prototypes of several critical building blocks in the super-regenerative receiver. Based on these we have implemented a complete super-regenerative CMOS receiver that comprises the 5 GHz on-chip slot antenna, the 5 GHz VCO with on-chip standing wave resonator, the on-chip phase-locked loop, and the synchronizer.

The entire signal path of the receiver is differential, and careful attention is paid to the symmetry over the whole layout. To reduce the substrate noise coupling, guard rings are placed around critical analog blocks. Several test points (on-chip output pads) are located along the signal path on the die for measuring intermediate signals. The super-regenerative receiver prototype is fabricated in an 8-level-metal 0.13 μm RF CMOS process. A die micrograph is shown in Figure 5.1. The receiver including the on-chip antenna occupies 2.4 mm^2 and the total die area including pads is $4mm^2$. This device is packaged in a LCC 84 package and mounted onto the test PCB, which is illustrated in Figure 5.2. Three versions of the board are designed: one with LCC84 package directly mounted, one with LCC85 socket mounted for easy test of different test chips, the other with an IC directly wire-bonded. All these boards provide DC bias voltages, reference current, comparator reference voltages to IC, and they also set the initial states of the receiver (e.g. external digital control of the VCO bias current DAC and frequency channel number).

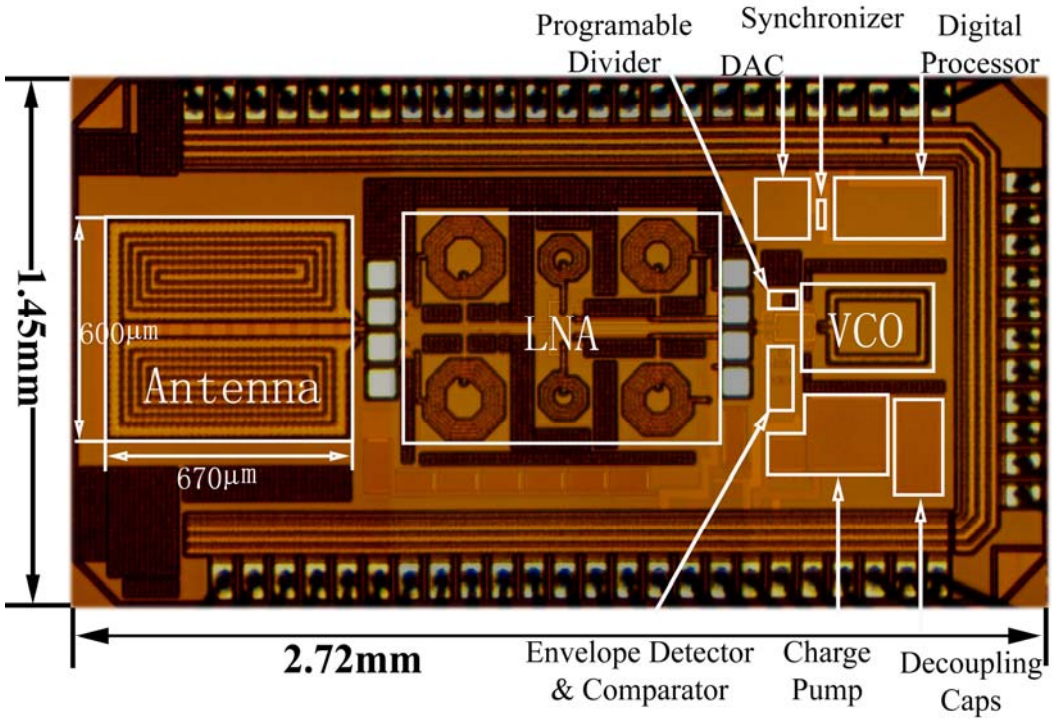


Figure 5.1: Receiver die micrograph.

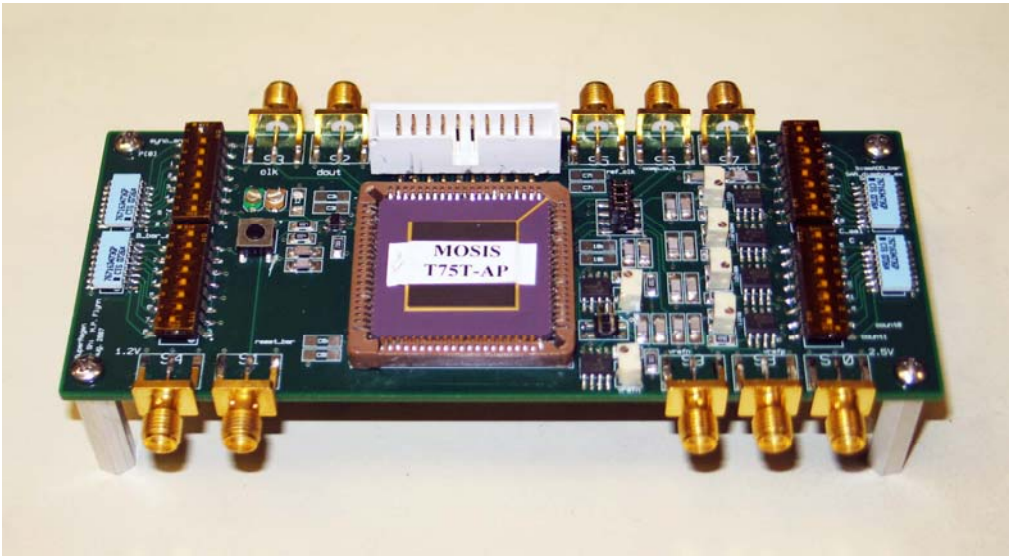


Figure 5.2: Photograph of the receiver test PCB..

A block diagram of the test setup is shown in Figure 5.3. Three function generators (Agilent 33250A, Agilent 33120A, etc.) generate the system clock (value depending on the received data rate), the reference clock (around 10.6 MHz), and the system reset signal, respectively. The system can be reset manually by pushing an on-board reset switch or automatically by the external reset signal. A signal generator (Agilent E4437B or HP 8350B) generates the OOK modulated RF signal, using Pseudo Random Binary Signal (PRBS) data supplied from a HP 33120A pulse generator, which is externally triggered by a function generator. The output frequency of this function generator determines the transmitted signal data rate. The OOK modulated RF signal is then fed to a horn antenna, which generates the transmitted RF electromagnetic signal. This is received by the on-chip antenna in the receiver. The output digital signal from the receiver is read by a logic analyzer (Intronix 32 channel logic analyzer), and compared with the transmitted data. The setup of the complete system is shown in Figure 5.4.

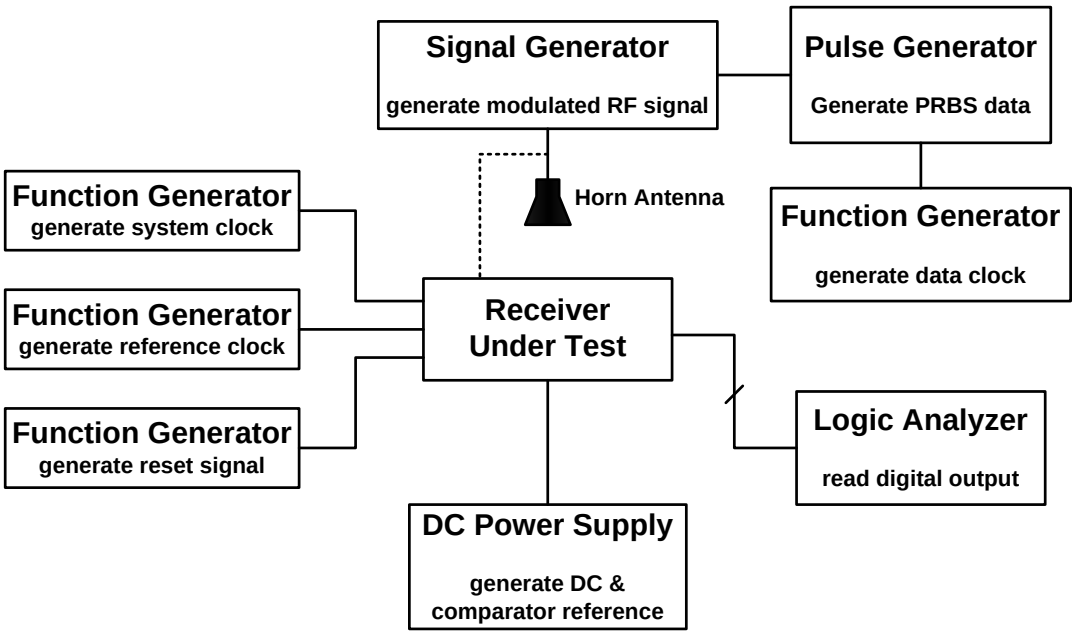


Figure 5.3: Block diagram of receiver test setup.

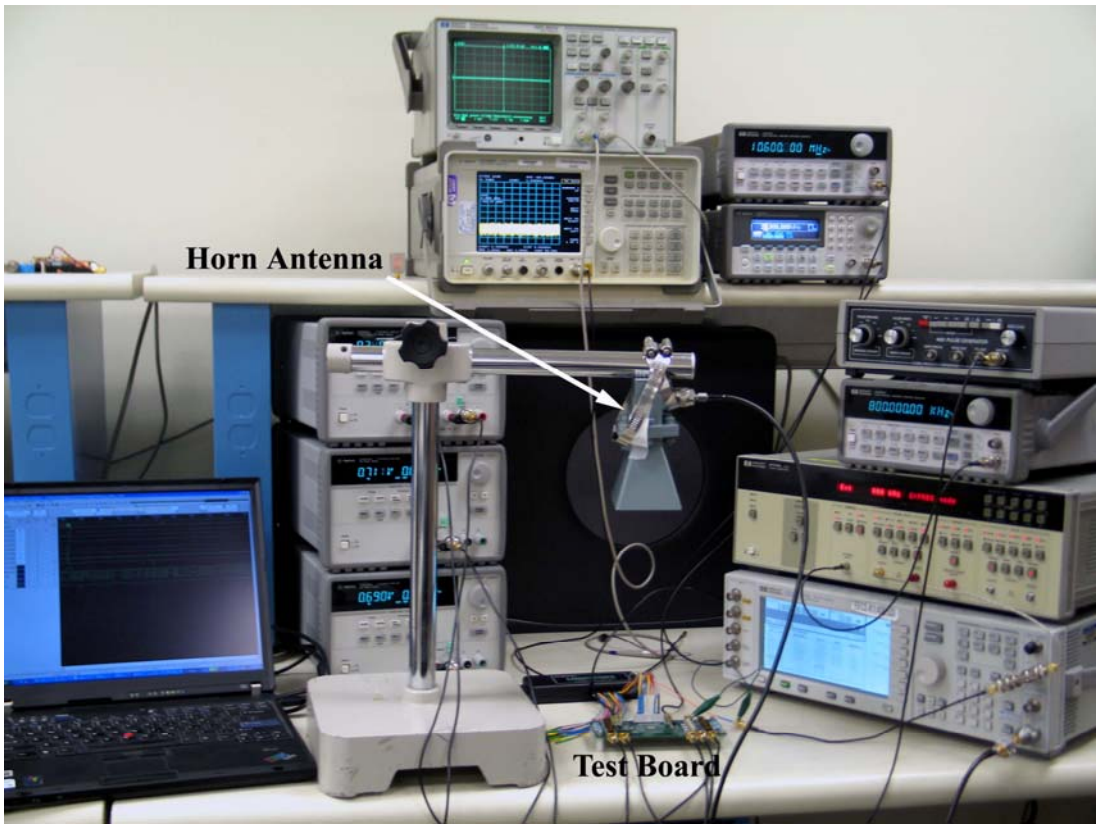


Figure 5.4: Receiver measurement setup.

To measure the Bit Error Rate (BER) and sensitivity of the receiver alone, the on-chip antenna is removed using a laser trimmer and a pseudo-random NRZ modulated signal is fed to the input of the LNA through a GSSG probe as shown in Figure 5.5. The results are shown in Figure 5.6, and a 10 dBm sensitivity improvement is observed when the synchronizer is enabled. The entire receiver draws 6.6 mW, which corresponds to 5.5 nJ per received bit at the data rate of 1.2 Mb/s. The measured results are summarized and compared with [12] in Table 5.1. The results are also compared with other super-regenerative receivers reported in Table 5.2.

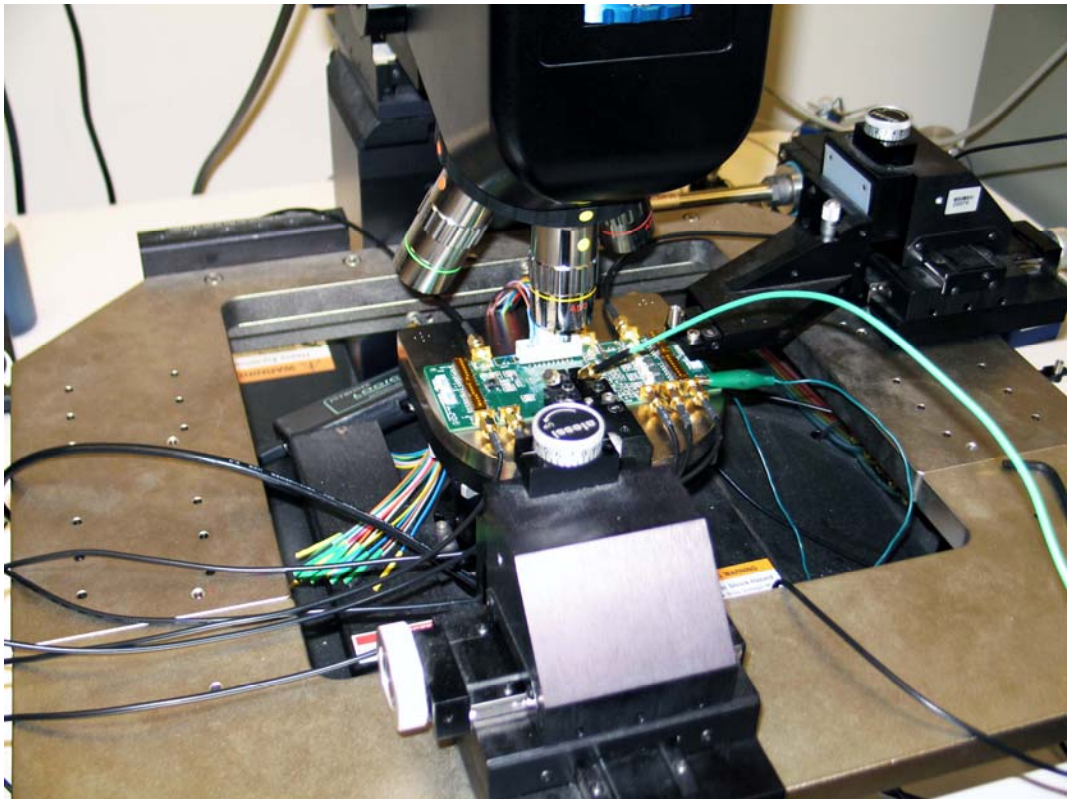
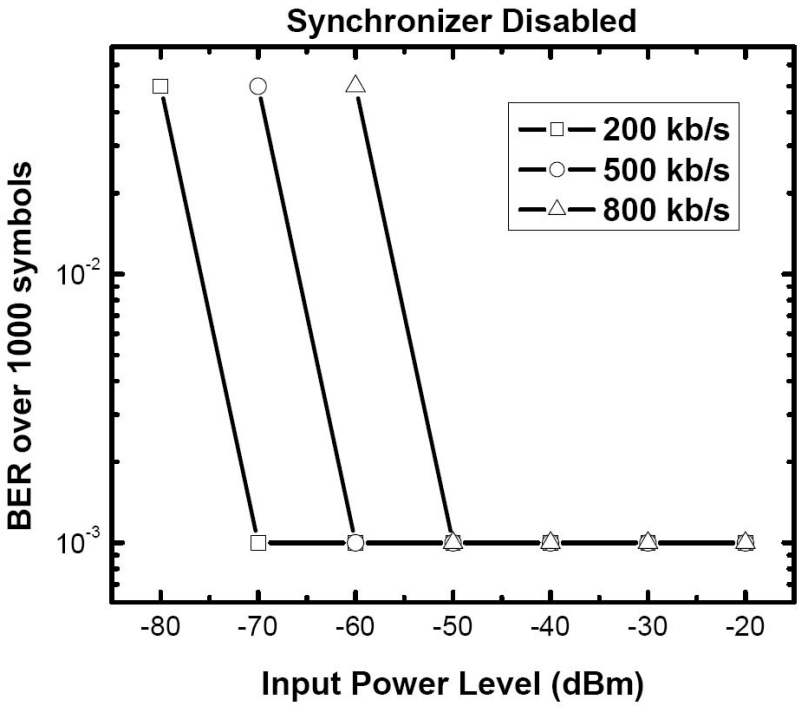
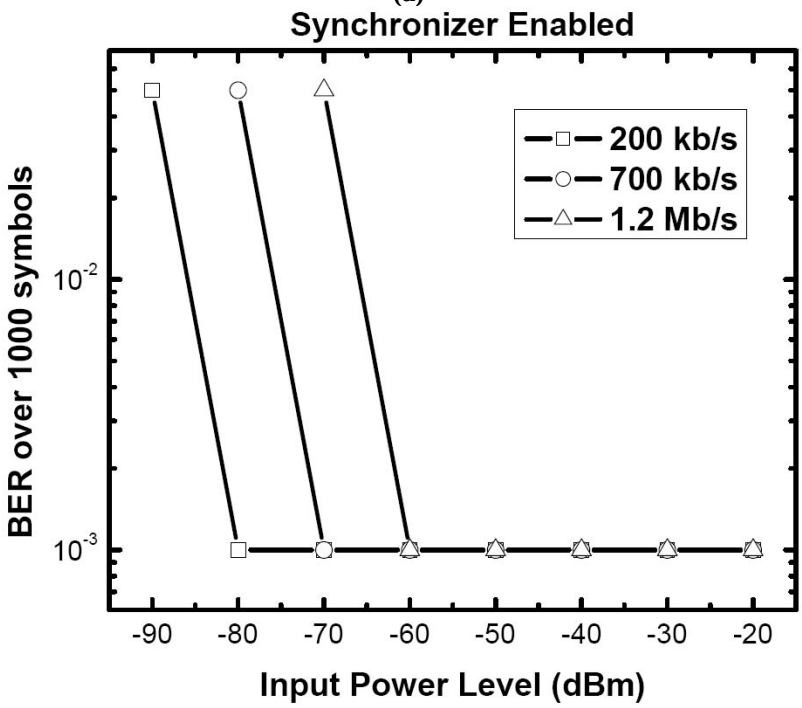


Figure 5.5: Receiver measurement setup on probe station.



(a)



(a) **(b)**

Figure 5.6: Measured receiver BER. (a) BER vs. input power level at different data rate with synchronizer disabled. (b) BER vs. input power level at different data rate with synchronizer enabled.

Table 5.1: Summary of receiver measurement results.

		This work	[12]
RF Frequency		4. 9184-5.0668 GHz	2.35-2.53 GHz
Power Consumption		6.6 mW	2.8 mW
Sensitivity		-90 dBm	-90 dBm
Adjacent Channel Rejection		30 dB	30 dB
Data Rate	**w/ on-chip antenna**	120 kb/s	-
	w/o on-chip antenna	200 kb/s to 1.2 Mb/s	500 kb/s
BER		≤0.1%	≤0.1%
Channel Number		8	9
Energy per received bit		5.5 nJ @ 1.2 Mb/s, 55 nJ@120 kb/s	5.6 nJ@500 kb/s
Synchronization		On chip (digital PLL)	Manual
On-chip Antenna		Yes	No
Tank Q		35	~15
Die Area		2.4 mm^2 inc. antenna	1 mm^2
Technology		0.13 μm CMOS	0.13 μm CMOS

Table 5.2: Comparison of super-regenerative receivers.

	Vouilloz [11]	Otis [18]	Moncunill-Geniz [16]	This work
Operating Frequency	1 GHz	1.9 GHz	2.4 GHz	5 GHz
Sensitivity	-107.5 dBm	-100.5 dBm	-90 dBm	-90 dBm
Data rate	100 kbps	5 kbps	115.2 kbps	200 kb/s to 1.2 Mb/s
BER	0.1%	0.1%	0.1%	0.1%
Power Consumption	1.2 mW	400 µW	2.7 mW	6.6 mW
Energy per bit	12 nJ/bit	80 nJ/bit	23 nJ/bit	5.5 nJ/bit
Quench signal	External analog sawtooth	External digital square	External analog sinusoidal	Internal digital
Tank	Discrete inductor	BAW resonator	Microstrip line	On-chip Resonator
On-chip antenna	No	No	No	Yes
Technology	0.35 µm CMOS	CMOS	Discrete BJT	0.13 µm CMOS

Six on-chip inductors are used in the LNA of the receiver. These occupy large die area, similar to the area of the on-chip antenna, as shown in Figure 5.1. And they can also pick up the electromagnetic signal transmitted by the horn antenna, interfering with the wanted signal received by the on-chip antenna. This can seriously deteriorate the performance of the receiver. To overcome these problems, an inductorless differential LNA discussed in section 3.3.2 is employed to replace the inductor LNA. The layout of the whole receiver is shown in Figure 5.7. Simulation results show that it has similar power consumption to the first prototype receiver, but smaller die area: the receiver including the on-chip antenna occupies 1.4 mm^2 and the total die area including pads is 3 mm^2.

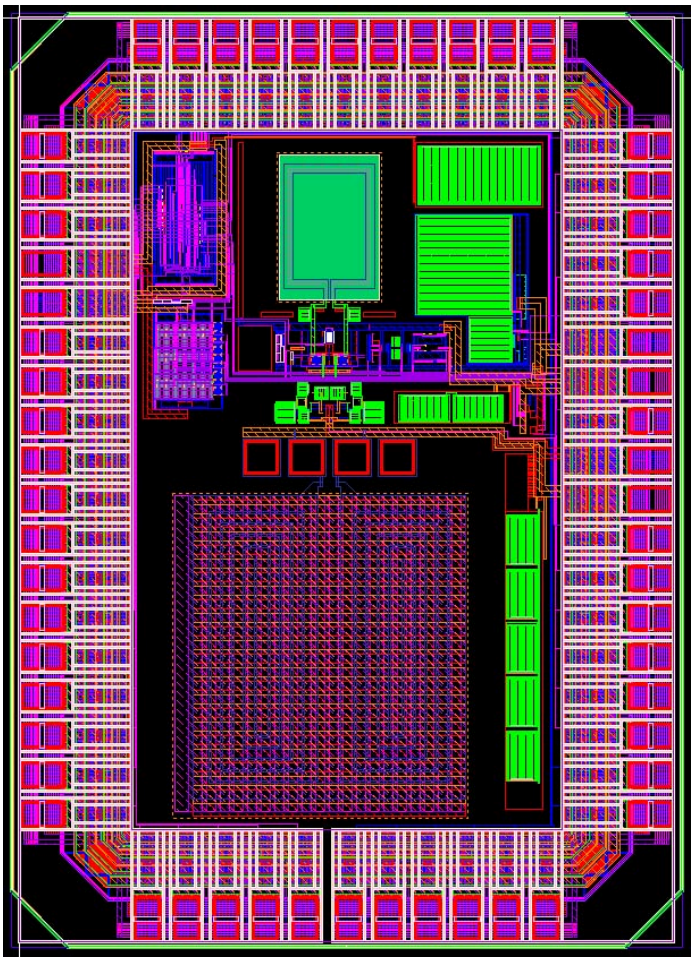


Figure 5.7: Layout of the second prototype receiver.

CHAPTER VI

CONCLUSION

In this project we have developed a fully integrated CMOS receiver for applications such as wireless sensor networks, wireless system implantable neuroprosthetic devices, RFID, etc. In this receiver, a 5 GHz on-chip resonator and a 5 GHz on-chip slot antenna are integrated into a single chip. An all-digital PLL synchronizes the received data clock with the transmitter. The prototype 5GHz receiver, implemented in 0.13 μm CMOS, achieves a highest data rate of 1.2 Mb/s, dissipates 6.6 mW from a 1.5 V supply, and occupies a die area of 2.4 mm^2. A summary of conclusions and contributions of this work is as follows:

- The phase noise of integrated oscillators is limited by the low quality factor of on-chip inductor. In this receiver, a novel on-chip capacitively-loaded, transmission-line-standing-wave resonator is employed to replace on-chip inductors. The simulated resonator quality factor is 35, which is verified by the phase noise measurements of a prototype VCO incorporating this resonator. Some theory is derived to explain the higher quality factor of the on-chip resonator. A methodology is developed for the design of this on-chip resonator.
- A novel on-chip capacitively-loaded, transmission-line-standing-wave resonator is employed in a low phase noise 5 GHz VCO, to achieve a measured phase noise of -117 dBc/Hz at a 1 MHz offset. The prototype 5 GHz VCO, implemented in 0.13 μm CMOS, dissipates 3 mW from a 1.2 V supply, and occupies a compact die area of 0.11 mm^2. The VCO achieves a FOM of -186 dBc/Hz, and

outperforms most recently published CMOS VCOs in terms of phase noise, tuning range and die area.

- In this project, an on-chip antenna is designed in collaboration with Nader Behdad and integrated into the receiver. An efficient shielding technique is used to shield the antenna from the low-resistivity substrate underneath it. Two on-chip slot antenna prototypes are designed and fabricated. The 9 GHz prototype occupies a die area of only 0.3 mm^2, and is fabricated in a standard 0.13 μm RF CMOS process. The measurement results indicate that the antenna shows an active gain of -4.4 dBi and an efficiency of 9% in spite of its close proximity to the lossy silicon substrate. A second prototype, operating at 5 GHz, is fabricated in the same process. This antenna occupies a die area of 0.47 mm^2, achieves a passive gain of approximately -17.0 dBi at 5 GHz. The second prototype is integrated into the final design of the receiver.
- A new type of envelop detector is employed in this receiver. In this envelop detector, transistors biased in weak inversion mode are used to follow the change in the input oscillation signal amplitude. Simulation results show that the detector can detect RF signals with data rates up to 10 Mb/s at 5 GHz with ultra low power consumption, and achieves higher efficiency.
- Unlike other reported super-regenerative receivers, this receiver includes a synchronizer. The synchronizer, implemented with an all-digital PLL, synchronizes the received data clock with the transmitter. Early/late detection logic is used in the synchronizer to change the sampling position. The measurement results show that 10 dBm sensitivity improvement is observed when the synchronizer is enabled.
- Unlike all previous designs, using off-chip components or low-quality on-chip inductors, the proposed CMOS receiver is fully integrated with on-chip resonator and on-chip slot antenna.

- The receiver works at 5 GHz with 8 tunable channels. The frequency is higher than previous designs. The higher operating frequency enables the integration of on-chip antenna, or other microwave components in the future. This also enhances the maximum detectable RF signal data rate.
- A new version of the super-regenerative receiver utilizing an inductorless LNA is designed. The inductorless LNA eliminates the problem of electromagnetic signal interference by on-chip inductors in LNA, and greatly shrinks the system die area. The simulation results show similar power consumption in the second prototype.

There are several issues that await exploration in future research studies. Here we present several new ideas which may improve the performance of the receiver.

First, the on-chip resonator can be improved. Figure 6.1 illustrates a new transmission-line resonator suggested by G.Taylor [60]. Instead of a single shield at the bottom of the transmission line as in Figure 3.6a, the sides of the transmission line are also shielded. This forms a semi-open coaxial cable structure, which should provide better shielding from the lossy substrate. The shielding metal on the sides loads the transmission line and also provides loading capacitors to the resonator. Therefore this resonator should provide an even higher quality factor than the current design. The only practical obstacle in this design is the EM simulator handling capability, since the current design already reaches the highest memory capacity the EM simulator can simulate. To overcome this problem, one segment of the whole structure can be simulated at one time, and then all the simulation results can be combined together. Alternatively an EM simulator with a large memory capacity can be used in the future.

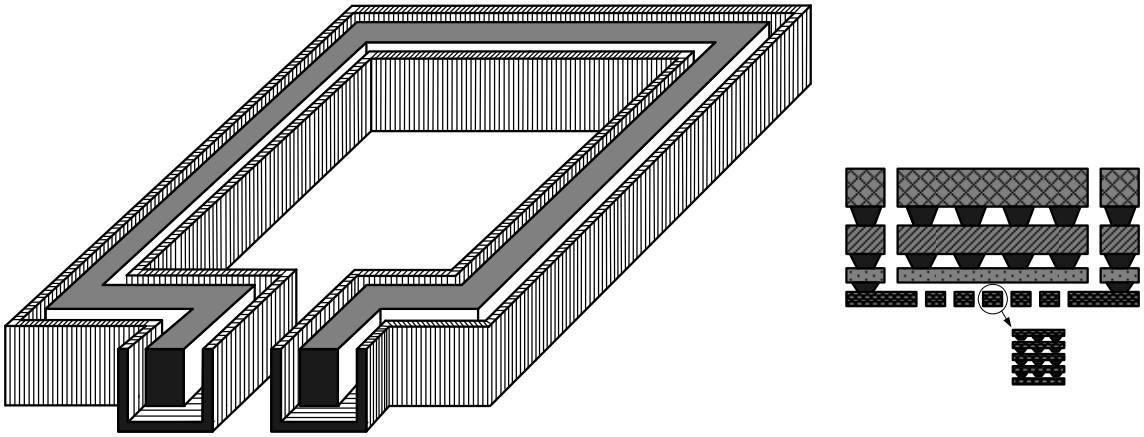


Figure 6.1: New transmission-line resonator.

In the envelope detector (Figure 3.26), a differential-to-single-ended converter is used to overcome the output common-mode level change problem of the super-regenerative oscillator as the oscillator turns on and off periodically in detection mode. A new VCO can be employed to eliminate this problem. Figure 6.2 is the schematic of the VCO, where the same resonator is used. But the center of the transmission-line resonator is connected to V_{DD}. In this way the output oscillation is always around V_{DD}, and there is no common-mode change problem. On the other hand, a center-AC-ground will improve the resonator performance and provides an even higher quality factor. When the resonator is driven differentially, voltages on the left and the right transmission-line strips are always in opposite phase, and the center point always has the minimum voltage swing (ideally zero).

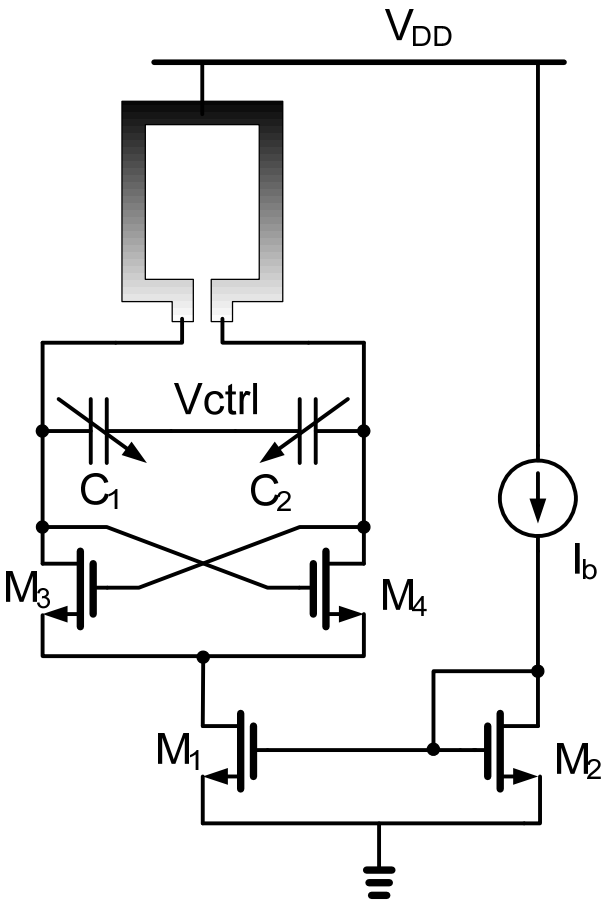


Figure 6.2: Schematic of the new oscillator.

Finally, a fully integrated transceiver can be designed by integrating a transmitter with the receiver. Figure 6.3 shows the block diagram of the system. The on-chip antenna is reused and an RF duplexer is employed to switch between the transmitting mode and receiving mode. At 5 GHz, the design of good performance passive on-chip duplexer is challenging. Recently, Q. Li and Y.P. Zhang [61] reported a passive high-performance RF CMOS transmitting/receiving switch or duplexer, which can be used in this transceiver. To save power, the same frequency synthesizer with VCO is reused for the receiver and the transmitter. During the transmission, a push-pull power amplifier (PA) can be used to transmit the RF signal from the modulator. In the receive mode, the system works like the receiver, and the transmitter blocks are disabled to save the power.

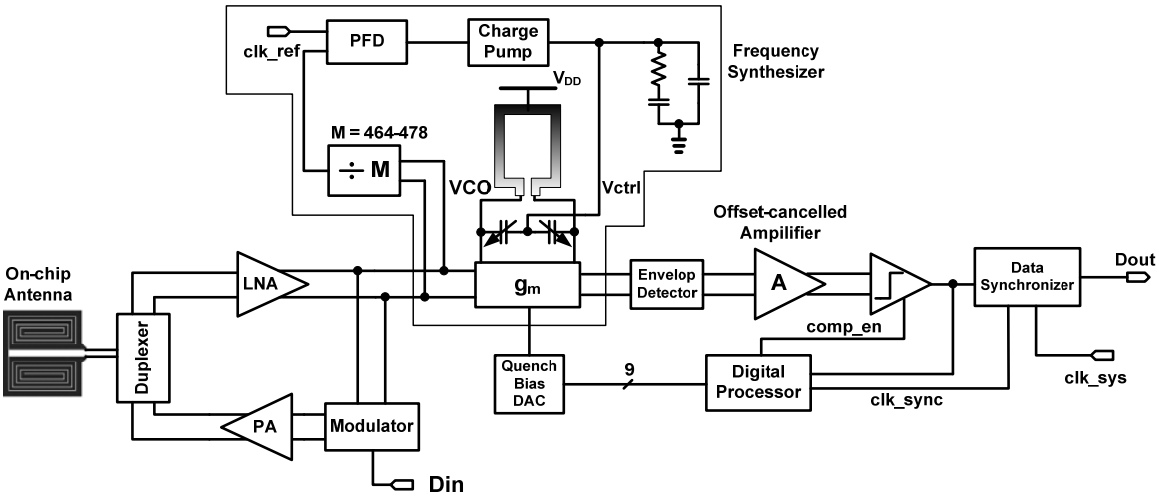


Figure 6.3: Block diagram of the proposed transceiver.

APPENDIX A

ON-CHIP FILTER

A band pass RF filter is anther component for integration onto the chip. Though it is not included in the receiver prototypes in this work, it is still an important part of a conventional fully-integrated receiver. In this section we describe the design of an on-chip filter.

The insertion loss and the bandwidth of integrated on-chip filters are limited by the low quality factor of on-chip inductors. At 5 GHz, inductor Q typically ranges from 5 to 15. To overcome this problem, Q-enhanced LC band pass filters have been studied [62-64]. A critical problem faced with this type of on-chip filter is the high power consumption required to achieve low insertion loss and acceptable dynamic range. At higher frequencies this problem gets worse since inductor Q typically is smaller.

Capacitive termination in the resonators reduces the required length of the transmission line; while periodic capacitive loading reduces wave velocity and wavelength to a fraction of the already reduced value. Similar techniques are employed for VCO design in a compact 5 GHz standing-wave resonator-based VCO as described in section 3.1. A higher Q is achieved since a short transmission line has low substrate and Ohmic losses. Finally, the insertion loss is further reduced with a simple Q-enhancement scheme.

A.1 Filter Design

As shown in Figure A.1 (a), the prototype direct-coupled 2-pole filter consists of two resonators, a negative transconductance (g_m) and matching circuits. A coupled resonator structure similar to that proposed and implemented on a Duroid substrate in [27] is adopted. To make this resonator structure practical for on-chip implementation, techniques introduced in section 3.1.1 are used to improve and enhance-Q. Standing-wave resonators, with simulated Q of 35, are used to reduce insertion loss and power consumption. Negative g_m circuits are utilized to overcome loss in the resonators, so that the insertion loss is further reduced. Matching circuits are used to form 50 Ω input and output impedances.

The equivalent circuit of the coupled resonators is shown in Figure A.1 (b), where the series L-C on the left and right is the equivalent circuit of a Q-enhanced resonator. Coupling between resonators is predominantly magnetic, since at resonance the electrical field in the resonators is maximized near the open-gap side while the magnetic field is maximized at the opposite side [27]. This magnetic-dominant coupling can be modeled as an inductor-formed impedance inverter in Figure A.1 (b).

To achieve an optimum Q for a given resonance frequency, the tradeoff between line length and capacitance is optimized following the methods described in section 3.1. In the final design, capacitors of 3 pF are loaded at the two ends of the resonator transmission line. The combination of the slow-wave effect and capacitive loading at the ends reduces the length of the transmission line to only $0.04\lambda_0$ (λ_0 is the wavelength in free space).

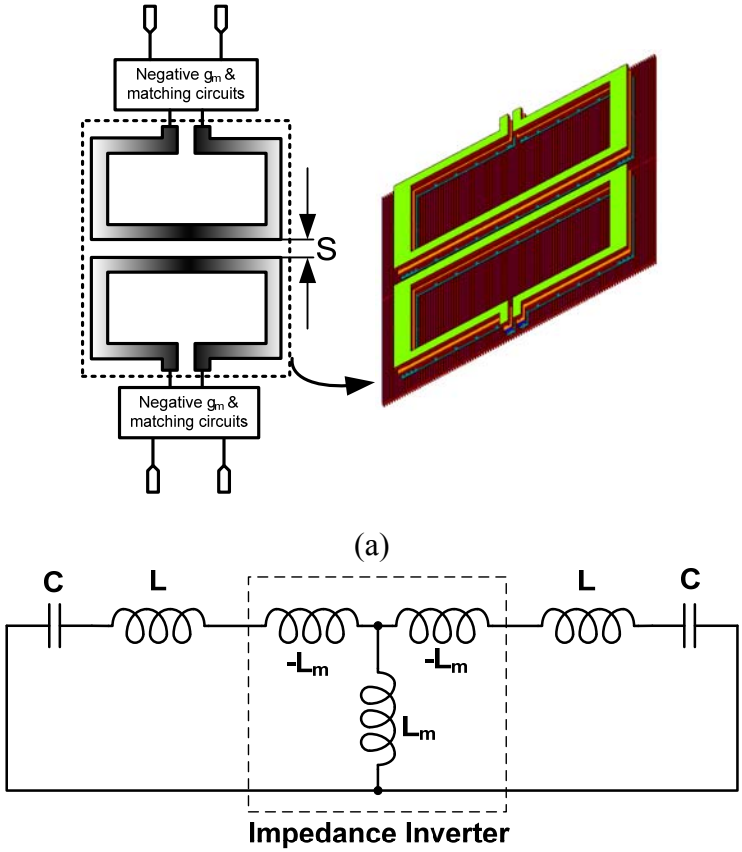


Figure A.1: (a). Block diagram of the direct coupled 2-pole filter. (b). Equivalent circuit of coupled resonators.

The coupling coefficient between the two resonators is determined using the pole splitting method [27] in conjunction with a 3D EM simulator (Zeland IE3D). In the pole splitting method, the relationship between the frequency separation of the poles and the coupling coefficient is determined by:

$$K = \frac{f_a^{\,2} - f_b^{\,2}}{f_a^{\,2} + f_b^{\,2}} = \frac{L_m}{L}, \tag{A.1}$$

where f_a and f_b are the frequencies of the two poles, L_m and L are the inductance values in the equivalent circuit shown in Figure A.1 (b). Figure A.2 shows the coupling coefficient

(*K*) as a function of the horizontal distance between two resonators. Based on these values a 2-pole Chebyshev band pass filter is designed. The simulated filter center frequency is 5.2 GHz and the bandwidth is 8%.

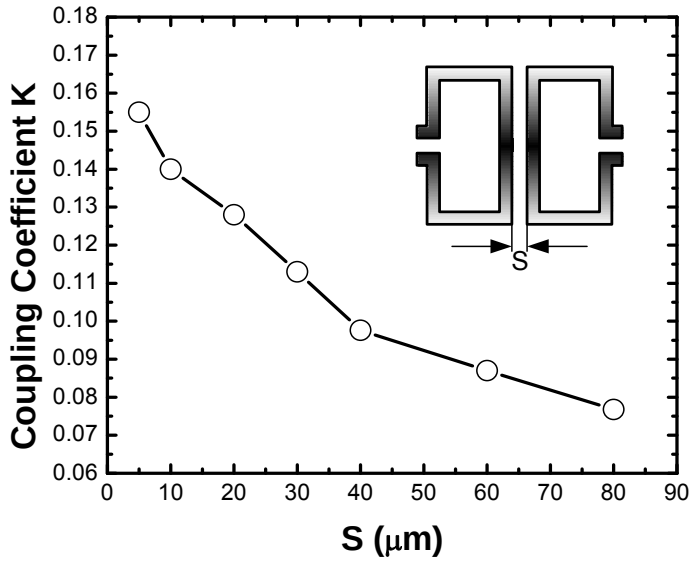
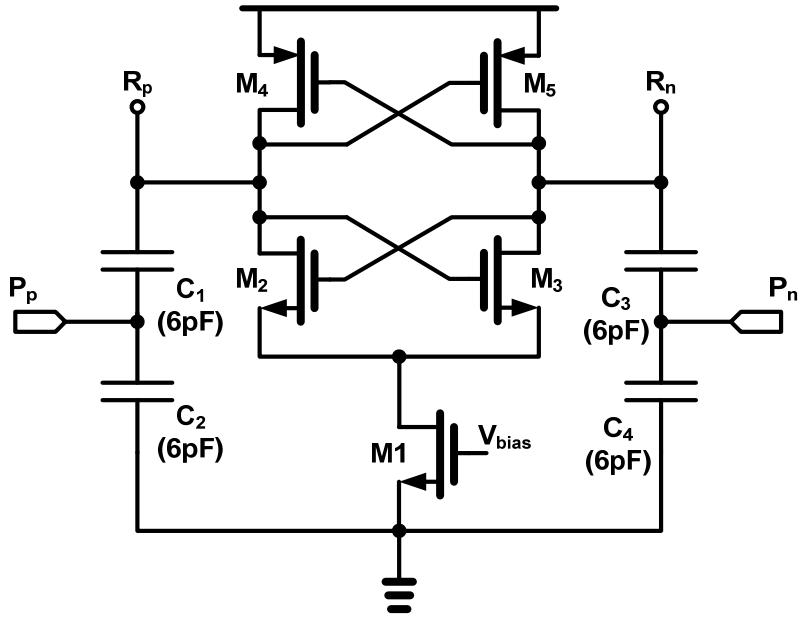


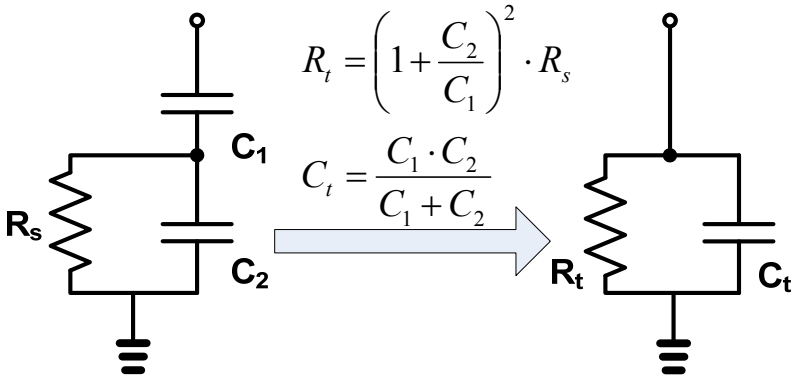
Figure A.2: Simulated coupling coefficients as a function of the horizontal separation between the resonators.

A.2 Q-Enhanced Circuit and Impedance Match

Figure A.3a shows schematics of the negative g_m circuit and matching circuit blocks in the filter block diagram. The cross-coupled FETs introduce negative resistance. Current reuse due to the use of NMOS and PMOS cross coupled FETs improves power efficiency. Two sets of capacitors (C_1-C_4) with an impedance transformation ratio of 4 impedance match resonator high impedance to 50 Ω (Figure A.3b). These capacitors also form loading capacitors (C_t in Figure A.3b) at the ends of resonators.



(a)



(b)

Figure A.3: (a) Q-enhacement and matching circuit schematic (R_p and R_n are connected the resonator). (b) impedance transformation.

B.3 Test Results of the Prototype RF filter

The prototype on-chip filter is fabricated in the same 0.13 μm CMOS. A die micrograph is shown in Figure A.4. The filter occupies 0.3 mm^2 and the total die area including pads is 0.6 mm^2. To measure the characteristic of the filter, two GSSG probes and a network analyzer are used. The system is calibrated and measured following the

method described in Appendix B. The filter transfer S_{21} characteristic is shown in Figure A.5. An insertion loss of 0 dB is achieved at 5.03 GHz with 9.7% 3 dB bandwidth. To measure the in-band IIP3, two signals close in frequency (one at 5 GHz and the other at 5.1 GHz) at different power levels were introduced into the filter. Care was taken to ensure the third-order IM lies well within the filter pass band. For the out-of-band case, two out-of-band signals (one at 5.6 GHz and the other at 6.2 GHz) at different levels were introduced into the filter, again keeping the third-order IM well within the filter pass band. Figure A.6 shows the measured IIP3, where the in-band and out-of-band IIP3 are -8.0 dBm and 7.8 dBm, respectively.

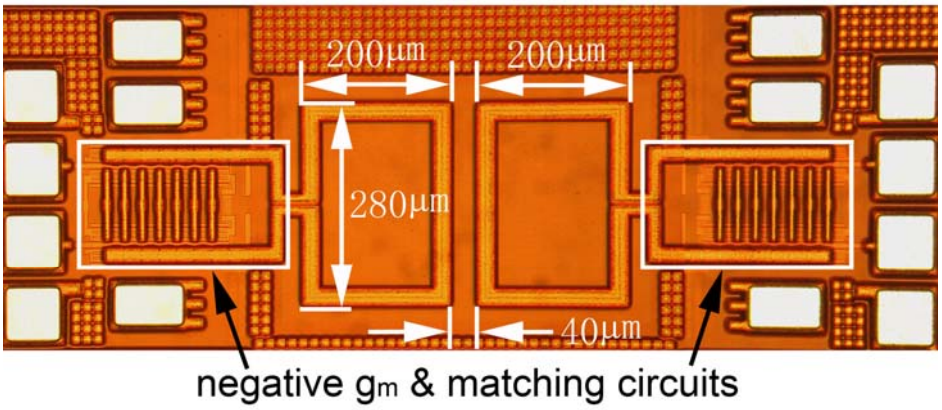


Figure A.4: Die micrograph of the on-chip filter.

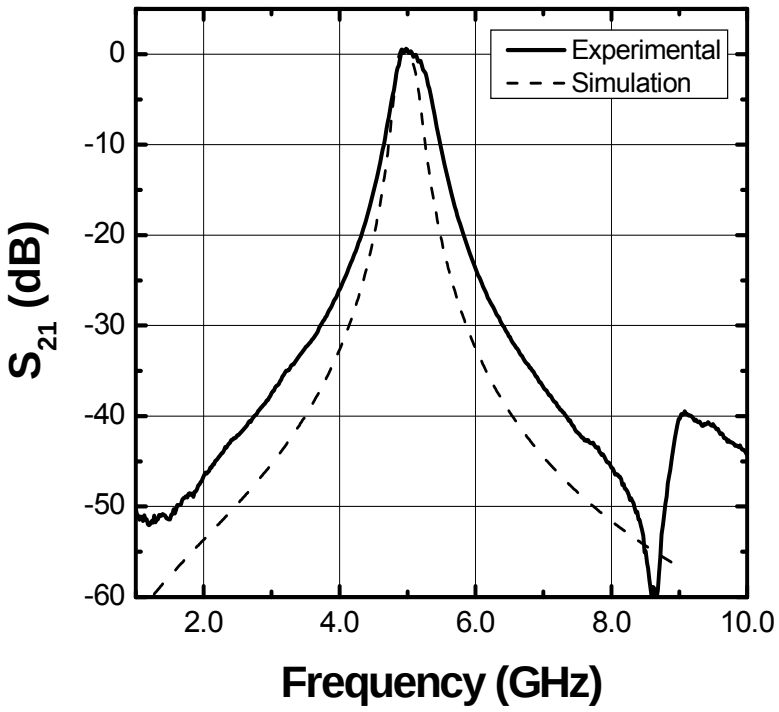
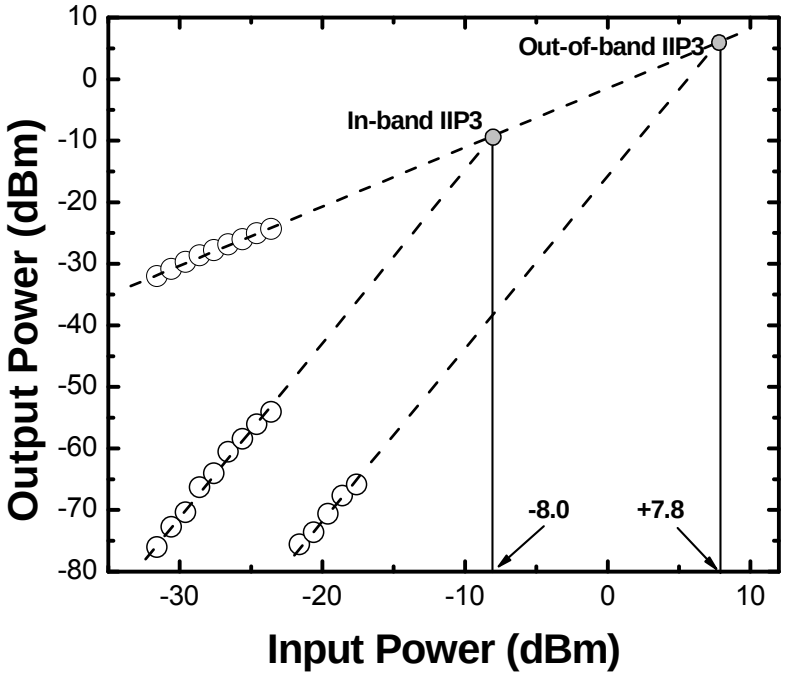
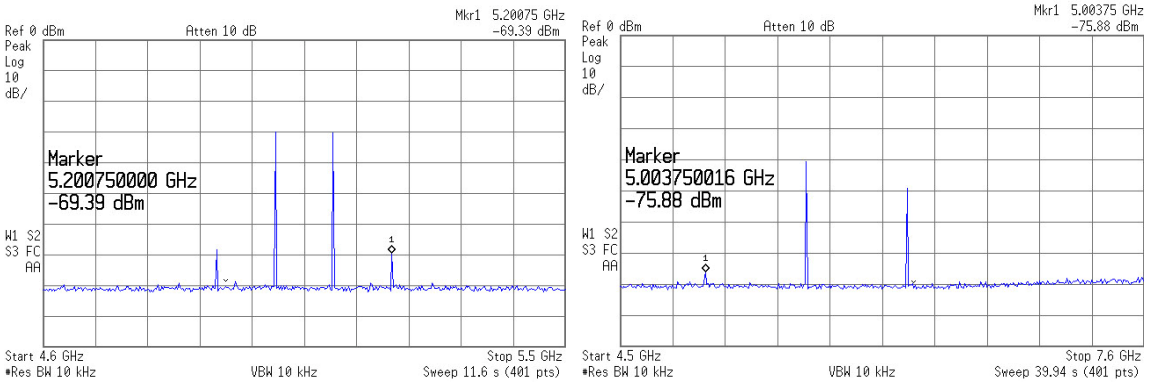


Figure A.5: Measured and simulated filter transfer response.

The filter core draws 2.4 mA from a 1.2 V supply. Table A.1 summarizes the measured performance of the on-chip filter. This prototype is also compared with other recently published Q-enhanced filters in Table B.2. This prototype on-chip resonator based filter outperforms most recently published CMOS on-chip filter in terms of power consumption and die area.





In-band IIP3 Out-of-band IIP3

Figure A.6: Measured in-band, out-of-band IIP3, and corresponding output spectrums.

Table A.1: Measured filter performance summary

Center Frequency	5.03 GHz
Bandwidth	9.5% (-3dB), 6% (-1dB)
Input 1dB Compression	-16.7 dBm
Output Noise Floor	-94 dBm
In-band dynamic range	77.3 dB
In-band IIP3	-8.0 dBm
Out-of-band IIP3	7.8 dBm
Supply Voltage	1.2 V
Power Consumption	2.88 mW
Die Area	0.3 mm^2

Table A.2: Comparison of on-chip filters.

Reference	**Technology**	**f_0 (GHz)**	**Gain (dB)**	**Power Supply (V)**	**PDC (mW)**	**BW**	**Die area (mm^2)**	**P1dB (dBm)**	**Dynamic Range (dB)**
This work	CMOS 0.13 µm	5.03	0	1.2	2.88	9.5% (6% -1 dB BW)	0.3	-16.7	77.3
[65]	CMOS 0.35 µm	2.19	-10-0	1.3	5.0	2.4%	0.1	-30	38
[66]	CMOS 0.25 µm	2.14	0	2.5	17.5	2.8%	3.5	-13.4	56
[64]	CMOS 0.8 µm	0.84	0	2.7-3.0	77	2.1%	2	-18	75

APPENDIX B

MEASUREMENT OF DIFFERENTIAL FILTERS

Differential filters show many advantages over their single-ended counterparts. But the measurement of them is more difficult, since almost all commercially available measurement equipment is designed for single-ended measurement. So in this appendix, a measurement procedure using normal single ended measurement equipment is described. This measurement procedure is used to test the on-chip filter in this project.

A fully differential two-port building block can be modeled as a four-port block. The relationship between standard four-port S-parameters and the differential mixed mode S-parameters has been analyzed in [67, 68]. Based on their theory and analysis, it clearly indicates that differential mixed-mode S-parameters can be calculated from four-port S-parameters. The measurement setup in Figure B-1 is used to measure the 16 S-parameters of the differential filters. Then the measured S-parameters (S_{std}) will be transformed to differential mixed-mode S-parameter (S_{mm}) according to equation 11 using Matlab or Agilent ADS.

$$S_{mm} = \frac{1}{2}\begin{pmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{pmatrix} S_{std} \begin{pmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{pmatrix}^{-1}, \tag{B.1}$$

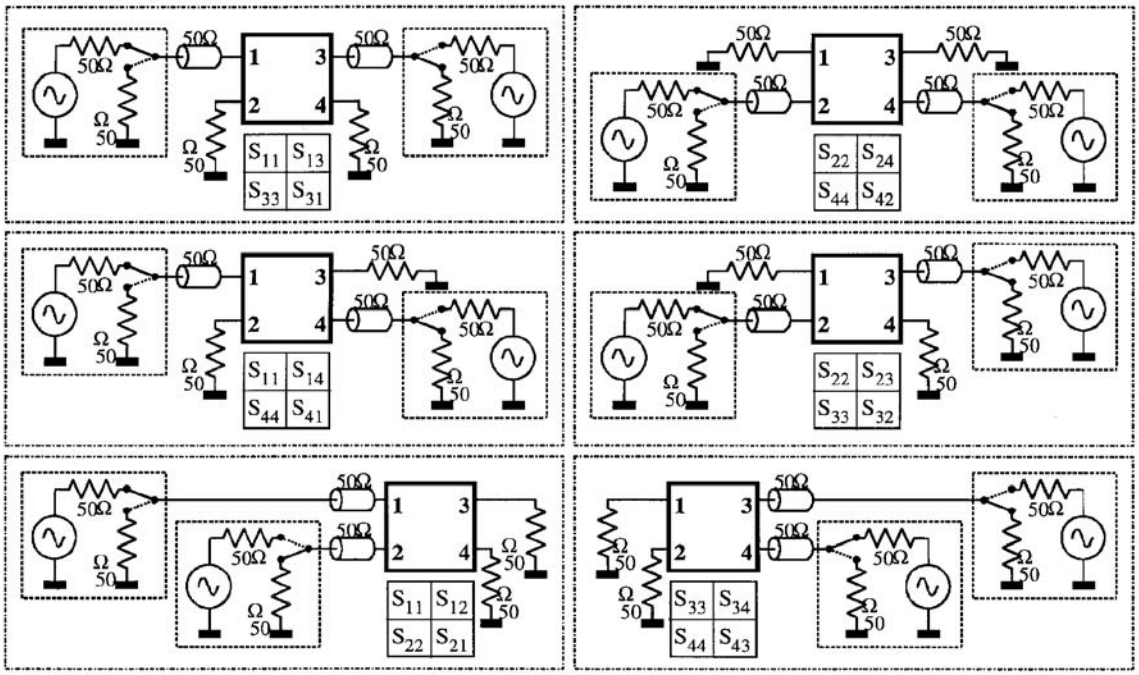


Figure B.1: Measurement setup for the measurement of the differential filters.

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