THE UNIVERSITY OF MICHIGAN

COLLEGE OF ENGINEERING
Department of Electrical Engineering

Instrumentation Report

ELECTROSTATIC PROBES FOR ISIS-A SATELLITE

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1.0 INTRODUCTION

This report describes a Langmuir Probe System which has been designed and built to be carried aboard the ISIS-A Satellite. In this experiment, the current collected by a cylindrical probe mounted on the satellite is measured as the probe potential is swept through a range of negative and positive voltages with respect to the spacecraft, as shown in Fig. 1. The voltage output of the system, which is proportional to the collected current, is interpretable in terms of ionospheric electron temperature and density.* In most respects, the system is the same as those successfully flown on earlier rockets and satellites. However, several improvements were incorporated in this system, including: (1) a new ramp voltage generator which is limited if the system output exceeds a specified value, (2) a latching relay driver, and (3) various logic and control circuitry.

The system consists of an electronics package, Fig. 2, mounted on the interior of the spacecraft and two probe assemblies, one of which is shown in Fig. 3, mounted on the exterior of the spacecraft. Coaxial cables connect the probes electrically to the electronics package.

*L. H. Brace, "The Dumbbell Electro-Static Ionosphere Probe," 1962.

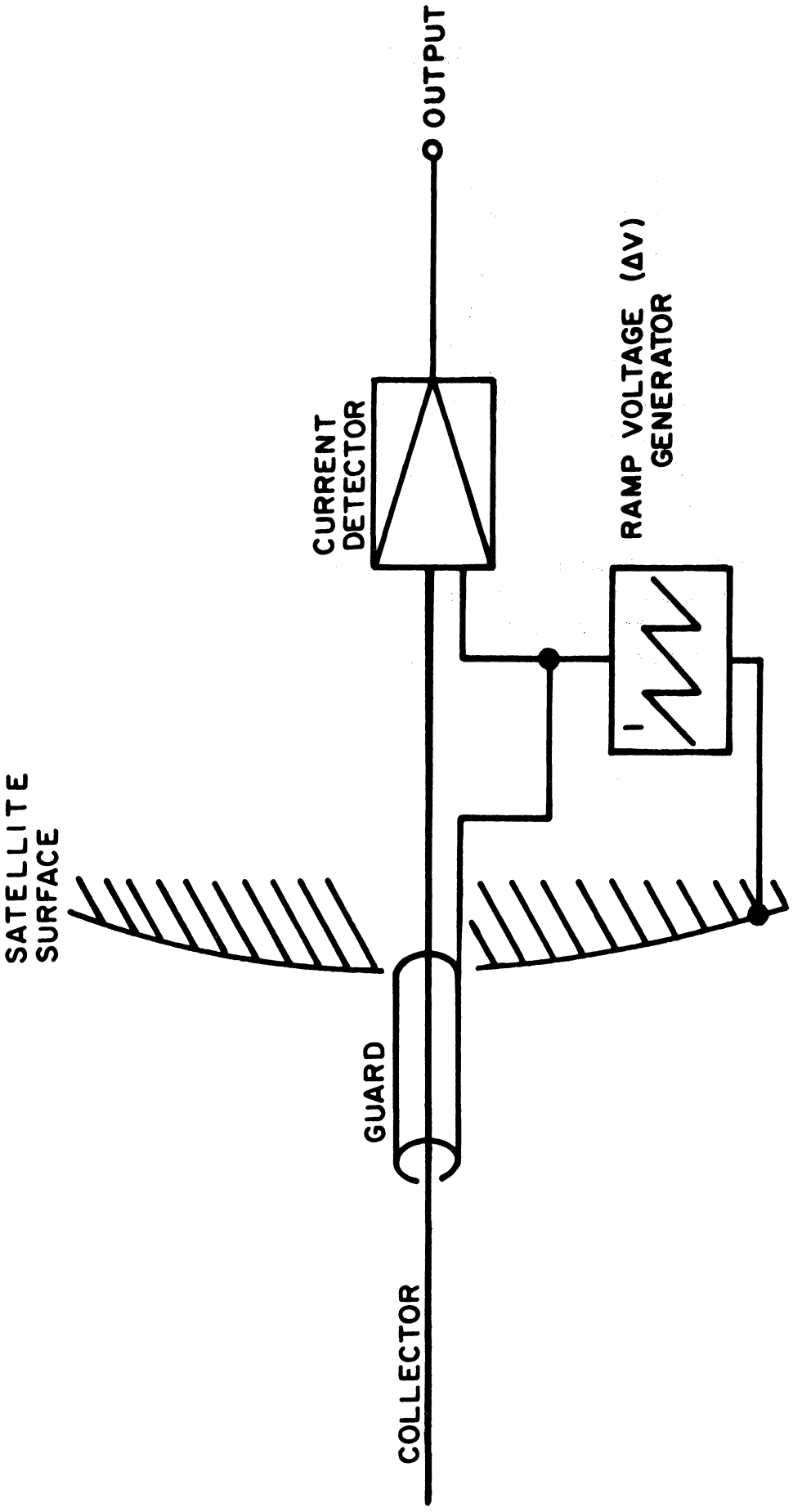


Fig. 1. Electrostatic probe experiment.

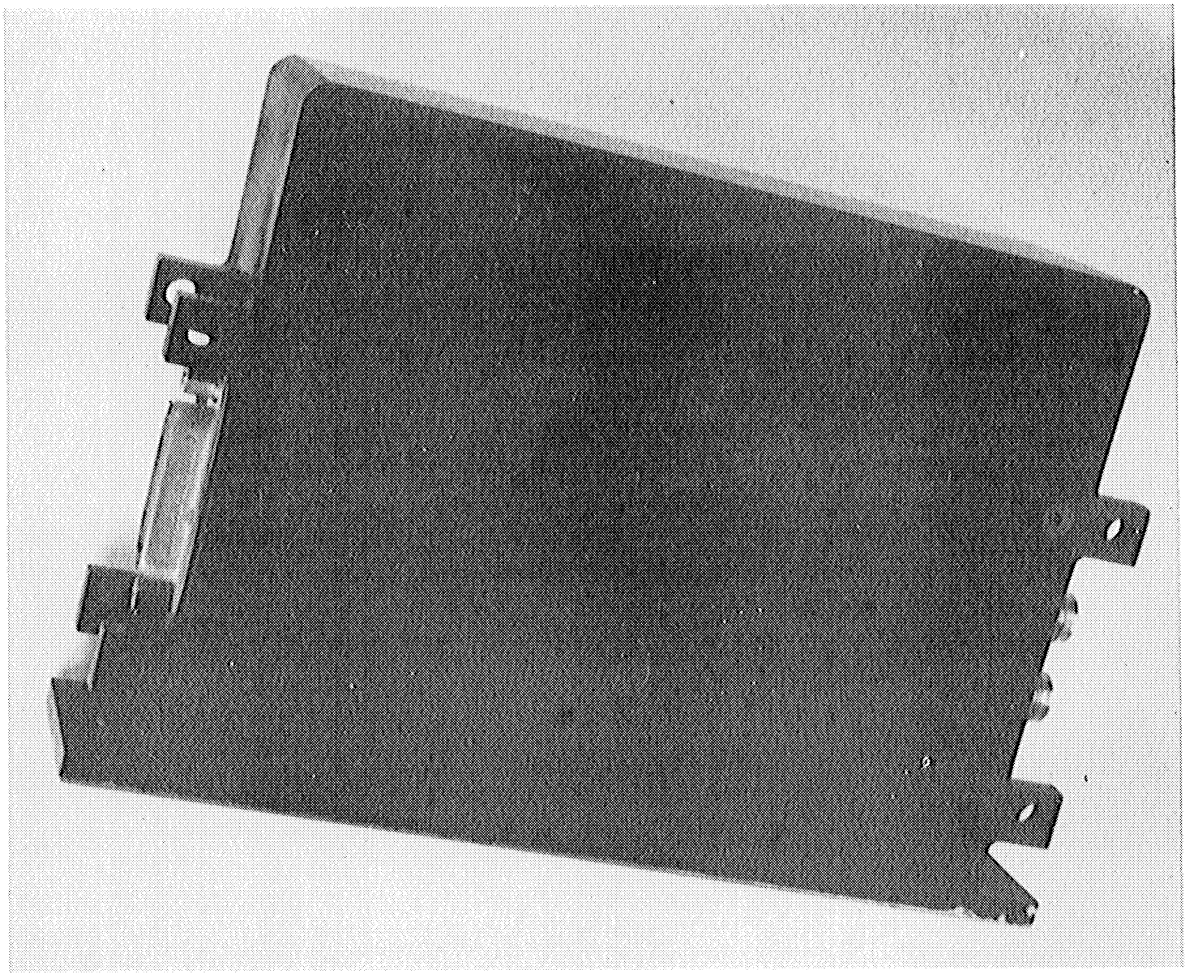


Fig. 2. Electronics unit.

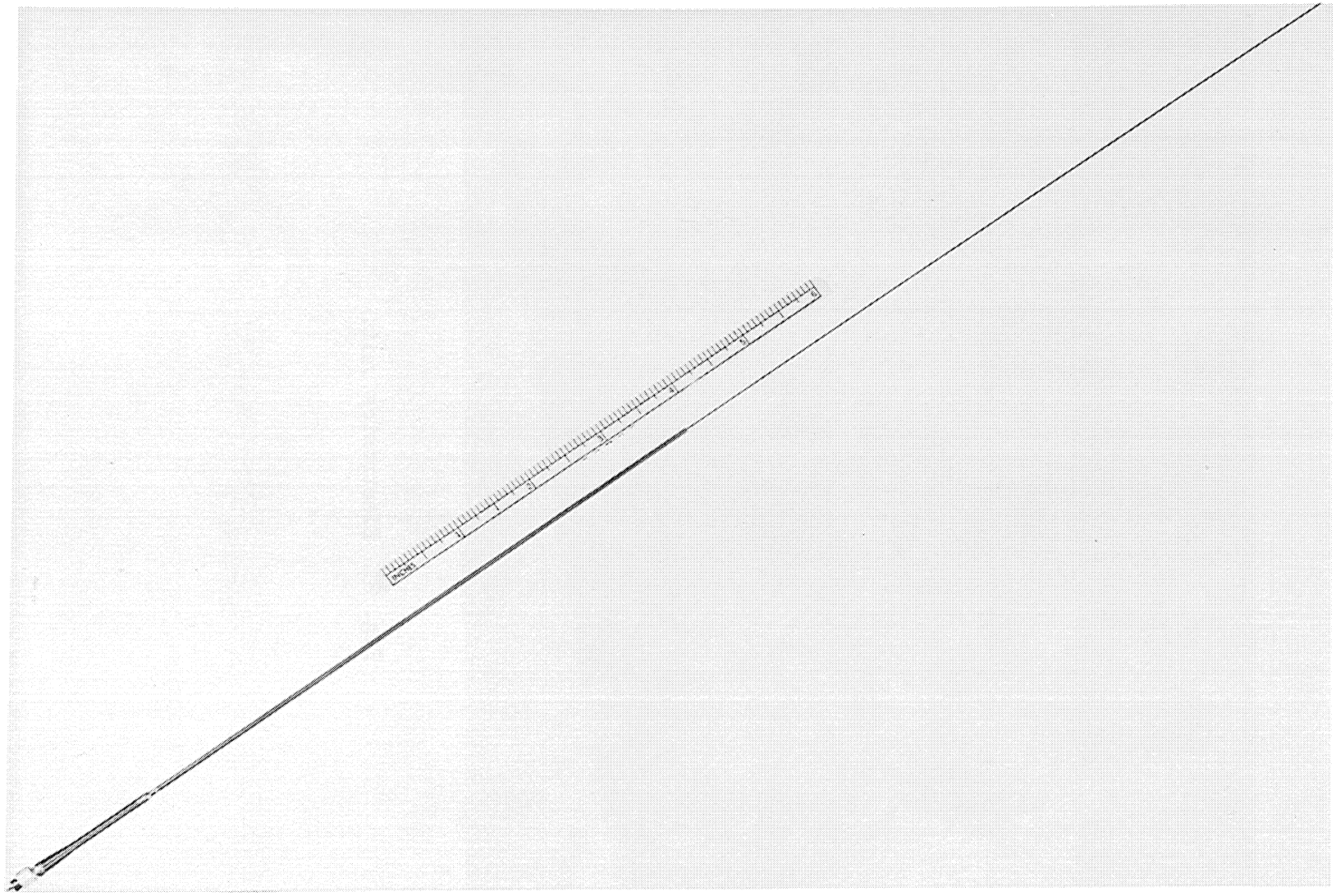


Fig. 3. Cylindrical probe.

2.0 SYSTEM DESCRIPTION

2.1 PROBE ASSEMBLY

The probe assembly consists of a probe electrode, guard electrode and the probe mount, which can be attached to or removed as a unit from the spacecraft at any time before the shroud is attached, without disturbing any of the other spacecraft assemblies. The collector and guard electrodes are mounted on a connector with a concentric spring arrangement that allows the probe assemblies to be folded out of the way for stowing and to return to their desired position at shroud ejection. Figure 4 shows details of the probe assembly.

2.1.1 Collector Electrode

The collector electrode is a stainless steel rod 9 in. long and 0.022 in. in diameter.

2.1.2 Guard Electrode

The guard electrode is a stainless steel tube 0.065 in. O.D. and 9 in. long. It is concentric with the collector electrode and insulated from it with teflon tubing. The resistance between the two electrodes is on the order of 10^{10} ohms or greater at room temperature.

The guard electrode is driven with the same voltage as the collector and hence places the collector beyond the sheath of the satellite surface and provides a continuous sheath at the collector-guard boundary.

2.1.3 Probe Mount

The probe mount provides a base for mounting the probe assembly and also contains two rf filters, one for the collector and one for the guard, to prevent conduction of rf interference to the electronics package.

2.2 ELECTRONICS UNIT

The electronics unit contains a dc-dc convertor, two dual range current detectors, a ramp voltage generator, a master timer, calibration circuits, and logic to control detector sensitivities, probe switching and other functions. A block diagram of the system is shown in Fig. 5 and the schematic is shown in Fig. 6.

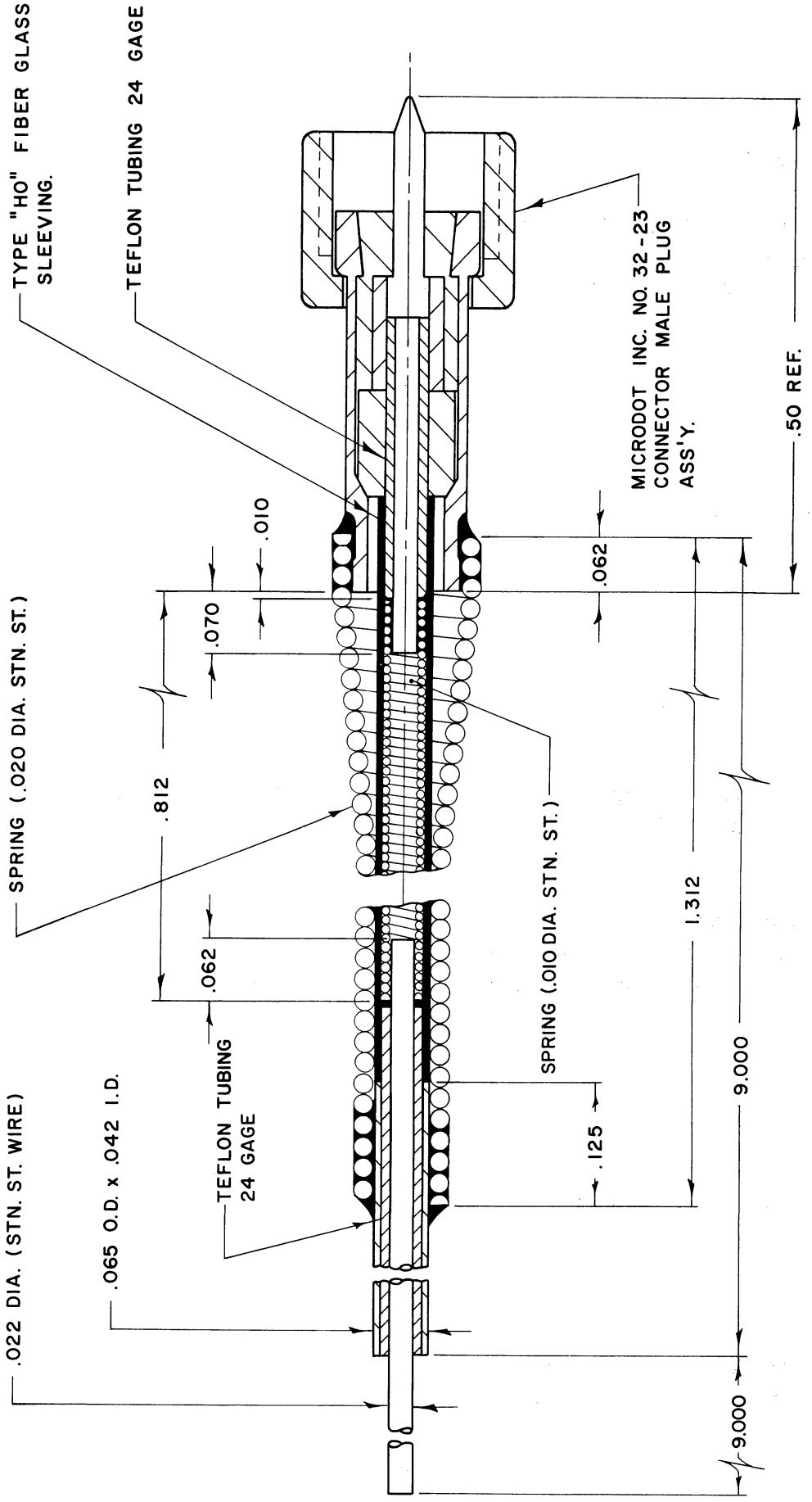
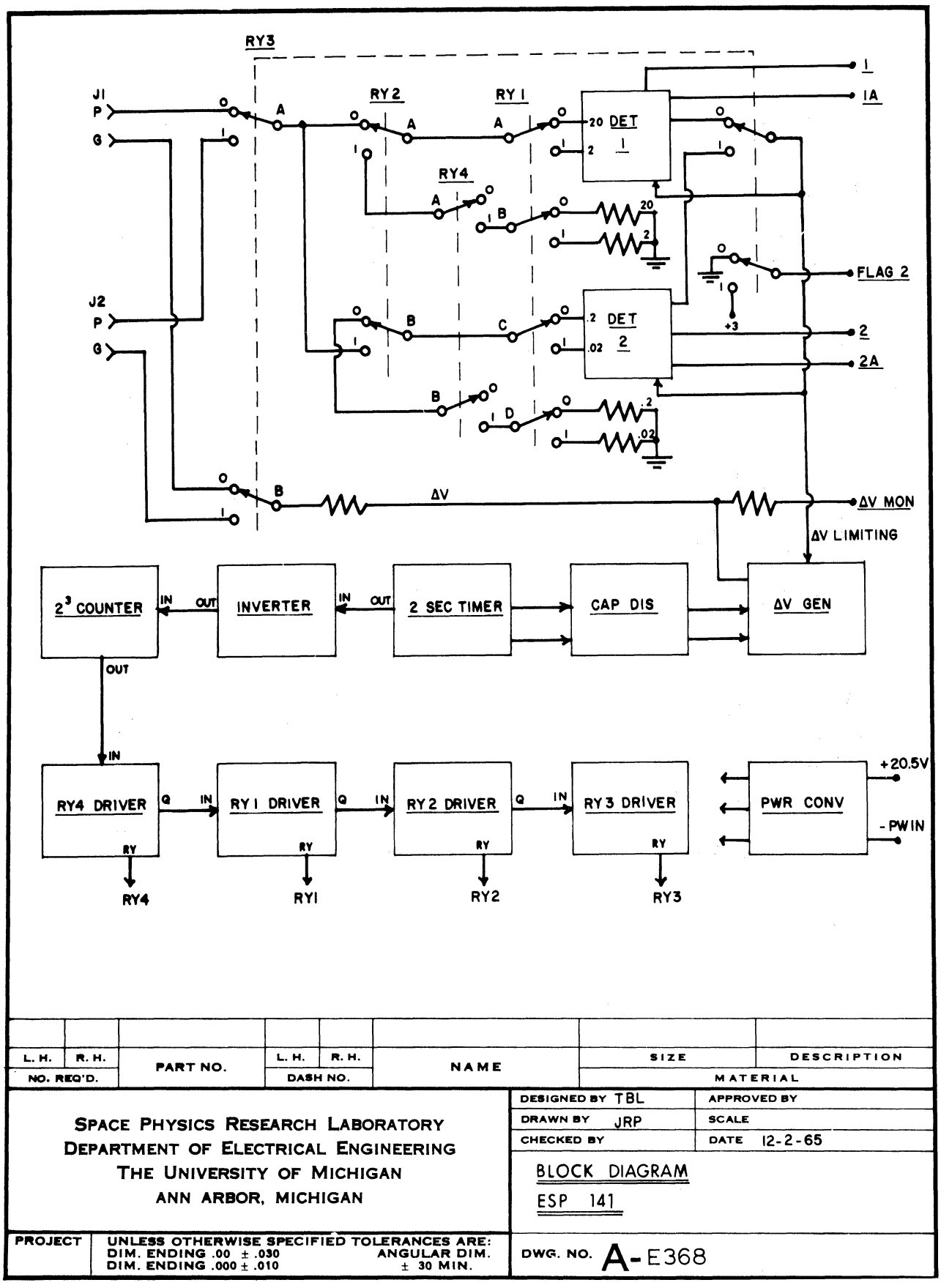


Fig. 4. Probe assembly drawing.



L. H.	R. H.	PART NO.	L. H.	R. H.	NAME	SIZE	DESCRIPTION
NO. REQ'D.			DASH NO.			MATERIAL	

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DEPARTMENT OF ELECTRICAL ENGINEERING
THE UNIVERSITY OF MICHIGAN
ANN ARBOR, MICHIGAN

DESIGNED BY TBL	APPROVED BY
DRAWN BY JRP	SCALE
CHECKED BY	DATE 12-2-65

BLOCK DIAGRAM
ESP 141

PROJECT

UNLESS OTHERWISE SPECIFIED TOLERANCES ARE:
DIM. ENDING .00 ± .030 ANGULAR DIM.
DIM. ENDING .000 ± .010 ± 30 MIN.

DWG. NO. A-E368

Fig. 5. System block diagram.

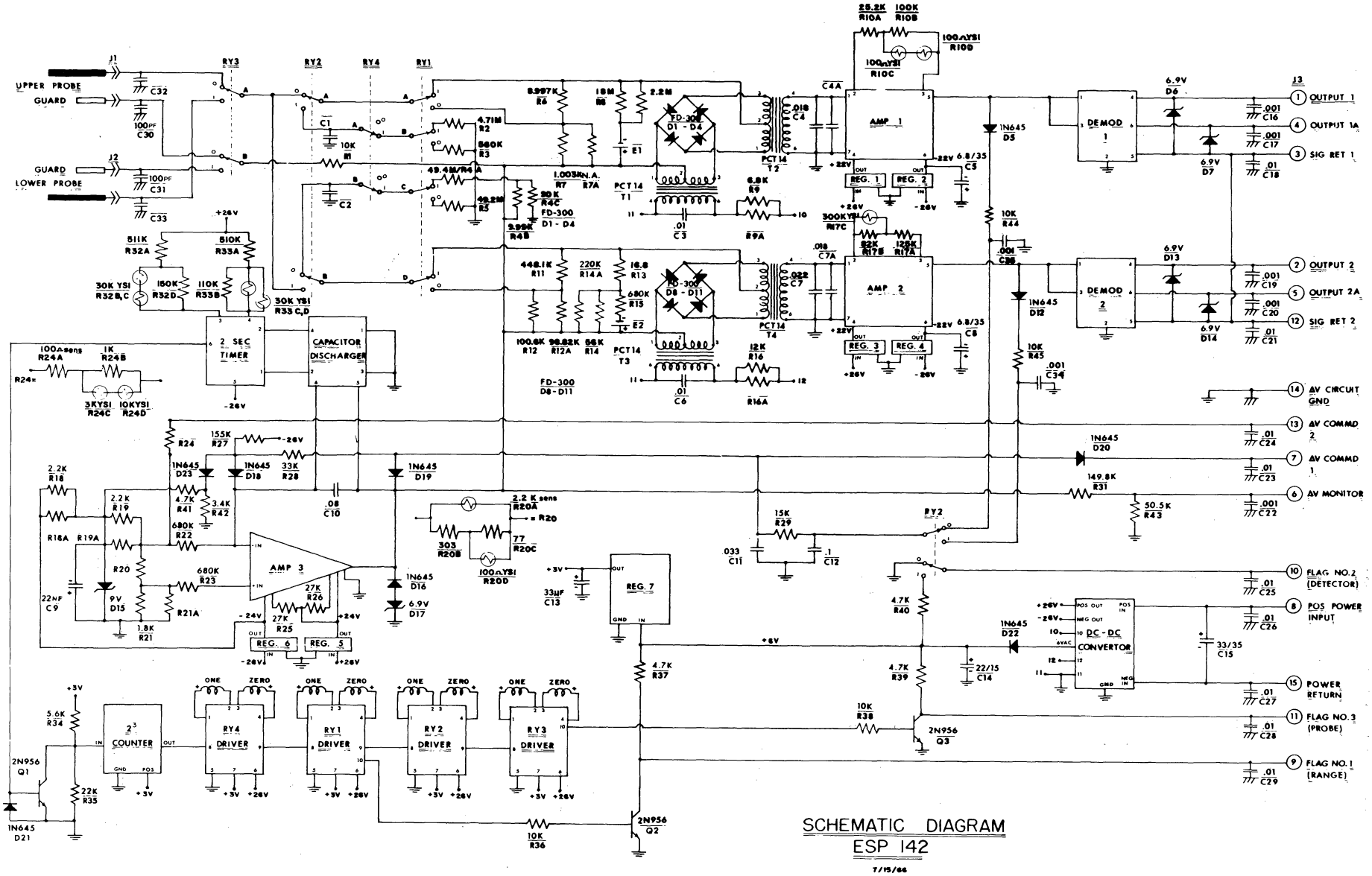


Fig. 6. System schematic diagram.

The unit measures 6.55 x 4.18 x 1.24 in., and weighs 1.78 lb. It is designed to operate with input voltages between 18 and 50 v over a temperature range of -40° C to +60° C at a constant input current of about 85 ma.

2.2.1 The dc-dc Convertor

The dc-dc convertor converts the spacecraft supply voltage to suitable voltages for the various electronic subcircuits. It is a standard convertor circuit utilizing a Zener reference diode for primary regulation.

Since the primary voltage is clamped with a reference diode and the load current is kept constant, the operating frequency of the convertor remains constant. To insure that this constant frequency would meet the spacecraft requirement of 1800 hz ± 3%, the characteristics of the transformer core were measured through a pilot run and used for operating frequency computations.

A positive temperature coefficient resistor in the convertor starting circuit allows the convertor to turn on over the required temperature range of -40 to +60°C at the minimum supply voltage of 18 v.

Figure 7 shows the test results for the dc-dc convertor of the prototype system, ESP141. The convertor starts its voltage regulation at approximately 18 v input over the required temperature range. Since it employs simple primary regulation, the power input is proportional to the input voltage and the input current remains constant (approximately 85 ma) within the regulation range.

2.2.2 Dual Range Current Detector

A prime instrumentation requirement of a Langmuir Probe experiment is a floating input current detector, as indicated in Fig. 1. A dc amplifier employing a diode ring modulator* is used in this case. The diode ring modulator is a proven, reliable system, which is well suited to space instrumentation because of its small size and low power consumption. It also has a high common mode input voltage capability which is utilized in this system.

Two completely isolated dual range current detectors are used to increase the reliability of the system. Each detector consists of a diode ring modulator, a modulator driver, an ac amplifier and a demodulator.

To insure the accuracy of the current detectors, the following steps were taken; (1) The diodes utilized in the demodulator section were matched over the entire operating temperature range, (2) a temperature compensating resistor network was added to the ac amplifier section to ensure constant amplifier gain,

*L. H. Brace, "Transistorized Circuits for Use in Space Research Instrumentation," 1959.

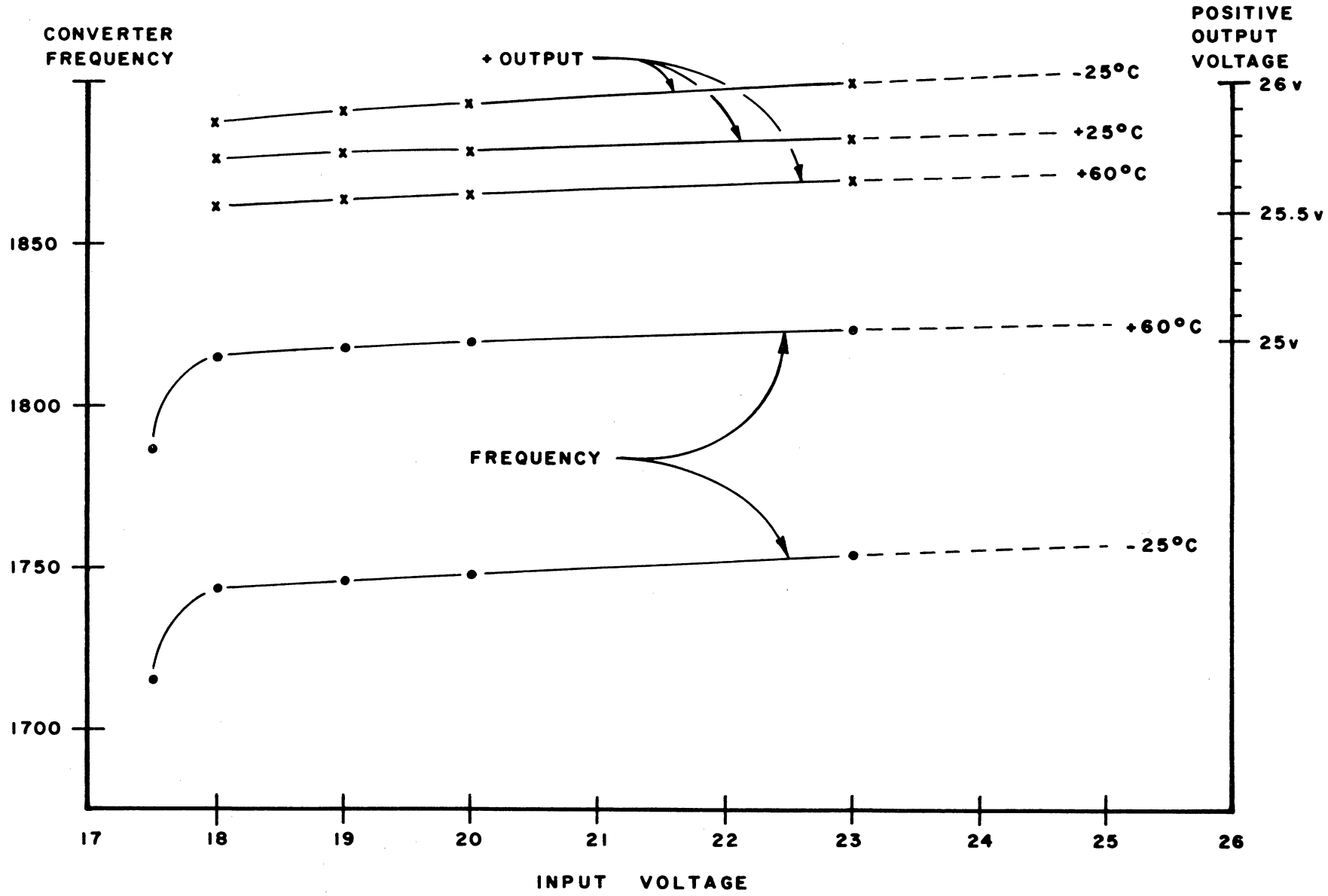


Fig. 7. Dc-dc converter characteristics.

and (3) the modulator section was prebiased to assure linearity over the entire measured current range. Figure 8 is the schematic diagram of one detector.

The detector input resistance is dominated by a shunt resistor across the ring modulator. The input resistance of the modulator itself is approximately 100k. The shunt resistances are chosen such that the connection of either detector to the probe will cause not more than 1% deviation at the detector output. The driving power for the modulator is obtained from a separate winding of the dc-dc convertor transformer. The operating frequency of the transformer is near optimum for modulator operation.

The frequency response of the detector is limited primarily by the low pass LC filter of the demodulator. The detector rise and fall times are 2 and 5 msec, respectively. Figure 9 shows a typical detector output with a dummy probe resistor connected to the input.

Detector No. 1:

Range:	20 μa and 2 μa full scale
Input Impedance:	1.1 kΩ for 20 μa
	19 kΩ for 2μa
Output Impedance:	3.1 kΩ for both no. 1 and no. 1A
Output Voltage:	0-6.8 v (normal mode)
	0-5.5 v (ΔV cmd mode)

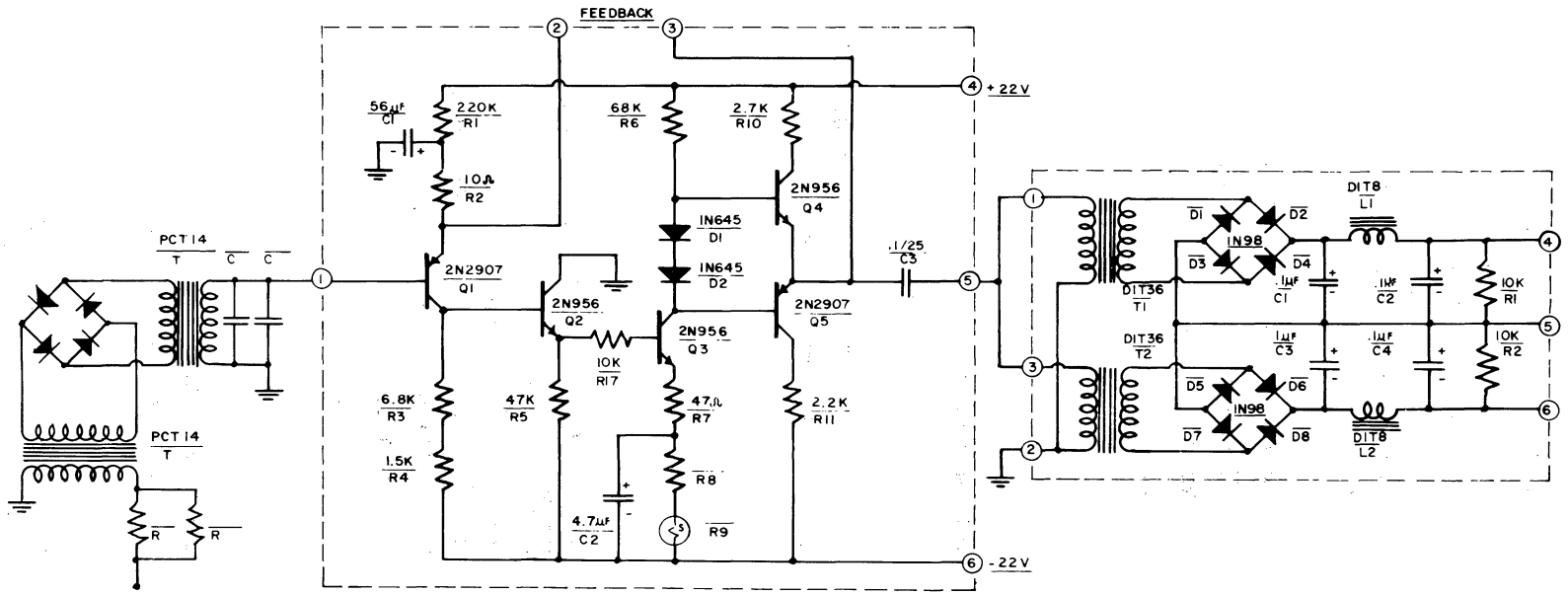
Detector No. 2:

Range:	0.2 μa and 0.02 μa full scale
Input Impedance:	55.8 kΩ for 0.2 μa
	93.2 kΩ for 0.02 μa
Output Impedance:	3.1 kΩ for both no. 2 and no. 2A
Output Voltage:	0-6.8 volts (normal mode)
	0-5.5 volts (ΔV cmd mode)

2.2.3 Ramp Voltage (ΔV) Generator

The ramp voltage (ΔV) generator produces a continuous sawtooth wave form which is applied to the probe. Two ramp slopes are available and are controlled by ground command.

Figure 10 shows the operational amplifier integrating circuit used to generate the ramp voltage. The output voltage of the ramp generator, Er is expressed as follows:



ENGINEER TBL	DRAFTSMAN JRP
SPACE PHYSICS RESEARCH LABORATORY DEPARTMENT OF ELECTRICAL ENGINEERING UNIVERSITY OF MICHIGAN ANN ARBOR, MICHIGAN	AMPLIFIER AND DEMODULATOR ESP 14 B-E294 018-901
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Fig. 8. Detector schematic diagram.

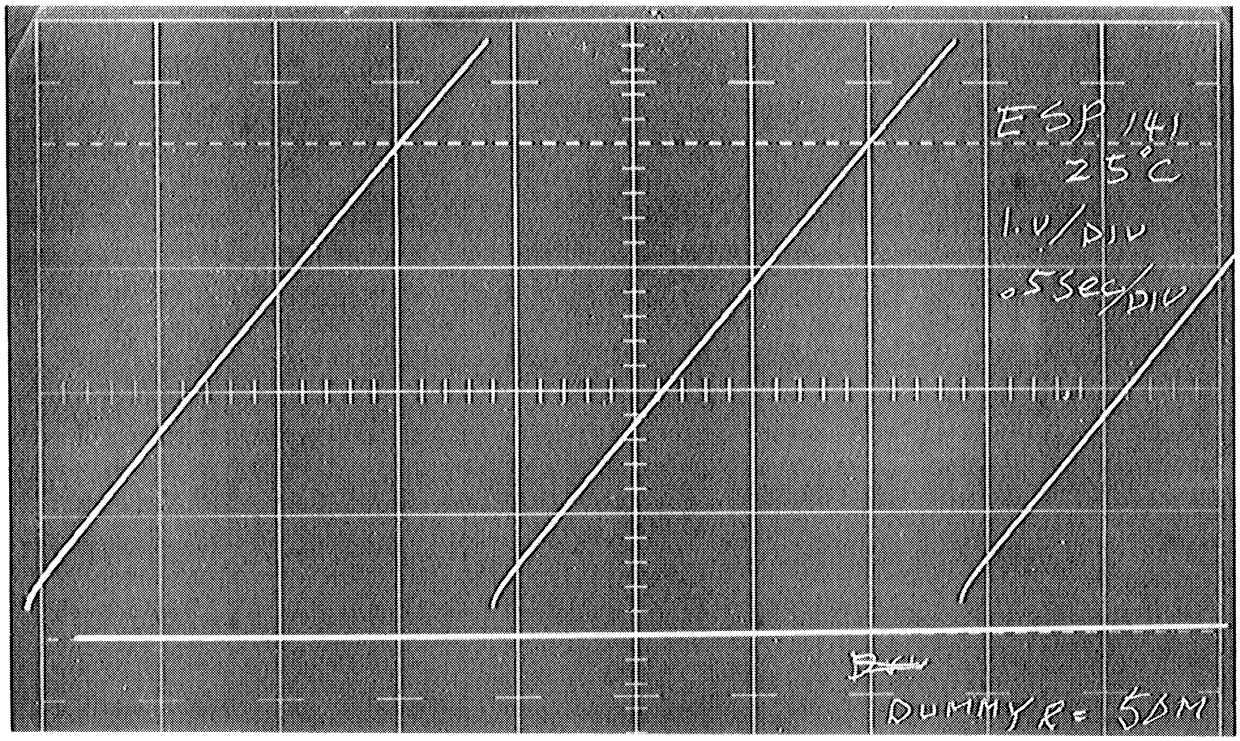

Fig. 9. Typical output waveform with dummy resistor.

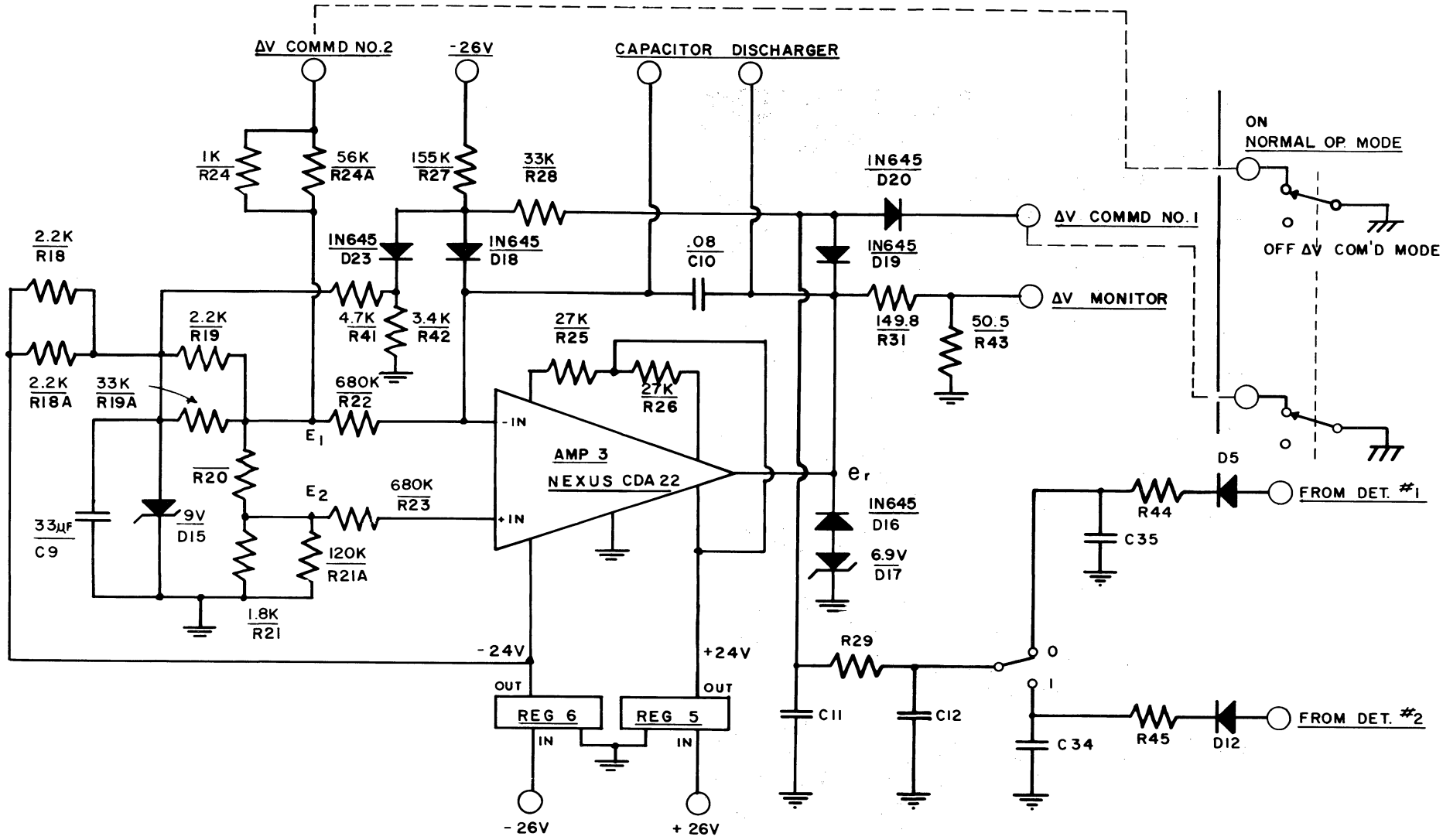

Fig. 10. ΔV generator and limiter.

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SPACE PHYSICS RESEARCH LABORATORY DEPARTMENT OF ELECTRICAL ENGINEERING UNIVERSITY OF MICHIGAN ANN ARBOR, MICHIGAN	ΔV AND LIMITER ESP 14	11-13-65 5-25-65
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$$Er \cong E_2 - (E_1 - E_2)\, t/rc$$

The starting point is set by the fixed voltage E_2 and the slope is determined by $(E_1 - E_2)\, t/rc$. The integrating capacitor is periodically discharged by transistor switches which are controlled by the master timer, as shown in Fig. 11. For normal operation the ΔV command side of resistor R24 is grounded producing the low level ramp voltage, Lo ΔV. When the ΔV command is initiated this ground connection is removed thus increasing the voltage levels of E1 and E2 and producing the higher level ramp voltage, Hi ΔV. Both wave forms are shown in Fig. 12.

Since the measuring accuracy of the system depends upon the accuracy of the ramp voltage applied to the probe, several steps are taken to insure the reliable operation of this portion of the system, among them are the following: a very stable silver mica capacitor is used for the integrating capacitor; a zero temperature coefficient zener diode is used to stabilize the ΔV input voltages, E1 and E2 over the operating temperature range; and the operational amplifier used is a very stable, low offset current device, manufactured to Mil. Specs. Also, to increase the reliability of the ramp generator, a series parallel combination of four transistors is utilized for the capacitor discharge circuit, requiring the failure of two transistors to degrade the operation of this critical circuit.

ΔV Ramp Generator Data

	Hi ΔV	Lo ΔV
Magnitude:	-4 to + 20 v	-2 to +10 v
Slope:	12 v/sec	6 v/sec
Period:	2 sec	2 sec

2.2.4 ΔV Limiting Circuit

Due to the unpredictibility of the spacecraft potential, Hi and Lo ΔV ranges are provided to ensure that the probe voltage will be able to sweep positive enough to accelerate electrons in the plasma.

In the normal operating mode the ramp generator is held on Lo ΔV and the ΔV limiting circuit is inoperative. If the Lo ΔV mode does not supply sufficient probe voltage, due to excessive spacecraft potential, the ramp voltage can be commanded to the Hi ΔV mode. During this ΔV command mode, the ΔV limiting circuit becomes operative. In this mode the ΔV ramp voltage is limited to sweep no higher than is required to cause full scale detector output (approximately 5.5 v) for the duration of the sweep.

The purpose of this circuit is to be sure that the positive sweep is no higher than necessary to obtain measurements while still allowing the flexibility

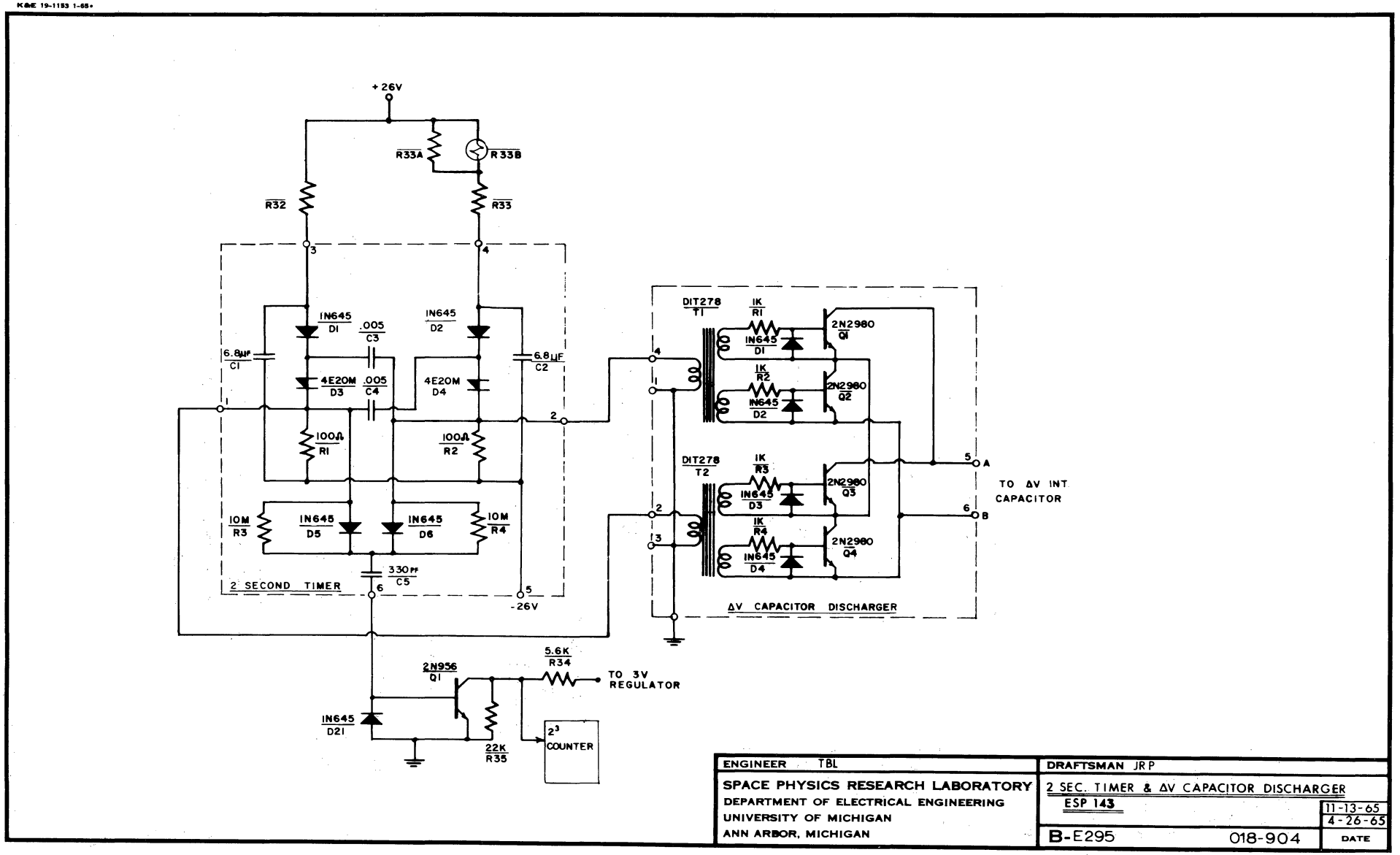

Fig. 11. Master timer and ΔV capacitor discharge circuit.

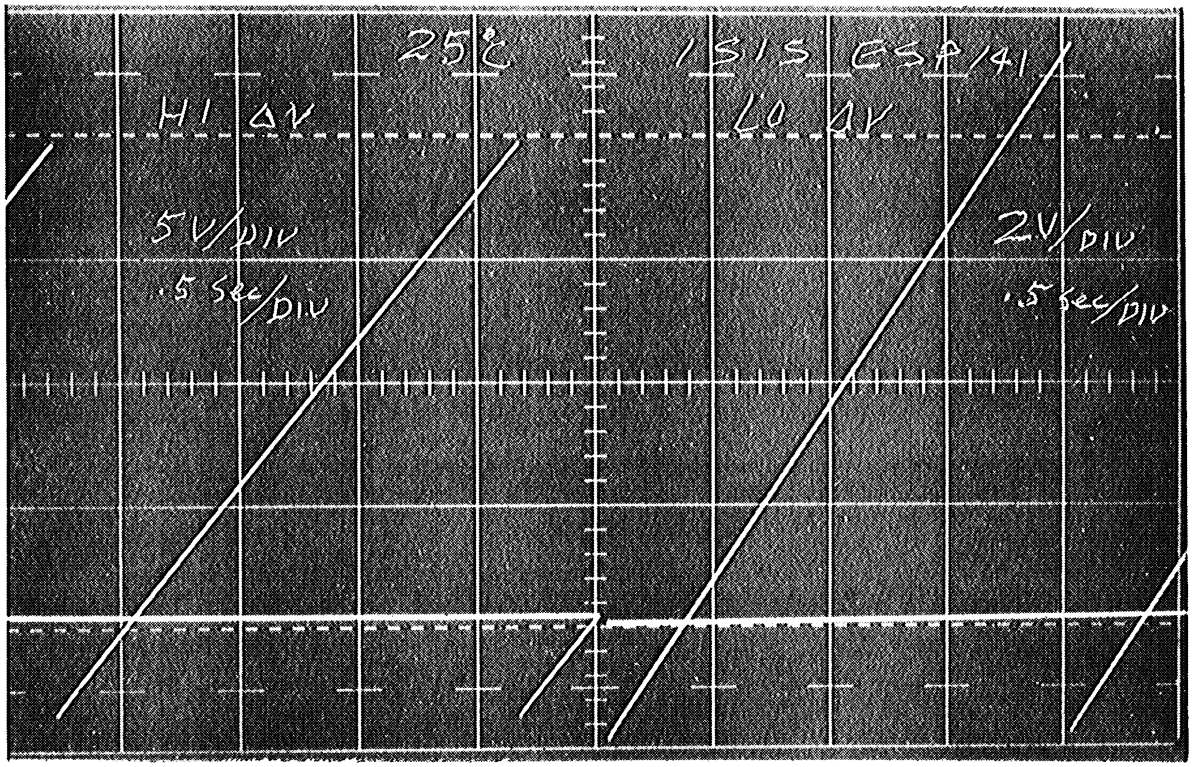

Fig. 12. ΔV waveform.

of increasing the sweep voltage if the spacecraft potential were more negative than anticipated.

The following is a description of the circuit operation: Referring to Fig. 6, the ac carrier of either amplifier 1 or 2 is rectified by a diode, filtered by R29, C11 and C12, and applied to the voltage divider consisting of R27 and R28. R27 is chosen such that when the demodulated amplifier output is approximately 5.5 v, the voltage at the junction of R27 and R28 rises to -4.5 v and D18 begins to conduct, stopping the ΔV sweep.

When not in the ΔV command mode, the ΔV command 1 line renders the ΔV limit circuit inoperative by grounding the output of the filter through diode D20.

While in the ΔV command mode, limiting is prevented during the negative portion of the ΔV sweep by the combination of D19, D23, R41, and R42 which clamp the limiter voltage at -3.5 v, thus rendering the limiter inoperative.

2.2.5 Logic and Associated Circuits

The logic circuits, shown in Fig. 5, consist of a master timer, a pulse shaping circuit, a three-stage ripple counter and the latching relay drivers. All sequencing functions of the system, including probe switching, detector range changing, and system calibration, are controlled by the logic circuit and are synchronized with the master timer period as shown in Fig. 13.

2.2.5.1 Master Timer. A simple Shockley diode relaxation oscillator is used for the master timer and is shown in Fig. 11. The timer is actually two sychronized timers, paralleled for reliability. Either timer is capable of operating the system independently. The 2-sec timer period, although not critical, is held to within ±2% over the operating temperature range by means of a resistor temperature compensating network. The output of the timer drives the capacitor discharge circuit of the ramp generator and the pulse shaping circuit for the ripple counter.

2.2.5.2 Ripple Counter. The ripple counter is a standard 2^3 counter utilizing three Texas Instrument SN 510 integrated circuit flip-flops. The SN 510's were chosen because of their small size and minimal power consumption.

2.2.5.3 Relay Drivers. Latching relays are used throughout the system for various functions such as probe switching, calibration, and detector range changing. The relay driver circuit, as shown in Fig. 14, utilizes a transistor switch to discharge a capacitor through a relay coil to latch the relay in either of its stable states. Thus, the relay does not require the steady power drain of the conventional relay. The control signals for the relay drivers are obtained from the flip-flops of the counter chain. Figure 14 is the schematic diagram of counter chain and the relay drivers.

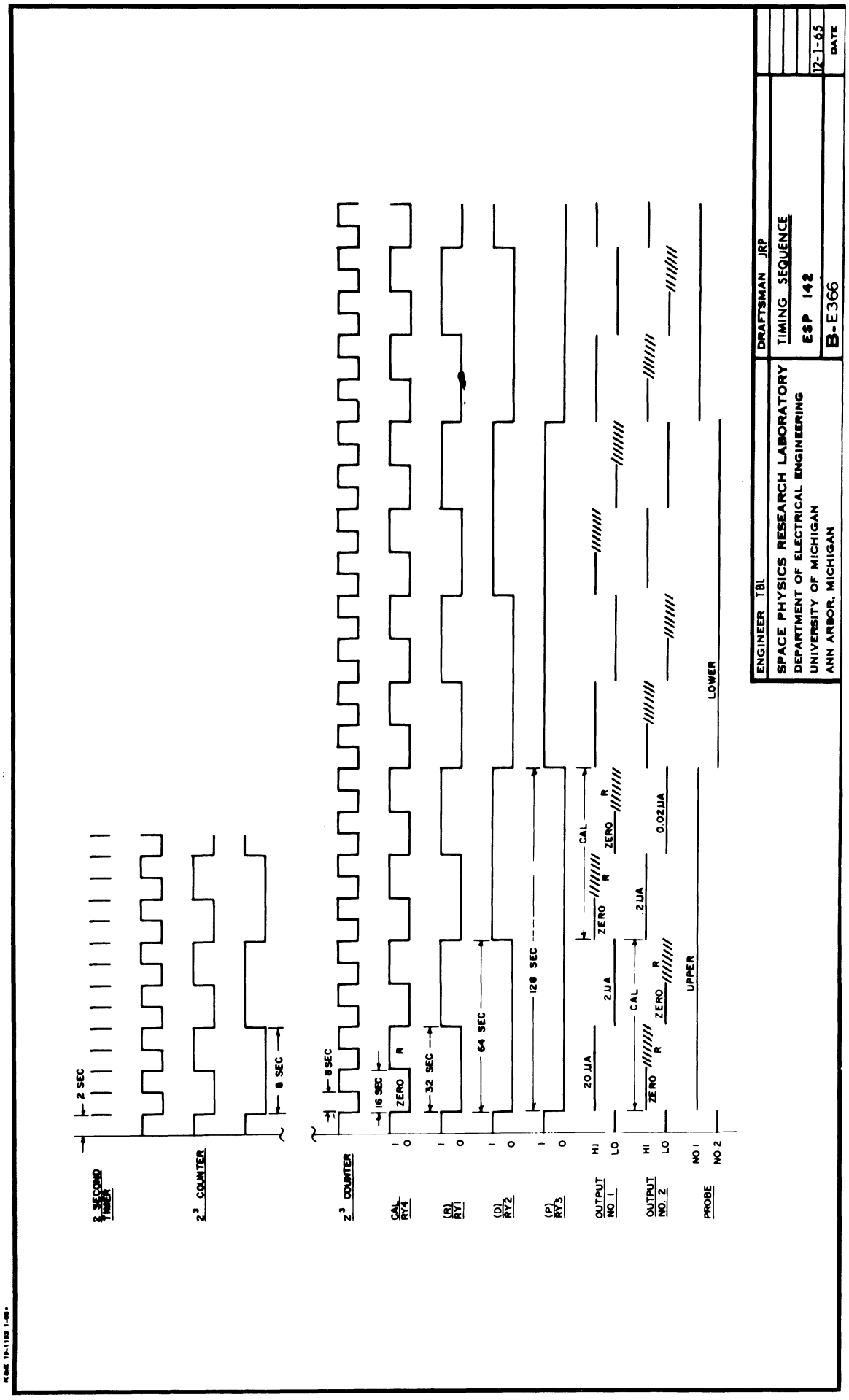

Fig. 13. Timing sequence.

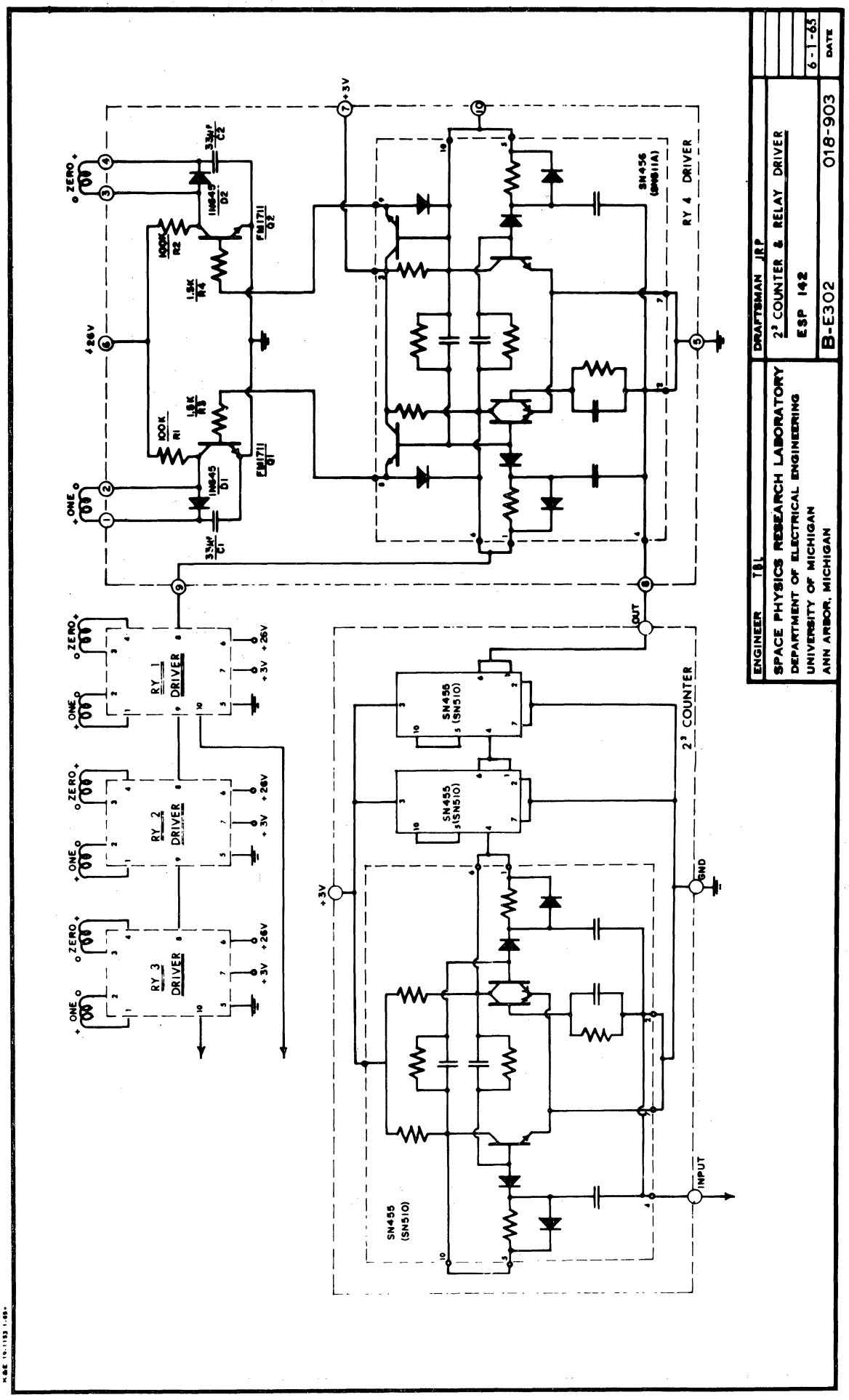

Fig. 14. Relay driver and 2^3 counter circuits.

3.0 SYSTEM CALIBRATION

One of the systems two detectors is used for current measurements at all times. The detector not engaged in measurement at any given time is calibrated. The calibration sequence consists of a zero current mode and a simulated current mode for each detector range.

During the calibration sequence, the probe is disconnected from the detector. For the zero current mode, only a capacitor, equivalent to the probe cable capacitance, is connected to the detector. For the simulated current mode, a known resistor, appropriate in value for the associated detector sensitivity, is connected to the detector. The equivalent probe cable capacitance is also connected during this mode.

The accuracy of the detector calibration is limited only by the accuracy of the calibrate resistors and the slope of the ramp voltage. For this reason, the calibration resistors are chosen to with 1% and the ΔV slope is kept within 1% over the entire operating temperature range.

To reduce the size of the calibration resistor for the most sensitive detector range (0.02 μa), this calibration resistor is not returned to ground, but to a point which is at 9/10 of the ΔV voltage. This allows the use of a calibration resistor of only 1/10 the value it would normally be if it were returned to ground. Figure 15 shows the scheme.

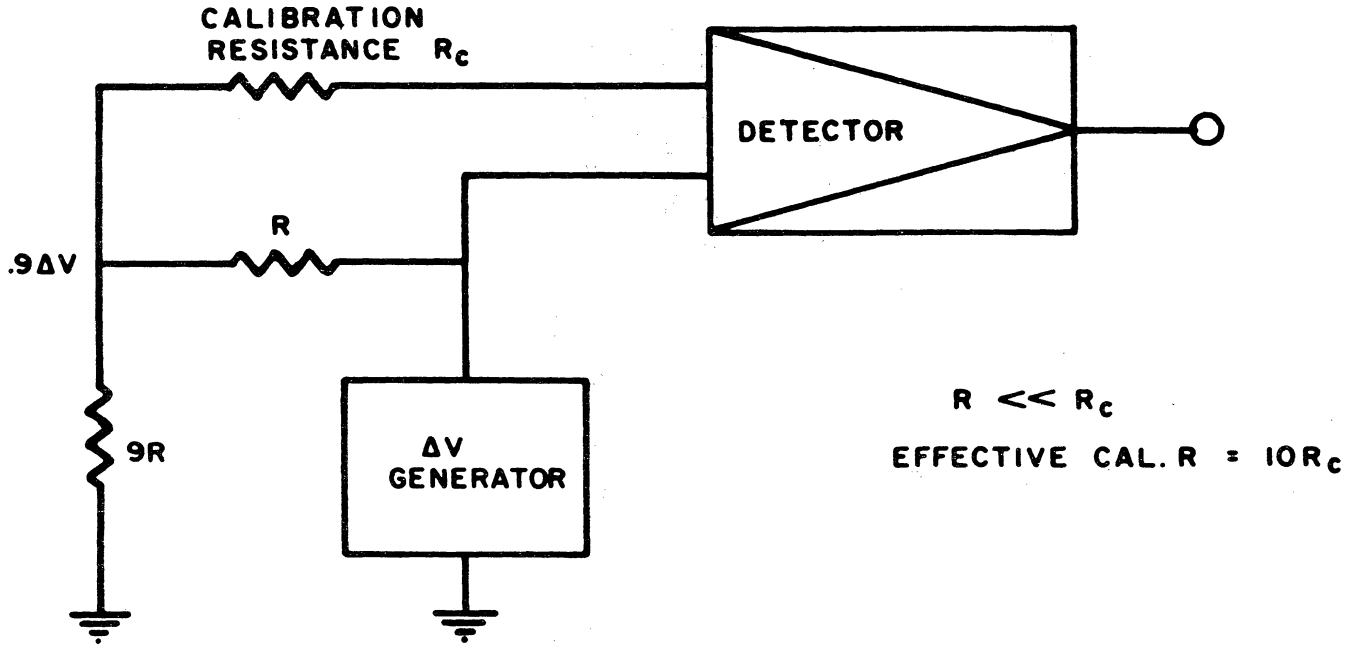

Fig. 15. Calibration scheme.

4.0 DATA CONSIDERATIONS

Due to the great amount of data obtained during the spacecraft orbital lifetime it is almost mandatory to rely on automated means of data processing. For this reason the various modes of system operation are monitored in such a manner as to lend themselves easily to computer methods of data reduction.

Three system monitor flags are brought out of the system. Flag No. 1 indicates the high or low current detection ranges. Flag No. 2 indicates which system is performing the measurement, and Flag No. 3 indicates which probe is being utilized for measurements.

If we denote the high (6 v) flag output as "1" and the low (0 v) output level as "0," the following table describes the operation of the system except for Hi-Lo ΔV changes. ΔV will change only on command and will be obvious from the data during calibrate.

Flag Output			System Operating Mode	
1 (R)	2 (D)	3 (P)	Output 1 20 & 2 μa	Output 2 0.2 & 0.02 μa
0	0	0	20 μa measure with upper probe	0.2 μa calibrate and zero reference
1	0	0	2.0 μa measure with upper probe	0.02 μa calibrate and zero reference
0	1	0	20 μa calibrate and zero reference	0.2 μa measure with upper probe
1	1	0	2.0 μa calibrate and zero reference	0.02 μa measure with upper probe
0	0	1	20 μa measure with lower probe	0.2 μa calibrate and zero reference
1	0	1	2.0 μa measure with lower probe	0.02 μa calibrate and zero reference
0	1	1	20 μa calibrate and zero reference	0.2 μa measure with lower probe
1	1	1	2.0 μa calibrate and zero reference	0.02 μa measure with lower probe

5.0 PACKAGING

To accommodate all the components necessitated in the ISIS-A mission, in an existing enclosure design, it was decided to use a high-density packaging module approach. Cordwood techniques are used for several modules with a three layer system utilized for the latching relay drivers. Figure 16 shows some of the individual modules and Fig. 17 shows the inside of the assembled package.

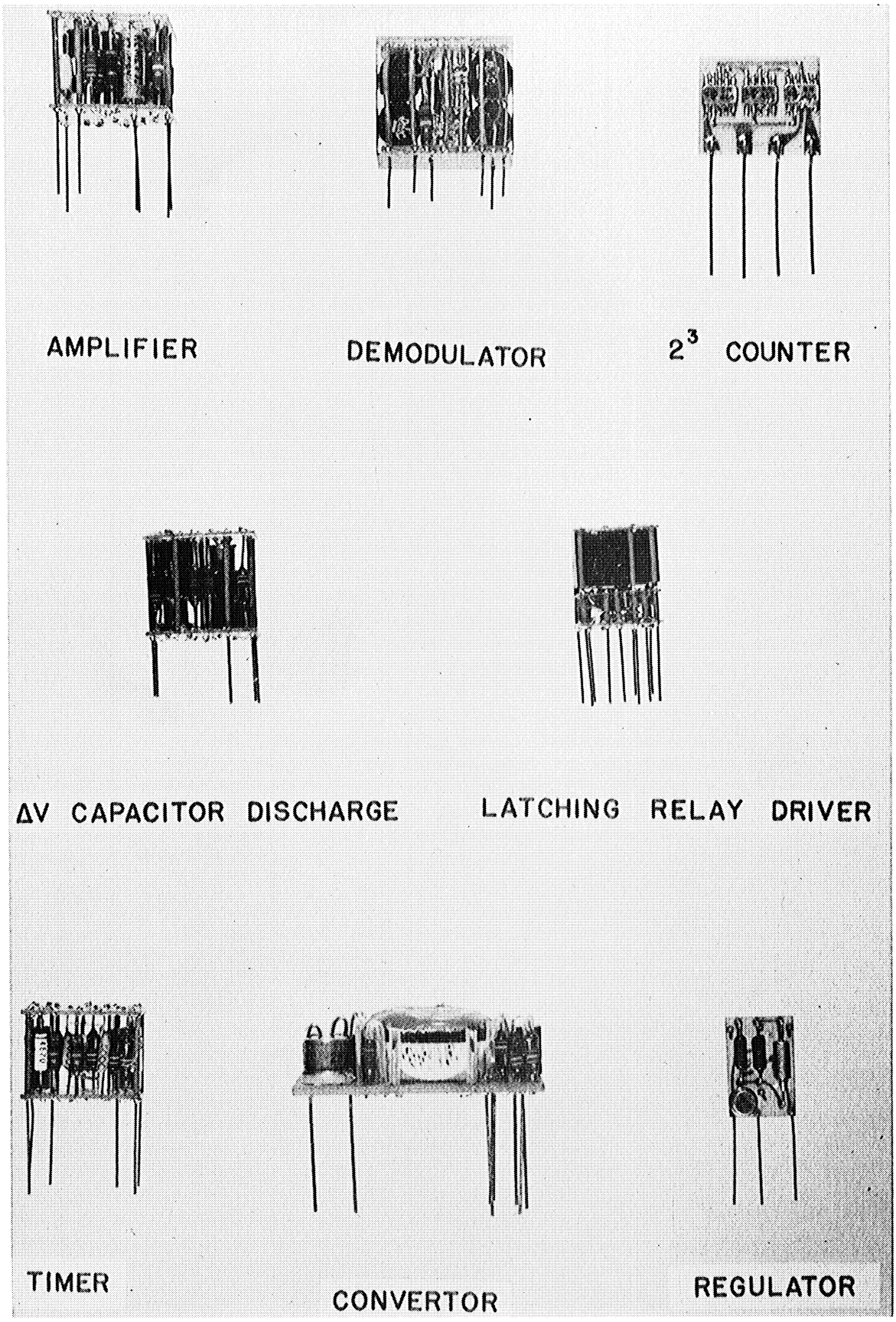

Fig. 16. Circuit modules.

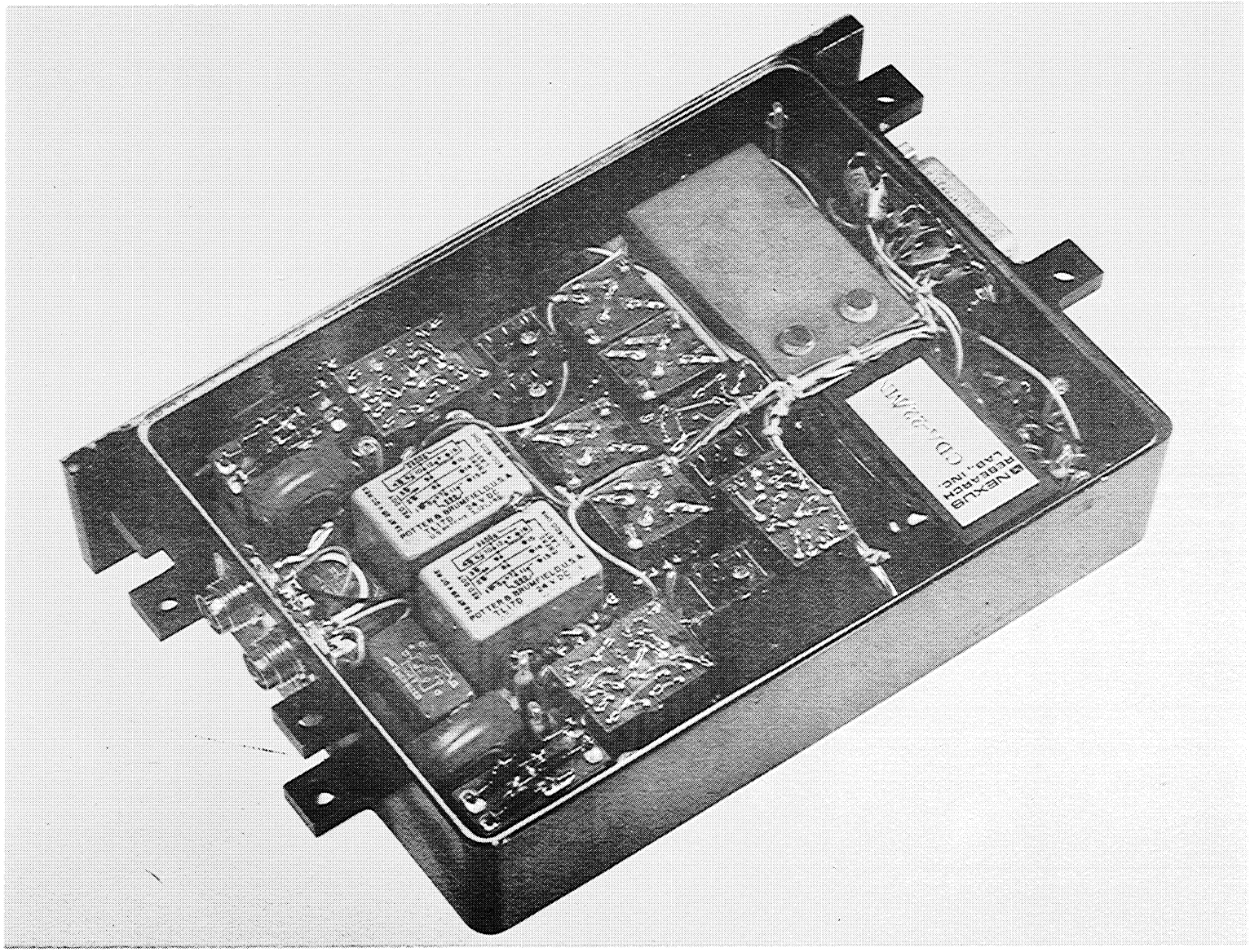

Fig. 17. Electronics package.