Adaptive Impedance Matching Circuits Based on Ferroelectric and Semiconductor Varactors

by
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CHAPTER I

Introduction

1.1 Motivation

Tunability, reconfigurability, and adaptability for radio frequency (RF) and microwave circuits are highly desirable because they not only enhance the functionality and performance but also reduce the circuit size and cost. Adaptive circuits are particularly valuable for RF front-ends in portable devices, where specifications are stringent and circuit real estate is expensive.

Modern smart-phone application is an excellent example to illustrate the benefits which adaptive circuits could bring. As shown in Figure 1.1, a smart phone usually offers wireless connectivity in addition to the typical cellular phone service. For instance, the iPhone™ 3G manufactured by Apple Inc. supports a number of wireless standards including UMTS[1], GSM[2]/EDGE[3], Wi-Fi, Bluetooth, and Assisted GPS[4]. Since specifications of the air interface vary widely from one standard to another, multiple transceiver units are usually employed in a smart phone to support multiple standards. An apparent drawback of using multiple transceivers is that it costs a significant amount of circuit board area, which is especially abominable for the

[1]Universal Mobile Telecommunications System
[2]Global System for Mobile communications
[3]Enhanced Data rates for GSM Evolution
[4]Global Positioning System

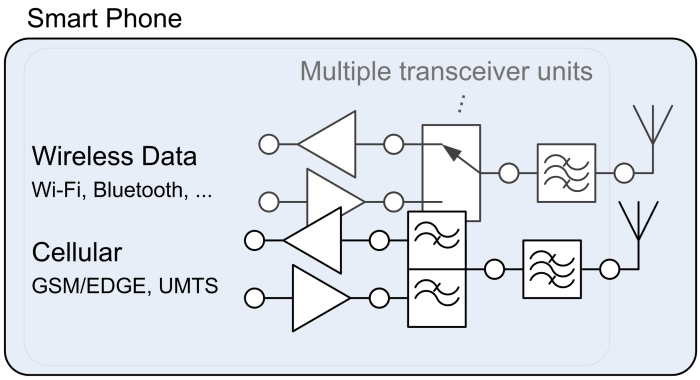


Figure 1.1: A smart phone with multiple transceiver units to provide the services specified by various wireless standards.

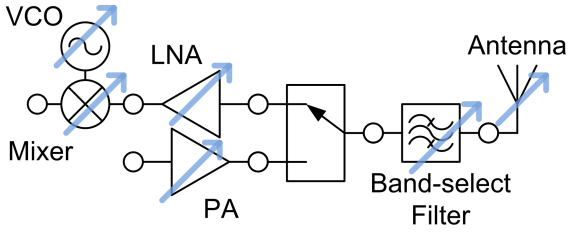


Figure 1.2: Block diagram of an adaptive RF front-end.

handset application. An alternative solution to multistandard front-end is to introduce adaptability to the RF circuits, as illustrated in Figure 1.2. Using an adaptive front-end module that supports more than one standard would considerably reduce the number of components, circuit size, and cost.

In general, RF front-end circuits can be designed to adapt to different types of operating conditions, such as frequency band, receive signal strength, transmit power level, and operating environment, which are discussed as follows.

1. *Frequency Band* – RF circuits with adaptive operating frequency is highly desirable for wireless applications. More often than not, today's wireless devices are required to possess multiband capability. For example, a wireless router supporting 802.11 a/b/g/n standards requires a front-end module that can

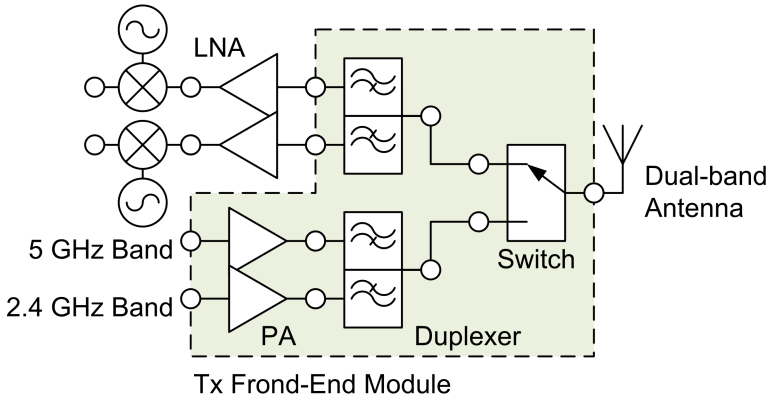


Figure 1.3: Block diagram of a typical dual-band Tx front-end module for WLAN applications.

be operated at both 2.4 and 5 GHz bands. A typical implementation of the dual-band transmitter front-end module for WLAN[5] applications utilizes two sets of transmit/receive paths and two duplexers, as shown in Figure 1.3. The complicated circuitry and multiple duplexers all add to the circuit size and cost. On the contrary, if the components are tuned such that they can work at both frequency bands, it would eliminate the need for duplexers and multiple transceiver units. Due to the tremendous benefits, the pursuit of adaptability for multiband applications has drawn vast amount of attention and research efforts [2–6].

2. *Receive Signal Strength* – For a wireless receiver, the demand on RF performance (e.g. noise figure, linearity, phase noise, and etc.) varies widely depending on the strength of the received signal. For example, the noise figure is of utmost importance when the received signal is barely perceptible, whereas the linearity becomes critical as the impinging signal is overwhelming. Thus, only when the RF front-end is adaptive to the receive signal strength can the trade-

[5]Wireless Local Area Network

offs between the RF performance and power consumption be made in real-time, which would reduce the overall power consumption and therefore extend the talk time of the handset [7], [8].

3. *Transmit Power Level* – In hand-held devices, power amplifier (PA) modules oftentimes operate at a varying power level depending on their distance to the communicating base stations. By adjusting the biasing voltage/current [9–12] or load impedance [13–15] of the PAs according to the operating power level, the overall power efficiency can be considerably improved.

4. *Operating Environment* – Compensating the variation of antenna impedance is one major application for which circuits adaptive to their operating environment are required. It is a well-known fact that the input impedance of a cell-phone antenna is sensitive to the presence of nearby objects and human bodies. Typical impedance variation resulting from holding a PIFA[6] by hand may cause 25% of the incident power to be reflected [16]. Therefore, correcting the impedance mismatch would enhance the radiating power level, improve the range of communication, and extend the talk time of the mobile devices. In addition, since PAs are sensitive to their load impedance, which is often the input impedance of the antenna if no isolator is used in between, correcting for the mismatch also preserves the performance of PAs and prevents potential damages caused by excessive power reflections [17], [16].

Specifically, this thesis studies impedance matching circuits that are adaptive to either transmit power level or operating environment, aiming at the realization of high performance intelligent RF front-ends. The study is divided into two dis-

[6]Planar Inverted-F Antenna

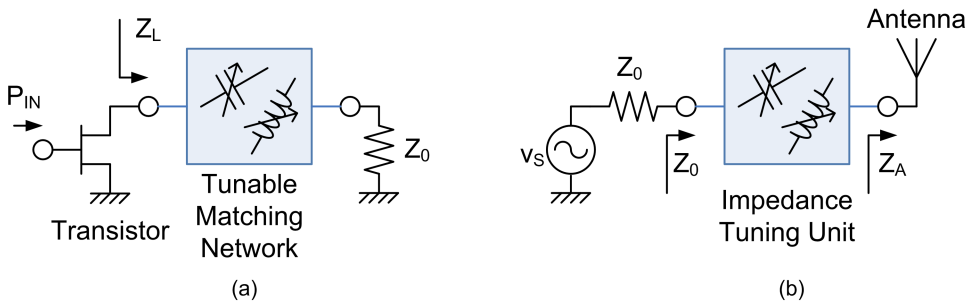


Figure 1.4: Applications of the adaptive impedance matching circuits studied in this work: (a) tunable matching networks for PA efficiency enhancement and linearity improvement, and (b) impedance tuning units for automatically compensating the input impedance variation of an antenna.

tinct topics: (a) linear and efficient PAs using tunable matching networks that are dynamically controlled according to the input power level, and (b) adaptive matching systems based on impedance tuning units to automatically compensate the input impedance variation of an antenna, as depicted in Figure 1.4(a) and (b), respectively.

1.2 Varactor Technologies

Tuning elements are indispensable building blocks for adaptive impedance matching circuits. Electronically controllable varactors are most practical and convenient tuning elements for providing tunability in RF/microwave circuits. Current varactor technologies fall into three major categories: semiconductor-based varactor diodes, microelectromechanical system (MEMS) varactors, and ferroelectric-based varactors. Performance comparison of the three varactor technologies is summarized in Table 1.1 [18], [19].

Conventionally, reverse-biased diodes have been used as varactors. Varactor diodes are intrinsically fast and compatible with integrated circuit process. However, they are lossy and nonlinear. Furthermore, the possibility of being driven into

Table 1.1: Comparison of Varactor Technologies

	Semiconductor-based	MEMS	Ferroelectric-based
Tunability	high	low	medium
Quality Factor	medium	high	medium
Bias Voltage	medium	high	medium
Tuning Speed	fast	slow	fast
Power Handling	low	medium	high
Linearity	can be improved [20]	high	can be improved [21]

forward-biased region under large RF swing makes it unattractive to use varactor diodes for high power design.

MEMS varactors have been widely used by researchers for tunable RF circuit design. MEMS components have the advantages of having low loss and high linearity; nevertheless, they also have a number of serious drawbacks, including high bias voltage requirements, low power handling capability, slow tuning speed, as well as costly packaging requirements.

Thin-film ferroelectric capacitors, on the other hand, require relatively low bias voltage, exhibit high power handling capability, are intrinsically fast, and can be fabricated at low cost. Currently, the quality factor of the thin-film ferroelectric capacitors is comparable to that of varactor diodes. Research work is underway to further improve their quality factor. Finally, despite the fact that ferroelectric materials are intrinsically nonlinear, a linearity-improving technique based on properly designing the device architecture has been proposed and proven to be effective, though at the cost of quality factor and tuning speed [21]. The same technique has later been applied to varactor diodes and proven to enhance their linearity as well [20].

In this thesis, both semiconductor-based and ferroelectric-based varactors are used as tuning elements for the adaptive impedance matching circuits. Specifically,

the ferroelectric capacitors are based on barium strontium titanate ($Ba_xSr_{1-x}TiO_3$, abbreviated BST) technology developed in the University of Michigan at Ann Arbor.

1.3 Thesis Overview

This thesis covers the design and implementation of adaptive impedance matching circuits for RF front-ends with applications in the design of PAs and antenna tuning units (ATUs). The tuning elements used in this work include both semiconductor and ferroelectric varactors. To use intrinsically nonlinear ferroelectric materials for wireless front-end applications, which usually have stringent linearity requirements, a technique for improving the linearity of the ferroelectric varactors is also discussed. The overview of the thesis work are described as follows.

1. *A Linearity-Improving Technique for Ferroelectric Varactors* – The linearity of ferroelectric capacitors is significantly improved using a circuit-oriented approach, as opposed to material-oriented approaches. The linearity-improving technique is fully analyzed to quantify the tradeoffs between the quality factor and tuning speed of the linearized varactors. The technique is applied to parallel-plate BST capacitors. Up to 16 dB improvement on third-order intercept point at input (IIP_3) is achieved. Hot tuning measurements show that the BST capacitors experience no tunability degradation at RF voltage swings as high as 20 V.

2. *A Tunable Matching Network for Power Amplifier Efficiency and Linearity Improvement* – Variable load technique based on tunable matching networks has been used previously to enhance the power efficiency of PAs at reduced drive levels. However, most of the tunable matching networks often degrade

the linearity of the PAs by introducing AM-PM distortions when they are dynamically tuned. In this thesis, a suitable topology for the tunable matching network is chosen to prevent the introduction of AM-PM distortions and the subsequent linearity degradation. Moreover, for the first time, it is demonstrated that both the efficiency and linearity of PAs can be improved using tunable matching networks that are dynamically controlled according to the instantaneous power level.

3. *An Impedance Tuner and Its Application in an Adaptive Matching System* – A general-purpose impedance tuner is proposed. The impedance tuner is designed based on all-pass networks and implemented using ferroelectric varactors. An adaptive matching system based on the impedance tuner is proposed for the application of automatically compensating the impedance variation of an antenna. The loop dynamics of the adaptive matching system is analyzed and simulated.

The thesis is organized as follows. The linearity-improving technique for ferroelectric capacitors is detailed in Chapter II. Next, Chapter III is devoted to the demonstration of improving PA efficiency and linearity using a dynamically controlled tunable matching network. Following that in Chapter IV, a ferroelectric-based impedance tuner is designed, fabricated, and measured whereas an adaptive matching system is proposed, analyzed and simulated. Finally, the thesis is summarized and future directions are given in Chapter V.

CHAPTER II

A Linearity-Improving Technique for Ferroelectric Varactors

2.1 Introduction

Varactors are essential components in tunable microwave circuits. Ferroelectric materials, which allow for their permittivity being adjusted by application of an electric field, are legitimate candidates for varactors. Among them, barium strontium titanate (BST) has been used in various microwave circuits, such as filters, phase shifters, and matching networks, to provide the benefit of tunability [6, 22–27].

Compared to MEMS varactors, thin-film BST capacitors exhibit a higher tuning ratio under relatively low bias voltages. However, due to the inherent nonlinear nature of the ferroelectric materials, linearity has been a concern, especially for high power applications and spectrally-packed communication systems.

Linearity improvement of ferroelectric capacitors can be achieved through proper design of the device architecture, rather than modifying the ferroelectric material. While previous researchers have proven the effectiveness of architectural approaches for improving the linearity of gap capacitors [28], in this work, a simple method to reduce the nonlinearity of parallel plate capacitors is suggested. The same technique has also been proposed in [29], [1] and [30], and later applied to semiconductor-

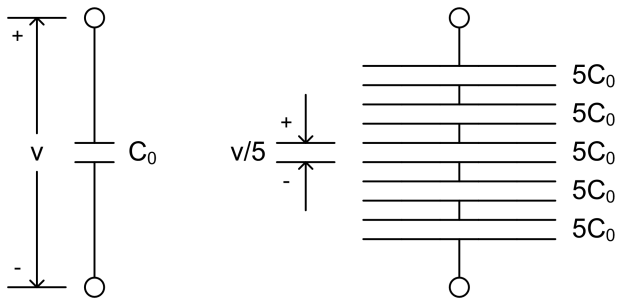


Figure 2.1: Basic concept underlying the proposed technique illustrated by a 5-stacked capacitor example (from [1]).

based varactor diodes as well [20]. The major contribution of this work is to present an analysis of the technique for studying the tradeoffs and optimization of BST varactor-based circuits for wireless communication applications.

The basic concept underlying the linearity-improving technique is illustrated in Figure 2.1. As the RF swing across the varactor increases, the capacitance of the varactor starts to deviate from the value set by the DC bias voltage, resulting in signal distortion. Connecting a number of identical capacitors in series readily reduces the RF swing across each capacitor, which in turns lessens the variation of the total capacitance, thus improving the linearity. Using an N-stacked capacitor reduces the voltage swing across each element to $1/N$ of the original swing. To maintain the same capacitance as that of a single capacitor, each element should be N times as large. As a result, the area of an N-stacked capacitor would be N^2 times as large as that of a single capacitor having the same capacitance value. Though the quadratic increase of the occupied area seems disadvantageous, the size of multiple-stacked capacitors is still compact because of the high permittivity of the BST thin film.

In this chapter, a device architecture for improving the linearity of parallel-plate BST capacitors based on the aforementioned concept is proposed and experimentally demonstrated. The details of the architecture and the circuit analysis are presented

in Section 2.2. Following that, the design considerations are summarized in Section 2.3. Next, in Section 2.4, the fabrication process is described and measurement results are shown and discussed. Finally, conclusions are provided in Section 2.5.

2.2 Device Architecture and Analysis

The device architecture is illustrated in Figure 2.2(a) with a 5-stacked example. Five capacitors are connected in series through top and bottom electrodes alternatively. Thin-film resistors link together top or bottom electrodes respectively to ensure that the bias voltage is applied to each capacitor equally. Figure 2.2(b) shows the schematic of the device architecture.

Adding bias resistors preserves the tunability but inevitably degrades the tuning speed and the quality factor. Large bias resistances increase the time constant, thus, reducing the tuning speed, while small resistances result in higher loss, lowering the quality factor. To analyze the overall performance of the proposed architecture and to quantitatively determine the effects of the resistance, the circuit schematic is rearranged, as shown in Figure 2.2(c).

As can be seen in Figure 2.2(c), a composite capacitor with five elements can be viewed as a single capacitor at the center connected to two 4-port RC stages in cascade. In general, this viewpoint applies to any composite capacitor with an odd number of elements. That is,

$$N = 2n + 1; \qquad n = 1, 2, \ldots \tag{2.1}$$

In (2.1), N is the number of elements and n can be any positive integer. In this sense, an N-staked capacitor with odd number of elements can then be viewed as a single capacitor with n cascaded RC stages. It is helpful to describe such a ladder network

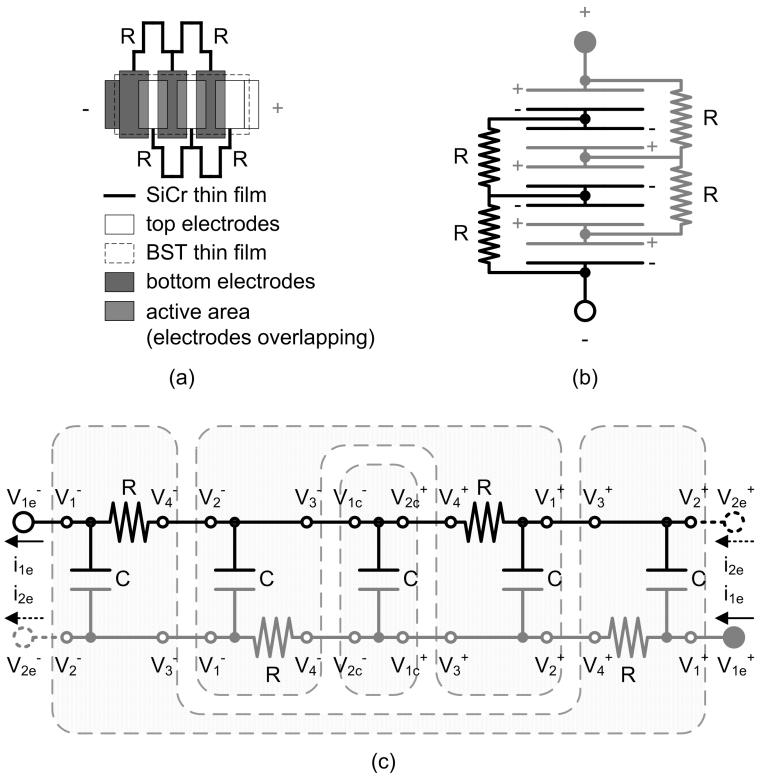


Figure 2.2: A 5-stacked example for the proposed device architecture: (a) simplified layout, (b) schematic illustration, and (c) rearranged schematic for analysis.

with a 4-port matrix that is similar to the $ABCD$ matrix for a 2-port network, as in

$$\begin{pmatrix} 0 & 1 & 0 & 2Z \\ 1 & 0 & 0 & 0 \\ -Y/2 & Y/2 & 0 & 1+YZ \\ Y/2 & -Y/2 & 1 & -YZ \end{pmatrix} \begin{pmatrix} v_3 \\ v_4 \\ -i_3 \\ -i_4 \end{pmatrix} = \begin{pmatrix} v_1 \\ v_2 \\ i_1 \\ i_2 \end{pmatrix}, \tag{2.2}$$

where, in this case, $Z = R$ and $Y = j\omega C$. On the other hand, the center capacitor is considered as a 2-port network, where the voltages across and currents flowing through its terminals have the following relationship:

$$\begin{pmatrix} v_{2c} \\ i_{2c} \end{pmatrix} = \begin{pmatrix} -1 & 0 \\ -Y & 1 \end{pmatrix} \begin{pmatrix} v_{1c} \\ i_{1c} \end{pmatrix}. \tag{2.3}$$

The direction of currents is flowing into the positive terminals.

Using (2.1), (2.2), and (2.3), a N-staked capacitor can then be described by

$$\begin{pmatrix} 0 & 1 & 0 & 2Z \\ 1 & 0 & 0 & 0 \\ -Y/2 & Y/2 & 0 & 1+YZ \\ Y/2 & -Y/2 & 1 & -YZ \end{pmatrix}^n \begin{pmatrix} v_{1c} \\ -v_{1c} \\ i_{1c} \\ -Yv_{1c} + i_{1c} \end{pmatrix} = \begin{pmatrix} v_{1e} \\ v_{2e} \\ i_{1e} \\ i_{2e} \end{pmatrix}. \tag{2.4}$$

By applying the boundary condition $i_{2e} = 0$, since the corresponding port is open, one can solve (2.4) and obtain the relations between the voltages and currents. We define

$$a_N \equiv v_{1c}/v_{1e} \tag{2.5}$$

and

$$Y_N \equiv i_{1c}/v_{1e}, \tag{2.6}$$

where a_N is the voltage transfer ratio between the voltage across a single capacitive unit and the voltage across the entire composite capacitor, and Y_N is the overall

admittance of the composite capacitor with N capacitive units. For $N = 3$, 5, 7, and 9, a_N and Y_N are solved and are listed in Appendix A. The results have also been verified by simulations.

It will be shown that the expressions for the tuning speed and the quality factor of the N-stacked capacitor are related to a_N in (2.5) and Y_N in (2.6), respectively. Before going through the derivation, the capacitance value of each capacitor in an N-stacked capacitor can be first determined. Since there are N capacitors in series, for the overall capacitance being the same as that of the single capacitor, the capacitance of each capacitor must be N times as large, i.e.

$$C = NC_0 = (2n+1)C_0, \tag{2.7}$$

where C_0 is the capacitance of the single capacitor before scaling.

To derive the expression for the tuning speed, the asymptotic response of a_N at lower end of the frequency spectrum,

$$a_N \approx \frac{1}{1 + j\omega\frac{3n(n+1)}{2}RC}, \quad \text{for} \quad \omega \ll \frac{1}{RC}, \tag{2.8}$$

is examined. Note that (2.8) is the same as the response of a series RC circuit, which has a time constant

$$\tau_N = \frac{3n(n+1)}{2}RC = \frac{3n(n+1)(2n+1)}{2}RC_0. \tag{2.9}$$

Next, to obtain the expression of the quality factor, at high frequency, the overall admittance of the composite capacitor can be simplified to

$$Y_N \approx Y\frac{(2n+1) + YZ}{(2n-1)^2 + (2n+1)YZ}, \quad \text{for} \quad |YZ| \gg n-1. \tag{2.10}$$

In this case, $Z = R$ and

$$Y = G + j\omega C = j\omega C(1 - j\frac{1}{Q}), \tag{2.11}$$

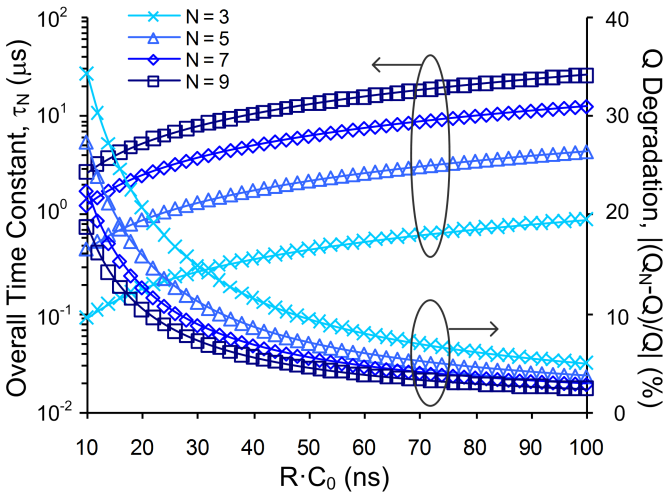


Figure 2.3: Tradeoff between tuning speed and quality factor illustrated by potting time constant (2.9) and degradation of quality factor (2.12) versus design parameters. R is the bias resistance, while C_0 is the capacitance of the single capacitor before scaling. In this example, $Q = 50$ and the frequency is 1.3 GHz.

where G is the effective parallel conductance and Q is the quality factor of the capacitive unit at the frequency of interest, ω. Q is a function of the dielectric loss of the ferroelectric thin-film and the conductor loss of the electrodes. Using (2.10), along with (2.7) and (2.11), one can show that the quality factor of the composite capacitor with finite bias resistance R is

$$Q_N = \frac{\mathrm{Im}(Y_N)}{\mathrm{Re}(Y_N)} \approx Q\left(1 + \frac{Q}{\omega R C_0}\left(1 - \left(\frac{2n-1}{2n+1}\right)^2\right)\right)^{-1}. \tag{2.12}$$

Equations (2.9) and (2.12) quantitatively show the tradeoff between the tuning speed and the quality factor. This tradeoff is illustrated in Figure 2.3, where the quality factor degradation and the time constant are plotted versus RC_0 for composite capacitors with various N's. In this example, the quality factor of the single capacitor, Q, is assumed to be 50, and the frequency is 1.3 GHz.

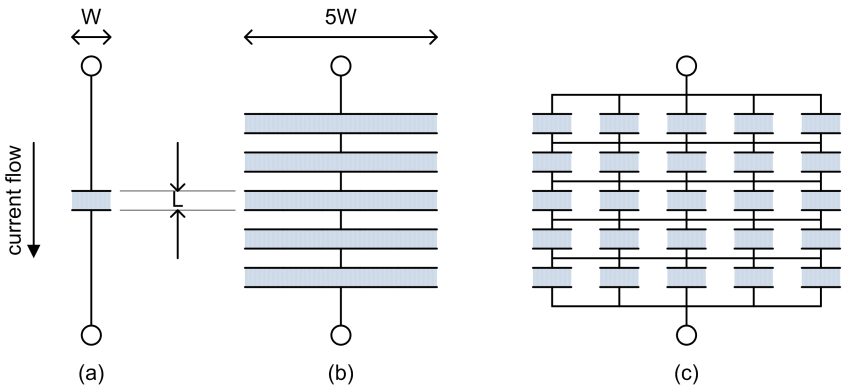


Figure 2.4: Proper scaling for preserving quality factor: (a) original single capacitor, (b) stacked capacitor, and (c) an equivalent array perspective.

2.3 Design Considerations

2.3.1 Quality Factor

Quality factor can be maintained through proper scaling. For an N-stacked capacitor, each capacitive element is N times as large as the single capacitor. Scaling the capacitive element by N times along the direction perpendicular to the current flow, as shown in Figure 2.4(b), would reduce the loss per unit element. This would cancel the loss increase introduced by the series connection of multiple elements. Figure 2.4(c) presents an alternative perspective for the proposed architecture as an N-by-N array of capacitors, in which each unit has the value of the single capacitor before scaling as in Figure 2.4(a). The array perspective is helpful in explaining the preservation of the quality factor. Since neither series nor parallel combination of identical capacitors affects the quality factor, an array, which is basically the series combination of parallel combinations (or *vice versa*), would have the same quality factor as that of each building block.

Properly scaling the physical dimensions of the capacitive units could preserve the quality factor. However, the bias resistors of the N-stacked capacitor would in-

evitably introduce losses, lowering the quality factor of the composite capacitor. In general, as R becomes larger, the RF current through the resistors decreases, which lessens the deleterious effect of the bias networks on the quality factor.

2.3.2 Tuning Speed

As the number of elements increases and the capacitance of each element is scaled up, the tuning speed of the stacked capacitor would decrease if the resistance of the bias resistors is not scaled down accordingly. As derived from the previous analysis, to maintain the tuning speed, the resistance may be scaled according to (2.9). Although the tuning speed can be maintained through reducing R when N is increased, the RF performance, such as quality factor, would be degraded if R becomes excessively small.

2.3.3 Number of Elements

The number of elements, N, should be determined based on requirements such as linearity, tuning speed, quality factor, and device area. The linearity is improved as N increases because of the reduced RF swing across each element, while it is beneficial to have lower N for applications requiring fast tuning. The device area expands quadratically with N, which seems to be a disadvantage. However, in some occasions, it is necessary to connect capacitors in series in order to obtain small capacitance on the high-permittivity BST.

2.4 Fabrication and Measurement

2.4.1 Fabrication Process

The BST capacitors are fabricated on 430-μm-thick sapphire substrate. The substrate has a dielectric constant of 9.39 as the electric field is perpendicular to its C-axis. The bottom electrodes composed of Ti/Au/Pt (20/2000/1000 Å) are deposited first. BST thin-film is then deposited using Pulse Laser Deposition (PLD) technique with a 50/50 BST target (i.e. $Ba_{0.5}Sr_{0.5}TiO_3$). The measured film thickness is 400 nm. The top electrodes composed of Pt/Au (1000/2000 Å) are then deposited. Subsequently, BST thin-film is etched in the regions other than the parallel-plate capacitor area.

Thin-film SiCr lines with thickness of 100 nm are then deposited by sputtering. Following that, the metal contacts composed of Cr/Au (200/500 Å) are formed to connect the bias resistors to the electrodes and serve as the bottom electrodes of the metal-insulator-metal (MIM) capacitors in other regions. Silicon nitride (Si_3N_4) thin-film, serving as the dielectric layer in the MIM capacitors and also the passivation for the BST capacitors, is deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD) technique. The measured film thickness is 1300 Å. Finally, the other metal traces are electroplated with gold to approximately 8 μm.

The photograph of a 5-stacked capacitor is shown in Figure 2.5. The device area of this capacitor is 350×160 μm^2, including the bias resistors and the passivation layer. The capacitance of it is approximately 1.4 pF at zero bias.

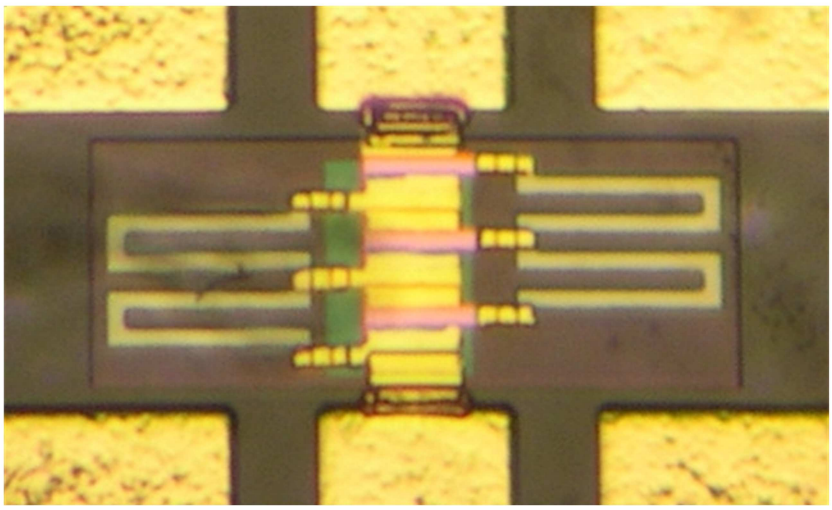


Figure 2.5: Photograph of a 5-stacked capacitor. Device area: $350 \times 160\ \mu m^2$.

2.4.2 Capacitance and Quality Factor

Small-signal scattering parameters of the BST capacitors are measured using a network analyzer (Agilent E8364B). On wafer measurement is performed. The scattering parameters are converted to $ABCD$ parameters for the ease of the post-processing. The capacitance is obtained from $\mathrm{Im}(B)$, while the total quality factor is calculated directly by $|\mathrm{Im}(B)/\mathrm{Re}(B)|$.

The capacitances and the quality factors at various bias points for $N = 1$, 3, 5, 7, and 9 are plotted in Figure 2.6. This set of the capacitors provides 2:1 tuning ratio at approximately 10 V. As can be seen, the capacitances for different N's are almost the same except for $N = 1$, where the capacitance is less than that of the multiple-stacked capacitors by approximately 7%. This difference could result from the additional parasitic capacitance that arises from the horizontal gaps between the electrodes of the multiple-stacked capacitors. The quality factors of the stacked capacitors are less than that of the single capacitor. This is due to the loss introduced

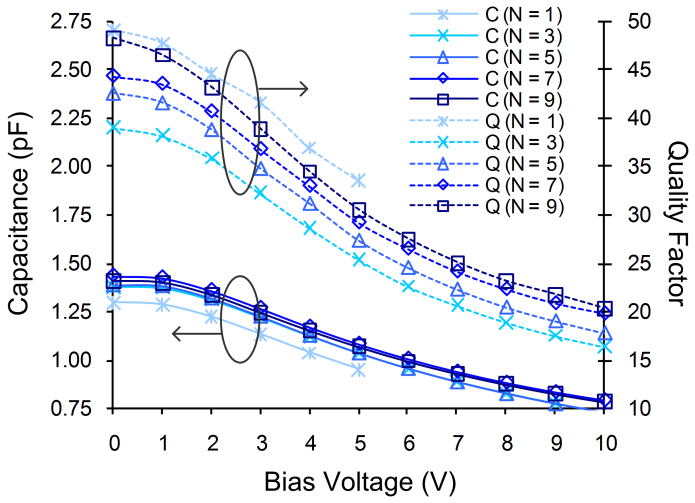


Figure 2.6: Measured capacitances and quality factors (at 1.3 GHz) of the BST capacitor with different numbers of element under various bias voltages.

by the bias resistors, as explained in Section 2.2 and estimated by (2.12). The measured resistance of the bias resistor is 12 kΩ in all capacitors. Since the resistance is not scaled down but remains constant for the stacked capacitors measured, the quality factor degrades less as the number of elements increases. Figure 2.7 shows the comparison between the measured quality factors and those predicted by (2.12) based on the measured quality factor of the single capacitor at various bias voltage. The observed quality factors deviate from the estimated ones by less than 12%.

2.4.3 Tuning Speed

The measurement setup for measuring the tuning speed of the N-stacked BST capacitors is shown in Figure 2.8. An 1-kHz square wave with low and high voltages being 0 and 3 V, respectively, is used as the input signal. The output is connected to an 1-kΩ load and monitored using an oscilloscope.

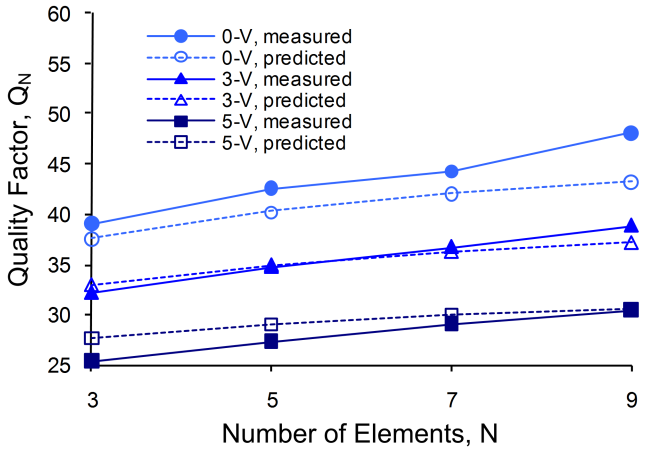


Figure 2.7: Measured (solid) and predicted (dash) quality factors for capacitors with $N = 3$, 5, 7, and 9 at various bias voltages.

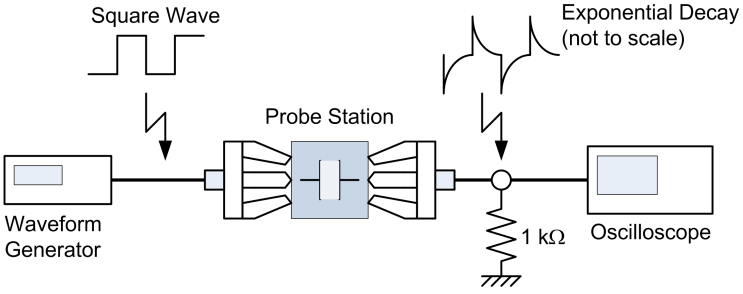


Figure 2.8: Measurement setup for the tuning speed of the stacked BST capacitors

The output waveform $v_O(t)$ decays exponentially and is of the form

$$v_O(t) = a \cdot e^{-t/\tau} + b, \tag{2.13}$$

where a and b are constants and τ is the time constant of the overall circuit, which includes not only the device under test (i.e. the N-stacked BST capacitor) but also the 1-kΩ load. However, since the 1-kΩ load is much smaller than the bias resistance of the N-stacked BST capacitor, its contribution to the time constant is basically negligible.

After the output waveform $v_O(t)$ is measured, one can calculate the time constant τ by the following equation:

$$\tau = \frac{t_2 - t_1}{\ln\left(\frac{v_O(t_1) - v_O(t_1+\Delta t)}{v_O(t_2) - v_O(t_2+\Delta t)}\right)}, \tag{2.14}$$

where t_1 and t_2 are two arbitrary but different time instants and Δt is an arbitrary nonzero time delay.

Figure 2.9 shows the comparison between the measured time constants and the estimated values by (2.9). The capacitance at 3-V bias is used in these calculations. As can be seen, the difference between the measurement and estimation increases along with N, which may be due to the parasitic elements, such as the effective resistance resulted from the leaking current in the BST thin-film, that are not included in the simple model presented above.

2.4.4 Intermodulation Distortion

As a measure of linearity, the third-order intercept point at input (IIP_3) is measured. The measurement setup is shown in Figure 2.10. It consists of two signal generators, two power amplifiers, two isolators, a power combiner, a probe station,

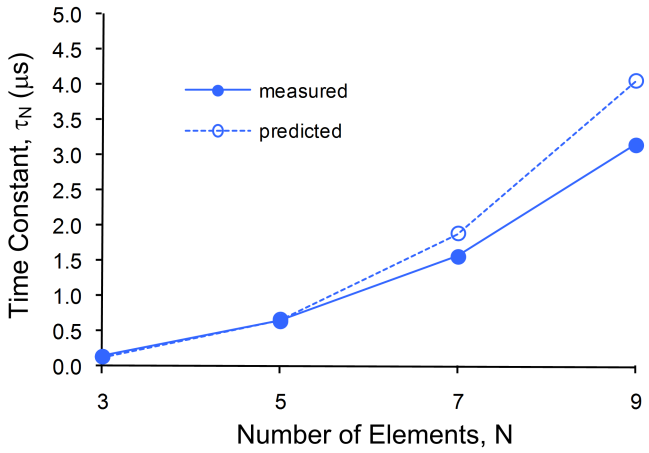


Figure 2.9: Measured (solid) and predicted (dash) time constants for capacitors with $N = 3$, 5, 7, and 9.

an attenuator, a spectrum analyzer, and two bias-tees. The power amplifiers are used to increase the input power level so that it is large enough for the BST varactors to produce high enough intermodulation products over the noise floor of the spectrum analyzer. The isolators are used to protect the power amplifiers from any reflected power and prevent possible leak-through from one signal generator to another. The attenuator is placed before the spectrum analyzer to reduce the output power level, reducing the internal intermodulation generated by the spectrum analyzer, which could otherwise mask the intermodulation tones of interest.

Two-tone signals with center frequency and frequency spacing of 1.3 GHz and 1 MHz are used. The frequency 1.3 GHz is chosen because it is the center frequency of the isolators used in the measurement setup. The measured IIP_3 for capacitors with various numbers of elements is shown in Figure 2.11. At zero bias, an IIP_3 improvement of up to 16 dB is obtained. The IIP_3 of the 5-stacked case at 3-V bias is not measured because the intermodulation products are too small to be measured by the spectrum analyzer used in this experiment.

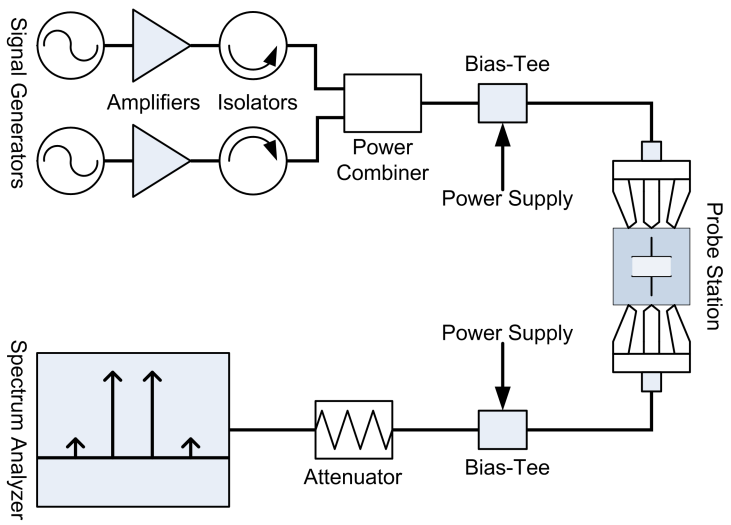


Figure 2.10: Setup for meauring the IIP_3 of the BST varactors.

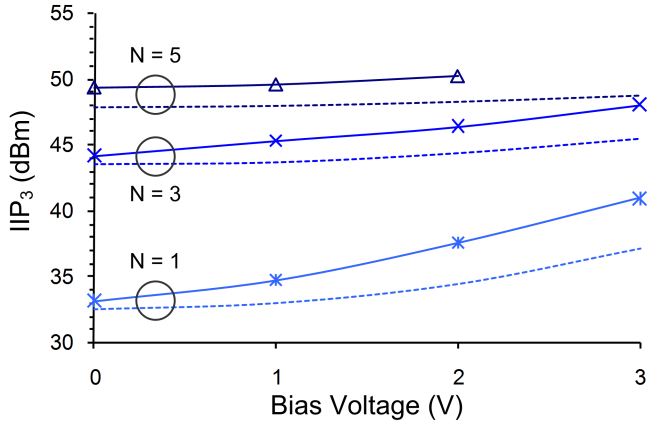


Figure 2.11: Simulated (dash) and measured (solid) IIP_3 for $N = 1, 3,$ and 5 at various bias voltages, where N is the number of stacked capacitors.

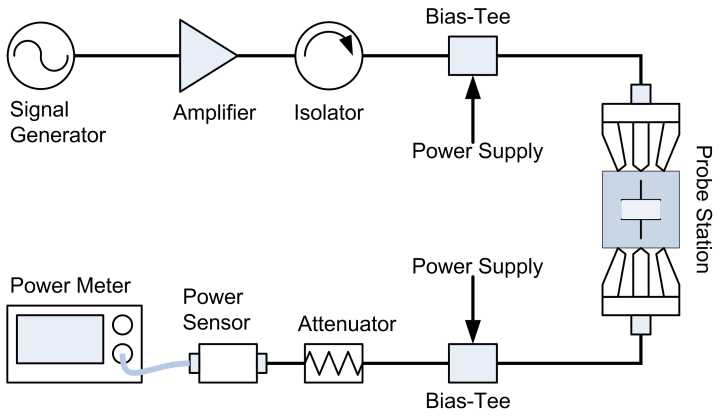


Figure 2.12: Setup for hot tuning measurement.

The simulated IIP_3 is also shown in Figure 2.11 for comparison. While the results from the analysis in Section 2.2 are useful for linear circuits, the time-domain counterparts of (2.2) and (2.3) are used to describe the cascaded RC stage and the center capacitor, respectively, for nonlinear simulations. The C-V curve of BST varactors is modelled using the expression derived in [31].

2.4.5 Hot Tuning

One manifestation of varactor nonlinearity is its variation of capacitance with the RF amplitude across it. Tunability degradation of BST varactors under large signal excitation has been presented at low frequency in [32]. In this work, hot tuning measurements (i.e. measuring the capacitance at various input power levels) are performed at 1.3 GHz on the stacked BST capacitors with $N = 1$, 3, and 5. As shown in Figure 2.12, the setup for the hot tuning characterization included a power amplifier to increase the input power level, an isolator to present impedance match to the amplifier, and a power meter to measure the output power with high resolution.

The method used here for the hot tuning characterization is similar to that described in [33]. The first step is to record the power meter readings at low input power level at various bias voltages. Next, the difference between the power meter readings and input power level (i.e. the insertion loss of the circuitry between the signal generator and the power sensor) is calculated and related with the capacitance values at corresponding bias voltages, which are already known from the small-signal measurement results using the network analyzer as described in Section 2.4.2. The outcome is an one-to-one mapping from the insertion loss to the capacitance value. From then on, one can obtain the capacitance value by measuring the insertion loss between the signal generator and the power sensor.

Under various RF input power levels and biased at different voltages, the stacked BST varactors with $N = 1$, 3, and 5 are tested and the power meter readings are recorded. The insertion losses are calculated and the corresponding capacitances are obtained from the established one-to-one mapping described above. The obtained capacitances are then normalized to the capacitance of the varactor biased at 0 V under the lowest input power level in order to manifests the relative change in capacitance that occurs as the input power level varies. The normalized capacitances of the BST varactors under test are shown in Figure 2.13. The input power level is swept from 0 to 28 dBm. Through circuit simulation, it can be found that the 28 dBm input power would result in 20-V peak-to-peak swing across a 1.4-pF capacitor at 1.3 GHz. As can be seen in Figure 2.13, at zero bias, the capacitance of the single capacitor drops by 20% as RF voltage swing increases, whereas, for $N = 3$ and 5, the capacitance hardly varies with the RF swing. Also, One can see that, under large signal excitation, the tunability of the stacked capacitors is much less degraded than that of the single capacitor.

2.4.6 Phase Shifter Using Linearity-Improved BST Varactors

A phase shifter is designed based on all-pass network [34], [35]. Stacked BST varactors with $N = 5$ are used in the phase shifter. The photograph of the fabricated circuit is shown in Figure 2.14(a).

Due to fabrication errors, the inductances of the spiral inductors deviate from the designed values. After replacing part of the inductors with bond-wires to adjust the inductance, the phase shifter is measured. Its small-signal response at 2.4 GHz is shown in Figure 2.14(b). The insertion loss was less than 2 dB and the input and output return losses were greater than 10 dB. The relative phase shift over 0 to 25-V bias voltages is approximately 90°.

The center frequency and frequency spacing of the two-tone signals for measuring the intermodulation distortion of the phase shifter are 2.4 GHz and 1 MHz, respectively. The IIP_3 observed is greater than 40 dBm.

2.5 Conclusions

A technique is proposed to improve the linearity of thin-film parallel-plate BST capacitors. The technique is analyzed to provide design equations relating to the quality factor and the tuning speed of the linearity-improved varactors. The linearity improvement provided by this approach is demonstrated by IIP_3 and hot tuning measurements. A phase shifter employing BST capacitors using the proposed technique is designed and fabricated. The good linearity presented by the phase shifter demonstrates the usefulness of this technique for tunable microwave circuits in practice.

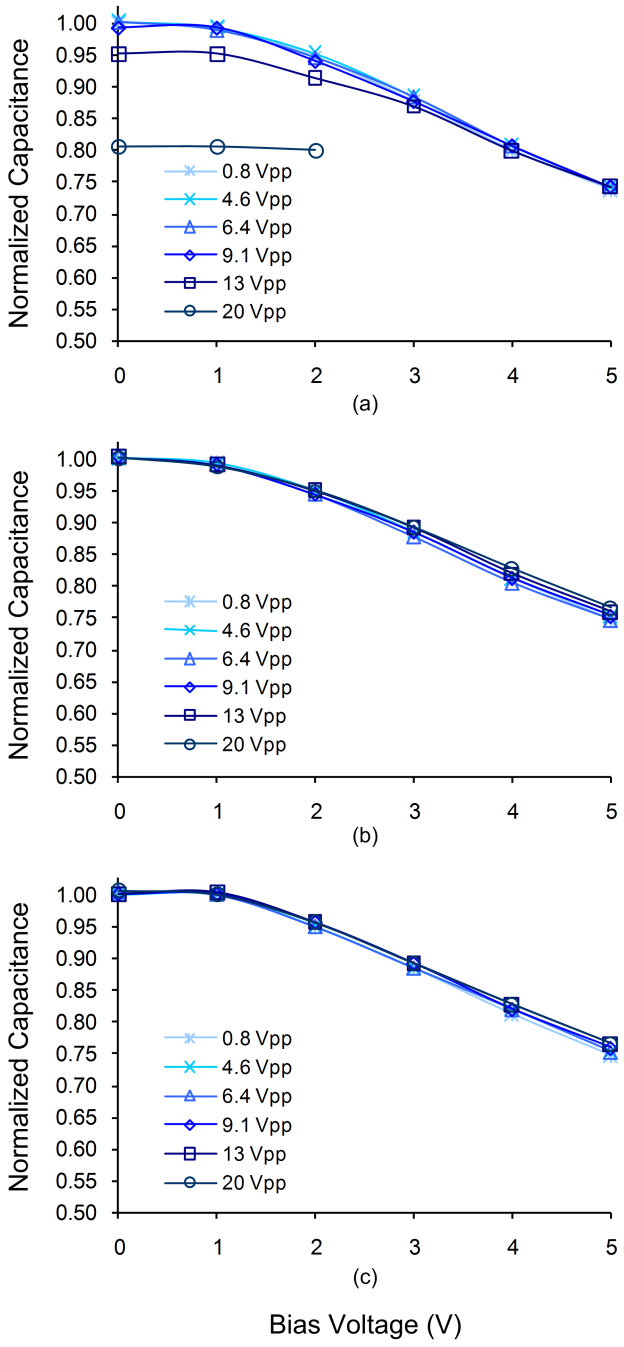
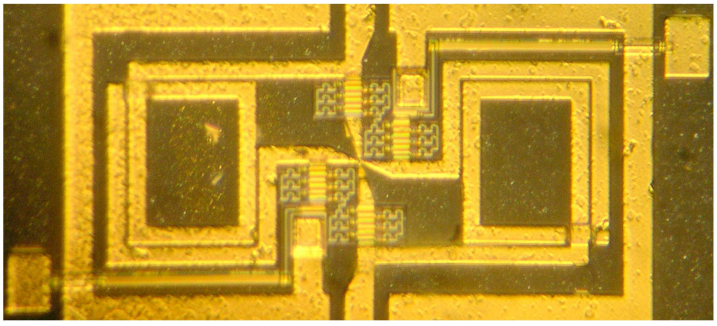
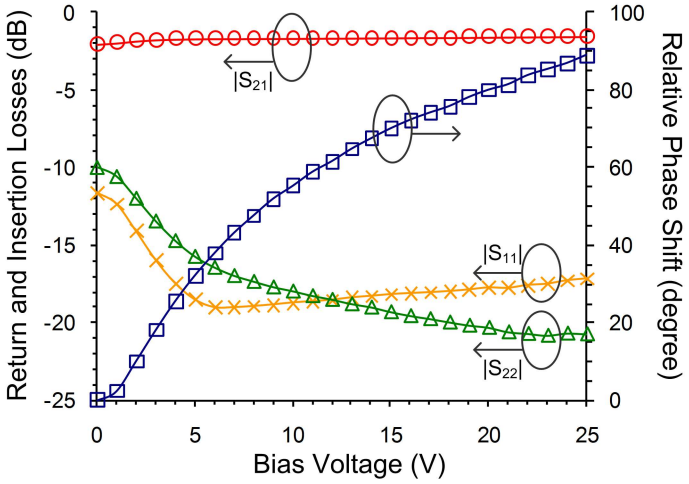


Figure 2.13: Hot tuning measurement: capacitance normalized to zero-bias capacitance for (a) $N = 1$, (b) $N = 3$, and (c) $N = 5$ under different input power at various bias voltages.



(a)



(b)

Figure 2.14: Phase shifter: (a) photograph and (b) small-signal response at 2.4 GHz.

CHAPTER III

A Tunable Matching Network for Power Amplifier Efficiency and Linearity Improvement

3.1 Introduction

Power amplifiers (PAs) account for a significant portion of energy consumption in wireless transceivers. Improving the power efficiency of PAs is especially important for mobile applications because the battery life is limited. Meanwhile, there are stringent linearity constraints on PAs in many modern communication systems employing nonconstant envelope signals. It remains a challenge in PA design to achieve linear amplification with high power efficiency.

It is known that PAs suffer from efficiency degradation at reduced drive levels. Various techniques, such as dynamic biasing [9], [10], envelope-tracking [11], [12], tunable matching networks [13–15], and Doherty amplifiers [36–38], have been proposed to improve PA's efficiency under low power operation. The dynamic biasing technique usually requires efficient DC-to-DC converters, whereas the envelope tracking approach needs efficient envelope amplification, both adding to the overall power consumption. Doherty amplifier implementation requires multiple devices and extra dividing/combining circuits, which adds to the cost, size, and circuit complexity. On the other hand, tunable matching networks, using passive elements such as tunable

capacitors, do not consume DC power. In addition, circuit complexity using tunable matching network approach is minimal because matching networks are integral parts of any amplifier circuit.

Using loadline theory, one can show that PA's maximum power efficiency can be achieved over the input drive variation if the load resistance presented to the transistor is adjusted to its optimum value according to the input power level [39]. A power-adaptive tunable output matching network, which presents different load impedances at different power levels, can therefore be used to enhance the overall PA efficiency. Moreover, we have shown that tunable matching networks can be used to compensate the amplitude and phase distortions generated by the transistors [15]; therefore, tunable matching network approach may be more preferable to the other aforementioned efficiency-improving techniques.

In this work, a medium-power amplifier with a varactor-based tunable output matching network is designed, fabricated, and tested. The tunable matching network is dynamically controlled according to the instantaneous input power level such that it not only presents an optimum load to the PA but also keeps PA's gain and phase constant, resulting in both efficiency enhancement and linearity improvement. The linearity improvement allows the PA to be operated at a smaller power back-off and therefore at a higher output power level, thus compensating for the extra losses that tunable matching networks usually introduce.

The chapter is organized as follows. In Section 3.2, the design and analysis of PAs with tunable matching networks are described. In Section 3.3, the measurement results are presented. Finally, the conclusions are given in Section 3.4.

3.2 Design

3.2.1 Implementation of Tunable Matching Network

To design a PA with a tunable output matching network that presents a variable load, one first has to determine the desired load impedances. For an ideal class-B amplifier, the load resistances required to maintain the maximum power efficiency at various power levels can be derived using loadline theory as shown in [39]. In practice, the load impedance required to achieve the maximum efficiency at a particular drive level can be determined by load-pull measurement or through nonlinear simulations, depending on the availability of accurate nonlinear device models.

As an example, the simulated load trajectory to achieve the maximum efficiency for a pHEMT device (FPD1500 by Filtronic) biased in class-AB region at various output power levels ranging from 16 to 22 dBm is shown in Figure 3.1(a). (The optimum load trajectory of a HBT device exhibits a similar trend [14].) Ideally, at the terminal of a transistor's current source, the desired load impedance is purely real. However, at the external terminal of the transistor, the desired load trajectory deviates from the real axis due to the drain-to-source capacitance, bondwire inductance, and package parasitic effects, as illustrated in Figure 3.1(b). The desired load impedance variation can be implemented by using a variable resistance R_L and a fixed LC matching network, as shown in Figure 3.1(c). There are numerous matching network configurations that allow one to implement the variable load resistance. However, not every circuit configuration is appropriate for the PA applications where there are stringent linearity constraints. In fact, most of the tunable matching network configurations introduce a large phase variation in S_{21} when providing the desired impedance variation. This causes AM-PM distortion when the tunable matching networks are dynamically tuned according to the instantaneous

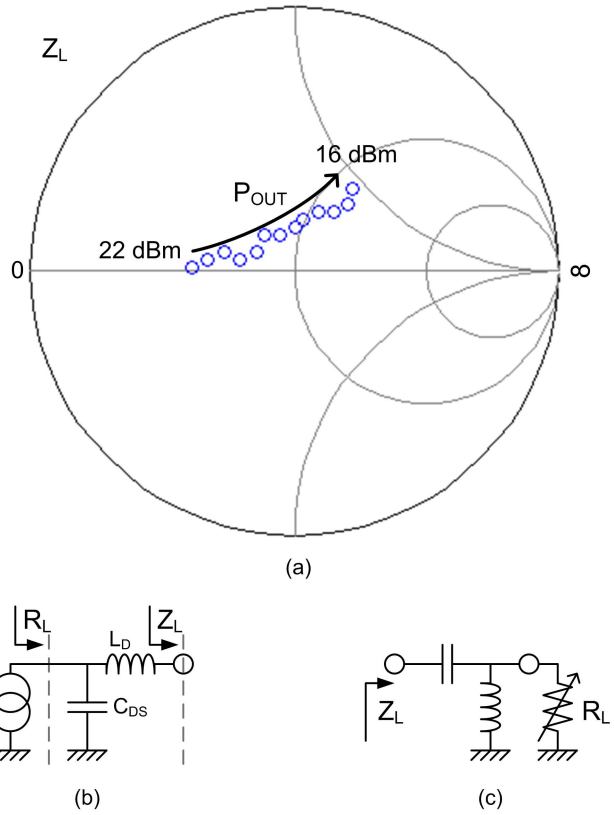


Figure 3.1: (a) Simulated trajectory of the load impedance (Z_L) for a pHEMT device that maximizes the efficiency at various power levels. (b) The The desired load trajectory deviates from the real axis due to reactive components at the drain terminal of the transistor. (c) The desired load impedance can be realized by a variable resistor and a fixed matching network.

power level, thus degrading the linearity of the PAs. To avoid the linearity degradation, one plausible solution is to use matching networks with constant phase, as suggested in [14]. Here, a high-pass T-network, which presents a constant phase characteristic, is used to implement the tunable matching circuit. The schematic of the T-network is shown in Figure 3.2(b). The T-network serves as a variable impedance transformer that transforms impedance Z_0 to the desired variable load resistance without introducing phase variations.

The input impedance and the phase difference between input and output currents of the T-network terminated with impedance Z_0, as shown in Figure 3.2(b), are given

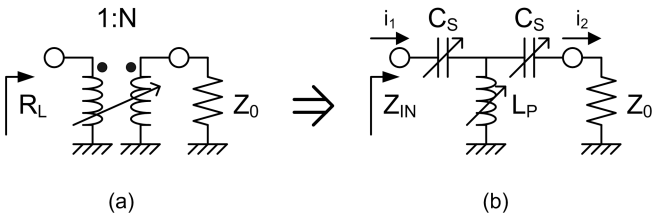


Figure 3.2: (a) Variable transformer configuration and (b) its implementation using a high-pass T-network.

by:

$$Z_{IN} = \frac{\omega^2 L_P C_S}{Z_0 \frac{C_S}{L_P} + \frac{1-\omega^2 L_P C_S}{j\omega L_P}} + \frac{1-\omega^2 L_P C_S}{j\omega C_S}, \tag{3.1}$$

and

$$\Delta\phi \equiv \measuredangle(i_2/i_1) = \tan^{-1}\left(\frac{Z_0}{\frac{1}{\omega C_S} - \omega L_P}\right). \tag{3.2}$$

When the circuit is designed at a frequency ω_0 satisfying

$$\omega_0 = \frac{1}{\sqrt{L_P C_S}}, \tag{3.3}$$

the input impedance and phase difference between input and output ports can then be reduced to:

$$Z_{IN} = \frac{L_P/C_S}{Z_0} \qquad \text{and} \qquad \Delta\phi = \frac{\pi}{2}. \tag{3.4}$$

Therefore, as long as the product of the tunable capacitance and inductance remains constant, the impedance can be varied according to the inductance to capacitance ratio of the network while maintaining the phase difference between input and output signals.

Given the desired range of the variable resistance R_L, the capacitance tuning ratio τ required for the series varactors C_S can be determined from (3.3) and (3.4):

$$\tau \equiv \frac{C_{S,max}}{C_{S,min}} = \sqrt{\frac{r_{L,max}}{r_{L,min}}}. \tag{3.5}$$

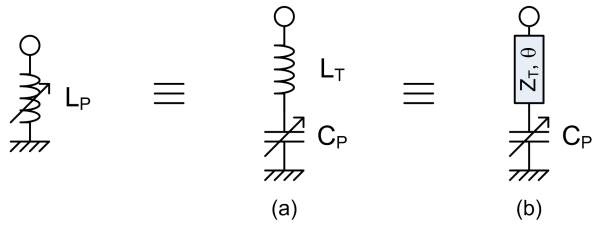


Figure 3.3: The implementations of tunable inductor using varactor with either (a) fixed inductor, or (b) transmission line.

where $r_{L,max}$ and $r_{L,min}$ are the maximum and minimum values of the desired load resistance R_L normalized to the system impedance Z_0. $C_{S,max}$ and $C_{S,min}$ are the maximum and minimum capacitances required for the varactor to achieve the desired load variation.

The tunable inductance L_P can be implemented by a varactor in series with either a fixed inductor or a transmission line, as shown in Figure 3.3(a) and (b), respectively. It can be shown that, to achieve the required tuning range for the inductance L_P while keeping the required tunability of the varactor C_P the same as that of C_S, the value for the fixed inductor in Figure 3.3(a) should be:

$$L_T = \frac{Z_0}{\omega_0}(\sqrt{r_{L,max}} + \sqrt{r_{L,min}}). \tag{3.6}$$

As for the transmission line implementation of tunable inductor (Figure 3.3(b)), it can be shown that the normalized characteristic impedance z_T and electrical length θ of the transmission line should satisfy the following condition:

$$\tan\left(\frac{\theta}{2}\right) = \frac{\sqrt{r_{L,max}r_{L,min}} - z_T^2 + \sqrt{(r_{L,max} + z_T^2)(r_{L,min} + z_T^2)}}{(\sqrt{r_{L,max}} + \sqrt{r_{L,min}})z_T}. \tag{3.7}$$

Based on the above equation, as the characteristic impedance of the line increases, its length decreases. However, simulation shows that, under the same input power, the voltage swing across the varactor increases as the length of the transmission line decreases. That is, when a shorter line is used, the input power that the varactor is

able to handle becomes less. Therefore, there is a tradeoff between the circuit size and the power handling capability when using transmission line implementation of tunable inductor.

3.2.2 Design of PA with Tunable Output Matching Network

A medium-power amplifier is designed at 1750 MHz. A tunable matching network is implemented at the output of the PA based on the design equations in Section 3.2.1. The PA's schematic is shown in Figure 3.4. The transistor in use is a pHEMT chip FPD1500 from Filtronic. The drain and the gate are biased at 2 and -0.9 volts, respectively, for class-AB operation. Load-pull simulations are performed to find the desired load trajectory for output power ranging from 16 to 22 dBm, which is shown previously in Figure 3.1(a). The desired load resistance R_L can then be obtained by curve-fitting the input impedance of the circuit shown in Figure 3.1(b) to the desired load trajectory. Based on the results obtained through the curve-fitting, R_L varies from 22.5 to 100 Ω as the output power level decreases form 22 to 16 dBm. Correspondingly, the minimum and maximum values of the normalized desired load resistance, $r_{L,min}$ and $r_{L,max}$, are 0.45 and 2, respectively. The tuning ratio required for the varactors in series C_S can be obtained by (3.5) from the analysis in Section 3.2.1. The transmission line implementation of the tunable inductor shown in Figure 3.3(b) is chosen for this design. The tuning ratio required for the varactors in shunt C_P is related to the transmission line parameters. As previously discussed, a high characteristic impedance ($\sim 95\,\Omega$) line with short electrical length (40°) is used in favor of a smaller circuit size, though it results in a higher tuning ratio requirement for the varactor C_P. The capacitances for the varactors in the tunable

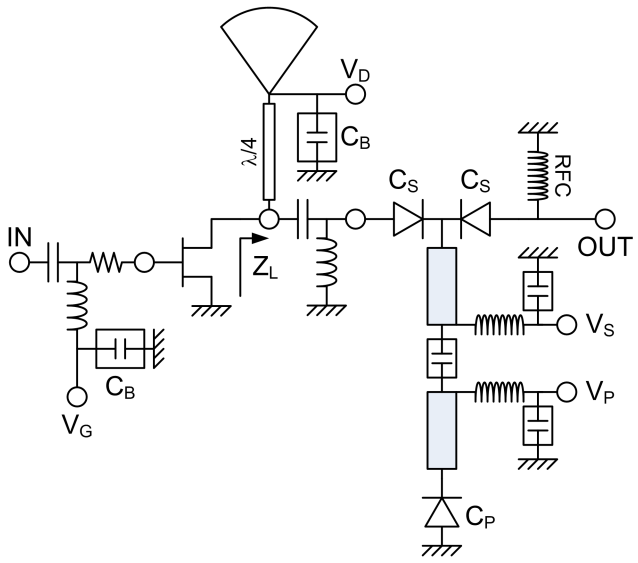


Figure 3.4: The schematic of PA with tunable output matching network.

matching network are obtained through simulation and plotted versus the desired load resistance in Figure 3.5.

As shown in Figure 3.4, RF chokes (RFCs) and blocking/bypassing capacitors are used for the bias network of the tunable matching network. Note that the blocking/bypassing capacitors should present low impedance to the GHz RF signal but present high impedance to the control signals (V_S and V_P), which follow the input envelope variation at MHz speeds.

The complete PA is simulated using Agilent's Advanced Design System (ADS). The simulated power-added efficiency (PAE) of the PA with R_L ranging from 22.5 to 100 Ω is shown in Figure 3.6. As the load impedance increases, the efficiency peak moves from high power to low power region, thus enhancing the efficiency at reduced drive levels. Note that the maximum output power level is lower than the initially specified 22 dBm due to the matching network's losses, which are not included in the load-pull simulation.

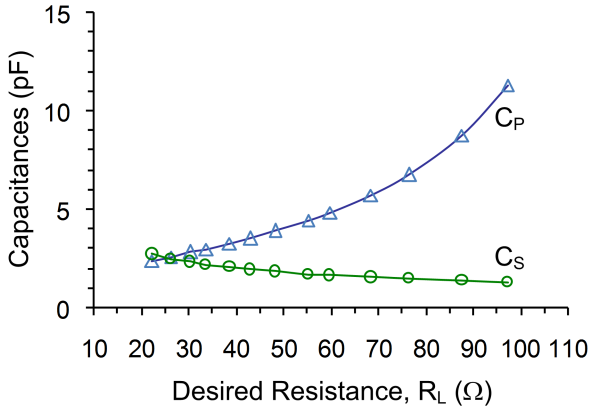


Figure 3.5: Required capacitances for the varactors in the tunable matching network versus the desired load resistance.

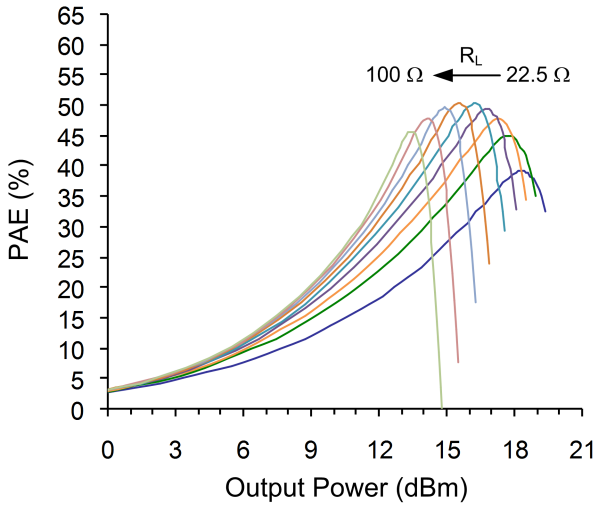


Figure 3.6: Simulated power-added efficiency (PAE) of PA with various R_L ranging from 22.5 to 100 Ω.

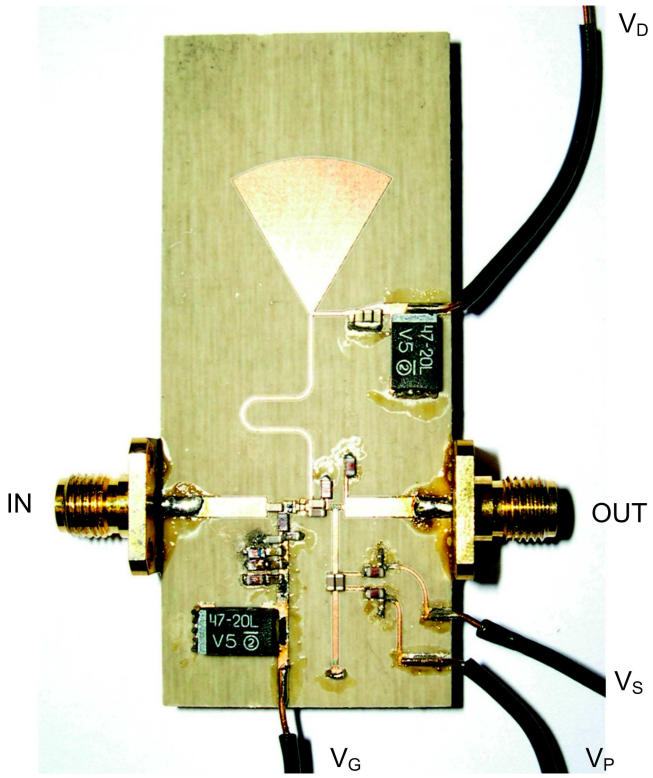


Figure 3.7: The photograph of the fabricated power amplifier.

3.3 Fabrication and Measurement

The medium-power amplifier with the tunable output matching network described in Section 3.2.2 is fabricated on a RO4003C™ board. Commercially available hyperabrupt GaAs varactor diodes (MA46480-277 by M/A-COM) are used as the tuning elements in the matching network. Transistor and varactor chips are wire-bonded to the rest of the circuit. Multiple capacitors, including large tantalum capacitors, are placed in shunt at gate and drain bias networks to prevent bias supply modulation, which can give rise to memory effects. The photograph of the fabricated ampliifer is shown in Figure 3.7.

The tunable output matching network is first tested separately using a network analyzer (Agilent E8364B). The small signal response at the designed frequency of

1750 MHz is measured. The impedance presented by the tunable matching network is shown on the Smith chart in Figure 3.8(a). The bias voltages are varied from 0 to 18 volts. The contours for constant dissipation loss and the desired load trajectory are also shown in Figure 3.8(a). As can be seen, over the desired impedance variation, the dissipation loss of the tunable matching network is less than 1.5 dB.

The insertion phase (phase of S_{21}) of the tunable matching network is also measured. The constant phase contours are plotted in Figure 3.8(b) with 5° step. Along the desired load trajectory for the maximum PA efficiency (bold curve), the variation of the insertion phase introduced by the tunable matching network is within 20°. One has the freedom to add a small prescribed amount of phase variation without changing the position of the load impedance dramatically. This can be employed to correct for the AM-PM distortion generated by the transistor with a minimal compromise in efficiency enhancement.

3.3.1 Performance of PA with Tunable Matching Network under Single-Tone Excitation

The medium-power amplifier is measured using a microwave transition analyzer (HP 70820A). First, the amplifier is tested under a large collection of bias voltages applied to the varactors. The PAE, gain, and insertion phase of the PA at 1750 MHz plotted versus its output power are shown in Figure 3.9(a), (b) and (c), respectively. Note that the measured output power level deviates from the simulation results, primarily due to the nonlinear device model inaccuracy.

Next, in order to improve the PA's efficiency and linearity, the bias voltages for the tunable matching network at each power level are selected such that the highest possible PAE is achieved while maintaining the gain and phase flatness over the

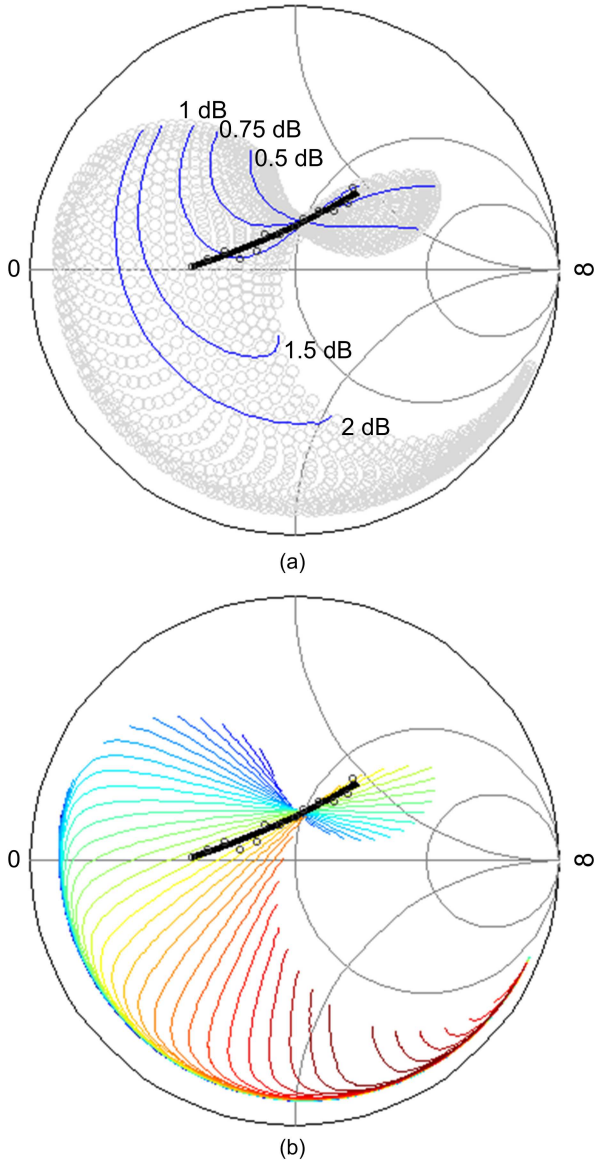


Figure 3.8: (a) Contours of constant dissipation loss (thin curves) and desired load trajectory (bold curve) plotted against impedance coverage of the tunable matching network; (b) contours of constant insertion phase (5° step).

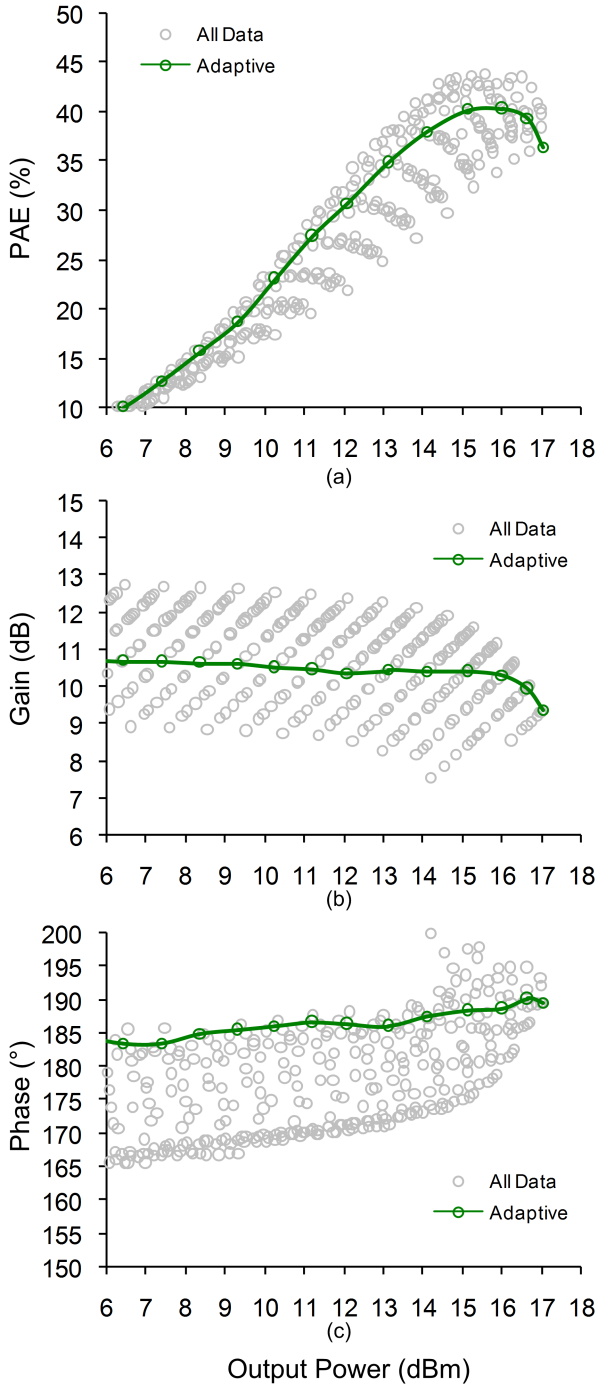


Figure 3.9: Measured (a) PAE, (b) gain, and (c) insertion phase of PA with tunable matching network under various bias voltages and input power levels (circular markers). Solid lines show the corresponding responses when the bias voltages of the tunable matching network are selected to obtain the highest possible efficiency while maintaining gain and phase flatness.

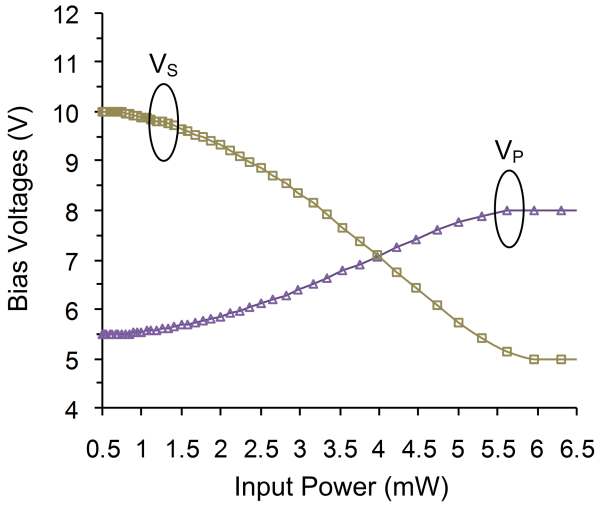


Figure 3.10: Required bias voltages for the varactors in the tunable matching network versus the input power to the PA. V_P and V_S are the bias voltages for varactors C_P and C_S, respectively, as shown in Figure 3.4.

input power variation. The required bias voltages for the varactors in the tunable matching network are plotted versus the input power to the PA in Figure 3.10, where V_S and V_P are the bias voltages for the varactors C_S and C_P, respectively. The corresponding responses of the PA are shown as solid lines in Figure 3.9. As can be seen, the variations in the gain and insertion phase of the PA with the tunable matching network are less than 1.5 dB and 10°, respectively. Note that, due to the linearity constraint imposed, the PAE of the PA with the tunable matching network does not reach its potential maximum. However, the difference is less than 4% in the worst case.

3.3.2 Performance of PAs under Modulated Signal Excitation

The measurement setup for testing the PA with the tunable matching network under a modulated signal is shown in Figure 3.11. Within the personal computer

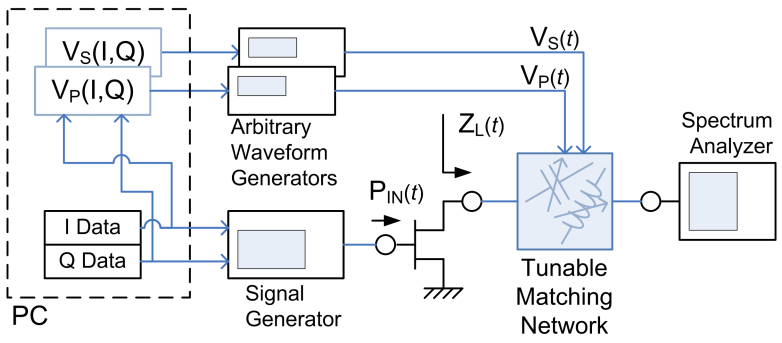


Figure 3.11: Setup for testing the PA with the tunable matching network under the excitation of a modulated signal.

(PC), the biasing waveforms ($V_S(t)$ and $V_P(t)$) are generated according to the base-band in-phase (I) and quadrature (Q) components of the modulated signal based on the relations shown in Figure 3.10. Using NI LabVIEW[1], the biasing waveforms are downloaded to arbitrary waveform generators (Agilent 33220A) through GPIB[2], which provide the bias voltages for the varactors in the tunable matching network. The modulated signal is generated by a signal generator (Agilent E4438C) based on the same baseband I/Q data segments, which are preloaded through GPIB using LabVIEW. The PA's output is connected to a spectrum analyzer (Agilent E4443A).

Two-Tone Signal

The PA is first tested using a two-tone signal. A two-tone signal is basically a modulated signal with I component being sinusoidal and Q equal to zero. The two tones are centered at 1.75 GHz and separated by 0.48 MHz. The third-order intermodulation (IM_3) components are measured. The drain efficiency and IM_3 of the PA are plotted versus the total output power and shown in Figure 3.12, where three different conditions of varactor biasing are considered:

[1]http://www.ni.com/labview/
[2]General Purpose Interface Bus

(i) fixed bias voltages for low input power level ($V_P = 5.5$ V and $V_S = 10$ V)

(ii) fixed bias voltages for high input power level ($V_P = 8$ V and $V_S = 5$ V)

(iii) variable bias voltages dynamically controlled according to the instantaneous input power level (V_P and V_S are functions of P_{IN} as shown in Figure 3.10)

Comparing condition (i) and (ii), it can be seen that condition (i) exhibits better drain efficiency whereas condition (ii) shows lower intermodulation distortion, clearly illustrating the tradeoff between efficiency and linearity. As for condition (iii), the intermodulation distortion is the lowest because the tunable matching network is dynamically biased to reduce the AM-AM and AM-PM distortions of the PA. The drain efficiency of condition (iii) approaches condition (i) and (ii) at the low and high power ends, respectively.

WCDMA Signal

The PA is also tested using a 3GPP WCDMA uplink signal (DPCCH + 1DPDCH) [40] with a peak-to-average ratio of 3.3 dB. The complimentary cumulative distribution function (CCDF) plot of the signal is shown in Figure 3.13. The bias voltages for the varactors in the tunable matching network are dynamically adjusted according to the instantaneous input power level. Although a WCDMA uplink signal is used here for demonstration, the technique itself is not limited to a particular modulation format.

For comparison, a PA with a fixed matching network is also designed and fabricated. The load impedance presented by the fixed matching network, located on the desired load trajectory for maximum efficiency, is chosen such that the PA meets the -33 dBc adjacent channel power ratio (ACPR) specification [40] at the same power level as the PA with the tunable matching network.

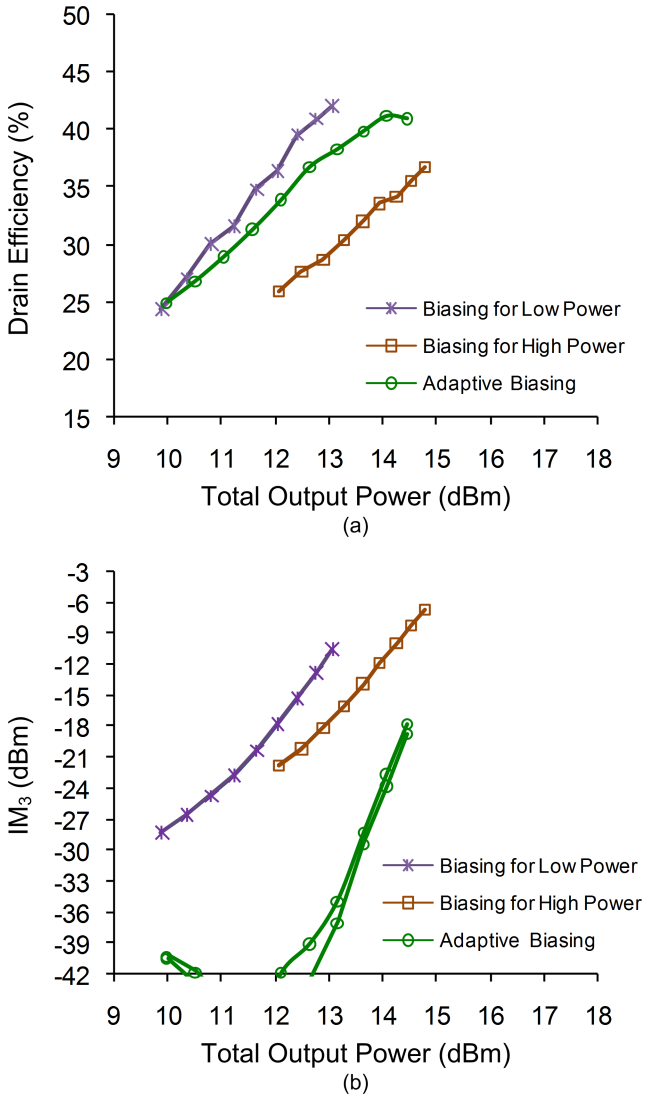


Figure 3.12: Two-tone test: (a) drain efficiency, and (b) lower/upper IM_3 of the tunable PA with varactor bias voltages fixed for low input power level (star markers), fixed for high input power level (square markers), and adaptively controlled according to the instantaneous input power level (circular markers).

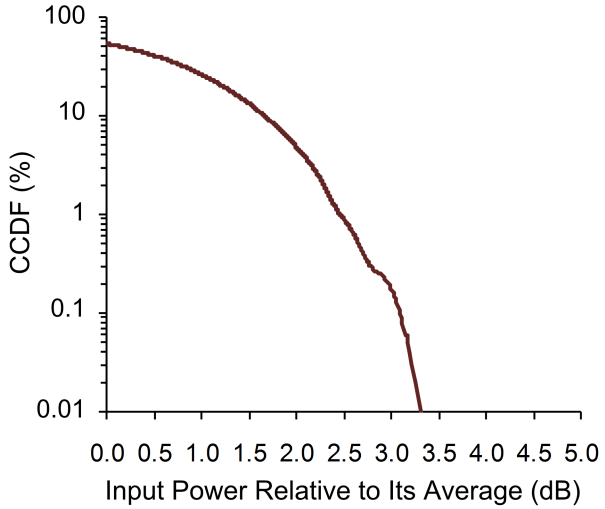


Figure 3.13: Complementary cumulative distribution function (CCDF) plot of the 3GPP WCDMA uplink signal with DPCCH+1DPDCH.

The drain efficiency and the ACPR at 5-MHz offset for both PAs are plotted versus average output power in Figure 3.14(a) and (b), respectively. The maximum output power of the PA with the tunable matching network is approximately 15 dBm while maintaining an ACPR of below -33 dBc and a drain efficiency of 43%. As can be seen, under the same linearity constraint, the PA with the tunable matching network is superior in terms of power efficiency. The difference in drain efficiency between the two PAs is as high as 5% at the output power level of 13 dBm, which corresponds to approximately 13% reduction in the DC power consumption. It should be noted that, due to the limited quality factor of varactor diodes, the tunable matching network has a higher insertion loss compared to the fixed matching network, which reduces the overall efficiency improvement expected from the tunable matching network. The enhancement in power efficiency could be more significant if the tuning elements were replaced by MEMS [33] or ferroelectric-based [21], [6] varactors with higher quality factors compared to semiconductor-based varactor diodes.

Furthermore, the ACPR of the PA with the tunable matching network is better than that of the PA with the fixed matching network by up to 5 dB at low power region, as shown in Figure 3.14(b). In general, as long as the tunable matching network is controlled in such a way that the PA presents flat AM-AM and AM-PM responses, one can expect to have less spectral regrowth and a better ACPR.

3.4 Conclusions

A circuit configuration for tunable matching networks that introduces no phase variation while providing a variable impedance is presented. The design equations for the presented circuit configuration are derived. The circuit configuration is suitable for enhancing the efficiency of PAs at reduced drive levels especially when there are linearity constraints.

A 1750-MHz medium-power amplifier with a tunable output matching network using the proposed configuration is designed, fabricated, and tested. By adjusting the bias voltage of the varactors in the tunable matching network, the efficiency can be improved at various power levels. Experimental results also show that, the bias voltages for varactors can be chosen such that the AM-AM and AM-PM distortions of the amplifier are reduced. Moreover, under the excitation of a 3GPP WCDMA signal, the PA with the dynamically controlled tunable matching network according to the instantaneous input power shows both higher efficiency and linearity when compared with a PA with a fixed matching network, demonstrating the effectiveness of the tunable matching networks in achieving both efficiency enhancement and linearity improvement for PAs.

Although it is not within the scope of this work, the tunable matching approach

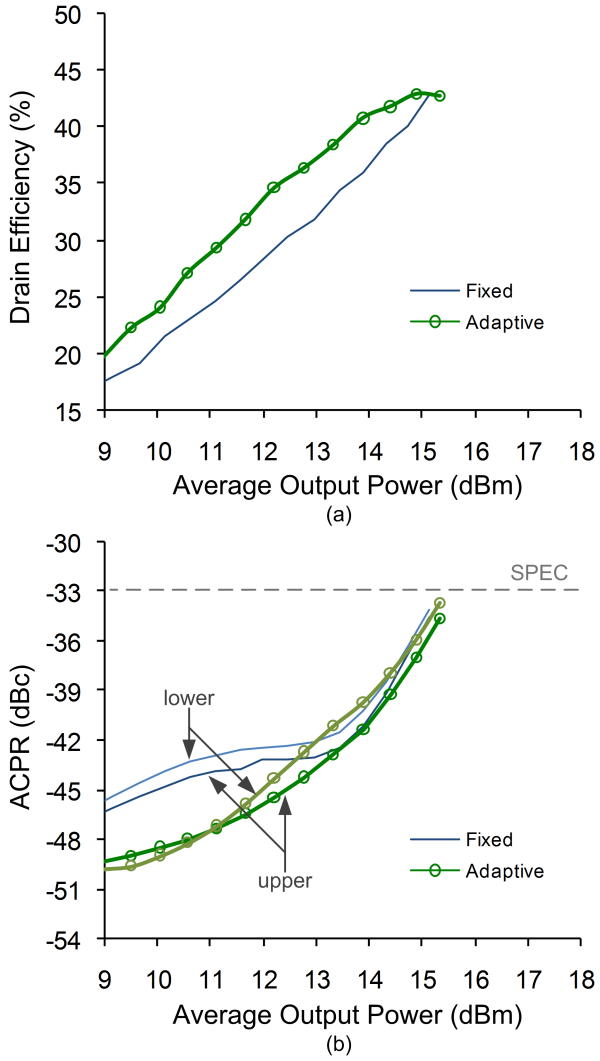


Figure 3.14: (a) Drain efficiency and (b) lower/upper adjacent channel power ratio (ACPR) at 5-MHz offset of PAs with fixed matching network (without markers) and tunable matching network (with circular markers) under the excitation of the WCDMA signal.

can also be used for power control to enhance the average power efficiency of PAs and to increase the battery life. One may combine the tunable matching approach with the drain/collector bias control technique for a wider power control range. Other applications of tunable matching networks include multiband PA design for multistandard transceivers and compensation of antenna impedance mismatch due to interactions with nearby objects.

CHAPTER IV

An Impedance Tuner and Its Application in an Adaptive Matching System

4.1 Introduction and Motivation

The input impedance of an antenna is sensitive to the nearby objects and human bodies [17], [16]. Consequently, in mobile applications, the antenna input impedance may change from time to time. The variation of the antenna impedance causes impedance mismatch, which results in power reflection and subsequently reduces the transmit power and link quality. The reflected power are harmful to PAs that are directly connected to the antenna. High voltage standing wave ratio (VSWR) may permanently damage the transistors in the PAs. Besides, the antenna impedance variation also causes degradation in PA performance, reducing the power efficiency. Therefore, antenna tuning, i.e. compensating the antenna impedance variation, is important for mobile devices to avoid the aforementioned drawbacks.

Due to the time-varying nature of the antenna impedance variation, antenna tuning is an application where adaptive impedance matching circuits are highly desirable. The antenna impedance value at a particular time instant is subject to the operating environment and is therefore unpredictable. Hence, an antenna tuning unit must be able to detect the antenna impedance variation and adjust itself to correct

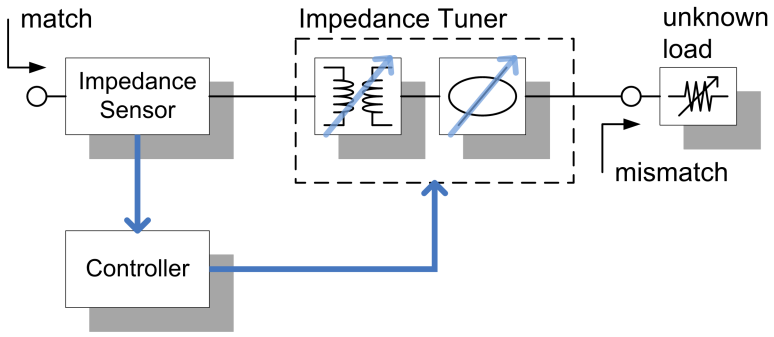


Figure 4.1: Block diagram of the proposed adaptive matching system.

for the deviation in real time. To automatically compensate for the impedance variation of an antenna, an adaptive matching system as shown in Figure 4.1 can be used. It is a closed-loop system consisting of an impedance tuner, an impedance sensor, and a controller. Among them, the impedance tuner is the key component that is responsible for transforming any unknown load impedance to the system impedance while introducing as low insertion loss as possible.

An impedance tuner is one indispensable component in applications such as source-pull and load-pull measurements for noise [41], [42] and large-signal characterizations [43], [44] of transistors. They can also be specifically designed as tunable matching networks that may be either connected to antennas to compensate for antenna impedance variations [17], or placed right after power amplifiers (PAs) to provide optimal load conditions at different frequency bands [2–6] or power levels [13–15].

Over the years, various general-purpose impedance tuners, which are designed to cover the entire Smith Chart, have been demonstrated. Circuit configurations for these tuners include stub-based [45–47], loaded-line [33], and double-slug [48]. Among them, the double-slug configuration, providing uniform coverage in the four quadrants of the Smith chart, is most suitable for applications where no information

of the load impedance to be matched is known *a priori*. In a double-slug tuner, the cascaded sections of a fixed transformer (a slug), a phase shifter, and another fixed transformer together perform the function of a variable transformer.

Here, an impedance tuner based on all-pass networks [34] is proposed. Composed of a variable transformer and a phase shifter, both designed based on all-pass networks, the proposed impedance tuner provides uniform coverage in the four quadrants of the Smith chart like a double-slug tuner does but however exhibit a lower circuit complexity. Besides, it also has the advantage that the mapping between the transformed impedance and the control signals is more straightforward when compared with stub-based or loaded-line tuners. Thus, when used in an adaptive matching system, the proposed tuner can be controlled using less complicated control schemes involving no look-up tables and DSP units.

This chapter covers impedance tuners that are designed based on all-pass networks and the application in an adaptive matching system. In Section 4.2, the design of the impedance tuners is detailed. In Section 4.3, an implementation of the tuner based on ferroelectric varactors is demonstrated. In Section 4.4, the analysis and design of an adaptive matching system based on the impedance tuner are presented. Finally, Section 4.5 summarizes the work on the impedance tuners and the adaptive matching system.

4.2 Design and Simulation

The proposed impedance tuner is composed of a phase shifter and a variable transformer. Both the phase shifter and variable transformer are designed based on all-pass networks. The schematics of generic all-pass networks are shown in Fig-

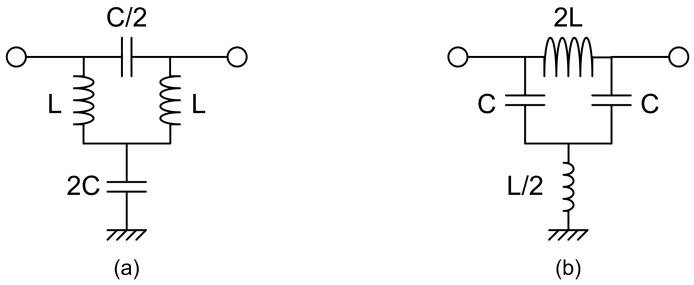


Figure 4.2: Generic all-pass networks: (a) series-C configuration, and (b) series-L configuration.

ure 4.2. As can be seen, two types of all-pass networks are available – series-C and series-L configurations. Although these two configurations theoretically have the same performance, the series-L configuration, however, requires more overall inductance per unit than the series-C configuration. Since inductors usually occupy a large area and suffer from low quality factors, the series-C configuration is therefore preferable to the series-L configuration in practice. As a result, series-C configured all-pass networks are used throughout this study.

The design equations for the all-pass network can be found in [34] and are included here. Since the all-pass network is symmetric and reciprocal, it can be described by

$$S_{11} = \frac{1}{2}(\Gamma_e + \Gamma_o), \tag{4.1}$$

and

$$S_{21} = \frac{1}{2}(\Gamma_e - \Gamma_o). \tag{4.2}$$

Γ_e and Γ_o are the even-mode and odd-mode reflection coefficients, respectively, and can be expressed as follows.

$$\Gamma_e = \frac{jWz - 1}{jWz + 1}, \tag{4.3}$$

and

$$\Gamma_o = \frac{1 - j\frac{W}{z}}{1 + j\frac{W}{z}}, \tag{4.4}$$

where

$$z = \frac{1}{Z_0}\sqrt{\frac{L}{C}}, \tag{4.5}$$

and

$$W = \Omega - \frac{1}{\Omega}. \tag{4.6}$$

Ω is the normalized frequency:

$$\Omega = \omega\sqrt{LC}, \tag{4.7}$$

where ω is the radial frequency.

4.2.1 Phase Shifter

As long as $\sqrt{L/C} = Z_0$ is satisfied, the all-pass network would provide a prescribed amount of phase shift without any power reflection (i.e. $S_{11} = 0$). Therefore, in the phase shifter design, both the capacitance and inductance must be tunable so that their ratio can be maintained in order to provide a perfect match at all times. However, because electronically tunable inductors are difficult to obtain, in practice, only variable capacitors are incorporated [35, 49, 50]. Although one may use a fixed inductor in series with a varactor to achieve a tunable inductance, it is often avoided because the approach leads to additional insertion loss. Moreover, the circuit performance is usually acceptable even with fixed inductors. The schematic of a varactor-incorporated all-pass network is shown in Figure 4.3(b), where the bias voltage V_B is applied through the input and/or output ports, and a large resistor R_{BB} is used to provide DC ground. If one wishes to separately bias the varactors in series and those in shunt, the structure shown in Figure 4.3(c) can be used.

The value of the fixed inductor L is an important design parameter for maximizing the return loss, i.e. reducing the reflected power, over the whole range of the phase

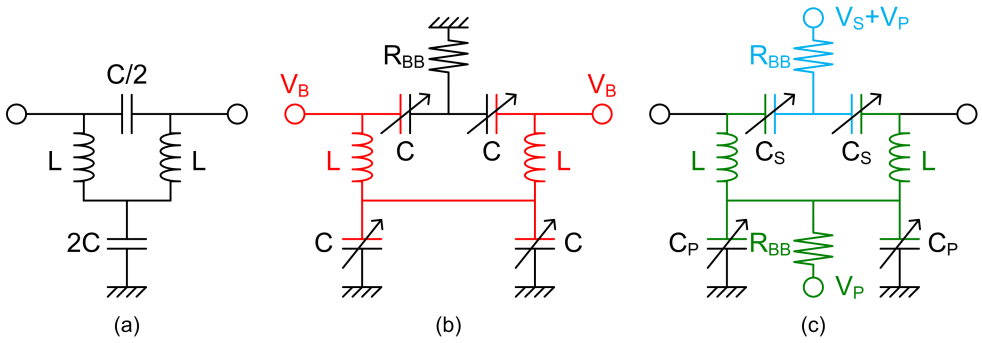


Figure 4.3: (a) Generic all-pass network; (b) all-pass network incorporating varactors that are biased through input/output ports; (c) all-pass network that has two biasing nodes to separately bias the series and parallel varactors.

variation provided by the phase shifter. To derive the design equations, we first assume that

$$L = tL_0, \tag{4.8}$$

where t is the variable to be determined, and

$$L_0 = \frac{Z_0}{\omega}, \tag{4.9}$$

where Z_0 is the reference impedance, which is equal to the system impedance in this case. It can be inferred from (4.1), (4.3), and (4.4) that for $S_{11} = 0$, two solutions exist:

$$z = 1, \tag{4.10}$$

and

$$W = 0. \tag{4.11}$$

By solving (4.10) and (4.11), one gets

$$C = tC_0, \tag{4.12}$$

and

$$C = C_0/t, \tag{4.13}$$

respectively, where C is the capacitance of the varactors, and

$$C_0 = \frac{1}{\omega Z_0}, \tag{4.14}$$

where Z_0 is the reference impedance. Therefore, if $t \neq 1$, there will be two nulls in $|S_{11}|$ as the varactors are tuned from tC_0 to C_0/t. The tuning ratio required for the varactors τ, which is the ratio between tC_0 and C_0/t, is therefore t^2 or t^{-2} depending on whether t is larger or smaller than 1. It can be written as

$$\tau = e^{2|\ln t|}. \tag{4.15}$$

Next, the insertion phase of the phase shifter (i.e. the phase of S_{21}) is examined under the conditions specified in (4.12) and (4.13). First, the condition $C = C_0/t$ always results in $S_{21} = -1$, i.e. the insertion phase is 180°, with no dependence on t. On the other hand, when $C = tC_0$, the insertion phase can be expressed as follows.

$$\phi = \pi - 2\tan^{-1} W = \pi - 2\tan^{-1}\left(\Omega - \frac{1}{\Omega}\right) = \pi - 2\tan^{-1}\left(t - \frac{1}{t}\right), \tag{4.16}$$

which is a function of t. The overall phase shift between the two points where $S_{11} = 0$ can then be expressed in terms of t:

$$\Delta\phi = \pi - \phi = 2\tan^{-1}\left(t - \frac{1}{t}\right). \tag{4.17}$$

Based on (4.17) and (4.15), the desired phase shift $\Delta\phi$ is plotted versus the required varactor tuning ratio τ in Figure 4.4.

According to Figure 4.4, to design a phase shifter with a phase shift of 90°, one would choose $\tau = 2.618$. From (4.15), there are two solutions: $t = 0.618$ and $t = 1.618$. The insertion phase and return loss for both cases are plotted versus normalized capacitance, C/C_0, as shown in Figure 4.5. The phase variation of 90° is achieved for both cases as the capacitance varies from $0.618C_0$ to $1.618C_0$.

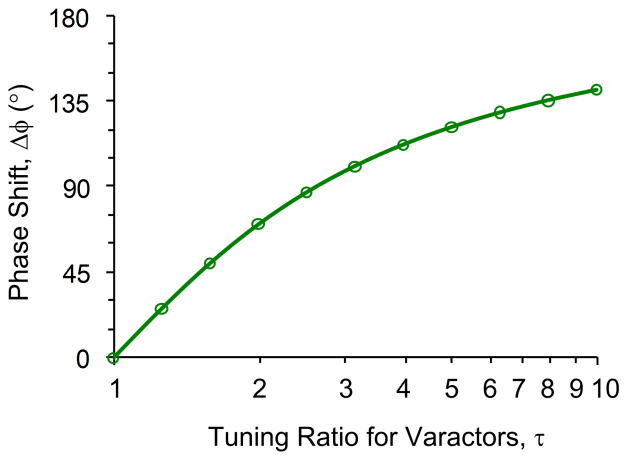


Figure 4.4: Desired phase shift and required varactor tuning ratio for a single-stage all-pass phase shifter.

It can also be inferred from Figure 4.4 that, for a single-stage all-pass phase shifter, there is no way to achieve a 180° phase shift. However, in the impedance tuner design, a phase shift of 180° or more is often needed in order to have a full angular coverage of 360°. As a result, a two-stage all-pass network must be used. The design equations for a two-stage all-pass phase shifter are derived as follows. First, the S-parameters of a two-stage all-pass network ($S_{11}^{(2)}$ and $S_{21}^{(2)}$) can be expressed in terms of the S-parameters of a single-stage all-pass network (S_{11} and S_{21}):

$$S_{11}^{(2)} = \frac{S_{11}(1 - S_{11}^2 + S_{21}^2)}{1 - S_{11}^2}, \tag{4.18}$$

and

$$S_{21}^{(2)} = \frac{S_{21}^2}{1 - S_{11}^2}. \tag{4.19}$$

For $S_{11}^{(2)} = 0$, several solutions exist:

$$z = 1 \quad \text{and} \quad W = 0, \pm 1, \tag{4.20}$$

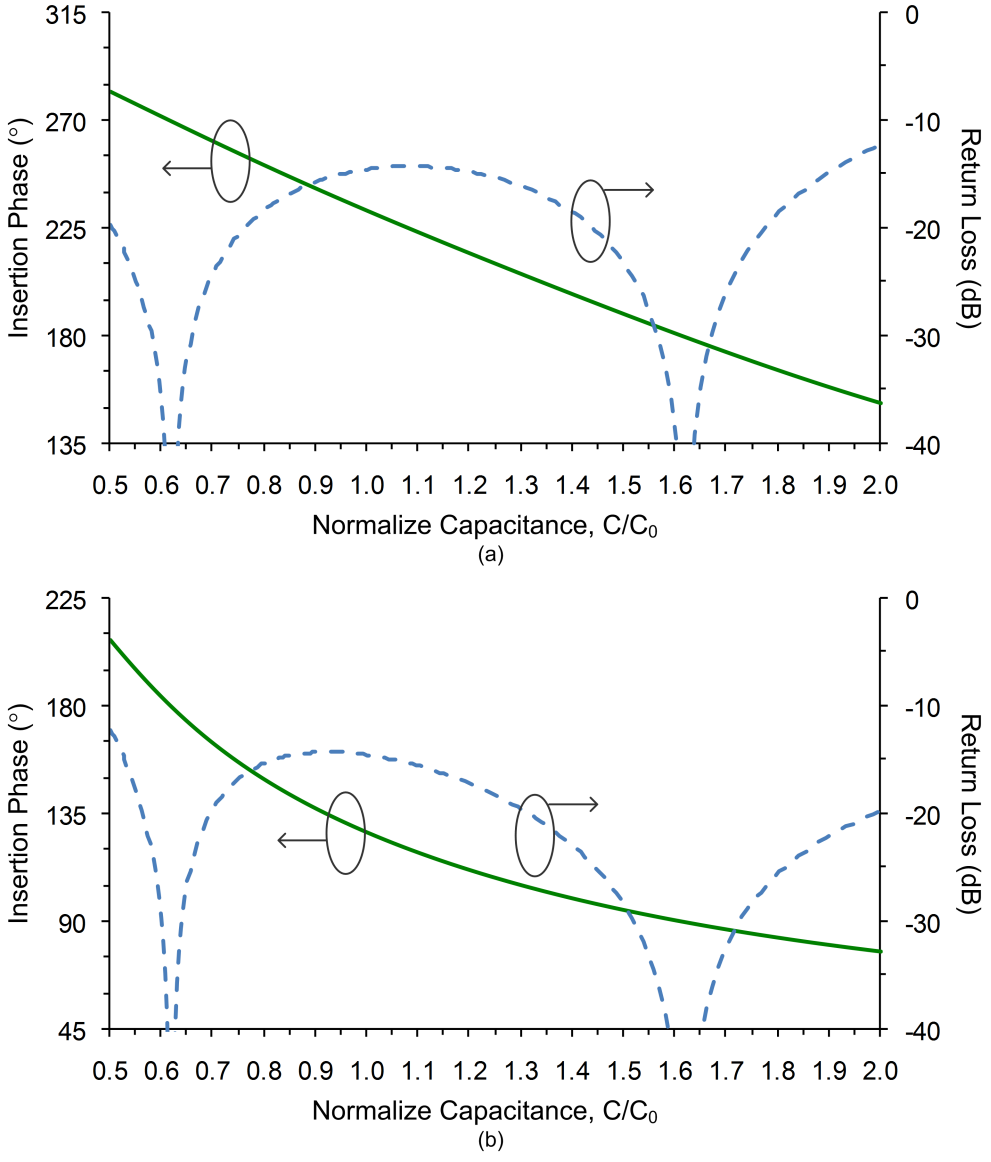


Figure 4.5: The insertion phase and return loss of single-stage all-pass phase shifters designed for 90° phase shift (a) $L = 0.618L_0$, $C_{max} = 1.618C_0$, $C_{min} = 0.618C_0$; (b) $L = 1.618L_0$, $C_{max} = 1.618C_0$, $C_{min} = 0.618C_0$.

Table 4.1: Design Parameters for Phase Shifters Based on All-Pass Networks

	Single-Stage		Two-Stage	
Desired Phase Shift	90°		180°	
L/L_0	0.618	1.618	0.786	1.272
C_{max}/C_0	1.618	1.618	2.058	1.272
C_{min}/C_0	0.618	0.618	0.786	0.486

$L_0 = Z_0/\omega$ and $C_0 = 1/(\omega Z_0)$, as defined in (4.9) and (4.14), respectively.

which lead to

$$C = \begin{cases} tC_0 \\ \frac{C_0}{t} \\ (\frac{\sqrt{5}-1}{2})^2 \frac{C_0}{t} \\ (\frac{\sqrt{5}+1}{2})^2 \frac{C_0}{t} \end{cases} \tag{4.21}$$

It can be found that, by choosing $t = ((\sqrt{5}-1)/2)^{1/2} = 0.786$ or $t = ((\sqrt{5}+1)/2)^{1/2} = 1.272$, the deeps in return loss would be evenly distributed over the varactor tuning range. For $t = 0.786$ and $t = 1.272$, the insertion phase and return loss are plotted versus normalized capacitance, C/C_0, in Figure 4.6. In both cases, 180° phase variation is achieved with a varactor tuning ratio of 2.618. The design parameters for both the 90° single-stage and 180° two-stage phase shifters are summarized in Table 4.1.

4.2.2 Type I Variable Transformer

Using all-pass networks, there are two approaches to design a variable impedance transformer. First approach to achieve a variable impedance transformation is to use a 90° phase shifter that is designed with a reference impedance (Z_0 as in (4.9) and (4.14)) other than the system impedance (Z_0 as in (4.5)). We call this approach type I variable transformer design. In the regular phase shifter design, the reference impedance is set to the same values as the system impedance. In the type I variable

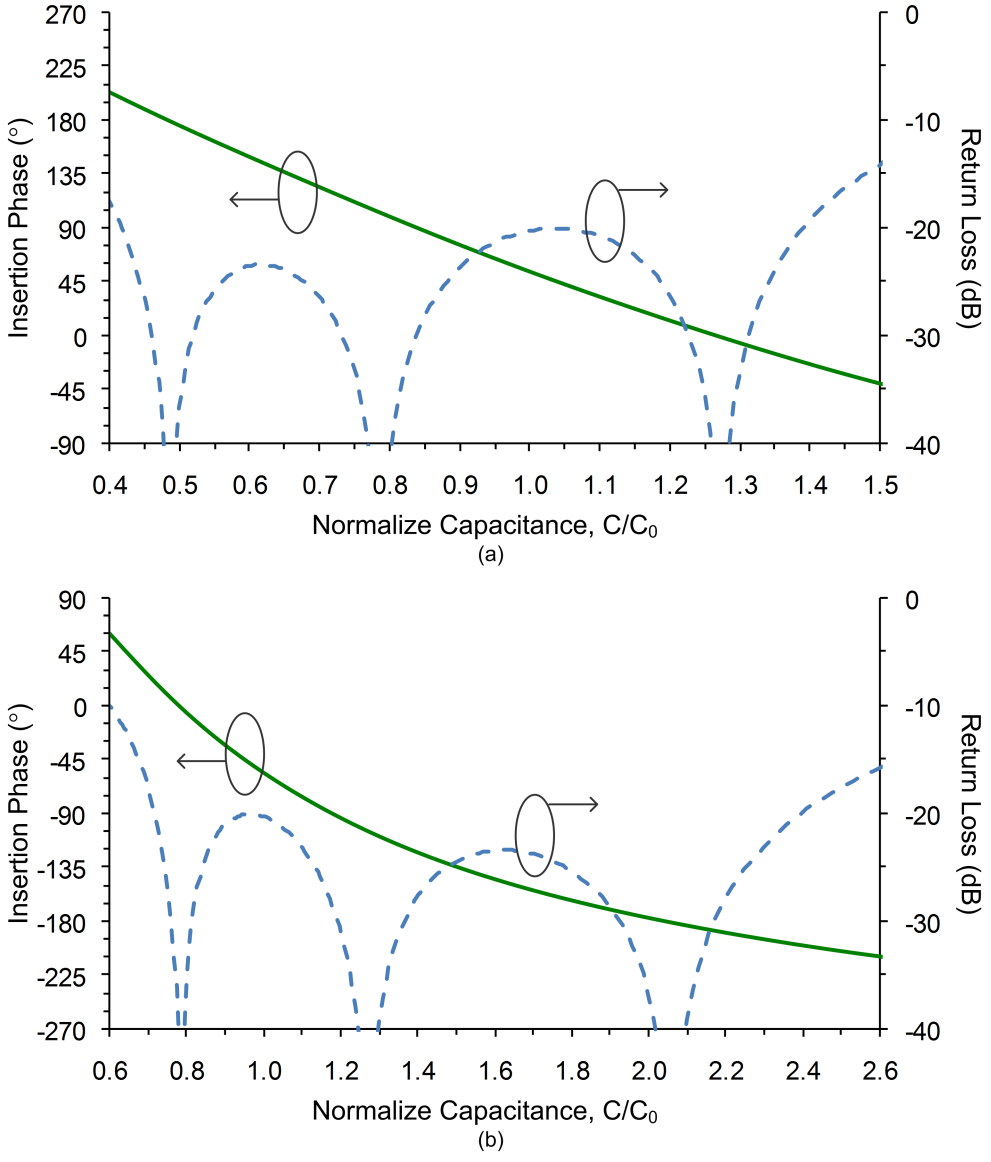


Figure 4.6: The insertion phase and return loss of two-stage all-pass phase shifters designed for 180° phase shift: (a) $L = 0.786L_0$, $C_{max} = 2.058C_0$, $C_{min} = 0.786C_0$; (b) $L = 1.272L_0$, $C_{max} = 1.272C_0$, $C_{min} = 0.486C_0$.

transformer design, on the other hand, they should be different. Figure 4.7 illustrates how variable impedance transformation can be achieved by a phase shifter designed with a reference impedance that is different from the system impedance. Here, we use the notation Z_T to represent the reference impedance so that it is not confused with the system impedance, Z_0. In this example, $Z_T = Z_0/4$. In Figure 4.7(a), Z_{BT} (impedance before transformation) is transformed to Z_{AT} (impedance after transformation) by a phase shifter. Here,

$$Z_{BT} = Z_0, \tag{4.22}$$

and its corresponding reflection coefficient when referenced to Z_0 is at the center of the Smith chart, as shown in Figure 4.7(b). Figure 4.7(c) shows the reflection coefficient referenced to Z_T, which is

$$\Gamma_{BT,Z_T} = \frac{Z_{BT} - Z_T}{Z_{BT} + Z_T}. \tag{4.23}$$

After the phase shifter, the phase of the reflection coefficient is increased by twice the insertion phase of the phase shifter. The reflection coefficient after the phase shifter referenced to Z_T is

$$\Gamma_{AT,Z_T} = \Gamma_{BT,Z_T} \cdot e^{2j\phi}, \tag{4.24}$$

where ϕ is the insertion phase of the phase shifter, which varies form 90° to 180° in this example. As shown in Figure 4.7(d), the reflection coefficient spreads on a circle centered at the origin with a radius equal to $|\Gamma_{BT,Z_T}|$. Next, the impedance after the transformation, Z_{AT} is calculated:

$$Z_{AT} = Z_T \frac{1 + \Gamma_{AT,Z_T}}{1 - \Gamma_{AT,Z_T}}. \tag{4.25}$$

Finally, the reflection coefficient referenced to the system impedance is

$$\Gamma_{AT,Z_0} = \frac{Z_{AT} - Z_0}{Z_{AT} + Z_0} = \frac{z_T^2 - 1}{z_T^2 + 1 - 2j z_T \tan\phi}, \tag{4.26}$$

where

$$z_T \equiv \frac{Z_T}{Z_0}. \tag{4.27}$$

The final result is plotted in Figure 4.7(e). Depending on the phase shift, different amount of impedance transformation can be achieved. When $\phi = 90°$, $\tan\phi$ approaches infinity, $\Gamma_{AT,Z_0} = 0$, and $Z_{AT} = Z_0 = Z_{BT}$, i.e. no impedance transformation is achieved. On the other hand, when $\phi = 180°$, the magnitude of the reflection coefficient reaches its maximum

$$|\Gamma_{AT,Z_0}|_{max} = \left|\frac{z_T^2 - 1}{z_T^2 + 1}\right|. \tag{4.28}$$

The maximum impedance transformation ratio (ITR) is therefore the square of the ratio between Z_T and Z_0, i.e. z_T^2 or z_T^{-2} depending on whether Z_T is larger than Z_0 or not, and can be written as

$$ITR_{max} = e^{2|\ln z_T|}. \tag{4.29}$$

Note that, besides the variable impedance transformation, a variable phase shift is also introduced by the variable transformer, as can be seen in Figure 4.7(e). Therefore, the phase and magnitude of the reflection coefficient cannot be independently controlled using an impedance tuner based on type I variable transformers.

4.2.3 Type II Variable Transformer

As described in Section 4.2.2, since the type I variable transformer not only introduces a variable impedance transformation but also phase variations, it is not suitable for applications where independent control of the phase and magnitude of the reflection coefficient is desired. To resolve this problem, an alternative approach to design a variable transformer, also based on all-pass networks, is presented here.

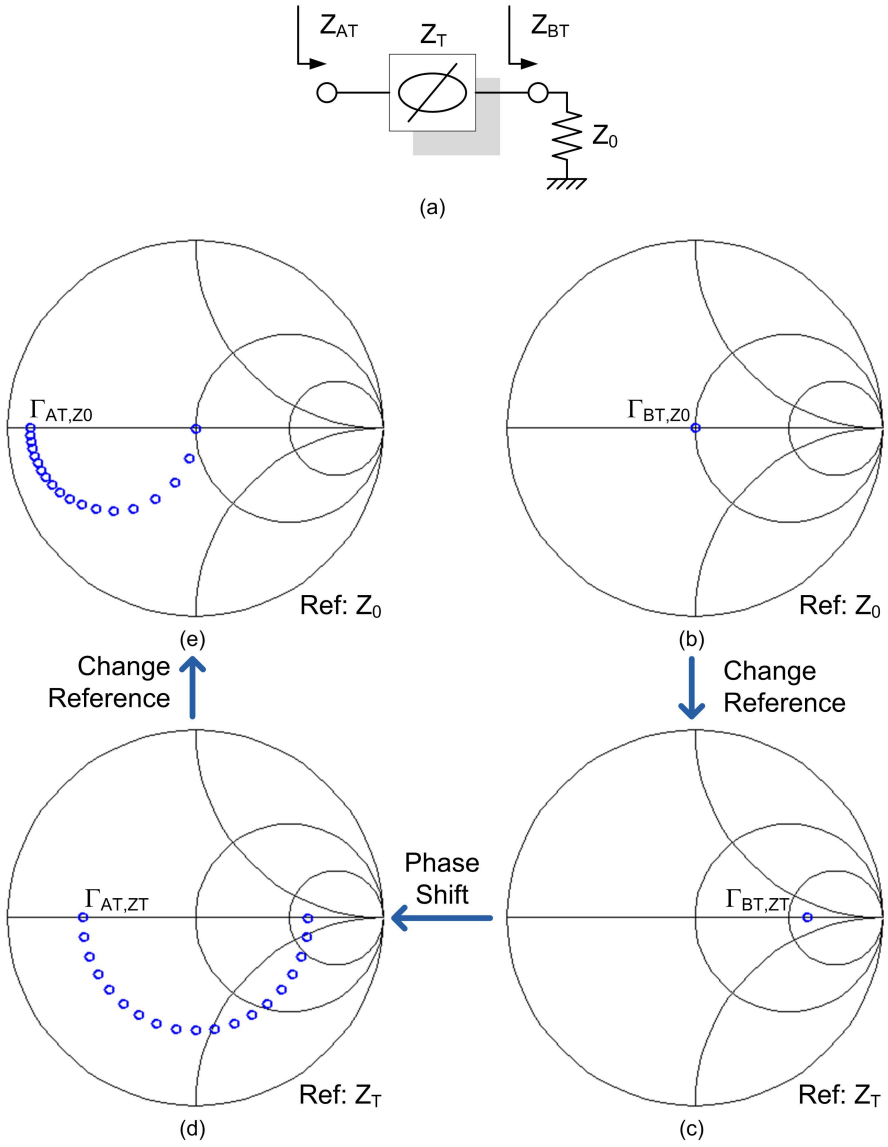


Figure 4.7: Illustration of how variable impedance transformation can be achieved by a phase shifter designed for a reference impedance, Z_T, which is different from the system impedance Z_0. (a) Schematic; (b) Z_{BT} referenced to Z_0; (b) Z_{BT} referenced to Z_T; (b) Z_{AT} referenced to Z_T; (e) Z_{AT} referenced to Z_0.

We call this approach type II variable transformer design. The type II variable transformer is implemented using an all-pass network with separate bias voltages for the varactors in series and shunt, as shown in Figure 4.3(c).

For the type II variable transformer, the fixed inductance

$$L = L_0 = \frac{Z_0}{\omega}, \tag{4.30}$$

where Z_0 is the system impedance and ω is the design frequency. The capacitances of the series and parallel varactors are

$$C_S = (x+1)C_0 \tag{4.31}$$

and

$$C_P = \frac{C_0}{x+1}, \tag{4.32}$$

respectively, where x can be any arbitrary number ranging from -1 to ∞, and

$$C_0 = \frac{1}{\omega Z_0}, \tag{4.33}$$

where Z_0 is the system impedance. It can be shown that the even-mode and odd-mode reflection coefficients of the variable transformer are

$$\Gamma_e = \frac{(j\omega L + \frac{1}{j\omega C_P}) - Z_0}{(j\omega L + \frac{1}{j\omega C_P}) + Z_0} = -\frac{1+jx}{1-jx}, \tag{4.34}$$

and

$$\Gamma_o = \frac{\frac{1}{Z_0} - (j\omega C_S + \frac{1}{j\omega L})}{\frac{1}{Z_0} + (j\omega C_S + \frac{1}{j\omega L})} = \frac{1-jx}{1+jx}, \tag{4.35}$$

respectively. Following that, the S_{11} and S_{21} of the variable transformer can be derived:

$$S_{11} = \frac{1}{2}(\Gamma_e + \Gamma_o) = -j\frac{2x}{x^2+1}, \tag{4.36}$$

and

$$S_{21} = \frac{1}{2}(\Gamma_e - \Gamma_o) = \frac{x^2-1}{x^2+1}. \tag{4.37}$$

It can be inferred from (4.36) that, as x varies from 0 to 1, the magnitude of the S_{11} increases from 0 to 1 whereas the phase of the S_{11} remains the same. From (4.31) and (4.32), when x varies from 0 to 1, C_S varies from C_0 to $2C_0$ whereas C_P varies from C_0 to $C_0/2$. That is, the required varactor tuning ratio for the type II variable transformer is only 2, which can be easily achieved using either semiconductor-based or ferroelectric-based varactors.

Note that, as can be inferred from (4.31) and (4.32), as C_S increases, C_P must decrease, and *vice versa*. The bias voltages of C_S and C_P, i.e. V_S and V_P as shown in Figure 4.3(c), exhibit the same behavior. Therefore, depending on the C-V characteristic of the varactors, the bias point can be chosen so that $V_S + V_P$ remains approximately constant as $|S_{11}|$ of the variable transformer varies. This reduces the number of the control voltages required by the type II variable transformer from two to one.

4.2.4 Impedance Tuner

An impedance tuner is designed at 2 GHz. The schematic of the tuner is shown in Figure 4.8. It consists of a two-stage phase shifter as described in Section 4.2.1 to achieve up to 180° phase variation, a type I variable transformer as described in Section 4.2.2, and a DC blocking capacitor to isolate the bias voltages of the phase shifter and variable transformer.

Using the last column of Table 4.1 with $Z_0 = 50\ \Omega$, the fixed inductance and maximum capacitance required for the varactors in the two-stage phase shifter are calculated to be 5.06 nH and 2.02 pF, respectively. As for the variable transformer, the design goal is to obtain an maximum impedance transformation ratio of 19

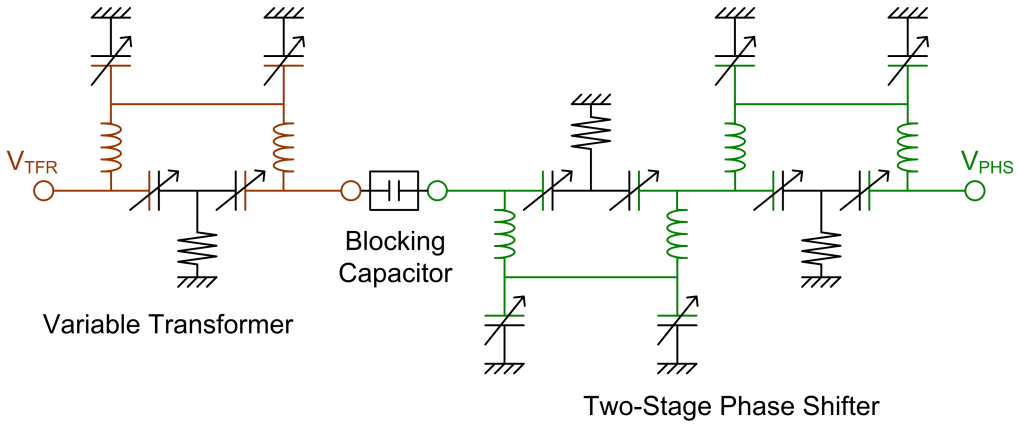


Figure 4.8: The schematic of the impedance tuner.

($|\Gamma| = 0.9$). Using (4.29), the normalized reference impedance z_T can be either 0.23 or 4.36. In favor of a smaller inductance value, $z_T = 0.23$ is chosen. Using the second column of Table 4.1 with $Z_0 = z_T \times 50\ \Omega$, the fixed inductance and maximum capacitances required for the varactors in the variable transformer are calculated to be 1.48 nH and 11.2 pF, respectively. For the varactors in both the phase shifter and variable transformer, tuning ratio of 2.618 is required.

To implement of the impedance tuner, chip inductors with nominal value of 4.8 and 1.5 nH from Coilcraft[1] (0201CS Series) are used for the fixed inductances in the phase shifter and variable transformer, respectively, whereas parallel-plate BST capacitors are used for the varactors. Simulation results using finite quality factor of 40 for the varactors and the S-parameters of the inductors provided by the manufacturer show that the achievable impedance transformation ratio is around 5.7 ($|\Gamma| = 0.7$). The simulated impedance coverage at 2 GHz is plotted in Figure 4.9(a). The maximum dissipation loss of the impedance tuner is approximately 3 dB, as shown in Figure 4.9(b).

[1]Coilcraft, Inc. (http://www.coilcraft.com/)

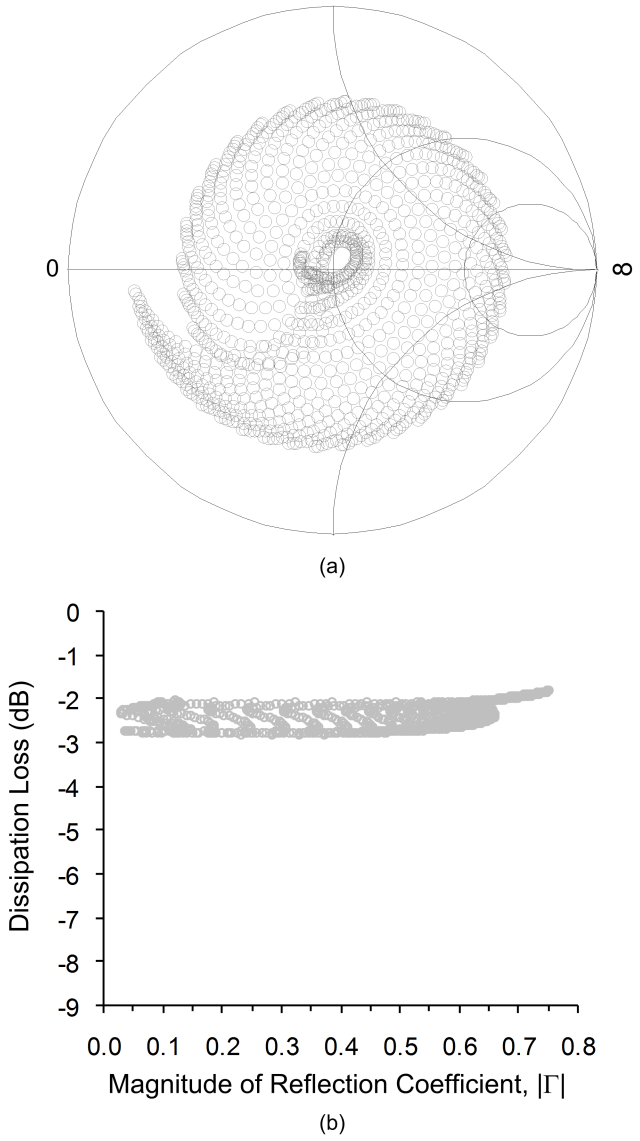


Figure 4.9: Simulated (a) impedance coverage and (b) dissipation loss of the impedance tuner.

4.3 Fabrication and Measurement

The impedance tuner designed in Section 4.2.4 is fabricated on a 430-μm-thick sapphire substrate. The bottom electrodes of the BST capacitors, which are composed of Ti/Pt (20/1000 Å), are first deposited. Next, BST thin film is deposited using Pulse Laser Deposition (PLD) technique with a 50/50 BST target ($Ba_{0.5}Sr_{0.5}TiO_3$) at 650°C temperature under 300-mTorr O_2 pressure. The measured film thickness is 250 nm. The top electrodes made of Pt (1000 Å) are then deposited. After that, the BST thin film is etched everywhere on the substrate except for the area where parallel-plate capacitors are formed.

Thin-film SiCr lines with a thickness of 100 nm are then deposited by sputtering for biasing purpose. Following that, the metal contacts composed of Cr/Au (200/5000 Å) are formed to connect the bias resistors to other circuitry. SiO_2 thin film with a thickness of 4000-Å is deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD) technique for passivation. Finally, the other metal traces of 2-μm gold are formed.

After the clean-room process is done, chip inductors from Coilcraft and blocking capacitors from Dielectric Laboratories[2] are mounted onto the substrate using silver epoxy. Photograph of the fabricated impedance tuner is shown in Figure 4.10. The overall circuit size is 4.3×1.2 mm^2.

The ferroelectric-based impedance tuner is measured using a network analyzer (Agilent E8364B). On-wafer measurement using ground-signal-ground (GSG) probes is performed. Bias voltages are applied through the probes using bias-tees. The bias voltages for both the phase shifter and variable transformer are swept from 0 to 18 V (3:1 tuning ratio for the BST capacitors is reached at 14 V).

[2]Dielectric Laboratories, Inc. (http://www.dilabs.com/)

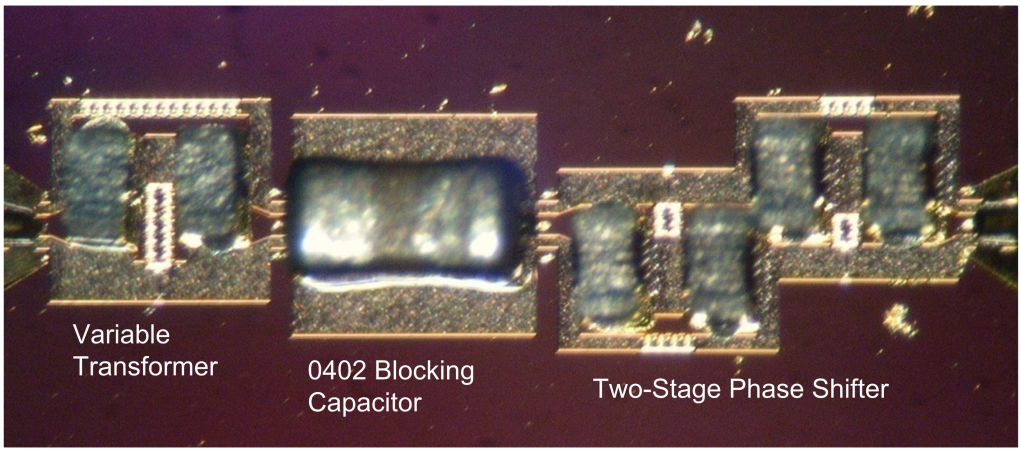


Figure 4.10: Photograph of the fabricated impedance tuner. Circuit size: 4.3×1.2 mm^2.

Measured impedance coverage and dissipation loss are plotted in Figure4.11. At 2 GHz, the maximum impedance transformation ratio achieved is approximately 4 ($|\Gamma| = 0.6$), which is less than that in simulation because the actual quality factor of the fabricated BST capacitors is lower ($Q = 33$ at 0 V). Also, due to the variation in the process and the values of the capacitance, the operation frequency of the impedance has deviated from the design frequency, which results in a smaller impedance coverage than predicted by simulations.

At 1.8 GHz, as shown in Figure 4.11(b), the measurement results are closer to the simulation results. Maximum dissipation loss at this frequency is approximately 5.5 dB.

Because of the broadband nature of the all-pass networks, the proposed impedance tuner may also be used at other frequencies. For example, the measurement results at 1.5 GHz show that the maximum impedance transformation ratio is 3.2 and the dissipation loss is less than 5 dB for all bias voltages, as presented in Figure 4.11(c). Equal coverage in the four quadrants of the Smith chart is observed.

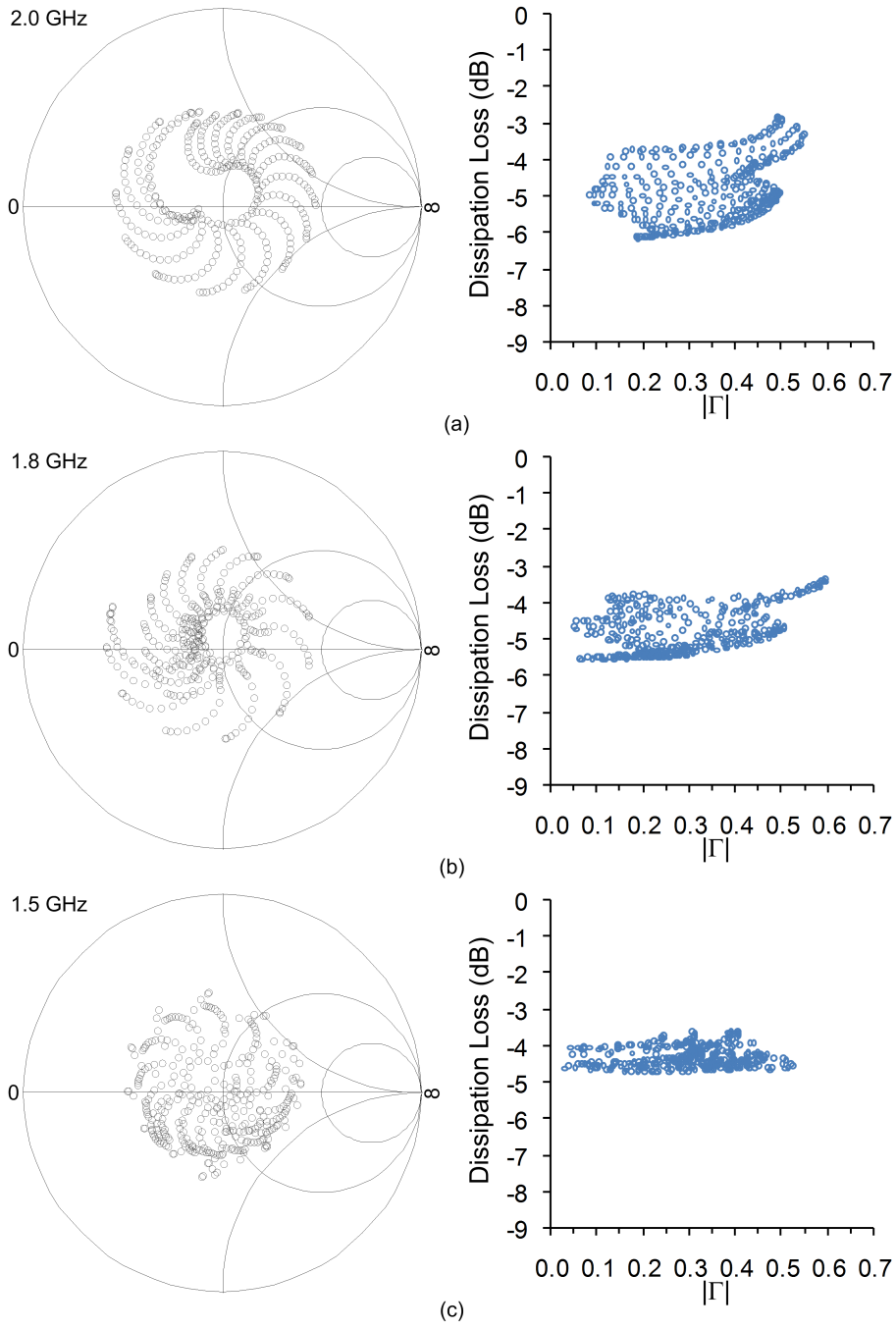


Figure 4.11: Measured impedance coverage and dissipation loss versus magnitude of reflection coefficient $|\Gamma|$ of the impedance tuner at (a) 2 GHz, (b) 1.8 GHz, and (c) 1.5 GHz.

4.4 Application in an Adaptive Matching System

As discussed in Section 4.1, the impedance tuner can be used in an adaptive matching system like the one shown in Figure 4.1 for applications such as automatic compensation of antenna impedance variations. Figure 4.12 illustrates the detailed block diagram of such an adaptive matching system. As can be seen, the adaptive matching system consists of three functional blocks: an impedance tuner, an impedance sensor, and a controller. The impedance tuner is composed of a variable transformer and a phase shifter, providing independent controls on the magnitude and phase of the reflection coefficient. The impedance sensor is implemented using a $\lambda/4$ transmission line with a characteristic impedance equal to the system impedance. The controller includes a logarithmic amplifier, a phase detector, and two integrators. The logarithmic amplifier and phase detector are used to generate the error signals, which indicate whether the matching condition is achieved or not. The error signals are then integrated for generating the control signals. Finally, the control signals are fed back to the variable transformer and phase shifter.

4.4.1 Impedance Tuner

The impedance tuner is divided into two functional blocks, i.e. the variable transformer and phase shifter. From a system perspective, it is desirable to have independent controls on the magnitude and phase of the reflection coefficient presented by an impedance tuner because this results in simpler control scheme. Therefore, the type II variable transformer described in Section 4.2.3 is most suitable for the impedance tuner implemented for the adaptive matching system. The phase shifter used here requires a 180° phase shift to achieve a 360° full angular coverage. Hence, a

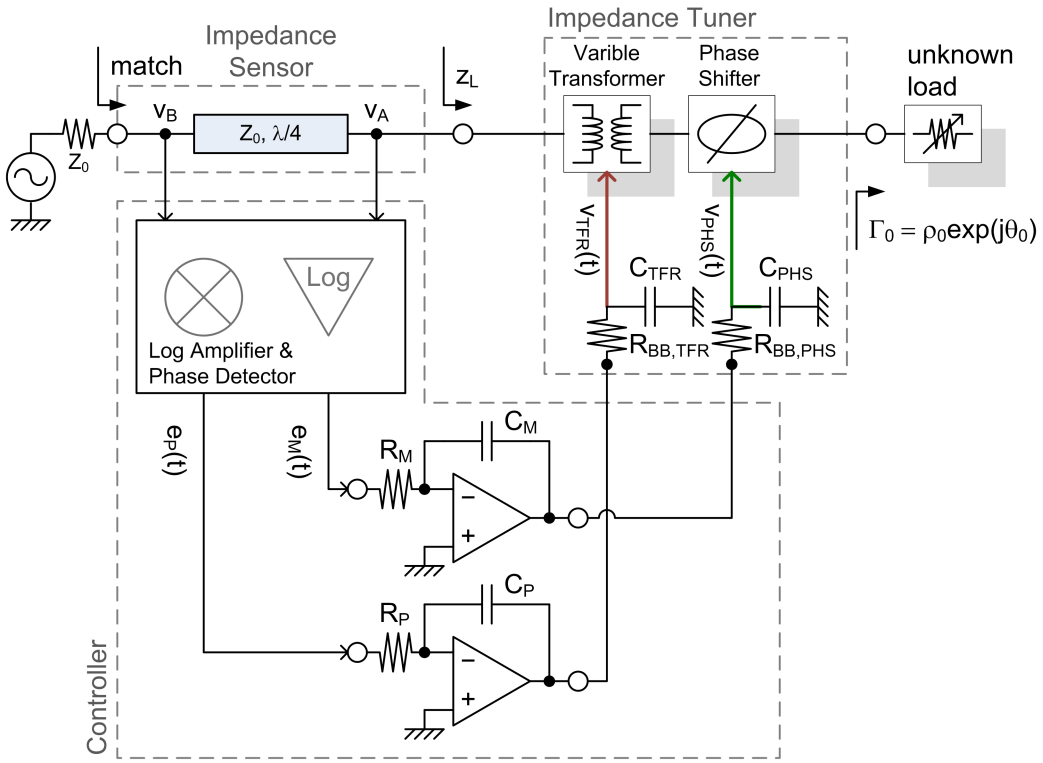


Figure 4.12: Detailed block diagram of the proposed adaptive matching system.

two-stage all-pass phase shifter described in Section 4.2.1 can be used. The schematic of the tuner is shown in Figure 4.13

Figure 4.14 shows the block diagram of the impedance tuner, where a few variables are introduced for the convenience of explaining how automatic matching can be achieved by the system. First, Γ_0 represents the reflection coefficient of the unknown load.

$$\Gamma_0 = \rho_0 \cdot e^{j\theta_0}. \tag{4.38}$$

Next, Γ_U represents the reflection coefficient of the unknown load after being transformed by the phase shifter.

$$\Gamma_U = \rho_0 \cdot e^{j\theta}, \tag{4.39}$$

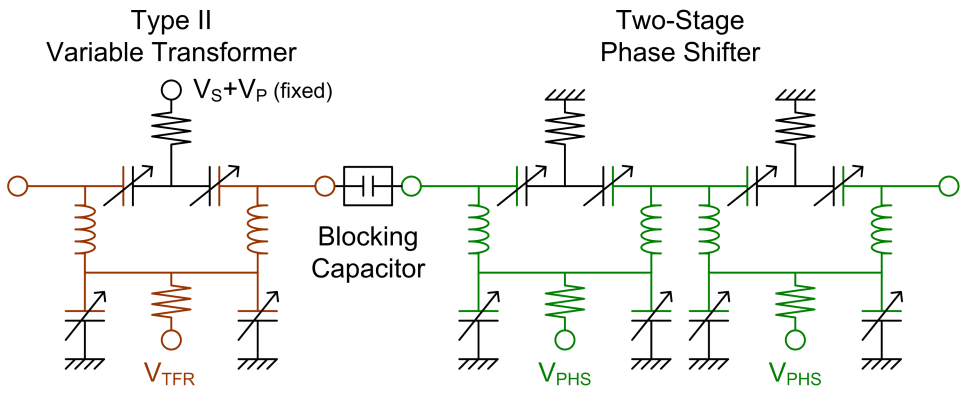


Figure 4.13: The schematic of the impedance tuner.

where

$$\theta = \theta_0 + 2\phi, \tag{4.40}$$

where ϕ is the phase shift introduced by the phase shifter. There is a factor of two in front of ϕ because the reflected signal passes through the phase shifter twice. Note that (4.39) and (4.40) imply that the $|S_{11}|$ of the phase shifter is zero, which is not completely true but an acceptable assumption because, as can be seen in Figure 4.6, the return loss of a two-stage all-pass phase shifter is higher than 20 dB over the range of the 180° phase variation. Finally, z_L represents the normalized impedance of the unknown load after being transformed by the impedance tuner. It is also the normalized impedance seen by the impedance sensor, as illustrated in Figure 4.12. It can be derived that

$$z_L = \frac{z_U + S_{11,TFR}}{1 - z_U\, S_{11,TFR}}, \tag{4.41}$$

where $S_{11,TFR}$ is the S_{11} of the type II variable transformer as in (4.36), and

$$z_U = \frac{1 + \Gamma_U}{1 - \Gamma_U}, \tag{4.42}$$

i.e. z_U is the normalized impedance of the unknown load after being transformed by the phase shifter.

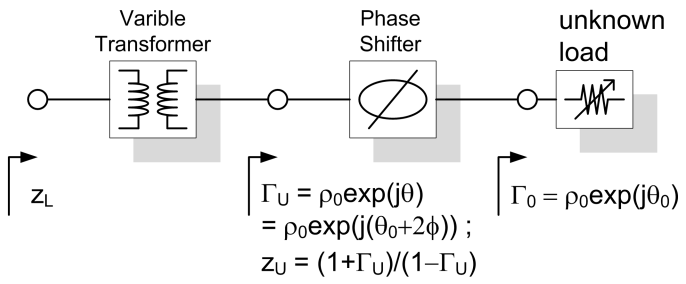


Figure 4.14: Block diagram of the impedance tuner. Γ_0 represents the reflection coefficient of the unknown load. Γ_U represents the reflection coefficient of the unknown load after being transformed by the phase shifter. z_L represents the normalized impedance of the unknown load after being transformed by the impedance tuner.

Using (4.41) and (4.36), it can be found that, if $|z_U| = 1$, then $|z_L| = 1$. That is, when the normalized impedance of the unknown load after being transformed by the two-stage all-pass phase shifter is unity ($|z_U| = 1$), the type II variable transformer has no effects on the magnitude of z_L. On the other hand, the phase of z_L can be controlled by the variable transformer. Based on this property, the goal of transforming the unknown load impedance to the system impedance can be achieved in two steps:

1. *Step One* – First, the phase shifter is adjusted until the magnitude of z_U is equal to unity, i.e. $|z_U| = 1$. As mentioned above, $|z_U| = 1$ always leads to $|z_L| = 1$.

2. *Step Two* – Next, the variable transformer is adjusted until the phase of z_L is equal to zero, i.e. $\measuredangle z_L = 0$.

As the two-step transformation described above is done, $z_L = 1$ is achieved and the matching condition is satisfied. The following sections will cover the design of the impedance sensor and controller for performing the two-step transformation.

4.4.2 Impedance Sensor

The impedance sensor is implemented using a quarter-wave transmission line. The transmission line has a characteristic impedance equal to the system impedance. Based on the node voltages (v_A and v_B) of the $\lambda/4$ line, one can uniquely determine the normalized load impedance (z_L) by the following equation:

$$z_L = j\frac{v_A}{v_B}. \tag{4.43}$$

Let's define

$$A \equiv \left|\frac{v_A}{v_B}\right| = |z_L| \qquad \text{and} \qquad \alpha \equiv \measuredangle\left(\frac{v_A}{v_B}\right) = -\frac{\pi}{2} + \measuredangle z_L. \tag{4.44}$$

When a matched load ($z_L = 1$) is connected to the impedance sensor, the node voltages v_A and v_B would have the same magnitudes and a 90° phase difference. That is,

$$A = 1 \qquad \text{and} \qquad \alpha = -\frac{\pi}{2}. \tag{4.45}$$

The above conditions can therefore be used to verify whether the matching condition is achieved or not.

The impedance sensor can also be implemented using lumped elements, e.g. a Π-network as shown in Figure 4.15, if a smaller circuit size is desired.

4.4.3 Controller

As shown in Figure 4.12, the controller is composed of a logarithmic amplifier, a phase detector, and two integrators. The output of the logarithmic amplifier is of the form

$$e_M = \ln(A), \tag{4.46}$$

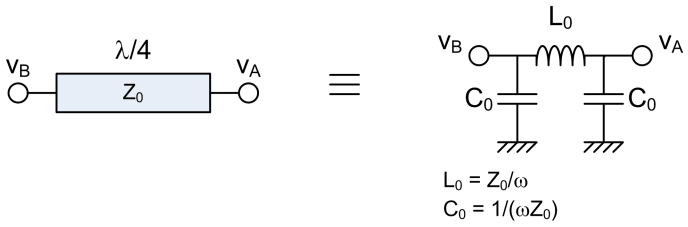


Figure 4.15: Lumped-element implementation of the impedance sensor can be used to replace the quarter-wave transmission line if a smaller circuit size is desired.

whereas the output of the phase detector is of the form

$$e_P = \cos\alpha. \tag{4.47}$$

The output signals of the log amplifier and phase detector, e_M and e_P, can be used as error signals, which are basically indicators on whether the matching condition is achieved or not. It can be shown that, when the conditions in (4.45) are achieved, both e_M and e_P become zero. The functions of the log amplifier and phase detector can be implemented using off-the-shelf components, e.g. AD8302 by Analog Devices[3].

Next, the error signals are separately fed into the two integrators to generate the control voltages, v_{PHS} and v_{TFR}, for the phase shifter and variable transformer, respectively. As shown in Figure 4.12, the integrators are implemented based on op-amps. The relations between the error signals and control signals are derived.

$$\tau_{PHS}\tau_M \frac{d^2}{dt^2} v_{PHS} + \tau_M \frac{d}{dt} v_{PHS} + e_M = 0, \tag{4.48}$$

where $\tau_{PHS} = R_{BB,PHS}C_{PHS}$ and $\tau_M = R_M C_M$. $R_{BB,PHS}$ is the bias resistance and C_{PHS} is the effective input capacitance experienced by the bias signal of the phase shifter. R_M and C_M are the input resistance and feedback capacitance of the

[3]Analog Devices, Inc. (http://www.analog.com/)

integrator in the loop for controlling the phase shifter, respectively. Similarly,

$$\tau_{TFR}\tau_P \frac{d^2}{dt^2} v_{TFR} + \tau_P \frac{d}{dt} v_{TFR} + e_P = 0, \tag{4.49}$$

where $\tau_{TFR} = R_{BB,TFR} C_{TFR}$ and $\tau_P = R_P C_P$. $R_{BB,TFR}$ is the bias resistance and C_{TFR} is the effective input capacitance experienced by the bias signal of the variable transformer. R_P and C_P are the input resistance and feedback capacitance of the integrator in the loop for controlling the variable transformer, respectively.

Note that, depending on the polarity of $\frac{d}{dv_{PHS}} e_M$ and $\frac{d}{dv_{TFR}} e_P$, it may be necessary to reverse the polarity of e_M and/or e_P so that the loops provide negative feedbacks instead of positive feedbacks.

4.4.4 Loop Dynamics

The adaptive matching system is constructed and modelled in Advanced Design System (ADS). The impedance tuner described in Section 4.4.1 is designed based on varactors with a quality factor of 50 at approximately 2 GHz. Large bias resistance of 10 kΩ is used to minimize the effect of bias resistors on the RF performance. The log amplifier and phase detector are modelled using SDD (Symbolically Defined Devices) components in ADS. The input resistances of the integrators, R_M and R_P, are set to 1 kΩ. The feedback capacitance C_M should be large enough so that the transient response of v_{PHS} is not underdamped. Otherwise, it may cause undesired modulation on the RF signal passing through the impedance tuner. Through simulation, C_M of 5 nF is chosen to ensure an overdamped response for the loop. As described in Section 4.4.1, the matching condition is to be achieved through a two-step transformation – first a transformation by the phase shifter to achieve $|z_U| = 1$, and next a transformation by the variable transformer to achieve $\angle z_L = 0$. Therefore, the speed of the loop for controlling the variable transformer should be slower than that for

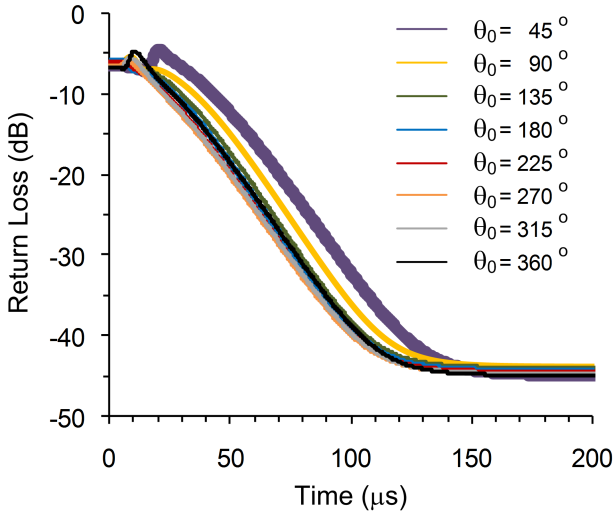


Figure 4.16: Simulation return loss versus time. The reflection coefficient of the unknown load (Γ_0) has a magnitude of 0.6 and various phase ranging from 45° to 360°.

the phase shifter. Because of this, the feedback capacitance C_P is chosen to be 50 nF, i.e. 10 times of C_M, so that the loop for controlling the phase shifter converges faster than the loop for controlling the variable transformer.

An envelope simulation is performed in ADS. In the simulation, the magnitude of the reflection coefficient of the unknown load, i.e. ρ_0, is set to 0.6, whereas the phase θ_0 varies from 45° to 360°. The results are shown in Figure 4.16, where the return loss of the unknown load after being transformed by the adaptive matching system is plotted versus time. Initially, the loops are open. Once the loops are closed at 5 μs, the return loss starts to increase, goes above 20 dB within 100 μs, and finally settles at approximately 45 dB for all eight different states. The return loss of 20 dB means that the reflected power is only one hundredth of the incident power, therefore indicating an excellent impedance match. Achieving 20-dB return loss within tens of μs is fast enough for applications such as compensating the input impedance variation of an antenna, which is a relatively slow process.

4.5 Conclusions

A general-purpose impedance tuner is proposed. The impedance tuner is composed of a variable transformer and a phase shifter, offering equal coverage in the four quadrants of the Smith chart. Designed based on an all-pass network topology, the phase shifter and variable transformer are analyzed and the design equations are derived.

An implementation of the impedance tuner is demonstrated based on parallel-plate BST varactors. The BST varactors are fabricated on a sapphire substrate. Chip inductors and blocking capacitors are mounted on the same sapphire board. The overall circuit size of the tuner is 4.3×1.2 mm^2. On-wafer characterization is performed using GSG probes. Maximum impedance transformation ratio of approximately 4 is observed. At 1.8 GHz, the dissipation loss is less than 5.5 dB for all bias voltages, which are within 18 V.

An adaptive matching system based on the proposed impedance tuner is presented. It targets the application of automatically compensating for the input impedance variation of an antenna. The adaptive matching system is a closed-loop system that consists of an impedance tuner, an impedance sensor, and peripheral control circuitries. The adaptive matching system is analyzed, designed and simulated. Simulation results show that the system is able to transforms a unknown load to the system impedance within 100 μs.

Although not discussed in the previous sections, the linearity of impedance tuners is also important when the tuners are used in wireless transmitters. The linearity of the proposed tuner can be improved by using the multiple-staked BST capacitors described in Chapter II. Since the tuning speed requirement on the varactors is

low for the application of antenna tuning, the linearity of the BST varactors can be improved with minimum degradation in the quality factor according to the linearity-improving technique discussed in Chapter II.

CHAPTER V

Conclusions

5.1 Thesis Summary

This thesis covers the design and implementation of impedance matching circuits that are adaptive to either transmit power level or operating environment. Specifically, the study is divided into two major directions: (a) linear and efficient PAs using tunable matching networks that are dynamically controlled according to the input power level, and (b) adaptive matching systems based on impedance tuning units to automatically compensate the input impedance variation of an antenna.

In this thesis, both semiconductor-based and ferroelectric-based varactors are used in the adaptive impedance matching circuits. In Chapter II, a linearity-improving technique is proposed, analyzed, and demonstrated on parallel-plate BST capacitors. Up to 16 dB improvement on IIP_3 is achieved, demonstrating the effectiveness of the linearity-improving technique. The tradeoff between the quality factor and tuning speed of the linearized varactors is studied, which is useful for providing design guidelines in applications that require fast tuning of the varactors.

Next, in Chapter III, a medium-power amplifier with a diode-based tunable matching network is designed, fabricated, and measured. The tunable matching network is dynamically controlled according to the input power level to present a

variable load impedance to the transistor. Measurement results show that both the linearity and power efficiency of the PA are improved when compared with a PA with a fixed matching network. This work demonstrates, for the first time, that both the linearity and power efficiency of a PA can be improved using tunable matching networks.

Finally, in Chapter IV, a general-purpose impedance tuner is proposed and discussed. The impedance tuner, consisting of a phase shifter and a variable transformer, is designed based on lumped-element all-pass networks. The design equations for the phase shifter and variable transformer are derived. An implementation of the impedance tuner based on parallel-plate BST capacitors is demonstrated. Compared to stub-based MEMS tuners, the lumped-element based tuner is preferable for cellular frequency bands because of its compact size. Finally, an adaptive matching system based on the impedance tuner for the application of automatically compensating antenna impedance variations is proposed, analyzed, and simulated.

5.2 Future Directions

5.2.1 Tunable Matching Networks for PA Performance Enhancement

In this thesis, the dynamic control of the tunable matching network is demonstrated using an instrument-based lab setup, i.e. PC and arbitrary waveform generators. One future direction would be replacing the instruments with control circuitries that are integrated within the PA modules and transceivers. One of the challenges for the control circuitries is to generate high enough voltage for biasing the varactors. Furthermore, in order to dynamically correct for the distortion, the speed of the varactor bias must be faster than the envelope of modulation signals (usually

MHz), which adds to the challenge in bias voltage generation.

Since it is difficult to generate high voltages in such a high speed, therefore, another future direction would be to bias the tunable matching network according to the average power level rather than the fast-varying instantaneous power level. This would reduce the requirement on the bias voltage generation. Tunable matching networks biased according to the average power level would still provide considerable power efficiency enhancement for PAs. Although it may not improve the linearity of PAs, however, there is usually large design flexibility at low power levels for PA designers to trade linearity for efficiency. Furthermore, controlling the tunable matching network according to the slow-varying average power level also relaxes the requirement on tuning speed of the varactors, which allows one to use linearity-improved BST varactors as described in Chapter II or MEMS varactors, taking advantage of their high linearity.

5.2.2 Impedance Tuners for an Adaptive Matching System

The design considerations of impedance tuners include insertion loss, impedance coverage, complexity of the control scheme, circuit size, and linearity. In this thesis, we have emphasized on the equal impedance coverage in the four quadrants of the Smith chart, compact circuit size, and simple control scheme. In the future, more efforts may be made toward low insertion loss and high linearity implementations.

To reduce the insertion loss of the impedance tuner, the varactors must exhibit high quality factors while providing reasonable tuning range. Besides continuing the efforts in improving the quality factor of ferroelectric-based varactors, one may also consider using MEMS varactors to take advantage of their low loss and high linearity.

The drawback that the tuning speed of MEMS varactors is low would be tolerable because the application of antenna impedance compensation does not require fast tuning.

The sources of nonlinearity in impedance tuners are the tuning elements, i.e. the varactors. To improve the overall linearity of the impedance tuner, one must use highly linear varactors. As described above, MEMS varactors should be considered because of their high linearity. Another option would be the linearity-improved ferroelectric varactors as discussed in Chapter II.

APPENDICES

APPENDIX A

Voltage Transfer Ratio and Overall Admittance

Applying the boundary condition that $i_{2e} = 0$, one can derive the normalized voltage across the center element, a_N, and the overall admittance of the composite capacitor, Y_N, as defined in (2.5) and (2.6), respectively, by solving (2.4). The closed-form formula can be obtained using mathematic software; however, they are complicated and cumbersome. Moreover, large number of elements is not practical in real circuits. Therefore, only the solutions for $N = 3, 5, 7,$ and 9 are listed below. a_N's are

$$\begin{aligned} a_3 &= \tfrac{-1+x}{1+3x}, \\ a_5 &= \tfrac{1+x+x^2}{1+9x+5x^2}, \\ a_7 &= \tfrac{-1+2x+3x^2+x^3}{1+18x+25x^2+7x^3}, \quad \text{and} \\ a_9 &= \tfrac{1+2x+7x^2+5x^3+x^4}{1+30x+75x^2+49x^3+9x^4}; \end{aligned}$$

Y_N's are

$$\begin{aligned} Y_3 &= Y\tfrac{3+x}{1+3x}, \\ Y_5 &= Y\tfrac{5+5x+x^2}{1+9x+5x^2}, \\ Y_7 &= Y\tfrac{7+14x+7x^2+x^3}{1+18x+25x^2+7x^3}, \quad \text{and} \\ Y_9 &= Y\tfrac{9+30x+27x^2+9x^3+x^4}{1+30x+75x^2+49x^3+9x^4}, \end{aligned}$$

where $x = Y \cdot Z = j\omega C \cdot R$.

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