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UNIVERSITY OF MICHIGAN

AUTOMATIC REDUCTION OF WIND TUNNEL DATA

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for the period

August 17, 1951 to November 17, 1951

Project
M-938

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Progress Report No. 3

AUTOMATIC REDUCTION OF WIND TUNNEL DATA

INTRODUCTION

This progress report will be chiefly concerned with the work of this project during the period August 17, 1951 to November 17, 1951. The general background and initial studies yielding the present sub-task and design criteria were presented in Progress Report No. 1. Progress Report No. 2 presented the specific progress and design under the sub-tasks of Report No. 1.

After conversations with Wright Field representatives, it was decided that each Progress Report should be complete in itself, instead of reporting progress by sub-tasks which would require reference to previous reports.

In general, the work during this reporting period has brought into being concrete designs for the specific components of the block diagram, Figure 1.

A minor design change in the information channel has taken place from that previously invisioned. This change now uses a closed loop balancing network for the DC output of the information channel back through the biasing section after the class A amplifier. This may be seen by comparing Figures 1 and 2. An additional closed loop was deemed necessary to

maintain amplitude control of the 2 kc carrier and is shown in Figure 17. A design change also was made in the previously reported class A AC amplifier, enabling the use of over 45 db of feedback and better gain control, Figure 7.

Progress and present status of each unit will be reported as sections of the block diagram, Figure 1, and subsidiary units, such as the 2 kc carrier, 400 cycle power, DC operational amplifiers, regulated B^+ supplies, and operational procedures for the use of this equipment.

BACKGROUND

This system of data reduction will use analogue methods of computation for calculation of desired measurements in wind tunnel work. The system will take the output of sensing units, operate on them, correct for tares, position, etc., and produce either the desired measurement or co-efficient to be applied to some type of DC voltage sensing recorder. It is thought that it might be valuable to apply a digital conversion to this analog output, but this is not part of this contract.

In studying a sample computation, let us assume that we have two strain gage elements on a cantilever sting of a balance system. The output of these two units will be proportional to moments while the desired measurements are force and center of pressure. Each of these strain gage elements will become the end instruments for a separate channel of

information. The gages will be incorporated into bridges, operated with a 2 kc carrier and the output will be an amplitude modulated signal with a 180^{o} phase reversal for negative or positive forces. Figure 3 is a block diagram of this system.

This signal will be amplified through the class A amplifier (reference Figure 1) of which the gain control will represent a composite of constant multiplying terms determined by calibration for each new test set-up. This composite multiplying term can be determined by applying a known force and varying the gain of each channel until its output directly represents the applied force or moment.

The output will be summed with a carrier so that the total output will be amplitude modulated without phase reversal. This summed signal then will be rectified directly. At the same time, a carrier equal to that summed in will be rectified through a separate channel and subtracted from the above rectified signal. This yields a DC voltage proportional to the actuating quantity times a lumped constant of the system.

This DC signal will be applied through weighting factors to a DC operational amplifier used for summing the two hypothetical parallel channels. The weighting factors will be determined by the position from a reference point on the sting, tares, tunnel corrections, and the decision of whether center of pressure or force is desired. The output of the DC operational amplifier will be the desired quantity. It is possible

to perform both calculations simultaneously by utilizing two DC amplifiers, as shown schematically in Figure 3.

Balance in normal strain gage bridges and other sensing units will be accomplished in two steps. The first will be the initial correction which will be applied directly to the strain gage bridge to bring the zero point within the limits of the automatic balancing system and will be manual in the initial test set-up. The second step will take any normal unbalances due to temperature and other causes and correct for them by changes in the bias voltage. This will be accomplished, only when the channel is not computing, by sensing the DC output of the rectifiers, chopping and amplifying the error signal to a servo-motor that will vary the bias to bring the error signal to zero.

The DC operational amplifiers will have their own automatic AC balancing loop.

INFORMATION CHANNEL

60 CPS PARALLEL "T" FILTER

The problem of eliminating 60 cps pick-up from the output signal of the sensing unit was considered important enough to take precautionary steps before any trouble was experienced. It was realized that any pick-up originating in the sensing units or their associated leads would not modulate the 2 kc carrier but would simply be superposed upon it. This meant

that a filter which had a very sharply tuned null frequency would be required because no appreciable attenuation could be tolerated in the neighborhood of the carrier frequency.

The filter appearing to have the desired characteristics was a parallel "T" filter tuned for 60 cps. This type filter has a very sharp null at the chosen frequency, but the attenuation at frequencies differing fron the null frequency by a factor of three or four is very slight. Since it was also decided to place this filter as far forward as possible in the information channel, namely, between the input transformer and the class A amplifier, a 60 cps parallel "T" filter having the proper impedence was designed. The schematic of this filter is shown in Figure 4.

As can be seen in the circuit diagram, this filter has two variable resistors which are used to tune the filter for 60 cps. These two controls are varied by means of screwdriver adjustments on the exterior of the can in which the filter is mounted. This method of mounting was chosen to eliminate the possibility of accidentally detuning the filter once it is properly adjusted.

The frequency response of the parallel "T" filter is shown in Figure 6. It has a 60 cps attenuation of approximately 60 db while attenuating frequencies greater than 1 kc by the constant amount of approximately 2.5 db. Thus the side-bands for any signal will be attenuated very little in passing through the filter.

A question may arise concerning 120 cps pick-up. It is true that the filtering action is relatively poor at this frequency, but the magnitude of any pick-up of this frequency will probably be small compared to the magnitude of the 60 cps pick-up.

CLASS A AMPLIFIER

Preliminary investigations into the output voltages of the sensing unit led to the estimation that the maximum output would be of the order of 10 millivolts. Hence, assuming that the desired maximum input to the DC operational amplifiers be of the order of 50 volts, the desired gain of the class A AC amplifier would have to be 5000, or 74 db. This led to the design of a class A amplifier reported in Progress Report No. 2 in which the servo balancing was accomplished in the sensing unit bridge circuit. It has been found since then that this method of balancing is not feasible, in the case of an automatic balancing system, due to the fact that both the amplitude and phase must be balanced simultaneously to obtain a null. Also, the voltage level at which balancing was to have been accomplished was so low that the noise problem became appreciable. The design of the new balancing is described in the Error Biasing and the Background sections of this report.

The above-mentioned redesign of the balancing loop and the decision to use an input transformer, which has a turns ratio of 1:10 and has its secondary electrostatically shielded

from the primary, have necessitated a redesign of the class A amplifier. In making this redesign, it was decided to include the gain control in the negative feedback loop of the amplifier by varying the amount of negative feedback.

The open-loop frequency response of this redesigned amplifier without the input transformer is shown in Figure 8. The maximum open-loop gain is 70.8 db at 1500 cycles. Including the input transformer, the overall gain of the class A amplifier is approximately 90 db. This is 15 db more gain than necessary and will be used as the minimum amount of feed-back yielding a flat frequency response over a much greater range than that required by the expected band width.

With this redesign, the lower open-loop gain has allowed the use of fewer stages, resulting in increased stability. This increase in stability has made it possible to use a design of the feed-back loop in which the feed-back may be varied from 15 db to 45 db.

In Figure 8, the frequency response of both the open loop and the closed loop systems with the maximum desired feed-back of 45 db are shown. The frequency response was not carried below 10 cps due to a lack of test equipment that would yield accurate input signals and readings below this frequency. However, the stability of the prototype was checked using 55 db of negative feedback and no oscillations occurred. With this margin of safety, it is reasonable to expect this system to remain stable for normal changes of tube characteristics and

circuit variations.

The new class A amplifier is shown schematically in Figure 7. The gain control is in the cathode circuit of the first stage. Minimum overall gain is obtained when the negative feedback is fed directly into the cathode, and maximum gain when the negative feedback is fed through a resistor to ground. The cathode follower output stage was added to permit the amplifier to work into the prescribed loads without distorting the output signal. The input impedance of the demodulator reflected back to the amplifier is 62,500 ohms. But this is in parallel with the feedback loop which has an impedance of approximately 50,000 ohms, hence the total load impedance has a constant value of approximately 28,800 ohms. This is small compared with the 200,000 ohm plate resistor on the last amplification stage, hence the impedance matching stage was added.

In the expected operating frequency range, the maximum undistorted output is approximately 60 volts, which is well beyond the maximum desired input voltage to the operational amplifier, namely 50 volts.

It must be kept in mind that the gain of the class A amplifier must remain fixed after the system has been balanced, since the class A amplifier is no longer in the closed loop and any changes in gain will appear as a change in error signal. It is expected that this will introduce no hardship since the gain in the class A amplifier will be set during calibration

and will be allowed to remain at that value over a relatively long period of time, whereas the balance circuit will be activated before and after each run.

BIAS SUMMING AND PHASE SHIFTING

The output of the sensing units will have a phase reversal of 180° when passing through the zero actuating balance point. However, the diode bridge rectifier is not a phase sensitive device; its DC output will have the same polarity regardless of the phase of the input AC signal. It is therefore necessary to add a 2 kc carrier as bias at the output of the class A amplifier (Figure 9). This bias carrier will be in phase with the reference, and of sufficient amplitude to keep the input to the rectifier in phase with the bias carrier regardless of the phase of the class A amplifier output, thus yielding a biased signal that does not require a phase sensitive rectifier.

The DC output of the diode-bridge rectifier will be linearly proportional to the magnitude of this biased signal. The DC equivalent of the 2 kc bias carrier is obtained by applying the 2 kc bias carrier to a separate diode bridge. This DC output is then subtracted from the DC equivalent of the biased signal giving a DC voltage proportional to the input signal.

Due to the possibility of small phase shifts occurring in the class A amplifier and the phase shift in a Schaevitz transformer, it was necessary to insert a passive phase shift

network (Figure 5) into the bias circuit. By means of this adjustable network the phase of the bias can be adjusted during calibration so that it is identical with the output signal of the class A amplifier. The phase shift network has an attenuation factor of two. This loss remains approximately constant for all phase settings. The range of phase angle available is approximately zero to 180°.

At present, it is believed that the maximum output voltage of the class A amplifier will be of the order of 50 volts; therefore, the bias circuit is designed to provide a maximum bias of 60 volts. It is planned, however, to incorporate an attenuator in the bias circuit to facilitate reducing the bias, if this seems advisable.

DIODE BRIDGE RECTIFIERS

To rectify the amplitude modulated 2 kc output of the class A amplifier so that the modulating signal could be obtained, a full wave rectifier was inserted. The problem was to find a rectifier which would be linear over the desired range of signal voltages, namely, five to fifty volts. The unit that was finally chosen was the Sylvania 1N40 Germanium Diode Bridge. After testing the diode bridge with a series of resistive loads across it, it was found that 10,000 ohms appeared to give the best linearity characteristics. Figure 10 shows the linearity characteristics with a 10,000 ohm resistive load across the bridge. With a 2 kc input, the linearity is

better than one percent between input voltages of two and fifty volts. This figure (Figure 10) represents two 1N40's chosen at random. The agreement between the two units tested is better than the plotting accuracy.

Adding a carrier to the output of the class A amplifier insures that the signals being rectified will remain within the linear range of the diodes.

CLASS AB_1 AMPLIFIER

The class AB_1 amplifier, Figure 11, consists of three stages of voltage amplification, a phase inverter stage, using two type 12AU7 tubes, and a push-pull power amplifier stage, using two type 6AQ5 tubes. An impedance matching transformer is used at the output.

Each information channel has one AB_1 amplifier driving the variable phase of the servo-motor in the error balancing loop.

Figure 12 is a graph of the frequency response of this amplifier taken with a B^+ voltage of 250 volts and working into a load of 250 ohms. This response is flat from 100 cps to 10 kc. The amplifier will be operated at 400 cps.

The characteristics of this amplifier are not changed appreciably with a B^+ of 300 volts. Hence, to simplify the power supply requirements, it has been decided to operate with a B^+ of 300 volts.

The DC input circuit will use sufficient derivative and

integral network, before the 400 cps chopper, to stabilize the balancing loop.

SERVO MOTOR

After examining the characteristics of several motors, it has been determined that the Bendix Eclipse-Pioneer CK-2 motor (Signal Corps, No. MO-18A) is the most suited for the job at hand.

The CK-2 is a two-phase 400-cycle motor rated at 26 volts on the fixed phase and 0-40 volts on the variable phase.

The measured impedences of the two windings at several frequencies are tabulated below:

FREQUENCY	IMPEDENCE IN OHMS	
	Fixed Phase Terminals 2-4	Variable Phase Terminal 1-3
2000	123.4	520
1000	68.0	295
400	40.7	186

It is noted that at higher frequencies, the impedences of both windings are increased. Since the torque of the motor is dependent on current, a higher voltage is required at the higher frequencies for the same torque output. Nevertheless, the sensitivity of the system at 2000 cycles is still very acceptable, even though the motor is operated at five times its designed frequency.

With 26 volts on the fixed phase of the motor, the voltage

required on the variable phase to drive a 20,000 ohm Micro-pot is approximately 9 volts at a frequency of 400 cps and about 15 volts at a frequency of 2000 cps.

At present, the CK-2 motor drives a 20,000 ohm Micro-pot in the error biasing bridge, Figure 13, through a reduction gear of about 200:1. The torque is transmitted through a clutched shaft 8" long. The length of the shaft enables the potentiometer to be driven by the motor without having the balancing bridge influenced by pick-up due to the high power level at the motor. The clutch provides protection for the Micro-pot when a large unbalance causes the motor to drive the potentiometer to its stops. At this point, the clutch, which can be adjusted to any given tension, allows the motor to continue turning without placing undue strain on the mechanical stops of the Micro-pot.

ERROR BIASING BRIDGE

The error biasing bridge will obtain a 2 kc carrier from the bias control in phase with the signal being applied to the bias summing circuit. This signal will be applied across an ordinary resistance bridge, as shown in Figure 13. Three arms of this bridge will be 10,000 ohm resistors; the fourth arm will be a 20,000 ohm Micro-pot. This potentiometer will be used only as a variable resistance driven by a servo motor previously described.

When the variable resistance is at its mid-point, the

bridge will be in balance and no output will be applied to the bias summing transformers. When the Micro-pot is either less than or greater than the other arms of the bridge, the amplitude of the output signal will depend on the magnitude of the unbalance and will be applied to the summing circuit. The phase of this signal will be a function of the direction of the unbalance, yielding either zero or 180^{0} phase relationship with the 2 kc carrier.

When the class AB_1 amplifier receives an error signal from the diode detector, an amplified error signal is applied to the motor in a phase such that rotation of the motor will take place, driving the variable resistance to unbalance the bridge; this unbalance will be of a phase and amplitude to be summed in the bias summing transformers thereby reducing the error voltage to zero.

DC OPERATIONAL AMPLIFIER

In order to carry on the necessary computations in the wind tunnel data reduction system, it is necessary to employ a number of DC operational amplifiers similar to those used in electronic differential analyzers (analog computers). At first it was thought that REAC (Reeves Electronic Analog Computer) amplifiers, which incorporate the necessary AC drift stabilizing loop, could be used, and one such amplifier was ordered for test purposes. The DC performance of the amplifier was satisfactory, but the AC frequency response (see Figure16)

was not considered good enough for the ultimate requirements of the wind tunnel system. Hence, a new DC operational amplifier was designed.

Before describing the new amplifier, it might be well to review briefly the theory of operational amplifiers. The block diagram in Figure 14 shows the essential components of the operational amplifier; a high gain DC amplifier (gain= $-\mu$, an input impedance, Z_i and a feedback impedance Z_f).

The output voltage e_2 is by definition equal to $-\mu e'$, where e' is the input to the high gain amplifier. If we neglect the current into the high gain amplifier (i.e., neglect any grid current of the input tube, it follows that $i_1 = i_2$. Hence:

$$\frac{e_1 - e'}{Z_i} = \frac{e' - e_2}{Z_f} \qquad (1)$$

Substituting $e' = -\frac{e_2}{\mu}$ into the equation (1), we can solve for the output voltage e_2 as a function of the input voltage e_1 . Thus

$$e_2 = -\frac{Z_f}{Z_i} \frac{\mu}{\mu + (1 + \frac{Z_f}{Z_i})} e_1 \qquad (2)$$

If $\mu \gg 1 + \frac{Z_f}{Z_i}$, then

$$e_2 \cong -\frac{Z_f}{Z_i} e_1 \qquad (3)$$

which is the fundamental equation governing the behavior of the operational amplifier. If Z_i and Z_f are resistors R_i and R_f

respectively, then the operational amplifier multiplies any input voltage e_1 by a constant $-\frac{R_f}{R_i}$. If Z_i is resistor R and Z_f is a capacitor C, then

$$e_2 = -\frac{Z_f}{Z_i} e_1 = -\frac{1/Cp}{R} e_1 = \frac{1}{RC}\int e_1\,dt \qquad (4)$$

that is, the operational amplifier output voltage e_2 is the time integral of the input voltage e_1. By introducing any number of input voltages through separate input resistors, the operational amplifier can be used to sum voltages.

The above analysis assumes that $\mu \gg 1 + \frac{Z_f}{Z_i}$ in order for equation (3) to hold. Actually, the DC amplifier gain μ is a function of frequency ω, or more generally, a function of the operator p. For high frequencies the gain μ will fall off until it is equal to or less than $1 + \frac{Z_f}{Z_i}$ and we must return to the original equation (2) to study the stability of the system. When $\mu(P) = -(1 + \frac{Z_f}{Z_i})$ the denominator of equation (2) becomes zero. This means that if we make a Nyquist plot in the complex μ plane to determine stability, the critical point will be $-(1 + \frac{Z_f}{Z_i}) + j\,0$. According to Bode's minimum phase shift criteria, the critical point will not be encircled in the μ plane and we will have a stable system if the amplitude of $\mu(j\omega)$ does not fall off faster than 12 db per octave before $\mu < 1 + \frac{Z_f}{Z_i}$. The most feedback occurs when $Z_f = 0$ so that our DC amplifier frequency response should be designed to fall off at less than 12 db per frequency octave until $\mu < 1$. In order to provide a safe margin of

stability, the order of 8 db per octave or less is desirable.

The general design procedure, then, is to decide first on a DC circuit for the amplifier; after the amplifier is built, capacitors or resistor-capacitor combinations are inserted into the circuit in the proper locations so that the gain μ falls off at a rate considerably less than 12 db per frequency octave.

The DC amplifier circuit which was finally arrived at is shown in Figure 15. There are three stages of amplification, giving the necessary 180° phase shift, and a cathode follower output is provided. The gain of the amplifier is 90 db or about 30,000. The circuit employs two 5691 twin triodes (these are RCA red base tube equivalents of the 6SL7) for the DC balancing circuit and the three stages of amplification. The cathode follower output is provided by a 12SN7, which can operate into a 20K load. Provision is made in the second half of 5691#1 for manual or automatic (drift-stabilized) balance. In order to check the balance of the amplifier a 28 volt relay is provided. When energized, this relay disconnects the external feedback and input impedances Z_f and Z_i and introduces a 40:1 ratio of feedback to input resistance. One percent precision resistors are used throughout the amplifier. The power input to the amplifier include 12 volts DC for filaments and B supply voltages of $+300$, -190, and -350.

The frequency response of the DC amplifier is compared with the REAC amplifier in Figure 16. The response of the Air Comp Mod 4 computer amplifier falls off considerably less than

12 db per octave over the entire range down to zero db, and over the lower region of the curve (which is the most important, since $/+\frac{Z_f}{Z_i}$ is seldom greater than 20 db) the response falls off at approximately 6 db per octave. Square wave response of the operational amplifier with all possible ratios of Z_f/Z_i indicates complete stability with practically no overshoot in the transient.

The proposed circuit for the AC drive stabilizing network is similar to one already being used.* An analysis of drift-stabilization along with the circuit itself will be presented in the next Progress Report.

SUBSIDIARY UNITS

2 KC CARRIER

The oscillator design for the 2 kc carrier is the Wien Bridge or resistance-capacitance circuit, which has high stability in amplitude and frequency. In Progress Report No. 2 the idea was presented that the amplitude control of this unit

*Ref. Howe, Howe & Rauch, Application of the Electronic Differential Analyzer to the Oscillation of Beams, Including Shear and Rotary Inertia, External Memorandum UMM-67 (January 1951, University of Michigan Engineering Research Institute).

was sufficient for the accuracy required of the equipment. It has been decided that increased accuracy would be gained which would help insure the overall design accuracy of 1% if a closed loop servo were added to the 2 kc oscillator section.

The fundamental idea in this new control involves driving a triode to cut off and filter out all frequency components but the first harmonic to yield a sine wave of good amplitude stability. This would then drive a power amplifier of 6L6's in push-pull parallel. The output would be rectified, compared to a DC standard and the difference applied to a DC amplifier, the last plate of which would control the plate voltage of the over-driven triode sections, completing the loop and controlling the amplitude of the slicer (over-driven triode) output. Figure 17 presents a block diagram of the arrangement.

The power amplifier, consisting of six 6L6 type tubes in push-pull parallel and its B + supply has been constructed and will be tested during the first week of December 1951, Figures 18 and 19. The general circuit of the oscillator, Wien Bridge, has been built and tried in a power oscillator, which is being used to supply 2 kc power for test purposes. The description of this power oscillator was given in Report No. 2. The final 2 kc oscillator, slicer, low pass filter, drivers for the power amplifier, rectifier, comparitor circuit, and DC amplifier have been designed and are in process of construction. The exact circuit has not been tested sufficiently to be presented at this time.

400 CPS POWER

The 400 CPS oscillator will use the same circuit design as that used for the 2 kc carrier, i.e., Wien Bridge. The system will differ in that there will be no feedback loop for amplitude control.

The amplitude control on the 400 cycle power supply is not critical and can effect the information channel only by reduction of sensitivity in the balancing loop, which might permit a larger error. The sensitivity of this loop is an order of magnitude greater than that required to reduce a given error to such value that it is well within the design accuracy. Therefore, the normal amplitude control of the oscillator will be sufficient.

The overall system will be composed of a Wien Bridge oscillator, class A amplifier and buffer stage, and a class AB_2 power amplifier, consisting of beam power tubes in push-pull parallel. The oscillator design has been completed and construction should be finished the first week of December 1951. Further tests are required to determine the power requirement of the balance motors and the 400 cycle choppers to complete the class AB_2 power amplifier.

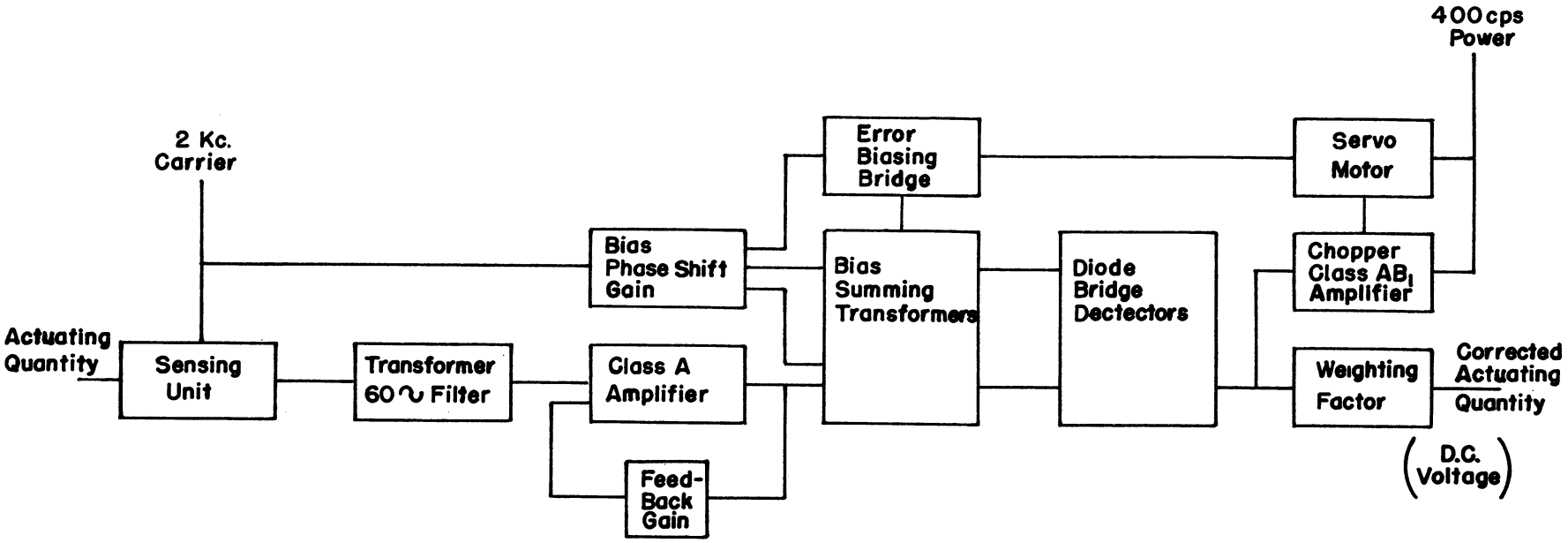
TEST EQUIPMENT

A class AB_2 power amplifier, Figure 20, was designed and built to obtain the necessary power and impedence matching required to conduct tests on the CK-2 servo motor, balancing bridges, and other components or combinations of components of

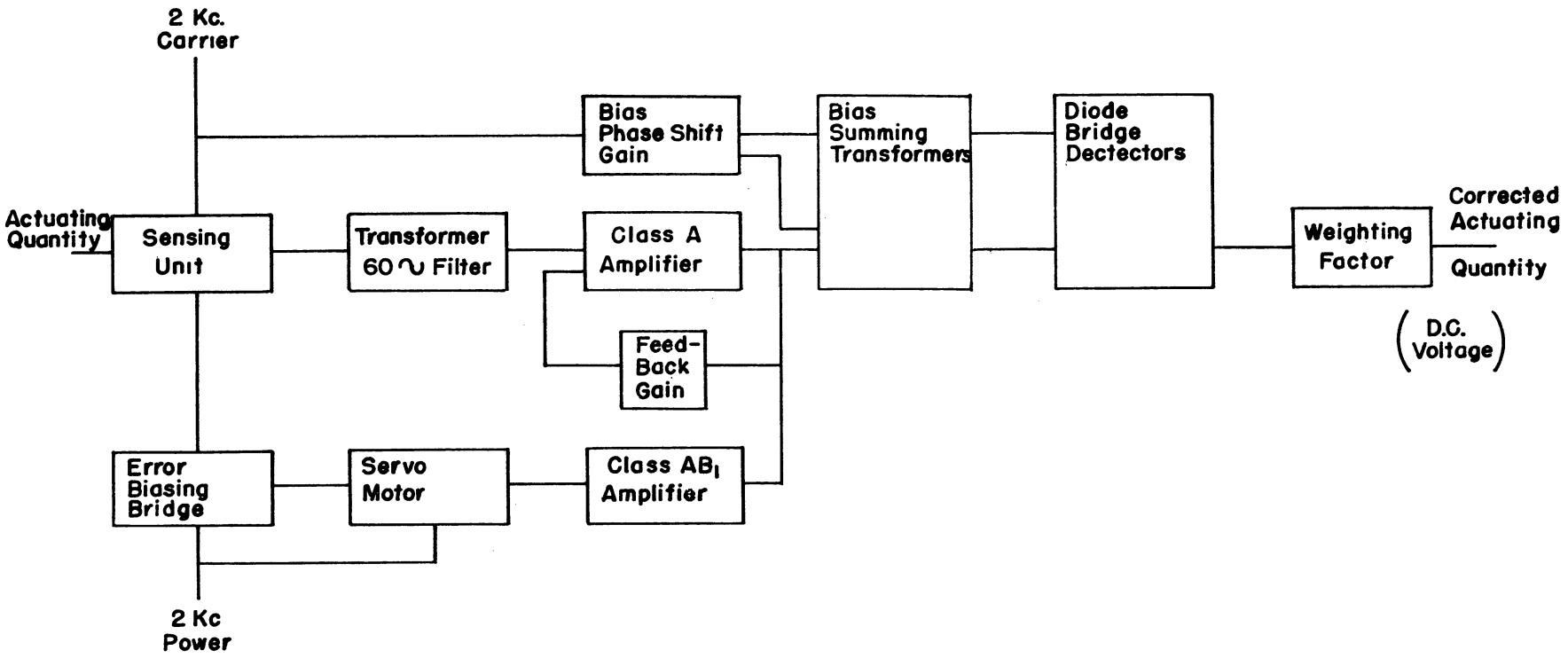
the information channel.

This amplifier has a voltage amplification stage, a phase-inverter stage, and cathode follower inputs to two 6L6's in push-pull.

With a resistive load, the power of this amplifier is 47 watts. For an inductive load, the maximum output is somewhat less.

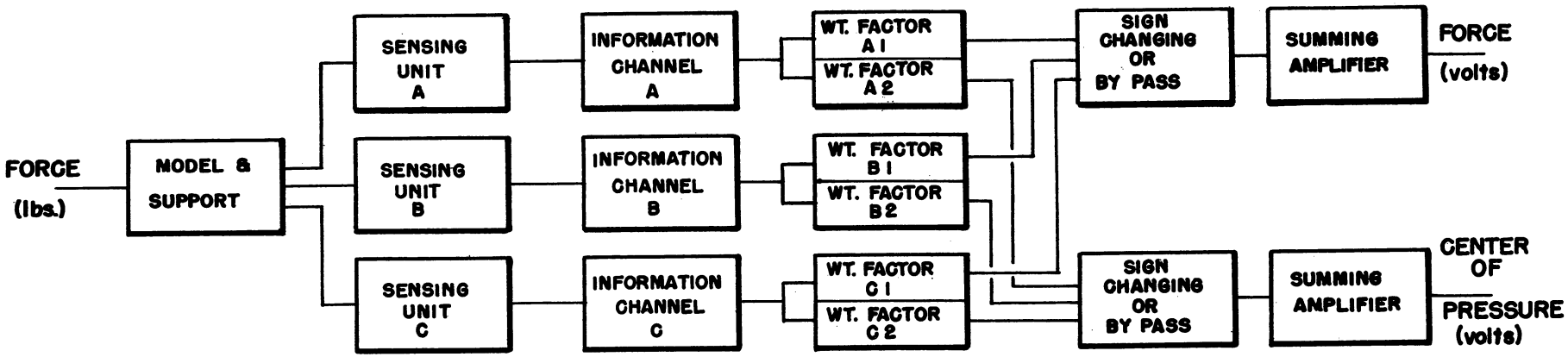


BLOCK DIAGRAM OF ONE CHANNEL OF INFORMATION
MARK I MOD. 2
FIGURE 1.

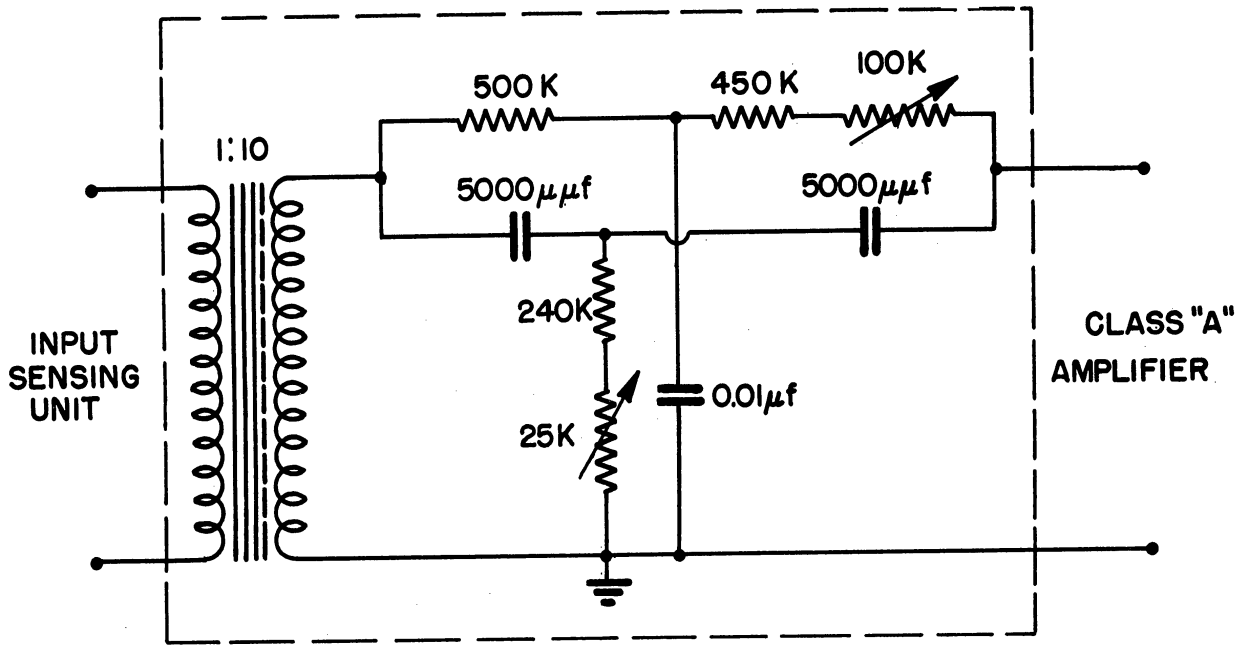


BLOCK DIAGRAM OF ONE CHANNEL OF INFORMATION
MARK I MOD. I

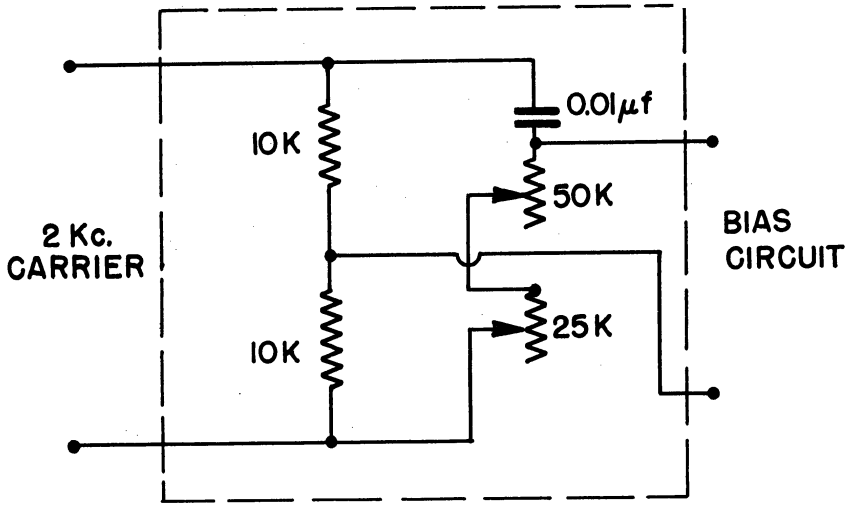
FIGURE 2



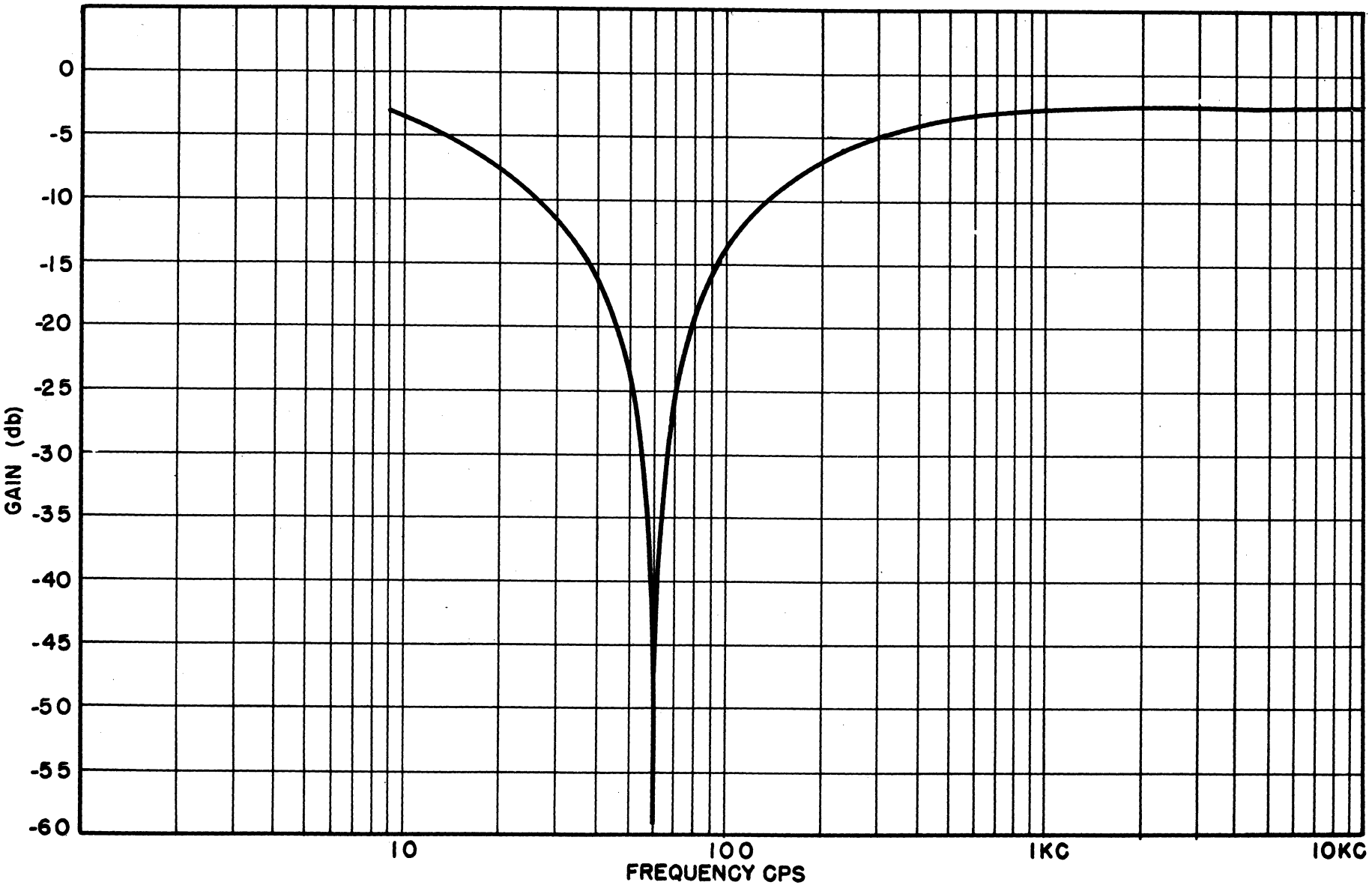
BLOCK DIAGRAM OF FORCE SYSTEM
FIGURE 3



"60" CPS PARALLEL "T" FILTER
FIGURE 4

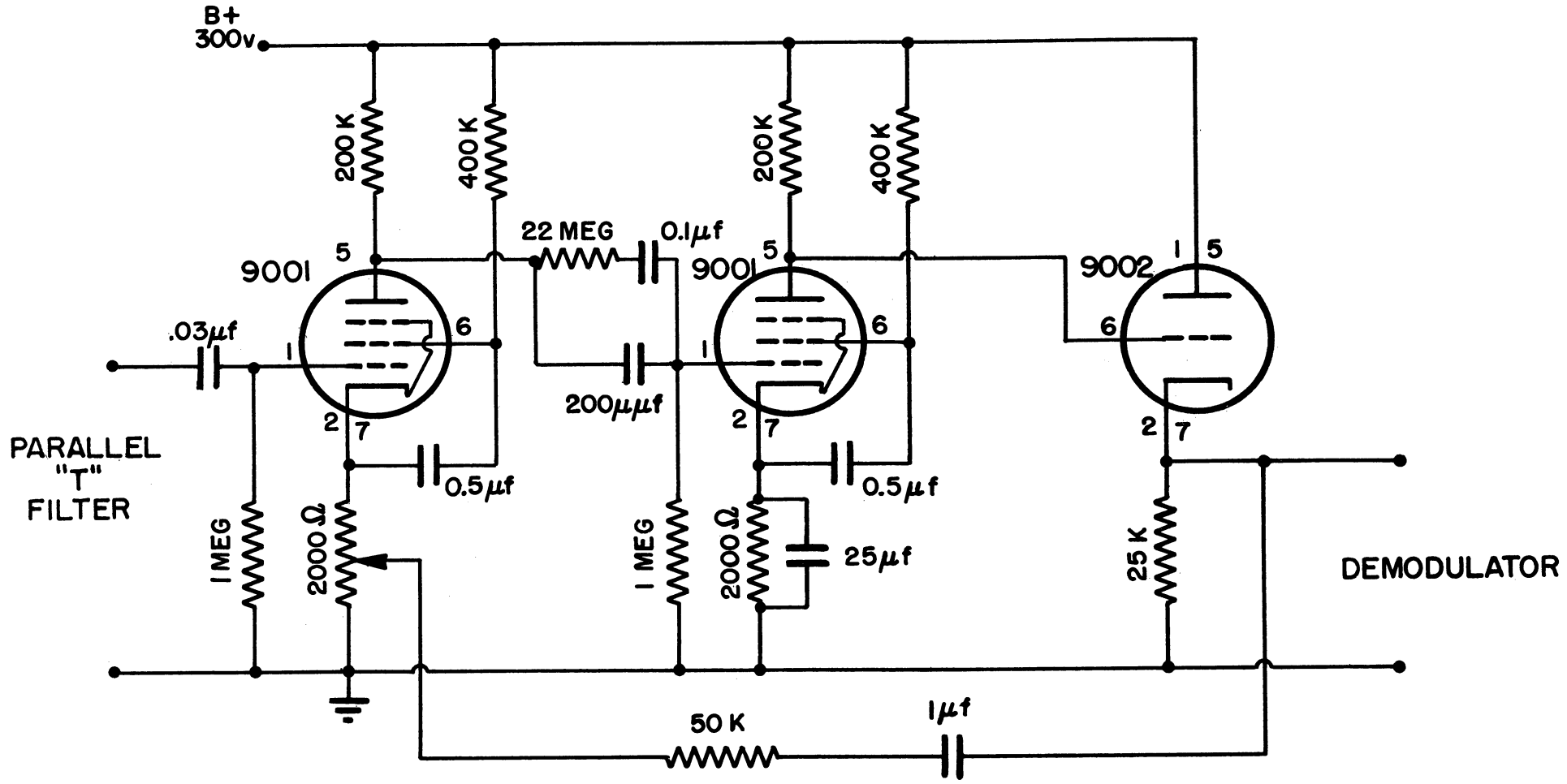


PHASE SHIFTING CIRCUIT
FIGURE 5

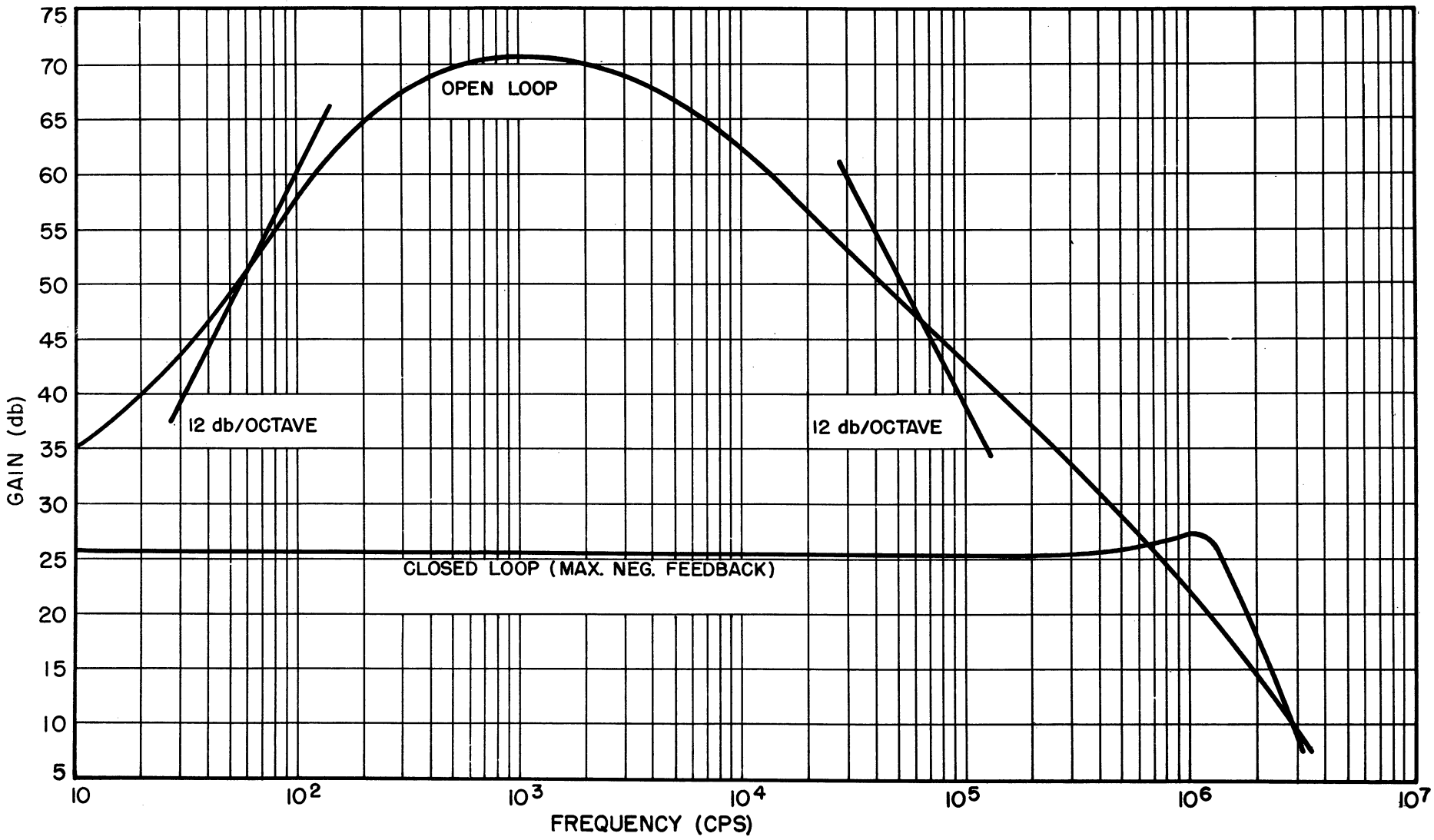


FREQUENCY RESPONSE 60∿ FILTER

FIGURE 6



CLASS A AMPLIFIER
FIGURE 7



FREQUENCY RESPONSE OF CLASS A AMPLIFIER
FIGURE 8

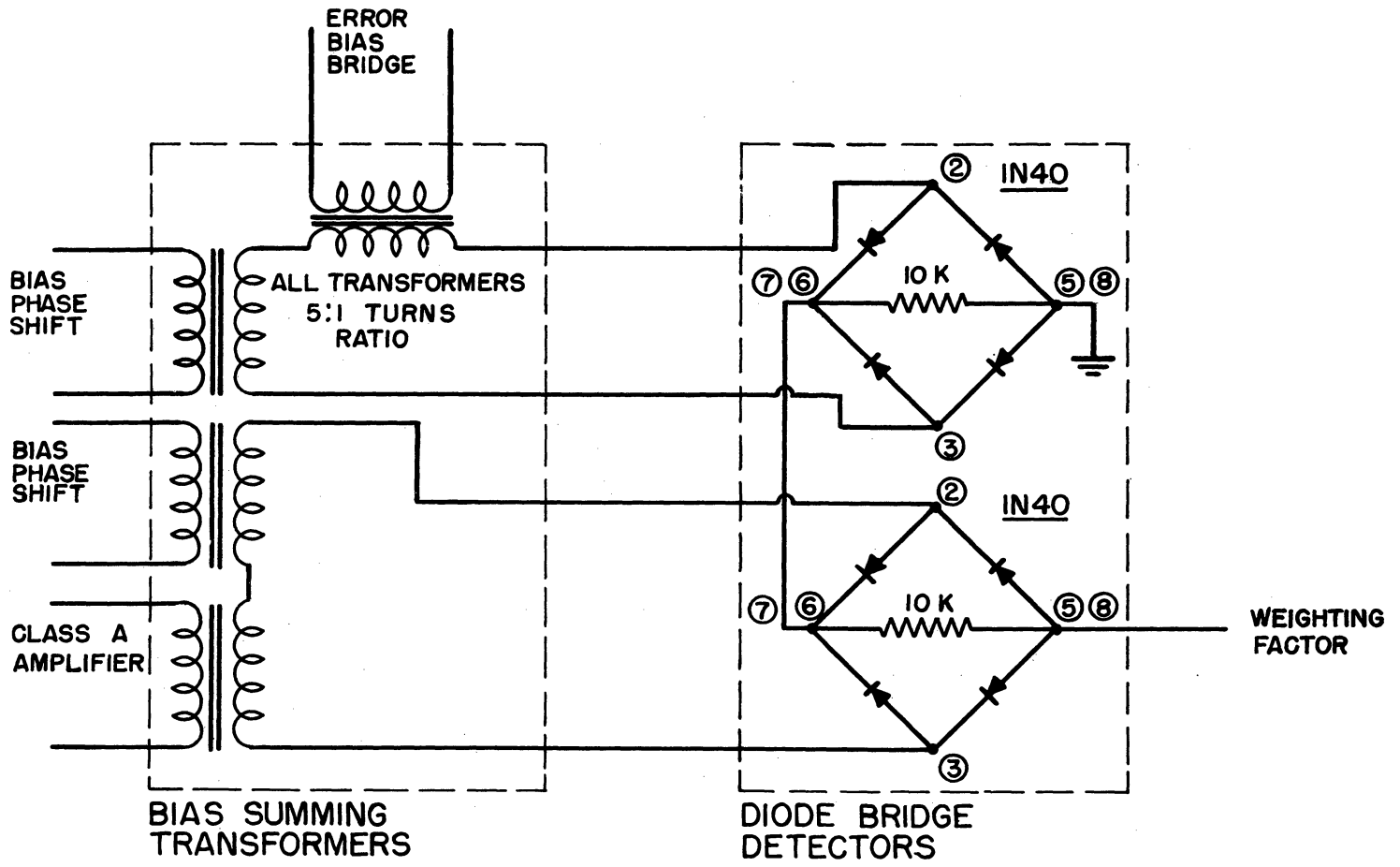
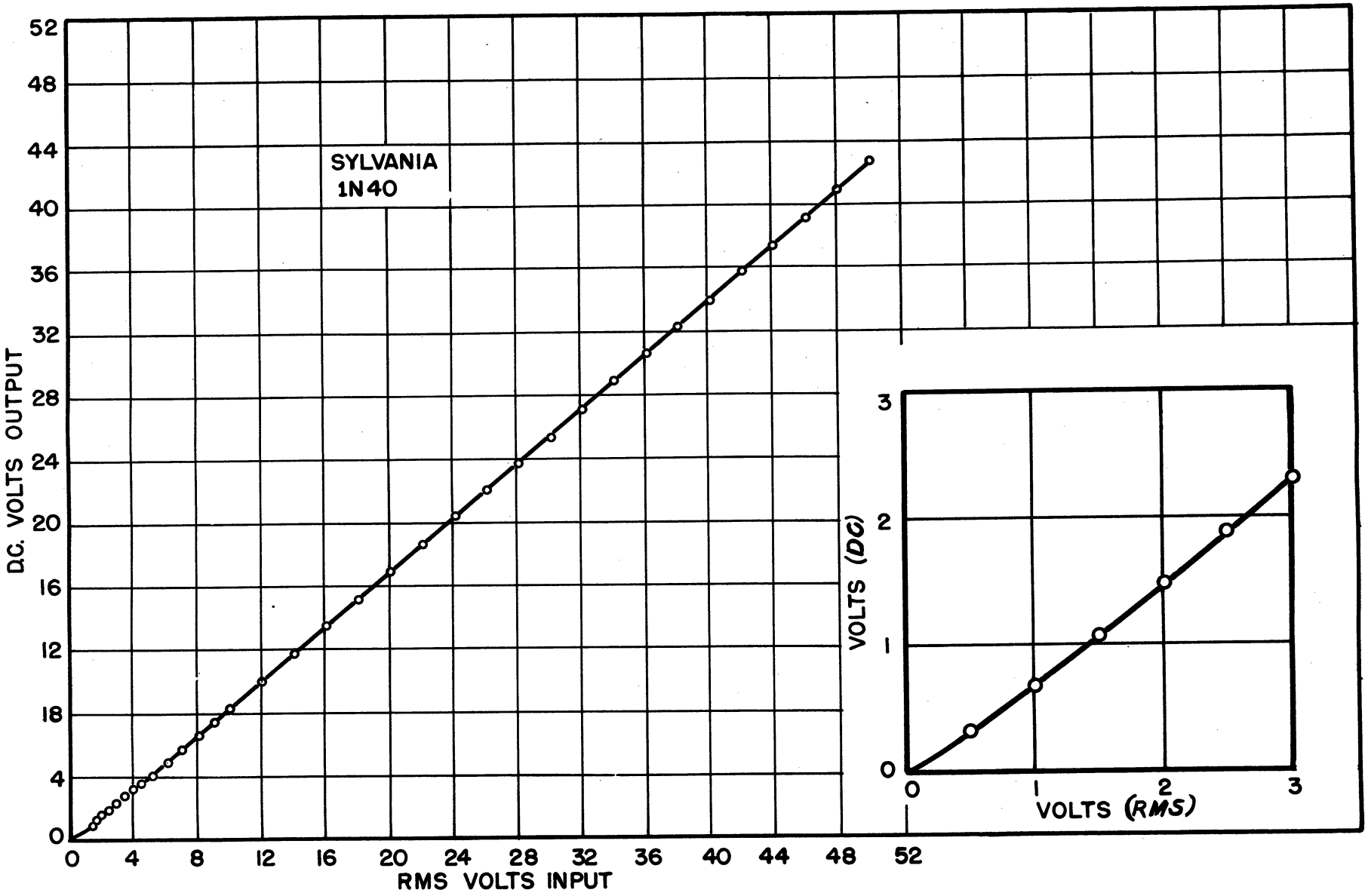
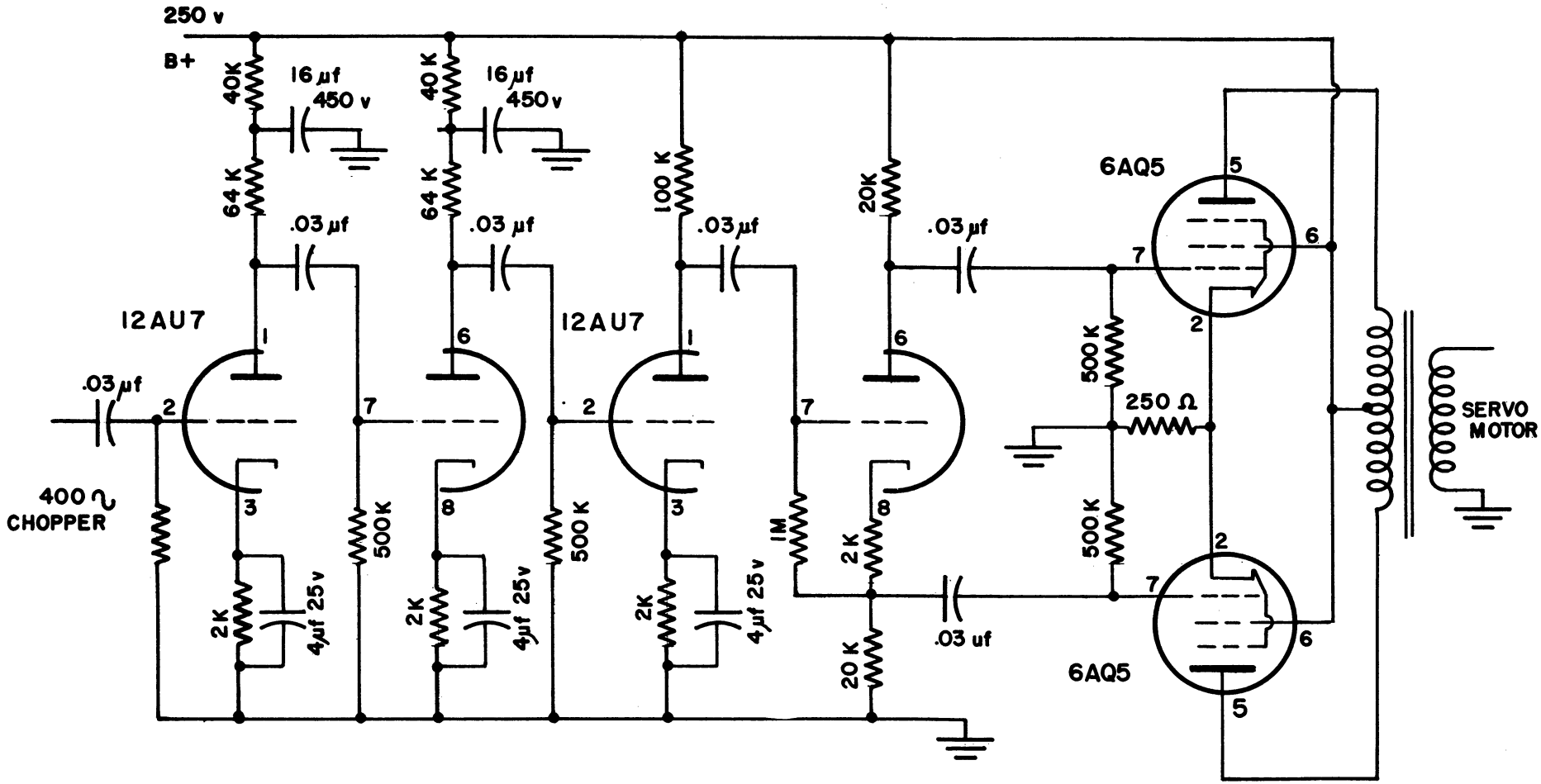

ERROR
BIAS
BRIDGE
BIAS
PHASE
SHIFT
ALL TRANSFORMERS
5:1 TURNS
RATIO
BIAS
PHASE
SHIFT
CLASS A
AMPLIFIER
IN40
10 K
IN40
10 K
WEIGHTING
FACTOR
BIAS SUMMING
TRANSFORMERS
DIODE BRIDGE
DETECTORS

FIGURE 9

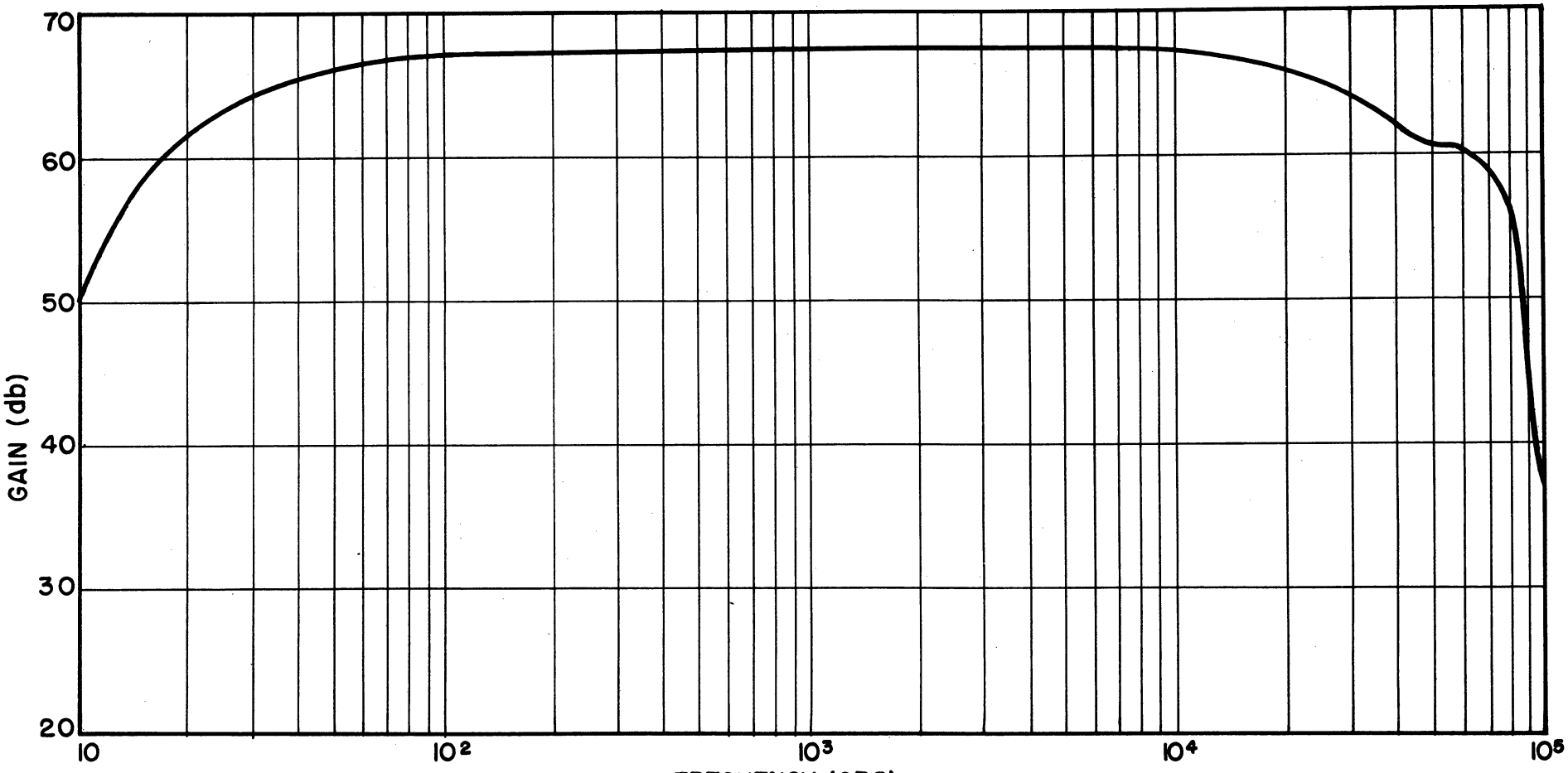


DIODE LINEARITY
FIGURE 10



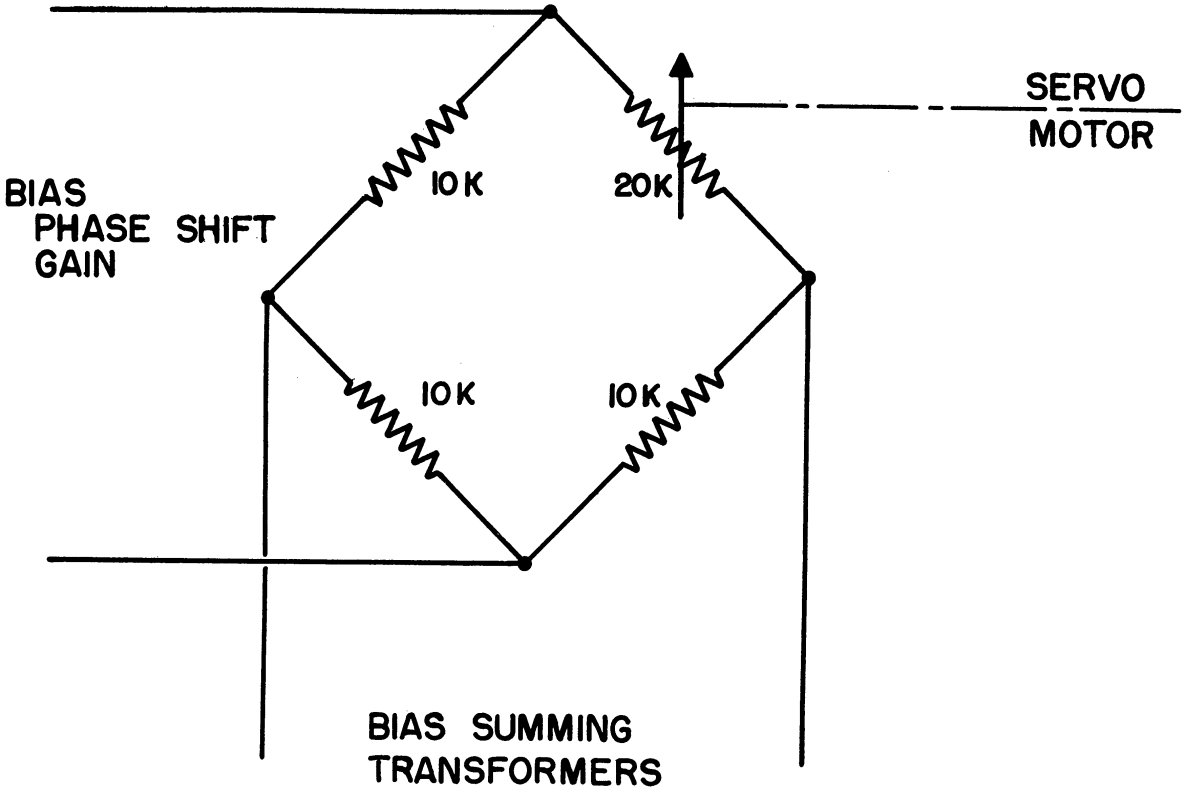
CLASS AB_1 AMPLIFIER

FIGURE //

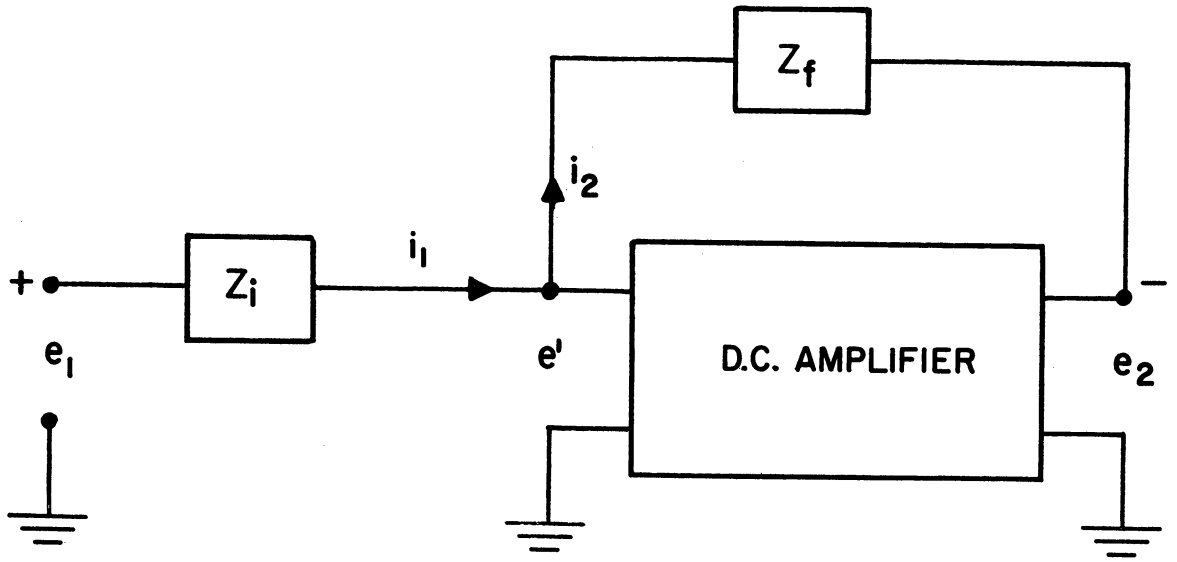


FREQUENCY RESPONSE OF CLASS AB, AMPLIFIER

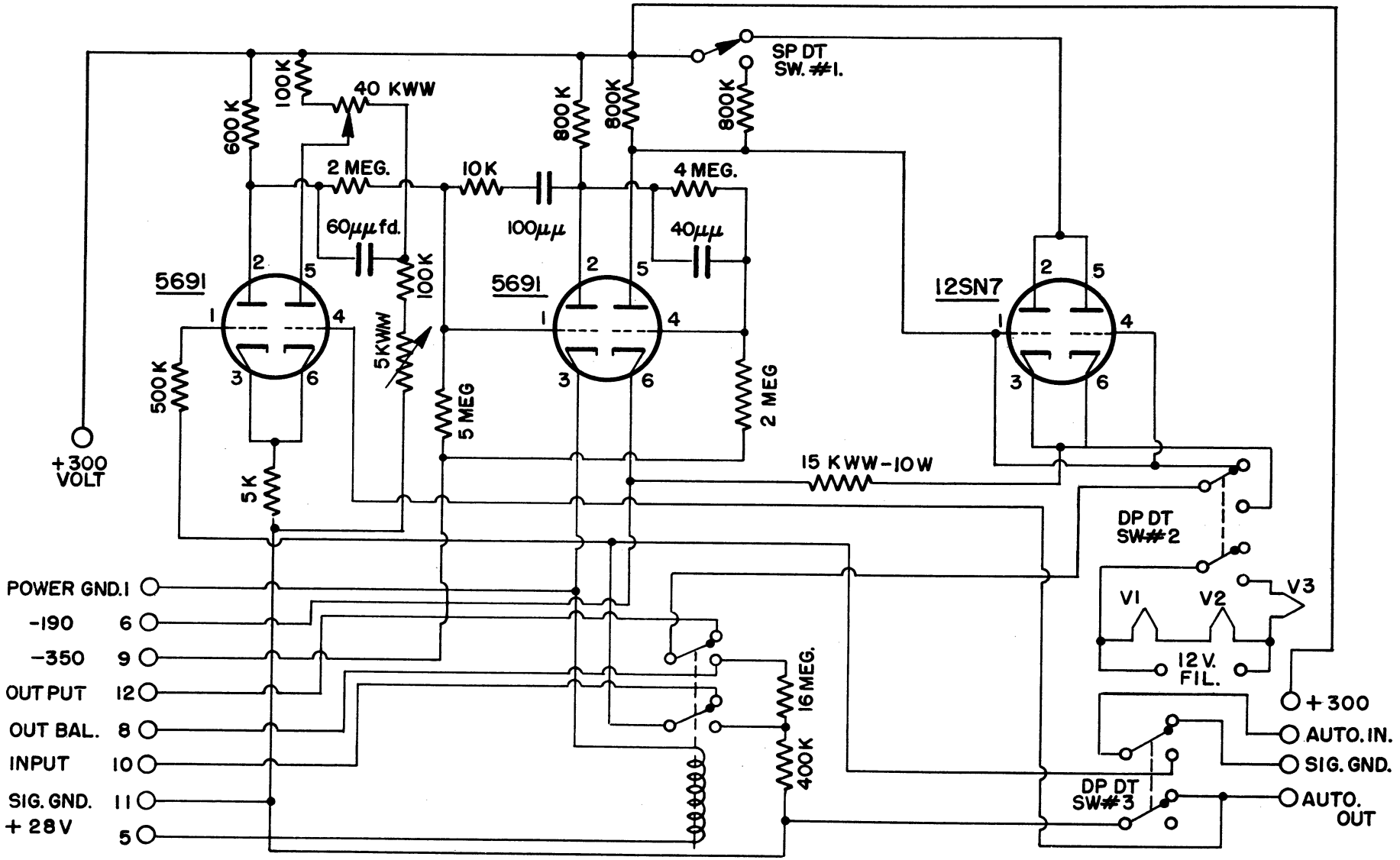
FIGURE 12



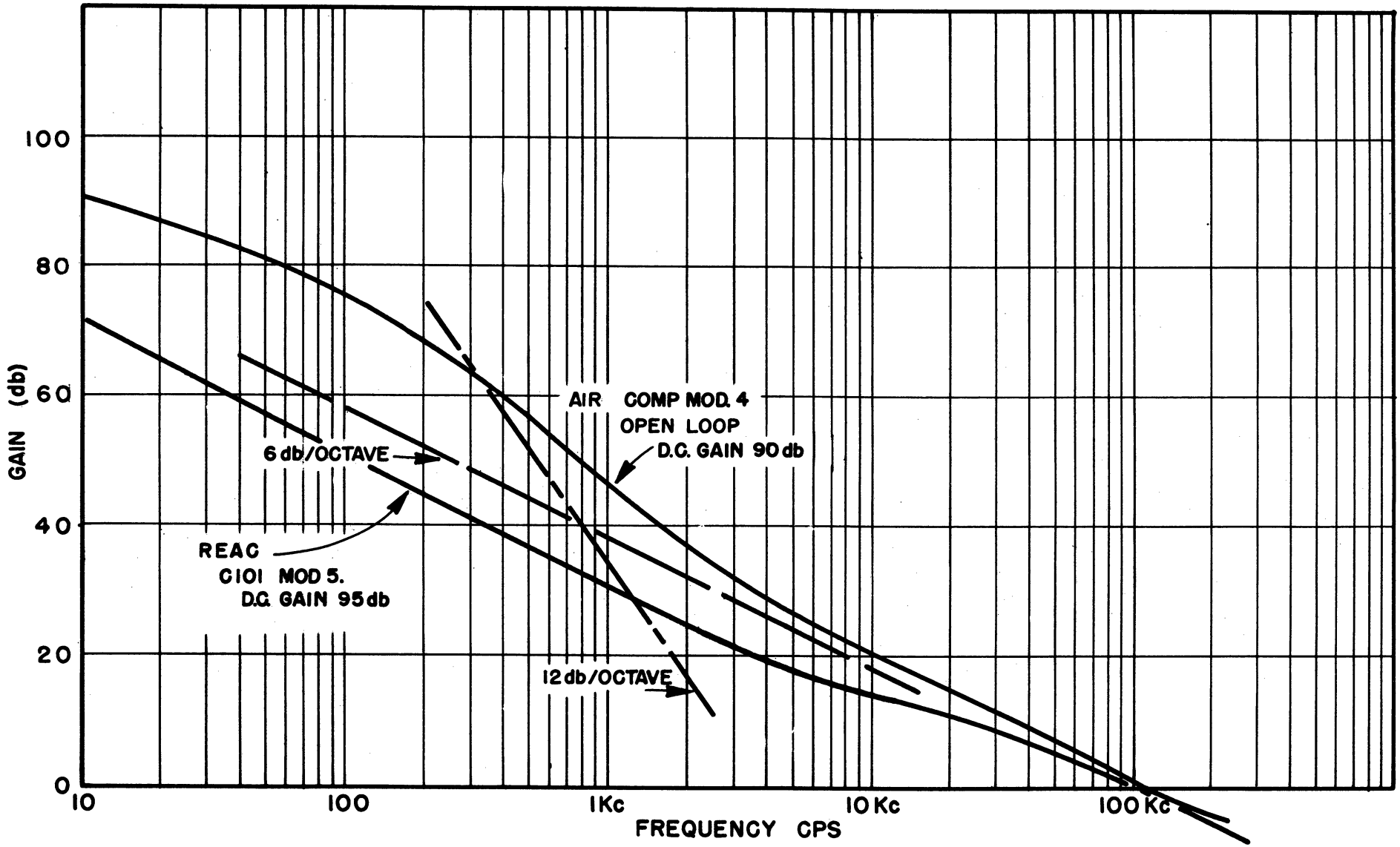
ERROR BIASING BRIDGE
FIGURE 13



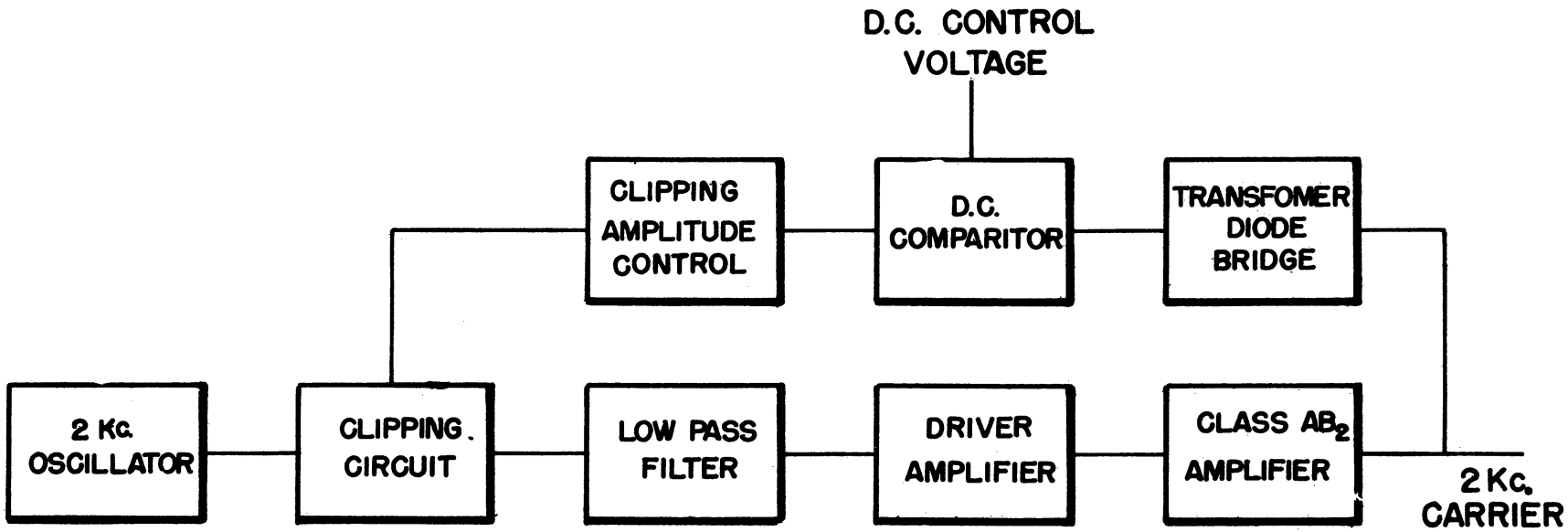
BLOCK DIAGRAM OF AN OPERATIONAL AMPLIFIER
FIGURE 14



D.C. OPERATIONAL AMPLIFIER
AIR COMPUTER MOD. 4
FIGURE 15

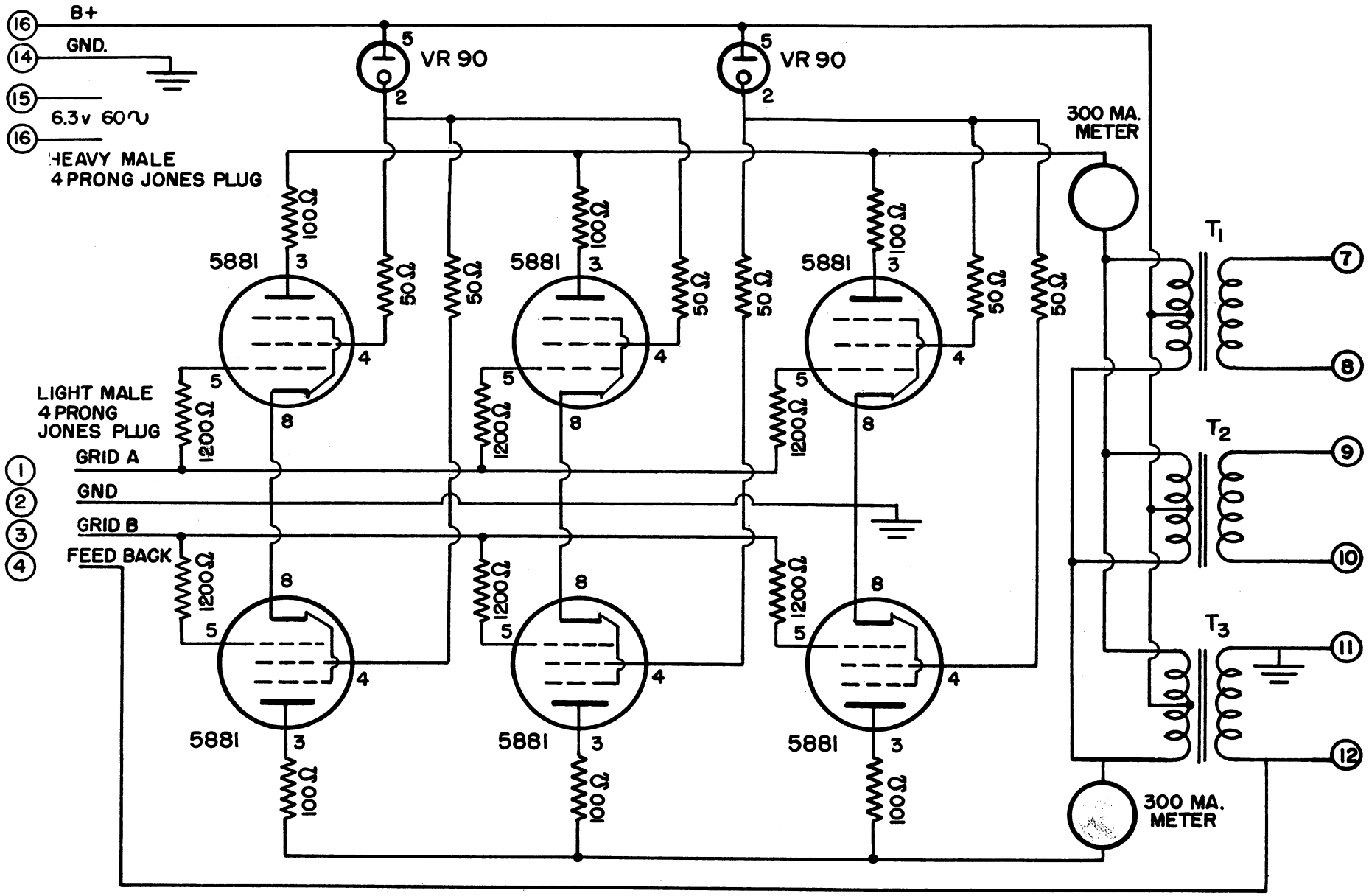


DC OPERATIONAL AMPLIFIER
AIR COMPUTER MOD. 4
FIGURE 16

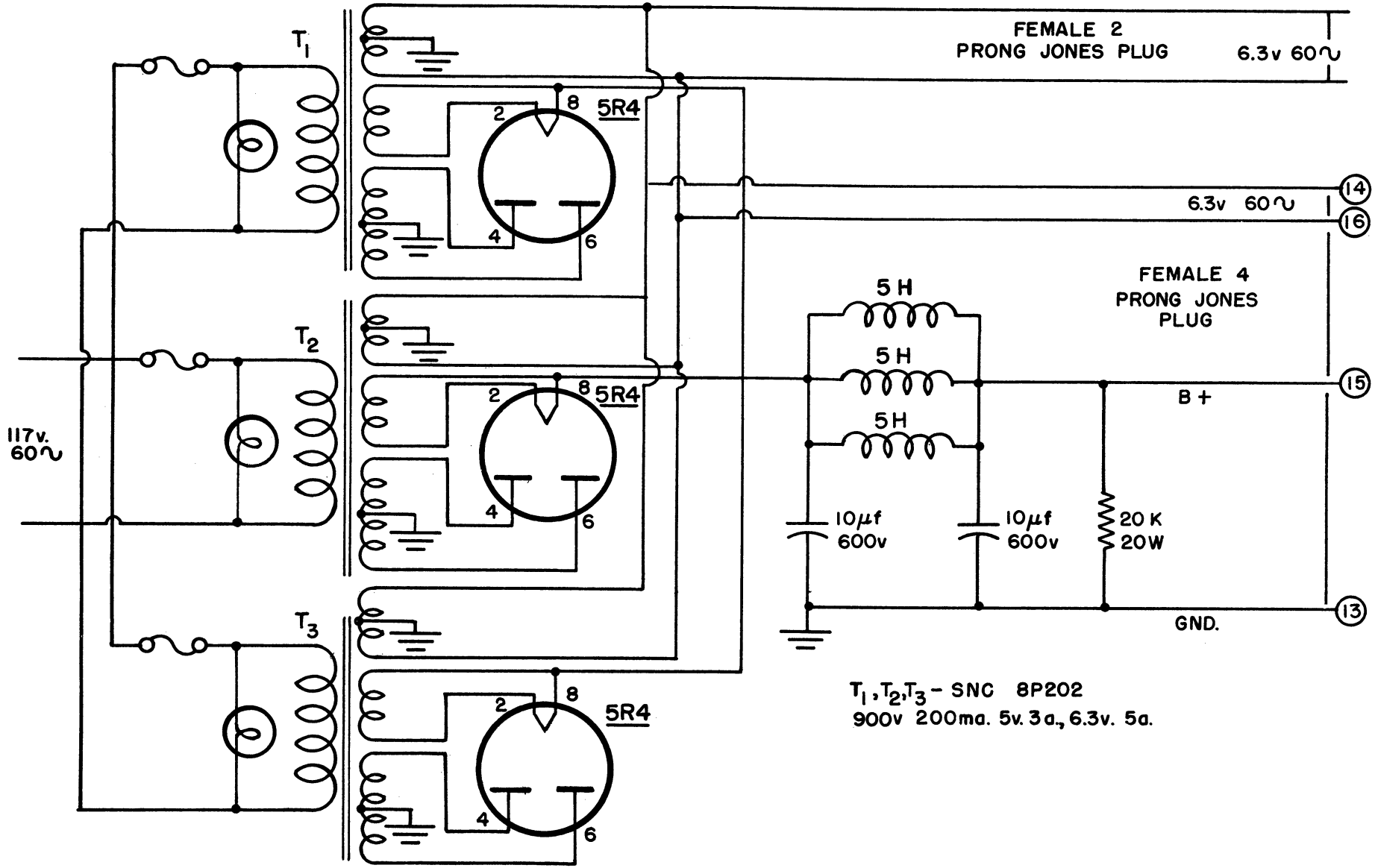


BLOCK DIAGRAM OF 2Kc. CARRIER AMPLITUDE CONTROL

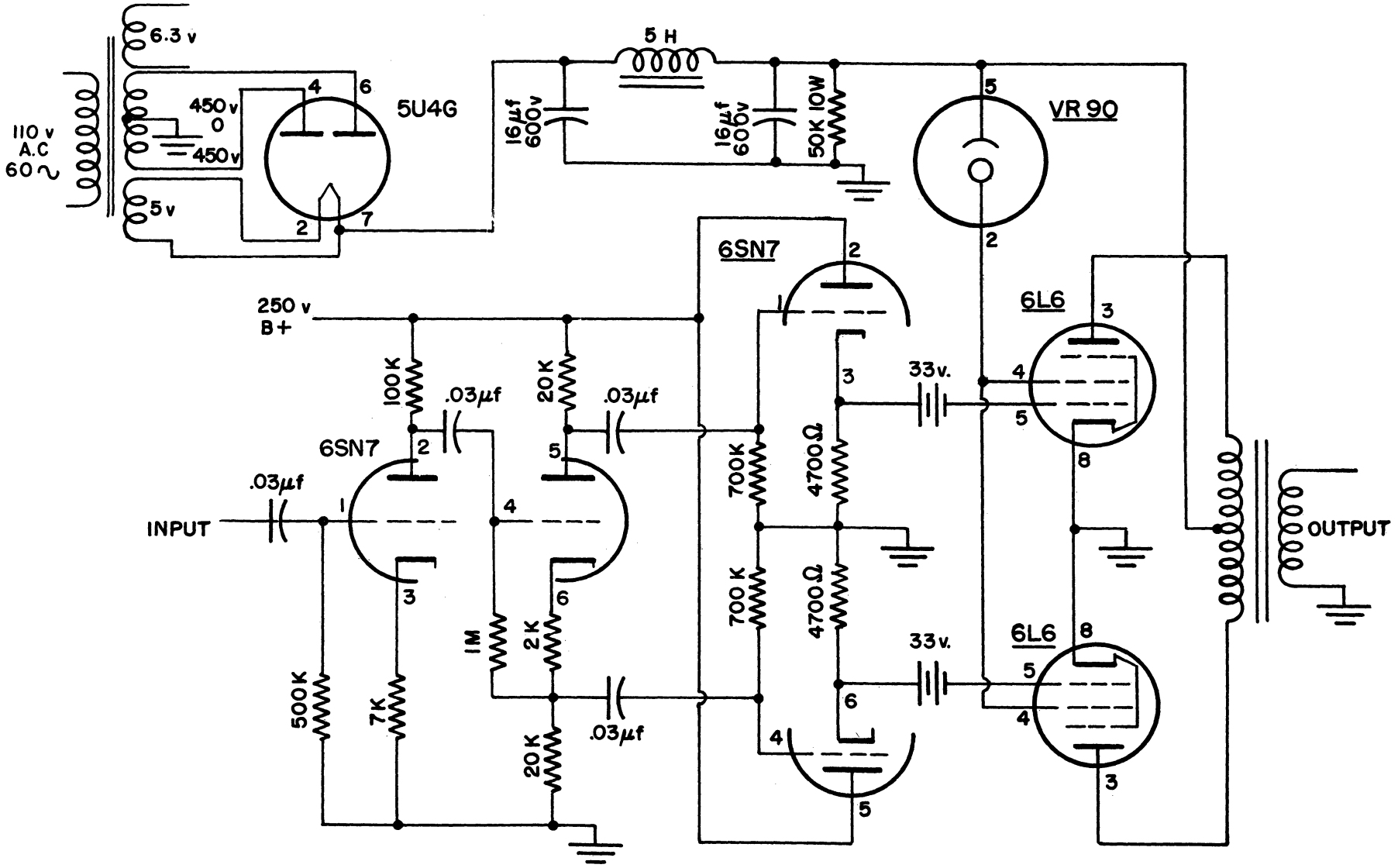
FIGURE 17



2Kc. POWER AMPLIFIER
FIGURE 18



B SUPPLY 2Kc. POWER AMPLIFIER
FIGURE 19



CLASS AB_2 AMPLIFIER & POWER SUPPLY
FIGURE 20