Study of ferroelectric-thin-film thickness effects on metal-ferroelectric-SiO_2–Si transistors

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This article examines the thickness effects of ferroelectric films on gate tunneling suppression and charge control in metal-ferroelectric-insulator-semiconductor field-effect transistors (MFISFETs). The formalism used is based on a blocking-layer model for the ferroelectric film and a self-consistent solution of the Poisson and Schrödinger equation. We show that with a polar ferroelectric the threshold voltage of the FET can be altered by controlling the ferroelectric film thickness. We also study the thickness dependence of the capacitance–voltage curve and the surface charge density and the effects of ferroelectric hysteresis. The tunneling probability and leakage current calculation in a MFISFET device are provided in this article. Ferroelectrics-based transistors show higher sheet charges and lower tunneling currents than oxide-based devices. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1470249]

I. INTRODUCTION

The electronic industry is in part driven by the shrinking gate length of metal oxide semiconductor field-effect-transistors (MOSFETs). However, it is now quite clear that once gate lengths approach ~ 0.05 μm the Si/SiO_2 structure will no longer be viable for transistors. The reason is the high gate leakage current that occurs once the oxide thickness approaches ~ 20 Å. To overcome this problem, in recent years there has been a growing interest in ferroelectric thin films. Ferroelectrics are materials which have a large dielectric constant (in the range of $\sim 100\epsilon_0$) and can also have a high polar charge if the films are below the Curie temperature for the material. Due to the high dielectric constant, it is possible to use it as a gate oxide material to avoid tunneling since, for the same gate capacitance, the ferroelectric film can be much thicker than a SiO_2 film. In devices the ferroelectric thin film is usually integrated with SiO_2 forming a gate dielectric stack metal-ferroelectric-insulator semiconductor field-effect-transistor (MFISFET) to prevent severe lattice mismatch between the ferroelectrics over silicon. In spite of some progress in the case of the integration of ferroelectric films in devices, there are a number of fundamental and technology challenges that need to be addressed.

The issues that need to be addressed in MFISFETs are: (i) what is the dielectric constant ϵ, coercive field E_c, and saturation field E_{sat} for a thin ferroelectric film; (ii) how can the polar charge available in the ferroelectric film be exploited to design devices with controllable threshold voltages? For example, can we alter the threshold voltage by simply controlling ferroelectric thickness under the gate? (iii) What does the capacitance–voltage ($C-V$) profile of the MFISFET look like and what information can be extracted from its analysis? On a more fundamental level, there are issues of ferroelectric domains in the films, the role of strain or coercive field, the presence of a ''dead'' layer or an intermediate layer with no ferroelectric effect in a thin film, etc. In this article we will address some of these issues. We start with a brief summary of the existing literature on ferroelectrics.

A large number of studies have been carried out to examine the synthesis and optimization of ferroelectric thin films. So far, most studies have been focused on the deposition of ferroelectric materials directly on the electrodes in memory devices [ferroelectric random access memories]. Various techniques such as metalorganic decomposition,[1] rf sputtering,[2] pulsed-laser deposition,[3] sol-gel processing,[4] metalorganic chemical-vapor deposition,[5] and molecular beam epitaxy (MBE)[6] have been applied. A large variation of the results in switching properties has been found for different electrodes, film thicknesses, and film composition. The empirical measurement of the saturation field varies considerably between different studies and most published values are for the coercive field rather than the saturation field. The significant distribution in results can be attributed to the electrode/interface properties, stoichiometry, and surface morphology. An issue that will be examined in his article is the effect of ferroelectric film thickness on the tunneling and charge control of the MFIS capacitor. It is important to understand how the film thickness affects the properties of the ferroelectric films.

The thickness effects of ferroelectric thin films can provide important information on interface-related properties. It has been found that a reduction in the film thickness results in a decrease in dielectric constants, remnant polarization, dielectric breakdown fields, and the tetragonal distortion c/a, and causes an increase of the coercive field, band-gap energies, and the diffuseness of the phase transitions.[7,8] Mechanisms such as domain transitions,[9] stresses,[10] defects,[11] and electrode/film interfacial blocking layers,[12–14] have been postulated for studies of thickness effects in ferroelectric thin films. Two models have emerged to explain the

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thickness effects. One is based on the domain structure transition from multi-domain predominance to single domain predominance at a critical grain size in the thin film. The other is the film/electrode interfacial blocking layer model. It is assumed that a thin amorphous low-dielectric layer is formed at the interface when the ferroelectric materials are deposited on the substrate, reducing the effective dielectric constant and remnant polarization and increasing the loss tangent and coercive field of the entire film. The first model postulates that the lack of the domain walls and the low domain wall mobility in the single domain predominated film in the small grains may result in thickness related size effects. It is expected that in high quality epitaxially grown ferroelectric films the blocking layer model will be valid. In this article, the blocking layer model is chosen to examine effects of ferroelectric film thickness in a MFISFET device by studying the switching properties, surface charge densities, and the tunneling probability.

In the next section we present our formalism which is used to examine gate tunneling, $C-V$ curves, and the effect of ferroelectric film thickness on the device. In Sec. III, we present our results. Finally we conclude in Sec. IV.

II. THEORETICAL FORMALISM

In the article we will examine a MFISFET structure in which we have a general ferroelectric having a large dielectric constant and a polar charge defined by the remnant and spontaneous polarization. There are a large number of ferroelectric materials being examined experimentally—some with no polarization at room temperatures, and some with large polarization values. We have chosen values for the dielectric constant and polarization which are possible for several ferroelectric materials. In addition to introducing the theoretical formalism that can address MFISFETs, our studies provide guidelines on what the potential of such devices would be.

The theoretical formalism applied by us has several ingredients. These are: (i) A self-consistent solution of the Schrödinger equation and Poisson equation. We have extended the model previously published by us to accomplish this,[15,16] (ii) A model for incorporating the polar charge in the ferroelectric region self-consistently with the field in the ferroelectric region; (iii) A model for how the polar charge and dielectric control of the ferroelectric region depend upon the thickness of the film; (iv) A charge tunneling model.

Results shown here are based on a self-consistent charge control model which is capable of introducing multiple epilayers with material properties that can vary continuously. This model first obtains the potential profile in a MOS structure by solving the Schrödinger equation and Poisson equation self-consistently. The solution of the Schrödinger equation yields the confined charge terms in the Poisson equation which, in turn, determine the potential profile. The potential profile is then fed back into the Poisson equation until the solution goes to convergence. The details of this charge model have been published elsewhere.[15,16]

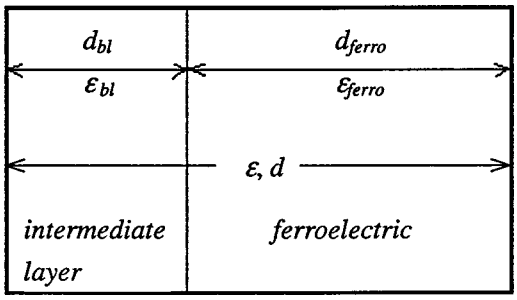

FIG. 1. The structure of the ferroelectrics blocking-layer model.

A. Ferroelectric blocking-layer model

It is known that when a thin layer of ferroelectric is grown on a substrate the entire film does not display a uniform ferroelectric behavior. Near the substrate there is a region of more or less fixed thickness (which varies somewhat with growth parameters) called the intermediate layer (or dead layer) where the material properties are not those of a ferroelectric material. We use the blocking model to describe the ferroelectric properties.

The blocking layer model of ferroelectric thin film is introduced by assuming the combination of a low-dielectric layer of thickness d_{bl} with a dielectric constant ϵ_{bl}, and a high-dielectric layer of thickness d_{ferro} with a dielectric constant $\epsilon_{\mathrm{ferro}}$, as shown in Fig. 1. The overall dielectric constant ϵ of these two layers is, consequently

$$\frac{d}{\epsilon}=\frac{d_{\mathrm{bl}}}{\epsilon_{\mathrm{bl}}}+\frac{d_{\mathrm{ferro}}}{\epsilon_{\mathrm{ferro}}}, \tag{1}$$

where d is the overall thickness of the ferroelectric film. The ferroelectric polarization is introduced as the boundary condition at the ferroelectrics/blocking layer interface

$$\epsilon_{\mathrm{ferro}}\mathbf{E}_{\mathrm{ferro}}+\mathbf{P}_{\mathrm{ferro}}=\epsilon_{\mathrm{bl}}\mathbf{E}_{\mathrm{bl}}, \tag{2}$$

where $\mathbf{E}_{\mathrm{ferro}}$ and $\mathbf{E}_{\mathrm{bl}}$ are the electric fields in the ferroelectric region and in the blocking layer. $\mathbf{P}_{\mathrm{ferro}}$ is the polarization field due to switching dipoles. According to Larsen *et al.*,[12] remnant polarization is a function of the applied field rather than the film thickness. Thus the coercive field E_c is independent of the film thickness, while the measured coercive voltage V_c can be related to the film thickness as

$$V_c=V_0+E_c d. \tag{3}$$

Here the presence of V_0 is due to the interface layer. The value of E_c can be determined from the measurement of V_c as a function of film thickness. Back to Eq. (2), the polarization properties of ferroelectric materials as a function of the applied electric field $\mathbf{E}$ can be described by the following approach. The magnitude of saturated polarization hysteresis loop is defined by

$$p_{\mathrm{sat}}^{+}(\mathbf{E})=P_s\tanh[(\mathbf{E}-E_c)/2\delta], \tag{4}$$

where

$$\delta=E_c\left[\ln\left(\frac{1+P_r/P_s}{1-P_r/P_s}\right)\right]^{-1}. \tag{5}$$

The positive superscript in Eq. (4) refers to the forward biasing of the loop. P_r and P_s are the remnant and spontaneous polarization, respectively. The magnitude of saturated polarization in the reverse loop, P_{sat} is defined as

$$P_{\text{sat}}(\mathbf{E}) = -P^{+}_{\text{sat}}(-\mathbf{E}). \tag{6}$$

B. Charge tunneling model

The one-dimensional electron tunneling from the semiconductor to the gate surface can be considered as tunneling through a smoothly varying potential. The analytical expression for the total tunneling probability T is given by

$$T = \exp\left[-\frac{1}{\hbar}\int_{x_1}^{x_2}[8m^*(V(x)-E)]^{1/2}dx\right], \tag{7}$$

where E is the energy of the particle, m^* is the effective mass of the barrier, $V(x)$ is the potential barrier along x direction, and x_1 and x_2 are points where $E=V(x)$. In some cases, electrons can be induced at the ferroelectrics/oxide interface and leads to charge tunneling as well. This effect will be added to the total tunneling probability. The tunneling current density for substrate injection is calculated based on the independent electron approximation and elastic tunneling assumption. If the transverse component of the electron energy (E_t) is assumed conserved during tunneling through the dielectric stack and a parabolic dispersion relation is used for the transverse component, the tunneling current (J) is described by the Wentzel–Kramers–Brillouin (WKB) approximation of tunneling current using Eq. (7) for $T(E)$

$$J = \frac{4\pi q m_t}{h^3}\int_0^{E_{FS}} T(E)(E_{\text{FS}}-E)dE, \tag{8}$$

where E_{FS} is the fermi level in the semiconductor substrate and m_t is the transverse electron effective mass.

III. RESULTS AND DISCUSSION

As noted in the introduction, there are several types of ferroelectric materials. Materials like $LiNbO_3$ have dielectric constants in the range of $\sim 40\ \epsilon_0$ and the polar charge is not affected by the external field. Materials like BST, depending upon composition, have high dielectric constants ($\sim 100\ \epsilon_0$) and may or may not have polar charges depending upon the Curie temperature. Below the Curie temperature the polar charge is determined by the external field as described by Eqs. (4) and (5). In this article we will examine the general case where the material polarization is controlled by the external field. The formation can be generalized to field-independent polar charge case and no polar charge cases in a simple manner.

The structure simulated consists of a blocking-layer BST film on a standard SiO_2/Si structure. The intermediate 12 Å SiO_2 layer is included since in real structures such a layer may be needed to improve the lattice mismatch between the ferroelectric film and silicon, and the inversion layer is at the high quality SiO_2/Si interface. For the simulations we assume that the silicon is doped p type at 1×10^{17} cm^{-3}. The Schottky barrier height of BST is taken to be 1.7 V after Ref. 3. Other related material parameters follow our previous publication.[15]

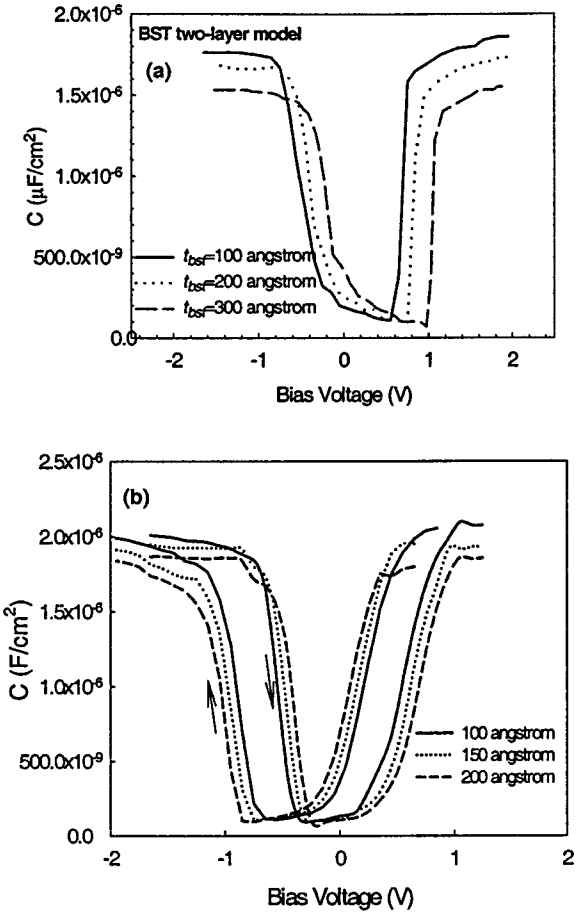

FIG. 2. (a) The capacitance–voltage curve of a BST-oxide MFISFET for various BST thicknesses under forward biasing; (b) The $C-V$ curves for various BST thicknesses under reverse and forward biasing.

The polarization properties of BST thin film under 20 nm have not been reported in literature. Therefore, several assumptions have been made in the simulation. The stoichiometry of barium strontium titanate is chosen to be $Ba_{0.68}Sr_{0.32}TiO_3$ for a reasonably large polarization and a high dielectric constant. The overall thickness of BST film is varied and includes an 8-Å-thick blocking layer with a dielectric constant $\epsilon_{\text{bl}}=30$. The dielectric constant of the ferroelectric part of the film is 300. These data are obtained by fitting the empirical results[17] using Eq. (2). The distribution of saturation charge is taken as 10^{14} charges/cm^2 at the pure-ferroelectric/blocking layer interface, which refers to a saturation polarization of 16 μC/cm^2.[18] The remnant to spontaneous polarization ratio is assumed 0.8, and the coercive field is 40 kV/cm.[18]

We have shown counterclockwise curves in the capacitance–voltage ($C-V$) relation under forward and reverse biasing due to the nature of hysteresis polarization of ferroelectrics without applying the blocking-layer model.[15] Figure 2(a) illustrates the $C-V$ curves of MFISFET devices with various ferroelectric film thicknesses under the forward bias. The blocking-layer thickness is kept at 8 Å for all cases.

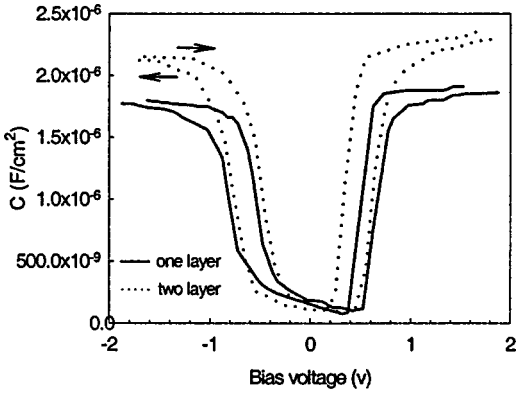

FIG. 3. Comparison of the capacitance–voltage curves for MFISFET modeled with the blocking layer and without blocking layer for the same overall BST thickness = 100 Å.

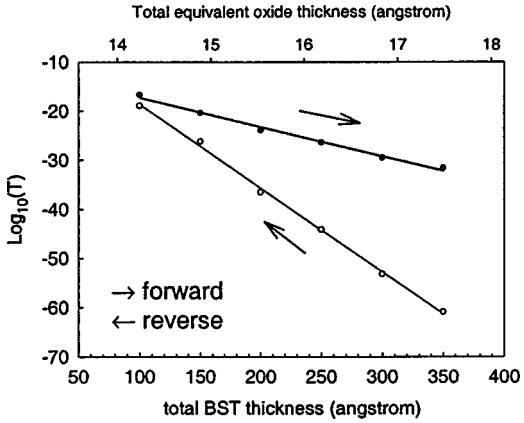

FIG. 4. The tunneling probability of forward- and reverse-bias modes in a BST MFISFET device based on the blocking-layer model at a fixed sheet charge = 10^{13} cm^{-2}.

As the BST film thickness increases, the threshold voltage increases as shown. This is caused by the decreased electric field and reduced polarization charges, according to Eq. (4). The maximum capacitance is lowered as well due to the smaller overall effective thickness. The results show that a 100 Å change in the ferroelectric thickness alters the threshold voltage by ~0.4 V.

The biasing direction combined thickness effects are shown in Fig. 2(b). It is interesting to point out that increasing the film thickness also enhances the ferroelectric behavior since the $C-V$ separation due to the hysteresis is more significant. We have seen that the polar charge density decreases as thickness under forward bias in Fig. 2(a). Under reverse bias and high positive fields, the polar charge density reaches a saturation value which is not thickness dependent. The induced surface charge density becomes proportional to the film thickness, and will be discussed later in Fig. 6.

In order to see how important the presence of the blocking layer is we compare the $C-V$ results for the blocking layer model and a model where there is no blocking layer. The results are shown in Fig. 3. The blocking-layer modeled MFISFET has the same total BST thickness ($d_{\text{ferro}}+d_{\text{bl}}$) as the other one. Both curves show clear counterclockwise hysteresis. The overall effective thickness for the blocking-layer model is increased by the blocking layer and, consequently, the maximum capacitance is lower. The threshold voltage is also raised due to the positioning of the polarization charge and the Si/SiO_2 interface.

Although the capacitance–voltage curves do not provide direct measurement of the ferroelectric properties, this simple measurement reveals important information. First, the shift of threshold voltage indicates changes in the thickness (as shown in Fig. 2) and the strength of polarization. The latter can be explained by the fact that the induced charge density is related to the polarization. Next, the equivalent oxide thickness of the ferroelectric film can be used to estimate the dielectric constants of the ferroelectrics and the blocking layer, when various film thicknesses are available.

Figure 4 demonstrates the tunneling probability as a function of BST film thickness of the blocking-layer model. The thickness of the blocking layer is assumed constant for various film thicknesses and the results are for conditions where the sheet charge density is 10^{13} cm^{-2}. The forward bias loop exhibits higher probability because it requires higher electric fields to achieve the equivalent charge, resulting in higher tunneling probability. The tunneling probability can be greatly suppressed if the BST thickness increases from 100 to 200 Å while the equivalent oxide thickness increases only 1.3 Å. The WKB approximation of gate leakage current from the substrate injection is shown in Fig. 5(a).

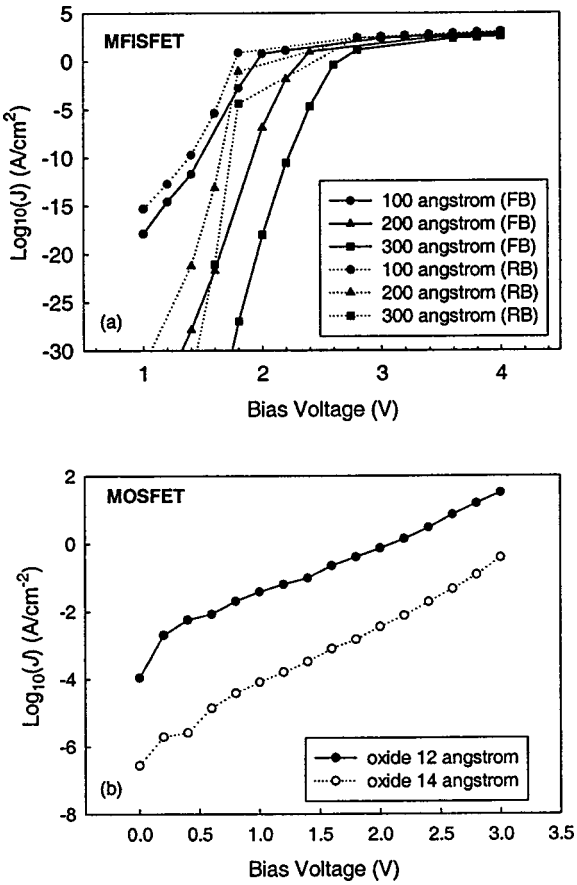

FIG. 5. (a) Gate tunneling current from substrate injection vs the bias voltage of a MFISFET structure. "FB" represents forward biasing, and "RB" refers to reverse biasing. (b) Simulated tunneling currents in the oxide-based MOSFET for comparison.

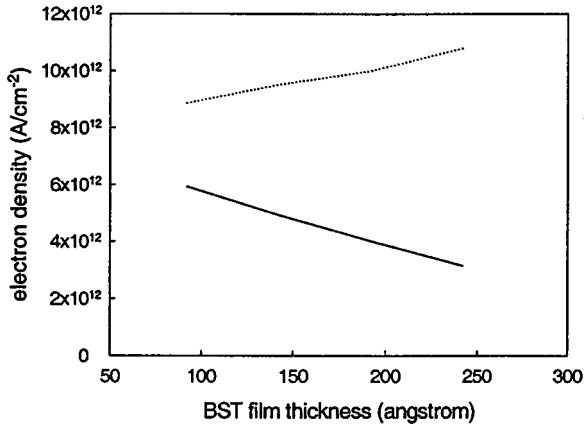

FIG. 6. The sheet charge density as a function of BST thickness at the bias voltage=1 V under different biasing directions. The solid line represents forward bias, and the dotted line represents reverse bias.

Although the tunneling probability under the reverse bias is less than under the forward bias with the same amount of two-dimensional electron gas (2DEG) charge, the leakage current is larger at the same voltage, which is the result of the counterclockwise hysteresis. The tunneling current finally becomes very large past 1.5 V. It is because the inversion charge is turned on very fast and close to a saturation value in ferroelectrics. Second, the energy gap barrier is much smaller than silicon dioxide. However, considering the voltage operating range for future devices, this should not be a serious problem. The tunneling current of an oxide-based structure is shown in Fig. 5(b) for comparison. Results show that the ferroelectrics with the same equivalent oxide thickness are 10^{-10} lower than the conventional structure.

Figure 6 shows the surface 2DEG as a function of ferroelectric film thickness and biasing loop applying 1 V on the gate. The reverse and forward biasing loops show reverse trends in the surface charge density as the thickness varies, which again explains Fig. 2(b). Under the forward biasing loop, the polar charge density is not thickness dependent and reduces for thicker films, which in turn generates less 2DEG. While under the reverse bias, the polar charge is almost constant for all thicknesses. It is interesting to compare these results with what has been reported in the AlGaN/GaN system.[19] There is a layer fixed polar charge due to spontaneous polarization and piezoelectric effect at the AlGaN/GaN heterointerface. It is found that as the AlGaN thickness is increased the 2DEG density starts to increase and then saturates. Situations for the ferroelectric film on the silicon semiconductor have similar behaviors under reverse biasing. However, it should be noted that the degree of saturation polarization is strongly related to the assumption of P_r/P_s ratio. Measurements providing information given in Fig. 5 would thus be extremely useful in establishing detailed thickness dependence of the polar properties. For comparison, the surface charge density in a conventional oxide transistor is around $\sim 10^{12}$ cm^{-2} for the same equivalent oxide thickness range ($\sim$14 Å). Ferroelectrics-based transistors are able to get higher sheet charge density.

As already noted in this article, we have assumed that the nonferroelectric blocking layer has the same stoichiometry and similar properties as the ferroelectrics except the polarized charges and the dielectric constant. This is supported by transmission electron microscopy investigation that continuous crystalline structure is observed from the blocking layer to the ferroelectrics.[12] Moreover, the high dielectric constant of the ferroelectrics comes from the polarization charge, not the energy band gap. Therefore, we assume the electron mass and the energy band gap to be the same as the ferroelectrics. We have also made assumptions of the blocking layer thickness. It is expected that the nonferroelectric layer of a high quality epitaxially grown ferroelectric film will be very thin in our simulation. However, there is not much impact on our simulation results even for a 20 Å blocking layer. This will cause an increase of about 1.4 Å in the effective oxide thickness for the worst 100 Å case and a shift in the threshold voltage of less than 0.05 V.

IV. CONCLUSION

In this article we have examined charge control issues in a MFISFET structure using the blocking-layer model. While there are other experimental studies which validate this model, it is not known if this model is applicable to vary small thickness films. Our studies show that $C-V$ and other measurements in a MFISFET would be quite sensitive to model details and would thus provide details on polar charge, coercive field, etc., in thin film ferroelectrics. Our study also shows that ferroelectric film thickness can be used to alter threshold voltage of the devices and, most importantly, greatly suppress gate to channel tunneling.

At present there are few experimental studies on the MFISFET. Given the potential of such structures in next generation silicon based technology such studies would be very important. The model presented here should be capable of interpreting these results and extracting parameters critical for the future device design.

ACKNOWLEDGMENTS

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