Reduction of dislocation density in mismatched SiGe/Si using a low-temperature Si buffer layer

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(Received 26 February 1997; accepted for publication 14 April 1997)

The reduction of the dislocation density in relaxed SiGe/Si heterostructures using a low-temperature Si(LT-Si) buffer has been investigated. We have shown that a 0.1 μm LT-Si buffer reduces the threading dislocation density in mismatched $Si_{0.85}Ge_{0.15}$/Si epitaxial layers as low as $\sim 10^4$ cm^{-2}. Samples were grown by both gas-source molecular beam epitaxy and ultrahigh vacuum chemical vapor deposition. © *1997 American Institute of Physics.*
[S0003-6951(97)03424-4]

SiGe/Si heterostructures have gained considerable attention for both electronic and optoelectronic applications due to their compatibility with existing Si technology.[1–5] In particular, there are device applications where a strained Si channel layer of a field-effect transistor needs to be grown on relaxed SiGe to produce a type II heterostructure band lineup. Producing relaxed, nearly defect-free SiGe alloys has been difficult due to the 4% mismatch between Si and Ge. Above the critical thickness, threading dislocations form in the SiGe epilayer, resulting in material degradation and poor device performance.[6] Both superlattices and step-graded layers have been used as techniques to reduce the strain energy while minimizing threading dislocations.[7–13] While some reduction was obtained,[7–9] the dislocation densities are still too high ($\sim 10^9$ cm^{-2}) for any practical device application.

Recent reports indicate that the use of amorphous, polycrystalline, and low-temperature buffer layers can significantly reduce dislocation densities in nitride, InAlAs/InP, and SiGe technologies.[14–16] We have investigated the use of a low-temperature Si (LT-Si) buffer layer for reducing the threading dislocation density in relaxed SiGe heterostructures. We report the characterization of these heterostructures grown by both gas-source molecular beam epitaxy (GSMBE) and ultrahigh vacuum chemical vapor deposition (UHV-CVD), and of heterojunction bipolar transistors (HBTs) using LT-Si buffers.

A number of relaxed SiGe samples with and without the LT-Si buffer layer were grown by GSMBE. Pure Si_2H_6 and solid Ge were used as source materials. The samples were grown on (100) p^+ Si substrates. Each sample consists of a 0.1 μm Si layer grown at 700 °C followed by a 0.1 μm LT-Si buffer layer grown at 450 °C. A 0.5 μm $Si_{0.85}Ge_{0.15}$ layer was then grown at 570 °C. Growth of the entire structure was monitored by *in situ* reflection high-energy electron diffraction measurements. The image displayed a streaked (2×1) pattern during growth of Si at 700 °C, which turned spotty during growth of the LT-Si buffer layer. The streaked pattern was restored after a few monolayers of growth of SiGe at 570 °C. The control sample consists of a 0.1 μm Si layer also grown at 700 °C followed by a 0.5 μm $Si_{0.85}Ge_{0.15}$ layer grown at 570 °C. Each SiGe sample thickness exceeds the thermodynamically stable critical thickness of 0.4 μm.[17] The threading dislocation densities were examined by transmission electron microscopy (TEM) using a JEOL 2000-FX microscope with an accelerating voltage of 200 kV. Both cross-section TEM and plan-view imaging were performed.

Bright-field cross-section (200) imaging of heterostructures without and with the LT-Si buffer layer are shown in Figs. 1(a) and 1(b), respectively. In the samples without the LT-Si buffer layer, the threading dislocations propagate throughout the alloy layer, as expected. An examination by bright field plan-view (022) imaging indicates a threading dislocation density of $7.56\times10^9\pm2.08$ cm^{-2} in the sample

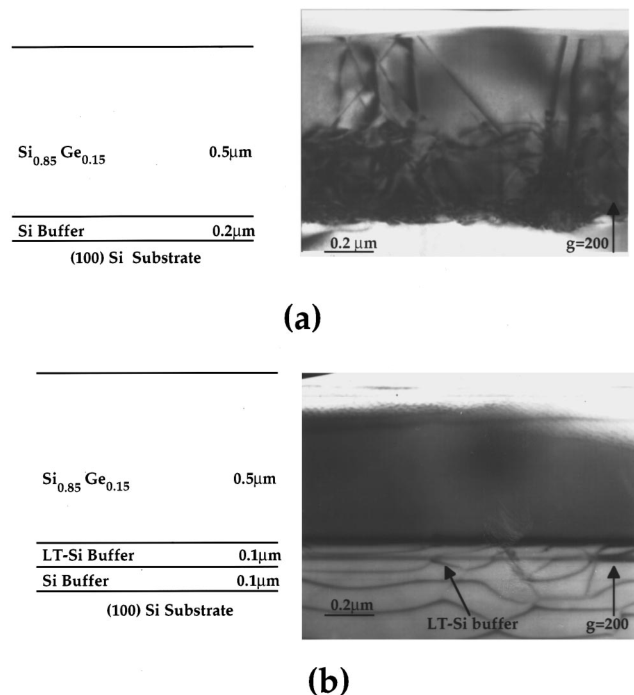

FIG. 1. Bright field (200) cross-section TEM images of 0.5 μm thick $Si_{0.85}Ge_{0.15}$ grown at 570 °C on (100) Si substrates (a) without any low-temperature Si(LT-Si) buffer and (b) with a 0.1 μm LT-Si buffer layer grown at 450 °C. Both samples have a 0.1 μm Si buffer layer grown first on the substrate at 700 °C.

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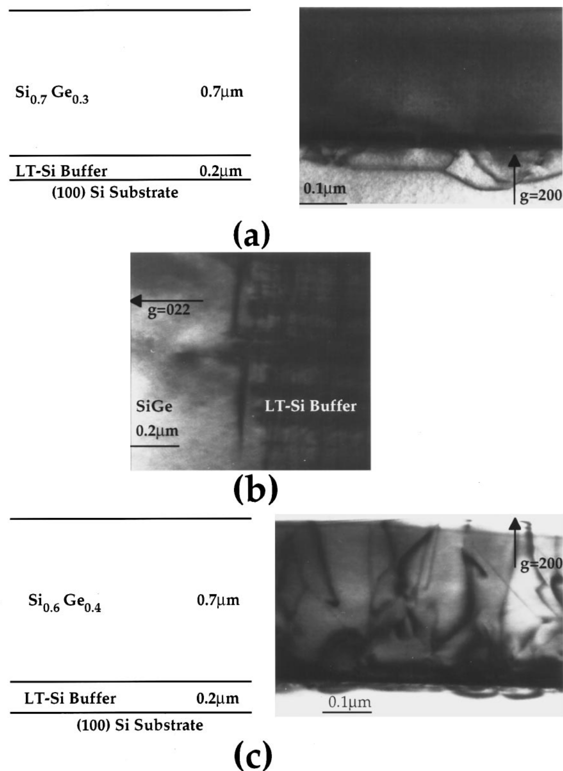
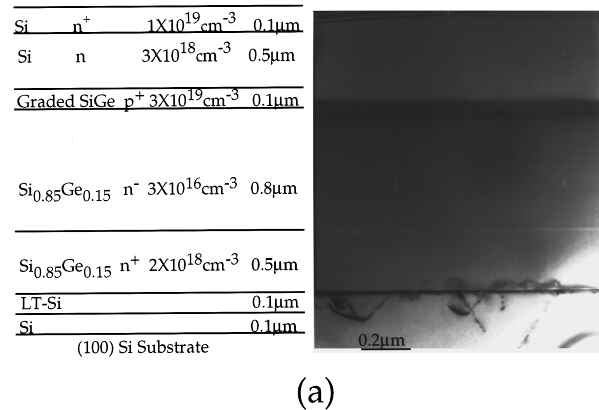


FIG. 2. TEM images of SiGe samples grown on (100) Si substrates by UHV-CVD. The samples contain a 0.2 μm LT-Si buffer layer grown at 425 °C on the substrate followed by 0.7 μm of SiGe grown at 525 °C. (a) and (b) show the bright field (200) cross-section and (022) plan-view TEM of a $Si_{0.7}Ge_{0.3}$ layer, respectively. (c) shows the cross section of a $Si_{0.6}Ge_{0.4}$ layer.

without the LT-Si buffer layer. It is evident in the sample with the LT-Si buffer layer, Fig. 1(b), most or all of the threading dislocations are prevented from propagating into the SiGe layer. These results, along with an examination by plan-view imaging of the same structure, indicate that the threading dislocation density is $\leqslant 10^4$ cm^{-2} in the SiGe epilayer. Room-temperature Hall measurements were performed on 1 μm thick boron doped $(3.4\pm 1.8\times 10^{17}$ cm$^{-3})$ $Si_{0.7}Ge_{0.3}$ samples. The hole mobility increased from 160 ± 18 cm^2 V^{-1} s^{-1} to 200 ± 2.5 cm^2 V^{-1} s^{-1} by including the LT-Si buffer layer.

Motivated by these results, we then examined the effectiveness of the LT-Si buffer layer for several relaxed $Si_{1-x}Ge_x$ samples with varying x grown on (100) p^+ Si substrates by UHV-CVD. Ultralarge scale integration grade silane (100%) and germane (10% in helium) were used as material gas sources. The samples consist of an initial 0.2 μm LT-Si buffer layer grown at 425 °C followed by 0.7 μm $Si_{0.7}Ge_{0.3}$ and $Si_{0.6}Ge_{0.4}$, respectively, grown at 525 °C. Bright field (200) cross-section and (022) plan-view imaging of the $Si_{0.7}Ge_{0.3}$ sample, shown in Figs. 2(a) and 2(b), indicate a near defect-free SiGe region. The bright field (022) plan-view image of the same sample, shown in Fig. 2(b), indicates that the dislocations are contained within the LT-Si buffer layer. For higher (40%) Ge containing samples, as shown in Fig. 2(c), optimization of the LT-Si buffer layer thickness for minimizing the threading dislocation density is under investigation.



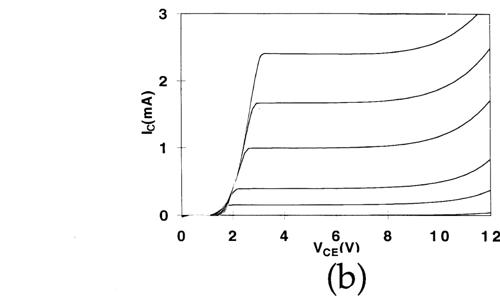


FIG. 3. (a) Cross-section TEM image and (b) dc common-emitter current–voltage characteristics of a $n-p-n$ SiGe/Si bipolar transistor grown with the LT-Si buffer grown at MBE.

Double crystal x-ray measurements of the $Si_{0.85}Ge_{0.15}$ layer without and with LT-Si buffer layers show that the width (full width at half-maximum) of the rocking curve corresponding to the alloy peak is reduced from 450 arc s to 371 arc s, respectively.

The mechanism for threading dislocation reduction is still under investigation. We suspect that because of the low growth temperature, a large number of point defects are generated in the LT-Si buffer layer. As the misfit dislocations propagate through the LT-Si layer, they become trapped by the defects and are annihilated.

From Fig. 1(b), one should note the existance of threading dislocations in the substrate region just below the LT-Si buffer layer. We believe that the threading dislocations found deep inside the substrate are generated from the activation of Frank–Read sources, which can relieve the strain in the SiGe epilayer.[18] The bowing mechanism is also observed in samples using graded layers and superlattices to relieve strain.[10,19]

We have grown and fabricated preliminary SiGe/Si $n-p-n$ HBTs with LT-Si buffer layers. The complete heterostructure is shown in Fig. 3(a). It can be seen that the active region of the structure is defect-free although the area of 10×10 μm^2 is shown in Fig. 3(b). The dc current gain is ~ 6 and the breakdown voltage is more than 10 V. The V_{ce} offset voltage is ~ 1.5 V and the Early voltage is approximately 1000 V.

Recent reports have shown that higher electron mobilities are measured in strained Si grown on relaxed SiGe than in bulk Si due to band splitting at the SiGe/Si heterojunction.[20,21] Strained Si surface channel n-metal–oxide–semiconductor field-effect transistors grown on re-

laxed SiGe, which exploit the LT-Si buffer layer are being investigated.

In conclusion, we have investigated a new defect density reduction method for SiGe heterostructures that uses a LT-Si buffer layer. Both gas-source MBE and UHV-CVD technologies have demonstrated threading dislocation densities as low as 10^4 cm^{-2}. Preliminary SiGe/Si $n-p-n$ HBTs exploiting the LT-Si buffer layer have been grown and fabricated.

The work is supported by the Air Force Office of Scientific Research under Grant No. F49620-95-1-0013 and by an AASERT Fellowship (AFOSR) under Grant No. F49620-94-0404.

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