

Growth of GaAs on SiO_x by molecular-beam epitaxy

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We have investigated the molecular-beam epitaxial growth and photoluminescence properties of GaAs on SiO_x. It is seen that material with a grain size of 0.6–0.8 μm can be grown directly on the dielectric. The properties improve further when the layers are short-term annealed with a halogen lamp. Optimum grain sizes of 1.6 μm are obtained when the as-grown material is annealed at 950 °C for 10 s, and very strong luminescence is observed in the same material. Photoconductive detectors made on the overgrown GaAs show large responsivities.

I. INTRODUCTION

Selective epitaxy is likely to become an increasingly important technology for the realization of two- and three-dimensional integrated devices.¹ By proper annealing of the overgrown polycrystalline GaAs on SiO_x, it is possible to drastically increase integration density and speed of integrated circuits.² Because of the various limiting physical effects and increasing parasitic effects as the device dimensions are reduced, it is important to improve the quality of the overgrown GaAs. There is, therefore, an intrinsic need to study the process of overgrowth, which also opens up the possibility of placing active electronic and optoelectronic devices on SiO_x and on silica fibers. Here we have investigated the controlled growth of GaAs on SiO_x films. The polycrystalline GaAs has been grown under different conditions and has been characterized by high-resolution scanning electron microscopy (SEM) and photoluminescence experiments. The effects on the crystalline properties of the film upon short-term halogen-lamp annealing have been investigated. Crystals with large (1.6-μm) grain sizes are obtained, and planar photoconductive detectors made with the annealed layers exhibit large responsivities, unlike earlier observations with radiation-damaged silicon-on-sapphire.³ The devices may, therefore, be very useful for optical communication applications.

II. MBE GROWTH OF GaAs ON SiO_x

For the first set of experiments, a 2000-Å SiO_x layer was deposited on an undoped and cleaned LEC (100) GaAs wafer by plasma-enhanced chemical vapor deposition (CVD) and on *p*-type (100) Si by CVD. To prepare the dielectric film for overgrowth, it was degreased in organic solvents and etched in 5:1:1::H₂SO₄:H₂O₂:H₂O. The film was loaded into a three-chamber RIBER 2300 growth facility and was initially baked at 400 °C for 30 min. The different parameters related to growth rate and substrate temperature are outlined in Table I. The growth experiments relate to the first three samples: UM473, 544, and 545. The overgrown GaAs film thickness varied from 1 to 3 μm. To compare the prop-

erties of the polycrystalline films with single crystal ones grown under identical conditions, 250-μm-wide openings were defined in the SiO_x layer on GaAs substrates by photolithography and etching.

Low-temperature photoluminescence spectra of the polycrystalline and single-crystal regions are shown in Fig. 1. An SEM micrograph of the two regions are shown in the inset. Very sharp excitonic (1.516 and 1.511 eV) and carbon-related transitions (1.491 eV) are observed in the single crystal, whereas a broad peak (FWHM = 20.5 meV) at 1.45 eV is observed in the polycrystalline region. The latter is typical of heavily mismatched polycrystalline semiconductors. It may be noted from the data in Table I that in the case of sample 545, whose growth was initiated at a low temperature, luminescence was not observed. It is clear that high-temperature growth and lower growth rates are necessary. While the higher growth temperature provides greater surface mobility for atoms to find their appropriate lattice sites, the lower growth rate helps in reducing lattice defects and thereby improves the luminescence intensity. Also, we believe that the photoluminescence characteristics (peak intensity and linewidth) of sample 473 are better than those of sample 544 since the former is thicker (3 μm). The grain boundaries and dislocations merge and coalesce to give a gradual increase in grain size. The driving force for the increase in grain size is the reduction of extra free energy stored in the grain boundary.

Next we consider the properties of layers grown after a preanneal for 10 min at 600–650 °C in as As₄ ambient before growth of the GaAs layer. The binary film was grown at 650 °C with an increasing growth rate of 0.3–5.6 Å/s. The total GaAs thickness was 1 μm. By comparing the photoluminescence (PL) intensities of samples 552 and 544 in Table I, it is evident that the former, grown with preannealing, shows a stronger luminescence. From the RHEED pattern observed during the growth of the two samples, stronger reconstruction was observed in the preannealed one. We believe that during the annealing a smoothening of the dielectric surface occurs, and this favors larger grain size of GaAs and better growth.

III. POST-GROWTH LAMP ANNEALING STUDIES

The different polycrystalline GaAs films were then annealed for a few seconds in a halogen-lamp station under

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TABLE I. Growth parameters and properties of GaAs grown on SiO_x.

Sample	Structure	Growth condition			PL peak energy (eV)	Relative peak intensity (a.u.)	Peak linewidth (FWHM) (meV)
		Rate	Substrate temperature	Film thickness			
UM 473	polyGaAs/SiO _x	1 μm/h	620 °C	3 μm	1.461	13.8	18.0
UM 544	polyGaAs/SiO _x	"	650 °C	1 μm	1.464	5.3	40.3
UM 545	polyGaAs/SiO _x	1 μm/h	450–650 °C	1 μm	No signal		
UM 522 ^b	polyGaAs/SiO _x /GaAs	"	690 °C	1 μm	1.442	40	71.6
UM 591 ^b	polyGaAs/polyAlAsSiO _x /Si	"	AlAs/760 °C	1 μm	1.469	10	42.4
		GaAs/690 °C					
UM 601 ^b	polyGaAs/SiO _x /Si	"	690 °C	1 μm	1.460	2.3	21.9

^a 0.28 Å/s 500 Å + 0.56 Å/s 1000 Å + 2.8 Å/s 35 000 Å + 5.6 Å/s 0.5 μm.

^b Preannealed at 650 °C/10 min before GaAs growth.

flowing N₂ or forming gas. Photoluminescence spectra in Figs. 2 and 3 show the results obtained by annealing two samples at different temperatures. It is clear that annealing at 950 °C gives very high-quality material. In fact, as seen in Fig. 2, the energy of the peak emission for this sample (1.519 eV) is close to the 2-K exciton transition energy in single-crystal GaAs. As the annealing temperature is increased, the film approaches amorphous behavior. This can be understood by considering the relative band gaps in crystalline and amorphous phases of GaAs. The polycrystalline phase can be regarded as being composed of a single-crystal phase together with amorphous grain boundaries. Usually, E_g (amorphous) is smaller than E_g (crystalline). Therefore,

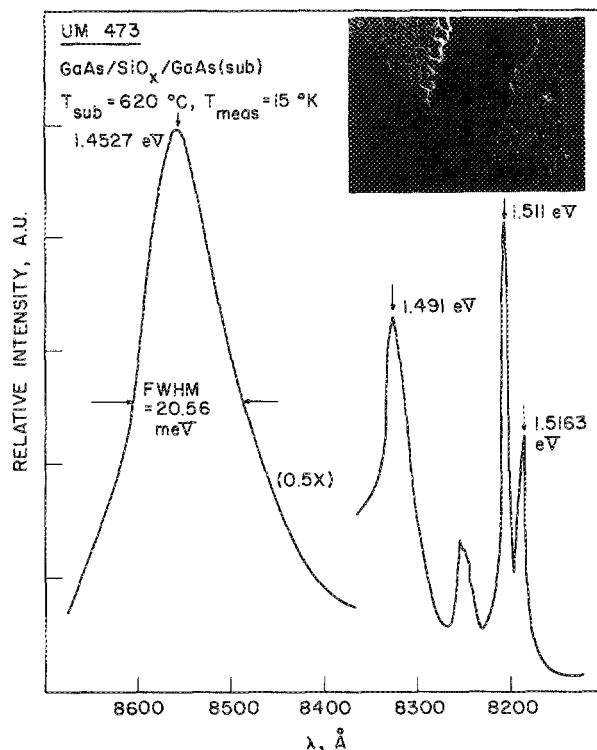


FIG. 1. Low-temperature photoluminescence spectra of single-crystal and polycrystalline GaAs grown on SiO_x. The inset shows the two regions.

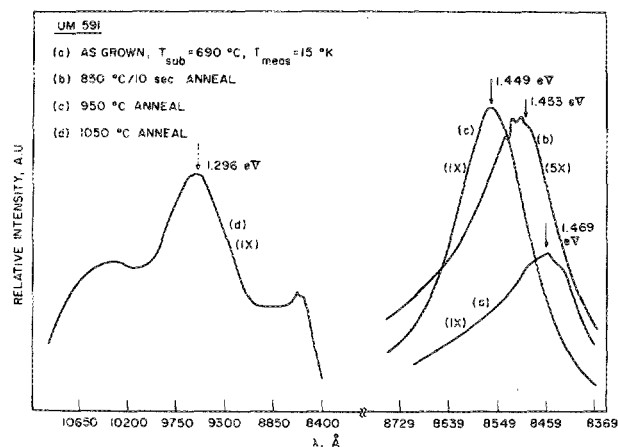


FIG. 2. Low-temperature photoluminescence peaks of as-grown and lamp-annealed GaAs on Si/SiO_x with a preanneal before growth.

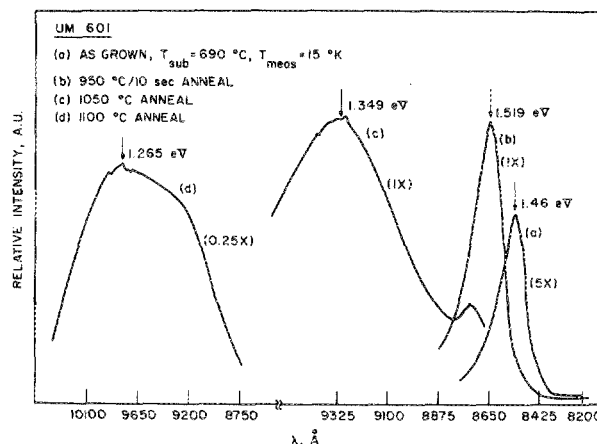
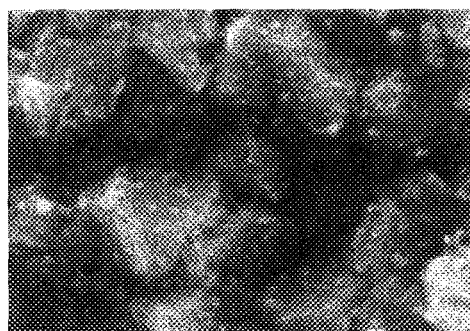


FIG. 3. Low-temperature photoluminescence peaks of as-grown and lamp-annealed GaAs grown on Si/SiO_x with a preanneal.



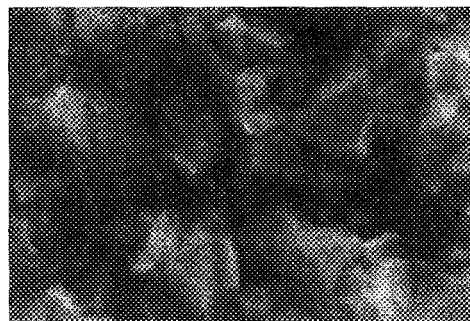
35kV X40,000 400nm

(a)



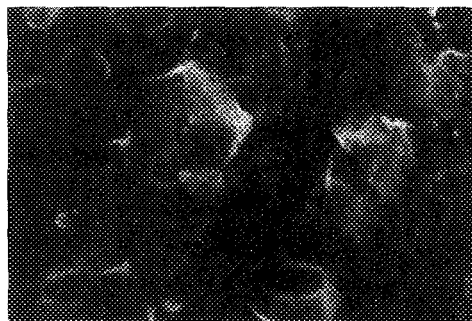
35kV X40,000 400nm

(b)



35kV X40,000 400nm

(c)



35kV X40,000 400nm

(d)

FIG. 4. SEM photomicrographs of GaAs/SiO_x (a) as grown and lamp-annealed for 10 s at (b) 850 °C, (c) 950 °C, and (d) 1050 °C in argon.

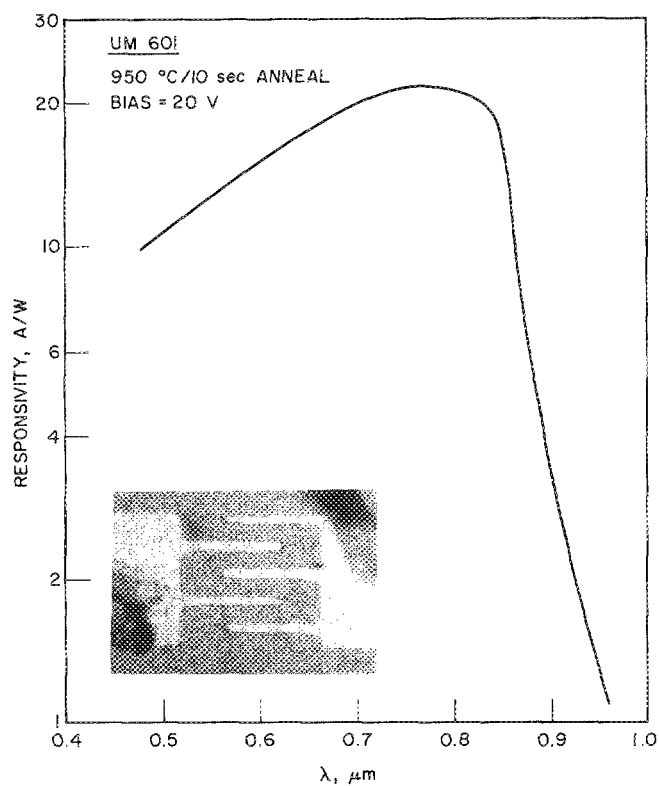


FIG. 5. Spectral response of interdigitated photoconductive detector made on polycrystalline GaAs/SiO_x. The device, with a 14- μm contact spacing, is shown in the inset.

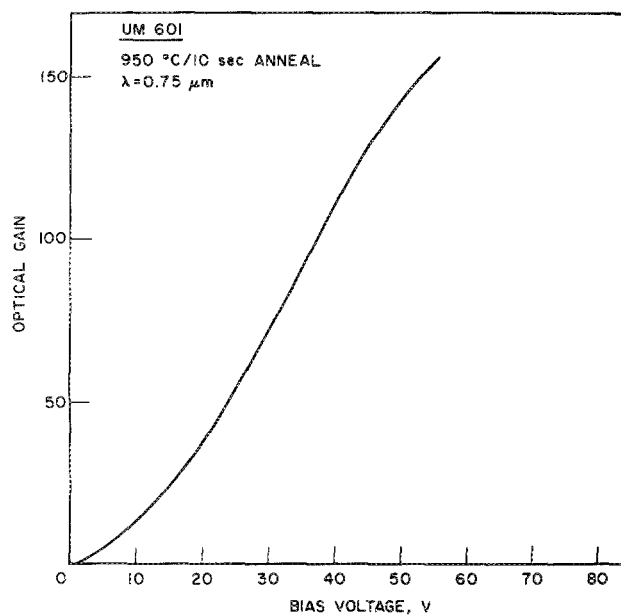


FIG. 6. Dependence of optical gain of GaAs/SiO_x photoconductor on bias.

the shift of the PL peaks to lower energies for the samples annealed at higher temperatures is indicative of amorphous behavior.

The annealing mechanism can be better understood by considering the SEM micrographs of Fig. 4. The grain size of the unannealed crystal is approximately $0.6\text{ }\mu\text{m}$. As the annealing temperature is increased from 850 to $1050\text{ }^{\circ}\text{C}$, the grain size first increases to a maximum of $\sim 1.6\text{ }\mu\text{m}$ and then decreases. This behavior can be understood by considering the following model. At low thermal energy levels, the grain sizes grow because of the reduction of excess free energy at the grain boundaries. As the annealing temperature is increased, a secondary recrystallization is favored. A new grain can be formed between two larger grains, and in this case the size and orientation difference are the driving forces. Secondary recrystallization will fill existing voids, which can result in increased PL intensity. This is observed in our data of Figs. 2 and 3. Note that in the sample annealed at $950\text{ }^{\circ}\text{C}$ the grain size is very uniform, and most of the voids and boundaries are filled with new grains. This is probably the reason why this sample exhibits the best optical properties.

IV. DEVICE RESULTS

Interdigitated photoconductive detectors, with a contact spacing of $14\text{ }\mu\text{m}$, were made on sample 601 annealed at

$950\text{ }^{\circ}\text{C}$ for 10 s. The spectral response of the device is shown in Fig. 5, and the behavior is similar to single-crystal devices. The optical gain of the devices is greater than 150 for bias values $\sim 50\text{ V}$, as shown in Fig. 6. These large gains are contrary to the observed behavior in amorphous materials.² These devices are, therefore, very attractive for long-range optical communication applications.

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¹Y. Inoue, K. Sugahara, S. Kusunoki, M. Nakaya, T. Nishimura, Y. Horiba, Y. Akasaka, and H. Nakata, *IEEE Electron Device Lett.* **EDL-7**, 327 (1986).

²Y. H. Lo, J. M. Hong, M. C. Wu, and S. Wang, *IEEE Electron Device Lett.* **EDL-7**, 586 (1986).

³P. R. Smith, D. H. Auston, A. M. Johnson, and W. N. Augustyniak, *Appl. Phys. Lett.* **38**, 47 (1981).