Lattice-mismatched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ modulation-doped field-effect transistors on GaAs: Molecular-beam epitaxial growth and device performance

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We describe here the properties of $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ modulation-doped heterostructures and field-effect transistors grown directly by molecular-beam epitaxy on GaAs substrates. The generation and nature of dislocations in the films have been studied by transmission-electron microscopy. The final heterostructure contains a series of compositional steps of $In_xGa_{1-x}As$ ($0 \leqslant x \leqslant 0.53$) to generate and control the dislocation movement. The modulation-doped heterostructures are characterized by $\mu_{300\,K} = 8\,150$ cm^2/V s ($n_s = 2.7\times10^{12}$ cm^{-2}) and $\mu_{20\,K} = 26\,100$ cm^2/V s ($n_s = 2.1\times10^{12}$ cm^{-2}) which compare very favorably with values measured in similar lattice-matched heterostructures on InP. 1.4-μm gate-modulation-doped field-effect transistors exhibit g_m (ext) = 240 mS/mm and $f_T = 21$ GHz. The drain current variation with gate bias is linear and the transconductance is uniform over a sizeable voltage range. These material and device characteristics indicate that $In_xGa_{1-x}As/In_xAl_{1-x}As$ transistors (with x varying over a certain range to vary ΔE_c) can be designed on GaAs or even other mismatched substrates.

I. INTRODUCTION

$GaAs/Al_xGa_{1-x}As$ and $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ modulation-doped field-effect transistors (MODFETs) have emerged as leading devices for high-frequency and low-noise applications. The $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterostructure lattice matched to InP has recently been investigated in many laboratories around the world because of inherent advantages over the GaAs/AlGaAs system. Some of these attributes are a higher electron mobility and velocity at room temperature compared to GaAs, a large Γ-L separation in InGaAs, and a large conduction-band discontinuity in the heterostructure. The last parameter, coupled with the fact that the InAlAs can be more heavily doped than AlGaAs, results in more efficient transfer doping and sheet electron concentration. Indeed, very promising dc and microwave performance is being reported in 1-μm and submicron-gate MODFET devices.[1,2]

To enhance the performance of InP-based devices, we have recently grown and characterized pseudomorphic $In_{0.53+x}Ga_{0.47-x}As/In_{0.52}Al_{0.48}As$ modulation-doped heterostructures.[3] A steady improvement in electron mobility and velocity is seen with increase of In content in the channel, without any significant change in the electron effective mass. 1.0-μm- and submicron-gate MODFETs made from these heterostructures also show improved performance over lattice-matched devices.[2,4] However, it is difficult to make $x > 0.15$ in the channel without creating misfit dislocations and degrading the performance.

In a pseudomorphic heterostructure, there is always the issue of long-term reliability under repeated thermal cycling and other environmental changes. Only recently has this issue in MODFETs been addressed by Peercy *et al.*[5] An alternative by which it is possible to take advantage of high In content in the channel and avoid pseudomorphic strain is to use strain-relaxed mismatched heterostructures. Rather than do this on InP substrates, it is worthwhile to take into account a larger mismatch and attempt growth on GaAs or Si substrates. This also provides a technique for integrating InGaAs/InAlAs devices with the more established Si or GaAs integrated circuit technology. The overriding cause for concern here in the large densities of dislocations that are generated and their effect on the material characteristics and device performance. In fact, recently, the performance of 0.1-μm-gate $In_{0.5}Ga_{0.5}As/In_{0.5}Al_{0.5}As$ MODFETs grown by molecular-beam epitaxy on GaAs substrates has been reported by Wang *et al.*[6] Good dc and microwave performance was obtained in spite of the mobilities in the channel being very low (5200 cm^2/V s at 300 K and 6000 cm^2/V s at 77 K). 0.4-μm-gate $In_{0.08}Ga_{0.92}As$ metal-semiconductor field-effect transistors (MODFETs) on GaAs with promising dc and microwave performance have also been recently reported by Shih *et al.*[7] These early studies clearly demonstrate that reasonably high-performance InGaAs/InAlAs devices can be made on GaAs substrates. We have therefore investigated the molecular-beam epitaxial (MBE) growth of these modulation-doped heterostructures, in an attempt to achieve transport properties similar to that in lattice-matched heterostructures on InP substrates. In what follows, we will discuss the molecular-beam epitaxial growth and characteristics of $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterostructure on GaAs and the properties of MODFETs made from them. The In composition is chosen to be the lattice-matched value on InP for comparison.

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II. MBE GROWTH OF $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ ON GaAs

The techniques that are conventionally used for lattice-mismatched semiconductor heteroepitaxy are (a) two-step growth,[8–10] (b) incorporation of a strained layer superlattice (SLS) buffer[8,11] or a linear graded composition buffer layer,[12] and (c) *in situ* or post-growth thermal treatment.[8,13,14] Since the minimum-energy configuration for lattice-mismatched strained epitaxy favors an island growth mode,[15] two-step growth with different substrate temperatures and growth rates is applied. With a lower substrate temperature, surface nucleation of the epilayer dominates over surface migration to form small islands. It is suggested that a thickness of 50–100 nm for this growth mode is sufficient to complete the substrate surface coverage.[8] Conventional lattice-matched homo- or heteroepitaxial growth conditions are then applied to complete the second-step growth. A large number of the misfit dislocations generated in the first-step buffer layer thread up through the entire epilayer. In the case of GaAs on Si, which is about 4% lattice mismatched, dislocation densities of $\sim 10^8$ cm^{-2} in the active layer are generally observed.[16]

In order to reduce the threading dislocation density, an SLS or linearly graded composition buffer is commonly used.[8,11] The SLS creates an additional strain energy field in the epilayer which can interact with the threading dislocations. It is possible for the threading dislocations to recombine with each other in the superlattice region or bend at the strained interface and propagate along the interface to the edge of the substrate. It is found that the dislocation density in the GaAs epilayer grown on Si can be lowered to the range of 10^7 cm^{-2} by incorporating an SLS.[8,17] On the other hand, linearly composition graded buffer layers have been considered a better approach.[8] It has been reported that with the incorporation of linearly graded buffer layers, the density of threading dislocations is still high, but x-ray rocking curve half-widths[18] and the electron mobility[19] in the active layer suggest an improvement. Thermal treatment is a useful technique for material recovery. *In situ* and/or post-growth annealing have been widely studied for the strained epitaxy of GaAs on Si.[13,14] However, such annealing can only reduce dislocation density to the range of 10^7 cm^{-2}. So far none of these methods has been successful to the degree required.

In our study, we have examined the growth of several different compositions of $In_xGa_{1-x}As$ on GaAs by cross-sectional transmission-electron microscopy (XTEM). Figure 1 shows the XTEM micrographs for $\sim 1\%$ and $\sim 2\%$ lattice-mismatched InGaAs/GaAs growth by MBE under conditions described later. The InGaAs layer is directly grown on a 0.3-μm GaAs buffer layer on the substrate. After growth of the ternary layer, ten periods of a InGaAs/GaAs superlattice are grown. This is seen at the top of the figures. It is found that when the misfit is less than 2%, few threading tails of the misfit dislocations can be observed. This means that the dislocation density in the epilayer is below the detection limit ($\ll 10^6$ cm^{-2}). In order to understand the interfacial misfit dislocation network in Fig. 1(a) through TEM, a 0.15-μm $In_{0.15}Ga_{0.85}As$ epilayer was grown on a GaAs substrate. The plan-view TEM micrograph of the misfit dislocations structure at the $In_{0.15}Ga_{0.85}As$/GaAs heterointerface is shown in Fig. 2. After the strain relaxation, most of the misfit dislocations are confined at the heterointerface. A detailed study of the misfit dislocations generation and propagation for InGaAs/GaAs strained heteroepitaxy is discussed elsewhere.[20]

In the case of the $In_{0.53}Ga_{0.47}As$/GaAs heterostructure there is a 3.8% lattice mismatch. The only way to avoid a high threading dislocation density in this large lattice-mismatched system is to use the composition step-grading technique, which was first applied by Olsen *et al.* using vapor phase epitaxy.[21] They found that the technique was much more efficient than linear grading as a dislocation filter. From several calibration experiments we found that each step of the compositional gradient should not be higher than 10% In. Above 10% In, a large number of threading dislocations was found in the later composition steps. Again, the gradient should not be too low, otherwise the dislocation

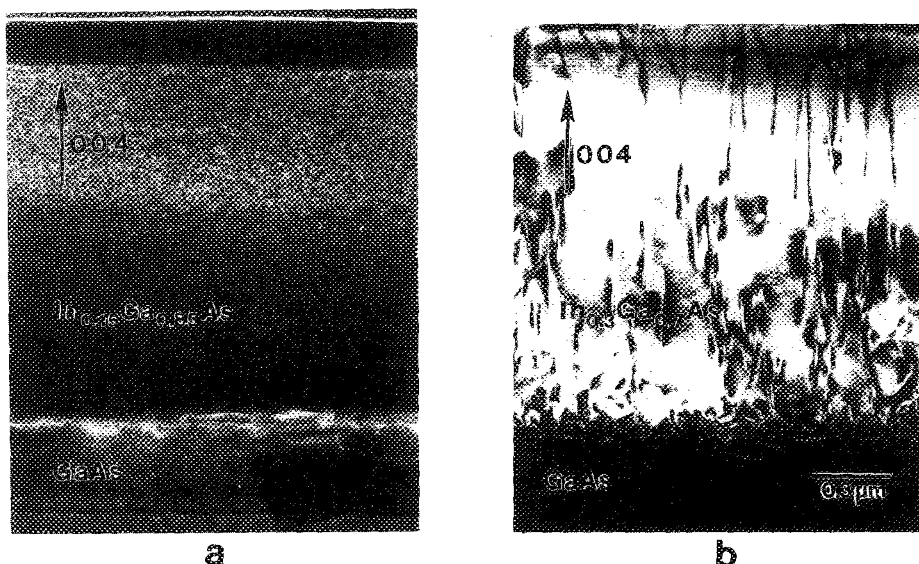


FIG. 1. Cross-sectional TEM micrograph of $In_xGa_{1-x}As$/GaAs heteroepitaxial structure for (a) $x = 0.15$ and (b) $x = 0.3$.

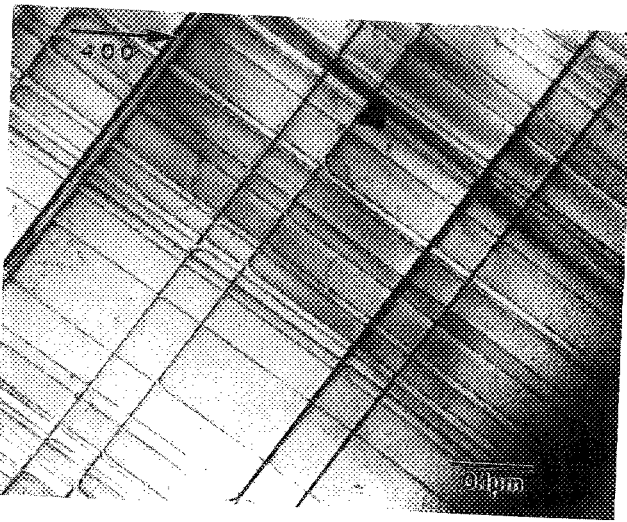


FIG. 2. Plan-view TEM micrographs of general misfit dislocation network at the $In_{0.15}Ga_{0.85}As/GaAs$ heteroepitaxial interface grown by MBE.

propagation is not effectively checked. Moreover, the lower the gradient, the higher the critical layer thickness. This means that very thick layers would be needed at each step for complete misfit strain relaxation. In our experiments, 300-nm steps were used for each composition. Below this thickness, the electron mobility was seriously affected by the interfacial misfit dislocations.[19] The schematic of the MODFETs is shown in Fig. 3. Five step-graded buffer layers were first grown on the semi-insulating GaAs substrate at decreasing substrate temperatures in the range of 550–450 °C. A 1.0-μm $In_{0.53}Ga_{0.47}As$ buffer layer followed by a 0.5-μm undoped $In_{0.52}Al_{0.48}As$ layer were then grown. The active layers are composed of a 0.1-μm undoped $In_{0.53}Ga_{0.47}As$ channel, 50-Å undoped $In_{0.52}Al_{0.48}As$ spacer layer, a 300-Å Si-doped $In_{0.52}Al_{0.48}As$ layer (3×10^{18} cm^{-3}), and a 100-Å GaAs cap layer with a Si doping density of 5×10^{17} cm^{-3}. The incorporation of the GaAs layer[1] provides two advantages. First, the quality of the Schottky diode on GaAs is better than on doped InAlAs, and second, a difficult gate recessing step is eliminated. All the active layers were grown at 450 °C and at a rate of 1 $\mu m/h$ for $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ and one As partial pressure of 1×10^{-5} Torr. A XTEM micrograph of the strained epilayer is shown in Fig. 4. It is found that the majority of the misfit dislocations are contained at the five heterointerfaces. Some of the dislocations thread through the bulk $In_{0.53}Ga_{0.47}As$ buffer layer and cluster in the $In_{0.52}Al_{0.48}As$ layer. These dislocation clusters may be due to phase separation in the InAlAs alloy which was grown at 450 °C.[22]

Temperature-dependent Hall measurements were made on photolithographically defined clover leaf samples using the van der Pauw technique. The temperature-dependent mobility and sheet electron concentration for the heterostructure with which FETs were made are shown in Fig. 5. The measured parameters at 300 K are $\mu = 8150$ $cm^2/V\,s$, $n_s = 2.7\times10^{12}$ cm^{-2}, and at 20 K are $\mu = 26\,100$ $cm^2/V\,s$ and $n_s = 2.1\times10^{12}$ cm^{-2}. These transport parameters are quite comparable to those measured in lattice matched heterostructures on InP,[1,2] indicating that interface roughness does not pose a severe limitation. It may be mentioned that the mobility values obtained in the course of this study are the highest obtained for this heterostructure grown on

Thickness	Layer	Doping
100 Å	n GaAs	(5E17)
300 Å	n+ $In_{0.52}Al_{0.48}As$	(3E18)
50 Å	i $In_{0.52}Al_{0.48}As$	
0.1 μm	i $In_{0.53}Al_{0.47}As$	
0.5 μm	i $In_{0.52}Al_{0.48}As$	
30Å/30Å	InGaAs/InAlAs	(30 Periods)
1.0μm	$In_{0.5}Ga_{0.5}As$	
0.3 μm	$In_{0.5}Ga_{0.5}As$	
0.3 μm	$In_{0.4}Ga_{0.6}As$	
0.3 μm	$In_{0.3}Ga_{0.7}As$	
0.3 μm	$In_{0.2}Ga_{0.8}As$	
0.3 μm	$In_{0.1}Ga_{0.9}As$	
0.3 μm	GaAs buffer	
	GaAs Substrate	

FIG. 3. Schematic cross section of the modulation-doped $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterostructure above a compositional step-graded buffer on a GaAs substrate.

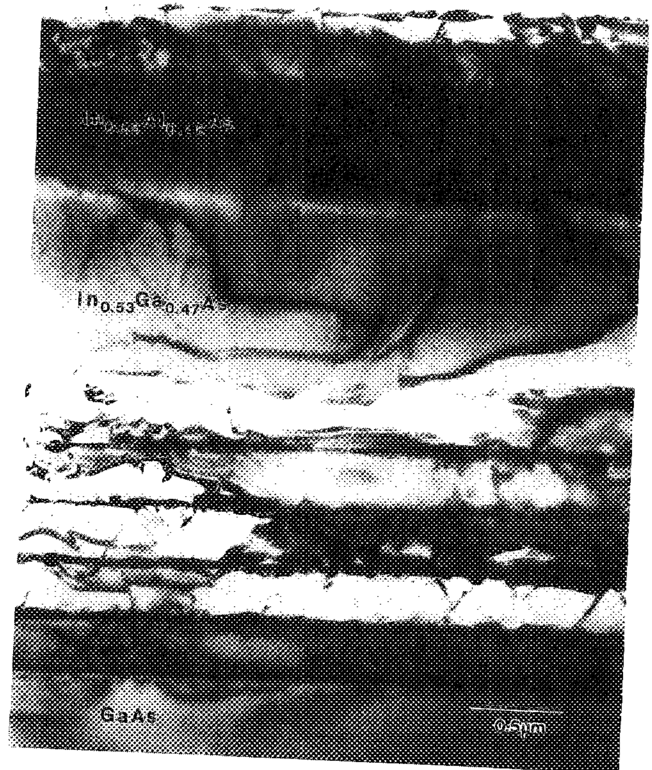


FIG. 4. Cross-sectional TEM micrograph of the modulation-doped heterostructure grown by MBE.

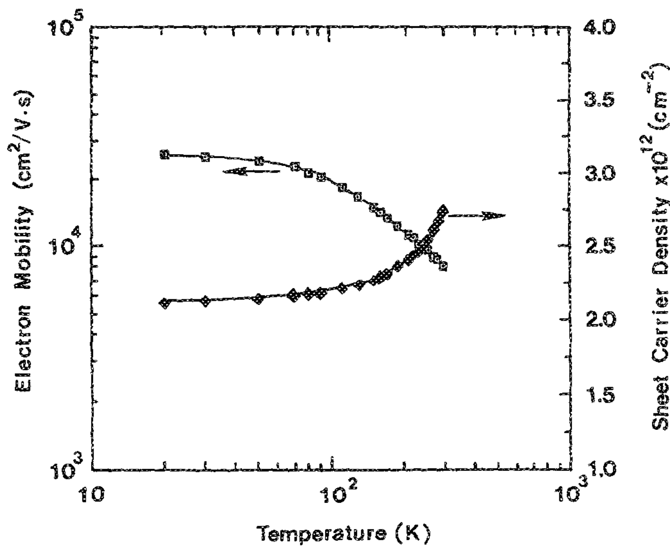


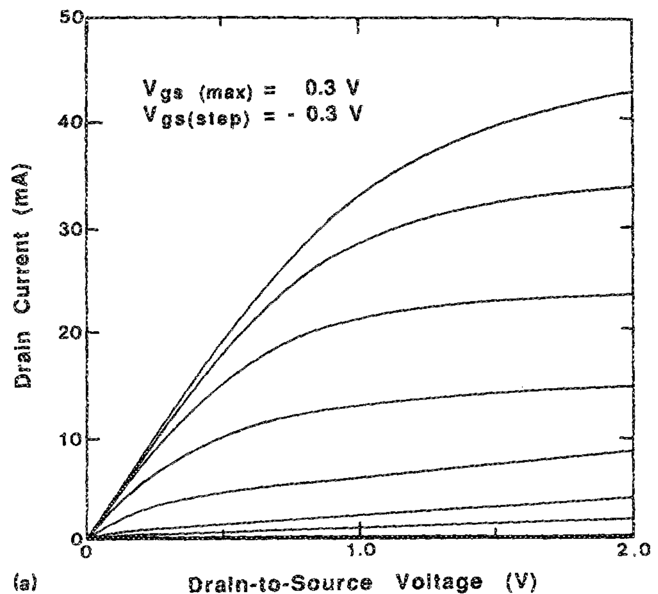
FIG. 5. Sheet carrier density (n_s) and electron mobility (μ) dependence on temperature for $In_{0.53}Ga_{0.47}As/In_{0.52}Ga_{0.48}As$ MODFETs on GaAs substrate.

GaAs. The results also indicate that practical heterostructures can perhaps be grown on Si substrates.

III. DEVICE FABRICATION AND CHARACTERIZATION

1.4-μm-gate transistors were fabricated with heterostructures whose transport characteristics are shown in Fig. 5. After mesa-etching for device isolation, Ga/Au/Ni/Ti/Au were evaporated in that sequence and rapid thermal annealed for 10 s at 425 °C to form the source and drain ohmic contacts. The source-drain separation is approximately 3.5 μm. 500-Å Ti/3000-Å Au was evaporated to form the gate contact. The gate dimension is 1.4×200 μm^2. The native oxides on the surface were removed just before the ohmic contact and gate metal depositions by immersing the samples in buffered HF for 30 s. The room-temperature gate-source current-voltage characteristics typically exhibit a leakage current of ~300 μA at -2 V, in spite of the top GaAs layer. We believe that the high leakage current is due to the large dislocation density and surface roughness.

Room-temperature drain current-voltage characteristics are depicted in Fig. 6(a), where good pinchoff is demonstrated. The output conductance g_{DS} was 16.5 mS/mm. The extrinsic dc transconductance is 240 mS/mm compared to a typical value of 400–450 mS/mm in a lattice-matched InP-based device with the same gate length. Very little hysteresis is observed in the characteristics, which suggests a low density of defects in the barrier layer and its interface with the channel. Figure 6(b) illustrates some features of the transistor dc characteristics. The greater confinement in the two-dimensional electron gas due to a larger band offset ($\Delta E_c \cong 0.51$ eV) results in a linear variation of I_{DS} and a uniform transconductance is exhibited over a sizeable gate voltage range. The typical source resistance was $R_S = 5$ Ω from which an intrinsic transconductance of 320 mS/mm is derived. The I_{dss}, values are the same as measured in lattice-matched transistors.[4] The microwave S parameters were measured in the range of 0.045–26.5 GHz using a cascade prober and an HP 8510 automatic network analyzer under various bias conditions. The variation of current gain with frequency is shown in Fig. 7. A value of $f_T = 21$ GHz is derived, while the value of $f_{max} = 20$ GHz, obtained from a measurement of maximum available gain with frequency, is slightly lower. This phenomenon of f_{max} having a value less than f_T is not well understood. However, parasitic conduction due to the dislocations is partly responsible for this phenomenon.[6] The best 1.4-μm lattice-matched InGaAs/InAlAs/InP transistors have $f_T = 30$–35 GHz at 300 K.[4] It is clear, therefore, that the mismatched transistors investigated here have very favorable dc and microwave characteristics.



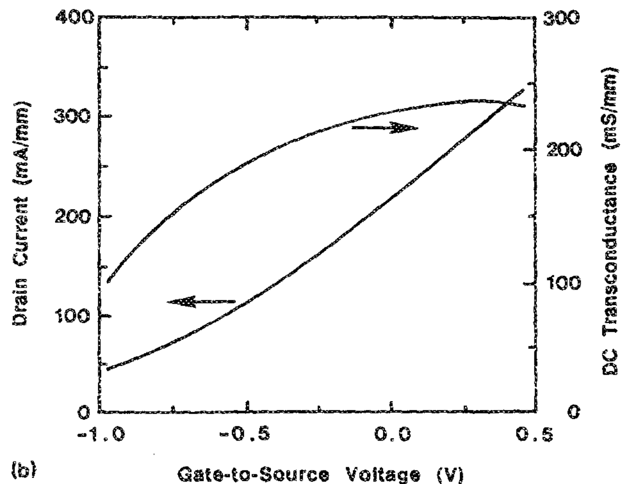


FIG. 6. (a) Drain current-voltage characteristics and (b) variation of drain current and dc transconductance with gate bias for a 1.4×200 μm^2 gate $In_{0.53}Ga_{0.47}As/In_{0.52}Ga_{0.48}As$ MODFETs on GaAs.

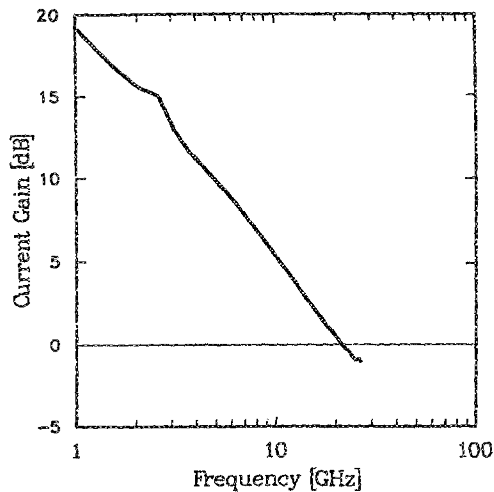


FIG. 7. Variation of current gain (h_{21}) with frequency in a $1.4\times200\ \mu m^2$ gate MODFET.

IV. CONCLUSIONS

It has been demonstrated that excellent dc and microwave characteristics can be obtained in $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ MODFETs grown directly on GaAs substrates. The strain-relieved heterostructures were grown by molecular-beam epitaxy and a series of variable composition buffer layers were incorporated to generate and control the propagation of dislocations in the active region. TEM studies have been made to characterize the confinement of dislocations. The Hall mobilities of the 2DEG [n_s (300 K) $= 2.7\times10^{12}$ cm^{-2}] are 8150 and 26 100 cm^2/V s at 300 and 20 K, respectively. An extrinsic transconductance of 240 mS/mm and f_T of 21 GHz are measured at 300 K for 1.4-μm-gate devices. These characteristics compare very favorably with equivalent lattice-matched devices on InP substrates. Better performance is expected with submicron devices. This work also suggests that high-performance InGaAs/InAlAs MODFETs can be made on other mismatched structures, such as Si, with proper control of the growth parameters and dislocation motion.

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[1] W.-P. Hong and P. Bhattacharya, IEEE Electron Dev. Lett. **9**, 352 (1988).

[2] U. K. Mishra, A. S. Brown, S. E. Rosenbaum, C. E. Hooper, M. W. Pierce, M. J. Delaney, S. Vaughn, and K. White, IEEE Electron Dev. Lett. **9**, 647 (1988).

[3] W.-P. Hong, G. I. Ng, P. K. Bhattacharya, D. Pavlidis, and S. Willing, J. Appl. Phys. **64**, 1945 (1988).

[4] G. I. Ng, W.-P. Hong, D. Pavlidis, M. Tutt, and P. K. Bhattacharya, IEEE Electron Dev. Lett. **9**, 439 (1988).

[5] P. S. Peercy, B. W. Dodson, J. Y. Tsao, E. D. Jones, D. R. Myers, T. E. Zipperian, L. R. Dawson, R. M. Biefeld, J. F. Klem, and C. R. Hills, IEEE Electron Dev. Lett. **9**, 621 (1988).

[6] G. Wang, Y. Chen, W. J. Schaff, and L. F. Eastman, IEEE Trans. Electron. Dev. **35**, 818 (1988).

[7] H. Shih, B. Kim, K. Bradshaw, and H. W. Tserng, IEEE Electron Dev. Lett. **9**, 604 (1988).

[8] J. S. Harris, S. M. Koch, and S. J. Rosner, Mater. Res. Soc. Symp. Proc. **91**, 3 (1987).

[9] T. Soga, T. Imori, and M. Umeno, Jpn. J. Appl. Phys. **26**, L536 (1987).

[10] A. Chin, P. Bhattacharya, K. H. Chang, and D. Biswas, J. Vac. Sci. Technol. B **7**, 283 (1989).

[11] T. Nishimura, K. Mizuguchi, and N. Hayafuji, Jpn. J. Appl. Phys. **26**, L1141 (1987).

[12] M. S. Abrahams, L. R. Weisberg, C. J. Buiocchi, and J. Blanc, J. Mater. Sci. **4**, 223 (1969).

[13] Y. Fukuda and Y. Kohama, Jpn. J. Appl. Phys. **26**, L597 (1987).

[14] C. Choi, N. Otsuka, G. Munns, R. Houdre, H. Morkoc, S. L. Zhang, D. Levi, and M. V. Klein, Appl. Phys. Lett. **50**, 992 (1987).

[15] P. R. Berger, K. Chang, P. Bhattacharya, J. Singh, and K. K. Bajaj, Appl. Phys. Lett. **53**, 684 (1988).

[16] N. Chand, R. Fisher, A. M. Sargent, D. V. Lang, and A. Y. Cho, Mater. Res. Soc. Symp. Proc. **91**, 233 (1987).

[17] N. El-Masry, N. Hamaguchi, J. C. L. Tarn, N. Karam, T. P. Humphreys, D. Moore, S. M. Bedair, J. W. Lee, and J. P. Salerno, Mater. Res. Soc. Symp. Proc. **91**, 99 (1987).

[18] S. Sakai, T. Soga, M. Takeyasu, and M. Umeno, Mater. Res. Soc. Symp. Proc. **67**, 15 (1987).

[19] T. S. Kim, H. D. Shih, J. M. Anthony, D. L. Farrington, J. A. Keenan, and T. M. Moore, J. Vac. Sci. Technol. B **7**, 376 (1989).

[20] K. H. Chang, P. K. Bhattacharya, and R. Gibala, Appl. Phys. **66**, 2993 (1989).

[21] G. H. Olsen, M. S. Abrahams, C. J. Buiocchi, and T. J. Zamerowski, J. Appl. Phys. **46**, 1643 (1975).

[22] A. S. Brown, M. J. Delaney, and J. Singh, J. Vac. Sci. Technol. B **7**, 384 (1989).