Epitaxial La-doped $SrTiO_3$ on silicon: A conductive template for epitaxial ferroelectrics on silicon

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Use of an epitaxial conducting template has enabled the integration of epitaxial ferroelectric perovskites on silicon. The conducting template layer, $La_xSr_{1-x}TiO_3$ (LSTO), deposited onto (001) silicon wafers by molecular-beam epitaxy is then used to seed {001}-oriented epitaxial perovskite layers. We illustrate the viability of this approach using $PbZr_{0.4}Ti_{0.6}O_3$ (PZT) as the ferroelectric layer contacted with conducting perovskite $La_{0.5}Sr_{0.5}CoO_3$ (LSCO) electrodes. An important innovation that further facilitates this approach is the use of a low-temperature (450 °C) sol–gel process to crystallize the entire ferroelectric stack. Both transmission electron microscopy and x-ray diffraction analysis indicate the LSCO/PZT/LSCO/LSTO/Si heterostructures are epitaxial. The electrical response of ferroelectric capacitors (for pulse widths down to 1 μs) measured via the underlying silicon substrate is identical to measurements made using conventional capacitive coupling method, indicating the viability of this approach. © *2002 American Institute of Physics*. [DOI: 10.1063/1.1484552]

There has been an increasing effort to integrate ferroelectric thin films with silicon complementary metal–oxide–semiconductor technology to enable commercially viable, high-density, nonvolatile ferroelectric memories, and other technologies. Among different proposed integration architectures, the stacked architecture with one transistor and one capacitor (1T-1C) is preferred.[1] In such a memory cell, the drain is contacted to the bottom electrode of the ferroelectric capacitor through a silicon plug that is typically polycrystalline. A diffusion barrier layer is interposed between the bottom oxide electrode and silicon wafer to eliminate the strong propensity for a chemical reaction at the interface during thermal processing of the ferroelectric capacitor.[2–5] Since these barriers are typically deposited onto a polycrystalline Si plug that contacts the pass transistor, the whole ferroelectric stack is also polycrystalline. While such an approach is quite valuable, it would also be of interest to explore the possibility of growing epitaxial ferroelectric layers, thus ensuring a significantly higher polarization as well as uniform properties over large scales and at small feature sizes. Such an approach is especially important when the ferroelectric grain size is commensurate with that of the lateral dimensions of the storage cell.[6]

On another related front, there has been significant progress in the growth of epitaxial oxides on semiconductors.[7–10] Of specific interest is the development of epitaxial $SrTiO_3$ (STO) on silicon for use as an alternative gate dielectric.[11–13] We have previously demonstrated that this insulating STO layer can be effectively used as a template layer to seed the epitaxial growth of ferroelectric layers.[14] We, therefore, posed this question: Is it possible to chemically alter the STO layer to make it conducting, thereby providing both desiderata simultaneously, namely a conducting barrier and a structural template? This letter reports that this is indeed possible. It is enabled by the fact that

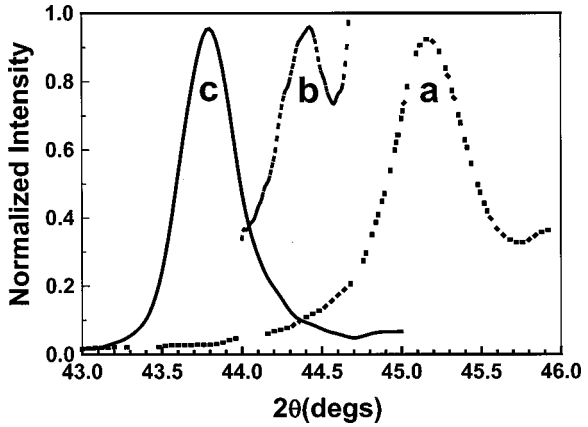

FIG. 1. θ–2θ x-ray diffraction patterns of LSCO/PZT/LSCO grown on various substrates: (a) on LSTO/Si by sol gel at 450 °C, (b) on STO by sol gel at 450 °C, and (c) on STO by PLD at 650 °C.

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the resistivity of the STO (normally an insulator) can be systematically altered through chemical substitution at either the Sr site (e.g., by La), the Ti site (e.g., by Nb), or the O site (by vacancies) to make it conductive.[15]

The $La_xSr_{1-x}TiO_3$ (LSTO) layer was deposited onto (001) Si wafers using a molecular-beam epitaxy approach similar to that reported by McKee *et al.*[11] This process involves the use of an intermediate silicide layer and alkaline earth oxide formation to enable the transition from silicon to perovskite. Using this process, films with lanthanum content from 0–30 at. % were grown. As an illustrative example, we have used a 27% La substitution with a LSTO layer thickness of 60 nm. $La_{0.5}Sr_{0.5}CoO_3$ (70 nm)/$PbZr_{0.4}Ti_{0.6}O_3$ (120 nm)/$La_{0.5}Sr_{0.5}CoO_3$ (70 nm) (LSCO/PZT/LSCO) heterostructures were fabricated on LSTO/Si substrates using a combination of both magnetron sputtering (for the LSCO layers) and sol–gel (for the PZT layer). A 100 nm thick aluminum film was first deposited on the back side of the silicon wafer to facilitate ohmic contact for vertical measurements. All three layers were annealed for 1 h each at 450 °C in 1 atm of oxygen. The details of the sol–gel processing are reported elsewhere.[16] For comparison, epitaxial LSCO/PZT/LSCO heterostructures (with the same PZT composition and thickness) were deposited by pulsed laser deposition (PLD) on single crystal (001) STO substrates and by conventional sol–gel at 650 °C. For electrical testing, 50 μm diameter platinum dots were patterned by standard photolithography followed by a lift off and wet etching. The electrical properties of the capacitors were measured vertically from the back side of the silicon substrate to the top electrode.

A typical θ–2θ x-ray diffraction scan in the vicinity of the 200 and 002 peaks of LSCO/PZT/LSCO is shown in Fig. 1.[17] In-plane ϕ-scans (not shown) reveal that the films are epitaxial with the expected four-fold symmetry as a consequence of the in-plane orientation locking of the PZT layer with that of the LSTO template layer. A *c*-axis lattice parameter of 4.04 Å was calculated from the diffraction patterns. In Fig. 1, we compare the diffraction pattern from this film to those from films grown on (001) STO substrates by PLD 650 °C and by sol gel at 450 °C. The film deposited by PLD is epitaxial with a high degree of *c*-axis orientation; however, the *c*-axis length is significantly longer (4.12 Å). Finally, the sol–gel film deposited on STO is highly *c*-axis oriented with a lattice constant of 4.08 Å.

Transmission electron microscopy (TEM) characterization of the LSCO/PZT/LSCO/LSTO/Si heterostructure is shown in Fig. 2. Figure 2(a) is a cross-sectional dark-field TEM image of the heterostructure. Electron diffraction patterns from each of the layers are shown in Figs. 2(b)–2(d). Clean and sharp interfaces are visible between the LSTO layer and the underlying Si as well as between the LSCO layer and the underlying LSTO layer. An intermediate layer approximately 5 nm thick formed by the interdiffusion of cations, e.g., Co^{2+}, Sr^{2+}, Pb^{2+}, Zr^{4+}, and Ti^{4+}, was observed between the PZT layer and the underlying LSCO layer. Selected-area electron diffraction (SAED) studies [Figs. 2(b)–2(d)] revealed the epitaxial growth of each layer. A more detailed description of the microstructure and the interfacial chemistry of the heterostructures will be reported elsewhere.[18]

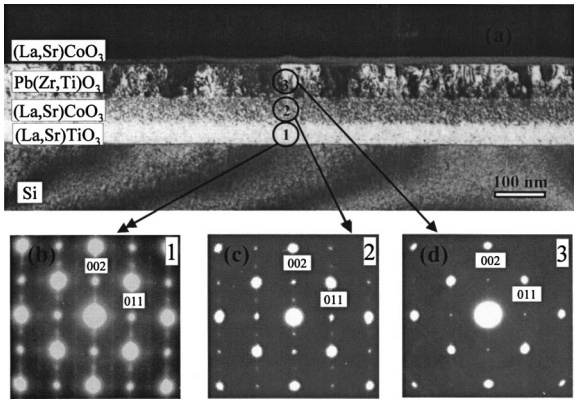

FIG. 2. (a) A dark-field TEM image of LSCO/PZT/LSCO/LSTO/Si in which the LSCO and PZT layer were prepared at 450 °C; (b–d) show SAED patterns from the various layers in the heterostructure.

We have subjected the capacitors to a variety of stringent electrical tests to probe the performance characteristics of these highly oriented films. The 120 nm thick PZT films exhibit resistivity values of $1-3\times10^{10}$ Ω cm at 5 V that do not change appreciably from 1–12 V. The ferroelectric responses under both quasistatic (i.e., low-frequency hysteresis loops) as well as dynamic (i.e., under short pulse testing) are shown in Fig. 3. The remnant polarization (P_r) and coercive voltage are about 25 μC/cm^2 and 1 V, respectively at 5 V. Several comparisons are of interest with respect to the hysteresis loops. First, at 5 V, the loops for the 450 °C-processed films are almost the same as that of a capacitor stack processed at 650 °C using our conventional sol–gel process. This indicates that the ferroelectric behavior of the PZT layer processed at 450 °C is likely to be similar to that of the film processed at 650 °C. Second, there is very little difference in the shape, symmetry, and magnitude of the hysteresis loops when measured in either the vertical or horizontal capacitive coupling geometry. This strongly suggests the absence of an insulating interface between the silicon substrate and the LSTO template/barrier layer. Third, typical hysteresis loops from the film deposited by PLD are very rectangular and the remanent polarization is of the order of 50–60 μC/cm^2 at 5 V, while those deposited at 450 °C show similar square loops, although with a smaller polarization.

Figure 3(b) shows the pulse-width dependence of polarization [switched (P^*)–nonswitched ($\hat{P}$)]. A key point of reference is the value of this pulse polarization at a pulse

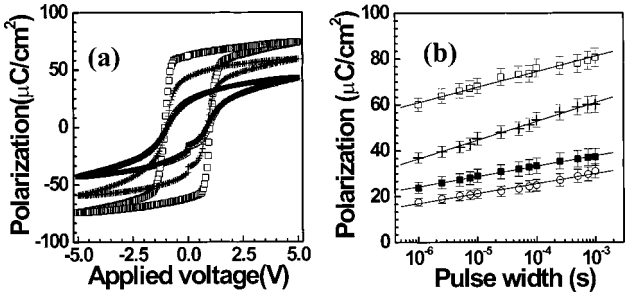

FIG. 3. (a) Hysteresis loops and (b) pulse-width dependence of polarization for LSCO/PZT/LSCO test capacitors made on various substrates: (●) made by sol gel on LSTO/Si at 450 °C, capacitive coupling; (○) made by sol gel on LSTO/Si at 450 °C, vertical transport; (■) made by conventional sol gel on LSTO/Si at 650 °C, capacitive coupling; (+) made by sol gel on STO at 450 °C; (□) made by PLD on STO at 650 °C.

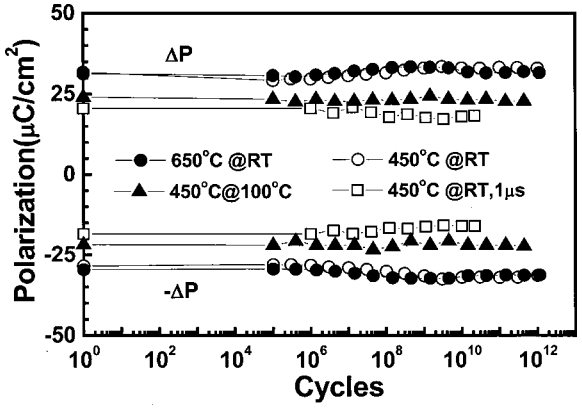

FIG. 4. Fatigue characteristics of capacitively coupled LSCO/PZT/LSCO test capacitors at room temperature and 100 °C made by the following methods: (●) made by conventional sol gel at 650 °C, 8.6 μs write pulse width, 130 μs read pulse; (○) made by sol gel at 450 °C, 8.6 μs write pulse width, 130 μs read pulse; (▲) made by sol gel at 450 °C, tested at 100 °C using 8.6 μs write pulse width, 130 μs read pulse; (□) made by sol gel at 450 °C, 1 μs write and read pulses.

width of 1 μs. The data shows that this is ~20 μC/cm^2 at 5 V and increases to about 32 μC/cm^2 at 1 ms. We note that the pulse-width dependence is almost the same as that of a ferroelectric stack prepared on the same substrate (i.e., LSTO/Si) using a conventional 650 °C sol–gel process as well as the epitaxial films prepared on STO substrates. Also, we observe no difference in the pulse-width dependence when measured via both vertical transport and capacitive coupling. This suggests that there is no significant resistive drop across the LSTO/Si interface, at least for pulse widths down to 1 μs. Quantitative fits of the pulse-width dependence for the four samples yield a slope that is essentially the same (~4.5 μC/cm^2 per decade) for all of them. The structural data (Figs. 1 and 2) coupled with the ferroelectric measurements suggest the following: the lower polarization observed in the epitaxial films on silicon can be traced to two sources, namely the smaller *c*-axis lattice parameter and the very likely possibility of the formation of *a*-axis oriented PZT grains. A smaller *c*-axis lattice parameter translates to a smaller tetragonality $(c/a-1)$ and consequently a lower polarization [since $(P_s)^2 \propto (c/a-1)$].[19]

Our previous results have clearly demonstrated that the use of a conducting perovskite electrode (such as LSCO) can eliminate polarization fatigue.[3,4,20] Figure 4 shows the test capacitors subjected to polarization fatigue testing via bipolar-pulsed cycles of 5 V at 1 MHz. Fatigue for epitaxial film on LSTO/Si at room temperature (measured with 1 ms and 1 μs pulses) and at 100 °C, when compared to the performance of the same ferroelectric stack processed at 650 °C via conventional sol gel, shows no observable degradation.

In summary, we have demonstrated an epitaxial perovskite template (cation-substituted $SrTiO_3$) approach that has enabled us to create epitaxial LSCO/PZT/LSCO ferroelectric capacitors at a low temperature of 450 °C on silicon substrates. The ferroelectric capacitors exhibit very desirable properties, of particular relevance to nonvolatile memories. The polarization properties of these films, although large enough to be usable in actual memories, are significantly smaller compared to films deposited on STO substrates, presumably as a consequence of the large thermal expansion mismatch between silicon and these perovskites. This mismatch leads to two effects, namely a decrease in the *c*-axis lattice parameter (which is clearly observable by x-ray diffraction) as well as the possible formation of *a*-axis oriented PZT grains, both of which will directly affect the polarization properties. Future work will have to address this rather complicated problem through the use of stress-compensation layers.

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