The piezoresistance of aluminum alloy interconnect structures

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The effects of applied strain on the resistivity of Al thin film metallization interconnects have been measured with a novel methodology that uses thermal expansion mismatch to produce the strain. The interconnect volumetric strain is induced by thermal cycling of passivated and unpassivated interconnects between ≈ 70 and 373 K. The coefficient of piezoresistivity, defined as $d\rho/d\epsilon_v$, where $\rho=$resistivity and $\epsilon_v=$volumetric strain, is determined by properly accounting for the degree of interconnect constraint and thermal expansion mismatch strain induced during temperature changes. The volumetric strains are calculated for unpassivated and passivated lines of varying thickness and width. A model which incorporates the geometrical and piezoresistance effects on the measured interconnect resistance during temperature changes is described. The coefficient of piezoresistivity is calculated by a fitting procedure which provides an accurate and consistent fit for both unpassivated and passivated interconnects of different geometries and different strain states. The measured coefficient $d\rho/d\epsilon_v$ is 2.0×10^{-5} Ω cm in tension, similar to earlier results in bulk Al samples measured in compression but significantly higher than values recently measured in Al interconnects. The application of the calibrated coefficient of piezoresistivity for the measurement of electromigration-induced stresses in novel interconnect test structures will be described. © *1999 American Institute of Physics.* [S0021-8979(99)09803-5]

I. INTRODUCTION

High resolution measurements of metallization interconnect resistance during the early stages of electromigration reliability testing have the potential for characterizing aspects of electromigration-induced processes such as local changes in the vacancy concentration,[1] solute concentration[2,3] void growth,[4] or mechanical stress.[5] In particular the measurement of stresses during electromigration may provide information about the diffusion pathways, electromigration driving forces, and the mechanics of stress development in confined interconnects. Interconnect mechanical stresses may be interpreted from resistance change measurements via the piezoresistance effect, defined as the change of material resistivity due to volumetric strains or equivalently hydrostatic stresses. These measurements require a precise definition of the interconnect volume contributing to the resistance signal, detailed knowledge of the mechanical state of the interconnect volume, and accurate calibration of the coefficient of piezoresistivity for interconnect materials. Unfortunately the interpretation of sensitive resistance measurements is often complicated by several processes such as solute redistribution which occur in the Al alloys at elevated electromigration test temperatures.

Recent measurements of the piezoresistance effect in Al interconnects have provided inconsistent results (summarized in more detail below) possibly due to complicating factors described above. We propose and utilize a novel methodology to measure the coefficient of piezoresistivity, defined as $d\rho/d\epsilon_v$, where $\rho=$resistivity and $\epsilon_v=$volumetric

strain. The method utilizes thermal expansion mismatch to induce interconnect strain during temperature cycling. Careful resistance measurements during the temperature cycling in combination with a model for interconnect thermal expansion mismatch strain allows for the determination of the coefficient of piezoresistivity. The temperatures during cycling are primarily below room temperature in order to prevent complicating contributions to the resistance describe above.

We review previous piezoresistance measurements for Al in bulk and patterned interconnect samples and describe the mechanical model, the thermal cycling experiments, and results which yield the coefficient of piezoresistivity. The ultimate motivation for this work is to aid in the interpretation of the early resistance changes and mechanical stress evolution during electromigration that characterize the kinetics of electromigration-induced processes. Applications for the calibrated coefficient of piezoresistivity in electromigration-induced stress evolution measurements using novel interconnect test structures will be described.

II. BACKGROUND

Extensive experiments to measure the effects of pressure (i.e., negative hydrostatic stress) on the resistance of bulk metals have been performed by Bridgman.[6] Those results for bulk Al samples in compression are $\Delta R/R_0\Delta\sigma=4.2 \times 10^{-2}$ GPa^{-1} and $\Delta R/R_0\Delta\sigma=9.16\times 10^{-2}$ GPa^{-1} at 0 and $-183\,°C$, respectively. More recent work by Sundqvist and Rapp[7] for Al wire under hydrostatic compression yielded $\Delta R/R_0\Delta\sigma=4.25\times 10^{-2}$ GPa^{-1} in the range 20–40 °C. A complicating factor in comparing various piezoresistance ($\Delta R/R_0\Delta\sigma$) measurements is the variation of R_0 with temperature. We note however that the temperature effect on R_0

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does not entirely account for the variation of $(\Delta R/R_0 \Delta \sigma)$ between the 0 and $-183\,°C$ Bridgman data. Further, in order to compare various experimental data, a more fundamental expression of the piezoresistance effect is defined as the coefficient of piezoresistivity $\Delta \rho / \epsilon_v$, where $\Delta \rho$ is the change in material resistivity and ϵ_v is the applied volumetric strain. The Bridgman data may then be expressed (see the Appendix) as $\Delta \rho / \epsilon_v = 1.06 \times 10^{-5}\ \Omega\,cm$ at $0\,°C$ and $\Delta \rho / \epsilon_v = 2.27 \times 10^{-5}\ \Omega\,cm$ at $-183\,°C$.

Beverly, Alers, and Prybala[8] measured the piezoresistance response of passivated Al interconnects on Si substrates between 20 and $200\,°C$, where the strains were applied by bending of the Al interconnect–Si substrate structure. They report a coefficient $(\Delta \rho / \rho_0 \Delta \sigma)$ which increased with temperature, from ≈ 0 at room temperature to a maximum and constant value $(\Delta \rho / \rho_0 \Delta \sigma) = 1.2 \times 10^{-5}\ MPa^{-1}$ at $120\,°C$ and above. This value may be converted to $\Delta \rho / \epsilon_b = 2.7 \times 10^{-6}\ \Omega\,cm$ (see the Appendix), where ϵ_b is the longitudinal bending strain and a nominal value of ρ_0 at $120\,°C$ is used. This value is significantly less than found by Bridgman. It is not clear to what magnitude the applied bending stress includes the hydrostatic stress component, or equivalently to what extent the applied longitudinal bending strain (ϵ_b) includes the volumetric strain (ϵ_v). Again note that in this methodology the unstrained resistivity (ρ_0) increases with temperature which itself produces a temperature dependence on $\Delta \rho / \rho_0 \Delta \sigma$. Other factors such as temperature-dependent metallurgical evolution, voiding, or mechanical yielding may also have complicated the measurements and contributed to the observed $(\Delta \rho / \rho_0 \Delta \sigma)$ coefficient. These careful tests suggest that minimizing the complicating contributions to the total resistance by using pure Al conductors or by low temperature testing may be beneficial in determining the piezoresistance effect in interconnects.

Several attempts to provide a piezoresistance interpretation to electromigration-induced early resistance changes in interconnects have been made. Scorzoni[9] illustrated that possible competing contributions to the measured resistance changes, such as void growth and the corresponding relaxation of hydrostatic (tensile) stresses, prevent simple characterizations of the piezoresistance effect. Alers, Beverly, and Oates[10] made careful resistance measurements on Al via structures during electromigration testing. Their analysis showed that attempted correlations between the detected resistance change and piezoresistivity effects were inconclusive.

Verbruggen[5] and co-workers measured reversible resistance changes during electromigration testing of unpassivated Al lines at $150\,°C$, and attributed these as due to mechanical stress buildup and the piezoresistance effect. Interestingly their simulations of mechanical stress evolution yield a net positive stress when averaged along the entire interconnect. Typical simulations of the stress dipoles which develop during electromigration[11] yield a net zero stress state averaged along the entire line if material is conserved during electromigration-induced diffusive mass flux processes. In this case no net piezoresistance effect would be detected if the total interconnect resistance is monitored, since the resis-

tance increase (due to the local region of tensile stress increase) would cancel the resistance decrease (due to the local compressively stressed region). Thus the Verbruggen piezoresistance interpretation of the measured resistance changes is consistent with but dependent upon their asymmetric stress simulations[5] which show a net induced stress change when averaged along the interconnect. A more precise correlation between resistance and stress evolution requires an accurate characterization of both the sign and magnitude of the actual hydrostatic stresses at well-defined volumes of the interconnect and an accurately determined coefficient of piezoresistivity. We illustrate a methodology to characterize stresses in well-defined interconnect structures during thermal cycling which allows for an accurate determination of the piezoresistance effect.

III. RESISTANCE MODEL

The resistance of a conducting wire undergoing a change in temperature can be described by

$$R(T) = \frac{(L_0 + \Delta L)(\rho_0 + \Delta \rho_{\text{th}} + \Delta \rho_{\text{st}})}{(W_0 + \Delta W)(H_0 + \Delta H)}, \tag{1}$$

where ΔL, ΔW, and ΔH are the changes in interconnect length, width, and thickness due to thermal expansion, respectively, ρ_0 is the initial material resistivity, and $\Delta \rho_{\text{th}} = (d\rho/dT)\Delta T$ is the change in the resistivity due to a temperature change ΔT. The term $\Delta \rho_{\text{st}}$ describes the change in the material resistivity induced by the volumetric strain (ϵ_v) due to interconnect thermal expansion mismatch with the constraining surrounding. Note that the Al temperature dependence of the resistivity ($d\rho/dT = 11.45\ n\Omega\,m/°C$) is independent of composition for Al-dilute solute content alloys.[12] The volumetric strain will depend explicitly on the temperature change and the degree of constraint induced by thermal expansion mismatch between the interconnect and the surrounding material, and is therefore dependent on interconnect geometry. Thus thermal expansion affects the measured resistance in two ways, by the variation of interconnect dimensions with temperature and by the variation of thermal mismatch strain with interconnect geometry.

Both the interconnect dimensions and the applied mismatch strains are determined by the constraint placed on the interconnect by the Si substrate and encapsulating layers and must be properly determined in order to interpret the interconnect resistance during temperature changes, Eq. (1). The mismatch strains in the interconnect length, width, and thickness dimensions can be computed for the various degrees of constraint, encapsulating materials, and interconnect geometry. For example, the linear thermal mismatch strains in wide ($W \gg H$) unpassivated Al lines on Si substrates in the length (ϵ_x) and width (ϵ_y) directions are given by $\epsilon_x = (1 - \nu)(\alpha_{\text{Si}} - \alpha_{\text{Al}})\Delta T \approx \epsilon_y$, where $\nu = $ Poisson's ratio for Al, and where α_{Al} and α_{Si} are the thermal expansion coefficients for Al and Si, respectively. The wide line strain is approximately equibiaxial, $\epsilon_x \approx \epsilon_y$, with the strain in the thickness direction (ϵ_z) given by $\epsilon_z = -2\nu \epsilon_x$, and with relaxation of ϵ_y at the line edge. The applied strains for passivated wide lines are similar but with increased ϵ_y and ϵ_z at the line

TABLE I. Calculated dimensional changes and strain terms as a function of temperature change (ΔT) for various interconnect conditions: narrow passivated, wide unpassivated, and narrow unpassivated. The thermal expansion coefficient for the Al, Si, and SiO$_2$ are $\alpha_{Al} = 24 \times 10^{-6}/°C$, $\alpha_{Si} = 3 \times 10^{-6}/°C$, and $\alpha_{SiO_2} = 1.5 \times 10^{-6}/°C$, respectively. L_0, W_0, and H_0 are the length, width, and thickness dimensions, respectively, of the line at the initial temperature prior to cycling.

	Narrow passivated	Wide unpassivated	Narrow unpassivated
ΔL	$L_0\alpha_{Si}\Delta T$	$L_0\alpha_{Si}\Delta T$	$L_0\alpha_{Si}\Delta T$
ΔW	$W_0\alpha_{Si}\Delta T$	$W_0\alpha_{Si}\Delta T$	$-W_0\nu(\alpha_{Si})\Delta T$ $+ W_0(\alpha_{Al}\Delta T)$
ΔH	$H_0\alpha_{SiO_2}\Delta T$	$-H_0 2\nu(\alpha_{Si})\Delta T$ $+ H_0(\alpha_{Al}\Delta T)$	$-H_0\nu(\alpha_{Si})\Delta T$ $+ H_0(\alpha_{Al}\Delta T)$
ϵ_x	$(\alpha_{Si}-\alpha_{Al})\Delta T$ $-\nu(\alpha_{Si}-\alpha_{Al})\Delta T$ $-\nu(\alpha_{SiO_2}-\alpha_{Al})\Delta T$	$(\alpha_{Si}-\alpha_{Al})\Delta T$ $-\nu(\alpha_{Si}-\alpha_{Al})\Delta T$	$(\alpha_{Si}-\alpha_{Al})\Delta T$
ϵ_y	$(\alpha_{Si}-\alpha_{Al})\Delta T$ $-\nu(\alpha_{Si}-\alpha_{Al})\Delta T$ $-\nu(\alpha_{SiO_2}-\alpha_{Al})\Delta T$	$(\alpha_{Si}-\alpha_{Al})\Delta T$ $-\nu(\alpha_{Si}-\alpha_{Al})\Delta T$	$-\nu(\alpha_{Si}-\alpha_{Al})\Delta T$
ϵ_z	$(\alpha_{SiO_2}-\alpha_{Al})\Delta T$ $-\nu(\alpha_{Si}-\alpha_{Al})\Delta T$ $-\nu(\alpha_{Si}-\alpha_{Al})\Delta T$	$-2\nu(\alpha_{Si}-\alpha_{Al})\Delta T$	$-\nu(\alpha_{Si}-\alpha_{Al})\Delta T$
ϵ_v	20.64×10^{-6} (ΔT)	13.44×10^{-6} (ΔT)	6.72×10^{-6} (ΔT)

edges due to the constraining effect of the passivation there. Narrow unpassivated lines are nearly uniaxially strained in the length direction, $\epsilon_x = (\alpha_{Si} - \alpha_{Al})\Delta T$, with $\epsilon_y \approx \epsilon_z = -\nu\epsilon_x = -\nu(\alpha_{Si} - \alpha_{Al})\Delta T$. Narrow passivated lines are triaxially strained to an extent which is dependent upon the interconnect aspect ratio (W/H). For example in lines with $W/H = 1$ the strains approach $\epsilon_x \approx \epsilon_y \approx \epsilon_z$ especially if plasticity allows for relaxation of shear stresses.[13] Table I summarizes the temperature dependence of interconnect dimensions and strains used in the following calculations. The line averaged volumetric strains calculated for passivated and unpassivated interconnects for several aspect ratios are in excellent agreement with those calculated by finite element methods[14] and with those measured in Al lines.[13,15]

We may now simulate the interconnect resistance as a function of temperature including both dimensional and piezoresistance effects, Eq. (1), for several states of constraint. First consider a "free" Al interconnect, unsupported and unconstrained by any substrate or passivation and which is therefore allowed to freely expand with temperature. For this example the $R(T)$ behavior is computed from Eq. (1) with no piezoresistance effect ($\Delta\rho_{st} = 0$) and with the interconnect dimensions determined solely by α_{Al}. The data are shown in Fig. 1 plotted as the fractional change in resistance from the initial value, $\Delta R/R_0$. Next consider an Al interconnect fully constrained by the Si substrate and encapsulating SiO$_2$ passivation, but again with no piezoresistance effect ($\Delta\rho_{st} = 0$). The $\Delta R/R_0$ behavior in this constrained case is indistinguishable from the free interconnect resistance during thermal cycling, indicating that the constraining effect (with no piezoresistance effect) on interconnect resistance is negligible, Fig. 1. Finally, again consider the fully constrained interconnect with a coefficient of piezoresistivity[6] $\Delta\rho/\epsilon_v = 2.27 \times 10^{-5}$ Ω cm at $-183°C$. The simulated $\Delta R/R_0$ behavior in this case clearly illustrates the piezoresistance effect, Fig. 1. Thus Eq. (1) combined with a detailed simula-

tion of interconnect dimensions and mismatch strains may be used to deduce the piezoresistance effect and coefficient of piezoresistivity in interconnects during temperature cycling. We describe the resistance measurements during low temperature thermal cycling and the analysis used to measure the piezoresistance effect in unpassivated and passivated Al interconnects.

IV. EXPERIMENT

Single level and multiple level Al alloy interconnect structures were fabricated for resistance monitoring during temperature cycling between ≈ 70 and 373 K. The single level patterns were patterned from 0.4-μm-thick Al-0.5% Cu-1% Si films which were deposited in a low base pressure load-locked multichamber sputter deposition system onto oxidized Si (100) 150 mm diam substrates. Single level four-terminal test structures were defined using standard plasma etching methods to produce 4 μm wide and 2500 μm long
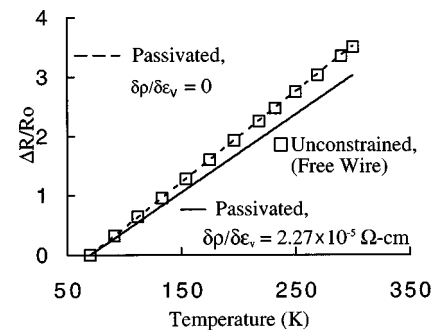

FIG. 1. Simulated resistance change data ($\Delta R/R_0$) for three conditions of interconnect constraint; unconstrained "free wire" interconnect, fully constrained passivated interconnect without piezoresistance effect ($d\rho/d\epsilon_v = 0$), and fully constrained passivated interconnect with piezoresistance ($d\rho/d\epsilon_v = 2.27 \times 10^{-5}$ Ω cm).

TABLE II. Dimensions and fractional resistance change as a function of temperature ($\Delta R/R_0\Delta T$) for the single and multiple level interconnect structures.

	Multiple level structure	Single level structure	
	Passivated	Passivated	Unpassivated
L (μm)	800	2500	2500
W (μm)	0.8	4	4
H (μm)	0.4	0.4	0.4
$\Delta R/R_0\Delta T$	1.08×10^{-2}/°C	6.38×10^{-2}/°C	6.66×10^{-2}/°C

FIG. 2. Measured resistance behavior for the narrow passivated multilevel interconnect as a function of temperature between $\approx$70 and 300 K.

interconnects terminated by large pads. Several wafers were passivated with 2-μm-thick chemical-vapor deposited SiO$_2$ layers at approximately 400 °C, with pad openings subsequently defined and etched to allow for wire bonding. Both passivated and unpassivated structures were annealed, diced and placed in 24 pin ceramic packages.

The multiple level test structures consisted of multilayered Ti/Al-1% Cu/TiN-(top) metallizations deposited onto Si(100) oriented 150 mm substrates covered with deposited dielectric layers, with the Al layer thickness approximately 0.8 μm. The sputter depositions were done in an identical system as used for the single level structures, with the interconnect patterning processes also identical to those described above. The test structure consisted of discrete lower-level interconnect segments connected to the upper metallization levels by W-filled via plugs. The tested structures were passivated by 0.6-μm-thick plasma-enhanced chemical-vapor deposited SiO$_2$ similarly deposited at 400 °C and subsequently received full processing. Die containing the test structures were placed into 24 pin ceramic packages for electrical testing. The dimensions of both the single level and multiple level structures are summarized in Table II.

Thermal cycling experiments on the single level structures were conducted between 175 and 375 K in a liquid N$_2$ and He cooled cryostat[16] which was heated (when necessary) by a resistance heater embedded in the package holder. Careful resistance measurements were made on heating from the minimum temperature since the temperature ramp, stability, and control were optimum during heating rather than during cooling. These measurements were made as part of an earlier experimental program[16] but have not been previously reported.

The packaged multiple level structures were mounted on a cantilevered holder containing an embedded Joule–Thompson refrigerator manufactured by MMR Technologies, Santa Clara, CA. The cooling is achieved by expansion of compressed N$_2$ in small expansion channels within the substrate holder and is assisted by a vacuum pump on the exhaust side of the cooling chamber. The temperature is accurately controlled (to $\pm$0.1 °C) by active control of current supplied to a resistance heating element embedded in the holder. The entire sample and refrigerator-holder system are enclosed in an evacuated chamber to minimize convective heat transfer from the ambient chamber walls to the device under test. Temperature control and the function of the monitoring electronics are actively controlled via custom 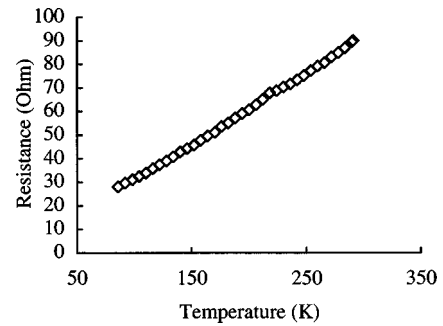instrumentation software running on a computer within the National Instruments Labview programming environment. Four-terminal resistance measurements were taken as the temperature increased from the minimum temperature, $\approx$70 K for this system, since as before temperature stability and control are optimized during heating rather than during cooling.

The $\Delta R/R_0$ behavior is calculated from the form of Eq. (1) appropriate for each sample geometry and constraint. For the wide single level structures a nearly equibiaxial strain state is assumed for the unpassivated single level line, since $W/H\approx10$, and for which a slight relaxation in ϵ_y is assumed. A triaxial mismatch strain state is assumed for the wide passivated single level line, with relaxation assumed in the thickness direction again due to the wide line geometry ($W/H\approx10$) as discussed earlier. The coefficient of piezoresistivity ($d\rho/d\epsilon_v$) is found by a fitting procedure which provides an accurate and consistent individual fit to Eq. (1) appropriate to both the unpassivated and passivated resistance data.

Similarly, the resistance of the multiple level structures is also computed by Eq. (1) using the mismatch strains (Table I) appropriate for narrow passivated lines. As before the coefficient of piezoresistivity is found by finding the value of which accurately reproduces the measured $R(T)$ behavior.

V. RESULTS

The $R(T)$ data for the narrow passivated multiple level line between $\approx$70 and 300 K are shown in Fig. 2. The simulated $\Delta R/R_0$ behavior for this interconnect under two conditions of constraint and the measured $\Delta R/R_0$ data are illustrated in Fig. 3, where R_0 is the resistance at the lowest temperature of the cycle. In the first condition we calculate the resistance of the multiple level interconnect which is fully constrained by passivation but with no piezoresistance effect. In the second condition the interconnect is similarly constrained but the calculation includes the piezoresistance effect. As shown in Fig. 3 the observed $\Delta R/R_0$ is accurately simulated using a coefficient of piezoresistivity $d\rho/d\epsilon_v$ $=2.0\times10^{-5}$ Ω cm, similar to that found by Bridgman for bulk Al in compression.

The $R(T)$ data for the wide single level unpassivated and passivated structures between 175 and 375 K are shown in Fig. 4. We note the difference in the resistance behavior may
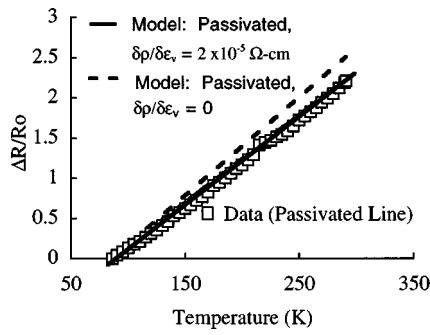
FIG. 3. Measured $\Delta R/R_0$ data for the narrow passivated multilevel interconnect, and simulated $\Delta R/R_0$ behavior for the narrow passivated interconnects with $(d\rho/d\epsilon_v = 2.0 \times 10^{-5}$ Ω cm) and without $(d\rho/d\epsilon_v = 0)$ the piezoresistance effect.

FIG. 5. Simulated and measured $\Delta R/R_0$ behavior for both passivated and unpassivated single level interconnects, illustrating the consistent fit using a coefficient of piezoresistivity $d\rho/d\epsilon_v = 2.0 \times 10^{-5}$ Ω cm.

be in part due to variations in line cross section for these interconnects, however initial width and thickness effects are accounted for in the simulation and $\Delta R/R_0$ calculations. The resistance simulations of these samples are shown in Fig. 5 along with the measured $\Delta R/R_0$ data. Note that the measured data are accurately reproduced by Eq. (1) when using the same coefficient of piezoresistivity $(d\rho/d\epsilon_v = 2.0 \times 10^{-5}$ Ω cm) as used for the multiple level structures. For illustration, we also include in Fig. 5 the simulation of the wide passivated line $\Delta R/R_0$ behavior under the assumption of $d\rho/d\epsilon_v = 0$, and demonstrate that a finite piezoresistance effect is required in order to adequately describe the observed behavior.

We have shown (Figs. 3 and 5) that the coefficient value $d\rho/d\epsilon_v = 2.0 \times 10^{-5}$ Ω cm consistently describes the piezoresistance effect in Al-based interconnects with different geometry and thermal mismatch-induced volumetric strains, and conclude that this value of the coefficient of piezoresistivity is appropriate for Al-based interconnects under these conditions.

VI. DISCUSSION

The coefficient of piezoresistivity measured here $(d\rho/d\epsilon_v = 2.0 \times 10^{-5}$ Ω cm) is consistent with the range of values previously determined by Bridgman[6] for bulk Al in a similar temperature range. However our results do not indicate a temperature dependent coefficient as found in that ear-
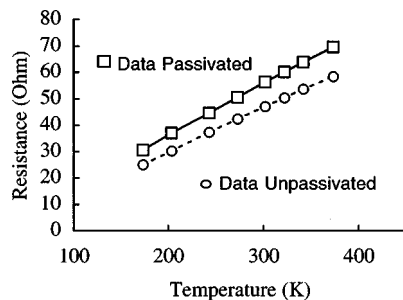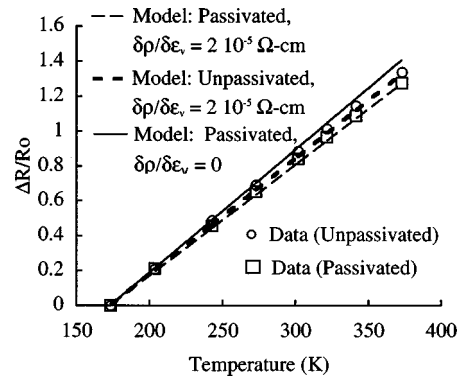

FIG. 4. Measured resistance behavior for the wide single level unpassivated and passivated interconnects as a function of temperature between 175 and 375 K.

lier work. It is possible that the thermal cycling methodology yields a coefficient which is averaged over the range temperatures measured.

It is interesting that the previous piezoresistance characterization[8] of thin film metallization interconnects yielded a significantly lower coefficient $d\rho/d\epsilon_v$ (by a factor of ≈ 7) as calculated from their $(d\rho/\rho_0 d\sigma)$ data. A likely source of this discrepancy is the difference between the computed linear bending strains (ϵ_b) and the actual volumetric strains (ϵ_v) applied during the bending. Further comparisons between these data require knowledge of the temperature dependence of the (unstrained) reference resistance (R_0) or resistivity (ρ_0) used in that earlier work.

The validity of the methodology for piezoresistance characterization illustrated here depends critically on the following factors. We assume that the constraining effects of the passivation and substrate are well described by the thermal expansion mismatch simulations. Close correlation between the simulated stresses and those calculated by finite element modeling[14] and measured by x-ray methods[13,15] support our thermal expansion mismatch strain simulations. We further assume that the interconnect provides an elastic mechanical response to the applied (hydrostatic component of) stresses during temperature cycling. That is, we assume that no void growth or shrinkage occurs during the thermal cycling. This assumption is supported by the (primarily) low temperatures used during the thermal cycling, such that void growth or shrinkage by diffusional processes is eliminated during the time scales used in these experiments. Finally, we assume that the temperature response of the Al resistivity is described by the constant factor $d\rho/dT$, which has previously been validated.[12]

The correspondence between the coefficients of resistivity measured in bulk and thin film interconnect materials suggests that the factor $(d\rho/d\epsilon_v)$ describes the fundamental piezoresistance response in Al, and may be used to characterize the kinetics of electromigration-induced stress evolution in confined interconnects. However it is critical in these applications that the measured resistance changes come from well-defined sections of the electromigration test structure.[17] For example in multiply probed interconnect segments[17] the actual electromigration-induced tensile-compressive stress

dipole may be measured by piezoresistance interpretation of the detected resistance shifts measured along individual segments of the interconnect. Future work will explore such mechanical stress characterizations of electromigration-induced processes.

VII. CONCLUSIONS

A novel methodology to measure the effect of mechanical stress on the resistivity of Al interconnects has been evaluated. Precise resistance measurements of Al alloy interconnects during thermal cycling primarily below room temperature, combined with an explicit description of thermal mismatch-induced volumetric strains, allowed the determination of the coefficient of piezoresistivity for Al-based interconnects. The result $(d\rho/d\epsilon_v = 2.0 \times 10^{-5} \ \Omega \ \text{cm})$ consistently describes the piezoresistance effect in Al interconnects of various geometry and thermal expansion mismatch strain, and is in close agreement with earlier results determined in bulk Al materials.

ACKNOWLEDGMENTS

APPENDIX

Typical measurements of the piezoresistance effect result in data of the form $(\Delta R/R_0 \Delta \sigma_H)$, where ΔR is the change in resistance from the original (R_0) for an applied hydrostatic stress $(\Delta \sigma_H)$. However the fundamental expression of the piezoresistance effect is the change in resistivity $(\Delta \rho)$ due to applied volumetric strains $(\Delta \epsilon_v)$, defined as the coefficient of piezoresistivity, $\Delta \rho/\epsilon_v$. This coefficient may be deduced from the various measured data as follows.

Consider the change in measured resistance due to applied strains in a sample with original dimensions L_0, W_0, and H_0 (length, width, and thickness, respectively). The fractional resistance change is due to contributions from both geometry (as the sample deforms) and piezoresistivity,

$$\delta R/R_0 = [(\rho L/WH) - (\rho_0 L_0/W_0 H_0)]/(\rho_0 L_0/W_0 H_0). \tag{A1}$$

However the change in sample dimensions with applied linear strain (ϵ_l) varies as $L = L_0(1 + \epsilon_l)$, etc. Thus under equitriaxial straining (as due to an applied hydrostatic stress) Eq. (A1) may be reduced to

$$\delta R/R_0 = [\rho - \rho_0(1+\epsilon_l)]/\rho_0(1+\epsilon_l) \approx (\delta \rho/\rho_0) - \epsilon_l. \tag{A2}$$

The approximation is valid for small strains, and note that the significance of the term ϵ_l in Eq. (A2) varies inversely on the magnitude of δR or $\delta \rho$. For the small values of δR typically measured the term ϵ_l provides a reasonably significant correction to the measurements. The resistance change due to applied hydrostatic stress $(\delta \sigma_H)$ is

$$\delta R/R_0 \delta \sigma_H = (\delta \rho/\rho_0 \delta \sigma_H) - \epsilon_l/\delta \sigma_H$$

$$= (\delta \rho/\rho_0 \delta \sigma_H) - \frac{1}{3B}, \tag{A3}$$

where we have used Hooke's Law $(\sigma_H = B\epsilon_v = 3B\epsilon_l)$ and B=bulk modulus. The coefficient of piezoresistivity may then be calculated by

$$\delta \rho/\epsilon_v = B\rho_0 \left[\delta R/R_0 \delta \sigma_H + \frac{1}{3B} \right]. \tag{A4}$$

Values of $\delta \rho/\epsilon_v$ calculated from Bridgman's $\delta R/R_0 \delta \sigma_H$ data for bulk Al in compression yield $\Delta \rho/\epsilon_v = 1.06 \times 10^{-5} \ \Omega \ \text{cm}$ at $\approx 0 \ °\text{C}$ between 0 and 0.7 GPa. At $-183 \ °\text{C}$ Bridgman's data give $\Delta \rho/\epsilon_v = 2.27 \times 10^{-5} \ \Omega \ \text{cm}$ in a similar pressure range. More recent data[7] for narrow Al wire in compression confirm $\Delta \rho/\epsilon_v = 1.06 \times 10^{-5} \ \Omega \ \text{cm}$ in the temperature range 20–40 °C and between 0.2 and 1.0 GPa.

The Beverly[8] result for thin film Al interconnects $(\Delta \rho/\rho_0 \Delta \sigma = 1.2 \times 10^{-5} \ \text{MPa}^{-1})$ measured at 120 °C may be converted to $\Delta \rho/\epsilon_b = 2.7 \times 10^{-6} \ \Omega \ \text{cm}$, using $B=75$ GPa and $\rho_0 = 3 \times 10^{-6} \ \Omega \ \text{cm}$. The discrepancy between this result and the bulk data may be due in part to the difference between the measured linear bending strain (ϵ_b) and the actual volumetric strain (ϵ_v) which produces the piezoresistance.

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