Low-Level Linear Microsecond Gate*

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A linear transmission gate for use in scintillation counter coincidence experiments is described. The gate is suitable for negative pulses of microsecond duration and is linear over a range of 0.01 to 5 v. The circuit is relatively simple, uses no vacuum tubes, and is reliable over long periods of use. The use of low-level gates can increase the usable counting rate of a multichannel coincidence system by an order of magnitude.

INTRODUCTION

ONE of the principal limitations encountered in conventional "fast-slow" coincidence systems[1] in nuclear spectroscopy is that each "slow" or linear part of a system must be able to operate at the full counting rate of the individual detector to which it is connected. This is especially the case when the coincidence rate is a very small fraction of the singles rates, as in multiple coincidence systems, where the usable source strength may be limited not by chance coincidence considerations but by counting rate limitations of the linear amplifiers or pulse-height analyzers. It has already been pointed out[2] that this difficulty may be eliminated by the use of a low-level linear gate at the output of each detector so that the "slow" circuits need to operate only on pulses corresponding to "fast" coincidence signals. Unfortunately low-level gate circuits used in this application are often subject to drift or require frequent adjustment. As counters and multichannel analyzers of continually improved resolution come into use, the need for a stable and relatively trouble-free gate circuit makes itself felt. The circuit to be described, which is based on the six-diode gate of Millman and Puckett,[3] is simple to construct of readily available components and has proved to require no attention over long periods of operation.

GATE UNIT

In Fig. 1, diodes D_2 through D_7 constitute the basic six-diode gate. The operation of the gate is explained in detail by Millman and Taub[4]; suffice it to say here that in the absence of a trigger pulse, points A and B are held at $-V_0$ and $+V_0$, respectively, so that D_4 and D_7 conduct, cutting off the remaining diodes. The gate is opened by pulsing point A to $+V_0$ and B to $-V_0$, cutting off D_4 and D_7, and allowing D_2, D_3, D_5, and D_6 to conduct through R_9 and R_{10}. The input signal then passes through the gate via parallel paths through D_2 and D_3, and D_5 and D_6. Resistors R_5 through R_8 help to equalize the forward diode currents but have a negligible effect on the operation of the circuit.

At the input, R_1 and R_2 are used to terminate the delay line carrying the input signal. Common-collector stage Q_1 provides a low source impedance for the gate, which helps to reduce pickup of the trigger pulses. D_1 is a dc restorer and may be omitted for low input duty cycles. Common-collector stage Q_2 is needed to provide a high load impedance to the six-diode gate. The minimum load on Q_2 is set by R_{12}, making the input impedance of Q_2 about 15 k. This allows the gate to pass signal pulses as large as $V_0/2$ or more. The output will satisfactorily drive loads of the order of 1 k through interconnecting cables several feet long without observable attenuation due to cable capacitance. The over-all gain is close to unity, except for attenuation by the voltage divider formed of R_{12} and the external load resistance. The rise time, determined by Q_1 and Q_2, is about 0.15 μsec, depending somewhat on the source and load impedances.

Although no pedestal is produced by the six-diode gate itself, one occurs in this application. When the gate is closed, the base current of Q_2 flows to ground through D_8, so that the base has a slight positive voltage with respect to ground. When the gate is opened, this point becomes connected to R_4 and its potential drops very nearly to zero, producing a negative pedestal at the output. Because this pedestal is small and constant, it is not felt to be objectionable. Reverse currents through the cutoff gate diodes D_3 and D_6 may also contribute to the pedestal.

If the instantaneous voltages of points A and B do not pass through zero simultaneously, transient "spikes" may occur at the beginning and end of the gate period. These can also be produced by capacitive pickup of the trigger pulses. To some extent, varying the relative values of $+V_0$ and $-V_0$, and dressing the interconnecting leads, will allow cancellation of these spurious signals. In any event these cause little difficulty since they are very short and so are lost during subsequent amplification.

The six-diode gate itself passes pulses of either polarity equally well; however, the present circuit is intended for

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[1] Several surveys of coincidence systems are to be found in the literature, e.g., E. Fünfer and H. Neuert, *Zählrohre und Szintillationszähler* (G. Braun, Karlsruhe, 1959), Part IIIE, pp. 10–12 and S. De Benedetti and R. W. Findley, *Handbuch der Physik* (Springer-Verlag, Berlin, 1958), Vol. 45, p. 222.

[2] P. R. Chagnon, Rev. Sci. Instr. 24, 990 (1953).

[3] J. Millman and T. H. Puckett, Proc. IRE 43, 27 (1955).

[4] J. Millman and H. Taub, *Pulse and Digital Circuits* (McGraw-Hill Book Company, Inc., New York, 1956), Chap. 14.

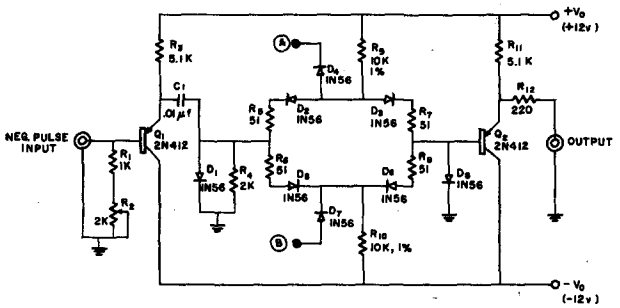

FIG. 1. Circuit diagram of the gate unit.

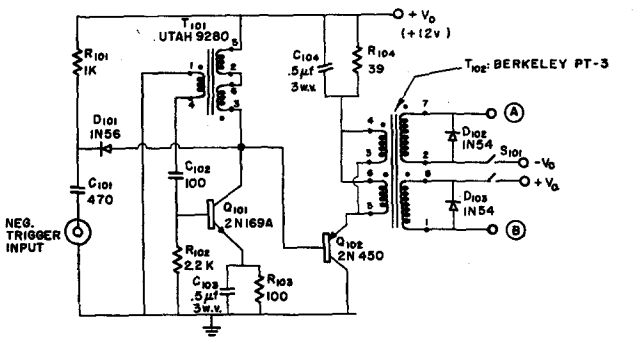

FIG. 2. Circuit diagram of the trigger unit.

use with negative photomultiplier pulses. If it is desired to adapt it to positive signals, D_1 and D_8 should be reversed, and Q_1 and Q_2 replaced by npn types, with appropriate changes in power supply polarity.

In order to realize the full advantages of low-level gating, the input pulses should be clipped to somewhat less than the gate length, and delayed so that the entire signal pulse falls within the gate. Even if this is not done, the gate unit itself will shorten the signals by passing the instantaneous input voltage during the time it is open, i.e., for the length of the trigger pulse. In this case there is a risk of pileup of the input pulses before they are gated.

If the preamplifier is designed to limit the signals to some value less than V_0, no feedthrough of oversize pulses can occur.

TRIGGER UNIT

Millman and Taub[4] discuss the optimum values of dc and pulse voltages to be applied to points A and B for a given input pulse amplitude. In this application it was felt desirable to depart from these values and bias the "off" diodes to the full power supply voltage in order to assure rejection of oversize pulses and to simplify the design. The requirements placed upon the trigger circuit are then that points A and B should be held at $\mp V_0$ when the gate is closed, with pulses of $\pm 2V_0$ superimposed when the gate is to be open. For use with NaI(Tl) signals, the gate duration should be about 1 μsec and the A and B pulses must be simultaneous. These requirements are conveniently met by the trigger unit of Fig. 2. When a negative trigger is applied, blocking oscillator Q_{101} generates a pulse whose amplitude is very nearly $-V_0$ and whose duration is approximately 1.4 μsec with rise and fall times of 0.2 μsec. Thus the gate opens for 1.2 μsec and is fully open for 1.0 μsec. Q_{102} is a common-collector stage driving T_{102}, which has turns ratios 1:1:2:2. Thus the required output signals are generated at A and B.

T_{101} may be any 1:1:1 pulse transformer which gives a suitable pulse length. C_{102} also influences the pulse length and may be varied to provide a fine adjustment. The blocking oscillator may be triggered by any of the conventional means; with the triggering method shown, a reasonably fast negative pulse of a few volts amplitude is required. Excessively large input pulses will distort the blocking-oscillator waveform and result in increased spurious output at the gate. S_{101} is normally closed; when gate action is not desired, it may be opened, and the gate unit is then open to all incoming pulses.

R_{103} and R_{104} are included to provide a degree of protection against thermal runaway at high repetition rates. It is difficult to estimate the transistor dissipations under pulse conditions. In practice the trigger units have been operated in excess of 25 000 pps without any indication of instability.

One trigger unit may be used to operate several gate units.

POWER SUPPLY

Two power supply voltages of equal magnitude and opposite polarity, indicated as $\pm V_0$, are required. This value has been made 12 v in the units constructed, although they operate satisfactorily with values as low as 0.5 v with considerable loss of rise time accompanied by reduction in the pedestal and "spike" amplitudes. At 12 v, each gate unit requires 5 ma and each trigger unit requires (from one power supply only) about 2 ma for each 1000 pps repetition rate. Simple full-wave supplies, shunt-regulated by Zener diodes, have been found to be very satisfactory.

PERFORMANCE

Four gate units operated by two trigger units have been in continuous operation for more than a year. These are mounted in a metal box installed in a relay rack among several vacuum tube circuits. They are subject to ordinary diurnal and seasonal temperature variations of several degrees C as well as to variations due to changes in adjacent equipment. Input signals are NaI(Tl) scintillation counter pulses clipped to 0.75 μsec length and delayed so as to be centered within the gate interval. Input pulse amplitudes range from 0.01 to 5 v.

Two of the gate units feed single-channel analyzers; the other two alternately feed a commercial 256-channel analyzer, and it is mainly on the performance of these two that the following remarks are based.

Maintenance. One diode in one gate unit suffered an unexplained decrease in back resistance after about six months, and had to be replaced. No other maintenance or adjustment has been required.

Linearity. No deviation from linearity has been observed beyond the limits of the pulse-height analyzer (approximately 1%).

Gain drift. No change in gain attributable to the gate circuits has been observed. The sensitivity for this measurement is about 0.5%.

Pedestal. The pedestal amplitudes of the four gates are -0.05 to -0.1 v. Slow variations within this range occur over periods of several weeks. These do not appear to be correlated with temperature or line voltage variations. The pedestal is usually offset by adjusting the zero level of the analyzer. When the analyzer is set to take in a 5-v input range, pedestal drifts amount to ± 1 channel/week, which is indistinguishable from the zero-level drift of the analyzer itself.

Transients. After suitable dressing of interconnecting leads, transient "spikes" of about 0.05 v amplitude, 0.05 μsec duration, and either polarity are observed at the gate output at the beginning and end of the gate period. These are almost invisible at the linear amplifier output and at worst only contribute an additive constant, as does the pedestal.

Feedthrough. No capacitive feedthrough of input pulses has been observed. No feedthrough of oversize pulses has been observed with input pulses of 7 v, at which level the preamplifiers limit.

Resolution. With a 3-crystal pair spectrometer having all channels gated, an over-all system resolution of 2.5% at 5 Mev is consistently attained for singles rates in excess of 10^5 pps. Before the gates were installed, and when the pulse-height analyzer was gated via its coincidence input, the system resolution began to deteriorate with singles rates of 10^4 pps. This was accompanied by a loss of efficiency in the side channels due to counting losses in the single-channel analyzers.

ACKNOWLEDGMENT

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