ENGINEERING RESEARCH INSTITUTE
THE UNIVERSITY OF MICHIGAN
ANN ARBOR

Final Report

COMPUTER COMPONENTS DEVELOPMENT

Compiled and Edited by: D. C. Ray
Project Supervisor: H. L. Garner

Project 2452

NATIONAL SECURITY AGENCY
SIGNAL CORPS PROCUREMENT OFFICE
CONTRACT NO. DA-49-170-sc-1791
WASHINGTON, D.C.

September 1957

The present report has been compiled and edited by D. C. Ray from Report No. 2452-1-P by H. L. Garner, K. R. Monroe, and R. A. Carlsen; Report No. 2452-2-P by R. T. Denton, W. P. Brown, and W. K. Kilmer; Report No. 2452-3-P by R. A. Carlsen, D. C. Ray, and H. L. Garner; and Report No. 2452-4-P by K. R. Monroe and H. L. Garner. Authors of the present report also include H. Ruston and C. Wickman.

TABLE OF CONTENTS

TABLE OF CONTENTS (Concluded)

LIST OF ILLUSTRATIONS

ABSTRACT

The objective of the program was the development of a basic set of switching elements which could be used to fabricate certain logical configurations. It was also desired that the basic limitations of the component parts of the circuitry be determined and clarified. A natural breakdown of the problem led to research into four distinct regions of existing component development.

In Chapter 1, an analysis is made of a pulse amplifier of the type employed in the SEAC computer gating package. There are two ways of investigating the performance of a given circuit. The first of these is a theoretical analysis of the circuit, and the second is experimentation. The theoretical work, unless grossly inapt assumptions are made, will give the investigator at least an order-of-magnitude feeling for values of circuit parameters and frequencies of operation. In this chapter, linear circuit analysis and a graphical method of analysis are used, and the results are compared with experimental results. Agreement between the theoretical and experimental results is reasonable on the basis of the assumptions made.

In Chapter 2, the gating circuitry is studied, and it is found that the speed of operation of a diode gating structure is limited by 1) the amount of noise which can be tolerated in the circuit, and 2) the magnitude of current required per gate input. Both of these limiting factors are dependent on the reverse transient properties of the semiconductor diodes used in the gate structure. As the frequency of operation is increased, the reverse transient is accentuated by the required increase in gate current. This chapter is a study of the effect of various diode parameters on over-all gate performance.

Chapter 3 presents design information for a pulse transformer applicable to the pulse amplifier circuitry and an analysis of the frequency limitations and circuit characteristics of the transformer independent of its circuit environment.

The first section is an investigation of the effects of tube, transformer, and external circuit parameters on the output characteristics of tube-transformer pulse amplifiers. A simplified low-frequency equivalent circuit for the transformer is assumed in this section. Equations are derived which relate the maximum available load current to the circuit parameters, and it is shown that a resonant transformer design will allow maximum load current.

The second section is a study of the limitations on circuit operation imposed entirely by the transformer characteristics. The effects of core material, core size and shape, and winding geometry on transformer characteristics are indicated, and some measurements of these effects are presented.

In Chapter 4, two possible configurations for interconnection between a package output and gate inputs are considered. The first one employs n cables,

each terminated at the gate input. It is found that this interconnection necessitated equality between the gate impedance and the characteristic impedance of the cable if no power loss is to be permitted. The second configuration consisted of a singly terminated cable with each gate input tapped off at n different points of the cable. This interconnection requires that the gate impedance be much larger than the characteristic of the cable to minimize reflections. This type of interconnection is more desirable and experimental data prove this out.

The operation of delaying pulse trains for proper time phasing at the gate inputs is also considered in Chapter 4. It was found that a delay network manufactured by Advance Electronics Laboratories (8-T-300a) would operate satisfactorily at the desired frequency.

In Chapter 5, the research on gating circuitry, pulse amplifiers, transformers, and interconnection are utilized in the design of a standard package. A modified form of the standard package is then used in fabricating a T_4 pulse generator and a minor cycle counter. Experimental results show that the components will allow 5 Mc operation and possibly higher. It should be emphasized that throughout the different phases of research work for this project, rectangular pulses were assumed and employed whenever possible. With less stringent requirements on the pulse wave shape, it is feasible that higher speeds of operation could be realized.

OBJECTIVE

The object of this program has been the engineering development of a basic set of switching elements. It was desired that the circuitry developed be capable of operating at switching rates an order of magnitude greater than rates presently employed in conventional digital switching circuits. This implies that the circuitry must operate effectively at a switch rate of $\sim$10 Mc/sec. Another objective of the program has been the determination and clarification of basic limitations of the component parts of the circuitry.

DESIGN PHILOSOPHY

It is almost impossible to design high-speed switching circuitry on a hit-or-miss basis. This is due primarily to the inadequacies or limitations of the basic elements. None of the basic elements--diodes, tubes, transformers, etc.--is perfect. The successful circuit design must function correctly in spite of these basic difficulties. The task of the circuit designer is the optimization of the circuit design so that the best possible performance is obtained. In other words, the designer must be acutely aware of the limitations of the basic component, and the design must account for these limitations.

Component limitations are the primary factors governing the specification of the basic design philosophy. Let us then begin the discussion of design philosophy with a short explanation of the component limitations.

Perhaps the worst limitation arises from the capacitance associated with the basic components. All components such as tubes and diodes have shunt capacitance between elements. There also exists additional capacitance in the form of stray capacitance due to wiring. To produce a voltage pulse at a given point, it is necessary first to charge the capacitance at that point. An examination of a typical dynamic circuit configuration would reveal that capacitance is charged from three components, diode gates, tubes, or transformers. The gates and the tubes will approximate constant current generators, while the output from the transformers approximates a constant voltage generator. With a constant current generator the effect of capacitance is obtained from the following equations:

$$e = 1/C \int_0^t i \, dt$$

$$\text{if} \quad i = 0, \; t < 0$$

$$i = I, \; t \geq 0$$

then

$$\Delta e = I/C \, \Delta t \quad .$$

The ratio of $\Delta e/\Delta t$ is determined by the ratio of I/C.

As a base, consider the standard one megacycle dynamic circuitry used in the SEAC, MIDAC, and various other computers. The goal is to increase the operation speed of this basic circuit by at least a factor of ten. Can the ca-

pacitance at the various critical points be decreased by a factor of ten? The answer is obviously no. It is apparent that the capacitance which presently exists cannot be substantially reduced. Some small reduction of capacitance is obtainable if more direct wiring is employed. However, this reduction may be nullified if the tube selected for the power amplifier has greater interelectrode capacitances than the 6AN5.

Next let us consider the effects obtained if the circuit action is speeded up by increasing the available charging current I. If perfect diodes were available, this would be a feasible solution, except from the viewpoint of power dissipation. However, presently available diodes suffer undesirable transient effects during the switching interval. In particular, the transient recovery of diodes from conduction to nonconduction must be given serious study. The diode does not recover instantly, due to the existence of the minority carriers in the diode at the time of switching. The diode is not switched until these carriers have diffused out of the active diode region. The number of carriers found in the diode at the time of switching is proportional to the magnitude of the forward current. Thus, for any given diode the fastest recovery time is obtained with the minimum forward current. The recovery time will roughly increase in proportion to an increase in forward current. Preliminary studies have indicated that back recovery effects are not as serious as might first be expected. Even so, it is still important to obtain fast recovery times. This means that only small increases in charging current can be obtained. The increase in charging current will never approach an order of magnitude.

One consideration remains. If the voltage Δe is reduced, a faster operation can be achieved. This means that a gate designed to give a 10-v pulse at 1 Mc/sec should function adequately at 10 Mc if the voltage swing is reduced to 1 v. This is the desired low-current gate. The reduction of the gate-voltage swing must be accompanied by a proportional increase in the g_m of the power amplifier tube. In the MIDAC 1 Mc/sec circuits the 6AN5 tube has an effective g_m of about 7000 μmhos. A MIDAC gate structure operating at 10 Mc/sec requires a pentode-type tube with a g_m of 70,000 μmhos. It is possible with existing tubes to achieve a g_m of 50,000 μmhos.

Let us now examine in somewhat more detail the effects of g_m and gate-voltage changes on the performance of a dynamic switching circuit.

A transformer of optimum design will deliver a secondary current of magnitude

$$I_s = \frac{I_p^2 T}{4E_o C_p} \qquad I_g N = I_s$$

where

I_p is the primary current,

C_p is the capacitance seen at the primary,

E_o is the magnitude of the pulse from the secondary,

T is the rise time desired,

I_g is the current required for one gate drive, and

N is the maximum permissible number of gate drives.

Now

$$I_p = g_m E_g ,$$

where E_g is the grid swing.

The loss occurring in the gating can be accounted for by setting

$$E_g = A E_o \qquad A < 1$$

E_g may also be expressed in terms of current and capacitance:

$$E_g = \frac{B I_g T}{C_g} ,$$

where

C_g is the capacitance seen by the output of the gating circuit, and

B is the efficiency of the gating configuration.

Combining the previous formulae yields

$$N = \frac{g_m^2 T^2 AB}{4 C_p C_g}$$

or

$$N = \frac{M^2 T^2 E}{4} ,$$

where

$M = \frac{g_m}{\sqrt{C_p C_g}}$, a figure of merit, (see Appendix A) and

E = AB, the gate efficiency defined as the product of the gate-structure current and voltage-transfer ratios.

For the purpose of illustration assume

$$T = 10^{-8} \text{ sec},$$

$$E = 1/25, \text{ and}$$

$$M = 5 \times 10^{9} \text{ rad/sec}.$$

For the above values N = 25. It is noted that a rather inefficient gate structure was assumed. Also, the formula does not account for transformer losses which certainly are not negligible at 10 Mc/sec. In spite of various losses which have been neglected, the above calculation is important. It indicates that 10-Mc dynamic circuitry, which will provide an adequate number of gate drives, can be achieved.

Little has been said about the transformer design. The ultimate efficiency of a transformer at high frequencies is primarily dependent on the core material. To be sure, different methods of construction produce better transformers, but at high frequencies the core material remains the dominant factor. The choice of a core material must be a compromise between permeability and core losses.

In brief, the design philosophy adopted seeks to minimize the gating currents and the gate-voltage swing. The power-amplifier design effort is directed toward a circuit having a very high g_m and an excellent figure of merit.

1. PULSE AMPLIFIER

1.1 Theoretical Analysis of Pulse Amplifiers

1.1.1 QUALITATIVE DISCUSSION OF A PENTODE, TETRODE, OR CASCODE TRIODE PULSE AMPLIFIER

If the amplifying component is a vacuum tube, then a pulse transformer is required to match the tube to the lower impedance of the gating structure. The tube and transformer then comprise a pulse amplifier. Operation of such a pulse amplifier is best understood by consideration of three different phases of the pulse: the rise, the flat top or duration, and the fall or decay.

1.1.1.1 The Rise.—Initially the pulse amplifier has on its grid a voltage e_{g_1}, which keeps the tube in a low-conduction state. The plate voltage is the supply voltage since there is negligible d-c drop in the transformer. This quiescent point corresponds to point A of Fig. 1.1. When a pulse is applied by the gating structure, the grid is suddenly raised to the positive value e_{g_2}. Since there is plate-circuit shunt capacitance, the plate voltage cannot change instantly; hence, the plate characteristics are traversed to point B. The tube is now drawing much more current than previously, the capacitance begins to charge, and the plate voltage begins to fall. The plate characteristics are traversed along the e_{g_2} curve towards zero plate volts, and the voltage across the transformer increases. This process continues until the current in the transformer secondary is in equilibrium with the plate current. At the equilibrium point, the capacitance is charged (draws zero current at this instant) and no further increase in transformer voltage will occur. This point is where the line of the load resistance, referred to the primary, intersects the e_{g_2} curve, and it marks the end of the rise-time response of the pulse amplifier. This point is marked C on the figure, and it occurs where the tube is "bottomed." Bottomed operation is desirable since the plate voltage in the bottomed condition changes very little as the tube ages.[1] Hence, the amplitude of the output pulse should remain near the standard value over the useful life of the tube.

1.1.1.2 The Duration.—The rise time is so short that the transformer primary inductance does not have time to begin drawing a great deal of current. However, once the capacitance is charged, the transformer has an almost constant voltage impressed and magnetizing current will begin to build up comparatively rapidly. The point of operation on the plate characteristics will move away from point C back up the e_{g_2} curve toward the knee. This means that the plate voltage is increasing, the transformer voltage is falling, and the output pulse is drooping. The magnitude of the droop will depend upon the primary inductance, the

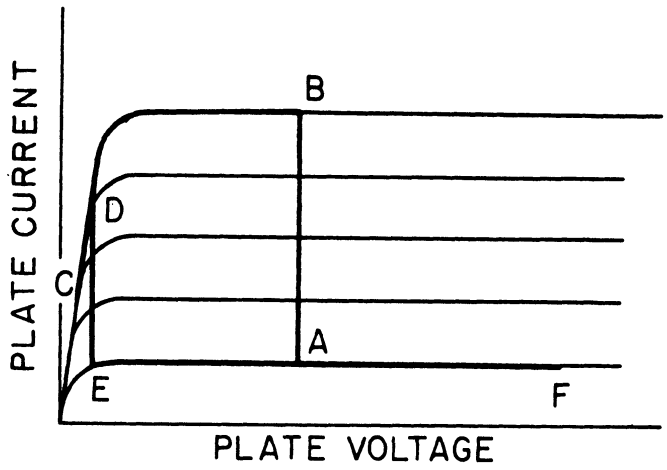


Fig. 1.1. Pentode operating path.

pulse duration, and the plate resistance of the tube in the bottomed condition. If the transformer inductance could be made large, then the magnetizing current and output pulse droop could be kept small. However, as will be seen in the next section, the amount of transformer inductance that may be used at a given repetition rate is fixed by factors other than magnetizing current.

1.1.1.3 The Fall.—At the end of the pulse, the increased magnetizing current has increased the total tube current up to point D on the curves. At this time, the grid is again switched suddenly to e_{g_1}, and again, because of plate shunt capacitance, the voltage cannot change instantly and the plate characteristics are traversed to point E. At this time we have essentially a parallel RLC circuit with an initial charge on the capacitance and with an initial current in the inductance. The R is the load resistance referred to the primary side of the transformer. As the capacitor discharges, the operating point travels along e_{g_1} to A, at which point a critical damping resistance is switched in and the load resistance is switched out by diodes. The current in the inductance then decays and produces a back voltage out to point F and finally back to point A before the next pulse comes along. Rough sketches of important waveforms during a pulse period are shown in Fig. 1.2.

In "speeding up" SEAC-type circuitry, an important factor is plate-circuit shunt capacitance. If the transformer is to recover after one pulse before the next one comes along, the resonant frequency of the transformer primary inductance and the plate-circuit shunt capacitance must be equal to or greater than the desired repetition rate.[2] This means that the allowable transformer inductance is fixed by the tube and stray capacitances so that the magnetizing current and pulse-top droop which result from this amount of inductance must simply be tolerated. If the inductance is made lower than is necessary to allow sufficiently fast recovery, and/or if the load resistance is made too small, the magnetizing current will carry the path of operation back around the knee of the curve where a very small further increase in magnetizing current will cause the plate voltage to rise quickly to the supply voltage and the load current and

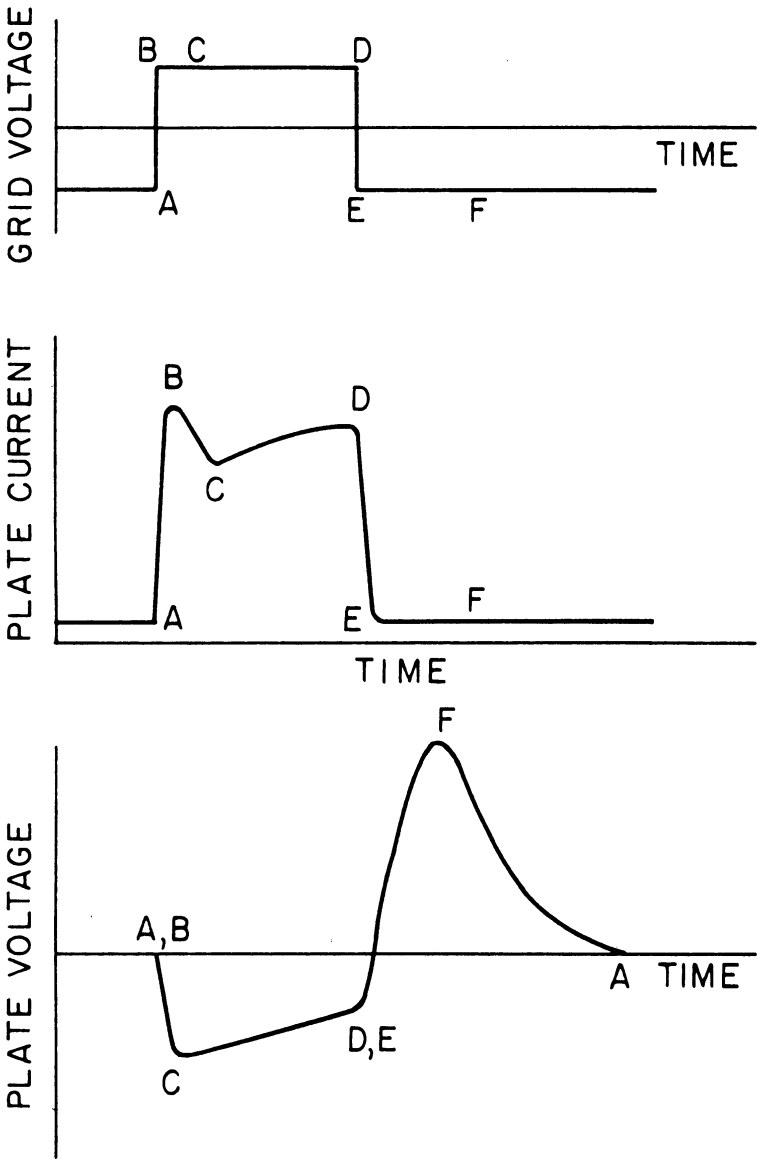


Fig. 1.2. Pentode waveforms.

voltage to fall to zero before the grid pulse is over. That is, the amplifie will not "hold up" a pulse of the width being amplified. This condition indicates that the limit to which the circuit may be loaded has been exceeded.

The same circuit may be loaded more heavily if the grid is drive positive so that the knee to which the magnetizing current must creep is The extent to which this may be carried is limited by either the current dissipation ratings of the tube employed. Usually the plate dissipatio since high plate current occurs only at low plate voltage and vice versa type of amplifier. Consequently, the limit is set by screen dissipatio cathode current, according to which rating is reached first.

1.1.2 QUALITATIVE DISCUSSION OF A TRIODE PULSE AMPLIFIER

From the considerations similar to the preceding, we see that the path of operation on triode plate characteristics is ABCDEFA, as shown in Fig. 1.3. The waveforms are sketched in Fig. 1.4. These waveforms are similar to the pentode case, except that the plate current increases during the transformer backswing where the plate voltage rises above the supply voltage. This additional current may become a significant part of the average plate current, which is undesirable because, in the case of a triode, the tube rating which is likely to be exceeded first is that of average cathode current. The current increase may be eliminated by using a large quiescent bias or possibly by feedback. The first of these would require a large grid swing to drive the tube into heavy conduction, and this is undesirable. Hence, the solution appears to be feedback which would bias the grid more negative as the plate swings positive. This feedback can presumably be derived from the regular package output which is swinging negative at the required time. Further discussion of a triode amplifier is given in section 1.1.3.1.

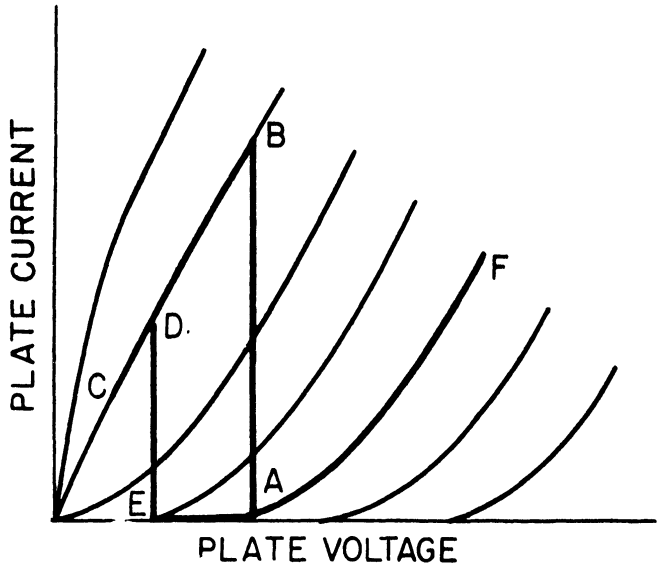


Fig. 1.3. Triode operating path.

1.1.3 LINEAR CIRCUIT ANALYSIS OF POSSIBLE AMPLIFIER CONFIGURATIONS

1.1.3.1 General Discussion.—It is the purpose of this section to develop formulae to be used to estimate the number of gate drives that may be expected from several amplifier configurations. In Appendix D it is shown that the maximum load current from a tube-transformer pulse amplifier is given by

$$I_{L_{max}} = \frac{23}{140\pi^2} \frac{\Delta I^2}{C_p f E_s} - \frac{35\pi^2}{23} f E_s C_s \quad , \tag{1.1}$$

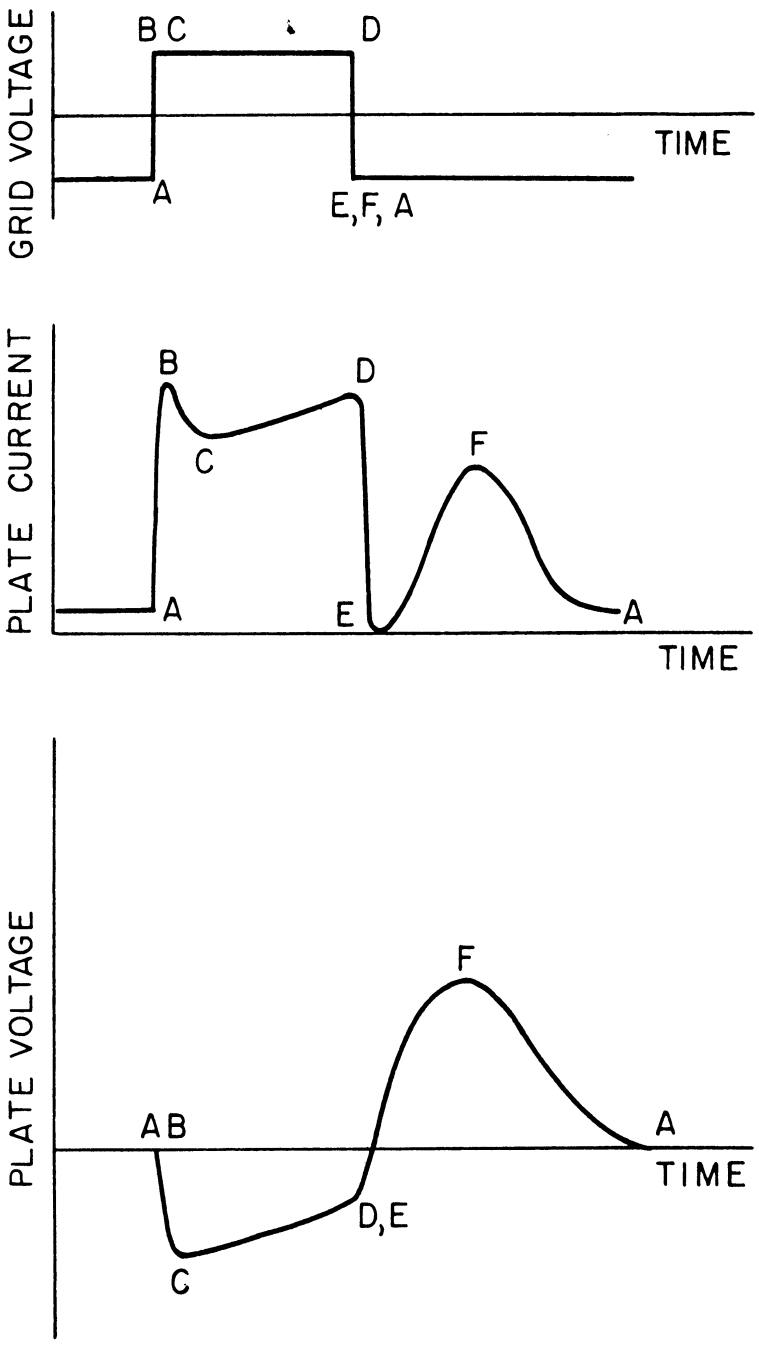


Fig. 1.4. Triode waveforms.

where:

ΔI = pulse-plate current
C_p = primary shunt capacitance
E_s = secondary voltage
C_s = secondary shunt capacitance
f = frequency of operation

If we assume:

(1) that a linear analysis is valid; i.e., that $I = g_m e_g$, where g_m is the tube transconductance and e_g is the grid voltage change,

(2) that one volt of noise clipping is necessary and there is a drop of 2 volts in the diode logic so that $E_s = e_g + 3$, and

(3) that secondary capacitance may be neglected,

then Eq. (1.1) may be rewritten as

$$I_{L_{max}} = \frac{23}{140\pi^2} \frac{g_m^2 e_g^2}{C_{pf} (e_g + 3)} . \tag{1.2}$$

The current required per gate is calculated by considering the circuit of Fig. 1.5. A current I_1 is required to charge and discharge the input capacitance of the pulse amplifier; hence, a current of $2I_1$ is required in the "and" pull-up resistor. From noise considerations it is necessary to have a current I_2 flowing in clamp diode D_1. Hence, the input gate current, I_{gate}, is

$$I_{gate} = 2I_1 + I_2 \tag{1.3}$$

The current I_1 is given by

$$I_1 = \frac{C_g e_g}{0.1 T} = 10f C_g e_g , \tag{1.4}$$

where $T = 1/f$ = pulse repetition period.

The number of gates that may be driven by a gating package is then

$$N = \frac{I_{L_{max}}}{I_{gate}} = \frac{\frac{23}{140\pi^2} \frac{g_m^2 e_g^2}{C_{pf} (e_g + 3)}}{20 f C_g e_g + I_2} . \tag{1.5}$$

Eq. (1.5) applies only as long as none of the ratings of the tube employed are exceeded.

Within the ratings of the tube employed, Eq. (1.5) applies to several amplifier configurations provided the proper input and output capacitances and g_m's are used. Capacitances for several configurations are as follows:

(a) If a pentode or tetrode tube is used, the input capacitance may be taken as the capacitance from the control grid to the cathode and to the screen grid plus stray wiring capacitance. The output capacitance is the capacitance from the plate to the cathode and to the screen and suppressor grids plus transformer and stray capacitances. These input and output capacitances, except for the stray components, are ordinarily published by tube manufacturers.

(b) In a triode the Miller Effect capacitance becomes the dominating part of the input capacitance. This capacitance has a transient and a steady-state component. However, as shown in Appendix B, the steady-state value is

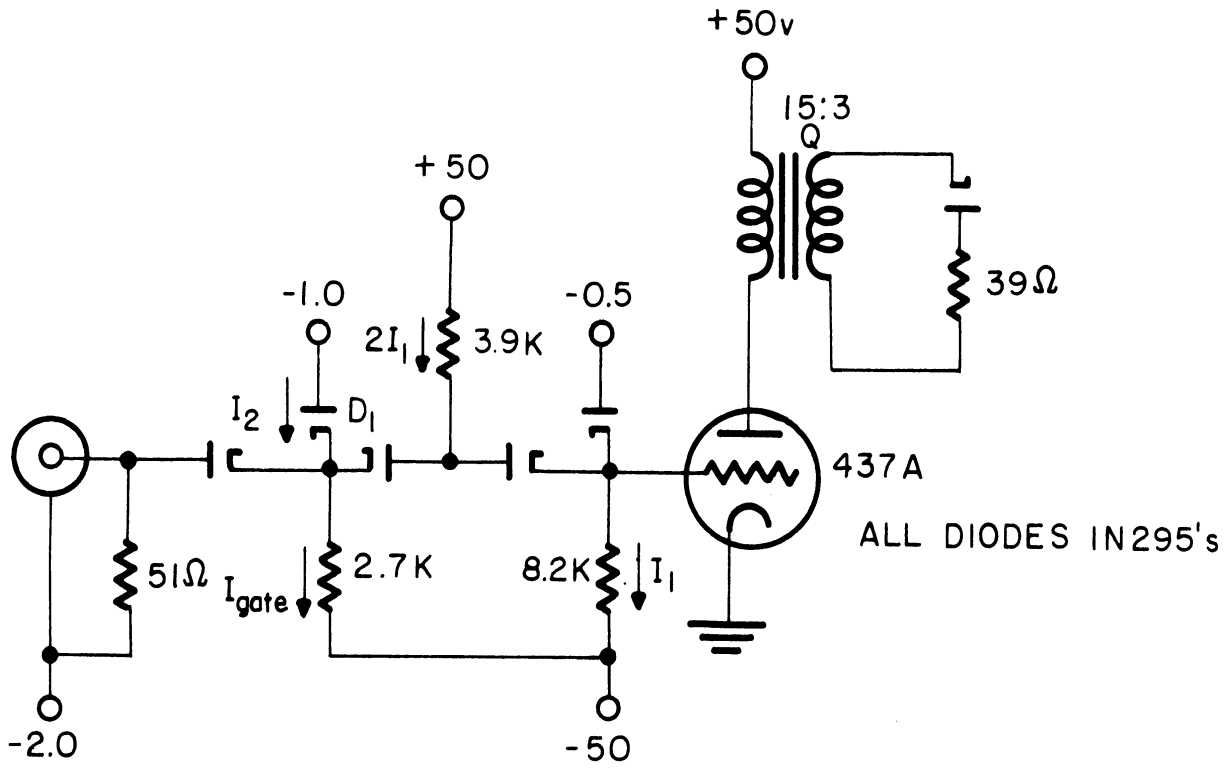


Fig. 1.5. Triode test circuit.

reached in such a short time that the transient may be neglected for operation at frequencies equal to or less than 10 mcps. The input capacitance is then effectively given by

$$C_g = C_{gk} + (1 - A)\, C_{pg} \quad . \tag{1.6}$$

Some experimentation has been performed with the 437A triode to illustrate the Miller Effect. The circuit used was the same as that shown in Fig. 1.5. Results of the experiment are shown in Fig. 1.6. Fig. 1.6(a) shows the grid waveform with the plate supply turned off. In this case the capacitance at the grid is just the grid-to-cathode capacitance and the stray capacitance. The gate pull-up and pull-down currents are large enough to charge and discharge the grid capacitance. In Fig. 1.6(b) the plate supply voltage is turned on, the tube has gain, and the Miller capacitance, which is now present, is large enough to require a comparatively long time to charge and discharge. Presumably it is possible to increase gate currents to the point where they would be able to charge and discharge even the large Miller capacitance in a sufficiently short time. However, such large gate currents would have adverse effects upon the transients in the gating diodes and would require a greater amount of noise clipping. Also, a given triode would be able to drive only a very small number of such high-current gates. It should be possible to drive the input capacitance of the triode by a rather low-power pentode as in Fig. 1.7, whose small input capacitance could be driven by comparatively low-current gates. The backswing of the pentode's transformer

(a) 0.1 μsec/major division
2.0 v/major division

(b) 0.1 μsec/major division
2.0 v/major division

Fig. 1.6. Waveforms for the triode circuit.

would then tend to keep the triode biased off during its transformer's backswing, thereby reducing the triode average plate current. However, if the rise time of the pulse is not to deteriorate too drastically in this cascade pulse amplifier, then the rise time of the pentode stage and of the triode stage must be the same as for a single-stage amplifier. Since rise times of cascaded stages, with rise times T_1, and T_2, add in the square root according to the formula

$$T = \sqrt{(T_1^2 + T_2^2)} , \qquad (1.7)$$

the rise-time requirements on the individual stages become more stringent. In fact, each stage must now rise in only 0.707 of the time that a single-stage pulse amplifier would be allotted.

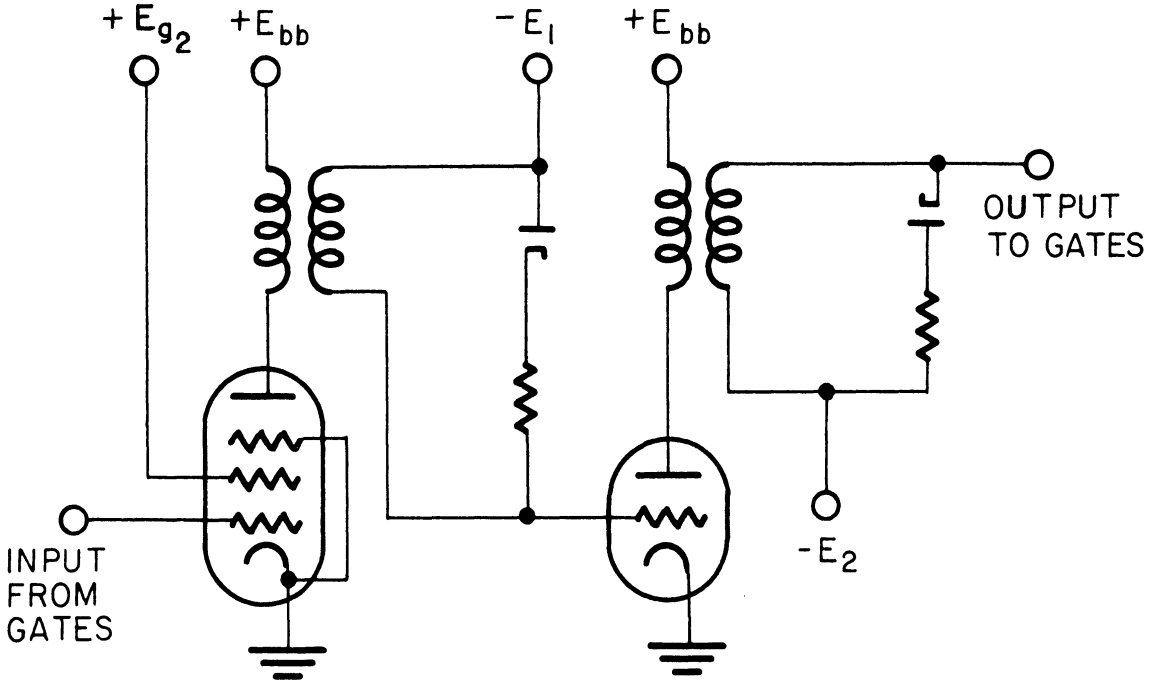


Fig. 1.7. Pentode-triode pulse amplifier.

(c) The cascode circuit of Fig. 1.8 represents an approach which reduces the input capacitance due to the Miller effect. A high figure of merit is

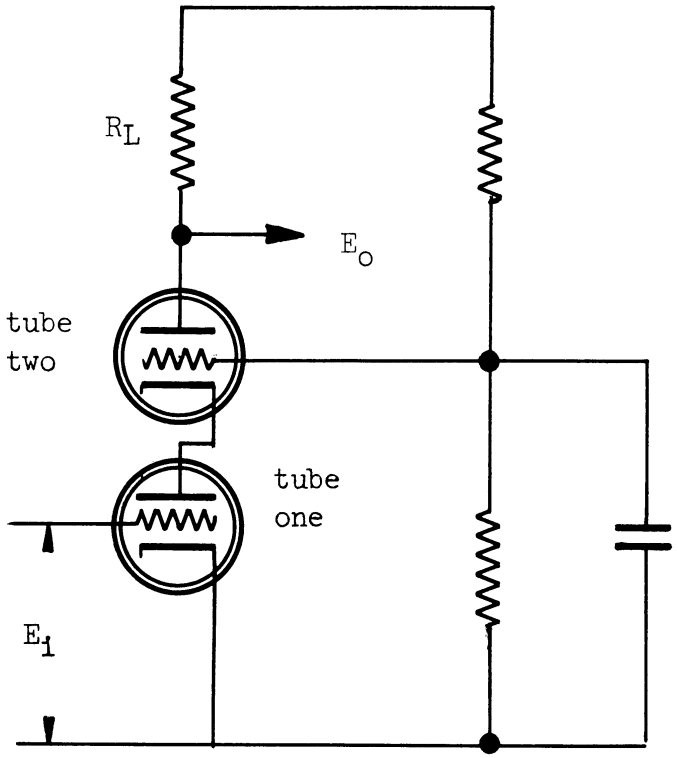


Fig. 1.8. The cascode circuit.

thereby obtained from the very-high-g_m triodes (see Appendix A). The Miller effect in this circuit depends on the gain to the plate of tube one, K_1; K_1 is small because the plate load for tube one is the impedance looking into the cathode of tube two, which is a small impedance approximately equal to $1/g_m$.

Thus we may write

$$C_g = C_{gk} + (1 - K_1)\, C_{pg} \quad . \tag{1.8}$$

To determine the input capacitance, one must first determine the impedance R_e looking into the cathode of tube two. R_e may be found from a consideration of the equivalent circuit of Fig. 1.9. The following equations are written by inspection of the equivalent circuit:

$$I_p = \frac{-\mu\,(E_g - E_{p1})}{2r_p + R_L} \tag{1.9}$$

$$E_{p1} = -\mu\, E_g - I_p\, r_p \quad . \tag{1.10}$$

Substituting (1.10) into (1.9) and simplifying, one obtains

$$I_p = \frac{-\mu\, E_g\, (\mu + 1)}{(\mu+2)\, r_p + R_L} \tag{1.11}$$

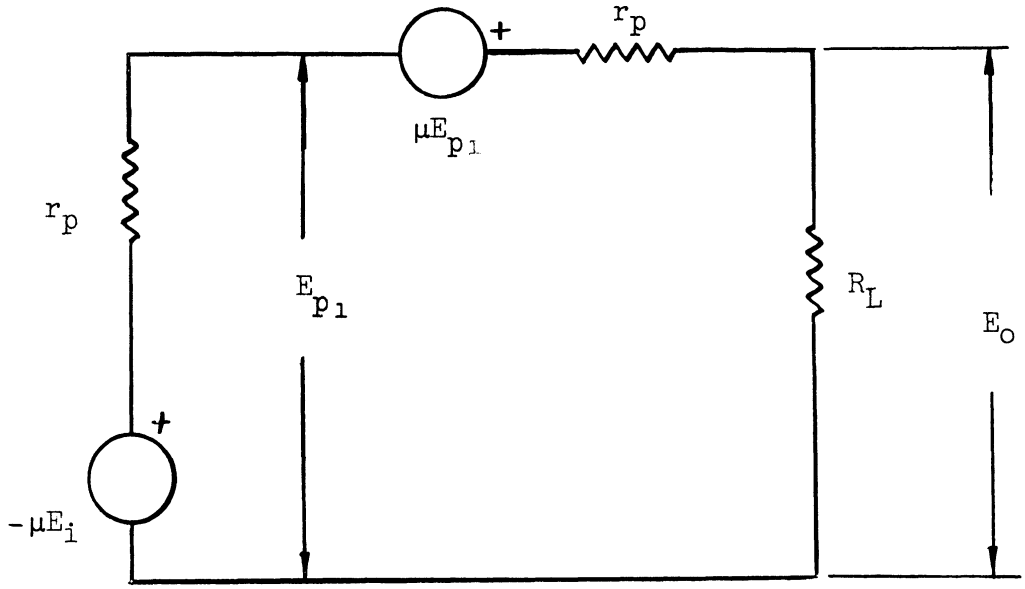


Fig. 1.9. Cascode equivalent circuit.

Substituting (1.11) into (1.10), one has

$$E_{p_1} = \mu E_g + \frac{\mu E_g (\mu + 1) r_p}{(\mu + 2) r_p + R_L} \tag{1.12}$$

The impedance we desire is evidently the ratio of voltage to current at that point:

$$R_e = \frac{E_{p_1}}{I_p} \quad . \tag{1.13}$$

Substituting (1.11) and (1.12) into (1.13), one has finally

$$R_e = \frac{r_p + R_c}{\mu + 1} \quad . \tag{1.14}$$

The gain K_1 is that of a triode with plate load R_e:

$$K_1 = \frac{-\mu R_e}{r_p + R_e} \tag{1.15}$$

$$= \frac{-\mu(r_p + R_L)}{(\mu + 2) r_p + R_L} \quad .$$

Therefore, from (1.8) the input capacitance is

$$C_g = C_{gk} + \left[\frac{\mu(r_p + R_L)}{(\mu + 2) r_p + R_L} + 1 \right] C_{gp} \quad . \tag{1.16}$$

If $R_L \ll (\mu + 2)\, r_p$, this may be simplified to

$$C_g \doteq C_{gk} + (2 + R_L/r_p)\, C_{gp} \quad . \tag{1.17}$$

The figure of merit of the cascode circuit is also dependent on the output capacitance, which is evidently the capacitance plate-to-grid plus some fraction of the capacitance plate-to-cathode since this latter capacitance does not have the full output voltage impressed. The effect of C_{pk} will be that of a capacitance whose size is C_{pk} multiplied by the ratio of the voltage impressed on C_{pk} to the total output voltage. Thus

$$C_p = C_{pg} + \frac{K_2 - K_1}{K_2} C_{pk} \tag{1.18}$$

where K_2 = overall gain.
The gain K_2 is

$$K_2 = E_o/E_i = (R_L I_p)/E_i \quad . \tag{1.19}$$

Substituting I_p from (1.15), one has

$$K_2 = \frac{-\mu(\mu + 1)\, R_L}{(\mu + 2)\, r_p + R_L} \quad . \tag{1.20}$$

If $R_L \ll (\mu + 2)\, r_p$, this reduces to

$$K_2 \doteq -(\mu/r_p)\, R_L = -g_m R_L \quad . \tag{1.21}$$

Substituting the values for K_1 and K_2 into the formula for output capacitance, one has

$$C_p \doteq C_{pg} + \frac{\mu(\mu + 1)\, R_L - \mu\,(r_p + R_L)}{\mu(\mu + 1)\, R_L}\, C_{pk}$$

$$= C_{pg} + \left[1 - 1/(g_m R_L)\right] C_{pk} \quad . \tag{1.22}$$

The figures of merit for particular tubes in a cascode configuration with an overall gain of 20 are presented in Table 1.1. Of these tubes, the 416A is evidently the best. A test circuit using the 437A triode has been studied experimentally to study the feasibility of the cascode circuit.

TABLE 1.1

FIGURE OF MERIT OF CASCODE TRIODES WITH AN OVERALL GAIN OF 20

	417A	437A	416A
C_g(μμf)	13.5	20.1	8
C_p(μμf)	3.28	4.4	2
g_m(ma/volt)	24	45	50
M(rad/μsec)	3600	4780	12,500

1.1.3.2 Predicted Gate Drives for Particular Tubes and Configurations.—

1.1.3.2.1 436A Tetrode.

The current I_2 of Eq. (1.3) has been determined experimentally to be about 4 ma. Allowing 5 pF for grid-circuit stray capacitance and a voltage gain of 40, the input capacitance for the 436A is calculated to be 23 pF. The output capacitance with the transformer in place was calculated from the undamped transformer ringing frequency to be about 10 pF. The transconductance is 30 millimhos. Hence, Eq. (1.5) may be rewritten as

$$N = \frac{23}{140\pi^2} \frac{(30)^2 (10^{-6}) e_g^2}{f (e_g + 3) 10^{-11}} \frac{1}{20(23)(10^{-12}) f e_g + 4 \times 10^{-3}} . \qquad (1.23)$$

This equation is plotted as a function of frequency with grid swing as a parameter in Fig. 1.10(a).

1.1.3.2.2 Cascode 437A.

Again assuming a voltage gain of 40, the input capacitance of 437A's in cascode is calculated to be 27.5 pF. The output capacitance is about 10 pF and the transconductance is 45 millimhos, so that Eq. (1.5) is evaluated to be

$$N = \frac{23}{140\pi^2} \frac{(45)^2(10^{-6}) e_g^2}{f (e_g + 3) 10^{-11}} \frac{1}{20 f (27.5)(10^{-12}) e_g + 4(10^{-3})} . \qquad (1.24)$$

and is plotted in Fig. 1.10(b).

1.1.4 GRAPHICAL CIRCUIT ANALYSIS

Linear circuit analysis is useful in analyzing this type of pulse amplifier in an approximate manner. It tells one the tube parameters which are important and gives one the ability to estimate with very little calculation the number of gate drives that may be expected from a particular amplifier configuration. If a more precise description of the pulse waveform is desired, one can resort to a graphical analysis of the pulse amplifier.

1.1.4.1 General Discussion.—If the grid signal waveform is assumed to be known, then from the plate characteristics of the tube and a known RLC load, the output-voltage waveform may be plotted. From the same set of calculations, the magnetizing current, the capacitive current, the load current, and the total tube current and voltage may be plotted. If the tube has a screen grid, and if the screen-grid characteristics are available, then a plot of screen-grid current may also be obtained by reading the screen current, point by point, for the previously calculated pairs of values of plate voltage and control-grid voltage.

The transformer and its load may be approximated by the circuit of Fig. 1.11. The leakage inductance is small[3] and may be neglected without serious error.

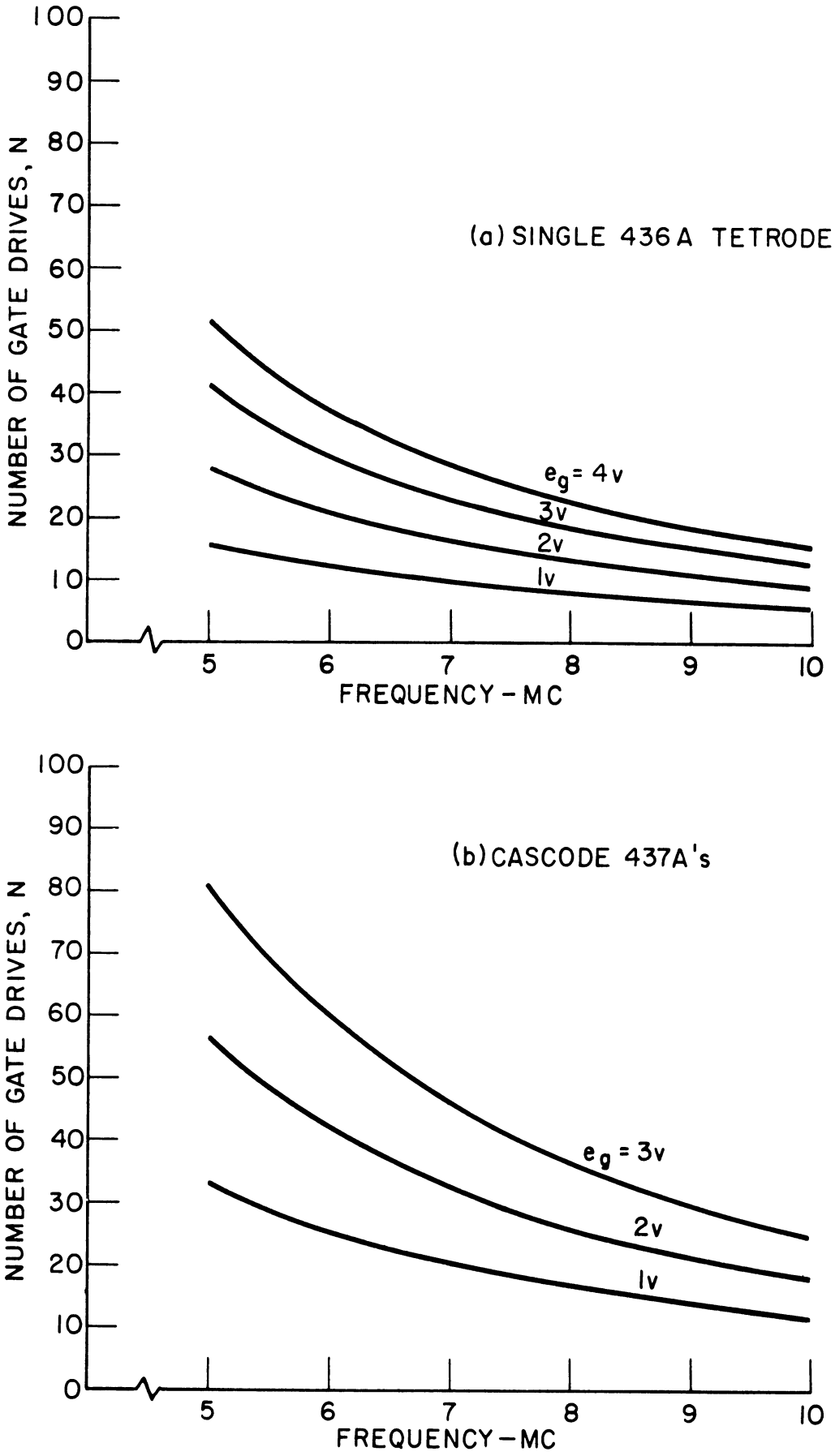
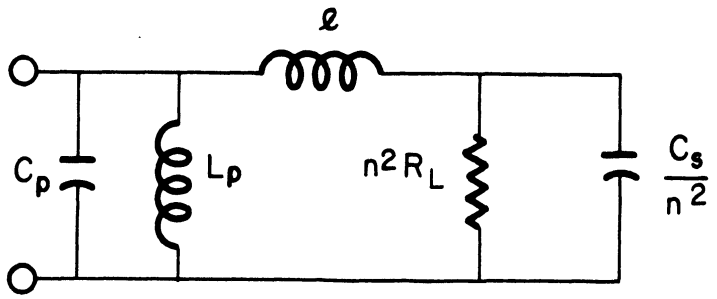


Fig. 1.10. Variation of number of gate drives with frequency.



ℓ = Transformer leakage inductance
L_p = Transformer primary inductance
C_p = Primary shunt capacitance
C_s = Secondary shunt capacitance
R_L = Secondary load resistance
n = Step-down turns ratio

Fig. 1.11. Approximate transformer equivalent circuit.

In this case, the plate load for the tube reduces to a parallel RLC circuit as in Fig. 1.12.

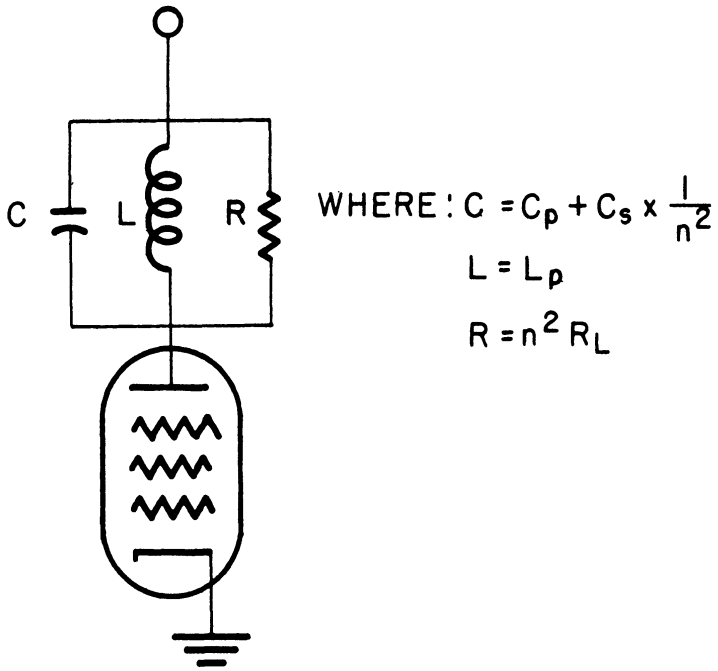


Fig. 1.12. Approximate plate load presented by the transformer and its load.

The essence of the analysis is that the grid waveform may be approximated by true step functions occurring at regular intervals of time as in Fig. 1.13. The approximation becomes more accurate as the number of steps is increased and the time between steps is decreased. The approximation becomes exact in the

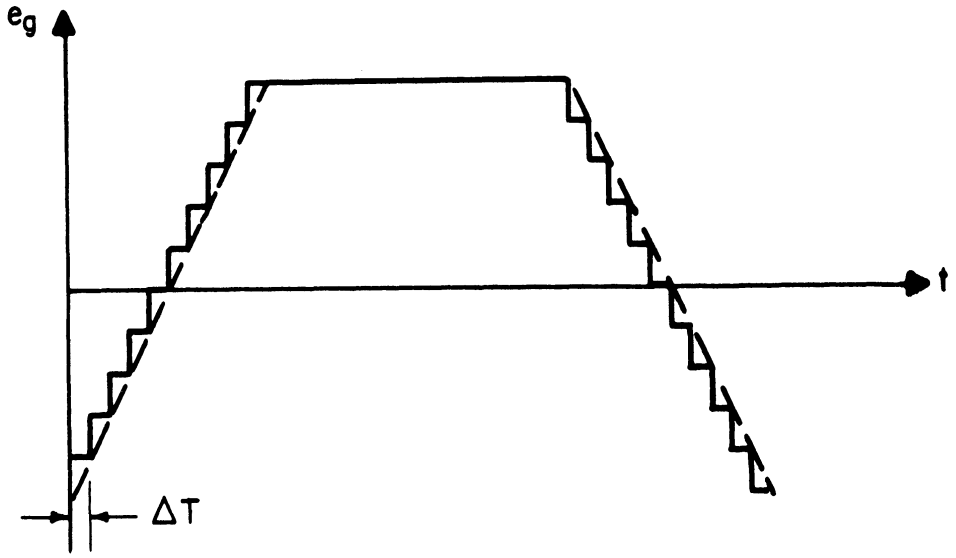


Fig. 1.13. Approximation of a waveform by steps.

limit as the number of steps tends to infinity and the time between steps tends to zero.

The steps of voltage at the grid will result in steps of current through the tube. The tube current-step increase may flow through any of the three paths: R, L, or C. However, a true step increase will flow through C at the initial instant of application, and, if sufficiently short times, Δt, are used, then it is approximately true that the capacitor current will not change appreciably during one time interval. Hence, the voltage across the capacitor will increase during the first interval, and during the second interval this voltage will begin to force current through the resistive load according to Ohm's Law and will begin to change the current in the inductance according to Lenz's Law. Note that an error has been introduced: actually some resistive current will flow as soon as the capacitor has acquired the most minute charge, and also the inductive current will begin to change. However, if the time interval is taken quite small, then the error will be small.

Before the pulse is applied, the grid is at some steady potential, there is some steady flow of plate current, and all this current flows through the primary of the transformer, which is a d-c short circuit. Hence, initially, there is no output voltage e_p and there is no current in either the capacitor or the resistor. Then at $t = 0+$, the grid voltage is suddenly increased and causes a sudden increase in the plate current of i_{b_1}. The problem to be solved then is as illustrated in Fig. 1.14.

For times $t \ll RC$, the currents may be shown to be approximately

$$i_{R_1} = i_{b_1} \frac{t}{RC} \left(1 - \frac{t}{2\,RC}\right) \qquad (1.25)$$

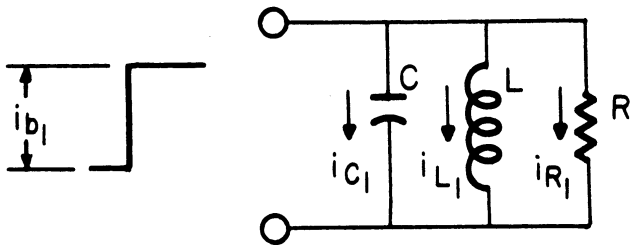


Fig. 1.14. The problem arising from a step grid voltage.

$$i_{L_1} = i_{b_1} \left(\frac{t}{2\,RC} \right)^2 \tag{1.26}$$

$$i_{c_1} = i_{b_1} \left(1 - \frac{t}{2\,RC} \right)^2 , \tag{1.27}$$

provided that the circuit is critically damped. Presumably the increase in plate current i_{b_1} is not known. However, it is known that the output voltage is given by

$$e_{P_1} = E_{bb} - e_{b_1} , \tag{1.28}$$

and it is also known that the output voltage must be given by

$$e_{P_1} = \frac{1}{C} \int i_{c_1}\, dt = i_{R_1} R = L \frac{di_{L_1}}{dt} . \tag{1.29}$$

If we now apply the approximation that the capacitive current is a constant for short times, we have

$$e_{P_1} = i_{c_1} \frac{t}{C} \text{ for } t \ll RC . \tag{1.30}$$

and at the end of the first interval we have

$$i_{c_1} \frac{\Delta t}{C} = E_{bb} - e_{b_1} , \tag{1.31}$$

where

t = $\Delta t-$ (just before the second grid step), and

e_{b_1} = the plate voltage at $t = \Delta t-$ and is unknown.

But i_{c_1} is given by

$$i_{c_1} = i_{b_1} - i_{R_1} - i_{L_1} . \tag{1.32}$$

Therefore,

$$\left(i_{b_1} - i_{R_1} - i_{L_1} \right) \frac{\Delta t}{C} = E_{bb} - e_{b_1} . \tag{1.33}$$

This last equation may be rewritten in the form of a load line, drawn on the plate characteristics, and e_{b_1} and i_{b_1} read off. Given e_{b_1} and i_{b_1}, the currents i_{c_1}, i_{L_1}, and i_{r_1} may be calculated. This procedure may be generalized to the following recursion formulae:

$$E_j = E_{bb} + (i_{r_{j-1}} + i_{L_{j-1}})\,\Delta t/C - e_{p_{j-1}} \tag{1.34}$$

$$e_{b_j} = E_j - (\Delta t/C) i_{b_j} \tag{1.35}$$

$$e_{p_j} = E_{bb} - e_{b_j} \tag{1.36}$$

$$i_{r_j} = e_{p_j}/R \tag{1.37}$$

$$i_{L_j} = i_{L_{j-1}} + e_{p_j}(\Delta t/L) \tag{1.38}$$

$$i_{c_j} = i_{b_j} - i_{R_j} - i_{L_j} \tag{1.39}$$

From these equations, known initial conditions, given grid waveform, and the plate characteristics of the tube used, a complete solution may be obtained.

1.1.4.2 A Specific Example of Graphical Analysis.—The discussion of the preceeding section and the method of applying the formulae to a particular situation can probably be clarified by consideration of a particular example.

Consider the cascode 437A circuit of Fig. 1.15 with input grid signal as in Fig. 1.16 and plate characteristics as in Fig. 1.17. Assume a transformer primary inductance of 200 μhy, a shunt capacitance of 10 pF, and a load resistance referred to the primary of 2k (this value of resistance slightly overdamps the circuit). The plate supply voltage will be taken as 200 volts and the upper grid supply as 75 volts.

Assuming that there has been no input pulse for a sufficiently long time for all transients to have died out, all the plate current will flow through the inductance, and there will be no output voltage and no resistive or capacitive component of current. The grid voltage will be -1.0 volt. Evaluating Eq. (1.34) for these conditions gives E_o = 203.2 volts and substituting into Eq. (1.35) gives

$$e_{b_o} = 203.2 - 200\, i_{b_o} \ . \tag{1.40}$$

This load line is the j = 0 line of Fig. 1.17, and at the intersection with the e_g = -1.0-volt curve, one can read e_{b_o} and i_{b_o} to be 200 volts and 16 ma, respectively. From Eq. (1.36) through (1.39), one calculates $e_{p_o} = 0$, $i_{r_o} = 0$, i_{L_o} = 16 ma, and $i_{c_o} = 0$, respectively. This concludes the first iteration.

For the second iteration, j = 1, t = Δt = 2 mμ sec, and the grid voltage has increased to -0.5 volt, as in Fig. 1.16. Equation (1.34) is again evaluated to be

$$E_1 = 203.2 \text{ volts} \ . \tag{1.41}$$

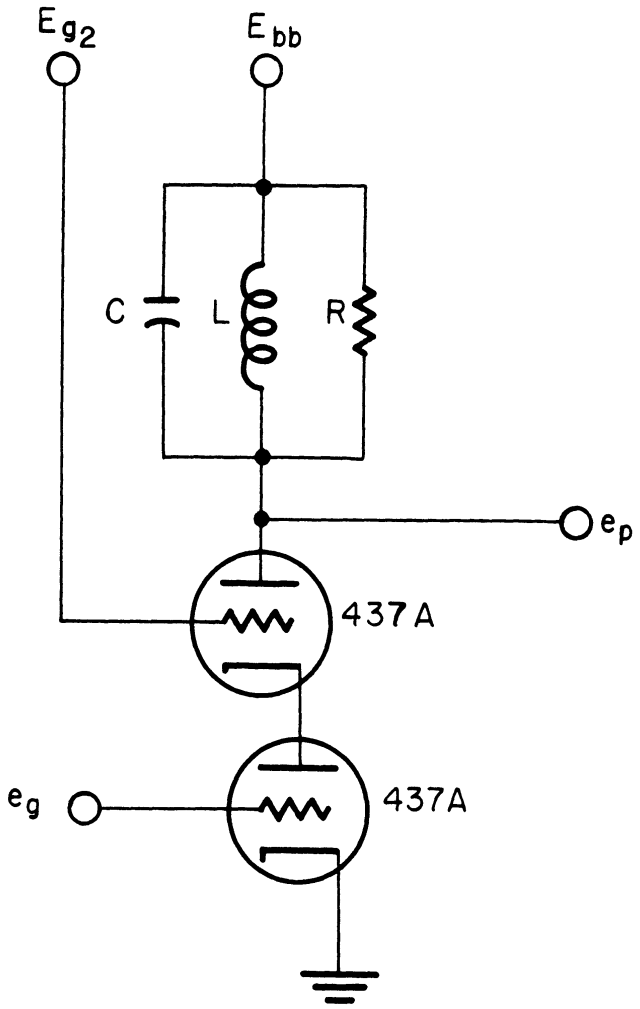


Fig. 1.15. Cascode circuit used in the graphical analysis example. C = tube interelectrode capacitance, plus stray capacitance = 10 pF; L = 150 μhy; R = 2K.

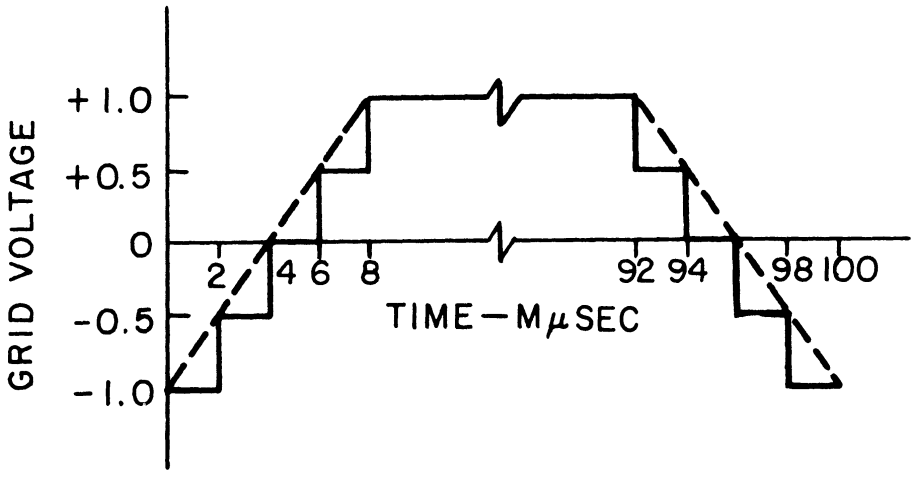


Fig. 1.16. Input signal.

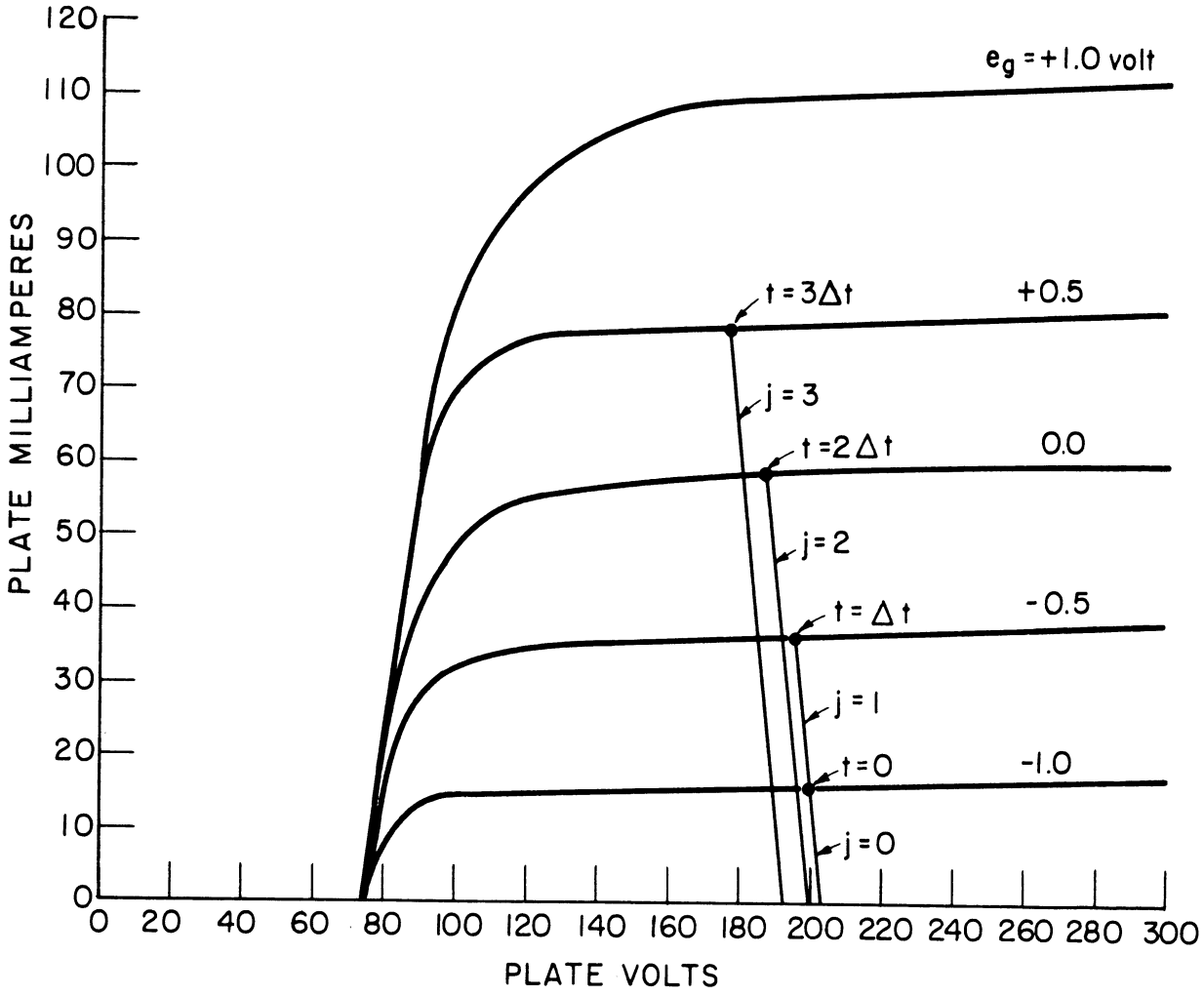


Fig. 1.17. Plate characteristics for graphical analysis.

Therefore, Eq. (1.35) is again

$$e_{b_1} = 203.2 - 200\, i_{b_1} \quad . \tag{1.42}$$

From the intersection of this j = 1 load line with the e_g = 0.5-volt curve, e_{b_1} and i_{b_1} are read as 196 volts and 36 ma, respectively. From Eq. (1.36) through (1.39), one calculated, respectively, e_{p_1} = 4 volts, i_{r_1} = 2 ma, i_{L_1} = 16.05 ma, and i_{c_1} = 18 ma. The second iteration is now ended. Further iterations may be performed similarly with the results being as shown in Table 1.2. These results are presented graphically in Fig. 1.18. Experimental results using the same voltages and circuit parameters are presented for comparison in the photograph of plate voltage in Fig. 1.19.

The graphical method of analysis yields results which agree quite well with experimental results. However, it is a very time-consuming method and, therefore, does not lend itself to an investigation of the effects of varying circuit parameters if calculations are performed by hand. Therefore, the problem

TABLE 1.2

RESULTS OF THE GRAPHICAL ANALYSIS EXAMPLE

j	e_{g_j}	e_{b_j}	i_{b_j}	e_{P_j}	i_{R_j}	i_{L_j}	i_{C_j}	E_j	t
0	-1	200	16	0	0	16.00	0	203.2	0
1	-0.5	196	36	4	2	16.05	18	203.2	2
2	0.0	188	58	12	6	16.21	35.8	199.6	4
3	+0.5	178	79	22	11	16.50	51.5	192.44	6
4	+1.0	162	109	38	19	16.90	73.1	183.5	8
5	+1.0	149	106	51	25.5	17.58	63	169.2	10
6	+1.0	138	104	62	31	18.4	54.6	157.6	12
7	+1.0	128	100	72	36	19.36	44.6	147.7	14
8	+1.0	120	97	80	40	20.42	36	139	16
9	+1.0	114	93	86	43	21.56	29.4	132.1	18
10	+1.0	108	90	92	46	22.8	21.2	126.9	20
11	+1.0	105	86	95	47.5	24.06	14.4	121.8	22
12	+1.0	102	83	98	49	25.36	8.6	119.3	24
13	+1.0	100	80	100	50	26.69	3.3	116.9	26
14	+1.0	99.5	79	100.5	50.25	28.03	0.72	115.3	28
15	+1.0	98.6	77.5	101.4	50.7	29.38	- 2.58	114.2	30
16	+1.0	99	78	101	50.5	30.72	- 3.22	114.6	32
17	+1.0	99.5	79	100.5	50.25	32.06	- 3.31	115.24	34
18	+1.0	100	80	100	50	33.39	- 3.39	116	36
19	+1.0	100.6	80.7	99.4	49.7	34.71	- 3.7	116.7	38
20	+1.0	101.1	81.2	98.9	49.5	36.03	- 4.33	117.5	40
21	+1.0	101.8	82.1	98.2	49.1	37.34	- 4.34	118.2	42
22	+1.0	102.4	83	97.6	48.8	38.64	- 4.44	119.1	44
23	+1.0	103	84	97	48.5	39.94	- 4.44	119.9	46
24	+1.0	103.8	84.7	96.2	48.1	41.32	- 4.72	120.67	48
25	+1.0	104.5	85.3	95.5	47.8	42.59	- 5.09	121.7	50
26	+1.0	105.3	86.1	94.7	47.35	43.85	- 5.1	122.6	52
27	+1.0	106	87	94	47	45.10	- 5.1	123.54	54
28	+1.0	106.8	87.9	93.2	46.6	46.34	- 5.04	124.42	56
29	+1.0	107.7	88.6	92.3	46.15	47.57	- 5.12	125.4	58
30	+1.0	108.4	89.2	91.6	45.8	48.79	- 5.39	126.4	60
31	+1.0	109.1	90	90.9	45.45	50.00	- 5.45	127.32	62
32	+1.0	110	90.4	90	45	51.20	- 5.80	128.2	64
33	+1.0	111	91.2	89	44.5	52.38	- 5.68	129.24	66
34	+1.0	112	92	88	44	53.55	- 5.55	130.38	68

TABLE 1.2 (Continued)

j	e_{g_j}	e_{b_j}	i_{b_j}	e_{P_j}	i_{R_j}	i_{L_j}	i_{C_j}	E_j	t
35	+1.0	112.9	92.9	87.1	43.55	54.71	- 5.36	131.51	70
36	+1.0	113.8	93.4	86.2	43.1	55.86	- 5.56	132.55	72
37	+1.0	114.6	94	85.4	42.7	57.00	- 5.70	133.59	74
38	+1.0	115.7	94.7	84.3	42.15	58.12	- 5.57	134.54	76
39	+1.0	116.7	95.1	83.3	41.65	59.23	- 5.78	135.8	78
40	+1.0	117.7	95.9	82.3	41.15	60.31	- 5.56	136.9	80
41	+1.0	118.5	96.3	81.5	40.75	61.40	- 5.85	138.0	82
42	+1.0	119.7	97	80.3	40.15	62.47	- 5.62	138.9	84
43	+1.0	120.6	97.6	79.4	39.7	63.53	- 5.63	140.2	86
44	+1.0	121.6	98	78.4	39.2	64.57	- 5.77	141.25	88
45	+1.0	122.7	98.6	77.3	38.65	65.60	- 5.65	142.35	90
46	+1.0	123.7	99	76.3	38.15	66.61	- 5.76	143.35	92
47	+0.5	129.1	77	70.9	35.45	67.55	-26	144.65	94
48	0.0	138.3	56	61.7	30.85	68.37	-43.22	149.7	96
49	-0.5	151	35	49	24.5	69.02	-58.52	158.14	98
50	-1.0	166.6	15.1	33.4	16.7	69.46	-71.06	169.7	100
51	-1.0	179.8	15.1	20.2	10.1	70.33	-65.33	182.83	102
52	-1.0	192.7	15.4	7.3	3.65	70.43	-58.68	195.9	104
53	-1.0	204.4	15.7	- 4.4	- 2.2	70.37	-52.47	207.5	106
54	-1.0	214.0	15.9	-14.0	- 7.0	70.28	-47.38	217.0	108
55	-1.0	223.5	16.0	-23.5	-11.75	69.96	-42.21	226.7	110
56	-1.0	231.8	16.0	-31.8	-15.9	69.54	-37.64	235.1	112
57	-1.0	239.3	16.0	-39.3	-19.65	69.02	-33.37	242.5	114
58	-1.0	246	16.0	-46	-23	68.41	-29.41	249.2	116
59	-1.0	252	16.1	-52	-26	67.72	-25.72	255.1	118
60	-1.0	257	16.2	-57	-28.5	66.96	-22.26	260.3	120
61	-1.0	261.3	16.2	-61.3	-30.65	66.14	-19.29	264.7	122
62	-1.0	265.1	16.3	-65.1	-32.55	65.27	-16.42	268.4	124
63	-1.0	268.1	16.3	-68.1	-34.05	64.36	-14.01	271.6	126
64	-1.0	270.9	16.4	-70.9	-35.45	63.42	-11.57	274.2	128
65	-1.0	272.1	16.5	-72.1	-36.05	62.46	- 9.91	275.5	130
66	-1.0	274.0	16.6	-74	-37	61.48	- 7.88	277.3	132
67	-1.0	275.7	16.6	-75.7	-37.85	60.47	- 6.02	278.9	134
68	-1.0	276.9	16.6	-76.9	-38.45	59.45	- 4.4	280.2	136
69	-1.0	277.9	16.7	-77.9	-38.95	58.44	- 2.79	281.1	138
70	-1.0	278.7	16.7	-78.7	-39.35	57.39	- 1.34	281.9	140
71	-1.0	279.0	16.7	-79.0	-39.5	56.34	- 0.14	282.3	142
72	-1.0	279.1	16.7	-79.1	-39.55	55.29	+ 0.96	282.4	144
73	-1.0	278.8	16.7	-78.8	-39.4	54.24	+ 1.86	282.1	146

TABLE 1.2 (Continued)

j	e_{g_j}	e_{b_j}	i_{b_j}	e_{P_j}	i_{R_j}	i_{L_j}	i_{C_j}	E_j	t
74	-1.0	278.5	16.7	-78.5	-39.25	53.20	+ 2.75	281.8	148
75	-1.0	278.0	16.7	-78.0	-39	52.16	+ 3.54	281.3	150
76	-1.0	277.3	16.7	-77.3	-38.65	51.13	+ 4.22	280.6	152
77	-1.0	276.5	16.6	-76.5	-38.25	50.11	4.74	279.8	154
78	-1.0	275.7	16.6	-75.7	-37.85	49.10	5.35	278.9	156
79	-1.0	274.8	16.6	-74.8	-37.4	48.11	5.89	277.95	158
80	-1.0	273.7	16.6	-73.7	-36.85	47.13	6.32	276.94	160
81	-1.0	272.5	16.5	-72.5	-36.25	46.17	6.58	275.8	162
82	-1.0	271.2	16.5	-71.2	-35.6	45.22	6.88	274.5	164
83	-1.0	270.0	16.5	-70.0	-35	44.28	7.22	273.1	166
84	-1.0	268.6	16.4	-68.6	-34.3	43.37	7.33	271.9	168
85	-1.0	267.2	16.3	-67.2	-33.6	42.48	7.42	270.4	170
86	-1.0	265.9	16.3	-65.9	-32.95	41.61	7.64	269	172
87	-1.0	264.3	16.3	-64.3	-32.15	40.75	7.70	267.6	174
88	-1.0	262.8	16.2	-62.8	-31.4	39.94	7.66	266	176
89	-1.0	261.1	16.2	-61.1	-30.55	39.13	7.62	264.5	178
90	-1.0	259.7	16.2	-59.7	-29.85	38.34	7.71	262.8	180
91	-1.0	258.0	16.2	-58.0	-29.0	37.57	7.63	261.4	182
92	-1.0	256.4	16.1	-56.4	-28.2	36.82	7.48	259.7	184
93	-1.0	255	16.1	-55	-27.5	36.09	7.51	258.1	186
94	-1.0	253.4	16.1	-53.4	-26.7	35.38	7.42	256.7	188
95	-1.0	252	16.1	-52	-26.0	34.69	7.41	255.1	190
96	-1.0	250.4	16.0	-50.4	-25.2	34.02	7.18	253.7	192
97	-1.0	249.0	16.0	-49	-24.5	33.37	7.13	252.2	194
98	-1.0	247.6	16.0	-47.6	-23.8	32.74	7.06	250.8	196
99	-1.0	246	16.0	-46	-23	32.13	6.87	249.4	198
100	-1.0	244.4	16.0	-44.4	-22.2	31.54	6.66	247.8	200
101	-1.0	243	16.0	-43	-21.5	30.97	6.53	246.3	202
102	-1.0	241.7	16.0	-41.7	-20.85	30.42	6.43	244.9	204
103	-1.0	240.4	16.0	-40.4	-20.2	29.88	6.22	243.6	206
104	-1.0	239.2	16.0	-39.2	-19.6	29.36	6.24	242.4	208
105	-1.0	238.0	16.0	-38	-19	28.86	6.14	241.2	210
106	-1.0	236.9	16.0	-36.9	-18.45	28.37	6.08	240.0	212
107	-1.0	235.9	16.0	-35.9	-17.95	27.90	6.05	238.9	214
108	-1.0	234.8	16.0	-34.8	-17.4	27.44	5.96	237.9	216
109	-1.0	233.8	16.0	-33.8	-16.9	26.99	5.91	236.8	218
110	-1.0	232.6	16.0	-32.6	-16.3	26.56	5.74	235.8	220
111	-1.0	231.4	16.0	-31.4	-15.7	26.14	5.56	234.6	222
112	-1.0	230.3	16.0	-30.3	-15.15	25.74	5.41	233.4	224

TABLE 1.2 (Concluded)

j	e_{g_j}	e_{b_j}	i_{b_j}	e_{P_j}	i_{R_j}	i_{L_j}	i_{C_j}	E_j	t
113	-1.0	229.5	16.0	-29.5	-14.75	25.35	5.40	232.4	226
114	-1.0	228.4	16.0	-28.4	-14.2	24.98	5.22	231.6	228
115	-1.0	227.4	16.0	-27.4	-13.7	24.62	5.08	230.6	230
116	-1.0	226.4	16.0	-26.4	-13.2	24.27	4.93	229.6	232
117	-1.0	225.3	16.0	-25.3	-12.65	23.94	4.71	228.6	234
118	-1.0	224.4	16.0	-24.4	-12.2	23.62	4.18	227.5	236
119	-1.0	223.9	16.0	-23.9	-11.95	23.30	4.65	226.8	238
120	-1.0	223.0	16.0	-23	-11.5	23.00	4.50	226.2	240
121	-1.0	222.1	16.0	-22.1	-11.05	22.71	4.34	225.3	242
122	-1.0	221.3	15.9	-21.3	-10.65	22.43	4.12	224.4	244
123	-1.0	220.5	15.9	-20.5	-10.25	22.16	3.99	223.7	246
124	-1.0	219.8	15.9	-19.8	- 9.9	21.90	4.0	222.9	248
125	-1.0	218.9	15.9	-18.9	- 9.45	21.66	3.69	222.2	250
126	-1.0	218.1	15.9	-18.1	- 9.05	21.42	3.53	221.3	252
127	-1.0	217.5	15.9	-17.5	- 8.75	21.19	3.46	220.6	254
128	-1.0	216.9	15.9	-16.9	- 8.45	20.97	3.38	220.0	256
129	-1.0	216.4	15.8	-16.4	- 8.2	20.75	3.35	219.4	258
130	-1.0	215.7	15.8	-15.7	- 7.85	20.54	3.11	218.9	260
131	-1.0	215.0	15.8	-15.0	- 7.50	20.34	2.96	218.2	262
132	-1.0	214.3	15.8	-14.3	- 7.15	20.15	2.80	217.6	264
133	-1.0	213.8	15.7	-13.8	- 6.9	19.97	2.73	216.9	266
134	-1.0	213.3	15.7	-13.3	- 6.65	19.79	2.56	216.4	268
135	-1.0	212.7	15.7	-12.7	- 6.35	19.62	2.43	215.9	270
136	-1.0	212.3	15.7	-12.3	- 6.15	19.46	2.39	215.4	272
137	-1.0	212.0	15.7	-12.0	- 6.0	19.30	2.40	215.0	274
138	-1.0	211.4	15.7	-11.4	- 5.7	19.15	2.25	214.6	276
139	-1.0	211.0	15.7	-11.0	- 5.5	19.01	2.19	214.1	278
140	-1.0	210.5	15.7	-10.5	- 5.25	18.87	2.08	213.7	280
141	-1.0	210.0	15.7	-10.0	- 5.0	18.74	1.96	213.2	282
142	-1.0	209.5	15.7	- 9.5	- 4.75	18.61	1.84	212.7	284
143	-1.0	209.1	15.7	- 9.1	- 4.55	18.49	1.86	212.3	286
144	-1.0	208.7	15.7	- 8.7	- 4.35	18.37	1.72	211.9	288
145	-1.0	208.3	15.7	- 8.3	- 4.15	18.26	1.59	211.5	290
146	-1.0	207.9	15.7	- 7.9	- 3.95	18.15	1.50	211.1	292
147	-1.0	207.5	15.7	- 7.5	- 3.75	18.05	1.40	210.7	294
148	-1.0	207.2	15.7	- 7.3	- 3.60	17.95	1.35	210.4	296
149	-1.0	207.0	15.7	- 7.0	- 3.50	17.86	1.34	210.2	298
150	-1.0	206.7	15.7	- 6.7	- 3.35	17.77	1.28	209.9	300

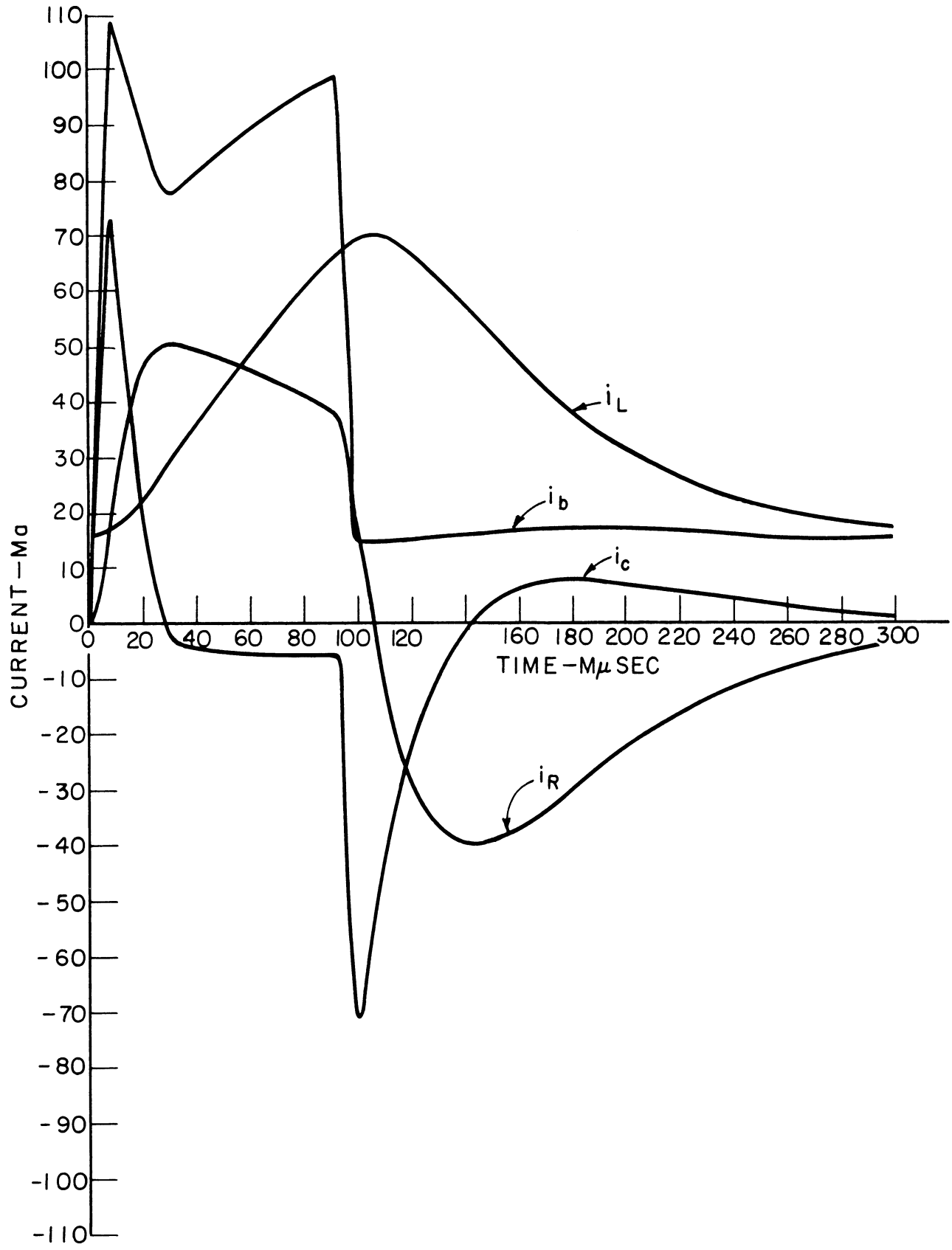
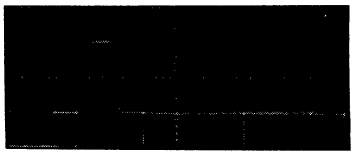
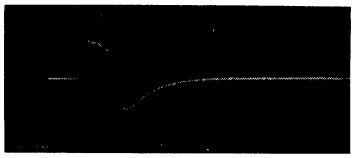


Fig. 1.18. Results of the graphical analysis example.



(a) Grid waveform
1 volt/major division
100 μsec/major division



(b) Plate waveform
100 volts/major division
100 μsec/major division

Fig. 1.19. Experimental waveforms.

of programming an automatic computer to perform the graphical analysis routine was considered and the results are included in Appendix H. Such a program can be modified easily, or even automatically, so that circuit parameters can be varied at will. Furthermore, the speed of a computer as compared with hand computation makes feasible the analysis of a circuit when subjected to a train of pulses rather than just an isolated pulse, as considered here. Any differences between the first and n'th pulses of the train can be observed as can the build-up of the magnetizing current to its steady-state waveform. The load current can be varied to determine the ultimate number of gate drives. Average powers and currents can be computed for each set of impressed voltage and load conditions. Briefly, this analysis can be used to investigate pulse amplifiers in considerable detail and with an accuracy which is consistent with the accuracy of an average family of plate-characteristic curves.

1.2 Experimental Results and Circuits

As a check on the validity of our results, an experimental investigation was made of the circuits which had been analyzed theoretically. Since no generator was available which was capable of producing the desired signal input, it was decided that the pulse amplifier should be made to furnish its own input by means of the dynamic flip-flop circuit. Consequently, dynamic flip-flops using the 436A tetrode and cascode 437A triodes have been built and tested. Both of these circuits were designed for 5 mcps operation; the transformers used were chosen to have a primary inductance which allowed for a sufficiently rapid recovery and with a turns ratio which gave the secondary voltage which was necessary to drive the delay lines. Diagrams for the 437A and the 436A circuits are shown in Figs. 1.20 and 1.22, respectively.

1.2.1 437A CASCODE CIRCUIT

This circuit was capable of supplying 200-ma load current before the flip-flop stopped working. The plate and upper-grid supply voltages are the

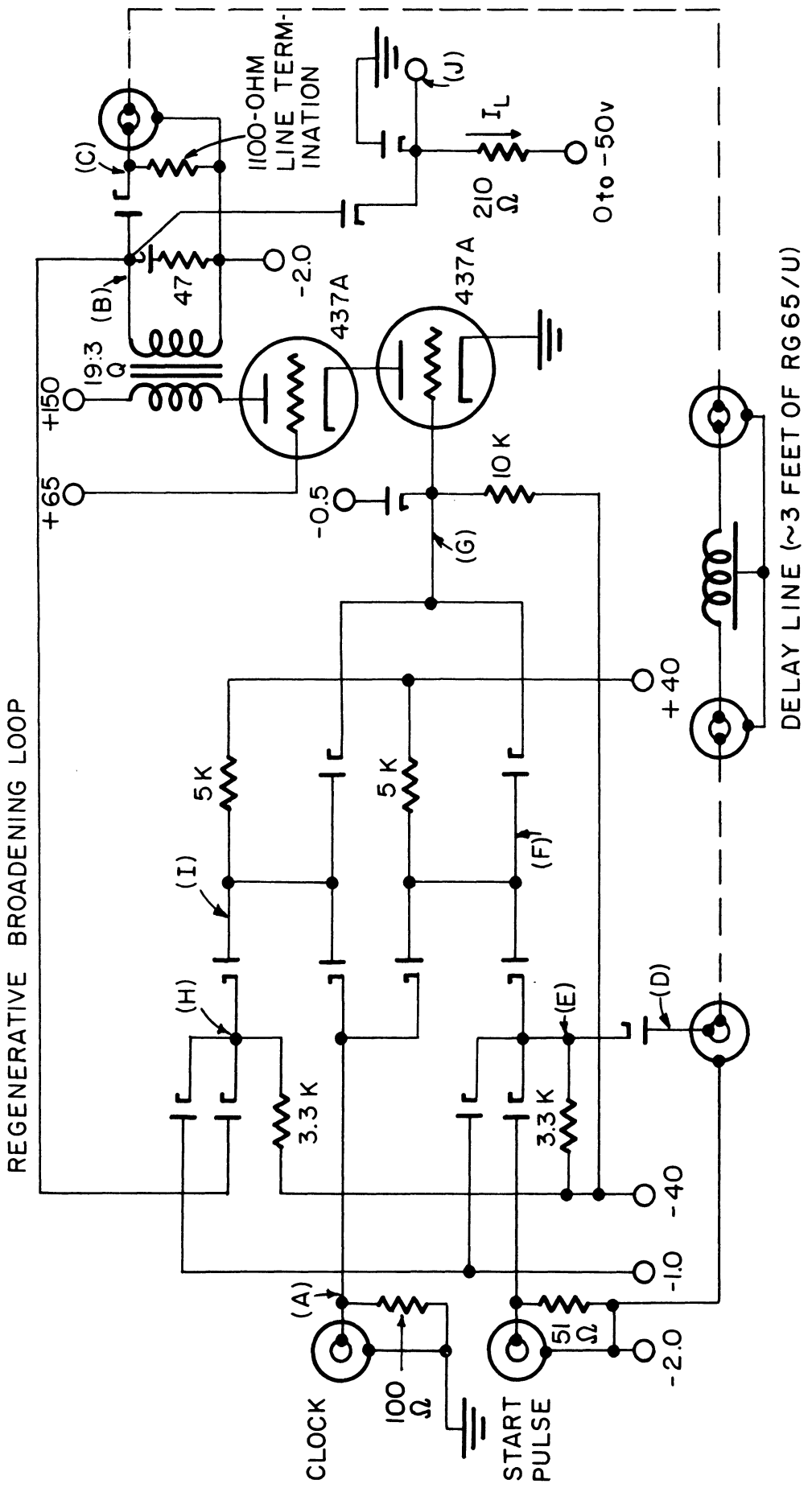


Fig. 1.20. Cascode 437A dynamic flip-flop for 5-mc operation.

maximum that may be used to remain within the rated 45-ma average cathode current of the tube. Table 1.3 gives the plate, upper-grid, and total cathode currents as a function of the load current. The transformer secondary should always be heavily loaded to keep the grid dissipation and cathode current low. Western Electric recommends that the grid dissipation be kept below 20 milliwatts, and this is done in this circuit at all loads. However, the average cathode-current rating is exceeded unless the secondary is loaded.

TABLE 1.3

VARIATION OF TUBE CURRENTS WITH LOAD CURRENT FOR CASCODE 437A'S

I_L (ma)	0	25	50	75	100	125	150
I_P (ma)	24	26	29	31	33	35	36
I_{grid} (ma)	30	26	24	20	17	14	11
$I_{cathode}$ (ma)	54	52	53	51	50	49	47

The 200-ma load current represents about sixteen 12-ma gates that this circuit is capable of driving. Typical waveforms for this circuit are shown in Fig. 1.21.

1.2.2 436A CIRCUIT

This circuit becomes inoperative when the load current exceeds 350-ma or about twenty-nine 12-ma gates.

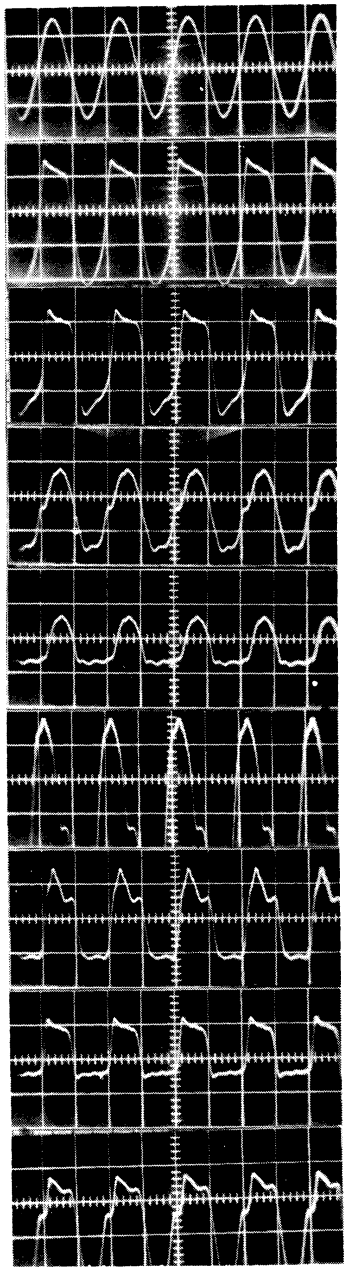
Again the transformer secondary should always be loaded to keep the screen dissipation below the rated value as indicated in Table 1.4.

TABLE 1.4

VARIATION OF TUBE CURRENTS WITH LOAD CURRENT FOR THE 436A

I_L (ma)	0	25	50	75	100	125	150	175	200
I_P (ma)	15	17	18	19	20	21	22	23	24
I_S (ma)	37	35	34	32	31	30	29	28	26
P_S (watts)	2.77	2.62	2.55	2.4	2.32	2.25	2.17	2.10	1.95

Waveforms for this circuit are given in Fig. 1.23.



Waveform at
Point (A) 10 v/cm

Point (B) 10 v/cm

Point (C) 10 v/cm

Point (D) 5 v/cm

Point (E) 5 v/cm

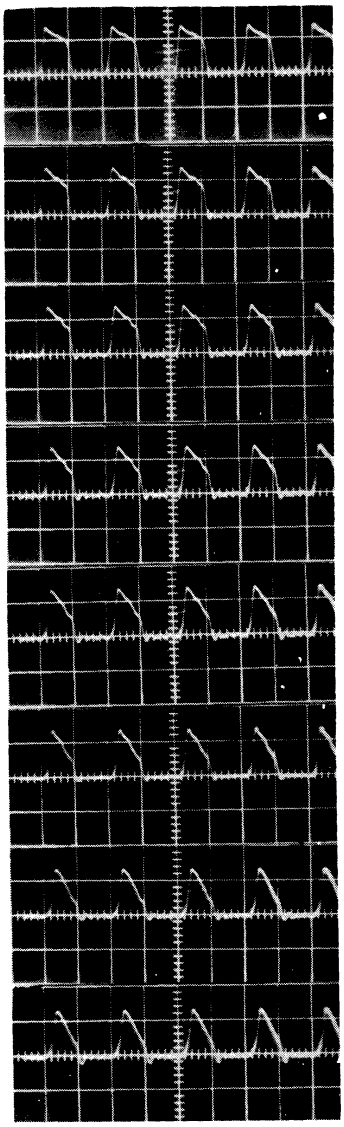
Point (F) 2 v/cm

Point (G) 2 v/cm

Point (H) 10 v/cm

Point (I) 5 v/cm

(a)



5 v/cm
I_L = 25 ma

I_L = 50 ma

I_L = 75 ma

I_L = 100 ma

I_L = 125 ma

I_L = 150 ma

I_L = 175 ma

I_L = 200 ma

(b)

Fig. 1.21. Waveforms for the 437A dynamic flip-flop. (a) Waveforms at various points in the circuit of Fig. 1.20 for I_L = 25 ma. (b) Waveforms at (J) for the indicated magnitudes of I_L.

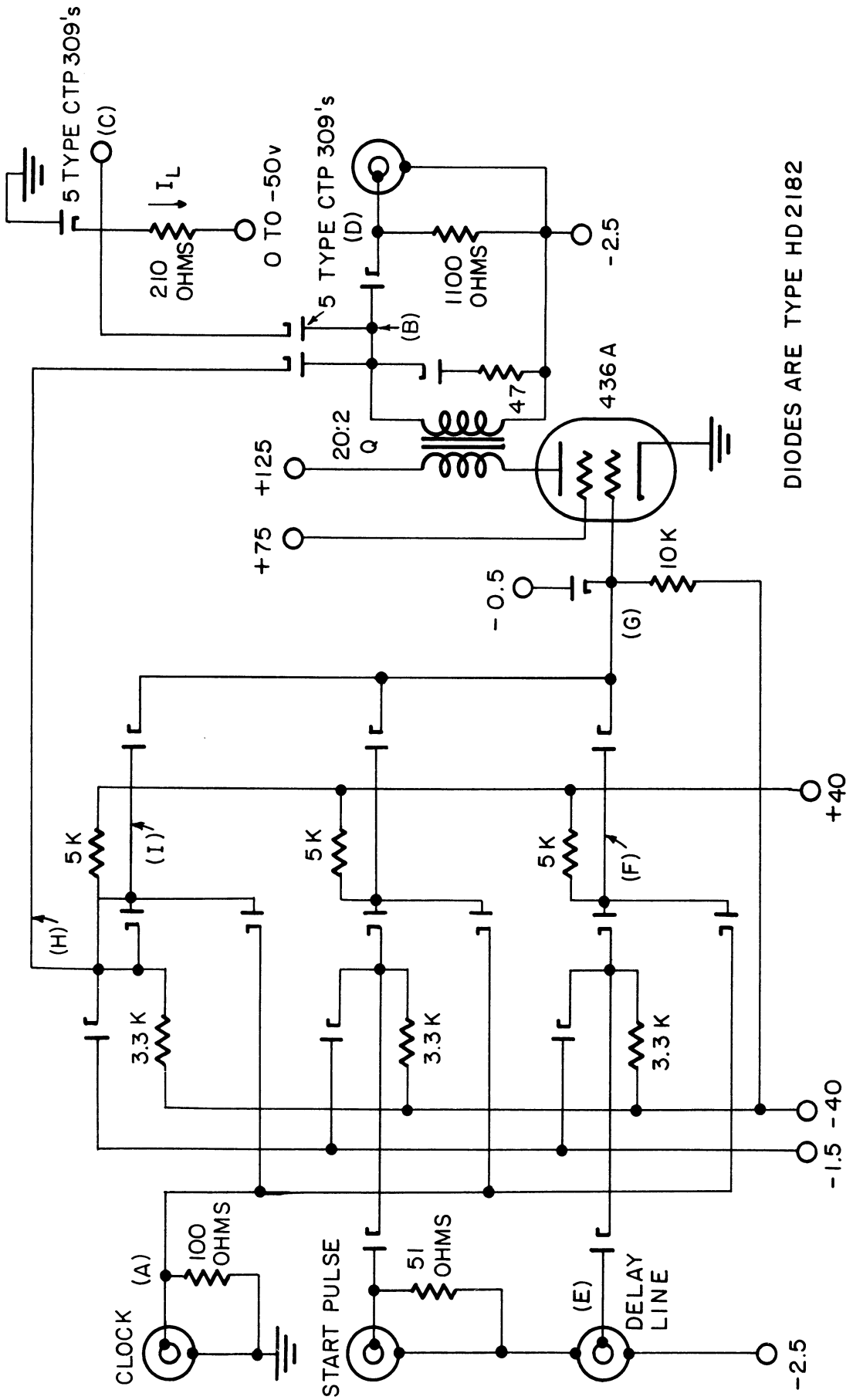
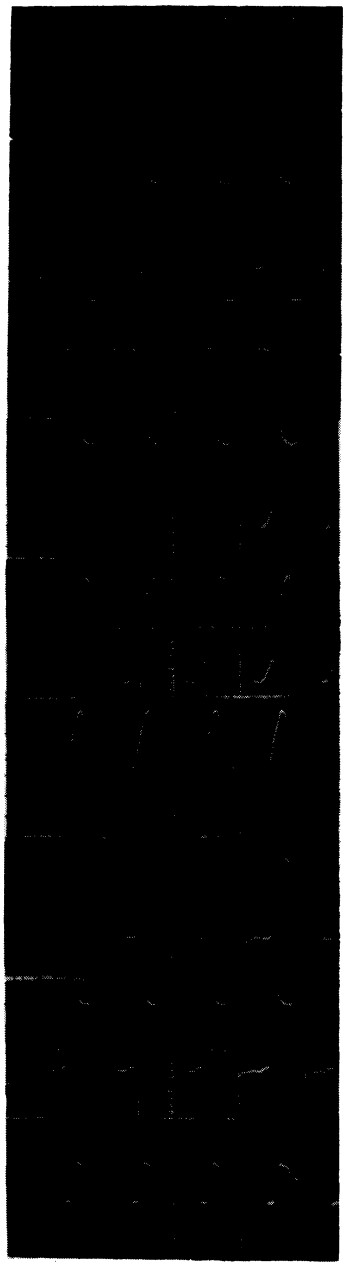


Fig. 1.22. 436A dynamic flip-flop for 5-mc operation.



Waveform at
Point (A) 10 v/cm

Point (B) 10 v/cm

Point (C) 5 v/cm

Point (D) 5 v/cm

Point (E) 2 v/cm

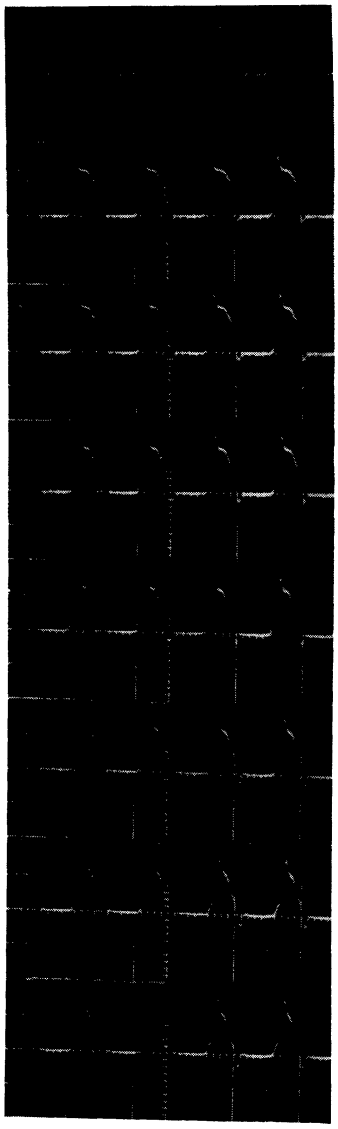
Point (F) 2 v/cm

Point (G) 2 v/cm

Point (H) 5 v/cm

Point (I) 5 v/cm

(a)



5 v/cm
I_L = 25 ma

I_L = 50 ma

I_L = 75 ma

I_L = 100 ma

I_L = 125 ma

I_L = 150 ma

I_L = 175 ma

I_L = 200 ma

(b)

Fig. 1.23. Waveforms for 436A dynamic flip-flop. (a) Waveforms at various points in the circuit of Fig. 1.21 for I_L = 25 ma. (b) Waveforms at (c) for the indicated magnitudes of I_L.

1.3 Conclusions

Both the 436A and the cascode 437A circuits work fairly well at 5 mcps and provide enough gate drives to be useful computer packages. Neither of these tubes was able to produce as many gate drives as the theory predicted. This is partially because the gate drives were predicted from a linear circuit analysis, which cannot hope to predict accurately the behavior of this nonlinear pulse amplifier, but can give only more or less qualitative information about the desirable properties of the components to be used. However, the main reason that these circuits are not actually able to produce the number of gate drives predicted is that they are both limited by power or current considerations before the theoretical number of gate drives can be reached. Thus, a more realistic analysis should include the tube limitations on cathode current and power dissipation. The theoretical number of gate drives minus the experimental number indicates roughly the increase in gate drives that we would obtain if the tube dissipation could be increased with the other tube parameters held constant.

Further testing of these 5-mcps circuits has been conducted with a view to determining how they may be interconnected (see Chapter V). Preliminary tests with essentially the same circuits, but with different lengths of delay line and with different (lower inductance) transformers, indicate that it should be possible to obtain approximately 10 gate drives from the 436A circuit at 7 mcps.

Because these pulse amplifiers are limited by current or power ratings, tubes with high power ratings are desirable.

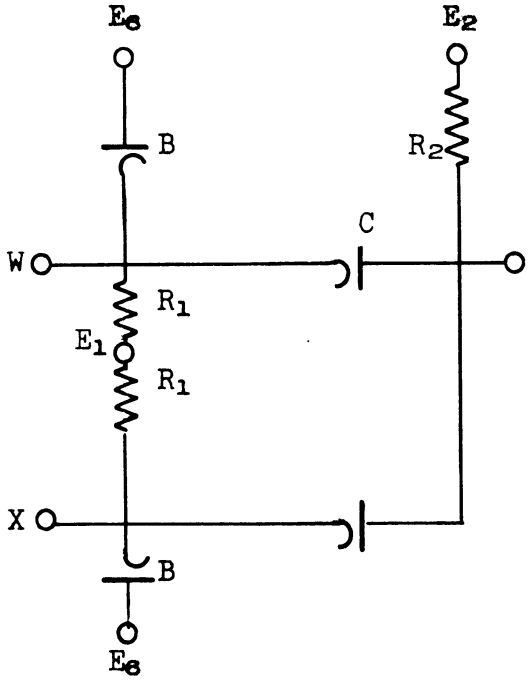
If tubes were available which would deliver a larger plate-current swing than the tubes used here with the same grid-voltage swing, that is, with higher g_m's, then it might well be possible to design an amplifier of this type to operate at higher frequencies. However, considering the careful manufacturing processes that were necessary to produce the tubes used here,[4] it seems unlikely that significantly better tubes will be developed in the near future.[5]

2. GATING CIRCUITRY

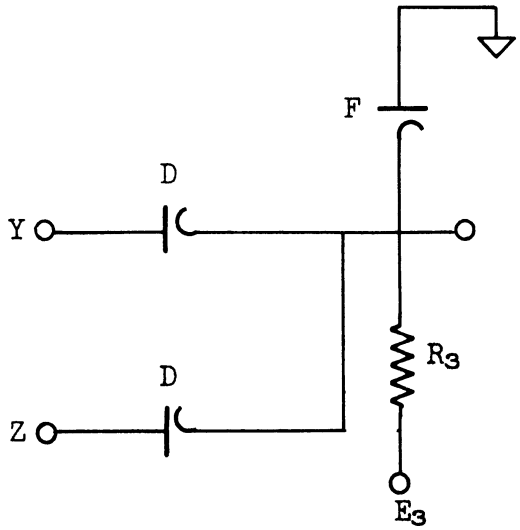
2.1 Operation of Gating Structure

The circuit of a typical gate structure is shown in Fig. 2.23. This circuit consists of two parts—an "and" gate followed by an "or" gate. The typican "and" structure shown below has the C diodes arranged in such a manner that the output voltage is equal to the lowest voltage applied to the diodes. Let us assume, therefore, that we have two voltage levels, 0 and 1. The 1 level shall be the highestlevel. If all the inputs of the "and" structure are high, then the output is high or in the one state. However, if any one of the inputs to the "and" structure is low or in the zero state, the output of the "and" structure is also in the zero state. This can be verified by studying the circuit given. The "and" gate output is clamped to the zero level by the B clamp diode and pull-down resistor R. Therefore, in the absence of any signal the gate is automatically clamped to the zero level.

A typical "or" gate is also shown below. The "or" gate implements the logical function Y + Z which is the disjunction of Y · Z. The gate must provide an output if either of the inputs are high. This can be verified by an examination of the circuit.



Typical "and" gate W · X

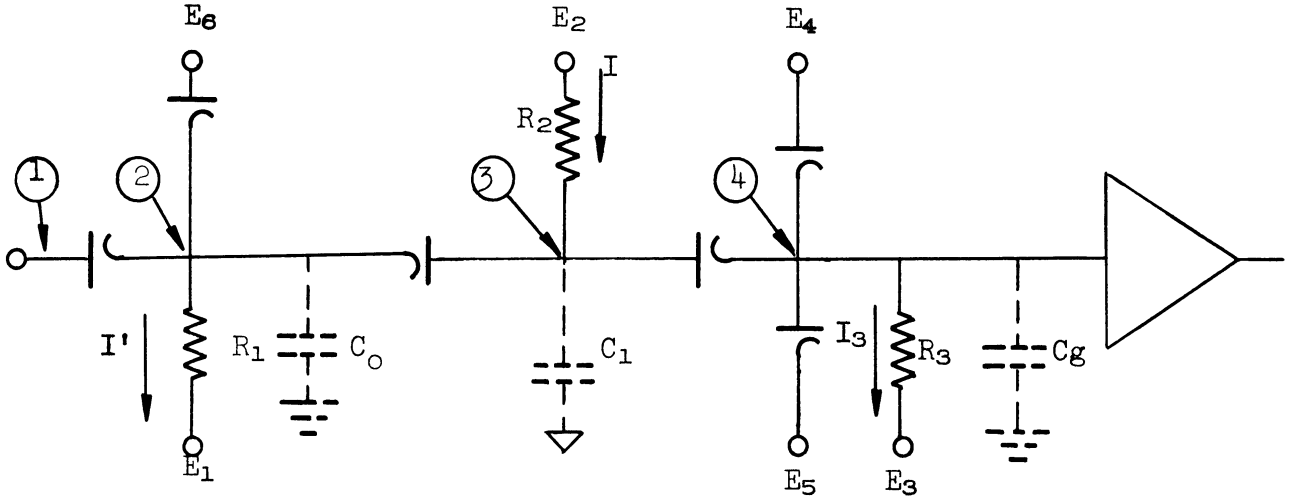


Typical "or" gate Y + Z

If either of the preceding "and" gates provides a 1 output, it can be seen that the output of the "or" gate is 1. On the other hand, if neither of the "and" inputs provides a high output, the "or" output will be zero.

2.2 Gate Requirements for Ideal Diodes

Some general remarks can be made regarding the gate configuration below where perfect diodes are assumed.



First, if the gate voltage swing is small compared to the supply voltages, the charging and discharing of the capacitance associated with the gate occurs at approximately constant current. If the grid capacitance C_g is required to discharge in time Δt through the grid pull-down resistance R_3, the grid pull-down current I_3 is then:

$$I_3 = \frac{E_g C_g}{\Delta t} \quad . \tag{2.1}$$

The gate current I required to swing the grid E volts in Δt seconds is given by:

$$I = \frac{(E_g + E_n)C}{\Delta t} + \frac{E_g C_g}{\Delta t} + I_3 \quad , \tag{2.2}$$

where

$I = 2I_3$ if C_1 is neglected,
$\Delta t = T/10$,
T = the clock period, and
E_n = amplitude of the noise clipping at the "or" gate input.

Example: Let T = 100 mμsec (10 Mc operation)
E_g = 1 volt
E_n = 1 volt
C_g = 30 μμf
C_1 = 5 μμ1
I_3 = 3 ma
I = 7 ma

Second, the input gate current must satisfy two requirements, namely, I' must be greater than I and must satisfy Eq. (2.3). Equation (2.3) is the requirement placed on the input gate current by the discharge time of the circuit input capacitance. The input capacitance of each gate must discharge through the input pull-down resistance.

$$I' \geq \frac{E_o C_o}{\Delta t} \quad , \tag{2.3}$$

where

E = amplitude of the signal applied to the gate input.

The grid-pulse rise time is also influenced by another factor. The grid pulse can rise no faster than the slowest rising input, but in a clocked computer the information inputs are up before the clock pulse arrives. This stresses the necessity of having a well-shaped clock pulse with a rise and fall time less than or equal to the rise time desired for the grid pulse.

If the above requirements are met, that is, if (1) the input signal is more positve than the grid clip level, and (2) the slowest input rises faster than the desired grid rise, then in the ideal diode case, the grid wave-shape is independent of the input wave shape and is a function of gate current I and any wave shaping that may be done on the grid.

These requirements are fundamental to gating operation,and although they were considered for the ideal diode case, they apply equally well to the non-ideal diode case with only slight modification.

2.3 Application of Nonideal Diodes to Gating Circuits

Unfortunately, the diodes in a gating structure are far from ideal; therefore, the emphasis has been placed on the effect of diode transients on the circuit of Fig. 2.23.

It is the diode transient characteristics, particularly the reverse transient, which ultimately limit high-speed gating performance. For example, the reverse transient current of the pulsed "and" diode is primarily responsible for noise at the "and" gate output. If the frequency of operation would be increased by a factor of two with E_g held constant, the gate current I and the initial forward current of each of the pulsed "and" diodes would be increased by approximately a factor of two. Increased forward current would accentuate noise, thus demanding increased noise clipping,and ultimately a large gate current is required to charge capacitance C_1 the additional ΔE_n voltage.

Therefore, emphasis has been placed on diode transients and their resulting effect on the operation of a high-speed logical circuit. The following sections discuss Diode Characteristics (2.3.1), and Diode Specification (2.3.2) for the gating circuits.

2.3.1 DIODE CHARACTERISTICS

In this section the factors which affect diode transients for low current are discussed. Back and forward transient measurements, static characteristics, and experimental results of testing are included.

2.3.1.1 Back Transients.—The recovery time as specified by diode manufacturers in their literature is not applicable to the problem at hand. In general, the manufacturers have specified reverse-recovery time as the time required to reach a particular back resistance for steady-state currents of the order of 30 ma. This is approximately three times larger than the current required in the typical gate circuit considered by this project. It has not been found feasible to extrapolate the recovery time at low currents from the data supplied by the manufacturer. Therefore, during the early phase of this project, a quantity of data was taken to supplement the manufacturers' data. The purpose of this work was first to compare diodes and second to gain insight into factors affecting diode transients. A summary of these tests is included at the end of this section. For the purpose of this report, however, the following transient tests have been used. The biases and currents are those encountered in the proposed logic circuit of Fig. 2.23. The gate circuit itself has been used as a test circuit whenever possible. Those factors affecting reverse recovery of point-contact diodes are:

$$I_B = f(I_f, E_b, R_c, prf) \quad ,$$

where

I_f = steady-state forward current,
E_b = back bias,
R_c = circuit resistance in series with the diode, and
prf = pulse repetition rate.

Their effect on circuit operation are as follows.

2.3.1.1.1 Effect of Forward Current (I_f) on Recovery Time.

The reverse current in a point-contact diode is primarily a function of the forward current previous to switching. That is, the magnitude of the carrier gradient in the N region determines the amplitude and duration of the reverse current after switching.

The importance of the effect of diode reverse-transient currents can be verified by the following experiment. The test consists of observing the current flow in a pulsed diode. A 100-ohm resistance is inserted in the diode circuit between the anode and ground. Normally, a current I_f is allowed to flow in the diode. The diode is then pulsed and the transient current is observed by the voltage which is developed across the 100-ohm resistor. The data and circuit are shown in Table 2.1. The included photographs are the voltage wave-shapes at point (2') and can be calibrated directly in ma.

Before the positive biasing pulse was applied, the voltage drop across the 100-ohms was negative. The shaded area is then the integral of the reverse current or, as defined here, the "lost" charge. The amplitude of the input pulse was adjusted so that the back bias was equal to approximately -1.5 volts at the end of the 50 mμsec pulse.

These reverse currents are of major concern in high-frequency switching as they represent losses not present in the ideal diode. For example, in the ideal diode the gate current I must supply charge to the capacitance C at the "and" pull-up resistor, the capacitance C_g at the tube grid, and current to the grid pull-down resistor. In the nonideal case the gate current must supply an additional amount of charge which is lost to the grid-clamp diode. The input gate current I' to a particular pulsed "and" gate input must also be increased by an amount ϵ ($I'' = I' + \epsilon$) to supply the reverse current taken by the pulsed input clamp diode. Obviously, the number of gate drives from a package output is directly dependent upon the current required per gate input. Therefore, it is particularly important that the lost charge be a minimum.

Since the reverse current is dependent to a large extent on the previous forward current, the magnitude of the noise at the "and" gate output is intimately related to the gate current I. To increase the frequency of operation of a package by a factor of two (or to increase the grid swing by a factor of two), all currents are increased by a factor slightly larger than two. Therefore, noise resulting from the reverse current of the pulse "and" diode* is a function of frequency of operation. The advantage, then, in the small grid signal approach to the over-all problem, as far as diode transients are concerned,

---

*The mechanism by which the "and" contributes to the noise at the "and" gate is considered in detail in Section 2.3.1.3.

is that the diode currents are comparatively small, thus minimizing the effect of diode back-current.

The lost charge is of sufficient importance to warrant the use of this measurement for the diode comparison. The following table is a ranking of the diodes tested. The lost charge has been taken as indicative of the transient properties. Diodes have been rated as inferior to the HD 2109, which has the best overall characteristics, if they have poorer forward conduction or a larger lost charge. The Hughes 2182 and Clevite 309 are representative of diodes with high forward conduction but inferior back-transient properties.

DIODES TESTED

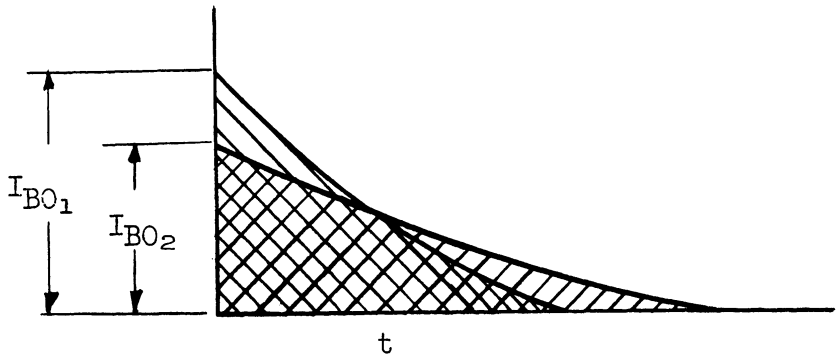
Diode	Inferior to Hughes 2109	
	Statically	Transient
Raytheon IN295	x	
Hughes IN191	x	
Hughes HD2108	x	
Transitron S5G	x	x
Transitron IN251	x	x
Hughes IN629	x	x
Hughes silicon junction	x	x
Hughes HD2191		x
Radio Receptor type W		x
PSI silicon diffusion computor diode	x	x
Hughes IN117	x	x
Clevite CTP309		x
Hughes IN118		x
Raytheon IN306		x
Hughes 2182		x

2.3.1.1.2 Effect of Back Bias on Reverse Recovery.

It can be shown that a reverse field contributes to the removal of hole storage charge.[6] That is, the initial reverse-current spike is higher for increased back bias.

If the duration of the switching pulse were much longer than the 50 mμsec pulse used here, the areas under the reverse-current curves would be constant and the only effect of increased back bias would be to increase the initial reverse current I_{BO}.

$$E_b > E_b \qquad I_{BO} > I_{BO}$$



In Fig. 2.1 the initial back current and the current at 20 mμsec after switching has been plotted for one of the Hughes 2182 diodes where the reverse current is significant and for the Hughes 2109 where it is not. Note that when the transient is significant, the initial back current increases as expected while the back current at 20 mμsec becomes constant for $E_o > 6$ volts. The implication for the gate operation is that the back-biased diode becomes approximately a constant current device. That is, regardless of the back bias the reverse current is essentially constant.

One definition frequently used for the recovery time of a diode is: that time required to obtain a specified back resistance for a given back-bias condition. This definition is somewhat ambiguous since the back resistance is more a function of the back bias specified than an indication of the true transient behavior. A measure of the time required for the diode to reach a back current of, say, 1 ma would perhaps be a more adequate definition of recovery time. The following tabulation for the Hughes 2182 illustrates this point.

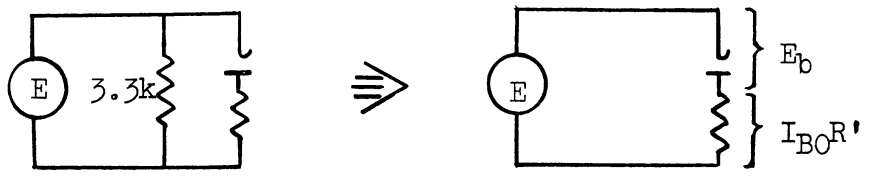
E_b	$R_B(t') = \frac{E_b}{I_B(t')}\ \Omega$
1/2	83
3	273
6	500
10	835
15	1250

$R_B(t')$ and $I_B(t')$ are the resistance and back currents respectively at 20 mμsec.

Gate design and performance is intimately connected with the transmission of charge and therefore the most appropriate criterion of diode performance is the measurement of the "lost charge" that was discussed in connection with Table 2.1.

2.3.1.1.3 Effect of Circuit Resistance in Series with a Back Biased Diode

Another factor which can alter diode transient performance is the amount of impedance in series with the diode. In the previous sections resistance was added in series with the test diode to monitor diode currents. In some cases where relatively poor transient diodes were used (IN117), this small resistance coupled with a low back bias and large forward currents limited the reverse-current spike. The reason for this can be explained with the aid of the following circuit:



Unless $I_{BO}R' \ll E$, the series resistance may be sufficiently large to limit the reverse current. This limitation on the reverse current is quite common for junction diodes. The four photographs of Fig. 2.2 illustrate the contribution of series resistance. Note that when the back bias was increased to 4 volts, the 200-ohm resistance no longer limited the initial back current. In fact, if the scope did not mask the leading edge of the transient, the initial transient would be very large when the series resistance is zero. Certainly the series resistance then sets an upper limit on the initial transient spike.

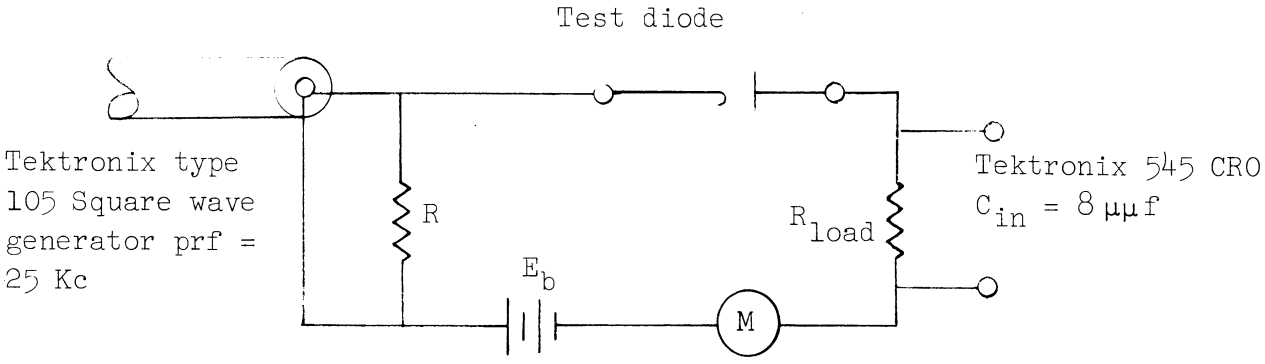
Note that in the logic circuit of Fig. 2.23 series resistance of the input and grid-clamp diode is zero. The series resistance of the back-biased "and" diode is to a first approximation the dynamic resistance of the unpulsed input-clamp and "and" diode in series.

If now the diode has little or no lost charge, as is the case of the Hughes 2109, the effect of series resistance is certainly negligible. Therefore, it is reasonable to conclude for this application that the reverse current of good transient diodes is independent of series resistance even at small back-bias voltages.

2.3.1.1.4 Back Recovery as a Function of Pulse-Repetition Rate.

The back transient is independent of the pulse repetition frequency if the diode under test has had sufficient time to establish the steady-state minority-carrier gradient before being back-biased. If the pulse-repetition rate is such that the above condition is not satisfied, the magnitude of the reverse transient will be affected. This fact is illustrated in Fig. 2.3. The test circuit was pulsed with successive 50 mμsec pulses at a 10 Mc repetition rate. The voltage developed across the 100-ohm resistance is indicative of the diode reverse current. Since the forward transient duration is 10 mμsec or less for most diodes considered, it is possible to conduct gate tests using pulse-repetition rates lower than the basic clock frequency. This procedure is justified up to a frequency of 10 Mc.

In the preceding section the reverse transient was investigated using a 50 mμsec pulse. During the initial phase of this project, the reverse transient measurements were taken on the circuit shown below. These test results have been included to augment data in the preceding section. For some diodes, the reverse transient persists for times greater than 50 mμsec. Therefore, testing with a 25 Kc square wave allowed observation of the complete back transient.



A 25 Kc square wave was used as the input signal and the back bias was varies by changing E_b. The forward current through the diode was varied by changing the amplitude of the input signal. An approximation of the forward current was read on an average current-reading meter. The current read on the meter is a good approximation of the forward current because the average of the reverse current through the diode over half a period is negligible compared to the average forward current. The data taken were as follows:

(a) Reverse current at t = .05 mμsec.
(b) Time for reverse current to reach 5 mils.
(c) Ratio of initial reverse current to forward current (called the a/b ratio).
(d) Initial back current.

These tests were run using two different values for the back bias, namely, -1.5 and -3.0 volts, and different forward currents.

The back transient test circuit, wave shape, and results are shown graphically in Figs. 2.8 to 2.16. There is good agreement between the data in these figures and that in Table 2.1 with one exception. There is an apparent gross disagreement on the characteristics of the HD2182 diode. Actually this disagreement is the result of testing two different groups of HD2182 diodes. One group consistently exhibited poor transient characteristics while the other group exhibited characteristics comparable to those of the good HD2109 diode. This is a good arguing point for user tests.

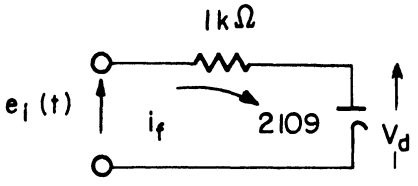
2.3.1.2 Forward Transients.—For diodes of the quality used in typical gating circuits, the forward transients have a negligible effect. To investigate the characteristics of the forward transient, a Tektronix 545 oscilloscope with a

rise time of 12 mμsec was modified by bypassing the furnished vertical amplifier and using instead two cascaded distributed amplifiers (Hewlett Packard 460A and 460B), each with a band-width of 140 Mc. The overall rise time of the probe, amplifiers, and 545 CRT plates is approximately 6 mμsec.

The forward transient test circuit and the resulting data are shown in Fig. 2.17. The voltage developed across the load resistor is an indication of the forward current. Notice that the significant portion of the forward transient is over in less than 10 mμsec for the HD2182, CPT309, Ray 295, and HD2109. A poor forward transient diode, the Hughes 117, has been included to illustrate the difference between good and poor transient diodes.

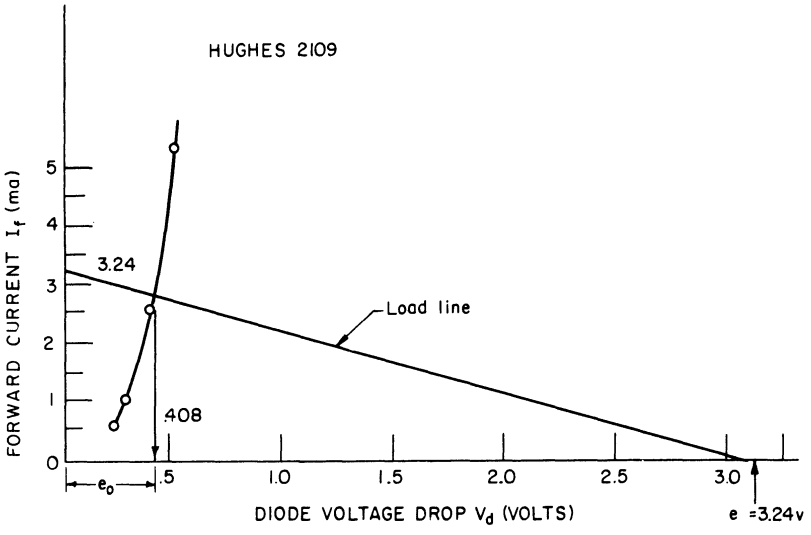
It follows trom Fig. 2.17 that the HD2109 and Ray 295 will function well as grid-clip diodes. Clip, clamp, and limiter are words used interchangeably in connection with a pulsed circuit. Here (Fig. 2.23) Diode F is used to clamp the grid at - 1/2 volt and Diode G clips the positive swing of the grid signal at + 1/2 volt. Figure 2.18 shows the various diodes used as clips (Diode G) in the package of Fig. 2.23. Note the consistency of results of Figs. 2.17 and 2.18.

A somewhat different situation is encountered when a diode is being used to clip a sine wave. It is observed that a good forward transient diode will not clip a sine wave but will only reduce the amplitude of the input signal. In Fig. 2.19 the dependence of the clipped wave-shape on the diode static-characteristics is shown. A sample computation for the case when the input voltage is equal to 3.24 volts is shown below. It is the nonlinear portion of the 2109 characteristic that is responsible for the rounded response. Improvement of output wave shape could be obtained by increasing either e_{in} or the series resistance or both.



$e_i(t) = i_f R + V_d$

$t = 15$ mμsec, $e_i = 3.24$

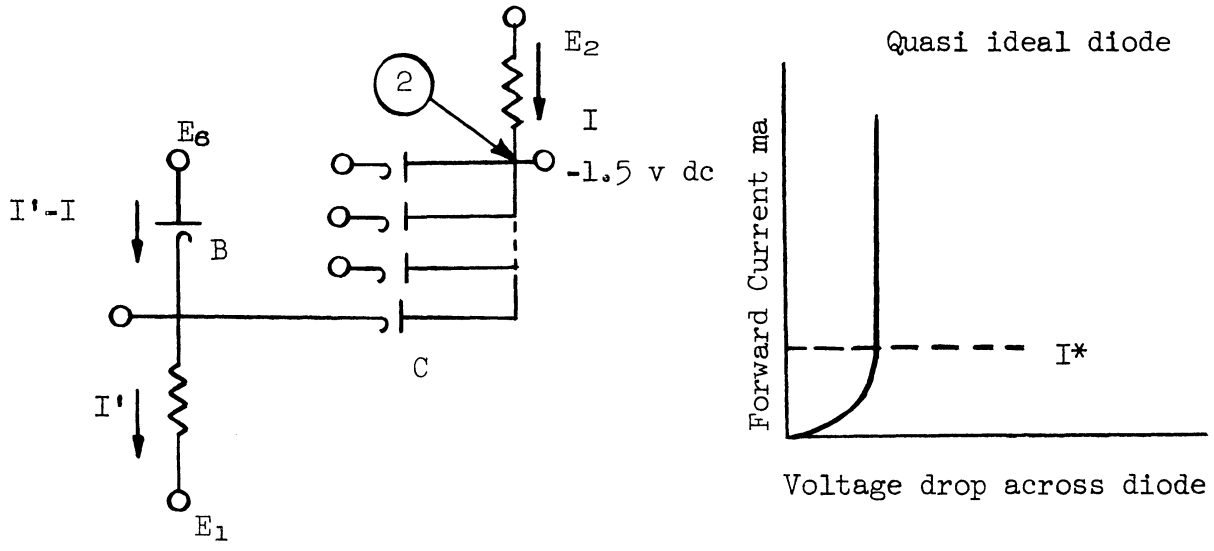


2.3.1.3 Static Forward Characteristics.—The two major problems associated with gating structure are (1) noise when all but one of the "and" inputs

are pulsed and (2) the availability of grid-capacitance charging current when all inputs are pulsed. It is necessary to consider both static and dynamic diode characteristics if noise is to be minimized. In this section the importance of static characteristics as related to static noise will be pointed out. Static noise is defined as the d-c level change in the quiescent condition at the "and" output and the dynamic noise is the component of noise resulting from the reverse-current surge from the pulsed "and" diodes.

$$\text{Total noise} = \text{Dynamic noise} + \text{Static noise}$$

Two examples, (a) and (b), will illustrate the importance of diode static characteristic to gate noise.



(a) Consider an "and" gate for which (n - 1) of the n inputs have been pulsed. The input clamp diodes have been assumed to be quasi-ideal (the quasi-ideal diode characteristic is shown above) while the "and" diodes (C) have realistic characteristics. The current through the input clamp is a minimum when all but one of the inputs are pulsed. If $I' - I \geq I^*$, the voltage drop across the input clamp will be constant.

The voltage supply E_6 necessary for point (2) to be at -1.5 volts is $E = -1.5 + V_c^-$. If (n-1) gates are pulsed, the drop across the "and" diode will be $V_c + \Delta V_c^-$ as the nonpulsed "and" diode is now passing the entire gate current I. The new d-c level at point (2) E_2' is given by

$$E_2' = E_6 - V_c$$

$$E_2' = E_6 - (V_c^- + \Delta V_c)$$

$$V_c = -|V_c^-| = \text{voltage drop across the "and" diode when passing a current I/n.}$$

The static noise is then the difference between E' and -1.5 volts.

$$\text{Static Noise} = -1.5 - E_2'$$
$$\text{Static Noise} = -1.5 - [E_6 - (V_{\bar{c}} + \Delta V_c)]$$
$$\text{Static Noise} = -1.5 - (-1.5 + V_{\bar{c}}) + V_{\bar{c}} + \Delta V_c$$
$$\text{Static Noise} = \Delta V_c$$

ΔV_c is the difference in the voltage drop across the unpulsed "and" diode when the current through it changes from I to I/n. As the number of gates approach infinity, $V_{\bar{c}}$ approaches zero and ΔV_c then is the voltage drop across the diodes when passing the gate current I. This then establishes a lower limit for the noise clipping needed for an infinite number of "and" gate inputs.

A tabulation of this minimum noise for four diodes is included below.

Minimum Noise for an n Input and Gate
(n = ∞) and gate current I(ma)

Diode	4 ma	8 ma	12 ma
309	.35V	.39V	.415V
2182	.36V	.40V'	.44V
2109	.44V	.545V	.625V
295	.5V	.66V	.85V

(b) Now consider the case where the clamp diodes also have realistic characteristics. It can be shown that:

$$\text{Static Noise} = \Delta V_B + \Delta V_c \ ;$$

ΔV_B = the incremental potential drop due to the finite slope of the input clamp characteristics.

If the minimum current I* (Fig. 2.5) is above the knee of the static curve, ΔV_B will be much less that ΔV_c when I/n is small (1 ma) even when Diodes B and C are identical. Two conclusions can be drawn regarding the effect of static characteristics on gate operation. First, the static characteristics of particularly the "and" diode contribute appreciably to the total noise when n is large. Second, it may not necessarily be desirable to reduce the gate current I in an effort to reduce transient effects.

Figure 2.4 illustrates the agreement between actual gate performance and calculations made from the diode static characteristics. An estimate of the total noise was made by assuming each of the pulsed "and" diodes supplied an additional current I_{BO} to the unpulsed "and" diode. The total current to the unpulsed "and" diode during the first instant is equal to $I + (n - 1)I_{BO}$ where I_{BO}

is a function of the forward current $I_f = I/n$. The requirement for the minimum input clamp current of the unpulsed "and" diode, if capacitance is neglected, is given by:

$$I' - I - (n - 1)I_{BO} \geq I^*$$

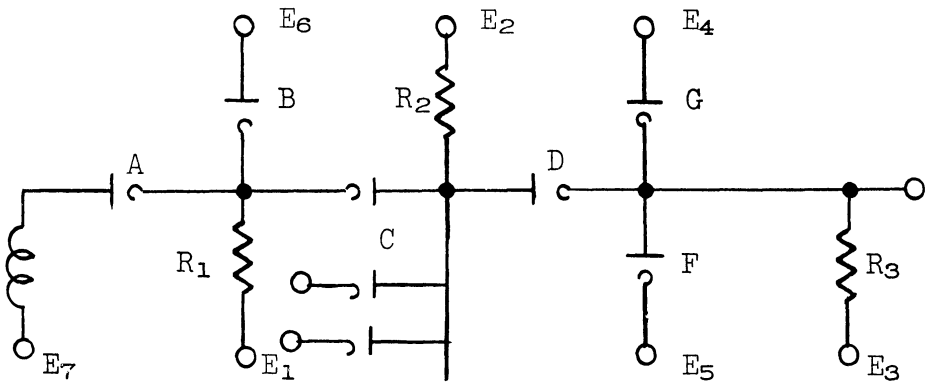
However, capacitance is certainly not negligible and a large portion of the initial back current goes into the capacitance at points (2) and (3). In fact, dynamic noise is to a certain extent reduced by capacitance at point (2). A sample computation for a five input "and" gate using 2109's as input clamps and "and" diodes is shown on the next page. The values used for $I_{BO} = f(I_f)$ were obtained from Fig. 2.15.

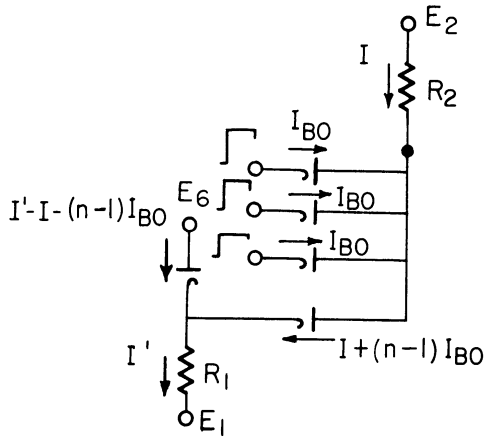
A number of diodes have been tested for static forward characteristics. Figures 2.5 and 2.7 are plots of the average characteristics. The diodes of Fig. 2.5 have been taken as representative of those tested both with regard to transient and static characteristics. Figure 2.6 gives an indication of the consistency of static characteristics within a batch.

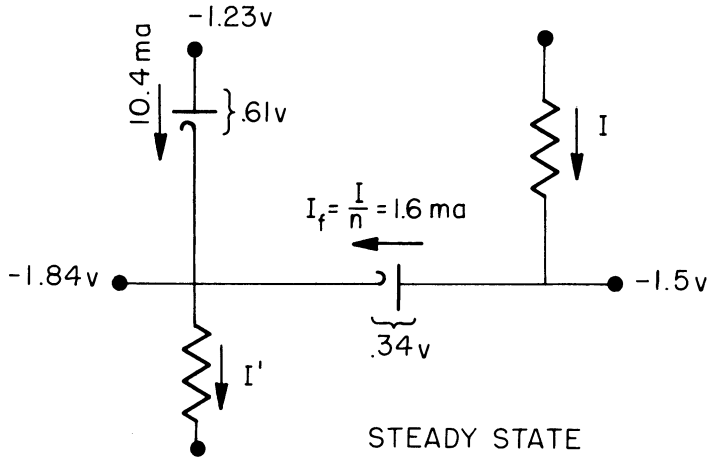
2.3.2 DIODE SPECIFICATION

The information of the preceding section provides a basis for predicting diode performance in any particular logical circuit. The following sections emphasize the relationship between diode characteristics and operational details of a diode gating circuit. The experimental results of testing a clocked and unclocked package are included. Finally, an experimental correlation between static and dynamic characteristics is drawn to show their close relationship.

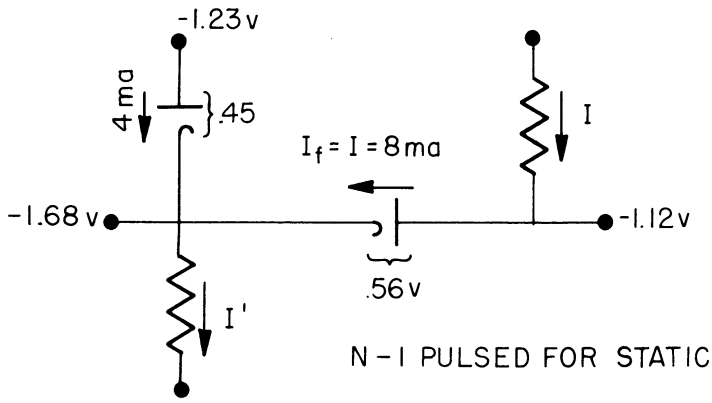
2.3.2.1 Diode Requirements.—In general, the two major considerations in gate design are noise and the effective use of available gate current. Both factors depend primarily on the diode back-transient characteristics. A typical "or"-"and"-"or" gating configuration is shown below. The previous material on diode transients provides a theoretical basis for diode assignment to the various positions A through F. The experimental testing in the following Sections 2.3.2.2 and 2.3.2.3 substantiates these diode requirements.



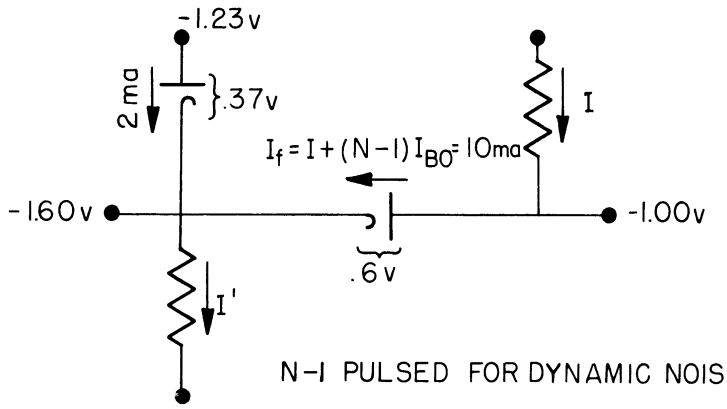




STEADY STATE



N-1 PULSED FOR STATIC NOISE



N-1 PULSED FOR DYNAMIC NOISE

(1) The "or" Diodes A and D require high forward conduction. For frequencies below 10 Mc forward transient are of negligible importance. One would anticipate that the back transient of the "or" diodes would not be objectionable. However, experimental results will show later that the grid "or" Diode D must have the best possible back-transient properties while the back transient of Diode A is not critical.

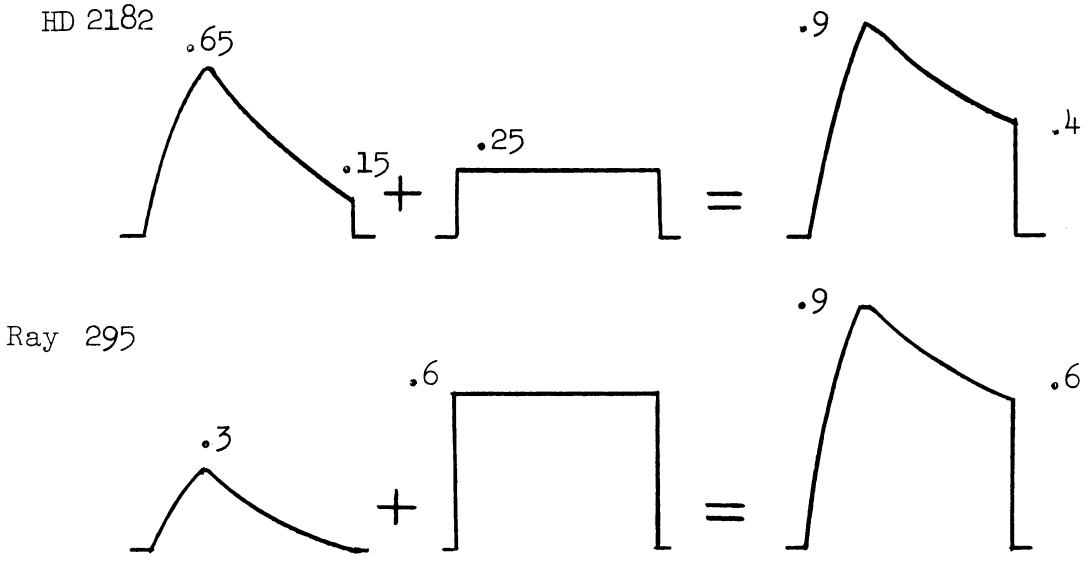
(2) It is desirable that the input-clamp Diode B and the "and" Diode C have a minimum back transient "lost charge." The importance of the static characteristics of this diode has already been pointed out.

(3) The grid-clamp Diode G is required to have good back-transient properties as current lost through this diode represents a loss of grid-capacitance charging current.

(4) Diode F is required to clip the grid signal. In Section 2.2.1.2 it was shown that Diode F may be a good clip in this situation despite poor transient properties. In fact, the forward drop across this diode may be used to advantage to eliminate the use of the E_5 supply. What is actually desired in all cases is a diode which is as nearly ideal as possible. The following tests will outline the criteria for choosing diodes. They will point up the fact that because of the nonideal characteristics it is best in all cases to use diodes with good transient properties with high forward-conduction as a secondary consideration. Of those diodes tested the Hughes 2109 stands out as best fitting this criteria.

2.3.2.2 Experimental Testing, Unclocked.—The diode requirements outlined in the previous section may be verified by comparative testing of diode types at various positions in the package. The gate in Fig. 2.23 has been designed for 10 Mc operation. Fifty mμsec pulses have been applied to this circuit at a 60-cycle repetition rate. The results and conclusions of comparative diode testing are summarized below.

It is desirable that the input clamp diode have both good transient and static characteristics. The Hughes 2109 best fulfills this requirement. The best "and" diode is considered to be the one which contributes the least noise. The total noise has been defined as the additive combination of the static and dynamic noise. The results of comparative tests are shown in Table 2.2. Note that in the case of the 309 and 2182 diodes the experimental and computed static-noise levels differ widely. This is not surprising as these relatively poor transient diodes have considerable reverse transient current flowing at the end of a 50 mμsec pulse even for small forward currents (see Figs. 2.9 and 2.10). It is possible to have the same total noise for a number of combinations of reverse current and static characteristics as shown below. Of the diodes tested, the Hughes 2109 gives the best performance.



Noise composition

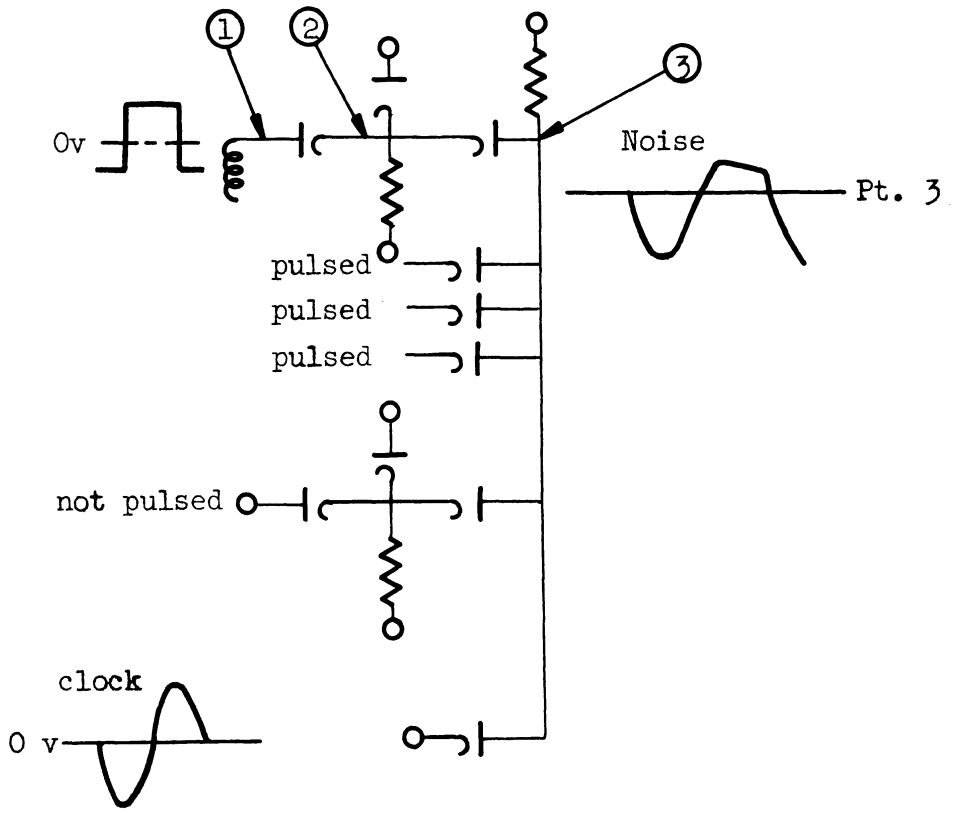
Experimental results have shown that it is necessary to increase the input gate current I' when inferior transient diodes are used in the "and" position. The surge of reverse current to the unpulsed input clamp may be sufficient to cut the n^{th} input off.

There are no situations in which a poor transient diode would intentionally be used as an "and" diode. However, the presence of the reverse current does assist in charging the grid capacitance when all the n inputs are pulsed.

The experimental measurements pertaining to the performance of the grid-clamp diode G are shown in Fig. 2.20. As previously stated, this diode must have excellent back recovery characteristics. The forward conduction is of minor importance, as the supply voltage may be adjusted to give the desired tube bias. In this particular application (Fig. 2.23), it is desirable to use the steady-state drop of the 2109 to establish the grid bias of -.45 to -.5 volt by tying the diode plate to ground and thereby eliminating the E_4 supply.

The experimental results pertaining to the grid-clip Diode F were discussed in Section 2.3.1.2 under forward transients (Fig. 2.18). In the 10 Mc gate of Fig. 2.23 a grid swing of 1 volt was specified. The desired bias condition of -.5 to +.5 volt may be obtained by tying the cathode of the clip diode and plate of the clamp diode to ground. The 2109 has been chosen for both these diode positions because of its transient properties and not on the basis of its forward conduction for a particular application.

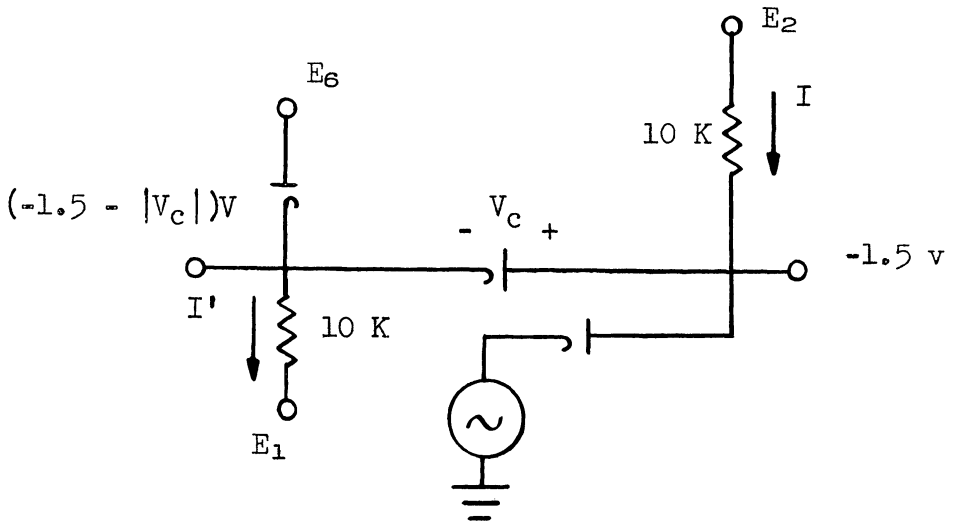
2.2.2.3 Experimental Testing, Clocked.—



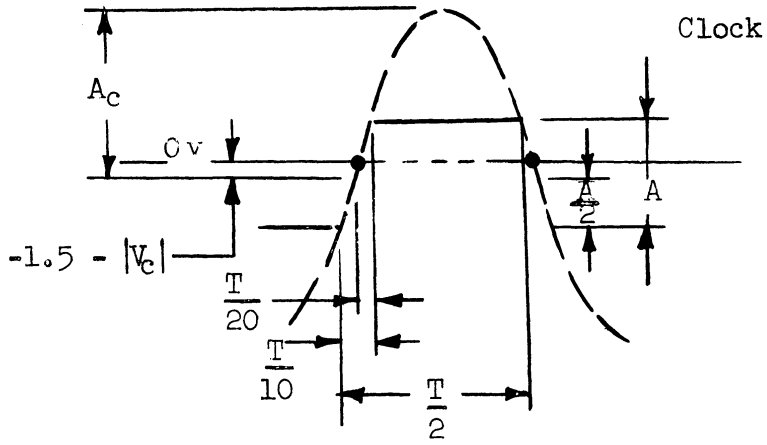
The introduction of a clock signal into the gate circuitry has the following additional features. Since a clocked system is always multiple phase, the first level logic (input "or") always reaches maximum amplitude prior to the clock-pulse-rise. Noise resulting from the reverse current of the pulsed "and" diodes is therefore completely eliminated because the pulsed "and" diodes have not experienced a forward current just prior to the pulse. The reason for this is that point (3) in the above figure has been pulled negative by the clock and has back biased the "and" diodes. The noise phenomenon is now a function of the static properties of the unpulsed "and" diode and the reverse transient current of the clock diode.

Noise at point (3), resulting from the addition of the static noise ($\Delta V_B + \Delta V_C$) and the back-transient noise of the clocked diode, is the factor limiting high-frequency gate operation. At present the tube and transformer have placed the upper limit for practical operation at about 7 Mc, thus making a legitimate test using high pulse-repetition rates impossible above 7 Mc.

To circumvent this frequency limitation a simulated gate has been used and operated at clock frequencies from 5 to 20 megacycles. The circuit is shown below.



The clock (the voltage source shown) is an electron-coupled oscillator, operating class C. The wave shape of the clock signal with reference to the signal pulses is important for effective gating. Notice in the figure below that the steepest portion of the sine wave or clock signal is used for wave-shaping. The information pulse is required to rise and fall to amplitude A in T/10 where T is the clock period.



The amplitude of the clock pulse is given by

$$A_c \sin \frac{2\pi}{20} = A/2$$

$$A_c = \frac{A}{2} \frac{1}{\sin 18^\circ}$$

$$A_c = 1.618A$$

The voltage about which the clock is centered is given by:

$$\text{Clock center voltage} = -1.5 - V_c + A/2$$

Taking the 10 Mc gate of Fig. 2.23 as an illustrative example, the clock centering voltage is:

$$V_c = .34 \text{ volt}$$

$$A = 3.5 \text{ volts}$$

$$\text{Clock centering} = -1.5 - .34 + 1.75 \text{ volts} = -.09 \text{ volt.}$$

There is little error in centering the clock voltage about ground as is done in the test circuit.

The amplitude of the clock is then given by:

$$A_c = 1.618A = 5.67 \text{ volts.} \quad (6.00 \text{ v used in test})$$

As the frequency of operation increases, the gate current I must increase to charge the circuit capacitance in the manner prescribed by Eq. 2.2 of Section 2.2. The circuit of Fig. 2.23 is taken as a typical 10 Mc gate and is used as the basis for the following formulation.

Let $I' = I + 4$ ma.

Then based on the conditions given above:

$$I = \frac{4}{5} f$$

f = clock frequency in Mc, and
I = gate current in ma.

Test results at 5 Mc (Fig. 2.4) show a noise voltage of .54 as compared to .55 volt (Fig. 2.25) for the unclocked case at 10 Mc. The clock diode has had a forward current history (8 ma) which is roughly equivalent to the sum of the forward currents of the 4 pulsed diodes of Fig. 2.25. It is anticipated then that the total resulting noise voltage will be equal for the two cases. The dynamic noise ϵ resulting from the back transient of the clock diode has been added to the computed static noise for the case where 4 or 5 inputs are pulsed. The data for the 295 show the dependence of total noise on diode static characteristics as the 2109 and 295 have equivalent back-transient properties with the 295 having inferior static characteristics.

Test results at 5 Mc (Fig. 2.26) show the noise at point (3) to be approximately equal to the static drop across the unpulsed diode if the information pulse leads the clock by T/10 seconds. It is still necessary that "and" diodes

have good reverse-transient characteristics but for a slightly different reason than in the unpulsed case. Consider a situation where none of the inputs has been pulsed. Each "and" diode will then send a surge of reverse current to point (3) at the termination of the clock pulse. Noise at any time during the clock cycle is objectionable. However, it is the back-transient properties of the clock diode that are particularly critical.

2.3.2.4 Experimentally Observed Correlation Between Static Characteristics and Back-Transient Properties.—The previous discussion has been concerned with diode characteristics; the forward conduction is measured statically and the back transients are measured dynamically. The back transient has been characterized by the amount of lost charge. It is known from manufacturing techniques that these characteristics are basically opposed. To obtain a high conduction, it is necessary to use either a large junction area or high impurity concentration. Both of these factors contribute heavily to diode reverse-current. Figure 2.21 indicates the relationship between conduction and the reverse transient lost charge. The dynamic forward resistance $\partial V_d/\partial I_f$ vs the lost charge (for I_f = 9 ma) has been plotted for those diodes which have been tested. It should be pointed out that the number of diodes constitutes a small sample and the diodes obtained tended to represent the best available products of the manufacturers contacted.

It is obvious that the most desirable diode is that one which comes closest to realizing ideal diode properties. However, due to the aforementioned qualities of commercially available diodes, it is evident that a choice must be made between good forward conduction and good transient properties. It is the opinion of the authors that it is necessary to have back-transient properties equivalent to those shown for the Hughes 2109, giving diode static characteristics secondary consideration. The Hughes 2109 represents the best compromise of the diodes tested to date.

2.4 Gate Structure Performance

In this section, the performance of two experimental packages is considered. The first is designed for 10 Mc operation and the second is an operational package for 5 Mc operation. The 10 Mc circuit of Fig. 2.23 has been tested on a single-pulse basis. Although a more complete test with a continuous chain of 50 mμsec and a clock would have been desirable, tube and transformer studies have shown operation at a 10 Mc repetition rate to be impractical. Figure 2.3 verifies the assumption that diode transients are unaltered by a 10 Mc pulse repetition rate. Therefore, the single-pulse test results are indicative of actual operation at 10 Mc.

A 5 Mc package (Fig. 2.24) has been tested under legitimate operating conditions. The specification of voltage and current magnitudes and a summary of

the gate performance is covered in the two succeeding sections. The remaining sections discuss the effect of tube grid characteristics upon the grid signal wave-shape and finally the upper limit of gate performance.

2.4.1 SPECIFICATION OF LEVELS AND CURRENTS

In this section the design specifications for a 10 Mc gate (Fig. 2.23) and 5 Mc gate (Fig. 2.24) are discussed.

(a) Currents - Fig. 2.23

A discussion of the input logic stage is dependent upon the tube-transformer configuration only to the extent that the bias levels and grid capacitance must be known. In this particular example, a grid swing of 1 volt and an effective total grid capacitance of 30 μμf has been used as the basis of computation. Assuming a value of 5 μμf for C_1, the gate current I can be compuated from Eq. (2.2) of Section 2.2.

$$I = \frac{(E_g + E_N)C}{\Delta t} + \frac{E_g C_g}{\Delta t} + I_3 \quad ,$$

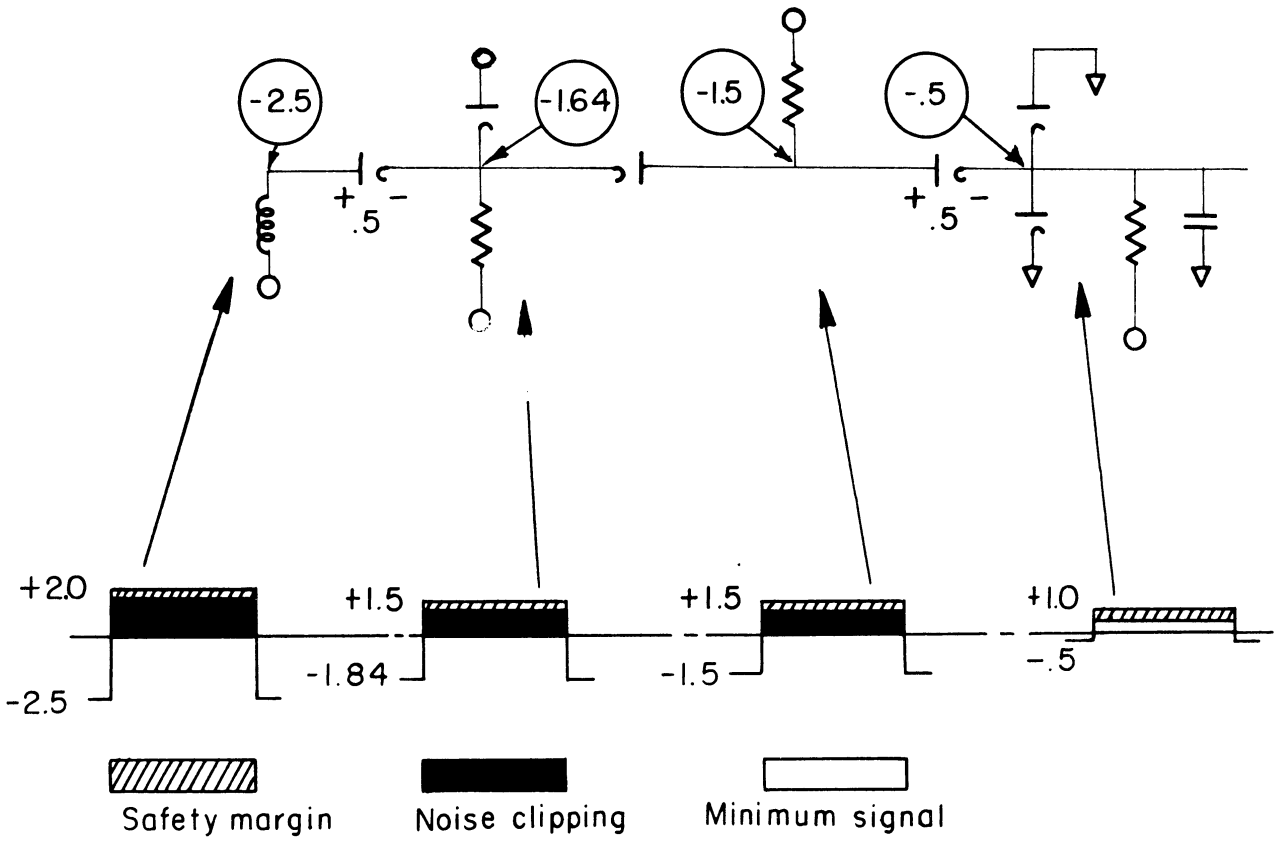
where

E_g = grid swing = 1 volt,
E_N = noise clipping = 1 volt,
C_g = 30 μμf,
C_1 = 5 μμf,
$I_3 = \frac{E_g C_g}{\Delta t}$ = grid pull-down resistor current, and
$\Delta t = \frac{T}{10}$ = 10 mμsec;
I = 7 ma.

An estimate of the average current lost in the grid clamp diode may be made from Fig. 2.20 (about 1 ma). Therefore, to insure sufficient current to swing the grid, 8 ma has been used. An input gate current of 12 ma has been found satisfactory.

Levels: Fig. 2.23

If "and" diode limiting is to be avoided, the level at which "and" limiting would take place must be greater than the grid level by some factor of safety. Since the drop across the "or" diodes can be expected to be from .4 to .5 volt, the minimum amplitude of the gate input E_o can be established. To insure no "and" limiting of the grid signal, a .5 volt safety factor is assumed. The following sketch shows the composition of the information pulse at the various points in the circuit. The noise clipping levels on the input and grid "or"



diodes can be increased or decreased as justified by environmental tests. The levels shown have been found satisfactory in the work to date.

(b) Currents - Fig. 2.24

Figure 2.24 is illustrative of gate performance at 5 Mc. The 436A requires a grid swing of -2.0 to 2.0 for optimum tube-transformer performance. The effective grid input capacitance is 20 μμf. The gate current I is given by:

E_g = 4 volts
E_N = 2 volts
C_g = 20 μμf
C = 5 μμf

$$I_3 = \frac{E_g C_g}{\Delta t} = \text{grid pull-down resistance current}$$

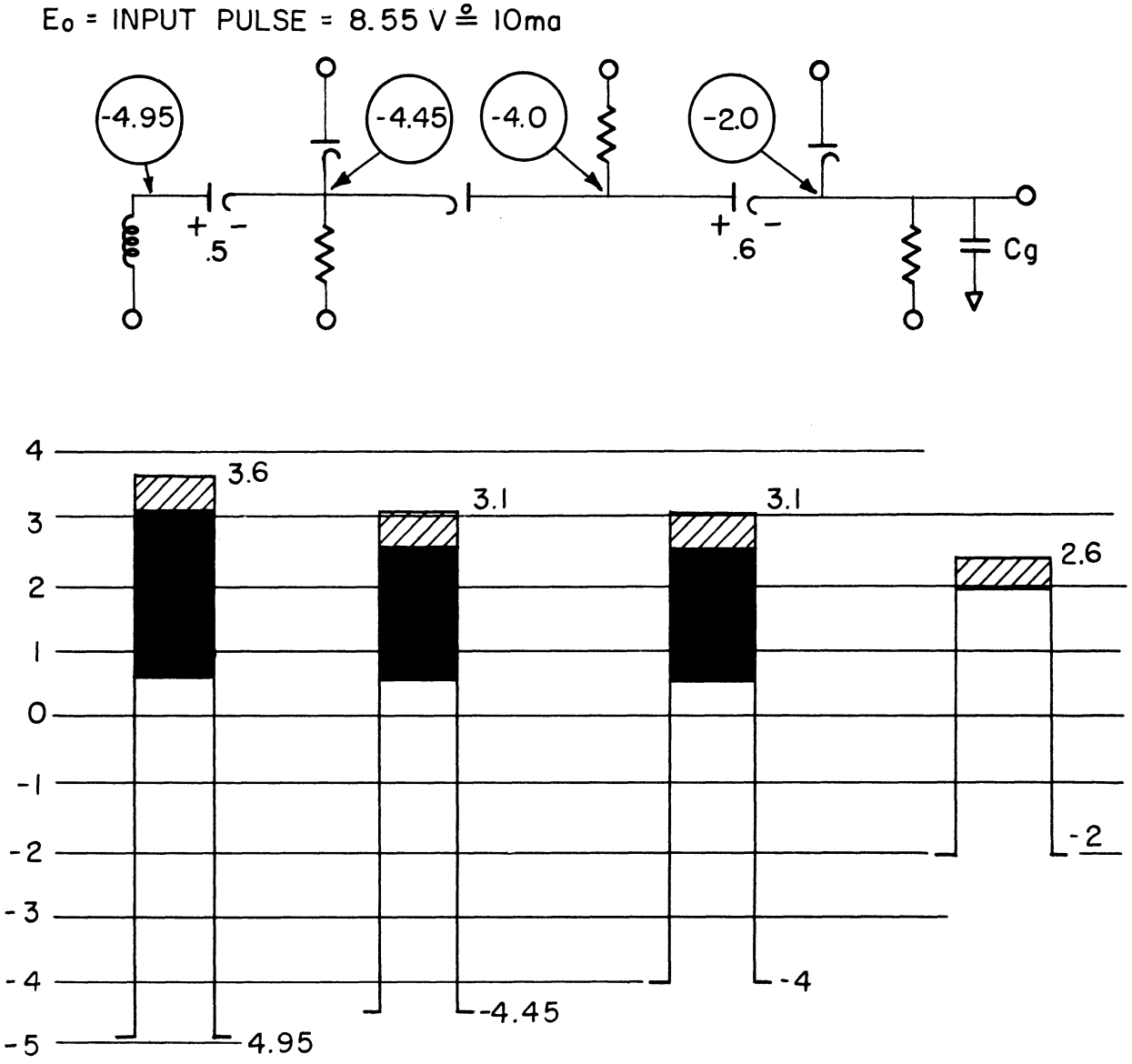
$$\Delta t = \frac{T}{10} \quad 20 \text{ μsec}$$

$$I = \frac{(E_g + E_N)C}{\Delta t} + \frac{E_g C_g}{\Delta t} + I_3$$

I = 9.5 ≐ 10 ma
I' = 14 ma

Levels: Fig. 2.24

Notice that a grid-clip diode has not been included; the 436A grid is an effective clip as the grid characteristics limit the signal at the desired level (+ 2.0 volts). It is therefore necessary that "and" diode limiting below + 2.0 be avoided. The noise clipping levels indicated are conservative and may later be reduced.



2.4.2 GATE PERFORMANCE

In this section the performance of a 10 Mc gate (Fig. 2.25) and a 5 Mc gate (Fig. 2.26) is discussed. It is desirable to assign a figure of merit or efficiency to a circuit. Let gate efficiency E be defined as the product of current efficiency A and voltage efficiency B.

$$E = \frac{A\,B}{100}\,\%$$

$$B = \frac{E_g}{E_o} \times 100 = \text{voltage efficiency}$$

$$A = \frac{I/2}{I''} \times 100 = \text{current efficiency}$$

$$I'' = I' + I_B \text{ (Diode B)}$$

The voltage efficiency B is the ratio of the grid swing E_g to the amplitude of the input signal required for satisfactory gate operation. The current efficiency A is defined as the ratio of current required to charge the grid capacitance C_g to the gate current necessary to drive one "and" input. The current needed to drive a gate is the "and" pull-down current I' plus the reverse current of the input clamp diode.

Figure 2.23

Computation of Gate Efficiency.

$E_o = 4.5$ volts
$E_g = 1$ volt
$I = 8$ ma
$I'' = I' + I_{B(\text{average})} = 12 + 2 = 14$ ma
Then $A = 22.2\%$
$B = 33.3\%$
$E = 7.4\%$

The term gate efficiency should be used with caution, as the same gate with different values of grid swing and capacitance will have a different efficiency. For example, consider the same circuit with a grid swing of 2 volts.

$E_o = 5.5$ volts
$E_g = 2$ volts
$I = 16$ ma
$I'' = I' + I_B = 20 + 3 = 23$ ma
Then $A = 36.4\%$
$B = 34.8\%$
$E = 12.65\%$

Gate efficiency is improved by decreasing grid capacitance, noise clipping, and the input current I".

Wave Shapes.

The first four photographs in Fig. 2.25 show the wave shape of the signal as it progresses through the unclocked package when all inputs are pulsed. The delay (4 mμsec) of the pulse from the input to the "and" [point (2)] to the grid [point (4)] is shown in the next photograph. The time delay is due to the finite time required to charge the circuit capacitance. The noise resulting at the "and" output [point (3)] when different combinations of "and" inputs are pulsed is shown in the last four photographs. The negative undershoot at the termination of the noise is primarily the result of the back transient from the input "or" diode. A high conduction "or" has been used to minimize the drop across the input "or" diode with little regard given to its transient properties. It is felt that the resulting negative undershoot is not objectionable and therefore the relatively poor back-transient properties of this diode can be tolerated. The effect of small variations of the input-pulse amplitude E_o and the gate current I on the noise is shown in Table 2.3. It is observed that the total noise is only slightly affected by an increase of E_o and I.

Figure 2.24

Computation of Gate Efficiency.

E_o = 9.0 volts
E_g = 4.0 volts
I = 10 ma
I" = I' + $I_{B(average)}$ = 14 + 2 = 16 ma
A = 31.3%
B = 44.5%
E = 13.8%

Wave Shapes.

Typical pulse wave-shapes and levels are shown in Fig. 2.26. The events indicated in the time sequence can be quickly summarized as follows:

(1) The output of the previous package (No. 2) arrives before the clock (No. 1) by 20 mμsec.

(2) If all inputs are pulsed, point (3) rises with the clock and falls with the earliest input (No. 4). The negative swing results from the back transient of the input "or" diodes. A CTP309 has been used as the input "or" diode for its high conduction property (despite its poor back-transient characteristics). If the undershoot is undesirable, the CTP309 diode can be replaced with a Hughes 2109. The portion "A" of (No. 4) is the level of point (3) when the clock is positive and none of the "and" diodes is pulsed.

(3) The grid signal (No. 6) rises with point (3) (a slight delay results from the 2 volts of noise clipping) and falls when the clock pulls the regenerative gate down. Notice that the grid signal did not reach + 2.0 volts because point (3) was about +1 volt during the latter portion of the pulse. "And" limiting has taken place, thus emphasizing the importance of the trailing edge of the input pulse.

(4) When point (3) falls, the "and" gate grid "or" diode experiences a back transient which pulls the grid signal slightly negative despite the effort of the regenerative gate to hold the grid up (No. 6). The back transient of an "or" diode at this time is particularly undesirable. Therefore, the 309 diode was dropped in favor of the Hughes 2109 for use as the grid "or" diode.

The delay δ' from the grid to output is 28 mμsec. This may be reduced by approximately 10 mμsec, if the grid is driven to +2.0 volts. The package delay δ measured under this condition is 34 mμsec. All measurements were taken with a Tektronix 545.

The noise indicated in No. 9 has been obtained using Hughes 2109 diodes of the quality shown in Table 2.1 (I_{BO} = 1 ma). A recent order of one hundred 2109's has the following distribution of initial back currents:

I_{BO} (ma)	1	2	3	4	5	6
Number of Diodes	8	37	37	13	5	0

at I_f = 9 ma
E_B = 1.5 volts.

The diodes used for tests in this report have been taken from the initial shipment of 2109's received. An increase in noise of about 1.0 to 1.3 volts can be expected with inferior 2109's. It is essential that all "and" diodes and grid "or" diodes be tested with a circuit of the type used in Table 2.1 before use in a package if the noise level is to be maintained at .5 to .8 volt.

2.4.3 EFFECT OF GRID CURRENT ON GRID WAVE-SHAPE

Under certain operating conditions, the tube grid can be used to clamp the grid signal. This can be brought about by driving the grid positive and drawing grid current. For example, the cascoded 437A's of Fig. 2.25 will clip the grid signal at +2 volts, thus eliminating the need for Diode F if it were desirable to push the grid that much positive. In Fig. 2.24 the grid-clip diode has been elimated as the clip function is performed by grid to cathode "diode" of the 436A. In any case, the gate current lost to the tube grid should be considered. In this particular case, if the grid is swung from -1/2 to +1/2 volts, the grid characteristics will contribute to the clipping action. However, for a

grid swing of -1/2 to +1/2 volt, grid characteristics have no effect on the grid wave-shape.

2.4.4 UPPER LIMIT OF PERFORMANCE

Preliminary results indicated that the tube-transformer combination and/or delay lines would be the factors limiting high-speed operation. Therefore, it was deemed desirable to divorce the input logic stage from the remainder of the package and outline those factors that would limit the operation of the input circuitry. Gate performance is directly related to the diodes employed and therefore any remarks must be necessarily restricted to current diode development. The factors limiting gate operation are (a) noise and (b) input gate current I".

In Section 2.2.3 noise was measured as a function of clock frequency. It was assumed that the grid swing and noise clipping level was maintained constant as frequency of operation was increased. That is, the gate current doubled for an increase in frequency by a factor of two. The above assumptions are unrealistic for two reasons. (1) The noise clipping levels must increase as the frequency (gate current) increases due to the increased reverse current of the gate diodes, and (2) the grid swing will not necessarily remain constant. Both of these factors will result in larger gate currents than have been assumed here. It is difficult, however, to anticipate the contribution of these factors from data taken at 10 Mc. Therefore, the data in Fig. 2.22 represent the lower limit of noise voltage, since it has been assumed that the grid swing and the noise clip level remained at 1 volt for all frequencies.

Gate noise has been measured under two conditions at 10 Mc. In Section 2.3.2.2 (unclocked) the source of dynamic noise was the reverse current of the pulsed "and" diodes. In Section 2.3.2.3 (clocked) the dynamic noise was the result of the clock diode reverse-transient. The noise as a function of clock frequency has been replotted in Fig. 2.22.

It is possible to compute total gate noise from a knowledge of the diode static characteristics and measurements of the initial back current as a function of forward current. This has been done for the unclocked gate using Hughes 2109 diodes. The instantaneous input-clamp current i_b and unpulsed "and" current i_c have been derived from the following equations. The total noise has been computed from the static curves for the 2109 by the method that was used for Fig. 2.4.

If the 10 Mc gate is taken as a basis for computation, an equation relating gate current to clock frequency can be written [Eq. (2.4)]. Assuming a five input "and" gate with 4 of 5 inputs pulsed, the normal steady-state current through any "and" diode is given by Eq.(2.5).

$$I = \frac{4}{5} f\ ma \qquad (2.4)$$

f = clock frequency in Mc

$$I_f = \frac{I}{5} \tag{2.5}$$

An equation relating I_{BO} to the forward current can be obtained from Fig. 2.15 Eq. 2.6) . Substituting Eq.(2.5) in (2.6), I_{BO} as a function of gate current I is given by Eq.(2.7). The initial current to the unpulsed "and" diode is given by Eq. (2.8).

$$I_{BO} = .18\, I_f + .24 \text{ ma} \tag{2.6}$$

$$I_{BO} = .036\, I + .24 \text{ ma} \tag{2.7}$$

$$i_c = I + (m - 1)\, I_{BO} \qquad m = 5$$

$$i_c = 1.144\, I + .96 \text{ ma} \quad . \tag{2.8}$$

Let I' = I + 6 ma. A 6 ma minimum clamp current is much larger than is necessary for low frequency operation but it is necessary to avoid input clamp cut-off at 40 Mc. The current through the unpulsed input clamp is given by Eq. (2.9). A comparison of the computed results with the experimental noise measurement at 10 Mc (Fig. 2.25) shows that .1 volt should be added to the computed values to adjust the experimental results to computed data. The normalized results are plotted in Fig. 2.27.

$$i_b = I' - i_c$$

$$i_b = 5.04 - .144\, I \quad . \tag{2.9}$$

The magnitude of the input gate current is a factor which will set a practical limit on the frequency of operation. For example, the input current to a pulsed "and" gate input at 40 Mc is equal to 38 ma plus the reverse current lost to the back-biased input clamp and pulsed "and" diode. In practice, it will be the restricted number of gate drives that will limit the frequency of operation rather than gate noise resulting from diode transients.

2.5 Summary

The speed of operation of a diode logic circuit is limited by the amount of noise which can be tolerated in the circuit and the magnitude of current required per gate input. As frequency of operation is increased, all gate currents must necessarily increase if a given grid swing is to be maintained. It is the increased gate current that is primarily responsible for the decadent performance as frequency is increased.

Noise has been shown to be the result of diode reverse-transient currents and the static characteristics of the unpulsed input clamp and "and" diodes. The reverse-transient properties have been given priority over the static characteristics. It is true that the static characteristics of the unpulsed "and" diode contribute to the static noise, but this additional .2 to .3 volt of noise is a small price to pay for a diode with really good back-transient properties. The crux of the diode specification has been to obtain the best possible forward conduction without sacrificing back-transient properties.

Not only are the reverse transients important for the reduction of noise but also the reverse current of the input clamp, "and" diodes, and grid-clamp diodes represent a charge loss not present in the gate using ideal diodes. The reverse transients of two diodes, the clock diode and the "or" diodes on the tube grid, are particularly critical. The forward transients have been shown to be negligible by comparison to the reverse transient. It is recommended that all diodes be checked for forward conduction and back-transient properties before use in the gate circuit. Of the diodes tested, the Hughes 2109 represented the best compromise of diode characteristics.

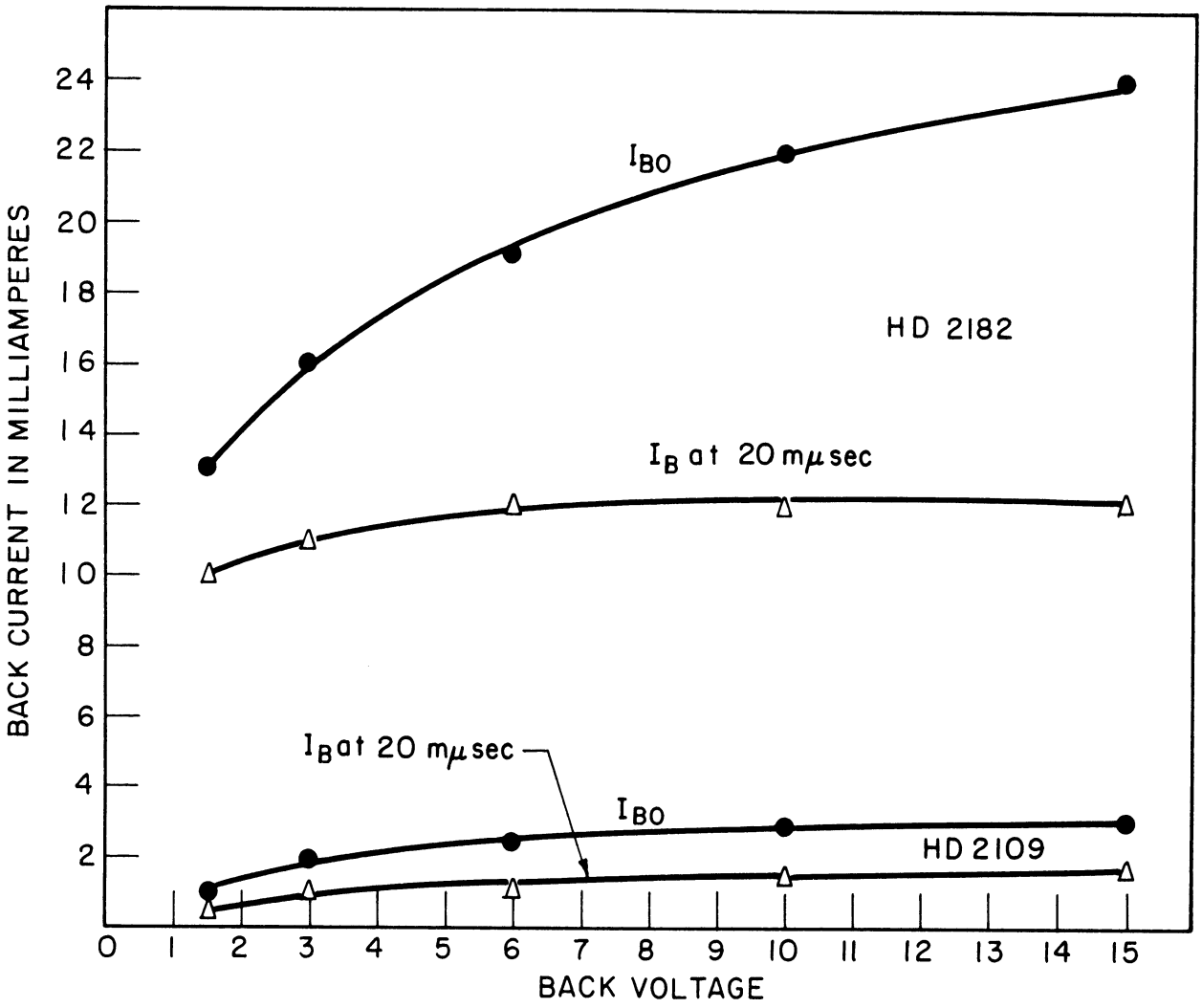
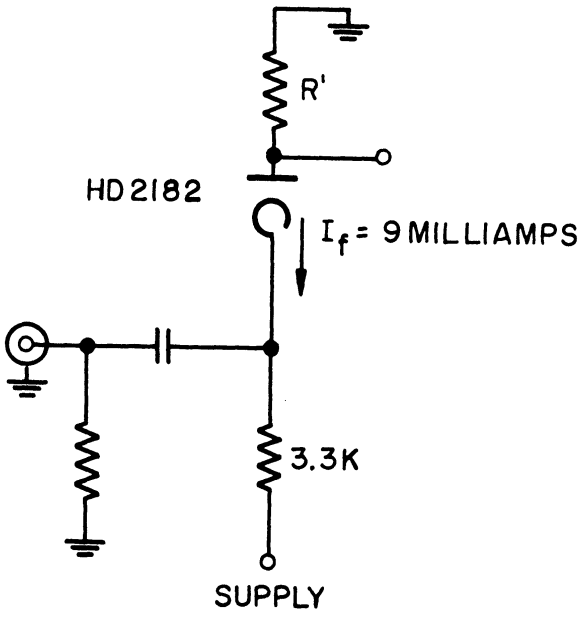
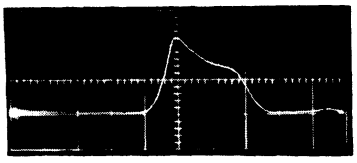
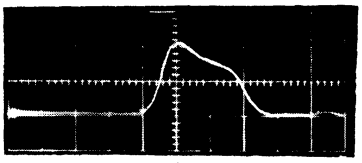


Fig. 2.1. Effect of back bias on back recovery.

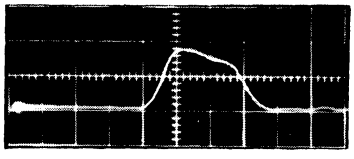




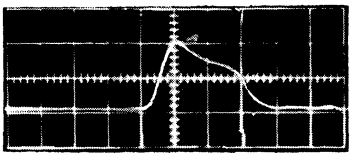
R' = 50 Ω
E_b = -1.5 v



R' = 100 Ω
E_b = -1.5 v



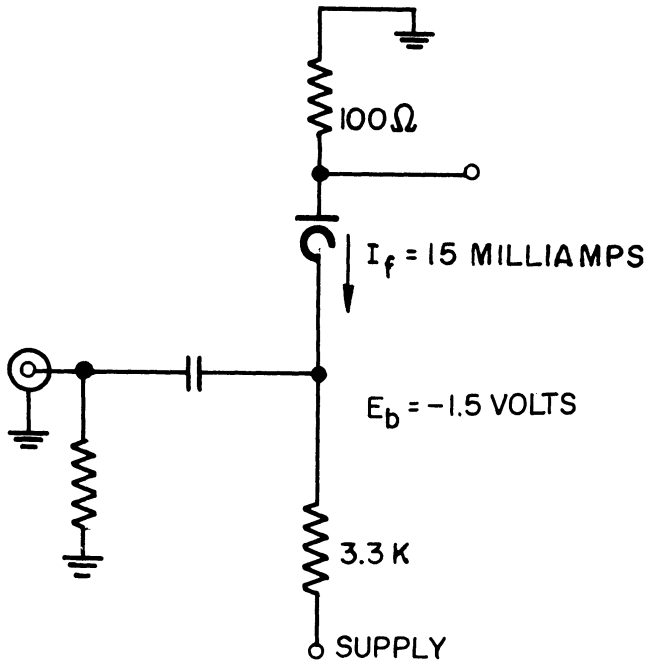
R' = 200 Ω
E_b = -1.5 v

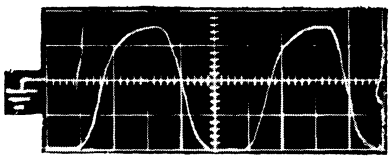


R' = 200 Ω
E_b = -4.0 v

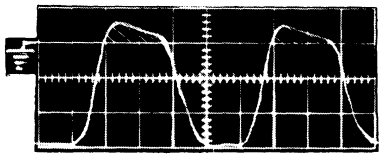
Current = 10 ma/div
Time = .02 μsec/div

Fig. 2.2. Effect of circuit series resistance R' on back recovery.

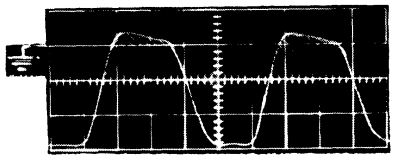




Input voltage
1 v/div
.02 μsec/div

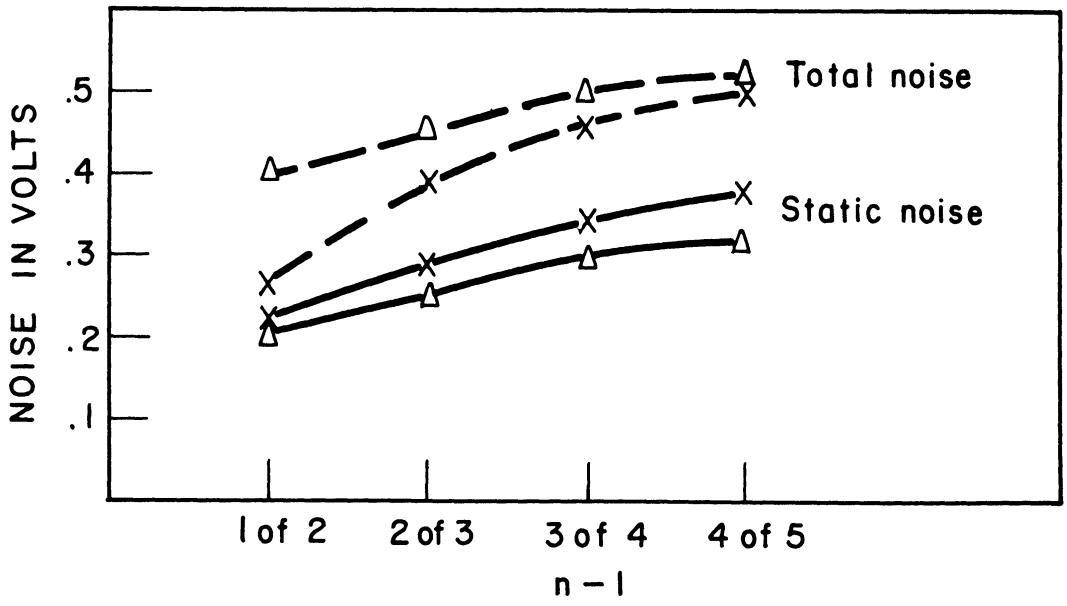


HD 2109
5 ma/div
.02 μsec/div



Ray 295
5 ma/div
.02 μsec/div

Fig. 2.3. Back recovery at a 10 Mc repetition rate.



Circuit: see Fig. 2.23
Specifications: I = 8 ma
I' = 12 ma
Symbols: Δ = actual case
X = computed case

Fig. 2.4. Noise as a function of the number of gates pulsed.

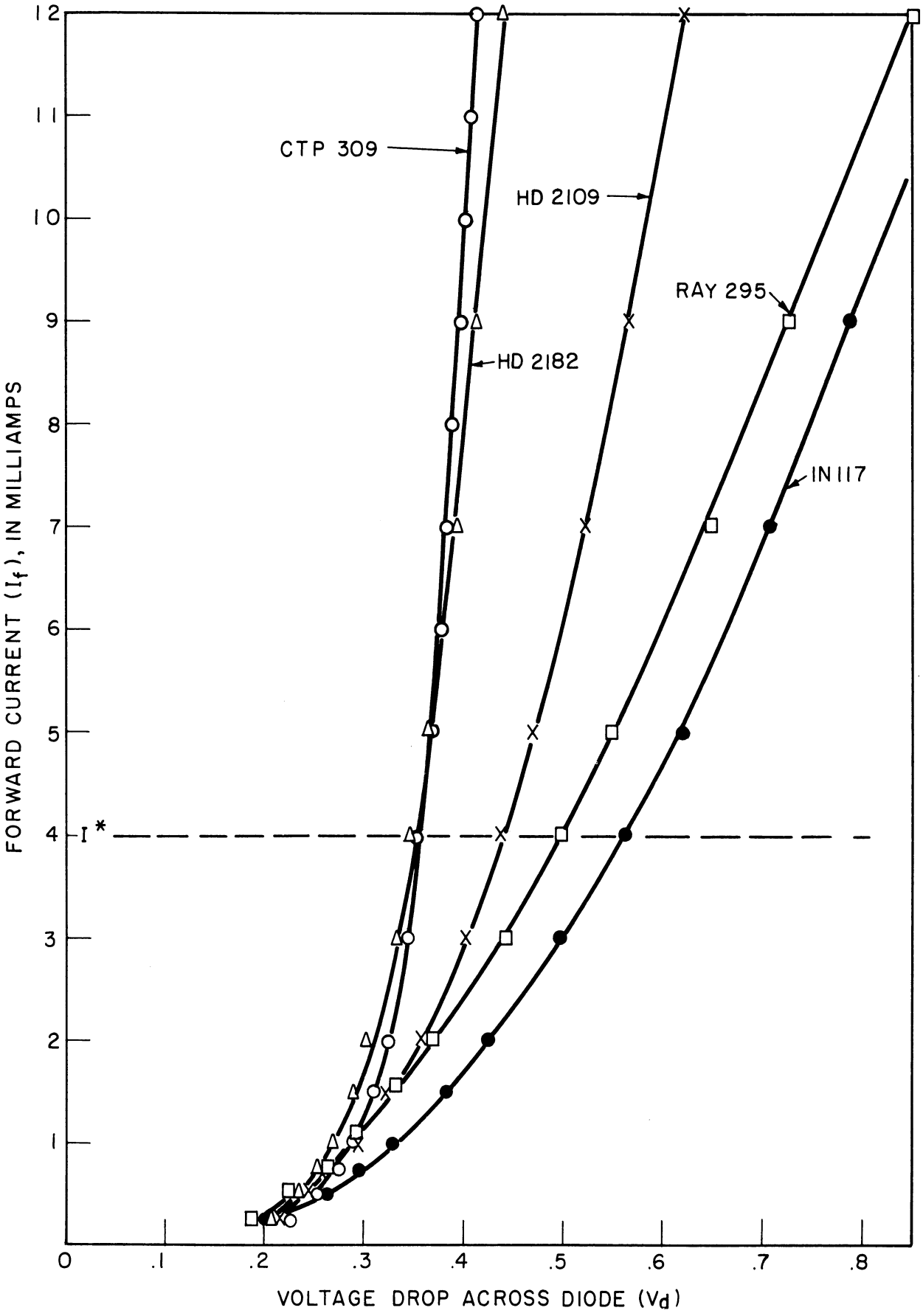


Fig. 2.5. Static characteristics of representative diodes.

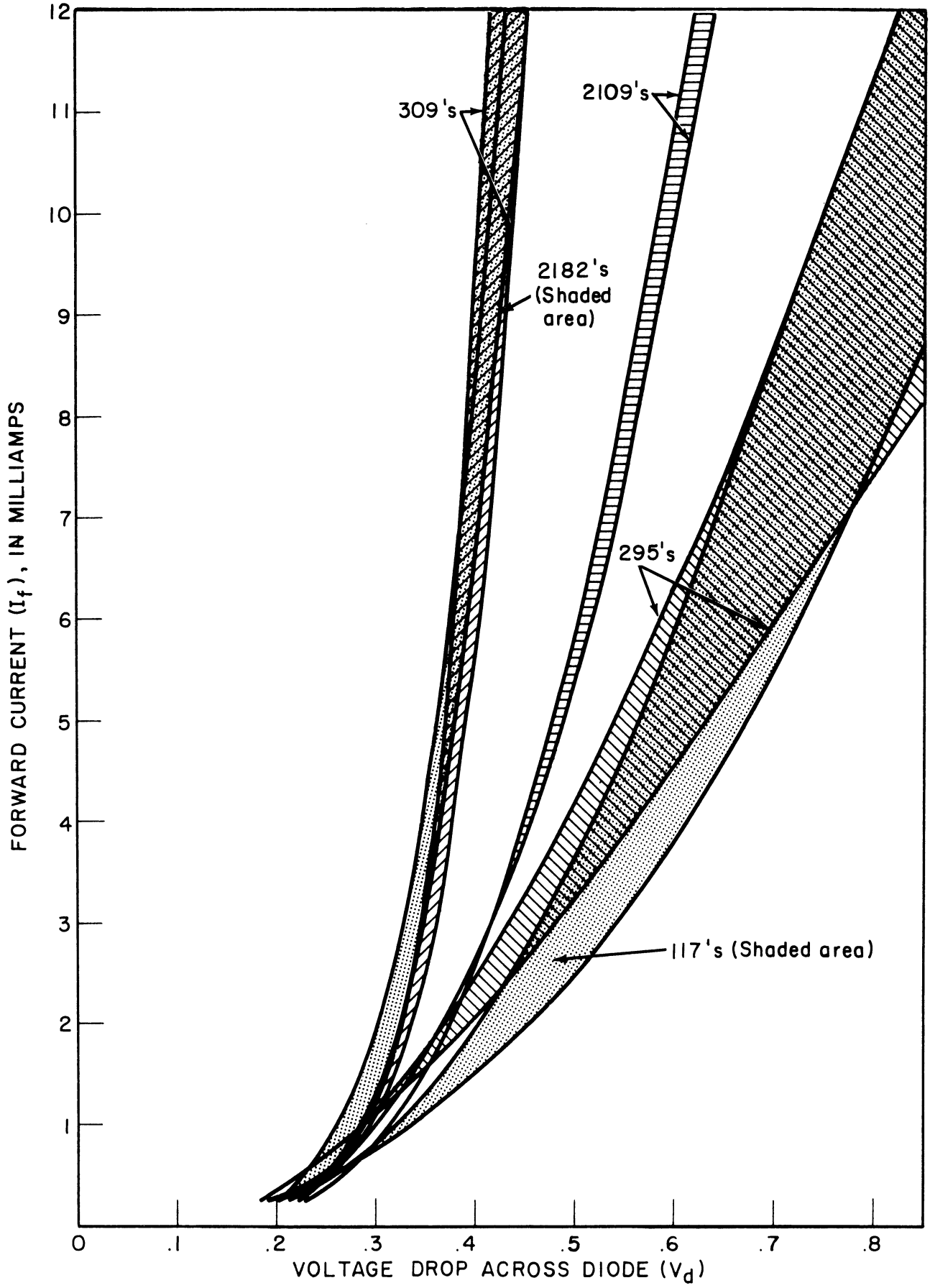


Fig. 2.6. Deviation of static characteristics.

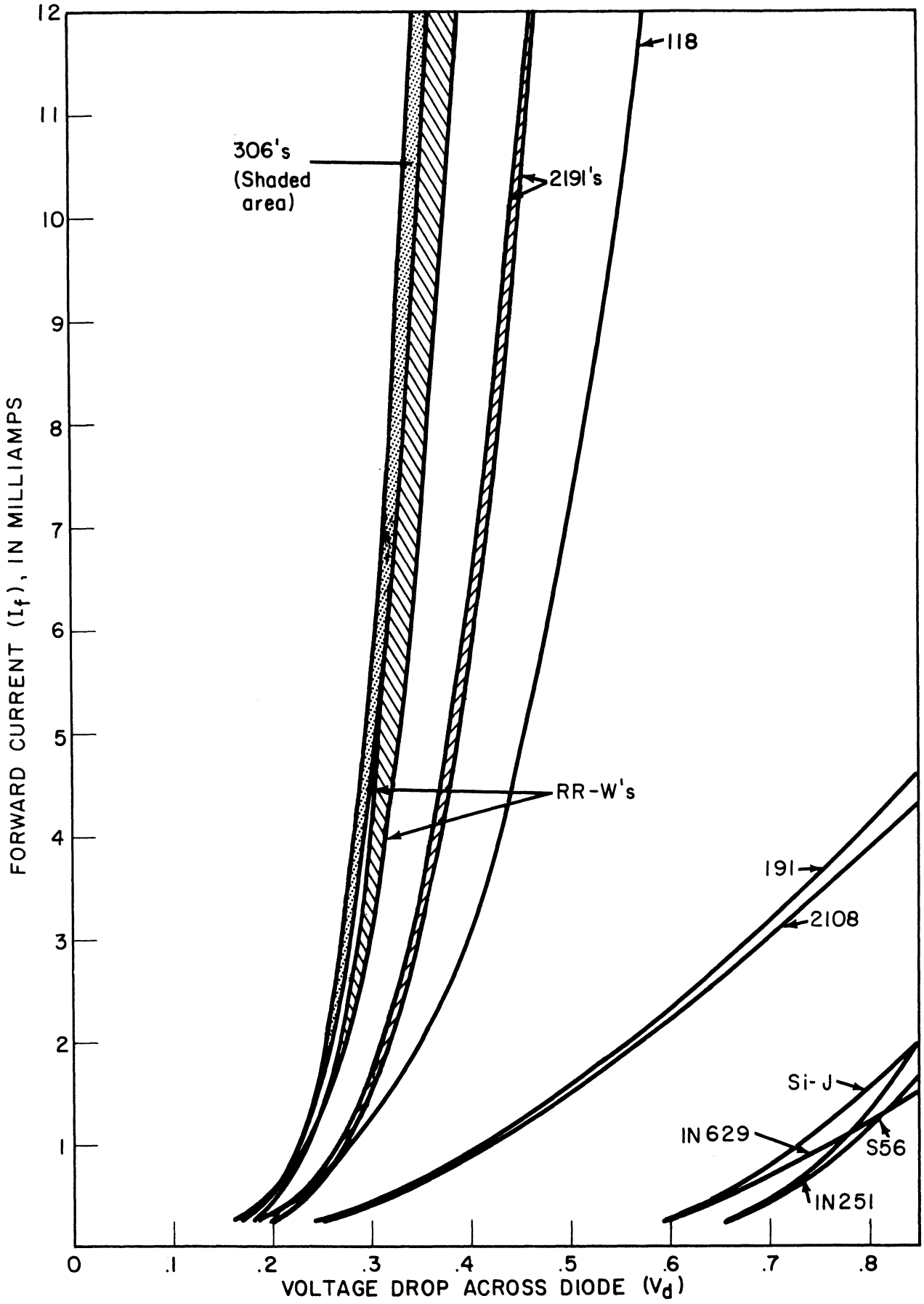
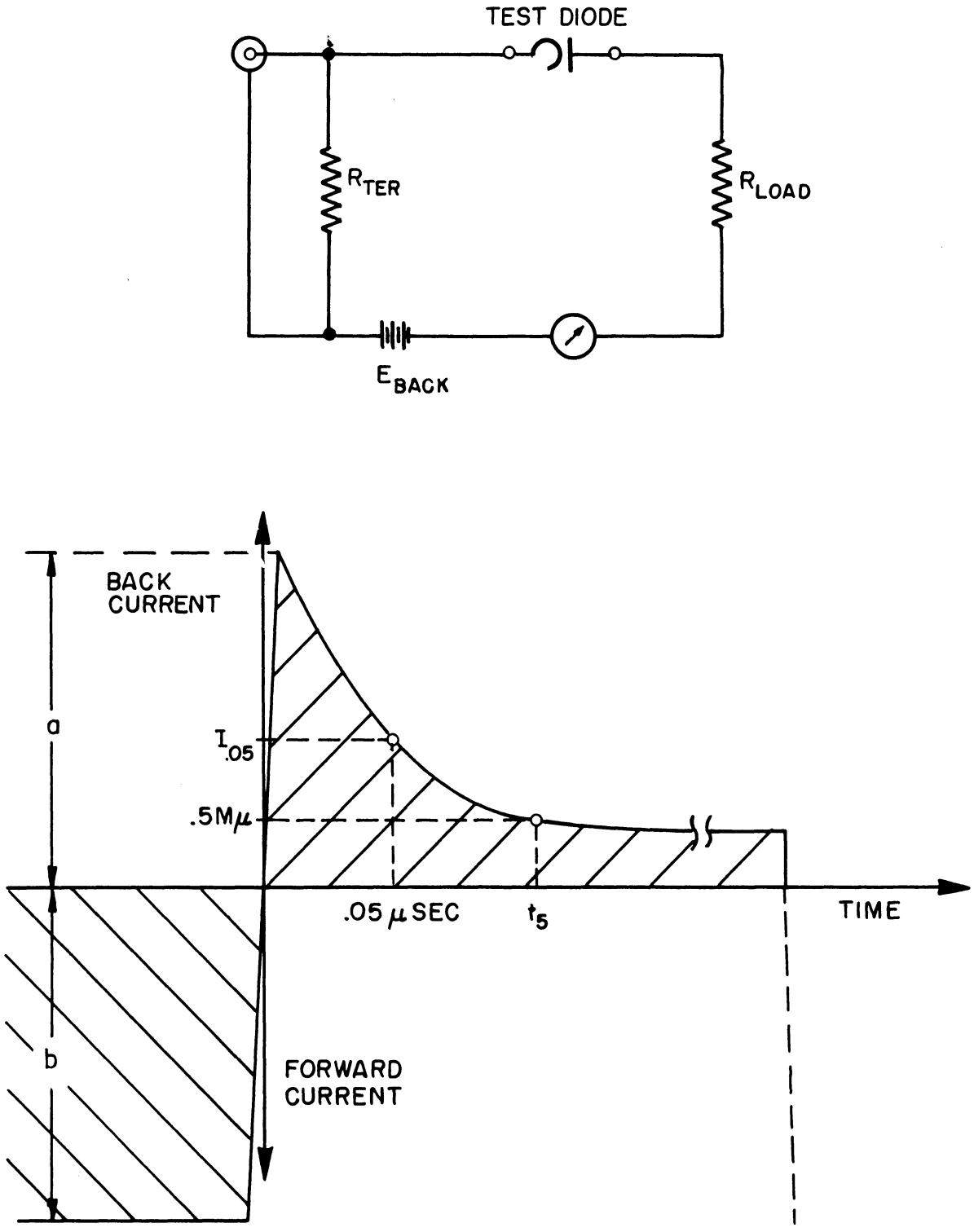


Fig. 2.7. Static characteristics of additional diodes tested.



Forward and reverse current at R_{load}

Fig. 2.8. Back transient test circuit at 25 Kc.

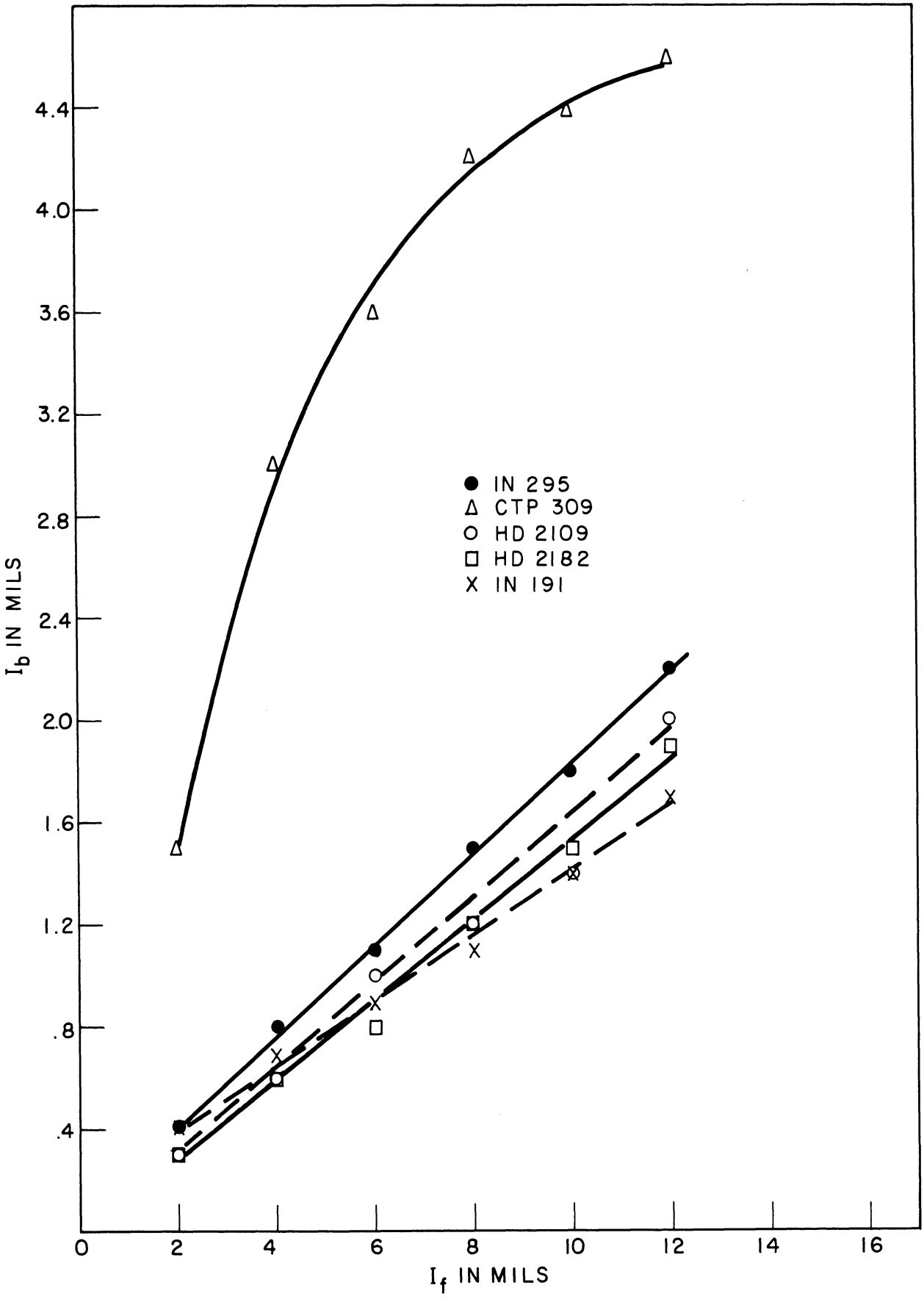


Fig. 2.9. Current at t = .05 μsec vs forward current, E_b = -1.5 v.

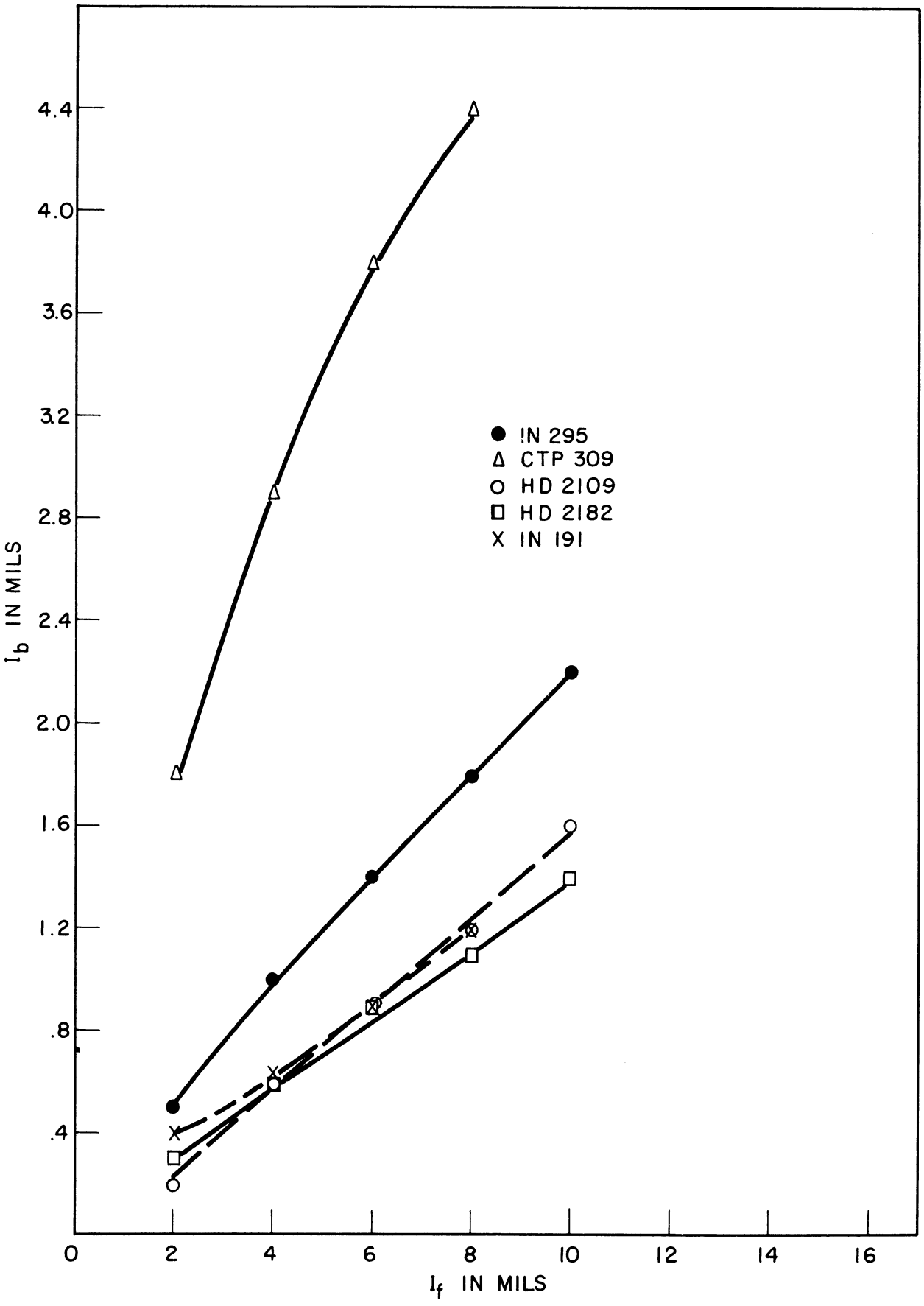


Fig. 2.10. Current at t = .05 μsec vs forward current, E_b = -3.0 v.

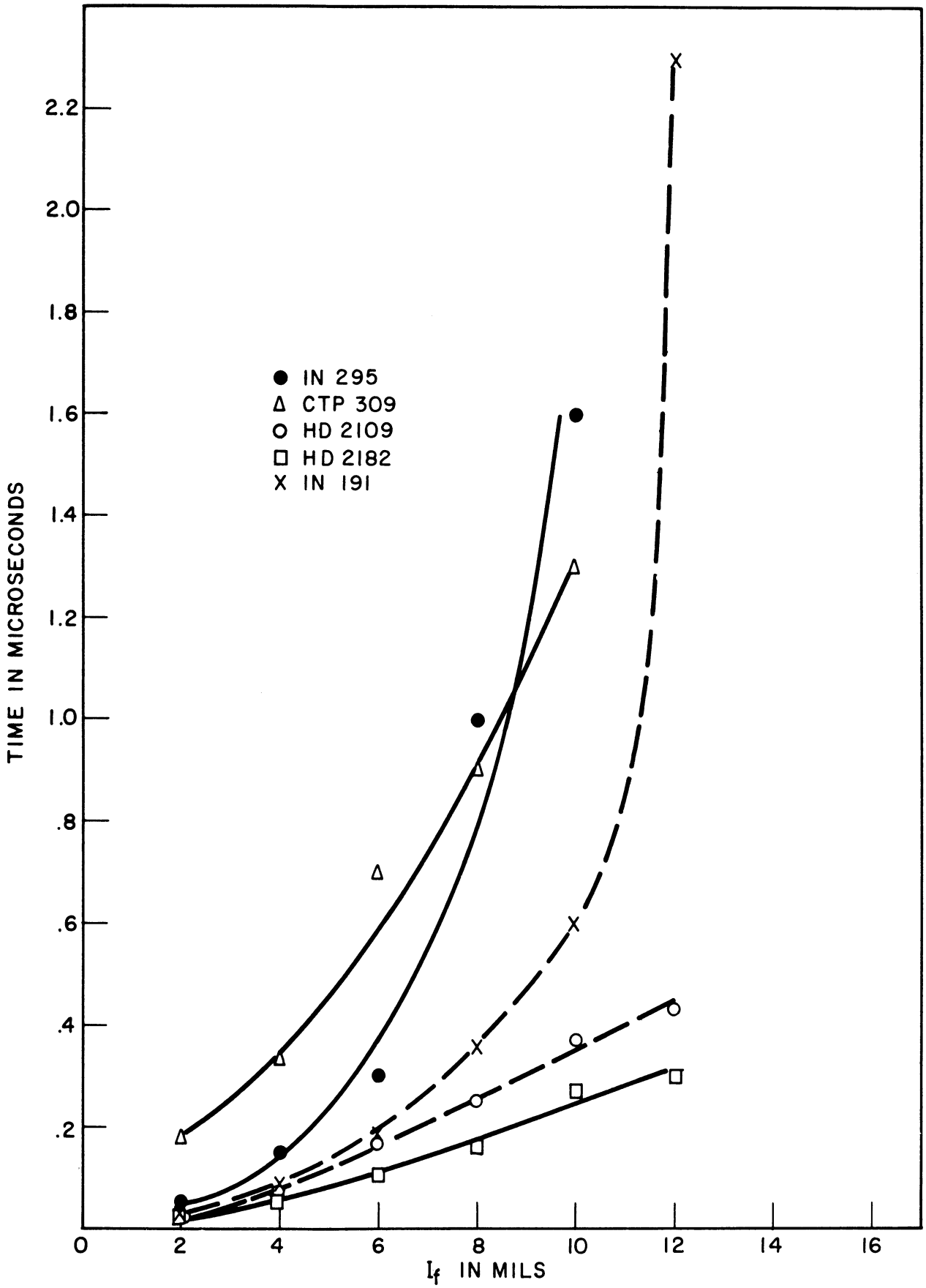


Fig. 2.11. Time at I_b = .5 mil vs forward current, E_b = -1.5 v.

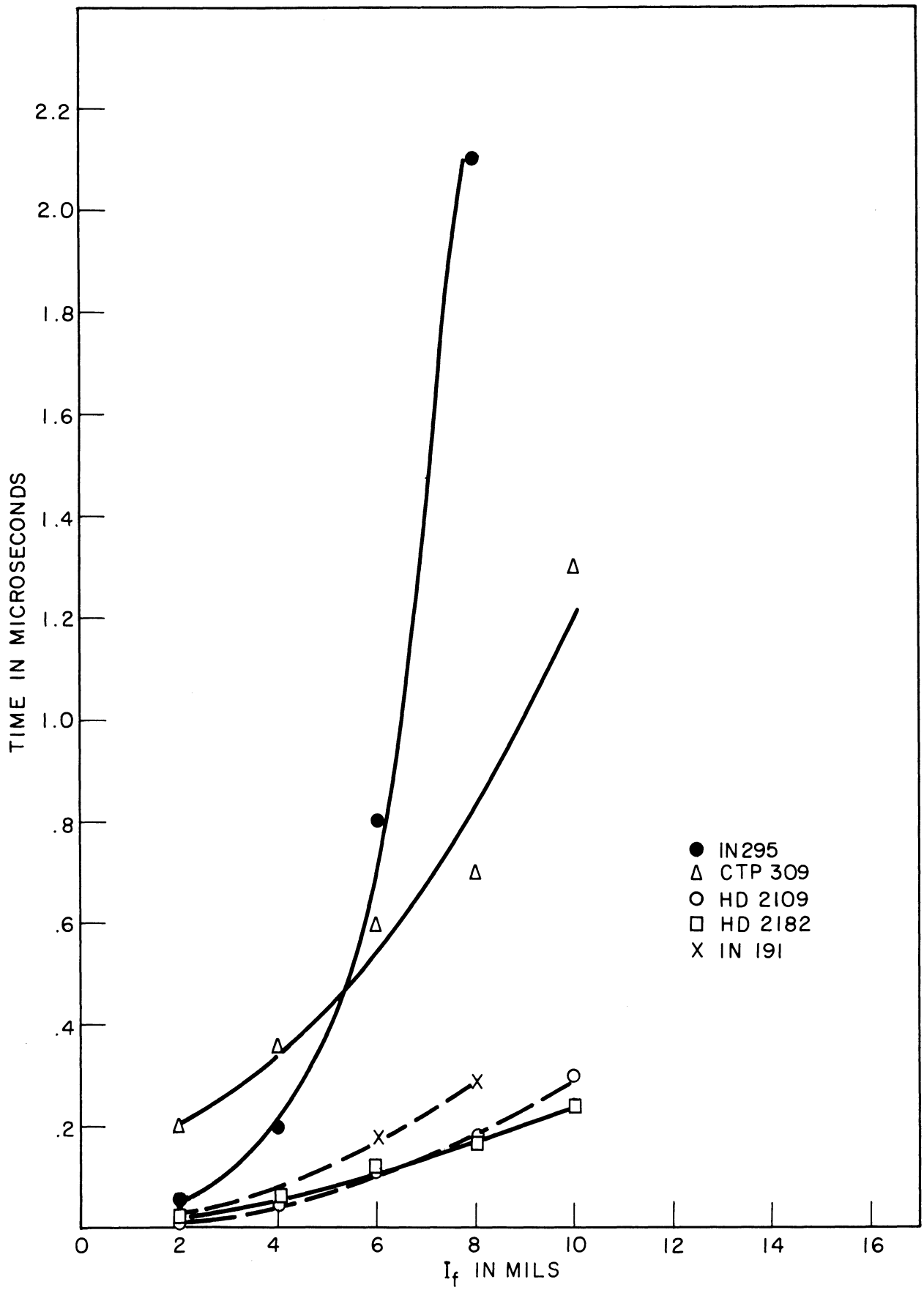


Fig. 2.12. Time at I_b = .5 mil vs forward current, E_b = -3.0 v.

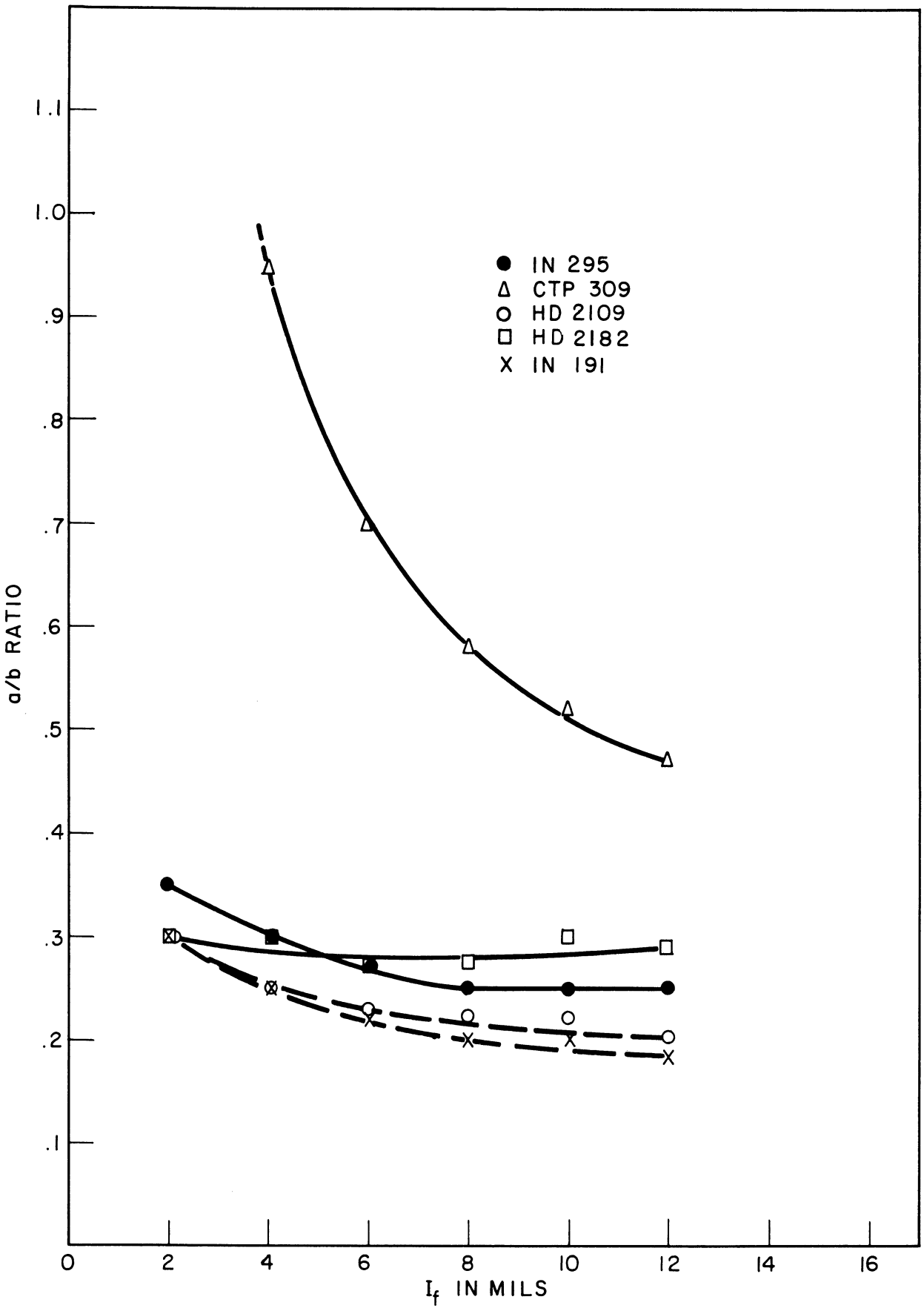


Fig. 2.13. a/b ratio vs forward current, E_b = -1.5 v.

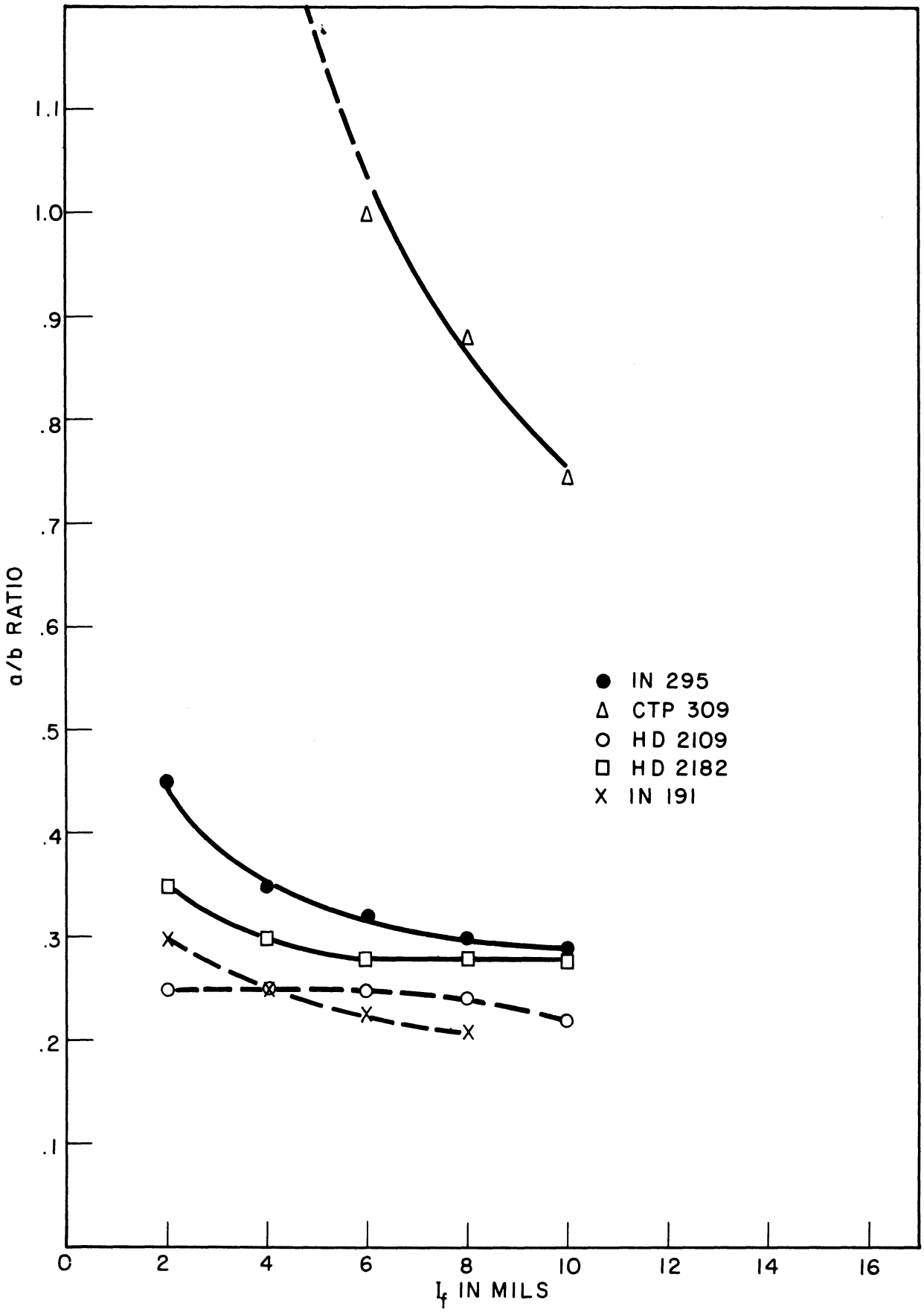


Fig. 2.14. a/b ratio vs forward current, E_b = -3.0 v.

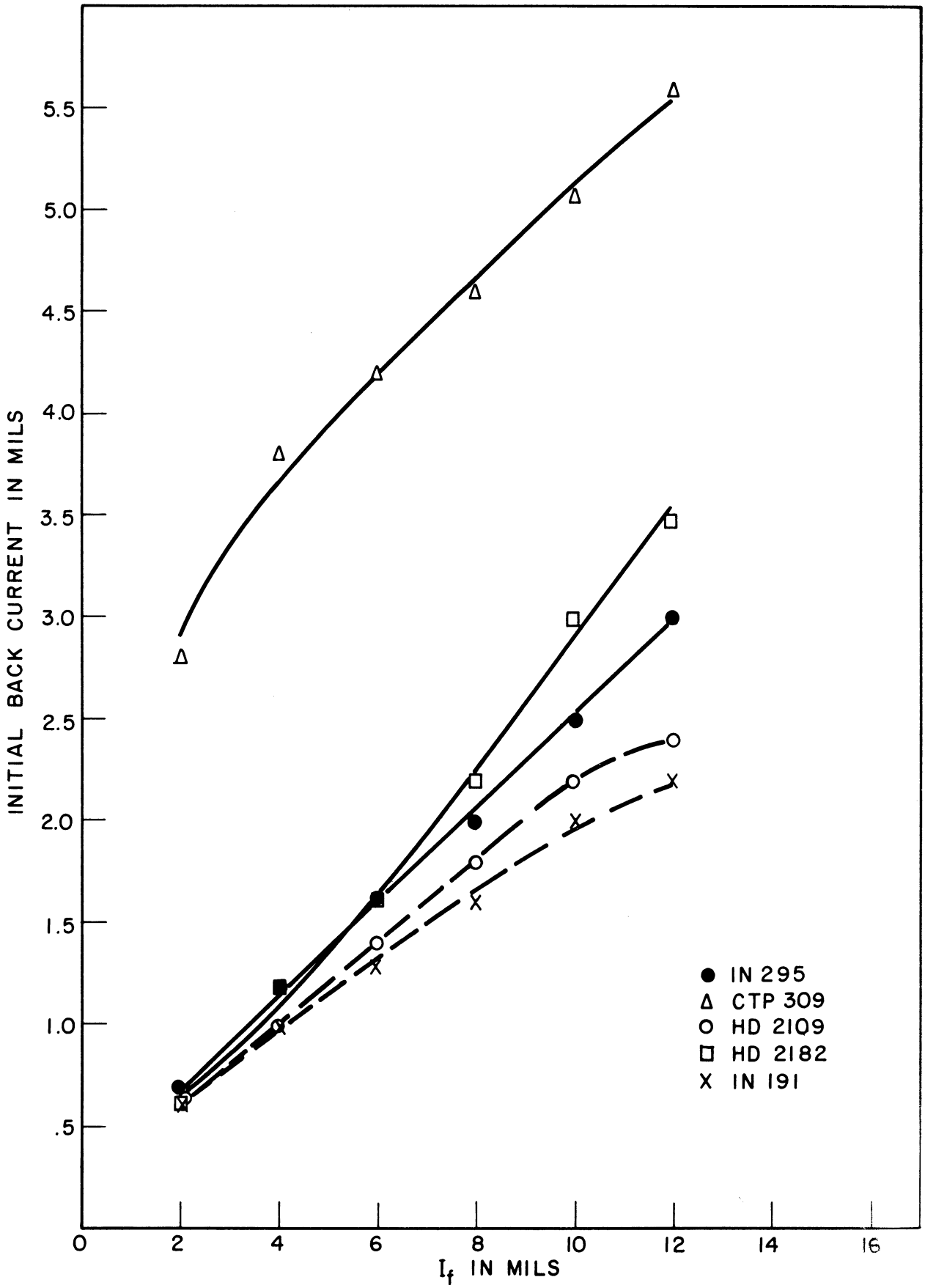


Fig. 2.15. Initial back current vs forward current, E_b = -1.5 v.

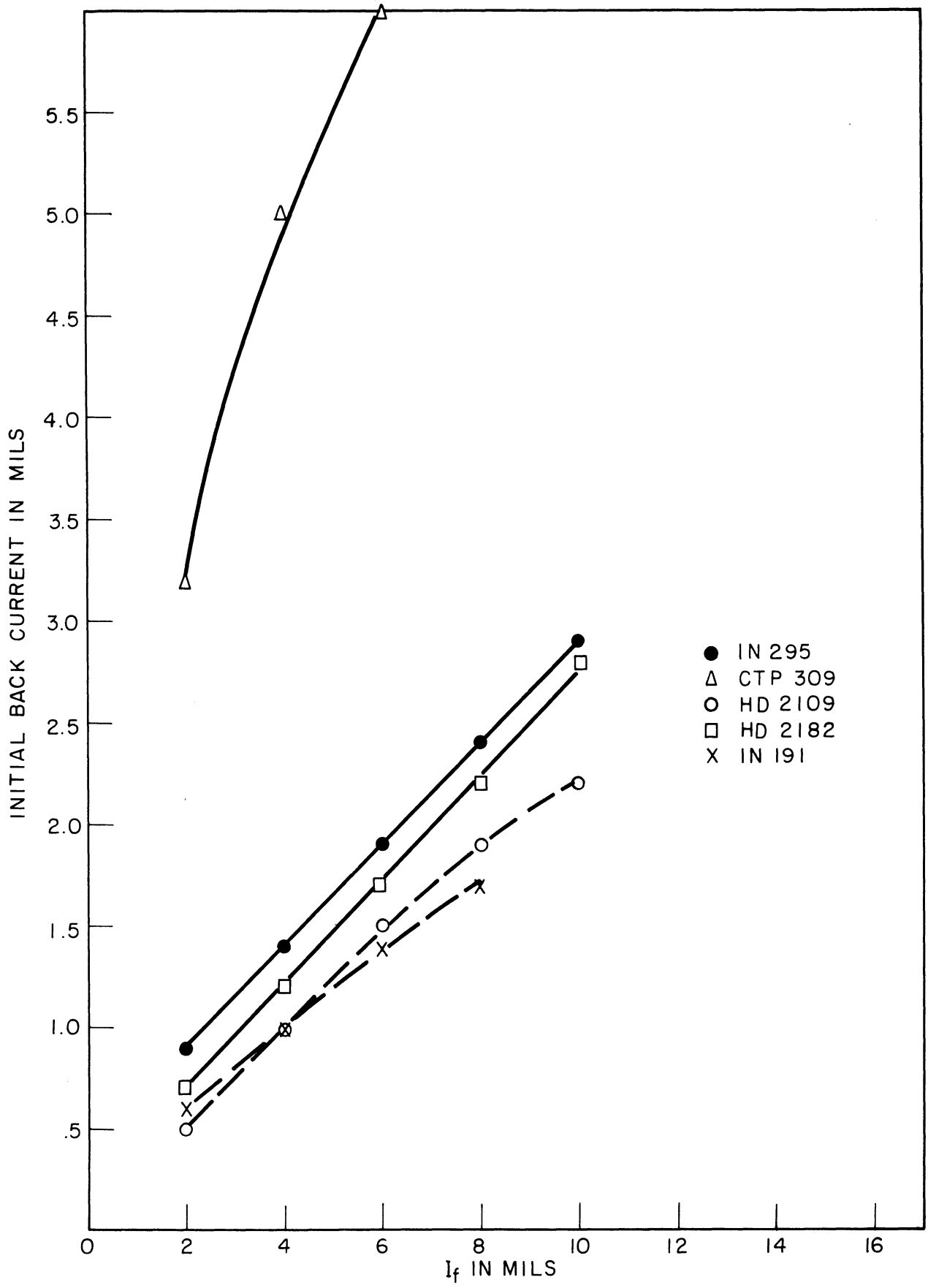
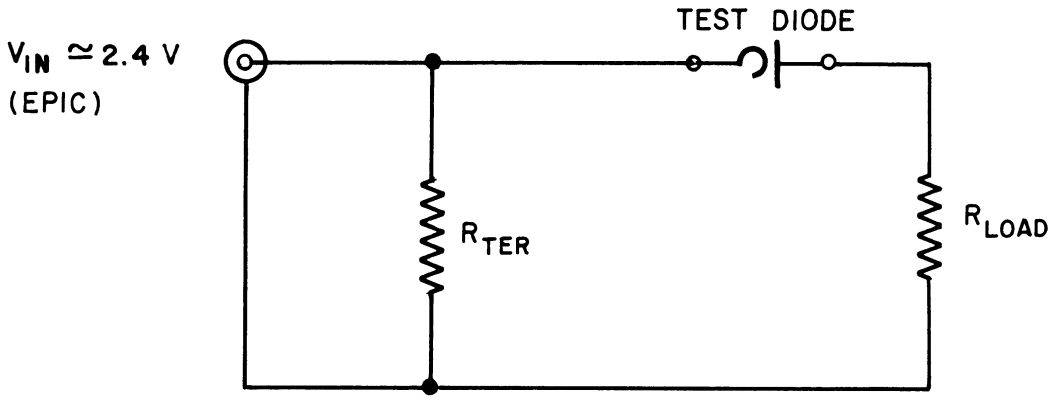
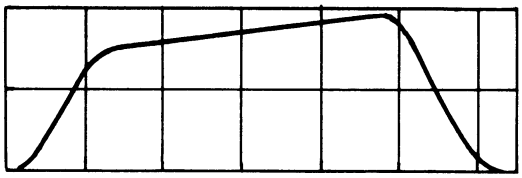


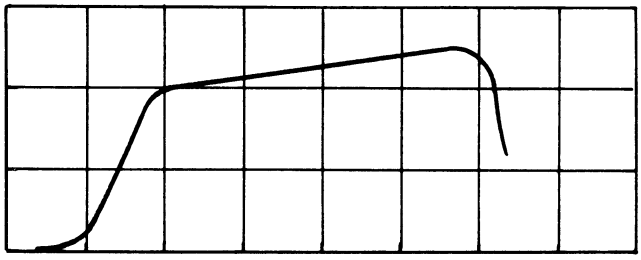
Fig. 2.16. Initial back current vs forward current, E_b = -3.0 v.



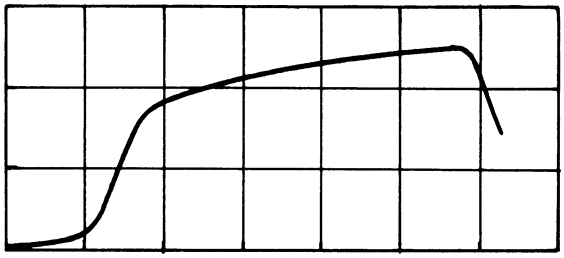
Current wave forms



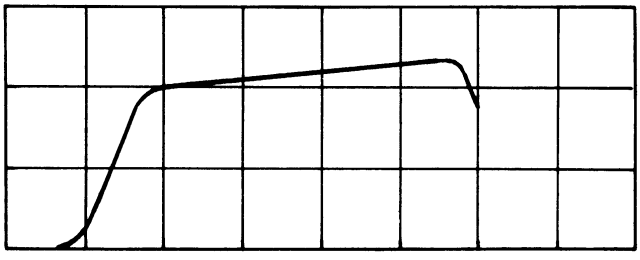
IN 117



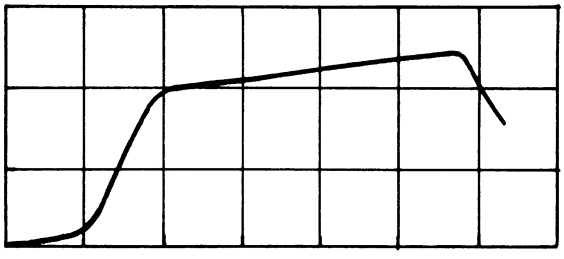
HD2182



CTP 309



Ray 295

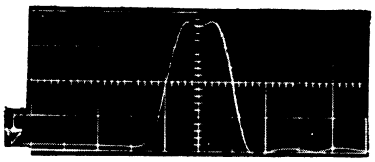


HD2109

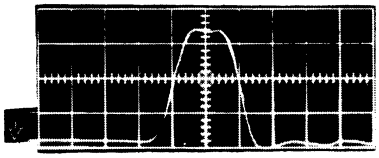
Time scale: .008 μsec/cm
Amplitude scale: .85 volts/cm

Fig. 2.17. Forward transients.

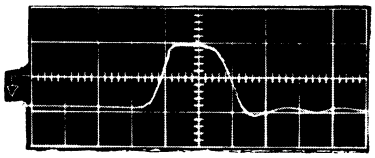
Grid signal with no attempt at clipping



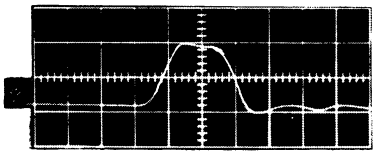
IN117



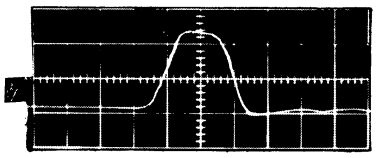
CTP309



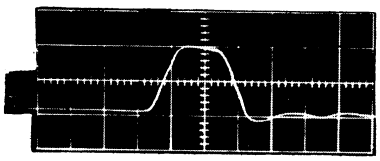
HD2182



Ray 295



HD2109



Time scale: 0.020 μsec/div
Amplitude scale: 0.5 volt/div

Fig. 2.18. Determination of the best clip diode (G).*

*See Fig. 2.23 for the circuit used.

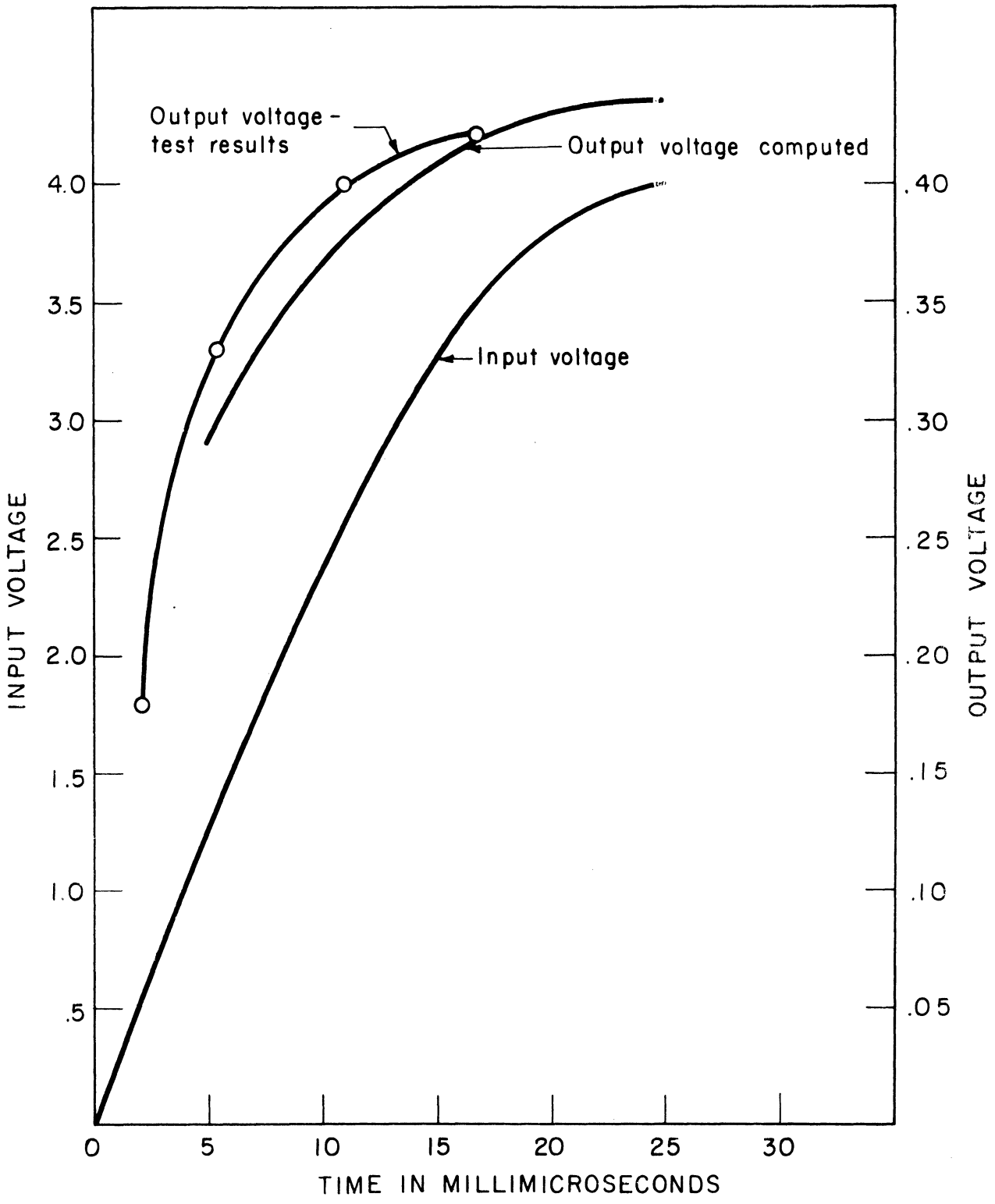
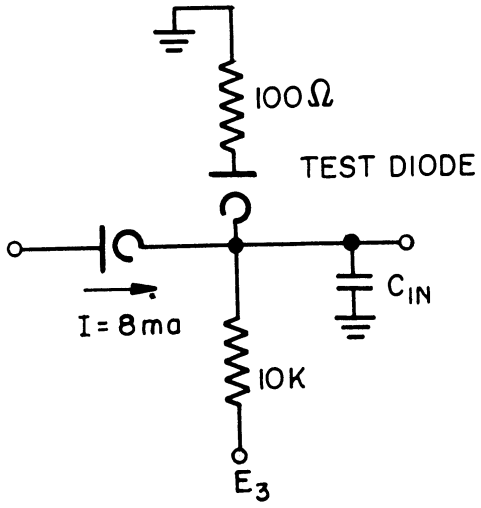
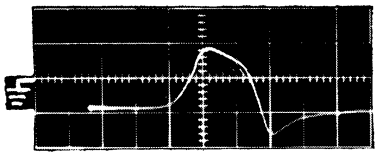


Fig. 2.19. Effect of static characteristics on wave shape.

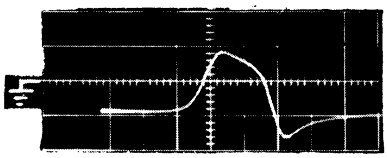
Circuit:



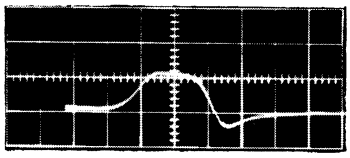
CTP 309



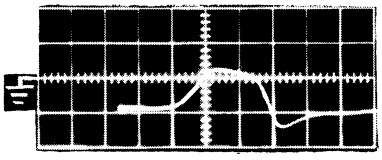
HD2182



Ray 295



HD2109



Time scale: 20 mμsec/div
Amplitude scale: 5 ma/div

Fig. 2.20. Experimental determination of the best grid-clamp diode.

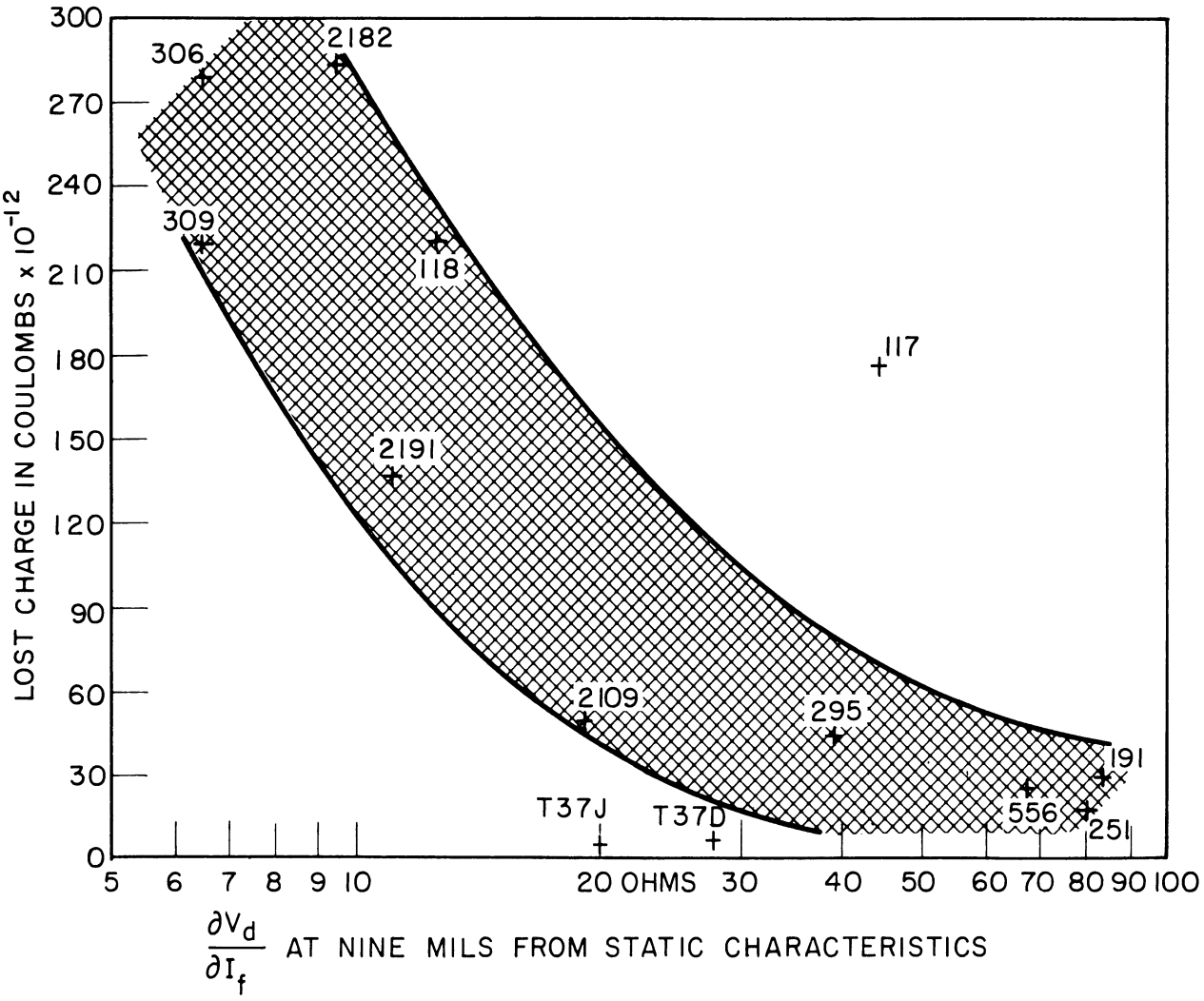
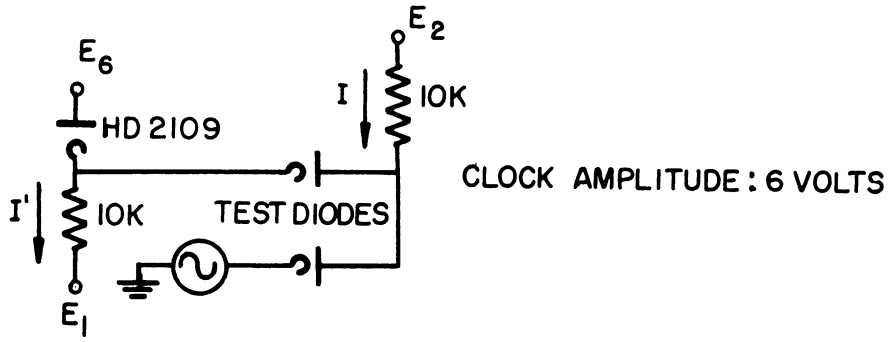


Fig. 2.21. Experimental correlation between static characteristics and lost charge.



Frequency	I	I'	Static Noise	Clock Noise	Total Noise	Test Diodes
5 Mc	4	8	.26	.15	.41	HD2109
10	8	12	.36	.18	.54	
15	12	16	.44	.20	.64	
20	16	20	.51	.30	.81	
5	4	8	.44	.2	.64	Ray IN295
10	8	12	.49	.30	.79	
15	12	16	.67	.33	1.00	

Total noise = Static noise + Clock noise

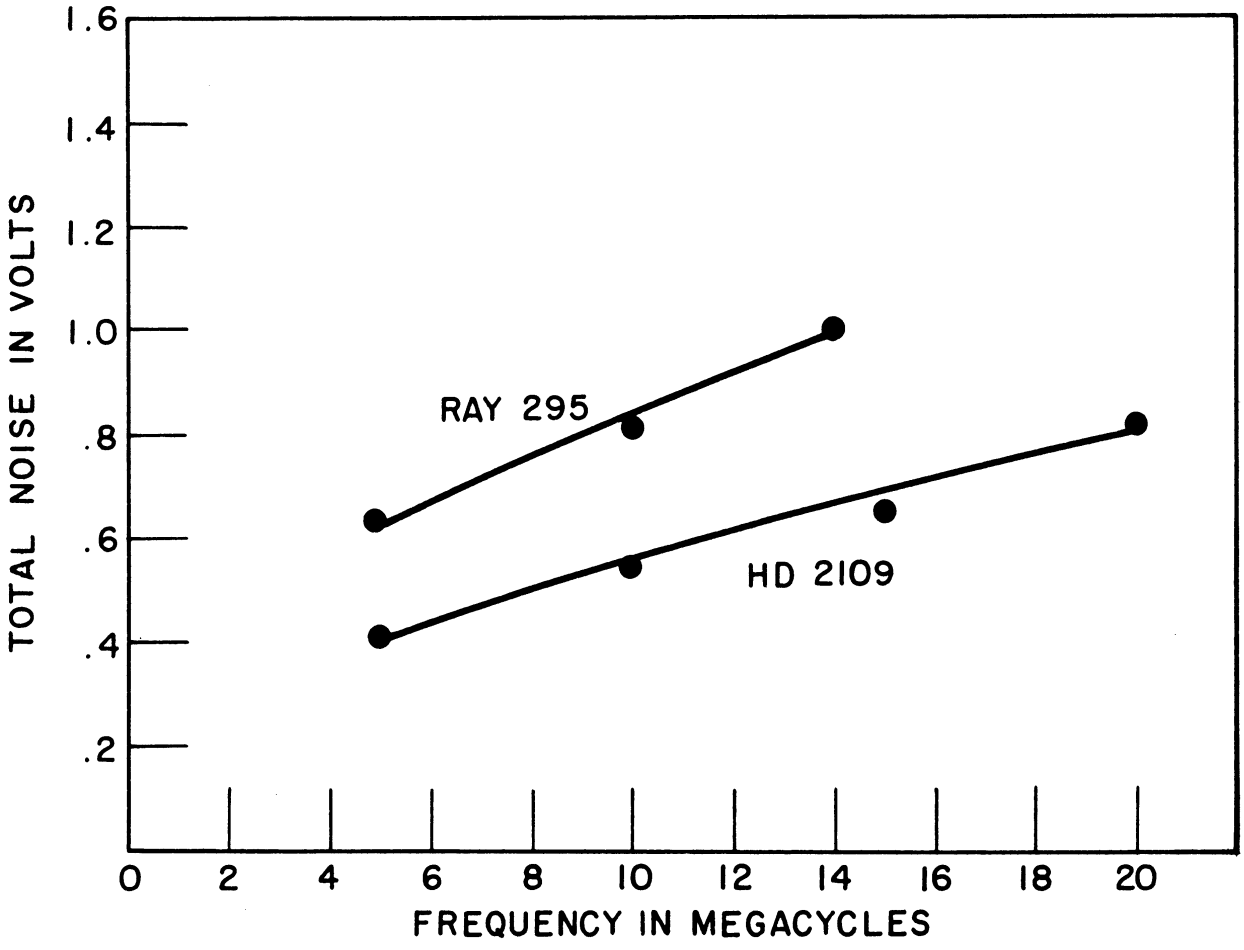


Fig. 2.22. Noise variation with frequency.

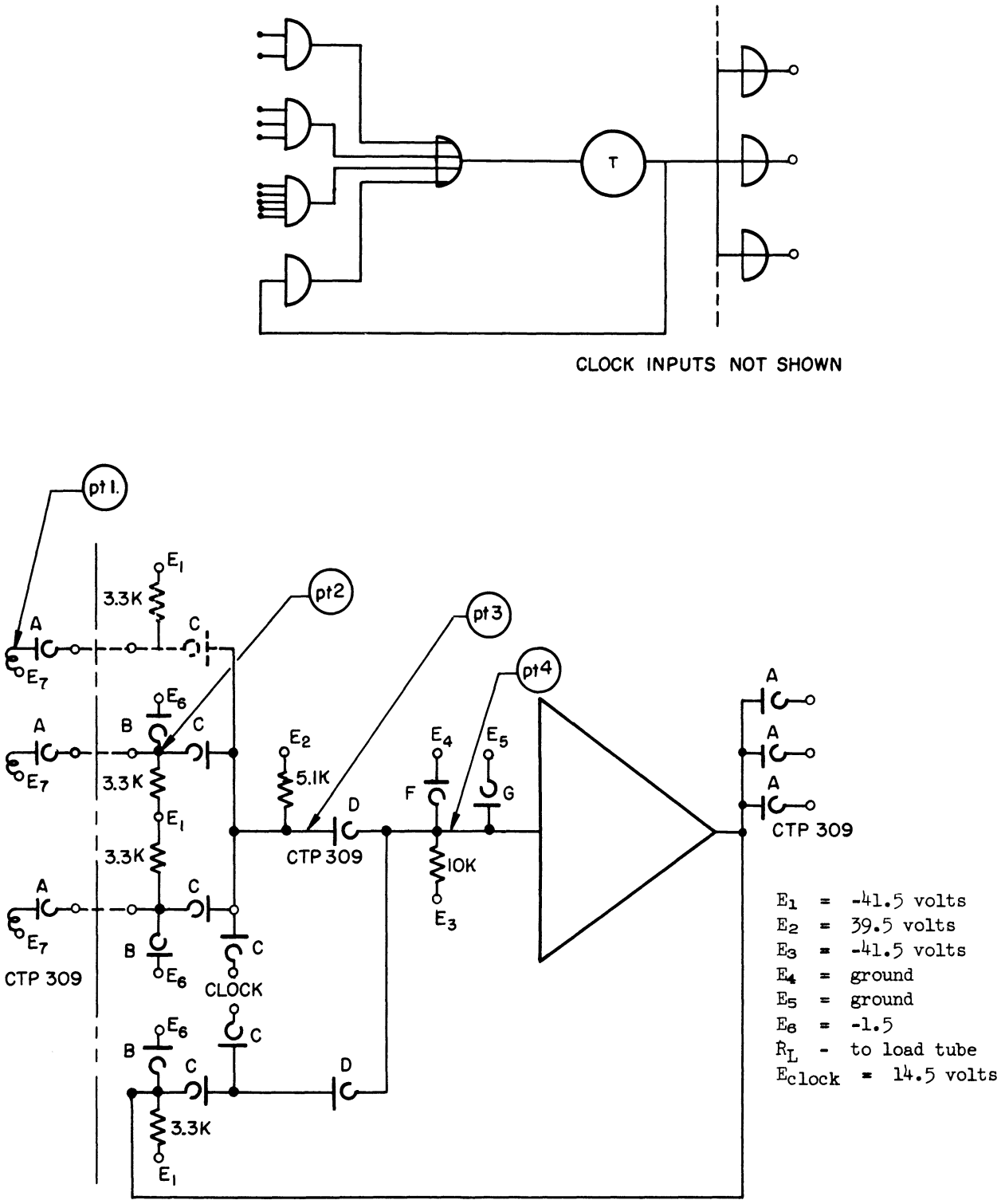
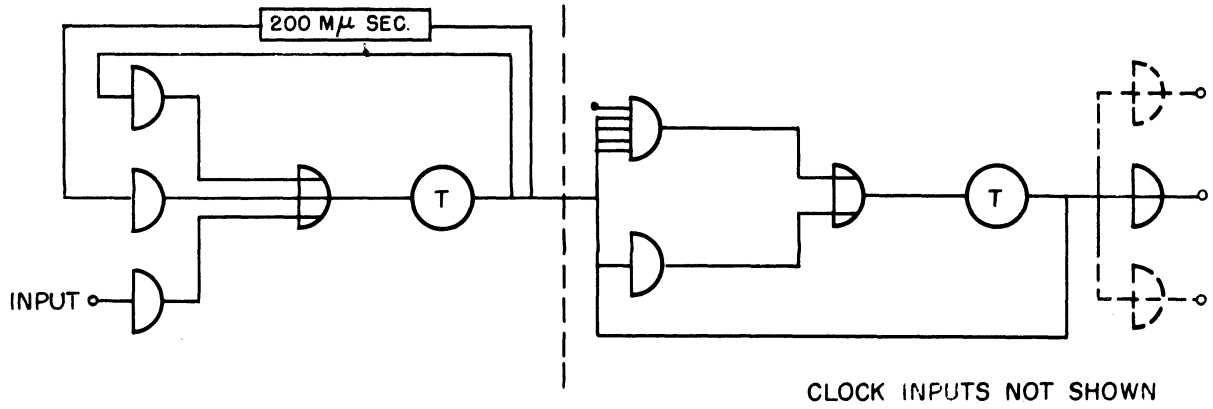


Fig. 2.23. 10 Mc experimental package.



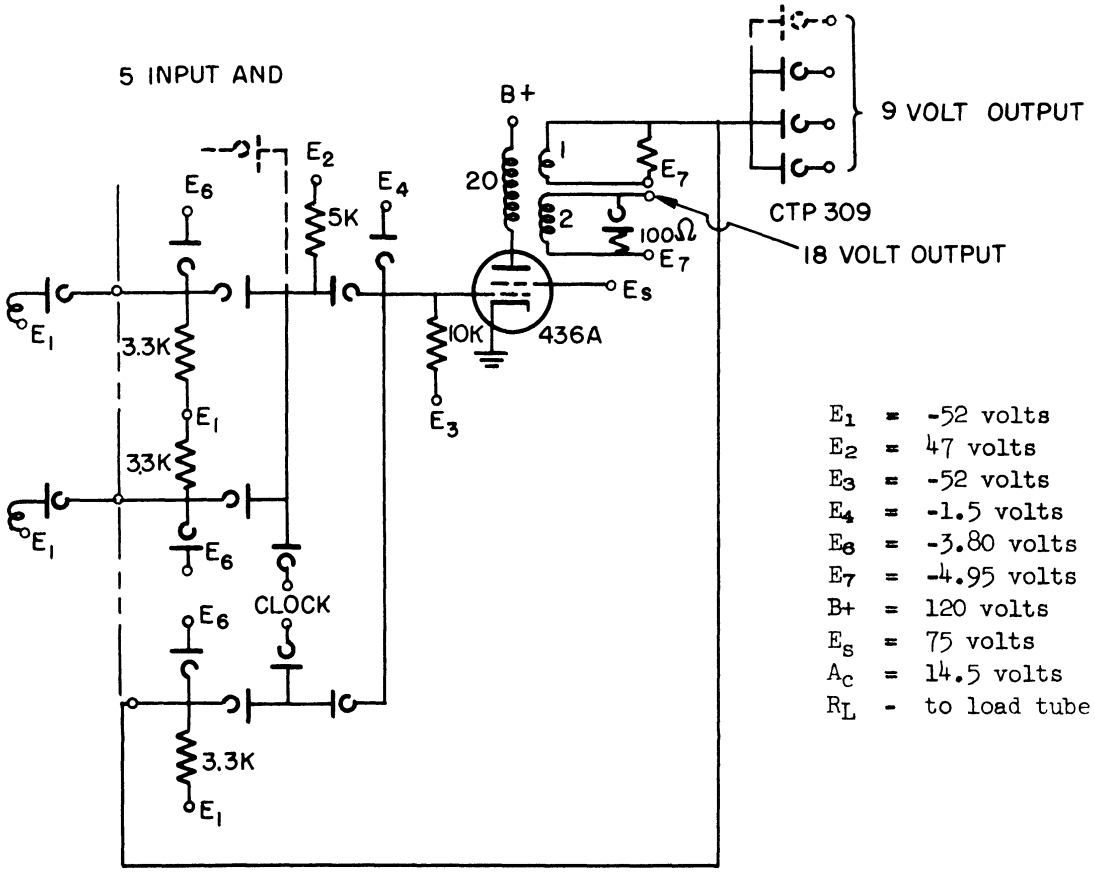
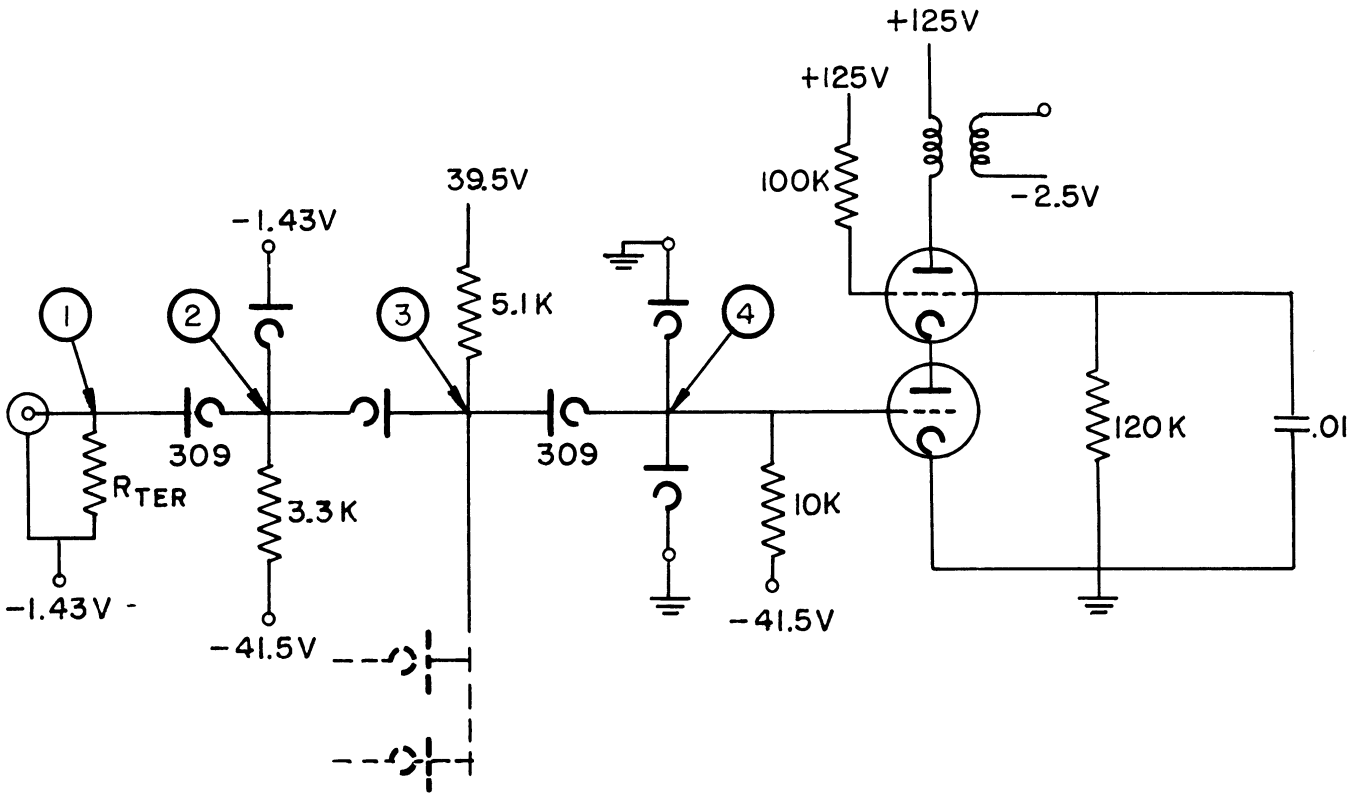


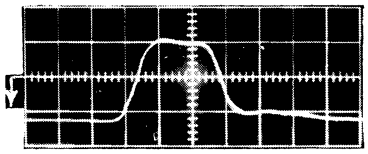
Fig. 2.24. 5 Mc experimental package.



Note: All diodes 2109's unless otherwise indicated.

CONDUCTION

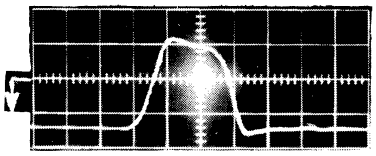
Pt 1



2 v/div

.020 μsec/div

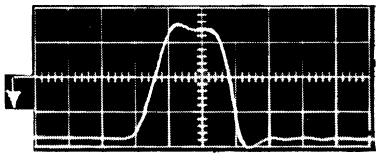
Pt 3



1 v/div

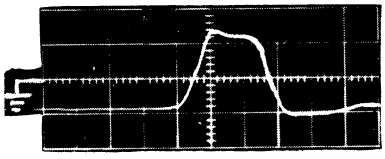
.020 μsec/div

Pt 2



1 v/div
.020 μsec/div

Pt 4

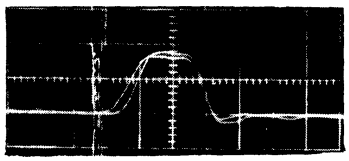


.5 v/div
.020 μsec/div

Fig. 2.25. 10 Mc gate performance.

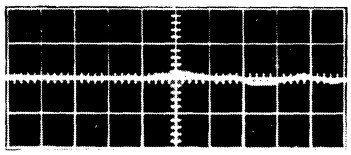
DELAY

Pt 2 to Pt 4

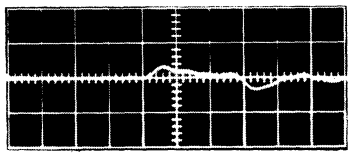


at Pt 2 2 v/div
at Pt 4 .5 v/div

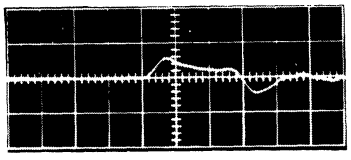
Time = .020 μsec/div



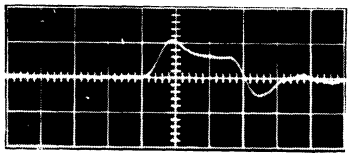
1 of 5 pulsed



2 of 5 pulsed



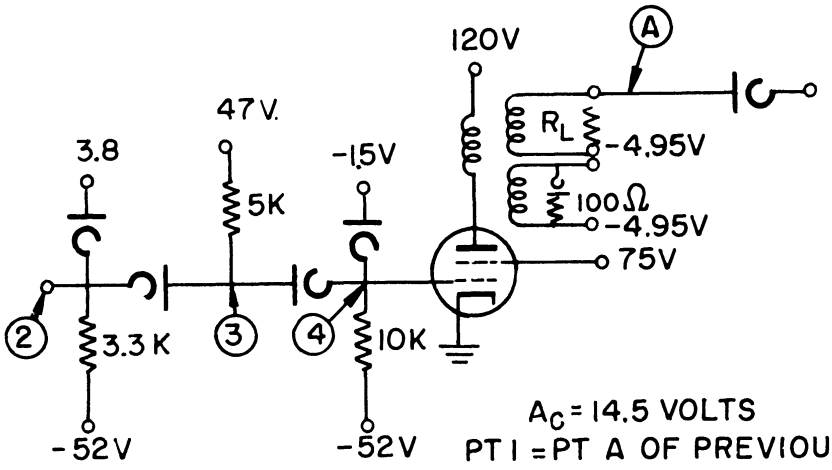
3 of 5 pulsed



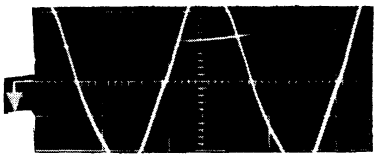
4 of 5 pulsed

.5 v/div
.020 μsec/div

Fig. 2.26. 10 Mc gate performance.

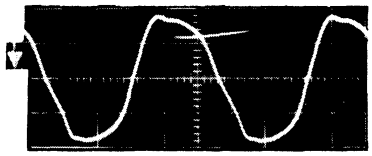


E_o = 9.0 volts
I = 10 ma
I' = 14.4 ma



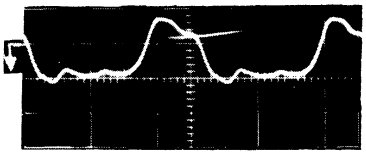
No. 1

Clock phase 2
5 v/div



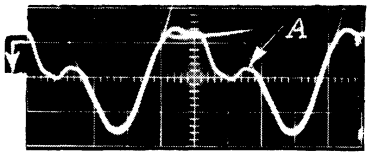
No. 2

Input-point 1
5 v/div



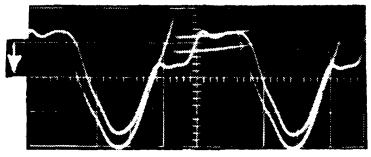
No. 3

Point 2
5 v/div



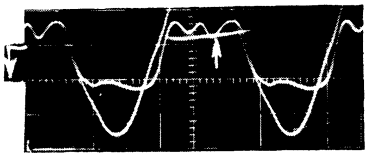
No. 4

Point 3
5 v/div



No. 5

Regen. gate
5 v/div

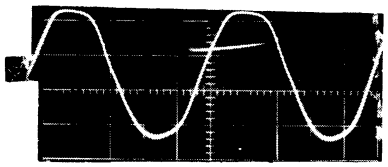


No. 6

Point 4
2 v/div

Time scale: 40 millimicroseconds/div

Fig. 2.27. 5 Mc gate performance.

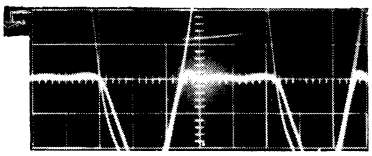


No. 7

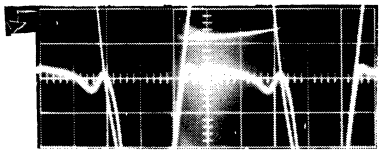
Output
10 v/div

Noise

Noise*



No. 8



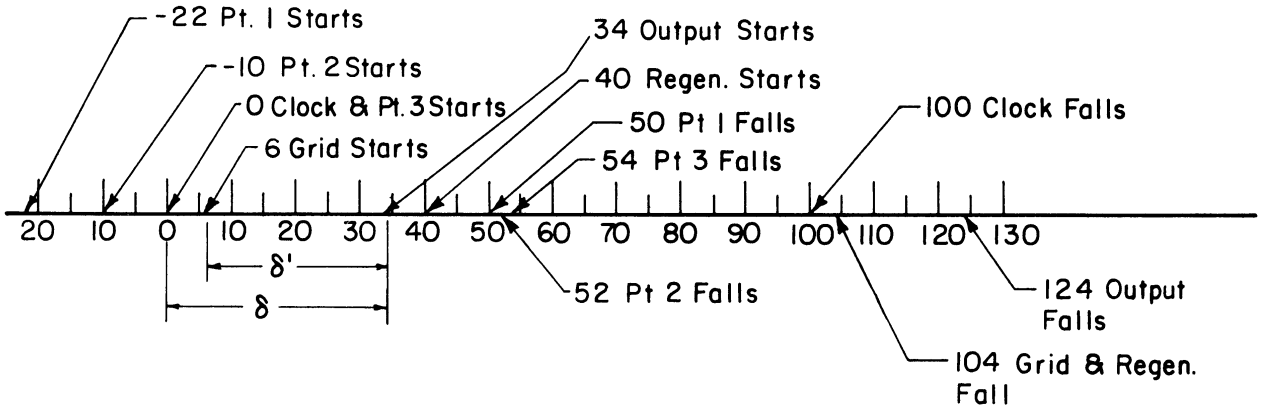
No. 9

0 of 5 pulsed
2 v/div

4 of 5 pulsed
2 v/div

Time scale: 40 millimicroseconds/div

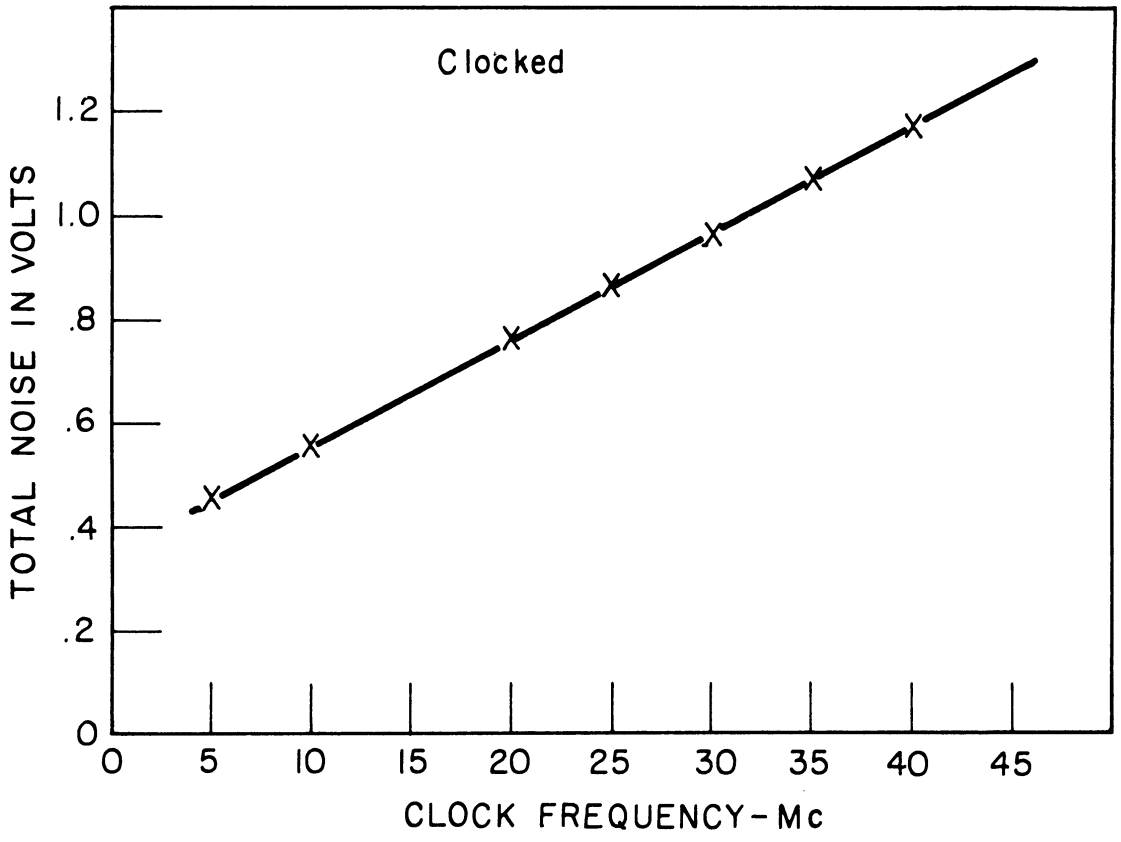
Pulse Time Sequence in Millimicroseconds



Note: Pulse "starts" when it goes through zero.
Pulse "falls" when it goes through zero.

Fig. 2.28. 5 Mc gate performance.

*Computed static noise is equal to .418 volt.



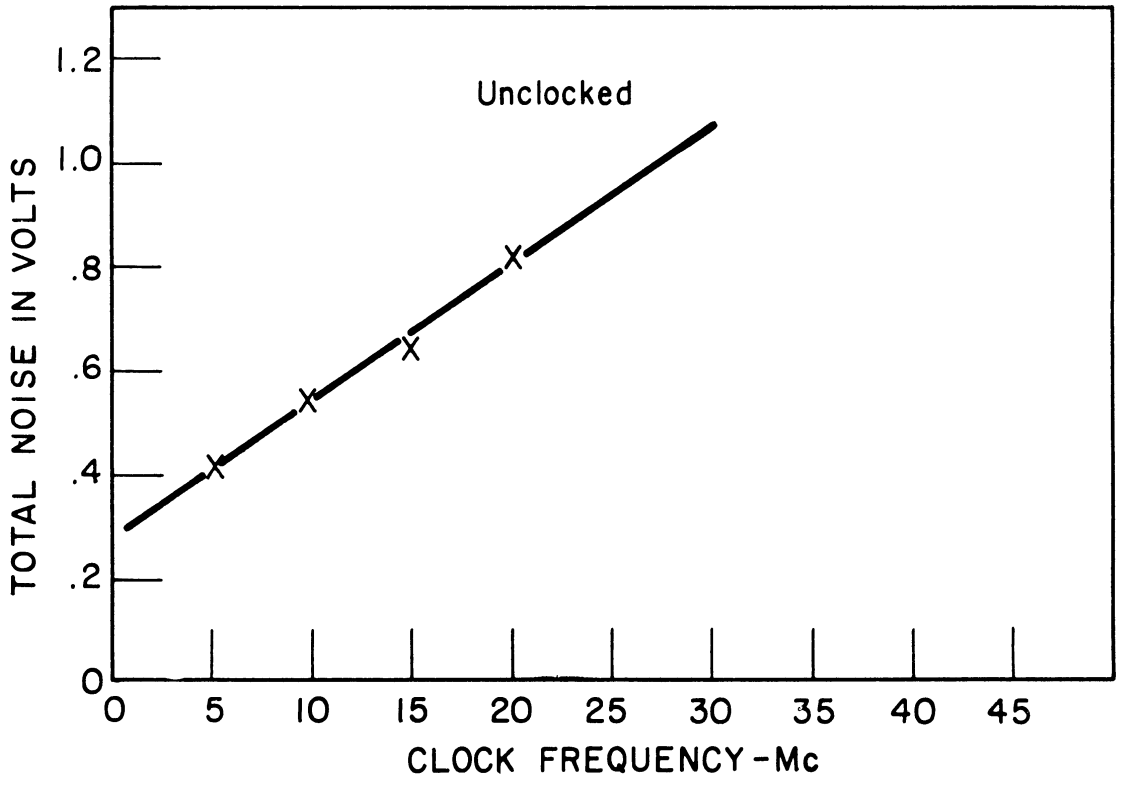
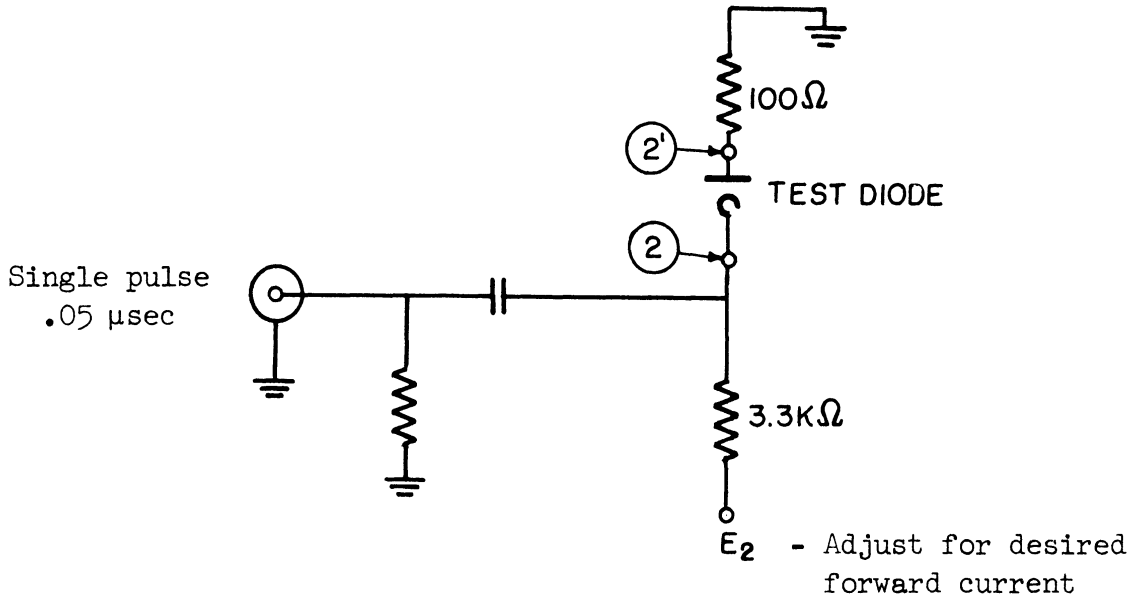


Fig. 2.29. Upper limit of performance.

TABLE 2.1

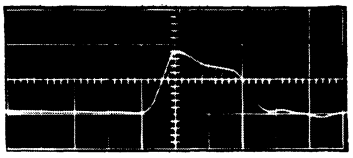
BACK RECOVERY AS A FUNCTION OF FORWARD CURRENT



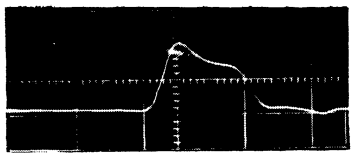
Diode	I_f Forward Current	I_{BO} Initial Reverse Current	Q_L Lost Charge	E_b Back Bias
CTP 309	3 ma	4 ma	110×10^{-12}	- 1.5 volts
	9	8	202×10^{-12}	- 1.5
	15	12	378×10^{-12}	- 1.5
Ray 295	3	1.0	18×10^{-12}	- 1.5
	9	2.0	45×10^{-12}	- 1.5
	15	3.0	77×10^{-12}	- 1.5
HD2182	3	4	104×10^{-12}	- 1.5
	9	10	252×10^{-12}	- 1.5
	15	13	402×10^{-12}	- 1.5
HD2109	3	0.5	6.5×10^{-12}	- 1.5
	9	1.5	21×10^{-12}	- 1.5
	15	2.0	36×10^{-12}	- 1.5

TALBE 2.1 (Cont.)

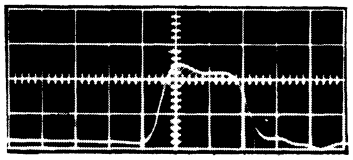
Forward Current of 9 mils in All Cases



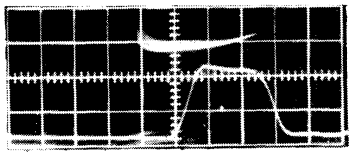
CTP 309
10 ma/div
.02 μsec/div



HD 2182
10 ma/div
.02 μsec/div



Ray 295
5 ma/div
.02 μsec/div



HD 2109
5 ma/div
.02 μsec/div

TABLE 2.2

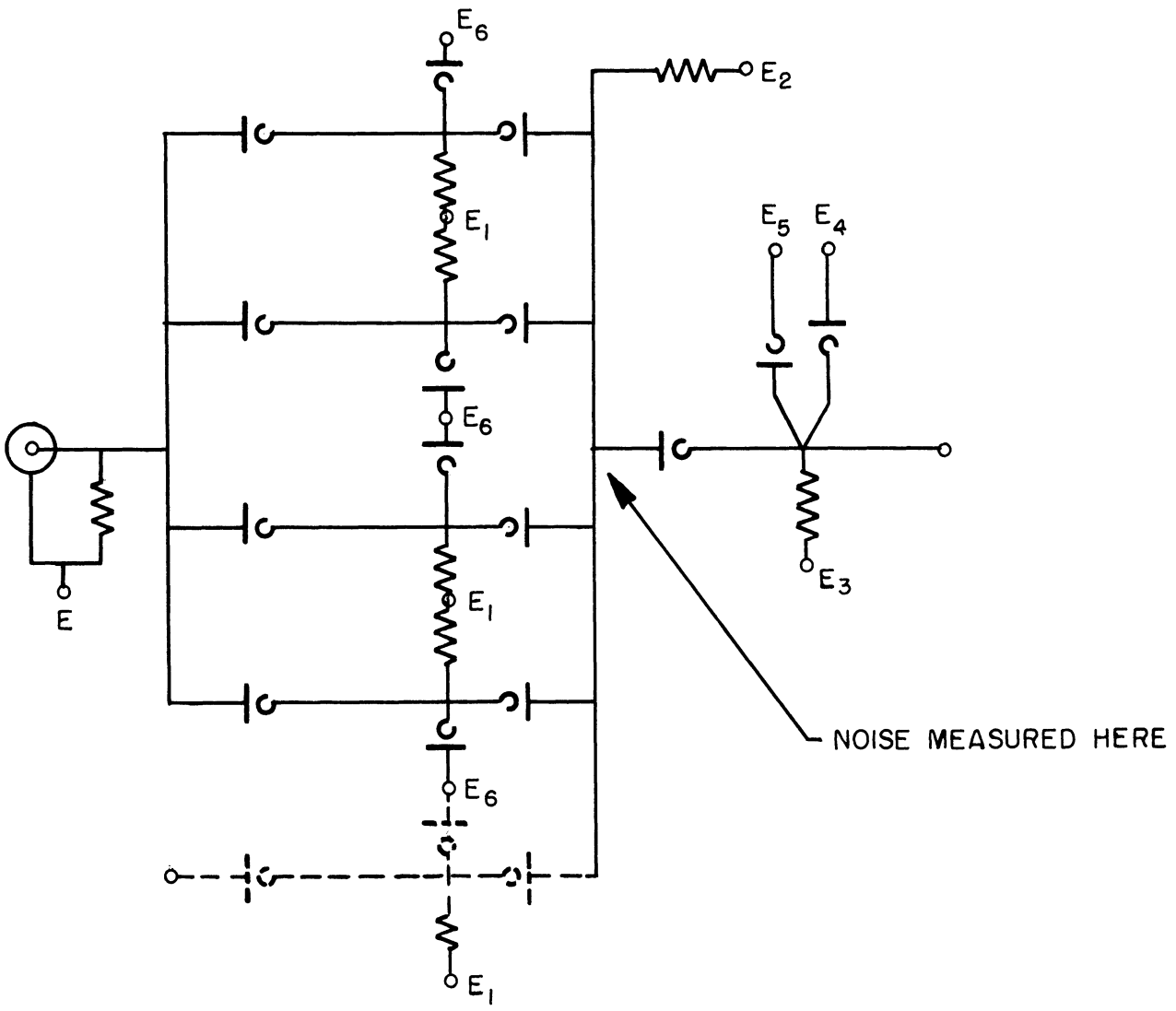
EXPERIMENTAL DETERMINATION OF THE BEST "AND" DIODE

Input Clamp Diode	"And" Diode	Total Noise	Static Noise	
			Meas.	Comp.
2109	309	.7	.35	.16
2109	2182	.9	.4	.25
2109	295	.9	.6	.61
*2109	2109	.55	.32	.38

*Best diode

TABLE 2.3

SECONDARY FACTORS AFFECTING NOISE



n	E_o	Total Noise	Static Noise	Currents
5	3.0	.48	.32	I = 8 ma
5	4.8	.52	.32	I' = 12 ma
5	3.0	.60	.40	I = 12 ma
5	4.8	.65	.40	I' = 16 ma

n = number of inputs to "and" gate
n-1 inputs pulsed in all cases
All diodes are Hughes 2109's.

3. PULSE TRANSFORMER

3.1 Pulse-Amplifier Analysis

The first half of this chapter is an investigation of the effects of tube, transformer, and external circuit parameters on the output characteristics of tube-transformer pulse amplifiers. A simplified low-frequency equivalent circuit for the transformer is assumed in this section. Equations are derived which relate the maximum available load current to the circuit parameters, and it is shown that a reasonant transformer design will allow maximum load current.

3.1.1 GENERAL QUALITATIVE ANALYSIS

The combination of vacuum tube and transformer exhibits certain fundamental properties when used as a pulse amplifier. It is the purpose of this section to investigate these properties and relate them to circuit capabilities of the tube transformer combination for a particular configuration and type of tube. The configuration considered is shown in Fig. 3.1(a). Figure 3.1(b) shows the simplified equivalent circuit, considered in this analysis, in which L is the primary inductance of the transformer, C is the parallel combination of tube plate capacitance, transformer winding capacitance, and reflected secondary capacitance, and R is the secondary load resistance reflected into the transformer primary. It is also assumed that the tube in Fig. 3.1(a) has pentode-like plate characteristics as shown in Fig. 3.2. It should be noted that the true grid capacitance is neglected in this analysis since we are here concerned primarily with output characteristics of the configuration. Grid capacitance will primarily affect the design of gating structures used to drive the tube. Transformer leakage inductance, coupling capacitance, and core loss also have been neglected as second-order effects.

The output of the tube-transformer configuration with a rectangular pulse on the grid can be derived qualitatively as follows. First, assume the input voltage to the grid is as shown in Fig. 3.3(a). Then, referring to the curves of Fig. 3.2, the tube will be quiescent at point A with grid voltage e_{g_1} until the pulse arrives at the grid. When the pulse arrives, the grid voltage will immediately increase to e_{g_2} and the plate current, I_p, will jump to I_b with an increase of ΔI. This increment of current will start charging the parallel RC combination in the plate circuit and the operating point will move along the tube characteristic of $e_g = e_{g_2}$ from B to C. The voltage across the plate load at this instant is $(E_b - E_c)$ with a current of $\Delta I'$ flowing through the reflected secondary load, if the assumption is made that the magnetizing current through L has not increased

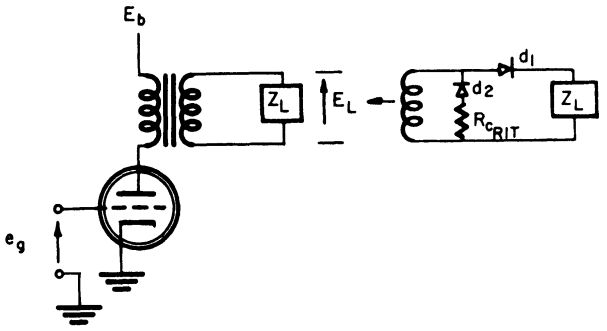


Fig. 3.1(a). Typical pulse-amplifier configuration.

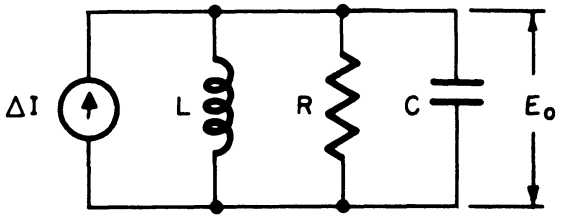


Fig. 3.1(b). Equivalent circuit for pulse amplifier.

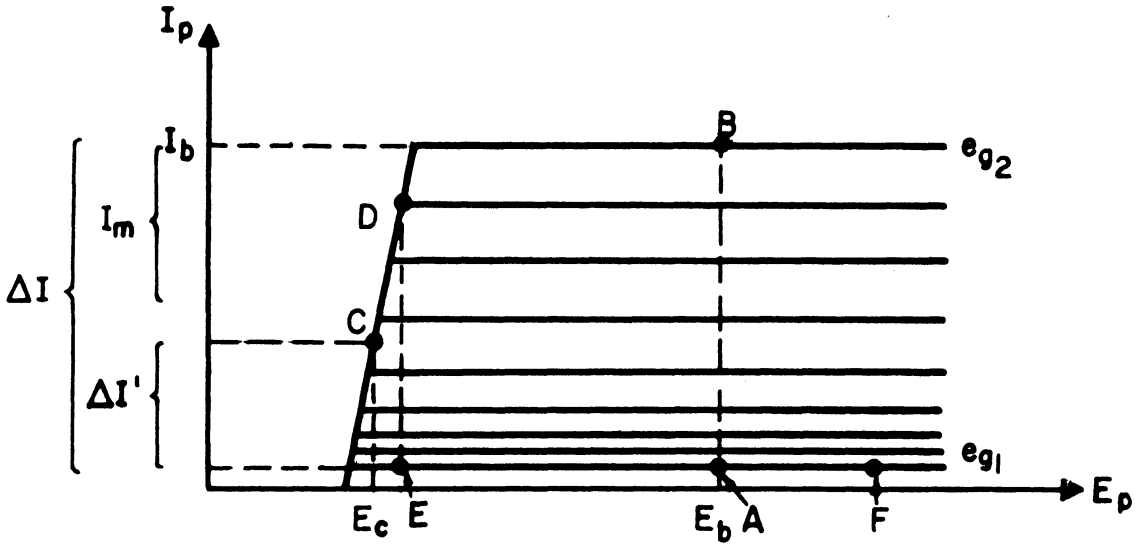


Fig. 3.2. Vacuum-tube plate characteristics.

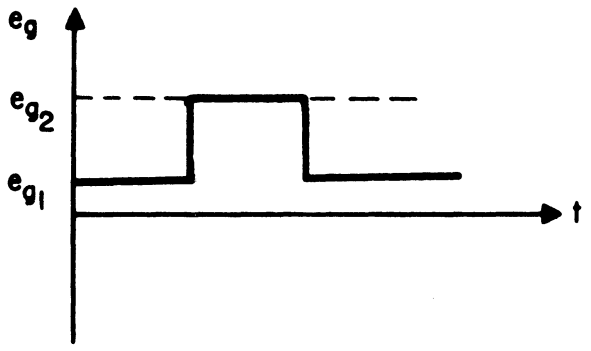


Fig. 3.3(a). Input signal to grid.

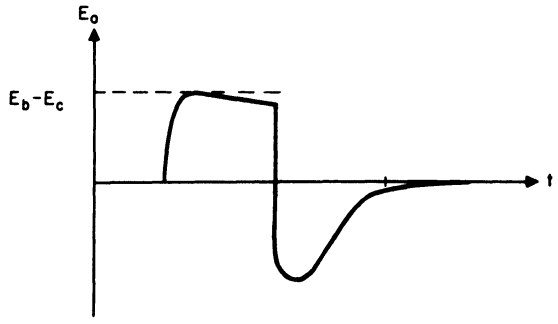


Fig. 3.3(b). Transformer output voltage.

significantly while the parallel RC combination is charging. During the flat-top portion of the pulse, the magnetizing current will be increasing so that the operating point of the tube will be moving back up the characteristic toward the knee. There will be only a slight droop across the top of the pulse as the operating point moves up the curve, as long as the operating point does not go over the knee of the curve. Suppose that by the end of the pulse the operating point is at D. If the grid voltage now drops back to e_{g_1}, the plate current will drop and the tube will be operating at E. The operating point will then move back past A to some point F and drop back to A as the energy stored in the parallel RLC combination is dissipated and the voltage decays. The rate at which the energy is dissipated is dependent on the relative values of resistance, capacitance, and inductance. The output voltage also may or may not have an oscillatory decay, depending on whether the system is underdamped or overdamped. Figure 3.3(b), which indicates the voltage response of the transformer primary for a rectangular pulse on the grid, is shown with a critically damped recovery. It can be shown that a critically damped circuit has the fastest possible recovery without overshoot.[7]

It is rather revealing to consider the limitations on transformer output voltage and current due to stray capacitance, tube capacitance, plate current drive, and output pulse shape as they are reflected in the E_p - I_p trajectory of the tube during the pulse interval. If, for example, a certain minimum rise time, τ_1 is specified and a certain output voltage (E_b - E_c) is required, then there will be a minimum R and a maximum C so that the parallel combination can be charged through a voltage (E_b - E_c) in time τ by a current ΔI with the operating point moving from B to C. If R is too small or C is too large, then the operating point will never get to point C, and may not even get over the knee of the curve. This will give a reduced output voltage and may cause the pulse to be too narrow. A narrow pulse may also be produced if, during the flat-top portion of the pulse, the increasing magnetizing current carries the operating point over the knee of the curve. If the operating point goes over the knee, then a slight increase in magnetizing current will drive the operating point back to B and the output voltage will go to zero. There will correspond to a given set of operating conditions a L_{min} which will limit the magnetizing current to a value less than I_m. L_{min} is a function of I_m, E_b - E_c, and τ_2 (pulse width). If L is fixed at some value larger than L_{min}, then by the end of the pulse the tube will be operating at some point D with a magnetizing current less than I_m flowing through the inductance and a voltage E_b - E_c across the capacitor. With given initial conditions and a specified R, L, and C, the output voltage during the recovery time can be calculated quite readily.[8] It can be shown, for example, that recovery time for a given L and C will be shortest with no overshoot when $R = 1/2 \sqrt{L/C}$. R can be switched to this value during the recovery time by the proper use of diodes, as will be shown later. The output voltage with critical damping will then be down to $E \simeq 0.01 (E_b - E_c)$ after a time $\tau = 2\pi \sqrt{LC}$.

We have indicated in this section some of the circuit limitations of the tube-transformer configuration when used as a pulse driving source for an isolated pulse without considering the effects of a train of pulses. The effects of a train of pulses will be important in computer circuit applications since the

tube-transformer input may be only an isolated pulse or may be a whole series of pulses, and ideally the pulse output should have the same shape in either case. If the pulse output is not the same in both cases, then the circuit must be designed so that the worst pulse shape, which occurs following a long train of pulses, will still satisfy the minimum output pulse requirements. The following two sections are devoted to a qualitative analysis of the further circuit restrictions imposed by the requirement that the tube-transformer can act as a driving source for a train of pulses.

3.1.2 RESONANT-TRANSFORMER ANALYSIS

One way to eliminate the pulse-to-pulse interaction due to a train of pulses is to design the transformer so that it will completely recover from one pulse before the next one is present. It can be shown[9] that the minimum recovery time till be $T_{R_{min}} = \pi\sqrt{LC}$ where L and C refer to the elements in the plate circuit of Fig. 3.1(b). If the pulse repetition frequency is f_p, and if the pulses have equal on-off periods, then it follows that for $T_{R_{min}} = 1/2\ f_p = \pi/\omega_p$, the transformer will just recover during the off pulse period. If we define ω_T, the transformer resonant frequency, as $\omega_T = 1/\sqrt{LC}$, we see that a resonant transformer tuned to the pulse repetition frequency will just recover during the off pulse period. In other words, we require that $\omega_T = 2\pi f_p = \omega_p$, or that the transformer be tuned to the pulse repetition frequency. It turns out that a transformer tuned to ω_p will not recover in $1/2\ f_p$ seconds without excessive overshoot. Overshoot is undesirable because it might cause false triggering, so the transformer must be damped by adjusting R to critical damping. This value of R is given by $R_{crit} = 1/2\sqrt{L/C}$ and can be obtained with a transformer loading scheme as shown in Fig. 3.1(a), where d_1 isolates Z_L during recovery and d_2 switches in R_{crit}. With critical damping the transformer will not completely recover in $1/2\ f_p$, but the magnetizing current will be reduced to about 0.08 times what it was at the end of the pulse. It is shown in Appendix C that this reduction is enough to make the pulse output relatively independent of the past history of the circuit. The fact that the resonant frequency of the transformer must be greater than the operating frequency sets an upper limit on the transformer inductance for a given capacitance. This condition plus the constraint that the operating point may not go over the knee of the characteristic curve may be used to analyze the operation of a given tube-transformer load configuration. This analysis is carried out in Appendix D and shows that

$$I_{L_{max}} = \frac{23}{140\pi^2}\frac{\Delta I^2}{C_T f_p E_L} - \frac{35\pi^2}{23} f_p E_L C_s \ , \qquad (3.1)$$

where

I_L = load current referred to the transformer secondary,
ΔI = tube driving current as defined in Fig. 3.1(b),
E_L = pulse output voltage referred to the transformer secondary,
f_p = pulse repetition frequency,
C_T = tube primary capacitance and transformer primary capacitance, and
C_s = transformer secondary capacitance.

There is one remaining constraint on the circuit parameters, imposed by the pulse rise-time requirements. As mentioned previously, for a given minimum rise time, pulse voltage ($E_b - E_c$), tube driving current ΔI, and equivalent capacitance, there will be a certain minimum load resistance; which means that there will be a certain maximum load current. An analysis of this situation is developed in Appendix E, giving the relationship

$$I_{L_{max}} = 40\, C_s f_p E_L \ln \frac{\Delta I \sin \pi/10}{4\pi E_L f_p C_T} , \qquad (3.2)$$

where the symbols have the same meanings as for Eq. (3.1). Thus we see that for particular values of f_p, ΔI, C_s, C_T, and E_L there will be a maximum load current specified by either Eq. (3.1) or Eq. (3.2), whichever is least. It should be noted that, in general, Eq. (3.1) will fix the maximum load current since it gives a lower maximum load current than Eq. (3.2).

3.1.3 NONRESONANT-TRANSFORMER ANALYSIS

It might seem that it would be possible to reduce transformer magnetizing current during the pulse interval and thus increase load current by increasing the transformer primary inductance. This would remove the restriction due to Eq. (3.1) and allow the load current to be fixed by Eq. (3.2). Offhand this would seem like a significant improvement since substitution of typical values for f_p, ΔI, E_L, and C_T into Eqs. (3.1) and (3.2) shows that Eq. (3.2) would give several times as much load current. This improvement is more apparent than real, however, because the large value of primary inductance will cause a large pulse-to-pulse interaction which puts an additional restriction on the output load current. The interaction is caused by the transformer-stored energy piling up from pulse to pulse. For large values of primary inductance, only a small amount of energy will be stored per pulse, but only a small fraction of this energy will be dissipated during the off pulse period. This means that for a long train of pulses, stored energy will be accumulating in the transformer until a steady state is reached where the energy stored during a pulse period is equal to the energy dissipated during the off pulse period. For a train of pulses with equal on and off periods, and a large enough inductance so that there will be negligible sag, the steady-state condition will obviously occur when the output voltage during the off pulse period is equal to the output voltage during the pulse period and of opposite sign. This means that for a specified output pulse voltage, E_L, circuit capacitance will have to be charged through $2E_L$, from $-E_L$ to $+E_L$ during the pulse rise time. The nonresonant transformer is analyzed in Appendix F, where the following relation is obtained:

$$e^{-[I_L/10 f_p E_L (C_s + N^2 C_T)]} = [(N\Delta I/I_L) - 3]/[(N\Delta I/I_L) - 1] . \qquad (3.3)$$

This equation gives a relation between the specified E_L, ΔI, f_p, C_s, C_T, and N and the allowed I_L. Substitution of a range of values for N gives a curve of I_L

vs N from which we can select an optimum turns ratio to get maximum I_L. Substitution of typical values for E_L, ΔI, f_p, C_s, and C_T into Eqs. (3.1) and (3.3) will give a comparison of maximum load current for typical resonant- and nonresonant-transformer designs as shown below. Let

$$\begin{aligned} E_L &= 5 \text{ v}, \\ \Delta I &= 60 \text{ ma}, \\ C_s &= 50 \times 10^{-12} \text{ f}, \\ C_T &= 6 \times 10^{-12} \text{ f}, \text{ and} \\ f_p &= 5 \times 10^6 \text{ cps}. \end{aligned}$$

Then substitution into Eq. (3.1) gives $I_{L_{max}} = 83$ ma and substitution into Eq. (3.3) for a range of values for the turns ratio gives the curve I_L vs N shown in Fig. 3.4 so that $I_{L_{max}} = 47$ ma. Thus, a resonant-transformer design would allow a larger load current for circuit values typical of our application.

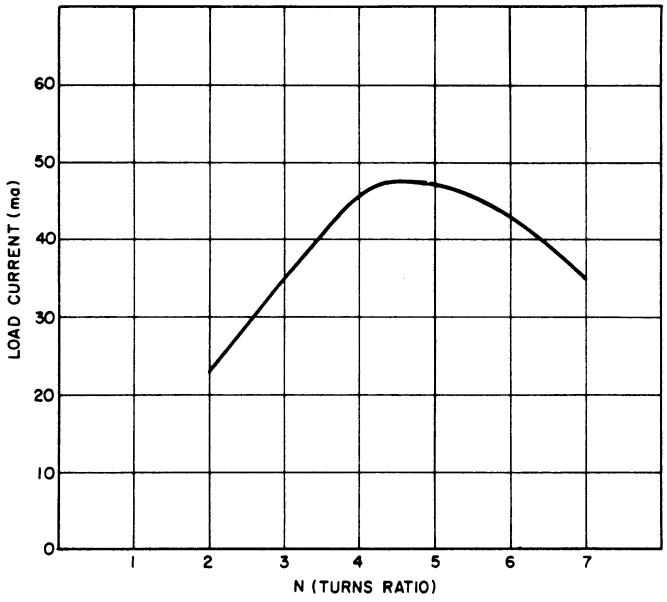


Fig. 3.4. Relationship of load current to turns ratio for nonresonant transformer.

3.1.4 SUMMARY

Several basic limitations on the circuit operation of the tube-transformer configuration have been discussed. These limitations are independent of transformer core characteristics as long as the characteristics do not deteriorate from their low-frequency values. For ferrite core materials, these characteristics appear to be relatively constant up to and beyond ten megacycles.

On the basis of the basic circuit limitations we have derived several equations which give restrictions on output load current for two different types of transformer design. The two types of transformer design considered were a low-

inductance and a high-inductance transformer. The low-inductance configuration is resonant at the operating frequency. It has been shown that for particular values of circuit parameters, the low-inductance transformer will deliver about twice as much secondary load current. No analysis has been made of any but these limiting cases of primary inductance because of the complexity of the analysis. It seems reasonable to suppose, however, that maximum allowable secondary load current will decrease monotonically as inductance is increased from the resonant value.

3.2 Pulse-Transformer Investigation

The following is a study of the limitations on circuit operation imposed entirely by the transformer characteristics. The effects of core material, core size and shape, and winding geometry on transformer characteristics are indicated and some measurements of these effects are presented.

3.2.1 CORE

In general there are two distinct regions of interest concerning the core of a pulse transformer, the magnetic properties of the material and the geometrical shape of the core. In this section a short outline of the theory of ferromagnetic materials is presented and this is followed by a discussion of the properties of the ferrites tested. The discussion of core loss and permeability explains what can be expected of ferrites with respect to these properties and the effect of these properties on the operation of the transformer. The final portion of the core discussion explains why the cup core is the best geometry for our application, and also contains a qualitative discussion of the core dimensions.

3.2.1.1 Theory of Ferromagnetism.—According to the classical theory, ferromagnetic materials exist in a state of spontaneous magnetization. In their native state, however, the total magnetization is zero because the material is composed of a large number of domains, each magnetized to saturation in different directions giving a net zero magnetization. These materials can be magnetized by applying an external magnetic field which shifts the size and orientation of the domains so that there exists a total overall magnetization. There are two distinct methods by which domains are reoriented to provide an overall magnetization in the material. First, unfavorably oriented domains may be rotated so that they are more favorably oriented with a resulting increase in the net magnetization. Secondly, favorably oriented domains may be increased in size at the expense of less favorably oriented domains, thus giving a net overall magnetization.

There are two forces acting in ferromagnetic materials tending to maintain the domains in their equilibrium states. These forces are due to stress anisotropy and magnetocrystalline anisotropy. The stress anisotropy is an imposed anisotropy due to stresses of one sort or another which deform the crystal lattice

or to impurities which form inclusions in the crystal lattice. The magnetocrystalline anisotropy is due to the crystalline nature of the material which favors one orientation of a domain over another. Thus it is evident that there are forces acting on the domains which tend to maintain the status quo, that is, net zero magnetization in the material.

As mentioned above, as the domain walls tend to expand, contract, or rotate under the influence of an external field, they are retarded by stress and magnetocrystalline anisotropy forces which tend to maintain them in their equilibrium position. One can picture the motion of domain walls through a mass-spring-damper mechanical analog. The domain walls are pictured as having a fixed mass with the motion retarded by the forces due to stress and magnetocrystalline anisotropy and damped by losses in the material. The process of magnetization, then, corresponds to imposing an external field on the material and moving the domain walls so that there exists a more favorable orientation of the magnetization within the material.

It should be fairly evident now that the mobility of the domain walls determines the permeability of the material. This means that it is desirable that the retarding forces acting on the domain walls during motion be small. In ferrites, these forces may be made small by a proper mixture of materials in the formation of the mixed crystalline structures and by proper heat treatments. In this way large permeabilities are realized.

The body resistance of the ferrite materials, however, is also a function of the anisotropy energy, and as the anisotropy is reduced, the body resistance is also reduced with a resulting increase in the eddy current loss. This is an undesirable effect and therefore a proper balance between the requirement of low anisotropy for high permeability as opposed to the high loss associated with this low anisotropy must be considered in any particular application.

It has been found that three factors influence the high frequency performance of the ferrite materials: (1) domain-wall motion, (2) dimensional resonance, and (3) ferromagnetic resonance. The effects of domain-wall motion have been discussed; as mentioned above, the motion is simply analogous to a mass-spring-damper system. Dimensional resonance is, however, an entirely different phenomenon. The effects of dimensional resonance seem to be directly related to the size of the magnetic material under test. It is apparently a cavity-type resonance effect resulting from the high dielectric constant of ferrite materials, which gives wavelengths in the material of the same order of magnitude as the dimensions of the sample under test. The third high-frequency effect is ferromagnetic resonance. Ferromagnetic resonance effects are caused by the fact that the material is composed of spinning electrons, which make up the magnetic field. Each of them contributes an elementary magnetic moment, which, under the influence of an external d-c field, will precess around an equilibrium orientation. Now if an external a-c field of the same frequency as the precession frequency is applied in the proper direction, the spinning electrons will absorb energy, giving a resonance effect.

Of the above factors one need consider only the first. Ferromagnetic resonance effects occur at much higher frequencies than those associated with this project, and the pulse transformers being used are of such a size that dimensional resonance effects are not involved. Therefore, one need only consider the first effect, domain-wall motion. As mentioned above, by analogy with a mass-spring-damper system one associates stress anisotropy and magnetocrystalline anisotropy with the effective spring constant. The mass of the wall is a constant determined by the material, as is the damping. The effective spring constant can be varied by different manufacturing processes to alter the stress anisotropy, or by mixing different types of crystals together to get a zero magnetocrystalline anisotropy. If, to obtain a high permeability, this is done, one will have a low effective constant and therefore a low resonant frequency. In power applications, this is done and results in resonant frequencies of the order of a megacycle. Since we are interested in operation at much higher frequencies, and since permeability is not of major importance, we will do well to maintain a high spring constant, giving a high resonant frequency of the domain-wall motion, and consequently a low permeability. By maintaining a high effective spring constant, that is, high stress anisotropy and high magnetocrystalline anisotropy, one will also reduce the eddy-current losses by increasing the body resistance, and the hysteresis losses will also be reduced. It has been found that General Ceramics type Q material most nearly fits these requirements. It has a rather low permeability, a high body resistance, and a high frequency cutoff well above ten megacycles.

3.2.1.2 Core Resistance and Permeability.—At high frequencies there are two core-material characteristics which are of particular interest: core permeability and resistance. The core resistance must be considered at high frequencies to account for the losses associated with transmission through the transformer.

Perhaps the best way to define core resistance is in terms of the resistance calculated from the open-circuit damping characteristics of the particular transformer under consideration. The damping of the sinusoidal ringing after the pulse is due to losses in the core material, losses principally due to the losses associated with domain-wall motion and eddy currents. In the materials under consideration the physical resistivity of the core material is sufficiently large to render the eddy currents relatively small, with the domain-wall losses probably accounting for a major portion of the loss.

The effective loss resistance may be calculated by consideration of the simple RLC equivalent circuit associated with the pulse tail. The pictures of Fig. 3.6 reveal the wide variation in the magnitude of the loss resistance associated with any particular core material. These pictures were taken at the secondary of an open-circuited transformer which was pulsed by an Epic pulser driving a 436A tetrode which was biased so that the tube was cut off after the pulse. The calculations shown below the pictures illustrate the general procedure followed in the approximate determination of the effective core resistance.

Due to the effects of domain-wall motion, the permeability of a ferrite

material is not a constant over the entire frequency spectrum. The general nature of the frequency characteristics of a ferrite material is illustrated in Fig. 3.5.

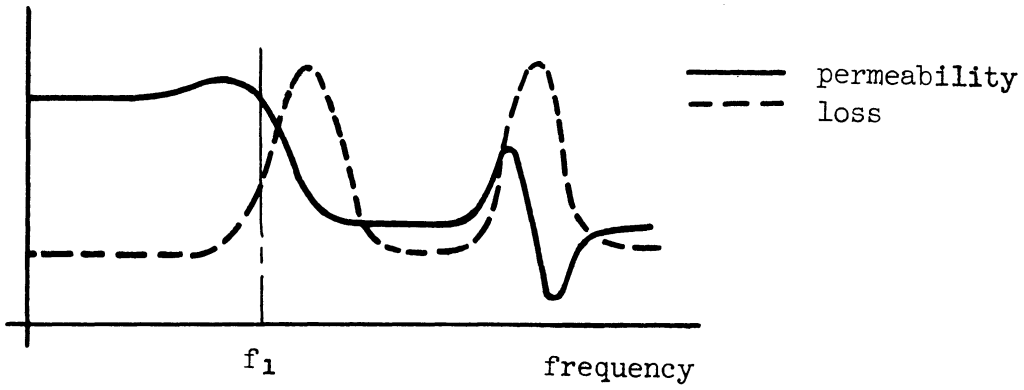
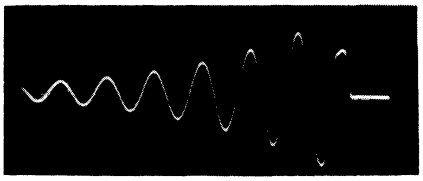


Fig. 3.5. Frequency characteristics of ferrite materials.

Type Q Material



Type H Material

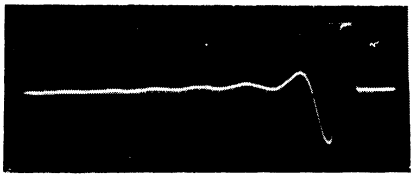


Fig. 3.6. Open-circuit damping characteristics.

3.2.1.2.1 Calculation of the Effective Loss Resistance

The damping of the ringing is a simple RC-type of damping. Therefore one proceeds as follows:

RC = time for ringing to decay to 36.8% of its initial value. The RC time constant can be found from the pictures of the damping.
C = $1/4\pi^2 L_p f^2$.
L_p = primary inductance of transformer obtained by measurement on Q meter.
f = frequency of ringing obtained from picture of ringing.
R = parallel combination of R_{source} and R_{core} loss.
R_{source} = source resistance estimated from the tube characteristics.

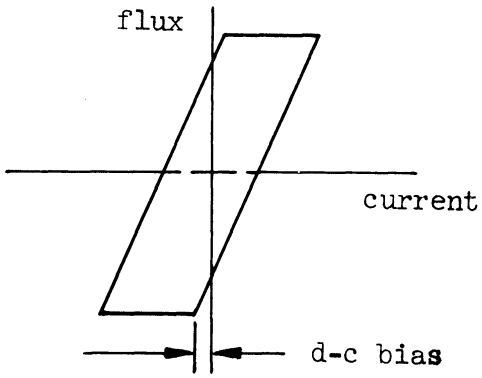
Knowing everything but R_{core} loss, it is possible to calculate the approximate magnitude of the effective core-loss resistance.

The frequency f_1 for any particular ferrite is a function of the mate-

rials and the proportions of the mixture. Materials such as MnZn ferrite, having high permeabilities and low resistivities, have in general a lower value of f_1 than materials such as NiZn ferrite (type Q material is a NiZn ferrite), which has a very high resistivity and a relatively small permeability.

For any particular circuit configuration, there are two factors which determine the optimum value of primary inductance and consequently the optimum core permeability. The first of these is the consideration of the magnetizing current drawn from the tube. From this viewpoint it is desirable that the primary inductance be as large as possible. In this case the magnetizing current is then small. The second consideration is concerned with the natural resonant frequency associated with the transformer. From noise and damping considerations it is desirable that the transformer have a resonant frequency which is equivalent to the highest repetition frequency which is to be encountered in the operation of the dynamic package. From this viewpoint it is then desirable that the transformer inductance be as small as possible. This is in direct conflict with the first consideration. For the above reasons it is obvious that ideally one desires a core material with a large permeability during the pulse and a small permeability after the pulse. If this is so the inductance will be large during the pulse and the magnetizing current will therefore be small. After the pulse the inductance will become small and consequently the resonant frequency will increase.

At first it was thought possible that the core material could be d-c biased so that the above described permeability characteristic could be obtained. Figure 3.7 will help illustrate the general idea of d-c biasing.



incremental permeability = slope of hysteresis curve at point under consideration.

Fig. 3.7. Idealized hysteresis loop.

From the above it is obvious that it is theoretically possible to bias the core material negatively so that the permeability of the core is high during the pulse and low after it. However, because 1) the core materials under consideration do not exhibit the abrupt change from high to low permeability as shown in Fig. 3.7, 2) the biasing current required for this operation is prohibitively large, 3) the capacitance associated with this d-c winding is very large, it has been determined that d-c biasing is not a practical approach to the problem.

In the process of testing the various cores and winding configurations, it has been observed that the tightness of the screw holding the two halves of the cup core together is a fairly critical factor in the determination of the primary inductance to be expected from any particular winding. If the screw is too loose, the reluctance of flux path through the core is increased due to the air gap, and the primary inductance thereby decreases. If the screw is made too tight, the material becomes stressed and the permeability decreases due to stress anisotropy. Between these two extremes there is a point at which the effective permeability of the core will be a maximum.

It is fairly obvious that a high-loss material will not operate as efficiently in a dynamic circuit as a low-loss material. The effective loss current drawn by the core material represents a definite decrease in the magnitude of the output current to be expected from a tube-transformer combination. However, even aside from the fact that a high-loss material is inefficient, it has been experimentally observed that there is another factor which dictates that the core material used in the dynamic circuit consist of low-loss material. While testing the various core materials in a dynamic flip-flop, it was observed that the core materials became quite hot when the loss was high. The resulting expansion was so large that the screw holding the two halves of the cup core together expanded past its elastic limit, and upon completion of the test and cooling of the pulse transformer, it was found that the two halves of the cup core were slightly loose. As mentioned above, this is undesirable because the primary inductance will decrease if the screw loosens. Therefore it is evident that the high-loss materials are not only less desirable for reasons of efficiency, but also for reasons of reliability.

3.2.1.3 Core Geometry.—At the outset of this investigation it was not obvious which type of core geometry, toroidal or cup core, was best suited for our application. If one compares the toroid and cup core on the basis of minimum reluctance per unit core volume, it appears that the toroid is best suited for our application. In actual practice, however, it is found that the leakage flux associated with a toroid core is prohibitively large. For this reason it has been decided that the cup core is the best geometry for our purposes.

In determining the optimum shape and dimensions of the cup core, there are two factors which must be considered: the reluctance associated with the core, and the leakage flux associated with the winding. There are many possible schemes one could use to reduce the reluctance associated with the core. The simplest of these consists of varying the core post radius. A simplified analysis consisting of the computation of the reluctance versus core post radius has shown that it is desirable that this radius be as large as possible. In the limit this means that the core post radius should approach the inner radius of the outer wall of the cup core. The main factor determining the magnitude of the leakage flux is the proximity of the winding to the core. If the winding fits the core tightly, the leakage will be a minimum. From these considerations it is obvious that the best cup-core geometry is one in which the core window area is just large enough to accommodate the winding.

3.2.2 EQUIVALENT CIRCUIT

In order that one may gain further insight into the relationship between transformer response and the various transformer parameters, it is desirable that the transformer be represented by an equivalent circuit. There are many equivalent circuits of varying complexity which can be used to represent the transformer. At the one extreme one can consider a circuit of distributed capacitances and inductances, whereas at the other extreme one can consider a simple RLC circuit. The criteria for the selection of a particular equivalent circuit must be a compromise between simplicity and an adequate representation of transformer response. It has been determined by observation of the transformer response under various conditions of load and stray parameters that an adequate equivalent circuit consists of a parallel RLC circuit with the addition of a series leakage inductance. This circuit and a brief explanation of the nature of the circuit parameters is shown in Fig. 3.8.

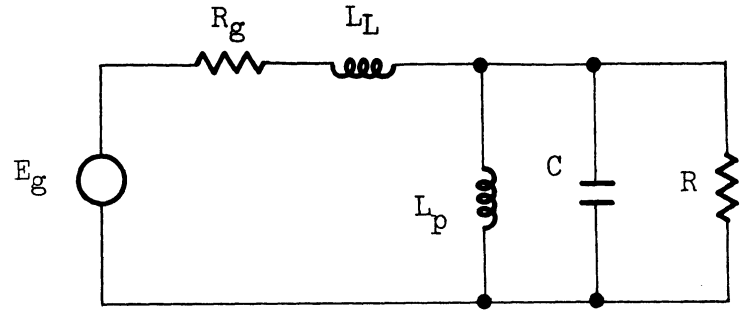


Fig. 3.8. Transformer equivalent circuit.

where

R_g = source resistance,
L_L = transformer leakage inductance,
C = parallel combination of: C_{xfmr}, C_{tube}, C_{wiring}, and C_{sec}/n^2,
L_p = transformer primary inductance, and
R = parallel combination of: n^2R_{load} and R_{core}.

The above equivalent circuit may be simplified by dividing the pulse response into three separate regions corresponding to the rise, top, and fall of the pulse. Since the frequency spectrum for the leading edge of the pulse is composed predominantly of very high frequencies, one may analyze the pulse rise by making use of the high-frequency equivalent of the basic circuit. This circuit consists of the series leakage inductance and the parallel RC combination. For a similar reason the equivalent circuit for the top of the pulse is the low-frequency equivalent of the basic circuit. Since the leakage reactance is negligible and the capacitive reactance is large at low frequencies, the pulse-top response can be adequately represented by a parallel RL combination. The equivalent circuit for the fall and the pulse tail consists of a parallel RLC circuit.

Using the above equivalent circuits and a knowledge of the various circuit parameters, it is possible to calculate the transformer response under varying conditions. The rise circuit reveals that the leading edge of the pulse is

determined to a large extent by the leakage inductance and the capacitance associated with the circuit. Large values of leakage inductance and capacitance lower the rate of rise of the leading edge of the pulse and also introduce oscillations on the top of the pulse which are sometimes undesirable. Using the low-frequency equivalent circuit, it is possible to calculate the droop associated with transmission through the transformer. It should be noted, however, that the transformer is not the only factor contributing to pulse droop. One must also consider the inherent droop associated with the tube characteristics. As the transformer magnetizing current increases, the point of operation moves along the tube characteristics with a resulting pulse droop. The droop associated with a properly designed transformer is in the neighborhood of four to five percent of the pulse amplitude, whereas that associated with the tube characteristics may be appreciably larger.

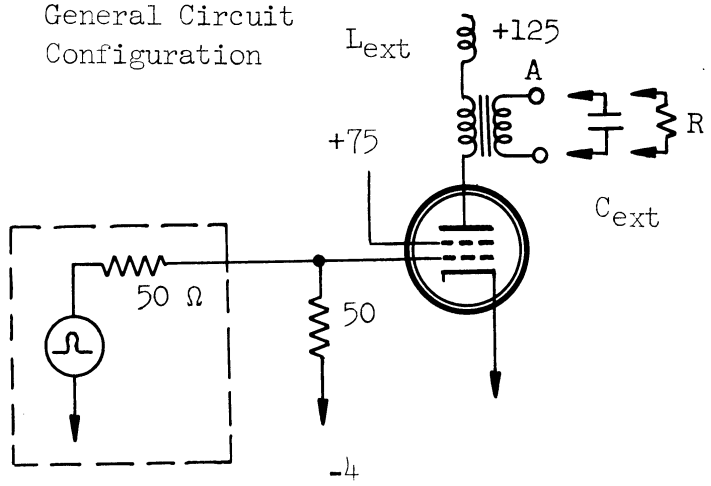
The parallel RLC circuit is very useful because it enables one to determine easily the optimum damping resistance for any particular transformer, and it also affords one a means of determining the natural resonant frequency of the undamped transformer. In fact, the parallel RLC circuit is entirely sufficient for the representation of the entire pulse response when a simplified general analysis is desired. The pulse transformer-amplifier analysis included in this section assumes, for simplicity's sake, that such a circuit is valid. This is true as long as it is remembered that the analysis is slightly optimistic in that the harmful effects of leakage inductance are ignored. (Refer to Appendix E for an illustration of the procedure followed in analyzing a transformer-tube configuration.)

Perhaps the most convincing verification of the above equivalent circuits are the pictures (Fig. 3.9) taken under experimental conditions. The pictures of the pulse response of the various winding configurations reveal that those windings with large values of leakage inductance and capacitance have, as is to be expected, lower rates of rise and more pronounced ringing on the pulse top than those with relatively small stray parameters. Pictures of the pulse response when the stray parameters were externally increased by the addition of inductance and capacitance are also included. These pictures also verify the strength of the equivalent circuit as an adequate means of representing the transformer pulse response.

3.2.3 WINDING

The selection of a particular type of winding is governed by the stray parameters associated with that winding. Of the seven winding configurations tested, it has been observed that a simple layer-type winding has the best pulse characteristics (see Fig. 3.11 for illustration of the seven winding types considered). The reason for this is that a layer-type winding minimizes leakage inductance and yet does not exhibit an excessively high value of interwinding capacitance even if insulation between windings is eliminated.

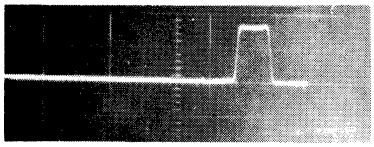
General Circuit Configuration



epic pulser

20:2-type "Q" core

All pictures 10 v/cm, 0.1 μsec/cm and taken at pt "A" unless otherwise noted.



input to grid
5 v/cm
0.1 μsec/cm

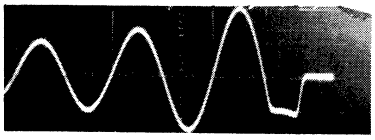
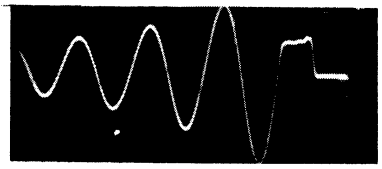
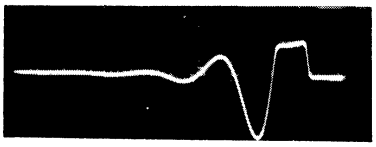


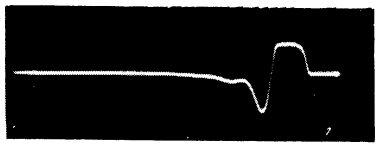
plate waveform;
open sec
100 v/cm
0.1 μsec/cm



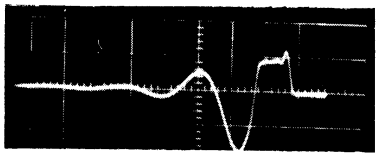
L_{ext} = 0
C_{ext} = 0
R = ∞



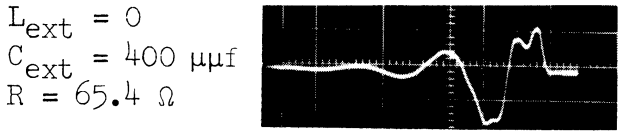
L_{ext} = 0
C_{ext} = 0
R = 65.4 Ω



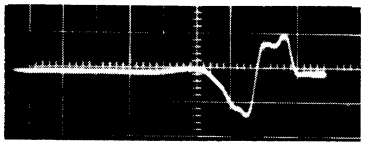
L_{ext} = 0
C_{ext} = 0
R = 15.7 Ω



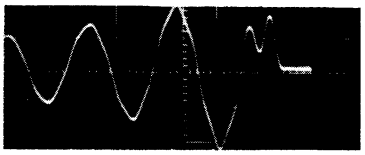
L_{ext} = 0
C_{ext} = 100 μμf
R = 65.4 Ω



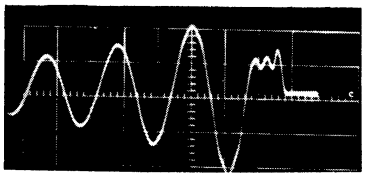
L_{ext} = 0
C_{ext} = 400 μμf
R = 65.4 Ω



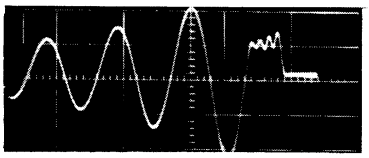
L_{ext} = 0
C_{ext} = 400 μμf
R = 32.7 Ω



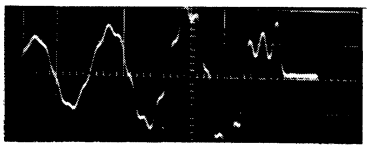
L_{ext} = 0
C_{ext} = 400 μμf
R = ∞



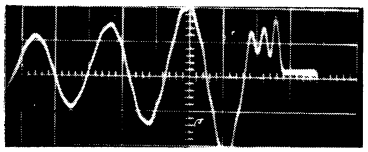
L_{ext} = 11 μh
C_{ext} = 0
R = ∞



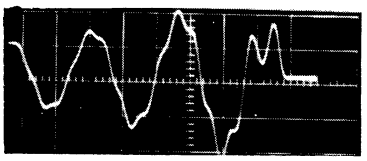
L_{ext} = 5.4 μh
C_{ext} = 0
R = ∞



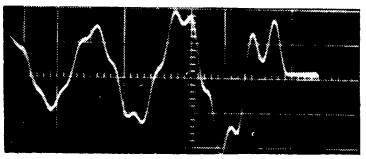
L_{ext} = 11 μh
C_{ext} = 100 μμh
R = ∞



L_{ext} = 5.4 μh
C_{ext} = 100 μμh
R = ∞



L_{ext} = 5.4 μh
C_{ext} = 400 μμf
R = ∞



L_{ext} = 11 μh
C_{ext} = 400 μμf
R = ∞

Fig. 3.9. Pulse response when the magnitude of the stray parameters is increased.

In order that one may be assured of reliable and reproducible performance, care must be taken in the manner in which the transformer is wound. The positive secondary should be wound closest to the core post with the primary wound in a neat, orderly, solenoidal fashion over it. The negative secondary is then wound on top of the primary. It is also quite important, from the viewpoint of interwinding capacitance, that the leads be placed so that the voltage gradient between the ends of any two leads be a minimum. Figure 3.10 illustrates the final winding form.

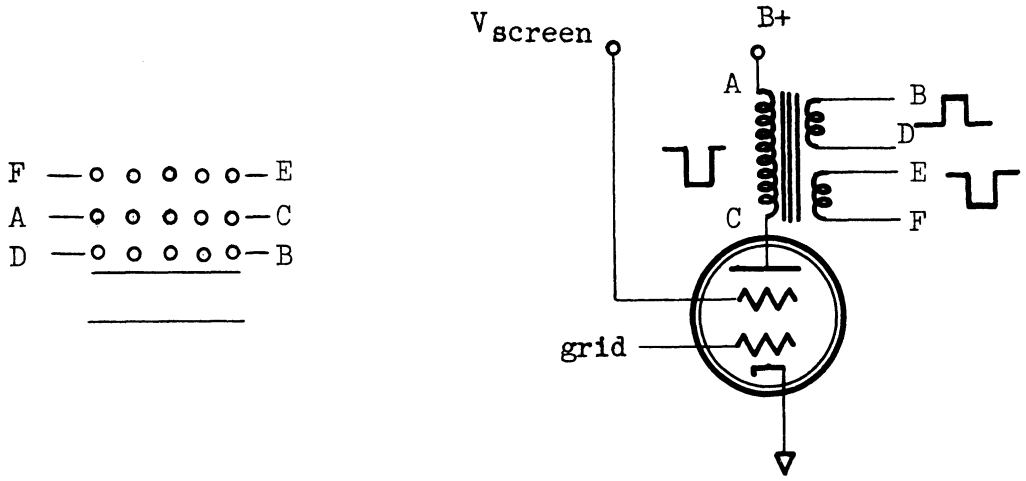


Fig. 3.10. Final winding form.

The stray parameters associated with the layer-type winding have been both measured and calculated. In general one can expect a leakage inductance in the range of one to four percent of the primary inductance and a shunt capacitance of the order of three to five μμf. The calculation of the capacitance involves the determination of the dynamic energy storage within the winding under a pulsed condition, and the calculation of leakage inductance involves the determination of the energy storage within the winding when the secondary is short circuited.[10] The accuracy of these calculations should not be relied upon too heavily. However, they do give one an idea of the order of magnitude of the stray parameters associated with any particular winding. The best means of determining the magnitude of the stray parameters are by the measurement techniques discussed below.

The methods found most useful for the measurement of the stray parameters involved the use of a Q meter for the leakage measurements and an undamped transformer for capacitance measurements. The leakage measurements simply involved short-circuit measurements of the input inductance of the transformer. The capacitance measurements were somewhat more involved; it is necessary to measure transformer capacitance under pulsed conditions since the capacitance of interest is not the d-c capacitance of the winding but is the dynamic capacitance due to the voltage gradient between windings. The circuit shown in Fig. 3.12 was used to measure the dynamic capacitance.

The purpose of the tube is to insure that the source impedance is very

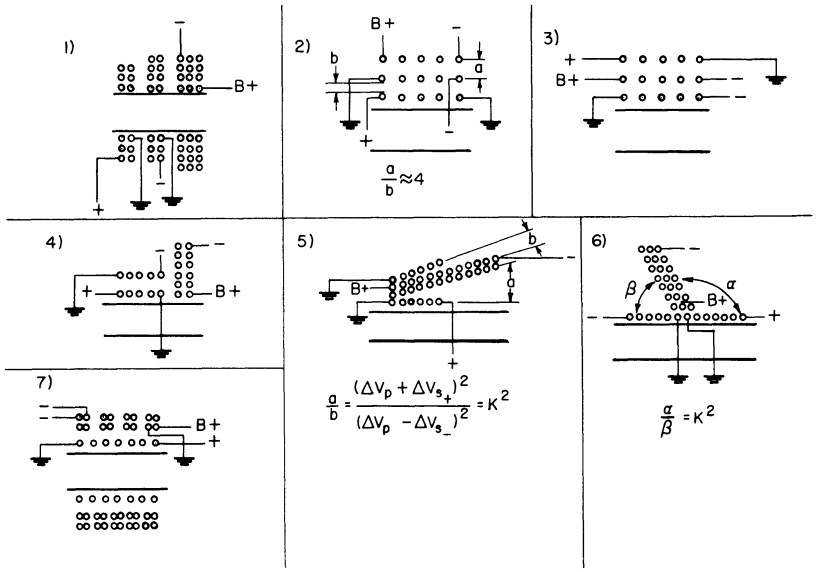
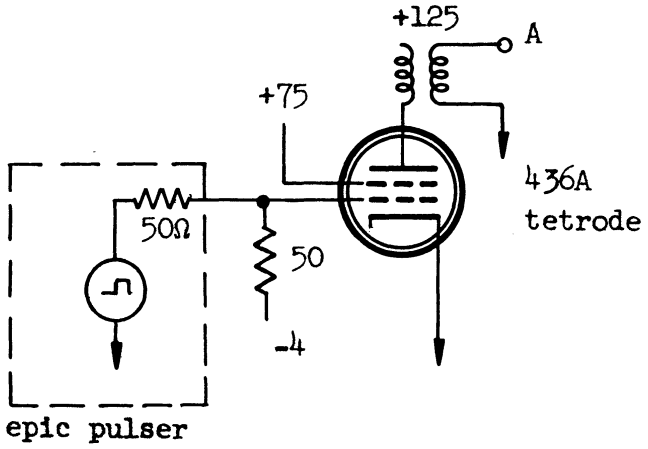


Fig. 3.11. Winding configurations.



Pictures of pulse at point "A" taken using Land camera and Tektronix 545 scope give frequency f (see below).

Fig. 3.12. Circuit for measurement of dynamic capacitance.

large after the pulse. If this is so, the transformer secondary will ring with a resonant frequency given by:

$$f = 1/2\pi \sqrt{L_p C}$$ (L_p and C as defined in section on equiv. circuit.)

Knowing all the variables in the resonant frequency equation except the magnitude of transformer capacitance, it is possible to arrive at a good estimate for the value of transformer capacitance.

3.2.4 GENERAL TRANSFORMER-DESIGN PROCEDURE

A simplified transformer-design procedure is given below. This procedure may be used to obtain an estimate of the order of magnitude of the transformer parameters required for any particular pulse application. The final design will be dependent upon the modifications which experimental tests of the initial design indicate are necessary.

(1) Knowing

ΔI = current "swing" available from the tube,
C_t = primary capacitance which consists of the parallel combination of tube, wiring, and transformer capacitance,
f_p = pulse repetition frequency,
E_L = required secondary output, and
C_s = secondary capacitance (load),

Compute

$$N_{opt} = \text{optimum turns ratio}$$

$$= \frac{23\Delta I}{70\pi^2 C_t f_p E_L}$$

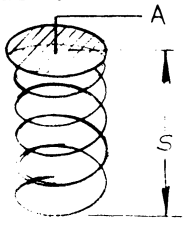
$$L_P = \frac{N_{opt}^2}{4\pi^2 f_p (C_s + N_{opt}^2 C_t)} .$$

(2) Choose a core material which has a high resistivity and a reasonable permeability (something similar to type Q material for our application).

(3) Knowing the core permeability, compute the required primary turns:

$$N_P \cong \left(\frac{L_P s}{\mu A} \right)^2$$

s = winding length,
A = winding area, and
μ = core permeability.



4. INTERCONNECTION AND DELAY LINES

4.1 Interconnection Problem

This section represents a study of the interconnection between a package output and gate inputs. Specifically, the problem considered is the connection of one package output to n different gate inputs.

There are two possibilities of interconnection. The first one employs n cables, each one terminated at the gate input. This arrangement is shown in Fig. 4.1. In general it will be necessary to add a delay network as indicated to bring the gate input into the proper phase.

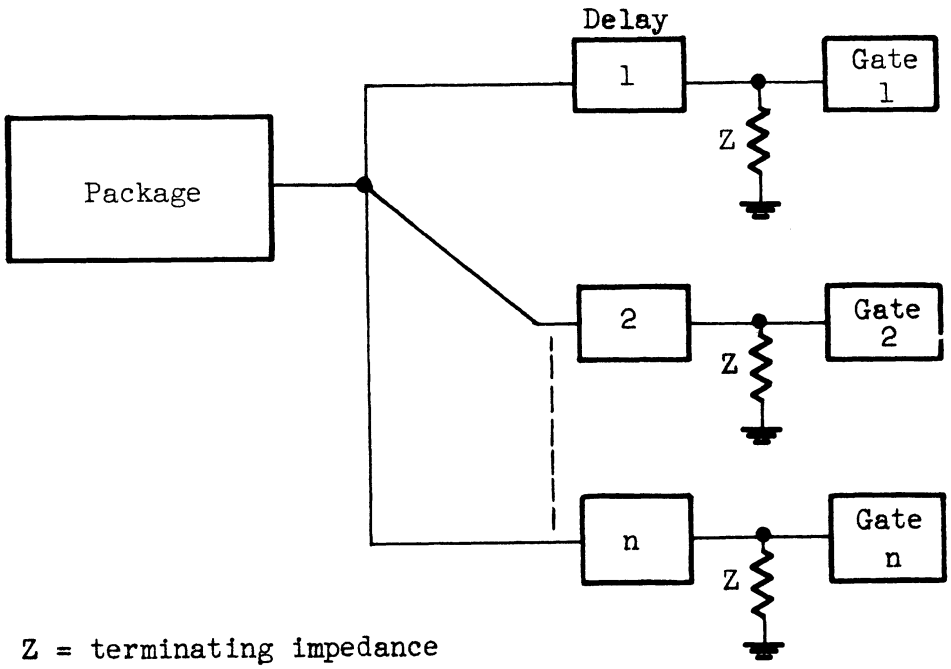


Fig. 4.1. Interconnection through n terminated cables.

The second alternative of interconnection consists of using a singly terminated cable with each gate input tapped off at n different points of the cable. This arrangement is shown in Fig. 4.2.

4.2 Interconnection Through n Terminated Cables

For the n terminated cable configuration, the following obtains for

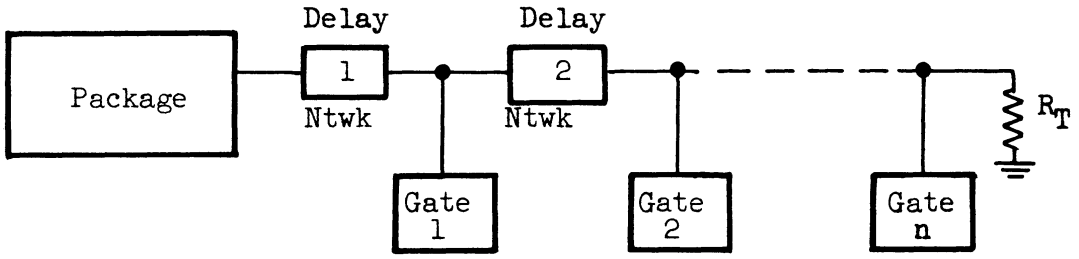


Fig. 4.2. Interconnection through singly terminated cable.

terminating impedance, power, etc.

Let

R_o = characteristic impedance of the cable,
I_K = input current to the k'th gate, and
E_K = input voltage to the k'th gate;

then $$Z_K = E_K/I_K = m \cdot R_o ,$$

where m may be a real or a complex number.

Since it is desired to terminate each gate to give maximum power transfer, an impedance Z is connected in parallel with each gate.

Then

$$R_o = \frac{Z_K Z}{Z_K + Z}$$

$$= \frac{mR_o \cdot Z}{mR_o + Z} .$$

Solving for the terminating impedance Z:

$$Z = \frac{m}{m - 1} R_o .$$

In general, the power dissipated in the k'th gate is given by

$$P_K = I_K^2 \, \mathrm{Re}[Z_K] = \left(\frac{E_K}{Z_K}\right)^2 \mathrm{Re}[Z_K] \qquad (4.1)$$

and the power loss in Z:

$$P_{K_L} = \left(\frac{E_K}{Z}\right)^2 \mathrm{Re}[Z] \qquad (4.2)$$

For simplicity's sake, the gate input impedance can be considered to be purely resitive. Then

$$Z_K = R_K = mR_o ,$$

and m in this case is a real number. Then also

$$Z = \frac{m}{m-1} R_o = R$$

is purely resistive.

Then (4.1) reduces to

$$P_K = \frac{E_K^2}{R_K} = \frac{E_K^2}{mR_o} ,$$

and (4.2) becomes

$$P_{K_L} = \frac{E_K^2}{R} = \frac{E_K^2}{mR_o}(m-1) = \frac{E_K^2}{R_o}\left(1 - \frac{1}{m}\right) .$$

The total power delivered to the gate and to the matching resistor is

$$P_T = P_K + R_{K_L} = \frac{E_K^2}{mR_o} + \frac{E_K^2}{R_o}\left(1 - \frac{1}{m}\right) = \frac{E_K^2}{R_o} .$$

Therefore

$$\% \text{ power loss in } R = 100 \times \frac{\text{power loss in } R}{\text{total power}} =$$

$$= 100 \times \frac{P_{K_L}}{P_T} = \frac{\frac{E_K^2}{R_o}\left(1 - \frac{1}{m}\right)}{E_K^2/R_o} \times 100 =$$

$$= 100(1 - 1/m) .$$

For no loss

$$1 - 1/m = 0$$

$$m = 1 .$$

Therefore, for no loss, it is necessary to make the gate impedance equal to the characteristic impedance of the cable.

If a maximum of 10% losses could be tolerated,

$$1 - \frac{1}{m} \leq .1$$

or

$$m \leq 1.11 .$$

Hence, for less than 10% power loss, the gate resistance should not exceed the characteristic resistance by more than 11%.

The above conclusion causes certain engineering difficulties. It appears that one has two choices: (1) in selection of a cable so that its R_o will be approximately equal to R_K, the gate resistance; or (2) in the design of a gate package so that its input impedance will be approximately equal to R_o. Unfortu-

nately, however, the variation of R_o and R_K is limited. The reasons for this are as follows. In general, it is desirable to have as little delay in the cable as possible. Delay per unit length is given by $\sqrt{LC}$. Therefore, small delay requires small L and/or C. Capacity C cannot be decreased beyond a certain fixed value; hence, L itself must be small. Then $R_o = \sqrt{L/C}$ will be low. Therefore the gate input resistance R_K should be low. For low R_K, ($R_K = E_K/I_K$), I_K must be large and/or E_K small. Large I_K will yield large losses in the gate, causing low gate efficiency. To avoid these losses, it is desirable to operate the gate at as low a value of current as possible. In addition, there is a very definite limit on the package output current, due to the tube and transformer limitations, and it is desired to drive as many gates as possible. Consequently, the current per gate must be low. These considerations impose the requirement that E_K, the gate voltage, be low. But a certain minimum voltage must be provided for the preservation of wave shape. It consequently follows that, if this termination is utilized, some engineering compromise must be made. An example using typical values for voltage, current, etc., follows:

Let $E_K = 4$ v
$I_K = 12$ ma

with RG-58/U cable, $R_o = 53\ \Omega$;

then

$$R_K = \frac{4}{12} \times 10^3 = 333\ \Omega ,$$

and

$$m = 333/53 = 6.3 .$$

$$\% \text{ power loss in } R = \left(1 - \frac{1}{m}\right) \times 100 = 84.2\% .$$

Therefore it is seen that, for these realistic values, only 15.8% of the available power will be consumed in the gate. Evidently, the great power loss will make this termination prohibitive. Therefore interest must be focused on the second possibility of termination.

4.3 Interconnection Through Singly Terminated Cable

When the interconnection between packages is accomplished by tapping off a single line, it is found that at any k'th tap point of the cable, the line will see a parallel combination of R_o and R_K, instead of R_o. Consequently, a discontinuity at the tap point will occur which will give rise to reflections.

As before $$R_K = \frac{E_K}{I_K} = mR_o ;$$

then the impedance seen at the discontinuity is

$$R_D = \frac{(mR_O)R_O}{R_O + mR_O} = \left(\frac{m}{m+1}\right) R_O \quad .$$

For no reflections,

$$R_D \approx R_O \quad \text{or} \quad \frac{m}{m+1} \rightarrow 1 \ ,$$

or

$$m \rightarrow \infty$$

for any finite m.

The reflection coefficient at any tap point is

$$\rho = \frac{\frac{R_D}{R_O} - 1}{\frac{R_D}{R_O} + 1} = \frac{\frac{m}{m+1} - 1}{\frac{m}{m+1} + 1} = -\frac{1}{2m+1} \quad .$$

Consequently $[1/(2m + 1)]$ of the input wave is reflected back to the sending end, and only $[2m/(2m + 1)]$ of the input wave is transmitted.

For a termination at the last tap:

$$R_O = \frac{R_T(mR_O)}{R_T + mR_O} \quad \text{or} \quad R_T = \frac{m}{m-1} R_O \ ,$$

where R_T is the terminating resistor.

The transmitted and reflected wave both experience a phase shift and attenuation in transmission. This phase shift and attenuation arise in both the cable and delay network. In general the attenuation is given by

$$\alpha_K = \alpha'_K + \alpha \cdot \ell_K \ ,$$

where

α_K = total attenuation of the k'th cable and the k'th delay network,
α'_K = attenuation of the k'th delay network,
α = attenuation factor of cable per unit length, and
ℓ_K = length of k'th cable.

Similarly,

$$t_K = t'_K + t \cdot \ell_K \ ,$$

where

t_K = total time delay of the k'th cable and the k'th delay network,
t'_K = time delay of the k'th delay network, and
t = time delay factor of cable per unit length.

Then, considering only the forward wave, if

$$E_{in} = \text{input voltage wave,}$$

$$E_1 = \text{voltage wave leaving the first discontinuity} =$$

$$= E_{in}\left(\frac{2m}{2m+1}\right) e^{-\alpha_1} e^{-st_1} \quad .$$

Hence, at the end of the line or the termination (after n'th discontinuity)

$$E'_n = \left(\frac{2m}{2m+1}\right)^n e^{-(\alpha_1 + \alpha + \ldots + \alpha_n)} e^{-s(t_1 + t_2 + \ldots + t_n)} =$$

$$= \left(\frac{2m}{2m+1}\right)^n e^{-\sum_{i=1}(\alpha_i + st_i)} = \left(\frac{2m}{2m+1}\right)^n e^{-\sum_{i=1} \alpha_i} u\left(t - \sum_{i=1}^{n} t_i\right) . \quad (4.3)$$

The above equation does not reveal the entire picture, since there are multiple reflections at every discontinuity, which Eq. (4.3) does not take into account.

The general mathematical expression for the voltage (or current) wave at the k'th discontinuity under matched conditions at the sending and receiving ends is given by*:

$$E_K = \left\{ \sum_{v=0}^{\infty} E_{in}\left(\frac{2m}{2m+1}\right)^{k-1}\left(\frac{1}{2m+1}\right)^{2v} e^{-\sum_{i=1}^{K}(1+2v)\alpha_i} \right.$$

$$\left. \cdot\, u\left[t - \sum_{i=1}^{K}(1+2v)t_i\right] \right\} (1 - \Phi) \quad , \qquad (4.4)$$

where

$$\Phi = \sum_{\ell=K+1}^{n-1} \left\{ \sum_{r=0}^{\infty} \left(\frac{2m}{2m+1}\right)^{2(\ell-K)} \left(\frac{1}{2m+1}\right)^{1+2r} \right.$$

$$\left. \cdot\, e^{-2\sum_{j=k+1}^{\ell}(1+r)\alpha_j} \cdot u\left[t - 2\sum_{j=K+1}^{\ell}(1+r)t_j\right] \right\} \quad .$$

*The derivation of (4.4) is given in Appendix G.

In a practical case, several terms of expression in Eq. (4.4) will suffice, since the series is strongly convergent, due to the exponential term. A general solution for n discontinuities, even with this convergence, will require a sizable amount of computing time. Hence, an experimental model was built for the purpose of studying reflections with this type of termination. This experimental model is shown in Fig. 4.3.

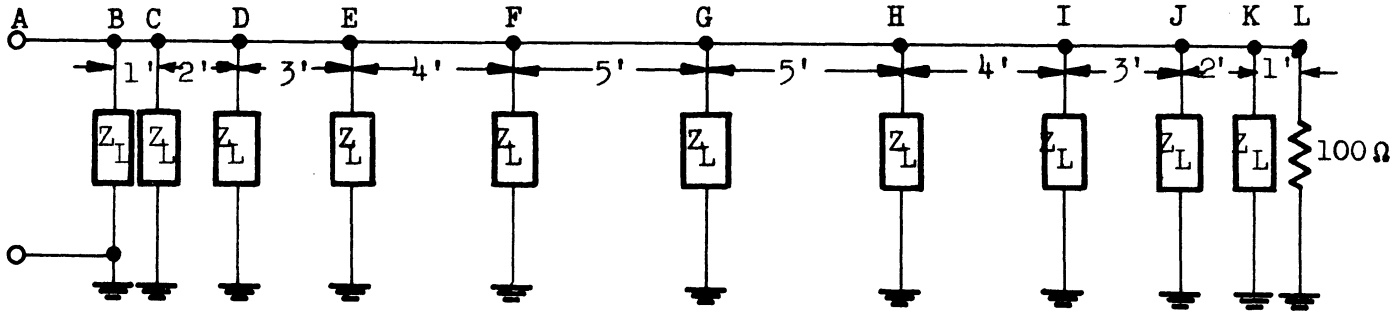


Fig. 4.3. Experimental model for reflection study.

The cable used was RG 62/U, which has the following characteristics:

$$C = 13.5\ \mu\mu f/ft$$

$$Z_o = 93\ \Omega$$

$$\text{attenuation} = .05\ db/ft$$

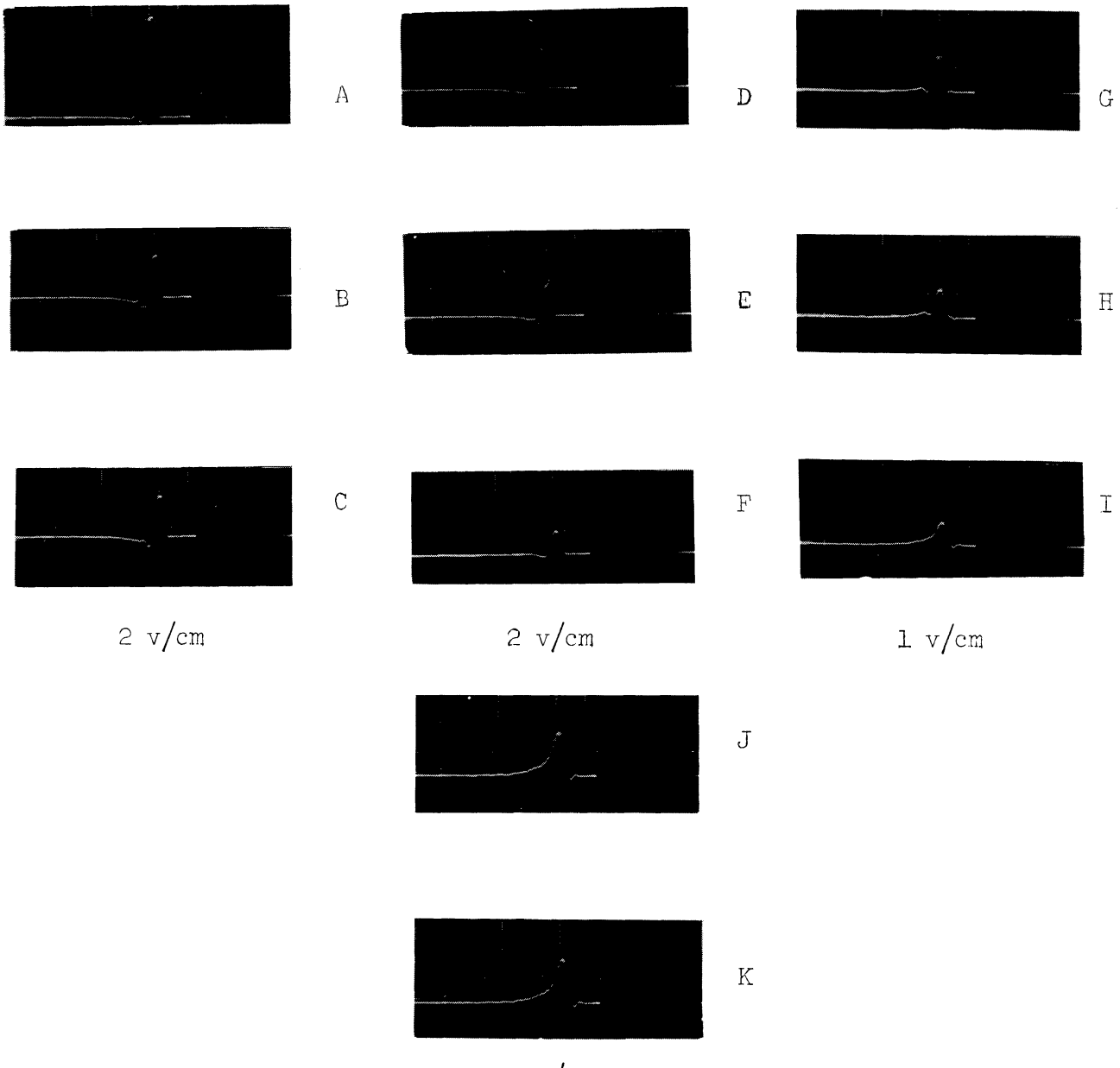
the following impedances are employed for Z_L:

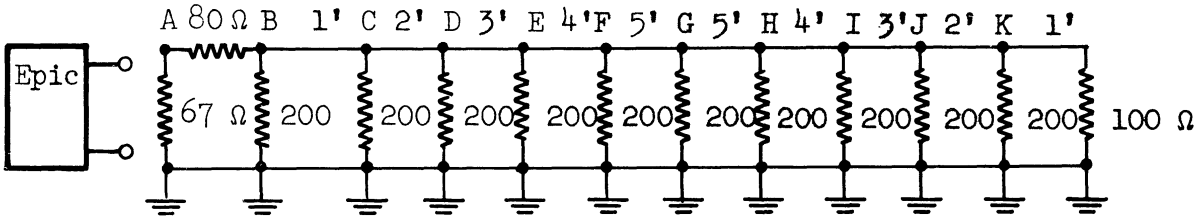
(a) a resistance of 200 Ω
(b) a resistance of 470 Ω
(c) a resistance of 560 Ω
(d) series connection of Raytheon IN295 diode and 500 Ω resistance (forward resistance of IN295 is approximately 75 Ω).

As indicated in Fig. 4.3, the cable length between discontinuities varied from 1 to 5 feet. For simplicity's sake, the delay network that will generally be connected between any two taps was omitted since such a network will not contribute (if properly matched) to reflections, but only to delay and attenuation.

4.3.1 200 Ω LOAD

A square pulse was applied through a matching network. The oscilloscope patterns were photographed at each terminal. As seen from Fig. 4.4, there is a fair reproduction of wave form up to terminal E, which represents a drive of 4 loads. Beyond E the rise time increases substantially, which results in poor wave shape. This distortion of wave shape is expected, since the ratio of load imped-





Cable: 62/U Cap/ft = 13.5 μμfd Z_o = 93 Ω
Epic must be terminated in 50 Ω $Z_{out\ epic}$ = 150 Ω

Fig. 4.4. Wave patterns with a 200 Ω load.

ance to the characteristic impedance is only m = 200/93 = 2.15.

The attenuation is shown in Table 4.1 in percent of input wave form (voltage at terminal B = 100%). As is seen from Table 4.1, there is essentially no attenuation at terminals C and D, and approximately 21% loss at terminal E. In general the conclusion can be drawn that with m = 2 the above termination is not advisable.

TABLE 4.1

ATTENUATION FOR 200 Ω LOAD

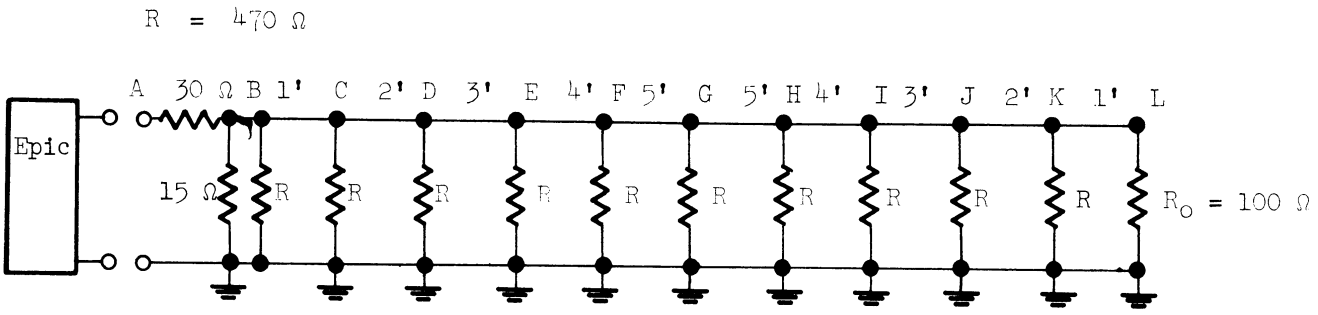
Terminal	Percent of Input	Percent Attenuation
B	100	0
C	100	0
D	100	0
E	78.5	21.5
F	57.0	43.0
G	43.7	56.3
H	35.6	64.4
I	28.5	71.5
J	26.6	73.4
K	26.6	73.4

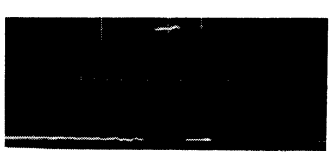
4.3.2 470 Ω LOAD

With this load, m = 470/93 = 5.05, and a marked improvement is observed in the oscillograph patterns at each terminal. These patterns are presented in Fig. 4.5, and if can be noted that the wave is relatively well preserved up to Terminal I, or for 8 discontinuities (8 loads). The rise time does not increase appreciably for the first four discontinuities, but from there on it does. For Terminals F through I, an improvement in rise time could be obtained through clamping. The attenuation data, presented in Table 4.2, shows that even with 11 loads there is no more than 36.4% attenuation of the input wave.

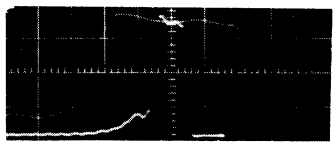
4.3.3 560 Ω LOAD

This higher load brought about an improvement of wave shapes at each discontinuity, as was expected (m = 560/93 = 6.03). The oscilloscope patterns are presented in Fig. 4.6. The rise time is essentially constant for the first five discontinuities (B through F), and not substantially greater at terminals G through I. As stated earlier, a partial preservation of rise time can be obtained through clamping.

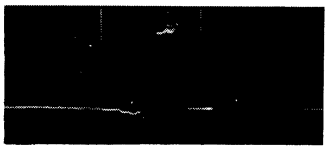




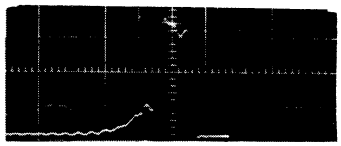
A
5 v/cm



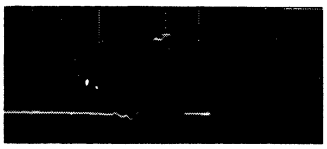
G
1 v/cm



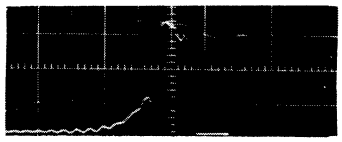
B
2 v/cm



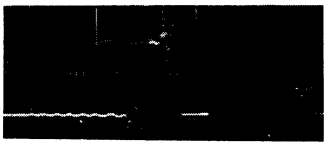
H
1 v/cm



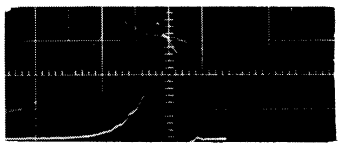
C
2 v/cm



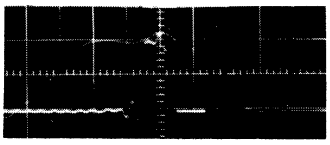
I
1 v/cm



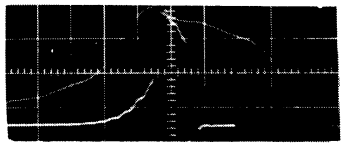
D
2 v/cm



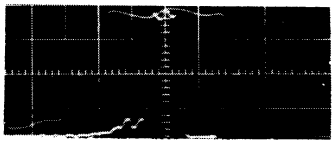
J
1 v/cm



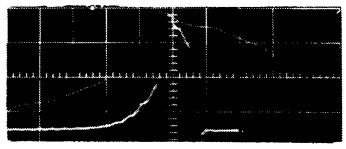
E
2 v/cm



K
1 v/cm

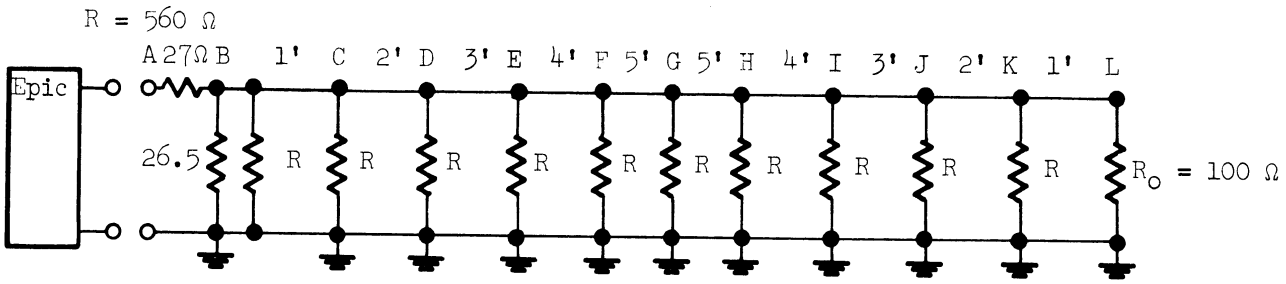


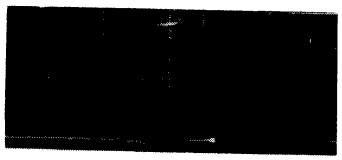
F
1 v/cm



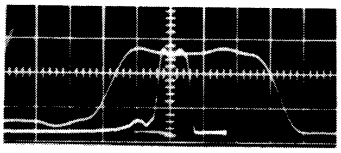
L
1 v/cm

Fig. 4.5. Wave patterns with a 470 Ω load.



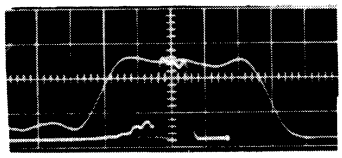


A
5 v/cm

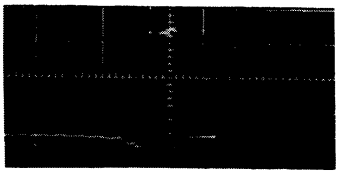


G
2 v/cm

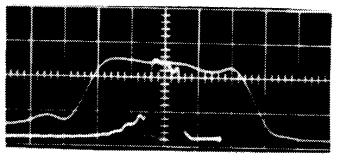
B
2 v/cm



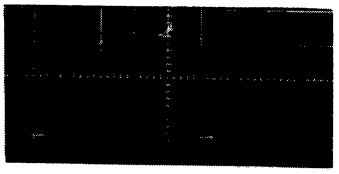
H
2 v/cm



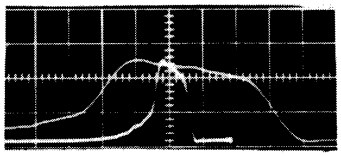
C
2 v/cm



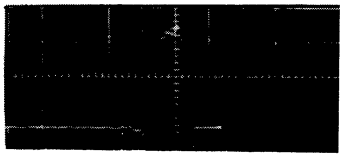
I
2 v/cm



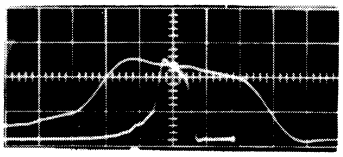
D
2 v/cm



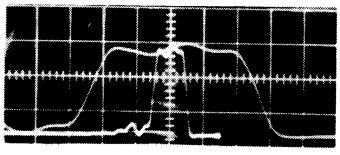
J
2 v/cm



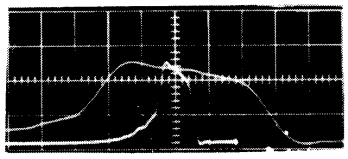
E
2 v/cm



K
2 v/cm



F
2 v/cm



L
2 v/cm

Fig. 4.6. Wave patterns with a 560 Ω load.

TABLE 4.2

ATTENUATION FOR 470 Ω LOAD

Terminal	Percent of Input	Percent of Attenuation
B	100	0
C	100	0
D	100	0
E	91	9
F	82	18
G	72.6	27.4
H	72.6	27.4
I	63.6	36.4
J	63.6	36.4
K	63.6	36.4
L	63.6	36.4

The attenuation data presented in Table 4.3 show little change from that of Table 4.2. The table indicates that this termination allows the system to drive at least 8 loads with adequate power transfer.

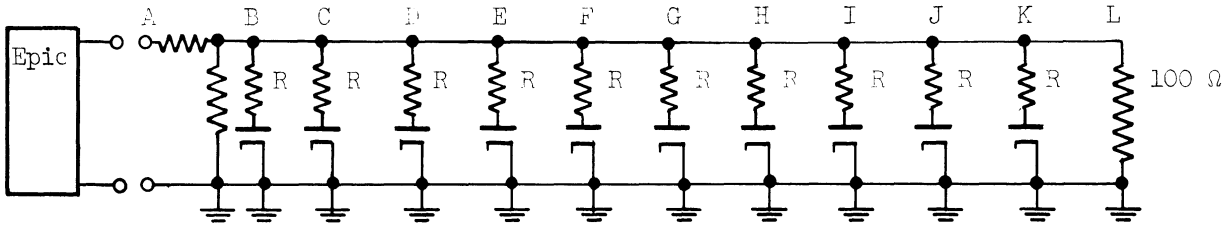
TABLE 4.3

ATTENUATION FOR 560 Ω LOAD

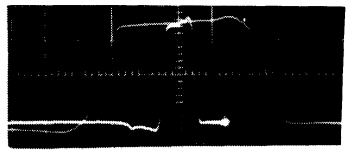
Terminal	Percent of Input	Percent Attenuation
B	100	0
C	100	0
D	100	0
E	93.6	6.4
F	80.6	19.4
G	77.5	22.5
H	71.0	29.0
I	71.0	29.0
J	64.5	35.5
K	64.5	35.5
L	64.5	35.5

4.3.4 RESISTOR-DIODE LOAD

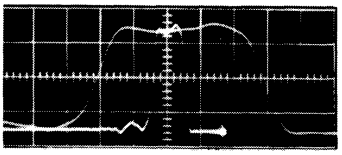
The resistor was 500 Ω and the diode was a Raytheon IN295 (forward resistance 75 Ω). The series connection of these two presented little change from the preceding 560 Ω load. The oscilloscope patterns are shown in Fig. 4.7, and comparison between these and those of Fig. 4.6 reveals that the reproduction of



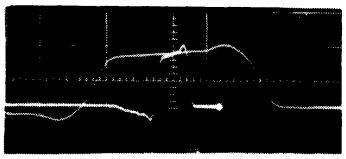
Diodes are Raytheon IN295 (forward resistance = 75 Ω)
R = 500 Ω



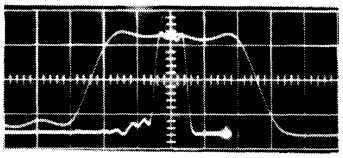
A
5 v/cm



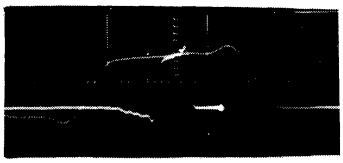
G
2 v/cm



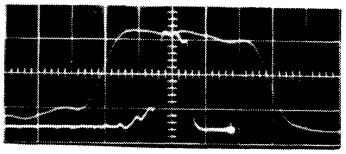
B
5 v/cm



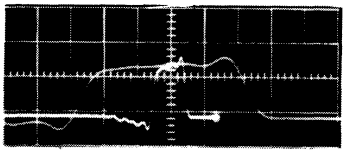
H
2 v/cm



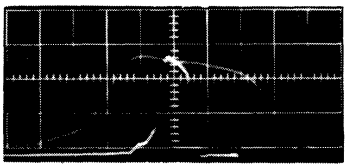
C
5 v/cm



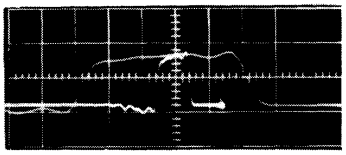
I
2 v/cm



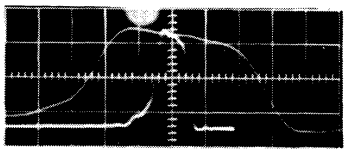
D
5 v/cm



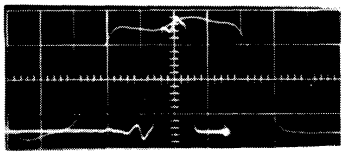
J
2 v/cm



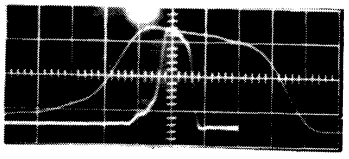
E
5 v/cm



K
2 v/cm



F
2 v/cm



L
2 v/cm

Fig. 4.7. Wave patterns with a resistance-diode load.

input is certainly no worse and at least 8 loads are permissible. The attenuation data shown in Table 4.4 again exhibits little departure from the two previous cases.

TABLE 4.4

ATTENUATION FOR RESISTANCE-DIODE LOAD

Terminal	Percent of Input	Percent Attenuation
B	100	0
C	100	0
D	100	0
E	87.5	12.5
F	80.0	20.0
G	75.0	25.0
H	70.0	30.0
I	70.0	30.0
J	67.5	32.5
K	67.5	32.5
L	67.5	32.5

It must be kept in mind that in actual practice delay networks would also be included in the interconnection configuration just described. The non-simplified circuit could possibly cause a modification of final conclusions with respect to the number of loads possible and the preservation of wave shapes. However, the test cable employed does not have the best bandwidth and attenuation properties of commercially available cables, and hence the test results should basically be representative of what can be expected in actual practice. Consequently, if interconnection with cables is deemed necessary, the interconnection through a singly terminated cable will yield the most satisfactory results.

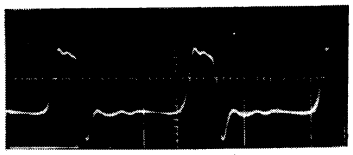
4.4 The Delay Network

The delay necessary in the computer for proper time phasing of the inputs to the gating structure can be accomplished in several ways. Only the two most readily available ways were investigated under this contract. The first method employs delay lines of the proper length, and the second method utilizes a delay network made up of lumped elements.

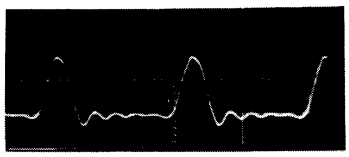
Due to the ease of acquisition, a commercial delay network of the proper bandwidth was purchased and tested. The delay network, manufactured by Advance Electronic Laboratories (Type 8T-300a), was chosen on the basis of its bandwidth, characteristic impedance, and attenuation. The input and output wave patterns for the network are shown in Fig. 4.8. This network consists of 20 m-derived sections,

and possesses an adequate bandwidth for sufficiently fast rise times.

It will be shown in Section 5 that if the delay network is not utilized, a 300 Ω cable is necessary for maximum power transfer for the voltage and current levels suggested. Such a cable is not presently available commercially. Therefore, if the number of gate drives is critical, i.e., if there is no power to be wasted, it is deemed necessary to use the commercial delay networks.



Input wave shape



Output wave shape

Fig. 4.8. Delay network patterns for 100 mμsec delay.

5. FUNCTIONAL CIRCUITRY

5.1. Introduction

In this section the final phase of the project is realized, i.e., the incorporation of all the previous phase results into functional computer units. Section 5.2 deals with the incorporation of the basic package into a pulse generator and a minor cycle counter. In Section 5.3 the requirements of a standard package and delay terminations are outlined for a specific case. The experimental results of this research should serve as a guide post for future research and should not be taken as the ultimate in diode-tube-transformer design due to the ever changing state-of-the art of the aforementioned components.

5.2. Incorporation of the Basic Package into Functional Computer Units

To complete the final phase of the project, a T_4 pulse generator and a minor cycle counter were built to demonstrate the functional performance of the basic package. Figure 5.1 is a block diagram of this equipment and is intended as a guide to the physical interconnection of the packages.

The minor cycle counter counts the T_4 pulses, modulo 16, generated by the timing generator. The three packages composing the minor cycle counter implement the logical function:

$$S = \overline{(\bar{S}_{-4}T_4C_{-1} + S_4\bar{T}_4C_{-1} + S_4T_4\bar{C}_{-1})}(S_{-4} + T_4 + C_{-1})$$

where

S = sum digit,

S_{-4} = sum digit from the previous count,

C_{-1} = carry digit, and

T_4 = output timing pulse of the timing generator.

The wave forms are shown in Fig. 5.2 and they are referenced to Fig. 5.1 with capital letters A through E. The reader will notice the count 1000 is missing from the sum output. This error does not represent a malfunction of the equipment, but results from a failure to destroy the carry digit at time T_{64}. It

was felt that the additional equipment needed to generate the proper reset timing pulse would not make any appreciable contribution to the demonstration, and as a result the digits are as shown in photo E.

Figures 5.3 through 5.8 are the detailed wiring diagrams of the equipment tested. The packages described here are essentially equivalent to the "standard package" outlined in the following section. The major exception is the method used to terminate the assertion delay lines at the package input. Normally the characteristic impedance of the delay line is designed to match the impedance presented by the input clamp and the 3.3 K ohm pulldown resistance during the pulse.* Since high delay 300-ohm lines are not commercially available, it was necessary to terminate the line (RG 65/U) in its characteristic impedance (1.0 k Ω) as shown on the assertion inputs of packages 2 and 3 of the minor cycle counter. Even with the E_7 supply set at -6.0 volts, the noise generated by this method of line termination is sufficient to bring the grid to -1.0 volt. One volt of noise on the grid is tolerable here because of the insensitivity of the 436A in the (-2.0)-to-(-2.0)-volt region of grid bias. These large noise voltages can, of course, be avoided if a line is available which will match the normal input gate impedance.

The major portion of the noise voltage present on the "straight wire" interconnection is more a function of the ground noise rather than "pickup" (photos B and B'). The "ground noise" in photo B' has been reduced by grounding the last package of the timing generator directly to Package No. 1 of the Minor Cycle Counter On these packages each supply, including ground, is connected to each package through a "ribbon plug" with each supply bypassed to package ground. The particular method used to reduce ground noise will depend upon the computer design. This equipment was tested and operated at 5 Mc with approximately 2.5 volts of ground noise.

There are some points that should be emphasized with regard to the transformer connection in the circuit. A detailed procedure for transformer design is covered in Section 3.2.4. It is absolutely necessary that the primary winding be put on uniformly and that the respective layers be insulated from each other. It is also necessary that the primary winding connected to the plate be kept short because a long lead will contribute to the plate capacitance. The lead lengths of the secondary winding are not critical as secondary capacitance is reduced by the square of the turns ratio when referenced to the plate circuit.

*The desired delay line characteristics are discussed further in Section 5.3.

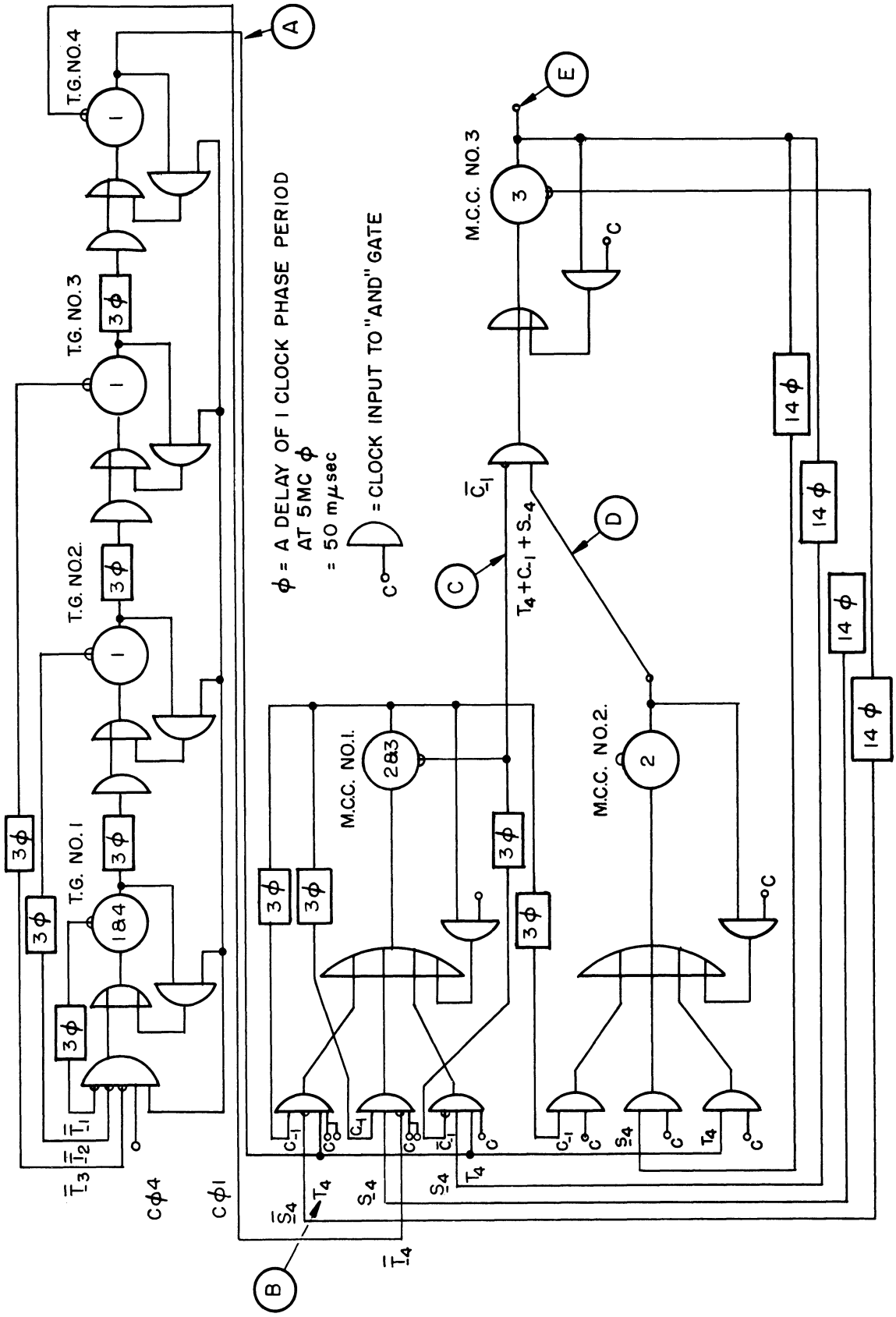
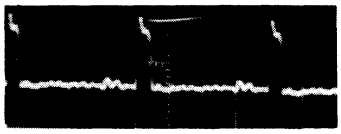


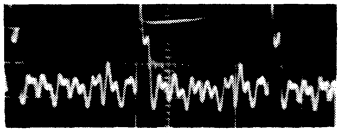
Fig. 5.1. T_4 timing generator and minor cycle counter.

Point A



5 v/div
200 mμsec/div

Point B

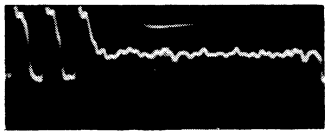


5 v/div
200 mμsec/div

Point B'

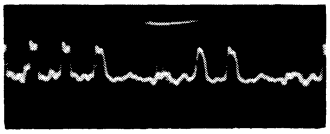
5 v/div
200 mμsec/div

Point C



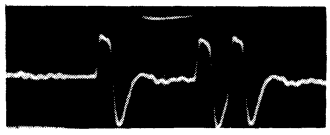
10 v/div
200 mμsec/div

Point D



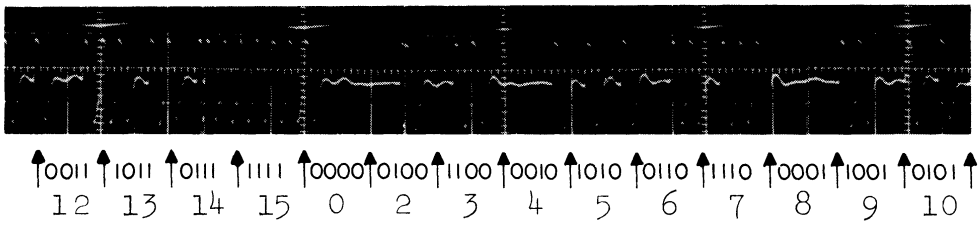
10 v/div
200 mμsec/div

Point E



10 v/div
200 mμsec/div

Point E - Sum Digits



SPECIFICATIONS (5 mc)

Supplies

E_1 = -52.5 v
E_2 = 46.0 v
E_3 = - 1.5 v
E_4 = - 3.0 v
E_5 = - 6.0 v
E_6 = + 5.0 v
E_S = 75 v
B+ = 120 v

Gate Current

I = 10 ma
I' = 15 ma
defined in section 2

Delay Line RG G5/U

Delay ≐ 40 mμsec/ft + 7%
Attenuation = .05 db/ft
Z_C ≐ 1.0 kΩ

Diodes

T. Generator: All Ray IN295 unless noted
Minor Cycle Counter: All HD2109

Tube

Western Electric 436A

Transformer

General Ceramic F289 cup core type Q
20:2:2 turns of AWG 34

Fig. 5.2. Wave forms and specifications.

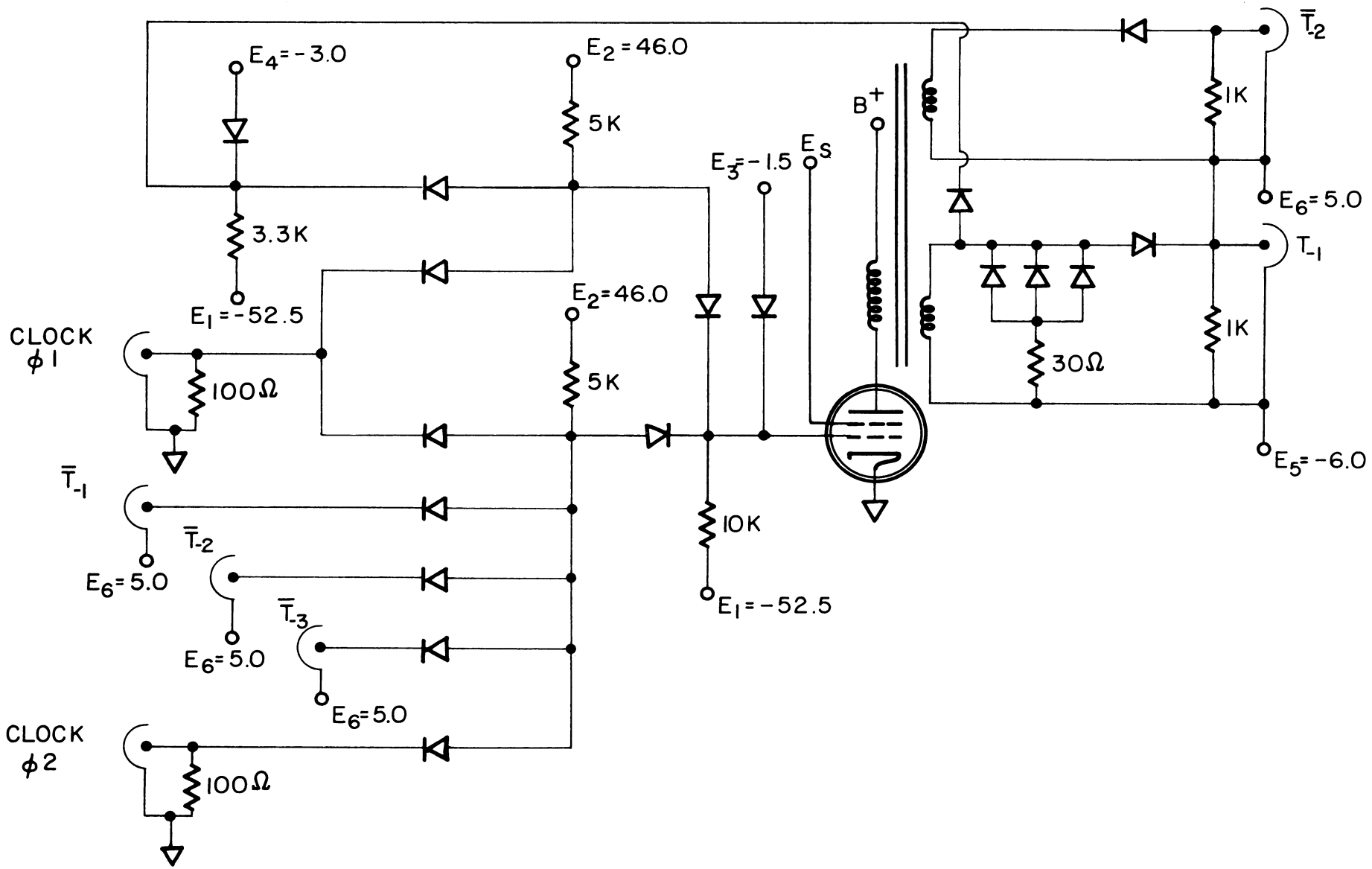


Fig. 5.3. Timing generator Package No. 1.

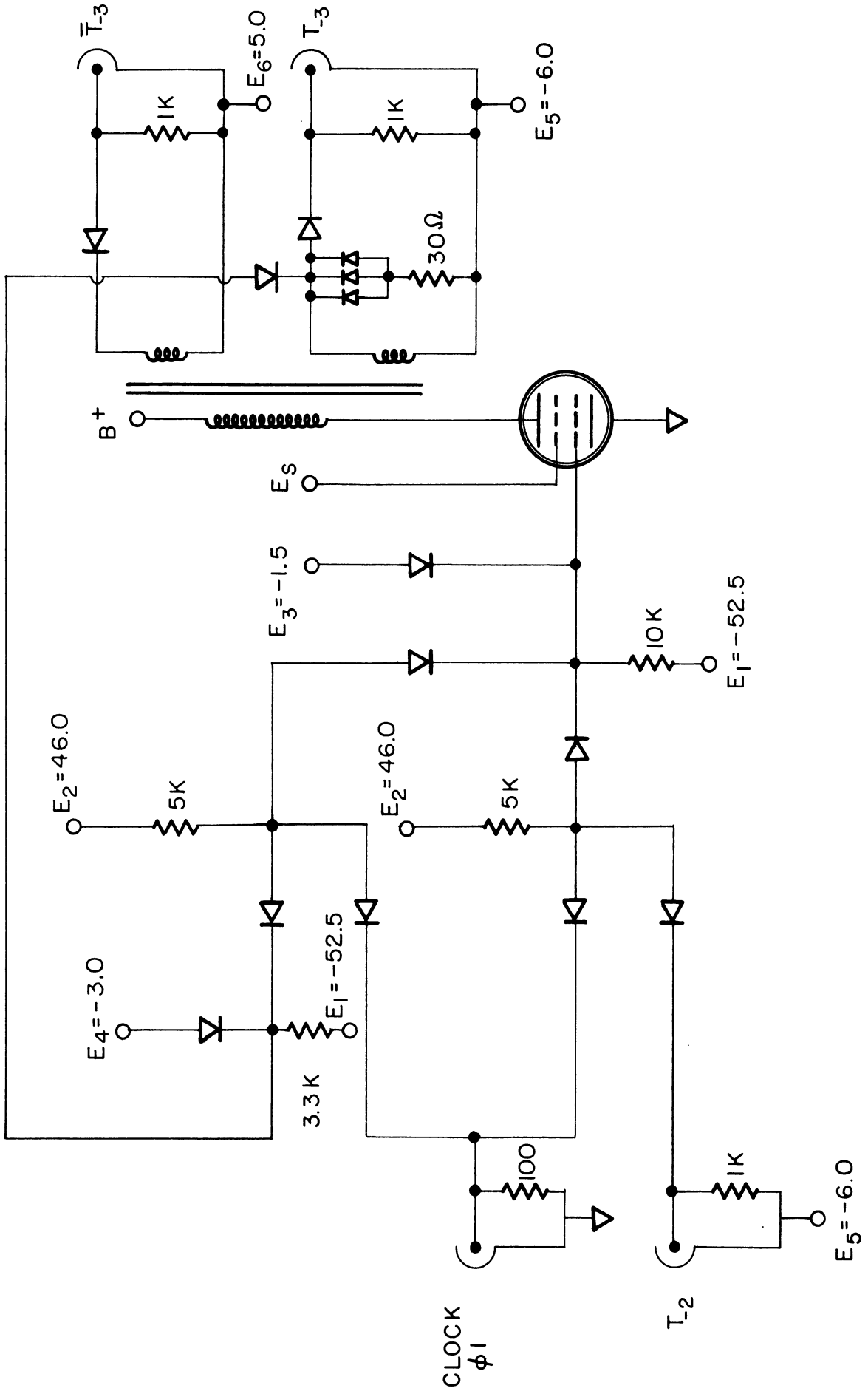


Fig. 5.4. Timing generator Package Nos. 2 and 3.

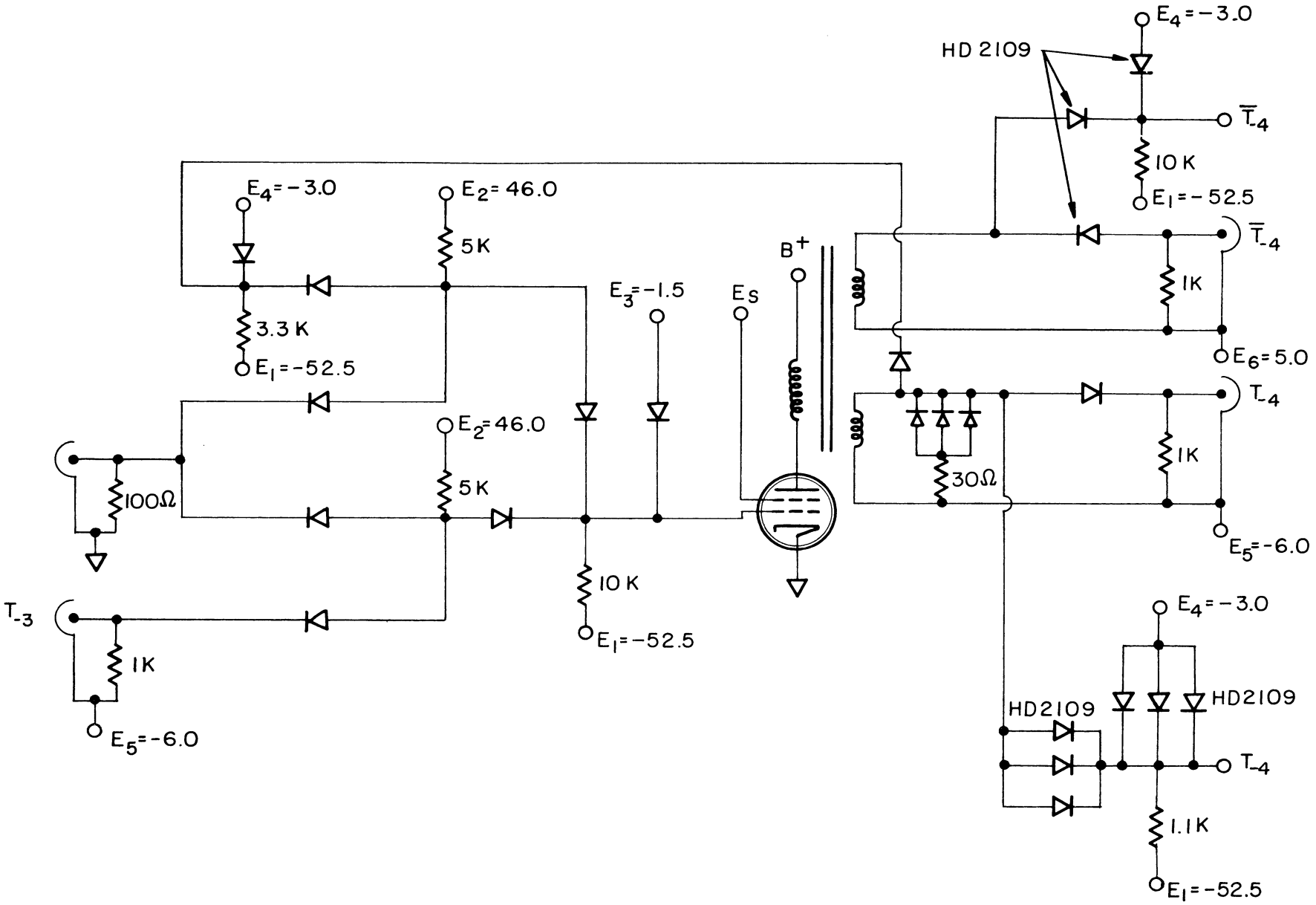


Fig. 5.5. Timing generator Package No. 4.

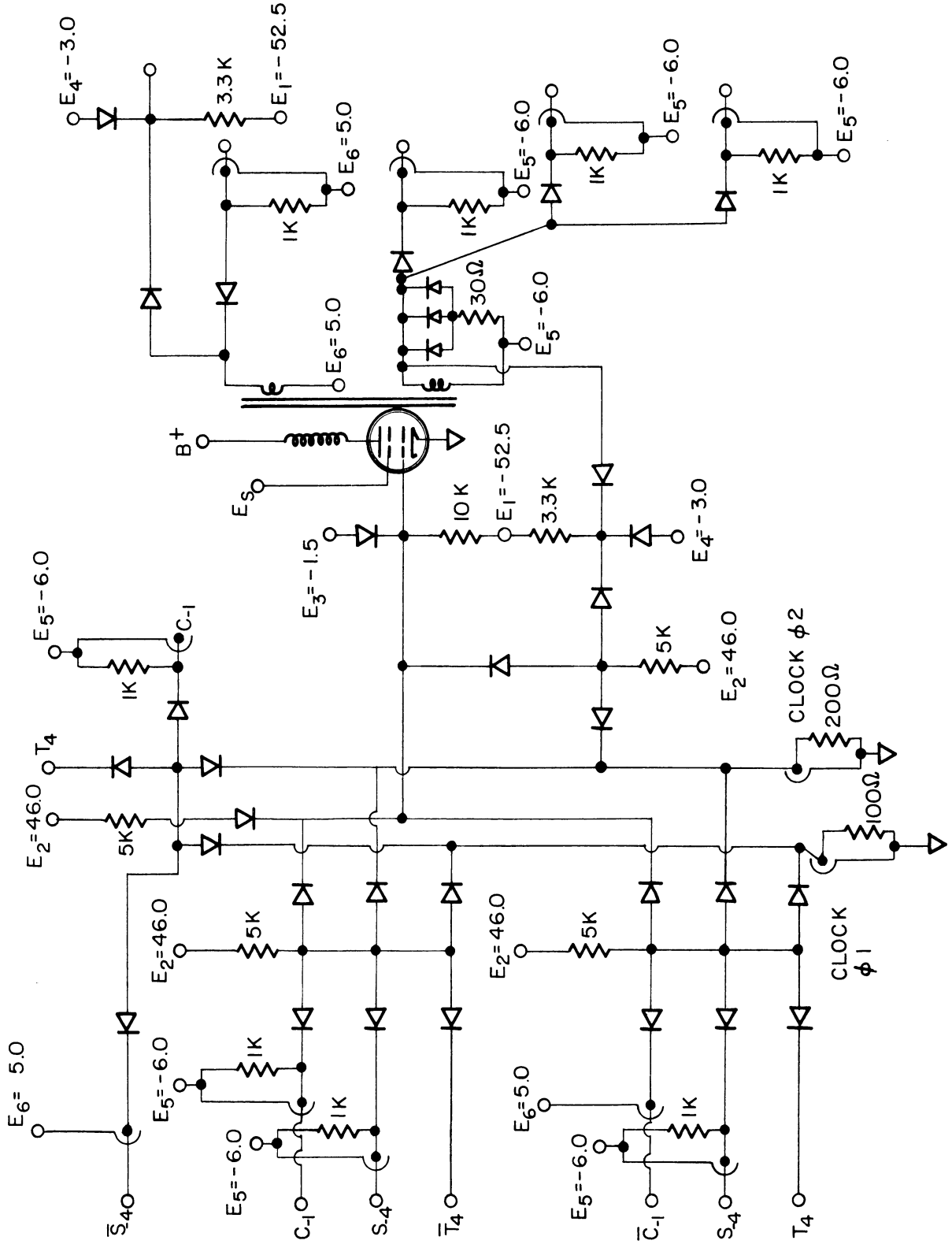


Fig. 5.6. Minor cycle counter Package No. 1.

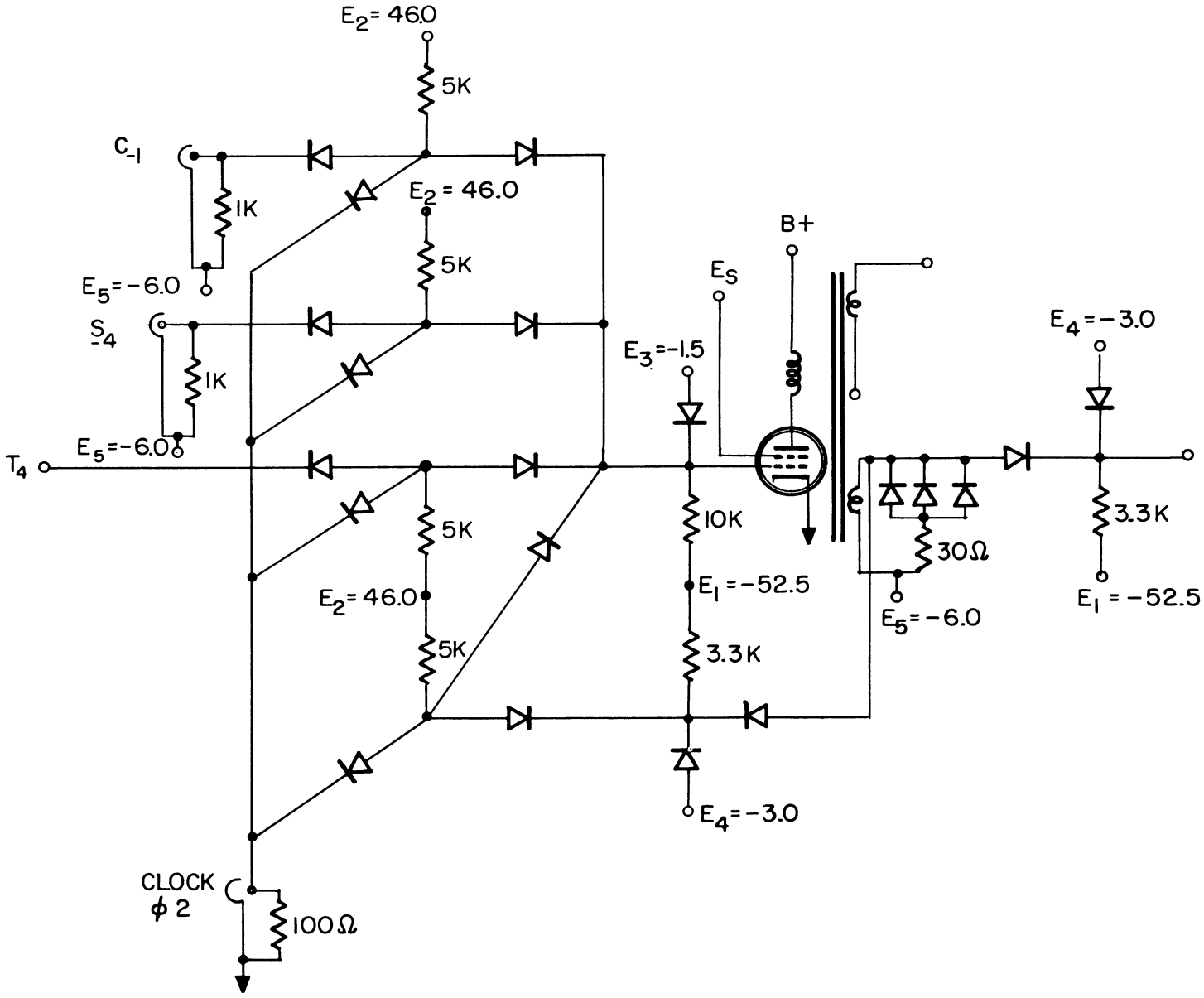


Fig. 5.7. Minor cycle counter Package No. 2.

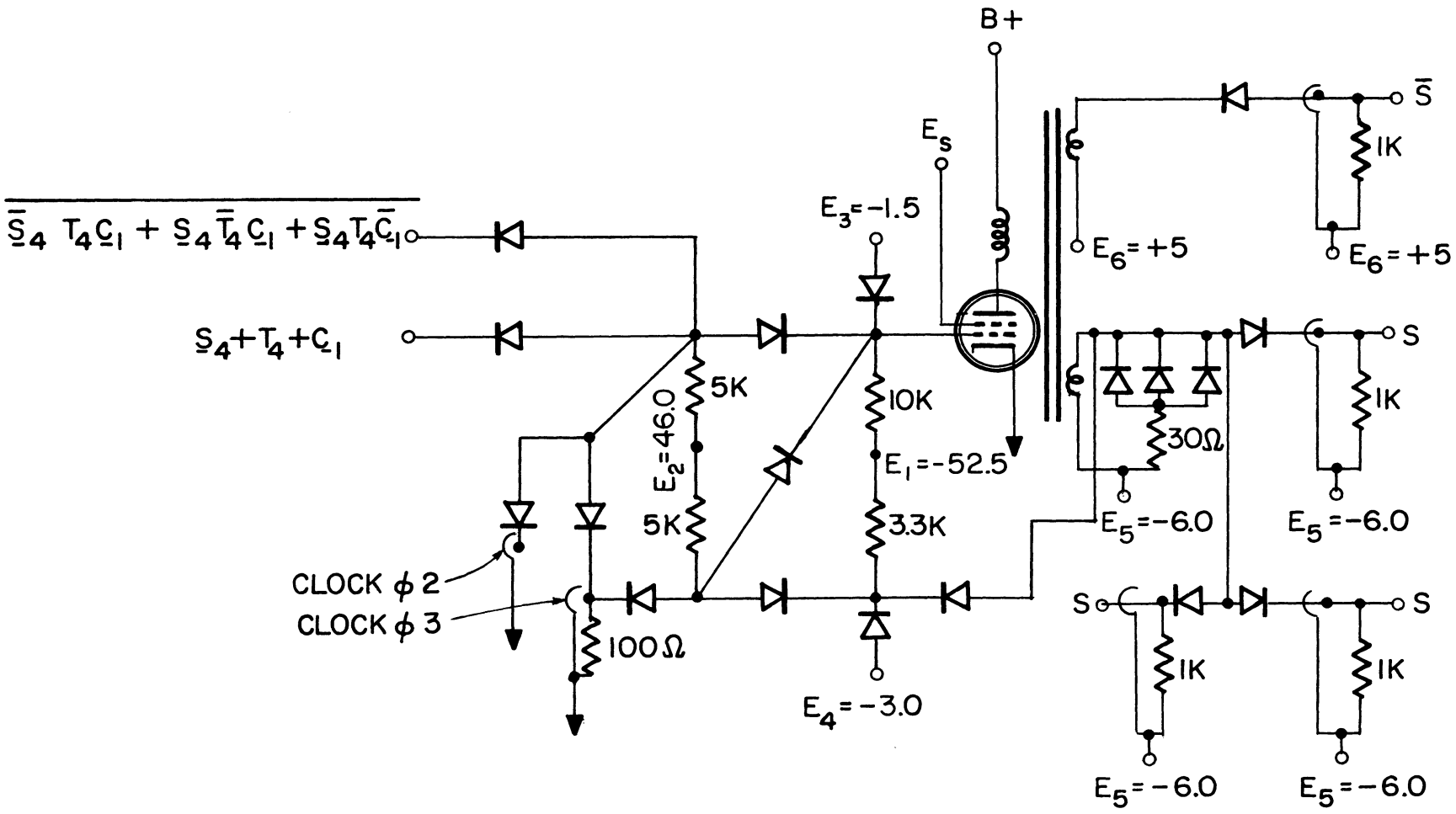


Fig. 5.8. Minor cycle counter Package No. 3.

5.3 Standard Package

Although the packages used in the logic described in the preceeding section were "tailor-made" as to the number of "and" gates and the number of legs on each of these gates to conserve components, it is usually desirable to have a very limited number of kinds of packages in a computer installation. It is suggested that a standard package of the form of Fig. 5.9 be used and that delay line packages be constructed as in Fig. 5.10 when lines must be driven. The input "and" logic of Fig. 5.9 should have the number of legs limited to five or less; as many five-legged "and" gates as desired may then be buffered together in the "or" stage of logic. The pull-down resistor R_1 of Fig. 5.9 should be conveniently available for change. In a package which is continuously pulsing, R_1 should not be more than 300 ohms (corresponding to 175 ma output current) in order that the screen power dissipation rating is not exceeded.[11] If many delay lines are driven, or if several outputs are driven from the negation winding or if a package is known to operate less than all the time (as in a timing-pulse generator, for example,)then R_1 may be increased above 300 ohms.

The nominal characteristic impedance of the delay lines to be used with these packages is a function of gate currents and signal amplitudes and may be calculated as follows:[12]

The current I_1 flowing in R_1 of Fig. 5.10(a) during a pulse which reaches a peak amplitude of $\neq$ 5 volts is given by

$$I_1 = (5 \neq 52.5)/3.3k = 17.25 \text{ ma.}$$

Therefore, the impedance of the gate during the flat top of the pulse is

$$Z_{gate} = 5/17.25 \text{ ma} \doteq 290 \text{ ohms.}$$

Therefore, if the gate is to match a line, the line should have about 300 ohms nominal characteristic impedance. The resistor R_2 of Fig. 5.10(a) is intended to absorb enough of the reflections which occur when the pulse is rising and falling to render them harmless.

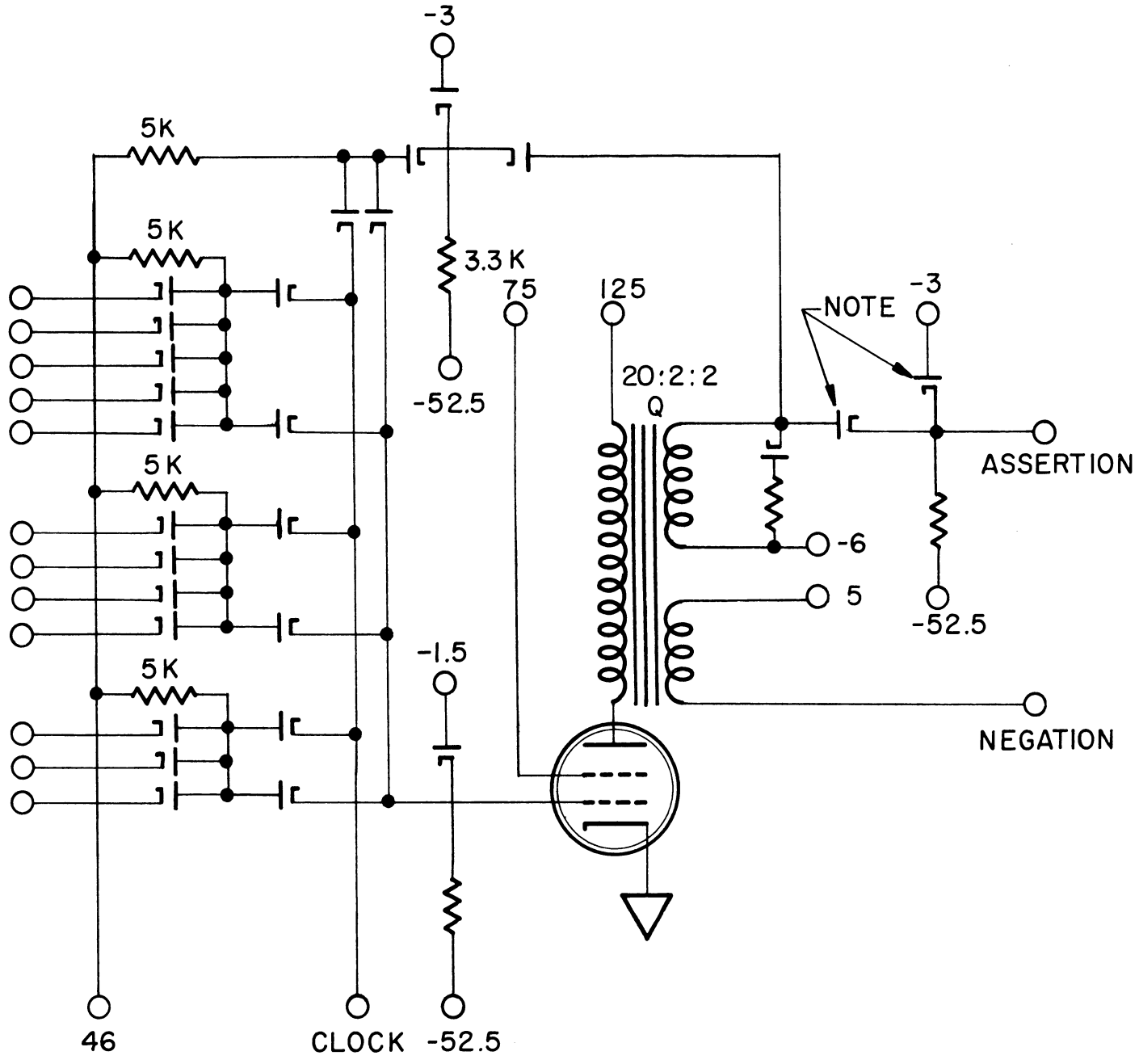
Given that 300-ohm line is being used, and that the negation output falls to -5 volts under pulsed conditions, the current flowing in the 5 k pull-up resistor is

$$I_2 = (46 - 5)/5 \text{ k} = 10.2 \text{ ma,}$$

but 17.25 ma are required with a 5-volt signal if the line is to be matched. Therefore, the resistor R_1 connected to $\neq$ 5 volts in Fig. 5.10(b) is added to absorb the additional 7 ma of current. This resistor then evidently has the value

$$R_1 = (5 \not / 5)/7 \text{ ma} = 1.4 \text{ k} \quad ,$$

and a standard 1.5 k resistor would be used. Here again, R_2 absorbs reflections which occur during the pulse rise and fall.



NOTE: Number of diodes used here depends on number of gates to be driven.

Fig. 5.9. Standard package.

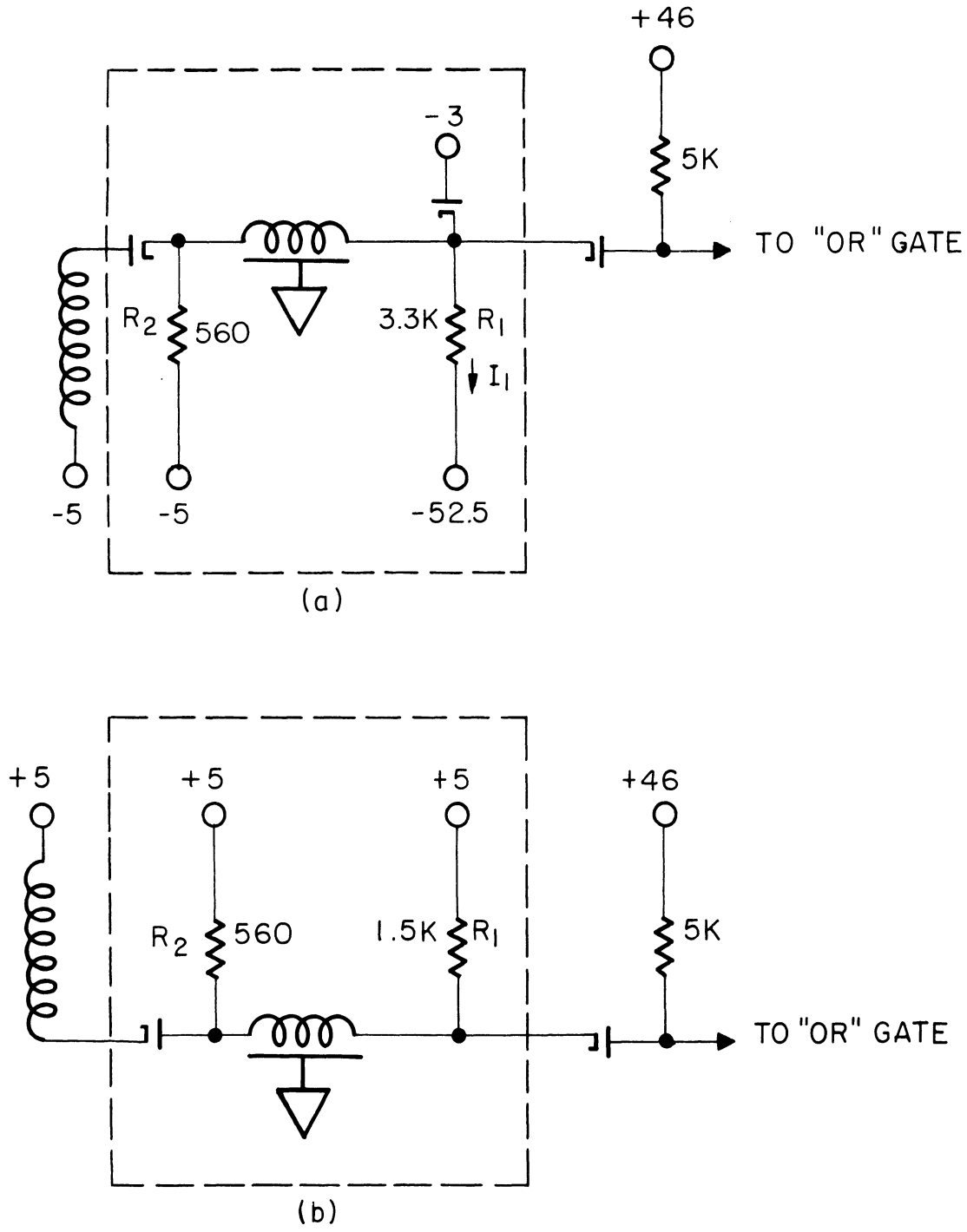


Fig. 5.10. Delay terminations. (a) For assertion outputs and (b) for negation outputs.

APPENDIX A

THEORETICAL COMPARISON OF VACUUM TUBES

The number of gate drives, N, for serial dynamic circuitry may be expressed as

$$N = \frac{M^2 T^2 E}{4}$$

where

$$M = \frac{g_m}{\sqrt{C_p C_g}}, \text{ rad/sec},$$

T = pulse rise time, sec, and

E = gate efficiency.

The quantity M may be defined as a vacuum-tube figure of merit for this type of circuitry; to obtain the largest number of gate drives at a given repetition rate, M should be as large as possible. Consequently, a survey of available tubes has been conducted with a view toward a maximum M. The results of this survey are presented in the following table, from which it is clear that the best of the conventional tubes is the 436A tetrode. However, some of the triodes available have extremely large transconductances and would have a better figure of merit than the 436A if it were not for the Miller effect capacity. The Miller capacitance decreases the figure of merit.

COMPARISON OF FIGURE OF MERIT OF VACUUM TUBES

	6AN5	6AK5	6AH6	404A	435A	418A	436A	5857	417A	437A	416A
C_{gp} ($\mu\mu$f)	0.075	0.01	0.03	0.05	0.035	0.05	0.07	0.004	1.8	3.5	1.25
C_{in} ($\mu\mu$f)	9.0	3.9	10.0	7.0	7.9	16	15	9.3	9.0	11.5	6.5
C_{out} ($\mu\mu$f)	4.8	2.85	2.0	2.5	2.9	2.7	3.5	2.2	.48	.9	0.7
g_m (ma/volt)	8	5	9	12.5	15.5	25	30	20	24	45	50
$M = \frac{g_m}{\sqrt{C_{in} C_{out}}}$ (rad/μsec)	1210	1490	2010	2990	3240	3790	4130	4410 (1)	(2)	(2)	(2)

(1) Secondary emission type.
(2) See section on the cascode circuit.

APPENDIX B

TRIODE INPUT CAPACITANCE

The grid is driven by a gating structure which may be approximated by a constant-current step source. The circuit to be considered is then as shown in Fig. B-1, and the small-signal equivalent of this circuit is shown in Fig. B-2. Applying Norton's theorem to the voltage generator and letting $R = (r_p\ R_L)/(r_p + R_L)$ gives the final circuit of Fig. B-3.

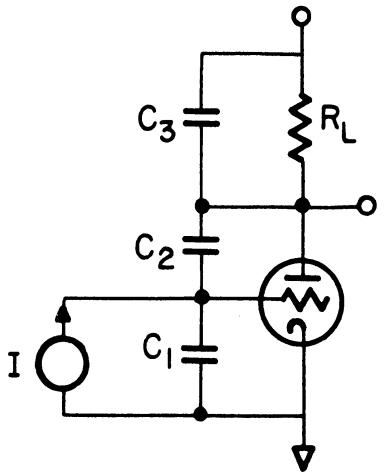


Fig. B-1

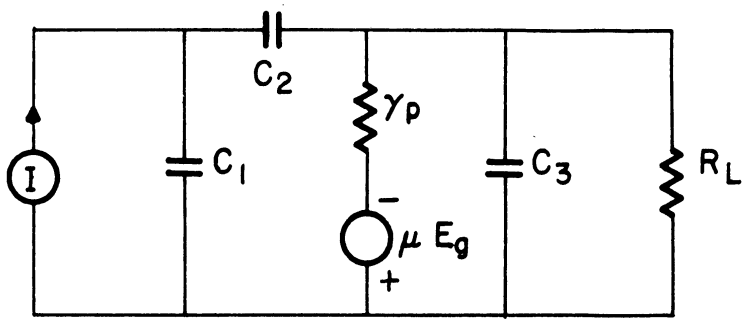


Fig. B-2

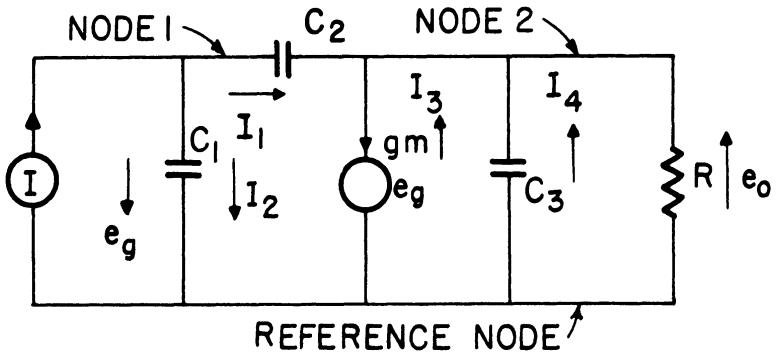


Fig. B-3

From this last circuit, one may write by inspection

$$I_1 = (e_o + e_g)\, pC_2$$

$$I_2 = e_g\, pC_1$$

$$I_3 = e_o pC_3$$

$$I_4 = \frac{e_o}{R} \quad .$$

For Node 1 $\quad I = I_1 + I_2 = (e_o + e_g)\, pC_2 + e_g\, pC_1$.

For Node 2 $\quad g_m e_g = I_1 + I_3 + I_4 = (e_o + e_g)\, pC_2 + e_o pC_3 + \frac{e_o}{R}$.

Rewriting: $\quad p\,(C_1 + C_2)\, e_g + pC_2 e_o = I$

$$(g_m - pC_2)\, e_g - (pC_2 + pC_3 + \frac{1}{R})\, e_o = 0$$

or:
$$\begin{bmatrix} p(C_1 + C_2) & pC_2 \\ g_m - pC_2 & -p(C_1 + C_3) - \frac{1}{R} \end{bmatrix} \times \begin{bmatrix} e_g \\ e_o \end{bmatrix} = \begin{bmatrix} I \\ o \end{bmatrix}$$

We wish to know the input capacitance, and since

$$e_g = \frac{1}{C_{in}} \int I\, dt \quad \text{or} \quad \frac{de_g}{dt} = \frac{I(t)}{C_{in}} \ ,$$

We then wish to find $(de_g/dt)(1/I(t))$. Hence, solve for pe_g for a step-function input I/p:

$$\frac{pe_g}{I} = \frac{p\,(C_2 + C_3) + \frac{1}{R}}{p\left\{(C_1 + C_2)\left[p(C_2 + C_3) + \frac{1}{R}\right] + C_2(g_m - pC_2)\right\}}$$

$$= \frac{\frac{1 + pR\,(C_2 + C_3)}{R(C_1C_2 + C_1C_3 + C_2C_3)}}{p\left[p + \frac{C_1 + (1 + g_mR)\,C_2}{R(C_1C_2 + C_2C_3 + C_1C_3)}\right]}$$

Let $A = \frac{C_2 + C_3}{C_1C_2 + C_1C_3 + C_2C_3}$,

$B = \frac{1}{R(C_1C_2 + C_1C_3 + C_2C_3)}$, and $\alpha = \frac{C_1 + (1 + g_mR)\,C_2}{R(C_1C_2 + C_1C_3 + C_2C_3)}$.

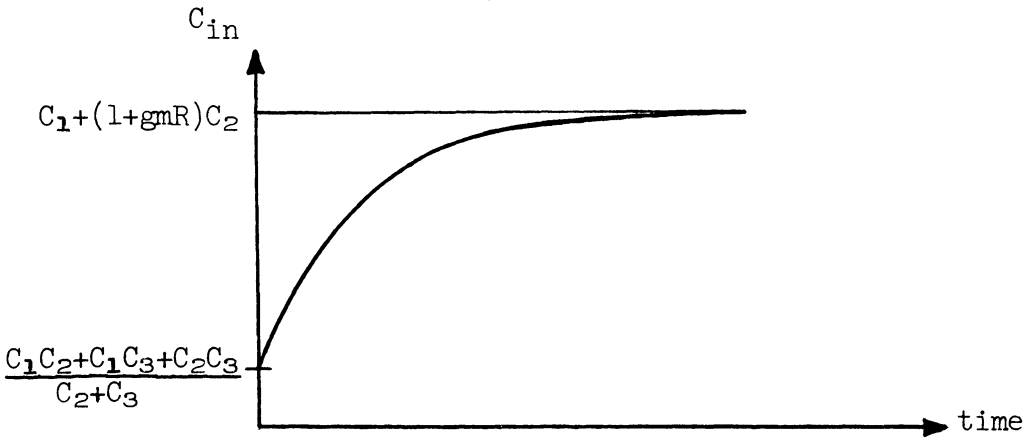
Then $\frac{pe_g}{I} = \frac{A}{p+\alpha} + \frac{B}{p(p+\alpha)}$,

and $\frac{1}{I}\frac{de_g}{dt} = Ae^{-\alpha t} + \frac{B}{\alpha}(1 - e^{-\alpha t})$

$$= \frac{(C_2 + C_3)\,e^{-\alpha t}}{C_1C_2 + C_1C_3 + C_2C_3} + \frac{(1 - e^{-\alpha t})}{C_1 + (1 + g_mR)\,C_2}$$

$$= \frac{1}{C_1 + (1 + g_mR)\,C_2} + \left[\frac{C_2 + C_3}{C_1C_2 + C_1C_3 + C_2C_3} - \frac{1}{C_1 + (1+g_mR)\,C_2}\right]e^{-\alpha t}$$

$$= \frac{1}{C_{in}} .$$



The input capacitance has reached 95% of its final value when $t = 3/\alpha$ or when

$$t = \frac{3\,R(C_1C_2 + C_1C_3 + C_2C_3)}{C_1 + (1 + g_mR)\,C_2} .$$

For the 437A triode with

$$R = 1k,$$
$$C_1 = 11 \text{ pF},$$
$$C_2 = 4 \text{ pF, and}$$
$$C_3 = 1 \text{ pF},$$

t_c is calculated to be 0.89×10^{-9} sec.

That is, the input capacitance has reached 95% of $C_1 + (1 + gmR) C_2$ in a time of the order of 1 mμsec for the 437A. This means that for 10-mcps (or less) operation, the input capacitance may be considered to be just

$$Cin = C_1 + (1 + gm\ R)\ C_2.$$

APPENDIX C

ANALYSIS OF STEADY-STATE MAGNETIZING CURRENT IN A TUNED, CRITICALLY DAMPED TRANSFORMER

If the magnetizing current increases by an amount I_m during each pulse and is attenuated by a factor K in each interval between, then the magnetizing current at the start of an Nth pulse approaches (as N approaches infinity)

$$\Big[(I_mK + I_m)K + I_m\Big]K + I_m + \cdots = \frac{I_mK}{1-K} \quad .$$

So, steady-state magnetizing current, $I_{m_{ss}}$, after a long pulse train, approaches

$$I_{m_{ss}} = \frac{I_mK}{1-K} \quad .$$

For a critically damped, tuned transformer, as in the text, where $K \simeq 0.08$,

$$I_{m_{ss}} = I_m \frac{0.08}{1-0.08}$$

$$I_{m_{ss}} = 0.083\ I_m \quad .$$

So, the steady-state magnetizing current will be only about 8.3% of the magnetizing current at the end of one pulse. This means that the output pulse will be essentially independent of the past history of the circuit.

APPENDIX D

ANALYSIS OF RESONANT-TRANSFORMER PULSE RESPONSE

It is assumed that the voltage across the transformer primary during the pulse period has a shape as shown in Fig. D-1 where $\tau_1 = 1/10f_p$, $\tau_2 = 3/10f_p$, and f_p is the pulse repetition frequency. The output voltage during transformer recovery is not shown. In general, magnetizing current in the primary inductance is given by

$$I_m = \frac{1}{L_p} \int_0^T E_o \, dt \quad .$$

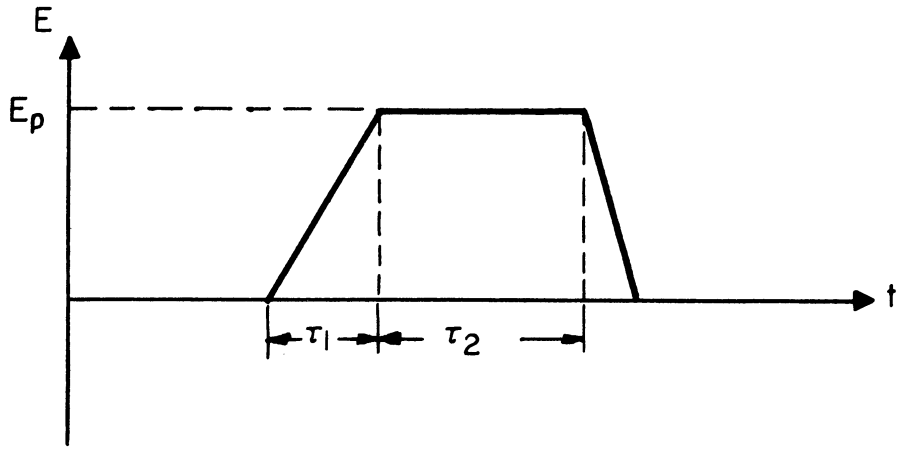


Fig. D-1 Transformer primary voltage.

For the primary voltage shape shown in Fig. D-1 the magnetizing current at the end of the flat-top portion of the pulse is

$$I_m = \frac{1}{L_p} \int_0^{\tau_1} \frac{E_p}{\tau_1} t \, dt + \frac{1}{L_p} \int_0^{\tau_2} E_p \, dt$$

$$I_m = \frac{E_p \tau_1}{2 L_p} + \frac{E_p \tau_2}{L_p}$$

$$I_m = \frac{7 E_p}{20 f_p L_p} \quad .$$

The maximum primary load current, I_{L_p}, will be

$$I_{L_p} = \Delta I - I_m - I_{m_{ss}} ,$$

where

ΔI = plate pulse current and

$I_{m_{ss}}$ = 2/23 I_m as shown in Appendix A for a critically damped transformer.

Further, we have

$$E_p = N E_L$$

and

$$I_{L_p} = \frac{1}{N} I_L ,$$

where E_L = secondary load voltage,
I_L = secondary load current, and
N = primary-to-secondary transformer turns ratio,

so that,

$$I_L = N\Delta I - \frac{7N^2E_p}{20\ f_pL_p} - \frac{7N^2E_p}{230\ f_pL_p} .$$

Since the transformer is tuned to the pulse repetition frequency, we have

$$\omega_p = \frac{1}{\sqrt{L_P\ (C_T + C_s/N^2)}} ,$$

or

$$L = \frac{N^2}{4\pi^2 f_p^2\ (C_s + N^2C_T)} ,$$

so

$$I_L = N\Delta I - \frac{35\ \pi^2}{23} f_pE_L\ (C_s + N^2C_T) . \qquad \text{(D-1)}$$

To find the optimum turns ratio for maximum load current, we take the derivative of I_L with respect to N and set the derivative equal to zero to get

$$N_{opt} = \frac{23\ \Delta I}{70\ \pi^2C_T\ f_pE_L} . \qquad \text{(D-2)}$$

Substituting this expression for N into Equation D-1 gives

$$I_{L_{max}} = \frac{23}{140\ \pi^2}\ \frac{\Delta I^2}{C_T f_p E_L} - \frac{35\ \pi^2}{23}\ C_s f_p E_L\ . \qquad \text{(D-3)}$$

APPENDIX E

ANALYSIS OF LIMITATIONS ON RESONANT-TRANSFORMER LOAD CURRENT DUE TO RISE-TIME REQUIREMENTS

The pulse rise time of the tube-transformer is analyzed, using the equivalent circuit shown in Fig. 3.1b. If a current ΔI flows out of the current generator, the primary pulse voltage during the pulse rise time is given by

$$E_{o(s)} = \frac{\Delta I}{C\left(S^2 + \frac{1}{RC}S + \frac{1}{LC}\right)} ,$$

since it has been shown that $I_{m_{ss}}$ will be negligible. The roots of the quadratic in the denominator are

$$r_1, r_2 = -\frac{1}{2RC} \pm \frac{1}{2}\sqrt{\frac{1}{R^2C^2} - \frac{4}{LC}} ,$$

$$r_1, r_2 = -\frac{1}{2RC}\left[1 \pm \sqrt{1 - \frac{4R^2C}{L}}\right] ,$$

$$\text{but } L = \frac{1}{4\pi^2 f_p^2 C} ,$$

$$\text{so } \quad r_1, r_2 = -\frac{1}{2RC}\left[1 \pm \sqrt{1 - (2RC\omega_p)^2}\right] .$$

Let

$$r_1 = -\frac{1}{2RC}\left[1 + \sqrt{1 - (2RC\omega_p)^2}\right]$$

$$r_2 = -\frac{1}{2RC}\left[1 - \sqrt{1 - (2RC\omega_p)^2}\right] .$$

Then,

$$E_{o(t)} = \frac{\Delta I}{C(r_1 - r_2)}\left(e^{r_1 t} - e^{r_2 t}\right) ,$$

and substituting gives

$$E_{o(t)} = \frac{\Delta IR}{\sqrt{1-(2RC\omega_p)^2}}\, e^{-\frac{t}{2RC}}\left[e^{\frac{\sqrt{1-(2RC\omega_p)^2}}{2RC}} - e^{\frac{\sqrt{1-(2RC\omega_p)^2}}{2RC}}\right] ,$$

and, since $2RC\omega_p > 1$,

$$E_{o(t)} = \frac{2\Delta IR}{\sqrt{(2RC\omega_p)^2-1}}\, e^{-\frac{t}{2RC}} \sin \sqrt{\omega_p^2 - (1/4R^2C^2)}\cdot t \quad .$$

However, for typical values,

$$\omega_p^2 \gg \frac{1}{4\ R^2C^2} ,$$

so

$$E_{o(t)} \simeq \frac{\Delta I}{C\omega_p}\, e^{-\frac{t}{2RC}} \sin \omega_p t \quad . \tag{E-1}$$

Then, since $E_{o(t)}$ is required to reach NE_L in $1/10f_p$ seconds,

$$R = N^2 \frac{E_L}{I_L} \quad \text{and} \quad C = \left(C_T + \frac{C_s}{N^2}\right) ,$$

substitution into (E-1) gives the relationship

$$NE_L \simeq \frac{\Delta I}{2\pi \left(C_T + \frac{C_s}{N^2}\right) f_p}\, e^{-\frac{I_L}{20f_pE_L(C_s+N^2C_T)}} \sin \frac{\pi}{10} \quad .$$

Rearranging gives

$$\frac{2\pi E_L f_p (C_s+N^2C_T)}{\Delta IN \sin \pi/10} = e^{-\frac{I_L}{20f_pE_L(C_s+N^2C_T)}} . \tag{E-2}$$

Plots of the left-hand and right-hand sides of this equation show that maximum load current can be drawn when

$$N^2 = C_s/C_T \quad .$$

Substituting this value for N into (E-2) and rearranging gives

$$I_{L_{max}} = 40\ C_s f_p E_L\ \ell n\ \frac{\Delta I \sin \pi/10}{2\ E_L \omega_p C_T} \quad . \tag{E-3}$$

APPENDIX F

ANALYSIS OF LIMITATIONS ON HIGH-INDUCTANCE TRANSFORMER LOAD CURRENT DUE TO RISE-TIME REQUIREMENTS

Because of the high primary inductance in this case, the tube-transformer can be represented by the equivalent circuit shown in Fig. F-1. $I_{m_{ss}}$ is given by

$$I_{m_{ss}} = \frac{I_m K}{1 - K} ,$$

as derived in Appendix A. For a transformer with large primary inductance, being driven by a train of pulses with equal on-off intervals, $\tau = 1/2f_p$,

$$I_m = \frac{E\tau}{L} = \frac{NE_L}{2f_p L}$$

and

$$K = e^{-\frac{N^2 R_L}{L}\tau} = e^{-\frac{N^2 R_L}{2f_p L}} .$$

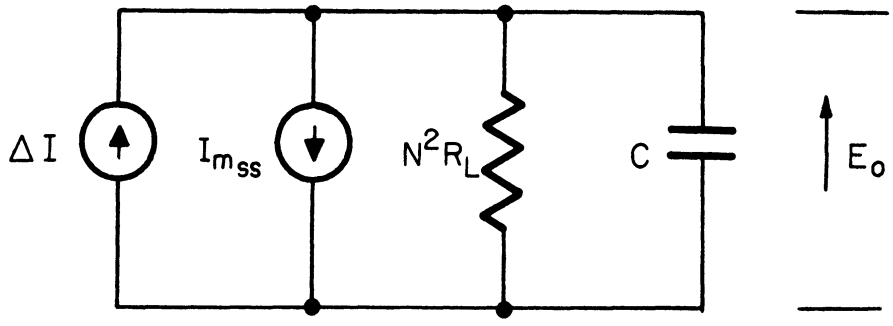


Fig. F-1. Equivalent circuit for nonresonant transformer during pulse rise.

Since

$$\frac{N^2 R_L}{2f_p L} \ll 1 ,$$

$$K \simeq 1 - \frac{N^2 E_L}{2f_L}$$

and

$$I_{m_{ss}} \simeq \frac{E_L}{NR_L} - \frac{NE_L}{2f_L} .$$

However, for large L, the second term is small compared to the first, so

$$I_{m_{ss}} = \frac{E_L}{NR_L} .$$

For the circuit of Fig. F-1

$$E_o = N^2R_L (\Delta I - I_{m_{ss}}) \left(1 - e^{-\frac{t}{N^2R_LC}}\right) ,$$

and since, as is discussed in the body of the report, E_o must rise through $2NE_L$ in a time $\tau = 1/10f_p$, we have the relation

$$2NE_L = N^2R_L (\Delta I - I_{m_{ss}}) \left(1 - e^{-\frac{1}{10N^2CR_Lf_p}}\right) .$$

Then, substituting for $I_{m_{ss}}$ and rearranging terms gives

$$e^{-\frac{1}{10N^2CR_Lf_p}} = \frac{\frac{N\Delta I}{E_L} R_L - 3}{\frac{N\Delta I}{E_L} R_L - 1} ,$$

but since $C = C_T + C_s/N^2$, and $R_L = E_L/I_L$, we have

$$e^{-\frac{I_L}{10E_Lf_p(C_s+N^2C_T)}} = \frac{\frac{N\Delta I}{I_L} - 3}{\frac{N\Delta I}{I_L} - 1} .$$

APPENDIX G

DERIVATION OF THE REFLECTION EQUATION

Let

E_{in} = input voltage wave,
α_k = total attenuation of the k'th cable and the k'th delay network,
t_k = total time delay of the k'th cable and the k'th delay network,
R_D = impedance seen at the discontinuity, and
R_k = impedance of the network at the discontinuity.

If $R_k = mR_o$,
then

$$R_D = R_k \parallel R_o = \frac{(mR_o)R_o}{mR_o + R_o} = \frac{m}{m+1} R_o \quad ,$$

and the reflection coefficient at the tap point,

$$\rho = \frac{\frac{R_D}{R_o} - 1}{\frac{R_D}{R_o} + 1} = \frac{\frac{m}{m+1} - 1}{\frac{m}{m+1} + 1} = - \frac{1}{2m + 1}$$

Evidently, the input to the first discontinuity is given by

$$E_1' = E_{in} e^{-(\alpha_1 + st_1)} \quad ;$$

hence

$\frac{2m}{2m+1} E_1'$ will be propagated toward the receiving end, and $- \frac{1}{2m+1} E_1'$ will be reflected toward the sending end. The voltage at the n'th discontinuity due to the forward wave alone is given by

$$E_n' = \left(\frac{2m}{2m+1} \right)^{n-1} e^{- \sum_{i=1}^{n} (\alpha_i + st_i)} =$$

$$= \left(\frac{2m}{2m+1}\right)^{n-1} e^{-\sum_{i-1}^{n} \alpha_i} u\left(t - \sum_{i=1}^{n} t_i\right) \quad .$$

However, at every discontinuity the $\frac{1}{2m+1}$ fraction of the input gives rise to multiple reflection. Hence, at every discontinuity, there appears a term representing the summation of all multiple reflection terms. Since every reflected wave must cover any distance twice before returning to starting point, a multiplicative factor must be of the form $\left(\frac{1}{2m+1}\right)^{2v}$. The forward input to the discontinuity, therefore, is given by the summation of all possible terms, or

$$E'_k = \sum_{v=0}^{\infty} \left\{ E_{in} \left(\frac{1}{2m+1}\right)^{k-1} \left(\frac{1}{2m+1}\right)^{2v} e^{-\sum_{i=1}^{k} [1+2v]\, \alpha_i} \right.$$

$$\left. \cdot u \left\{ t - \sum_{i=1}^{k} [1 + 2v]\, t_i \right\} \right\}$$

under the assumption of sending end termination, the total input to the discontinuity, however, will represent the forward input propagated from the sending end, and the reflected input approaching the discontinuity from the receiving end.

If the reflected input $= E'_k \Phi$,

then

E_k = total input to the discontinuity

$= E'_k - E'_k \Phi = E'_k (1 - \Phi)$.

Evidently the reflected input is activated by E'_k. The $\frac{2m}{2m+1}$ fraction is of even power, since the wave must travel the distance twice before it can get back to the k'th discontinuity. The $\frac{1}{2m+1}$ fraction, however, is of odd power, since there must be $2\mu+1$ reflections if the ware is to reach the k'th discontinuity.

$$\therefore \quad \Phi' = \sum_{\ell=k+1}^{n-1} \left\{ \sum_{r=0}^{\infty} \left(\frac{2m}{2m+1}\right)^{2(\ell-k)} \left(\frac{1}{2m+1}\right)^{1+2r} \right\}$$

if termination at the n'th tap is assumed.

The total reflection coefficient Φ would still have terms accounting for time delay and attenuation. Then finally

$$\Phi = \sum_{\ell=k+1}^{n-1} \left\{ \sum_{r=0}^{\infty} \left(\frac{2m}{2m+1} \right)^{2(\ell-k)} \left(\frac{1}{2m+1} \right)^{1+2r} \cdot \right.$$

$$\left. \cdot \; e^{-2 \sum_{j=k+1}^{\ell} [1+r]\alpha_j} \cdot u \left[t - 2 \sum_{j=k+1}^{\ell} (1+r)\, t_j \right] \right\} ;$$

henceforth

$$E_k = \left\{ \sum_{v=0}^{\infty} E_{in} \left(\frac{2m}{2m+1} \right)^{k-1} \left(\frac{1}{2m+1} \right)^{2v} e^{-\sum_{i=1}^{k} [1+2v]\, \alpha_i} \cdot \right.$$

$$\left. \cdot \; u \left[t - \sum_{i=1}^{k} (1 + 2v)\, t_i \right] \right\} (1 - \Phi)$$

APPENDIX H

GRAPHICAL CIRCUIT ANALYSIS EMPLOYING THE IBM 650 DIGITAL COMPUTER

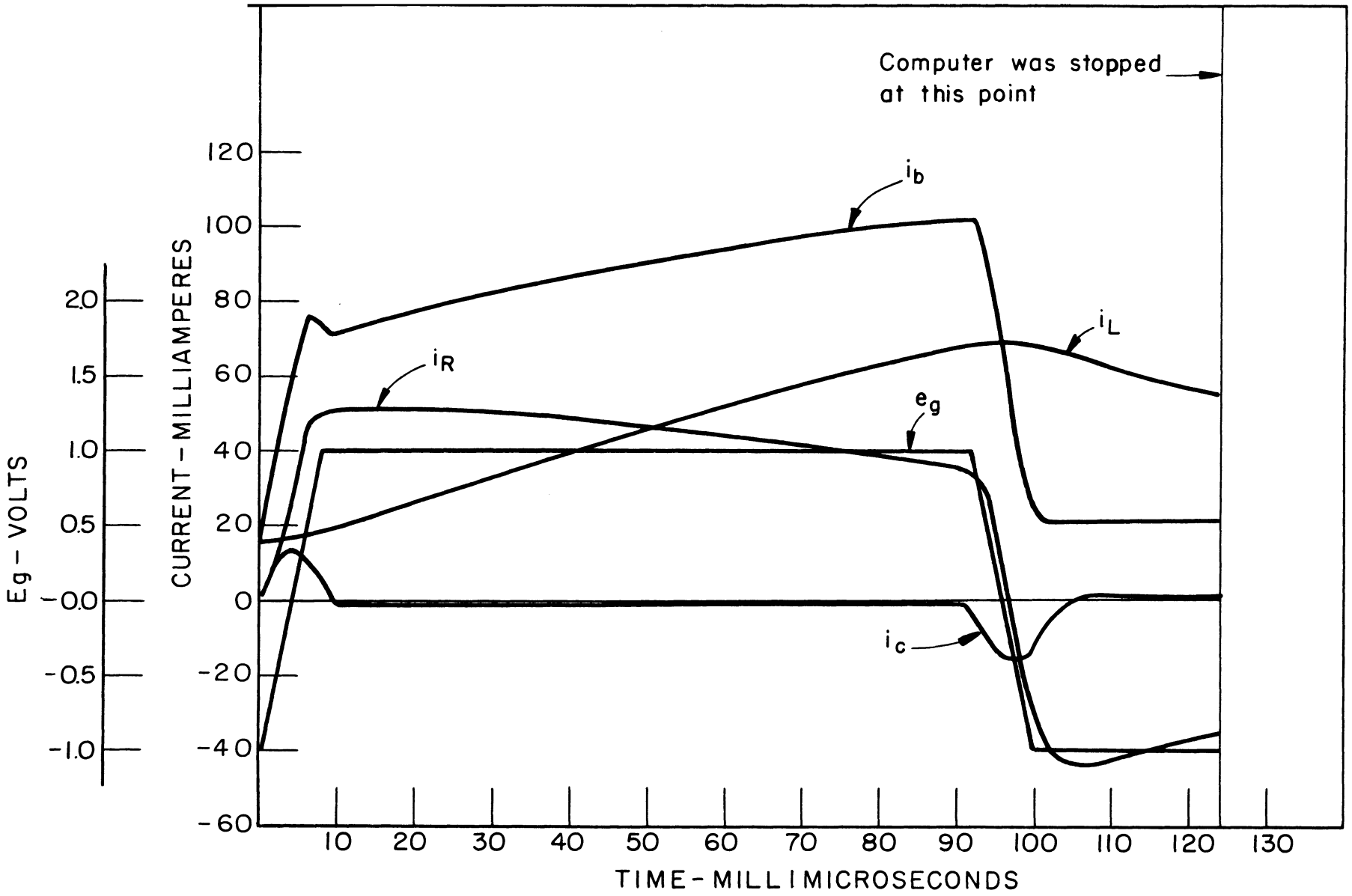
A program to perform the graphical analysis discussed in Section 1 has been prepared for the IBM 650 computer. The program has been run and the results obtained are shown in Fig. H-1.

The program consists of two major parts. The first reduces the type 437A plate characteristics to digitized form and then interpolates several intermediate curves. The second performs the numerical computations as indicated in Section 1.

Approximation of the characteristic curves was done by representing each curve by a number of straight line segments. The points thus obtained were converted to slope-intercept straight line equations. Each curve was represented by 4 segments. The method of interpolation used was to bisect the angle between a given segment and the respective segment on the next higher grid curve. This was repeated until 17 curves had been obtained from the original 5. Figure H-2 illustrates the original curves obtained experimentally. Figure H-3 shows the approximation used for representing these curves and Fig. H-4 shows the method of interpolation used. The equations solved by the program are listed after Fig. H-4.

The results obtained agree closely with what would be expected with the values of circuit constants used. It is felt that the program would be useful for evaluating various combinations of input values. The program has been written so that any parameter of the circuit may be varied at will as well as the input pulse conditions. Since the original tube curves are not exact, it is felt that more exact curve fitting methods or interpolation methods would not be justified.

The program was written in the "IT" language which is an interpretive translator from a mathematical language format to "SOAP" language. The deck of cards to the 650 program is available if desired.



Period - $200 \cdot 10^{-9}$ sec
Rise time of grid - $8 \cdot 10^{-9}$ sec
Grid swing -1.0 to +1.0

Tube - 2 437A's in cascode
L = $200 \cdot 10^{-6}$ henries
C = 10^{-12} farads
R = 2000 ohms

Fig. H-1. Graph of solution of program analysis.

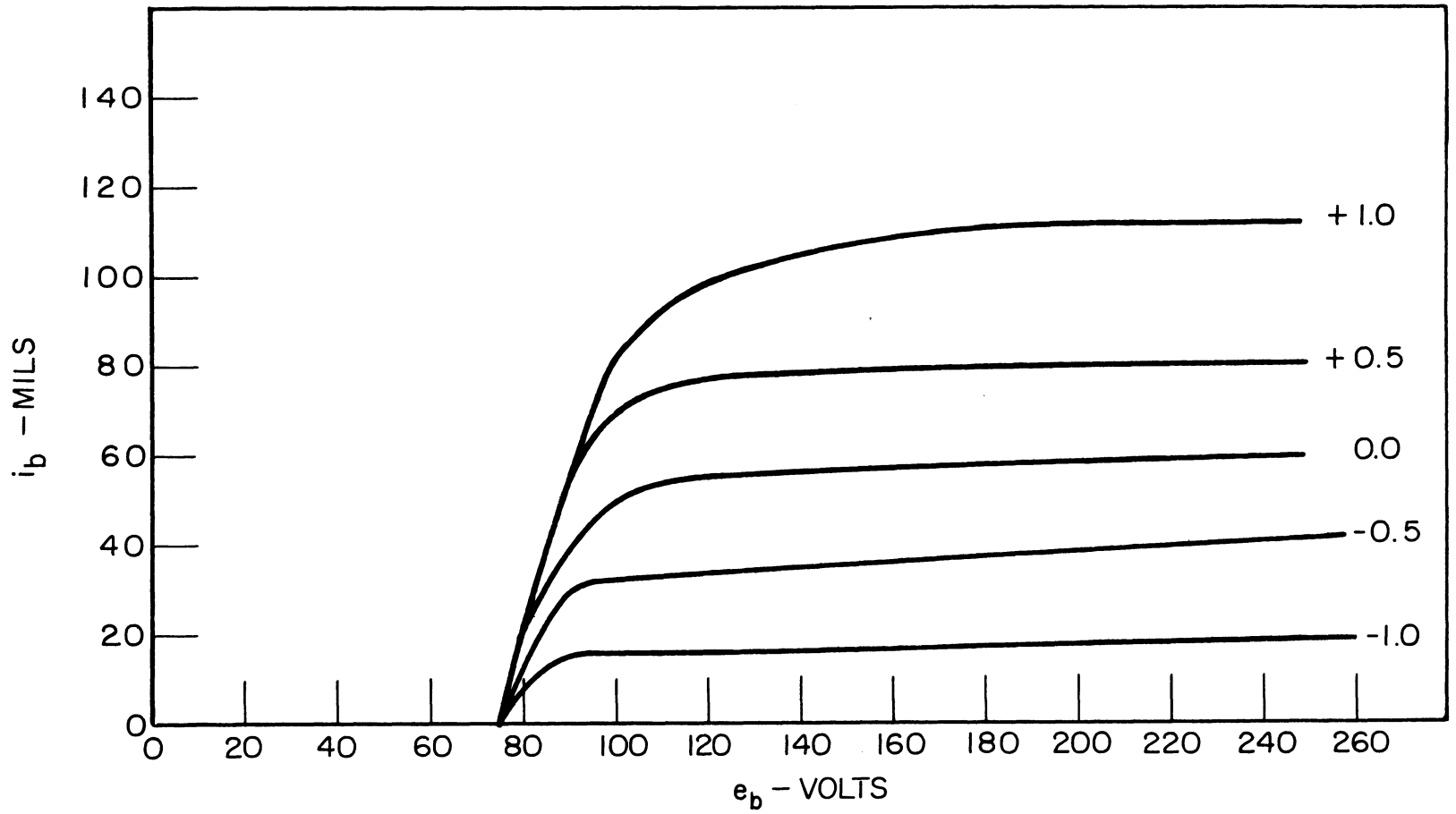


Fig. H-2. Plate characteristics of type 437A in cascode.

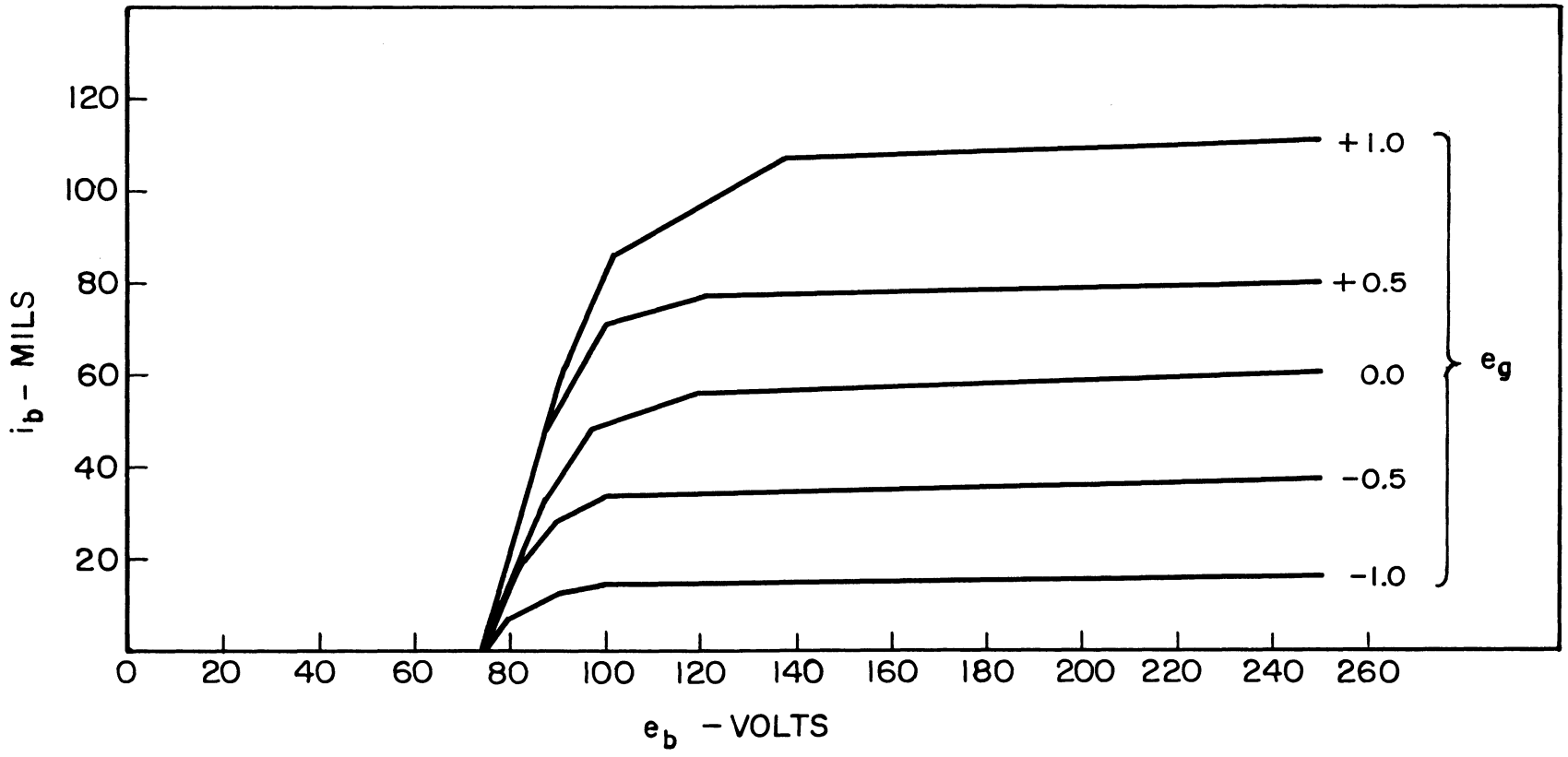
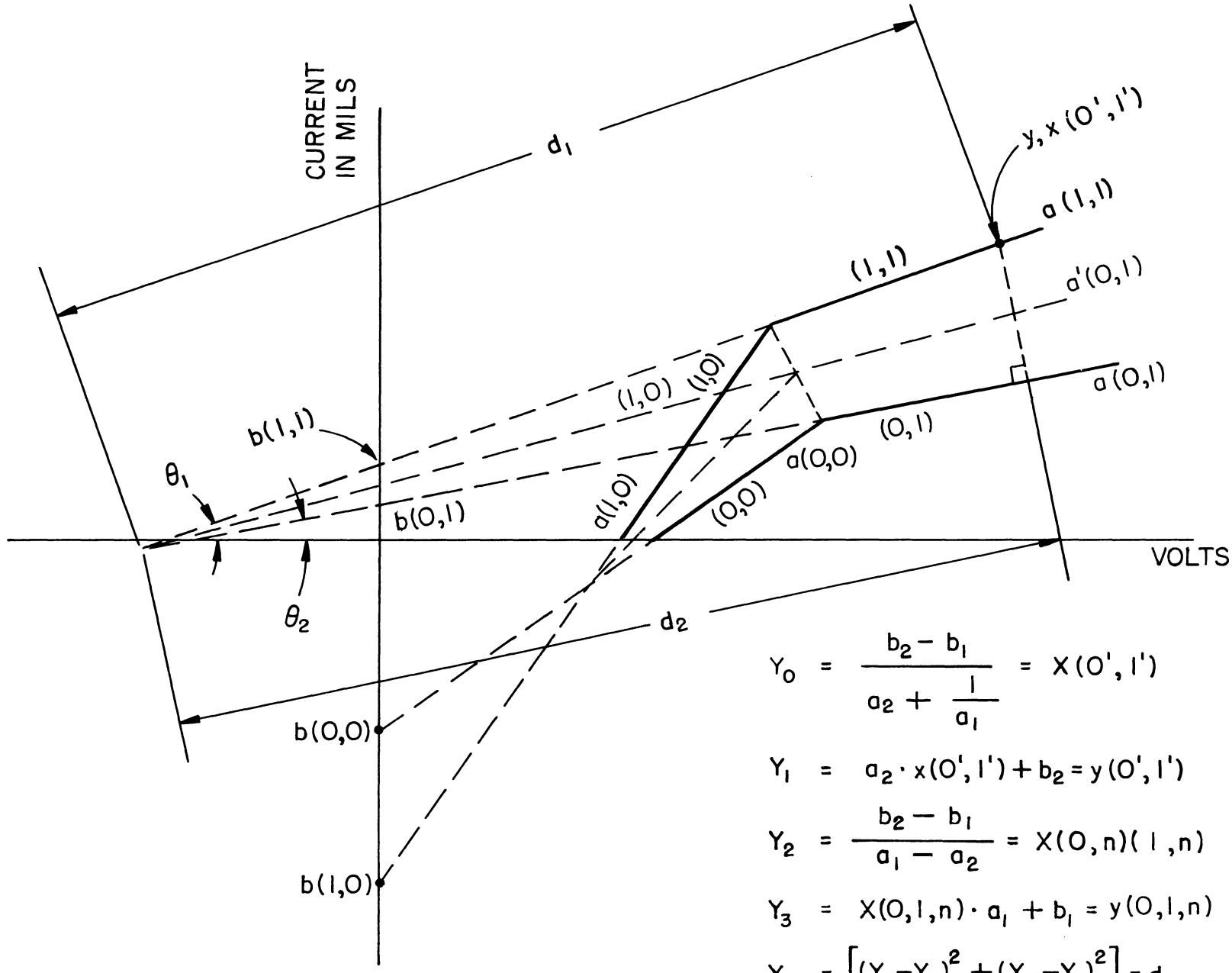


Fig. H-3. Approximated tube characteristics by straight line segments.



$$Y_0 = \frac{b_2 - b_1}{a_2 + \frac{1}{a_1}} = X(0', 1')$$

$$Y_1 = a_2 \cdot x(0', 1') + b_2 = y(0', 1')$$

$$Y_2 = \frac{b_2 - b_1}{a_1 - a_2} = X(0, n)(1, n)$$

$$Y_3 = X(0, 1, n) \cdot a_1 + b_1 = y(0, 1, n)$$

$$Y_4 = \left[(Y_2 - Y_0)^2 + (Y_3 - Y_1)^2\right] = d_1$$

Fig. H-4. Method of generation of intermediate curves.

$$Y_5 = \left\{ [x(0,1,n)^2 + y(0,1,n) - b_1] \right\}^{1/2} = d_2$$

$$Y_6 = \frac{d_2}{d_1} = \cos \theta_1$$

$$Y_7 = \left(\frac{1-\cos \theta_1}{1+\cos \theta_1} \right)^{1/2} = \tan \frac{1}{2} \theta_1 = a'_3$$

$$Y_8 = \frac{a_1 + a'_3}{1+a_1 \cdot a'_3} = \frac{\tan \theta_2 + \tan \frac{1}{2} \theta_1}{1 + \tan \theta_2 \tan \frac{1}{2} \theta_1} = \tan \left(\theta_2 + \frac{1}{2} \theta_1 \right) = a_3$$

$$Y_9 = y(0,1,n) - a_3 x\, x(0,1,n) = b_3$$

$$Y_0 = \frac{y^{(2)}_{lower} - y^{(1)}_{lower}}{x^{(2)}_{lower} - x^{(1)}_{lower}} = a'' \text{ (limiting line)}$$

$$Y_1 = y^{(2)}_{lower} - a' \cdot x^{(2)}_{lower} = b'' \text{ (limiting line)}$$

$$Y_2 = \frac{b''_3 - b_3}{a_3 - a''} = x_{\text{lower limit of bisector}}$$

$$Y_3 = b'' + a'' x_{lower} = y_{\text{lower limit of bisector}}$$

Fig. H-4 (concluded)

REFERENCES

1. C. C. Harris, "The 'Hard-Bottoming' Technique in Nuclear Instrumentation," Institute of Radio Engineers, Professional Group on Nuclear Instrumentation, Vol. NS-3, No. 2, March, 1956.

2. R. Denton, W. Brown, and W. Kilmer, Computer Components Development, The University of Michigan Engineering Research Institute Report No. 2452-2-P, January, 1957.

3. Ibid., p. 12, Table I.

4. G. T. Ford, "The 404A—A Broadband Amplifier Tube," Bell Labs Record, 27 (1949), 59.

5. A. H. W. Beck, Thermionic Valves—Their Theory and Design (Cambridge University Press, New York, 1953), p. 291.

6. R. A. Carlsen and D. C. Ray, Computer Components Development, The University of Michigan Engineering Research Institute Report No. 2452-3-P, Section 2.1, March, 1957.

7. For more complete discussion of the recovery of a parallel RLC circuit, see J. Millman and H. Taub, Pulse and Digital Circuits (McGraw-Hill Book Co., Inc., New York), pp. 52-57.

8. Ibid.

9. Ibid.

10. Ibid., pp. 258-262.

11. K. E. Monroe and H. L. Garner, Computer Components Development, The University of Michigan Engineering Research Institute Report No. 2452-4-P, March, 1957, p. 28, Table III.

12. R. D. Elbourn and R. P. Witt, "Dynamic Circuit Techniques Used in SEAC and DYSEAC," Trans. IRE, Vol. EC-2 (March, 1953), 2-9.