THIN FILM ELECTRONICS BASED ON ZNO AND ZNO/MGZNO HETEROJUNCTIONS

by

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To my beloved father

and

my mother

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In affirmation of my faith, I give all glory and praise to my Savior, the Lord Jesus Christ, who continues to strengthen and uplift my spirit. I am humbled and exceedingly joyful as a witness to his countless blessings.

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ABSTRACT

The ZnO TFT (Thin Film Transistor) has demonstrated improved electron mobility over entrenched, *a*-Si, technologies and is receiving considerable attention as an alternative TFT technology due to high transparency in the visible region and potential for flexible electronics on conformal substrates. This work studied the material properties of ZnO thin films deposited by pulsed laser deposition, provided a qualitative discussion of TFT operation, applied the buried-channel approach to enhance channel mobility, and demonstrated a complementary logic inverter circuit based on an *n*-channel ZnO TFT and a *p*-channel ZnTe TFT.

The material study in this work focused on optimal deposition conditions needed to realize low-resistivity ZnO thin films. Various techniques were used to illustrate the effect of decreasing polycrystalline ZnO grain size on carrier mobility and background carrier concentration as a function of thickness. Building on these results, discussion of TFT operating principles concentrated on explaining its dependence on carrier concentration and active-channel thickness. The resulting performance of surface-channel ZnO TFTs demonstrated saturation mobility of $\mu_{SAT} = 1.8 cm^2/Vs$, current on/off ratio of $I_{ON}/I_{OFF} > 10^9$, and off current of I_{OFF}=10pA.

A buried-channel approach to suppress the effect of electron trapping on carrier transport by isolating the ZnO active channel was presented. Quantum confined

structures, such as quantum wells, enhance speed of electronic devices due to carrier confinement. Quantum wells based on the $ZnO/Mg_xZn_{1-x}O$ ($x \leq 0.3$) material system have been grown on c-plane sapphire substrates. Luminescent properties characterized by low-temperature photoluminescence revealed quantum confinement with a systematic blueshift as a function of decreasing ZnO well width in the range from 3nm to 10nm. An enhancement in saturation mobility of $3.9 cm^2/V\text{-}s$ was achieved by utilizing the ZnO/MgZnO heterojunctions to fabricate a buried-channel TFT.

Finally, incorporation of a ZnTe TFT, exhibiting relatively high hole mobility ($\sim 5 cm^2/Vs$), and ZnO TFTs in a complementary logic inverter circuit demonstrated reasonable transfer characteristics. Inverter behavior is demonstrated, with a high output voltage of $V_{OH} > 14V$ and low output voltage of $V_{OL} < 0.2V$ are observed for a supply voltage of 15V. The small signal gain for the transfer characteristic is found to be $-dV_{out}/dV_{in} > 5$ at $V_{in} = 6V$.

Chapter I

INTRODUCTION

The modern era of semiconductor electronics owes its existence to the rapid expansion of the metal-oxide semiconductor field-effect transistor (MOSFET), first proposed in 1930 by Lilienfield [1] and developed for practical use in 1960 by Kahng and Atalla [2]. It offered more miniaturization, cost reduction, and longer operating lifetime than the vacuum tube. It is the most important device for very-large scale integrated circuits (ICs) used in logic and semiconductor memory devices. One distinct characteristic of IC technology is its complex integration of many thousands of active and passive devices made primarily in a single wafer of silicon, thus enabling new applications for electronics in communication, control, and data processing not possible with discrete components.

The first all thin-film integrated circuit for scanning an image sensor containing CdSe thin-film transistors (TFTs) was produced in 1965 by Weimer [3]. This allowed for fabrication of transistors and other passive devices on insulating substrates which reduces parasitic losses associated with embedded silicon substrates. Historically, the patent invention by Lilienfield [1] describing the flow of current varied by electrostatic influence from an insulated gate electrode in a semiconductor of minute thickness

actually describes the first thin-film field effect transistor. A typical TFT under normal operating conditions is shown in Figure 1.1. The application of a positive-bias to the gate electrode induces the accumulation of electrons in the case of an *n*-type semiconductor. At the same time, the positive input voltage at the drain leads to the flow of current as electrons flow from source to drain (reverse electrode voltages for a p-type semiconductor).

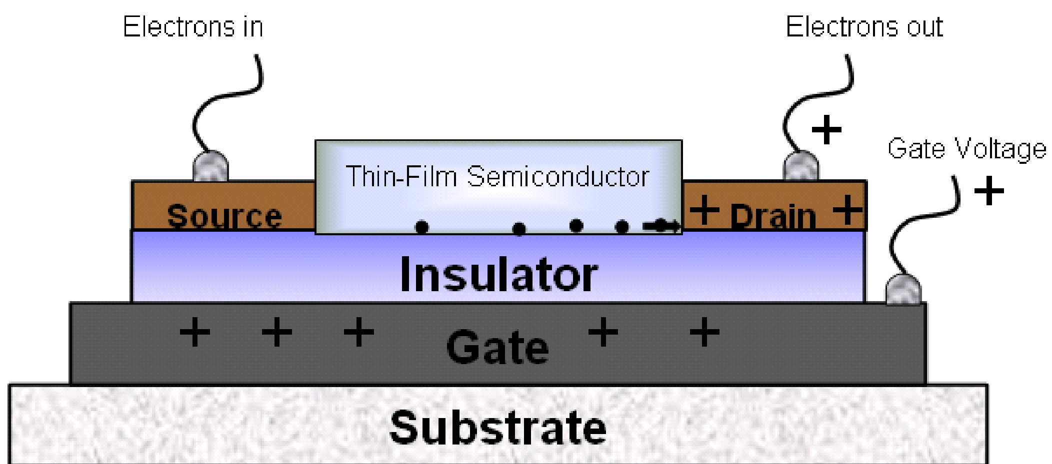


Figure 1.1 Typical TFT under normal operation conditions with electrodes marked.

Because of established processing techniques for silicon technology, MOSFETs developed more rapidly than TFTs. However, a new field of macroelectronics is emerging for thin-film, flexible, large area electronics and systems enabling TFTs. These applications include integrated displays, photovoltaics, embedded power sources, sensing devices, smart labels, lighting, and integrated logic devices. Figure 1.2 projects the emerging distribution of predicted growth forecasts for commercially accessible markets employing TFTs and thin-film electronics [4]. This includes inorganic and organic devices, semiconducting and printed, on rigid and flexible substrates.

Figure 1.2 Distribution of predicted growth forecasts for various emerging applications enabling TFT development.

1.1 Thin-Film Transistors for Display Electronics

Electronic display technology once limited to the bulky, rugged cathode ray tube (CRT) has matured into an expansive area of industrial commercial development and academic research. Whereupon plasma displays are commercially available for large size television monitors, active-matrix liquid crystal displays (LCDs) and active-matrix organic light-emitting diodes (OLEDs) are the leading technologies for portable display of information. LCDs which preceded OLEDs as the dominant mobile flat-panel display technology is a passive type of display which requires either front (reflective) or rear (transmissive) illumination. However, OLEDs are emissive devices which generate light at the display surface without the need for an external source of illumination. Typically both devices are fabricated on glass substrates, though use of glass substrates poses the undesirable characteristic of being rigid and fragile. Applications including electronic books (e-books), foldable cell phone displays, wearable displays, and compact military display systems are driving the growth for flexible electronic display technology. Flexible displays along with the integrated back-plane electronics compel the need for plastic or

thin metal foil substrates that are unbreakable, rollable, lightweight, and flexible. The back-plane electronics providing the active-matrix switching rely on thin-film transistors (TFTs).

Hydrogenated amorphous silicon (a-Si:H) and polycrystalline silicon (poly-Si) TFTs are the industry standard for the switching and drive circuitry of monolithic active matrix LCD and OLED technology. Overwhelming advantages in favor of poly-Si TFTs are motivated by the need to address low electron field-effect mobility ($< 1\ cm^2V^{-1}s^{-1}$) associated with a-Si TFTs, and enabling integrated complementary metal oxide semiconductor (CMOS) circuits with high performance n- and p-channel poly-Si TFT devices [5]. However, undesirable large OFF-state leakage current ($> 10^{-10}$ A) and high processing temperature are challenges in poly-Si TFT device development. The large leakage current limits charge switching between ON and OFF states. Suppression of high leakage current is concentrated on modification of the device structure or pixel circuit architecture [6]. There has been mounting interest in the use of oxide thin-film transistors (TFTs) as electronic back-plane switching devices for the next generation of large-area flat-panel display applications. Zinc oxide (ZnO) is receiving considerable attention as an alternative TFT technology due to high transparency in the visible region, high ON-to-OFF state switching ratio, and improved mobility over opaque a-Si. A snapshot comparison of the saturated channel mobility as a function of channel width/length (W/L) for various technologies is shown in Figure 1.3. Decreasing mobility with increasing W/L is consistent with all technologies presented. This is due to effects associated with contact resistance and fringing electric-field effects [7].

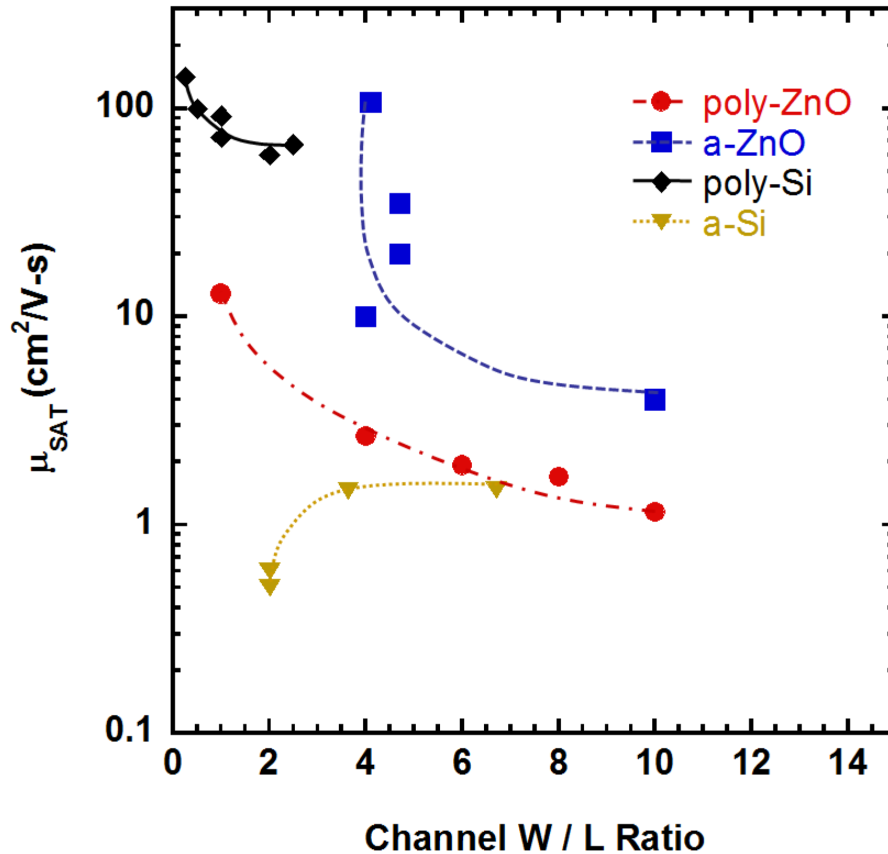


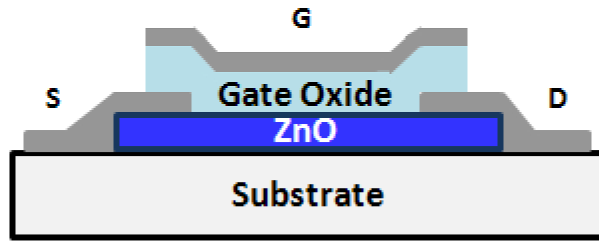
Figure 1.3 Comparison of saturated channel mobility of various TFT active channel material as a function of W/L [8-24].

1.2 Zinc Oxide Thin-Film Transistors

The first reported ZnO insulated-gate field-effect transistor fabricated in a coplanar configuration was demonstrated by Boesen and Jacobs in 1968 [25]. The wide band-gap (E_g=3.37eV at 300K) of ZnO prohibits device degradation due to carrier photo-generation with exposure to light. This intrinsic property alleviates the need for external shielding during device operation. In this work, polycrystalline ZnO TFT devices are fabricated and the effect of material properties on its DC operating characteristics is discussed. While the coplanar configuration is widely used with the conventional MOSFET device structure, there are essentially three types of TFT configurations: the coplanar, staggered

(top-gate), and inverted-staggered (bottom-gate) structures. The difference in configuration is defined by the position of the gate and source/drain electrodes with respect to the gate insulator and semiconductor layer. The coplanar structures have all three electrodes on one side of the semiconductor layer; whereas, the staggered structures have the gate electrode and the source/drain electrodes on opposite sides of the semiconductor layer [26]. Figure 1.4 depicts a schematic cross-section of the coplanar, top-gate, and bottom-gate ZnO TFTs. Because the bottom-gate TFT is the most extensively reported ZnO device of those previously mentioned, we will concentrate on its formation.

Processing of thin film transistors are composed of four key parts: the gate electrode, the gate insulator, the ZnO active channel region, and the source/drain ohmic contacts. Since the channel region-gate insulator interface is where carrier transport predominately takes place, considerable attention has been devoted to its development. Fixed interface charges (surface states) at the ZnO-gate insulator interface impede carrier flow due to scattering and are detrimental to carrier mobility along the ZnO channel region. As a result, the choice of gate dielectric and pre-ZnO layer surface preparation plays an important role in interface quality. Silicon dioxide, SiO_2, possesses the attributes of being an extremely good insulator and is the predominant gate dielectric as evidenced in the literature [9,27,28]. Experiments have been reported on the influence of different gate dielectrics on ZnO TFT properties. The use of high-k dielectrics (ε_r>3.9) allows for thicker gate dielectrics resulting in reduced gate leakage and increased capacitive coupling between the ZnO layer and the gate dielectric. This will make available stable operation of transistors with high operating currents at low operating voltages. There



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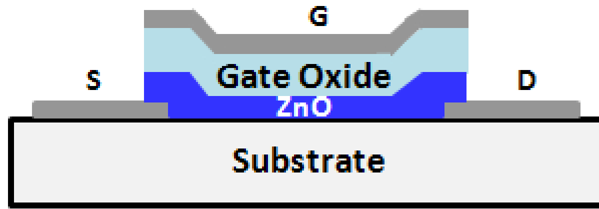

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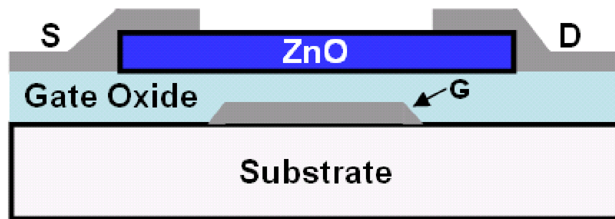


(c)

Figure 1.4 The schematic cross-section of the (a) coplanar; (b) staggered (top-gate); and (c) typical inverted-staggered (bottom-gate) TFT structures.

have been several reports on promising alternatives such as Si_3N_4 [8], SiN_x (ε_r=6) [11], (Ba,Sr)TiO_3 (ε_r=16-500) [29-31], Al_2O_3 (ε_r=7) [12], HfO_2 (ε_r~30) [32], and $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ (ε_r~51) [33]. Unfortunately, the use of high-k dielectrics does not alleviate electrical degradation caused by carrier trapping at the gate dielectric-active layer interface.

From these studies, it is clear that accumulation of carriers forming the conducting channel for a thin film transistor have to be physically separated in order to minimize

interface trapping and enhance device performance. One way that this can be achieved is by inserting a thin higher-gap material, MgZnO, adjacent to the gate insulator interface with carrier confinement in the lower-gap material, ZnO, thereby forming a buried-channel layer for carrier transport experiencing less scattering and surface interface trapping [34].

1.3 Complementary Electronics using Zinc Oxide Thin-Film Transistors

Flexible electronics that can be subjected to deformation, including twisting, bending, and stretching will provide for interesting applications. These applications include artificial sensor skin, radio frequency identification tags, and wearable electronics on the human body that can be used for computation, information storage, and sensing. Semiconducting oxides including polycrystalline ZnO and amorphous indium gallium zinc oxide (IGZO) have recently emerged as important candidates for thin film transistors intended for flexible electronics due to their relatively high carrier mobility (~10cm^2/Vs) and ability for low deposition temperature. These flexible transistors can be utilized in applications requiring flexible logic circuitry. Digital logic and related electronic circuitry would benefit tremendously from a complementary device technology in semiconducting oxides. However, these materials are all intrinsically n-type and have not demonstrated a reliable means for obtaining p-type thin films. Alternatively, polycrystalline ZnTe thin films are intrinsically p-type and exhibit relatively high hole mobility (~5cm^2/Vs) at low deposition temperatures (~200^{0}C). In this work, ZnO and ZnTe thin film transistors (TFTs) are fabricated and characterized. After electrically connecting the TFTs in the appropriate configuration, complementary logic inverters are demonstrated.

1.4 Objective and Organization of this Dissertation

The purpose of this dissertation is to develop a buried-channel technique, based on the polycrystalline ZnO/MgZnO material system, for improved thin film transistor performance and demonstration of a complementary logic inverter based solely on inorganic thin film transistor technology. Electron trapping near the gate dielectric/ZnO interface of conventional surface-channel ZnO TFTs significantly impacts carrier transport and thus limits device performance, specifically the field-effect mobility. Since electron accumulation with appropriate biasing occurs in close vicinity of the interface, typically on the order of 10nm or less, the fabrication of TFTs where conduction takes place in the higher quality ZnO material away from the gate dielectric interface is extremely beneficial. Tradeoffs with the thickness and conduction band offset for the higher energy gap, MgZnO, material are therefore critical to maintaining electron accumulation in the buried-channel. Afterwards p-channel ZnTe TFTs are demonstrated, and the integration of these devices with buried-channel n-channel ZnO TFTs for a complementary inverter circuit are shown to exploit this technologies' relevance for enabling logic integrated circuits (ICs). Figure 1.5 shows a flowchart of the dissertation outline.

Chapter II discusses material growth and characterization of polycrystalline ZnO thin films. Basic aspects of growth by pulsed laser deposition (PLD) are reviewed. The structural, optical, and electrical properties of thin film material are characterized by X-ray diffraction (XRD), transmission electron microscopy (TEM), photoluminescence, and Hall-effect measurement. These characterization techniques are later used to characterize

the grain size, orientation, optical energy gap, and alloy effects of the II-VI semiconductor, zinc telluride (ZnTe), and the alloy, magnesium zinc oxide (MgZnO).

Chapter III presents the operating and design principles of the TFT device. Qualitative description of conventional TFT operation and its dependence on the undoped background carrier concentration (N_B) and thickness (t_{ZnO}) of the active channel layer are reviewed. A two-dimensional numerical model of the TFT device assuming homogenous material is used to illustrate the effect of N_B and t_{ZnO} on the TFT semiconducting channel and output characteristics. Non-idealities of polycrystalline TFTs, such as field-effect mobility and threshold voltage extraction, introduce a certain degree of ambiguity. Mobility dependence on gate bias and threshold voltage by power law extraction gives insight into the transport characteristics' dependence on scattering and trapping mechanisms at the gate dielectric interface.

Chapter IV discusses the fabrication and static DC test results of ZnO TFTs. To avoid confusion associated with the use of different techniques, conventional square-law theory is used to extract the threshold voltage and field-effect mobility of the TFTs. The experimental dependence of N_B and t_{ZnO} on output characteristics are presented, and the results are used for developing reproducible TFTs and convey the need for active-channel layer tailoring to achieve increased mobility.

Chapter V presents the optical properties of ZnO/$Mg_xZn_{1-x}O$ (x=0.17) quantum wells (QWs) grown on c-plane sapphire substrates by pulsed laser deposition are presented. A blueshift in the low-temperature photoluminescence of the QWs illustrate quantum confinement effects as a function of ZnO well widths in the range from 3nm to 10nm. This demonstration of quantum confinement is suitable for fabricating buried-

channel TFTs with the lower energy gap ZnO layer and electron accumulation physically separated from carrier trapping effects at the gate dielectric interface.

Chapter VI discusses the fabrication and device characteristics of ZnTe TFTs. The ZnTe films exhibiting p-type carrier concentration form the active channel layer of the p-channel device. ZnTe layers were deposited by ablation of a ZnTe pressed target using PLD under vacuum (10^{-6} Torr). Despite the inferior transistor behavior of the ZnTe device, incorporation of the ZnTe and ZnO TFTs in a complementary logic inverter circuit demonstrates reasonable transfer characteristics. Static operation of the complementary thin-film inverter circuit is characterized and the results analyzed.

Chapter VII summarizes the obtained results and presents proposed directions for future work. Further studies on the introduction of high-k gate dielectrics for higher drive currents at lower operating bias are discussed. Exploration of device process techniques for a buried-channel ZnO TFT is suggested. Finally, further improvement of the ZnTe thin films are addressed for optimized static operation of purely inorganic complementary logic inverters.

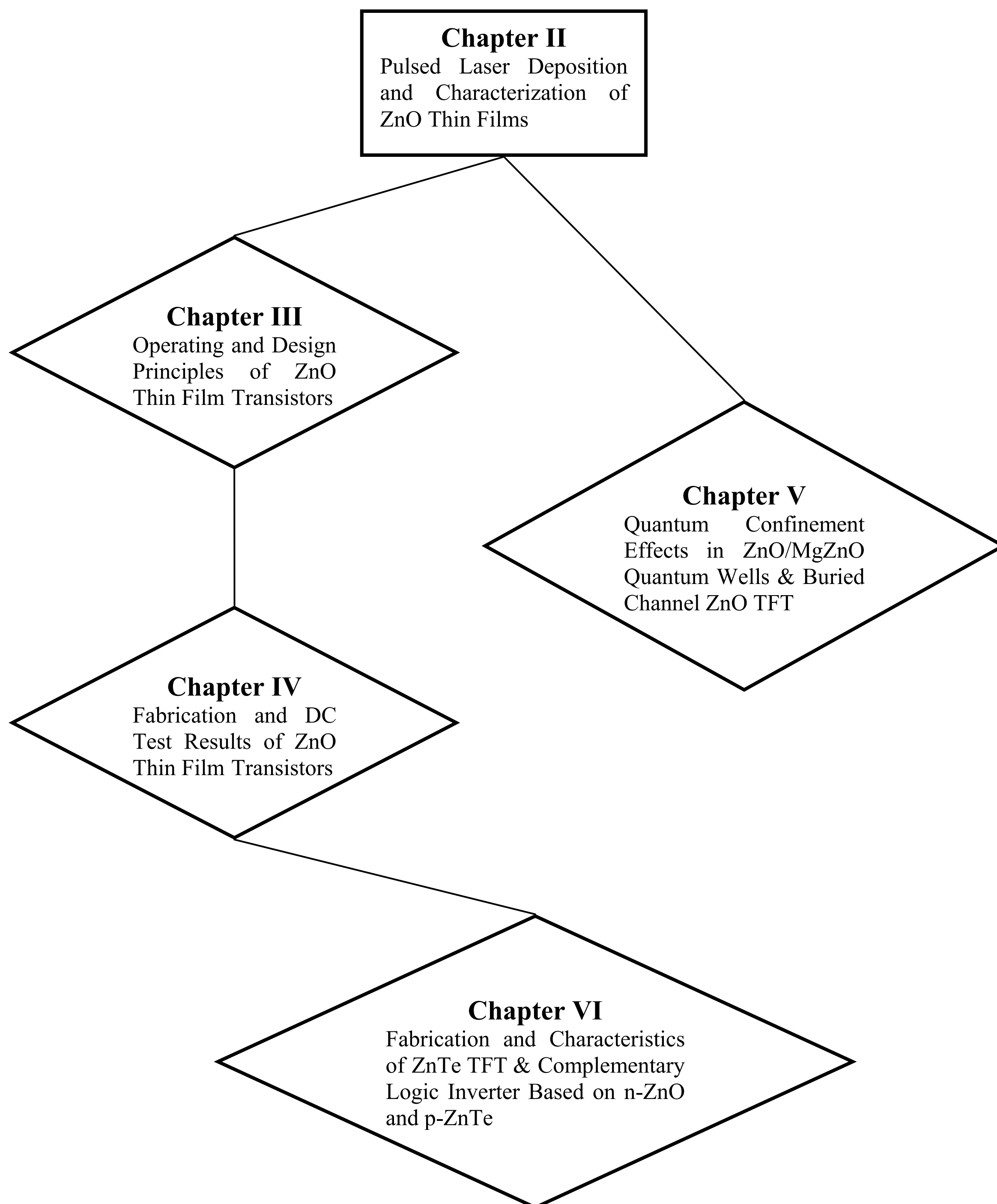


Figure 1.5 Flowchart of dissertation outline.

Chapter II

PULSED LASER DEPOSITION OF ZNO THIN FILMS

2.1 General Introduction of ZnO Properties

II-VI compounds giving rise to semiconducting materials cover a considerable part of the light spectrum; from near infrared (CdTe) into the ultraviolet (ZnS) region. In addition to the established II-VI wide band-gap compounds ZnS, ZnSe, ZnTe, CdS, and CdSe and other direct band-gap materials such as GaN and SiC, zinc oxide is a wide, direct gap semiconductor (ZnO, $E_g = 3.4eV$ at 300K) which has garnered the focus of intense materials research and device development. Distinguishing advantages of ZnO include: (i) the availability of large area native substrates [35], (ii) highly transparent in the visible region, (iii) an exciton binding energy of 60meV which ensures excitonic emission at temperatures above room temperature ($k_BT = 26meV$), (iv) its resistance to high energy radiation damage which enables application in hostile environments [36]; and (v) its susceptibility to wet chemical processing [37]. The comparison of material properties for ZnO and other wide band-gap compounds is given in Table 1. ZnO crystallizes in the wurtzite structure with a hexagonal lattice as shown in Figure 2 and is similar in energy gap to GaN. Furthermore with a lattice mismatch less than 1.8%, it is suitable as an alternative substrate for growth of high-quality GaN epilayers and its alloys [38]. ZnO, which has a tendency to grow with c-plane (0001) preferential orientation, has

Materials	Crystal Structure	Bandgap Energy (eV)	Lattice Constants a (Å)	c(Å)	Exciton Binding Energy (meV)
ZnO	Wurtzite	3.4	3.25	5.21	60
ZnS	Wurtzite	3.8	3.82	6.26	39
ZnSe	Zincblende	2.7	5.67		20
GaN	Wurtzite	3.4	3.19	5.19	21
6H-SiC	Wurtzite	2.9	3.08	15.1	---

TABLE 2.1 Comparison of material properties of ZnO with that of other wide band gap semiconductors.

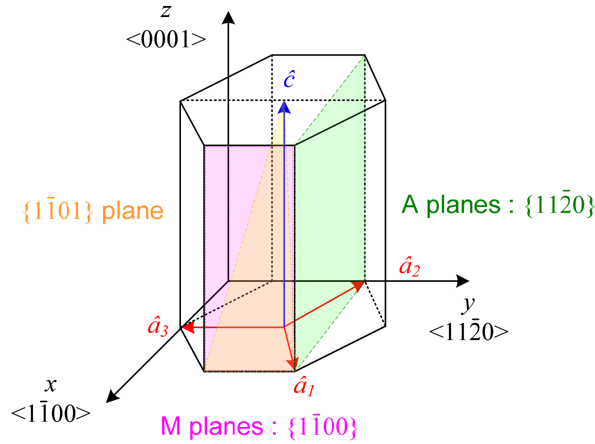


Figure 2.1 Wurtzite lattice for ZnO illustrating a-plane, c-plane, and m-plane.

been shown to exhibit m-plane (10$\bar{1}$0) orientation on cubic MgO substrates [39] and a-plane (11$\bar{2}$0) orientation on r-plane sapphire [40]. Though the natural structure of ZnO is wurtzite resulting in the existence of polarization along the c-axis, growth along these alternative orientations provide for nonpolar epitaxial ZnO.

Additional advantages associated with ZnO and other wide band-gap semiconductors are its thermal stability which facilitates high-temperature operation and the high breakdown voltage making it ideal for high-power switching devices. While the electron drift velocity of GaN and ZnO are comparable, the peak electric field for ZnO is

about 100kV/cm higher than GaN [41]. Its direct band-gap and large exciton binding energy make it attractive for optoelectronic devices such as ultraviolet (UV) photodetectors and blue-UV light emitters, such as light-emitting diodes (LEDs) and laser diodes (LDs). Other applications include surface acoustic wave devices [40], gas sensors [42], and transparent conducting films for solar cells [43]. The tremendous potential of ZnO and novel devices based on the II-VI material is further broadened by band-gap engineering. Alloying with CdO and MgO allows for modulation of the bandgap from 3.0eV ($Cd_yZn_{1-y}O$) to 4.0eV ($Mg_xZn_{1-x}O$). Heterojunctions based on the II-VI oxide semiconductor and its ternaries make possible the fabrication of such devices as high electron mobility transistors (HEMTs) [44] and tunable wavelength optoelectronic devices.

Realization of a homogeneous ZnO optoelectronic device requires n- and reliable p-type ZnO, which has been problematic. This is analogous to the p-type conductivity limitations that once hindered other wide band-gap II-VI materials such as ZnS, ZnSe, and GaN; similarly, there is an n-type doping limitation in the case of ZnTe. There have been reports on p-type ZnO material with the group V elements N [45], P [46], As [47], Sb [48], and Bi [49], though stability and reproducibility are controversial. With smaller ionic radii than that of O, N is the most promising dopant though P doping has resulted in the lowest resistivity p-ZnO material with ρ=0.6 Ω-cm [50,51]. Nonetheless, several authors have reported on the fabrication of ZnO homojunction light emitting devices [52]. In the absence of p-ZnO, high-quality heterostructure LED devices are possible and have been fabricated using p-GaN [53].

The shallow donor naturally occurring in n-type ZnO is attributed to native point defects associated with zinc and oxygen vacancies, interstitials, and antisites [54]. The equilibrium concentration of the defect affects the electrical and optical properties of the metal oxide. Using first-principle calculations of defect formation energy as a function of the Fermi energy, the two most abundant defects in Zn-rich material were shown to be zinc (V_{Zn}) and oxygen (V_O) vacancies which act as donors. Because V_O has lower formation energy than zinc interstitials (Zn_i), it is expected to occur in higher concentration. Though under O-rich conditions, V_{Zn} is the main native point defect. For both the Zn-rich and O-rich material, the transition from the -1 to -2 charge state of V_{Zn} occurs at approximately 0.8eV above the valence band. This is a possible mechanism for the pronounced broad-band green luminescence commonly observed at approximately 2.4eV by radiative transition between shallow donors and acceptors (V_{Zn}) [55,56]. However, recent density functional theory calculations have shown that hydrogen is the likely origin of native donor activity. Because hydrogen (H) is unavoidable in most growth environments, it was concluded that compensating effects due to H act to make p-type doping difficult [57,58].

Although high quality ZnO substrates have better structural, optical, and electrical properties, growth of ZnO single-crystal or polycrystalline thin films allow for variation of the film properties and incorporation of dopants by control of deposition conditions. ZnO thin films have been grown by various growth techniques, such as: sol gel, rf sputtering, metal-organic chemical vapor deposition (MOCVD) [59], molecular beam epitaxy (MBE) [39], and pulsed laser deposition (PLD) [60]. In this thesis, PLD is used for polycrystalline growth of c-axis oriented ZnO thin films on sapphire (c-Al_2O_3)

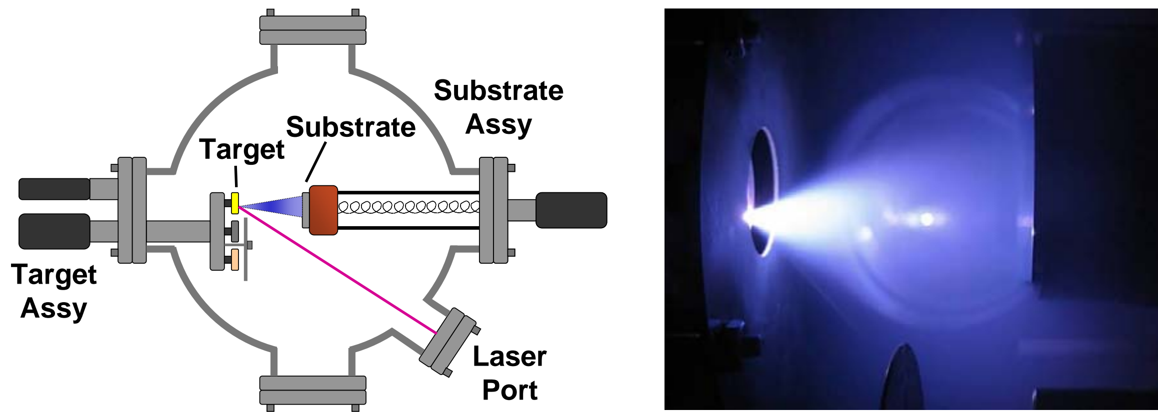
substrates for optically characterized quantum well structures and on thermally oxidized silicon substrates for eventual fabrication of thin film transistors.

2.2 Basic Aspects of Pulsed Laser Deposition

Pulsed-laser deposition (PLD) is defined as the formation of thin films and multilayer structures on a substrate by a plume of evaporated material created when an external pulsed laser source with sufficiently high-energy density ablates a flat target surface. The highly energetic plume of ablated species is forward-directed normal to the target surface and condenses on a substrate located opposite the target. The substrate is bonded to a substrate heater thus allowing good adhesion and making certain epitaxial quality for the deposited material. For deposition of metal oxide epitaxial films such as ZnO, oxygen (O_2) at high ambient gas pressures in the 10^{-4} to 10^{-2} Torr range are easily pumped into the chamber using a gas inlet valve and regulated with a mass flow controller thus enabling control of oxygen stoichiometry.

PLD offers the following advantages over competing thin-film growth techniques such as sputtering, molecular beam epitaxy (MBE), or metal-organic chemical vapor deposition (MOCVD): a) simple and versatile experimental setup with economical start-up cost; b) high-quality film growth at moderate substrate temperatures (typically ~600°C) with uniformities better than ± 0.5%; c) fast laser pulses giving rise to high peak energies which is advantageous for oxide thin films with high melting points [61]; and d) easily formed in-situ multilayer structures by target manipulation into and out of the beam of the energy source, laser. A schematic diagram of the PLD chamber illustrating the cone-shaped plume of target material directed at the heated substrate is shown in Fig. 2.2(a). Figure 2.2(b) displays the multilayer PLD system used in this thesis. The entire

system consists of three primary components: laser source, external optics, and deposition chamber.



(a)

(b)

Figure 2.2 (a) Schematic diagram of a pulsed-laser deposition chamber illustrating expansion of the plume profile and (b) the multilayer PLD system with KrF (λ = 248 nm) laser, focusing optics, and chamber.

Laser wavelengths between 200-nm and 400-nm are required of the external laser source due to the strong absorption exhibited for most materials in this range. As laser emission approaches 200-nm, the absorption coefficient of the target material tends to

increase and the penetration depth into the target are reduced [62]. This results in a thinner layer of the target material surface being ablated and a lower laser fluency threshold for ablation. The excimer laser, a gas laser system, emits its radiation directly in the UV and is generally the laser of choice for PLD work. Of the active excimer molecules used for commercial laser systems, KrF with an operating wavelength of 248-nm has the advantage of being a high gain system which also delivers sufficiently high output pulse energies. The KrF excimer laser with pulse duration of 25nsec used in this work was manufactured by Lambda Physik, Inc.

Between the laser source and the deposition chamber, optical elements are used to collect the radiation from the laser and focus it to a point on the target. Because the laser energy density (in J/cm^2) incident on the target is one of the factors which determines crystal quality and preserves composition of the ablated material during growth, significant care is taken to align the cylindrical collimating lenses. Once the laser beam profile on the target is optimized by way of lens ordering, the laser energy is then set for a desired minimum threshold fluence needed to ablate the target material.

After the laser beam passes through the optical elements, it passes through the laser window on the deposition chamber. Thus, the laser window must be periodically cleaned and unobstructed so that the desired laser fluence on the target is realized. The spherical PLD chamber manufactured by Neocera, Inc. contains the ZnO ceramic target 99.999% pure, substrate holder and heater assembly, and variable background gas (i.e. oxygen) which enables control of crystalline stability. The ability to adjust the target-to-substrate distance, S, is desirable in so far as it allows for adjustment of the growth rate. While a smaller S allows for lower laser energy, it also allows for undesired impurities which can

be as much as several microns in size being deposited within the thin film during growth. However, highly dense targets help reduce the generation of those unwanted impurities. Rotating the disk-shaped target attached to a target mount along its rotation axle allows for uniform erosion during deposition. As the evaporated target material condenses on the substrate, thermal distribution across the substrate surface (1-2.5 cm^2) becomes significant. Bonding the substrate to the substrate heater with an appropriate adhesive improves temperature uniformity. Silver paint, commonly used during microscopy sample preparation, is used for bonding due to its thermal conductivity, strong mechanical bond, and ease of substrate removal. With a basic foundation of PLD, the influence of growth conditions on structural and electrical properties of ZnO thin films are discussed next.

2.3 Material Characterization

ZnO thin films were grown on single-side polished sapphire (0001) and pre-oxidized silicon (100) substrates by pulsed laser deposition. The rotating single-crystalline ZnO target (99.999% pure) was placed at a distance of 4cm from the substrate and ablated using a KrF excimer laser (248nm, 6 Hz, 25 nsec) with a fluence on the target of 1.5 J/cm^2. The films were grown at an optimized substrate temperature of 600°C in ultra-pure oxygen (99.999%) ambient gas pressure of $p(O_2)$=30x10^{-3} Torr. Under the above PLD conditions, the resulting deposition rate is on the order of ~3 Å/sec.

The as-grown ZnO films were characterized using various techniques as necessary for optimizing growth conditions and gaining insight on details of material quality. Material surface morphology and crystalline texture are studied by atomic force microscopy (AFM) and x-ray diffraction (XRD), respectively. Film thickness is measured

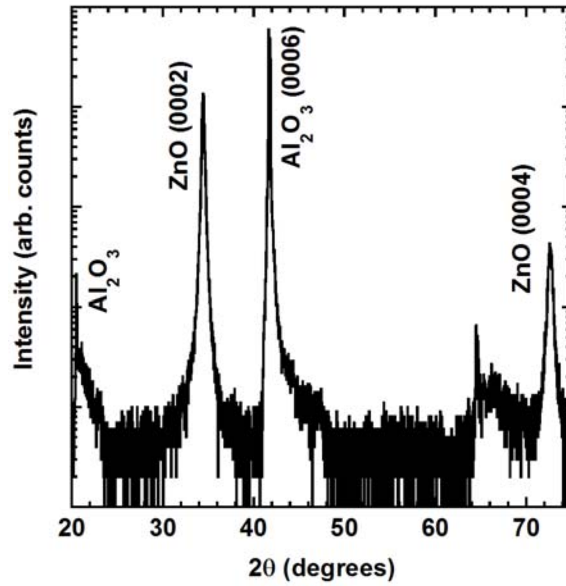
using optical reflectance, and the band-gap of the ZnO layers is gathered from the peak wavelength of the near-band-edge signal using low-temp photoluminescence (PL). Intrinsic electrical characteristics of the layer are studied by Hall effect measurement. The material characterization techniques used in this study are reported below together with the corresponding results. A detailed discussion on the structure and optical properties of single quantum well structures based on the ZnO/MgZnO material system using transmission electron microscopy (TEM) and PL, respectively, are found in Chapter 5.

2.3.1 Structural Characterization

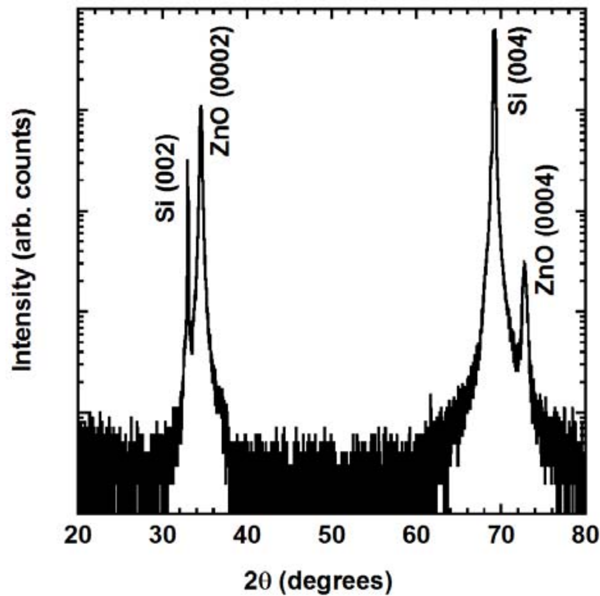
The XRD technique is commonly used to determine the crystalline quality and preferential orientation of the ZnO films. All the θ-2θ XRD results shown in this work were obtained using a Rigaku X-ray diffractometer with Cu $K\alpha$ radiation ($\lambda = 1.5406$ Å). Figure 2.3 (a) & (b) show θ-2θ spectra of polycrystalline thin films having wurtzite-type structure and strong growth orientation along the (000ℓ) on Al_2O_3 (0001) and SiO_2/Si (100) substrates, respectively. The 2θ diffraction angle occurred at 34.44^o for ZnO/Al_2O_3 and at 34.5^o for the ZnO/SiO_2/Si thin film. Based on the peak position of the (0002) diffraction, the lattice constant c was calculated using Bragg's law to be 5.204 Å for ZnO thin film on the Al_2O_3 substrate and 5.195 Å for that on the SiO_2/Si substrate. The full width at half maximum (FWHM) of the (0002) peak was measured to be 0.26^o and 0.28^o for Fig. 2.3 (a) and Fig. 2.3 (b), respectively. The crystalline grain size is calculated using the Scherrer formula given in Eq. 2.1:

$$D = \frac{0.89\lambda}{B\cos\theta} \tag{2.1}$$

where D is the crystallite grain size, λ the X-ray wavelength, θ the Bragg diffraction angle, and B the peak width at half maximum (FWHM). Whereas the grain size for a 300nm thick ZnO film on Al_2O_3 was 73nm, the grain size for a 90nm thick film on the



(a)

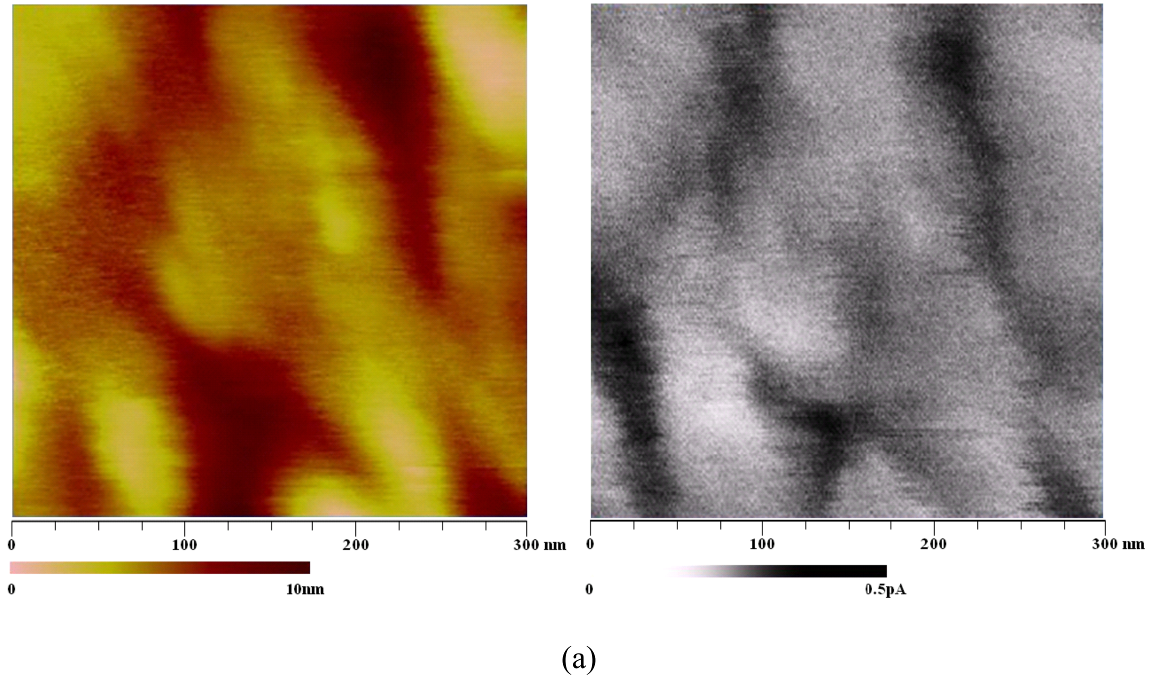


(b)

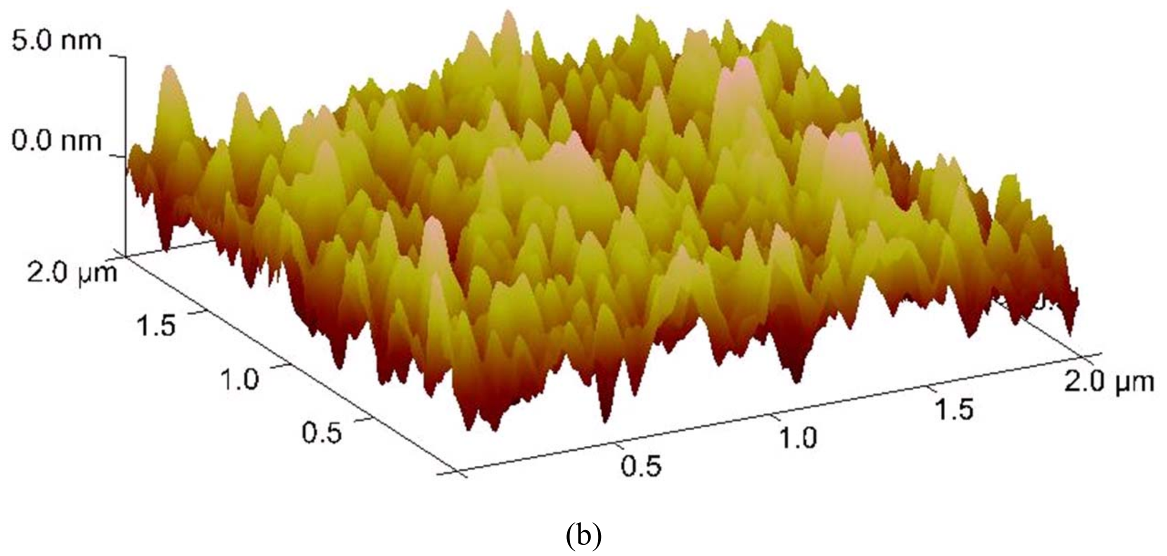
Figure 2.3 X-ray diffraction patterns for the ZnO thin films grown on (a) Al_2O_3 (0001) and (b) SiO_2/Si (100) substrates.

SiO_2/Si substrate was 68nm. It has been shown that the FWHM of the (0002) diffraction peak from XRD data decreases and the corresponding film grain size increases with an increase in ZnO thickness [63]. In this work the growth of ZnO thin films on amorphous SiO_2/Si substrates for application in thin-film transistors is expected to result in reduced stress in the film [64].

The surface topography of ZnO thin film (~ 90 nm) by PLD on SiO_2/Si substrates with a substrate temperature of 600°C were studied by atomic-force microscopy (AFM). An average surface roughness less than 3nm and grain size of approximately 10nm were observed in the as-grown film. Figure 2.4(a) shows the surface image and conduction mapping of the film over a 2×2 μm^2 area. The average surface roughness of the relatively smooth poly-ZnO film is about 1.5 nm as shown in Fig. 2.4(b). The film surface showed large crystals with good correlation between the topography and electrical mapping at a bias of 5V. This confirms good conduction through the thin film without the formation of 2D island growth.



(a)



(b)

Figure 2.4 (a) AFM surface image and conduction mapping and (b) surface roughness of poly-ZnO grown on SiO_2/Si (100) substrates.

2.3.2 Optical Characterization

When light with sufficient energy is incident onto a sample, absorbed photons impart excess energy to electrons within the material. This photo excitation causes electrons within the material to move into permissible excited states. These excited electrons eventually relax to their ground state. With radiative and nonradiative relaxation of the electrons, the emission of light called photoluminescence occurs. The most common radiative transition in semiconductors is between states in the conduction and valence bands. Hence, photoluminescence can be used to determine the band-gap. Thus, photoluminescence (PL) is the spontaneous emission of light from a material under optical excitation. PL spectroscopy is a nondestructive technique requiring very little sample manipulation that is used to optically characterize various material parameters. It is a selective and extremely sensitive probe of electronic states of a sample and is usually acquired at a temperature between 8K and 300K. This provides access to the energy level structure of a system. Features of the emission spectrum can be used to gauge surface quality and analysis of structural interfaces. Information gained from the PL peak position can be used to evaluate the band-edge emission, peak linewidth to spatial uniformity of the band-gap throughout the material, and peak intensity gives a measure of the radiative and nonradiative mechanisms present at material surfaces and interfaces.

The photoluminescence characterization in this work was performed using a Kimmon He-Cd (λ = 325nm) continuous wave laser source with a maximum output of 35mW. The spontaneous emission from the sample after being excited with the cw-laser is then collected and focused on a SPEX 500M spectrometer input slit. Inside the spectrometer, photoluminescence with different spectral components is separated at

different angles by an optical grating. Finally, the output slit of the spectrometer is connected to a photo-diode so that the luminescence signal intensities at different wavelengths can be recorded as the optical grating scans through a designated angular range. A lock-in amplifier detects and amplifies the small AC signal from the spectrometer. It then uses a phase sensitive detection technique at a specific reference frequency and phase to reject noise signals other than the reference frequency. A spinning chopper is used to synchronize the light from the continuous laser source with the lock-in amplifier. Background noise associated with the detected signal is therefore attenuated using this standard lock-in technique resulting in an optimized signal-to-noise ratio.

Energy band gap of ZnO (MgZnO will be discussed in Chapter 5) are thus determined by corresponding PL peaks. PL spectrum measured at low temperature for PLD ZnO material grown at 600°C is shown in Figure 2.5. Radiative transitions in semiconductors also involve localized defect levels. Assignment of the emission peak at 3.36 eV is attributed to the neutral donor-bound exciton ($D^{o}X$). As mentioned previously, $D^{o}X$ energy is 60meV in ZnO thus the actual band-gap is 3.42eV at T=10K. The intensity of the green luminescence (GL) band, centered around 2.3 eV, is used as a measure of the deep-level defects (i.e. V_O and Zn_i) commonly associated with bulk and epitaxial ZnO.

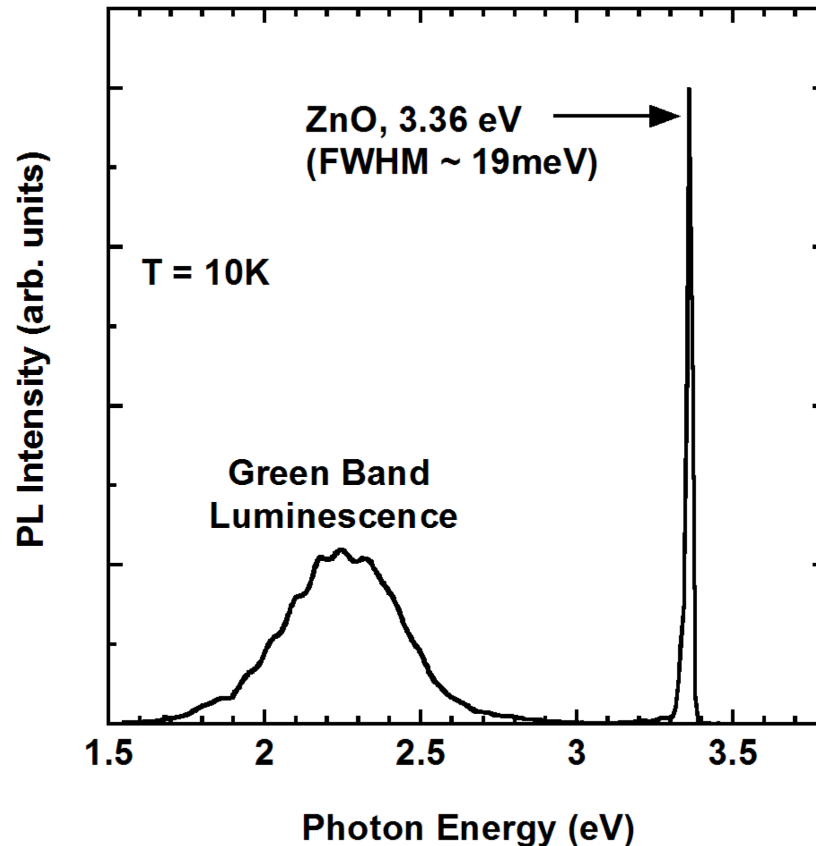


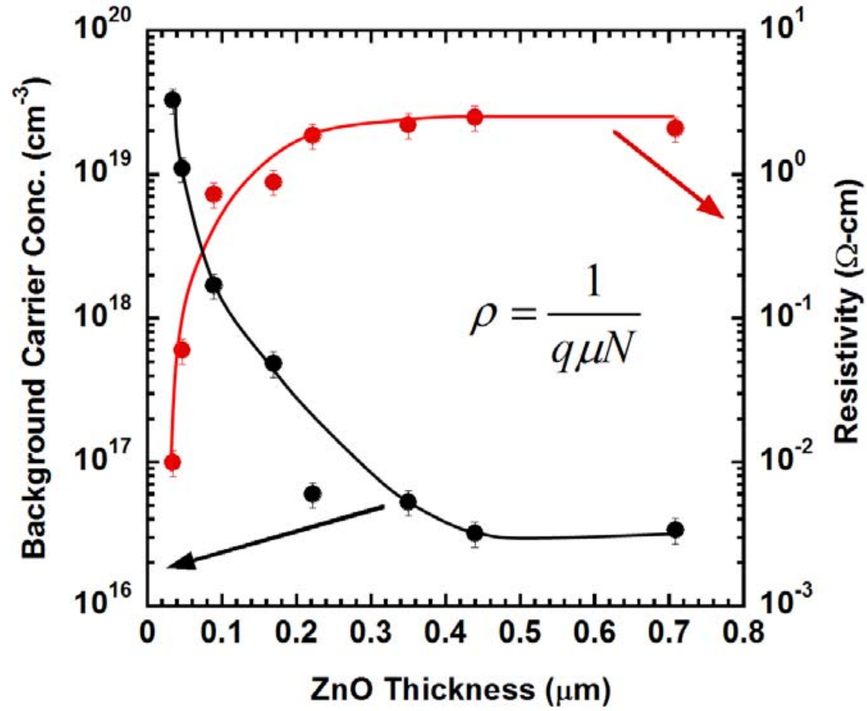
Figure 2.5 Photoluminescence spectra measured at low temperature for ZnO material grown at 600°C.

2.3.3 Electrical Characterization

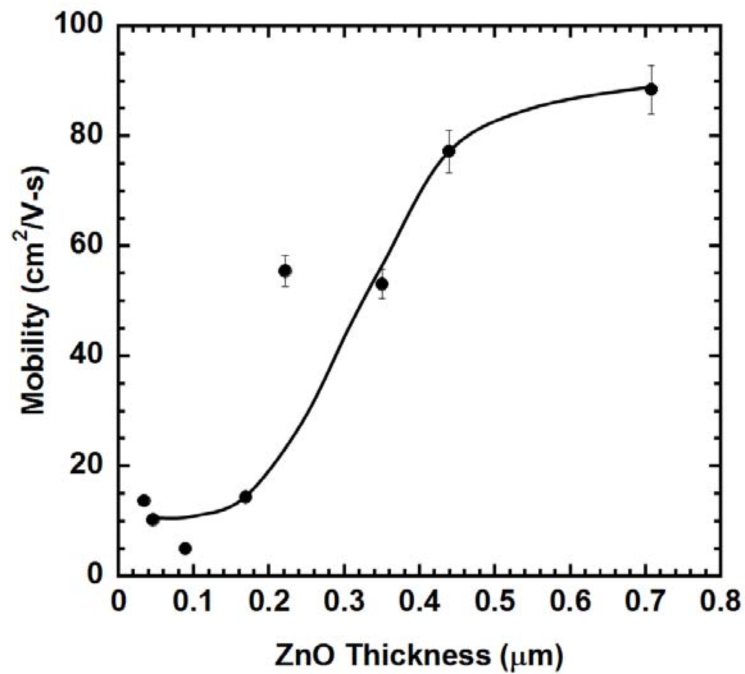
A result of considerable stress due to the lattice mismatch (~18%) between the deposited ZnO film and the Al_2O_3 substrate is an array of threading dislocations forming nanocrystalline grains separated by grain boundaries in the thin film. There is a high density of defects associated with the grain boundaries, which along with the point defects (V_O and Zn_i) cause an increase in the n-type background (undoped) concentration of polycrystalline ZnO. The grain boundaries also have a significant influence on electrical conductivity. Electrical conductivity parallel to the grain boundary is higher than the lateral conductivity. In practical application, carrier transport normal to the grain

boundaries is detrimental for high-performance transistors. Hence, post-annealing is used to decrease the dense number of grain boundaries thus improving the crystallinity of the ZnO thin film. Additionally, growth with low $p(O_2)$ has the largest number of oxygen vacancies, the electron concentration and conductivity is higher than ZnO at higher pressure. The stoichiometry improves with increasing oxygen supply, because the number of oxygen vacancies will decrease. With fewer oxygen vacancies, the resulting ZnO has a lower background concentration and higher resistivity.

It was found that the electrical properties of ZnO films on c-plane Al_2O_3 were dependent upon its thickness. Hall-effect measurements were used to characterize the films all grown under the same (i.e. temperature, pressure, laser fluence) conditions. The van der Pauw technique was used to determine the background carrier concentration (N_B), resistivity (ρ), and Hall mobility (μ) as a function of the ZnO thickness, as shown in Fig. 2.5 (a) & (b). Relaxation of stress in the ZnO film occurs with thicker films resulting in the increased crystallite grain size and fewer grain boundaries. Less the number of grain boundaries, the electrons experience less scattering and enhanced transport mobility. As will be shown in Chapter 3 and 4, ZnO TFTs are limited to channel thicknesses less than 60nm for current saturation due to channel "pinch-off". This presents a challenge because N_B increases for thinner films, likewise ρ decreases.



(a)



(b)

Figure 2.6 (a) The background concentration and resistivity and (b) carrier mobility of polycrystalline ZnO deposited on c-plane Al_2O_3 as a function of film thickness.

2.4 Conclusion

In conclusion, ZnO thin films can be grown by various physical deposition technologies. PLD offers the advantage of an economical experimental setup for growth of films at moderate substrate temperatures. Careful selection of the laser power density and appropriate beam profile of the excimer laser used to ablate pressed targets, along with manipulation of the PLD growth conditions (i.e. temperature, partial pressure, and gas flow rate), are analyzed to reduce particulate formation and 2D nucleation in favor of promoting unit-cell layer transport in ZnO thin films. A technique is developed for optimized growth of ZnO thin films to serve as active channel layers of a TFT based on these studies. The material study on ZnO material was characterized by XRD, AFM, PL, and Hall measurement. The studies provided valuable information concerning the structural, optical, and electrical properties of ZnO. From the electrical characterization, it was concluded that growth of thin films (30 – 50 nm) with background concentrations less than 10^{18} cm^{-3} for eventual fabrication of a thin-film transistor would be a challenge.

Chapter III

THE N-CHANNEL ZNO THIN FILM TRANSISTOR IN STATIC OPERATION

3.1 Introduction

As discussed in Chapter II, lower carrier concentrations are observed with increasing polycrystalline ZnO film thickness, resulting from the increase in the grain size [65]. However, ZnO TFT channel thicknesses are usually on the order of 40nm to ensure current saturation at low operating bias. This chapter provides qualitative details of the device structure and the basic theory of operation on which the TFT is based. Further, the simulated dependence of ZnO carrier concentration and channel layer thickness on TFT DC characteristics is discussed. Basic steps of TFT fabrication will be given in Chapter IV along with the device experimental DC characteristics.

The structure of TFTs differ from the conventional metal-oxide-semiconductor field-effect transistor (MOSFET) in so far as the typical n-channel MOSFET (NMOS) consist of two n+ regions diffused into a p-type substrate forming the source and drain contacts. Conversely for the n-channel TFT in the bottom-gate configuration, ohmic contacts with low specific contact resistance on the undoped ZnO semiconductor surface form the source and drain electrodes. This simplified structure of the n-channel TFT distinguishes the device from the NMOS and its normal mode of operation.

3.2 ZnO TFT Regions of Operation

A cross-sectional view and basic features of the ZnO TFT with an adjoining coordinate system is shown in Fig 3.1. The basic device dimensions are the channel length *L* in the *y*-direction, the channel width *W* in the *z*-direction, and the ZnO channel depth d_{ZnO} in the *x*-direction. TFTs are field-effect transistors which operate as majority carrier devices in the *accumulation* regime. In the device of Fig. 3.4, positive bias applied to the gate electrode with respect to the grounded source electrode induces an excess (or accumulation) of negative charge in the proximity of the ZnO-SiO_2 interface. These electrostatically induced electrons form a conducting channel and allows current to flow from the drain to the source. It is important to note that the source and drain contacts are ohmic with minimal resistance; furthermore unlike in a MOSFET, no depletion region forms between the source and drain contacts to isolate the conducting channel from the remaining ZnO surface. As a result, switching the TFT from its *off*-state (no conducting channel) to its *on*-state (conducting channel) is solely limited by the conductivity of the ZnO thin film. In principle, the absence of a depletion region suggests that the *threshold voltage* (V_{TH}), the minimum gate voltage required to induce a conducting channel, should be zero. However, a measurable V_{TH} is observed for TFTs and depends on the quality of the ZnO-SiO_2 interface. Initial electrostatic induction of electrons at low gate bias (sub-threshold regime) suffers from surface state trapping at the ZnO-SiO_2 interface. This has a detrimental effect on carrier transport along the ZnO channel layer and therefore negligibly small drain-to-source current flow. With further increase in gate voltage, the traps are eventually filled resulting in the formation of a conducting channel. The gate voltage at the onset of the conducting channel is defined as the turn-on voltage, V_{on}.

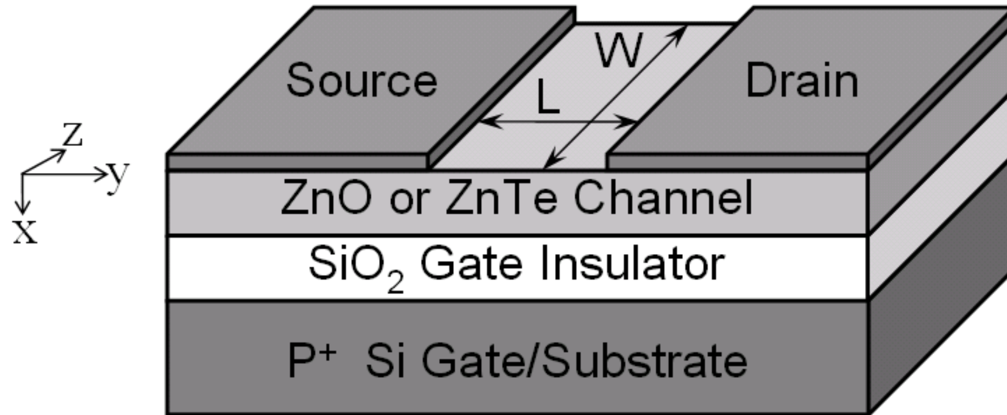


Figure 3.1 Cross-section of a typical ZnO bottom-gate TFT device.

Beyond this point, the channel becomes increasingly conducting in keeping with accumulative electron charge having increased carrier mobility. This carrier mobility dependence on gate bias will be discussed further in Chapter 4.

3.2.1 Depletion of Charge

When a negative bias is applied to the gate electrode, carriers in the n-type semiconductor are withdrawn and a depletion region forms at the gate-insulator surface. The extent of the depletion region is related to increasing negative gate bias. Thus, the depletion region widens as more electrons are withdrawn. The TFT is said to be in its *off*-state (no conducting channel). Fig 3.2 shows the schematic of a ZnO TFT operated in depletion. For wide band gap materials with overwhelming inherent n-type conduction such as ZnO, the bands are bent upward however the valence band is not closer to the Fermi level than the conduction band.

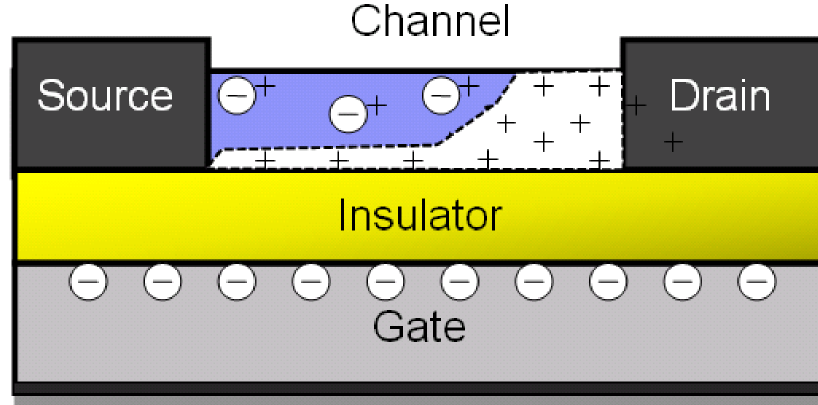


Figure 3.2 Schematic of ZnO TFT operation in depletion.

3.2.2 Accumulation of Charge

With a small positive drain bias, a negligibly small drain current will flow due to leakage currents and the conductivity of the thin film. Increasing the gate bias above zero ($V_{GS} > V_{DS} > 0$) results in the accumulation of charge at the ZnO-SiO_2 interface. The charge adjacent to the interface surface is now larger than that uniformly distributed throughout the remaining semiconductor volume and the thickness of this resulting surface accumulation layer is given by [66]

$$L_C = \frac{V_S}{E_S} \tag{3.1}$$

where V_S is the semiconductor surface potential and E_S the surface field. Fig. 3.3 shows the surface accumulation layer thickness as a function of V_{GS} for a ZnO TFT while varying carrier concentration in the semiconductor and use of different gate dielectric (SiO_2) thickness. The thickness of this layer is small on the on the order of 40Å and decreases with an increase of the electric field at the surface.

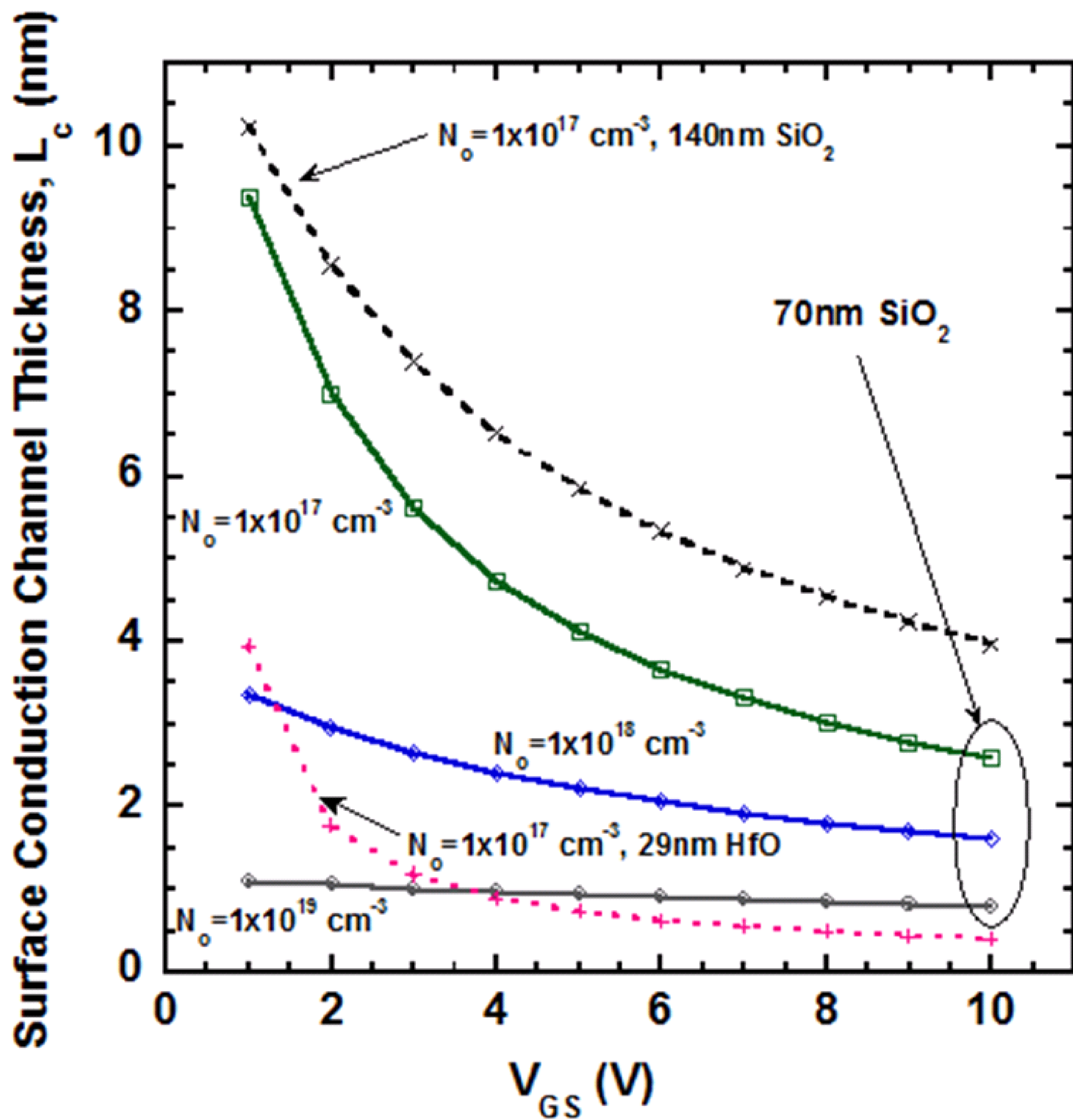


Figure 3.3 Surface accumulation layer thickness as a function of V_{GS} for a ZnO TFT with varying carrier concentration in the semiconductor, different gate dielectric (SiO_2) thickness, and a HfO gate dielectric.

A schematic of the ZnO TFT illustrating the accumulation of negative charge in the vicinity of the ZnO-SiO_2 interface is shown in Fig. 3.4. Hence, the device operates in the linear region and behaves like a voltage- controlled resistor with a small drain current. At some point along the channel where the drain bias equals the gate bias (V_{DS}=V_{GS}), a depletion zone (i.e. absent of free charge) begins to develop near the drain contact. Once the drain bias is increased above the gate bias (V_{DS} > V_{GS} > 0), the depletion zone width increases thus effectively reducing d_{ZnO}. The depletion zone eventually extends across the entire thickness of the ZnO layer near the drain contact resulting in the onset of pinch-off,

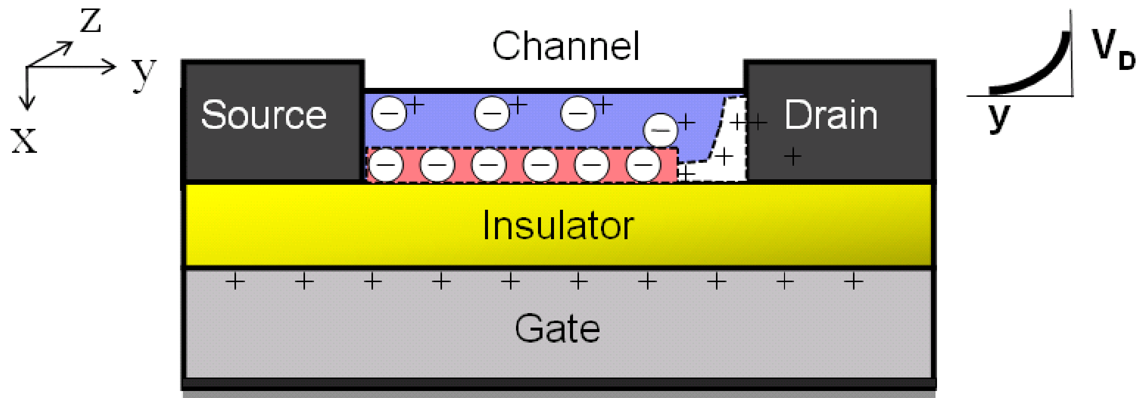


Figure 3.4 Schematic of a ZnO thin-film transistor illustrating the development of a depletion zone near the drain contact. For V_{DS} > V_{GS}, pinch-off of the entire channel thickness occurs near the drain.

and the drain current saturates. The depletion zone width, W_{depl}(y), at a distance *y* from the source is given by [67]

$$W_{depl}(y) = \frac{\varepsilon_{ZnO}}{C_{ins}}\left[\sqrt{1+\frac{2C_{ins}^2\left[V(y)-V_{GS}\right]}{qN_B\varepsilon_{ZnO}}}-1\right] \quad (3.2)$$

where ε_{ZnO} is the ZnO dielectric constant, C_{ins} is the capacitance of the gate dielectric, and V(y) is the drain voltage variation as a function of distance *y* along the semiconducting channel. Therefore, current saturation is determined by device geometry and material

properties. Fig. 3.5 gives the ZnO TFT maximum depletion zone width as a function of V_{DS} and V_{GS}. The figure suggests pinch-off for the entire thickness of the ZnO layer at a V_{GS}=10V and V_{DS}=15V for a ZnO TFT device with <40nm channel thickness (N_B=5x10^{17} cm^{-3}).

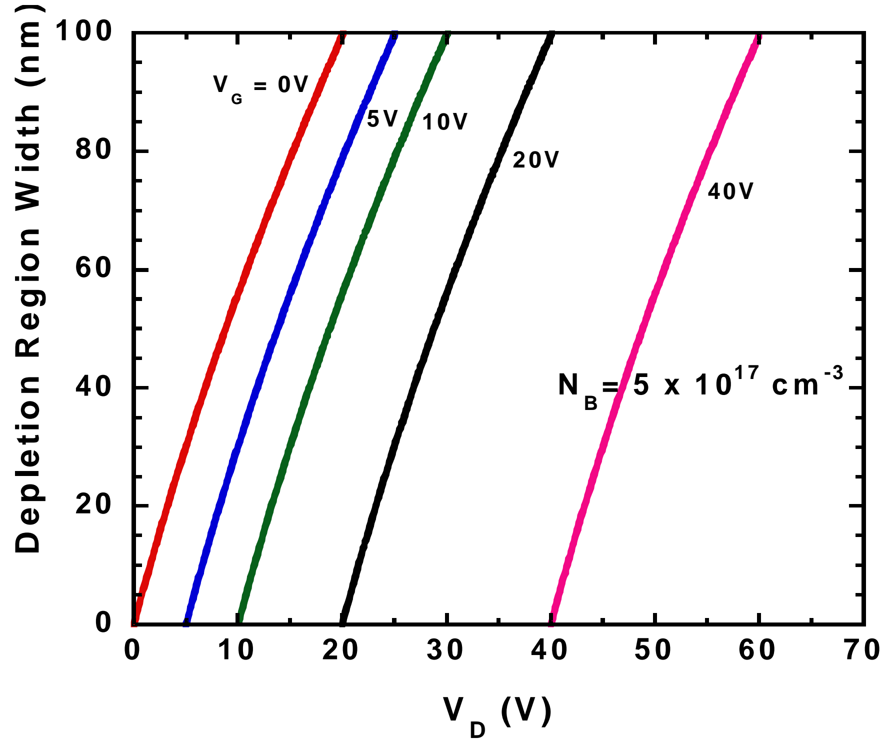


Figure 3.5 Depletion region width allowing TFT channel pinch-off as a function of V_{DS} and V_{GS} for a background concentration of N_B=5x10^{17}cm^{-3}.

Calculation of the device current-voltage characteristic consists of considering a differential drain voltage for an elemental section *dy* of the conducting channel, given by [68]

$$dV = \frac{I_D dy}{\mu W \left| Q_{acc}(y) + Q_{bulk} \right|} \tag{3.3}$$

where μ represents constant carrier mobility, $Q_{acc}(y)$ is the total accumulated charge per unit area induced at a position y along the channel, and Q_{bulk} is the bulk charge for n-type ZnO at equilibrium. Consistent with field-effect transistor operation, the drain voltage V_{DS} drop is a function of its position along the channel from (y = 0, $V(y)$ = 0) at the source to (y = L, $V(y)$ = V_{DS}) at the drain contact. At low drain bias, Q_{acc} is uniformly distributed over the entire channel and Q_{bulk} is a constant given by

$$Q_{bulk} = -qN_B d_{ZnO} \tag{3.4}$$

where q is the elemental charge with the sign of the majority carrier, N_B is the background concentration of ZnO, and d_{ZnO} is the thickness of the ZnO film. The total charge induced in the ZnO thin film forming the accumulation layer is given by

$$Q_{acc} = -C_{ins}\left|V_{GS} - V_{fb} - V(y)\right| \tag{3.5}$$

where V_{GS} is the gate-to-source voltage, V_{fb} is the flat-band voltage which accounts for the work-function difference between the ZnO material and the gate electrode, and V(y) is the drain voltage drop along the channel. Under ideal conditions, V_{fb} is considered to be negligible. Substituting Eq. (3.4) and (3.5) into Eq. (3.3) yield

$$I_D \int_0^L dy = \mu W \int_0^{V_D} \left[C_{ins}\left(V_{GS} - V(y)\right) + qN_B d_{ZnO}\right] dV \; . \tag{3.6}$$

The drain current as a function of the drain voltage at any point along the channel can now be obtained from Eq. (3.6). Drain current-voltage characteristics are derived for the linear and saturation regions of operation, as will be discussed in Chapter 4. It is worth noting that the expression for Q_{bulk} in Eq. (3.4) is no longer a constant value and now becomes

$$Q'_{bulk} = -qN_B\left(d_{ZnO} - W_{depl}(y)\right). \tag{3.7}$$

The depletion zone which forms near the drain contact will eventually cover the entire ZnO layer thickness near the drain contact; thus, the *pinched off* channel is now free of accumulated charge and the drain current saturates.

3.3 Two-Dimensional ZnO TFT Device Simulation

Numerical simulations of ZnO TFT DC characteristics provide an efficient means for complementing experimental investigations. The particular effects of physical parameters, such as channel thickness and carrier concentration, on the electrical behavior of TFTs cannot always be adequately modeled with one-dimensional analysis. In this thesis, two-dimensional simulations are used to better understand experimental results and further device development. Steady-state numerical simulations are performed using the two-dimensional device simulator Sentaurus Device [69], a commercial package by Synopsys, Inc. Because the simulation was originally configured for crystalline silicon devices, it is worth noting that the entire ZnO channel layer is assumed to be homogeneous. However, changes to the numerical settings to simulate the material ZnO allow for analysis of DC characteristics of the TFT based on this material. The simulated TFT device structure, illustrating contours of electron density in the channel region, shown in Fig. 3.6 consists of a 700Å SiO_2 gate insulator beneath a ZnO channel layer. The source-drain contact separation used is 10µm, and the bottom-gate contact is set to 14µm with a 2µm source/drain to gate overlap. Ideal ohmic contacts with low specific contact resistance are assumed for the source, drain, and gate electrodes. Parasitic resistance associated with the source and drain contacts is considered to have negligible influence on TFT characteristics in the long-channel device (W=100µm,

L=10μm) [70,71]. As a result, the TFT ON resistance in the linear regime ($V_{DS} < V_{GS}$) is given approximately by the channel resistance in the following expression:

$$R_{on} = \left.\frac{\partial V_{DS}}{\partial I_D}\right|_{V_{DS}\to 0}^{V_{GS}} = R_{ch} + R_S + R_D = R_{ch} + R_p \approx R_{ch} \tag{3.8}$$

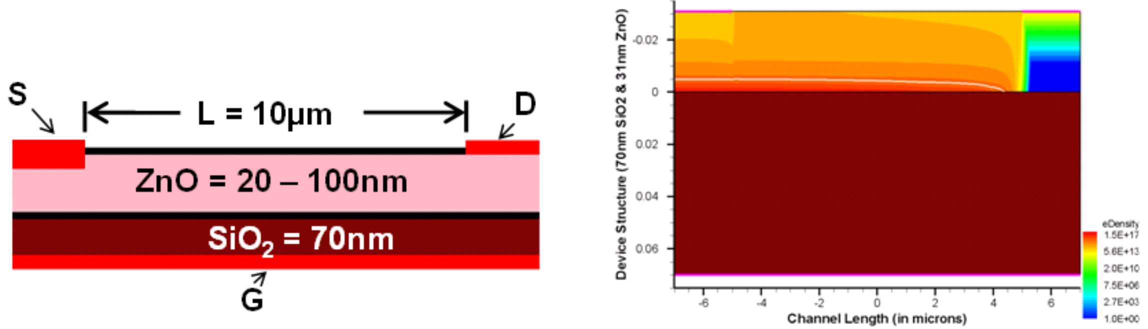


Figure 3.6 ZnO TFT device structure and example of electron density profile.

$$R_{ch} = \frac{L}{\mu C_{ins} W (V_{GS} - V_{TH})} \tag{3.9}$$

When $V_{DS} > V_{GS}$, a depletion zone forms at some point along the channel, replacing the channel accumulation in the first few nanometers near the ZnO-SiO_2 interface. In this region, free electrons are depleted and the channel consists only of the bulk charge $Q_0 = q\mu_n N_B$. The channel resistance now becomes a function of the depletion layer width and is given by

$$R_{ch} = \frac{L}{q\mu_n N_B W (d_{ZnO} - W_{depl}(y))} \tag{3.10}$$

where d_{ZnO} is the ZnO channel thickness and $W_{depl}(y)$ is the depletion layer width at y.

A uniform ZnO background carrier concentration profile is defined for the entire channel layer. Inclusions of donor traps were exponentially distributed at the ZnO-SiO_2 interface with the following expression:

$$N_T = N_0 e^{-\left|\frac{E-E_0}{E_s}\right|} \tag{3.11}$$

where N_0 is the peak trap concentration originating at the interface, E_0 is the central energy of the trap from the conduction band, and E_s is the width of the trap distribution. In the simulation, the trap distribution was varied until there was good agreement between the numerical model and experimental output data. The resulting trap density was set at $N_0=10^{13}cm^{-2}$, the exponential trap distribution was centered at the conduction band $E_0=0$, and the trap width was $E_s=35meV$ [72].

3.3.1 Effect of the ZnO Channel Thickness

The on-current and drain current saturation depends critically on the channel layer thickness in the TFT structure shown in Fig. 3.6. Increasing the channel layer thickness leads to higher on-current. One of the justifications for this is that the channel resistance decreases with increasing channel layer thickness. As a result, the conduction current flowing from the drain through the channel to the source experiences less opposition. As shown in Fig. 3.7, simulated characteristics of higher on-current with increasing channel layer thickness comes at the expense of degraded drain current saturation. This occurs as the variable thickness of the channel layer $d_{ZnO} - W_{depl}(y)$ between source and drain is excessively thick such that "pinch off" requires much higher drain voltage. In agreement with Fig. 3.5, current saturation is not observed for channel layer thicknesses >40nm with a background concentration $N_B=5x10^{17}cm^{-3}$ and operating voltages of $V_{GS}=10V$ and

V_{DS}=15V. Fig. 3.8(a) and (b) show the results of a 2D simulation of a ZnO TFT where the channel region has contour lines indicating the electron density along the ZnO channel layer. The depletion region for the 20nm device (Fig. 3.8a) is depleted of free carriers and its width pinches off the entire channel. Likewise, the depletion region for the 100nm device (Fig. 3.8b) is depleted of free carriers, but its width is not sufficient enough to pinch off the channel. For a ZnO background concentration of $N_B=5x10^{17}cm^{-3}$ and low operating voltages (V_{GS}=10V and V_{DS}=15V), channel pinch-off (current saturation) requires ZnO films $\leq$ 40nm.

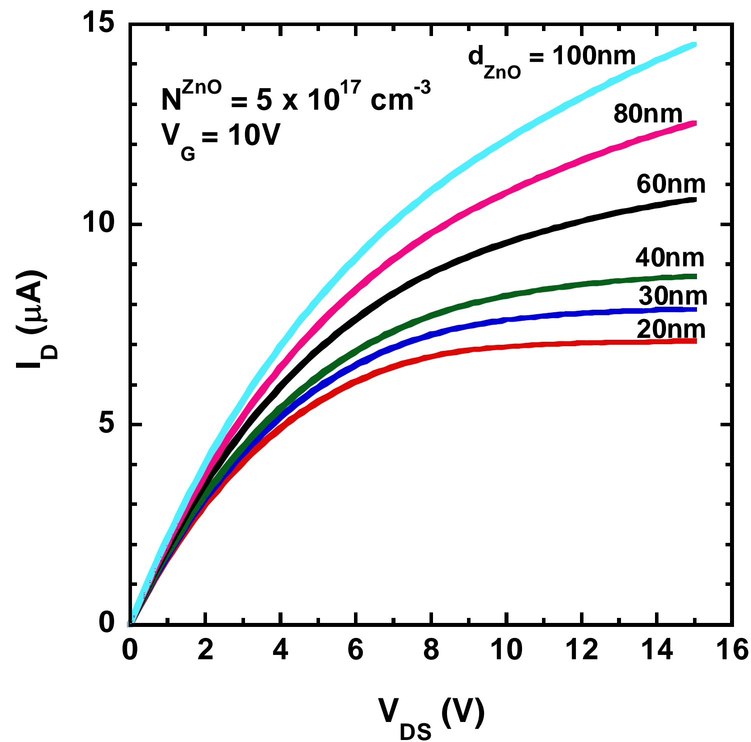
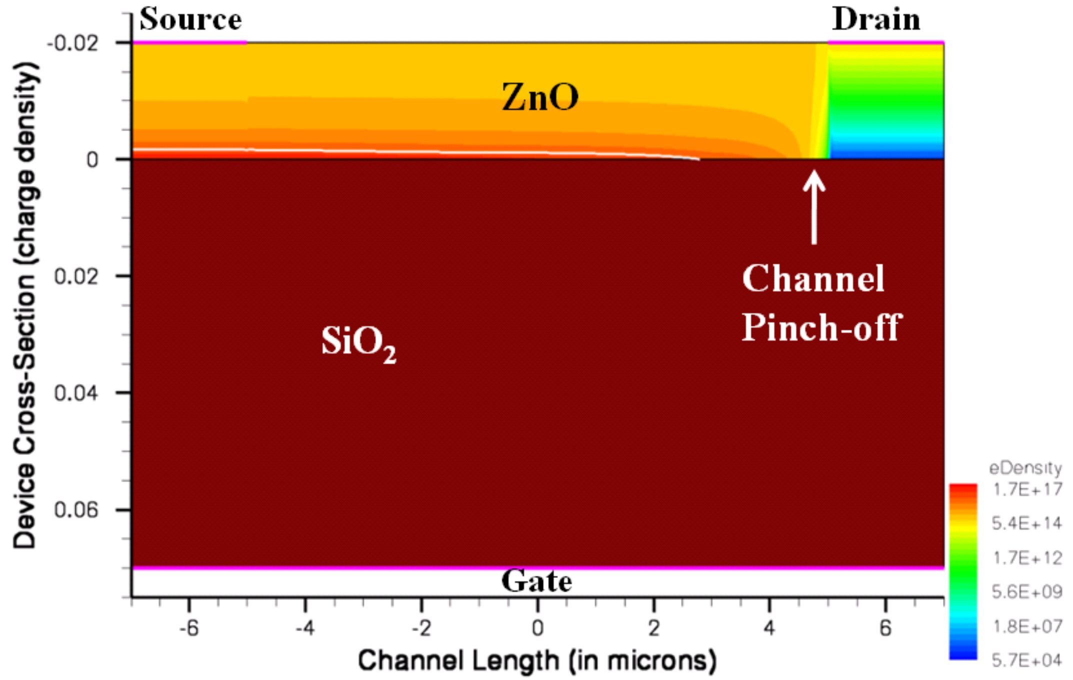
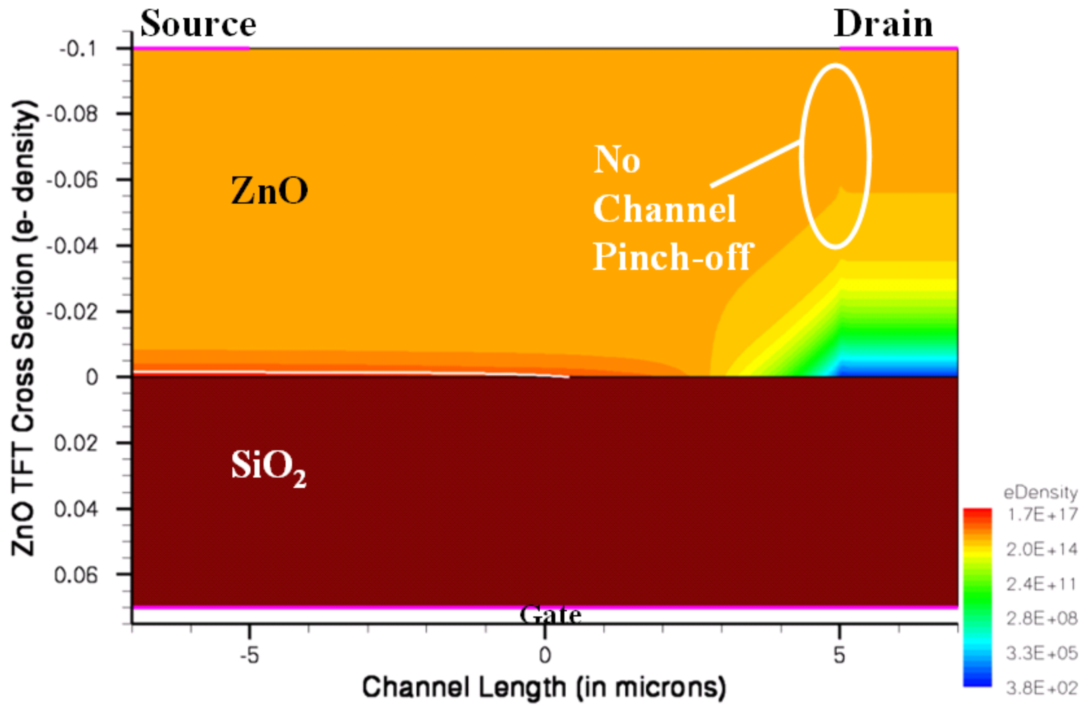


Figure 3.7 Simulated characteristics of the ZnO TFT in Figure 3.6 for different channel layer thickness.



(a)



(b)

Figure 3.8 Distribution of electron concentration contour lines for (a) 20nm and (b) 100nm ZnO TFTs.

3.3.2 ZnO Carrier Concentration Dependence

Figure 3.9 shows the dependence of the carrier density of undoped n-type ZnO thin film on the on-current and current saturation for a TFT with a 30nm thick channel layer. The on-current increases for high carrier concentrations, though current saturation would only occur at much higher drain operating voltage, for a given gate voltage. Even though a combination of carrier transport mechanisms (i.e. grain boundary scattering) influence the enhanced on-current, higher carrier concentrations providing more free carriers even after ZnO-SiO_2 interface trap filling is thought to be the primary mechanism. As shown, clear channel pinch-off is observed for $N_B \leq 7x10^{17}cm^{-3}$ under low voltage operating conditions. The effect of the carrier concentration on the depletion layer that forms near the drain contact was previously explained and is illustrated with the 2D simulation in Fig. 3.10(a) and (b).

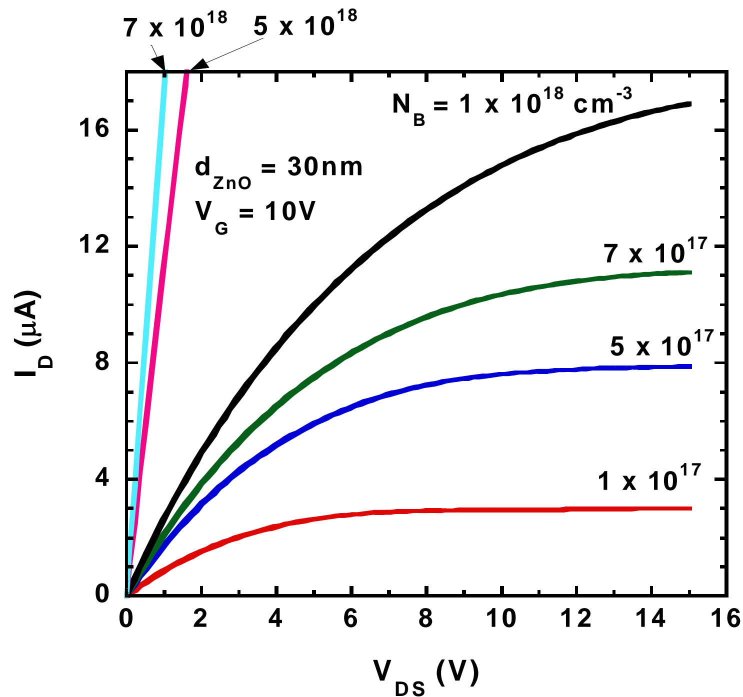
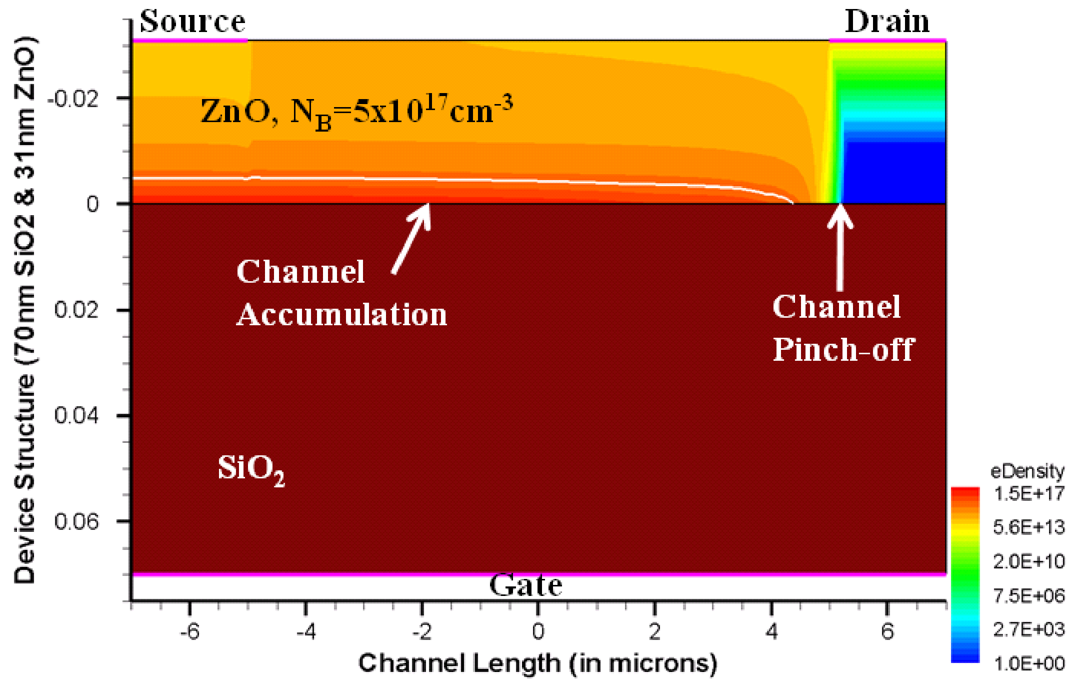
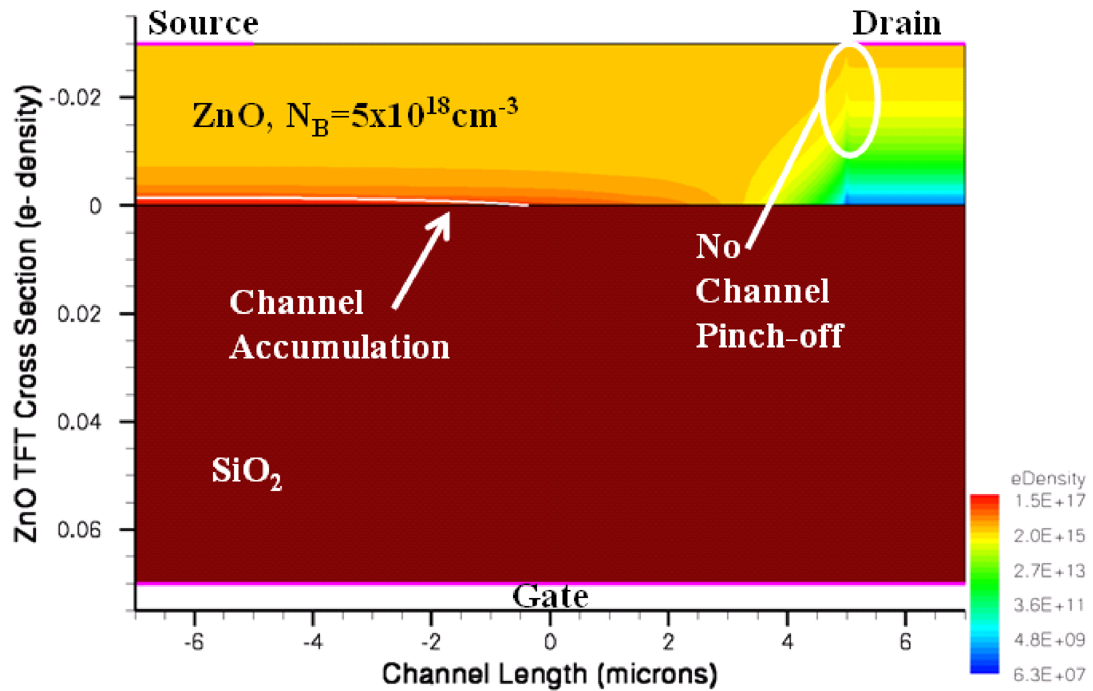


Figure 3.9 Simulated characteristics of the ZnO TFT in Figure 3.6 for different background carrier concentration.



(a)



(b)

Figure 3.10 Distribution of electron concentration contour lines for 30nm ZnO TFT with (a) $N_B = 5x10^{17}cm^{-3}$ and (b) $N_B = 1x10^{18}$ cm^{-3}. Pinch-off (current saturation) observed for lower carrier concentration.

The dependence of carrier concentration on the off-state leakage current is also a major requirement for the application of ZnO TFTs. Along with high on-current, low leakage current is needed for good selection of the on/off ratio. When V_{GS}=0V, a general form for the TFT off-state leakage current (I_{off}) with respect to the ZnO thickness and carrier concentration of the channel layer is given by

$$I_{off} = \frac{\sigma W d_{ZnO}}{L} V_{DS} \tag{3.12}$$

where σ is the electrical conductivity. Off-state I_D-V_{DS} curves are shown in Fig. 3.11 for different carrier concentrations and channel layer thickness. At high carrier concentration, I_{off} is purely ohmic and scales with thickness; whereas for lower concentrations, I_{off} decreases with decreasing thickness due to depletion effects. This is illustrated in Figure 3.12(a) and (b) for carrier concentrations of $5x10^{17}cm^{-3}$ and $5x10^{18}cm^{-3}$, respectively.

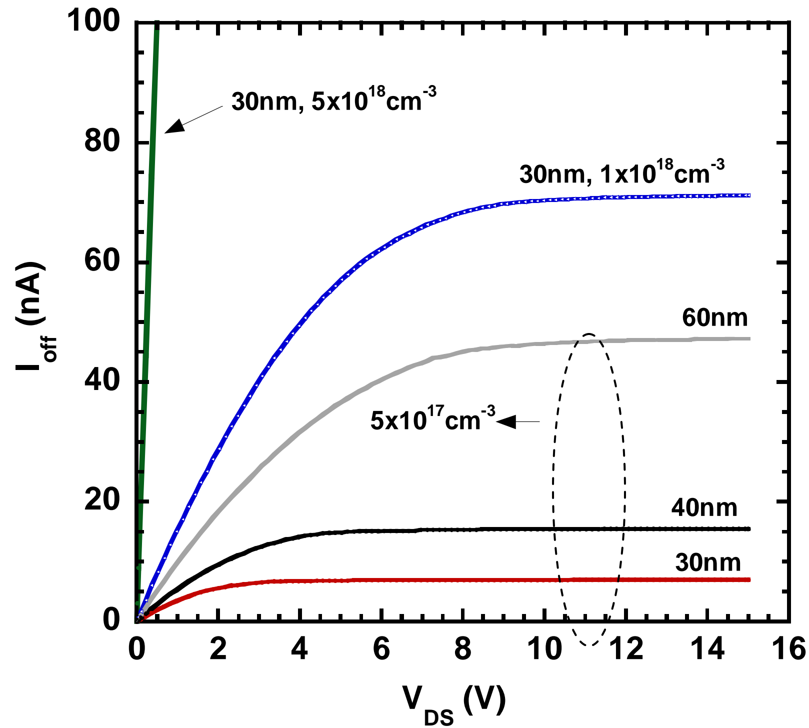
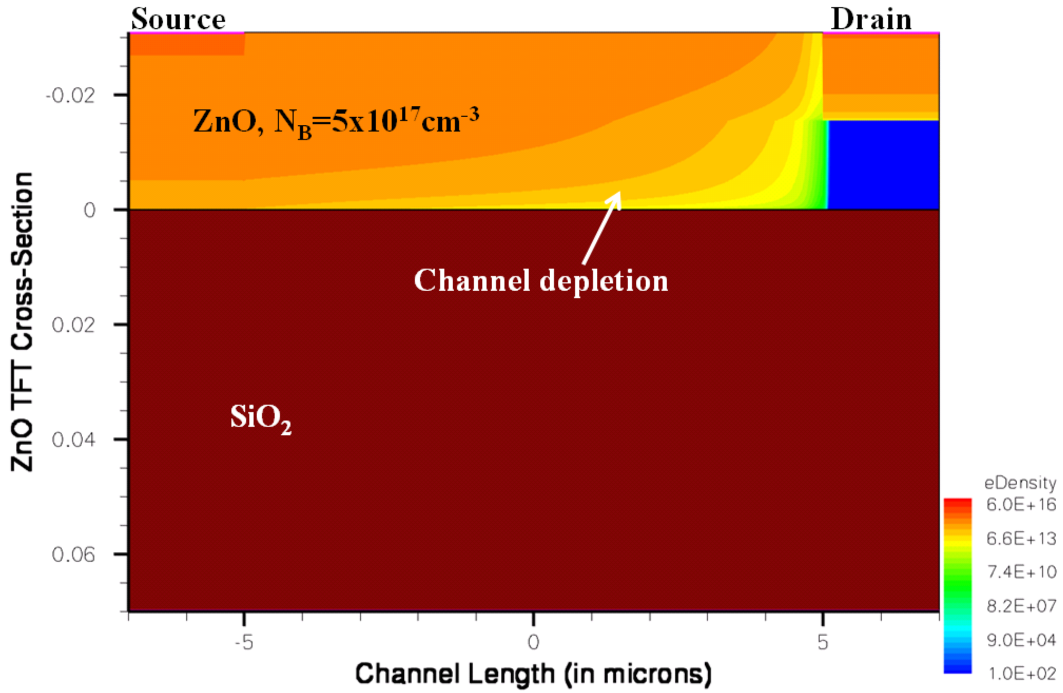
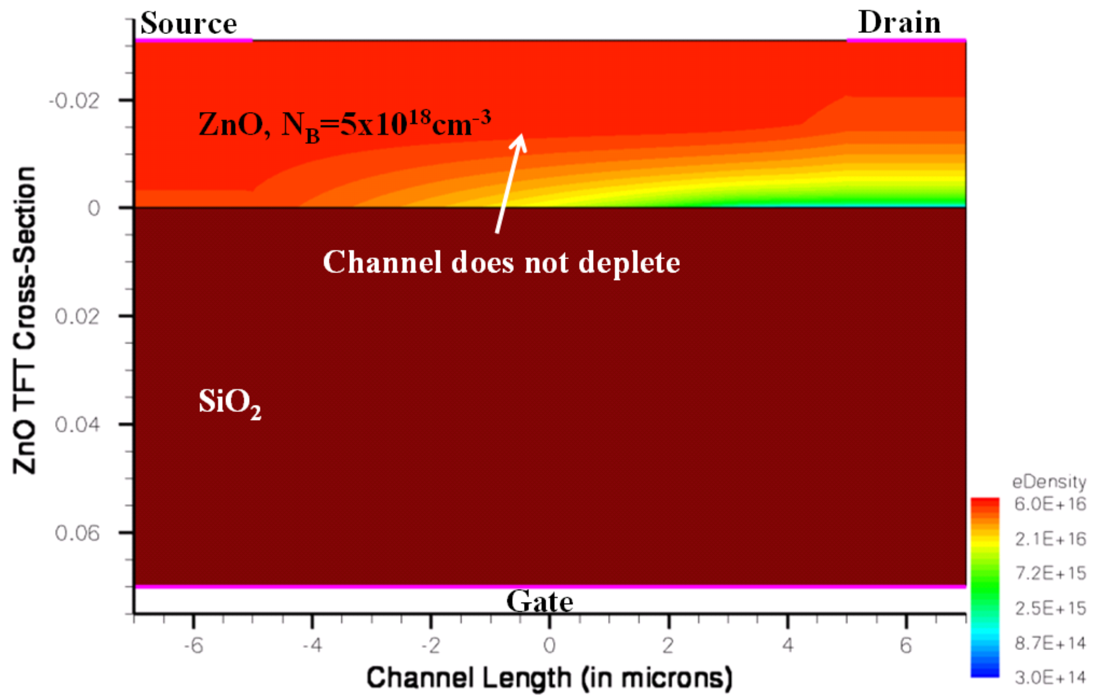


Figure 3.11 Simulated I_{off}-V_{DS} characteristics of the ZnO TFTs for different background carrier concentrations and ZnO thickness.



(a)



(b)

Figure 3.12 Distribution of the electron density in the off-state for a (a) $N_B = 5x10^{17}cm^{-3}$ and (b) $N_B = 5x10^{18}cm^{-3}$ ZnO TFT with a 31nm thick channel.

3.4 Conclusion

In summary, a perspective view and qualitative discussion of TFT operation distinguishing accumulation or depletion of carriers with application of gate voltage were discussed. Additionally, 2-D simulation models were used to provide an efficient way of investigating the effect of physical parameters on device characteristics, to be experimentally presented in Chapter 4. The "on" current and drain current saturation depends critically on background carrier concentration arising from ZnO material defects and the geometry of the ZnO channel. This chapter introduces a two-dimensional model of the TFT device illustrating the accumulation of electron charge at the ZnO-SiO_2 interface and the creation of the depletion layer near the drain contact. The on-current and off-current increases with channel thickness and carrier concentration at the expense of current saturation. This presents a trade-off for the particular device application. In Chapter 5, the 2-D device simulations presented in this chapter are used to model a buried-channel ZnO/MgZnO heterostructure TFT.

Chapter IV

FABRICATION AND DC CHARACTERISTICS OF ZNO TFT DEVICE

4.1 Introduction

This chapter discusses the fabrication of the ZnO TFT and experimental results of electrical characterization under static operation. The "on" current and drain current saturation depend critically on background carrier concentration arising from ZnO material defects and the geometry of the ZnO channel. Hence, the experimental dependence of ZnO material properties and channel thickness will be reported. Alternative analytical approaches for mobility dependence on gate bias and power-law extraction of threshold voltage better characterize the non-idealities associated with polycrystalline TFTs.

4.2 ZnO TFT Fabrication

The polycrystalline ZnO films used to fabricate bottom-gate TFTs were deposited on $1cm^2$ thermally grown SiO_2/p-Si (100) substrates by pulsed laser deposition (PLD). The p-type Si substrate is degenerately doped to serve as the gate electrode, and the SiO_2 layer serving as the gate insulator was approximately 700Å thick. SiO_2 has the advantage of being a stable, reproducible gate dielectric which allows for focus specifically on the ZnO channel characteristics. The ZnO films, with different thicknesses, were grown at a

substrate temperature of 600°C and varying partial pressure, from 10mTorr to 50mTorr. A KrF excimer laser operated at 248nm was used to ablate a commercial ZnO target. The laser repetition rate and pulse energy density were 6Hz and 2 J-cm^{-2}, respectively.

The success of the TFT device depends on the realization of high-quality ohmic contacts. The source and drain ohmic contacts are defined by conventional photolithography and e-beam evaporation metallization of Ti(300Å)/Au(700Å). Previous reports on the specific contact resistance of Ti/Au ohmic contacts to undoped ZnO are in the range of 10^{-4} to 10^{-5} Ω cm^2 [73,74]. In the next fabrication step, isolation of the devices is performed with photolithography patterning and a buffered hydrofluoric acid (BHF) etch. In the final processing step, patterning and e-beam evaporation of Ni(500Å)/Au(1000Å) gate metallization formed good ohmic contacts to the p-type silicon. Fig. 4.1(a) and (b) show a scanning electron micrograph and cross-section of the ZnO TFT.

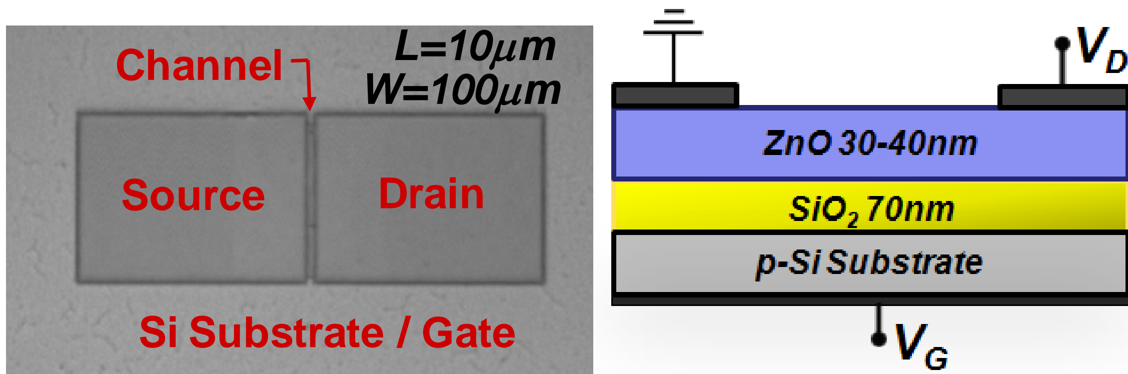


Figure 4.1 (a) Top view of a scanning electron micrograph and (b) cross-sectional view of a L=10μm (W/L = 10:1) ZnO TFT.

4.3 ZnO TFT Electrical Characteristics

Analysis of the current-voltage (I-V) characteristics for a TFT is in effect similar to those for conventional crystalline MOSFETs [67]. The following assumptions are

made in order to model the I-V characteristics: (1) the effective channel mobility is constant; (2) the source and drain ohmic contacts to ZnO have negligible contact resistance; (3) the flat-band voltage, V_{fb}, is taken to be much smaller than the threshold voltage, V_{th}, and thus negligible; and (4) the charge concentration is uniformly distributed throughout the thin-film. Another implied assumption is that the thickness of the thin ZnO semiconductor layer, d_{ZnO}, is much less than the channel length, L. This condition is consistent with the gradual-channel (long channel) approximation where the transverse electric field, $E_{\perp} \approx V_{GS}/d_{ZnO}$, is much larger than the electric field along the channel, $E_{\parallel} \approx V_{DS}/L$.

An analytical solution for the drain current expression in Eq. 3.4 will now be used to derive basic characteristics of TFT operation in the linear and saturation regions. When a sufficient bias is applied to the gate, a conducting channel forms between the source and drain electrodes. For a small V_{DS}, the increase in I_D is linearly proportional to V_{DS} for a given V_{GS} (the linear region). Thus, the low conductivity channel is analogous to a constant resistance and the drain current is expressed as

$$I_D = \frac{W}{2L}\mu_{eff}C_{ins}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{4.1}$$

where W is the channel width, L is the channel length, C_{ins} is the capacitance per unit area of the gate insulator, V_{TH} is the threshold voltage, and μ_{eff} is the field-effect mobility. For the condition when $V_{DS} \geq V_{GS}-V_{TH}$, the conducting channel is in saturation (pinch-off) and the region near the drain contact is depleted of free carriers. The drain current, I_D, now increases independently of the drain bias, V_{DS}.

$$I_D = \frac{W}{2L}\mu_{sat}C_{ins}(V_{GS} - V_{TH})^2 \tag{4.2}$$

Measured current-voltage, I_D-V_{DS}, output characteristics of a ZnO TFT with the linear and saturation regions indicated for various V_{GS} are shown in Fig. 4.2. The transfer

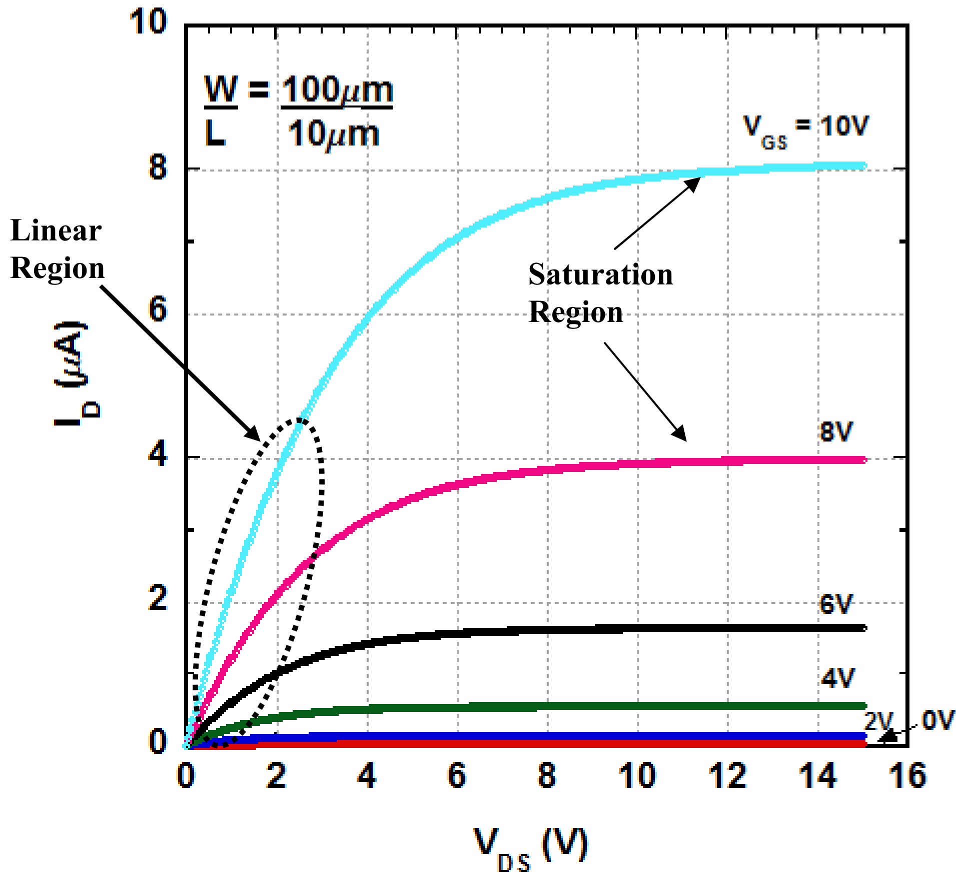


Figure 4.2 Measured current-voltage, I_D-V_{DS}, characteristics of a ZnO TFT for a 30nm thick channel.

characteristic, I_D-V_{GS} and $\sqrt{I_D}$ -V_{GS}, shown in Fig. (4.3) are a measure of the saturated drain current as a function of gate voltage for a sufficiently high V_{DS} value. Extrapolating the $\sqrt{I_D}$ as a function of V_{GS} curve down to the x-intercept indicates the threshold voltage, V_{TH}.

The threshold voltage extracted in Fig. (4.3) using the general square-law model discussed thus far introduces a degree of ambiguity. Recalling that for a

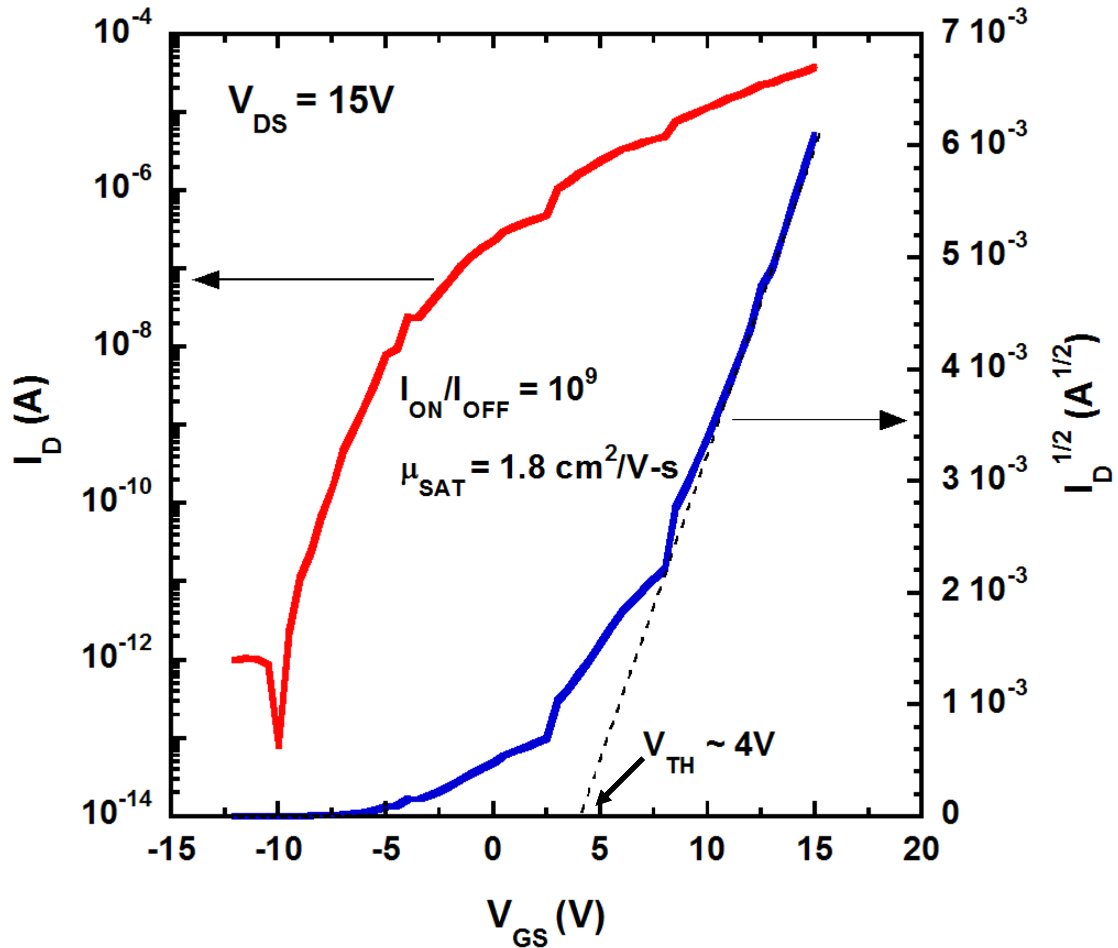


Figure 4.3 Measured transfer characteristics, I_D-V_{GS} and $|I_D|^{1/2}$-V_{GS}, of a ZnO TFT with 31nm channel thickness.

conventional MOSFET at low doping levels, V_{TH} in principle marks the onset of an inversion layer. Thus, it indicates the “threshold” where the MOSFET transitions from the *off*-state to the *on*-state. However as observed for the TFT, there is significant current flow for V_{GS} less than zero. To address this uncertainty, a turn-on voltage, V_{on}, identified

at approximately -10V is introduced. Using power-law dependence with gate bias, extraction of the threshold voltage ($V_{on} \approx V_{TH}$) will be discussed and applied to a ZnO TFT in Section (4.4.2).

According to Eq. (4.2), the saturation mobility is derived from the slope of the $\sqrt{I_D}$ -V_{GS} curve.

$$\text{slope} = \frac{\Delta\sqrt{I_D}}{\Delta V_{GS}} = \sqrt{\frac{W}{2L}\mu_{sat} C_{ins}} \tag{4.3}$$

From the measured characteristic (Fig. 4.3), a saturation mobility of μ_{SAT} = 1.8 cm^2/V s and threshold voltage of V_{TH} = 4V is obtained. A significant current flows at V_{GS}=0 suggesting that the TFT operates as a normally-on *n*-channel device. Further explanation on the extraction of the TFTs field-effect mobility and threshold voltage is given in Section (4.4.1) and (4.4.2). While improvement of TFT field-effect mobility has been central to most efforts to enhance device performance, the utility of ZnO TFTs also depends on current ON/OFF ratios. Both, the ON current and the OFF current, are directly dependent on the device geometry and material quality. Additionally, practical use of TFTs for pixel switching requires current ON/OFF ratios greater than 10^6. The measured characteristic of the ZnO TFT in Fig. 4.3 shows an I_{ON}/I_{OFF} = 10^9 and had a low gate leakage current, I_G=10^{-11} A.

4.3.1 Influence of Active Channel Thickness

The effect of the channel layer thickness on the electrical characteristics of ZnO TFTs was simulated in Sec. 3.3.1. In this section, the experimental dependence of the field-effect mobility, drive current, and on-to-off current ratio as a function of active

channel layer thickness, d_{ZnO}, is discussed. All of the active channel layers were deposited under similar growth conditions. It is expected from Fig. 2.6 that the carrier concentration will decrease and the mobility will increase due to less carrier scattering for increasing d_{ZnO}. This was indeed confirmed by the I_D-V_{DS} curves (V_{GS}=8V) in Fig. 4.4 for d_{ZnO} from 20 to 60nm. Current saturation of the 20-nm TFT is a direct manifestation of channel pinch-off, implying that the entire channel thickness is depleted of free electrons near the drain contact. The current saturation for the thinner channel comes, however, at the expense of lower drive current. This is related to the

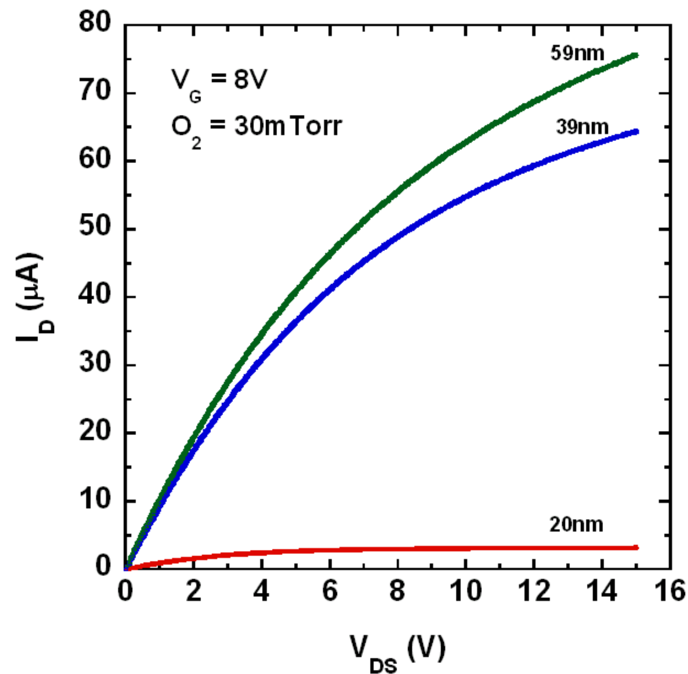


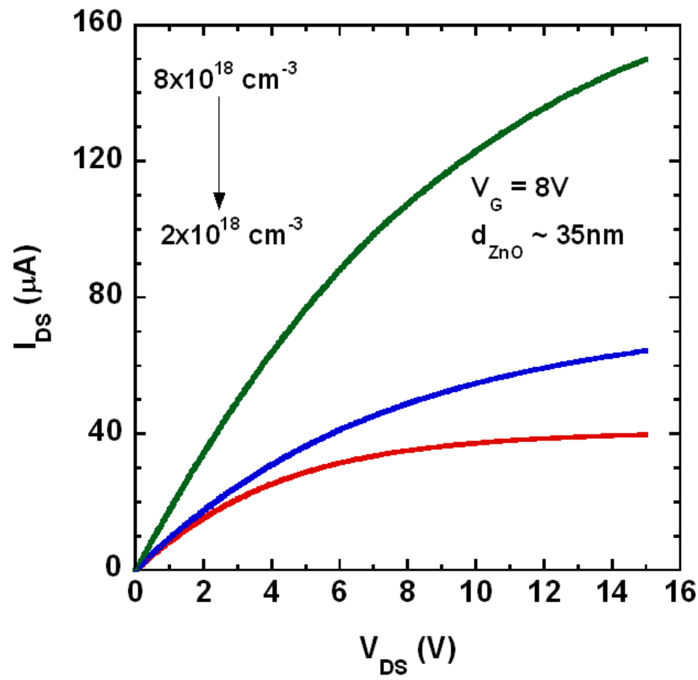
Figure 4.4 Output characteristics of ZnO TFTs as a function of active channel thickness deposited under similar growth conditions.

increase in the channel resistance with decreasing channel thickness (Eq. 3.3). From the transfer characteristics, the field-effect mobility of the 20, 39, and 59nm devices were estimated to be 2.0, 3.0, and 3.7-cm^2/V-s, respectively. Moreover, I_{on}/I_{off} increased from 3

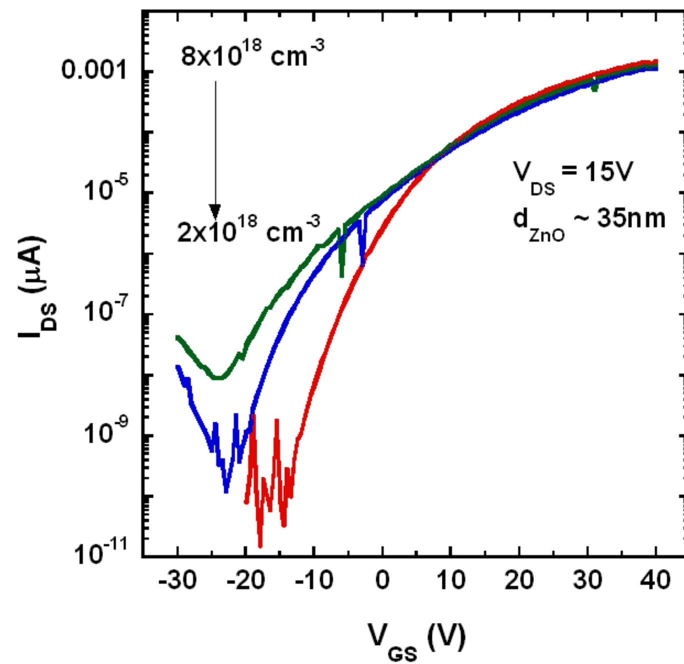
x 10^4 to 3 x 10^6 for thicker channels. The results are consistent with less scattering due to increased grain size for increasing ZnO thickness.

4.3.2 Influence of Carrier Concentration

The performance and device characteristics of ZnO TFTs with varying carrier concentration were investigated. A similar trend of the channel resistance with varying channel thickness is found for the influence of the background carrier concentration of the active thin-film channel. According to the discussion in Sec. 2.3.3, the crystal quality of the ZnO film improves as the film thickness increases. The relaxation of the stress in the thicker films paves the way for decreasing defects causing a decrease in the carrier concentration. Resistivity increases with decreasing carrier concentration, suggesting the dependence of TFT characteristics on intrinsic ZnO properties. Fig. 4.5(a) show that the ZnO TFTs with similar thickness exhibit typical field-effect characteristics with higher drive current for increasing carrier concentration. Carrier concentration was examined by Hall measurement of co-deposited thin films on sapphire substrates. Higher off current, reduced on-to-off current ratio, and decreased mobility are observed for larger background carrier concentrations (Fig. 4.5(b)).



(a)



(b)

Figure 4.5 Output characteristics of ZnO TFTs as a function of carrier concentration deposited under similar conditions.

4.4 Non-idealities of Polycrystalline TFTs

Theoretical derivation and calculation of drain current versus drain and gate voltage characteristics for TFTs are commonly obtained using the gradual-channel approximation, discussed in the previous section. Because conduction takes place in a surface layer within 40Å proximity of the SiO_2/ZnO interface, it is expected that TFT characteristics will be influenced by trapping at surface states. The influence of these surface states may vary along the channel and cause detrimental effect on the field-effect mobility. It is also thought to introduce ambiguity with respect to extraction of the threshold voltage, and its distinction from the turn-on voltage. In this section, non-idealities associated with polycrystalline TFTs are discussed and expressions for TFT characteristics derived based on approaches given by Hoffman and Ortiz-Conde for the channel mobility and threshold voltage, respectively [75,76].

4.4.1 Mobility Dependence on Gate Bias

The field-effect mobility, μ_{FE}, is a performance measure which is directly proportional to the operating speed of a TFT. It quantifies the transit time for an electron to cross the ZnO channel region from the ohmic source contact to the drain contact. The transit time, τ, is given by

$$\tau = \frac{L^2}{\mu_{FE} \times V_{DS}} \tag{4.4}$$

where L is the channel length, μ_{FE} is the field-effect mobility, and V_{DS} is the drain-to-source voltage. Therefore, μ_{FE} describes the TFT's "switching time" from the ON-state to the OFF-state and, as expressed in Eq. (4.1) and Eq. (4.2), when increased leads to higher

drive currents. With a positive external bias applied to the gate electrode, mobility associated with initial electron charge injection from the source contact in the polycrystalline ZnO channel suffers predominately from grain boundary scattering and ZnO-SiO_2 interface trapping [72]. Increasing the positive gate voltage to higher values increases the accumulation of electron charge in the channel region, specifically at the ZnO-SiO_2 interface. This additional charge essentially suppresses the detrimental carrier transport mechanisms owing to free carrier "screening" of scattering charges and filling of trap states; consequently, further induced charge is free to drift, in the process, experiencing increased mobility. The charge screening effect for polycrystalline material is illustrated in Fig. 4.6.

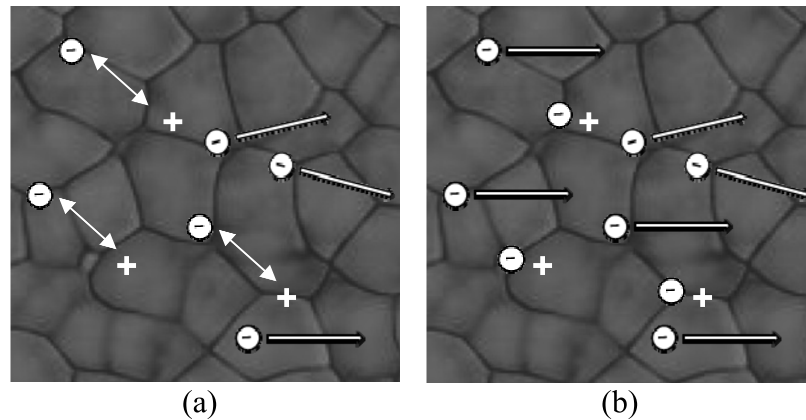


Figure 4.6 Effect of carrier transport in the ZnO TFT channel region (a) by scattering and trapping mechanisms and (b) "screened" fixed charge from polycrystalline grain boundaries for higher channel charge [64].

This mobility dependence on gate bias is in direct contradiction to the constant μ_{FE} commonly expressed for field-effect devices. R. L. Hoffman has developed methodology for average mobility, μ_{avg}, and incremental mobility, μ_{inc}, extraction based on basic understanding of device operation [75]. This method of analysis is used to characterize the channel mobility of the TFT devices in this thesis. There is, however, an

intentional rationale for labeling the two channel mobilities as μ_{avg} and μ_{inc}. Since the transverse electric field at each point in the conducting channel depends on the gate bias, one should expect that analytical mobility expressions related to charge transport will be a function of gate bias.

In order to characterize the gate-dependent channel mobility of a TFT, a set of transfer curves measured for V_{DS} ranging from 10mV to 15V are presented in Fig. 4.7. At high gate bias the 5, 10, and 15V curves are essentially overlaid while those curves less than 1V are separated by a decade in current. This distinction in the separation of the transfer curves allows for determination of the transition from the linear region to the saturation region. In the linear region, for $V_{DS} < V_{GS}$, the charge accumulation across the

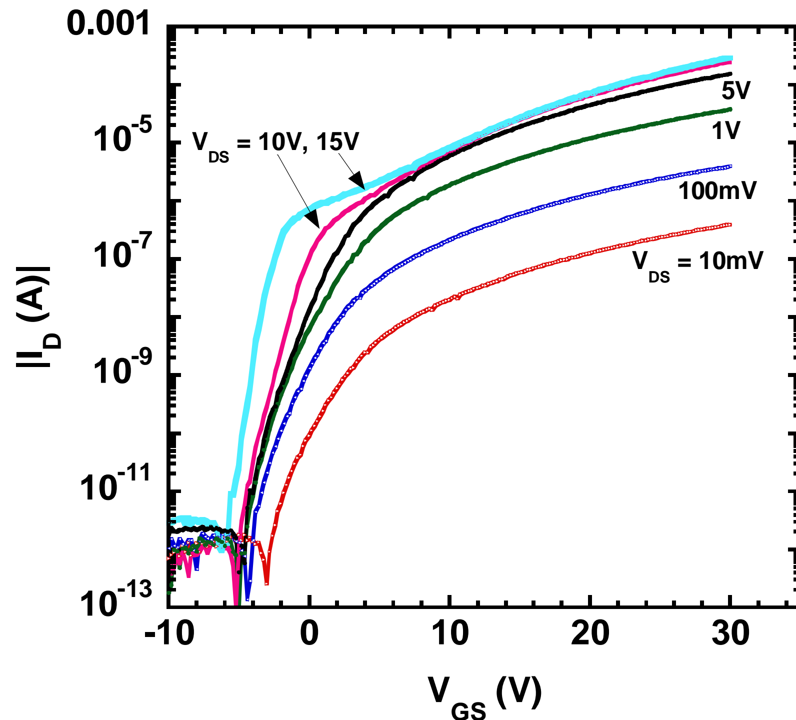


Figure 4.7 Set of, log $|I_D|$-V_{GS}, transfer curves measured for V_{DS} ranging from 10mV to 15V illustrating operation in the linear and saturation region.

entire length of the channel is essentially uniform (i.e. the depletion layer near the drain contact is nonexistent). With this small V_{DS}, and sufficient V_{GS} to ensure above-threshold current conduction where drain current is drift-dominated, Eq. (4.1) is modified and becomes

$$I_D \approx \frac{W}{2L}\mu_{eff}C_{ins}\left[(V_{GS}-V_{TH})V_{DS}\right], \qquad 0<V_{DS}<V_{DS,sat};V_{GS}>V_{TH} \tag{4.5}$$

which is an approximation for linear region operation of the TFT.

TFT carrier mobility is now derived from the channel conductance (variation of I_D with V_{DS}), g_{ch}, given by

$$g_{ch}(V_{GS}) = \lim_{V_{DS}\to 0}\left(\frac{\partial I_D}{\partial V_{DS}}\right) \tag{4.6}$$

at small drain bias (< 1V) where the conductance is expressed as a function of V_{GS}. The V_{DS}= 100mV and V_{DS}=1V transfer curves where chosen for calculation of g_{ch} from the TFT's measured data in Fig. 4.5. Substituting Eq. (4.5) in Eq. (4.6) yields

$$g_{ch}(V_{GS}) = \frac{W}{L}\mu_{avg}(V_{GS})C_{ins}(V_{GS}-V_{TH}) \tag{4.7}$$

where μ_{avg} is the average mobility of the induced channel charge expressed as Q_{ind} = $C_{ins}(V_{GS}-V_{TH})$. Rearranging equation (13), μ_{avg}

$$\mu_{avg}(V_{GS}) = \frac{g_{ch}(V_{GS})}{\frac{W}{L}Q_{ind}} = \frac{g_{ch}(V_{GS})}{\frac{W}{L}C_{ins}(V_{GS}-V_{TH})} \tag{4.8}$$

corresponds to the average mobility of all induced charge in the channel as a function of V_{GS}. Eq. (4.8) is similar to the usual approach for extraction of μ_{FE}; if not for the fact, μ_{avg} (V_{GS}) defines and calculates the mobility as a function of V_{GS} as shown in Fig. 4.6. Thus, μ_{avg} characterizes the average mobility of cumulative charge induced in the channel.

It can be further seen from Fig. 4.8 that the incremental mobility, μ_{inc}, also varies as a function of V_{GS}. In principle, μ_{inc} characterizes the mobility of incremental charge, ΔQ_{ind}, induced in the channel as a function of incremental V_{GS}, ΔV_{GS}. This explicitly accounts for the incremental increase of induced charge in the channel with incrementally increasing V_{GS}. For instance, μ_{inc} is generally taken to increase at higher V_{GS} as interface traps are gradually filled and additional incremental charge is induced. However, it is important to note the effect of grain boundary trap state densities and grain size of the nanocrystalline ZnO thin film on TFT performance characteristics. The gate bias assisted accumulation of carriers is limited by the number of grain boundaries along the channel length. Variation of the potential barrier (V_b) associated with each grain boundary is also gate bias dependent. For V_{GS} values above threshold, V_b reduces to a value comparable to kT/q and has a small contribution in control of the mobility; although, the field-effect mobility does have an inverse exponential dependence on the number of grain boundaries [72]. The μ_{inc} is defined by differentiating the conductance, g_{ch} (V_{GS}), with respect to V_{GS} by

$$g_{ch}^{'}(V_{GS}) = \frac{\Delta g_{ch}(V_{GS})}{\Delta V_{GS}} = \frac{W}{L}\mu_{avg}(V_{GS})C_{ins}\,, \tag{4.9}$$

resulting in

$$\mu_{inc}(V_{GS}) = \frac{g_{ch}^{'}(V_{GS})}{\frac{W}{L}C_{ins}}\,. \tag{4.10}$$

The above set of equations, Eq. (4.6) to (4.10), enable the analytical calculation of μ_{avg}-V_{GS} and μ_{inc}-V_{GS}. As the mobility of induced charge within the TFT channel region, for a given interface quality, depends on scattering and trapping mechanisms, $\mu_{inc}(V_{GS})$

gives insight into the transport characteristics for incremental increases in V_{GS}. Although $\mu_{avg}(V_{GS})$ is more practical for device characterization, because it defines the average mobility of cumulative charge in the channel at a given V_{GS}.

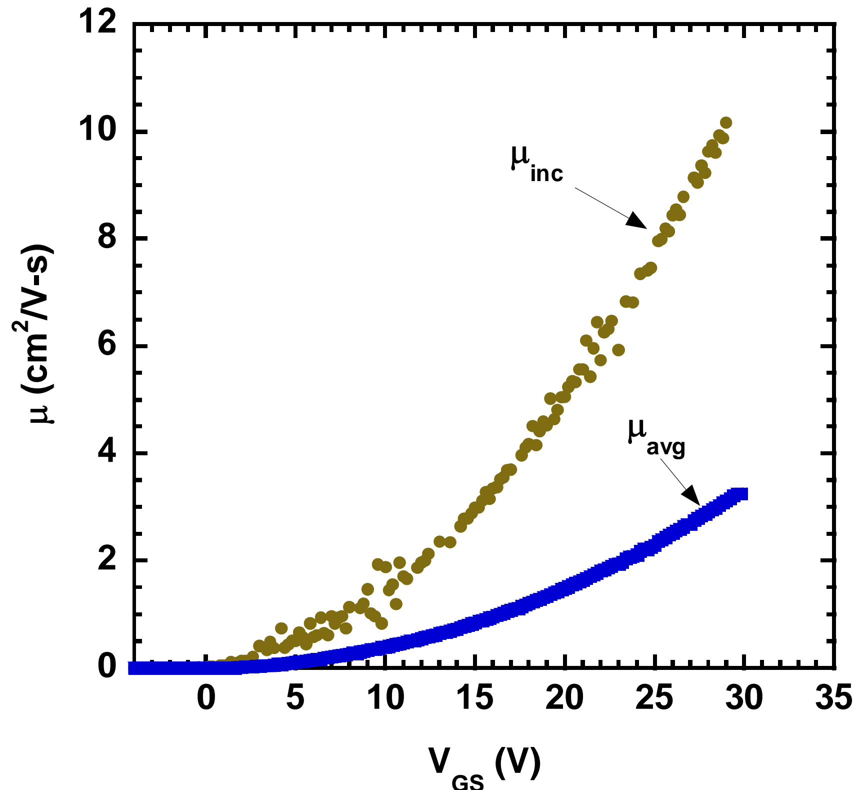


Figure 4.8 Average mobility, μ_{avg}, and incremental mobility, μ_{inc}, dependence on gate bias.

4.4.2 Threshold Voltage by Power Law Extraction

The threshold voltage, V_{TH}, is an important parameter which introduces a certain degree of ambiguity for thin-film transistors. The basic operating principle of the threshold voltage specifies the transition from the sub-threshold regime, where the drain current increases exponentially with increasing gate voltage, to the above-threshold regime [77]. The threshold voltage of ZnO TFTs, like thin-film transistors based on other

materials, is marked by the gate voltage where the accumulated majority carrier density at the ZnO-insulator interface equals the trap density [78]. Typically, TFTs are operated at high drain biases which provide a current larger than the ohmic current associated with the ZnO material. Thus V_{TH} extraction is performed here with drain current operation in the saturation region ensured by setting $V_{GS}=V_{DS}$. As illustrated in Fig. 4.3, V_{TH} is determined by plotting $\sqrt{I_D}$ vs. V_{GS} and linearly extrapolating from the curve's point of maximum slope to the V_{GS} axis x-intercept (i.e. where $I_D=0$). This conventional MOSFET approach accounts for TFT drain current with higher gate bias but fails to include current at lower bias, closer to the extrapolated threshold voltage. Considering the dependence of the field-effect mobility on gate voltage as discussed in the previous sub-section, the above-threshold drain current is modeled with a power-law dependence on gate bias with an empirical parameter, *m*, different than 2 in Eq. (4.11). The approach given by Ortiz-Conde is applied to the ZnO TFTs in this thesis to better estimate V_{TH} [76,79].

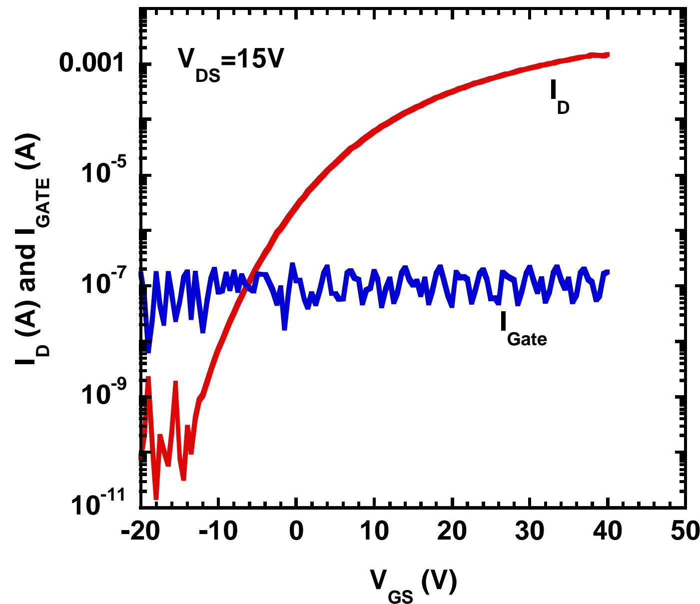


Figure 4.9 Measured transfer characteristics I_D-V_{GS} of a 34nm channel ZnO TFT.

In a TFT, the saturation drain current resulting from pinch-off of the channel near the drain contact is given by

$$I_{Dsat} = K\left(V_{GS} - V_{TH}\right)^{m} \tag{4.11}$$

where K is a conductance parameter with units of $A\text{-}V^{-m}$, m is an empirical parameter, and V_{TH} is the threshold voltage extracted from the power-law fit. Integrating the measured saturation drain current with respect to the gate bias is now used to define the function given by

$$H(V_{GS}) = \frac{\int_{0}^{V_{GS}} I_{Dsat}(V_{GS})dV_{GS}}{I_{Dsat}} \tag{4.12}$$

where $H(V_{GS})$ is numerically evaluated. The integral upper-limit value can be any gate voltage greater than the threshold voltage. Because this model describes drain currents in the saturation (above-threshold) region of the I_D-V_{GS} curve, Eq. (4.12) can be further simplified to only account for gate voltages equal to and above threshold.

$$H(V_{GS}) = \frac{\int_{0}^{V_0} I_{Dsat}(V_{GS})dV_{GS} + \int_{V_0}^{V_{GS}} I_{Dsat}(V_{GS})dV_{GS}}{I_{Dsat}} \tag{4.13}$$

Hence, $H(V_{GS})$ is approximated by

$$H(V_{GS}) \approx \frac{\int_{V_0}^{V_{GS}} I_{Dsat}(V_{GS})dV_{GS}}{I_{Dsat}} \tag{4.14}$$

Using measured I_{Dsat} data extracted from Fig. 4.9, numerically evaluated $H(V_{GS})$ as a function of V_{GS} is shown in Fig. 4.10. Substituting Eq. (4.11) into Eq. (4.14) yields

$$H(V_{GS}) = \frac{(V_{GS} - V_{TH})}{m+1} \tag{4.15}$$

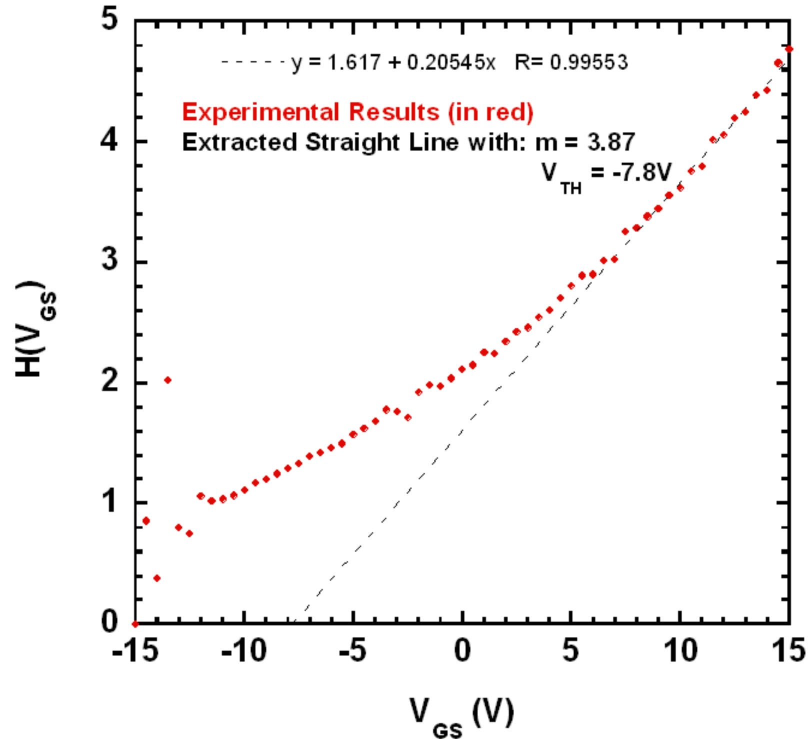


Figure 4.10 Extracted V_{TH} and empirical parameter, m, from the analytical approximation of $H(V_{GS})$-V_{GS}.

which results in a linear expression for $H(V_{GS})$. V_{TH} = -7.8V is now derived from the x-intercept by straight-line extrapolation over a wider range of V_{GS}, and the empirical parameter m=3.9 is determined from the straight-line slope.

For crystalline transistors, the drain current in saturation varies quadratically with the gate voltage. In a polycrystalline TFT the drain currents are much smaller and the field-effect mobility which depends on the induced charge is smaller than the band mobility (Section 4.4.1). The resulting conductance for a TFT increases as V_{GS} is increased, consistent with induced charge and screening effects, at a much faster rate than the conventional relationship based on square-law theory. Thus, the empirical parameter m is used to express this relationship for a TFT. Rearranging Eq. (4.11) in terms of the

conductance parameter K yields Eq. (4.16) shown in Fig. 4.11, along with a linear fit to get K=0.87 nA-V^{-m}.

$$K = \frac{I_{Dsat}}{(V_{GS} - V_{TH})^m} \tag{4.16}$$

In order to check the validity of the power law expression for the threshold voltage, experimental results of I_{Dsat}-V_{GS}, originally shown in Fig. 4.9, are compared with the simulated results based on the numerical calculation given in Eq. (4.11). Using K=0.87 and m=3.87, simulated I_{Dsat} shows good agreement with measured I_{Dsat} data as shown in Figure 4.12.

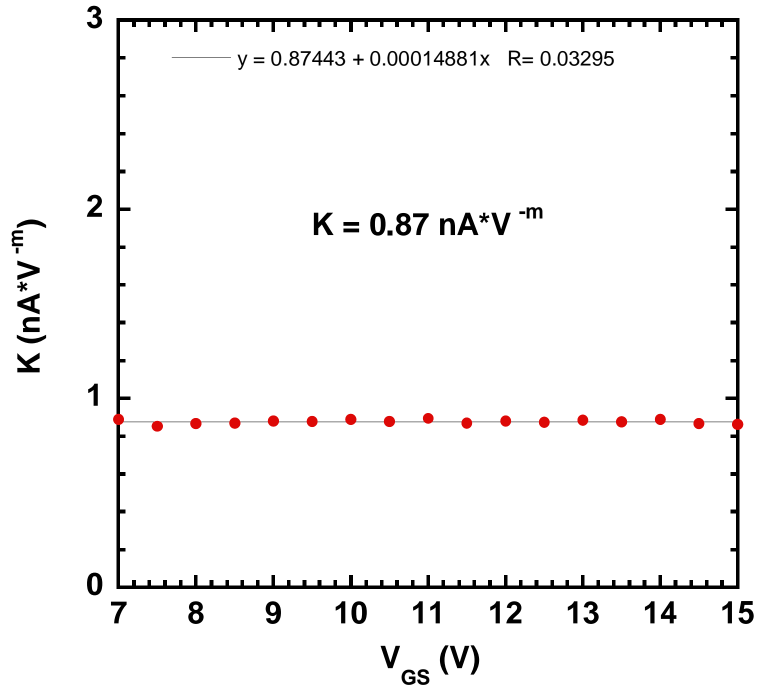


Figure 4.11 Extracted threshold voltage from the analytical approximation of H(V_{GS})-V_{GS}.

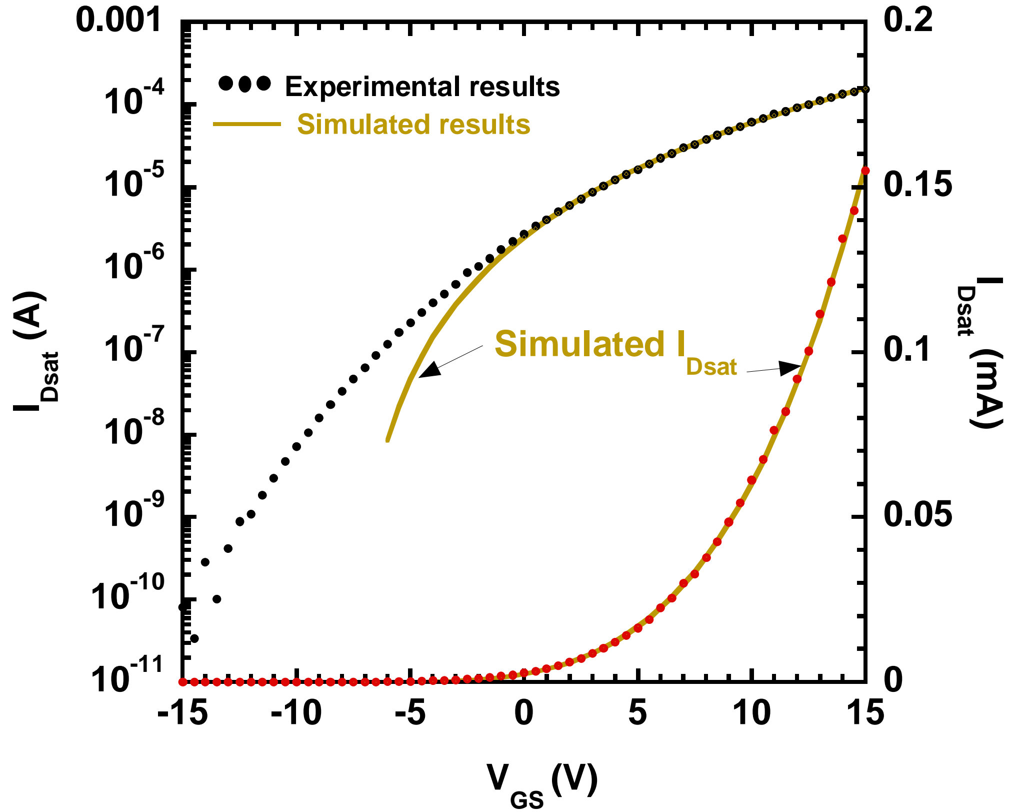


Figure 4.12 Experimental and simulated transfer characteristics of a ZnO TFT operated in saturation.

4.5 Conclusion

Bottom-gate ZnO TFTs were fabricated and tested, and the results have been analyzed using conventional approaches for field-effect transistors. The resulting performance of the ZnO TFTs demonstrated saturation mobility of μ_{SAT} ~ 2cm^2/Vs and current on/off ratio of $I_{ON}/I_{OFF} > 10^9$. A clear tradeoff is observed of increasing I_{ON} for high carrier concentration and thick channel layers, at the expense of increased I_{OFF} and degraded drain current saturation behavior. However, the experimentally observed performance parameters, μ_{SAT} and V_{TH}, introduce a certain degree of ambiguity. The mobility dependence on gate bias introduced two alternative expressions, μ_{avg} and μ_{inc}. This suggests that traps located at the ZnO-SiO_2 interface are detrimental to carrier

transport and compel a non-constant mobility. Furthermore for a TFT, $V_{TH} \approx V_{on}$ yields the onset of a conducting channel after interface trap filling. Overestimation of V_{TH} is explained using a power-law extraction technique.

Chapter V

PLD GROWTH AND CHARACTERIZATION OF ZNO/MGZNO HETEROJUNCTIONS AND APPLICATION TO BURIED-CHANNEL ZNO TFT

Much of the attention making ZnO attractive for optoelectronic devices operating in the visible and ultraviolet spectral regions is due to its ability to sustain large electric fields, higher breakdown voltages, close lattice matching for CdZnO and MgZnO ternary alloys, and strong excitonic effects in the material. Heterojunctions based on ZnO/$Mg_xZn_{1-x}O$ ($x<0.3$) have received considerable interest in recent years for application in UV light emitters and transistors [80]. Quantum wells associated with these heterojunctions may offer enhanced optical and electronic properties for these devices. By spatially separating the unintentionally doped donors from the free electrons, the momentum is increased owing to its quantization in the growth direction [44]. Much effort has been devoted to minimize carrier trapping at the interface of the gate dielectric and active channel of field-effect transistors [81]. Insertion of a thin higher-gap material, MgZnO, adjacent to the gate insulator interface with carrier confinement in the lower-gap material, ZnO, thereby forming a buried-channel layer for carrier transport, exploit the use of a heterojunction in a TFT for improved electron mobility.

Several research groups have successfully demonstrated the growth of high quality ZnO/$Mg_xZn_{1-x}O$ single quantum wells (SQWs), multiple quantum wells (MQWs),

and superlattices (SL) on various substrates by molecular beam epitaxy (MBE) [82-85], metal-organic vapor phase epitaxy (MOVPE) [86], and pulsed laser deposition (PLD) [87]. Bretagnon *et al.* [85] have studied the optical properties of single quantum well structures on (0001) Al_2O_3 substrates and observed the presence of strong polarization effects with 16% Mg in the barrier layer. Reports on the optical properties and associated polarization effects in ZnO/MgZnO quantum wells in the published literature are conflicting, with several authors reporting no polarization effects in ZnO/MgZnO quantum wells [88], motivating further investigation. The conflicting reports on the degree of polarization are likely associated with the ZnO/MgZnO heterojunction interface, where potential fluctuations due to defects or non-abrupt interfaces may play a significant role. Defects or potential fluctuations may result in the trapping of localized carriers/excitons, possible cancellation of polarization effects, and degradation of the radiative efficiency. In this chapter, the growth and optical characteristics of ZnO/MgZnO quantum wells grown by PLD are discussed. Temperature-dependent and excitation-dependent photoluminescence measurements are used to characterize radiative efficiency, polarization effects, and carrier and exciton localization effects in these structures. The quantum wells developed in this thesis are then incorporated into the fabrication of buried-channel TFTs in the interest of improving device performance

5.1 MgZnO Material Properties

The combination of the II-VI oxide semiconductor ZnO with binary compounds, MgO and CdO, give rise to band-gap energy modulation from the visible-to-ultraviolet range. The energy gap versus the *a*-axis lattice constant for these binary compounds is shown in Fig. 5.1. Single-phase, narrower band-gaps are attainable by alloying ZnO with

CdO. With increasing Cd^{2+} mole fraction up to 7%, $Cd_yZn_{1-y}O$ ($y \leq 0.07$), the band-gap decreases from 3.3 down to 3.0 eV [89]. CdZnO/ZnO heterostructures and quantum wells with ZnO serving as the barrier layer make wavelength tunability in the UV-visible range

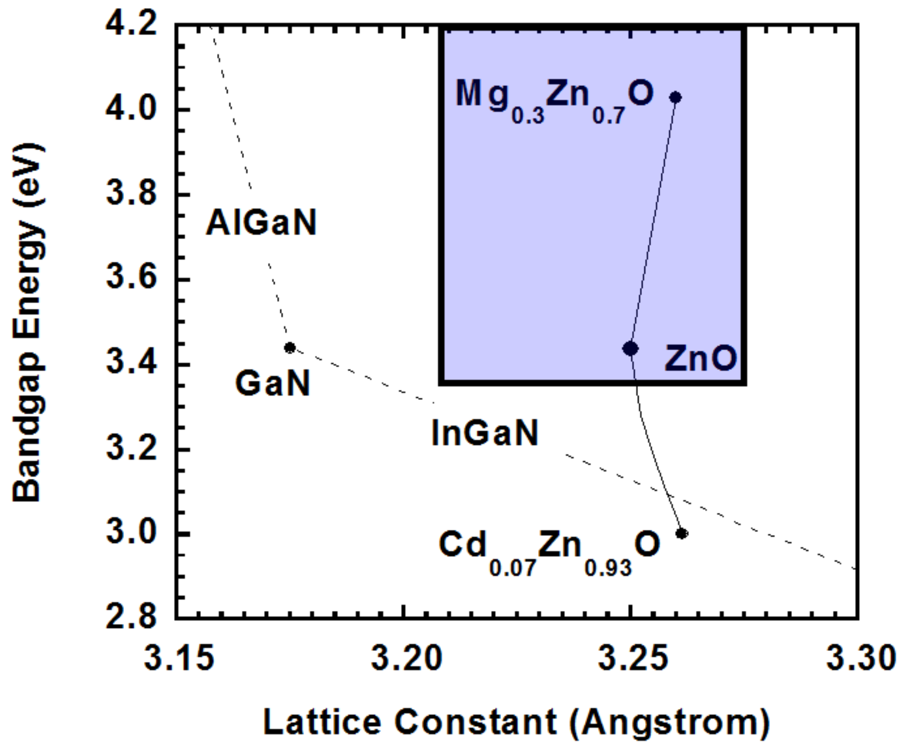


Figure 5.1 Bandgap energy versus the a-axis lattice constant of representative II-VI oxide binary compounds.

possible. However in this thesis, quantum confined heterostructures based on the ZnO/MgZnO material system are demonstrated. The direct band-gap energy of ZnO can be linearly increased to ~4.0 eV by alloying ZnO with cubic MgO. Single-phase $Mg_xZn_{1-x}O$ ($0 \leq x \leq 0.33$) thin films retaining the wurtzite crystal structure were demonstrated by *Ohtomo et al*. [90]. Segregation of the MgO impurity phase in ZnO was shown to occur for a solubility limit greater than 33mol%. There is a gradual change in the *a*-axis and *c*-axis lattice constants, but resulting negligible change in the cell volume up to this

solubility limit. The similarity of the Mg^{2+} (0.57Å) and Zn^{2+} (0.60Å) ionic radius is in agreement with this lack of significant change in lattice constant as Mg replaces Zn. Thus, $Mg_xZn_{1-x}O$ would serve as a suitable, lattice matched barrier layer for ZnO heterostructures with a band gap offset of ΔE_g=0.6 eV. The dependence of Mg content was confirmed by photoluminescence measurement taken at 10K using a continuous He-Cd laser (325nm). A small blueshift in the PL spectra is observed for increasing growth temperature corresponding to increased Mg content, however the $Mg_xZn_{1-x}O$ ($x \leq 0.17$) thin film at 600°C was chosen due to its symmetrical lineshape and small green-band luminescence (Fig. 5.2).

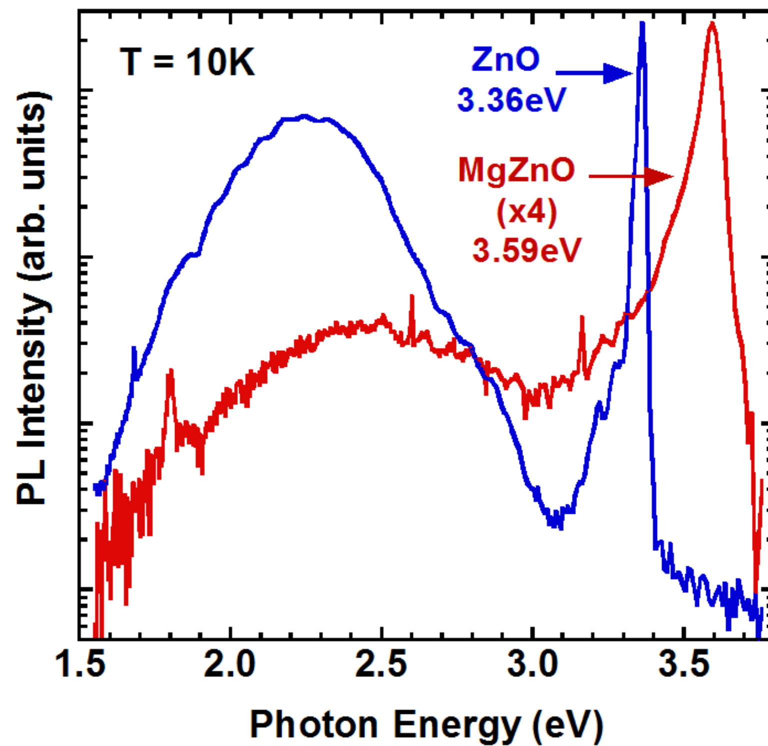


Figure 5.2 Low-temperature PL spectra of $Mg_xZn_{1-x}O$ (x=0-0.17) layers with a thickness of 300-nm. A small blueshift in the PL peak position as a function of the photon energy is observed.

5.2 ZnO/ $Mg_xZn_{1-x}O$ Quantum Well Fabrication

A quantum well is formed by surrounding the ZnO region with the wider-bandgap semiconductor, MgZnO. The width of the well and the height of the barrier determine the discrete energy states allowed to the electrons in the well. ZnO/$Mg_xZn_{1-x}O$ single-quantum well (SQW) and multiple-quantum well (MQW) structures were grown on c-plane sapphire substrates by pulsed laser deposition using a 248-nm KrF excimer laser to ablate a ZnO and 85%/15% ZnO/MgO sintered target. The substrate temperature and oxygen partial pressure for deposition were 600°C and 30mTorr, respectively. A thin ZnO nucleation layer of ~25nm was deposited at low temperature before the growth of the quantum well structure to improve the epitaxial quality of the MgZnO and ZnO epilayers. The thickness of the epitaxial layers was determined using optical reflectance spectra. Quantum well thickness was estimated based on calibration of deposition rate, with an error of ±4%. As mentioned in the previous section photoluminescence (PL) measurements were performed using the 325-nm line of a He-Cd laser as the excitation source, and temperature variation was obtained with a closed-cycle cryostat using helium gas. PL spectra were analyzed with a 0.5m Jobin Yvon spectrometer and standard lock-in techniques, with a spectral resolution of 1meV for settings used in these experiments.

Low-temperature PL was used to relate the bandgap energy to the Mg concentration, x, in the $Mg_xZn_{1-x}O$ barrier layers [90,91]. The Mg concentration, x, of the buffer and top cap layer was determined to be approximately 17% resulting in a total bandgap offset of ΔE_G=250meV. The thickness of the ZnO well region was varied from 3-10nm for the SQWs and 8nm for the MQW. An illustration of a blueshift in the transition energy with decreasing well width for a single quantum well based on the

$ZnO/Mg_{0.17}Zn_{0.83}O$ material system with band offset ($\Delta E_c/\Delta E_v$) of 70/30 is shown in Figure 5.3.

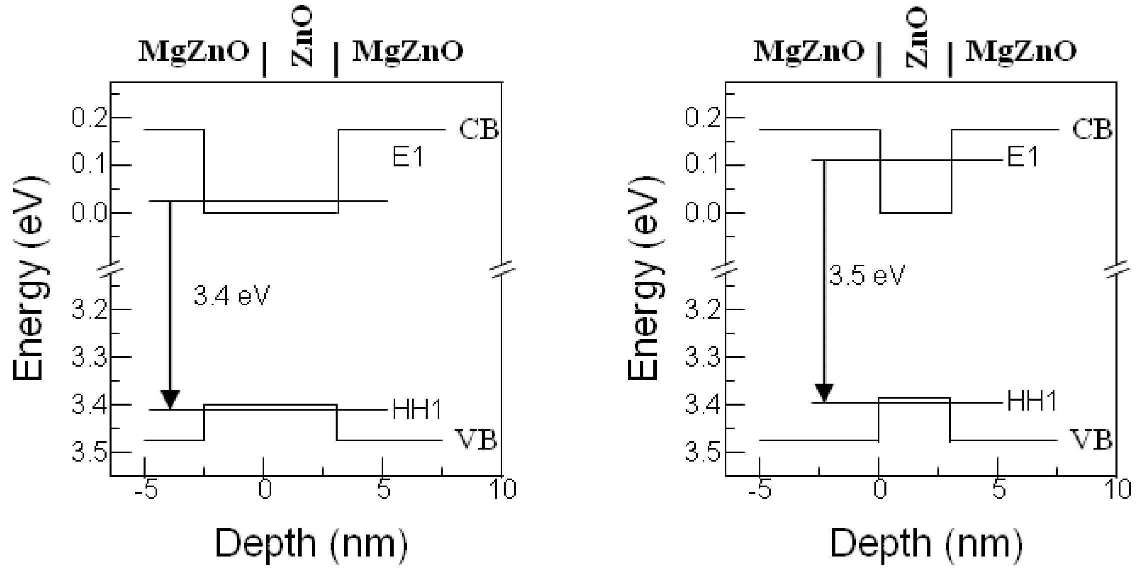


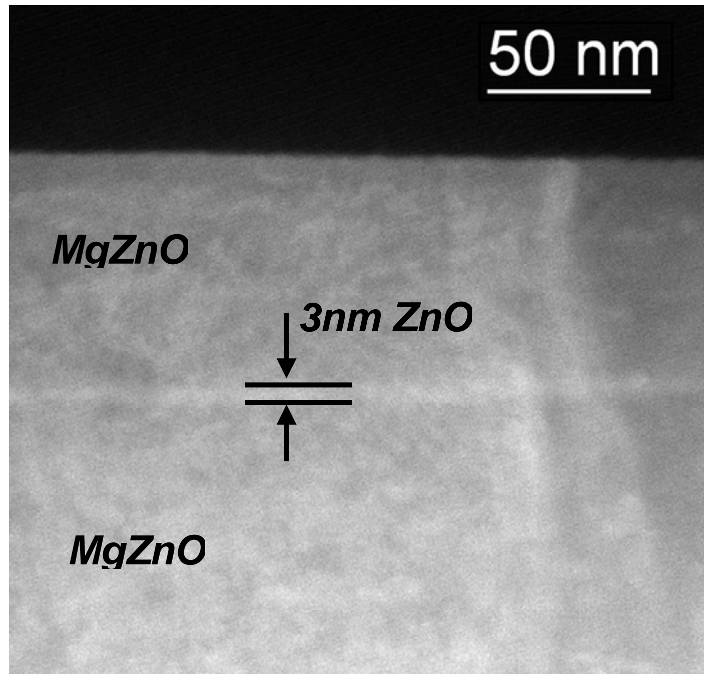
Figure 5.3 Band profile of a ZnO quantum well demonstrating a blueshift in energy with decreasing well width.

5.3 Single Quantum Well Characterization

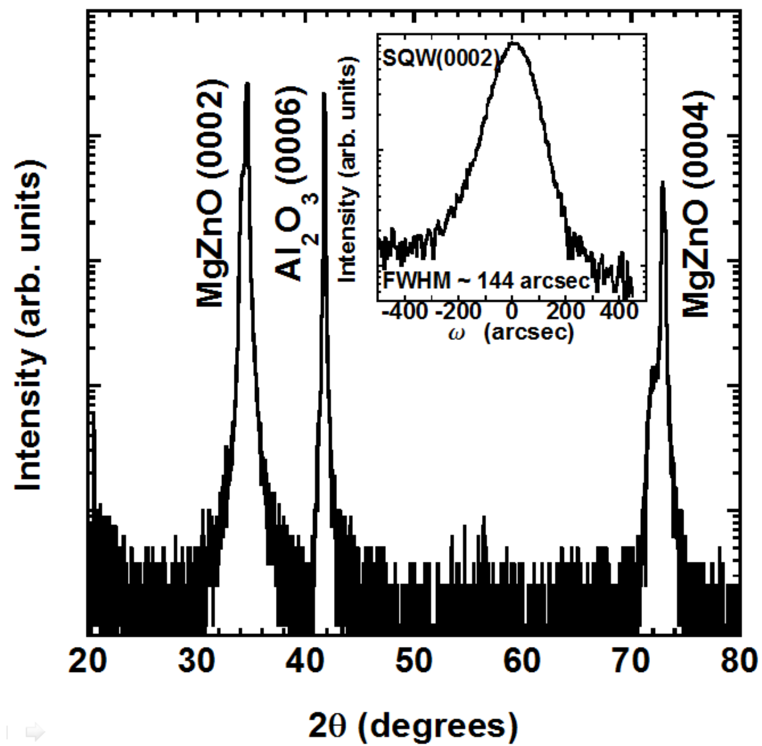
5.3.1 Structural Characteristics

Cross-sectional transmission electron microscopy (TEM) was used to resolve the abrupt interfaces between the ZnO well region and the $Mg_{0.17}Zn_{0.83}O$ barrier layers, as shown in Figure 5.4(a). The structure consisted of a 400nm $Mg_{0.17}Zn_{0.83}O$ buffer layer, a ZnO well layer, and a 50nm $Mg_{0.17}Zn_{0.83}O$ cap layer. The thickness of the well layer observed by TEM is consistent with the growth rate inferred by optical reflectance. Figure 5.4(b) shows the XRD θ-2θ scan of a SQW (L_w~3.2nm), indicating a c-plane orientation for the epitaxial layer. The inset of Fig. 5.4(b) shows the x-ray diffraction rocking curve of the (0002) ZnO/MgZnO diffraction peak, indicating the good crystalline

quality associated with a full-width at half maximum (FWHM) of approximately 144 arcsec. The surface roughness of the epilayers was found to be <10nm using atomic force microscopy.



(a)



(b)

Figure 5.4 (a) Cross-sectional TEM image and (b) θ-2θ XRD spectra with rocking curve showing the (0002) diffraction peak of the ZnO(3.0±0.2nm)/$Mg_{0.17}Zn_{0.83}O$ SQW on a sapphire substrate [92].

5.3.2 Optical Characteristics

Low temperature PL spectra of the SQW structures reveal quantum confinement with a systematic blueshift of the bandedge transition as a function of decreasing ZnO well width, as shown in Figure 5.5. Quantum well emission varies from 3.37eV to 3.49eV with a barrier emission at 3.62eV. LO-phonon replicas are observed with a separation of ~72meV from the quantized transitions, indicating high quality material. Data from Fig. 5.5 are summarized in Table 5.1, where there is a clear increase in excitonic line broadening of the SQWs from 21-36meV (full width at half maximum) with increasing ZnO well width (3.2 - 9.5nm). The increased linewidth of the excitonic transition peak may be a result of well-width fluctuations due to roughness along the well/barrier interface and/or nonuniformities in the MgZnO alloy composition. Nonuniformities in the MgZnO alloy composition are a possibility, where the linewidth of the PL response of a MgZnO thin film was measured to be 49meV. However, the low-energy tail of the PL spectra is characteristic of localized carrier/exciton trapping at bandtail states. This behavior is consistent with interface roughness fluctuations [93-95].

Figure 5.6 shows the temperature dependent PL spectra of the SQW with L_w=3.2nm. The intensity of the excitonic transition peak energy gradually decreases with increasing temperature. Thermal line broadening at elevated temperatures is consistent with dissociation of the main peak, DX^{QW}. The QW peak energy is plotted as a function of temperature and described with the Varshni empirical equation [96]

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{(T+\beta)} \tag{5.1}$$

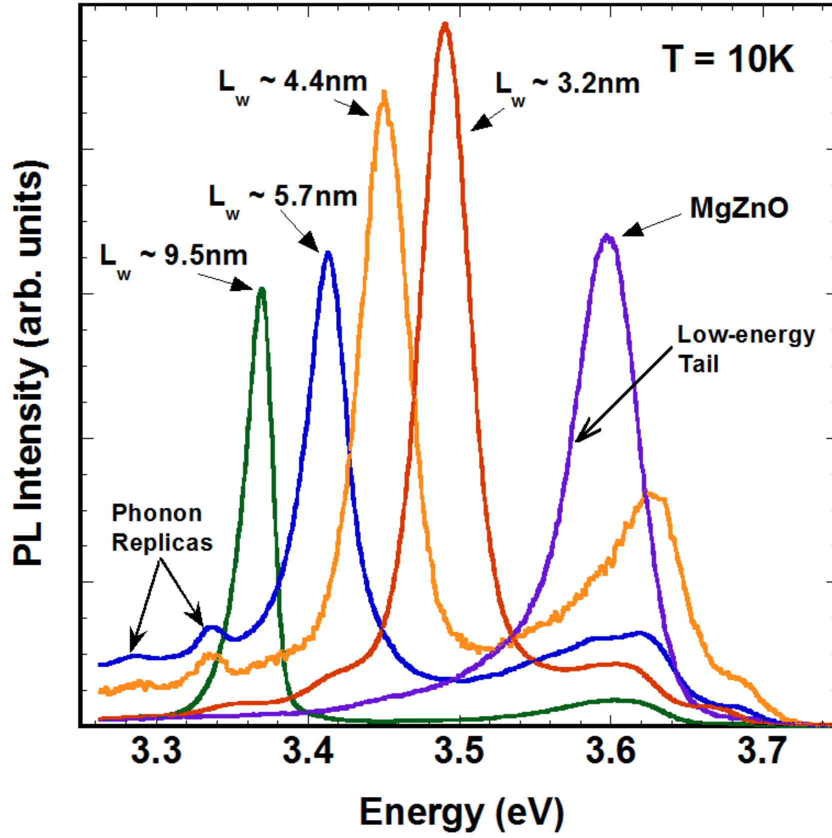


Figure 5.5 PL spectra of ZnO/MgZnO SQWs illustrating an excitonic blueshift with decreasing well thickness.

L_w (nm)	E_{ex} (eV)	FWHM (meV)
3.2	3.491	21
4.4	3.450	30
5.7	3.413	36
9.5	3.369	36
MgZnO	3.603	49

Table 5.1 FWHM of the excitonic line broadening for the ZnO/MgZnO SQWs as a function of increasing well width.

with values of α=1.47x10^{-3}eV/K and β=1890K for the MQW, as shown in Fig. 5.7(a). Figure 5.7(b) shows the PL peak energy obtained from the temperature-dependent PL for the SQW (L_w~3.2nm) in Fig. 5.5 for T<100K. The sample exhibits an "S-shape" behavior which is typical of carrier localization effects as a result of potential fluctuations at the well-barrier interface [97]. This anomalous displacement of the PL peak energy results in a redshift/blueshift of approximately 4meV.

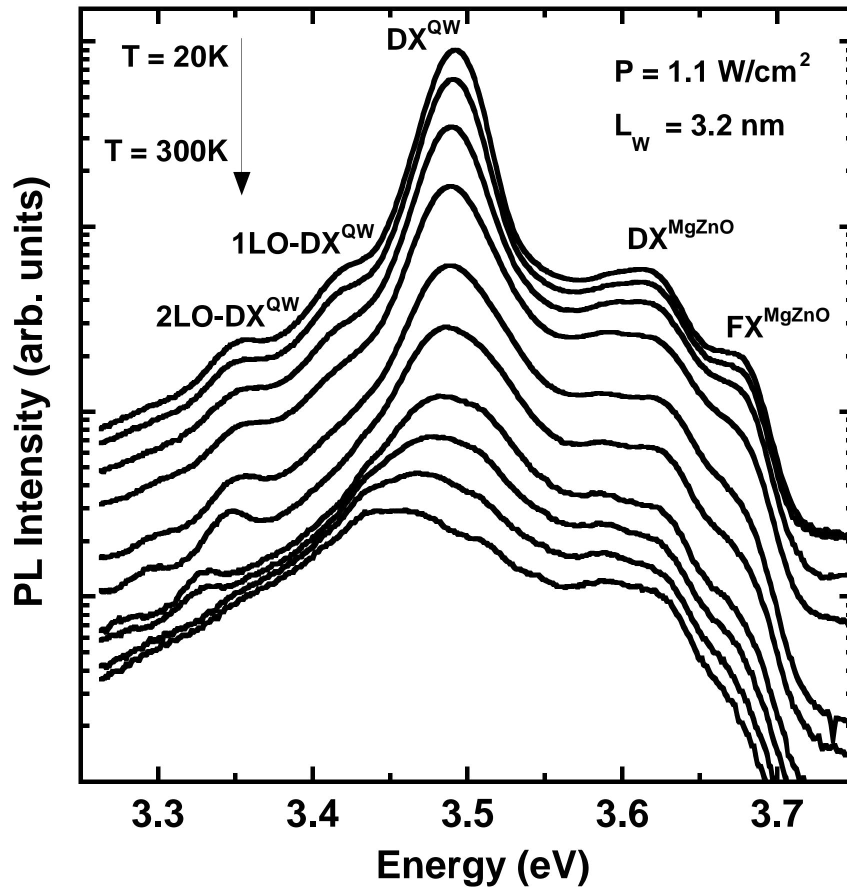
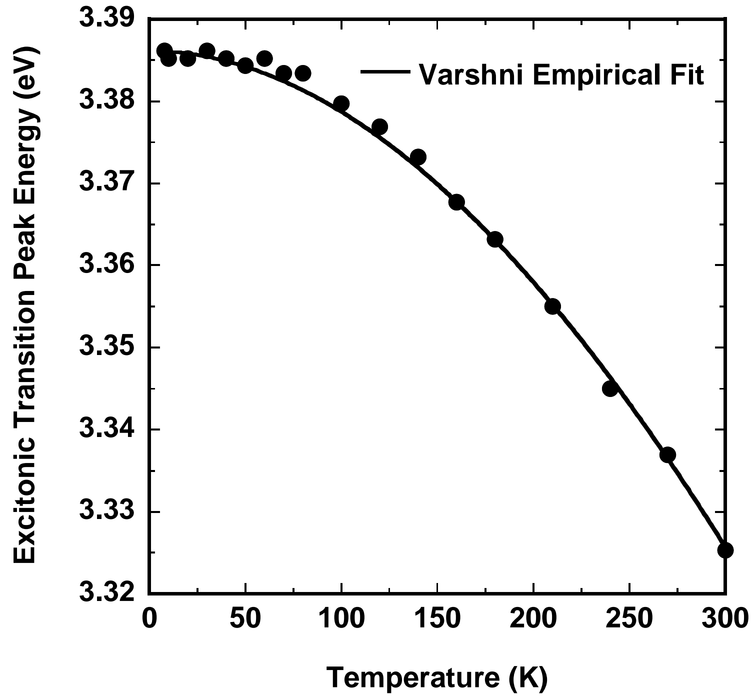
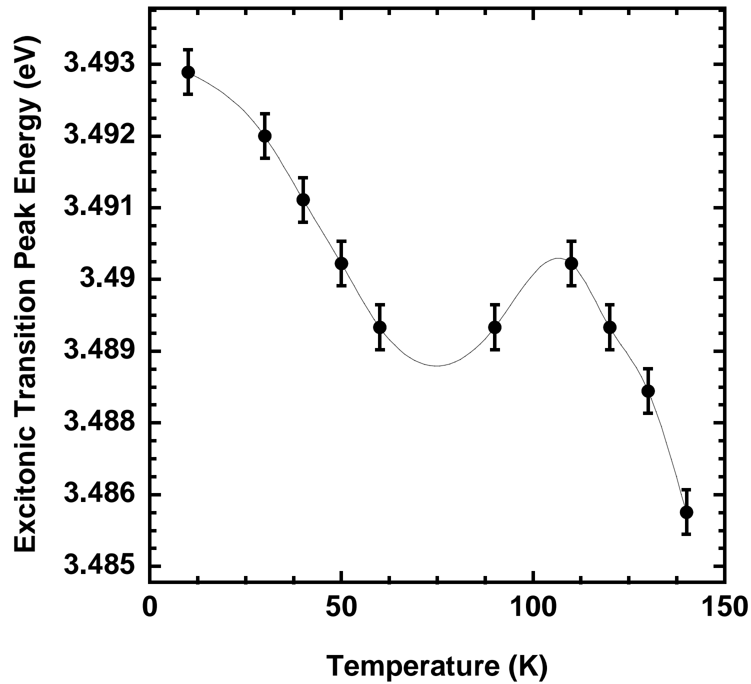


Figure 5.6 Temperature-dependent PL spectra of the ZnO/MgZnO (L_w~3.2nm) SQW.



(a)



(b)

Figure 5.7 PL peak energy as a function of temperature for (a) the 5-period ZnO/MgZnO MQW and (b) the ZnO/MgZnO (L_w~3.2nm) SQW exhibiting a red- then blue-shift emission between 20-100K.

5.3.3 Polarization and Carrier Localization Effects

Heterostructures based on polar materials with the wurtzite crystal structure can exhibit a strong Quantum Confined Stark Effect (QCSE) due to the internal electric field associated with the spontaneous polarization and/or piezoelectric effects. These polarization-induced effects reduce the oscillator strength of optical transitions, therefore degrading recombination efficiency. The near lattice match of ZnO and MgZnO suggests that piezoelectric effects should be minimal due to the small amount of strain. However, a significant degree of spontaneous polarization (P_{sp}=-0.025C/m^2 for ZnO) [98] is expected due to its wurtzite symmetry, similar to the GaN/AlGaN system (P_{sp}=-0.029C/m^2 for GaN) [99]. As described in the introduction, Bretagnon *et al*. [85] recently reported the observation of large internal electric fields as a function of Mg content for ZnO/MgZnO SQWs. However, weak or negligible polarization effects are observed in the ZnO/MgZnO SQW samples studied here, based on the bandedge transition energy and excitation power dependent photoluminescence. The excitation dependent PL for a SQW with L_w=3.2nm shows a negligible peak energy shift with excitation intensity (Fig. 5.8), where an energetic shift would be expected for strong polarization effects due to screening of the built-in electric field in the quantum well. The measured results are limited by maximum laser excitation energy of 2.2 W/cm^2.

The PL peak energies of the QWs shown in Fig. 5.4 are plotted as a function of well width in Fig. 5.9. The energetic position of the bandedge transition will be influenced by energy quantization in the 2-D system, exciton binding energy, and spontaneous and piezoelectric polarization effects. The calculated dependence of bandedge transition energy versus well width is plotted (Fig. 5.9) for cases with and

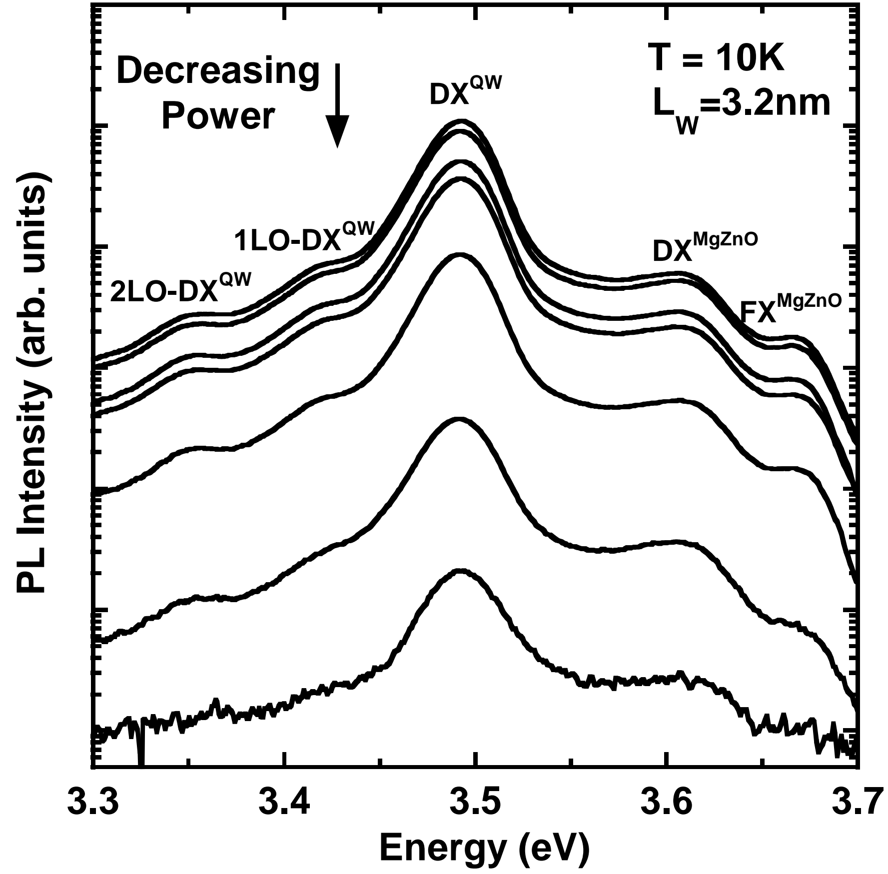


Figure 5.8 Excitation-power density dependent PL spectra of a SQW measured at 10K. There is no apparent blueshift with increasing intensity.

without polarization effects. Quantization of energy levels are calculated by

$$E_{ex} = E_g^{ZnO} + E_e + E_h - E_b^{QW} \tag{5.2}$$

assuming $0.24m_0$ and $0.78m_0$ for the electron and hole effective masses, respectively, and band offsets ($\Delta E_c/\Delta E_v$) of 70/30. Variation of the exciton binding energy with well width was accounted for according to the work by Coli and Bajaj [100]. Polarization effects were calculated assuming spontaneous polarization (P_{sp}) values (-0.025C/m^2 for ZnO, -

0.072C/m^2 for MgO) and piezoelectric coefficients, e_{33}=1.34C/m^2 and e_{31}=0.57C/m^2.[12] The PL peak energy dependence follows the calculated behavior, with values somewhere between expectation with and without polarization effects. This suggests that there is likely some degree of weak polarization effect in the quantum wells. As the well width approaches 10nm, there is a small, but measurable, red-shift of the peak energy below the ZnO bandedge. The small polarization effects may be attributed to point defects or potential fluctuations at the heterointerface associated with our PLD process, in comparison to the MBE process used by *Bretagnon, et al*. [85]

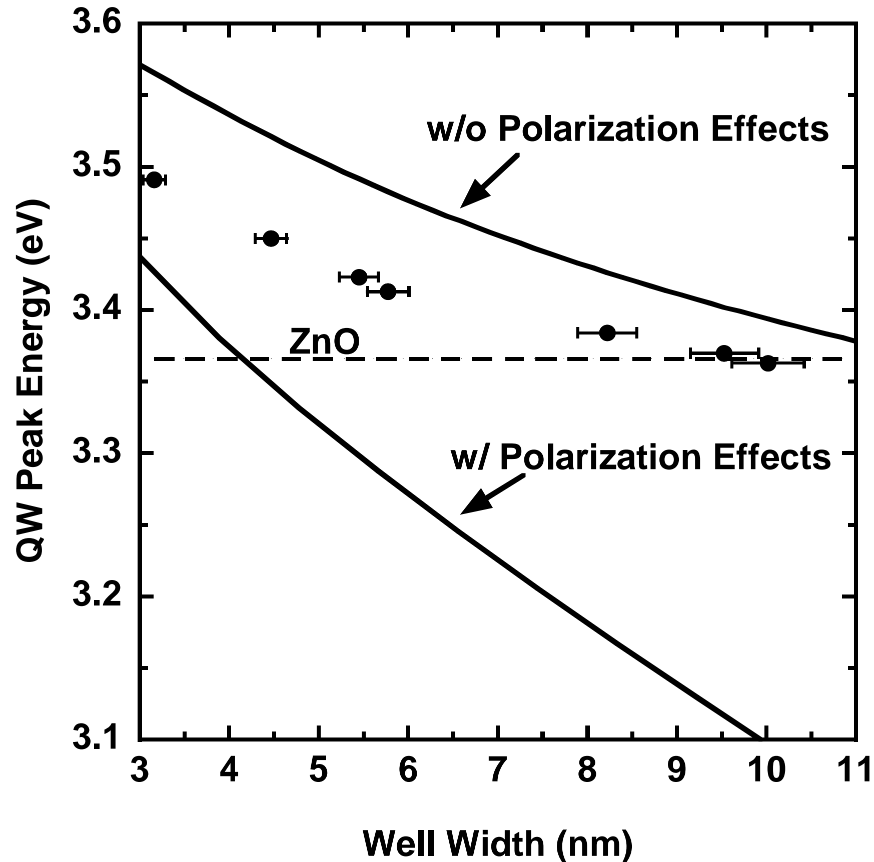
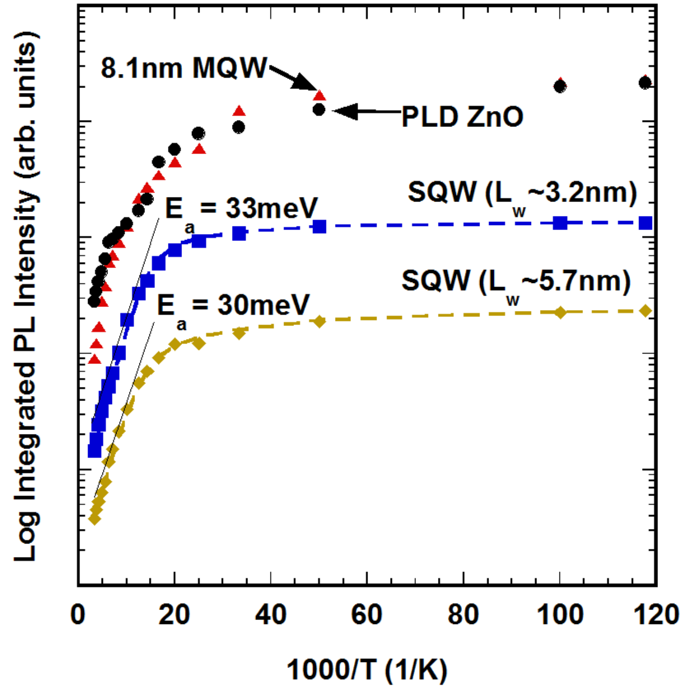


Figure 5.9 PL peak emission energy for c-plane SQWs as a function of the well width. The calculated ground state transition taking the exciton binding energy into account is plotted with and without the presence of polarization effects. SQW peak energy redshifts below the ZnO bandedge for well widths above 9.5nm.

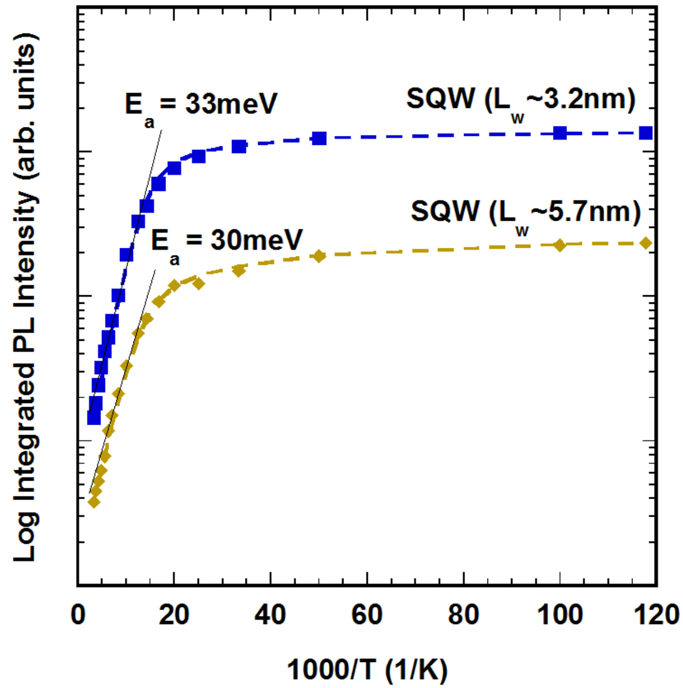
The integrated PL intensities as a function of inverse temperature are shown in Fig. 5.10(a) for two ZnO/MgZnO SQWs (L_w ~ 3.2 and 5.7nm), a MQW (L_w ~ 8.1nm), and for a 530nm thick ZnO layer grown by PLD. At low temperature, the larger active volume of the MQW enhances its integrated intensity above that of epitaxial ZnO. Thermal quenching of the integrated intensity is observed with increasing temperature for all samples, indicating the characteristics of nonradiative recombination mechanisms. Improved integrated intensity is observed for smaller well width, indicating the expected improvement associated with enhanced oscillator strength for increased quantum confinement. It should be noted that the possible existence of defects at the ZnO/MgZnO interface that could be the source of weak polarization effects are not deleterious to the optical properties in these structures, based on the strong radiative efficiency observed. Non-radiative processes may be examined from the temperature dependence using a dual activation energy Arrhenius model given by [93,95]

$$I(T) = \frac{I_o}{1 + Ae^{-(-E_a/kT)} + Be^{-(-E_b/kT)}} \tag{5.3}$$

where I_o is the intensity at T=0K (T~8.5K), A and B are coefficients that measure the efficiency of the quenching mechanisms within the QW, and k is Boltzmann's constant. The thermal activation energy values, E_a and E_b, quantify the impact of non-radiative channels on the PL integrated intensity. The fit of two of the quantum wells to this model is shown in Fig. 5.10(b). The activation energy E_a was determined to be 33±0.2meV and 30±0.4meV for the 3.2nm and 5.7nm SQW, respectively. Increased thermal activation energy, E_a, indicates a weaker influence of defect-related non-radiative recombination



(a)



(b)

Figure 5.10 (a) Integrated PL intensity as a function of temperature for ZnO/MgZnO SQWs (L_w of 3.2 and 5.7nm), 5-period ZnO/MgZnO MQW and a 530nm thick ZnO epitaxial layer. (b) Arrhenius plot fitted to the SQWs with the activation energy indicated by the slope in the high temperature region.

which may again be attributed to enhanced quantum confinement.

The lower activation energy value used to describe the second non-radiative channel, E_b, fits temperature dependence of the Arrhenius model between 20-80K. This suggest that E_b is used to explain thermal quenching of the PL intensity at low temperature (<100K). Moreover, this behavior is associated with the "S-shape" behavior of the temperature-dependent PL observed in Fig. 5.7(b). At temperatures <100K, emission from lower energy band-tail states is significant, where localized trapping of carriers/excitons in these lower energy states results in the initial redshift emission observed in the PL spectra. As temperature is increased, these carriers gain enough energy to escape from the localized potentials associated with interface roughness or defects at the ZnO/MgZnO heterointerface. Thermalization of the localized carriers into the higher energy states leads to a blueshift in the emission spectra. Above T=100K, expansion of the lattice crystal structure results in the characteristic redshift of the bandgap energy with temperature. For the L_w=3.2nm SQW, E_b is estimated to be (4.8±0.3)meV which corresponds to the localization energy of ~4meV observed in Fig. 5.7(b). Thus, E_b is an indication of the localization energy associated with the ZnO/MgZnO SQW.

Time-resolved photoluminescence (TRPL) experiments in Fig. 5.11 were performed at T=15K using a Nd:YAG high energy pulse laser system to further understand the emission mechanisms. The effect of non-radiative recombination mechanisms are negligible at low temperature, thus allowing for the analysis of radiative lifetime as a function of well width. Here, SQWs (L_w=4.4 and 5.7nm) were compared with the 530nm thick ZnO layer. The SQW with the 4.4nm well width appears to have a

faster decay lifetime when compared to the 5.7nm SQW. The longer recombination lifetimes with increasing well thickness further suggest that defect-related recombination is less significant for thinner quantum wells. This is further supported with the observed decreased PL peak emission intensity with increasing well width (Fig. 5.5). Suggesting that carrier trapping at localized states for thicker well widths delays recombination lifetimes, thus decreasing PL emission intensity [101].

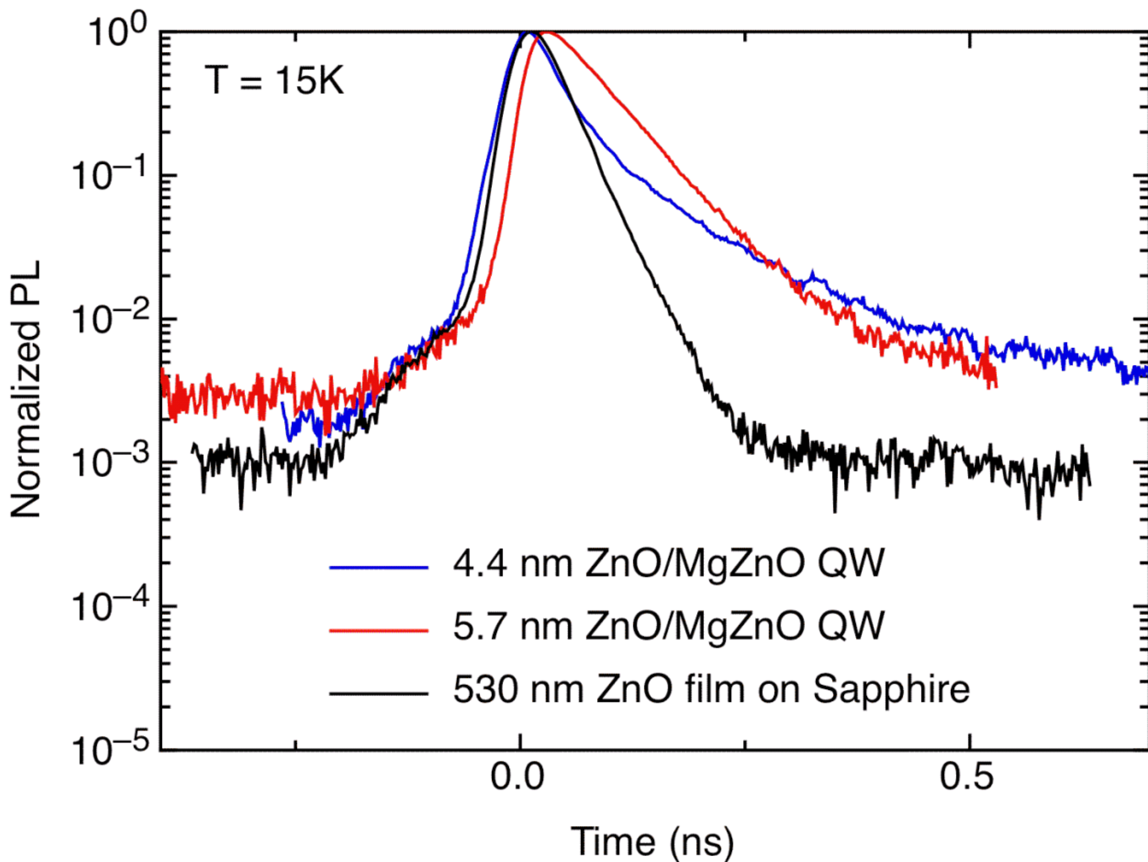


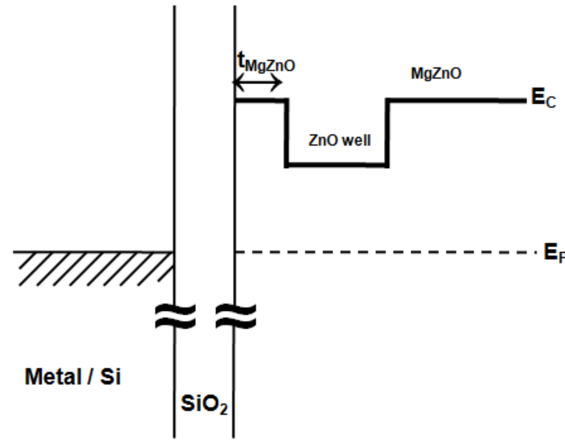
Figure 5.11 Time-resolved PL intensity as a function of ZnO/MgZnO SQW width (L_w of 4.4 and 5.7nm) and a 530nm thick ZnO epitaxial layer.

5.4 Buried-Channel ZnO/MgZnO TFT Device

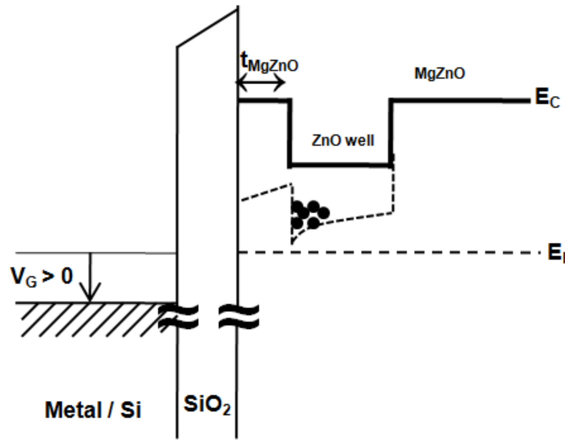
It was shown in Chapter 4 that the mobility dependence on gate voltage was due, in part, to the trapping of accumulated electrons at the SiO_2-ZnO interface of the TFT device. This is detrimental to device performance, specifically the carrier mobility. One approach to suppress the effect of electron trapping is to isolate the active ZnO channel away from the gate dielectric interface. Inserting the higher band-gap, $Mg_{0.17}Zn_{0.83}O$, forming a $Mg_{0.17}Zn_{0.83}O$-ZnO heterostructure at the gate dielectric interface confines carrier accumulation away from the SiO_2 surface thus improving carrier transport by reducing surface scattering. Buried–channel models to control the influence of the interface on carrier mobility have been shown for a-Si:H TFTs [81] and MOS-gated Si-Ge_xSi_{1-x} heterostructures [34]. The growth of heterojunctions based on the II-VI oxide semiconductor and its ternary alloy, $Mg_xZn_{1-x}O$ ($x<0.3$), by pulsed laser deposition with observed carrier confinement were successfully demonstrated and characterized in previous sections of this chapter. The fabrication and electrical characterization of a ZnO buried-channel TFT channel layer are discussed in this section. In particular, simulation of electron accumulation spatial dependence in the ZnO well region as a function of V_{GS} and experimental evidence demonstrating the transition of electron accumulation in the buried channel to electron build-up at the $Mg_xZn_{1-x}O$-SiO_2 interface by capacitance-voltage measurement are presented.

5.4.1 Simulation of ZnO Buried-Channel TFT

The conduction band-edge diagram for the SiO_2-$Mg_xZn_{1-x}O$-ZnO material system is shown in Fig. 5.12. The discontinuity in the conduction band leads to 2-D electron confinement. Depending on the value of a positive bias applied to the gate, the bands



(a)



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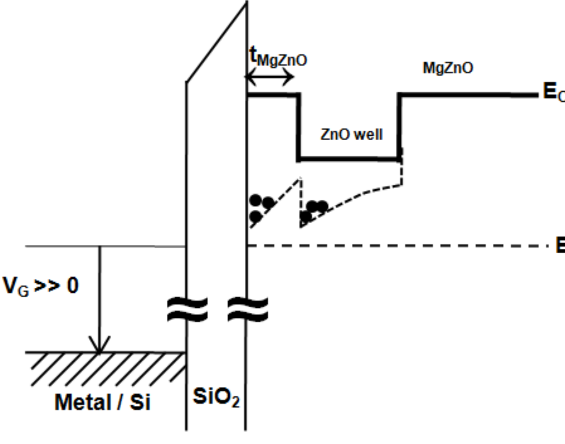


(c)

Figure 5.12 $ZnO/Mg_{0.17}Zn_{0.83}O$ SQW forming the channel region of a TFT (a) at flat-band (b) with the accumulation of electrons in the ZnO well region at small V_{GS} and (c) with the accumulation of electrons at the $SiO_2/Mg_{0.17}Zn_{0.83}O$ interface along with that in the well region at higher V_{GS}.

bend downward with electron charge confined at the heterointerface. At sufficiently high gate bias, the increasing electric field gives the electrons enough energy to surmount the barrier layer. Electron charge is eventually depleted from the barrier layer and accumulates at the gate dielectric interface. The electric field during the transition to surface channel operation is given by $E_{tran} = \Delta E_c / t_{MgZnO}$. If the MgZnO spacer layer is too large or ΔE_c is too small, a surface channel will form at low electric fields before the buried-channel accumulates.

A buried-channel TFT (BCTFT) structure is simulated similar to the ZnO TFT device simulation in Chapter 4. The dimensions (channel length L=10um, channel width W=100um, MgZnO spacer layer thickness t_{MgZnO}=5nm, ZnO well layer thickness t_{ZnO}=10nm, MgZnO cap layer thickness $t_{\mathrm{MgZnO_cap}}$=15nm, and gate dielectric thickness t_{SiO2}=70nm) were chosen to mirror a total active-channel thickness of 30-nm. Other parameters affecting device performance are the donor density $N_B=1x10^{17}cm^{-3}$ (which varies with either depletion or accumulation in the channel), areal trap density at the interface $N_T=1x10^{13}cm^{-2}$, and material Hall mobility $\mu=10cm^2/V\text{-}s$. As shown in Fig. 5.12 and Fig. 5.13(a) and (b), spatial distribution of carrier density is observed in a distance 5-15nm from the SiO_2 surface for V_{GS} of 5V and 10V, respectively. The increase of carriers at the MgZnO/SiO2 interface equals and begins to exceed that confined by the ZnO/MgZnO heterointerface barrier for a gate bias of 25V (Fig. 5.13(c)). As the gate voltage is driven to 30V, as shown in Fig. 5.13(d), the highest electron concentration resides near the MgZnO-SiO_2 interface. This efficiently demonstrates the spatial location of carriers confined to the well created by the ZnO/MgZnO heterostructure as a function of gate bias.

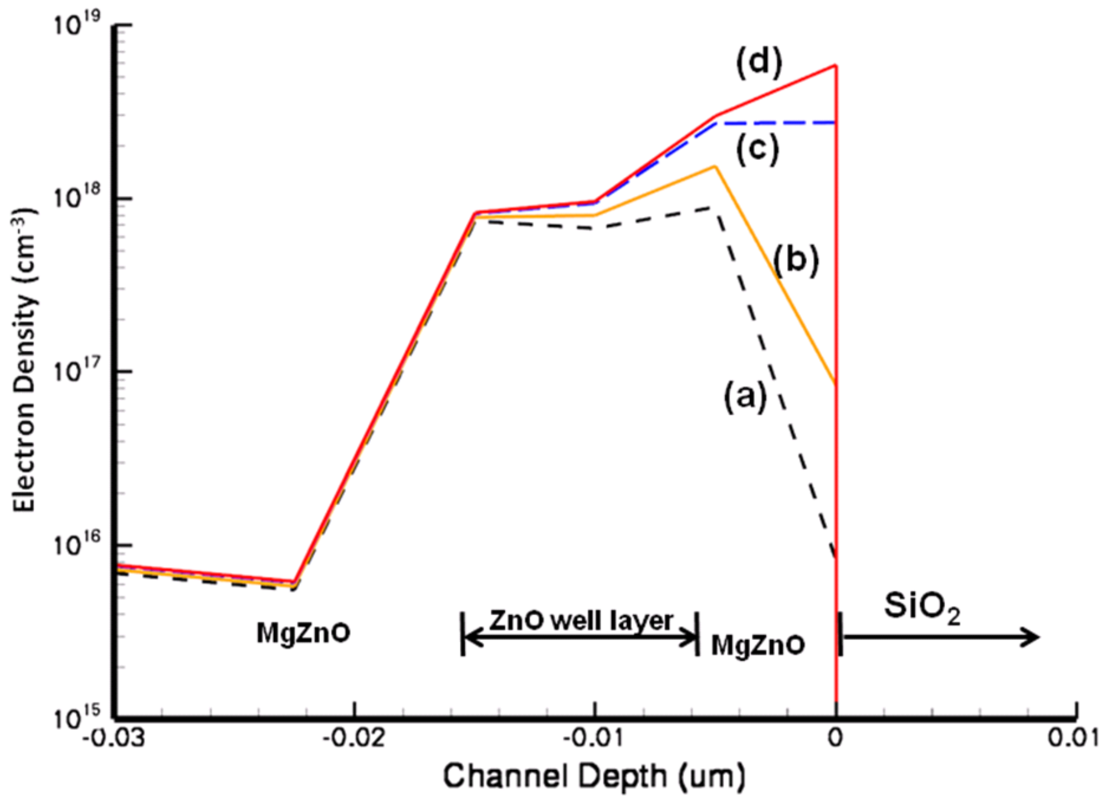


Figure 5.13 ZnO/$Mg_{0.17}Zn_{0.83}O$ SQW forming the buried-channel region of a TFT with spatial distribution of electron accumulation for four different gate bias conditions (a: accumulation 5-15nm from SiO_2 at V_{GS}=5V, b: increased accumulation of electrons near the ZnO/MgZnO interface at V_{GS}=10V, c: electron accumulation at the ZnO/MgZnO interface equals that at the SiO_2/MgZnO interface at V_{GS}=25V, and d: surface accumulation along the SiO_2 interface at V_{GS}=30V).

5.4.2 Buried-Channel TFT DC Characteristics

Transfer characteristics of a surface channel and buried-channel TFT are shown in Fig. 5.14. The gate bias was swept from -20 to +40V for these TFTs of identical thickness. Both devices are shown to have comparable on-to-off current ratio and on-current. The peak output current of the BCTFT was suspected to be significantly greater than the ZnO TFT; however, the current of the BCTFT may be limited by the higher resistivity associated with the 15-nm MgZnO layer adjacent to the source/drain contacts.

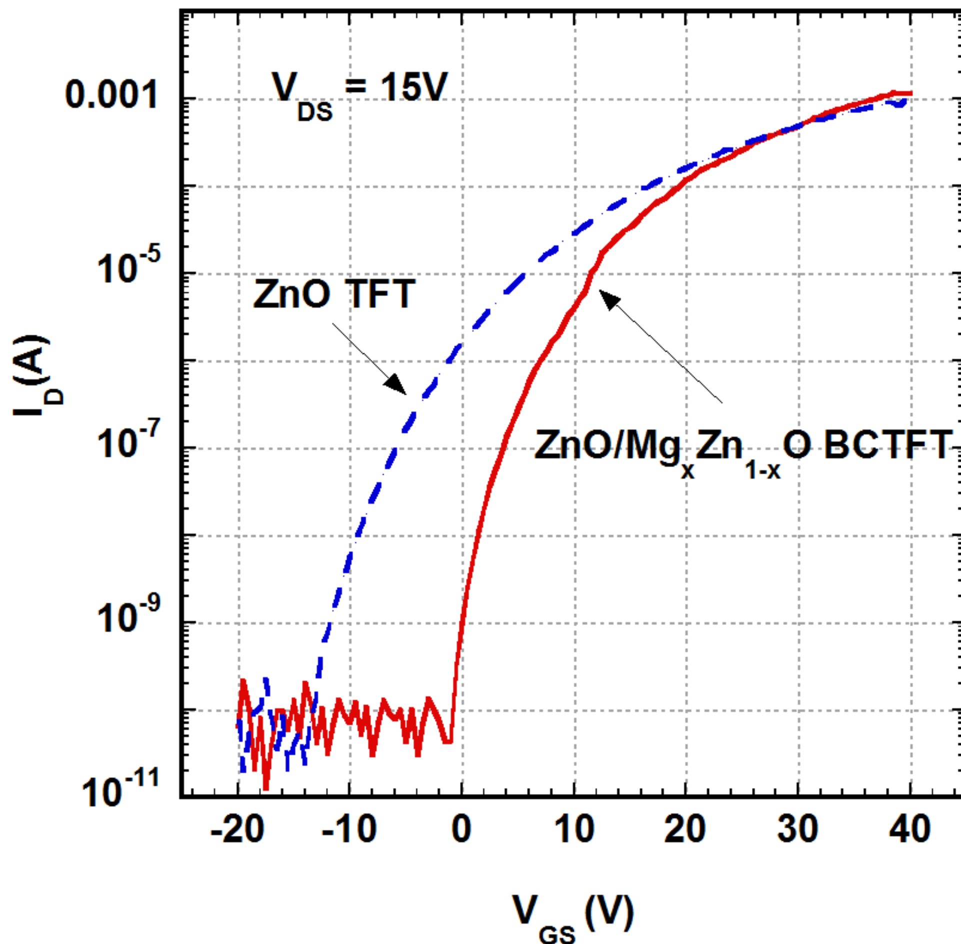


Figure 5.14 Transfer characteristics for a ZnO-$Mg_{0.17}Zn_{0.83}O$ buried-channel TFT and a surface channel ZnO TFT operated in saturation, V_{DS}=15V. The BCTFT has a much steeper subthreshold slope.

The capacitance-voltage characteristic of the BCTFT and the ZnO TFT (Fig. 5.15) are varied from depletion at negative gate bias to accumulation at high positive gate bias. Since, for positive gate bias, electrons are accumulated at the surface of the gate dielectric, the capacitance is equivalent to the capacitance of the 700Å SiO_2, C_{SiO2}=49 nF/cm^2. For negative bias, the entire active channel is depleted and the total capacitance is a series combination of C_{SiO2} and the capacitance associated with the depleted channel. The observed plateau at 15V indicates the buried accumulation of electrons in the buried-ZnO layer. The thickness of the higher gap, MgZnO, layer is found by [81]

$$C_{MgZnO} = \frac{C_{SiO2} C_{ZnO}}{C_{SiO2} - C_{ZnO}} \tag{5.4}$$

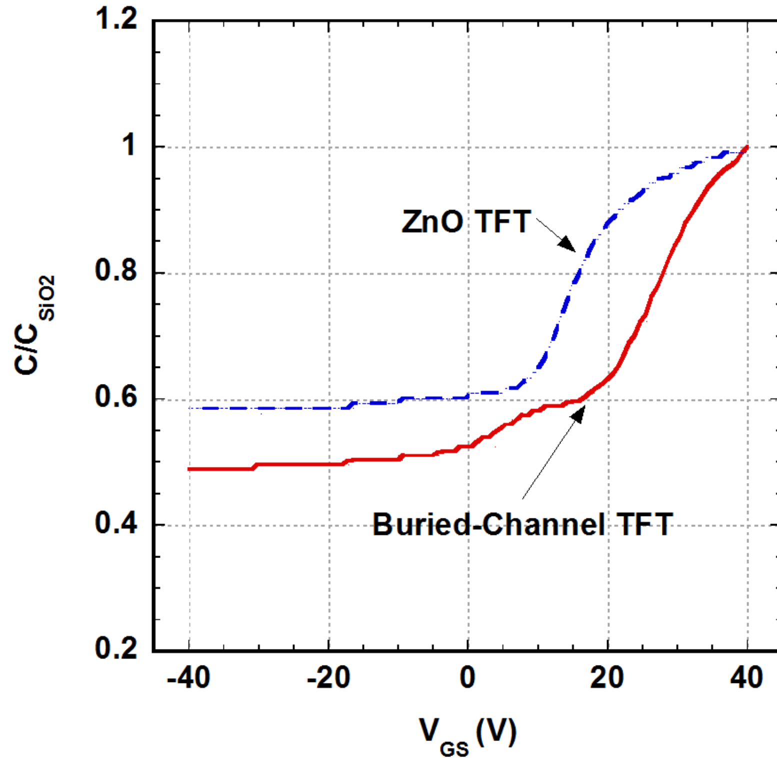


Figure 5.15 Capacitance-voltage (C-V) relation for a buried-channel and surface channel ZnO TFT of comparable thickness. The plateau in the C-V for the BCTFT denotes electron confinement in the buried channel ZnO layer at V_{GS}=15V.

where the buried-channel capacitance, C_{ZnO}, is 28 nF/cm^2. The calculated thickness of the $Mg_{0.17}Zn_{0.83}O$ layer adjacent to the SiO2 interface is 13.3 nm. This compares reasonably well with the 8-10 nm thickness expected from deposition growth rates. The saturation mobility calculated from the $(I_D)^{1/2}$-V_{GS} curve in Fig. 5.16 reached 3.9cm^2/V-s, which is significantly greater than that measured for a surface-channel ZnO TFT of comparable thickness.

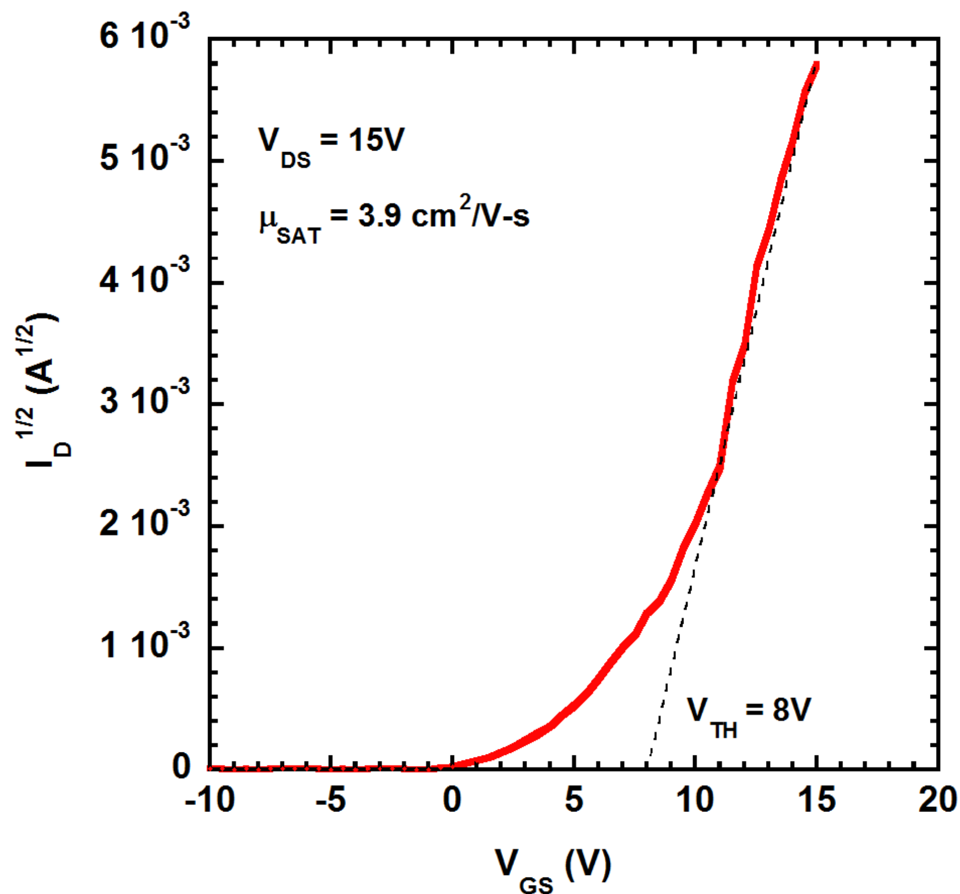


Figure 5.16 Transfer characteristics for a ZnO-$Mg_{0.17}Zn_{0.83}O$ buried-channel TFT at V_{DS}=15V. The increase in the calculated saturation mobility demonstrates a significant contribution due to isolation of the ZnO channel.

5.5 Conclusion

The optical properties of ZnO/MgZnO quantum wells grown by pulsed laser deposition on sapphire substrates have been studied by photoluminescence. The PL spectra of SQWs with abrupt interfaces demonstrate a clear blue shift with increased quantum confinement. A redshift of the PL peak energy for SQW with L_W>9.5nm in comparison to ZnO thin films indicate the existence of small built-in electric fields associated with polarization effects. Small polarization effects are contrary to some previous reports in literature, and may be attributed to defects or potential fluctuations at the well/barrier interface. The quantum efficiency of a 5-layer MQW is comparable to or exceeding that of a high quality ZnO thin film, suggesting that the heterointerfaces do not strongly influence non-radiative recombination. Fitting the integrated PL intensity of the SQWs with a dual activation energy Arrhenius model revealed the existence of two non-radiative mechanisms. Enhanced quantum efficiency, decreased PL linewidth, and higher thermal activation energy was observed for narrower well width and increased quantum efficiency. The anomalous “S-shape” behavior observed in PL peak energy versus temperature is consistent with the thermal activation energy extracted for integrated PL intensity versus temperature, where an activation energy of approximately 4-5meV is obtained and attributed to the trapping of localized carriers/excitons at energy states associated with potential fluctuations at the ZnO/MgZnO interface. This work suggests that ZnO/MgZnO quantum wells with high optical quality may be obtained using physical vapor deposition techniques with enhanced properties associated with quantum confinement, and will serve to further guide efforts to understand the properties of ZnO/MgZnO heterojunctions.

Buried-channel TFTs based on the ZnO/MgZnO heterojunctions were realized and demonstrated a saturation mobility approximately 4cm^2/V-s which was higher than surface-channel counterparts. This was confirmed by a plateau in the C-V curve, illustrating electron confinement in the ZnO buried layer. This suggests the use of this buried-channel approach to enhance carrier transport of polycrystalline ZnO TFT devices.

Chapter VI

COMPLEMENTARY INVERTER BASED ON N-CHANNEL ZNO AND P-CHANNEL ZNTE TFTS

Complementary electronics consisting of thin film transistors (TFTs) exploit this low cost technologies' relevance for enabling logic integrated circuits (ICs). This expands the use of TFTs as an entrenched back-plane pixel driving technology for active-matrix liquid crystal displays (AMLCDs) or active-matrix organic light emitting diode (AMOLED) emissive displays providing large-area coverage and demonstrates its potential use in elaborate digital structures such as ring oscillators, shift registers, and advanced logic gates (NAND, NOR) [102-104] for system-on-panel (SOP) computation on flexible substrates. The CMOS inverter is the basic building block of all digital designs and requires *p*-channel and *n*-channel field-effect transistors. Low-temperature processing of polycrystalline silicon TFTs, in *n*- or *p*-type, has attracted attention due to favorable device performance, thus enabling the realization of CMOS inverters with excellent output characteristics [105,106]. However, additional laser annealing for crystallization of a-Si to obtain high quality poly-Si films is a drawback with regard to fabrication complexity. Organic complementary inverters provide an alternative technology with device characteristics comparable to a-Si TFTs [107], although n-channel organic TFTs are susceptible to atmospheric decay. Recently, hybrid organic-

inorganic complementary inverter structures addressing instability associated with n-channel organic devices by adopting inorganic ZnO for the *n*-channel TFT and more commonly *p*-channel pentacene TFTs have been reported [108].

As discussed in Chapter 3, oxide thin film transistors based on ZnO and InGaZnO have recently received much attention [109,110] due to relatively high carrier mobilities (>5 cm^2/Vs) in comparison to a-Si and organic thin film counterparts (<1 cm^2/Vs). However, these oxide materials are intrinsically n-type due to oxygen vacancies, where p-type thin films are not readily achievable. The work presented in this chapter proposes a new purely inorganic complementary inverter using ZnO and zinc telluride (ZnTe). ZnTe, an intrinsically p-type semiconductor due to zinc vacancies, is an II-VI compound compatible with ZnO that presents an opportunity for integration with n-type ZnO for complementary electronics. While ZnTe electronic devices were demonstrated decades ago [111], little work has been done since then despite the attractive properties of p-ZnTe thin films including relatively high hole mobility (>20cm^2/Vs) and low deposition temperature (200^oC). In this chapter, a p-channel ZnTe TFT is electrically connected with a ZnO TFT to enable demonstration of a complementary inverter circuit.

6.1 ZnTe Characterization and TFT Device Fabrication

The zincblende semiconductor ZnTe is a promising material candidate for the fabrication of green light-emitting diodes (LEDs) due to its direct band gap of 2.3eV at room temperature [112]. Other applications include high efficiency multi-band photovoltaic cells [113] and THz electro-optic emitters and detectors [114]. Known techniques of ZnTe film growth include MOCVD [115], MBE [116], MOVPE [117], and PLD [118]. In this section, the characterization of ZnTe thin films grown by PLD and

MBE and the fabrication of p-channel ZnTe TFTs are discussed. The crystalline quality and preferred orientation of the ZnO films were discussed in Chapter 2.

6.1.1 Characterization of Thin-Film ZnTe

For the ZnTe thin films, molecular beam epitaxy (MBE) and PLD were both used for growth of the ZnTe active channel layers. ZnTe thin film growth by MBE at a rate near 0.3nm/s involved the evaporation of Zn and Te source materials, with the chamber pressure in the 10^{-7}-Torr range, and nitrogen doping using a plasma source at a substrate temperature (T_{sub}) of 250°C. With the substrate held at T_{sub}= 200°C and a comparable deposition rate, PLD proved as a relatively inexpensive alternative method for sequential deposition of ZnTe thin films. The ZnTe films by PLD were deposited under vacuum (10^{-6} Torr) with no intentional doping. ZnTe thin films deposited under these conditions on sapphire substrates exhibit a typical p-type carrier concentration and Hall-effect mobility of approximately 10^{17} cm^{-3} and 5 cm^2/Vs, respectively. X-ray diffraction (XRD, θ-2θ) analysis was used to characterize the crystal structure of the thin films and indicated polycrystalline ZnTe. X-ray peaks at 25°, 42°, and 49.5° corresponding to the (111), (220), and (311) reflections, respectively, are observed on a SiO_2/Si substrate in Fig. 6.1. With considerable increase in the x-ray intensity, the ZnTe film is observed to have a slight (111) preferred orientation.

6.1.2 ZnTe TFT Fabrication Process

The fabrication steps for the ZnTe TFTs are identical to those for the ZnO TFTs, except for the isolation mesa etch chemistry. Bottom gate ZnO and ZnTe TFTs were

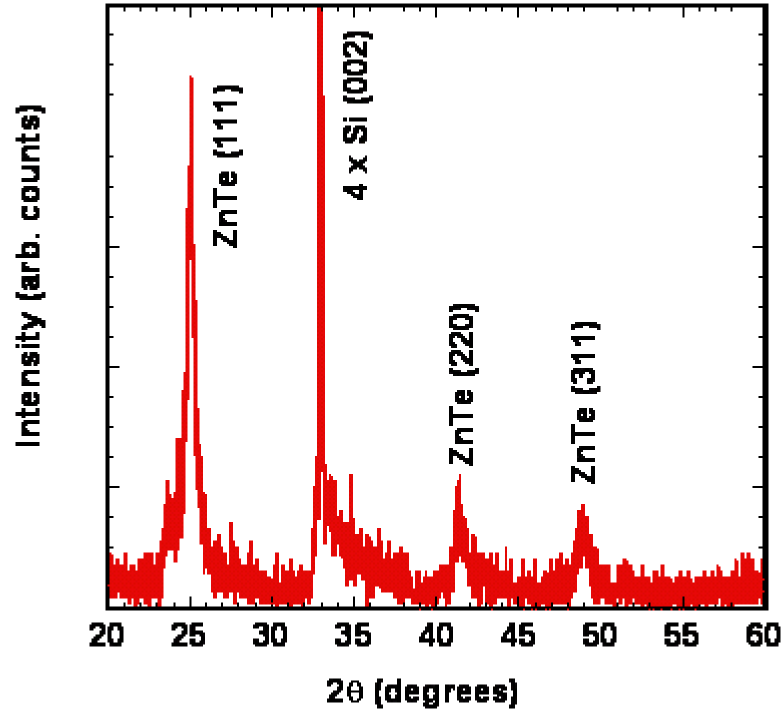


Figure 6.1 X-ray diffraction of the ZnTe film grown by PLD on a SiO_2/Si substrate.

fabricated using highly conductive (p^+) silicon wafers serving as the gate electrode with a 70-nm thermally grown silicon dioxide layer for the gate dielectric. Separate wafers were then used for fabrication of ZnO (n-channel) and ZnTe (p-channel) devices. Polycrystalline ZnO active channel layers 30-nm thick were synthesized by pulsed laser deposition (PLD) using a 248-nm KrF excimer laser to ablate a ZnO target (99.999%) with an oxygen partial pressure of 30mTorr at a rate near 0.3nm/s, as described in Chapter 4.

After deposition of the thin film layers, patterning was performed using AZ1827 photoresist and contact photolithography. Ti/Al/Au (300/300/700Å) and Ni/Au (500/1000Å) electrodes were deposited by vacuum evaporation to form the source and drain electrodes on ZnO and ZnTe respectively. Channel regions were patterned using photolithography and wet chemical etching. An isolation mesa etch, using an etch

chemistry of H_3PO_4: H_2O_2: H_2O (1:1:10) for the ZnTe layer and HCl: H_2O (1:10) for the ZnO layer, was then performed to electrically isolate active device regions. A top-view optical microscope image of the bottom-gate TFT structure used for n-channel ZnO and p-channel ZnTe devices is shown in Fig. 6.2. The schematic cross-section of both, the ZnO and ZnTe, devices have a nominal channel width (W) of 100µm and length (L) of 15µm (Fig. 3.1).

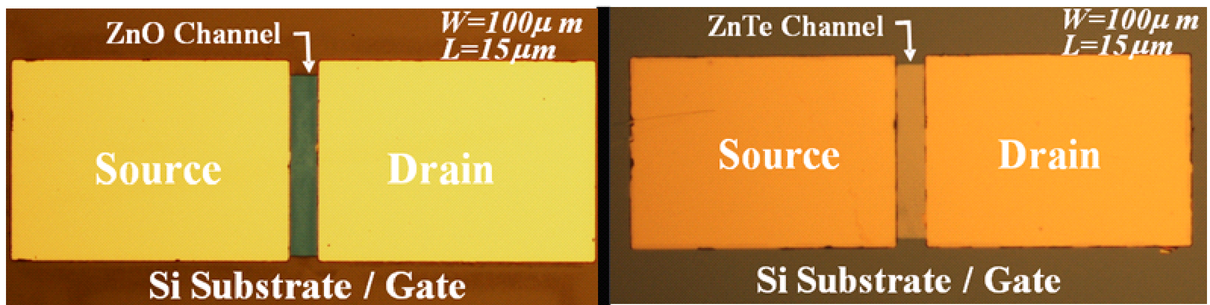
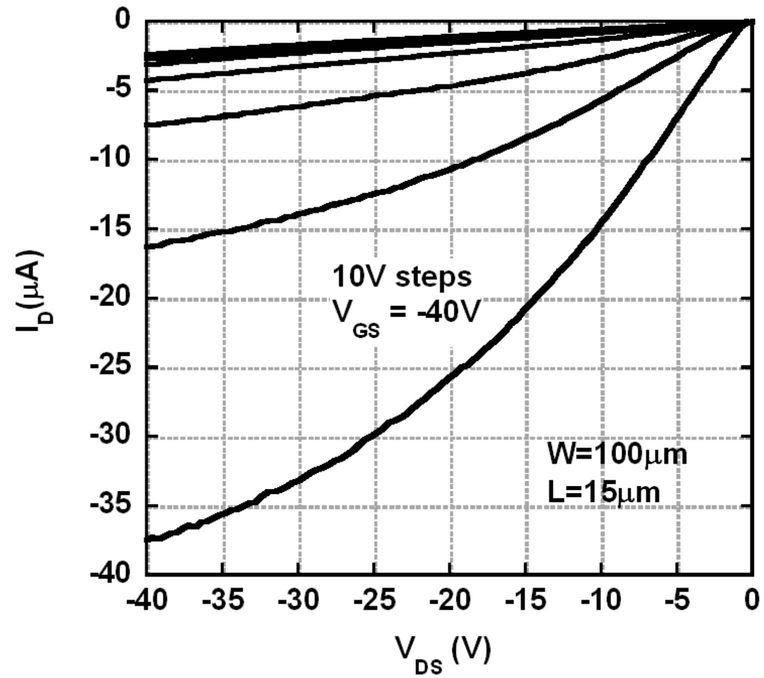


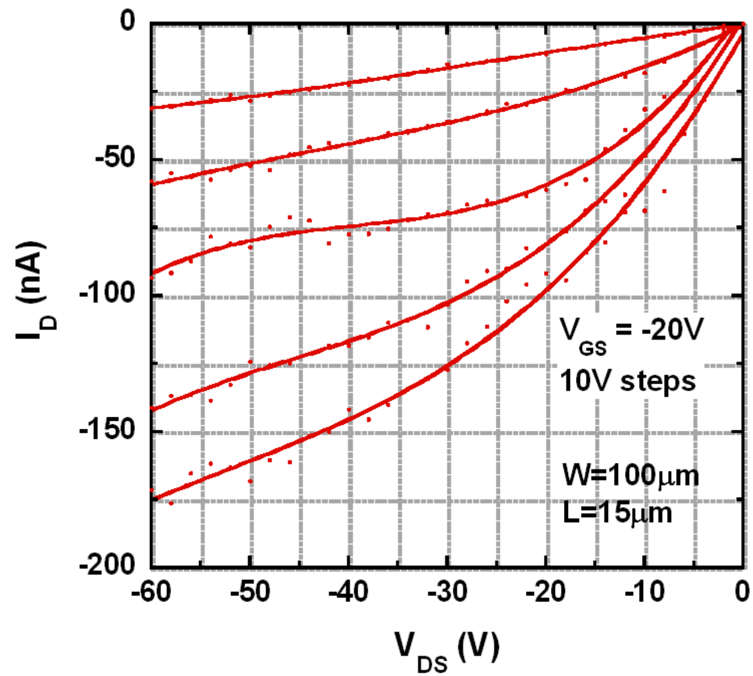
Figure 6.2 Top-view optical microscope image of the bottom-gate ZnO and ZnTe TFT devices.

6.2 ZnTe TFT DC Charcateristics

The *p*-channel ZnTe TFT uses accumulation mode just as the *n*-channel ZnO TFT; therefore, the drain current should be almost zero at zero gate-to-source voltage. This is highly dependent on the conductivity of the semiconductor material forming the active channel layer. However, a negative potential on the gate induces carriers and forms an accumulation layer at the ZnTe/SiO_2 interface in the *p*-channel TFT. Applying a negative voltage across the drain terminal with respect to the source yield the representative drain current characteristics for ZnTe TFTs formed by MBE and PLD with active channels (W/L = 100/15) shown in Fig. 6.3(a) and (b), respectively. Based on Hall



(a)



(b)

Figure 6.3 Drain current-voltage (I_D-V_{DS}) characteristics of a representative ZnTe TFT with the active channel layer deposited by (a) MBE and (b) PLD.

effect measurement of ZnTe thin films deposited simultaneously on sapphire substrates for a thickness of d_{ZnTe}=27nm, a carrier concentration of $N_B \sim 5x10^{17} cm^{-3}$ was measured. In Fig. 6.3(a), the drain current characteristic of the normally-on *p*-channel device has a maximum on-state current of 4μA at V_{GS}=-10V. The current does not drop significantly from V_{GS}=-10V to V_{GS}=0V, when the TFT should approach the off-state. This is directly related to the high conductivity associated with the ZnTe thin films used for the active channel layer of the *p*-channel TFT. This was confirmed by Hall effect measurements of ZnTe thin films on sapphire substrates where conductivity of 3.3 $\Omega^{-1} \cdot cm^{-1}$ was obtained. The ZnTe transistor behavior by PLD has lower current values than the MBE sample as shown in Fig. 6.3(b). Variation of the electrical behavior due to differences in deposition technique is not completely apparent, though the MBE ZnTe TFT because of its superior performance was chosen for connection with the ZnO TFT for realization of the complementary inverter circuit.

Drain current-voltage (I_D-V_{DS}) characteristics of ZnO and ZnTe TFTs for $|V_{GS}|$=15V with 3V steps in voltage are shown in Fig. 6.4. All electrical characteristics were measured in the dark at room temperature with a Keithley 4200 semiconductor parameter analyzer. The drain current characteristics increase linearly at low drain bias and exhibit well defined current saturation behavior from V_{DS}=0-15V for the ZnO TFT. In the case of the ZnTe TFT, non-linearity in the output curves at low drain-to-source voltage (V_{DS} < 5V) is characteristic of large source/drain contact resistance (R_c) which limits device performance [119]. Even so, the p-type channel TFT exhibits gate field-effect with substantial drain current in the off-state, suggesting high conductivity in the ZnTe layers. A maximum current of 4μA was measured for ZnTe TFT.

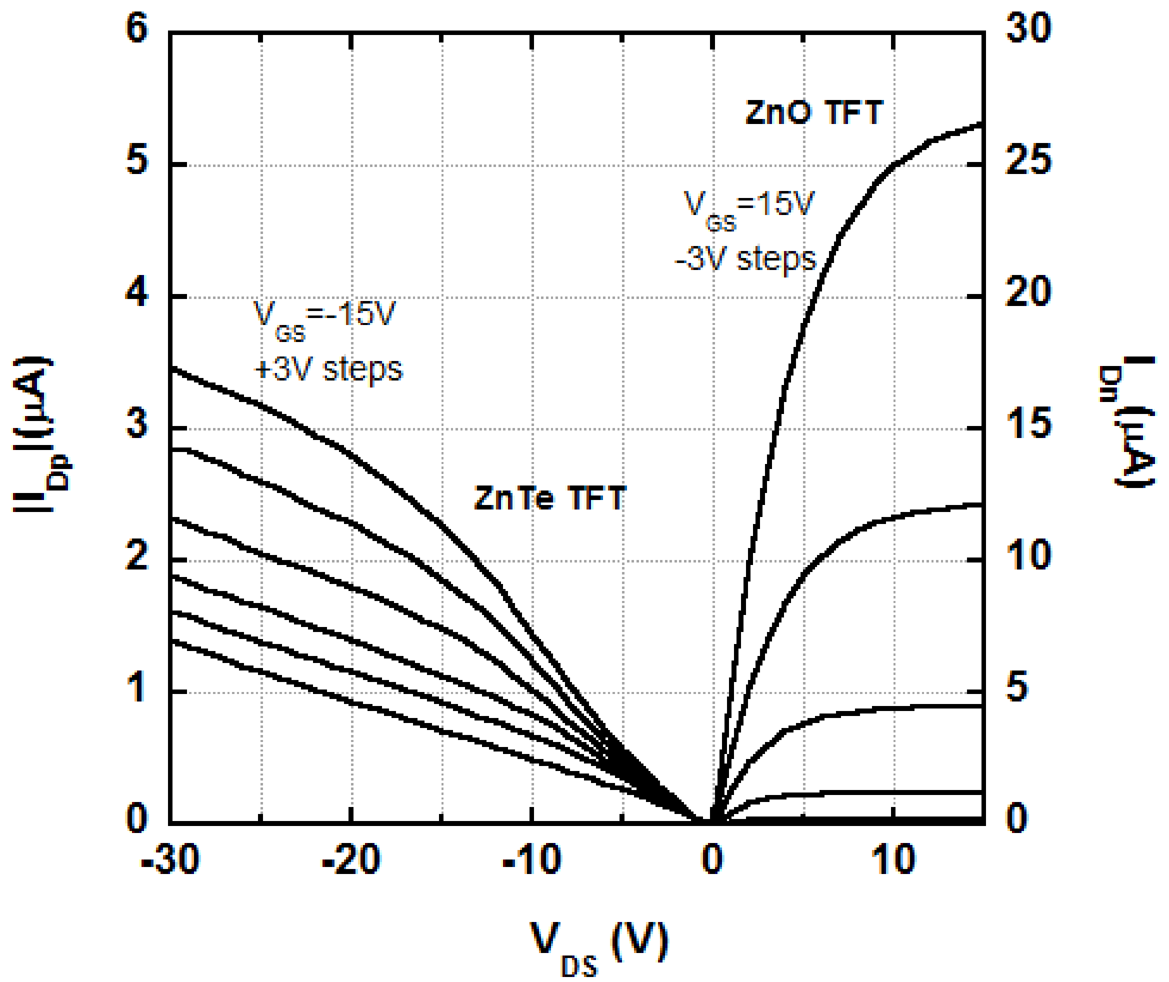
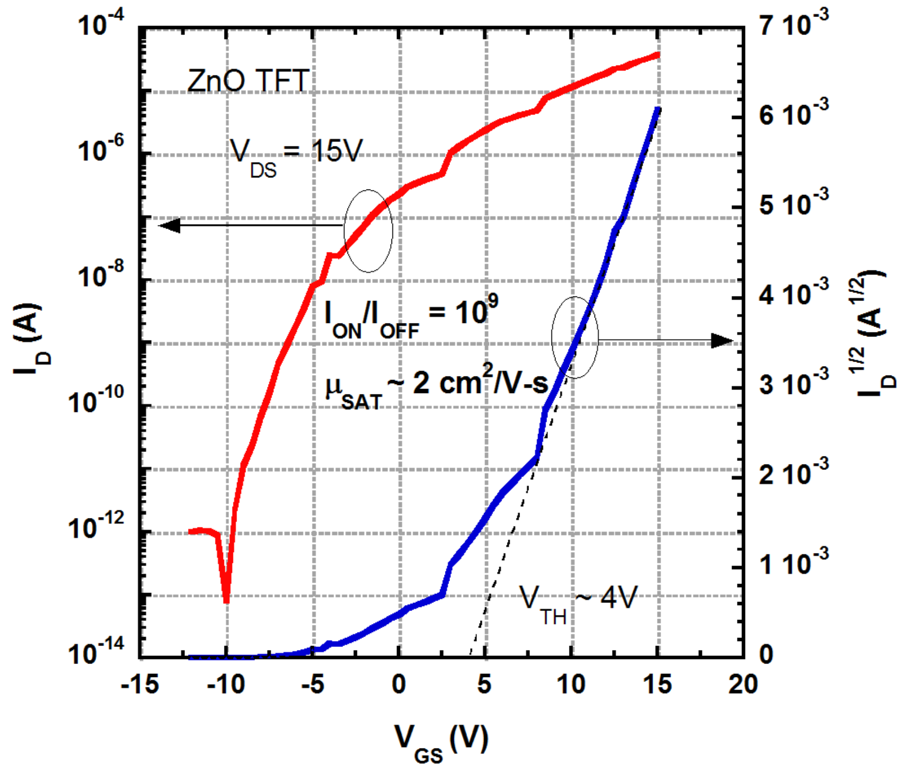
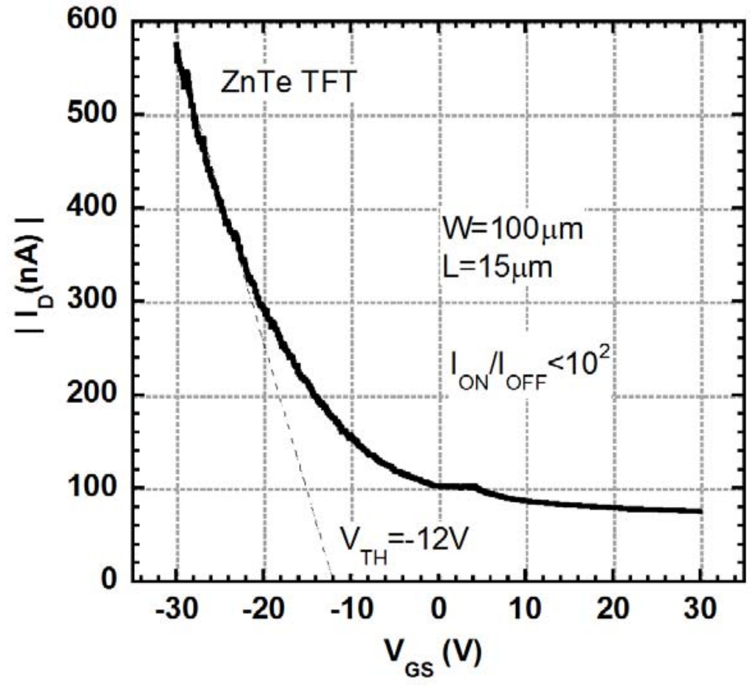


Figure 6.4 Drain current-voltage (I_D-V_{DS}) characteristics of a representative ZnTe (left) and ZnO (right) TFT.

The transfer curves, I_D-V_{GS} and $\sqrt{I_D}$-V_{GS}, for the ZnO TFT and ZnTe TFT are shown in Fig. 6.5(a) and (b), respectively. The threshold voltage (V_{TH}), field-effect mobility (μ_{FE}), and on/off current ratio are all obtained from the expression, $I_D = \frac{W}{2L}\mu_{FE}C_{ins}(V_{GS} - V_{TH})^2$, for the device operated in saturation where C_{ins} (~50nF/cm^2) is the capacitance per unit area of the gate insulator. The estimated saturation μ_{FE} for the ZnO TFT was 1.8 $cm^2/V \cdot s$, while that for the ZnTe TFT is 0.1 $cm^2/V \cdot s$. Significant drain voltage drop across the source/drain contacts due to large R_c (>10^3 $\Omega \cdot cm$) leads to an artificially small value for the extracted field-effect mobility [120]. Moreover, charge trapping at the $ZnTe/SiO_2$ interface suppresses carrier transport in the TFT channel. The on/off current ratios are 10^9 and 10^2 while V_{TH} are 4V and -12V for the ZnO and ZnTe TFTs, respectively. These results support that both TFTs operate as depletion mode (normally on) devices with an off current of 0.1pA in the case of ZnO. Further improvements in device performance are expected to result from contact technology development and higher gate dielectric quality.



(a)



(b)

Figure 6.5 Transfer (I_D-V_{GS}) characteristics for the (a) ZnO and (b) ZnTe TFTs.

6.3 Inorganic Inverter Based on *n*-channel ZnO and *p*-channel ZnTe

6.3.1 CMOS Inverter

A complementary metal-oxide semiconductor (CMOS) inverter is a basic logic circuit which inverts the input logic signal. More advanced combinatorial logic circuits such as NAND gates and NOR gates, essential for logic computation, are based on this basic complementary electronic circuit. The CMOS inverter consists of a *p*-MOS and an *n*-MOS field-effect transistor complementary paired, commonly referred to as the pull-up and pull-down transistors respectively. Modern electronic devices benefit from the low power dissipation associated with this *n*-MOS/*p*-MOS complementary configuration. For the traditional CMOS inverter borne of well established silicon technology, the *p*-MOS and *n*-MOS transistors are on the same wafer. An alternative approach used in this thesis is to electrically connect the *p*-channel TFT in series with the *n*-channel TFT as shown in Fig. 6.6. The two gates of the bottom-gate TFTs are adjoined by placement of both on a conductive stage during testing. Because of this, the input voltage V_{in} is applied to the conducting stage. The two drain contacts are connected together and the output voltage V_{out} is taken at this common drain terminal. The source contact of the *p*-channel ZnTe TFT is connected to V_{DD}, and the source electrode of the *n*-channel ZnO TFT is connected to ground.

A circuit diagram of the complementary inverter based on the p-channel ZnTe and n-channel ZnO TFT is shown in Fig. 6.7(a). The input voltage at the gates, given as

$$V_{in} = V_{GS,n} = V_{DD} + V_{GS,p}, \tag{6.1}$$

sweeps between ground and V_{DD}. First consider the low input voltage when V_{in}=0. The gate-to-source voltage ($V_{GS,n}$) of the n-channel ZnO TFT equals zero which turns it off.

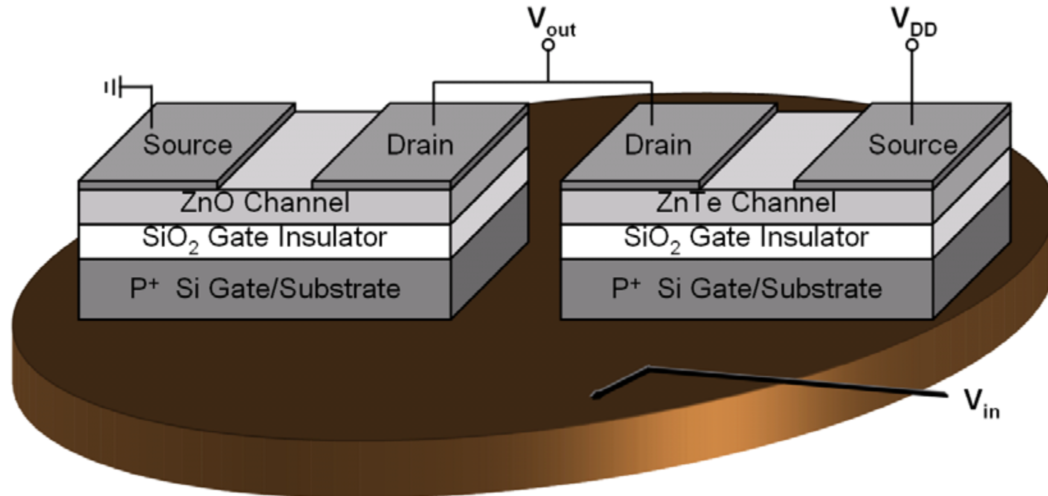
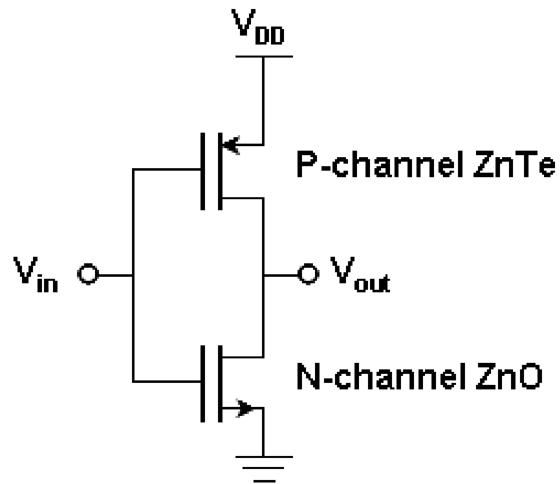


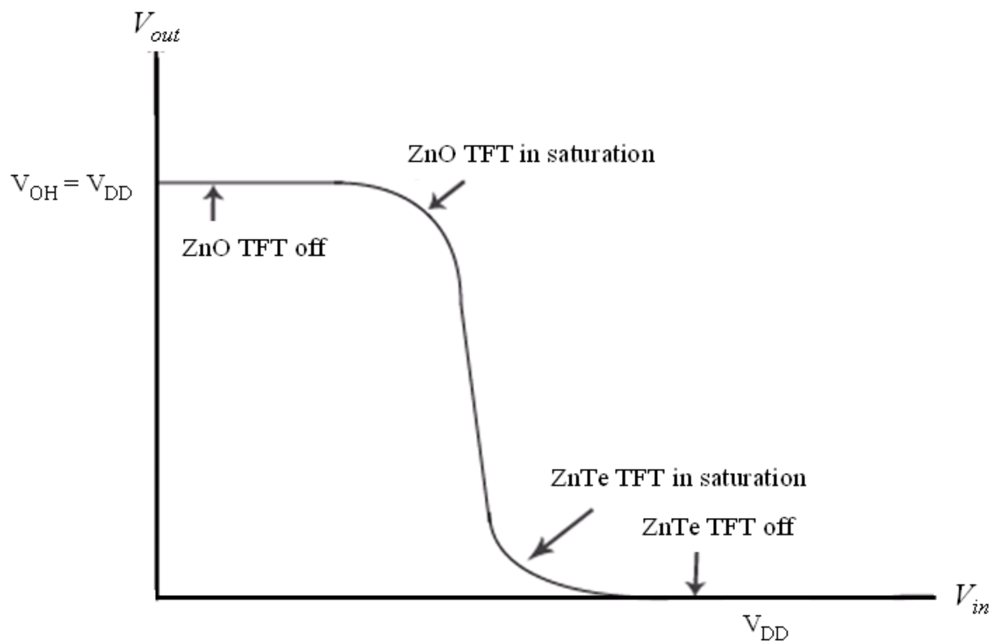
Figure 6.6 Schematic (3-D) view of the the bottom-gate n-channel ZnO and p-channel ZnTe based inverter. The conducting stage of the DC test station serves to apply V_{in} between the two gate contacts.

At the same time, the gate-to-source voltage ($V_{GS,p}$) of the *p*-channel ZnTe TFT is $-V_{DD}$ which turns it on. The conducting *p*-channel TFT pulls the output node up to V_{DD}. However with a high input voltage when $V_{in}=V_{DD}$, the gate-to-source voltage ($V_{GS,n}$) of the n-channel ZnO TFT equals V_{DD} which turns it on. The conducting *n*-channel TFT now pulls the output node down to zero with the gate-to-source voltage ($V_{GS,p}$) of the *p*-channel ZnTe TFT equal to zero which turns it off.

The output voltage as an electrical function of input voltage at the gate is expressed as the voltage transfer characteristic (VTC) ideally illustrated in Fig. 6.7(b). The transition from voltage output high, V_{OH}, to voltage output low, V_{OL}, should be as steep as possible resulting in high gain thus ensuring a fast transition from one logic state to the other: $1\leftrightarrow V_{OH}$ to $0\leftrightarrow V_{OL}$.. Since only one transistor is conducting, there is no static current. Power dissipation occurs only during switching transients when both transistors operate in saturation at $V_{DD}/2$. This final detail explains the unique characteristic of the inverter to enable zero standby power in CMOS circuits.



(a)



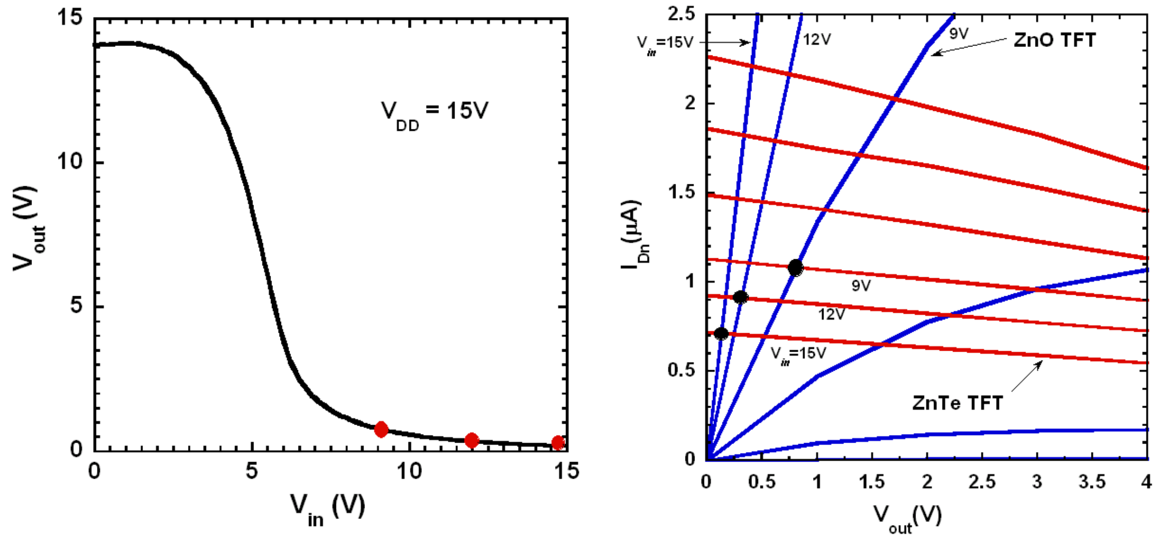
(b)

Figure 6.7 (a) Circuit diagram and (b) idealized voltage transfer characteristic of complementary p-channel ZnTe and n-channel TFT inverter.

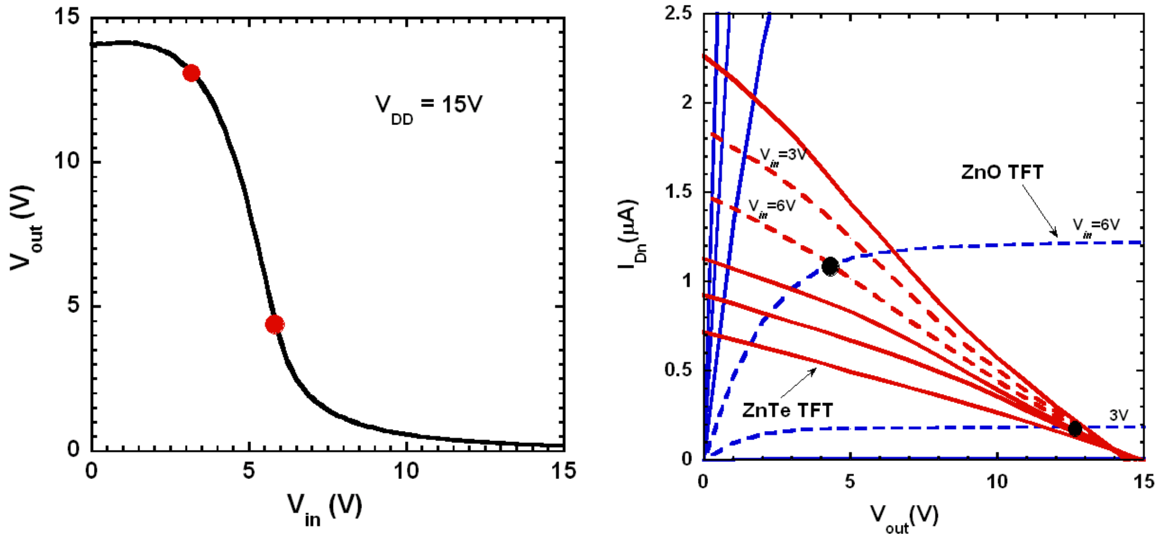
6.3.2 Voltage Transfer Characteristics of *n*-ZnO and *p*-ZnTe Inverter

For the complementary inverter, the drain current of the ZnO TFT must equal the drain of the ZnTe TFT under all static operating conditions. Graphical solution for the VTC of the complementary inverter is therefore possible by mapping the I_D-V_{DS} curves of the ZnTe TFT on those for the ZnO TFT. For arbitrary values of V_{in}, the corresponding value of V_{out} is obtained from the intercept of the two curves, $I_{Dn}=I_{Dp}$. In order to plot high-to-low transition ("rail-to-rail") of the transfer curve, I_{Dn} and I_{Dp} current matching is desired to be symmetrical. However, the drive current for the ZnO TFT is significantly higher than the ZnTe TFT. Load line analysis formed by superimposing the current characteristics of the ZnO TFT and ZnTe device is therefore given for V_{OL} in Fig. 6.8(a) and for V_{OH} in Fig. 6.8(b).

The VTC curve and voltage gain for static operation of the complementary thin-film transistor inverter circuit are shown in Fig. 6.9(a). Inverter behavior is demonstrated with a high output voltage of V_{OH}>14V and low output voltage of V_{OL}<0.2V for a supply voltage of V_{DD}=15V. The transition region gain for the transfer characteristic is found to be $-dV_{out}/dV_{in} > 5$ at a switching threshold of V_{in}=6V. In the case of the high-output state, the inability of the inverter to reach V_{DD} is limited by a turn-on voltage less than zero for the ZnO TFT and to a greater degree the gate leakage current for the ZnTe TFT. Moreover, a switching threshold voltage less than $V_{DD}/2$ suggest the impact of inferior operating performance from the ZnTe TFT. One approach to enhance performance is to design a wider ZnTe TFT for more symmetric I_D in Fig. 6.4. High off current for the ZnTe TFT yields a low-output state greater than zero evident from high inverter current (I_D) for V_{in}=15V, as shown in Fig. 6.9(b).



(a)



(b)

Figure 6.8 Load line analysis and mapping on measured voltage transfer chracteristic (VTC) curve for (a) voltage output low, V_{OL}, and (b) voltage output high, V_{OH}.

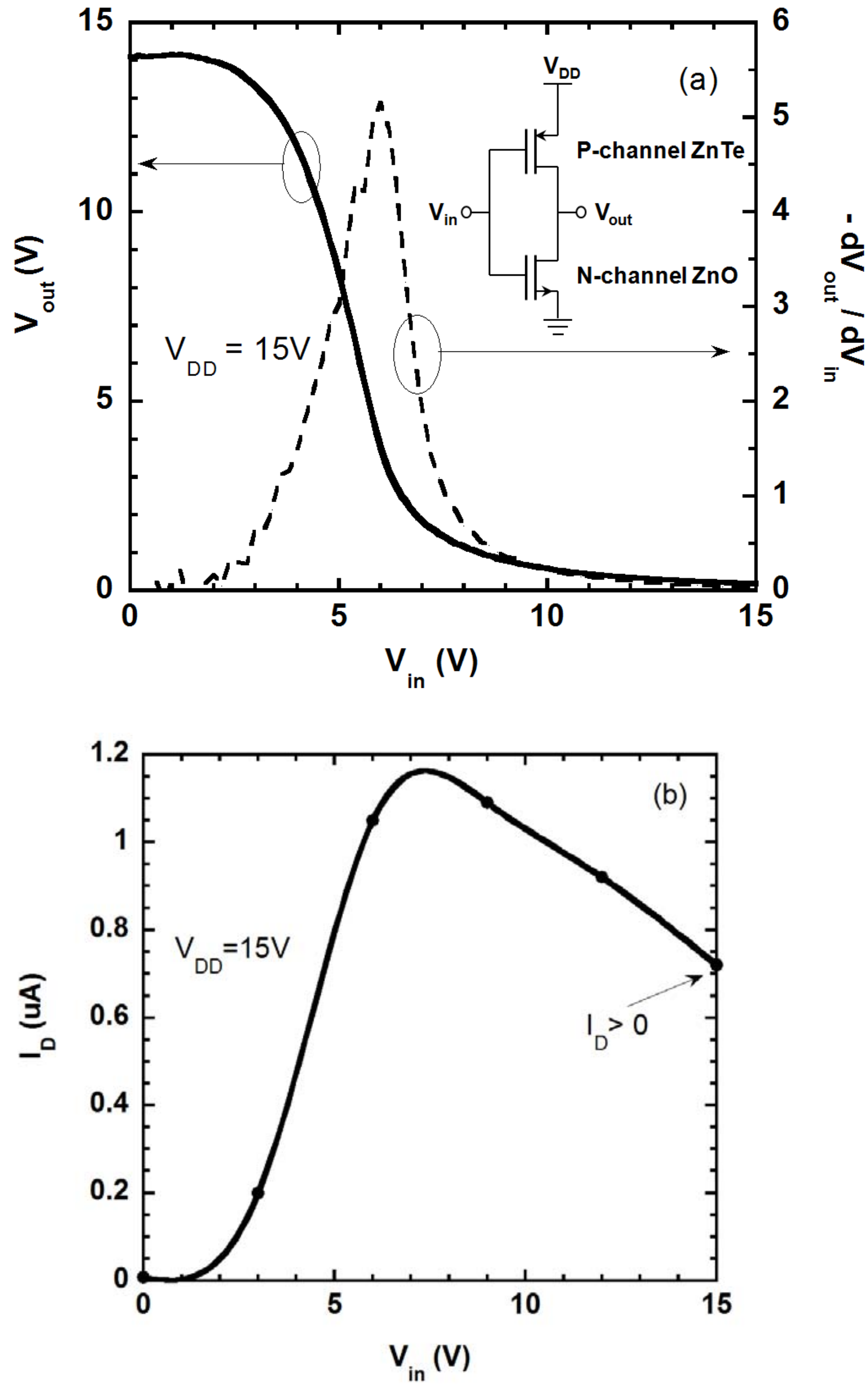


Figure 6.9 Measured voltage transfer characteristic and corresponding voltage gain (a) with switching current (b) of the complementary thin-film transistor inverter with p-ZnTe/n-ZnO channels [121].

6.4 Conclusion

Static inverter behavior has been demonstrated for V_{DD}=15V and $-dV_{out}/dV_{in} \sim 5$ by incorporating ZnTe and ZnO TFTs in a complementary logic circuit. ZnO TFTs exhibited a saturation mobility of μ_{SAT}=2 cm^2/V-s and $I_{ON}/I_{OFF}>10^9$. ZnTe TFTs fabricated by MBE and PLD were demonstrated with $I_{ON}/I_{OFF}=10^2$ limited by high off current and contact resistance. Despite the inferior transistor behavior of the ZnTe device, incorporation of the ZnTe and ZnO TFTs in a complementary logic inverter circuit demonstrates reasonable transfer characteristics. While this initial demonstration of this complementary circuit is believed to be significant, optimization of the doping, contact technology, and gate dielectric of the ZnTe TFTs are expected to provide dramatic improvements.

Chapter VII

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

The work presented in this thesis discusses a qualitative description of ZnO TFT operating principles, the demonstration of buried-channel TFT technology, and its novel application in a complementary logic inverter circuit. Four aspects have been addressed, including material growth and characterization, device fabrication and characterizations, growth and optical characterization of ZnO/$Mg_xZn_{1-x}O$ ($x \leq 0.3$) heterojunctions, and adopting *p*-type ZnTe TFT devices for inorganic complementary electronics. As mentioned in earlier chapters, ZnO TFT devices have demonstrated great potential for replacing entrenched a-Si technology in flexible integrated circuits and ushering in transparent electronics. This work advanced the understanding of fundamental electrical parameters in characterizing ZnO TFT performance, including channel mobility and threshold voltage, and demonstrated application of a buried-channel approach to enhance carrier transport.

The material study of this work concentrated on proper characterizations of ZnO thin films by pulsed laser deposition. Characterization by XRD, AFM, PL, and Hall measurement provided valuable information concerning the structural, optical, and electrical properties of ZnO. By and large, the study provided the optimized growth

condition of thin films and limitations on the background carrier concentration resulting from the naturally occurring defects associated with ZnO.

The device study focused on presenting a qualitative discussion of general *n*-channel (*p*-channel can be substituted by reversing polarities) TFT operation. Key parameters, such as mobility and threshold voltage, were extracted from current-voltage characteristics of ZnO TFTs using conventional gradual-channel approximation techniques. The resulting performance of a 30-nm ZnO TFT demonstrated saturation mobility of μ_{SAT} = 1.8cm^2/Vs, current on/off ratio of $I_{ON}/I_{OFF} > 10^9$, and threshold voltage of 4V. Further improvement in channel mobility and increasing I_{ON} is expected for high carrier concentration and thick channel layers, at the expense of reduced I_{OFF} and degraded drain current saturation behavior. A two-dimensional simulation of the ZnO TFT showed good quantitative agreement with experimental data confirming these findings with varying channel thickness and carrier concentration. Overestimation of the threshold voltage and mobility inaccuracy results from failure to account for the gate-bias dependent mobility. Accounting for these non-idealities of the polycrystalline ZnO TFT, V_{TH} = -8V which turns out to be a better measure as it corresponds to a greater degree with the turn-on voltage. The 30-nm device showed a maximum μ_{avg} of 3.5cm^2/V-s and μ_{inc} of 10cm^2/V-s for V_{GS}=30V.

The optical characterization study was used to examine single quantum wells fabricated from the ZnO/MgZnO material system with a bandedge offset of ΔE_g=0.25eV. A systematic blueshift as a function of decreasing ZnO well width down to 3.2nm resulted in increased integrated intensity. Demonstrations of quantum confinement lead to the application for a buried-channel TFT device structure. The purpose of the isolating

the high-quality ZnO layer from the gate dielectric interface was to enhance carrier transport in the channel region. A plateau in the capacitance-voltage curve denoted spatial confinement of electrons in the channel. The resulting buried-channel TFT exhibited a saturation mobility of 3.9cm^2/V-s. By removing the MgZnO layer adjacent to the source/drain contacts creating a single heterostructure, further improvement is expected in mobility by optimizing the active channel resistivity. This serves as an alternative approach to increase the most important device parameter, mobility.

Finally, a novel complementary logic inverter circuit adopting n-channel ZnO and p-channel ZnTe inorganic TFTs devices was initially demonstrated. The fabrication, circuit configuration, and characterization of exhibited inverter behavior were discussed. The transfer characteristic of the inverter was found to be $-dV_{out}/dV_{in} > 5$ at V_{in}=6V for a supply voltage of 15V. While this initial demonstration of this complementary circuit is believed to be significant, optimization of the doping and channel thickness of the ZnTe TFTs are expected to provide dramatic improvements.

7.2 Future Work

As a continual effort to advance the understanding of operating characteristics of polycrystalline ZnO TFTs, mobility dependence on gate bias $\mu(V_{GS})$ should be incorporated into analytical expressions to model the drain current. The degradation of the mobility is due to the large concentration of traps at the gate dielectric-polycrystalline ZnO interface. The accuracy of the model would require a greater consideration of this interface trap distribution. Useful information from Shockley-Read-Hall modeling of the total area density of grain boundaries in polycrystalline ZnO has been reported [72].

However, there is a degree of uncertainty associated with the controllability of traps when the thin films are formed by physical vapor deposition techniques.

Incorporating the buried-channel approach using ZnO as the buried layer in ZnO/$Mg_xZn_{1-x}O$ heterostructures introduced a viable alternative to enhance electron mobility in the *n*-type TFT channel. The buried-channel TFTs in this thesis were fabricated with double heterostructures. Eliminating the $Mg_xZn_{1-x}O$ layer, with lower conductivity, directly underneath the source/drain contacts of a bottom-gate device would serve to further improve carrier transport. Moreover, improved gate control with high-k gate dielectrics, such as HfO, Al_2O_3 and BST, will advance the performance of the device.

Finally, future studies developing contact resistance technology to ZnTe active-channel thin films and control of ZnTe doping as a function of thickness can provide a valuable contribution to take advantage of this *p*-type semiconductor for TFTs. The use of an improved ZnTe TFT device will advance the initial demonstration of the complementary logic inverter circuit presented in this thesis to provide low-power static dissipation.

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