HIGH DENSITY CROSSBAR STRUCTURE FOR MEMORY APPLICATION

by

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A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical Engineering)
in The University of Michigan
2011

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TABLE OF CONTENTS

List of Figures v
Abstract viii
Chapter
1. Introduction
    1.1 Background 1
    1.2 Resistive Random Access Memory (RRAM) 4
    1.3 History of RRAM Development and Research 9
    1.4 Amorphous Silicon Based RRAM 10
    1.5 High Density Crossbar Memory Architecture 13
    1.6 Vertical Integration of CMOS Circuit and Crossbar Memory 14
    1.7 Organization of the Thesis 16
2. Off-Chip Crossbar Array Development and Characterization
    2.1 Introduction 22
    2.2 Device Structure and Fabrication 23
    2.3 Characterization of High-Density Crossbar Array 25
        2.3.1. 1 Kbits Off-Chip Crossbar Memory Yield Measurement 26
        2.3.2. Prototype 8 by 8 Crossbar Memory Characterization 29
    2.4 Measurement System 31
        2.4.1 Switch Matrix System and Probe Card 33
        2.4.2 PCB Board for the Characterization of Crossbar Array 35
    2.5 Conclusion 38
3. Pillar shaped a-Si Resistive Memory with Inherent Diode Characteristics
    3.1 Introduction and Motivation 40
    3.2 Device Structure and Fabrication 41
    3.3 Switching Characteristics 44

3.3.1 DC Sweep Characteristics 44
3.3.2 Pulse Response Characteristics 47
3.4 Intrinsic Diode Characteristics Verification 47
3.5 Retention Characteristics 49
3.6 Endurance Characteristics 52
3.7 Multi-bit Storage Capability 55
3.8 Conclusion 57
4. On-Chip Integration of High Density Crossbar Array with CMOS Circuits
4.1 Introduction 60
4.2 Device Structure and Fabrication 63
4.3 Engineering of Bottom Electrode for Process Integrity 67
4.3.1 Silicidation Approach 67
4.3.2 Crystalization Approach 68
4.3.3 Metal Induced Crystallization Approach 69
4.3.4 Different Materials 69
4.4 Operation of the Integrated Crossbar Array Chip 72
4.5 Characterization of the Crossbar/CMOS Integrated Chip 74
4.5.1 DC Switching Characteristics 74
4.5.2 Storing and Retrieving Operation with Binary Bitmap Image 77
4.5.3 Storing and Retrieving Operation with Multilevel Bitmap Image 82
4.6 Conclusion 92
5. Development of RRAM Simulation Framework
5.1 Introduction and Motivation 101
5.2 General Model Framework 102
5.3 Filament Growth Modeling and Equation Derivation 103
5.4 I-V Equation and Derivation 108
5.5 Simulation Results and Discussion 110
5.6 Conclusion 113
6. Summary and Further Work
6.1 Development of High Density Crossbar Array and Measurement System 116
6.2 Inherently Rectifying I-V Characteristics of a-Si Based RRAM 117

6.3 On-chip Integration of High-Density Crossbar Array with CMOS Decoder 117
6.4 Development of Simulation Framework for RRAM 118
6.5 Multiple Layers Stacking of High-Density Crossbar Array 118
Appendix 122

LIST OF FIGURES

1.1. 3-D view of resistive random access memory (RRAM).. 4
1.2. Different types of switching characteristics.. 7
1.3. I-V characteristic of two different memory types.. 11
1.4.Schematic of the crossbar memory array and the sneak-path problem 13
2.1. SEM image and fabrication flow of the crossbar memory 24
2.2. Operational schemes for crossbar memory array.. 27
2.3. Yield and On/Off-state current ratio measurement of fabricated off-chip crossbar array 28
2.4. SEM image and program/read operation with 64 bit pattern of 8 by 8 crossbar memory 30
2.5. Measurement system consisting of the Keithley 3706, the NI USB-6259 and a probe card.. 35
2.6. Diagram of the PCB-based measurement system.. 37
2.7. Optical image of the PCB-based measurement system 37
3.1. SEM image and crossection schematic of fabricated pillar-shaped crossbar memory 43
3.2. Linear and semi-log I-V characteristics of pillar-shaped memory 46
3.3. Programming speed test of the a-Si devices 47
3.4. Pulse response of the a-Si device with rectifying I-V characteristics at on-states.... 49
3.5. Retention tests of the a-Si device at elevated temperatures...................................... 51
3.6. Endurance test of the a-Si device... 54
3.7. Multi-bit capability of the a-Si device 56
4.1. Schematic of the sneak path problem and solution for the problem......................... 62
4.2. The complete device structure of the integrated crossbar array............................... 66
4.3. I-V switching curve from SiGe based RRAM showing intrinsically rectifying I-V

characteristics 71
4.4 Retention characteristics of the SiGe-based RRAM.. 71
4.5. Die image of the CMOS decoder circuit.. 73
4.6. Schematic of the program/read schemes... 73
4.7. I-V switching characteristics from 10 different cells in the crossbar array 75
4.8. I-V switch characteristics plotted in log scale demonstrating current suppression at negative bias in the on-state 75
4.9. Threshold voltage distribution from 256 cells in the fabricated crossbar array........ 76
4.10. I-V characteristics of a device in the voltage range of -1 V to 3 V 76
4.11. The original black-and-white 40×40 bitmap image representing the University of Michigan logo 79
4.12. The reconstructed bitmap image from storing and retrieving data in the 40×40 crossbar array 79
4.13. A second test image, which is complementary to the original, to be stored in the array 80
4.14. The reconstructed image from storing the image in Fig. 4.13 in the same array.... 80
4.15. Histograms of the on- and off-state resistances for the data in Fig. 4.12 and Fig. 4.14, respectively 81
4.16. I-V characteristics of a single cell programmed with four different series resistance values (100 KΩ, 500 KΩ, 1 MΩ, 5 MΩ), demonstrating multilevel capability 86
4.17. Histogram of the on-state resistances for the four target values 86
4.18. Measurement diagram for the conventional programming scheme........................ 87
4.19. New measurement diagram that enables multilevel storage in the crossbar array . 87
4.20. Potential distribution without the current-rectifying characteristics at the crosspoints but with the application of external diodes to the unselected electrodes 88
4.21. Simulated potential distribution from the circuit configuration in Fig. 4.19 89
4.22. A color 40×40 test image with 10 different target levels to be stored in the array. 90
4.23. The reconstructed data map from the 40×40 array by storing and retrieving the image in Fig. 4.22. 90
4.24. False-color image of the error for the stored data.. 91
4.25. Histogram of the error values for the stored data 91

5.1. The barrier lowering effects in the presence of electric field and simulated I-V sweeps.....107
5.2. The filament growth and internal voltage across the switch element in series with series resistor.....112
5.3. Simulated multilevel characteristics as function of series resistance value.....112
6.1. (a) conventional crossbar memory array with 1 layer of active devices and (b) multi-stack memory. 120

ABSTRACT

In this thesis study, we utilized two-terminal resistive devices to construct high-density crossbar arrays for memory and logic applications. The performance advantages of the devices using a-Si as the resistance switching layer have been confirmed in this thesis study in terms of switching speed (< 50ns), high on/off current ratio ($> 10^6$), good data retention (> 6years), and programming endurance ($> 10^5$). The resistive memory was further engineered so that the devices can exhibit intrinsic diode-like I-V characteristics at on-state with reverse bias current suppressed to below 10^{-13} A and providing rectifying ratio $> 10^6$. The intrinsic diode behavior can be explained by the motion of Ag ions inside the a-Si matrix and are robust during device operation by surviving $> 10^8$ programming and erasing cycles. The intrinsic rectifying behavior is critical to solving the "sneak path" problem that has hindered high-density crossbar development. Based on these developments, we successfully demonstrated vertical integration of nanoscale crossbar arrays on CMOS circuits. The integrated crossbar/CMOS devices preserved all desired functionalities including low programming current, high on/off current ratio, excellent device uniformity, and the intrinsic rectifying characteristics. Integrated systems composed of a 40×40 crossbar array with 50 nm half-pitch have been fabricated on 180 nm technology node CMOS. For the first time, complex data patterns including binary 40×40 images and "color" 40×40 images can

be stored and retrieved in the integrated crossbar/CMOS system without having to use transistors as current steering elements at each crosspoint inside the array.

We further developed a framework for modeling the resistive switching devices. The modeling involves identifying and solving the filament growth equations together with the metal/insulator/semiconductor tunneling equation that can correctly predict the dynamic resistive switching characteristics including the apparent threshold effect, the dependence of switching time on voltage, and multiple level storage capability. The governing equations were further incorporated into conventional SPICE package and were used to successfully demonstrate several simple circuit operations.

CHAPTER 1

Introduction

1.1 Background

In 1965, Gordon Moore sketched out his prediction of the pace of silicon technology [1]. Decades later, Moore's law still remains firm today. Temporarily, the scaling gets even faster as of April 2011 with the introduction of multi-core CPU [2]. However, many researchers and reports predicted the paradigm will soon be seriously challenged because of fundamental size scaling limits, ever-increasing power consumption, and fabrication cost. Importantly, the field-effect transistor, the main building block of current CMOS technology will be hardly scaled below 10 nm regime because of increasing tunneling current, loss of effective gate control, and increased threshold fluctuations. As the dimension of devices approaches the 10 nm regime, non-transistor device concepts are being seriously studied for next generation electronics. Among several candidates of Non-FET electronics, crossbar architecture based on two-terminal resistive devices has been a main focus among researchers due to its structural simplicity, high storage density and large connectivity. Crossbar structures for electronics have been researched in several research groups including HP [3-6], IBM [7-8], Caltech [9], Samsung, University of Michigan [10-14], among many others. Numerous switching elements for crossbar memory architecture have been proposed. The switching elements

can store information and switch between different states (e.g. 'High-Resistance State', 'Low-Resistance State') by different mechanisms such as conducting filament formation in organic or inorganic materials, or conductivity change due to the redistribution of anions and cations (both types of devices are broadly termed RRAM) [15], phase change of a material from an amorphous state to a crystalline state (PCRAM) [16], and switching of magnetization in ferro-magnetic layers (FeRAM) [17].

The information stored in the switching element can be retrieved by sensing current flow through it in the presence of a read bias. All the proposed switching elements for crossbar architecture have pros and cons while finding an ideal memory system turns out to be quite elusive. For example, PCRAM utilizes localized joule heating and heat quenching to convert the switching materials between the amorphous phase and the crystallization phase. This heating and quenching process involves material expansion and contraction, leading to device fatigue failure [18]. Additionally, the heating requires high power consumption. FeRAM, a device type IBM have been working on for more than two decades, showed very promising characteristics in terms of fast switching (< 20ns) and very robust switching endurance ($> 10^{14}$). However, the fabrication process of this device is not compatible with CMOS and also requires large unit cell area ($>> 10F^2$ where F is the minimum feature size) [19]. For organic memory, the fabrication cost is low compared with other candidates, and easy to be adopted for roll-to-roll processes. However, the yield and reliability of the device is still quite questionable [20]. Here in this chapter, we will review the concept of resistive random access memory and the properties that make it one of the leading candidate with

emphasis on device operation, device terminology, device characteristics, development history, and its integration into high-density crossbar architecture.

1.2 Resistive Random Access Memory (RRAM)

Resistive random access memory (RRAM) is based on two-terminal resistive switching devices with a switching element sandwiched between two electrodes. Under the application of programming voltage, the switching medium turns from a high-resistance state to a low-resistance state. With the reverse of bias polarity, the switching medium can switch back to the high-resistance state. Figure 1.1 shows a 3-D view of a typical resistive random access memory and illustrates the two different resistance states. In this thesis study, we focus on filament-formation based RRAM discussed, in which the on-state is caused by the incorporation of metal clusters inside switching element and the formation of a conducting filament, as shown in figure 1.1 (a). The retraction of the filament leads to the recovery to the off-state, as shown in figure 1.1 (b). Other switching mechanisms, such as resistance change due to redistribution of anions (e.g. oxygen vacancies) in the switching layer also exist but will not be the focus of this study.

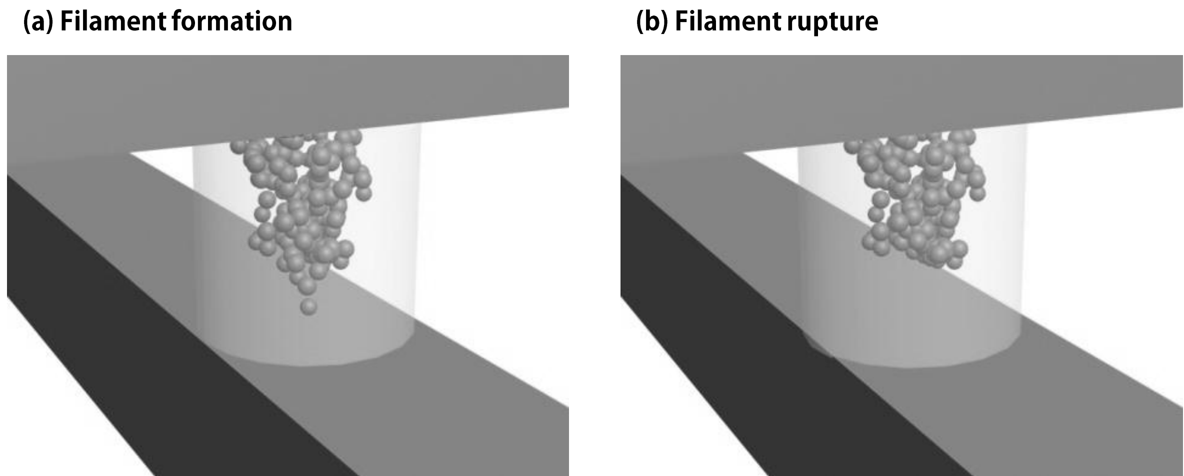


Figure 1.1. 3-D view of resistive random access memory (RRAM). (a) represents the device in the high-resistance state, and (b) represents low-resistance state. The switching element is sandwiched between the top electrode and the bottom electrode. With the application of programming voltage, the conducting filament is formed (a) and the filament can be broken with the application of erase bias in (b).

The switching elements can be composed of a broad range of materials, including chalcogenide materials (e.g. $Pr_{1-x}Ca_xMnO_3$, SrTiO) [21, 22], binary metal oxide materials (e.g. NiO, ZnO, TiO_2, HfO_2) [23-26], solid electrolytes (e.g. AgGeS, AgGeSe) [27] and other amorphous films such as amorphous silicon, amorphous carbon and even polymers. The switching characteristics can be categorized into unipolar switching and binary switching. If the device can be written and erased with one polarity of bias, the device is called "unipolar switching" device. On the other hand, if the device has to be written and erased with different polarities of bias, the device is called "binary switching" device. Regardless of the nature of the switching effect, for RRAM devices the process from high-resistance state to low-resistance state is termed SET process or write process and the oppose process is termed RESET process or erase process. The amount of time that the information is retained is termed as "retention time". The current (or resistance) ratio of the low-resistance state over the high-resistance state is termed as "on/off current ratio" or "resistance ratio".

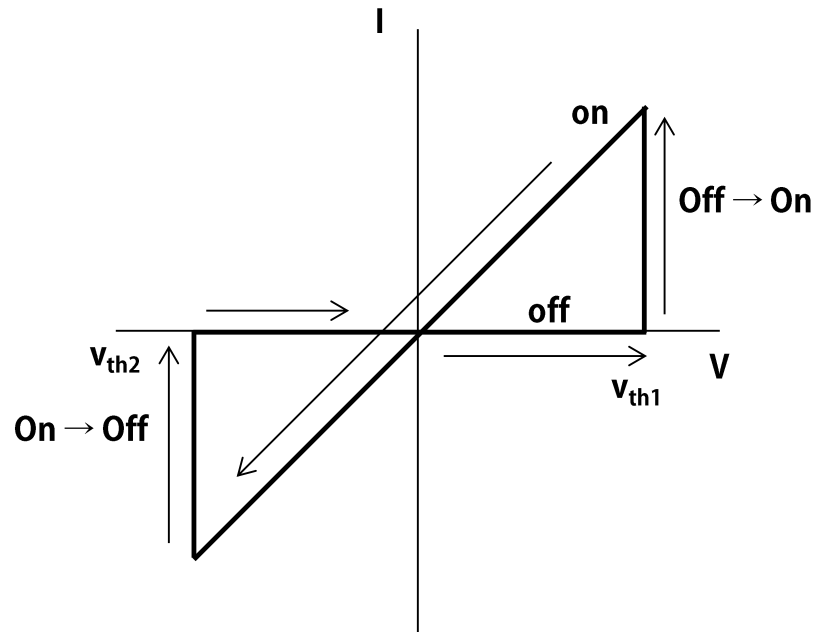
In bipolar switching, the device turns to low-resistance state if the voltage across the device is larger than a threshold voltage V_{th1} which is normally a parameter depending on the device geometry and switching material being used, as well as how the device is programmed, as we will see later. The switching can be very abrupt, as shown in figure 1.2 (a), and makes the device suitable for digital memory applications. After switching, the device resistance becomes low and the on-state can retain its resistance state even without electrical power. In order to turn the device off, a bias with opposite polarity to the write bias needs to be applied to the device. The device can be turned to

the high-resistance state when the bias across the device exceeds an erase threshold voltage V_{th2}.

For bipolar devices, the switching is mediated by the applied electric-field and the formation and destruction of the conduction paths depend on the field polarity. Widely accepted switching models which support field-driven switching include cation redistribution and filament formation [10-14], change of states in trap sites either in bulk [28] or interface [23] of the switching medium, and drift of anions such as oxygen vacancies [25].

In unipolar switching, the write process and erase process only depends on the amplitude of the applied signals but not on their polarity. As a result, thermal effects are typically involved during the switching process [29]. For unipolar device, current compliance has to be applied in order to limit the on-state current and thermal generation during set. During erase the current compliance is removed and the device turns to high-resistance state by flowing large enough current. For most of unipolar cases researched so far, the reset voltage, V_{th1} is smaller than the set voltage V_{th2}, while the reset current is larger than the set current. Usually, unipolar devices suffer from limited endurance cycles due to high on-state current and heating process. The operation window between set and reset voltages can also be limited and accidental erase can occur.

(a)



(b)

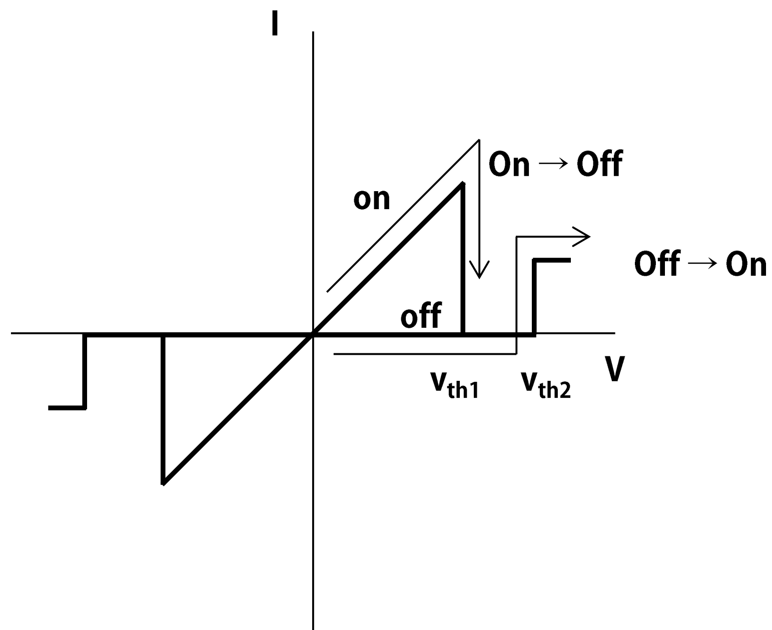


Figure 1.2. Different types of switching characteristics. (a) bipolar Switching (b) unipolar Switching

1.3 History of RRAM Development and Research

In 1962, T.K. Hickmott at General Electric Research Lab first reported that hysteretic current-voltage (I-V) characteristics can be observed in metal-insulator-metal (MIM) structures of $Al/Al_2O_3/Al$, indicating resistive switching occurs as a result of applied electric field [30]. This report stimulates researches on resistive switching devices using different materials. Soon, resistive switching was observed in semiconductor or metallic oxides such as BeO, TiO, NbO [31-33]. The researches in the 1960s were mostly conducted on binary metal oxides [34, 35]. In the 1990s, complex transition metal oxides, such as perovskite-type magnates and titanates, became the focus since the report of switching from $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) [21]. Recently, prototype RRAM devices composed of NiO, TiO, a-Si have been demonstrated by Samsung [23], HP [25], and us [10-14], although the first report on resistive switching in a-Si was published in 1970 [36]. Understanding the switching effect in RRAM devices can be a difficult task because a variety of switching mechanisms may come into play simultaneously. Direct observation of resistance switching is also difficult due to the nanoscale active region that is also covered by the top electrode. Through detailed studies, clear switching mechanisms on specific materials such as NiO, TiO, a-Si based RRAM have now been investigated and established. In addition, the operation of RRAM devices has been recently connected to the generalized memristor (more accurately, memristive device) concept [4, 37-38], and can be used to explain different device behaviors analog vs. digital and guide device modeling and circuit developments.

1.4 Amorphous Silicon based RRAM

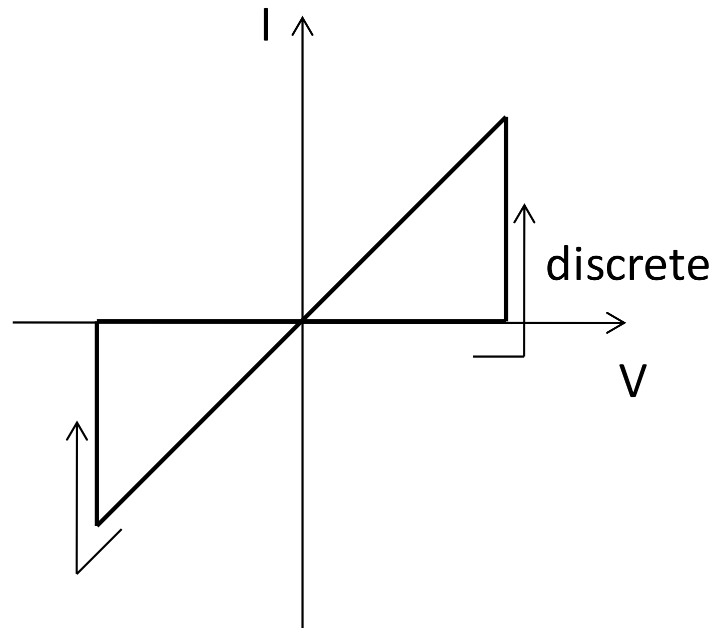
Most of this thesis discusses a-Si based RRAM, which has been shown by our group to exhibit a number of desired properties. The earliest reports of switching in amorphous silicon (a-Si) were published in 1970 [38] contemporaneously with some of the early literature on switching in chalcogenide glasses [39]. These initial investigations studied vacuum-evaporated films of a-Si in the range 0.3 ~ 2.0 μm thick fitted with titanium electrode. Similar observations were made on evaporated films of germanium, boron, and boron plus carbon as well [40-41].

With the development of glow-discharge deposition technique, a-Si of better quality can be deposited. Researchers at the University of Dundee studied metal/p+-n-i/metal devices deposited by the glow-discharge technique with gas-phase doping [42]. Insensitivity of on-state and off-state current between device fabrication batches was observed and exponential switching time dependency on applied bias was also found. Later experimental results have demonstrated a new metal/p+/V (vanadium) a-Si based device which, rather than exhibiting a two-state digital operation, has a continuum of stable states that are nonvolatile and fully programmable by single pulse [43]. This sort of analog memory type has been revisited in recent studies by us [10-14]. For example, in a recent study [10], we showed well-controlled analog-type memory performance by incorporating Ag particle into the a-Si matrix during film deposition. It also showed for the first time that the analog-type memory can mimic the operations of biological synapses.

Figure 1.3 compares digital-type memory and analog-type memory. For the digital-type memory shown in figure 1.3 (a), the switching between off-state and on-state

is sharp and fast. For the analog-type memory, many states can exist between the on- and off-states, and the device conductance can increase incrementally as shown in the figure 1.3 (b).

(a)



(b)

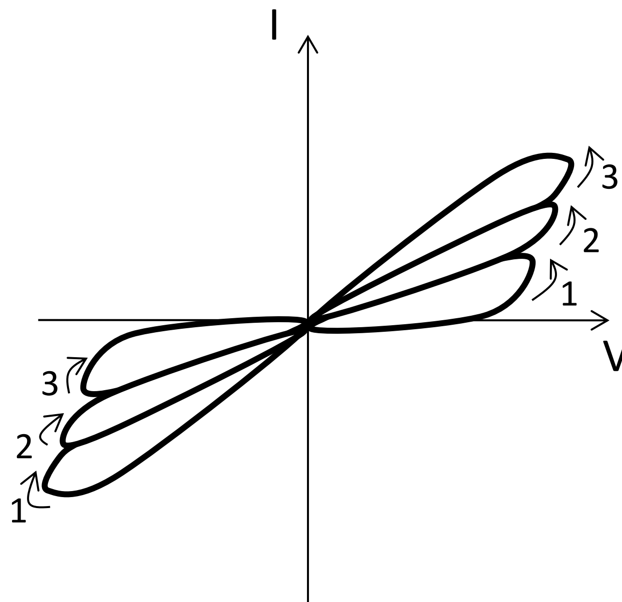


Figure 1.3. I-V characteristic of two different memory types. (a) Digital type memory with abrupt resistance changes. (b) Analog type memory with gradual resistance changes.

1.5 High Density Crossbar Memory Architecture

A crossbar is an assemble of individual two-terminal memory elements formed at the crosspoints between an array of parallel top nanowire electrodes and an array of nanowire bottom electrodes oriented at a right angle from each other, as shown in figure 1.4. Crossbar memory offers several advantages over current memory architecture such as NAND Flash and DRAM, because it has the ideally densely packed-structure which can hold one device with $4F^2$ size (where F is the smallest feature size such as the electrode line width) and it can provide large interconnectivity between the horizontal electrodes and the vertical electrodes in such a way that each memory bit can be programmed or read randomly. For comparison, NAND Flash has a cell size of $5F^2$ and cannot be programmed or read randomly. In principle, 2n inputs can be used to fully control the n^2 memory elements in a $n \times n$ crossbar array, making it attractive for next-generation data storage applications. However, bottlenecks for implementing operational crossbar array with reasonably large size do exist. Besides practical issues such as device reliability and material compatibility with CMOS fabrication, a fundamental bottleneck is the so-called sneak-path problem. Since the crossbar memory has large connectivity between the electrodes, the current path between two selected wires is not always unique, as schematically illustrated in figure 1.4. Here beside the path directly through the selected device, leakage paths represented as the dotted-line through three other devices also exist. If the target memory cell is at high-resistance state, and the three memory cells forming the leakage path are all in low-resistance state, a high current can still be measured through the selected electrodes which will produce an erroneous read signal.

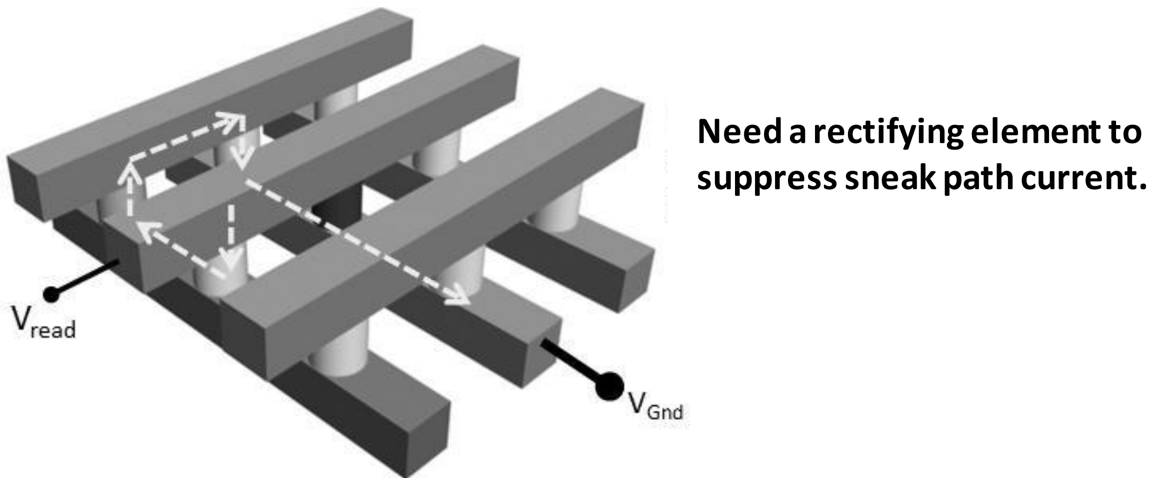


Figure 1.4. Schematic of the crossbar memory array and the sneak-path problem.

1.6 Vertical Integration Crossbar Memory on CMOS Circuit

The device scaling mandate which serves semiconductor industries more than 50 years has began to lose their validity [44]. The highly-scaled transistor and memory fabricated with ever-increasing fabrication cost now faces unexpected trade-off for the sake of increased density. As the device approaches to the 10 nm regime, the transistor have difficulty in turning the channel off, and memory start to see increasing leakage current which deteriorate memory retention characteristics. Therefore, economical and technical motivation for device scaling has been a question mark for the past decade. Researchers and engineers have turned their eyes on vertical scaling such as die-stacking [45], package-stacking, more importantly monolithic transistor stacking [46]. These 3-dimensional integrations of electronic components reduce delay associated with interconnection and communication between transistor, circuit block, chip, and printed circuit board. Also, obtaining smaller form-factor of electronic system has been facilitated with the aid of 3-dimensional integration. In particular, monolithic 3-

dimensional integration has been the focus of research since off-chip 3-dimensioanl integration does not provide fabrication cost reduction or significant system improvement compared with monolithic 3-dimensional integration. Despite all the economic and technical merits of monolithic integration, the wide use of monolithic integration has been hindered by temperature constraint after CMOS back-end process is finished. Therefore, circuits and memory elements with low-temperature process which is suitable for monolithic integration are highly required to be developed. In this thesis study, we succeeded in vertically integrating high-density crossbar arrays on CMOS after solving a number of technical issues such as temperature constraints and material compatibility. The integrated system in fact offers improved performance compared with standalone devices by reducing parasitic effects in the system. Storing and retrieving complex data patterns were successfully demonstrated for the first time with the development of a new programming scheme.

1.7 Organization of the Thesis

In chapter 1, several essential topics and background knowledge for RRAM have been reviewed and explained.

In chapter 2, the device structure and the operation of off-chip, standalone crossbar memory with 1 Kbits and 2.5 Gb/cm^2 will be discussed. The a-Si based devices exhibit high-yield ($> 98\%$), fast-switching (< 50ns), and good endurance ($> 10^6$ cycles). Two different measurement setups which enable multiple I/O pads access have been established and compared with the emphasis on pros and cons of each measurement system.

In chapter 3, pillar-shaped a-Si based RRAM will be discussed as high-density crossbar memory element. The device showed novel switching I-V characteristics with suppressed reverse-bias current at on-state.

In chapter 4, on-chip integrated crossbar memory/CMOS system with 10 Gbits/cm^2 density will be discussed. More importantly, fully operational crossbar memory has been demonstrated for the first time in the integrated system. New operational scheme for achieving multi-level storage capability has been proposed and verified with experimental and simulation data.

In chapter 5, simulation and modeling work on RRAM and other memristor devices will be discussed. The model reproduces experimental I-V characteristics including the apparent threshold effect, voltage-time dependence and multilevel storage. The simulation work also elucidates the physical origin of the resistive switching effects.

In chapter 6, future studies such as 3-dimensional multi-layer crossbar memory stacking have been proposed in order to further improve the storage density for memory and neuromorphic applications.

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Gigabit three dimensional double-stacked multi-level NAND flash memory with shared bit-line structure", *IEEE J. Solid-State Circuits* **44**, 208-216, 2009.

Chapter 2

Off-Chip Crossbar Array Development and Characterization

2.1 Introduction

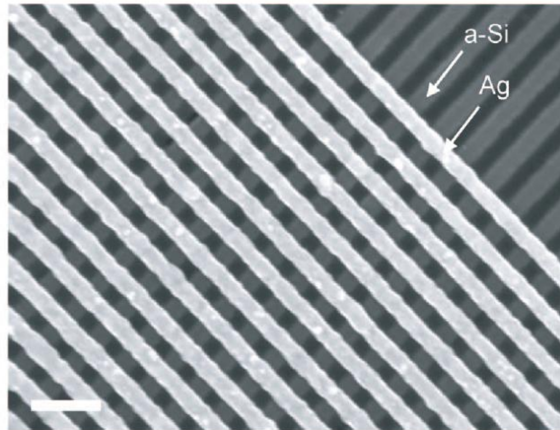
In this chapter, highly scaled a-Si based crossbar array with 1 Kbits and 2.5 Gbits/cm^2 was developed and tested. Crossbar memory structure have been the focus of research as future memory architecture, since its structure enables random access to any single bit in a array without operation latency and 4F^2 memory element packing. If the crossbar architecture combined with non-volatile memory elements can be successfully demonstrated, it would be a promising candidate for universal memory which fundamentally changes the overall memory hierarchy of modern computing system. Over the past 6 years, we have performed extensive studies on the a-Si based RRAM and demonstrated advantages of CMOS process compatibility, fast switching speed, reasonable retention characteristics, and excellent endurance characteristics [1-5]. With the aid of advanced nanotechnology, RRAM with sub 50 nm dimension has been studied and proved to show excellent switching characteristics as a very promising RRAM memory element [4]. In this study, our studies on the fabrication and measurement of off-chip crossbar memory with the a-Si based RRAM will be discussed. The fabricated crossbar memory successfully demonstrated basic functionality of memory array such as write operation, erase operation, and read operation as for the single cell memory case. A

simple word of 8 letters, e.g."CrossBar", was written to the prototype 8 by 8 crossbar memory array and retrieved successfully [5]. Additionally, discussion on the measurement setup for the crossbar memory will be also provided.

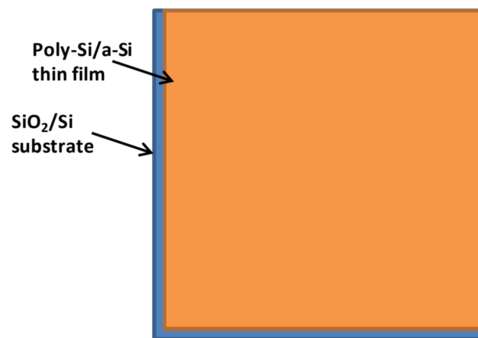
2.2 Device Structure and Fabrication

For the fabrication of off-chip crossbar memory, boron-doped poly-Si and a-Si films were first deposited on a Si/SiO_2 substrate (figure 2.1 (b)). The SiO_2 was thermally-grown from highly-doped p+-type Si substrate. E-beam lithography and RIE were carried out to form poly-Si nanowire electrodes which will serve as the bottom electrodes in the crossbar array. The a-Si switching layer was etched along with the poly-Si film during this process (figure 2.1 (c)). To make ohmic contacts to the poly-Si nanowire electrodes, the a-Si layer at the end of each nanowire was etched away, followed by Pt metal deposition. Spin on Glass (SOG) was coated on the device and cured to planarize the device. Later with the aid of ellipsometry, the SOG thickness was safely reduced to expose the surface of the bottom electrode/a-Si stack. The Ag top electrodes were patterned by e-beam lithography and subsequent lift-off process (figure 2.1 (d)). The active bottom electrode and top electrode were extended to the I/O pads for probe card contact by photolithography process and lift-off (figure 2.1 (e)). Finally, another layer of SOG was deposited and cured on the device in order to protect the Ag electrodes during measurement and storage. Figure 2.1 (a) is a representative SEM image of the fabricated device.

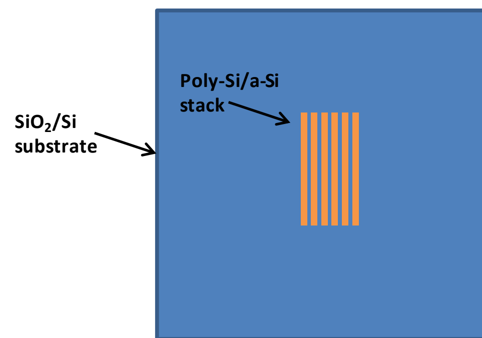
(a)



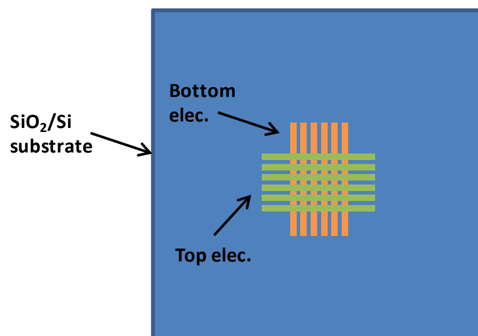
(b)



(c)



(d)



(e)

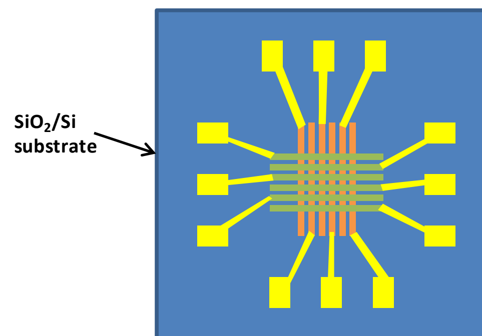


Figure 2.1. SEM image and fabrication flow of the crossbar memory. (a) SEM image of a fabricated off-chip crossbar memory. The scale bar represents 200 nm, (b)-(e) Fabrication sequences for the crossbar memory.

2.3 Characterization of High-Density Crossbar Array

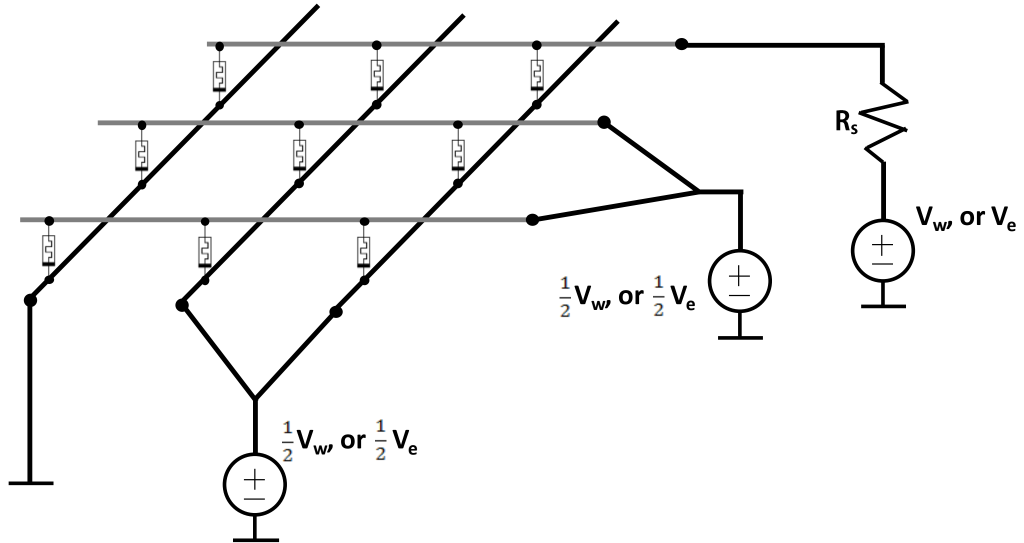
For the characterization of high-density crossbar memory, the voltages applied have to be carefully designed. For the write process, as shown in figure 2.2 (a), a half-voltage protecting scheme is used. In this setup, the write voltage V_{write} is applied to the selected "word line" (e.g. the selected top electrode), and the selected "bit" line (e.g. the selected bottom electrode) is grounded. In the meantime, a voltage with amplitude of $V_{write}/2$ is applied to all the unselected electrodes. Therefore, only the selected device, defined at the crosspoint between the selected word line and the selected bit line, will experience the full write voltage V_{write}, while the unselected devices will experience maximally a voltage of $V_{write}/2$. Specifically, the devices along the selected top electrode will be forward biased with amplitude of 1/2 V_{write} and the one along the selected bottom electrode will be reversely biased with amplitude of 1/2 V_{write}, while all other devices will experience ~ 0 V across them. Considering the programming speed is exponentially dependent on the applied voltage [6], this protective write scheme thus allows only the selected crosspoint to be addressed. For the read process, GND scheme is used in which all the unselected lines are terminated with GND (figure 2.2 (b)). Therefore, sneak leakage current paths as illustrated in figure 1.4 is avoided since cells outside of the selected word line or bit line will experience ~ 0 V and cannot produce large current. However, the GND scheme is only ideal when the parasitic resistance associated with the nanowire bottom and top electrodes is significantly smaller than device resistance. In the worst case considered in this study, the measured resistance of the poly-Si bottom electrode with 150 nm width and 50 nm height is about ~ 7.5 KΩ/μm. Since the spacing between adjacent cells is 300 nm, the line resistance between adjacent cells is approximately 2.25 KΩ. Assuming the

on-resistance of the device is ~ 100 KΩ and the series-resistance effect cannot affect more than 10% of the voltage drop across the devices, the series resistance of the poly-Si electrodes will limit the array to 4×4 (or 8×8 if the electrodes are contacted from both sizes).

2.3.1. 1 Kbits Off-Chip Crossbar Memory Yield Measurement

High density crossbar memories were built to verify the memory element scalability, reliability and reproducibility as well as to test crossbar array fabrication and measurement techniques. A 32 by 32 crossbar memory with feature size F = 100 nm was fabricated that offers 1 Kbits size and 2.5 Gbits/cm^2 density. Although the crossbar array was successfully fabricated and measured, programming of the 32×32 array as a whole was not feasible due to the series-resistance problem discussed in the previous section. As a result, the cells were programmed one by one with the intention to verify the uniformity of the cell performance in such high density arrays. The electrical yield of the 1 Kbits crossbar array was found to be higher than 95% as shown in figure 2.3 (a), (b). More significantly, each bit inside the 1 Kbits array can be addressed automatically with high fidelity using a group of preset write/erase/read programming pulses without having to adjust the programming signals manually, demonstrating the high reliability and uniformity of the a-Si based devices even at this aggressively scaled dimensions.

(a)



(b)

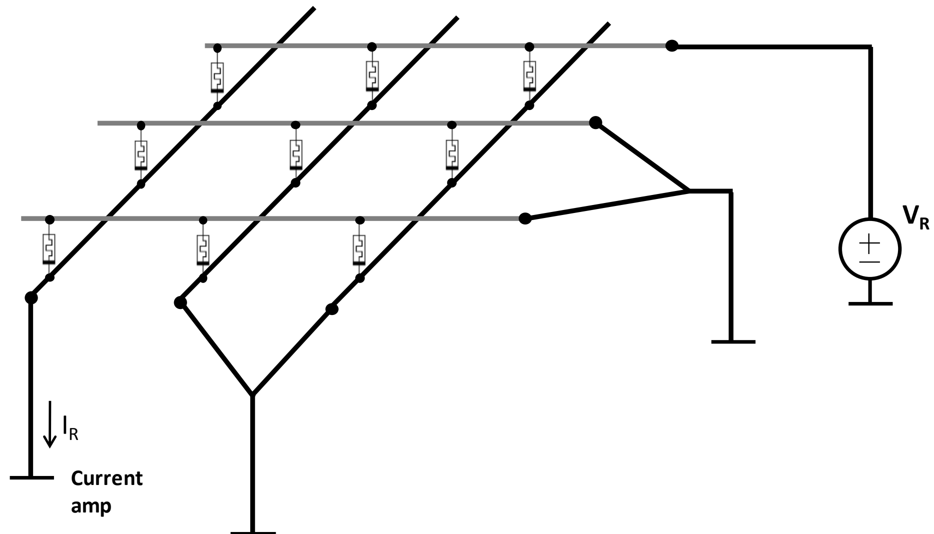
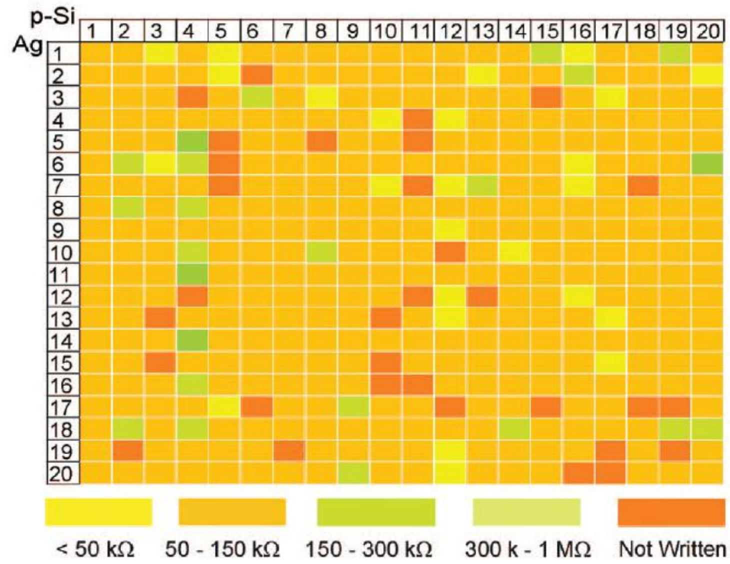


Figure 2.2. Operational schemes for crossbar memory array. (a) write/erase operation (b) read operation.

(a)



(b)

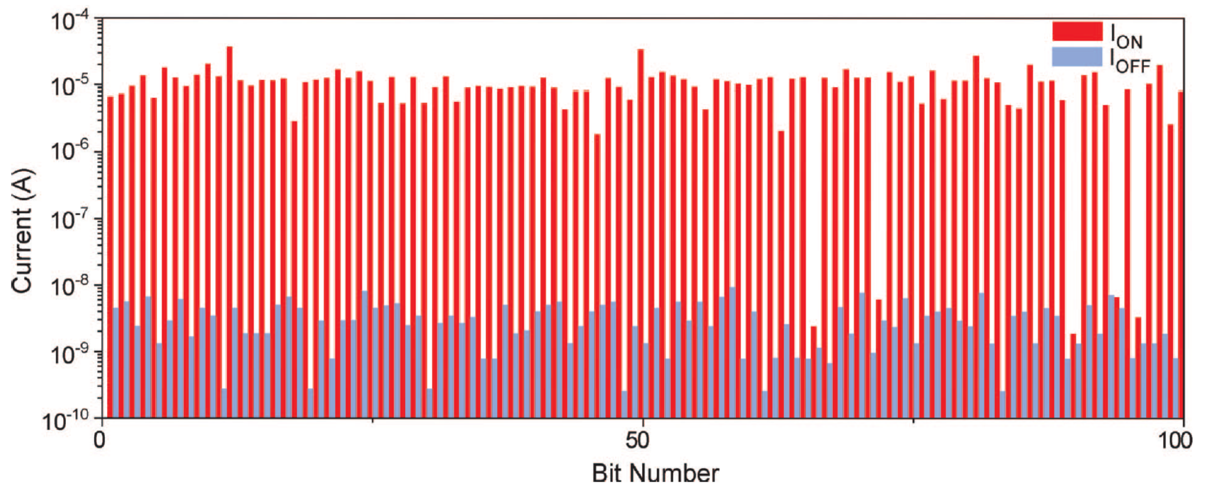
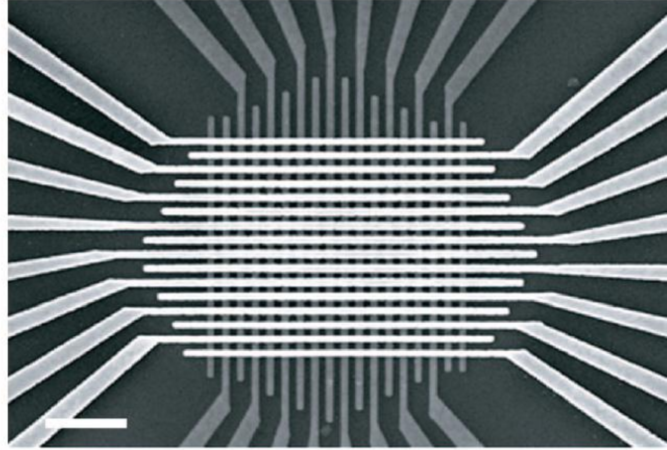


Figure 2.3. Yield and On/Off-state current ratio measurement of fabricated off-chip crossbar array. (a) False color image representing on-state resistance of the cells inside the 32×32 array. The cells were programmed with a uniform pulse of 200 µs 5.5V. Most on-state resistances are in the 50 KΩ ~ 150 KΩ range. (b) The on-state and off-state resistances from the first 100 devices inside the array. The ratio is larger than 10^3 in more than 90% of measured devices.

2.3.2. Prototype 8 by 8 Crossbar Memory Characterizations

To demonstrate the principle of array operation, a smaller 8 × 8 array (figure 2.4 (a)) with contacts at both ends of the electrodes was fabricated to minimize the series-resistance effect. The 8×8 crossbar memory array was programmed and read by using the protective voltage write scheme and GND read scheme discussed earlier. With the 64-bit pattern stored as a whole then followed by retrieval, instead of programming and reading one-cell at a time used for the larger 32×32 array, full functionality of the crossbar memory structure has been demonstrated. The series resistances and sneak path problems are effectively mitigated for the crossbar memory operation with the smaller array size, as discussed earlier. As shown in figure 2.4 (b), the word "CrossBar" can be stored as 64 bits into the 8×8 array. Each letter in the word is represented by 8 bits using the ASCII code and is stored in a row of the array. For example, 'C' is encoded with binary pattern of 01000011 and stored in row 1. Here, binary 0 is stored as the off-state and binary 1 is stored as the on-state in the corresponding device in the array.

(a)



(b)

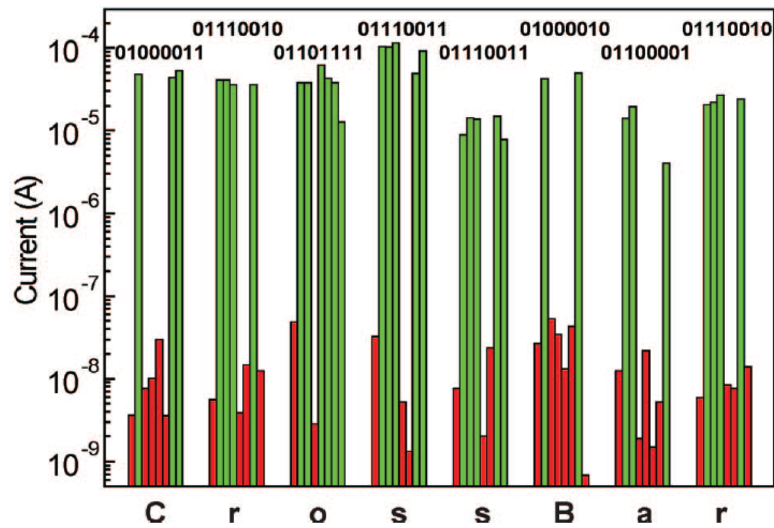


Figure 2.4. SEM image and program/read operation with 64 bit pattern of 8 by 8 crossbar memory. (a) Prototype crossbar memory with 8 by 8 array size. The scale bar is 2 µm. (b) Stored and retrieved bit patterns in the prototype crossbar array. Clearly, on-state and off-state were distinguishable between the two states and the information can be stored in the crossbar array.

2.4 Measurement System

The crossbar memory is a non-standard device in terms of device characterization and no commercial measurement system is configured to systematically test such devices. For simple measurements, a semiconductor parameter analyzer with a low noise pre-amplifier (Keithley 4200) was used for the DC I-V measurements to allow high resolution signal detection. For pulse measurements the programming pulse signals were generated by an arbitrary function generator (Tektronix AFG 3101) controlled by a Labview program. However, for measurement of high-density crossbar memory, the ability to access multiple I/O terminals simultaneously is essential to implement the appropriate programming and read schemes discussed in section 2.3. In this chapter, we discuss two different measurement setups which have been used by us to characterize high-density crossbar memories.

The criteria for assessing the measurement system for crossbar memory operation can are: 1) large bandwidth for high-speed input and output pulse signaling, 2) minimal static charge generation during multiplexing/demultiplexing of the data signals to the electrodes, 3) fast settle time for the configuration to be set, and 4) (optionally) portability of the measurement system. For an ideal measurement system to measure crossbar memory array, on-chip integration of the crossbar array with CMOS decoder and programming/sensing circuitry would be best in terms of fast measurement configuration setup, no-static charge generation, portability, and high speed signaling for input and output without parasitic RC effects. A prototype of the integrated crossbar/CMOS system will be discussed in Chapter 4. Here we discuss the two approaches that can be used to measure standalone crossbar arrays (or partially integrated

crossbar/CMOS systems). None of them satisfies all the criteria for the ideal measurement system. However, each of the measurement system has its own pros and cons.

2.4.1 Switch Matrix System and Probe Card

If portability and bandwidth of the measurement system are not essential, bulky but easy-to-use setups with commercial standalone instrumentations can be used to characterize the fabricated crossbar array. The measurement system that combines a 64-pin probe card and a Keithley 3706 switch matrix mainframe was represented in figure 2.5.

The NI USB-6259 data acquisition system is used for generating programming pulse, erasing pulse, and read pulse. The generated pulse is fed into the input of the switch card which is installed on the back-panel of the Keithley 3706. The Keithley 3706 has input at the back-panel which is called analog backplane. The analog backplane is connected to the inputs of every installed card at the back. By using analog-backplane, the wiring complexity can be reduced with common inputs for each switch card such as V_{write}, GND, and the amplifier port. The Keithley 3706 can hold 6 of 16×6 switch cards. The switch box can take 6 different inputs and route the inputs into any of the 16 output terminals. The fabricated device has 1 Kbits and the number of bottom electrode and top electrode is 32, respectively. Therefore, two switch cards are assigned to address the bottom electrodes and another two are assigned for the top electrodes. The outputs from the Keithley 3706 are applied to the device through a probe card. The probe card purchased from Accuprobe Inc, MA has 64 tungsten probe tips around a round shape hole in the middle of the probe card. The 64 tungsten probe tips are located with spacing of 250 μm. The probe card is held firmly to a holder installed to probe station (MA 150-STN). The signals were applied to the device through the probe tips, and the output current from the target bottom electrode was measured through a trans-impedance

amplifier (DA-1206) through the Keithley 3706 switch matrix. The converted voltage from the measured current is connected to the analog input port (analog-to-digital processor) of the NI USB-6259 data acquisition system. The Keithley 3706 and the NI USB-6259 are simultaneously controlled by custom Labview software through IEEE 488.2 (GPIB) ports.

The measurement setup combined with the switch matrix and the probe card is very useful for the crossbar-type memory, although pad layout for the crossbar memory has to be matched with the probe card design. There are several limitation and concerns when the switch matrix is used for the crossbar memory. The mechanical switch in the switch cards can generate static charge and sometimes erase the information stored in the memory elements. Also, the switching action is limited to hundreds of milliseconds due to the slow communication speed of IEEE 488.2 standard (GPIB), although the actual switching time of the mechanical switch is about 24 milliseconds (which is still not fast enough for high-speed testing, e.g. long endurance tests).

The 1 Kbits array and the 8 by 8 prototype array were tested by this setup with a typical programming pulse of 200 μs and 5.5 V. I_{ON} and I_{OFF} of each bit inside the array were measured with a current amplifier (Keithley 6485) at a read bias of 1.5 V.

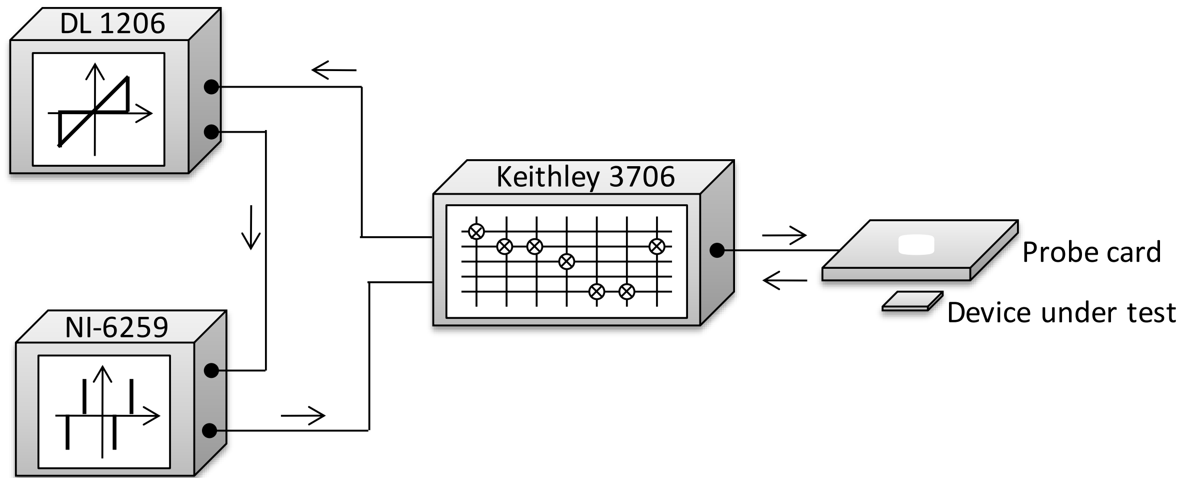


Figure 2.5. Measurement system consisting of the Keithley 3706, the NI USB-6259 and a probe card.

2.4.2 PCB Board for the Characterization of Crossbar Array

Rather than using bulky commercial equipment as the test setup, compact PCB-type measurement board was also developed to improve the portability and overall speed of the system. Figures 2.6 shows schematics of the PCB based measurement system, which comprises micro-controller (atmega128), crosspoint chip (AD8113), analog switch (ADG 1411), multiplexer (ADG 406), and de-multiplexer (ADG 406).

The overall system (optical image shown in figure 2.7) operation is described below: The microcontroller (atmega128) controls all the components in the PCB board. The microcontroller can communicate with a PC through RS-232 serial communication. The user interface through custom Labview software can take input parameters from the user and generate digital codes and send them to the micro-controller through RS-232 serial communication. Then, the microcontroller takes the digital codes and decodes them

and generates control I/O signals for the different components in the PCB board. For example, the user selects the desired bottom electrode and top electrode (which in turn determines one target device) and also defines the write pulse amplitude and width. Based on the user input, the Labview software generates 23 bytes (the first byte represents command code (whether write, erase, read), another 10 bytes represent I/O signal for one crosspoint chip, and the next 10 bytes represent the other crosspoint chip, and two bytes represent how long the pulse is.) The binary codes with 23 bytes in total are then transferred through serial communication with transfer speed of 9660 bits/sec. Once the micro-controller receives the data and saves the code in the embedded memory sitting inside micro-controller, it then sends the control I/O signals for the various components on the board based on the received information.

The USB-6259 feeds the write pulse, erase pulse, and read pulse to the input of the AD8113 which is connected to the top electrode. Instead of using probe stations and a probe card, here the fabricated device is wire-bonded to the 40 pin DIP chip carrier and plugged into a DIP socket on the PCB board. The 16:1 MUX sets the path between the selected bottom electrode and the outside current amp. The 1:16 DEMUX selects the series resistor from 16 possible values so that the device under test can be programmed with different series resistance values to control the programming current and allow for multi-bit storage. Finally, the signal from the device can be fed into an external current amplifier through the SMA connector.

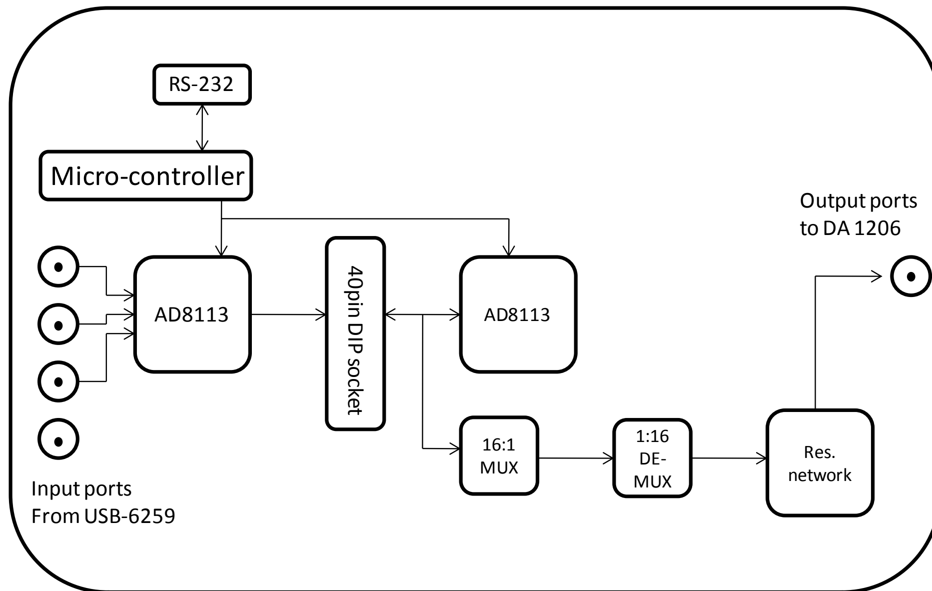


Figure 2.6. Diagram of the PCB-based measurement system.

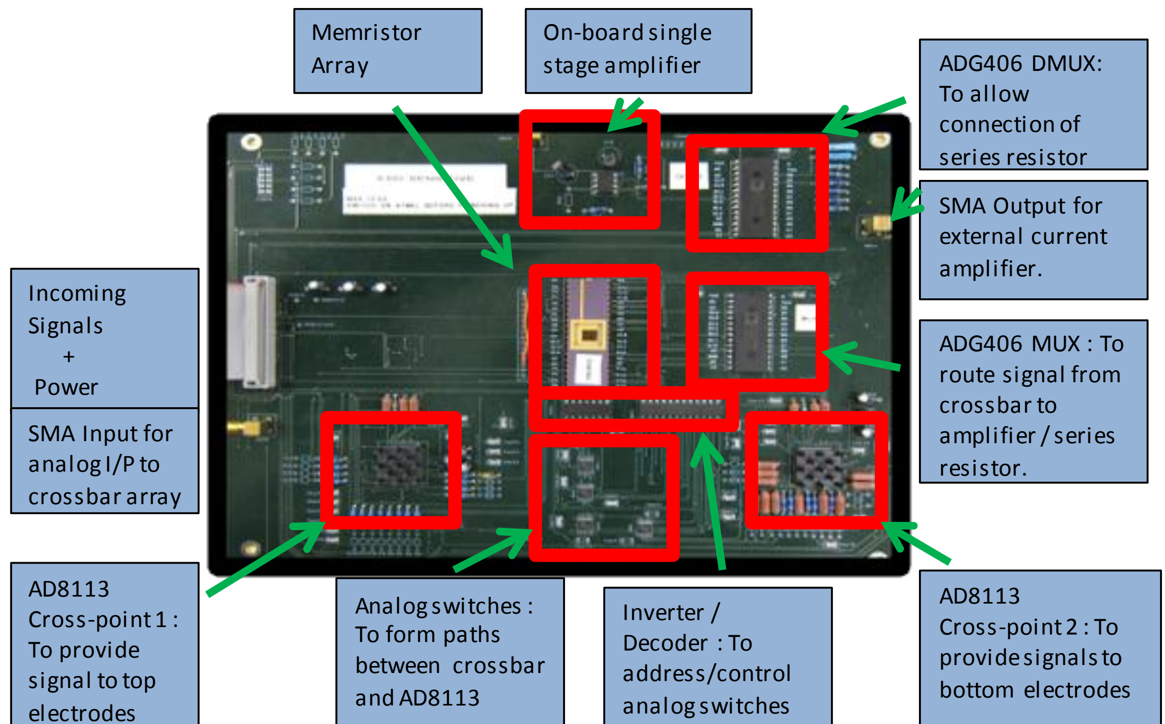


Figure 2.7. Optical image of the PCB-based measurement system.

2.5 Conclusion

In this chapter, our attempts to fabricate and test standalone high-density crossbar memories were discussed. To address the crossbar array, complex operational schemes, such as protective write scheme and GND read scheme need to be employed. The measured data from a prototype 8 by 8 crossbar array verified these write and read schemes. Two different measurement setups have been developed for high-density crossbar memory measurement and the pros and cons of these approaches are discussed. Still, both of the measurement setups have room for improvements. However, the best approach for testing high-density crossbar memory without suffering from RC-delay and static charge issues will be using on-chip, integrated decoder circuits. In chapter 4, a prototype integrated system with on-chip decoder circuits will be discussed.

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Chapter 3

Pillar shaped a-Si Based Resistive Memory with Inherent Diode Characteristics

3.1 Introduction and Motivation

In the previous chapters, we have discussed the basic operations of crossbar structures and their potential applications such as high-density resistive random access memory RRAM, programmable logic, and adaptive neuromorphic circuits [1-4]. For practical applications of the crossbar structure, however, crosstalk due to sneak path originated from reversely biased cells has to be suppressed [5]. So far, a few groups have reported using PN junctions and Schottky diodes in series with the resistive switching device in the so-called 1D1R approach to suppress crosstalk [6-7]. However, besides performance and integration issues it has been noted nanoscale diodes may lose their rectifying behavior below the 50 nm range due to enhanced tunneling effects [8]. In addition, the 1D1R structure is only compatible with so-called unipolar switches that can be turned on or off using just positive programming voltages. In this case the serially connected diode can remain forward-biased during programming to prevent voltage loss for the resistive memory device. For bipolar resistive switches memristors which require a negative bias voltage to switch the device off the 1D1R approach is thus inapplicable. These problems make addressing crosstalk a difficult challenge, particularly for high-density memory and logic systems. In this chapter, a resistive switching device which

offers intrinsic current-rectifying I-V characteristics at on-state is studied. In addition, a metal electrode was placed adjacent to the poly-Si electrode to reduce the series-resistance problem discussed in Chapter 2.

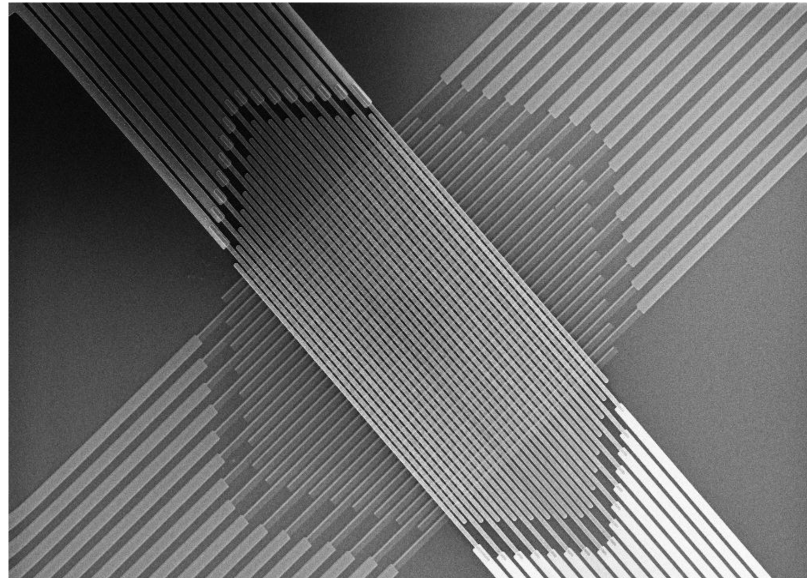
3.2 Device Structure and Fabrication

The device structure consists of a nanoscale pillar shaped a-Si switching layer capped with a Ag top electrode and a degenerately doped poly-Si bottom electrode. Briefly, the 150 nm thick poly-Si layer was first deposited and doped with solid boron source, followed by native oxide removal by hydrofluoric acid and baking at 130 °C. Undoped a-Si was deposited at 400 °C by plasma-enhanced chemical vapor deposition (PECVD). Care was taken during the poly-Si native oxide removal, baking, and the a-Si deposition processes to ensure the quality of the poly-Si and a-Si interface. The a-Si/poly-Si stack was then patterned through e-beam lithography and etching processes to form isolated nanowire electrode patterns. The active a-Si layer was further patterned into the nanoscale pillar structures with 100 nm diameter. The poly-Si electrodes and active a-Si pillars were isolated by spin-on-glass SOG and the final height of the a-Si pillars was controlled to 50 nm by using a high density plasma etcher with Cl_2 and O_2 gases mixture. Finally, Ag top electrodes were formed to cap the surface of the exposed a-Si pillars by e-beam lithography and lift-off processes.

Figure 3.1 (a) shows a 16×16 array of such devices fabricated using the processes discussed above. Figure 3.1 (b) shows a cross-sectional schematic of the device array illustrating the two-terminal device structure consisting of the active a-Si pillars buried in

SOG and sandwiched by Ag top and poly-Si bottom electrodes. An auxiliary side electrode of NiCr/Au (50 Å/350 Å) has also been incorporated next to the a-Si pillar structure to reduce the series resistance associated with the poly-Si bottom electrodes.

(a)



(b)

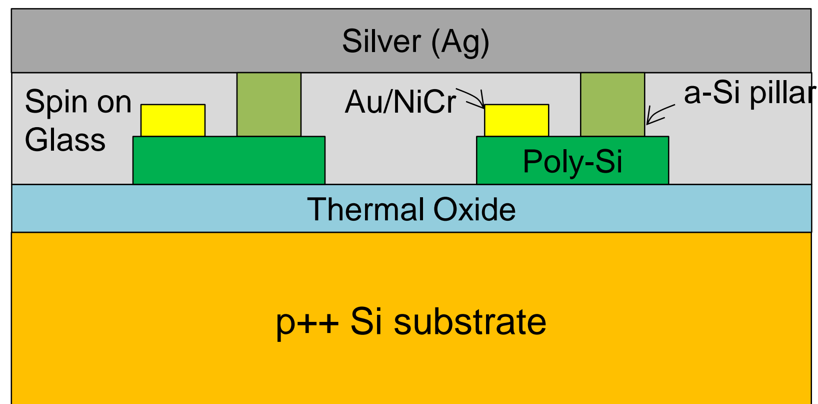


Figure 3.1. SEM image and crossection schematic of fabricated pillar-shaped crossbar memory. (a) Top view of the as-fabricated 16×16 crossbar array with a-Si based RRAM device. (b) Cross-section schematic of the device structure showing a-Si pillars isolated by SOG and the side electrodes to reduce series resistance.

3.3 Switching Characteristics

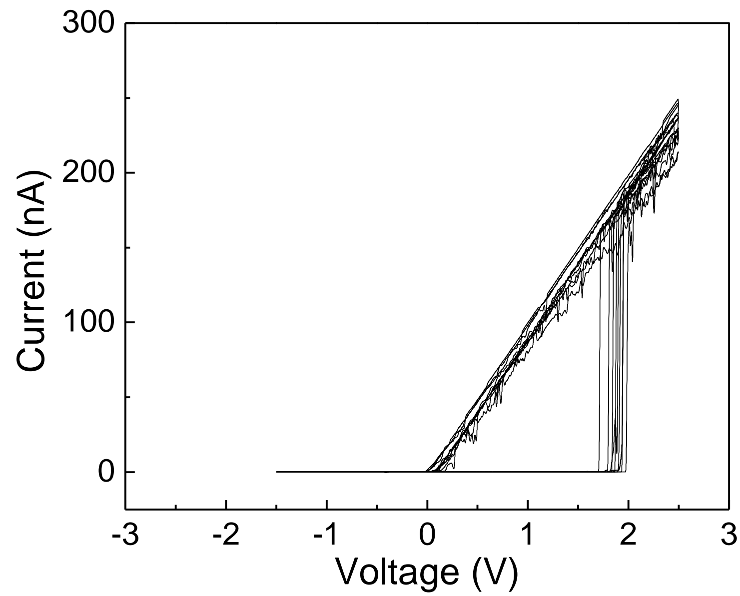
3.3.1 DC Sweep Characteristics

All measurements reported here were taken from devices in an array similar to that shown in figure 3.1. Figure 3.2 (a) shows ten consecutive switching curves of an as-fabricated device demonstrating the tight distribution of the threshold voltage V_T and the absent of high-voltage forming process for these devices. Unless listed otherwise a current limiting resistor of 10 MΩ was connected in series with the device during the write process to prevent damage due to excessive current, and no series-resistor was used during the erase and read processes. The lower threshold voltage of 2 V compared with our earlier studies 3.5 V (devices described in chapter 2) and the elimination of the forming process is likely due to improvements in the device fabrication control.

Interestingly, the device in figure 3.2 (a) shows a well-defined current-rectifying, diode-like behavior — even in the on-state current can only flow through when the device is at positive bias. This behavior is more evident in the inset to figure 3.2 (b) which plots the I-V data in semi-log scale. The reverse current is suppressed to be 10^{-13} A giving a rectifying ratio of 10^6 at 0.5 V. An on/off resistance ratio of 10^6 can also be obtained at the read voltage of 0.5 V. The I-V characteristics can thus be modeled as a 1D1R structure incorporated into a single two-terminal device and can be used to suppress sneak current paths in crossbar memory arrays. As already shown in figure 1.4, any sneak path will involve at least one reverse-biased cell, thus by employing cells with the current-rectifying characteristics the sneak paths can be blocked. The size of the crossbar array that can be accommodated depends on the rectifying ratio. Since in the worst case there are $(M - 1) \times (N - 1)$ potential sneak paths in a $M \times N$ crossbar array,

having a very large rectifying ratio as demonstrated here will be extremely valuable for practical applications with large-scale arrays. We note that at small reverse bias the device still remains in the on-state even though the current is suppressed, as can be verified from subsequent read operations, as discussed in chapter 3.4.

(a)



(b)

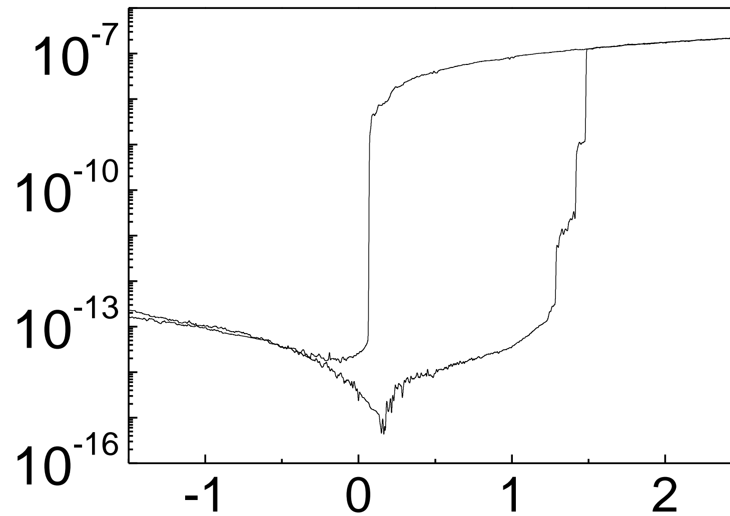


Figure 3.2. Linear and semi-log I-V characteristics of pillar-shaped memory. (a) 10 consecutive I-V sweeps of the device, including the forming process. The distribution of V_{th} for the device is very tight. (b) I-V plotted in semi-log scale highlighting the intrinsic diode-like characteristics at on-state.

3.3.2 Pulse Response Characteristics

The devices can be reliably programmed with 100 ns write/erase programming pulses as shown in figure 3.3.

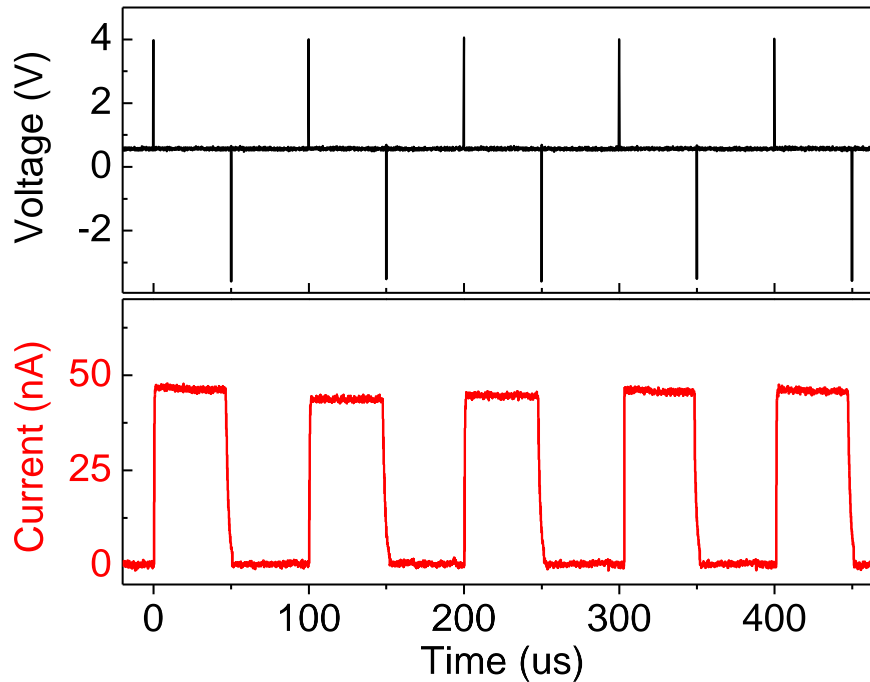


Figure 3.3. Programming speed test of the a-Si devices. Programming pulses of 4 V, 50 ns write; –3.5 V, 100 ns erase are sufficient to write/erase the device. The read pulse is 0.5 V, 50µS.

3.4 Intrinsic Diode Characteristics Verification

The interesting property of the device is that even though the device blocks current flow at small reverse bias (e.g. Fig. 3.1), it remains in the on-state and can only be erased with a sufficiently large negative bias. This effect was verified by a pulse/read measurement. As shown in figure 3.4, the device in on-state yields a 50 nA read current

at 0.5 V read bias. After the application of a −2 V, 100 ns pulse the device state was confirmed to be still in the on-state by the subsequent read pulse. To erase the device, a −3.5 V, 100 ns pulse was applied and the off-state was confirmed by the subsequent read pulse. This test shows that the intrinsic diode behavior is robust enough to survive voltage biases of at least $-V_{rease}/2$ to prevent accidental erasure during the programming of crossbar memories. Considering the worst case scenario of $(M - 1) \times (N - 1)$ possible sneak paths in an $M \times N$ crossbar array [5], the observed rectifying ratio of 10^6 can support a 100 Kbits array while ensuring a read voltage margin of 10. Almost identical intrinsic diode characteristics have also been observed in all 64 devices tested with the same configuration.

The intrinsic diode-like behavior may be explained by the motion of Ag ions inside the a-Si matrix. One possible explanation is that the Ag ions forming the conducting filament in the a-Si device at on-state can be partially retracted from the a-Si/poly-Si interface at small negative bias thus drastically suppressing the device conductance. The possible causes of this retraction include built-in electric field at the interface, and shallow trap potential between the PECVD a-Si and the poly-Si bottom electrode. Since the majority of the filament remains, the device still stays at the on-state. The partially retracted Ag ions can be readily injected again to the interface with much smaller bias (e.g., at V_{read}=0.5 V) than the regular programming. As a result the on-state of the device can be read out for all practical purposes. On the contrary the true erase process requires the filament to be fully removed, and after that the device requires voltage > V_T to be programmed again. Detailed studies are still underway to confirm the microscopic origin of the apparent intrinsic diode-like characteristics.

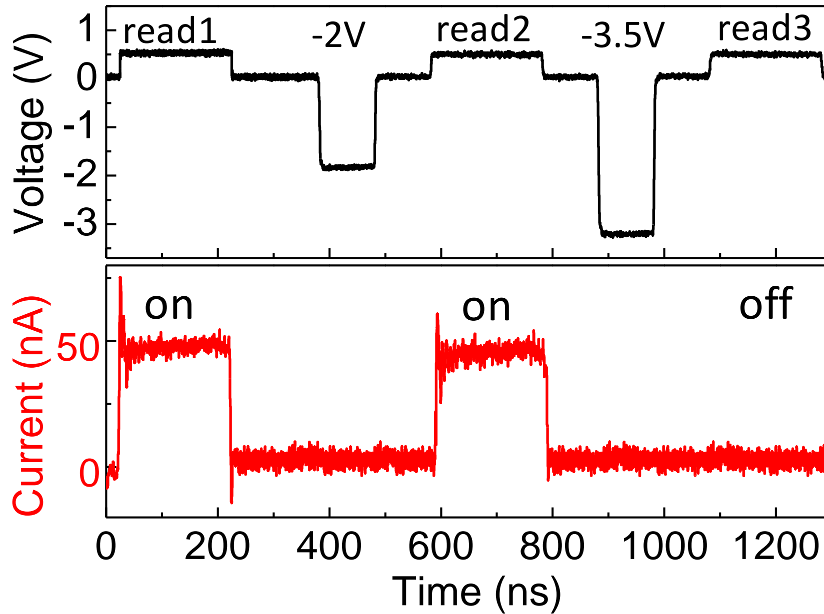


Figure 3.4. Pulse response of the a-Si device with rectifying I-V characteristics at on-states. The device can only be erased with high negative bias illustrating the robustness of the diode-like characteristics.

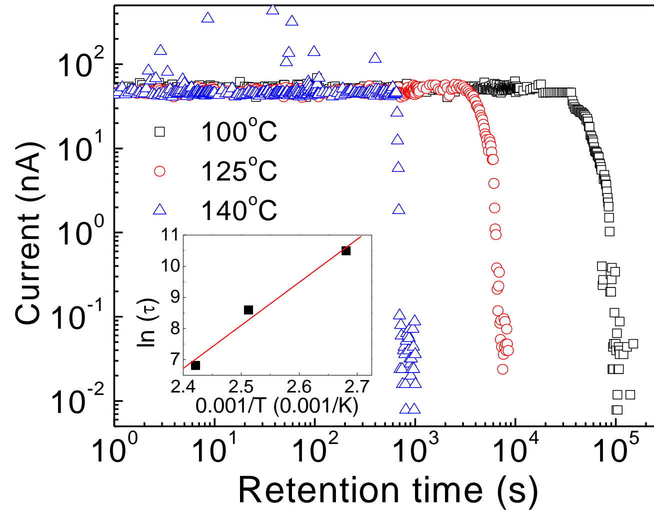
3.5 Retention Characteristics

Figure 3.5 (a) shows the retention characteristics of the device. Since the filament formation/elimination involves the thermal activation of Ag ions over a potential barrier, the retention time is dependent on temperature and the room-temperature retention time can be extrapolated from an accelerated temperature measurement as shown in figure 3.5 (a). The activation energy E_a for the Ag ion diffusion was extracted from the Arrhenius type plot in the inset which yields E_a =1.05 eV based on equation 3.1.

$$\tau = \tau_0 \times \exp(E_a/kT) \qquad \text{(Eq. 3.1)}$$

where τ is the retention time, k is Boltzmann constant, T is the absolute temperature, and τ_0 is a characteristic attempt time. The retention time at room temperature was then extracted from the inset to figure 3.5 (a) to be 4.6 years. Much longer retention estimated to be ~700 years at room temperature and 1.3 years at 85 °C has been observed with a higher programming current of 1µA in the figure 3.5 (b).

(a)



(b)

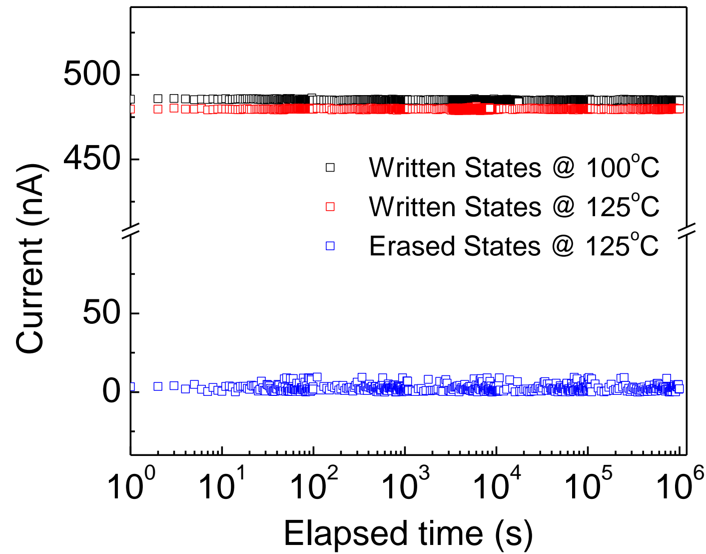


Figure 3.5. Retention tests of the a-Si device at elevated temperatures. The device was programmed to the on-state before each test and its conductance was periodically monitored with a 0.5 V, 5 ms read pulse. The inset plots the retention time vs 1/T at different temperature T. (a) Retention characteristics of the a-Si device programmed with 100nA. (b) Retention characteristics of the a-Si device programmed with 1µA.

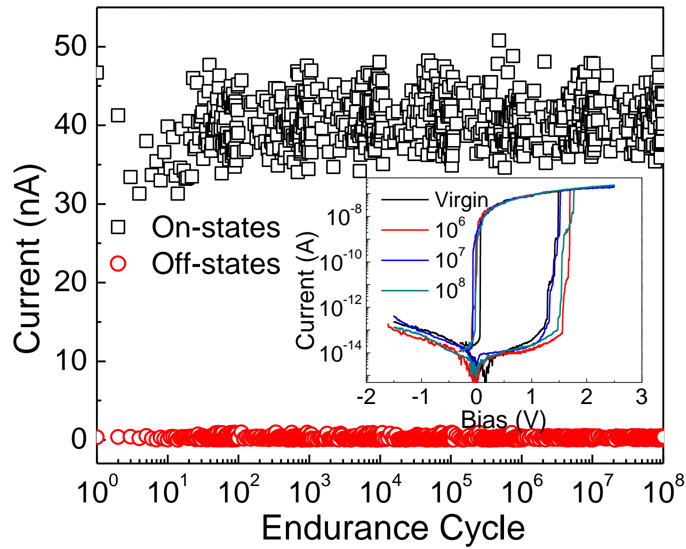
3.6 Endurance Characteristics

The low programming voltage and current used in our devices have also led to high endurance. As shown in figure 3.6 (a), the device shows no sign of degradation after of 10^8 write/erase cycles. The inset to figure 3.6 (a) shows dc I-V sweeps after different write/erase cycles. No change was observed after 10^8 write/erase cycles. The endurance is much longer than conventional metal oxide-based resistive switching memory such as NiO, TiO, CuO_x, and SrTiO [6, 14-16]. This excellent endurance is likely related to the minimized stress on the device during the write/erase processes at low programming currents, as our tests on devices with larger programming current show reduced endurance e.g., 2.4×10^7 for a device with programming current of 1 μA as shown in figure 3.6 (b). In the nanoscale a-Si based devices, the filament is believed to be formed by a single chain of discrete Ag ions and the programming speed is exponentially dependent on the applied bias [11], both of these effects ensure switching can occur at small programming currents for these devices. For example, switching current as low as 10 nA can be readily obtained in our devices with the aid of current-limiting series resistors. This may explain the high endurance observed in our devices as metal-oxide based RRAMs typically require more than 10 μA during programming. The effect of single filament formation can be reflected in the step-like increase in current in log-scale, as illustrated in figure 3.2 (b) and inset of figure 3.6 (a), i.e. the (tunneling) current is increased by a discrete amount when the tunneling distance between the filament front and the bottom electrode is reduced by one step length during the filament growth process. Notably, the size and locations of the current steps were conserved even after 10^8

write/erase cycles, suggesting the filament is always formed at the same location without excreting too much stress to the device.

Overall there appears to be a trade-off between retention and endurance, since higher current programming, which can lead to better retention (e.g. figure 3.5), normally results in larger stress to the a-Si film and results in reduced endurance (e.g. figure 3.6). Further studies such as direct imaging of the filament formation process may provide additional insight into the physics behind this observed tradeoff and continued material optimizations will likely yield further improvements of both device parameters.

(a)



(b)

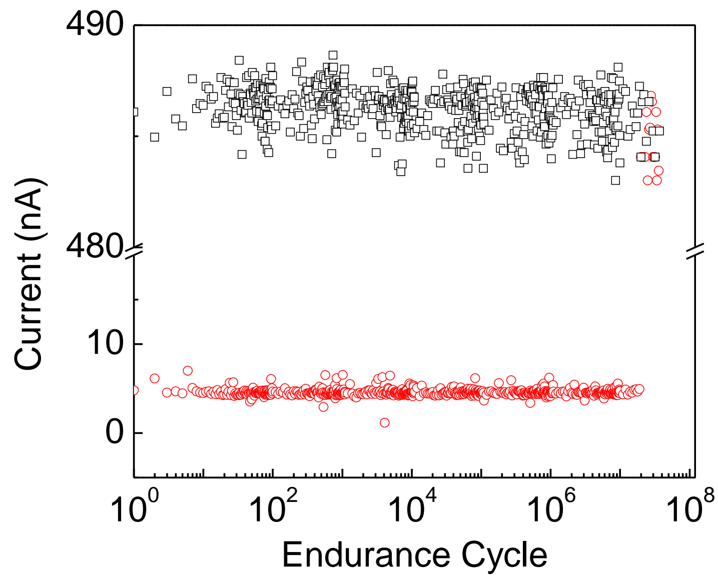
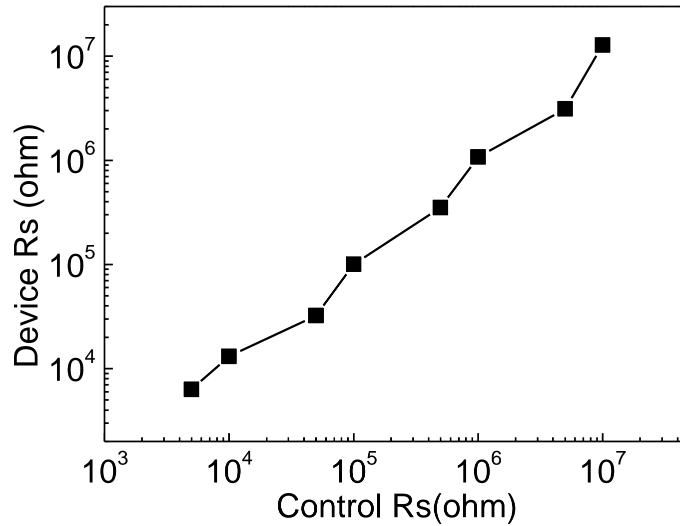


Figure 3.6. Endurance test of the a-Si device. (a) Endurance test showing the device can survive 10^8 write/erase cycles without significant degradation at a programming current of 100 nA. The write/erase pulses used in the endurance test are 5 V, 50 µs / −3 V, 50 µs. The read current at 0.5 V was recorded and plotted after write pulse and erase pulse (Only small portion of stored data is presented for better visual display). (b) Endurance test with programming current of 1µA.

3.7 Multi-bit Storage Capability

Figure 3.7 (a) shows the multilevel storage capability of the a-Si devices by controlling the programming current from 100 nA to 200 μA using a series of control resistors. The device on-resistance correlates well with the control resistance and 8 resistance levels corresponding to storing 3 bits per cell can be readily obtained. Programming currents higher than 200 μA have been avoided to minimize possible damage to the device. In addition, the device may be switched between different levels without having to be erased first, as shown in figure 3.7 (b). For example, after turning the device on with a series resistor of 100 MΩ the resistance of the series resistor was changed to 10 MΩ, and the device switches to the new resistance state after the bias voltage reaches a threshold voltage of 1.8 V. Below the threshold the previous resistance state is maintained. The I-V characteristics in this regard look similar to those expected from an analog memristor [17], although discrete jumps instead of smooth conductance changes are observed here. In addition, the control circuits here set the final resistance state independent of the previous device state, while in a true analog memristor the control circuits determines only the relative conductance change [1].

(a)



(b)

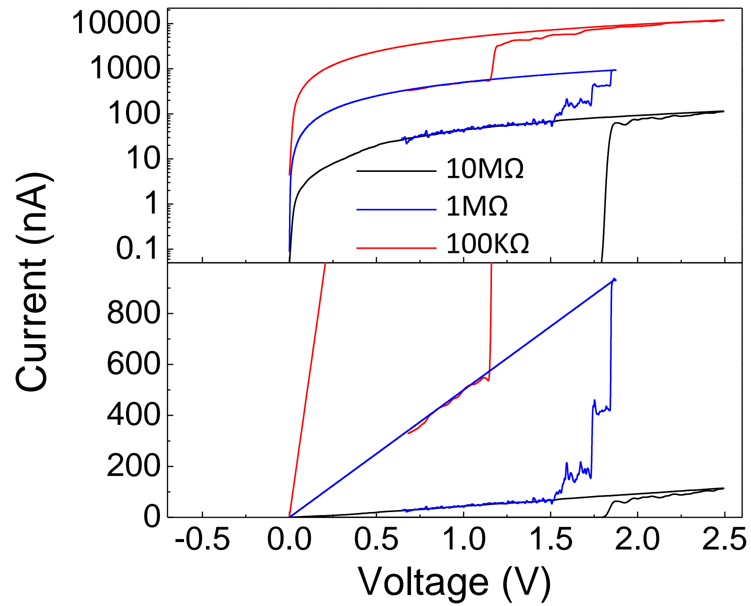


Figure 3.7. Multi-bit capability of the a-Si device. (a) Multi-bit capability of the device showing resistance control at eight different levels. The device resistance correlates well with that of the control resistor. 5 KΩ, 10 KΩ, 50 KΩ, 100 KΩ, 500 KΩ, 1 MΩ, 5 MΩ, and 10 MΩ were used to set the programming current. (b) Linear and log scale switching curves showing that the device can be changed from one resistance state to another without going through the erasing process.

3.8 Conclusions

In this chapter, nanoscale resistive switching devices with intrinsic diode characteristics were discussed. The devices show write/erase endurance 10^8, on/off current ratio > 10^6, programming speed 50 ns and retention 4 years. Most importantly, the intrinsic diode characteristics are reliable and can provide a possible solution to suppress crosstalk in crossbar memory or logic arrays. A functional memory system based on devices showing the intrinsic-diode characteristics will be discussed in Chapter 4.

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Chapter 4

On-Chip Integration of High Density Crossbar Array with CMOS Circuits

4.1 Introduction

In this chapter, the on-chip integration of high density crossbar memory with CMOS decoder circuits will be discussed. This work is the first demonstration of hetero-integration in which crossbar memory arrays without external transistors or diodes serving as select devices at each crosspoint are stacked directly on top of CMOS circuits to form a functional system.

As discussed in section 1.5, a fundamental problem for such passive crossbar arrays is that 'sneak paths' can be formed which correspond to parasitic current paths bypassing the target storage element as illustrated again in figure 4.1. To suppress current flowing through the sneak paths a memory cell in the crossbar memory essentially needs two elements: a memory switching element which offers data storage; and a select device which regulates current flow. Several reports have shown that it is possible to scale the switching element down to nanometer scale with excellent performance in terms of speed, retention, and endurance [13-15]. On the other hand, obtaining a suitable select device and integrating it to the crossbar array have become a bottleneck for resistive memory research since diodes based on crystalline materials are not suitable for low-temperature fabrication [16], while those based on low temperature materials suffer from

performance and reliability issues [8-11]. As a result, even though the fabrication of high-density crossbar arrays have been reported by several other group [17-19], none of the reported arrays were actually functional – the data were all taken from individual, isolated cells (either physically isolated or electrically isolated with all other cells grounded). To date, data from functional memory arrays reported have all been obtained from devices using transistors as select devices instead, which unfortunately do not offer competitive advantages compared to conventional floating-gate based memories. A number of approaches have been proposed to address the sneak path problem without using external transistors [7-12], however the demonstrations have been limited to the single-device level due to fabrication and device uniformity issues discussed above.

Instead of relying on an external diode as the select device, a more ideal approach is to take advantage of the inherent non-linear characteristics obtained in some resistive switches themselves to break the sneak current paths [20-23]. For example, inherently rectifying I-V characteristics at on-state were reported from several resistive switching devices [20-22]. Here we demonstrate that fully operational crossbar arrays without any external transistor or diode as the select element can indeed be built by employing such non-linear switching elements. By eliminating the requirement of having an external select device at each crosspoint, this approach significantly simplifies the crossbar array complexity and allows the array to be completed at low-temperature and directly integrated on top of underlying CMOS circuits. In the system demonstrated here, the CMOS circuits provide peripheral functionality such as address decoding to complement the data storage functionalities of the crossbar array. A new programming scheme was also developed to control the device on-resistance and allow for multi-level storage in the

array. The transistor-less and diode-less crossbar arrays can be further stacked on top of each other to maximize the density advantage offered by the nanoscale devices [4].

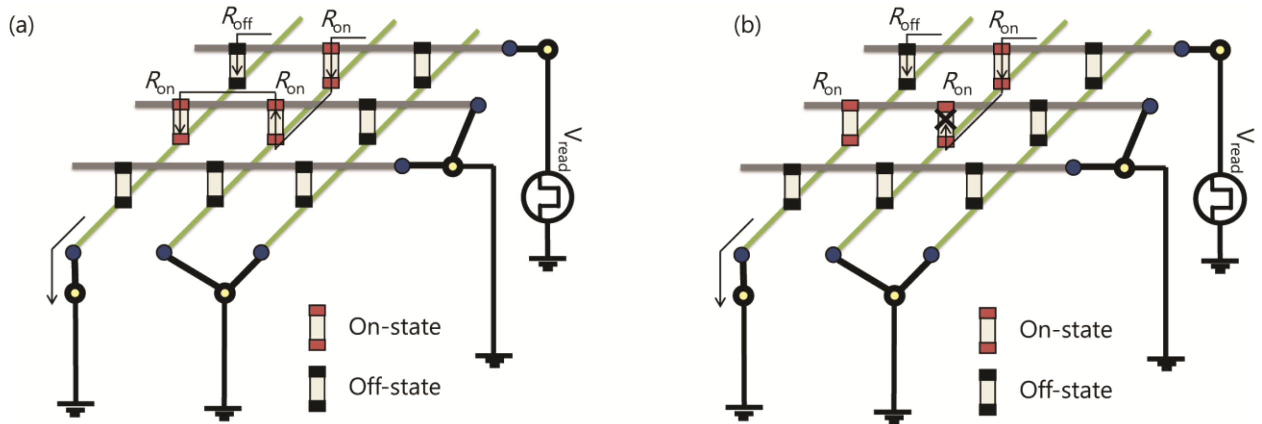


Figure 4.1. Schematic of the sneak path problem and solution for the problem. (a) Schematic of the sneak path problem. When the target cell is in the off-state, a high read current may still be mistakenly measured due to current flowing through other cells in the on-state in the array. Sneak paths always include at least one memory cell which is reverse biased. Therefore, the sneak path problem can be mitigated (b) if the resistive switching device also exhibits current-rectifying characteristics to block current from flowing through the reverse-biased cell.

4.2 Device Structure and Fabrication

The CMOS decoder circuit in the hybrid crossbar/CMOS system was prepared with IBM 7RF (0.18 micron CMOS) process through collaboration with researchers at HRL Laboratories. The 8 inches wafers were taken out from process line at the M5 layer without going through additional metal layer formation and subsequent poly-imide passivation. The whole 8" wafers were protected with thick photoresist and the wafers were transferred to University of Michigan for further processing. For crossbar array fabrication, first, the wafer was cut into 1cm by 1cm die size by using ADT dicing saw (ADT 7100) at the Lurie Nano-Fabrication facility. The thick photoresist was removed by dipping the dies in heated remover PR solution (Microlithography Chemical Corp) for 20 min. The photoresist-free wafer was loaded into sputter chamber (Enerjet Sputter Coater) and 15 nm of metallic W was deposited on top of the dies. The deposition condition was controlled with 1 A sputtering current and 7 mtorr chamber process. The wafer with pure metallic W surface was then deposited with 15 nm thick SiGe serving as the local bottom electrode. Compared with our previous studies, the use of SiGe compared with poly-Si allowed the film to be deposited at ~400 °C and can be performed directly on CMOS wafers. Then, again the sample was loaded into PECVD chamber and deposited with 20 nm of amorphous silicon at 350 ^{o}C serving as the active switching layer.

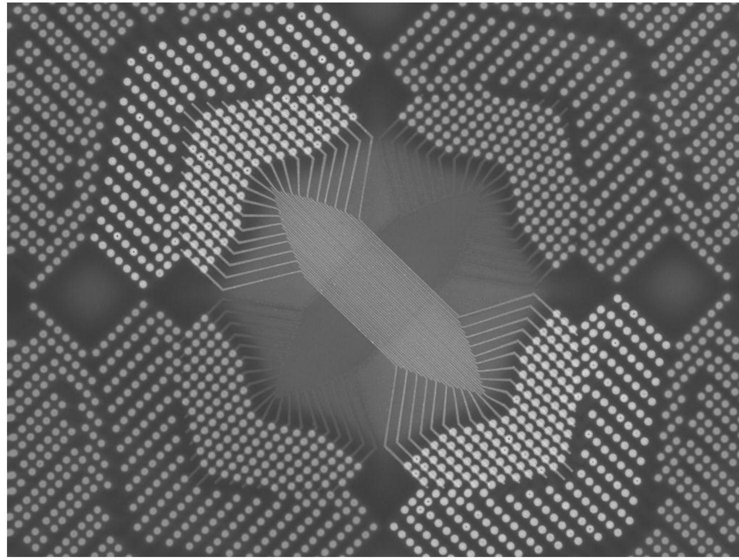
E-beam lithography was used to create line patterns of 50 nm in width and 100 nm in spacing. The sample was then developed with MIBK:IPA = 1:3 solution for 45 sec and rinsed with IPA for 20 sec. Then, 35 nm of Ni was e-beam evaporated and lift-offed for hard mask. The bottom electrode and switching layer stack were patterned with high-density plasma etcher (LAM 9400). The bottom electrode stack was then passivated with

PECVD oxide deposition and planarized by an etch-back process. The side-wall passivation protects corrosion of W stacks in touch with SOG (Spin on Glass). SOG was then deposited and cured. The SOG thickness was monitored with SEM and ellipsometry (*AUTO EL*). The as-prepared SOG thickness was about 300 nm thick but the thickness can vary by ± 10 nm depending on SOG baking conditions and the SOG age. The SOG layer was etched back to expose the surface of the switching a-Si layer. Again PMMA A2 was spin-casted and opened on via regions for top electrode. The residual SOG on top of top electrode vias was removed with high plasma density etcher followed by removal of PMMA etch mask with high plasma O_2 ashing. Again, PMMA with 2% anisole concentration was spin-coated. Electron beam lithography was performed for top electrode which is extended from the active area to the open via area. Table 4.1 summarizes all the fabrication steps. The SEM image of a completed integrated crossbar array is shown in figure 4.2.

Table 4.1. Fabrication sequences for the crossbar array integration.

Seq.	Process
1	Photoresist removal
2	W deposition
3	a-Si seed layer deposition
4	SiGe deposition
5	a-Si layer deposition
6	Ebeam lithography for bottom electrode
7	Ni ebeam evaporation
8	Lift-off Process
9	Bottom electrode etch
10	Sidewall passivation
11	SOG planarization
12	E-beam litho for Via open
13	Via etching
14	O_2 ashing
15	E-beam lithography for Top electrode
16	Ag / Pd E-beam evaporation
17	Lift-off

(a)



(b)

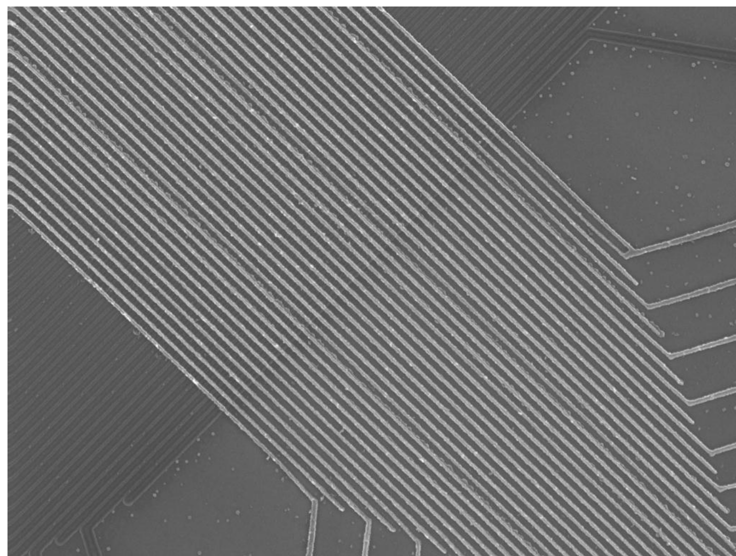


Figure 4.2. The complete device structure of the integrated crossbar array. (a) zoom-out version of the integrated device. The top electrodes are directly extended over to the open via region. (b) zoom-in of the crossbar array. The density of the crossbar memory is 10 $Gbits/cm^2$ with 100 nm pitch.

4.3 Bottom Electrode Choices

Previously, we have studied devices composed of a poly-silicon bottom electrode contacted with the a-Si switching layer and the devices showed switching characteristics with rectifying I-V and excellent memory performance [6,13,20]. For comparison, devices fabricated with metallic bottom electrodes such as W, Ni, Al showed only ohmic-like I-V switching curve. With normal thermal CVD chamber, high quality poly-Si only can be deposited at above 590 ^{o}C [24]. Making the situation worse, boron dopant requires temperatures around 800 ^{o}C by using RTP. These high temperatures will severely degrade the CMOS chip with worsened threshold distribution, reduced on current, increased off current and broken metallization [25-26]. Therefore, before on-chip integration of high-density crossbar memory with CMOS circuit can carried out, a new bottom electrode material which can be fabricated with lower temperature processes but can still preserve the switching characteristics with rectifying behavior needs to be developed.

4.3.1 Silicidation Approach

Silicidation is a process in which silicon reacts with some other metals such as Ti, Ni, Pt, Co, and Au and forms silicon metal compounds. In a silicidation process, there can be many phases of silicide, e.g. TiSi, $TiSi_2$ (C49), $TiSi_2$ (C54) [27] for the Ti-Si system. For a certain metal silicide, there is a phase that has lowest resistivity. Therefore in the silicidation process, it is important to develop the process that enhances certain phase growth while preventing the other phases growth [28-29]. Several metals such as

Ti, Pt, Ni, and Au were tried to form silicides as the bottom electrode at temperatures below 450 ^{o}C. However, without multi-chamber CVD which combines Si deposition, Ar sputtering, reactant metal, and annealing chambers together, suppression of native oxide growth on surface of Si is difficult [30]. Due to native oxide growth, Ni and Pt could not initiate a silicidation process with Si although those metals have lower or comparable activation energy for silicidation to Ti [31-33]. However, Ti is very reactant with Si for silicidation even in the presence of native oxide. Undoped a-Si and boron doped a-Si deposited at 400 ^{o}C was silicided with Ti at 450 ^{o}C for 5 hrs in the nitrogen-ambient chamber. The resistance of bottom electrode is reduced by 10^{3} times. However, The removal of the excessive Ti after silicidation is challenging and not compatible with the CMOS integration process.

4.3.2 Recrystallization Approach

Doped a-Si can be deposited at 400 ^{o}C and can be recrystallized at relative low temperatures as low as 450 ~ 500 ^{o}C [34-35]. The boron-doped a-Si sample was annealed at 400 ^{o}C in nitrogen chamber for 24 hrs. XRD data confirms growth of crystalline silicon phase (111) and conductance increased by 5 times. However, the resistivity is still 10^{3} orders of magnitude higher than desired, and the improvement on resistance of bottom electrode stack is not significant enough to be used for highly-scaled bottom electrode. This poor improvement in the conductance was thought to be due to relative low temperature for boron activation [36].

4.3.3 Metal Induced Crystallization Approach

Metal induced crystallization has been proposed in order to reduce annealing time and processing temperature [37]. Several metals such as Ni, Ag, Au, and Pd was reported as effective metal elements that enhances crystallization process of a-Si [38-39]. In a variant of this method, called Metal-induced lateral crystallization (MILC), metal is only deposited on some area of the a-Si to minimize metal contamination issues at device active area [40]. In this experiment, 40 Å of Ni, Ag, Au, and Pd were deposited on top surface of a-Si and annealed at 400 ^{o}C in N_2 ambient RTP chamber for 10 min. Enhanced nucleation process contacted with Ni was observed and several nucleation spots in a disc shape spontaneously are generated and expanded radially as annealing time increases. Despite reduced processing temperature and time for crystallization process, removal of excessive metals after annealing process is not compatible with the CMOS integration process.

4.3.4 Different Materials

In fact, obtaining poly-Si at lower temperatures has been long desired for several other applications such as poly-Si TFT, and on-chip integration of MEMS devices [41-43]. Along the effort to achieve lower temperature growth of highly-conducting Si material, poly-Si_xGe_{1-x} has been reported as an alternative material with reduced activation energy for dopant activation and crystallization [44-45]. Poly-Si_xGe_{1-x} can be easily deposited by introducing GeH_4 gas to the poly-Si deposition recipe. In addition, Boron doping has been shown to further lower the crystallization energy of SiGe. For

example, we found that poly-crystalline, boron-doped Si_xGe_{1-x} films can be grown at 425 ^{o}C, and offer resistivity as low as 25×10^{-6} ohm·m. Tests of standalone cells using Si_xGe_{1-x} as the bottom electrode show similar rectifying switching characteristics and reasonable retention characteristics as shown in figure 4.3 and figure 4.4. Based on these studies, boron-doped poly-Si_xGe_{1-x} was identified as the bottom electrode material for the integrated crossbar array. The ratio of Ge over Si was found to be 50% - 70% depending on SiH_4 : GeH_4 ratio during SiGe film growth.

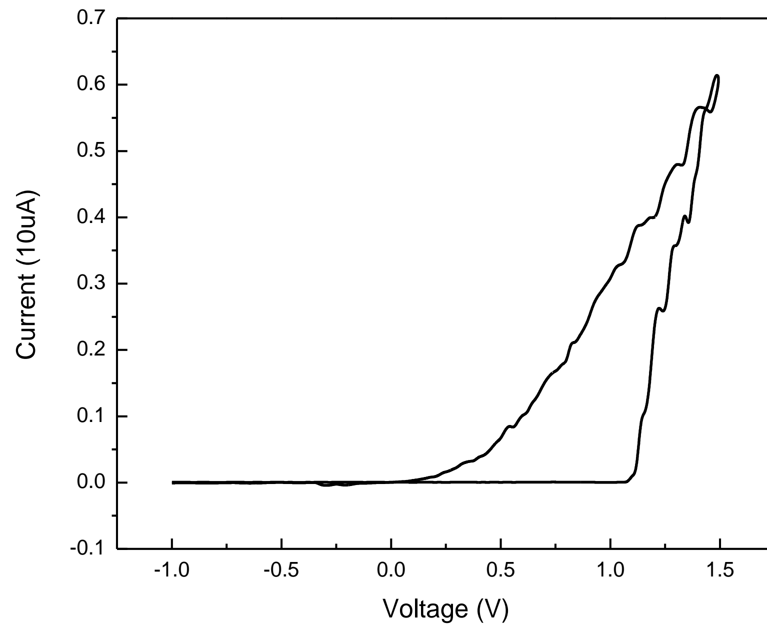


Figure 4.3. I-V switching curve from SiGe based RRAM showing intrinsically rectifying I-V characteristics.

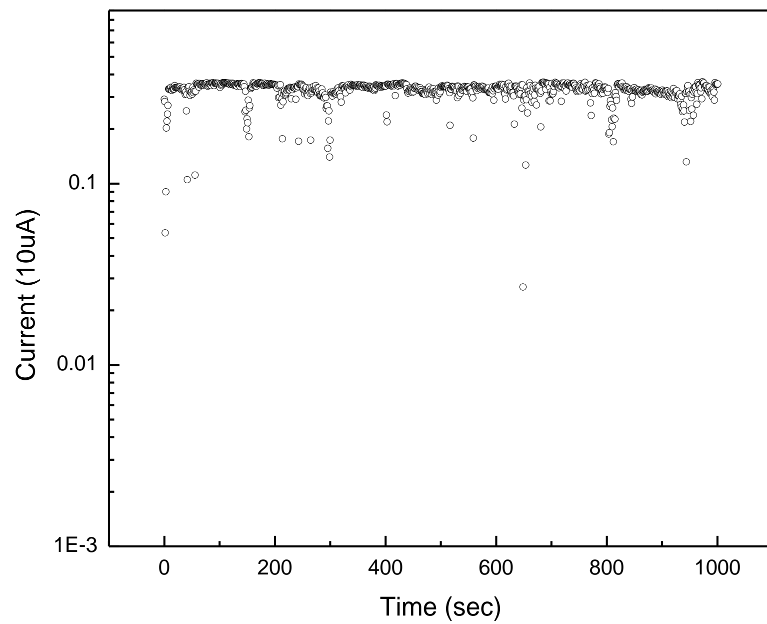


Figure 4.4. Retention characteristics of the SiGe-based RRAM

4.4 Operation of the Integrated Crossbar Array Chip

In this section, the operation of the integrated crossbar array chip will be discussed in detail. The decoder circuit (figure 4.5) for the crossbar array has four independently operating multiplexing circuits. Each of the multiplexing circuits can be controlled by 8 of I/O control signals. In this integrated system, to access a bit the corresponding address code inputted to the row decoder enables the target row (word-line) to be connected to one of the data input (DATA A) through CMOS pass transistors in the decoder circuit, while all other unselected rows (i.e. whose addresses do not match the input address code) are connected to the other data input (DATA B), schematically illustrated in figure 4.4. Similar configuration is used for the column electrodes (bit-lines) so when the right word-line and bit-line combinations are selected the desired programming or read voltage (supplied to DATA A) can be applied across the selected bit only, while all other unselected bits will be connected either with predefined protective voltages, ground, or left floating through DATA B. As a result, the integrated system allowed us to program the 1600 cells inside the 40×40 array randomly with only 2 DATA inputs and 5 address inputs at each side, instead of having to supply 40×2 data inputs simultaneously for the case without CMOS decoder circuitry.

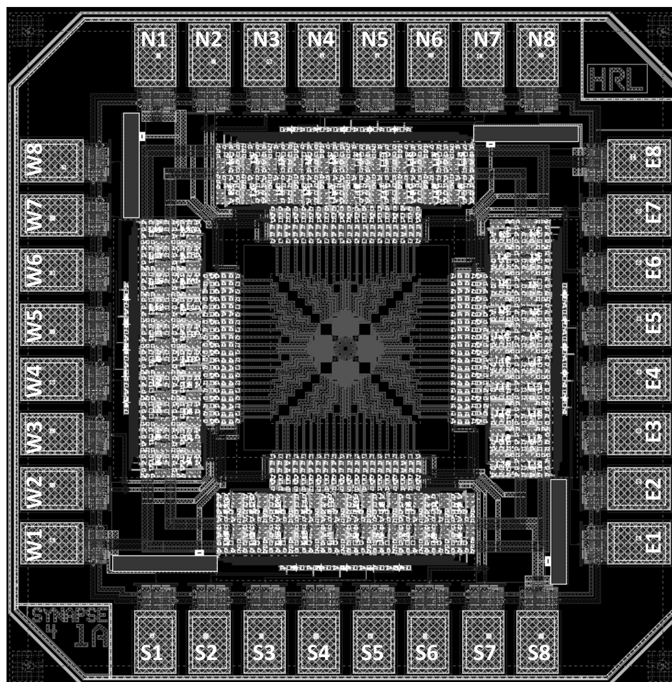


Figure 4.5. Die image of the CMOS decoder circuit.

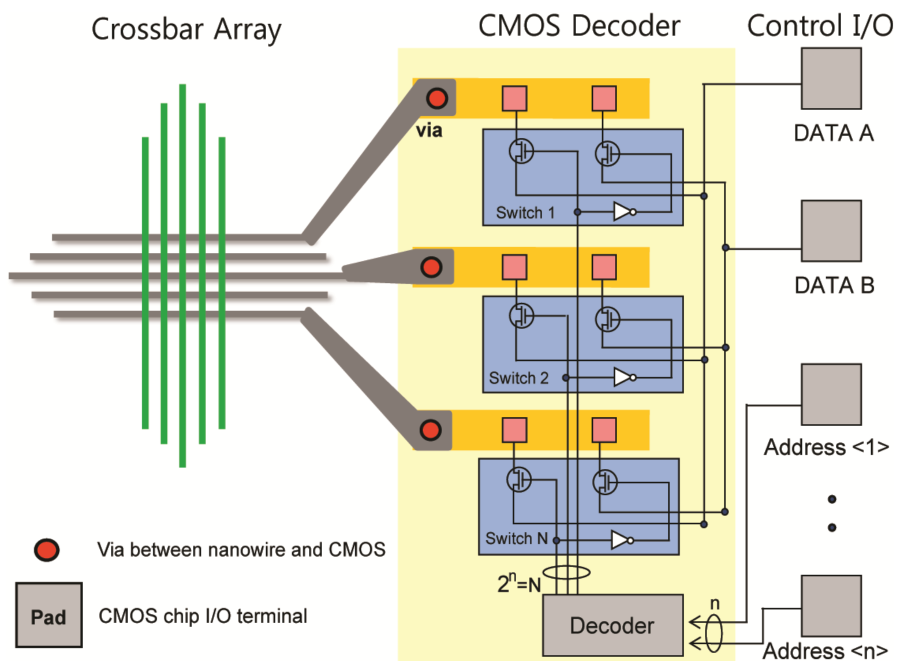


Figure 4.6. Schematic of the program/read schemes. Each column or row in the crossbar array is connected to one of the two external signal pads (DATA A for signal applied to the selected column/row, DATA B for signal connected to the unselected column/row) through CMOS decoder circuits controlled by address I/O pads.

4.5 Characterization of the Crossbar/CMOS Integrated Chip

4.5.1 DC Switching Characteristics

Figure 4.7 shows the I-V switching characteristics of the integrated crossbar/CMOS system using the programming method described in the chapter 4.4. Significantly, the fabrication of the crossbar array in the back-end-of-the-line fashion does not affect the CMOS device performance, and all programming and read signals can be passed through the CMOS circuit to the crossbar array as designed. In addition, figure 4.7 shows that very similar switching curves can be obtained from devices in the fabricated crossbar array with a narrow threshold voltage distribution. Tight distribution of the switching characteristics is a prerequisite to the operation of resistive memories at large scale to avoid accidental program/erase process when applying protective or read voltages. To further illustrate the switching parameter statistics, figure 4.9 plots the histogram of the threshold voltages obtained from 256 cells in the array, showing a tight distribution with an average threshold voltage of 2.30 V and standard deviation of 0.07 V. It is also noteworthy that the cells maintain an intrinsic current-rectifying behavior as shown in figure 4.8 such that the current at reverse bias is pronouncedly suppressed compared to the current at forward bias, consistent with earlier reports on similar stand-alone cells [20]. Again, even though the current through the device is suppressed at relatively small reverse bias, the device still remains in the on-state and only become erased with large (e.g. < -1.5 V) negative voltages. This effect was verified in figure 4.10, which shows that the on-state is not destroyed with reverse biases up to -1 V. The intrinsic current-rectifying characteristic is a key reason that the array studied here can operate without having an external transistor or diode at each crosspoint.

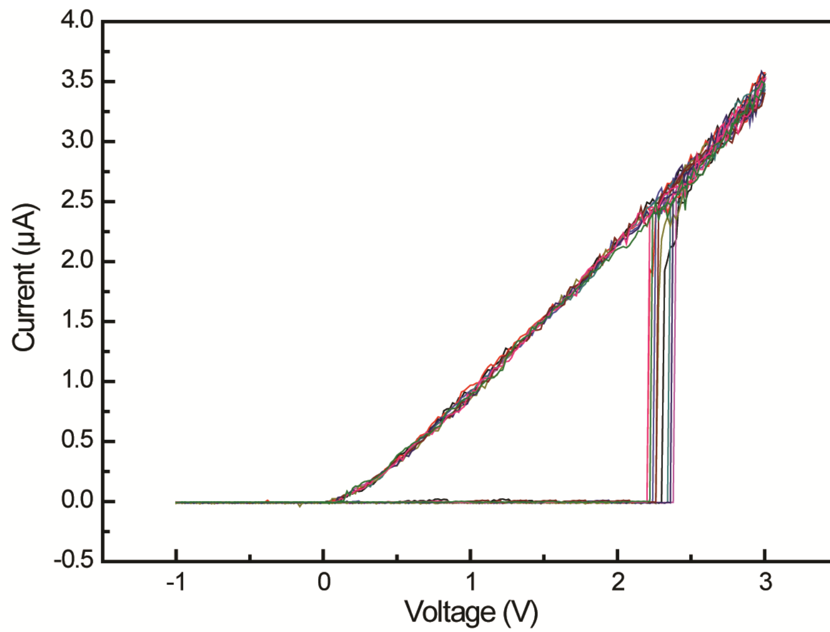


Figure 4.7. I-V switching characteristics from 10 different cells in the crossbar array.

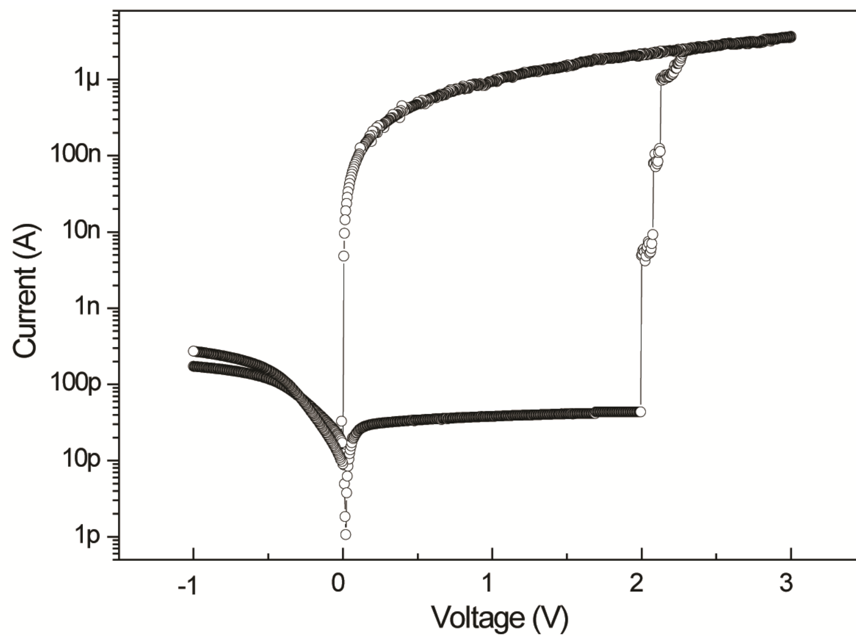


Figure 4.8. I-V switch characteristics plotted in log scale demonstrating current suppression at negative bias in the on-state.

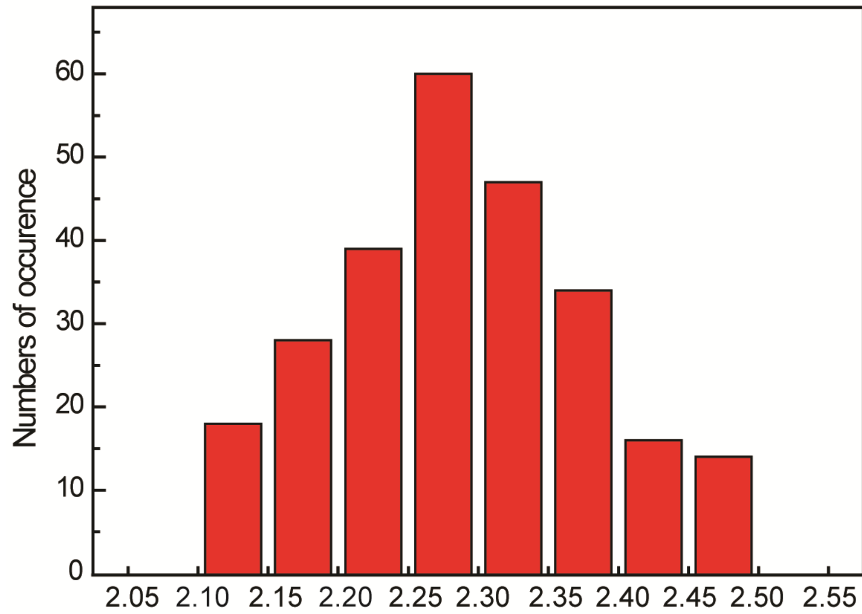


Figure 4.9. Threshold voltage distribution from 256 cells in the fabricated crossbar array. The threshold voltage was defined as the voltage at which the measured current is above 10^{-6} A.

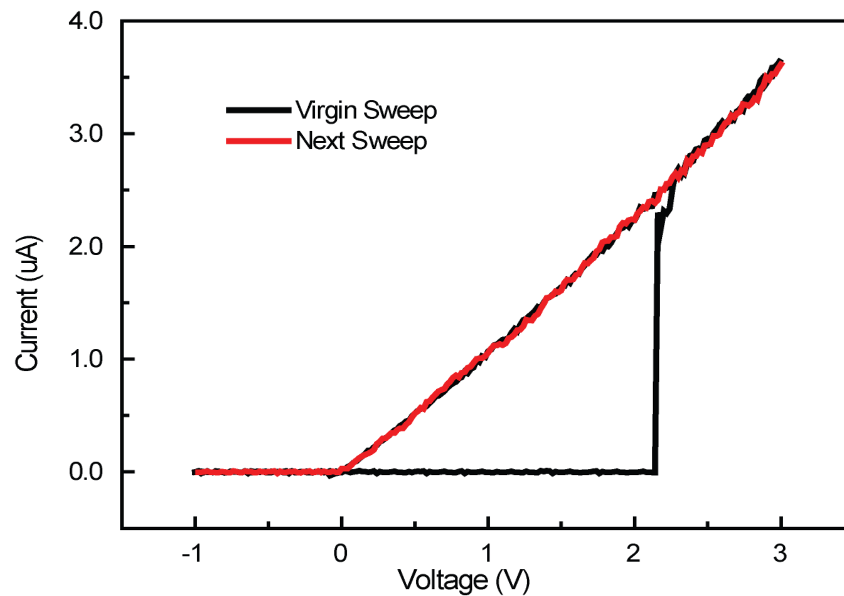


Figure 4.10. I-V characteristics of a device in the voltage range of −1 V to 3 V. Even though the current through the device is low at negative bias, the device remains in the on-state, as verified from subsequent voltage sweeps. The device can be erased with larger negative voltages (< −1.5 V).

4.5.2 Storing and Retrieving Operation with Binary Bitmap Images

To test the operation of the integrated crossbar array, a binary bitmap image with 1600 pixels (40×40) that represents the University of Michigan logo was prepared (figure 4.11 with the black pixels representing data 0, i.e. the 'off-state' and white pixels representing data 1, i.e. the 'on-state'). The image was then programmed into the 40×40 integrated array and read out. For writing '1' into a cell inside the array, a 3.5 V, 100 µs pulse was applied across the selected cell through the CMOS decoder circuit using the protocol discussed above, while the other unselected electrodes were connected to a protective voltage with amplitude equaling half of the programming voltage to minimize disturbance of unselected cells. The same approach was also used for writing '0' into a cell with a –1.75 V, 100 µs erase pulse. The programming/erasing was carried out based only on the input pattern and regardless of the current state of the memory cells, and a single programming/erase pulse was sufficient for a given cell. Once all data were programmed in an array, the information in the array was then read out one cell at a time by applying a 1 V, 500 µs read pulse across the target cell, while grounding all unselected electrodes through the CMOS decoder. To minimize cell wear out, the 40×40 array was divided into 25 8×8 sub-arrays and each sub-array was programmed as a whole followed by readout. The 40×40 pixel bitmap image was reconstructed by stitching results from the 25 8×8 sub-arrays together. The resulting image in figure 4.12 accurately reflected the initial target image, and clearly demonstrated that by taking advantage of the intrinsic non-linear I-V characteristics the integrated crossbar/CMOS system can function well without added transistor or diodes as select devices at each cell. To further illustrate the full functionality of the integrated crossbar array, a complementary image (figure 4.13) of

the original was stored into the same array using the same approach. The reconstructed image for the complementary bitmap was presented in figure 4.14, verifying every bit in the crossbar array can be reliably reprogrammed to either the 1 or 0 state. The reliability of the memory array was further illustrated by examining the on- and off-state resistance distribution, as plotted in figure 4.15 for the two cases. Clear separation between the 1 and 0 states was obtained, with at least 20 times difference in resistance between the worst cases.

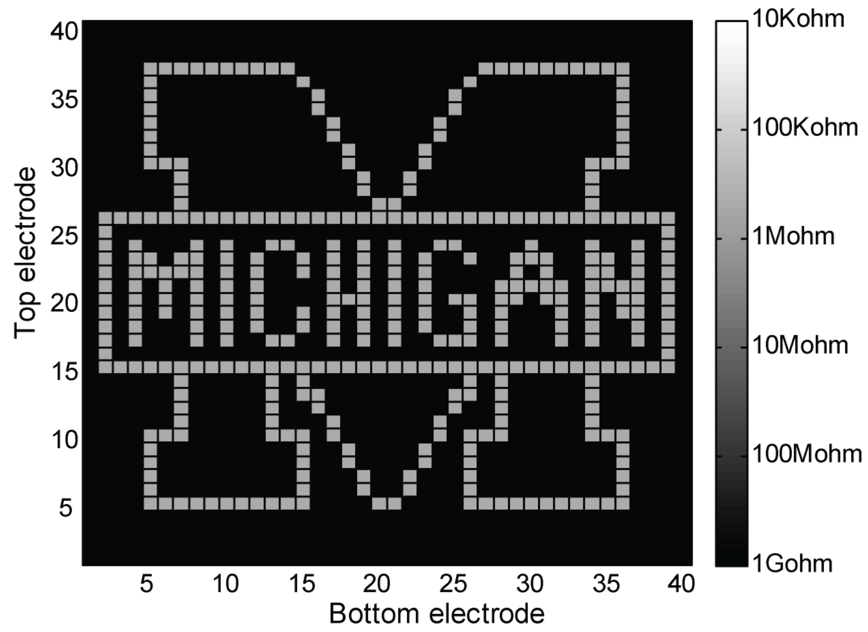


Figure 4.11. The original black-and-white 40×40 bitmap image representing the University of Michigan logo.

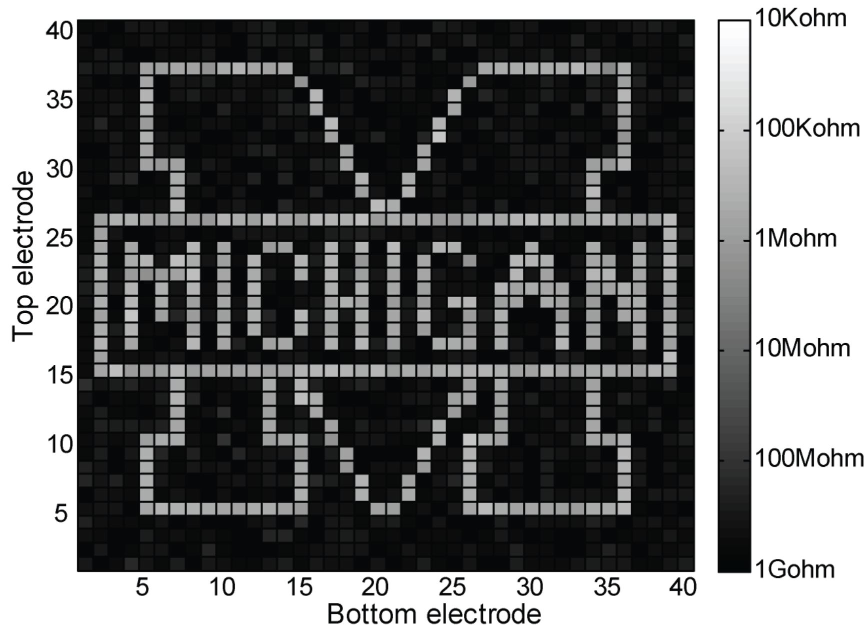


Figure 4.12. The reconstructed bitmap image from storing and retrieving data in the 40×40 crossbar array.

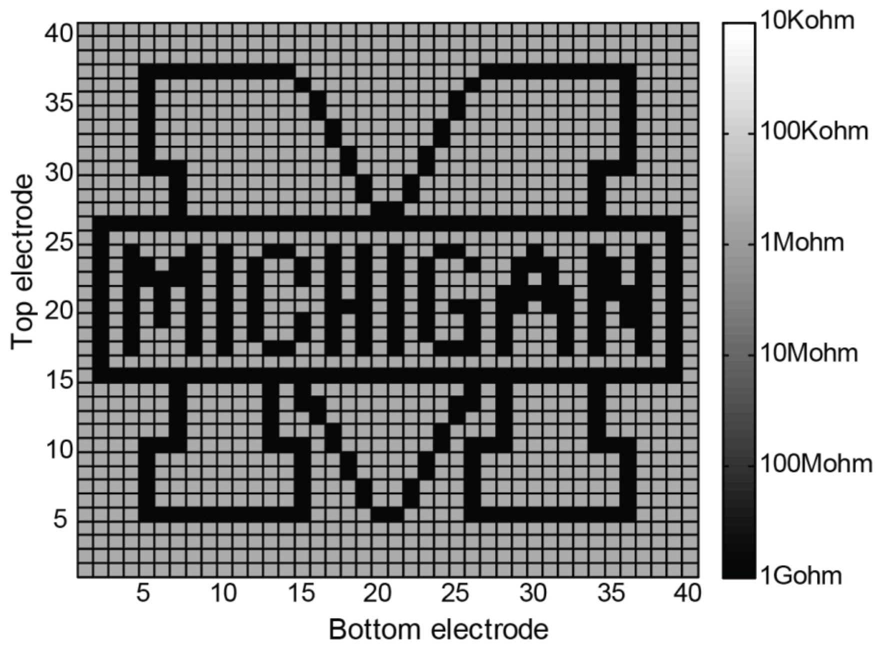


Figure 4.13. A second test image, which is complementary to the original, to be stored in the array.

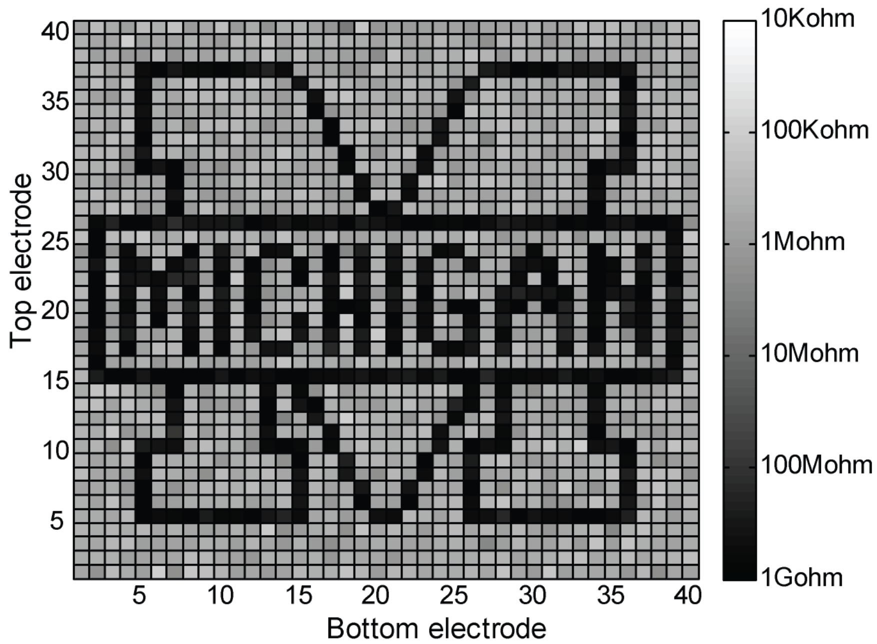


Figure 4.14. The reconstructed image from storing the image in figure 4.13 in the same array.

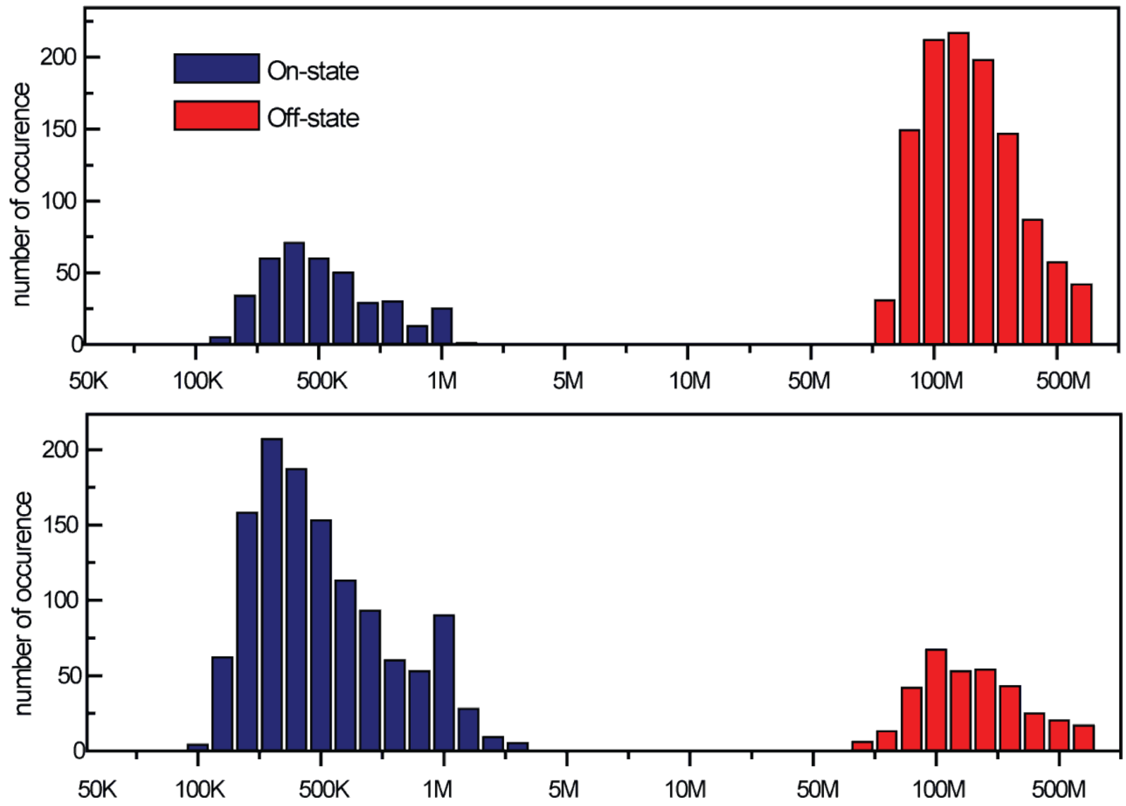


Figure 4.15. Histograms of the on- and off-state resistances for the data in figure 4.12 and figure 4.14, respectively.

4.5.3 Multi-level storage in the array

The large on/off current ratio offered by the cells (e.g. figure 4.8) suggests the possibility for multi-level cell (MLC) storage. Storing multiple levels or multi-bit in one memory element is necessary to satisfy the needs of increased storage density and is also required for neuromorphic applications which have been proposed to be ideally suited for these resistive devices [46-47]. Achieving MLC capability in resistive devices has been demonstrated by controlling the current compliance during switching, or equivalently by controlling the series resistance the cell sees [48-50]. To verify MLC capability for the devices in the integrated system, we programmed a single cell in the crossbar array (with all other cells in the off-state) with different series resistances (100 KΩ, 500 KΩ, 1 MΩ, 5 MΩ) and the results shown in figure 4.16 demonstrated that MLC is indeed possible with the on-state resistance of the cell controlled by the series resistor value. As discussed in section 3.7, this multi-level storage effect can be explained by the self-limiting filament growth model in which the filament growth rate is roughly an exponential function of the applied voltage across the memory device [48-49]. As the resistance of the memory device approaches the series resistance value, the voltage across the device is reduced by the voltage divider effect and filament growth significantly slows down resulting in a device resistance determined by the series-resistance [48-49]. The reproducibility of the MLC operation is verified in figure 4.17, which plots the resistance distribution from 30 different cells, each programmed into four different resistance states.

However, achieving multi-level storage in crossbar arrays is inherently much more difficult than achieving binary storage, since the series-resistance seen by the target cell (or equivalently, the programming current through it) will be affected by other cells in the

array. As illustrated in figure 4.18, the current flowing through the target cell is not only affected by the external series resistor, but also by the states of the half-selected cells sharing the same word line electrode, i.e. the actual series-resistance the target cell sees is the combination of the external series-resistance and those of the half-selected cells in parallel which cannot be determined beforehand. This effect explains why the resistance distributions obtained in the array shown in figure 4.15 are larger than those shown in figure 4.17 for individual cells, and why the distributions are also worse in lower panel of figure 4.15, which corresponds to a configuration with more cells in the on-state hence more leakage paths, compared to those in upper panel of figure 4.15. To address this problem, the parallel current paths must be blocked. To this end, we developed a new programming scheme to achieve these goals. In this approach, schematically illustrated in figure 4.19, external diodes (e.g. P6KE15A, Littelfuse Inc. used in this study) are connected to each unselected bit-line and word-line to prevent current flow into external electrodes and allow only the applied signals to path through. Once again, the intrinsic current-rectifying characteristic played a crucial role in making the approach feasible since it prevents current from flowing backwards at the crosspoints to reach the selected bit-line or word-line. Combining the intrinsic rectifying characteristics with external diodes, current flow through the half-selected cells can now be fully prohibited, enabling control over current in the target device during programming for multilevel storage capability. In addition, this approach reduces power consumption during programming, which has been another main drawback for conventional crossbar array programming. For comparison, our simulations (figure 4.20) show that without the intrinsic current-rectifying characteristics, programming current through the target cell cannot be

controlled even with the application of external diodes at the unselected electrodes. In the new scheme shown in figure 4.19, since the unselected bottom electrodes are virtually floated due to the reverse biased diodes, they may be charged up during programming to a potential close to the programming voltage. As a result, the unselected cells can potentially see large negative voltages (< –1 V) across them during programming. To reduce this effect, asymmetric protecting voltages were used for unselected word-lines and bit-lines, as shown in figure 4.19. The exact potential distribution across the entire crossbar array was simulated for the worst case scenario and presented in figure 4.21. By properly selecting the protective voltages, the maximum negative voltage the unselected cells could see was shown to be –0.8 V at the worst case during programming, not sufficient to disturb the state of the unselected cells.

Based on this new programming scheme, a randomly generated color (multilevel) map with 10 different levels (25 KΩ, 50 KΩ, 100 KΩ, 250 KΩ, 500 KΩ, 750 KΩ, 1 MΩ, 5MΩ, 7.5 MΩ, 10 MΩ) as presented in figure 4.22 was stored into the 40×40 array. Each target resistance value was set by a switchable series resistor and programmed with a single 3.5 V,100 μs voltage pulse. A set of 5×5 sub-arrays were programmed, followed by retrieving of all bits in the sub-arrays with 1 V, 500 μs read pulses without series resistor. The process was repeated to complete the 40×40 array and the reconstructed image is presented in figure 4.23. The stored/retrieved image roughly follows the same patterns as the original image; however, some errors are also visible due to the relative small spacing between the different resistance values used to store the 10 levels. The error, defined as $\frac{(R_{target} - R_{measured})}{R_{target}}$, is presented in figure 4.24 and 4.25. Overall 75% (1200/1600 cells) of the measured resistance values were within 50% of the target value,

i.e. $0.5R_{target} < R_{measure} < 1.5R_{target}$. The apparent asymmetry of the histogram plot shown in figure 4.25 is mainly due to the way error is calculated here (e.g. with an asymmetric range from $-\infty$ to 1). For digital information storage the error reported here is relatively large but may be improved further by using on-chip integrated current-compliance setups instead of an off-chip resistor to reduce parasitic effects. On the other hand, this level of error may not be a significant problem for neuromorphic applications as biological systems typically exhibit similar sized or even larger noise [51].

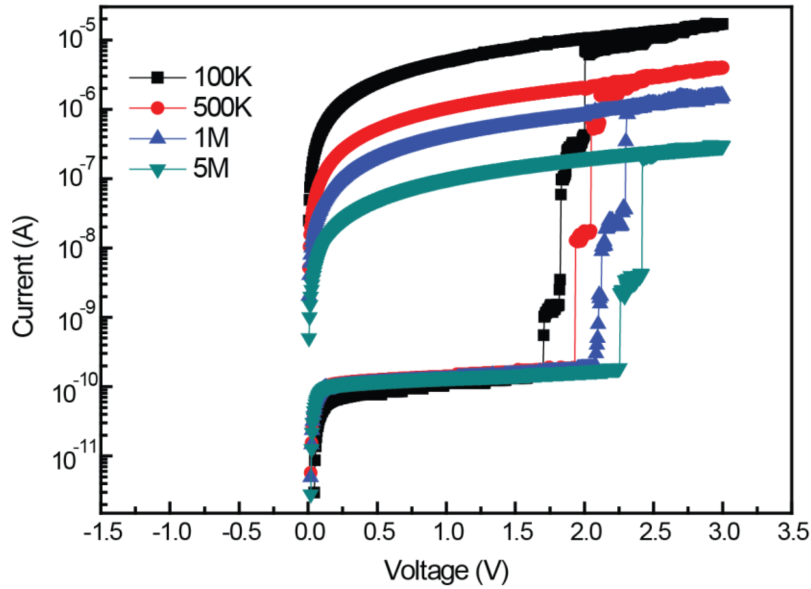


Figure 4.16. I-V characteristics of a single cell programmed with four different series resistance values (100 KΩ, 500 KΩ, 1 MΩ, 5 MΩ), demonstrating multilevel capability.

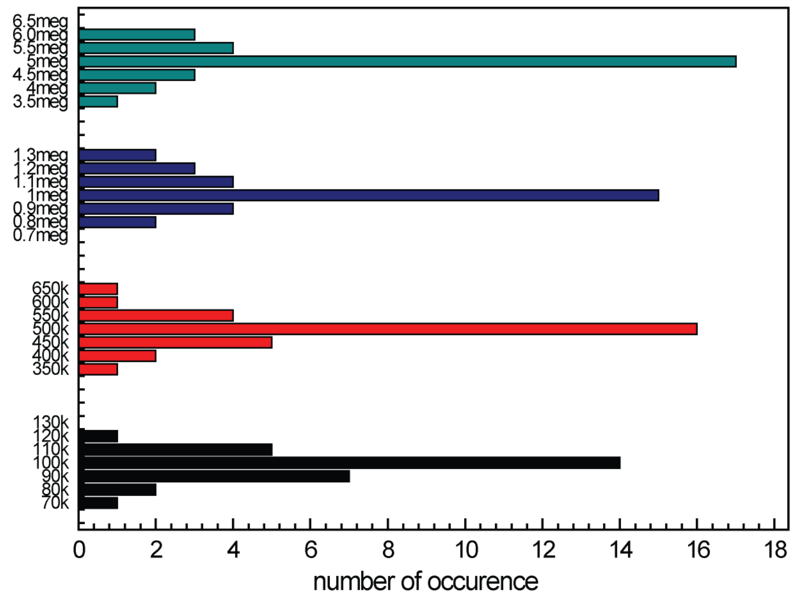


Figure 4.17. Histogram of the on-state resistances for the four target values. The data were collected from 30 different cells, each of which was programmed into all four levels.

Figure 4.18. Measurement diagram for the conventional programming scheme. In this case, the effective series-resistance seen by the target cell consists of additional current paths through half-selected devices and cannot be predicted beforehand.

Figure 4.19. New measurement diagram that enables multilevel storage in the crossbar array. Parallel current paths through the half-selected devices are blocked by the intrinsic current-rectifying characteristics at each crosspoint and the external diodes at the outside.

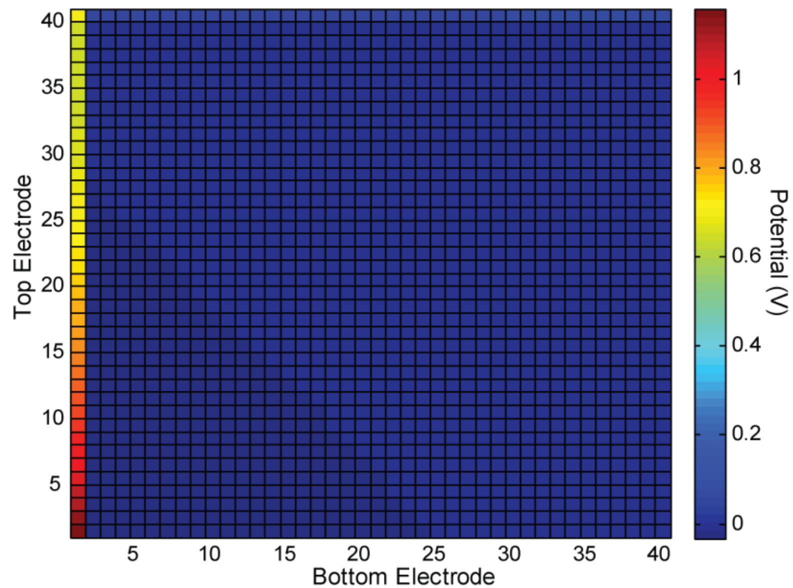


Figure 4.20. Potential distribution without the current-rectifying characteristics at the crosspoints but with the application of external diodes to the unselected electrodes. The worst case is simulated with the target cell (cell (0,40), upper left) in off-state (500 MΩ) and all others in on-state (500 KΩ). With the application of 3.5 V write pulse and symmetric 1.7 V protecting voltage applied to the unselected electrodes, only 0.5 V is actually applied across the target cell due to parasitic current paths through the half-selected devices resulting in a voltage divider effect with the external series-resistor.

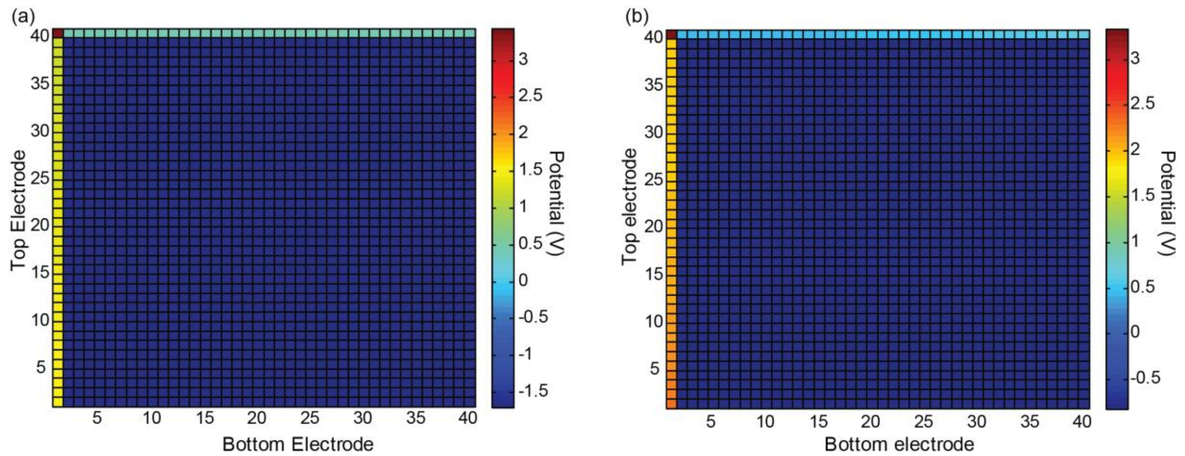


Figure 4.21. Simulated potential distribution from the circuit configuration in figure 4.19. The worst case is simulated with the target cell (cell (0,40), upper left) in off-state (500 MΩ) and all others in on-state (500 KΩ). The potentials of the bottom electrodes are raised by currents through the half-selected cells at the same row of the target cell, as shown in the change in color in the top-most row. (a) Application of symmetric protecting voltages. In this scenario, 1.7 V is applied to the unselected bottom electrodes and the unselected top electrodes. A large negative potential (~ –1.7 V) which can disturb the state of the unselected memory cells can build up across all the unselected memory cells, as represented by the blue color in cells (1,39) to (40,0). (b) Application of asymmetric protecting voltages. Here 3.0 V is applied to the unselected top electrodes, while 1.7 V is applied to the unselected bottom electrode. As a result, the unselected devices are biased with a –0.8 V negative voltage which will not disturb the state of the unselected memory cells.

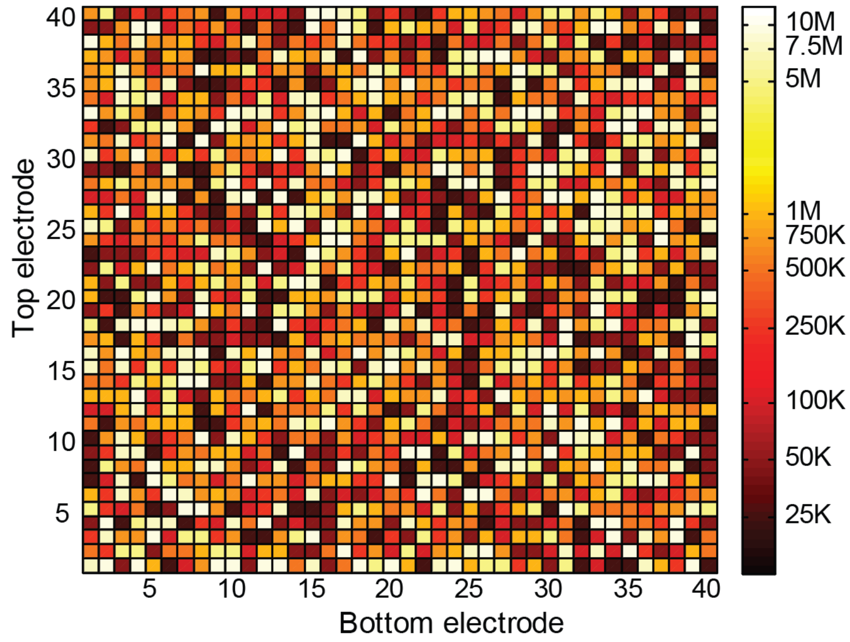


Figure 4.22. A color 40×40 test image with 10 different target levels to be stored in the array. The resistances are represented by the different colors as defined in the color scale bar on right.

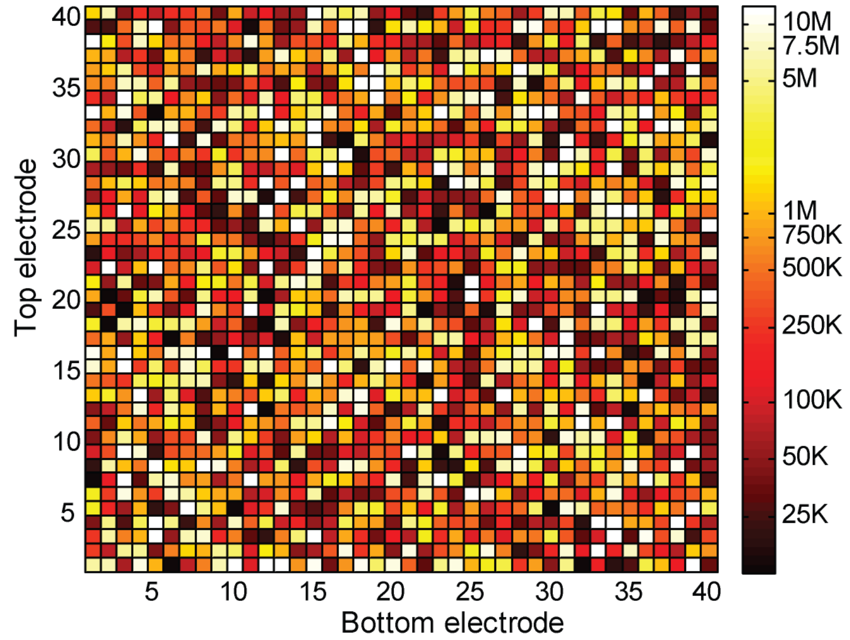


Figure 4.23. The reconstructed data map from the 40×40 array by storing and retrieving the image in figure 4.22. Same color scale is used.

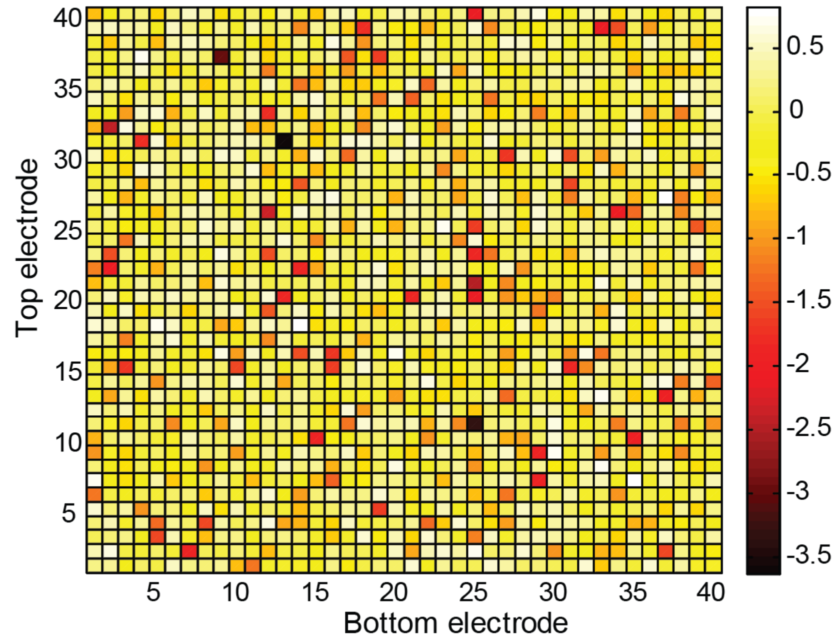


Figure 4.24. False-color image of the error for the stored data. The error was defined by $\frac{(R_{target} - R_{measured})}{R_{target}}$ and represented by different colors in the color scale bar on

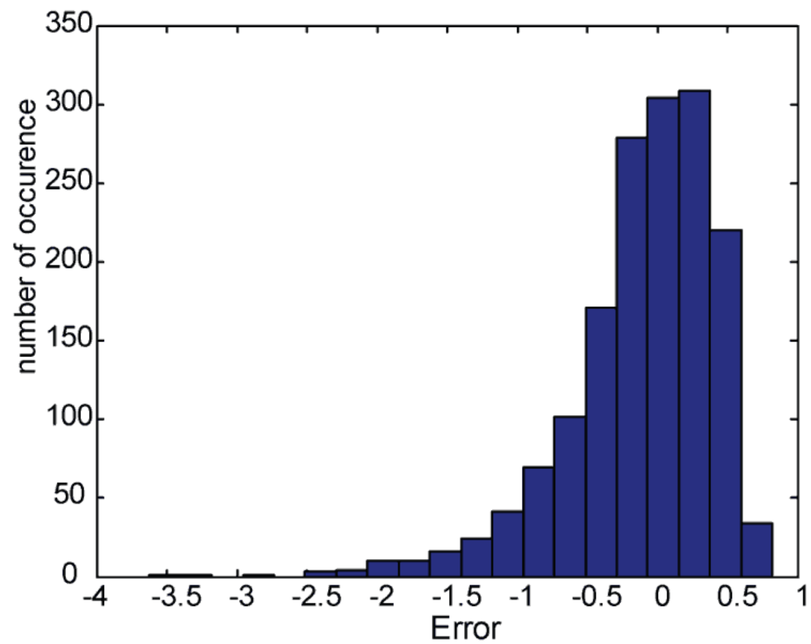


Figure 4.25. Histogram of the error values for the stored data.

4.6 Conclusions

In summary, integrated, hybrid crossbar/CMOS systems have fabricated and successfully characterized. The integrated systems been shown to function well by taking advantage of the intrinsic rectifying I-V characteristics of the switching device itself. Binary bitmap images were successfully stored and retrieved with considerable read margin. A new programming scheme was developed to allow the integrated crossbar array to store up to 10 different levels by eliminating the parallel current paths. These demonstrations suggest that it is possible to build high density storage and neuromorphic systems based purely on passive crossbar arrays without having to incorporate external select devices at each crosspoint [54-57]. This work is also one of the first demonstrations of 3-dimensioanl integration of nanoscale solid-state devices vertically on top of CMOS in a back-end process, and illustrated the possibility of 3D electronics for very high performance memory and logic applications.

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Chapter 5

Development of RRAM Simulation Framework

5.1 Introduction and Motivation

As discussed in the previous chapters, numerous RRAM (memristive) devices have been fabricated and characterized by a large number of groups from academia and industry, and people are starting to understand the mechanisms behind the device operation [1-8]. Like conventional transistor-based system, it is highly recommended to develop device and circuit models for these two-terminal, hysteretic resistive devices before these devices can be used in real-world applications. On the other hand, current simulation software such as SPICE does not offer such a device library. Previous attempts to simulate the memory array or circuit performance have either focused entirely on steady state, with fixed resistances assigned to the on-state or off-state of the devices, or used a fixed threshold voltage, fixed switching time and predetermined on resistance R_{on} with an existing device type (such as a voltage controlled switch) to mimic the resistance switching effect. Unfortunately, these approaches do not correctly characterize the critical dynamic switching effects associated with RRAM devices. In particular, as discussed in Chapters 2 ~ Chapter 3, previous experimental studies have shown that the threshold voltage, switching time and R_{on} are not fixed parameters but rather results from dynamic filament growth effects and vary with different circuit conditions even for the

same device. Therefore, an RRAM simulation component that can capture the dynamics of the device switching process will greatly aid the task of incorporating these important new technologies into circuit designs and help bring the use these devices closer to reality. In this chapter, we discuss our efforts to build one of the first models that can correctly predict all the major dynamic effects associated with the resistive switching devices. The model framework discussed here not only describes the RRAM cells we fabricated, but also serves as a general framework for many similar devices based on different materials.

5.2 General Model Framework

The model is based on the conceptual framework of memristive systems [1,2]. Central to the theory are the two generalized equations given below:

$$y(t) = h(\boldsymbol{s}, x)x(t) \qquad \text{(Eq. 5.1)}$$

$$\frac{d\boldsymbol{s}}{dt} = f(\boldsymbol{s}, x) \qquad \text{(Eq. 5.2)}$$

Equation 5.1 describes the relation between a time varying input, x, and the corresponding output y. h is a generalized transfer function that depends upon both the input and an internal state variable, **s**, which could be a vector representing some set of conditions internal to the device. For resistive devices discussed here, equation 5.1 is simply the usual I-V equation:

$$i(t) = g(\boldsymbol{s}, v)v(t) \qquad \text{(Eq. 5.3)}$$

where $v(t)$ is the arbitrary voltage input to the device, $i(t)$ is current output at time t, $g(\mathbf{s}, v)$ is the generalized conductance, and $\mathbf{s}$ is the state variable, the nature of which will be explained below.

Equation 5.2, on the other hand, is the key that differentiates memristive devices (e.g. devices with hysteresis) from other resistive devices. Unlike for conventional devices whose state is determined by the present input signals such as voltage or current, for a memristive device, the external signals control only the time derivative of the state variable, i.e. $d\mathbf{s}/dt$, and the state of the device is determined only after the time integral of the external signals, leading to a history-dependent, hysteretic behavior. Identifying the state variable and the dynamic equation 5.2 is thus crucial to understanding memristive, restive switching devices. For RRAM, the state variable **s** normally represents the length or width of the conductive (filamentary) region within the active area, and $f(\mathbf{s},x)$ is often a complex, non-linear function that captures the non-linear physical filament growth process occurring during the state transformation. We note that by self-consistently solving equations 5.2 and 5.3, the dynamic behavior of a broad range of resistive switching devices can be accurately predicted without resorting to hand-inserted parameters such as threshold voltage.

5.3 Filament Growth Modeling and Equation Derivation

As discussed in Chapter 3.4, the resistance switching in the a-Si based RRAM devices is caused by metallic Ag filament growth, and the state variable can be represented by the length of the filament, i.e., the increase or decrease of the filament

length changes the device resistance. The filament growth model can then be built based on the physical movement of constituent metal ions in the presence of electric field. In this field-assisted hopping process, metal ion clusters can overcome a hopping barrier and reach a new location, corresponding to the lengthening or shorting of the filament. This physical picture has been used to explain resistive switching effects in RRAMs based on a-Si and other materials [9]. The important rate equation 5.2 can then be derived. For simplicity, it is assumed that the ion moves in one dimension — parallel to the induced electric field. The growth rate of the filament is then determined by the "drift" speed of the leading ions, which can be modeled as a product of the distance travelled in each hop, d, and the frequency with which these hops occur. The latter is given by the attempt frequency, τ_0, scaled by a factor exponentially dependent on the energy barrier height for ion hopping. As schematically shown in figure 5.1 (a), under an applied bias, the apparent barrier height will be reduced from the barrier at zero-bias, U_a. Assuming the field is constant along the distance between the filament tip and the bottom electrode, the barrier will be lowered by $qVd/2(h-l)$; where l is the filament length and h is the overall gap width the filament needs to bridge. As a result, the filament growth rate will be enhanced exponentially as a function of the applied voltage, and the effect was verified recently experimentally [9]. The rate equation can then be derived as:

$$\frac{dl}{dt} = d\tau_0 \left(\exp\left(\frac{-qU_a + \frac{qV \cdot d}{2(h-l)}}{kT} \right) - \exp\left(\frac{-qU_a - \frac{qV \cdot d}{2(h-l)}}{kT} \right) \right) \quad \text{(Eq. 5.4)}$$

This equation is essentially the field-assisted hopping equations found in literature [10]. Or equivalently:

$$\frac{dl}{dt} = 2d\tau_0 \exp\left(\frac{-qU_a}{kT}\right) \sinh\left(\frac{qV\cdot d}{2kT(h-l)}\right) \quad \text{(Eq. 5.5)}$$

Where,

d is the hopping site distance

τ_0 is the characteristic ion hop attempt frequency

U_a is the activation potential

k is Boltzmann´s constant

T is the temperature in Kelvin

q is the charge on an electron

l is the filament length

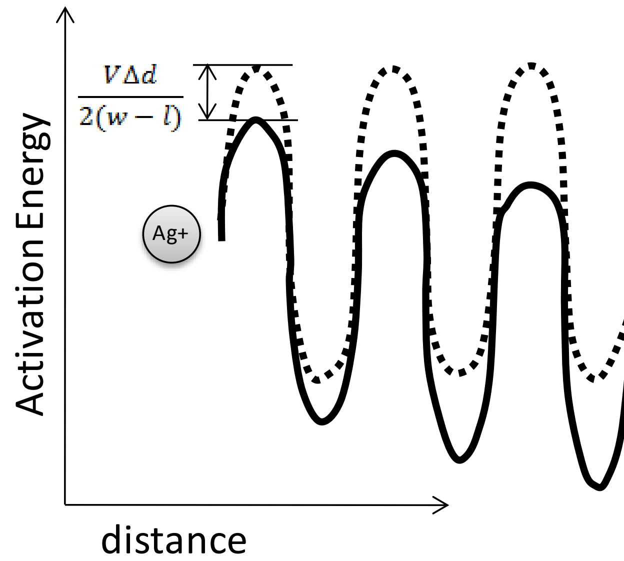
The second exponential term in equation 5.4 is included to account for the probability that the particle will hop backwards, towards the originating electrode.

On the other hand, one should note that equations 5.4 and 5.5 are limited to the voltage ranges such that $U_a - \frac{V\cdot d}{2(h-l)} > 0$. At very high field, such as when V is very large or h-l is very small $U_a - \frac{V\cdot d}{2(h-l)} < 0$, leading to a result that is non-physical. As a result, equation 5.5 will overestimate the filament growth rate at high field. In addition, under very high-field conditions the filament growth may be dominated by other processes instead such as the oxidation of the metal atoms into ions and reduction of the ions back into atoms, rather than drift of the ion at the tip of the filament. At high biases, it is thus reasonable to re-write equation 5.5 as

$$\frac{dl}{dt} = 2d\tau_0 \exp\left(\frac{-qU_a}{kT}\right) \sinh\left(\frac{V}{V_0}\right) \quad \text{(Eq. 5.6)}$$

where V_0 is treated as a free parameter. Equation 5.6 has been demonstrated to reproduce experimental data well such as multi-level storage capability and the apparent threshold effects.

(a)



(b)

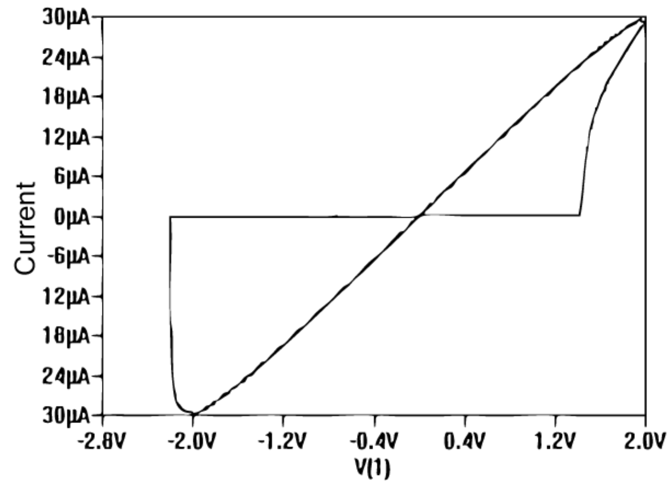


Figure 5.1. The barrier lowering effects in the presence of electric field and simulated I-V sweeps. (a) Barrier lowering effects for hopping in the presence of external electric field. (b) The simulated I-V curves for a RRAM device.

5.4 I-V Equation and Derivation

A number of studies have shown that the resistance changes in RRAM devices are caused by filament growth/retraction within a small distance (e.g. a few nm) of the dielectric/electrode interface. At such small distances when the filament has not bridged the electrodes, the governing current conduction mechanism is electron tunneling through the distance of *h-l*. Such tunneling effects have been well documented and developed previously [11-14]. The basic assumptions for adopting the MIS tunneling model to the RRAM I-V current equation are:

1) After the device has undergone an electroforming process, the nanoscale gap between the tip of the filament and the opposing electrode is expected to be on the order of a few nanometers. At such distances, there is good reason to believe that current is dominated by tunneling [15].
2) The "bulk" of the filament is assumed to be ohmic or is much more conductive than the region between the tip of the filament and the opposing electrode.

Based on the above assumptions the device I-V characteristics can be expressed using a tunneling current through a square barrier [14]: (Detailed derivation of this equation is explained in appendix.)

$$\mathrm{I} = \mathrm{A}\frac{4q\pi m(kT)^2}{{h_0}^3}\exp(-b_1)\frac{1}{(c_1kT)^2}\frac{\pi c_1 kT}{\sin(\pi c_1 kT)}(1 - \exp(c_1 qV)) \qquad \text{(Eq. 5.7)}$$

Where

$$b_1 = \begin{cases} \dfrac{2\alpha(h-l)\sqrt{q}}{3V}\left(\phi_0^{\frac{3}{2}} - (\phi_0 - V)^{\frac{3}{2}}\right) & \text{if } V < \phi_0 \\ \dfrac{2\alpha(h-l)\sqrt{q}}{3V}\phi_0^{\frac{3}{2}} & \text{if } V > \phi_0 \end{cases},$$

$$c_1 = \begin{cases} \dfrac{\alpha(h-l)}{V\sqrt{q}}\left(\phi_0^{\frac{1}{2}} - (\phi_0 - V)^{\frac{1}{2}}\right) & \text{if } V < \phi_0 \\ \dfrac{\alpha(h-l)}{V\sqrt{q}}\phi_0^{\frac{1}{2}} & \text{if } V > \phi_0 \end{cases},$$

A is the filament area

m is the effective electron mass

h_0 is planks constant

ϕ_0 is the barrier height with zero applied bias

and

$$\alpha = \frac{2\sqrt{2m}}{\hbar}.$$

To reduce the computational complexity for circuit modeling, the tunneling expression was simplified to

$$I = A \cdot q \frac{8\pi^2 m}{{h_0}^3} \frac{kT}{c_1 \sin(\pi c_1 kT)} \qquad V < \phi_0 \qquad \text{(Eq. 5.8a)}$$

$$I = A \cdot \frac{4\pi q^2 m}{{h_0}^3 \alpha^2 \phi_0} \left(\frac{V}{h - l}\right)^2 e^{-\frac{2\alpha\sqrt{q}(h-l){\phi_0}^{3/2}}{3V}} \qquad V > \phi_0 \qquad \text{(Eq. 5.8b)}$$

This simplification has been verified to produce good approximations in comparison with the full expression equation 5.7 within the relevant parameter space of the RRAM operation.

5.5 Simulation Results and Discussion

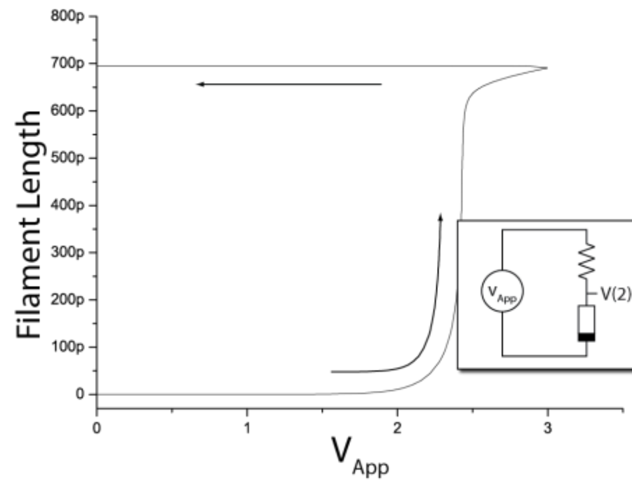
Equations 5.6 and 5.8 are specific forms of equations 5.1 and 5.2 in the memristor model and provide the framework to predict the RRAM characteristics. In addition, the RRAM device can be incorporated into a circuit so the voltage across it is further determined by the loading effect. For example, when the device is connected in series with other components (such as a static resistor in the inset of figure 5.2 (a)) or programmed with a current compliance, the voltage dropped across the device V_{ex} is no longer a constant and must be solved for self-consistently.

We were able to validate the model by comparing simulation results to previously reported experimental data [1, 9]. For example, figure 5.1 (b) shows the simulation results when an RRAM cell is programmed with a DC voltage sweep with a 50 KΩ series resistor. One can readily recognize the hysteretic loop and the apparent

threshold voltages related to the sharp resistance switching featured in figure 5.1 (b). In particular, we want to emphasize that only continuous equations were used, and the apparent threshold effect is in fact an artifact from the extremely non-linear exponential dependence of the growth rate on voltage as well as the tunneling currents. Due to the dynamic nature of the processes, the apparent threshold voltage is not fixed but depends on the sweep rate, as verified by both simulation and experimental data.

Further, we were able to gain insight into the dynamics of the switching event even when it may occur on a timescale that is difficult to observe experimentally and utilize such understandings to optimize the device operation. For example, figure 5.2 (a) shows the filament dynamics when an RRAM device is placed in series with a voltage source and a linear resistor R_s; the insert in figure 5.2 (a) illustrates the circuit schematic. Figure 5.2 (a) shows the filament length over time. Initially the potential across the cell follows that of the applied voltage and causes the device to switch at 2.3 V. As the device becomes less resistive, however, a voltage divider is formed between the RRAM cell and the series resistance. This has the effect of reducing the voltage across the RRAM cell (figure 5.2 (b)), retarding further filament growth. Eventually the resistance of the cell stabilizes at a value that is dependent on Rs, consistent with the experimental results discussed in Chapter 3.7. Similar effects were also observed with the application of nanosecond scale pulses. These simulations further verified the mechanism behind multi-level storage in these devices and will be used to guide continued device optimization.

(a)



(b)

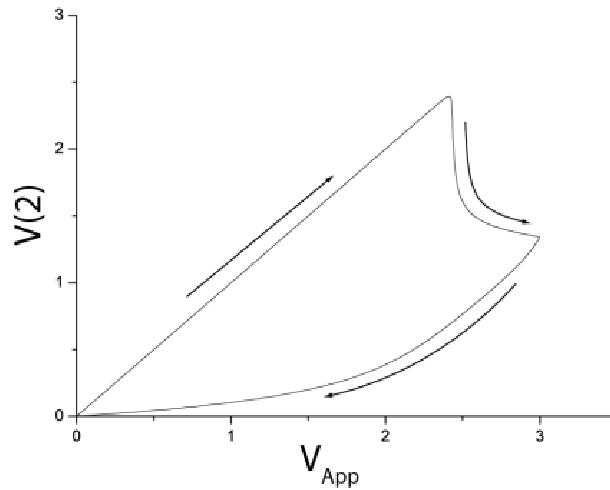


Figure 5.2. The filament growth and internal voltage across the switch element in series with series resistor. (a) Captured filament growth during switching (b) The voltage across the switching device as a function of external applied voltage V_{app}. After switching, the voltage across the switching device drops suddenly, self-liming the filament growth process.

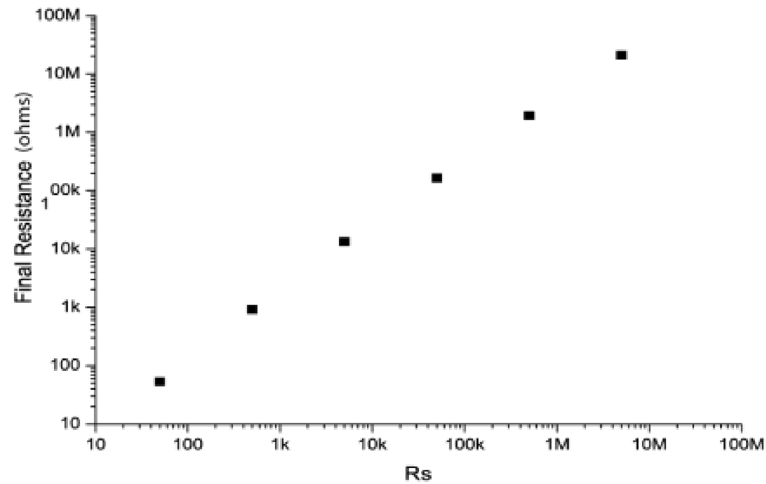


Figure 5.3. Simulated multilevel characteristics as function of series resistance value. The strong correlation between the series resistance and the final device resistance has been captured.

5.6 Conclusion

In this chapter, we discussed a framework to model RRAM devices by deriving and self-consistently solving the I-V and rate growth equations. The filament growth and rupture has been modeled with the field-assistant hopping picture. This model can accurately reproduce not only static but also dynamic behaviors of the RRAM devices observed experimentally. This modeling work in turn reveals the physical insight on the device operation. The model can be readily incorporated into conventional simulation tools and will provide a pathway to simulation of complicated circuit operation with these nanoscale resistance switching devices under real-world conditions.

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Chapter 6

Summary and Further Work

6.1 Development of High Density Crossbar Array and Measurement System

In chapter 2, a-Si based RRAM which had been verified as a very promising memory element in terms of fast switching time, long retention, and robust endurance characteristics [1-2] was demonstrated in the form of high-density crossbar memory. Fabrication of high density crossbar array with 1 Kbits and 2.5 Gbits/cm^2 was successfully performed with the aid of e-beam lithography and planarization techniques. Two different types of measurement systems, e.g. probe card/switch matrix system and PCB board based system were employed to characterize the high density crossbar array. The measurements results show the array still reproduces merits of individual a-Si based RRAM such as high yield ($>$ 98%), fast switching ($<$ 50 ns), and good endurance ($> 10^6$ cycles). In addition, a simple word, e.g. “CrossBar” represented by ASCII code was written into and retrieved from the prototype 8×8 crossbar array. Although the feasibility of a-Si based crossbar array as a promising memory was demonstrated in this chapter, inherent merits of crossbar such as random access and high packing density are still restricted due to the so-called “sneak path” problem. In the next chapter intrinsically rectifying I-V characteristics of a-Si based RRAM obtained by highly-

engineered interface between the a-Si switching layer and the poly-Si bottom electrode was exploited and characterized in order to cope with the "sneak path" problem.

6.2 Inherently Rectifying I-V Characteristics of a-Si Based RRAM

In chapter 3, devices in which the a-Si switching layer was shaped into pillar shapes with well-controlled a-Si/poly-Si interfaces were studied. This particular structure exhibited very narrow switching voltage distribution and more interestingly, rectifying I-V curve at on-state. The current flowing through on-state memory at negative bias was suppressed to 10^{-13}A, exhibiting rectifying ratio > 10^6. This unique feature has several advantages to solve the sneak path problem over other proposed strategies such as integrating an external rectifying element in series with the memory element [3] and using complementary memory configuration [4]. It is noteworthy that this intrinsic rectifying characteristic persists in the sub 50 nm regime of cell size and can be fully utilized in crossbar array operation. In addition, the retention characteristics (> 4.6years at room temperature) and endurance characteristics (> 10^8 cycles) of the fabricated pillar-type a-Si based RRAM were very desirable for non-volatile memory applications.

6.3 On-chip Integration of High-Density Crossbar Array with CMOS Decoder

In chapter 4, fabrication and characterization of high-density crossbar arrays with 1.6 Kbits and 10 Gbits/cm^2 directly on top of CMOS decoder circuits were discussed. Real crossbar array operations, which have not been fully developed and implemented in

the past due to the "sneak path" problem and cell uniformity problems, were successfully demonstrated by exploiting the unique intrinsically rectifying I-V characteristics of a-Si based RRAM and through a new programming scheme. The fabricated crossbar array with 1.6 Kbits successfully demonstrated storage and retrieval of bitmap images with 40 by 40 pixels. Separation of on-state resistance and off-state resistance by at least 20 times leads to the clear bitmap image reconstruction. In addition, multilevel storage and retrieval operations were also achieved by preventing the current bifurcation at the half-selected word line in the new programming scheme. Although pronounced noise in the reconstructed image was observed, the level of noise is considered bearable for neuromorphic applications when the level is compared to biological system.

6.4 Development of Simulation Framework for RRAM

In chapter 5, the two major governing equations for describing switching phenomena of RRAM were derived. First, the rate equation which models the growth of the conducting filament was derived based on field-assisted ion hopping theory. Second, I-V equation which calculates current across the device at applied bias was derived based on tunneling current through square potential barrier. By combining the two governing equations, the dynamics of the device can be naturally predicted such as the exponential dependency in switching time on the applied voltage and multilevel switching.

6.5 Multiple Layers Stacking of High-Density Crossbar Array

One natural project to follow up with is to use multiple stacks of crossbars to further improve the memory density [5], as schematically shown in figure 6.1. This type of 3D integration can in principle reduce the cell size from $4F^2$ to $4F^2/n$, where n is the number of layers, and offers a plausible approach to keep density scaling when size scaling has reached a limit, e.g. when F approaches 10 nm. The current a-Si based RRAM has Ag electrode as the top electrode which may be thermally-agglomerated at high temperature, e.g. during SiGe deposition for the next stack. However, this agglomeration problem can be significantly suppressed with a passivation that can hold Ag electrode in shape. New materials or new fabrication schemes can be developed and will give a pathway to overcome the present fabrication issues and enable the multilayer stacking of a-Si based RRAM. In this approach, all the CMOS control and I/O components will be at the bottom substrate layer since CMOS devices, relying on the crystalline Si substrate for channel formation, cannot be readily built into the multi-stack. Additional challenges that need be addressed include how to connect individual devices in different layers to the CMOS components without increasing the area overhead. With the very high storage density and large interconnectivity, this multilayer system can also be used for both very high density data storage (e.g. terabit and beyond) and neuromorphic system fabrication analogous to biological systems [6].

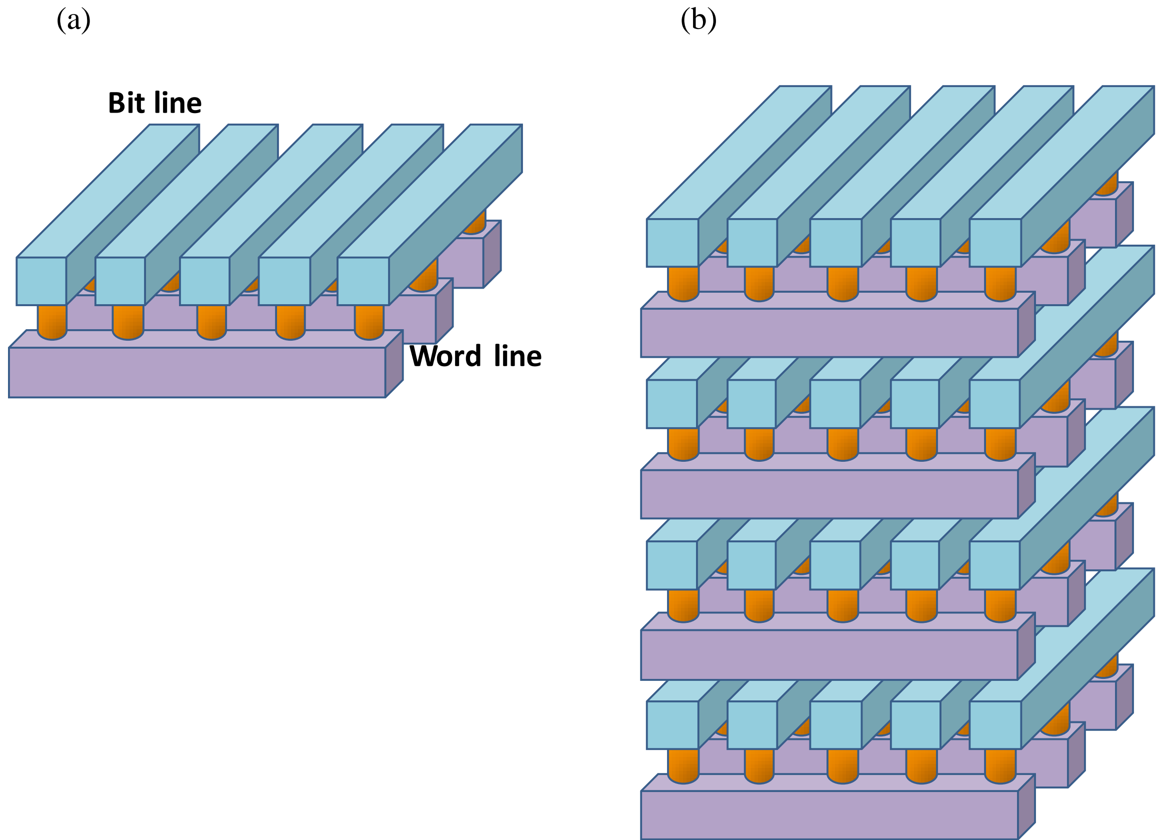

Figure 6.1. (a) conventional crossbar memory array with 1 layer of active devices and (b) multi-stack memory.

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Appendix

The current density in the x-direction due to electron tunneling from a conducting region 1 to a conducting region 2, through the forbidden energy gap of an insulator or semiconductor, is derived by Price and Radcliffe [1-2].

$$j = q\frac{4\pi m}{h^3}\int_0^\infty dE\{f_1(E) - f_2(E)\}\int_0^E P(E_x)dE_x$$

Where,

$$\ln P(E_x) = -\alpha\int_{x_1}^{x_2}\sqrt{q\phi - E_x}\,dx, \alpha = \frac{2\sqrt{2m}}{\hbar}$$

q is the charge on the electron, E is the electron energy, $f_1(E)$ and $f_2(.E)$ are the Fermi Dirac distribution functions in the two conducting regions, p_x, and p_y, are the quasi-electron momentum components normal to the direction of the current flow, p_y is the quasi-electron moment components in the direction of the current flow, and $P(E_x)$ is the ratio of the transmitted to the incident current or transition probability.

Taylor expansion of $P(E_x)$ near Fermi level was expressed below with $\varepsilon_x = \xi_1 - E_x$

$(\varepsilon_x = \xi_1 - E_x = 0)$

$$-\ln P(E_x) = b_1 + c_1\varepsilon_x + f_1\varepsilon_x^2 + \ldots$$

$$-\ln P(E_x) = \alpha \int_{x_{11}}^{x_{21}} \sqrt{q\phi - \xi_1 + \varepsilon_x}\, dx = \alpha \int_{x_{11}}^{x_{21}} \sqrt{q\phi - \xi_1} \sqrt{1 + \frac{\varepsilon_x}{q\phi - \xi_1}}\, dx$$

$$= \alpha \int_{x_{11}}^{x_{21}} \sqrt{q\phi - \xi_1} [1 + \frac{\varepsilon_x}{2(q\phi - \xi_1)} + \frac{1}{2}\frac{1}{2}(-\frac{1}{2}) \frac{\varepsilon_x{}^2}{(q\phi - \xi_1)^2} + ...] dx$$

$$\Rightarrow b_1 = \alpha \int_{x_{11}}^{x_{21}} \sqrt{q\phi - \xi_1}\, dx$$

$$\Rightarrow c_1 = \frac{\alpha}{2} \int_{x_{11}}^{x_{21}} \frac{1}{\sqrt{q\phi - \xi_1}}\, dx$$

$$\Rightarrow f_1 = -\frac{\alpha}{8} \int_{x_{11}}^{x_{21}} \frac{1}{(q\phi - \xi_1)^{\frac{3}{2}}}\, dx$$

x_{11} and x_{21} are the classic turning points between conducting region 1 and region 2 for electron with energy $E_x = \xi_1$.

Perform the integral in the current density equation derived by Price and Radcliffe [1-2] with only b1 and c1 kept in $P(E_x)$.

$$j = q\frac{4\pi m}{h^3} \int_0^\infty dE\{f_1(E) - f_2(E)\} \int_0^E P(E_x) dE_x = q\frac{4\pi m}{h^3} \int_{E_x}^\infty dE\{f_1(E) - f_2(E)\} \int_0^\infty P(E_x) dE_x$$

$$= q\frac{4\pi mkT}{h^3} \int_0^\infty P(E_x) dE_x \times \ln(\frac{1 + e^{(\xi_1 - E_x)/kT}}{1 + e^{(\xi_1 - E_x - qV)/kT}})$$

$$\because \int_{E_x}^{\infty} dE\{f_1(E)-f_2(E)\} = \int_{E_x}^{\infty} dE\{\frac{1}{1+e^{(E-\xi_1)/kT}} - \frac{1}{1+e^{(E-\xi_2)/kT}}\}$$

$$= [-kT\ln(1+e^{(\xi_1-E)/kT})]-[-kT\ln(1+e^{(\xi_2-E)/kT})]|_{E_x}^{\infty}$$

$$= kT\ln(\frac{1+e^{(\xi_2-E)/kT}}{1+e^{(\xi_1-E)/kT}})|_{E_x}^{\infty}$$

$$= kT\ln(\frac{1+e^{(\xi_1-E_x)/kT}}{1+e^{(\xi_2-E_x)/kT}})$$

$$= kT\ln(\frac{1+e^{(\xi_1-E_x)/kT}}{1+e^{(\xi_1-E_x-qV)/kT}}), \xi_2 = \xi_1 - qV$$

Plug $-\ln P(E_x) = b_1 + c_1\varepsilon_x$ into above equation and integrate,

$$j = q\frac{4\pi mkT}{h^3}\int_0^{\infty} P(E_x)dE_x \times \ln(\frac{1+e^{(\xi_1-E_x)/kT}}{1+e^{(\xi_1-E_x-qV)/kT}})$$

$$= q\frac{4\pi mkT}{h^3}\int_0^{\infty} e^{-b_1-c_1\varepsilon_x}dE_x \times \ln(\frac{1+e^{(\xi_1-E_x)/kT}}{1+e^{(\xi_1-E_x-qV)/kT}})$$

$$= q\frac{4\pi mkT}{h^3}e^{-b_1}[\int_0^{\infty} e^{c_1(E_x-\xi_1)}\ln(1+e^{(\xi_1-E_x)/kT})dE_x - e^{-c_1qV}\int_0^{\infty} e^{c_1(E_x-\xi_1+qV)}\ln(1+e^{(\xi_1-E_x-qV)/kT})dE_x]$$

Evaluate integral $\int_0^{\infty} e^{c_1(E_x-\xi_1)}\ln(1+e^{(\xi_1-E_x)/kT})dE_x$

$$\int_0^{\infty} e^{c_1(E_x-\xi_1)}\ln(1+e^{(\xi_1-E_x)/kT})dE_x = kT\int_{-\xi_1/k_BT}^{+\infty} e^{c_1kTE}\ln(1+e^{-E})dE$$

$$\approx kT\int_{-\infty}^{+\infty} e^{c_1kTE}\ln(1+e^{-E})dE$$

$$= \frac{kT}{c_1kT}[e^{c_1kTE}\ln(1+e^{-E})|_{-\infty}^{+\infty} - \int_{-\infty}^{+\infty} -e^{c_1kTE}\frac{dE}{1+e^{-E}}]$$

$$= \frac{1}{c_1}\int_{-\infty}^{+\infty}\frac{e^{c_1kTE}dE}{1+e^{-E}} = \frac{1}{c_1}\int_0^{+\infty}\frac{\beta^{-c_1kT-1}d\beta}{1+\beta}, \beta = e^{-E}$$

From the equation (55) in ref [3], note that

$$\int_0^{+\infty} \frac{x^{a-1}dx}{1+x} = \frac{\pi}{\sin(\pi a)}, \text{ if } \operatorname{Re}[a] < 1$$

Then,

$$\int_0^{\infty} e^{c_1(E_x-\xi_1)} \ln(1+e^{(\xi_1-E_x)/kT})dE_x = \frac{1}{c_1}\frac{\pi}{\sin(\pi c_1 kT)}$$

So, tunneling current becomes

$$j = q\frac{4\pi mkT}{h^3}e^{-b_1}[\int_0^{\infty} e^{c_1(E_x-\xi_1)}\ln(1+e^{(\xi_1-E_x)/kT})dE_x - e^{-c_1qV}\int_0^{\infty} e^{c_1(E_x-\xi_1+qV)}\ln(1+e^{(\xi_1-E_x-qV)/kT})dE_x]$$

$$= q\frac{4\pi mkT}{h^3}e^{-b_1}[\frac{1}{c_1}\frac{\pi}{\sin(\pi c_1 kT)} - e^{-c_1qV}\frac{1}{c_1}\frac{\pi}{\sin(\pi c_1 kT)}]$$

$$= q\frac{4\pi mkT}{h^3}e^{-b_1}\frac{1}{c_1}\frac{\pi}{\sin(\pi c_1 kT)}[1-e^{-c_1qV}]$$

$$= q\frac{4\pi m(kT)^2}{h^3}e^{-b_1}\frac{1}{(c_1kT)^2}\frac{\pi c_1 kT}{\sin(\pi c_1 kT)}(1-e^{-c_1qV})$$

Square barrier case:

Low bias

$$\phi = \phi_b - \frac{V}{L}x, V < \phi_b$$

$$b_1 = \alpha\int_{x_{11}}^{x_{21}}\sqrt{q\phi-\xi_1}\,dx = \alpha\int_0^L\sqrt{q(\phi_b-\frac{V}{L}x)}\,dx = \frac{2\alpha L\sqrt{q}}{3V}[\phi_b^{\frac{3}{2}} - (\phi_b - V)^{\frac{3}{2}}]$$

$$c_1 = \frac{\alpha}{2}\int_{x_{11}}^{x_{21}} \frac{1}{\sqrt{q\phi - \xi_1}} dx = \frac{\alpha}{2}\int_0^L \frac{1}{\sqrt{q(\phi_b - \frac{V}{L}x)}} dx = \frac{\alpha L}{V\sqrt{q}}[\phi_b^{\frac{1}{2}} - (\phi_b - V)^{\frac{1}{2}}]$$

High bias

$$\phi = \phi_b - \frac{V}{L}x, V > \phi_b, 0 < x < l, l = \phi_b \frac{L}{V}$$

$$b_1 = \alpha\int_{x_{11}}^{x_{21}} \sqrt{q\phi - \xi_1} dx = \alpha\int_0^l \sqrt{q(\phi_b - \frac{V}{L}x)} dx = \frac{2\alpha L\sqrt{q}}{3V}\phi_b^{\frac{3}{2}}$$

$$c_1 = \frac{\alpha}{2}\int_{x_{11}}^{x_{21}} \frac{1}{\sqrt{q\phi - \xi_1}} dx = \frac{\alpha}{2}\int_0^L \frac{1}{\sqrt{q(\phi_b - \frac{V}{L}x)}} dx = \frac{\alpha L}{V\sqrt{q}}\phi_b^{\frac{1}{2}}$$

To reduce the computational complexity for circuit modeling, the tunneling expression was simplified to

Low bias,

$$b_1 = \alpha\int_{x_{11}}^{x_{21}} \sqrt{q\phi - \xi_1} dx = \alpha\int_0^L \sqrt{q(\phi_b - \frac{V}{L}x)} dx = \frac{2\alpha L\sqrt{q}}{3V}[\phi_b^{\frac{3}{2}} - (\phi_b - V)^{\frac{3}{2}}]$$

$$= \frac{2\alpha L\sqrt{q}}{3V}\phi_b^{\frac{3}{2}}[1 - (1 - \frac{V}{\phi_b})^{\frac{3}{2}}] \approx \frac{2\alpha L\sqrt{q}}{3V}\phi_b^{\frac{3}{2}}[1 - (1 - \frac{3}{2}\frac{V}{\phi_b} + \frac{3}{8}(\frac{V}{\phi_b})^2)]$$

$$= \frac{2\alpha L\sqrt{q}}{3V}\phi_b^{\frac{3}{2}}[\frac{3}{2}\frac{V}{\phi_b} - \frac{3}{8}(\frac{V}{\phi_b})^2] = \alpha L\sqrt{q\phi_b} - \frac{\alpha LV}{4}\sqrt{\frac{q}{\phi_b}}$$

$$c_1 = \frac{\alpha}{2}\int_{x_{11}}^{x_{21}} \frac{1}{\sqrt{q\phi - \xi_1}}dx = \frac{\alpha}{2}\int_0^L \frac{1}{\sqrt{q(\phi_b - \frac{V}{L}x)}}dx = \frac{\alpha L}{V\sqrt{q}}[\phi_b^{\frac{1}{2}} - (\phi_b - V)^{\frac{1}{2}}]$$

$$= \frac{\alpha L}{V\sqrt{q}}\phi_b^{\frac{1}{2}}[1-(1-\frac{V}{\phi_b})^{\frac{1}{2}}] = \frac{\alpha L}{V\sqrt{q}}\phi_b^{\frac{1}{2}}[1-(1-\frac{V}{2\phi_b})] = \frac{\alpha L}{2\sqrt{q\phi_b}}$$

$$\Rightarrow j = q\frac{4\pi m(kT)^2}{h^3}e^{-b_1}\frac{1}{(c_1kT)^2}\frac{\pi c_1 kT}{\sin(\pi c_1 kT)}$$

$$= q\frac{4\pi m(kT)^2}{h^3}\frac{1}{(c_1kT)^2}\frac{\pi c_1 kT}{\sin(\pi c_1 kT)}e^{-b_1}(1-e^{-c_1 qV})$$

$$\approx q\frac{4\pi m(kT)^2}{h^3}\frac{1}{(c_1kT)^2}\frac{\pi c_1 kT}{\sin(\pi c_1 kT)}e^{-\alpha L\sqrt{q\phi_b}+\frac{\alpha LV}{4}\sqrt{\frac{q}{\phi_b}}}(1-e^{-\frac{\alpha L}{2\sqrt{q\phi_b}}qV})$$

$$= q\frac{4\pi m(kT)^2}{h^3}\frac{1}{(c_1kT)^2}\frac{\pi c_1 kT}{\sin(\pi c_1 kT)}e^{-\alpha L\sqrt{q\phi_b}}e^{\frac{\alpha LV}{4}\sqrt{\frac{q}{\phi_b}}}(1-e^{-\frac{\alpha LV}{2}\sqrt{\frac{q}{\phi_b}}})$$

$$= q\frac{8\pi m(kT)^2}{h^3}\frac{1}{(c_1kT)^2}\frac{\pi c_1 kT}{\sin(\pi c_1 kT)}e^{-\alpha L\sqrt{q\phi_b}}\sinh(\frac{\alpha LV}{4}\sqrt{\frac{q}{\phi_b}})$$

$$= \frac{16kT\pi^2 mq\sqrt{q\phi_b}}{\alpha L h^3\sin(\frac{\pi\alpha LkT}{2\sqrt{q\phi_b}})}e^{-\alpha L\sqrt{q\phi_b}}\sinh(\frac{\alpha LV}{4}\sqrt{\frac{q}{\phi_b}})$$

High bias, assume field is given by $F = V/L$.

$$b_1 = \alpha\int_{x_{11}}^{x_{21}}\sqrt{q\phi - \xi_1}dx = \alpha\int_0^l \sqrt{q(\phi_b - \frac{V}{L}x)}dx = \frac{2\alpha L\sqrt{q}}{3V}\phi_b^{\frac{3}{2}} = \frac{2\alpha\sqrt{q}\phi_b^{\frac{3}{2}}}{3F}$$

$$c_1 = \frac{\alpha}{2}\int_{x_{11}}^{x_{21}} \frac{1}{\sqrt{q\phi - \xi_1}}dx = \frac{\alpha}{2}\int_0^L \frac{1}{\sqrt{q(\phi_b - \frac{V}{L}x)}}dx = \frac{\alpha L}{V\sqrt{q}}\phi_b^{\frac{1}{2}} = \frac{\alpha\phi_b^{\frac{1}{2}}}{F\sqrt{q}}$$

And $c_1kT = \frac{\alpha L}{V\sqrt{q}}\phi_b^{\frac{1}{2}}kT \to 0$, so that $\sin(\pi c_1 kT) \to \pi c_1 kT$

$$\Rightarrow j = q\frac{4\pi m(kT)^2}{h^3}e^{-b_1}\frac{1}{(c_1kT)^2}\frac{\pi c_1 kT}{\sin(\pi c_1 kT)}$$

$$\approx q\frac{4\pi m}{h^3}\frac{1}{c_1^{\ 2}}e^{-b_1}(1-e^{-c_1 qV})$$

$$= q\frac{4\pi m}{h^3}\left(\frac{F\sqrt{q}}{\alpha\phi_b^{\frac{1}{2}}}\right)^2 e^{-\frac{2\alpha\sqrt{q}\phi_b^{\frac{3}{2}}}{3F}}\left(1-e^{-\frac{\alpha L\phi_b^{\frac{1}{2}}}{V\sqrt{q}}qV}\right)$$

$$= q\frac{4\pi m}{h^3}\frac{q}{\alpha^2\phi_b}F^2 e^{-\frac{2\alpha\sqrt{q}\phi_b^{\frac{3}{2}}}{3F}}\left(1-e^{-\alpha L\sqrt{q\phi_b}}\right)$$

$$\approx \frac{4\pi mq^2}{h^3\alpha^2\phi_b}F^2 e^{-\frac{F_0}{F}}, F_0 = \frac{2\alpha\sqrt{q}\phi_b^{\frac{3}{2}}}{3}$$

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