a-InGaZnO thin-film transistors for AMOLEDs: Electrical stability and pixel-circuit simulation

Charlene Chen (SID Student Member)
Katsumi Abe
Hideya Kumomi
Jerzy Kanicki (SID Member)

Abstract — Inverted-staggered amorphous In–Ga–Zn–O (a-InGaZnO) thin-film transistors (TFTs) were fabricated and characterized on glass substrates. The a-InGaZnO TFTs exhibit adequate field-effect mobilities, sharp subthreshold slopes, and very low off-currents. The current temperature stress (CTS) on the a-InGaZnO TFTs was performed, and the effect of stress temperature (T_{STR}), stress current (I_{STR}), and TFT biasing condition on their electrical stability was investigated. Finally, SPICE modelling for a-InGaZnO TFTs was developed based on experimental data. Several active-matrix organic light-emitting-display (AMOLED) pixel circuits were simulated, and the potential advantages of using a-InGaZnO TFTs were discussed.

Keywords — *Amorphous In–Ga–Zn–O (a-InGaZnO), thin-film transistor (TFT), current temperature stress (CTS), active-matrix organic light-emitting display (AMOLED).*

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1 Introduction

Active-matrix organic light-emitting displays (AMOLEDs) are now generally viewed as the next-generation display because of their vivid color, high contrast ratio, thin/light module, and low energy consumption.[1,2] Although hydrogenated amorphous-silicon (a-Si:H) thin-film transistors (TFTs) currently dominate the liquid-crystal-display (LCD) market due to their uniformity over large area, low cost of fabrication, and mature technology, the insufficient field-effect mobility and metastable shift in threshold voltage when subject to prolonged gate bias[3,4] make their application to AMOLEDs rather difficult. [In AMOLEDs, the drive TFT has to constantly supply a current to the organic light-emitting diode (OLED) instead of just acting like a switch.] Larger devices and more-complex pixel circuits are needed to realize acceptable a-Si:H TFT AMOLEDs, which greatly limits the display resolution.[5,6] As a result, TFTs based on other semiconductor materials have been explored as an alternative approach to realize reliable, high-resolution AMOLEDs.[7–9] Above all, amorphous In–Ga–Zn–O (a-InGaZnO) TFTs possess certain advantages including visible transparency, low processing temperature, good uniformity, adequate mobility, low off-current, sharp subthreshold swing, and potentially better electrical stability, which make them very attractive for AMOLEDs.[9–11] Several a-InGaZnO TFT AMOLEDs have already been demonstrated by other groups, indicating a promising future for these devices.[12,13] In this paper, we described properties of a-InGaZnO TFTs fabricated on glass substrates and studied their electrical stability by performing current temperature stress (CTS) measurements. The effect of stress temperature (T_{STR}), stress current (I_{STR}), and TFT-biasing conditions on the electrical properties of a-InGaZnO TFTs were investigated. Finally, an a-InGaZnO TFT SPICE model was developed, based on experimental data. We simulated several voltage- and current-programmed a-InGaZnO TFT AMOLED pixel circuits and analyzed their advantages over a-Si:H TFTs.

2 TFT fabrication and characterization

The a-InGaZnO TFTs were fabricated on glass substrates. The gate electrode Ti (5 nm)/Au (40 nm)/Ti (5 nm) was deposited by electron-beam deposition and patterned by lift-off. The gate insulator SiO_2 (200 nm) and a-InGaZnO thin film were both deposited by RF sputtering and patterned by wet etching. After annealing in air at 300°C for 20 minutes, the source/drain electrodes Ti (5 nm)/Au (100 nm)/Ti (5 nm) were deposited by electron-beam deposition and patterned by lift-off. A SiO_2 film as the back-channel protection layer (100 nm) was deposited by RF sputtering and patterned by wet etching. Finally, the TFTs were annealed in air at 200°C for 1 hour.[14] Electrical measurements were performed in the dark using a Hewlett-Packard 4156A semiconductor parameter analyzer. The measured TFT transfer and output characteristics are shown in Fig. 1. The a-InGaZnO TFTs exhibit very low off-current, a sharp subthreshold swing (0.4 V/dec), a threshold voltage (V_T) of ~3 V, and field-effect mobility (μ) of ~10 cm^2/V-sec. V_T and μ were extracted by linearly fitting the I_D–V_{GS} curve to the standard MOSFET equation. The fitting range was chosen to be between 10% and 90% of the maximum measured I_D (V_{GS} = 20 V).[15]

C. Chen and J. Kanicki are with the Department of Electrical Engineering and Computer Science, The University of Michigan, 1301 Beal Ave., Ann Arbor, MI 48109; telephone 734/936-0964, fax 734/615-2843, e-mail: kanicki@umich.edu.

K. Abe and H. Kumomi are with Canon Research Center, Inc., Tokyo, Japan.

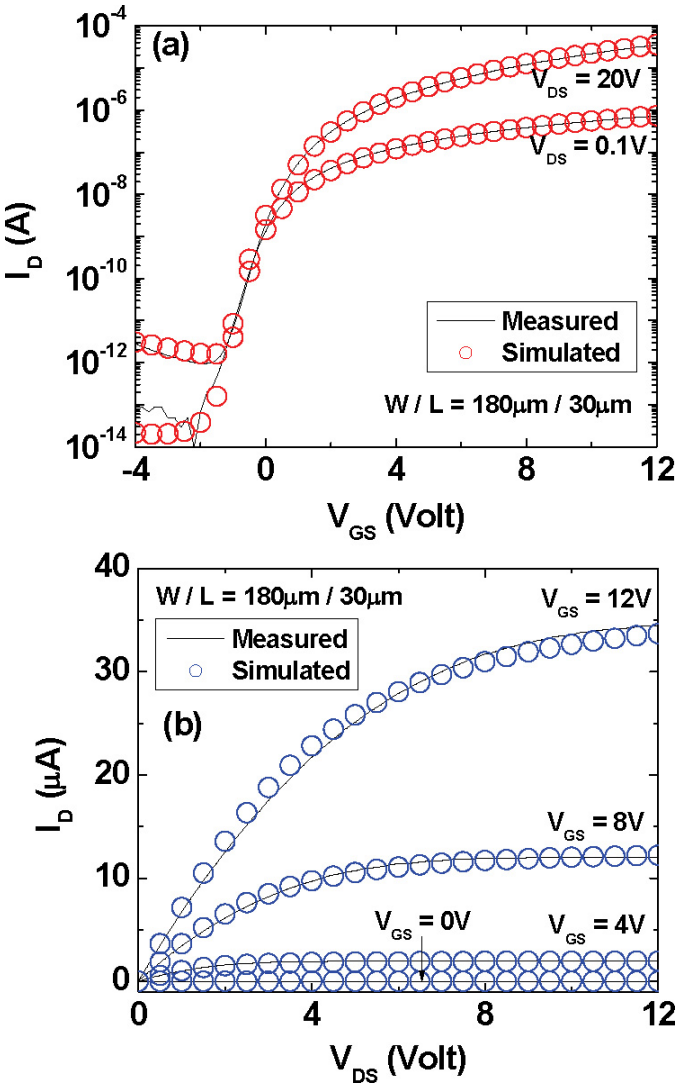

FIGURE 1 — Measured and simulated (using HSPICE) a-InGaZnO TFT (a) transfer and (b) output characteristics.

3 Current temperature stress (CTS) study

3.1 CTS measurement setup

Current temperature stress (CTS) measurements were performed in the dark by using a Hewlett-Packard 4156A semiconductor parameter analyzer. The device temperature was

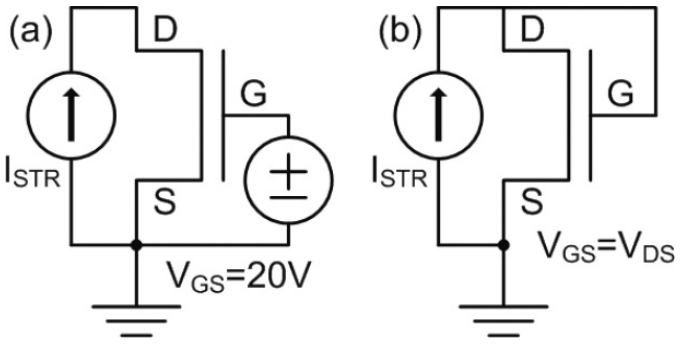

FIGURE 2 — The two CTS measurement setups (stress mode) used in this study (a) CTS_lin (V_{GS} = 20 V) and (b) CTS_sat (V_{GS} = V_{DS}).

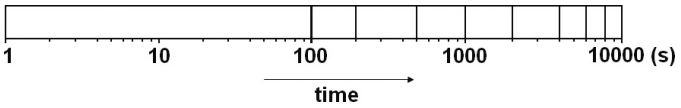

FIGURE 3 — The CTS was performed on a single TFT for a total of 10,000 sec. The white space indicates the stress mode; the black lines indicate when the stress mode is interrupted and switched to the sweep mode (Ref. 17).

regulated by a heated chuck and a Signatone temperature controller with a precision of 0.1 K. Before each measurement, the TFTs were placed on the heated chuck which is set at the desired measurement temperature for 30 minutes to allow for thermal equilibrium.

We used two different stress schemes for the CTS measurements: CTS_lin and CTS_sat.[16,17] CTS_lin and CTS_sat are equivalent to operating the TFT in the linear and saturation regimes, respectively. For CTS_lin, during the stress mode, the gate was biased at 20 V while a stress current (I_{STR}) was applied to the drain of the TFTs, as shown in Fig. 2(a). The same TFT were stressed for a total stress time (t_{STR}) of 10,000 sec, as illustrated in Fig. 3. At certain times (t_{STR} = 100, 200, 500, 1000, 2000, 4000, 6000, 8000, and 10,000 sec), the stress mode was interrupted and switched to the sweep mode where a quick gate voltage sweep (V_{GS} = –5 → 20 V) was applied to measure the transfer characteristic in the saturation regime of operation (V_{DS} = 20 V). For CTS_sat, during the stress mode, the gate and drain were externally shorted together, and I_{STR} was applied to the drain, setting the voltages at the gate/drain (V_{GS} = V_{DS}), as shown in Fig. 2(b). The total stress time and number of points when the stress mode was interrupted are the same as CTS_linear. In the sweep mode, the gate/drain voltages (V_{GS} = V_{DS}) were swept from –5 to 20 V to measure the transfer characteristics in the saturation regime. The same measurement procedure described above was repeated for several levels of stress current (I_{STR}) and stress temperature (T_{STR}) for both CTS setups. Table 1 summarizes the CTS conditions used in this paper. For both CTS setups, after the 10,000 sec CTS measurement, the TFT was

TABLE 1 — CTS conditions used in this study.

	Stress mode	Sweep mode	I_{STR} (μA)	T_{STR} (°C)
CTS_lin	I_D = I_{STR} V_{GS} = 20 V V_{DS}*	V_{GS} = -5→20 V V_{DS} = 20 V	10	40, 50, 60, 70, 80
			1, 10, 40, 100	60
CTS_sat	I_D = I_{STR} V_{DS} =V_{GS}**	V_{GS} = V_{DS} = -5→20 V	100	40, 50, 60, 70, 80
			40, 60, 80, 100	60

* V_{DS} increases with ΔV_T during the stress mode.
** V_{DS} = V_{GS} increases with ΔV_T during the stress mode.

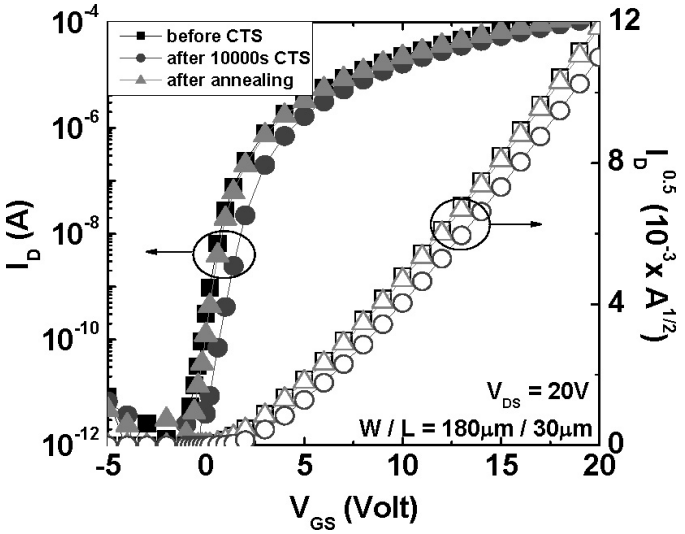

FIGURE 4 — a-InGaZnO TFT transfer characteristics before CTS, after 10,000-sec CTS, and after thermal annealing at 300°C in air for 1 hour.

annealed at 300°C in air for 1 hour to recover its initial characteristics, as shown in Fig. 4.

3.2 CTS effect on a-InGaZnO TFT electrical properties

Figure 5(a) shows an example of the TFT transfer characteristics measured during the sweep mode (V_{DS} = 20 V, V_{GS} = –5 → 20 V) of CTS_lin. The CTS_lin was performed at T_{STR} = 80°C with V_{GS} held at 20 V, and I_{STR} = 10 μA. For this level of stress current (I_{STR} = 10 μA), the drain-to-source voltage (V_{DS}) of the TFT is measured to be around 0.6 V, which indeed corresponds to the linear regime of operation. Figure 5(b) shows an example of the TFT transfer characteristics measured during the sweep mode (V_{DS} = V_{GS} = –5 → 20 V) of CTS_sat. The CTS_sat was performed at T_{STR} = 80°C with the gate and drain tied together, and I_{STR} = 100 μA, which sets V_{GS} = V_{DS} ~ 16.5 V. As we can see from Fig. 5, even after suffering through these strict CTS conditions for 10^4 sec, the TFT subthreshold slope and off-current remained almost the same, the field-effect mobility slightly (10%) decreases, and the threshold voltage only shifted ~2 V for both CTS setups. Recently, it has been shown that the electrical stability of a-ZnSnO TFTs is highly dependent on the Zn/Sn ratio.[18] We believe it is possible that the electrical stability of a-InGaZnO TFTs can be further improved by optimizing the film chemical composition.

3.3 Stress-temperature (T_{STR}) effect

We performed CTS measurements for both CTS setups at stress temperatures ranging from 40°C to 80°C. The stress currents are 10 and 100 μA for CTS_lin and CTS_sat, respectively. I_{STR} = 10 μA is sufficient for the maximum drive current level of a 15-in. XGA full-color AM-OLED

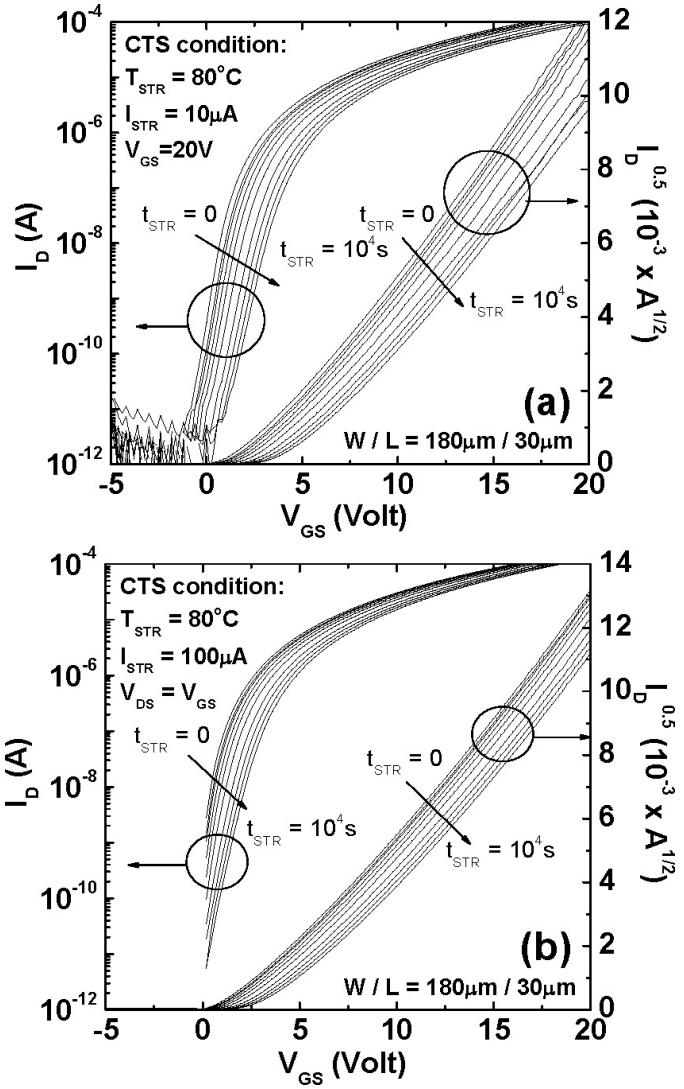

FIGURE 5 — a-InGaZnO TFT transfer characteristics measured during the sweep mode of (a) CTS_lin and (b) CTS_sat (Ref. 17).

(subpixel area A_{pix} ~ 30,000 μm^2), assuming a brightness (υ) of 1000 cd/m^2 and an OLED efficiency (η) of 5 cd/A:

$$I_{OLED} = \frac{\upsilon \cdot A_{pix}}{\eta}. \quad (1)$$

We used a much higher I_{STR} for CTS_sat to enhance the TFT parameter shifts since we observed that the TFTs are electrically more stable when stressed under CTS_sat compared to CTS_lin for the same I_{STR} level (see the next section for further details). The device degradation is defined as the change in threshold voltage (V_T):

$$\Delta V_T = V_T(t = t_{STR}) - V_T(t = 0). \quad (2)$$

V_T was extracted from linearly fitting $I_D^{1/2}$–V_{GS} measured in the sweep mode. The fitting range is chosen to be V_{GS} = 5–20 V to avoid the effect of the subthreshold regime at smaller V_{GS} values. It should be noted that the fitting range would affect the extracted V_T, due to the non-linearity of the $I_D^{1/2}$–V_{GS} curve, and therefore should be carefully chosen.

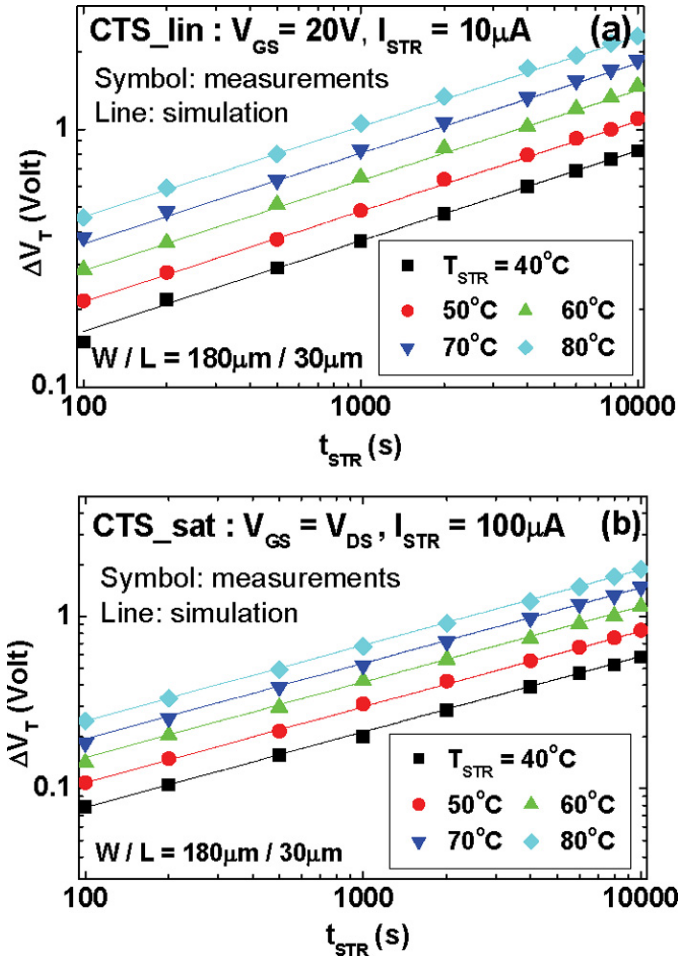

FIGURE 6 — Threshold-voltage shift (ΔV_T) as a function of stress time (t_{STR}) for various stress temperatures (T_{STR}) for (a) CTS_lin and (b) CTS_sat.

Figures 6(a) and 6(b) show the TFT threshold voltage shift (ΔV_T) as a function of stress time (t_{STR}) for various T_{STR} under CTS_lin and CTS_sat, respectively. For both CTS setups, ΔV_T increases with T_{STR} for a given t_{STR}. We also observed that

$$\Delta V_T \propto t_{STR}^{\beta}. \quad (3)$$

β is extracted to be 0.4 ± 0.05 for our a-InGaZnO TFTs. We have not observed any temperature dependence of β in the investigated T_{STR} range thus far.

A model that unifies the effect of stress temperature (T_{STR}) and stress time (t_{STR}) on defect creation was developed for a-Si:H TFTs.[19] This model assumes a distribution of energy barriers $D(E_a)$ for defect creation exists during bias stress: after a time t at a temperature kT all possible defect-creation sites with $E_a \leqq kT\ln(\nu t)$ will have converted into defects. The thermalization energy is therefore defined by

$$E = k \cdot T_{STR} \cdot \ln(\nu \cdot t_{STR}), \quad (4)$$

where k is the Boltzmann constant and ν is the attempt-to-escape frequency. We investigated possible application of this thermalization energy concept to a-InGaZnO TFTs. By

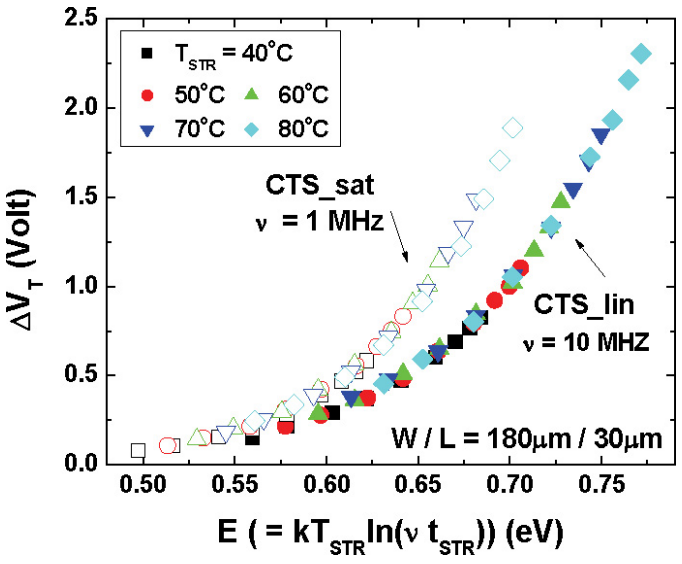

FIGURE 7 — Threshold-voltage shift (ΔV_T) as a function of thermalization energy (E), unifying the effect of stress temperature (T_{STR}) and stress time (t_{STR}) (Ref. 17).

plotting ΔV_T as a function of E, a unique curve is obtained for both CTS setups with only one fitting parameter, the attempt to escape frequency ν, as can be seen from Fig. 7. The value of ν is 10^7 Hz for CTS_lin and 10^6 Hz for CTS_sat and was determined to ensure the best overlap of the ΔV_T–E curves for all stress temperatures. It should be noticed that the thermalization energy is a function of ln(ν); therefore, the effect of 10^6 and 10^7 Hz are actually very close (14% difference). For a-Si:H TFTs, ν was extracted to be 10^{10} Hz and is believed to be associated with the breaking of weak Si–Si bonds.[19] Although the physical meaning of ν is unclear for our a-InGaZnO TFTs, Eq. (4) describes very well our experimental data in the investigated T_{STR} and t_{STR} range.

3.4 Stress current (I_{STR}) effect

We also performed CTS measurements at various I_{STR} levels. For CTS_lin, I_{STR} = 1, 10, 40, and 100 μA, and for CTS_sat, I_{STR} = 40, 60, 80, and 100 μA. Again, for CTS_sat, we did not explore lower I_{STR} levels for the same reason mentioned previously. The stress temperature (T_{STR}) was fixed at 60°C. Figure 8 shows the threshold-voltage shift (ΔV_T) as a function of t_{STR} for various I_{STR} levels under CTS_lin and CTS_sat. For CTS_lin, we can see that ΔV_T–t_{STR} is almost independent of I_{STR}. On the other hand, for CTS_sat, ΔV_T–t_{STR} increases with I_{STR} and becomes independent of I_{STR} once normalized to the injected charge Q_{inj} (= $I_{STR} \times t_{STR}$), as shown in Fig. 9. Q_{inj} is commonly used to evaluate the ΔV_T caused by trapped charge in the gate dielectric for c-Si MOSFETs.[20] We attribute this behavior to the following. The V_{GS} is fixed at 20 V for all levels of I_{STR} in CTS_lin; therefore, the channel induced charge will remain almost the same as long as the TFT operates in the linear regime. However, in CTS_sat, the V_{GS} adjusts accordingly to I_{STR}, and therefore, at higher I_{STR} values, we have a higher V_{GS}, and thus more

TABLE 2 — V_{DS} and V_{GS} values for both CTS conditions.

CTS condition	I_{STR} (μA)	V_{DS}*(V) (t_{STR} = 0)
CTS_lin V_{GS} = 20 V T_{STR} = 60°C	1	0.06
	10	0.56
	40	2.4
	100	7.5
CTS_sat V_{GS} = V_{DS} T_{STR} = 60°C	40	11.9 (=V_{GS})
	60	13.8 (=V_{GS})
	80	15.5 (=V_{GS})
	100	17.0 (=V_{GS})

* During CTS, V_{DS} increases with t_{STR}.

channel-induced charge. The V_{GS} and V_{DS} values are summarized in Table 2 for both CTS setups and all I_{STR} levels. We conclude from our experimental results that for the same I_{STR}, the a-InGaZnO TFTs are electrically more stable when V_{GS} is smaller.

3.5 CTS measurement modeling

In CTS_sat, V_{GS} increases with V_T in order to maintain a constant I_D, which is similar to the ΔV_T compensation mechanism in AMOLED pixel circuits. A model that can describe/predict the ΔV_T as a function of stress time (t_{STR}), stress temperature (T_{STR}), and stress current (I_{STR}) is beneficial in designing AMOLED pixel circuits. A stretched-exponential model based on the charge injection/trapping concept was developed for a-Si:H TFTs when subject to constant voltage stress.[21] We modified this model by taking into account that the gate overdrive voltage $[V_{GS}(t)–V_T(t)]$ is a constant during CTS_sat. An identical equation has also been derived for a-Si:H TFTs when subject to constant current stress, based on the carrier-induced defect creation model.[4]

$$\Delta V_T = \left[V_{GS}(t) - V_T(t)\right]^{\alpha} \cdot \left(\frac{t_{STR}}{\tau}\right)^{\beta}, \qquad (5)$$

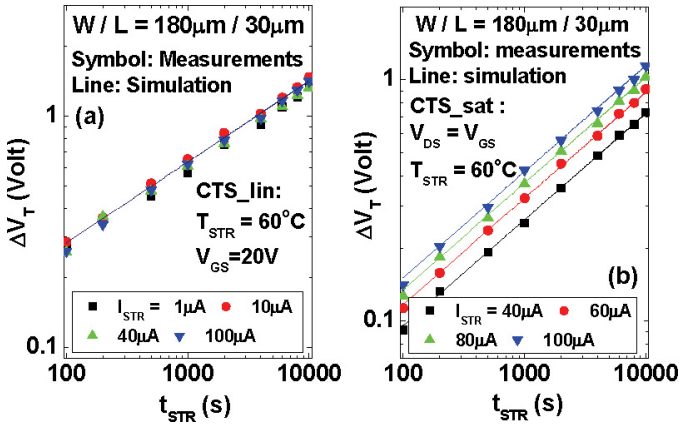

FIGURE 8 — Threshold-voltage shift (ΔV_T) as a function of stress time (t_{STR}) for various stress-current (I_{STR}) levels under (a) CTS_lin and (b) CTS_sat.

where α and β are the exponents for the gate overdrive voltage and stress time, respectively, $\tau = \tau_0 \exp(E_\tau/kT_{STR})$, and E_τ is the average effective barrier that the electrons in the a-InGaZnO channel need to overcome before they can enter the insulator, and τ_0 is the thermal prefactor for emission over the barrier. This power-law relation shows that there is no upper bound for ΔV_T which is in contrast to the stretched-exponential model. It should also be noticed that for very short stress times ($t_{STR} << \tau$), the stretched-exponential equation reduces to the exact same power law equation. However, Eq. (5) is only valid in the linear regime of operation since it assumes a uniform charge density along the channel. The channel charge in the saturation regime is reduced by the drain voltage and becomes $[1 + 1/(2 + \gamma)]$ times smaller, where γ is the nonlinear factor of the TFT transfer characteristics. Therefore, in the saturation regime, Eq. (5) becomes

$$\Delta V_T = \left[\frac{V_{GS}(t) - V_T(t)}{1 + 1/(2+\gamma)}\right]^{\alpha} \cdot \left(\frac{t_{STR}}{\tau}\right)^{\beta}. \qquad (6)$$

Equation (6) is not suitable for CTS_sat or any current-programmed pixel circuits because we do not control V_{GS} directly. It is, therefore, more straightforward to express Eq. (6) as a function of I_{STR} by using

$$I_{STR} = \frac{1}{2+\gamma} \cdot K \cdot \left(V_{GS} - V_T\right)^{2+\gamma}, \qquad (7)$$

where $K = (W/L)C_{ox}\mu_0$. By plugging Eq. (7) into Eq. (6), we can write the power-law equation as a function of I_{STR} instead of gate overdrive voltage:

$$\Delta V_T = \frac{\left(\frac{2+\gamma}{K} \cdot I_{STR}\right)^{\alpha/(2+\gamma)}}{\left(1 + \frac{1}{2+\gamma}\right)^{\alpha}} \cdot \left(\frac{t_{STR}}{\tau}\right)^{\beta}. \qquad (8)$$

The non-linear factor γ was extracted to be ~0.48 for our a-InGaZnO TFTs. By plotting $\log(\Delta V_T)$ as a function of

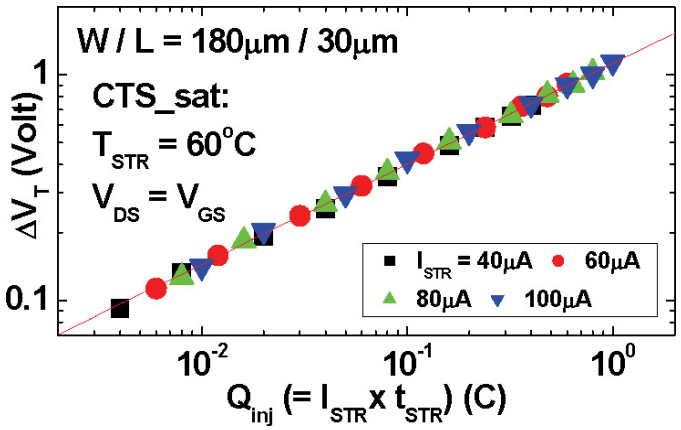

FIGURE 9 — Threshold-voltage shift (ΔV_T) as a function of injected charge (Q_{inj}) for various stress-current (I_{STR}) levels under CTS_sat (Ref. 17).

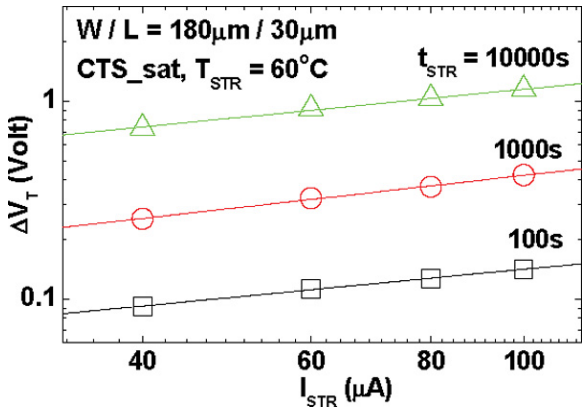

FIGURE 10 — Threshold-voltage shift (ΔV_T) as a function of stress current (I_{STR}) for various t_{STR} levels.

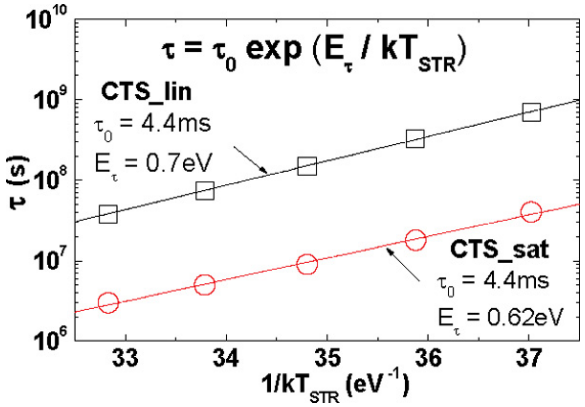

FIGURE 11 — Extracting the average effective barrier E_τ and thermal prefactor τ_0 from fitting parameter τ.

$\log(I_{STR})$ for several levels of t_{STR}, as shown in Fig. 10, we can obtain $\alpha/(2+\gamma) \sim 0.5$ from the slopes, and thus $\alpha \sim 1.24$.

On the other hand, CTS_lin can be modeled by the stretched-exponential model[21–23] because V_{GS} is held constant.

$$\Delta V_T = \left[V_{GS} - V_{T0}\right]^{\alpha} \cdot \left\{1 - \exp\left[-\left(\frac{t_{STR}}{\tau}\right)^{\beta}\right]\right\}. \qquad (9)$$

The simulation results of CTS_lin and CTS_sat are shown as the lines in Figs. 6 and 8. The same value of α = 1.24 were used in both simulations. β = 0.35 for CTS_lin and β = 0.44 for CTS_sat. The fitting parameter τ as a function of $(kT_{STR})^{-1}$ is plotted in Fig. 11. τ_0 is extracted to be 4.4 msec for both CTS setups, while E_τ = 0.7 and 0.62 eV for CTS_lin and CTS_sat, respectively. The parameters used in CTS simulations are summarized in Table 3.

4 a-InGaZnO TFT AMOLED pixel-circuit simulation

4.1 a-InGaZnO TFT for AMOLEDs

In the previous sections, we have explored the electrical properties and stability of a-InGaZnO TFTs and concluded that a-InGaZnO TFTs seem very promising for AMOLED application. The low off-current prevents the OLED current leaking from the TFTs during the off-state. The sharp subthreshold slope is beneficial to the TFT switching speed. The high field-effect mobility allows extra freedom when designing the pixel circuit. Smaller device sizes can be used, which increases the pixel aperture ratio. Moreover, lower gate overdrive voltages are sufficient to provide the desired current level. From the CTS measurement results obtained in this paper, lower gate overdrive voltages are also very beneficial to the TFT electrical stability. In the remaining sections of this paper, we will explore the possible application of a-InGaZnO TFTs to AMOLEDs by pixel-circuit simulations.

TABLE 3 — CTS modeling parameters.

	CTS_lin	CTS_sat
α	1.24	
β	0.35	0.44
γ	NA	0.48
τ_0	4.4 ms	
E_τ	0.7 eV	0.62 eV

4.2 a-InGaZnO TFT and OLED SPICE model

An a-InGaZnO TFT SPICE model was developed, based on the Rensselaer Polytechnic Institute (RPI) a-Si:H TFT model.[24] The required a-InGaZnO TFT SPICE parameters were extracted from experimental data. A Synopsys HSPICE simulation tool was then used to simulate the TFT characteristics (illustrated as the open circles in Fig. 1). We can see that the RPI a-Si:H TFT model with appropriate a-InGaZnO TFT SPICE parameters can reproduce our measured device characteristics very well. To model the behavior of the OLED, we used two junction diodes D_1 D_2 (HSPICE diode model level (1) with series resistors R_{S1} and R_{S2} connected in parallel with a capacitor C, shown in the inset of Fig. 12. SPICE parameters were extracted based on experimental data obtained within our group[5] and summa-

TABLE 4 — OLED SPICE parameters.

Area	12000 μm^2
D1	I_S = 4.2 nA, n = 7.8, I_K = 13 A
D2	I_S = 60 fA, n = 3.6, I_K = 32 mA
R_{S1}	2.6 mΩ
R_{S2}	27 mΩ
C	3 pF

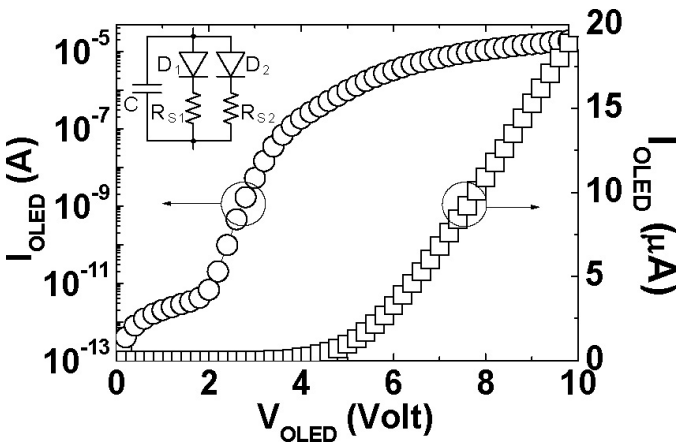

FIGURE 12 — Simulated OLED *I–V* characteristics.

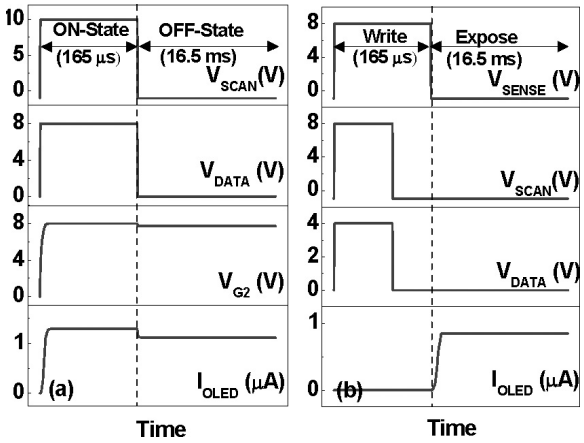

FIGURE 14 — Operation waveforms of the pixel circuits in Figs. 11(a), and 11(b), respectively, simulated by HSPICE.

rized in Table 4. The OLED area was assumed to be 12,000 μm^2 which is approximately the subpixel area of an RGB 3-in. QVGA display (63.5 × 190.5 μm). The OLED capacitor was calculated by assuming the capacitance per unit area is 25 nF/cm^2. The OLED *I–V* curve simulated by HSPICE is shown in Fig. 12.

4.3 Simple voltage-programmed pixel circuit

Thus far, all reported AMOLEDs driven by a-InGaZnO TFTs are based on the 2-TFT voltage-programmed pixel circuit,[12,13] as shown in Fig. 13(a). Since this simple circuit does not compensate for the TFT threshold-voltage variation (ΔV_T), the usage of this circuit requires the TFTs to be electrically very stable ($\Delta V_T \sim 0$). Synopsys HSPICE simulation tool with the a-InGaZnO TFT and OLED SPICE models developed in the previous section were used to evaluate the pixel-circuit performance. The simulated operation waveforms are shown in Fig. 14(a). Parameters used in the simulation are summarized in Table 5. Since the field-effect mobility of a-InGaZnO TFTs is ~10 times larger than that of a-Si:H TFTs, smaller device sizes (W/L = 24 μm/4 μm) and lower supply voltages (V_{DD} = 10 V) can be used in this circuit. We also investigated the effect of TFT threshold-voltage shift on the performance of this circuit, which will be discussed in later sections.

An additional TFT can be added to this circuit to prevent a sudden peak current from damaging the OLED, as shown in Fig. 13(b). The simulated operation waveforms are shown in Fig. 14(b). This circuit operates similar as the 2-TFT circuit except the current flows through the OLED only during the expose period.

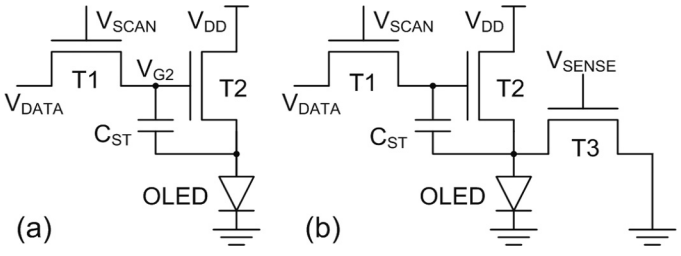

FIGURE 13 — Schematic diagrams of the (a) 2-TFT voltage-programmed pixel circuit and (b) the same circuit with an additional TFT (*T*3).

4.4 Current-scaling current-mirror pixel circuit

The 2-TFT voltage-programmed pixel circuit is very simple in design and enables a high aperture ratio. However, due to the current-driven nature of OLEDs and their steep *I–V* characteristics, current-programmed pixel circuits are more suitable to precisely generate distinct gray levels. Moreover, even if the a-InGaZnO TFTs are electrically very stable, it is still desirable to use a pixel circuit that can compensate for any non-ideal factors. Several current-programmed pixel circuits were developed for AMOLEDs.[25–27] Our group has previously explored the possible application of a-InGaZnO TFTs to a current-scaling pixel circuit that provides a wide dynamic OLED current (I_{OLED}) range and compensation abilities.[28] Here, we apply a-InGaZnO TFTs to a current-scaling current-mirror pixel circuit.[29] This circuit has similar performance as the previous circuit with a simpler driving scheme.

The current-scaling current-mirror pixel circuit consists of two switching TFTs (*T*1 and *T*2), one mirror TFT (*T*4), one driving TFT (*T*3), and two storage capacitors (C_{ST1} and C_{ST2}) connected between the scan line and ground with a cascade structure, as shown in Fig. 15. The

TABLE 5 — Parameters used in HSPICE simulation for pixel circuits in Figs. 13(a) and 13(b).

	(a)	(b)		(a)	(b)
T1	4/4		V_{DD} (V)	10	8
T2	24/4		V_{SCAN} (V)	-1→10	-1→8
T3	NA	8/4	V_{SENSE} (V)	NA	-1→8
C_{ST}	1pF		V_{DATA} (V)	3 ~ 9	1 ~ 7

TABLE 6 — Parameters used in HSPICE simulation for the 4-TFT current-scaling current-mirror pixel circuit.

	a-InGaZnO	a-Si:H [29]
T1, T3, T4	20/4	150/6
T2	4/4	10/6
C_{ST1} (fF)	360	
C_{ST2} (fF)	60	
V_{DD} (V)	12	18
V_{SCAN} (V)	-1→12	-5→25
I_{DATA} (μA)	0.2 ~ 5	

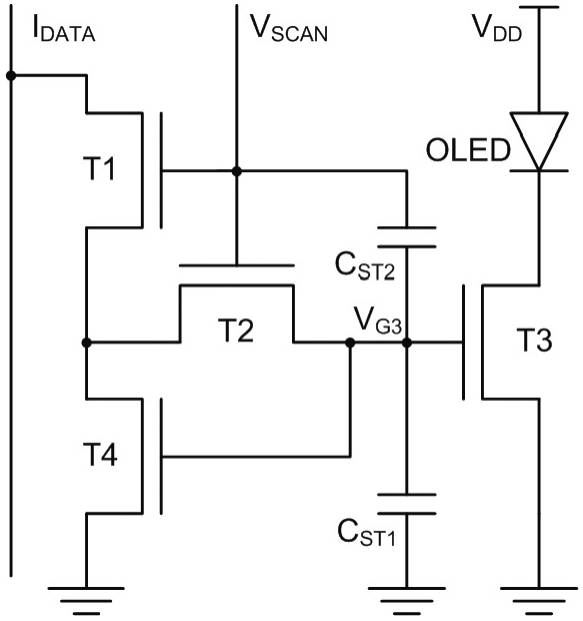

FIGURE 15 — Schematic diagram of the 4-TFT current-scaling current-mirror pixel circuit.

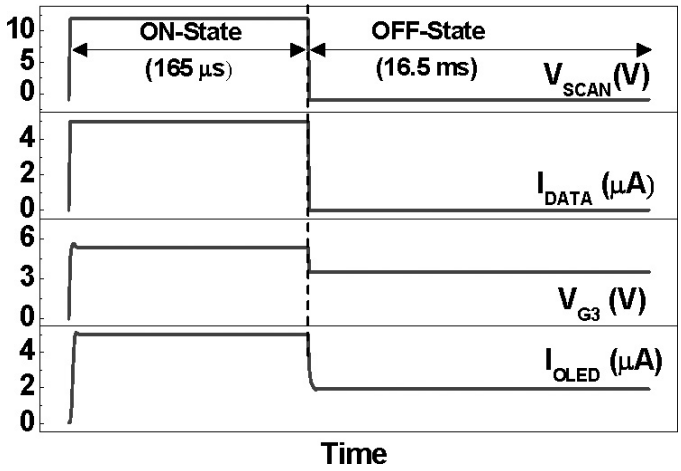

FIGURE 16 — Operation waveforms of the 4-TFT current-scaling current-mirror pixel circuit simulated by HSPICE.

operation detail of this circuit can be found elsewhere.[29] Parameters used to simulate this circuit are listed in Table 6 for both a-InGaZnO TFTs and a-Si:H TFTs.[29] Smaller device sizes (W/L = 20 μm/4 μm) and lower supply voltages (V_{DD} = 12 V) can be used for this circuit based on a-InGaZnO TFTs. Figure 15 shows an example of operation waveforms simulated by HSPICE.

4.5 Pixel-circuit simulation results

The OLED currents (I_{OLED}) delivered by the 2-TFT voltage-programmed pixel circuit and the 4-TFT current-scaling current-mirror pixel circuit as a function of V_{DATA} and I_{DATA}, respectively, are shown in Fig. 17. Since the OLED current value is different during the ON- and OFF-states (I_{OLED_ON} and I_{OLED_OFF}), we define the average OLED current (I_{OLED}) during one frame time as

$$I_{OLED} = \frac{I_{OLED\_ON} \cdot t_{ON} + I_{OLED\_OF} \cdot t_{OFF}}{t_{ON} + t_{OFF}}, \quad (10)$$

where t_{ON} (165 μsec) and t_{OFF} (16.5 msec) are the ON- and OFF-state periods, respectively (the frame rate is set to be 60 Hz). As we can see from Fig. 17, wide dynamic I_{OLED} range (~10^3) was achieved by both pixel circuits.

4.6 Impact of TFT instability on pixel-circuit operation

We also simulated the two pixel circuits assuming that the drive TFTs [*T*2 in Fig. 13(a), *T*3 and *T*4 in Fig. 15] exhibit 1 V of threshold-voltage shift (ΔV_T), as shown in Fig. 17. The percentage change in I_{OLED} (ΔI_{OLED}) is defined as

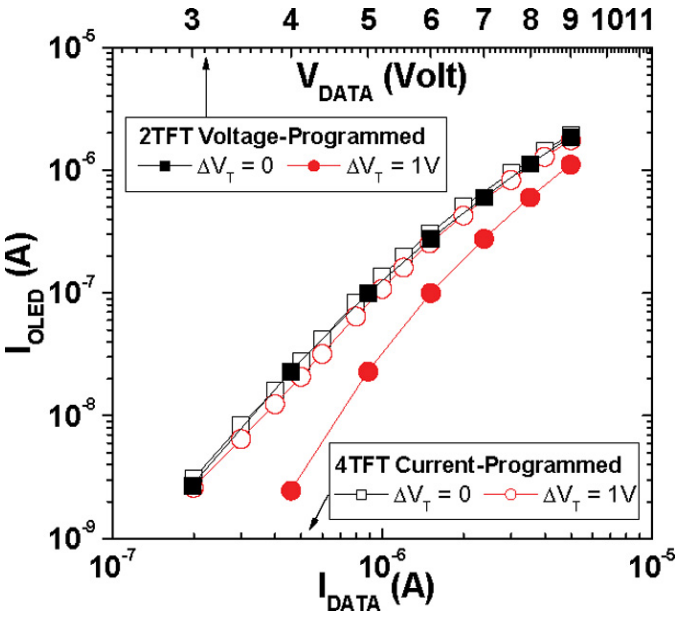

FIGURE 17 — I_{OLED} as a function of V_{DATA} for the 2-TFT voltage-programmed pixel circuit (solid symbols), and I_{DATA} for the 4-TFT current-scaling current-mirror pixel circuit (hollow symbols).

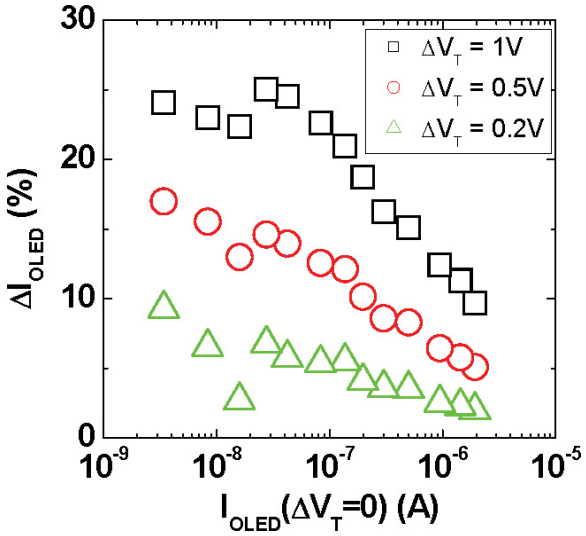

FIGURE 18 — ΔI_{OLED} as a function of I_{OLED} for the 4-TFT current-scaling current-mirror pixel circuit at several levels of ΔV_T.

$$\Delta I_{OLED} = \frac{I_{OLED}(\Delta V_T = 0) - I_{OLED}(\Delta V_T)}{I_{OLED}(\Delta V_T = 0)} \cdot 100\%. \quad (11)$$

We can see that the 4-TFT current-scaling current-mirror pixel circuit can compensate for ΔV_T within operating error range from 9 to 25%, depending on the I_{OLED} level, while the 2-TFT voltage-programmed pixel circuit does not compensate for ΔV_T at all (ΔI_{OLED}: 40–90%). Keeping in mind that 1 V of ΔV_T is quite large compared to the small gate overdrive (0–5 V) designed to be used in the pixel-circuit simulations. To further investigate the compensation ability of the 4-TFT current-scaling current-mirror pixel circuit, we plotted ΔI_{OLED} as a function of I_{OLED} for ΔV_T = 0.2, 0.5, and 1 V, as shown in Fig. 18. We can observe that ΔI_{OLED} is more severe at lower I_{OLED} levels due to the smaller gate overdrive of the drive TFT. The percentage error can be maintained below 10% for all levels of I_{OLED} if ΔV_T is smaller than 0.2 V. This result indicates that we need electrically very stable a-InGaZnO TFTs to be used for AMOLEDs.

5 Conclusion

We fabricated and characterized inverted-staggered a-InGaZnO TFTs on glass substrates. The TFTs exhibit adequate field-effect mobility, low off-current, and sharp subthreshold slope. To evaluate the electrical stability of a-InGaZnO TFTs, CTS measurements were performed. Several factors were considered, including the stress temperature, stress current, and biasing condition. We conclude that maintaining a lower temperature and smaller V_{GS} is beneficial to the TFT's electrical stability, and for the same level of I_D, the TFTs are more stable when operating in the saturation regime then in the linear regime. The a-InGaZnO TFTs exhibit ΔV_T ~ 1 V under 10,000 sec stress with I_{STR} = 100 μA, and T_{STR} = 60°C. The subthreshold slope, off-current, and field-effect mobility remain almost unchanged during the stress. Finally, a SPICE model was developed based on experimental data. Both simple voltage-programmed pixel circuits and current-programmed pixel circuits with ΔV_T compensation ability were simulated. Smaller device sizes and lower supply voltages could be used in a-InGaZnO TFT pixel circuits due to their superior electrical properties compared to those of a-Si:H TFTs. The voltage-programmed pixel circuits could be used provided that the a-InGaZnO TFTs are electrically very stable (ΔV_T ~ 0 V). Otherwise, the current-programmed pixel circuit is needed to compensate for ΔV_T. In conclusion, a-InGaZnO TFTs, if fully optimized, have great potential for higher resolution, lower power consumption, and more-stable operation AMOLEDs.

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