Investigation of Electrical Instabilities and Interface Charge in Zinc Oxide Thin-Film Transistors with High-k Dielectrics

by

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A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical Engineering)
in The University of Michigan
2012

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This thesis is dedicated to Dad, Mom, Mike, Karen, Grammy, and Grampie who have taught me that the most valuable asset in the world is unconditional love.

ACKNOWLEDGEMENTS

I sincerely thank Prof. Jamie Phillips, my doctoral committee chair and research advisor, for the opportunity to work with him and his group and for being an incredibly positive, supportive, and caring mentor. I would also like to thank my doctoral committee members: Prof. L. Jay Guo, Prof. Wei Lu, and Prof. Cagliyan Kurdak for their time and guidance throughout this work. I am extremely grateful to my collaborators at the Air Force Research Laboratory, Dr. Burhan Bayraktaroglu and Dr. Kevin Leedy, for providing various ZnO devices integral to this work and invaluable advice, guidance, and feedback. I would be remiss if I did not single out my group-mate, office-mate, and friend, Emine Cagin; words cannot describe the all-around positive influence she has had on my work and life. I cannot imagine my Michigan experience without her. I am severely indebted to my graduate program coordinator Beth Stalnaker; without her constant cheerful help I would not have been able to navigate the sea of rules and regulations that is graduate school. I would like to thank the past members of Dr. Phillips' research group who have helped and guided me along my doctoral path: Tim Murphy, Ding-Yuan Chen, Kaveh Moazzami, Weiming Wang, and Willie Bowen. I have had the great privilege to study, collaborate, commiserate, and socialize with a fantastic group of contemporaries while in the Phillips' Group: Pierre Emelie, Anne Itsuno, Jinyoung Hwang, Adrian Bayraktaroglu, Justin Foley, Bor-Chau Juang, Jimmy Chen, and Weiming Wang. I am grateful to a group of students from various research groups who generously donated their time and knowledge: Mike Hamilton, Alex Kuo, Siddharth Gaba, Yuchao Yang,

Wayne Fung, Andy Kuo, Christine Eun, Paul Barton, and specifically Patrick Shea, who's professionalism and humor I admire greatly. I have benefited from working along side students and staff members of the Lurie Nanofabrication Facility (LNF) and want to thank Brandon Lucas, Dr. Robert Gordenker, Ed Tang, Leslie George, Matt Oonk, Dr. Pilar Herrera-Fierro, and Steve Sostrom. For her valuable TFT advice, help with myriad LNF issues, and constant positive attitude, I sincerely thank Dr. Sandrine Martin. I would like to thank everyone at the Defense Microelectronics Activity (DMEA), where a great deal of this work was conducted, most notably: Fred Fraser, Ted Schantz, Carolynn Drudick, Kevin Geoghegan, Tom Gibbons, and Greg Allender. I am specifically grateful to Ajit Sandhu for being a selflessly supportive coworker. My time at DMEA would not have been as productive, successful, and fun without AJ. I could not have completed this work without the sincere trust, support, and advocacy of Janna Simons, and I thank her from the bottom of my heart. Finally, I conclude my acknowledgements by thanking Melinda for her love and support.

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ABSTRACT

Investigation of Electrical Instabilities and Interface Charge in Zinc Oxide Thin-Film Transistors with High-k Dielectrics

by

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Chair: Jamie D. Phillips

Exhibiting high electron mobility compared to amorphous Silicon, transparency in the visible spectrum, and compatibility with large area and flexible substrate applications, the semiconductor Zinc Oxide (ZnO) has become a major focus of research. This work investigates insertion of high dielectric constant (high-k) insulators into ZnO thin film transistors (TFTs) in an effort to reduce the threshold voltage (V_{TH}) and increase performance for next-generation devices.

Lead Zirconate Titanate (PZT), Barium Strontium Titanate (BST), Aluminum Oxide (Al_2O_3), and Hafnium Oxide (HfO_2) were selected for high-k investigation. Metal - Insulator - ZnO capacitors revealed that each material's high-k qualities can be integrated with ZnO, but PZT and BST show poor gate leakage characteristics above 10^{-2} A/cm^2, possibly due to small conduction band offsets with ZnO. Al_2O_3 and HfO_2 emerged as the most robust materials, however, each device exhibited clockwise hysteresis, which is indicative of interface charge. Devices also exhibited translational instability along the V_G axis. TFTs were fabricated with ZnO/high-k film stacks. In each case, the high-k dielectric effectively reduced the dielectric

equivalent oxide thickness and thus V_{TH}. HfO_2 emerged as the best candidate for ZnO/high-k devices.

Admittance Spectroscopy was found to be the most comprehensive technique to measure interface charge density in ZnO/HfO_2 films. D_{it} values were found to range from low 10^{13} to high 10^{11} $cm^{-2}eV^{-1}$. Bias - Temperature - Instabilities were investigated. Positive bias stress analysis reveal the dominant instability mechanism is carrier injection into the HfO_2. A new method was presented to characterize PBTI V_{TH} instabilities and extract dielectric charge trap density. N_T was found to be 7.5 x10^{18} cm^{-3}. Negative bias stress analysis shows the governing instability mechanism is charge state creation, likely, in the ZnO semiconductor. TFT stability under illumination was investigated. An increase in TFT I_{OFF}, subthreshold slope, -ΔV_{TH} and an initial increase in electron mobility can be explained via a model for polycrystalline TFT drain current via thermionic emission over grain barriers where illumination causes a reduction in grain boundary charge from a pre-illumination value of N_{GB} = 1.17$\pm$0.02 x10^{13} cm^{-2} and an increase in carriers due to photo-generation.

CHAPTER I

Introduction

This work presents an investigation of the integration of high-k dielectrics with ZnO for thin film transistor applications. Before the topic is presented, a brief background of how ZnO and high-k dielectrics came to be an important research topic will be presented.

1.1 Thin-film transistors

The most common electrical device, in fact the most populous man-made item in the world (with the possible exception of nails), is the Silicon based metal oxide semiconductor field effect transistor (MOSFET) [21], which was first reported by Atalla & Khang at Bell Labs in 1960. The MOSFET is an electrical switch, which, simply put, allows for the design of intelligent electrical systems. The eventual miniaturization and integration of tens, then hundreds, and now billions of transistors together is the basis of all 'smart technology' including the computer chips in everything from super computers and cell phones to the simplest children's toys. MOSFETs belong to a group of solid state devices that can be termed 'bulk' devices due to the fact that they must be fabricated on a, relatively, thick wafer cut from a single crystal, termed 'boule', of extremely pure Silicon. Due to the manufacturing process the boule diameter is limited, which limits the size of wafers and thus the maximum electronic

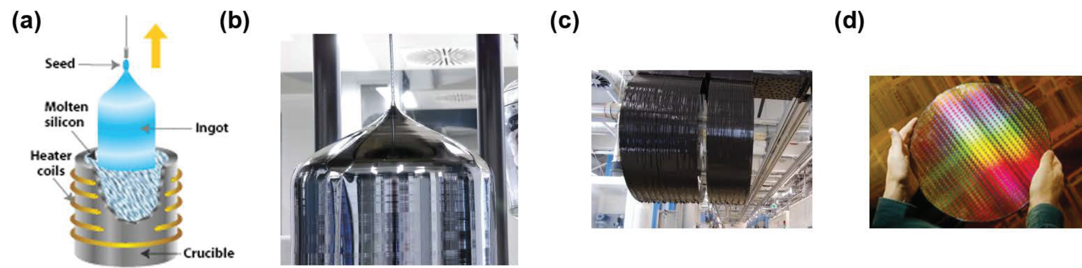


Figure 1.1: Bulk semiconductor technologies are limited by area of substrates (also called wafers), which are manufactured in sizes ranging from 2 to 12 inches in diameter. (a) Schematic of Si boule process. (b) Silicon boule. (c) Slicing a boule into wafers. (d) Fully processed wafer. [56, 55, 57]

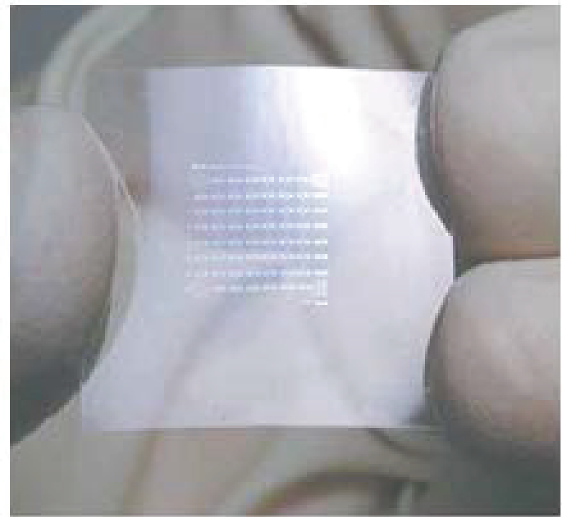
area of a smart device. In addition, the purity needs of the process require extreme manufacturing temperatures. As a result, Silicon MOSFETs are expensive to manufacture. A depiction of the Silicon manufacturing process can be seen in Figure 1.1.

Only in the last decade has miniaturization and large scale production resulted in devices of low-cost. As a result, the world's smart devices have been limited in their applications by size, temperature and cost restrictions. Flat panel TVs, LCD monitors, and smart phones would not be possible via only MOSFETs. Luckily, thin-film transistors (TFTs) were invented.

As the name alludes, 'thin film' devices are not manufactured on bulk semiconductors, but use various processes to deposit a thin film of semiconductor onto various substrates, which take the place of conventional Silicon wafers. Key advantages of thin film semiconductors include the capability to deposit semiconductors at low temperatures and large areas such that the conventional limitations of electronics to only small sizes and expensive single-crystal wafers have been eliminated. Instead of wafers, now electronics can be made on substrates of various sizes and shapes including glass and plastic. Thin film deposition technologies are ever-increasing the area that can be deposited. If you are reading this document electronically, odds are you are reading on a monitor or device made possible by thin film electronics. If you are

reading this document on paper, it is interesting to note that thin film semiconductors can now be printed on substrates with the very same ink-jet technology used in commercial printers, a deposition process that is a far cry from the bulk processes explained previously. An example of the large area electronics that TFT technology enables is shown in Figure 1.2(a). Just one example of the limitless possible applications that have been enabled is transparent circuits on flexible substrates such as the prototype demonstrated in Figure 1.2(b).

(a)



(b)

Figure 1.2: Technologies enabled by thin film electronics. (a) Large area display enabled by thin-film transistor technology [58]. (b)Transparent electronics on flexible plastic. The transparent TFT devices are made visible by adjusting the angle of the illumination [65].

Thin film technology has brought electronics from the 'old-world' of small-sizes and a handful of platforms to a 'new-world' of, nearly, limitless size and application-space.

1.2 What is a transistor?

In the case of thin film transistors, a transistor is a three terminal electronic device with two inputs and one output. At the most basic level, it can be thought of as a logical AND switch. From a purely operational sense a transistor can be viewed as Figure 1.3(a). The operation of the switch can be seen in Table 1.1. It will help to consider Input 1 (Drain) as a true input signal and Input 2 (Gate) as determining whether or not the transistor is 'on'. With this in mind, if the transistor (switch) is 'on' the input signal will pass from the Drain to the Output, called the Source (Cases 2 and 4 in Table 1.1). If the transistor is 'off' the signal will not pass from the input to output (Cases 1 and 3 in Table 1.1). Again, the Gate input determines whether the switch is 'off' or 'on'.

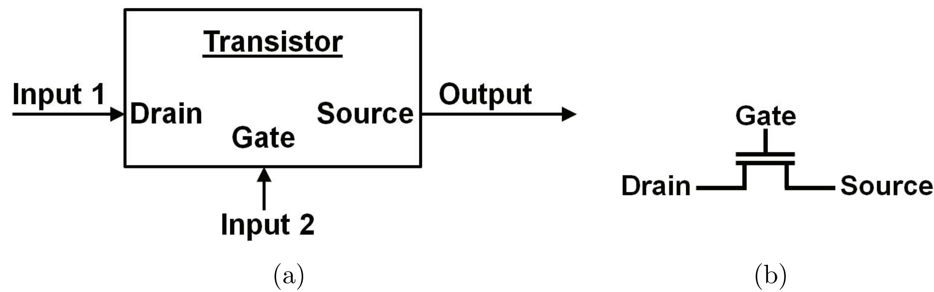


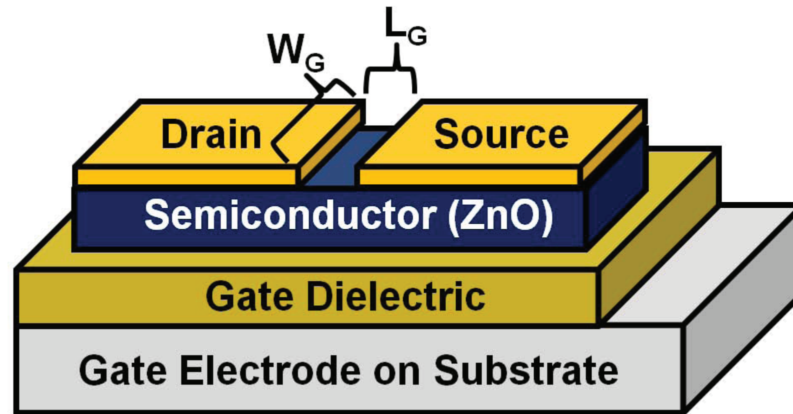
Figure 1.3: Transistors can be thought of as switches. (a) Thin Film Transistor can be thought of as a 'black box' switch. (b) Symbol universally used to represent a transistor.

	Input 1 Drain	Input 2 Gate	Output Source
Case 1	0	0	0
Case 2	0	1	0
Case 3	1	0	0
Case 4	1	1	1

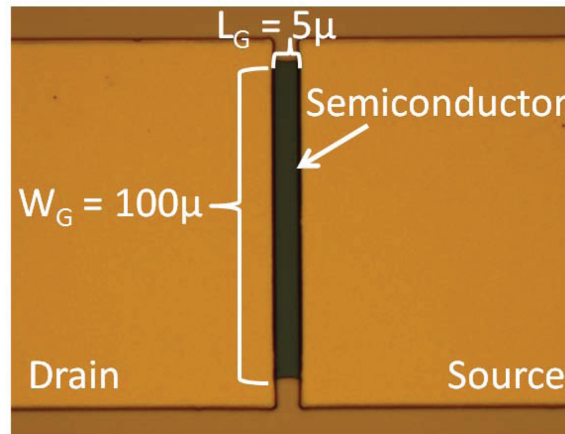
Table 1.1: Output Table for Basic TFT n-type Switch

1.3 How a thin film transistor works

Now that it is clear 'what' a transistor does, this subsection will discuss 'how'. The thin film transistor typically has five parts which operate together to make the switch: The Drain, Gate, Source, Semiconductor, and Gate Dielectric.



(a)



(b)

Figure 1.4: Basic Thin Film Tranistor. (a) Figurative representation of a Thin Film Transistor. (b) Optical microscope top-view of a ZnO Thin Film Transistor.

Drain: The Drain is an input that is usually biased at some static bias value. It is called the Drain because when the transistor is 'on' electrons will flow into this port like water flowing into a sink drain. In the bottom gate configuration, the Drain is on the top of the semiconductor.

Source: The Source is the output port. It is called the Source because when the transistor is 'on' electrons flow from this port to the Drain so it is the 'source' of electrons. In the bottom gate configuration the Source is located on the top of the semiconductor separated from the Drain by a length called the Gate Length (L_G).

Semiconductor: The semiconductor is the material the connects the Drain and Source. It has a special ability to act as an insulator or conductor. If the semiconductor acts like a low resistance (conducting) material, it will conduct an electrical signal from the Drain to Source. In this case, the transistor is considered 'on'. If the semiconductor acts like a high resistance (insulating) material, the transistor is considered 'off'.

Gate: The Gate is the second input and is located at the bottom of the TFT structure. The role of the Gate signal is to influence the semiconductor, controlling whether it acts as an insulator (switch 'off') or conductor (switch 'on'). It is called the Gate because it controls whether electrons can flow from the source to the drain or not, just as the gate in a damn determines whether water can flow from a reservoir to lower land.

Gate Dielectric: The Gate Dielectric is an insulating material that physically separates the Gate electrode from the semiconductor. It serves two purposes. First, as an insulator it keeps electrons from flowing out of the semiconductor. Secondly, it allows the electric field from the Gate electrode to influence the semiconductor changing its properties from an insulator to a conductor or visa versa, subsequently determining if the switch is 'on' or 'off'. In the case of an n-type semiconductor, like ZnO, a positive electric field on the Gate will attract electrons in the semiconductor. The electrons will collect near the semiconductor/gate dielectric interface and be available to conduct the electrical signal

between the Source and Drain ('on' state). Conversely, a negative electric field will repel electrons away from the semiconductor/gate dielectric interface and thus there will be no carriers for any electrical signal from the source to drain ('off' state).

Figure 1.4(a) schematically shows how the five key parts of a thin film transistor are configured. Figure 1.4(b) is an optical microscope top-view of a basic thin-film transistor. The Gate is not visible because it is underneath the other parts of the transistor.

1.4 TFT Application Example

As previously mentioned, ZnO based thin film transistors are being researched for large area display technologies. One application is the use of TFTs in the pixel circuitry of an Active Matrix Organic Light Emitting Diode (AMOLED) display such as that in Figure 1.2(a). Figure 1.5 shows a schematic and top view of pixel circuitry employing two thin film transistors. Figure 1.6 shows a cross-section depiction describing how the TFT is integrated into one pixel of an AMOLED display.

1.5 Amorphous Silicon thin-film transistors

The first significant driving application for the development of thin film transistors was display technologies. With this driving force, combined with the fact that the most well understood semiconductor is Silicon, it should be no surprise that the first dominant thin-film electronics solution was realized with Silicon. In 1979 LeComber, Speak, and Ghaith described an amorphous Silicon (a-Si) TFT deposited by glow-discharge that fit criteria for driving liquid crystal displays at that time. Current large area a-Si deposition is carried out by Plasma Enhanced Chemical Vapor Deposition

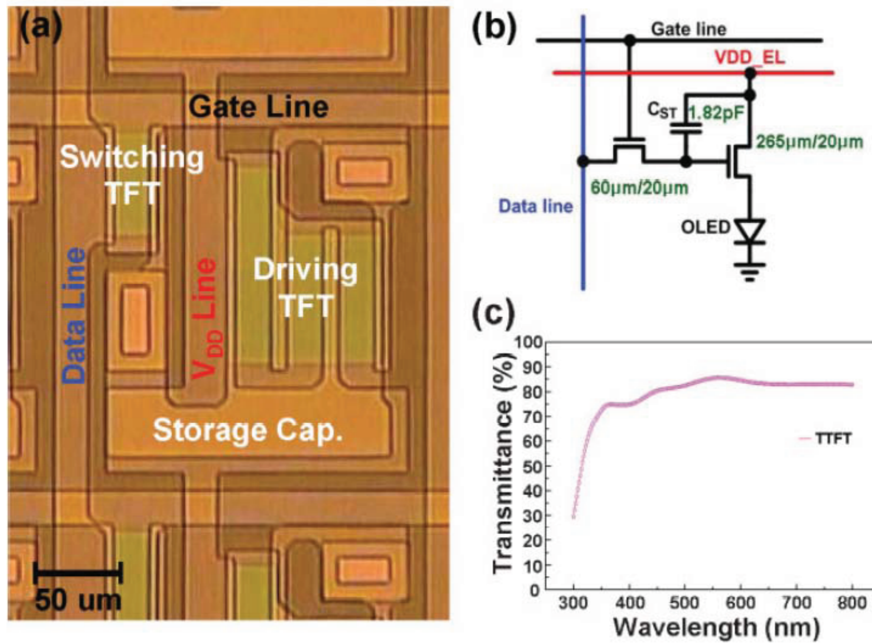


Figure 1.5: (a) Top-view of 2 transistor, 1 capacitor pixel structure for AMOLED back-plane. (b) Circuit diagram. (c) Transmittance of backplane pixel array [69]

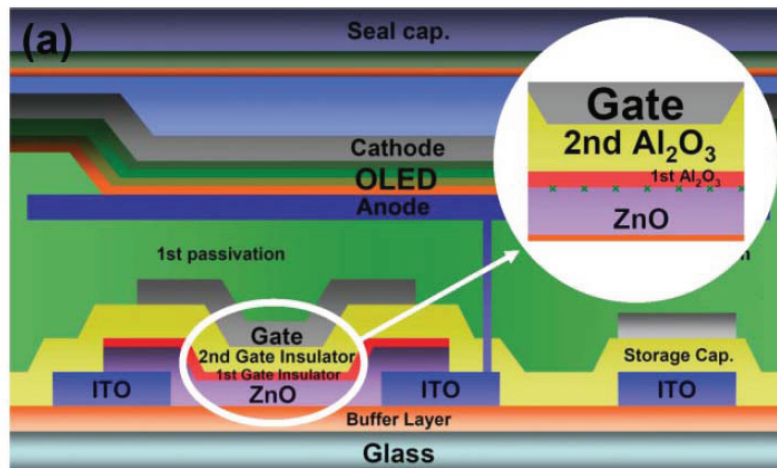


Figure 1.6: Schematic cross-section of TFT back-plane and OLED front-plane. Back-plane is 1st passivation layer and everything below. [69]

(PECVD) [30]. Though a-Si TFTs have been the dominant technology for nearly 30 years, there are some intrinsic drawbacks to using a-Si:

- Silicon will have an induced photo-current. As a result, special care and often extra process steps are required when using a-Si for display technologies.

- a-Si is a disordered matrix of Si atoms in which electrons conduct through the matrix by 'hopping' from allowed state to allowed state. This severely reduces the ability of electrons to react and move quickly in response to an electric field. This response is called electron mobility (μ), which is measures the speed of an electron (cm/second) per unit of applied electric field (V/cm) and has the units $cm^2/(V\ s)$. The low electron mobility renders a-Si undesirable for high-performance applications, including high-definition and high-speed display applications, not to mention any application requiring high-mobility.

As a result of these drawbacks, much research has been ongoing in the areas of improving a-Si mobility and replacing a-Si in TFTs altogether.

1.6 Alternatives to amorphous Silicon

a-Si has an electron mobility $\sim$1 $cm^2/V\ s$ due to electron conduction characteristics in a disordered matrix, but single crystal 'bulk' Silicon has an electron mobility of 1417 $cm^2/V\ s$ due to electrons moving through the conduction band of an extremely uniform crystal. Silicon researchers have come up with several methods to re-crystallize a-Si after it has been deposited in a thin-film form so that the semiconductor will re-gain some of its crystal-like properties. These methods create a form of Silicon termed poly-crystalline Silicon (p-Si), which can be thought of as many small single crystal Silicon regions in a matrix, but at each boundary electrons suffer mobility-killing scattering. Mobilities of p-Si have been demonstrated up to 360 $cm^2/V\ s$, but even those with lower mobilities show a uniformity less than 30%

[81]. Another drawback is that the re-crystallization process requires an anneal above 600°C or high energy laser annealing. The high temperature solution is not conducive to low cost or low temperature substrates, like all flexible substrates while the laser solution is not conducive to large area manufacturing.

Organic semiconductors have been a topic of intense research in the last two decades and the use of organic light emitting diodes in large area displays is wide spread. Organic TFTs have demonstrated the advantages of low temperature and large area compatible deposition techniques, but suffer from mobility values at or below 1.5 cm^2/V s for p-type TFTs and less for n-type [39].

Metal oxide semiconductors are a class of semiconductors that have demonstrated high mobilities, large area and low temperature deposition techniques, and transparency in amorphous or poly-crystalline form. Amorphous Indium Gallium Zinc Oxide (IGZO) and Zinc Tin Oxide (ZTO) have demonstrated mobilities $\sim$10 cm^2/V s theorized to be high for an amorphous material because electrons are drifting through ionic metal s-orbital, which permit a band-like conduction [22, 24]. While ZnO has a theoretical room temperature mobility of only 300 cm^2/V s, thin-film mobilities have been demonstrated as high as 110 cm^2/V s [5]. ZnO's thin-film form also retains its bulk wide band-gap and transparent qualities at deposition temperatures of 250°C making thin-film ZnO extremely attractive for high-performance and large area electronics on a host of substrates. One example of an application enabled by ZnO is low-cost wireless devices on various substrates: Currently, microwave electronics must be fabricated on single crystal semiconductors with extremely high mobilities such as GaAs and GaN. New reports of high-mobility thin-film ZnO show microwave performance and could be a significant disruptive technology [5].

Poly-crystalline ZnO is inherently n-type, thus a summary table of competing n-type thin-film technologies is presented in Table 1.2.

Figure of Merit	High Performance a-Si TFT [34]	Organic TFT [39]	IGZO [27]	ZTO [38]	ZnO [5]
μ (cm^2/V s)	1.5	0.02	14	43	110
I_D^{on}/I_D^{off}	$\sim 10^8$	$\sim 10^6$	$> 10^8$	10^7	10^{12}
I_D^{off} (pA)	0.1	1	0.1	1	0.01
V_{TH} (V)	2	$\sim$0.7	2.3	1.4	2
S (mV/dec)	300	170	200	180	100

Table 1.2: Summary of competing thin-film n-type technologies.

1.7 ZnO TFTs

As discussed previously, the great advantage of ZnO over Silicon is its ability to maintain more of its bulk high-performance mobility in addition to being light insensitive and transparent.

ZnO is a II-VI semiconductor with a wide band-gap of 3.437 eV at 2 K [46] that assumes a thermodynamically stable phase of wurtzite symmetry [52] as seen in Figure 1.7.

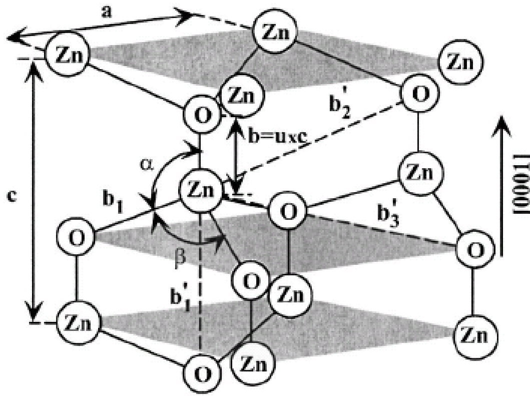
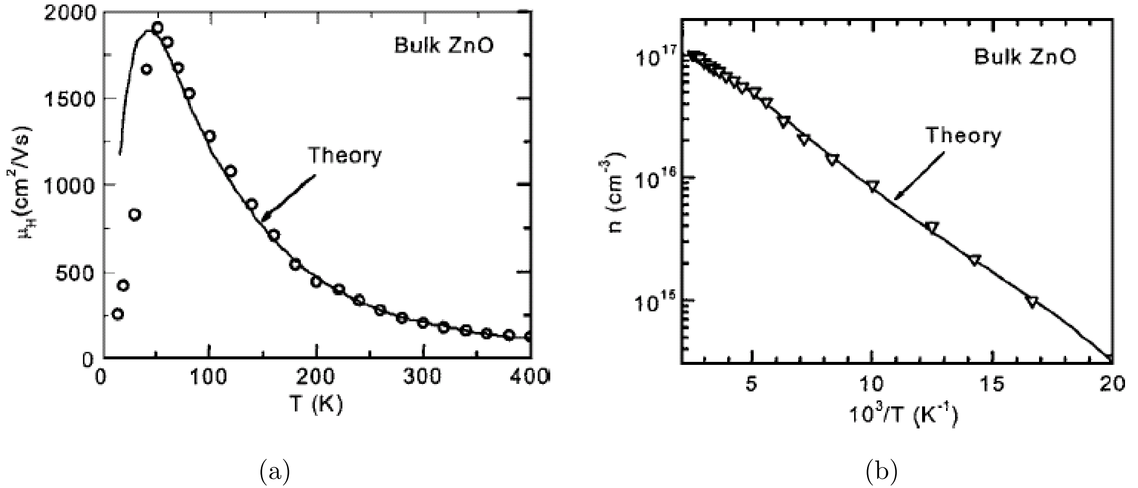


Figure 1.7: Schematic Representation of Wurtzitic ZnO structure [68].

ZnO's bulk mobility and carrier concentration with respect to temperature can be seen in Figure 1.8.

The saturation velocity (v_s) is a key value, more important than mobility, for high-speed devices. ZnO v_s is even higher than that of GaN [46], a material being



(a) (b)

Figure 1.8: (a) Hall Mobility of bulk ZnO with respect to temperature [47]. (b) Hall carrier concentration of bulk ZnO with respect to temperature [47].

heavily researched for its high speed and high electron mobility applications

such as microwave transistors. The transparency of bulk ZnO has been measured and the absorption coefficient of wavelengths with energies below the band-gap (wavelengths above cutoff frequency) is reported to be $\sim$2x10^{5}cm^{-1} [45]. ZnO thin-films have been reported with exceptional transparency, over 80% across the visible spectrum.

Despite huge advantages, ZnO TFT technology has a long way to go before understanding and maturity reach even a fraction of that of Silicon technologies. Before the work presented began ZnO TFTs had several key drawbacks when compared with a-Si technology.

- High threshold voltages (V_{TH}): ZnO TFTs with traditional SiO_2 or Si_3N_4 dielectrics exhibited V_{TH} values from 10 to 30 V.
- Unstable V_{TH}: Reports in this work and the literature report unstable V_{TH} values in various conditions with a low level of understanding of the mechanisms responsible.
- Large subthreshold slopes (S): Typically linked to interface charge, a topic that

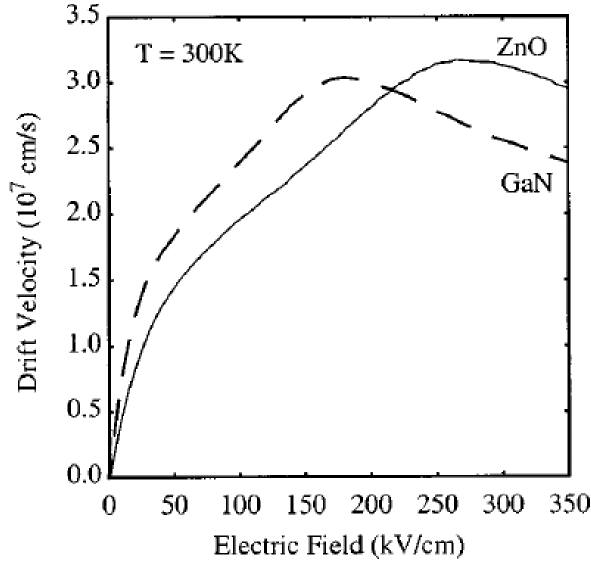


Figure 1.9: Comparison of calculated electron drift velocity vs electric field for wurtzite structure GaN (dashed) and ZnO (solid) at 300K [1]

has not been studied in depth for ZnO devices.

1.8 Research goals

The goal of the work presented is to advance understanding of ZnO thin-film transistors and contribute to improvement of next generation devices. Taking into account the powerful advantages of ZnO and the drawbacks mentioned above the work presented will have three major foci:

- Survey and investigation of high-k dielectrics for ZnO TFTs with low threshold voltage operation.
- Investigation of the interface between the ZnO and a high-k dielectric of choice.
- Investigation of the characteristics and mechanisms responsible for ZnO/high-k TFT instabilities.

Through these three research goals a new high-performance TFT material structure will be presented, the resulting device's interface and instability characteristics

will be reported, and a further understanding of ZnO/high-k devices will result.

Chapter I - Introduction This chapter provides a motivation and background for thin-film electronics. The benefits and drawbacks of ZnO as a thin-film semiconductor will provide motivation for the research presented.

Chapter II - ZnO and High-k Dielectric Thin-Films Chapter II provides information on the deposition techniques used for ZnO and the high-k dielectrics under investigation. The resulting electronic properties are reported as a baseline for understanding the role of each material in devices presented and studied in subsequent chapters.

Chapter III - Metal / High-k / ZnO Devices This chapter provides the first look at the integration of the high-k materials introduced in Chapter II with ZnO. The most basic semiconductor / dielectric device, the MIS capacitor, is presented and used as an initial research vehicle to evaluate the performance of the high-k dielectrics under investigation. This chapter serves as the first step in evaluating electronic devices and serves as a comfortable transition from discussing material properties to transistor properties, which will be heavily discussed in the next chapter.

Chapter IV - ZnO Thin Film Transistors with High-k Dielectrics The approach of this chapter is to familiarize the reader with TFT performance analysis and then report, analyze, and compare ZnO TFTs with different high-k dielectrics. The important result of V_{TH} lowering will be discussed and links between dielectric electronic properties and TFT performance will be made and used to evaluate and understand TFT performance. HfO_2 will emerge as the high-k dielectric of choice for ZnO/high-k high-performance TFTs; this specific material combination will serve as the research vehicle for the advanced topics of Interface State Density (Chapter V)

and transistor instability (Chapter VI).

Chapter V - Interface Charge Study of Insulator-ZnO Heterojunctions Earlier chapters provide motivation for the benefit of HfO_2 as the gate dielectric in ZnO TFTs. However, TFT performance drawbacks of decreased subthreshold slope and increased transfer curve hysteresis have been reported both of which are an indication of the presence of interface trapped charge (D_{it}). The purpose of this chapter is to investigate and characterize the role of D_{it} in ZnO/HfO_2 material stacks.

Chapter VI - Bias - Temperature Stress Studies on High-k/ZnO Devices Devices with superior performance are desirable for insertion into electronic products, but before a device can be used in a product, its performance stability must be assured. In Organic Light Emitting Diode displays, for example, a ZnO-based devices are extremely desirable for the switching and driving transistors in each pixel circuit. Stability is also a critical issue as a change as little as 0.1 Volt in V_{TH} could result in a pixel brightness change of 20% [31]. In this chapter the device stability with respect to applied gate voltage and temperature is presented. The stability results are analyzed and theories explaining the behavior are reported.

Chapter VII - Illumination Stability Investigation on High-k/ZnO Devices A great advantage of ZnO is its transparency in the visible spectrum. However, ZnO based devices have shown various performance instabilities under illumination. In display applications, devices will be subject to illumination in the visible spectrum. For high performance ZnO devices to qualify for, and harness the advantages useful to, the display community these instabilities must be understood. In this chapter we investigate illumination instabilities of high performance ZnO/HfO_2 TFT devices and their source mechanisms.

Chapter VIII - Future Work In this chapter important results and gains in understanding are presented along with the authors opinion about the advance of ZnO TFT technology. Key issues for the future of the technology will be discussed and an outline of important future work will be presented.

CHAPTER II

ZnO and High-k Dielectric Thin-Films

2.1 Thin-film ZnO

In this section the deposition technique and conditions for thin-film ZnO will be discussed and the results of the resulting thin-film used as the semiconducting layer throughout this work will be presented.

2.1.1 Deposition

Thin-film ZnO can be deposited via many methods including molecular beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD), solution spin-coating, atomic layer deposition (ALD), RF sputtering, and pulsed laser deposition (PLD). Each deposition technique has advantages and disadvantages, but RF sputtering and PLD have the largest operating windows in terms of variables such as temperature, pressure, and realizable large-area and achieve a high level of process control while still staying relatively inexpensive and easy to operate. MBE and MOCVD require extremely high vacuum and temperatures, while spin-coating a ZnO containing solution is cheap and simple, but affords comparatively little process control. ALD is a relatively new deposition technique and will be explained later as it is also used to deposit high-k Aluminum Oxide (Al_2O_3) and Hafnium Oxide (HfO_2) gate dielectrics. In this work we deposit thin-film ZnO via PLD.

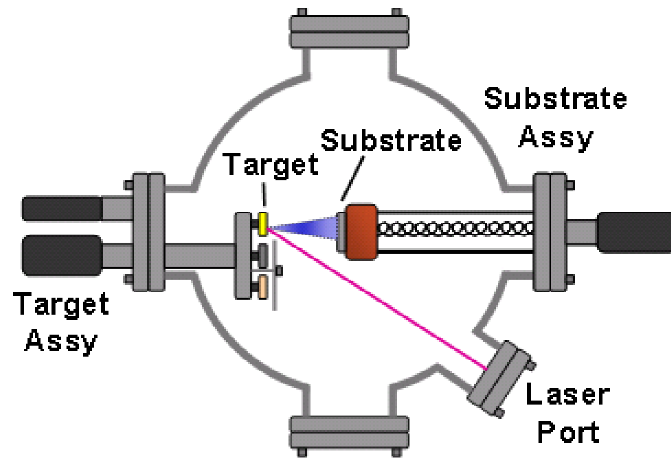
The pulsed laser deposition method uses high-power laser pulses to evaporate (ablate) ZnO from a 99.999% pure ceramic target placed in the vicinity of a substrate on which the ZnO is to be deposited. The ablated target particles form a plume and, when a substrate is located in the plume area, ablated species condense on the substrate. Figure 2.1(a) shows a schematic representation of the PLD deposition chamber and Figure 2.1(b) shows an actual picture illustrating the target, plume, and substrate during a PLD deposition.

In addition several variables can be controlled to optimize ZnO thin-film quality. Table 2.1 lists these variables, their process limits, and the values chosen for ZnO thin-films presented in this work.

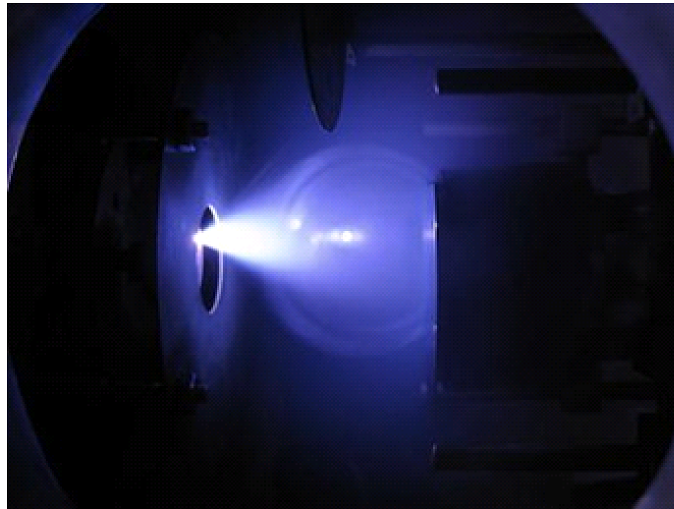
Deposition Variables	Range	ZnO Deposition (Univ. of Michigan)	ZnO Deposition (AFRL)
Substrate Temperature (^oC)	23 - 700	350	200
Oxygen Partial Pressure (mTorr)	<150	30	10
KrF Excimer Laser (nm)	248	248	248
Energy (mJ)	350 - 500	350 mJ	152mJ (2.6 J/cm^2)
Pulse Repetition Rate (Hz)	1-30	6	30
Target-Substrate Distance (cm)		4 - 12	9.5

Table 2.1: Pulsed laser deposition conditions

ZnO thin-film deposition was performed at two locations; the University of Michigan (UM) and Air Force Research Laboratory, Wright-Patterson (AFRL). Both locations used similar PLD systems supplied by Neocera, Inc. with a key difference being the PLD chamber at AFRL is dedicated solely to ZnO and is free of deleterious effects to the thin-films caused by non-ZnO material contamination. Over the course of this work, it will be made clear when UM ZnO or AFRL ZnO is employed.



(a)



(b)

Figure 2.1: Pulsed laser deposition. (a) Schematic diagram of pulsed laser deposition chamber. (b) Picture taken during pulsed laser deposition. The ZnO target, plume, and heater with substrate attached can be seen (the substrate is in-plane with the picture with a cross section too thin to be seen).

2.1.2 ZnO thin-film properties

All of the devices presented in this work are so-called 'bottom gate' devices, which means the gate electrode is the starting layer. The gate dielectric is deposited on the electrode, and then finally the ZnO semiconductor is deposited on the dielectric. As a result, meaningful ZnO thin-film characteristics presented are not just ZnO on a substrate, but ZnO on a gate dielectric used in this work. The schematic cross section of a bottom-gate device can be seen in Figure 2.2(a) followed by actual transmission electron micrographs (TEM) of PLD ZnO on ALD Al_2O_3 (on Silicon, Figure 2.2(b)) and ALD HfO_2 (on Silicon, Figure 2.2(c)).

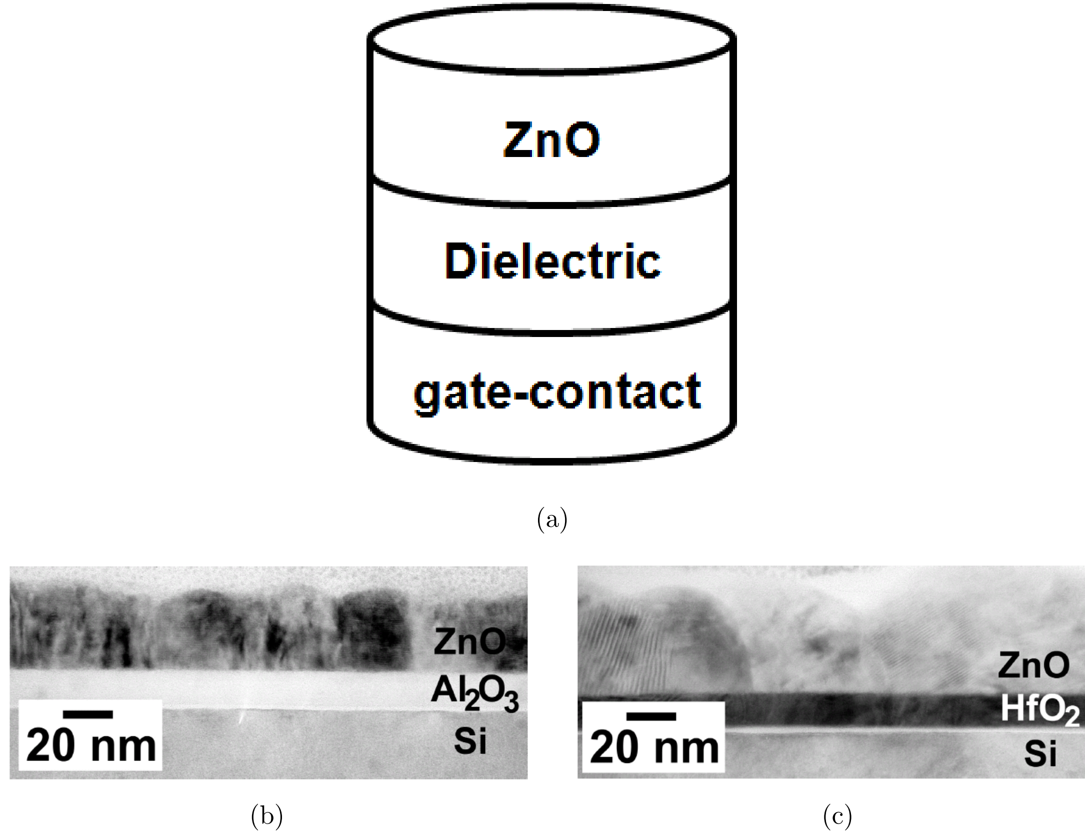


Figure 2.2: Cross section of bottom-gate dielectric/ZnO structures. (a) Schematic representation. (b) TEM image of AFRL ZnO deposited on ALD Al_2O_3 [5]. (c) TEM image of AFRL ZnO deposited on ALD HfO_2 [5].

Smooth interfaces between the ZnO and dielectrics are observed and ZnO grains are columnar in nature with smaller grain interface spacing seen for ZnO on Al_2O_3 and

a rougher surface seen for ZnO on HfO_2 [5]. The interfaces of poly-crystalline semiconductors are thought to create a barrier to electron flow and these 'crystal defects' often significantly limit electronic performance as is the case with poly-crystalline Silicon. With poly-crystalline thin-films exhibiting high electron mobilities, ZnO is a very defect/grain interface tolerant material, but grain boundary performance trends have still been predicted [28]. As a result, the film with less grain boundaries per area (larger grains) should be expected to perform better in a controlled environment.

The crystalline quality and orientation of a thin-film can be evaluated by the X-ray diffraction (XRD) technique. Figure 2.3 shows XRD scans of AFRL ZnO deposited on the ALD films mentioned above.

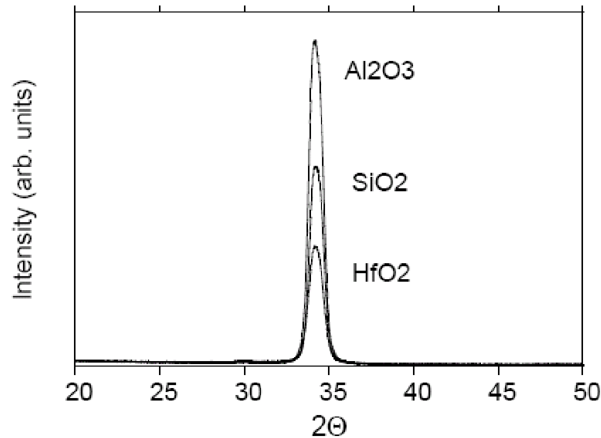


Figure 2.3: X-Ray diffraction pattern for AFRL ZnO thin-films on amorphous dielectrics

The peaks for ZnO on Al_2O_3 and HfO_2 were 34.17^{O} and 34.21^{O}, respectively, indicating strong 002 orientation. A stronger signal typically indicates a higher quality film or surface so the stronger Al_2O_3 signal may be due to the smoother surface compared with HfO_2 as seen in Figure 2.2(b) and 2.2(c).

The main electronic property of interest, mobility, was measured via the field effect mobility (μ_{FE}) which will be further explained in Section IV. The mobility of UM ZnO was found to be between 2.2 and 3.2 $cm^2V^{-1}s^{-1}$ and the mobility of AFRL ZnO

was found to be between 10 and 30 $cm^2V^{-1}s^{-1}$. The discrepancy between mobilities is most likely due to differences in PLD chamber history, impurity contamination, and majority carrier concentration. At UM, many materials such as Barium Strontium Titanate, Barium Titanate, and Lead Zirconate Titanate are deposited in the same PLD chamber as ZnO. At AFRL the ZnO PLD is dedicated solely to ZnO. It is thought that non-ZnO metals may significantly degrade ZnO film mobility and that may be the case here.

The donor concentration (N_D) of a semiconductor can be estimated using the capacitance-voltage profile of a metal-insulator-semiconductor capacitor (MIS-C) by the Mott-Schottky relation shown in Equation 2.1

$$N_D = \frac{2}{q\epsilon_s \left| \frac{d(1/c^2)}{dV_G} \right|} \tag{2.1}$$

where q is the elemental charge, ϵ_s is the dielectric permittivity of the semiconductor, C is the capacitance of an MIS-C, and V_G is the applied (gate) voltage on the MIS-C [35]. Using a Pt - HfO_2 - ZnO capacitor, N_D for AFRL ZnO was found to be 3.7x10^{16} cm^{-3}. Testing both Pt - Perovskite Oxide - UM ZnO capacitors (discussed in Section III), N_D for UM ZnO was found to be 3.4±2.2x10^{18} cm^{-3}. The trend in mobility and carrier concentration between UM ZnO and AFRL ZnO is commensurate with reports of increasing mobility with decreasing carrier concentration [6].

2.2 High-k thin-films

High-k films, in semiconductor electronics terminology, are films with a dielectric constant (κ), also termed relative permittivity, above that of SiO_2 (κ =3.9), the most widely used dielectric for decades. In this work we use high-k dielectrics to reduce the threshold voltage of thin-film transistors in order to allow the performance advantages of ZnO to function in voltage regimes compatible with many existing technologies

currently dominated by a-Si. High-k dielectrics allow more of an electric field put across a dielectric and a semiconductor to act on the semiconductor than a traditional dielectric, thus the required voltage needed to apply the field is reduced. In this way, we will employ high-k dielectrics to reduce the threshold voltage of ZnO TFTs. The theory can be understood by realizing that the electric flux density (D) must be continuous at the ZnO-gate dielectric (typically called gate oxide) interface [10]

$$D_{ox} = D_{ZnO} \quad units\,(C/m^2) \tag{2.2}$$

and that electric flux density is the electric field (E) in a material multiplied by the material's permittivity

$$D_{ox} = \kappa_{ox}\epsilon_0 E_{ox} = D_{ZnO} = \kappa_{ZnO}\epsilon_0 E_{ZnO} \quad units\,(C/m^2) \tag{2.3}$$

$$E_{ZnO} = \frac{\kappa_{ox}}{\kappa_{ZnO}} E_{ox} \tag{2.4}$$

.

From equation 2.4 one can see that the higher the relative permittivity of the gate oxide, the higher the electric field in the ZnO will be resulting in a device that modulates the same amount of charge in the ZnO with less applied gate bias resulting in a lower threshold voltage.

It is also important to realize that the final field actually modulated across the ZnO by the applied gate voltage is influenced by the thickness of the gate material as well as the dielectric constant as shown in equation 2.5.

$$E_{ZnO} = \frac{\kappa_{ox}}{t_{ox}\kappa_{ZnO}} V_{ox} \tag{2.5}$$

A term used in the Silicon device industry, so long dominated by SiO_2 gate

dielectrics is Equivalent Oxide Thickness (EOT). As Silicon transistors are scaled smaller and smaller, the gate dielectric needs to be thinner and thinner. Once in the single nanometer thickness range, SiO_2 starts to leak too much current to be an effective insulator, thus high-k dielectrics are employed. The EOT of a high-k dielectric is the thickness required by SiO_2 ($\kappa_{ox} = 3.9$) to achieve the same voltage modulation effect. As an explanation, assume there exists a dielectric X with $\kappa_{ox} = 39$ and similar leakage properties to SiO_2, a 50 nm gate thickness of dielectric X would have an EOT of 5 nm (but retain the insulation properties of a 50 nm, physical thickness, film). EOT is expressed in Equation 2.6.

$$EOT = \frac{\kappa_{SiO2}}{\kappa_{high-k}} t_{high-k} = \frac{3.9}{\kappa_{high-k}} t_{high-k} \tag{2.6}$$

When choosing a high-k gate dielectric several considerations must be taken into effect [82]:

- Dielectric constant: The higher the dielectric constant, the smaller EOT can be achieved.

- Leakage properties: The entire benefit of using a high-k material is low EOT with good leakage barrier. If dielectric X, mentioned above, has a dielectric 10x that of SiO_2, but leakage qualities 10x worse there is no advantage to using the material. Band gap and band alignment with ZnO contribute to this issue as we will see in Section III.

- Film morphology: In this work, bottom gate structures require ZnO to be deposited on the dielectric. Film morphology must be at a quality high enough for the ZnO to maintain high performance qualities and, of course, act as a good insulator. In Section 2.1.2 it has been shown that high quality ZnO is capable on our high-k materials of interest.

- Process compatible: The material must be able to be deposited and processed with in the bounds/limitations of the existing process.

- Interface quality: Clean low defect density interfaces are desired. Dangling bonds, impurities, and non-ideal interface characteristics will contribute to device performance degradation. In addition, an undesirable layer of low-k material often forms at the interface of a semiconductor and high-k dielectric, which significantly reduces the modulation advantages of using the high-k. Interface quality will be investigated heavily in this work, specifically in Section V.

- Reliability/Stability: The insertion of a new material into the device should not significantly impact the reliability or stability of the device, physically or electrically. Many dielectrics exhibit a fixed charge, which can significantly change the electrical performance of a device. Fixed charge, the stability, and reliability of choice ZnO/high-k dielectric devices will be studied throughout this work and explicitly in Section VI.

The Silicon CMOS device industry has been heavily investigating high-k dielectrics for over a decade and niche products, such as memory devices, have been employing high-k materials for much longer. As a result, some information regarding the six criteria explained above exists allowing us to identify a few key materials for integration with ZnO from the numerous high-k materials that have been investigated for electronic applications. The following four high-k materials will be investigated in this work:

2.2.1 Al_2O_3 deposited by atomic layer deposition

Al_2O_3 has been heavily researched as a near-term solution to reducing EOT in Silicon devices. With a $\kappa_{ox} = 9$ it is on the low side of high-k materials, but with a large band gap (E_G = 8.7 eV) and favorable conduction band offset with Silicon the leakage properties make it one of the most stable high-k materials, when

integrated with Silicon. An initial drawback was a thick interfacial layer of SiO_2 which would form between Silicon and Al_2O_3 completely eliminating the gains of the high-k material [82]. This issue was overcome by development of Atomic Layer Deposition (ALD). Via ALD, it is possible to deposit amorphous Al_2O_3 films with high-quality film morphology on without a native layer of SiO_2 forming. We will investigate Al_2O_3 via ALD as a possible high-k dielectric for ZnO devices.

2.2.2 HfO_2 deposited by atomic layer deposition

HfO_2 has emerged as another candidate for reducing EOT in Silicon devices. With a $\kappa_{ox} = 25$ it is more attractive than Al_2O_3, but with a smaller band gap ($E_G = 5.7$ eV) and conduction band offset, it has proven to be less stable when integrated with Silicon. HfO_2 devices have been reported with negligible hysteresis, which is a superior electrical stability result. A drawback is that non-negligible V_{FB} offsets have been reported, but thought to result from oxygen diffusing into the Silicon to from an uncontrolled interface layer with Silicon [82]. This issue is not expected to result in deleterious effects with integrated with ZnO. As we have seen with Al_2O_3, some undesirable interfacial effects can be eliminated by using the ALD deposition method. As a result, we will investigate HfO_2 via ALD as a possible high-k dielectric for ZnO devices.

2.2.3 Perovskite Oxides deposited by pulsed laser deposition

Lead Zirconate Titanate ($Pb[Zr_XTi_{1-X}]O_3$ or PZT) and Barium Strontium Titanate ($Ba_{0.5}Sr_{0.5}TiO_3$ or BST) are Perovskite oxides, which is a class of materials used in dynamic random access memory applications. Perovskite oxides can be ferroelectric, paraelectric, piezoelectric, and paraelectric and need to be in crystalline or poly-crystalline form to obtain extremely high-k values ($\kappa_{ox} > 300$). Research of Perovskite oxides as high-k dielectrics has required mono-layer control of the inter-

face and a crystal or poly-crystal growth via Molecular Beam Epitaxy. Pulsed Laser Deposition, as stated above, is a much more versatile and cost effective method of deposition and can still achieve poly-crystalline films. In addition, ZnO is deposited via PLD so that, with these materials, the dielectric and ZnO can be deposited in the same chamber in the same deposition run so that the interface is not exposed to air, which should result in a higher quality interface than otherwise can be expected. In this work we investigate PZT and BST deposited via PLD as standard high-k dielectrics, but also as non-standard dielectrics that could add functionality (like memory) to ZnO devices.

2.3 Atomic layer deposition of high-k thin-films

As mentioned above atomic layer deposition (ALD) is a method used to deposit ZnO, but it is also heavily used for depositing high-k dielectrics. In this work we investigate HfO_2 and Al_2O_3 deposition via ALD for use as high-k gate dielectrics for ZnO TFTs.

ALD was developed as a deposition technique with two significant advantages over other thin-film methods: completely conformal coverage and mono-layer control as depicted in Figure 2.4.

The ALD process involves repeated cycles of self-limiting reactions that result in mono-layer by mono-layer build up of a desired material based on the chemical precursors used. Figure 2.5 demonstrates one ALD cycle used to deposit a mono-layer of Al_2O_3.

1. First, tri-methyl aluminum is exposed to the substrate and the molecules react and bond with molecules on the surface until all surface sites are populated. (Figure 2.5(1))

2. Second, a purge removes all unreacted tri-methyl aluminum and free methyl

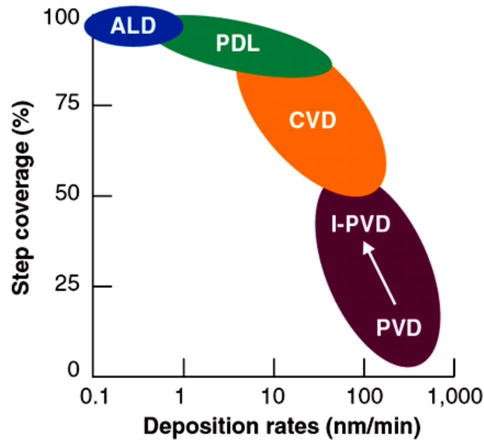


Figure 2.4: Deposition rate (thickness control) vs step coverage quality for leading thin-film deposition techniques [60]

groups from the chamber. (Figure 2.5(2))

3. Third, water vapor is exposed to the substrate and OH groups replace the mythyl groups weakly bonded to the Al (Figure 2.5(3)). There are two types of reactants used for incorporating Oxygen into materials like Al_2O_3 and HfO_2: water vapor or ionizing Oxygen gas via an Oxygen plasma. Both methods were investigated for Al_2O_3 , while only water vapor was investigated for depositing HfO_2.

4. Once all the surface sites have reacted with H_2O, the remaining water vapor is purged from the chamber leaving one mono-layer of Al_2O_3 on every surface site, regardless of orientation or angle.

The metal-organic precursor used for HfO_2 was tetrakis(ethylmethylamino)hafnium. In both cases, amorphous stochiometric Al_2O_3 and HfO_2 via ALD are investigated for insertion into thin-film ZnO devices.

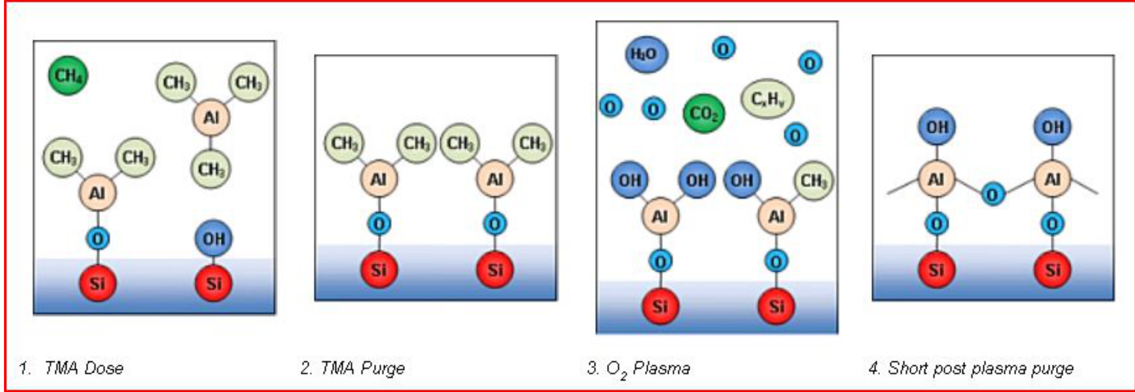


Figure 2.5: One cycle of ALD Al_2O_3 deposition [29]

2.3.1 ALD optimization

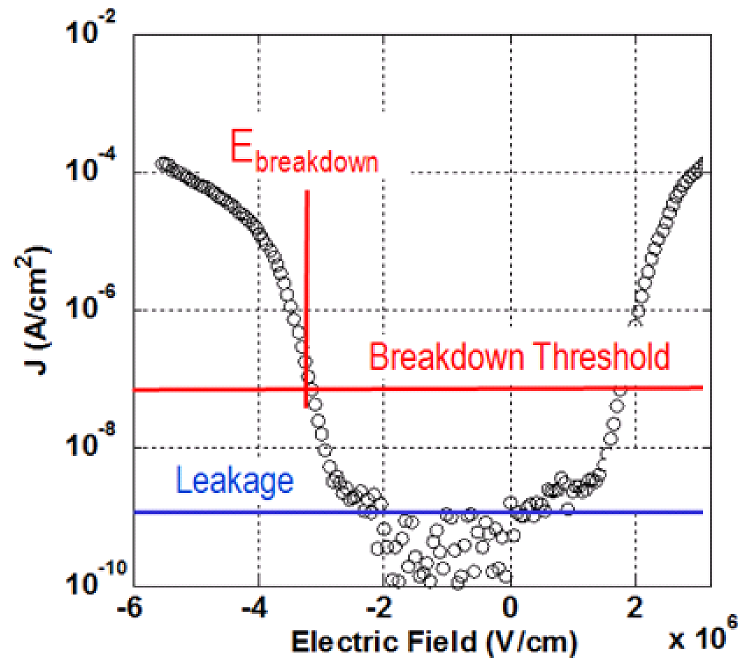
For our purposes of a high-k gate dielectric for ZnO TFTs we aim for a material with high dielectric constant and low leakage properties. The main variables in the ALD process are substrate temperature, chamber pressure, and plasma power and each was investigated to find the optimal values for Al_2O_3 and HfO_2 films. Deposited materials' dielectric constant values were tested by making metal-insulator-metal capacitors, measuring the capacitance then extracting the dielectric constant at zero volts using the relation

$$\kappa_{ox} = \frac{C_{MIM} t_{ox}}{\epsilon_0 Area}$$

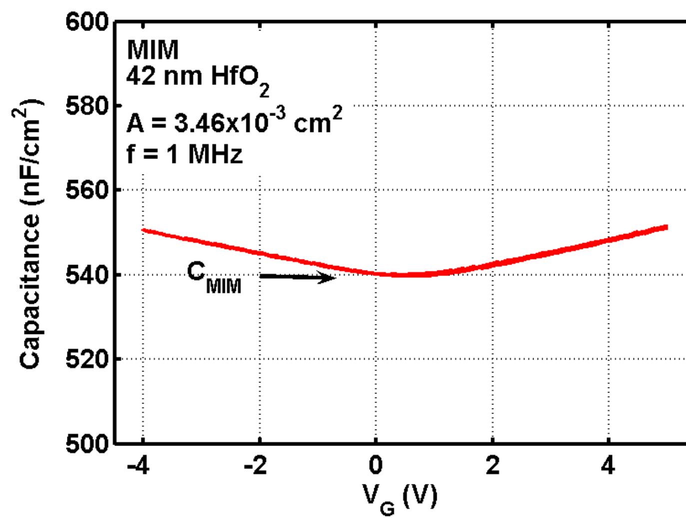
. The materials' leakage performance was evaluated by measuring the IV characteristics and taking the nominal value of leakage current in the low leakage region as shown in Figure 2.6(a).

Substrate temperature was varied from 100 to 350$^{\mathrm{O}}$C. The resulting dielectric constant and leakage values can be seen in Figure 2.7. The term 'plasma' indicates that Oxygen plasma was used to incorporate oxygen into the ALD process, while the term 'thermal' indicates water vapor was used.

With both materials there is a trend to higher dielectric constant values at higher temperatures while each material process appears to have its own leakage profile with

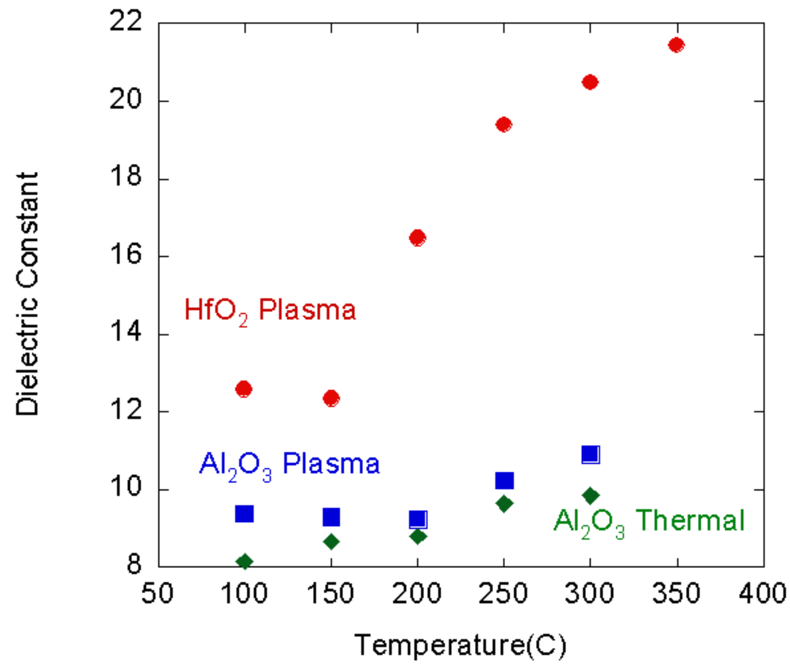


(a)

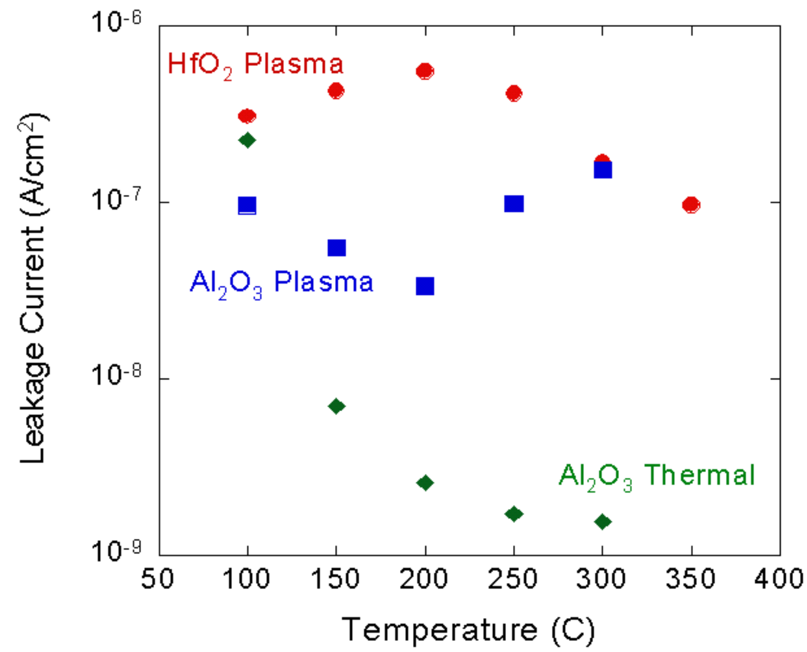


(b)

Figure 2.6: MIM characteristics used to track quality. (a) Example of MIM IV leakage. (b) Example of MIM CV plot.



(a)



(b)

Figure 2.7: Al_2O_3 and HfO_2 performance vs temperature. (a) Dielectric constant vs temperature. (b) Leakage current vs temperature.

temperature. The Al_2O_3 thermal process has the best leakage performance by two orders of magnitude while the HfO_2 plasma process has about twice the dielectric constant.

For the plasma processes, plasma power was varied from 100 to 300 Watts. The resulting thin-films' performance can be seen in Figure 2.8.

There is very little trend in dielectric constant or leakage current with plasma power. A slight increase in HfO_2 dielectric constant with increasing plasma power exists and it is unclear whether Al_2O_3 leakage current increases with plasma power or not.

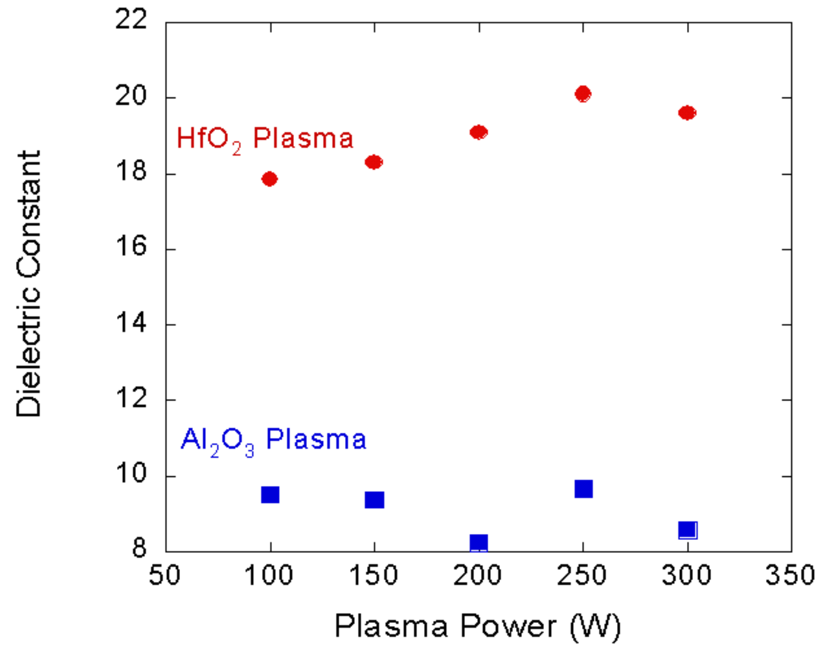
Chamber pressure was investigated, but before the study from 100 to 500 mTorr could be conducted, various flow rates involved in each ALD sub-cycle had to be carefully calibrated so that the result of all of the flows in each sub-cycle kept the chamber near the desired experimental value. Figure 2.9 shows the result of this optimization process for the desired chamber pressure of 300 mTorr.

Figure 2.10 shows the thin-films' performance with respect to chamber pressure.

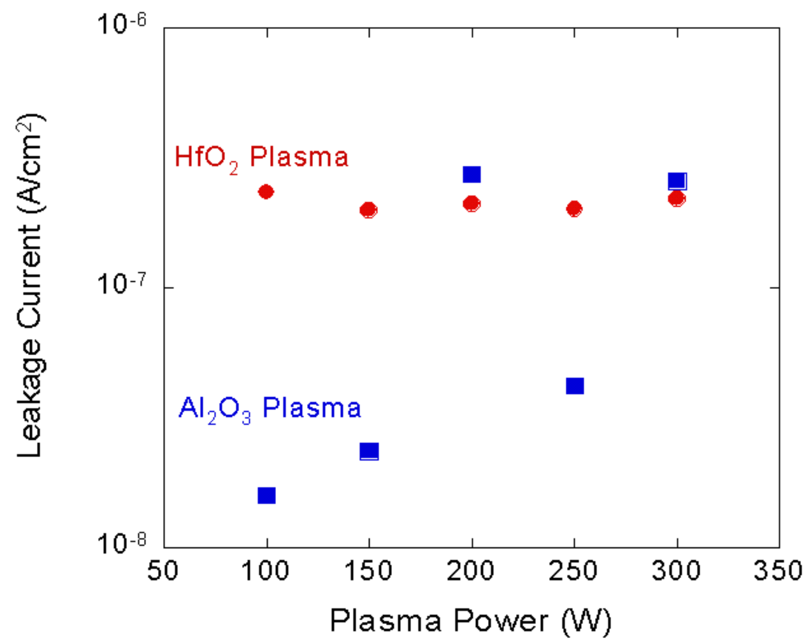
There seems to be no clear trend in thin-film performance with chamber pressure. For dielectric constant, there are peak values for the plasma processes, but it is unclear if this is due to statistical variation or a real trend.

2.3.2 ALD deposition summary

The films developed are amorphous in form as observed in transmission electron micrographs in Figure 2.2(b) and 2.2(c). From those figures thin interface layers can be seen between the Silicon and dielectric films, but no interfacial layer can be seen between the dielectric and ZnO, which is the interface of interest. From the investigation of the influence of ALD process variables on dielectric thin-film dielectric constant and leakage performance we find the optimal process conditions as described in Table 2.2. Work on high-k dielectrics sparked a collaboration with AFRL and



(a)



(b)

Figure 2.8: Al_2O_3 and HfO_2 performance vs plasma power. (a) Dielectric constant vs plasma power. (b) Leakage current vs plasma power.

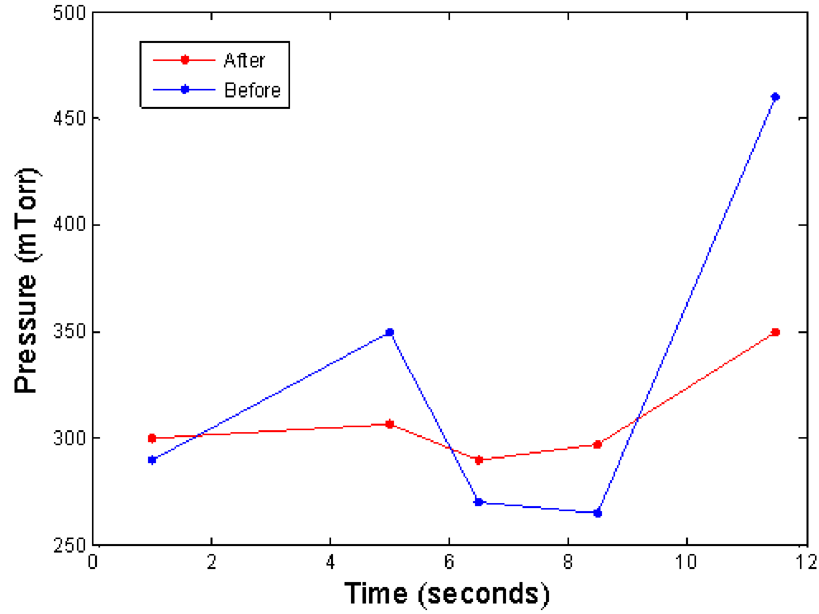
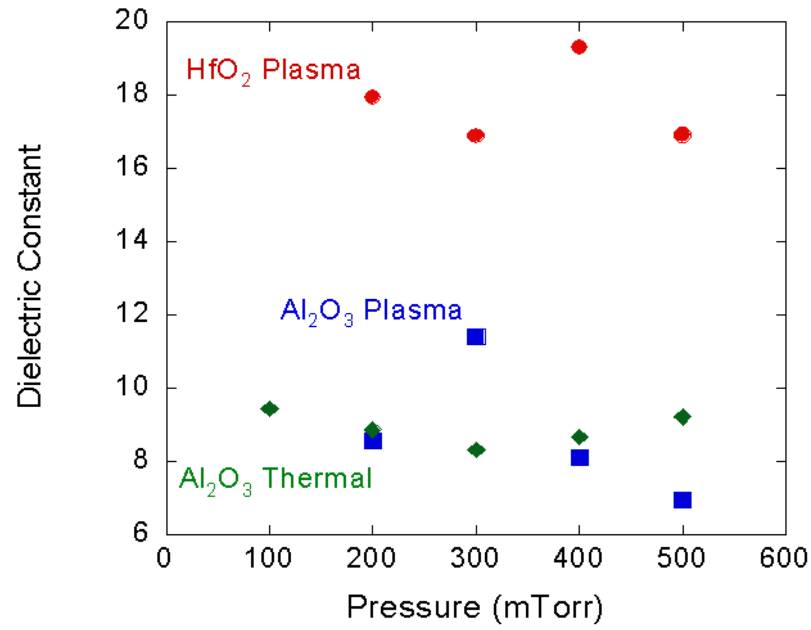


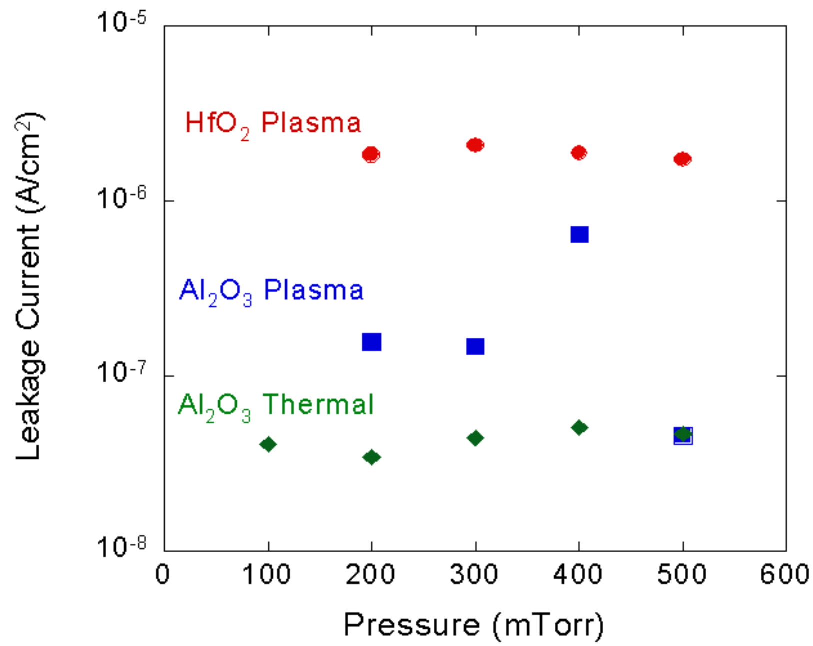
Figure 2.9: Chamber pressure throughout one entire ALD cycle before and after optimizing flow rates

ultimately resulted in their purchase of a Cambridge Nanotech ALD system on which a HfO_2 plasma process was mainly investigated. Optimal conditions and results of AFRL material, which were measured at the University of Michigan, has been tabulated below as well.

From the results of the investigation of ALD thin-film process conditions, we find similar results to those found in the Silicon industry; HfO_2 has an achievable κ_{ox} twice that of Al_2O_3, but Al_2O_3 has slightly better leakage performance. Leakage performance when integrated with ZnO is a much more important figure of merit and governed by additional factors, such as conduction band offset, not seen here. The next step is to integrate these dielectrics with ZnO and evaluate EOT and leakage properties.



(a)



(b)

Figure 2.10: Al_2O_3 and HfO_2 performance vs chamber pressure. (a) Dielectric constant vs chamber pressure. (b) Leakage current vs chamber pressure.

Thin-Film Process	Temp (^{O}C)	Plasma Power (Watts)	Chamber Pressure (mTorr)	Dielectric Constant	Leakage Current (nA/cm^2)	Breakdown Field ($10^6 V/cm$)
HfO_2 Plasma	350	250	Any	22	100	2
Al_2O_3 Plasma	250	100	Any	11	100	5
Al_2O_3 Thermal	300	N/A	Any	9	1	2
HfO_2 Plasma (AFRL)	250	300	(100 - 250)	19	10	3

Table 2.2: Al_2O_3 and HfO_2 optimal ALD process conditions. Films reported were nominally 20 nm in thickness.

2.4 Pulsed laser deposition of Perovskite Oxides

Both PZT and BST were developed at the University of Michigan. BST has been investigated for tunable dielectric permittivity applications such as voltage tunable microwave filters and PZT has been investigated for its piezoelectric and ferroelectric switching capabilities [14, 7].

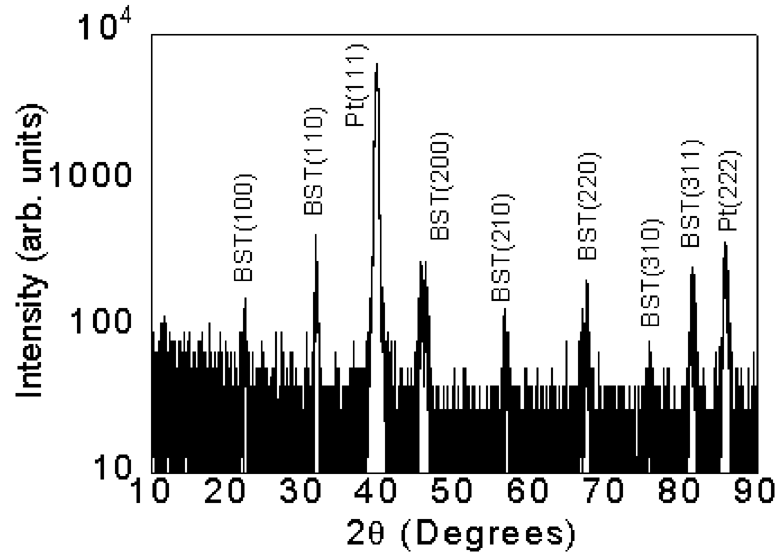
The same PLD system was used for the Perovskite Oxides as for the ZnO as explained in Section 2.1.1, but with the appropriate targets used for the film desired. The optimal PLD conditions for BST and PZT are shown in Table 2.3.

Deposition Variables	Range	BST	PZT
Substrate Temperature (^{o}C)	23 - 700	500	500
Oxygen Partial Pressure (mTorr)	$<$150	30	100
KrF Excimer Laser (nm)	248	248	248
Energy (mJ)	350 - 500	350	500
Pulse Repetition Rate (Hz)	1-30	10	10

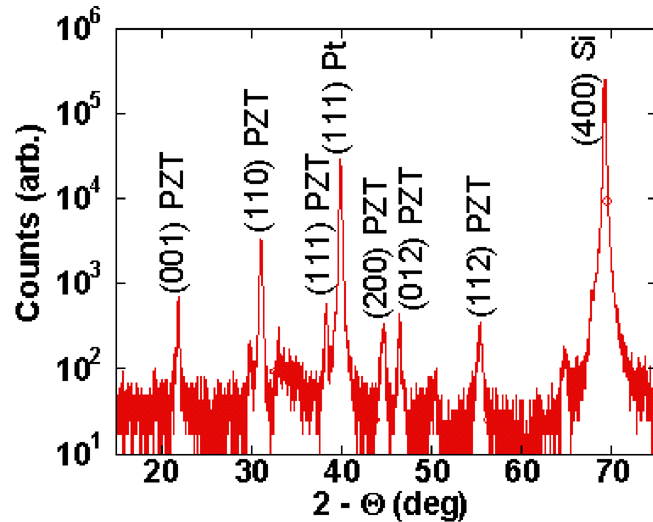
Table 2.3: Pulsed laser deposition conditions for BST and PZT

2.4.1 Perovskite thin-film properties

The crystalline quality of PLD BST and PZT were evaluated via XRD and the results can be seen in Figure 2.11. Both films' results show many crystal orientations of the desired material indicating no preferential orientation unlike the case with ZnO.



(a)



(b)

Figure 2.11: X-ray diffraction results for PLD thin-film (a) BST and (b) PZT

The electronic properties of BST, measured via a Pt-BST-Pt capacitors, can be

seen in Figure 2.12. The thin-film exhibits a high dielectric constant, peaking at $\kappa_{ox} = 700$, and paraelectric behavior of a 600 nm thick film. The leakage properties

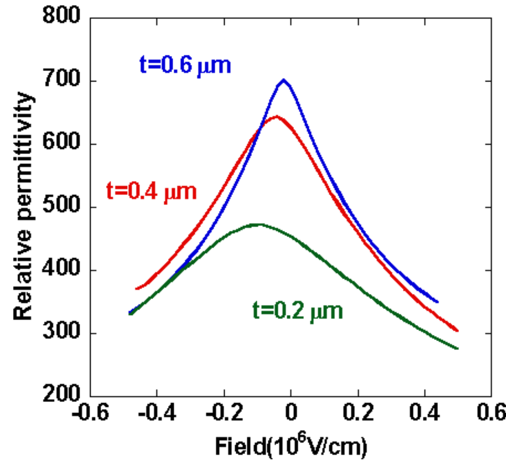


Figure 2.12: MIM capacitor results of a thin-film BST capacitor with varying film thicknesses.

of BST were studied on Pt - BST - ZnO capacitors with 740 nm of BST. Leakage currents were found to be in the range of 10^{-4} to 10^{-0} A/cm^2, which is extremely poor. Leakage characteristics are investigated further in Section 3.5.

The electronic properties of PZT via extraction from a Pt - PZT - ZnO (MIS) capacitor and will be presented in Chapter III. The extracted dielectric constant of a 900 nm thick PZT was found to be $\kappa_{ox} = 640$. Leakage currents were found to be in the range of 10^{-4} to 10^{-1} A/cm^2, which is extremely poor. Leakage characteristics are investigated further in Section 3.4.

Despite poor leakage performance and no preferred crystal orientation, both PZT and BST films deposited via PLD exhibit extremely high-k values. As a result (and due to the possible multi-functionality of Perovskite Oxides) both BST and PZT will be further investigated for use in ZnO devices.

2.5 Thin-film summary

From the investigation and development of ZnO with good material and electrical values, high-k ALD dielectrics, and very high-k and multi-functional Perovskite oxides we have identified several insulating thin-films as candidates for incorporation into ZnO thin-film devices. Moving forward, in Chapter III the integration of these high-k dielectrics with ZnO will be investigated followed by using these material systems for ZnO TFTs in Chapter IV.

CHAPTER III

Metal - High-k - ZnO Devices

It has been previously discussed that ZnO thin-films have desirable properties for electronic applications including thin film transistors. In Chapter II several high-k dielectrics have been identified and developed as candidates for the gate insulator layer in ZnO thin-film devices. Because the insulators will serve the function of modulating the gate electric field onto the ZnO, changing the carrier concentration and resistivity of the ZnO channel, it is important to study and understand the insulator-ZnO system in detail. This system is the key building block to most functional thin film devices. The metal - Insulator - semiconductor capacitor (MIS-Cs) is the research device used to probe the system.

Recent reports on ZnO/high-k material systems have focused on thin-film transistor performance, overlooking the MIS-C as a research vehicle. Past results focus on using ZnO in an MIS device actually have developed ZnO as a transparent conductor and used various other semiconductors for the active layer. As a result there is little reported past work on the topic of this investigation. In describing ZnO TFTs fabricated at room temperature, Zhang et al. reported significant CV hysteresis on the order of 2 V [85].

In this chapter we will use MIS-Cs to study the efficacy, advantages, and drawbacks of integrating the high-k dielectric thin-films developed in Chapter II with ZnO.

From the studies in this chapter we will be able to learn about each heterostructure's modulation characteristics and non-idealities, about the role and effect of these non-idealities, and how to minimize or take advantage of non-idealities and functionalities.

3.1 MIS-C theory

To be able to learn from our study of ZnO/high-k MIS-Cs we must understand what to expect from the results and what non-idealities exist that we can identify. Similarly to evaluating the thin-films in Section II, capacitance-voltage (C-V) and current-voltage (I-V) leakage measurements are conducted. From the I-V measurements we can learn about how well the gate dielectrics insulate when sharing an interface with ZnO. Band offsets and non-ideal leakage paths can contribute to poor leakage performance. From the C-V profile of an MIS-C a great deal of information can be learned as will be explained in this sub-section.

A MIS-C is simply a four layered structure as depicted in Figure 3.1(a); a contact metal, the insulating dielectric, the semiconductor, and another metal contact. In the ideal case we assume no contact resistance, perfect interfaces between each layer, and the insulator is perfect.

The equivalent circuit for an ideal MIS-C can be seen in Figure 3.1(b) as the capacitance of the dielectric in series with the capacitance of the semiconductor with a characteristic capacitance of

$$\frac{1}{C_{Total}} = \frac{1}{C_{OX}} + \frac{1}{C_{ZnO}} \tag{3.1}$$

where C_{Total} is the total capacitance of the system, C_{OX} is the capacitance of the gate dielectric (traditionally called 'oxide'), and C_{ZnO} is the capacitance of the depletion region that forms in the semiconducting ZnO when an electric field is applied. The capacitance of the dielectric is the material's permittivity divided by the film thick-

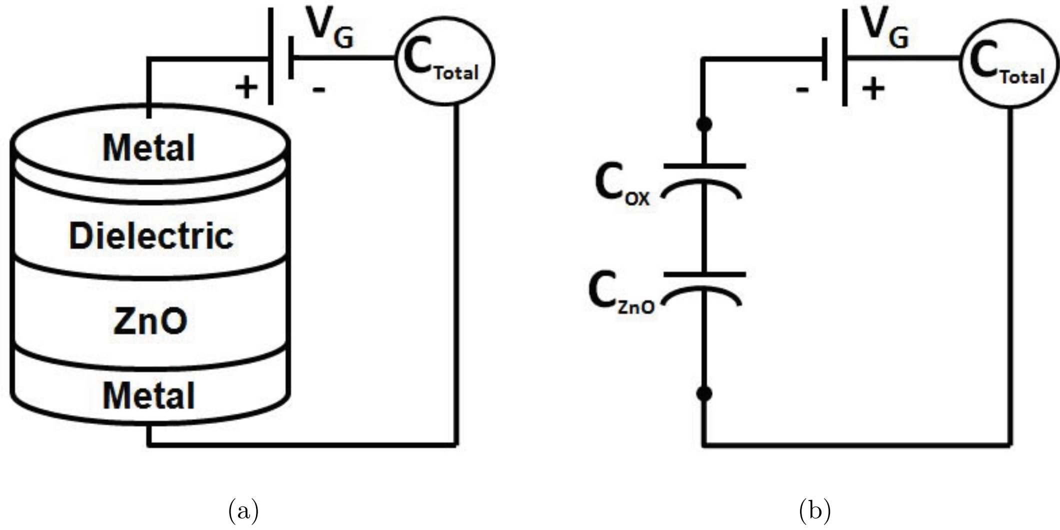


Figure 3.1: Ideal Metal-Insulator-Semiconductor Capacitor. (a) Schematic. (b) Equivalent circuit.

ness ($C_{OX} = \kappa_{ox}\epsilon_0/t_{ox}$) and the capacitance of the ZnO depletion region is the ZnO permittivity divided by the thickness of the depletion region so the total capacitance becomes

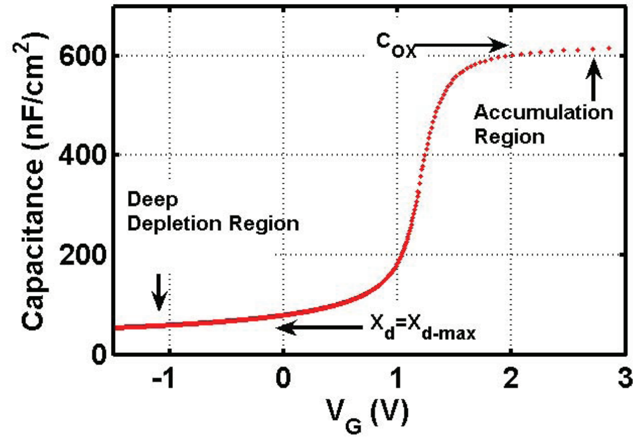
$$\frac{1}{C_{Total}} = \frac{t_{ox}}{\kappa_{ox}\epsilon_0} + \frac{x_d}{\kappa_{ZnO}\epsilon_0}$$

. When an applied voltage (V_G) is swept across an MIS-C x_d is the only dependent variable. In the case that x_d reaches a maximum (x_{d-max}), called deep-depletion, C_{Total} reaches a minimum and in the case where V_G is a polarity that attracts majority carries, called accumulation, there is no depletion region and $C_{Total} = C_{OX}$. In the critical voltage region between accumulation and deep-depletion analytical equations have been developed to calculate the semiconductor capacitance ($C_s = C_{ZnO}$), charge (Q_{ZnO}), and surface potential (ψ_{ZnO}) of an ideal MIS-C with respect to V_G and thus the ideal C-V profile can be evaluated [10]. An example of calculated C_{Total}, Q_{ZnO}, ψ_{ZnO} curves for a MIS-C with input material values can be seen in Figure 3.2.

With a solid understanding of the expected, ideal, C-V characteristics of a MIS-C device, we can test, learn from, and identify non-idealities in experimental data more

Input Variable	Value
$Temperature$(K)	300
$Area$ (cm)	3.46x10^{-3}
t_{ox} (cm)	297x10^{-8}
ϵ_{ox} (unit-less)	19.3
t_{ZnO} (cm)	2570x10^{-8}
ϵ_{ZnO} (unit-less)	10
ϕ_{MS} (eV)	1.2
N_D (cm^{-3})	3x10^{16}

(a)



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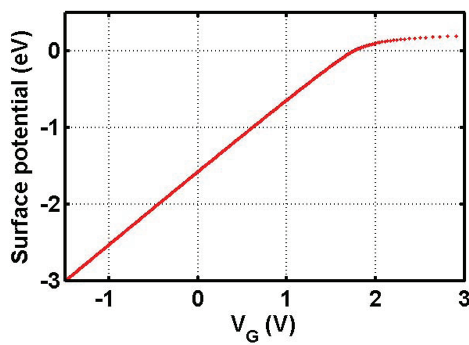
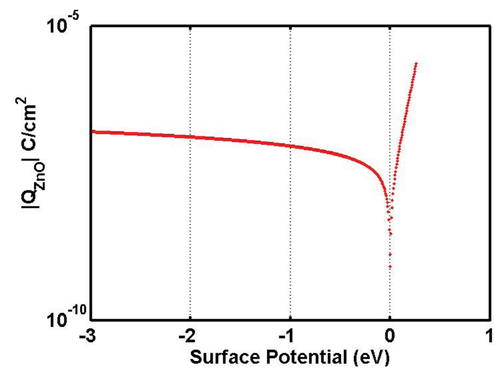


(c)



(d)

Figure 3.2: Calculated values for an ideal MIS-C device. (a) Table of input parameters. (b) C_{Total} vs V_G. (c) ψ_{ZnO} vs V_G. (d) Q_{ZnO} vs ψ_G.

effectively.

Another valuable perspective to view MIS-C devices is via the energy band diagram of an ideal MIS-C. From a band diagram one can understand what the potential values across the insulator and ZnO are, know what mode of operation a device should be in (depletion, flatband, accumulation), and look at various band offsets in the system. Figure 3.3 shows the band diagram for an ideal Platinum-HfO_2-ZnO capacitor in accumulation, flatband, and depletion. The band offsets were calculated using reported electron affinity values for the materials and it should be noted that actual heterojunction band offsets often deviate from those predicted via the electron affinity model.

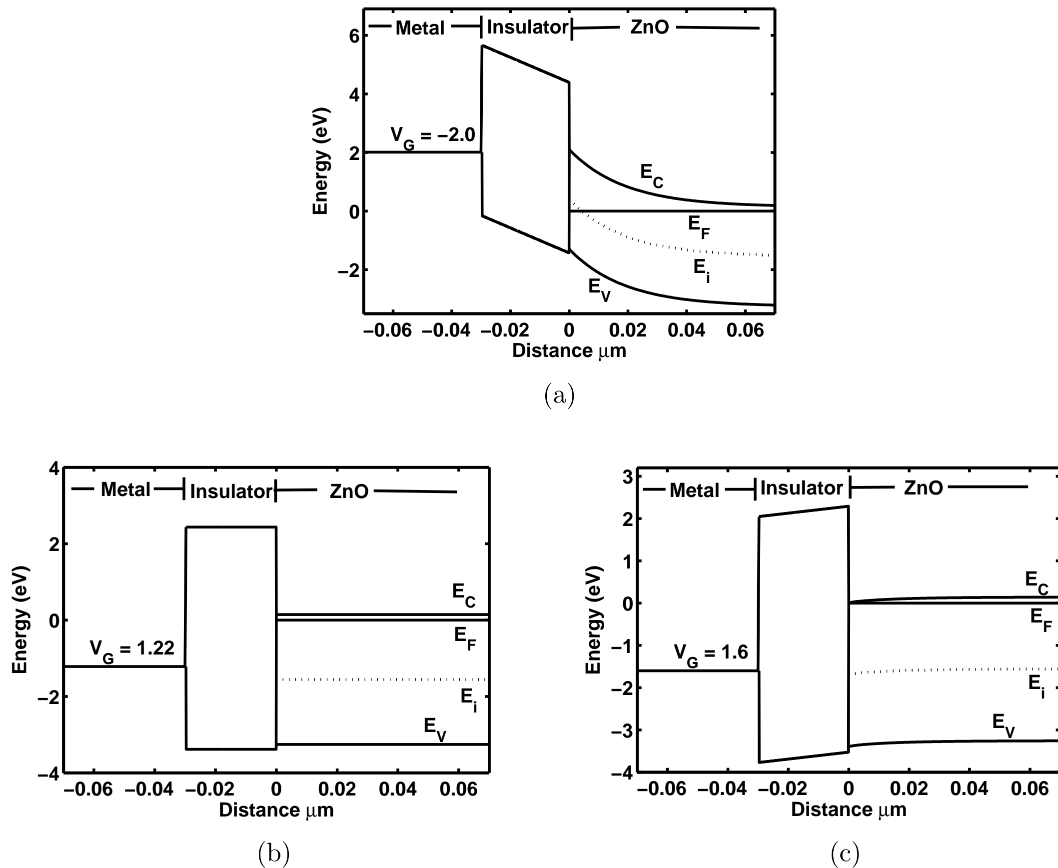


Figure 3.3: Energy band diagrams for an ideal Pt - HfO_2 - ZnO capacitor. (a) Depletion. (b) Flatband. (c) Accumulation.

From Figure 3.3 it can be seen that there is a very small band offset between the

valance band of HfO_2 and that of ZnO. This is insufficient as an insulator for holes, but it can be seen that the Fermi level is close to the conduction band indicating strong n-type action and considering the large band-gap of ZnO, holes are practically non-existent as a minority carrier.

3.1.1 MIS-C non idealities

As important as it is to understand the expected operation of an ideal MIS-C, as we develop new materials and devices it is equally important to understand non-idealities that are likely to occur during development. Significant work has been done in Metal-Insulator-Silicon capacitor theory to understand and explain non-idealities and their sources. Nearly all of these issues translate into all MIS-C development and most can be identified via C-V measurement.

Non-idealities in the dielectric (oxide) Three types of non-ideal charge that can be present in the dielectric are fixed oxide charge, mobile ionic charge, and trapped oxide charge. Fixed oxide charge is caused by impurities frozen or 'fixed' in the oxide during materials deposition or device processing. These charges have the effect of shifting the C-V curve of an MIS-C from the ideal condition.

Mobile ionic charge is caused by ions located in, and free to move through, the dielectric's material matrix. Under applied bias these charges move, hence changing the effect they have on the C-V depending on the applied voltage. Historically positive ions Sodium and Potassium will be pushed away from a positive applied bias and then pulled back as the bias sweeps towards negative, this results in a C-V hysteresis, which means the C-V curve, when taken from positive V_G values to negative V_G values is shifted in voltage from the C-V curve taken from negative V_G to positive V_G. In the case of positive mobile ions, the hysteresis is described as 'counter clockwise'.

This hysteresis effect is witnessed over time scales from seconds to minutes as the

longer the mobile ions are influenced by a field, the farther in the dielectric they move and thus the magnitude of the hysteresis will change as well.

Oxide trapped charge is charge that has been 'trapped' in oxide sites distributed throughout the oxide layer. Generally carriers will have been excited from the semiconductor into the oxide and when trapped, charges act as fixed charge causing a shift in the C-V profile. In this case, a field is required to populate the traps and carriers often de-trap with a reverse field or often simply with time. Oxide trapped charge is a contributor to unstable devices and will be studied in depth in future sections of this work. A C-V profile shift can be measured by comparing the measured flatband voltage (V_{FB}) with the ideal case. The flatband voltage is the V_G value at which the flatband capacitance (C_{FB}) occurs. C_{FB} can be calculated by the C-V calculations discussed above and an experimental MIS-C's V_{FB} is found to be V_G when $C = C_{FB}$. The ideal V_{FB} is the difference between the metal and semiconductor's work functions $V_{FB} = \chi_M - \chi_{ZnO}$. In our case, with a Platinum metal contact and ZnO semiconductor, $V_{FB-ideal} = 1.2$ V.

It should be noted that Silicon based memory devices based on the strictly controlled trapping and un-trapping of oxide and interface charge are in large-scale use today, so this is not always an unwanted condition, but in any case oxide trapped charge is an element of device performance that must be understood.

The time scale that charges can be trapped and un-trapped in the oxide range with the energy level at which the traps exist and also the distance the trap cites exist from the semiconductor/dielectric interface. Shallow traps near the interface can trap and de-trap on timescales less than one second while deep traps or traps located far from the interface can take minutes to many hours to trap or un-trap.

Non-idealities at the dielectric-ZnO interface In many cases of high-k integration with semiconductors many mono-layers of the dielectric at the interface with

the semiconductor experience chemical intermixing with semiconductor elements or other impurities essentially inserting a low-k capacitor between the C_{OX} and C_{ZnO} [44]. The most obvious effect on the MIS-C performance is a lowering of C_{OX} and the effective dielectric constant of your dielectric.

A more far-reaching non-ideality that can occur at the interface between the dielectric and ZnO is interface trapped charge (Q_{it}). Interface trapped charge is detrimental to device performance, limiting the speed, in voltage, that a device can modulate channel current. In thin film transistors, interface trapped charge is known to limit subthreshold slope performance, a performance metric for many applications. Q_{it} is caused by dangling bonds and impurities present during processing that create sites that are spatially located at the interface, but energetically distributed throughout the ZnO bandgap. This distribution of charge, in energy, results in a distorted C-V with a slope from depletion to accumulation less than that of the ideal case as depicted in Figure 3.4. The deviation from the ideal case is due to Dit as shown in Equation 3.2.

$$V_G^{ideal} - V_G^{meas} = \frac{q \int_{\phi_{S1}}^{\phi_{S2}} D_{it} \left(\phi_S\right) \delta\phi_S}{C_{OX}} \tag{3.2}$$

Q_{it} also causes slight dispersion in the C-V profile over a range of frequencies [3] and results in a spike in the conductance-voltage curve (G-V) [63]. Several of the interfaces investigated in this section show signs of Q_{it}; as a result a detailed study of interface trapped charge is presented in Chapter V. It is also possible for a slight 'clockwise' hysteresis to result from the occurrence of 'slow' interface traps where "some of the accumulated electrons are transferred into the unoccupied surface states during the upswing of V_G, and when V_G is swept down these states remain filled until the trapped electrons are thermally de-trapped" [64].

It is important to understand that interface trap time constants will trend with

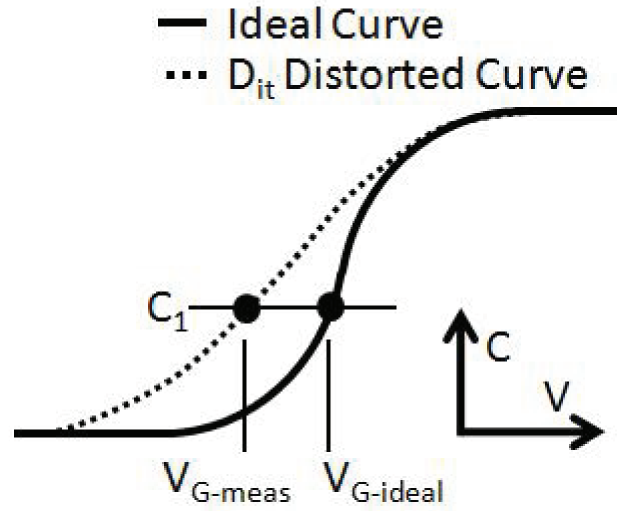


Figure 3.4: Representative Curves: Ideal C-V vs D_{it}-influenced C-V (adapted from [53])

energy within the bandgap. As a result, the frequency at which a C-V curve is taken will have various levels of contribution from interface trapped charge. A high frequency C-V might be immune to a large population of traps that cannot respond in the time scales necessary. Such a curve might look fairly ideal. A low frequency C-V sweep of the same device may suffer considerable slope distortion due to the contribution of a large population of interface states.

3.2 Fabrication

Platinum coated Silicon wafers were purchased from Radient Technologies and the Platinum served as our gate metal on which the insulators and ZnO were deposited to form the MIS-Cs. The insulators were deposited directly on the Platinum and then 2000 Å of ZnO was deposited on the insulators via PLD. Both materials were deposited via methods described in Chapter II. In order to make electrical contacts to the ZnO, circular metal ohmic contacts of Ti (200 Å) / Al (1000 Å) / Au (2000 Å) with an area of 3.5×10^{-2} cm^2 were deposited via electron beam evaporation and

photolithographic lift-off. Next, a gate via etch was performed so that the gate could be electrically contacted. PZT and BST are etched by a 1:2 Buffered Oxide Etch:H_2O solution. Al_2O_3 is etched by Buffered Oxide Etch and HfO_2 is etched in the LAM 9400 Reactive Ion Etch Tool at the University of Michigan using 3:2 Cl_2: BCl_2 gas ratio and an RF power of 300 Watts.

We tested devices at this juncture and found significant frequency dispersion, C-V accumulation slope, and conductance accumulation slope. These issues are all signs of gate leakage [3], which was confirmed to be high above $V_G = 2$ V directly corresponding to the accumulation region. A gate isolation etch was performed to eliminate ZnO from non-device areas surrounding the ohmic contact-defined MIS-Cs. Because the bottom gate was a blanket layer across the sample, the etch was done to eliminate carriers influenced by the gate, but outside the device structure. The ZnO device isolation etch was performed for 60 seconds in a solution of Buffered Oxide Etch(1): Deionized Water(2). The etch eliminated the gate-leakage and associated C-V characteristics. The resulting device structure is figuratively represented in Figure 3.5.

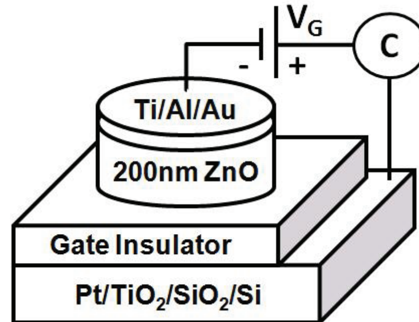


Figure 3.5: Metal-Insulator-Semiconductor Capacitor (MIS-C) Device

3.3 MIS-C testing

MIS-Cs were tested using an Alessi Probe Station and probe positioners in a dark box with Cascade Microtech 45 degree bend Tungsten probe tips. A Keithley 4200 Semiconductor Characterization System, with four current-voltage source-measurement units (SMUs) with auto-calibration functionality and one capacitance-voltage unit (CVU) with open and short cable compensation algorithms, was used for all electrical source and measurement testing. Initially, I-V and C-V sweeps were done from $V_G = 0$ V in slowly increasing voltage steps in order to make sure the limits of each insulator-ZnO system were known before full testing was completed on a device. Unless otherwise indicated, I-V sweeps were a single sweep from negative voltages to positive voltages and C-V devices were, "Dual-Swept", biased at the maximum positive voltage (V_{max}) for 5 seconds, swept to the minimum negative voltage (V_{min}), and immediately back to (V_{max}).

3.4 PZT/ZnO heterojunctions

Pt - PZT - ZnO capacitors with an area of 1.65x10^{-4} cm^2 and PZT thickness (t_{ox}) of 900 nm were fabricated and tested at a frequency of 1 MHz as shown in Figure 3.6.

First, $C_{OX} = 630$ nF/cm^2 and using $C_{OX} = \frac{\kappa_{ox}\epsilon_0}{t_{ox}} Area$ the dielectric constant of PZT in the MIS-C is found to be $\kappa_{ox} = 645$, Secondly, $C_{min} = 158$ nF/cm^2 corresponds to $t_{ZnO} = 56$ nm, which is very close to the deposition target thickness of 60 nm. We see a peak in C_{OX} at $V_G = 4$ V which could be result of the positive peak in in the PZT 'butterfly' C-V characteristic. This voltage corresponds to a coercive field of 44 kV/cm. In the case of typical ferroelectric C-V action, the pronounced clockwise hysteresis on the order of 4 V can be attributed to 'ferroelectric hysteretic memory window' and is equal to the 4 V hysteresis window reported on Pt-PZT-

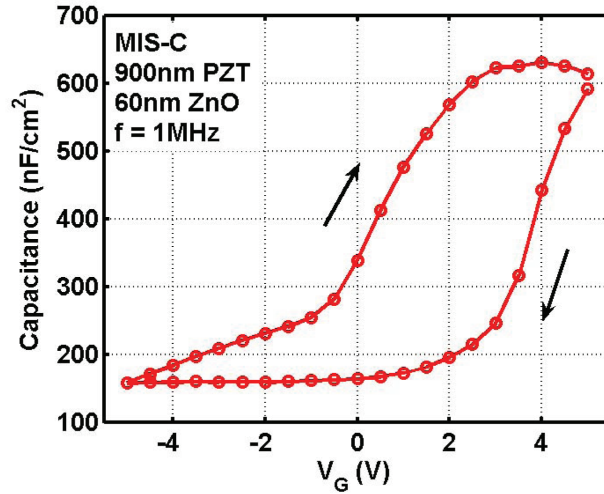


Figure 3.6: CV of Pt - PZT - ZnO capacitor

ZnO capacitors made with sol-gel processed PZT and the ZnO process described in Chapter II [7].

The I-V leakage characteristics of the Pt - PZT - ZnO capacitors can be seen in Figure 3.7. Immediately it can be seen that there is a large leakage in this MIS system

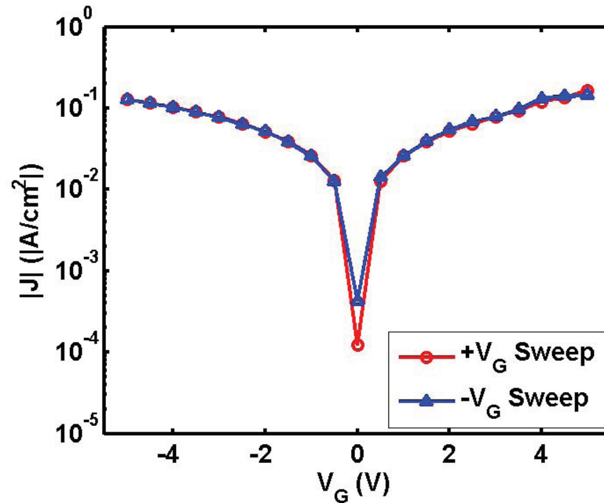


Figure 3.7: I-V leakage characteristics of Pt - PZT - ZnO capacitors

in both the forward and reverse directions. One possible reason for this high level of leakage is the PZT/ZnO conduction band offset [7]. The electron work function values used for PZT and ZnO are 3.5 eV and 4.45 eV respectively. Assuming a band

lineup that follows the electron work function, the conduction band discontinuity is 0.95 eV, which may not be large enough to act as an electron barrier. The energy band diagram for the Pt - PZT - ZnO material system can be seen in Figure 3.8.

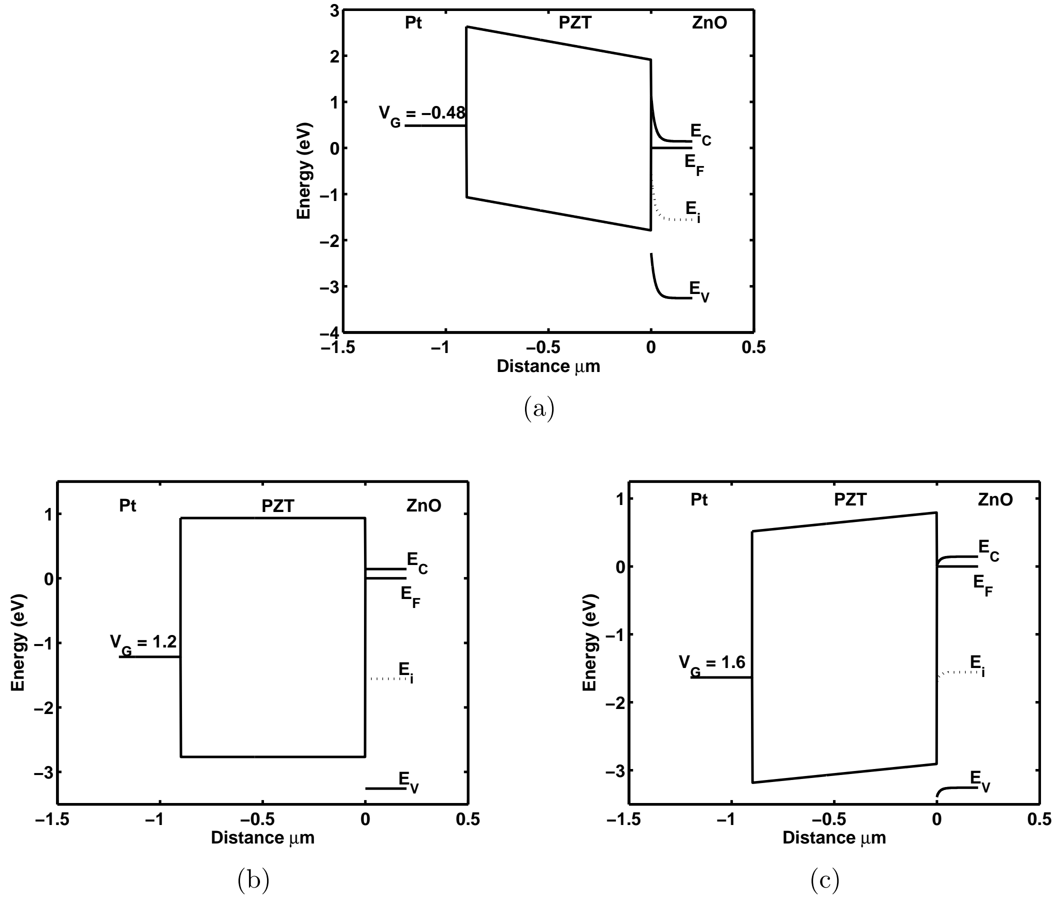


Figure 3.8: Energy band diagrams for an ideal Pt - PZT - ZnO capacitor. (a) Depletion. (b) Flatband. (c) Accumulation.

We see that the Pt - PZT - ZnO capacitor has a high C_{OX} and modulates the charge in the ZnO from depletion to accumulation as we expect a high-k material would. A large hysteresis is present in the system, which could be troublesome for typical TFT applications, but advantageous if used as a memory device. Finally, poor leakage performance of the MIS-C is certainly the large drawback of this material system, especially for such a large value of film-thickness.

3.5 BST/ZnO heterojunctions

Pt - BST - ZnO capacitors with an area of 1.65×10^{-4} cm^2 and a BST thickness of $t_{ox} = 740$ nm were fabricated and tested at a frequency of 1 MHz as shown in Figure 3.9.

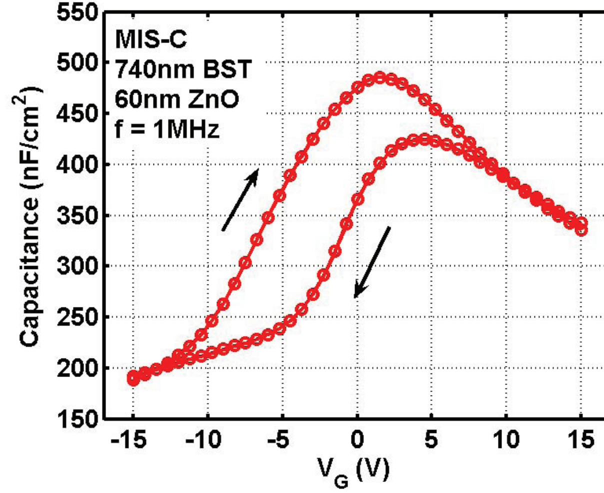


Figure 3.9: CV of Pt - BST - ZnO capacitor

The capacitance of the system contains a non-standard peak at $V_G = 1.5$ V and 4.5 V in the forward and reverse sweep directions, respectively. This peak behavior is due to the paraelectric nature of BST with a peak ϵ_{ox} at $V_{applied} = 0$ V. The 1.5 V offset in the forward direction C-V curve is likely due to the fact that in an MIS-C, 0 V across the dielectric occurs at the flatband condition ($V_G = V_{FB}$) and not at $V_G = 0$ V. In the ideal case the flatband condition is described by Equation 3.3

$$V_{FB} = \frac{\phi_{MS}}{q} = \frac{\chi_M - \chi_S}{q} \tag{3.3}$$

where χ_S and χ_M are the electron work functions of the semiconductor and dielectric contact metal, respectively. The work function used for Pt is 5.65 eV and for ZnO 4.45 eV resulting in V_{FB} =1.2 V, which is close to the offset value of 1.5 V. In the case of the reverse sweep with a peak at 4.5 V, which is 3 V different from the forward sweep

peak, it is likely oxide trapped charge or interface charge play a large role in producing this offset. In addition, between deep-depletion and accumulation a hysteresis voltage as high as 5 V is observed, which is also likely a result of oxide trapped charge or interface trapped charge. Investigations into the source of non-ideal charges in MIS-C devices are presented in Chapters V and VI. The value of C_{max} = 486 nF/cm^2 corresponds to the peak value of κ_{ox}. The peak dielectric constant of BST, taken from the maximum value of capacitance in the MIS-C, is found to be $\kappa_{ox} = 408$, which is much less than predicted by MIM structures measured in Chapter II. C_{min} = 189 nF/cm^2 corresponding to t_{ZnO} = 47 nm, which is 13 nm less than the deposition target thickness of 60 nm, but as it seems the C-V has not reached a minimum at V_{G-min}, we can only say that $t_{ZnO} > 47$ nm.

The I-V leakage characteristics of the Pt - BST - ZnO capacitors can be seen in Figure 3.10. As with PZT there is a large leakage in this MIS system in both the

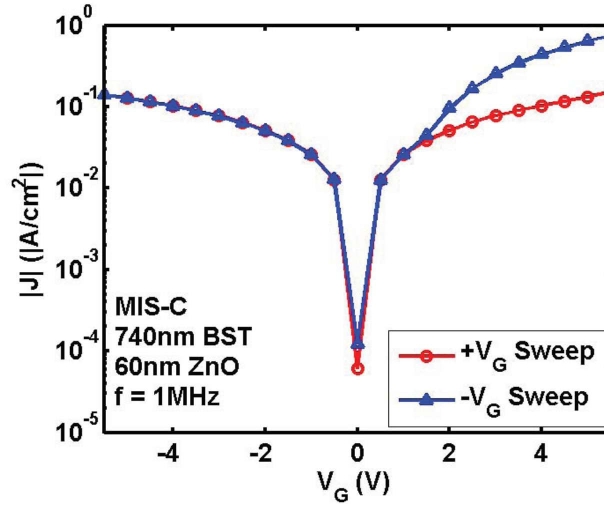


Figure 3.10: I-V leakage characteristics of Pt - BST - ZnO capacitors

forward and reverse directions. One possible reason for this high level of leakage is the BST/ZnO conduction band offset. The work function values used for BST and ZnO are 4.1 eV and 4.45 eV respectively. Assuming a band lineup that follows the work function model, the conduction band discontinuity is 0.35 eV, which is certainly

not large enough to act as an effective electron barrier. The energy band diagram for the Pt - BST - ZnO material system can be seen in Figure 3.11.

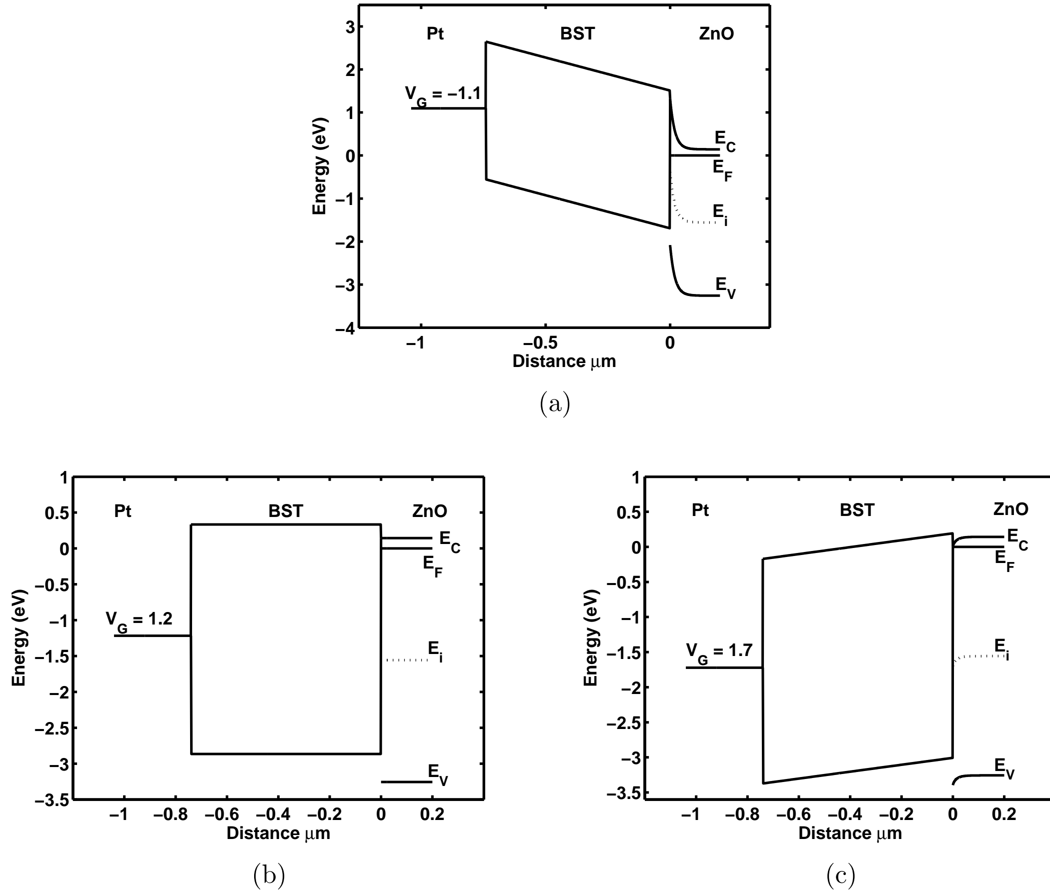


Figure 3.11: Energy band diagrams for an ideal Pt - BST - ZnO capacitor. (a) Depletion. (b) Flatband. (c) Accumulation.

Frequency dependent C-V curves were measured on the Pt - BST - ZnO from 5 kHz to 1 MHz and can be seen in Figure 3.12. Significant frequency dispersion is observed in the C-V curves in the accumulation region. While the frequency response of the BST was not investigated, this dispersion is typical of MIS-C devices with significant gate leakage, which is also the case with this material system.

In summary, Pt - BST - ZnO capacitors are able to take advantage of the very high-k nature of BST and do reflect the paraelectric characteristics of the dielectric. Unfortunately, as with PZT, a major drawback is the high leakage current present in

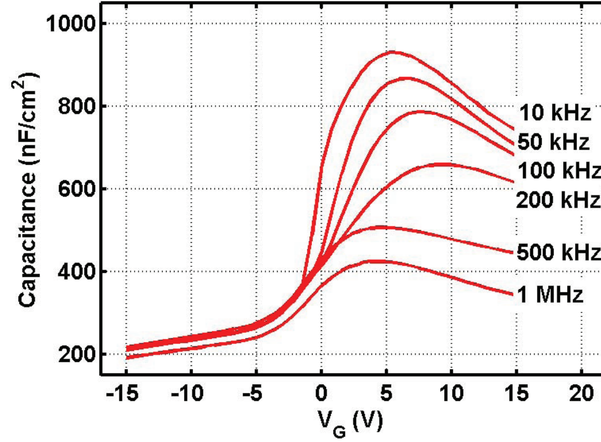


Figure 3.12: C-V of Pt - BST - ZnO capacitor at frequencies from 10 kHz to 1 MHz

this material system, which is likely due to the conduction band offsets between the dielectric and the ZnO.

3.6 Al_2O_3/ZnO heterojunctions

Un-isolated circular Pt - Al_2O_3 - ZnO capacitors with an area of 3.46x10^{-3} cm^2 were fabricated and tested at a frequency of 1 MHz. The Al_2O_3 was deposited via the ALD Thermal process discussed in Chapter II with t_{ox} =27 nm. The ZnO was deposited at AFRL with t_{ZnO} = 192 nm; both film thicknesses were measured by reflectance. and The capacitance-voltage and conductance-voltage curves are shown in Figure 3.13. C_{max} does not level out making the determination of C_{OX} and κ_{ox} challenging. The slope of the capacitance and conductance curves in the accumulation are tell-tale signs of leakage, which is further corroborated by the fact that the leakage current profile (Figure 3.14) shows significant leakage above $V_G = 1$ V. As a result C_{OX} can only be estimated as C at 1 V. $C_{OX} \approx 308$ nF/cm^2 corresponding to $\kappa_{ox} \approx 9.5$, which is the dielectric constant expected from the ALD thermal process. $C_{min} = 53$ nF/cm^2 corresponding to $t_{ZnO} = 165$ nm, which is on the same order as the measured thickness, but the source of the discrepancy is unclear. A clockwise hysteresis voltage

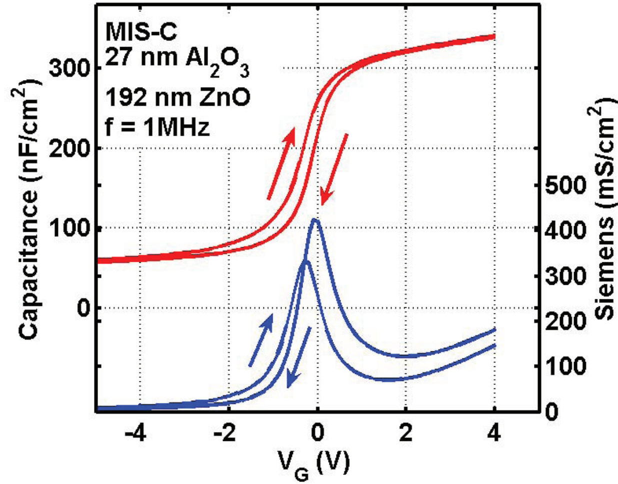


Figure 3.13: C-V and G-V of Pt - Al_2O_3 - ZnO capacitor

of 0.3 V is observed in both the C-V and G-V curves. A pronounced peak occurs between accumulation and depletion in the G_P curves, which has been closely tied to the presence of interface trapped charge [63]. The peak reaches $G_P = 425$ mS/cm^2 in the reverse direction, but only 335 mS/cm^2 in the forward direction, which may indicate more non-ideal charge present in the system after V_{max} bias than before. V_{FB} in the reverse direction is 0 V, which is 1.2 V less than the ideal case indicating oxide fixed charge may be present in the system.

The I-V leakage characteristics of the Pt - Al_2O_3 - ZnO capacitors can be seen in Figure 3.14. The MIS-C enjoys a 12 V range where leakage current is less than 10^{-7}

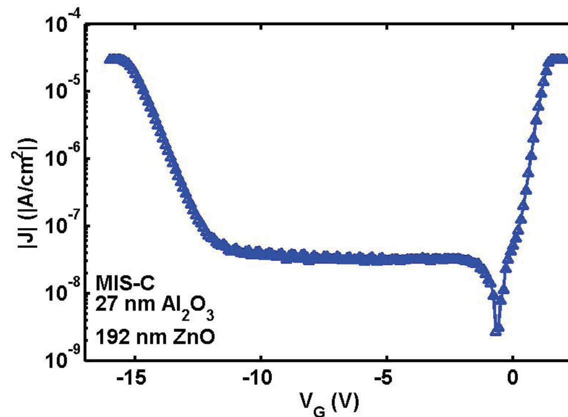


Figure 3.14: I-V leakage characteristics of Pt - BST - ZnO capacitors

A/cm^2. A non-ideal characteristic of these un-isolated devices is the asymmetric low-leakage range about the $V_G = 0$ axis. This asymmetry has been linked to un-isolated devices; in the case where V_G is positive, there is no limit to the carriers that can be attracted to the electrode, hence the isolating nature of the device is lost at positive values for V_G. From the superior leakage performance, compared to PZT and BST, one can expect the band offsets to be much larger in value. This is indeed the case and the energy band diagram for the Pt - Al_2O_3 - ZnO material system can be seen in Figure 3.15. The work function of Al_2O_3 is 1.35 eV and the resulting conduction

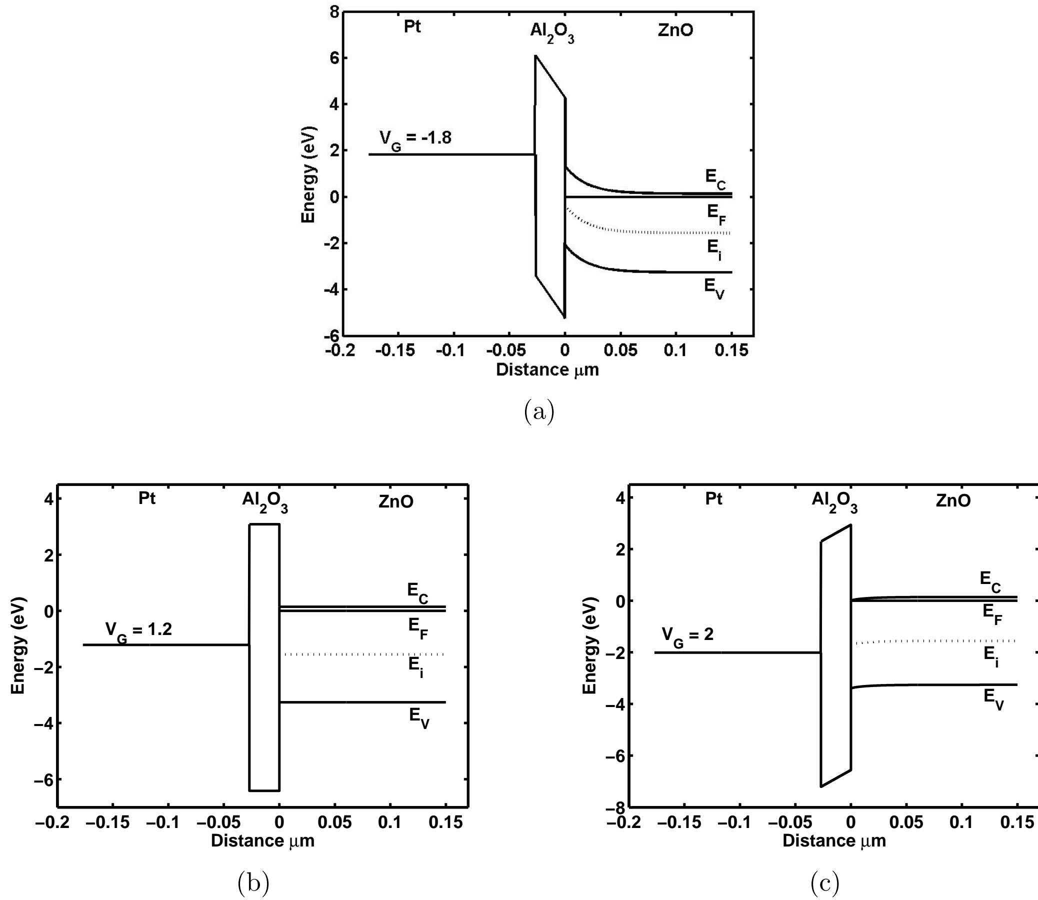


Figure 3.15: Energy band diagrams for an ideal Pt - Al_2O_3 - ZnO capacitor. (a) Depletion. (b) Flatband. (c) Accumulation.

band discontinuity between Al_2O_3 and ZnO is 3.1 eV over 3 times greater than those for PZT and BST dielectrics.

While it does not have the ϵ_{ox} values of PZT or BST, it has superior leakage characteristics which allow it to be an effective dielectric at much thinner thicknesses, boosting achievable C_{OX} values. It can be seen that superior leakage performance is largely due to advantageous energy band alignments. Though C_{OX} values reached little more than half those of PZT and BST, even with thicknesses 4% of the Perovskite oxides, Al_2O_3/ZnO has good modulation qualities, low hysteresis, and low leakage making it a promising candidate for high-k ZnO applications. Hysteresis, oxide trapped charge, and interface trapped charge are issues that may have a significant role in this material system and will be monitored as development continues in subsequent sections.

3.7 HfO_2/ZnO heterojunctions

Isolated circular Pt - HfO_2 - ZnO capacitors with an area of 3.46x10^{-3} cm^2 were fabricated and tested at a frequency of 500 MHz. The HfO_2 was deposited via the ALD Plasma process at AFRL as discussed in Chapter II with t_{ox} = 30 nm measured by ellipsometry. The ZnO was deposited at AFRL with a target t_{ZnO} = 200 nm. The capacitance-voltage and conductance-voltage curves are shown in Figure 3.16. C_{max} does level out and C_{OX} = 607 nF/cm^2 corresponding to κ_{ox} = 20.7, which is close to the value expected from the ALD process. C_{min} = 57 nF/cm^2 corresponding to t_{ZnO} = 154 nm, which is lower than the target thickness, but on the same order as the ZnO deposited for the Al_2O_3/ZnO investigation via the same process. It is not unusual to see thicknesses deviate from the target as variables including laser window coating and laser intensity degradation change from run to run and even over the course of a long run, such as needed to deposit over 150 nm of ZnO. A clockwise hysteresis voltage of 0.1 V is observed in both the C-V and G-V curves. A pronounced peak, G_p = 431 mS/cm^2 in the reverse direction and 429 ms/cm^2 in the forward direction, occurs between accumulation and depletion in the G_P curves,

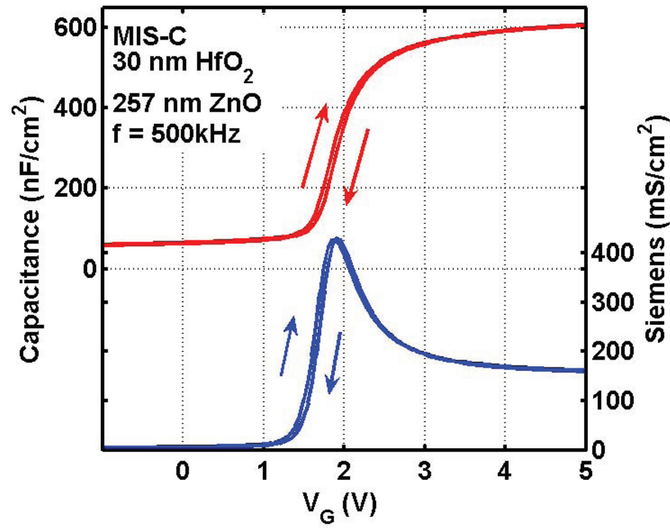


Figure 3.16: C-V and G-V of Pt - HfO_2 - ZnO capacitor

which has been closely tied to the presence of interface trapped charge [63]. V_{FB} in the reverse direction is 1.95 V, which is 0.75 V greater than the ideal case indicating oxide fixed charge may be present in the system. This issue is further investigated in Chapter VI.

The I-V leakage characteristics of the isolated Pt - HfO_2 - ZnO capacitors can be seen in Figure 3.17. The MIS-C has a 20 V range where leakage current is less

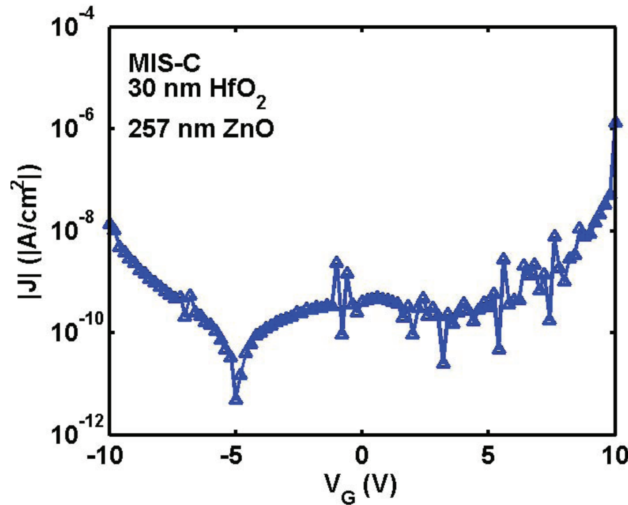
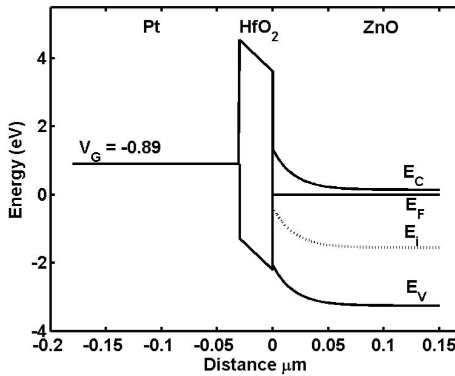


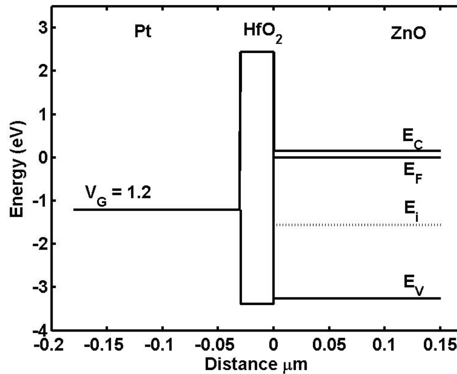
Figure 3.17: I-V leakage characteristics of Pt - BST - ZnO capacitors

than 10^{-8} A/cm^2 and a 10 V range where leakage current is less than 10^{-9} A/cm^2.

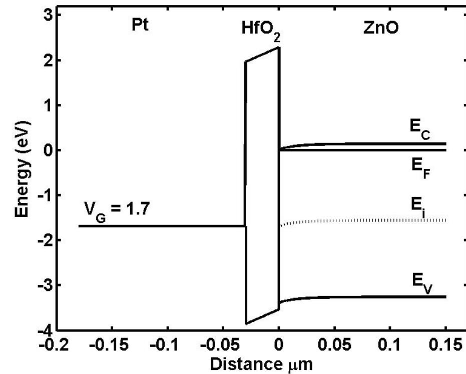
The leakage profile is symmetrical about $V_G = 0$ V with a rise in current observed at $V_G = \pm 10$ V. From these values we can calculate that the breakdown field for these devices is greater than 3.3x10^6 V/cm. As with Al_2O_3, one can expect the band offsets for HfO_2/ZnO to be much larger in value than those for PZT and BST on ZnO. This is indeed the case as the energy band diagram for the Pt - HfO_2 - ZnO material system can be seen in Figure 3.18. The work function of HfO_2 is 2.0 eV and



(a)



(b)



(c)

Figure 3.18: Energy band diagrams for an ideal Pt - HfO_2 - ZnO capacitor. (a) Depletion. (b) Flatband. (c) Accumulation.

the resulting conduction band discontinuity between HfO_2 and ZnO is 2.45 eV over 2 times greater than those for PZT and BST dielectrics, but 0.65 eV less than that of Al_2O_3. From the leakage data, it is clear that the conduction band discontinuity of HfO_2/ZnO is sufficient for superior low-leakage performance.

Frequency dependent C-V curves were measured on the Pt - HfO_2 - ZnO from 10 kHz to 500 kHz and can be seen in Figure 3.19. At 500 kHz a small dispersion

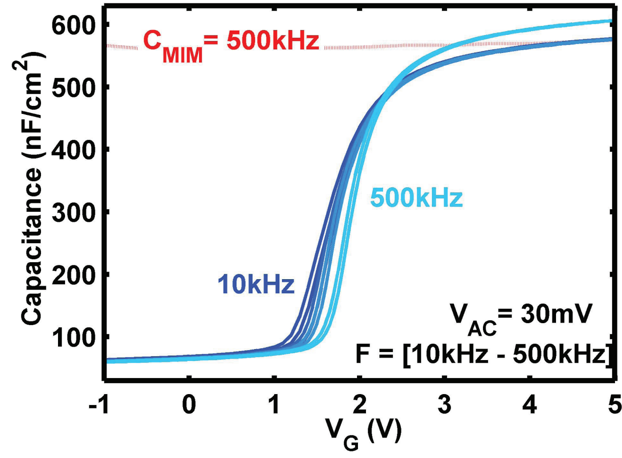


Figure 3.19: C-V of Pt - HfO_2 - ZnO capacitor at frequencies from 10 kHz to 500 kHz

is observed in the C-V curves in the accumulation region. In the depletion region, between 1 and 1.7 volts, a small frequency dispersion can also be seen, which has been shown to be indicative of interface trapped charge [3]. No signs of significant frequency dispersion or leakage properties are observed unlike the case with the BST/ZnO capacitor.

In summary, Pt - HfO_2 - ZnO capacitors have superior performance when compared against capacitors with PZT, BST, or Al_2O_3. HfO_2/ZnO has superior leakage performance allowing thinner films to be used as the gate dielectric. Thinner films used and a high dielectric constant allow these devices to achieve C_{OX} values as high (and higher) than those of the Perovskite oxides, which have κ_{ox} values over 20 times larger. With a dielectric constant twice that of Al_2O_3, equal (or better) leakage characteristics, and three times less hysteresis voltage values, HfO_2 is a clear front runner for high-k integration into ZnO devices. The frequency response is also well controlled.

Three drawbacks observed in each of the Pt - high-k - ZnO capacitors are hysteresis voltage, non-ideal V_{FB}, and various signs of interface trapped charge. Moving forward

we will investigate these drawbacks using our best performing material system (Pt - HfO_2 - ZnO) capacitors as the research vehicle.

3.8 C-V hysteresis

We observe a clockwise hysteresis in our MIS capacitors. Focusing on Pt - HfO_2 - ZnO devices, a 0.1 V hysteresis is observed, which corresponds to a charge of 4.1x10^{11} cm^{-2} via equation 3.4.

$$N_{it} = [V_G (C_{1\leftarrow}) - V_G (C_{1\rightarrow})] \left[\frac{\mathrm{C}_{ox}}{\mathrm{q}}\right] \tag{3.4}$$

Possible sources of C-V hysteresis include mobile ions in the insulator or interface trapped charge [64]. Further investigation yields trends in the magnitude of hysteresis with respect to applied bias, insulator thickness, and temperature, which leads to clues about the source of the hysteresis charge. The first clue is directionality; A commonly known source of hysteresis charge is insulator mobile ionic charge where, under bias, ions drift in the oxide according to the carrier type and bias polarity. This movement of charge in the insulator as a result of the applied measurement bias results in a C-V shift. Mobile charge is most often associated with positive charges which result in a counter-clockwise hysteresis direction. Because our hysteresis is in the clockwise direction, we do not suspect mobile ionic charge to be a contributor to our hysteresis charge. One theory explaining clockwise hysteresis in ZnO high-k dielectrics is that some of the accumulated electrons are transferred into unoccupied surface states during the upswing of V_G , and when V_G is swept down these states remain filled until the trapped electrons are thermally de-trapped [64]. Figure 3.20 shows the hysteresis of an MIS-C with 30 nm of HfO_2, showing the hysteresis increases with V_{max}. For data in this section $V_{min} = -4$ V. From this trend we hypothesize that at higher V_{max} values (i.e. more accumulated electrons, higher energy) more electrons

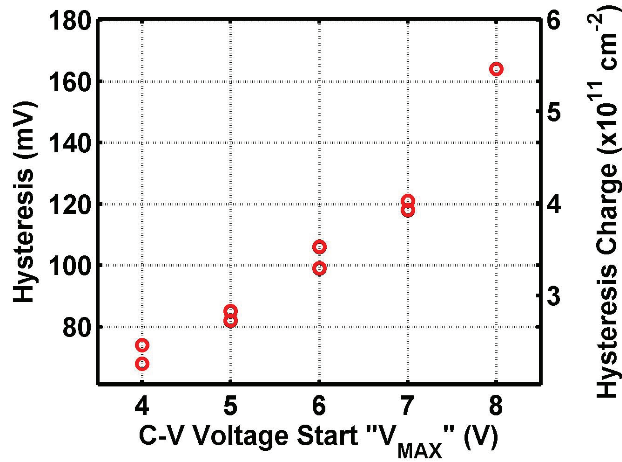


Figure 3.20: Hysteresis Voltage (left axis) and Charge magnitude (right axis) with respect to V_{max} of an MIS-C with 30 nm of HfO_2

are being trapped near the interface resulting in a higher hysteresis. In Figure 3.20 there are two data points for each V_{max} value. The experiment was run by measuring consecutive C-V curves from V_{max} = +4 V to +7 V and then measuring consecutive C-V curves from V_{max} = +4 V to +8 V. The higher data point at each V_{max} point is the second curve after a V_{max} = +7 V had been applied to the MIS-C. It is important to note that the hysteresis voltage and charge correlate with the V_{max} applied with no memory effects indicating the source of the hysteresis charge de-traps in a matter of a few seconds not several tens of seconds (or we would see memory effects in the second V_{max} = +4 V data point). The slope describing the trend is 70 mV/V_{max}, which equates to 6x10^{10} $\mathrm{cm}^{-2}\mathrm{V}_{\mathrm{max}}^{-1}$.

We also observe a decreasing trend in hysteresis with increasing temperature. Figure 3.21 shows hysteresis of a 30 nm HfO_2/ZnO MIS-C dual-swept from +7 V to -4 V at temperatures from 300 K to 400 K. This result indicates that elevated temperatures are eliminating some of the charge mechanisms causing hysteresis. It has been seen in other material systems that anneals, often at 200$^{\mathrm{O}}$C, are used to eliminate defect states or introduce elements that passivate charges that are detrimental to

device operation. In this case, from 300 K to 400 K, the magnitude of hysteresis voltage and charge reduces with temperature with a slope of roughly -0.6 mV/K and$-2.5\text{x}10^{9}$ cm^{-2}/K respectively. An important element of future work, in regards

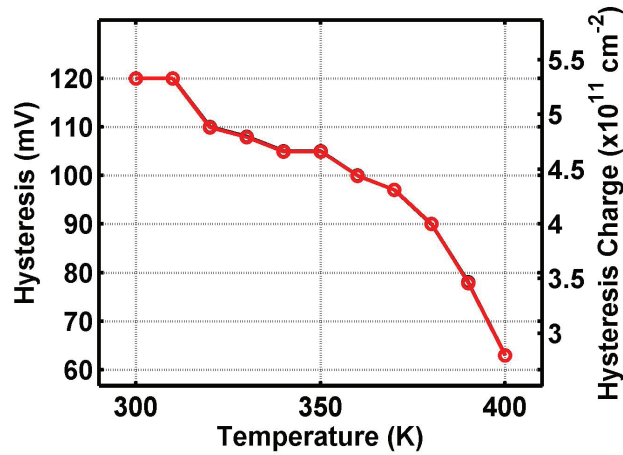


Figure 3.21: Hysteresis voltage (left axis) and charge magnitude (right axis) with respect to measurement temperature of an MIS-C with 30 nm of HfO_2

to temperature, is to characterize if temperature can be used to significantly and permanently reduce or eliminate hysteresis charge. In terms of identifying a source, knowing the source of hysteresis charge (or one of the sources) is highly temperature dependent is a clue to identification.

Finally, it can be seen that hysteresis voltage increases with insulator thickness. Figure 3.22 shows hysteresis values of MIS-Cs with 30 nm, 40 nm, and 60 nm of HfO_2 insulator at room temperature and swept from +7 V to -4 V. As these MIS-Cs were fabricated using the same process, from the thickness trend, it can be seen that the hysteresis voltage is scaling with the insulator capacitance with a slope approximately 3.2 mV/nm, but the associated charge remains constant. This result points not to charges in the insulator in general, but charges near or at the interface. From these results we can say it is likely hysteresis charge has a source of charges at or near the semiconductor/insulator interface whose number can be reduced by

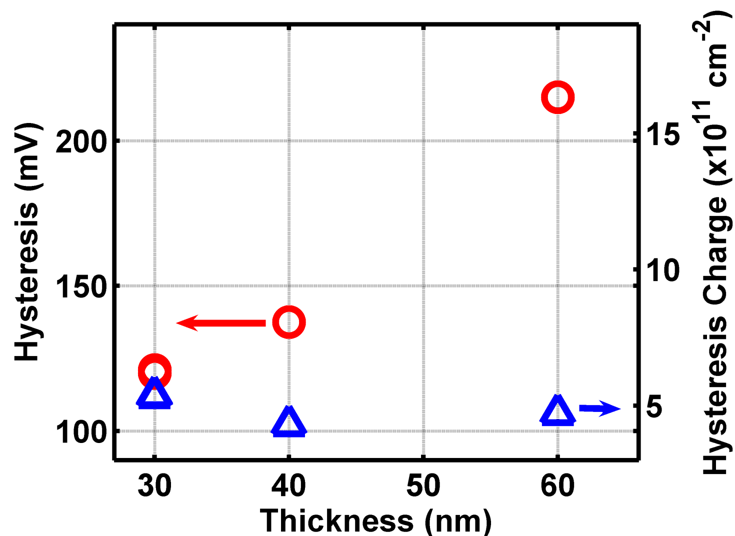


Figure 3.22: Hysteresis voltage (red) and charge magnitude (blue) with respect to insulator thickness of MIS-C devices with HfO_2 insulators

elevated temperatures. Bias-Temperature-Stress studies are performed in Chapter VI to learn more about the temperature and time characteristics of the charge and what process techniques may be available to eliminate this unwanted performance from our devices.

3.9 C-V translational instability

Another critical issue with MIS-C or TFT device performance can be termed translational instability (ΔV). In MIS-C devices a voltage of note is the flatband voltage (V_{FB}) and in TFTs a voltage of note is the threshold voltage (V_{TH}). Threshold voltage and threshold stability are a key components when selecting a material system for an application. Most applications require a very high level of threshold voltage stability, which means a low level of translational instability. One typical source of C-V transitional instability is fixed and trapped charge in the oxide. From analyzing the C-V curve's voltage instability under different experimental conditions (bias,

temperature, insulator thickness), we can learn about the characteristics, methods to reduce, and sources of the instability. The charge associated with a translational shift can be calculated via the equation 3.5.

$$N_{shift} = \left[V_{G2}\left(C_1\right) - V_{G1}\left(C_1\right)\right]\left[\frac{C_{OX}}{q}\right] \tag{3.5}$$

Figure 3.23 shows C-V translational stability with respect to applied V_{max} using

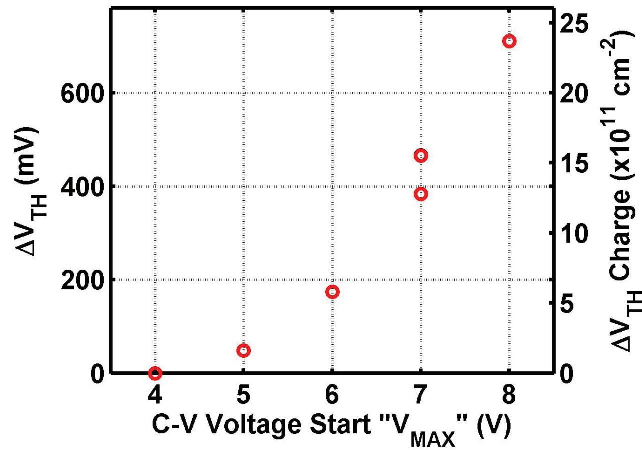


Figure 3.23: Translational shift voltage (left axis) and charge magnitude (right axis) with respect to V_{max} of an MIS-C with 30 nm of HfO_2

the C-V(V_{max} = +4 V) curve as the control to plot the C-V shift and associated charge. We see a shift over V_{max} = [4 V− 8 V] with a slope of 170 mV/V_{max} or 6x10^{11} cm^{-2} V_{max}. Because we see a shift at room temperature with very short times of applied bias (5 seconds) proportional to V_{max}, this indicates that there are pre-existing trap charges in the system, distributed in energy, above the band gap. As with the hysteresis study, after $V_{max} = 7$ V condition, we measured the $V_{max} = 4$ V condition again. The translational shift was not recovered as the $V_{max} = 4$ V condition took on the properties of the $V_{max} = 7$ V bias point. This non-recovery characteristic indicates that traps responsible for translational instability hold their charge for, at least, minutes. A possible source could be charge injected into the oxide

very close to the interface, very slow interface traps, or traps in the semiconductor. The recovery differences between the translational instability and hysteresis charge indicate two different sources of charge at acting on the MIS-C device.

C-V shift characteristics measured from a reference C-V at 300 K with a $V_{max} = 7$ V at temperatures from 300 K to 400 K can be seen in Figure 3.24 we see a positive C-V shift from 300 K to 360 K and then a reverse of the direction and at 400 K the shift is slightly negative.

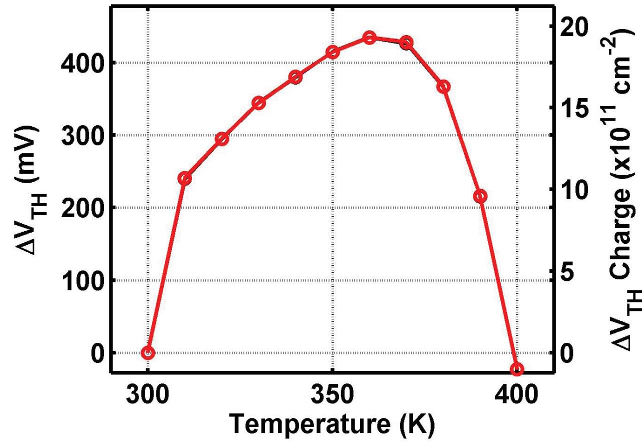


Figure 3.24: Translational shift voltage (left axis) and charge magnitude (right axis) with respect to measurement temperature of an MIS-C with 30nm of HfO_2

From this result, we may assume two mechanisms in play causing the C-V shift characteristics with temperature. First, at lower elevated temperatures, it seems the extra energy given to the carriers may cause them to find traps more efficiently (per V_{max}) and then become trapped. At temperatures above 360K, there seems to be a mechanism eliminating trapped states. At 400K we actually see a negative C-V translation, which, if trap elimination is occurring, makes sense because (from Figure 3.23) we know that a C-V(V_{max}= + 7 V) curve has populated traps compared with lower V_{max} curves.

The magnitude of the C-V(V_{max}= + 7 V) shift across different thickness of HfO_2

can be seen in Figure 3.25. Evaluating the translational shift across different film

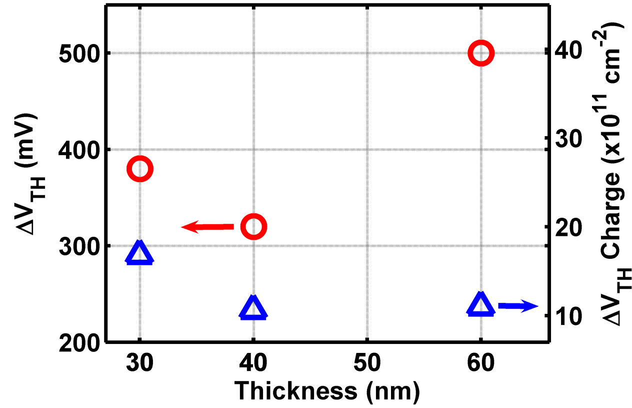


Figure 3.25: Translational shift voltage (red) and charge magnitude (blue) with respect to insulator thickness of MIS-C devices with HfO_2 insulators

thicknesses, we see a possible trend with thickness with a possible slope of 4 mV/nm (ignoring the 40 nm data point), but not in the charge associated with the shift. Again, this indicates the charges is independent of insulator thickness, and likely located at the insulator-ZnO interface or, perhaps, in the ZnO itself, but not in the insulator. Aside from the non-recoverability issue, the magnitude of the charge associated with translational instability is 2 – 3 times larger than that calculated for hysteresis. Both of these pieces of information, coupled with the various trends studied, will help us further understand and identify the sources of the charges responsible for various non-idealities in the HfO_2-ZnO system.

3.10 Summary

In this section four types of high-k dielectrics have been integrated with ZnO and their performance evaluated. HfO_2 has emerged as the best candidate for realizing high-performance ZnO/high-k devices. In addition, due to the C-V hysteresis and translational shift data, it can be seen that more investigation is needed to understand these various C-V non-idealities. As a first step, we will use several techniques to

probe interface trap density, linked to hysteresis, in Chapter V and temperature and bias trends, well suited for characterizing translational instabilities, in Chapter VI.

CHAPTER IV

ZnO Thin Film Transistors with High-k dielectrics

ZnO thin-film transistors (TFTs) have become the topic of much research in the recent past. Effective channel mobilities, on/off ratios, and I_{off} of ZnO transparent TFTs grown at low temperatures have been reported in the 0.2 – 3 $cm^2V^{-1}s^{-1}$ range, 10^7 [26], and 4 pA [50] respectively. One drawback to many of the ZnO TFTs reported is large threshold and operating voltages in comparison to a:Si TFTs in the range of 10 - 20 V [9, 50, 67, 4]. To reduce the operating voltage of a transistor one must increase the coupling of the gate electric field to the channel layer. This is often done by reducing the gate dielectric thickness or using gate dielectric material with a higher relative permittivity (high-k gate dielectric) as described in previous Chapters. Reports of ZnO TFTs with alternative dielectrics show mixed results; a 220 nm superlattice of Al_2O_3 ($\kappa_{ox} \approx 9$) and TiO_2 ($\kappa_{ox} > 40$) resulted in threshold voltages between 10 and 20 V [67], but 200 nm of a developed $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ dielectric ($\kappa_{ox} > 50$) resulted in a threshold voltage of 2 V and subthreshold slope of 0.25 V/dec [37].

In this Chapter, ZnO TFTs with various oxide high-k dielectrics are presented. Gate dielectrics reported include Si_3N_4($\kappa_{ox} \approx 7$), which is used as a low-k comparison device, BST, PZT, Al_2O_3, and HfO_2 each deposited as described in Chapter II.

4.1 Fabrication

All TFTs were made using the following steps:

1. Gate dielectric deposition: The gate dielectrics were all deposited on Pt / TiO_2 / SiO_2 / Si substrates purchased from Radient Technologies. The top Pt layer served as the gate metal anNorris2003d gate contact, on which the gate dielectrics were directly deposited as described in Chapter II.

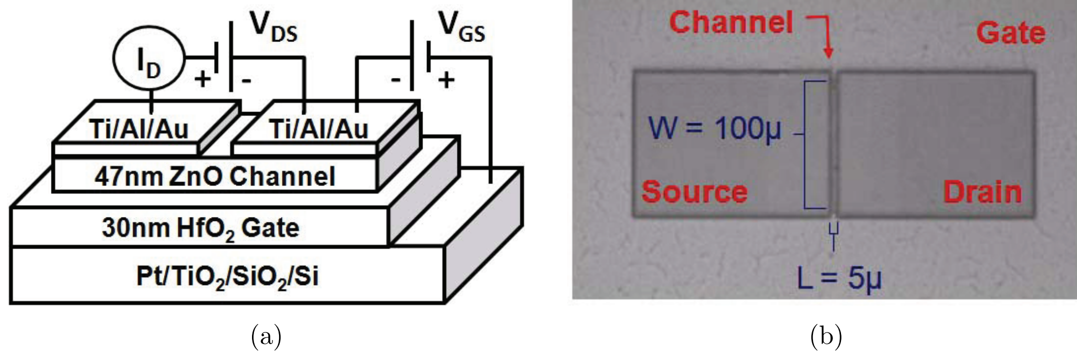
2. ZnO deposition: The ZnO was then deposited as described in Chapter II.

3. Source drain deposition: The source and drain contacts were patterned using conventional photolithography lift-off techniques. Ohmic contacts of Ti (200 Å) / Al (1000 Å) / Au (2000 Å) was E-beam evaporated using the Enerjet E-beam evaporator located in the Lurie Nanofabrication Facility at the University of Michigan. The contacts were 100 μm wide (W = 100 μm) by 150 μm long and 5 μm apart ($L = 5\mu$m) resulting in a transistor gate width/length ratio of $W/L = 20$.

4. ZnO isolation: Then a photoresist pattern, protecting the ZnO in device active regions was used during the ZnO isolation etch, which was carried out with a Buffered Hydrofloric Acid wet-etch.

5. Gate via etching: Finally, a photoresist pattern protecting all TFTs was used during the gate via etch in order to clear some part of the samples of gate dielectric so electrical connection could be made to the gate. The specific etch varied by material and can be found in Chapter II.

A schematic representation and optical microscope image of one TFT can be seen in Figure 4.1(a)



(a) (b)

Figure 4.1: Single ZnO thin film transistor. (a) Typical TFT Structure. ZnO thickness varies with sample. Gate dielectric material and thickness vary with sample. (b) Optical microscope picture of TFT. In this sample the dielectric layer is coincident with the ZnO layer, hence not visible.

4.2 Testing and parameter extraction

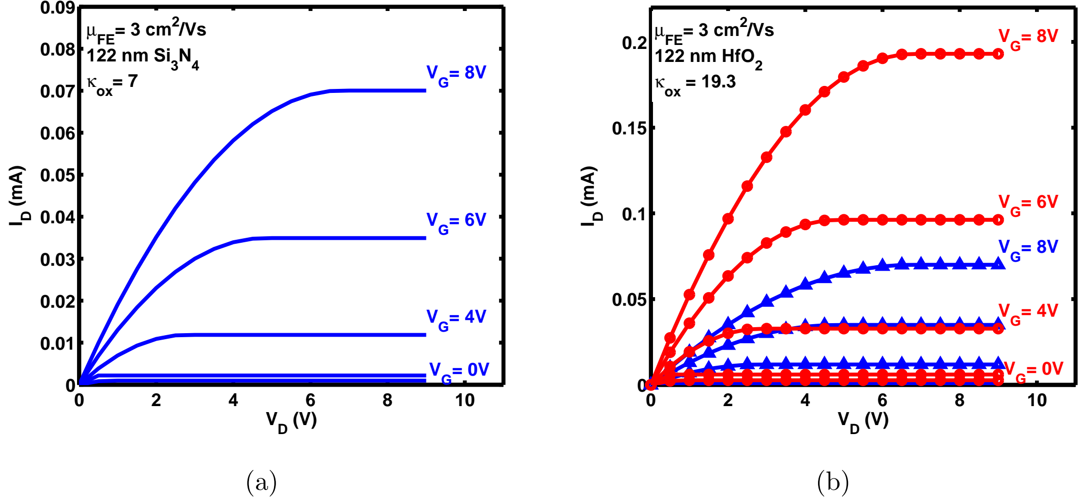
All TFTs were tested using a Keithley 4200 Semiconductor Characterization System attached to an Alessi Probe Station with a dark box. Each TFT was electrically connected as shown in Figure 4.1(a). Output curves (I_D vs V_{DS}) and transfer curves (I_D vs V_{GS}) were measured and the following performance metrics were extracted from the transfer curves as explained below: off-current (I_{off}), on-off current ratio (I_{on}/I_{off}), field effect mobility (μ_{FE}), threshold voltage (V_{TH}), and subthreshold slope (S).

On first order approximation, the ZnO TFT devices operation presented in this work can be modeled by equations developed for Silicon long channel devices using the gradual channel and depletion region approximations [53]. The output curves can be modeled by Equation 4.1

$$\begin{aligned} I_D &= \mu_n C_{ox} \tfrac{W}{L} \left[\left(V_G - V_{TH} - \tfrac{1}{2} V_D \right) V_D \right] \quad && V_D < (V_G - V_{TH}) \\ I_D^{sat} &= \mu_n C_{ox} \tfrac{W}{2L} \left(V_G - V_{TH} \right)^2 && V_D > (V_G - V_{TH}) \end{aligned} \tag{4.1}$$

where I_D is the drain current. A modeled output plot for a device with low-k dielectric and a device with high-k dielectric (with different influences on I_D via C_{ox} can be

seen in Figure 4.2.



(a)

(b)

Figure 4.2: Ideal output characteristics of a TFT. (a) TFT with low-k dielectric. (b) TFT with high-k dielectric ('o') and TFT with low-k dielectric ('Δ') from Fig a for comparison.

It is easy to see, with a high-k material, higher drive current values can be achieved with the same bias conditions as a low-k material. For example, the ratio of dielectric constants in Figure 4.2 is 2.8. For the TFT with the high-k dielectric I_D^{sat} at $V_G = 8$ is 193 μA, which is 2.8 times higher than the $I_D^{sat} = 70\mu$A at $V_G = 8$ for the TFT with the low-k dielectric. The concept of operating voltage can also be seen in Figure 4.2(b). If an application has a need to operate at $I_D = 30$ μA, we can see that the high-k TFT can achieve this result with $V_G = 4$ V and $V_D = 3$ V, but the low-k TFT requires $V_G = 6$ V and $V_D = 4$ V and, hence, has a higher operating voltage for that given application.

The transfer curves can also be modeled, on first order approximation using Equations 4.1 for $V_G > V_{TH}$. The range where $V_G < V_{TH}$ is called the subthreshold region and I_D can be approximated by the following equation [73]

$$I_D = I_{D1} exp\left(\frac{q(V_G - V_{TH})}{nkT}\right)\left(1 - exp\left(\frac{-qV_D}{kT}\right)\right) \tag{4.2}$$

where I_{D1} is a fitting parameter based on I_D at $V_G = V_{TH}$ and ${}^{kT}/_{q} = 26$ mV is the Thermal Voltage. The relation for subthreshold current will be explained further in this Chapter and Chapter V. Ideal curves for transfer operation can be seen in Figure 4.3.

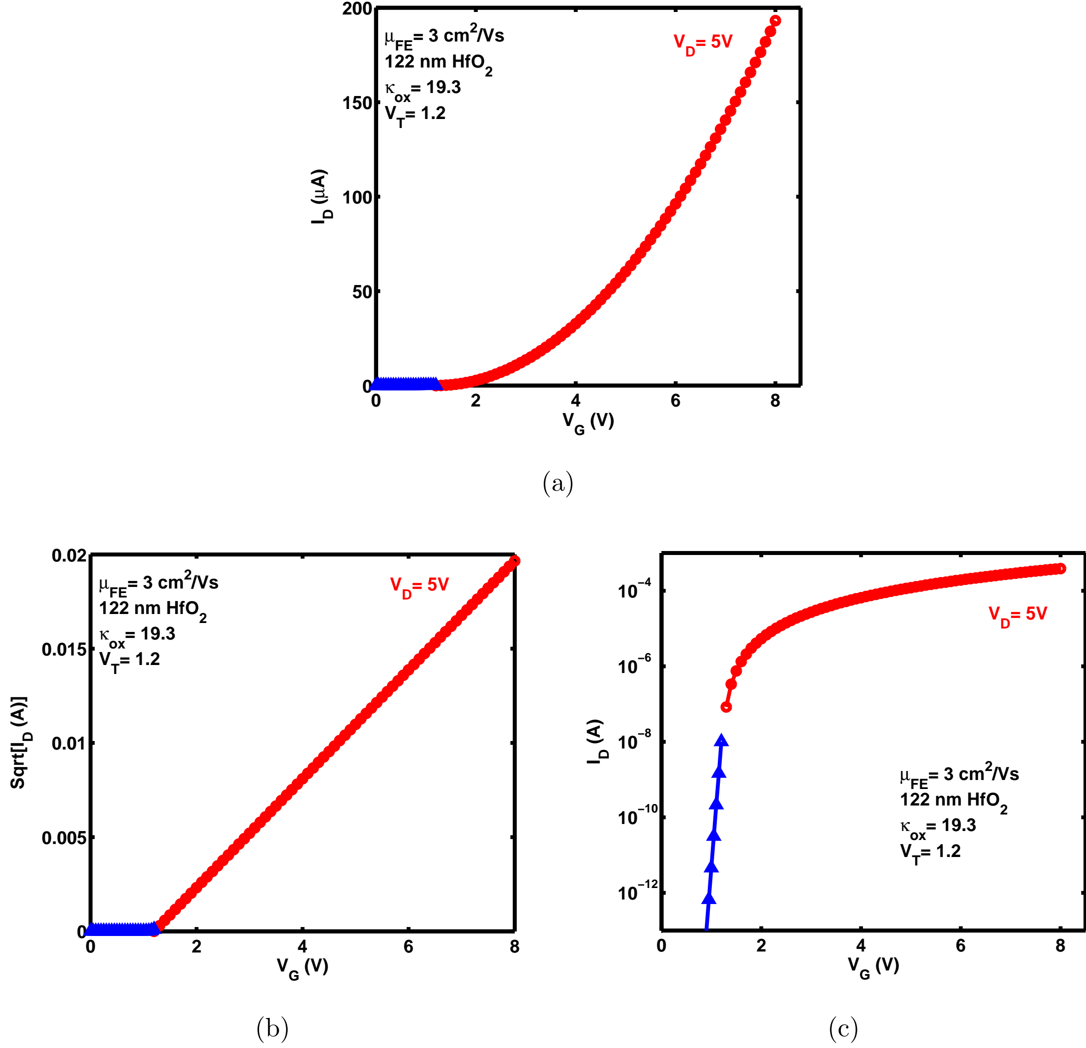


Figure 4.3: Ideal transfer curve operation. $V_G > V_T$: Equation 4.1 (red circles). $V_G < V_T$: Equation 4.2 (blue triangles). (a) Linear scale. (b) $\sqrt{I_D}$ vs V_G. Used for extracting TFT μ_{FE} and V_T. (c) Logarithmic plot. Used for evaluating subthreshold slope, off-current, and on-off current ratio.

4.2.1 Mobility extraction

In the case of polycrystalline ZnO TFTs, the most widely used method for reporting mobility is via the field-effect (or saturation) mobility (μ_{FE}), which is extracted from the slope of the linear region of the $\sqrt{I_D}$ vs V_{GS} plot shown in Figure 4.3(b). This method assumes ZnO TFTs follow the relationship developed for drain current in the saturation region (I_D^{Sat}) of a long channel MOSFET [53].

$$\begin{gathered} I_D^{Sat} = \mu_{FE} C_{ox} \frac{W}{2L} \left(V_{GS} - V_{TH}\right)^2 \\ \mu_{FE} = \left[\frac{\delta\left(\sqrt{I_D^{Sat}}\right)}{\delta V_G}\right]^2 \frac{2L}{W} \frac{t_{ox}}{\kappa_{ox}\epsilon_0} \end{gathered} \tag{4.3}$$

$\frac{\delta\left(\sqrt{I_D^{Sat}}\right)}{\delta V_G}$ is simply the slope of the curve in Figure 4.3(b). It should be noted that mobility is a property of the semiconductor and should be expected to be relatively stable across devices with the same semiconductor deposition process, however, reports have shown mobility to be influenced by interface charge density located, in energy, near the band-edge of polycrystalline-Silicon TFTs [12], which in turn can be influenced by process conditions and choice of gate dielectric. A practical example of fitting the slope of the $\sqrt{I_D}$ vs V_{GS} curve can be seen in Figure 4.4(b).

4.2.2 Threshold voltage extraction

The two extraction methods most commonly used for reporting the threshold voltage (V_{TH}) of ZnO TFTs are based on the MOSFET long channel approximation relation [53] The first method extracts V_{TH} from the transfer curve of a TFT in the linear region of operation (small V_{DS}). In this case Equation 4.1 reduces to

$$I_D = \mu_{FE} C_{OX} \frac{W}{L} \left[\left(V_{GS} - V_{TH}\right) V_{DS}\right] \tag{4.4}$$

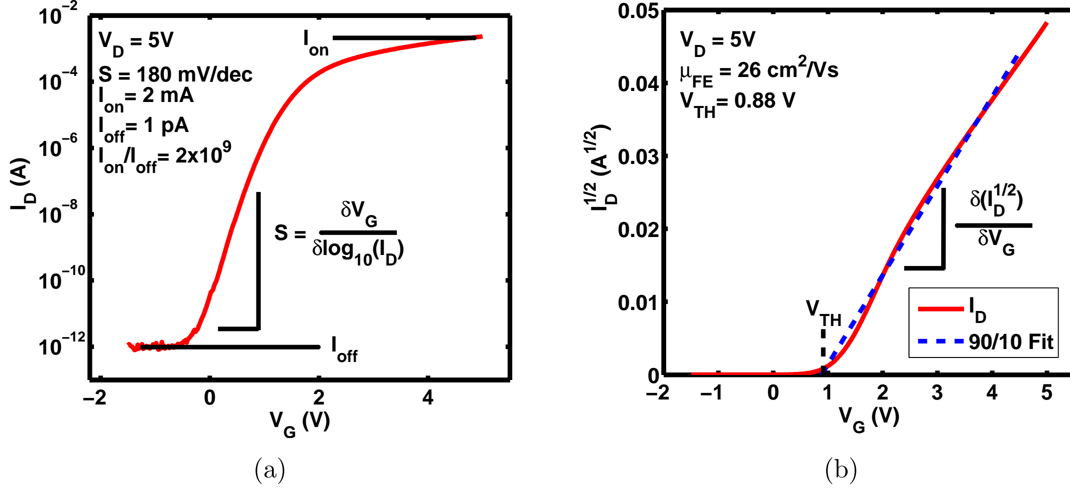


Figure 4.4: Practical example of TFT figure of merit extraction. (a) $\log_{10}(I_D)$ vs V_G plot of a ZnO TFT. (b) $\sqrt{I_D}$ vs V_G plot of a ZnO TFT.

and V_{TH} can be extracted from the x-intercept of a best fit to the on-state data of the I_D vs V_{GS} curve.

The second method extracts V_{TH} from the transfer curve of a TFT in the saturation region of operation ($V_{DS} > V_{DS}^{Sat} = V_{GS} - V_{TH}$) where Equation 4.1 takes on the form expressed in I_D^{sat} where V_{TH} now becomes the x-intercept of the fit to the on-state data of the $\sqrt{I_D}$ vs V_{GS} curve. For the ideal data in Figure 4.3(b), fitting I_D above $V_G = V_{TH}$ results in a line whose x-intercept is $V_G = 1.2$ V $= V_{TH}$. A practical example of extracting V_{TH} from the $\sqrt{I_D}$ vs V_{GS} curve can be seen in Figure 4.4(b).

It will be shown that, well behaved ZnO TFTs do exhibit behavior near-enough to MOSFET behavior so that $V_{TH}^{lin} \approx V_{TH}^{Sat}$ with good fits throughout most of the on-state data.

4.2.3 Subthreshold slope extraction

Subthreshold Slope (S) (technically the 'inverse subthreshold slope') is a performance metric used to characterize how efficiently a device transitions from the off-state to the on-state and is defined as the inverse of the slope of $log_{10}(I_D)$ vs V_{GS} (Equation 4.5) in the subthreshold region of operation of a transfer curve. The

subthreshold region of TFT operation is defined as $V_{GS} < V_{TH}$.

$$S = \left[\frac{\delta \log_{10}(I_D)}{\delta V_{GS}}\right]^{-1} \tag{4.5}$$

S can be seen as the inverse of the slope of the blue triangle data (calculated via Equation 4.2) in Figure 4.3(c) and is most often reported in mV/dec or V/dec. The lower S is, the more efficient the device in transitioning from off to on. For well behaved devices the subthreshold current maintains a value of S over many decades of I_D increase and the location to evaluate S is obvious. In many cases, S is not constant over a wide range of I_D so authors will report or show the specific range or point where S was determined. In this Chapter, the black line fitting a region of $\log_{10}(I_D)$ vs V_G serves this purpose. A practical example of the region where S is determined can be seen in Figure 4.4(a).

S has been found to also be a performance metric for the quality of the interface between semiconductor and gate dielectric. As a result S, is an extremely important figure of merit in this work. It will be shown in Chapter V that S can be used to estimate interface charge density, a key source of charge in TFTs that contributes to subthreshold slope in-efficiency.

4.2.4 Current magnitude related performance metric extraction

I_{off} (sometimes called I_{min}) is defined as the current of the TFT in the off-state. In cases where the off-state current is not flat, the minimum current is defined as the lowest current before turn-on. I_{off} can most easily be seen in $\log_{10}(I_D)$ vs V_{GS} plots such as shown in Figure 4.4(a). I_{on} (sometimes called Drive Current) is the maximum current in a transfer plot. Often to compare different devices, I_{on} will be measured at a specific V_G. I_{on}/I_{off} is defined as the Drive Current divided by the off current of a transfer curve for a given V_{DS}.

4.3 ZnO TFTs with Si_3N_4 dielectrics

ZnO TFTs with 122 nm of Si_3N_4 (κ_{ox} = 7, EOT = 68 nm) as the gate dielectric were fabricated and tested as a control TFT sample with a low-k dielectric. The output characteristics can be seen in Figure 4.5. This view of TFT performance is advantageous for understanding how the TFTs transition from linear to saturation regions and how flat I_D is in the saturation region. For Si_3N_4 it can be seen that at V_{GS} = 20 V, I_D = 260 μA and the device saturates near V_{DS} = 30 V. So, it can be said that for a device that needs to reach I_D = 260 μA, the region of operation is 30 V and the devices saturate well. As the all the performance metrics of interest are computed from the transfer curve, further analysis of the output curves is outside the scope of interest.

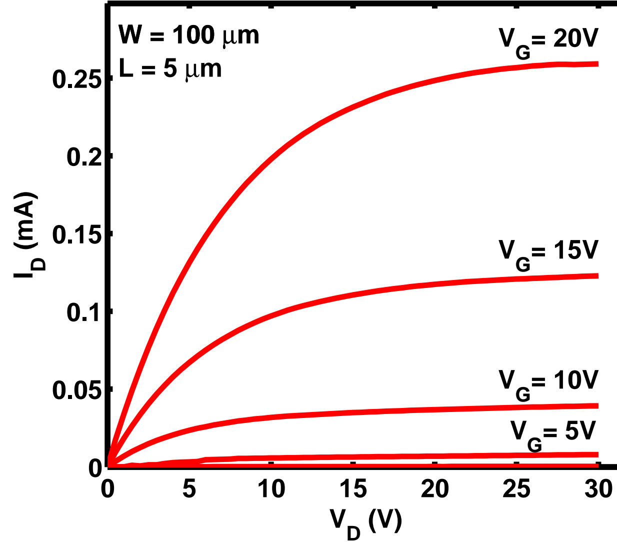
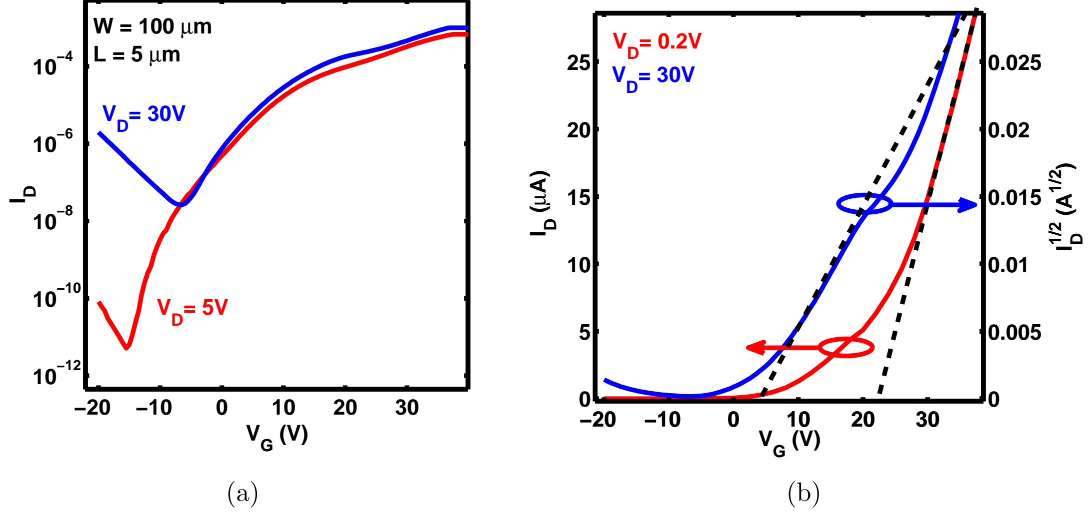


Figure 4.5: Output characteristics of ZnO TFT with Si_3N_4 gate dielectric

The transfer curves of a ZnO TFT with Si_3N_4 gate dielectric with t_{ox} = 122 nm and κ_{ox} = 6.6 can be seen in Figure 4.6. $\frac{\delta\left(\sqrt{I_D^{Sat}}\right)}{\delta V_G}$ = 1.15x10^{-3} $A^{1/2}V^{-1}$, which results in μ_{FE} = 2.74 $cm^2V^{-1}sec^{-1}$. S was measured at two different values of V_D with S = 1.5 V/dec for the V_{DS} = 1 V transfer curve and S = 2 V/dec for the V_{DS} = 5 V transfer curve. For V_{DS} = 1V, I_{off} = 1.3 pA. For V_{DS} = 5V, I_{on}/I_{off} = 1.3x10^8.



(a) (b)

Figure 4.6: Typical transfer curve characteristics for a ZnO TFT with SiN_X gate dielectric. (a) Semi-logarithmic plot of transfer curve. S ,I_{off} , and I_{on}/I_{off} can be extracted from this view. (b) I_D vs V_G of TFT in linear region (low V_{DS}) can be used to extract V_T (red). $\sqrt{I_D}$ vs V_G of TFT in saturation region can be used to extract V_T and μ_{FE} (blue).

Parameter	Unit	Region	Value
μ_{FE}	$cm^2V^{-1}s^{-1}$	$V_{DS} = 5V$	2.74
V_{TH}	V	$V_{DS} = 0.2V$	22
		$V_{DS} = 30V$	5
S	mV/dec	$V_{DS} = 1V$	1,500
		$V_{DS} = 5V$	2,000
I_{off}	pA	$V_{DS} = 1V$	1.3
I_{on}/I_{off}		$V_{DS} = 5V$	$1.3\text{x}10^8$

Table 4.1: Electrical Properties of ZnO TFT with 122nm SiN_X gate dielectric

Table 4.1 shows the performance results for a typical ZnO TFT with 122 nm of Si_3N_4. As expected, μ_{FE} is higher than typical a-Si TFTs and I_{on}/I_{off} is above the level needed for AMLCD applications. S is high compared to $S = 0.3$V/dec reported for a-Si TFTs [34] and V_{TH} is also high compared to V_{TH} values below 5V for a-Si TFTS developed for AMLCD applications [34], but typical for reported ZnO TFTs fabricated with low-k dielectrics. In addition, the V_{TH} instability issue renders these devices undesirable for use in most TFT applications.

4.4 ZnO TFTs with BST dielectrics

ZnO TFTs with 740 nm of Barium Strontium Titanate, $(Ba,Sr)TiO_3$ ($\kappa_{ox} \approx 500$, EOT = 5.8 nm), were fabricated and tested. The output characteristics can be seen in Figure 4.7.

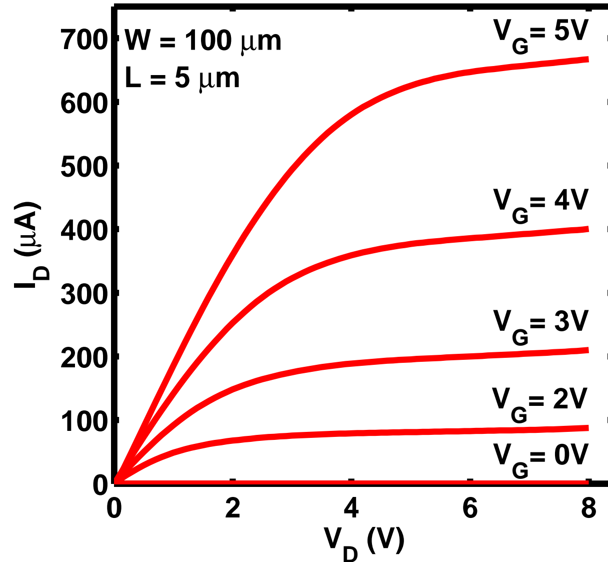
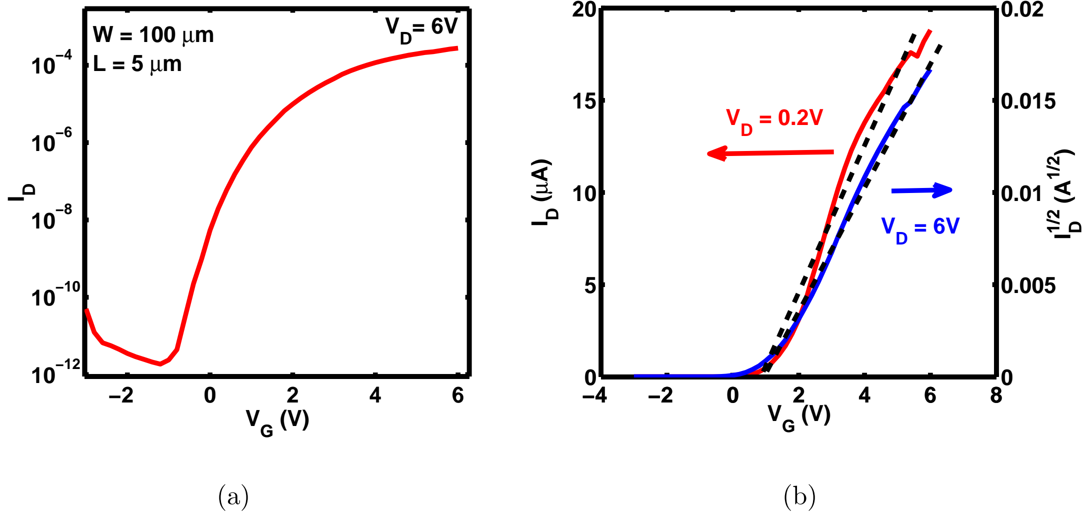


Figure 4.7: Output characteristics of ZnO TFT with 740 nm of BST gate dielectric

With an EOT that is 12% that of Si_3N_4, operation voltage region is expected to be decreased 88% compared with Si_3N_4. For $I_D \approx 300$ μA, V_G required for TFTs with BST is ~ 4 V, compared to ~ 20 V with Si_3N_4 and the operating voltage region

is ∼ 8 V compared to 30 - 40 V, both values show a reduction in voltage by about 80%. From the output curve, the influence of the high-k BST gate dielectric reducing operating voltage of a ZnO TFT is clear.

The transfer curve can be seen in Figure 4.8.



(a) (b)

Figure 4.8: Typical transfer curve characteristics for a ZnO TFT with 740 nm of BST gate dielectric. (a) Semi-logarithmic plot of transfer curve. S, I_{off}, and I_{on}/I_{off} can be extracted from this view. (b) I_D vs V_{GS} of TFT in linear region (red) and $\sqrt{I_D}$ vs V_{GS} in saturation region (blue).

The transfer curve operating voltage region has decreased from ∼40 V to ∼6 V as a result of the high-k BST, an 85% reduction compared to TFTs with conventional gate dielectrics, which is indicative of the EOT values of each material.

Extracted figures of merit can be seen in Table 4.2.

Parameter	Unit	Region	Value
μ_{FE}	$cm^2V^{-1}s^{-1}$	$V_{DS} = 1V$	2.27
V_{TH}	V	$V_{DS} = 0.2V$	1.2
		$V_{DS} = 6V$	1.2
S	mV/dec	$V_{DS} = 6V$	270
I_{off}	pA	$V_{DS} = 6V$	1.8
I_{on}/I_{off}		$V_{DS} = 6V$	$1.5x10^8$

Table 4.2: Electrical Properties of ZnO TFT with 740 nm BST gate dielectric

ZnO TFTs with BST as a high-k dielectric show improvement in most areas of performance. V_{TH} reduction from ∼25 V to ∼1.2 V (95%) is a direct result of the high dielectric constant of BST reducing the EOT. ZnO TFTs with BST exhibit more consistent V_{TH} values compared to TFTs with Si_3N_4 and PZT as evidenced by $V_{TH}^{lin} = V_{TH}^{Sat}$. S = 270 mV/dec, which is 86% less than TFTs with conventional gate dielectric. This result indicates these devices turn on much more efficiently than devices with conventional gate dielectrics. The relatively high μ_{FE}, low V_{TH}, low I_{off}, and $I_{on}/I_{off} > 10^7$ values show this TFT configuration is also a candidate for high-performance AMLCD applications. Two drawbacks to using BST in ZnO TFTs are the high temperature required for poly-crystalline deposition and BST's poor leakage performance.

4.5 ZnO TFTs with PZT dielectrics

ZnO TFTs with 900 nm of Lead Zirconate Titanate, (Pb,ZrO)TiO_3 (PZT) ($\kappa_{ox} \approx$ 640, EOT = 5.5 nm), were fabricated and tested. The output characteristics can be seen in Figure 4.9. With an EOT value reduction of 92% compared to Si_3N_4 we expect PZT to lower the operating voltage of ZnO devices to a similar fraction. For $I_D \approx 40\ \mu$A, V_G required for TFTs with PZT is $\sim$ 2 V compared to $\sim$ 10 V for Si_3N_4, an 80% reduction . The operating voltage region of Si_3N_4 is 30 - 40 V while PZT devices have $V_D \sim$ 1V, a 96% reduction from Si_3N_4 values. From the output curve, the influence of the high-k PZT gate dielectric reducing operating voltage of a ZnO TFT is clear.

The transfer curve can be seen in Figure 4.10.

The transfer curve operating voltage region has decreased from ∼40 V to ∼3 V as a result of the high-k PZT, which is a 92% decrease commensurate with the decrease in EOT. Extracted figures of merit can be seen in Table 4.3.

ZnO TFTs with PZT as a high-k dielectric show improvement in most areas of

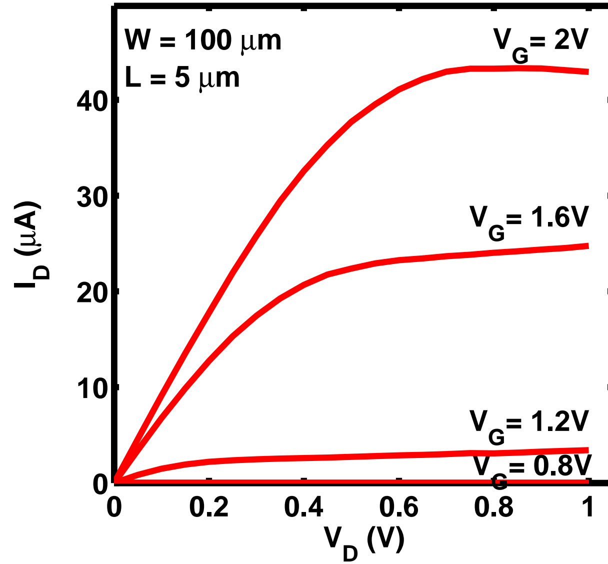
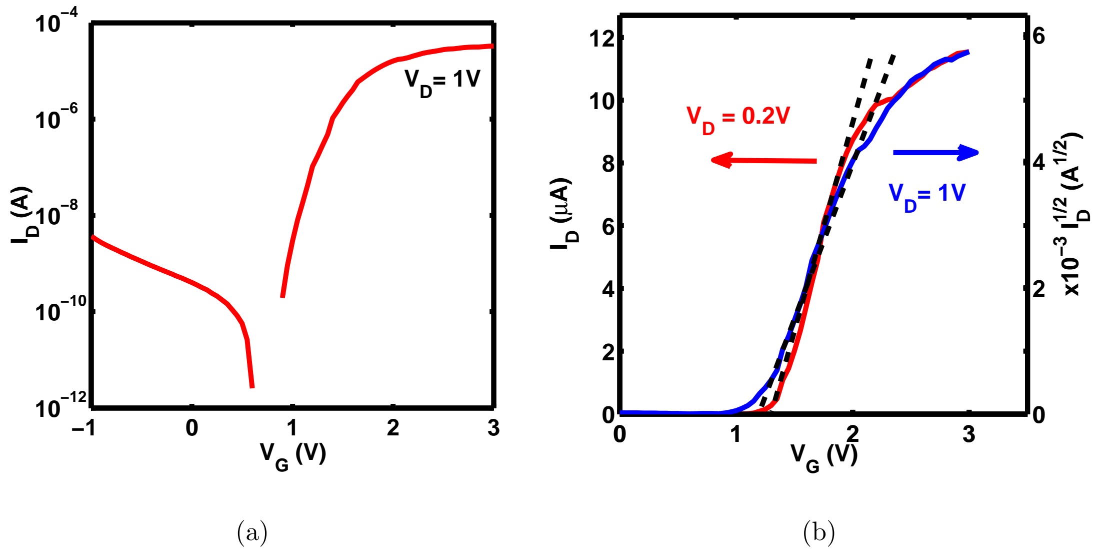


Figure 4.9: Output characteristics of ZnO TFT with 900 nm of PZT gate dielectric



(a)

(b)

Figure 4.10: Typical transfer curve characteristics for a ZnO TFT with 900 nm of PZT gate dielectric. (a) Semi-logarithmic plot of transfer curve. (b) I_D vs V_{GS} of TFT in linear region (red) and $\sqrt{I_D}$ vs V_{GS} in saturation region (blue).

Parameter	Unit	Region	Value
μ_{FE}	cm^2V^{-1}s^{-1}	$V_{DS} = 1V$	3.19
V_{TH}	V	$V_{DS} = 0.2V$	1.4
		$V_{DS} = 1V$	1.1
S	mV/dec	$V_{DS} = 1V$	100
I_{off}	pA	$V_{DS} = 1V$	2.5*
I_{on}/I_{off}		$V_{DS} = 1V$	1.3x10^7

Table 4.3: Electrical Properties of ZnO TFT with 900 nm PZT gate dielectric

performance. V_{TH} reduction from ∼25 V to ∼1.2 V (95% reduction) is a direct result of the high dielectric constant of PZT. This result combined with the relative consistency of V_{TH} ($V_{TH}^{Sat} = 1.1$ and $V_{TH}^{Lin} = 1.4$ V) proves the success of substituting a high-k gate dielectric into ZnO TFTs. Further, $S = 100$ mV/dec is 5% that of TFTs with conventional gate dielectric and almost 3 times less than that of BST. This result proves these devices turn on much more efficiently than devices with conventional gate dielectrics and suggests a semiconductor/dielectric interface with lower interface charge density than that of ZnO/BST. This low interface charge is likely a result of the PZT (an oxide dielectric) being readily integrated with ZnO (an oxide semiconductor) and a result of our process where we deposit our dielectric and semiconductor without breaking vacuum or performing any other process steps between depositions that could lead to interface quality degradation. When compared to BST, these advantages are not unique, so there must be another mechanism contributing to interface charge difference between PZT and BST.

Finally, it should be noted that this performance is remarkable for any TFT with such a thick gate dielectric, but issues with leakage current are significant and the high-temperatures needed to deposit poly-crystalline PZT preclude it from low-temperature applications.

4.6 ZnO TFTs with HfO_2 dielectrics

ZnO TFTs with 30 nm of Hafnium Oxide, (HfO_2) ($\kappa_{ox} \approx 20$, EOT = 6.1 nm), were fabricated and tested. The ZnO was deposited by pulsed laser deposition and the HfO_2 by plasma enhanced atomic layer deposition at AFRL-WP. The output characteristics can be seen in Figure 4.11. With an EOT 9% that of Si_3N_4 the

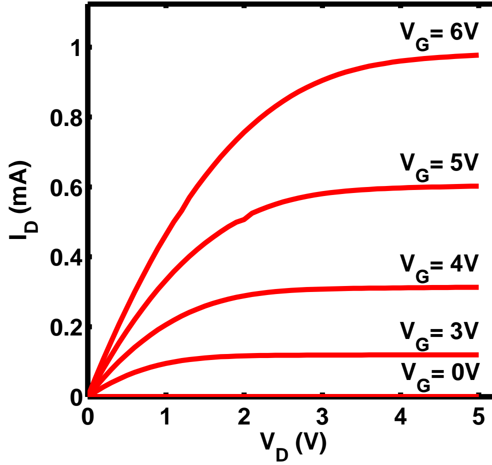


Figure 4.11: Output characteristics of ZnO TFT with 30 nm of HfO_2 gate dielectric

operating voltages are expected to be reduced by 91% for TFTs with HfO_2 compared to those with Si_3N_4. For $I_D \approx 300$ μA, V_G required for TFTs with HfO_2 is ~ 4 V, compared to ~ 20 V with Si_3N_4 and the operating voltage region is ~ 5 V compared to 30 - 40V so we see a reduction in operating voltages on the order of 86%. The transfer curve can be seen in Figure 4.12.

The transfer curve operating voltage region has decreased from ~40 V to ~6 V as a result of the high-k HfO_2 compared to TFTs with conventional gate dielectrics, an 85% reduction. Extracted figures of merit can be seen in Table 4.4.

ZnO TFTs with HfO_2 as a high-k dielectric show improvement in all areas of performance. V_{TH} reduction from ~25 V to ~2 V (92% reduction) is a direct result of the EOT of the HfO_2 dielectric. ZnO TFTs with HfO_2 show less V_{TH} uniformity

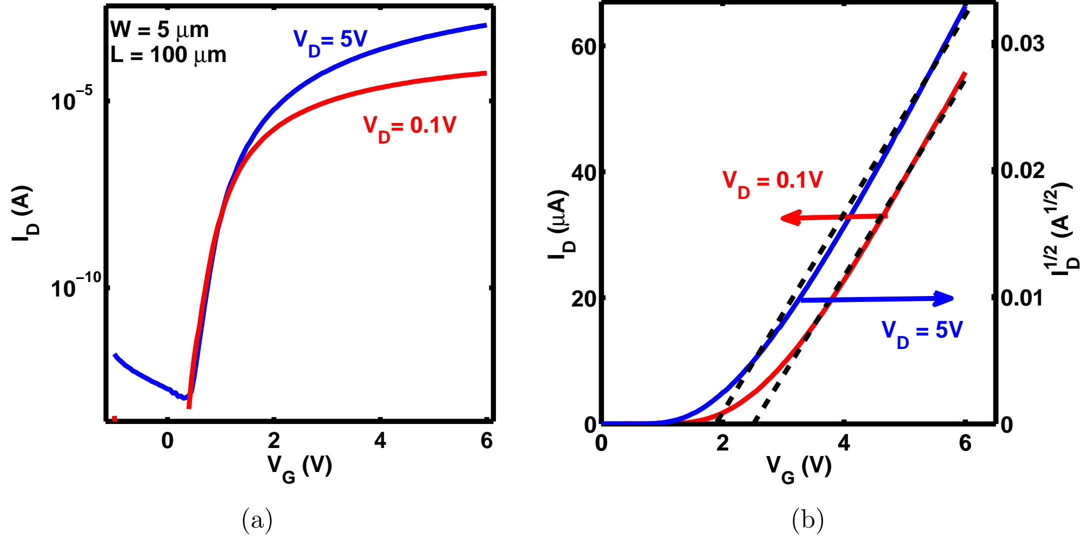


Figure 4.12: Typical transfer curve characteristics for a ZnO TFT with 30 nm of HfO_2 gate dielectric. (a) Semi-logarithmic plot of transfer curve. (b) I_D vs V_{GS} of TFT in linear region (red) and $\sqrt{I_D}$ vs V_{GS} in saturation region (blue).

Parameter	Unit	Region	Value
μ_{FE}	$cm^2V^{-1}s^{-1}$	$V_{DS} = 5V$	10.5
V_{TH}	V	$V_{DS} = 0.1V$	2.4
		$V_{DS} = 5V$	1.9
S	mV/dec	$V_{DS} = 0.1V$	105
		$V_{DS} = 5V$	105
I_{off}	pA	$V_{DS} = 5V$	0.1
I_{on}/I_{off}		$V_{DS} = 5V$	1.0x10^{10}

Table 4.4: Electrical Properties of ZnO TFT with 30 nm HfO_2 gate dielectric

from saturation region to linear region than BST, but is on the same order with PZT . S = 105 mV/dec is 95% less than TFTs with conventional gate dielectric and on par with that of PZT. It is important to consider that between the gate dielectric deposition, the sample was removed from the ALD system and exposed to clean room air for 2 days before the ZnO deposition, yet has similar S performance. This result indicates a relatively high quality semiconductor/dielectric interface is achievable with HfO_2 regardless of the interfacial surface of the dielectric being exposed to air. The high μ_{FE} can be attributed to the higher quality ZnO achieved by the PLD process developed by AFRL.

4.7 Summary

In this Chapter the successful integration of several high-k dielectrics into ZnO TFTs has been presented. The ultimate goal of reducing the operating voltage and threshold voltage of TFTs was realized. Each high-k material used achieved an EOT between 5 and 6 and the resulting V_{TH} compared to Si_3N_4 with an EOT of 68 can be seen in Figure 4.13

A summary table of key figures of merit can be seen in Table 4.5.

Parameter	Unit	Si_3N_4	BST	PZT	HfO_2
μ_{FE}	$cm^2V^{-1}s^{-1}$	2.74	2.27	3.19	10.5
EOT	nm	68	5.8	5.5	6.1
V_{TH}	V	22 5	1.2 1.2	1.4 1.1	2.4 1.9
S	mV/dec	1,500 2,000	270	100	105 105
I_{off}	pA	1.3	1.8	2.5*	0.1
I_{on}/I_{off}		$1.3x10^8$	$1.5x10^8$	$1.3x10^7$	$1.0x10^{10}$

Table 4.5: Figures of Merit for ZnO TFTs with high-k dielectrics

Subthreshold slope is an important figure of merit and as ZnO development continues to higher and higher mobilities, low values for S becomes increasingly important

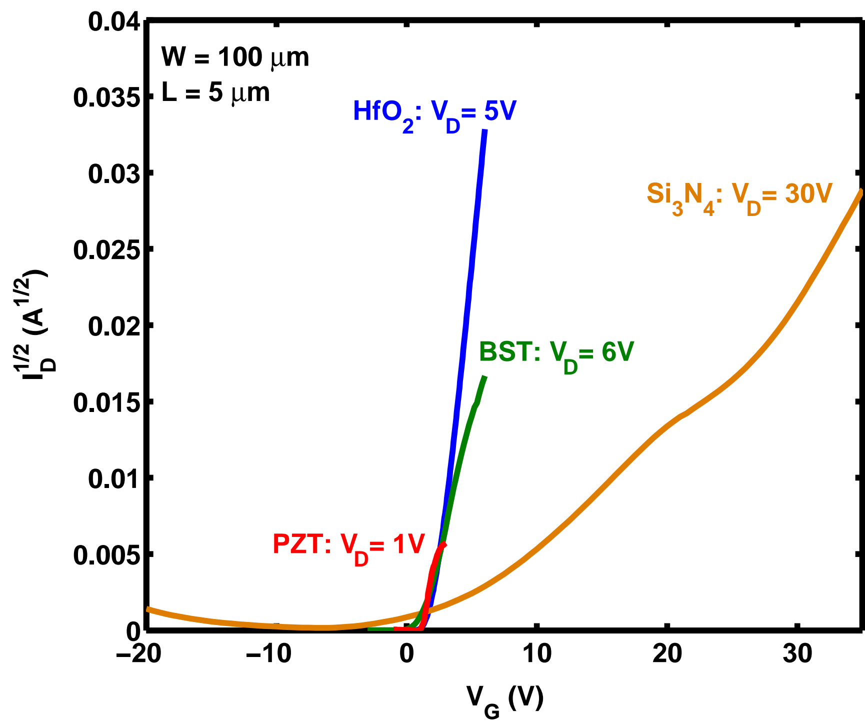


Figure 4.13: Demonstration of each high-k material effectively lowering V_{TH} compared to Si_3N_X.

to realize TFTs with higher and higher performance. From this TFT work, it can be seen that S changes with material and from work on MIS devices in Chapter III it can be seen that interface charge is present and influencing device operation. As a result a comprehensive study on interface charge density is carried out in Chapter V.

With the main goal, to reduce threshold voltage of ZnO TFTs, realized it is important to turn to V_{TH} stability issues. Fixed charges in the dielectric can cause non-ideal shifts in V_{TH} and also result in temperature and bias related instabilities, which if present and uncorrected, could render the devices unusable. In addition the understanding of the electrical characteristics and influences on grain boundaries in polycrystalline ZnO are not well understood and could contribute to device instability in terms of V_{TH} and S. As a result the investigation of ZnO TFTs with high-k dielectrics stability with respect to applied bias and temperature is carried out in Chapter VI.

Of the devices investigated in this section ZnO TFTs with thin HfO_2 gate dielectrics are the devices with the highest performance and meet and exceed the requirements for many applications including high performance AMLCDs. Further, researchers at AFRL have developed an anneal that, while not low-temperature, results in ZnO with mobilities over 100 $cm^2V^{-1}s^{-1}$ which opens up an entirely new group of applications for high-mobility TFTs, most notably microwave TFTs [5].

CHAPTER V

Interface Charge Study of Insulator-ZnO Heterojunctions

In previous Chapters the advantages of ZnO as a semiconductor have been shown and the advantages of ZnO/high-k structures have been illustrated. HfO_2 has emerged as the high-k dielectric of choice in this work and also for Silicon microelectronics due to the high dielectric constant, low leakage current, and low synthesis temperature. However, this work and recent studies have indicated potential drawbacks for integrating HfO_2 in ZnO thin film transistors including decreased device operation stability in the form of I_D-V_G hysteresis [8, 11, 85] and degradation of subthreshold slope characteristics [5, 85, 73], which may be linked to defects at the ZnO/dielectric interface. Understanding the characteristics of the ZnO/dielectric interface is an important step in advancing this exciting technology. Recent reports have estimated energy independent interface state density (N_{it}) and the energy dependent distribution of interface states (D_{it}) for ZnO/high-k interfaces via several methods. I_D - V_G hysteresis and subthreshold slope analysis on TFTs report N_{it} values of 2.7x10^{11} and 5.38x10^{12} cm^{-2} for ZnO/HfO_2 [8, 5] and 2.47x10^{12} cm^{-2} for ZnO/Ta_2O_5 [85]. Photo-excited trap-charge collection spectroscopy on Al_2O_3/PVP/ZnO structures has also been studied, where D_{it} peaks at 1.31 and 1.37 eV below the conduction band (E_C) were reported with values of 1x10^{13} and 5.1x10^{12} $cm^{-2}eV^{-1}$, respectively [42]. In

this Chapter, the density, energetic distribution, time constants, and capture cross sections of electrically active defect states in ZnO/HfO_2 structures are studied via several methods.

This Chapter will first discuss interface charge theory, then proceed with a discussion of the various techniques used in evaluation, results will be reported, and finally discussed.

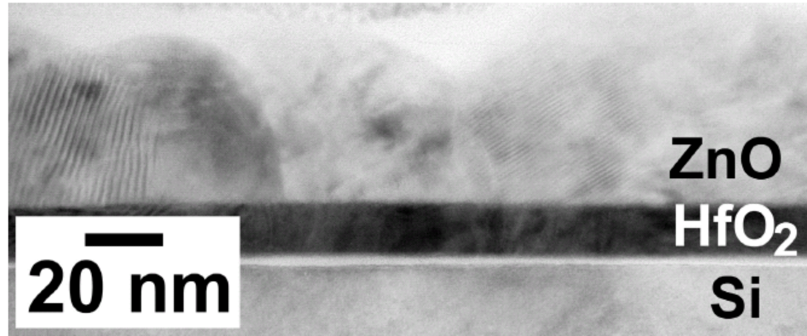
5.1 Interface charge theory

Interface charge is just one type of non-ideal charge that can be found in a semiconductor/dielectric system. Figure 5.1 graphically depicts the most common types of non-ideal charges, and their locations in the ZnO/dielectric system. This section will focus on characterizing interface trapped charge. To understand D_{it} it is important to look at this issue from a spacial and energy dependent perspective.

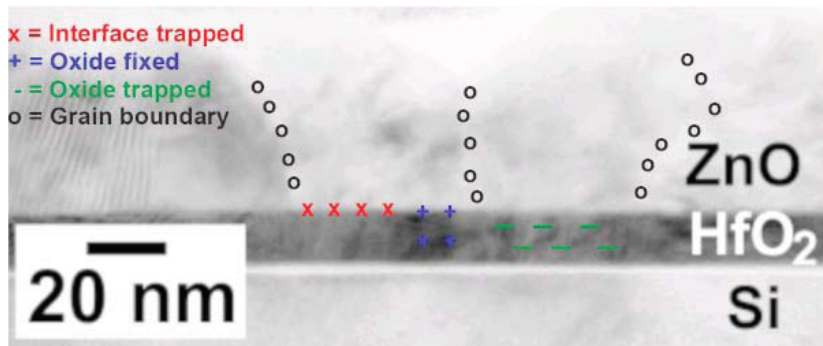
Spatially, interface trapped charges are located at the interface between the semiconductor and oxide as shown in Figure 5.1. Even in the most controlled and clean processes, the presence of impurities and crystal defects are present and responsible for excess electrons and ions that exist at this position in space and are the source of interface charge. This position in the device can also be seen in the diagram of a metal-insulator-semiconductor (MIS) capacitor in Figure 5.2.

With respect to energy, the impurities and defects at the interface cause the allowed energy states of the system to be different from those of the semiconductor alone. These states located within the forbidden energy gap play an important role in a device's non-ideal behavior. These allowed states are shown by the 'X's in Figure 5.3.

As the applied bias to a system with D_{it} ramps from deep depletion to accumulation (or visa versa), the Fermi level at the surface will cross each interface-impurity-allowed energy state and at each level the charge state of that trap must



(a)



(b)

Figure 5.1: (a) TEM image of AFRL ZnO deposited on ALD Al_2O_3 [5]. (b) Typical Non-ideal charges in semiconductor/dielectric system figuratively drawn to show spacial differences.

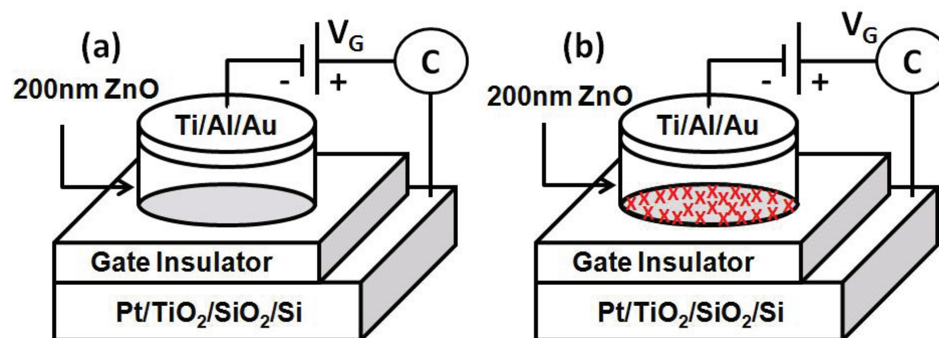


Figure 5.2: Location, in space of interface states. MIS-C device (a) without interface states and (b) with interface states (noted by red Xs)

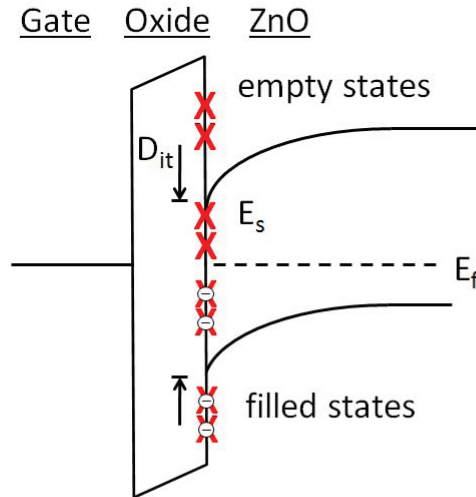


Figure 5.3: Location, in energy of interface states.

change. Because the interface charge, Q_{it}, can vary with allowed energy level, interface trapped charge density, D_{it}, can be represented by charge number per electron volt per area ($cm^{-2}eV^{-1}$). This change of charge with respect to applied bias has several implications:

- It introduces a voltage-dependent term Q_{it}/C_{OX} thus altering the capacitance of the system. Over a range of bias voltages that cause the Fermi level to cross many interface-allowed energy states, a distorted capacitance vs voltage curve with a non-ideal flatband voltage will result.
- By altering the capacitance performance of the system, Q_{it} limits a TFT's ability to modulate quickly, in voltage, from off to on.
- The loss in the system due to trapping and de-trapping acts as an interface resistance which changes the conductance-voltage characteristics of a device.
- In cases with extreme levels of D_{it} Fermi level pinning can occur. In these cases the Fermi level will not move with applied bias and the device is rendered useless. Fermi level pinning will be discussed later in this Chapter.

While each of the elements of device perturbation listed above are generally undesirable, we will describe how they can be used to characterize interface state density.

5.2 Interface Charge Evaluation Theory

Before reporting results of ZnO/HfO_2 interface trapped charge, in this Section, each technique utilized will be introduced and various advantages and disadvantages will be discussed.

5.2.1 TFT subthreshold slope

The value for estimated maximum energy independent interface state density, N_{it}^{max}, can be calculated from TFT transfer characteristics [5, 73] using the following equations flowing from equation 5.1, which is the characteristic equation for a transistor current in the subthreshold region.

$$I_D = I_{D1} exp\left(\frac{q(V_G - V_T)}{nkT}\right)\left(1 - exp\left(\frac{-qV_D}{kT}\right)\right) \quad (5.1)$$

where the non-ideality factor, n, accounts for the charge placed on the gate that does not result in inversion layer charge and is influenced by interface state charge capacitance, C_{it},

$$n = 1 + \frac{(C_b + C_{it})}{C_{ox}} \quad (5.2)$$

where C_b is the capacitance associated with charges in the semiconductor (historically called 'bulk'). Using the inverse of the slope of $\log_{10}(I_D)$ vs V_G (initially termed the inverse subthreshold slope, but now commonly referred to as simply subthreshold slope (S))

$$S = \frac{ln(10)nKT}{q} \quad (5.3)$$

one can calculate the maximum interface state density, N_{it}^{max}(termed "maximum" because this calculation assumes C_b to be small compared to C_{it}).

$$N_{it}^{max} = \left[\frac{S \cdot \left(\frac{q}{kT} \right)}{ln(10)} - 1 \right] \frac{C_{ox}}{q} \tag{5.4}$$

Calculating N_{it}^{max} is simple and the most often reported value for interface state density, but it does not reveal information about the energetic profile of interface states, just a per area value sum over the band-gap energies. This technique also does not provide information about the time constants or capture cross sections of interface charge. As a result N_{it}^{max}calculation is a good method for knowing, in a general sense, how much influence interface states may have in a particular material system or interface process and for comparing individual results to those reported by others. We will also use these values as a consistency test as we use more detailed techniques and then integrate those results over the band-gap energies producing a per area value comparable with this measurement and results reported in literature.

5.2.2 MIS capacitor capacitance-voltage

The remaining techniques used to understand the interface charge characteristics of the ZnO/HfO_2 material system use the MIS-C to extract D_{it}. Each technique leverages the discovery that capacitive and resistive losses due to interface charge alter the ideal MIS-C equivalent circuit as shown in Figure 5.4. The defect states alter the capacitance of the system as they add a charge state to the system (C_{it}). C_{it} is simply the interface state density (number of charges) times the electron charge, $C_{it} = q \cdot D_{it} \cdot Area$. Since these charges add to the capacitance, C_{it} can be modeled as a capacitor in parallel with the depletion capacitance of the semiconductor (C_S). The loss mechanism due to interface trap capture and emission of carriers can be modeled as a resistor, R_{it}, in series with C_{it} with a time constant of $\tau_{it} = R_{it} \cdot C_{it}$. In this work, the progression of techniques will be from simple towards complex. The first

technique simply uses the perturbation of the C-V profile of a device with interface charge to extract D_{it}. The next two techniques analyze only the real part of the admittance of a perturbed device and the final method utilizes the entire admittance spectrum to characterize the MIS capacitor, including interface charge.

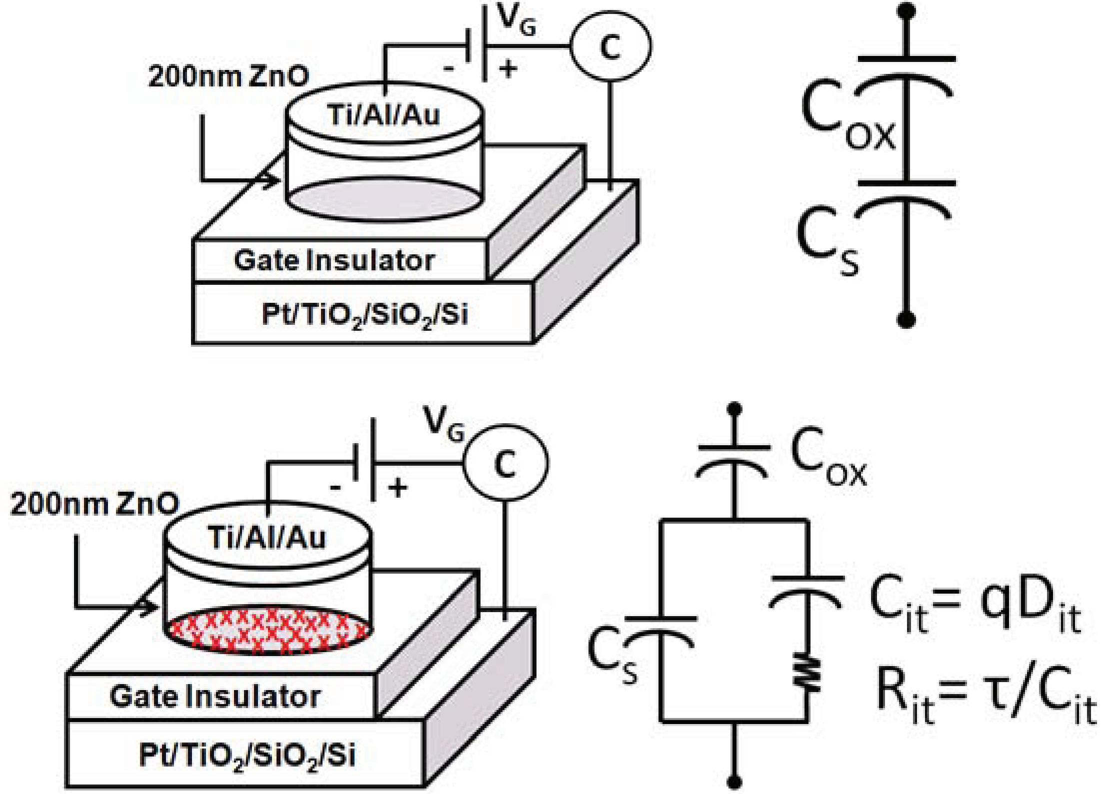


Figure 5.4: Schematic and equivalent circuit of ideal MIS and D_{it} influenced MIS device

From a C-V perspective, at any value of V_G all of the interface traps at energies below E_F corresponding to V_G will be filled causing an offset of capacitance in V_G-space from the ideal case. The shift in V_G-space can be represented by the relationship in Equation 5.5, which is a function of D_{it}. D_{it} is extracted using the V_G difference between an ideal C-V profile and the C-V profile of an MIS-C influenced by interface charge assuming D_{it} is a slowly changing function of ϕ_S.

$$V_G^{ideal} - V_G^{meas} = \frac{q \int_{\phi_{S1}}^{\phi_{S2}} D_{it}\left(\phi_S\right) \delta\phi_S}{C_{OX}} \tag{5.5}$$

The surface potential from the ideal case can be used to map V_G to band gap energy. In this way, a D_{it} vs band-gap energy ($E_C - E_F$) profile can be generated.

This technique is simple and allows D_{it} vs energy to be analyzed, but cannot give information about capture time constants and result confidence is limited by voltage measurement resolution and ideal model input value confidence.

5.2.3 MIS capacitor parallel conductance

The conductance technique, proposed by Nicollian and Goetzberger [61], is considered a very sensitive and complete method for determining D_{it} as it can identify interface trap densities of 10^9 cm^{-2}eV^{-1} and lower and can be used from depletion to weak inversion to find D_{it} [73]. The technique is based on the discovery by Nicollian and Goetzberger that the interface-influenced MIS-C equivalent circuit's admittance has a real part, termed conductance (G_P), that is a function of interface density and capture time constant. Figure 5.5 shows how Nicollian and Goetzberger mapped the equivalent circuit for an MIS-C with interface charge to parallel parameter form.

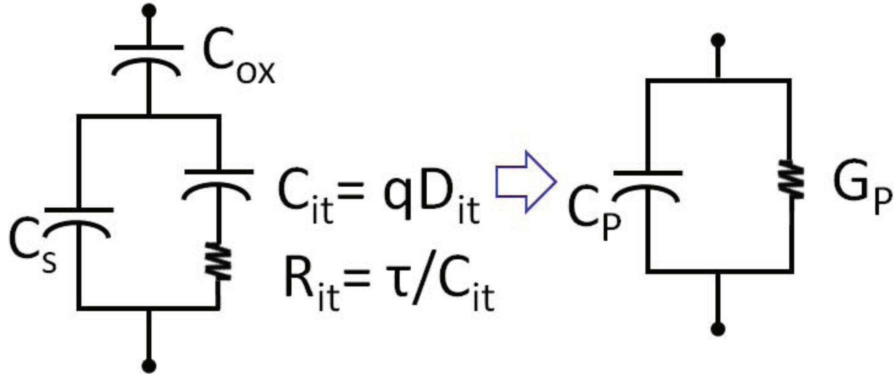


Figure 5.5: Basis equivalent circuit and equivalent circuit used for extraction of D_{it} via the parallel conductance methods

Through AC circuit analysis Nicollian and Goetzberger developed transformations that allow the measured values of conductance (G_m) and capacitance (C_m), of an MIS-C to be mapped to a radial frequency ($\omega = 2\pi f$) dependent formula for parallel

conductance,

$$G_P = \frac{\omega^2 G_m C_{ox}^2}{G_m^2 + \omega^2 \left[(C_{ox} - C_m)^2\right]} \tag{5.6}$$

which in turn could be divided by radial frequency to yield a normalized G_P explicitly containing D_{it}

$$\frac{G_P}{\omega} = \frac{\omega \tau_{it} q D_{it}}{1 + (\omega \tau_{it})^2} \tag{5.7}$$

which peaks when $\omega \cdot \tau_{it} = 1$ resulting in easy extraction of D_{it} from the peak value of G_P/ω

$$D_{it} = \left[\left(\frac{G_P}{\omega}\right)_{peak}\right]\left[\frac{2}{q}\right] \tag{5.8}$$

$$\tau_{it} \cdot \omega = 1 \tag{5.9}$$

In practicality, there is time constant dispersion which causes G_P/ω vs ω to follow the following relation [62]

$$\frac{G_P}{\omega} = \frac{q D_{it}}{2\omega \tau_{it}} \ln\left[1 + (\omega \tau_{it})^2\right] \tag{5.10}$$

resulting in the following D_{it} and $\tau_{it} \cdot \omega$ relationships

$$D_{it} = \left[\left(\frac{G_P}{\omega}\right)_{peak}\right]\left[\frac{2.5}{q}\right] \tag{5.11}$$

$$\tau_{it} . \omega = 2 \tag{5.12}$$

It can be seen from Equation 5.10 that G_P/ω will peak with either ω or τ_{it} as a sweep parameter. The following two techniques sweep these two parameters and extract D_{it} from the resulting normalized conductance peaks.

ω as the sweep parameter An example of normalized parallel conductance peak behavior can be seen in Figure 5.6. Test frequency is used to sweep ω in the frequency dependent version of the parallel conductance technique.

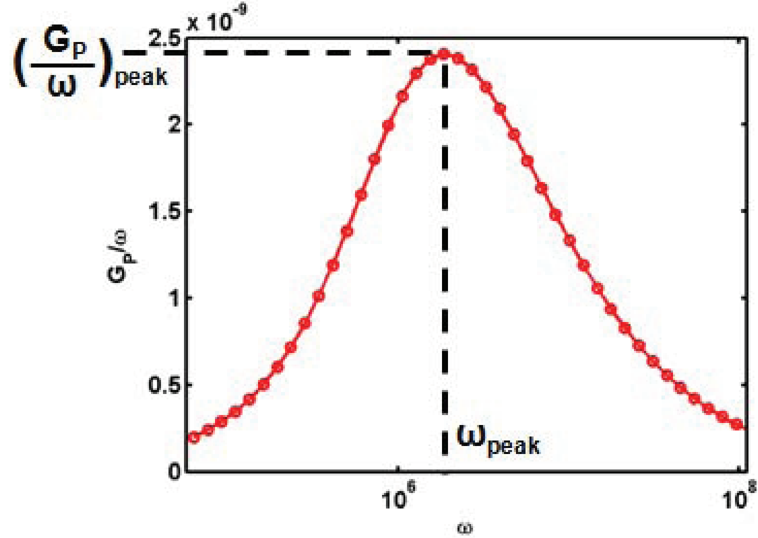


Figure 5.6: G_P/ω behavior with swept ω.

The Keithley 4200 SCS C-V capability was used to measure MIS-C capacitance and conductance versus frequency at gate voltages (V_G) from depletion to accumulation. The equations discussed above (Equations 5.11 and 5.12) were used to extract D_{it} and τ_{it} at each V_G where data fit theory, which corresponded to energies from depletion to above flatband. To construct D_{it} and τ_{it} vs ϕ_s plots, a simulated MIS-C ideal fit was used to map V_G to ϕ_s.

τ_{it} (temperature) as a sweep parameter Temperature is used to sweep τ_{it} in the temperature stimulated version of the parallel conductance technique (TSC). It has been shown [66] that only τ_{it} varies with temperature and it does so monotonically so that as Equation 5.10 peaks in temperature space,it is also peaking in τ_{it} space. As a result, values for D_{it} can be extracted in much the same way as with the frequency dependent method as shown in Figure 5.7.

The advantages of using the thermally stimulated conductance (TSC) technique to extract D_{it} include the requirement of only one measurement frequency and that one can choose that frequency to be low enough to prevent side effects, like those due to possible resistances in series with the MIS system [66, 19].

To conduct TSC measurements, the Keithley 4200 was used in concert with a temperature controlled cryogenic testing system.

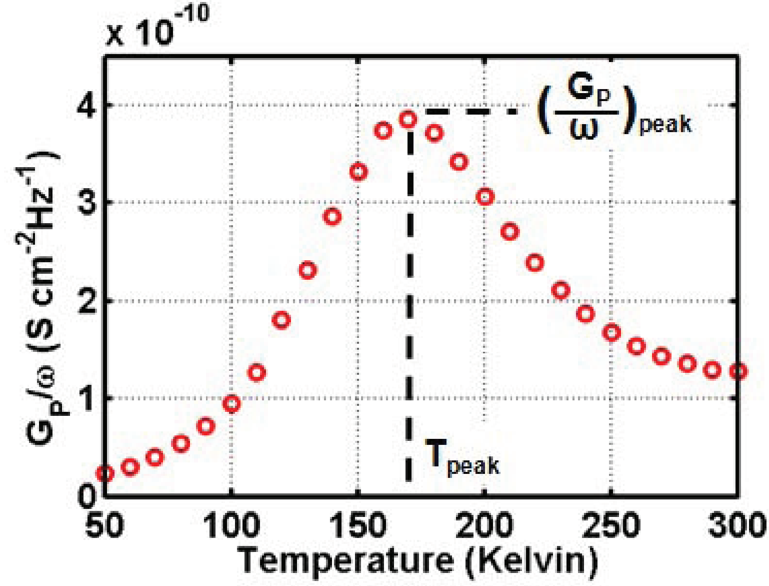


Figure 5.7: D_{it} extraction via Thermally Simulated Conductance Method (G_P/ω vs temperature).

We will show that our experimental data fits the time constant perturbed theoretical curves for D_{it} well (Equation 5.10). More specific details of the techniques employing G_P/ω can be found elsewhere [73, 61, 62, 80, 19].

5.2.4 Admittance spectroscopy (Cole-Cole Plotting)

Admittance spectroscopy is a method based on evaluating the frequency dependent admittance (Y) of an MIS-C plotted in the complex plane. This plot is called a Cole-Cole plot for Cole & Cole's work to describe dispersion and absorption in dielectrics [15]. Dispersion and absorption of dielectrics can be represented by the characteristic equation 5.13

$$\epsilon * -\epsilon_\infty = \frac{(\epsilon_0 - \epsilon_\infty)}{[1 + (i\omega\tau_0)^{1-\alpha}]} \tag{5.13}$$

$$\epsilon* = \epsilon'' - i\epsilon' \tag{5.14}$$

where $\epsilon*$ is the complex dielectric constant, ϵ'' and ϵ' are the real and imaginary parts of the dielectric constant, respectively, ϵ_∞ is the 'infinite frequency' dielectric constant, ϵ_0 is the 'static' dielectric constant, τ_0 is a generalized relaxation time, and α can assume values from 0 to 1 where 0 leads to the representation given by Debye for polar dielectrics. It will be shown that ZnO/HfO_2 MIS-C devices exhibit Debye behavior; as a result the discussion will proceed assuming $\alpha = 0$. Three important results flow from the characteristic equation above:

- $\epsilon*$ can be represented by a three component equivalent circuit (Figure 5.8, left) of the same form used to describe an MIS-C influenced by interface charge.
- The plot of $\epsilon*$ on the complex plane has a characteristic shape from which the three components of the equivalent circuit can be extracted (Figure 5.8, right).
- The Cole-Cole analysis can be conducted on an MIS-C influenced by interface charge as shown in Figure 5.9 and interface charge densities and corresponding time constants can be extracted.

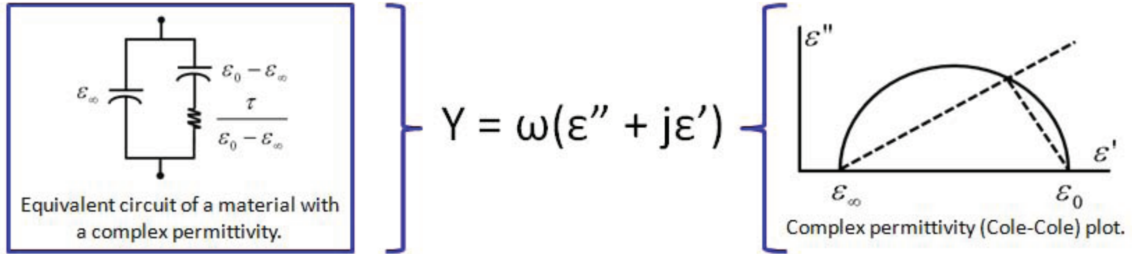


Figure 5.8: Characteristic representations of Debye dielectric constant

Cole & Cole compare the complex plane plotting and results analysis to that of a technique akin to the parallel conductance method discussed previously, "the experimental data are not readily analyzed by such a representation nor is the significance

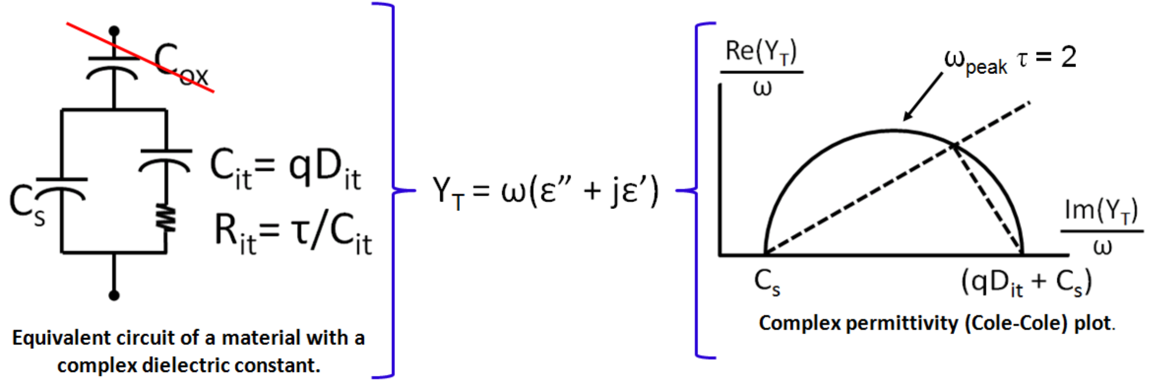


Figure 5.9: Representations of Cole-Cole analysis for MIS-C influenced by interface charge.

of departures from the expected behavior easily appreciated. A more convenient basis for discussion is the Argand diagram or complex plane locus in which the imaginary part of the complex dielectric constant is plotted against the real part, each point being characteristic of one frequency of measurement." [15]

Due to the three component equivalent circuit, the theory for dispersion and absorption of dielectrics can be applied to the measured admittance (Y) of an MIS-C device influenced by interface state charge density [49]. The equivalent circuits on the left side of Figures 5.8 and 5.9 show how the Cole-Cole circuit components are mapped to MIS-C circuit components. In MIS-C, the characteristic time constant value is not independent of energy and thus a correction needs to be accounted for before extracting values for interface state density and associated time constant [63, 49]. The following equations show how plotting Y on the complex plane allows the extraction of D_{it} and τ_{it}:

$$\epsilon'' = \frac{Re(Y)}{\omega} = \frac{G_{it}}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} ln\left[1 + (\omega\tau_{it})^2\right] \tag{5.15}$$

$$\epsilon' = \frac{Im(Y)}{\omega} = C_{it} + C_{SC} = q\frac{D_{it}}{\omega\tau_{it}} arctan\left(\omega\tau_{it}\right) + C_{SC} \tag{5.16}$$

D_{it} and τ_{it} can be directly obtained from a Cole-Cole plot of the measured AC admittance (Y); the distance between end points of the Cole-Cole plot equals $q \cdot Area \cdot D_{it}$. For a system with negligible surface potential standard deviation (σ_s), τ_{it} can be determined from the relation $\omega_{peak} \cdot \tau_{it} = 1.98$ where ω_{peak} is ω at the maximum value of G_{it}/ω.

Testing was done using a Keithley 4200 SCS in capacitance-voltage mode. Typically, impedance (Z) can be measured, C_{OX} can be mathematically removed, and then Y is determined ($Y = 1/Z$). Because data already existed in measured parallel capacitance (C_m) and conductance (G_m) form, that data was transformed to Y via the following equation:

$$Y = \left[\frac{1}{G_m - j\omega C_m} - \frac{1}{j\omega C_{ox}} \right]^{-1} \tag{5.17}$$

where $C_{OX} = 1.9x10^{-9}F$ was determined by off-mesa MIM capacitors. It is important to note that the assumption is made that all of the surface states are located at the semiconductor-gate oxide interface. A similar method to that described above can be made with the assumption of states distributed within a certain distance from the interface [49].

5.3 Interface Trapped Charge Results

5.3.1 TFT subthreshold slope

ZnO TFT devices with 30 nm of HfO_2 were tested using techniques and equipment discussed in Chapter IV and exhibit output and transfer curves that follow square law theory as shown in Figure 5.10, where estimated electron channel mobility in the saturation region, threshold voltage, and S were determined to be 26 $cm^2V^{-1}s^{-1}$, 1.1 V, and 180 mV/dec, respectively. $C_{ox} = 5.7\text{x}10^{-7}$ F/cm^2 was measured on parallel plate HfO_2 capacitors per methods described in Chapter II. N_{it}^{max} was found to be 7.2x10^{12}

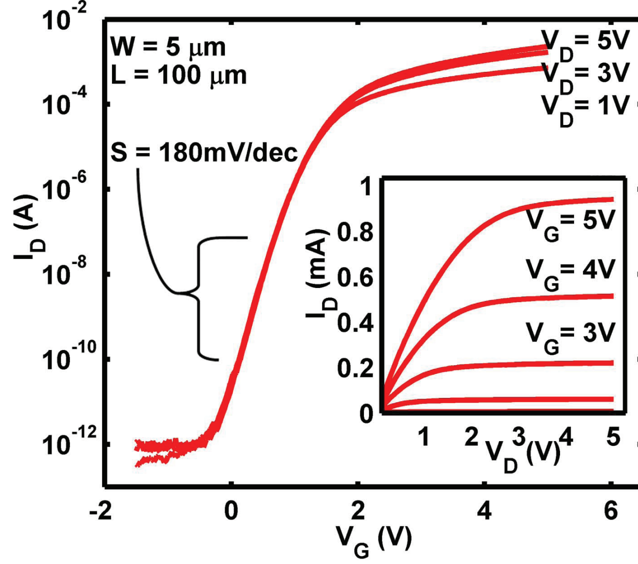


Figure 5.10: Measured I_D-V_G characteristics of ZnO TFT, extracted subthreshold slope, and (inset) I_D-V_D characteristics

cm^{-2}, comparable to previously reported values for ZnO/HfO_2 heterostructures [8, 5].

5.3.2 MIS capacitor C-V

Capacitance - Voltage curves for MIS-C devices with 200nm of ZnO and 30nm of HfO_2 were evaluated using a Keithley 4200-SCS with CV acquisition card. A comparison of measured and simulated C-V characteristics at 10 kHz is shown in Figure 5.11(a) with the region of interest for extracting D_{it} is denoted by circle data points. Simulation C-V values were acquired via the method described in Chapter III. ϕ_{MS} was chosen to be 1.658 eV, which is about 0.46 eV above the ideal value for ϕ_{MS}. We attribute this shift to fixed charges in the HfO_2; this phenomenon is studied in-depth in Chapter VI. The D_{it} energy spectrum corresponding to C-V deviation from ideal is shown in Figure 5.11(b) and can be seen to take on a roughly exponential shape with D_{it}= 3.0x10^{13}cm^{-2}eV^{-1} near the conduction band and 5.3x10^{12}cm^{-2}eV^{-1} 0.18 eV below.

As previously mentioned, D_{it} extraction via C-V profile is a good method to estimate D_{it}, but has many limitations including resolution limited by voltage mea-

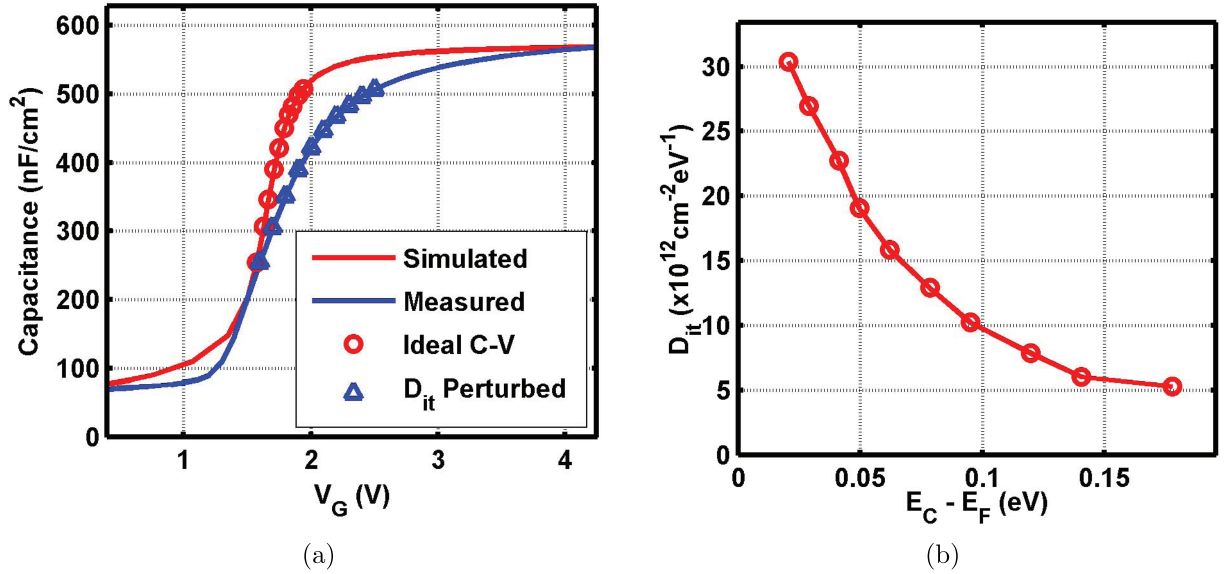
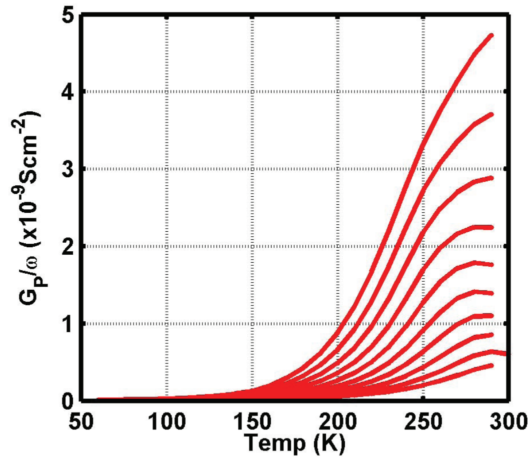


Figure 5.11: D_{it} extraction via CV Profile Ideal/Non-ideal Comparison. (a) Simulated capacitance (red) and measured capacitance (blue) vs applied voltage. (b) D_{it} via CV Profile vs energy below conduction band.

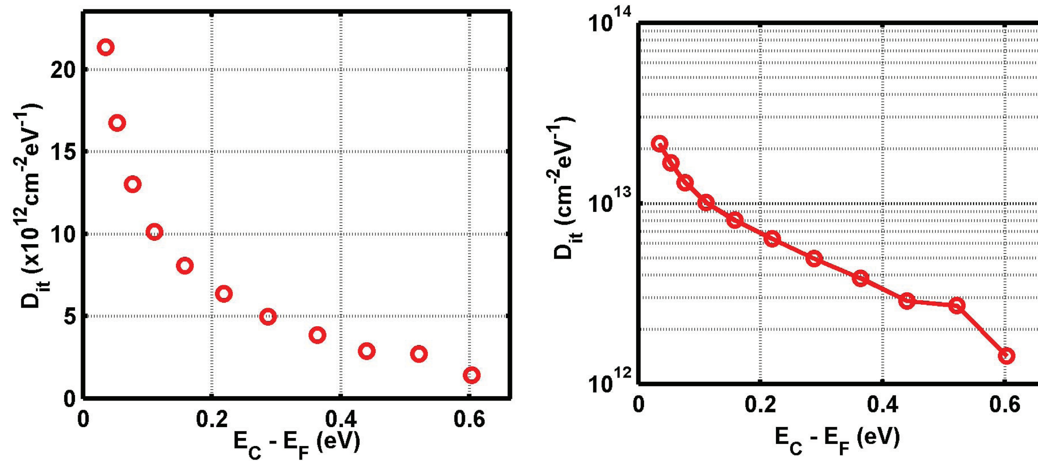
surement resolution and confidence is limited by compounding confidences of many simulation input variables. In the next sections, we introduce more rigorous approaches to experimentally determining D_{it}.

5.3.3 Thermally stimulated conductance (TSC)

The results from TSC measurements on an MIS-C device with 60 nm of HfO_2 gate dielectric at 10 kHz are presented in Figure 5.12. The temperature was swept from 30 Kelvin to 300 Kelvin (Figure 5.12(a)) and V_G was swept from strong depletion to accumulation. The farther into the band gap V_G probes, the higher the temperature at which G_P/ω peaks. As a result our highest measurement temperature, 300 K, limits us to probing no more than 0.6 eV below E_C. In the region of measurement validity we see D_{it} shape as nearly exponential with values of $D_{it} = 2.1\text{x}10^{13}$ cm^{-2}eV^{-1} near the conduction band and 1.3x10^{12} cm^{-2}eV^{-1} 0.6 eV below E_C, which is in general agreement with the TFT subthreshold slope method.



(a)



(b)

Figure 5.12: Thermally Stimulated Conductance Results. (a) $\frac{G_P}{\omega}$ vs Temperature. Each curve corresponds to a unique V_G bias point. (b) D_{it} determined via Thermally Stimulated Conductance.

5.3.4 Frequency dependent conductance

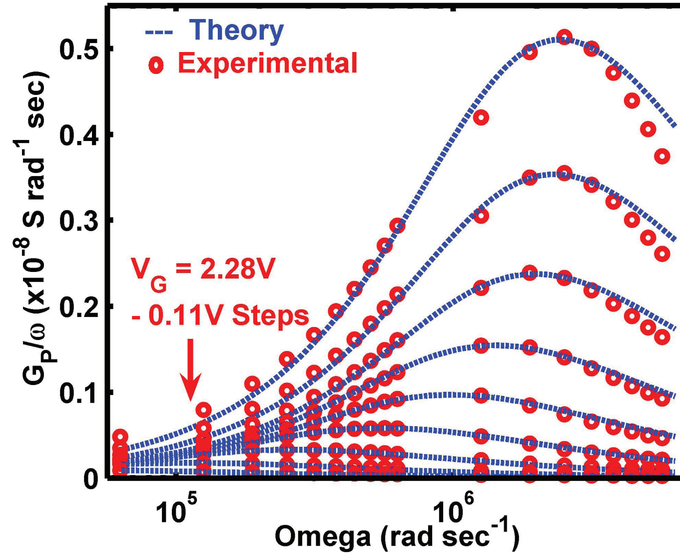
Measured G_P/ω vs ω for various gate biases is shown in Figure 5.13(a), where relations fit closely to the parallel conductance model in Equation 5.10. A contour plot of this data is similarly shown in Figure 5.13(b).

The shift in G_P/ω peaks with bias indicates efficient movement of the Fermi level with bias, where there is no clear evidence for Fermi level pinning [2]. The D_{it} values obtained from conductance measurements indicate a distribution of interface states in the range of 3.2x10^{13} to 4.1x10^{11} cm^{-2}eV^{-1} from near E$_C$ to E$_C$ – 0.8eV, as shown in Figure 5.14(a).

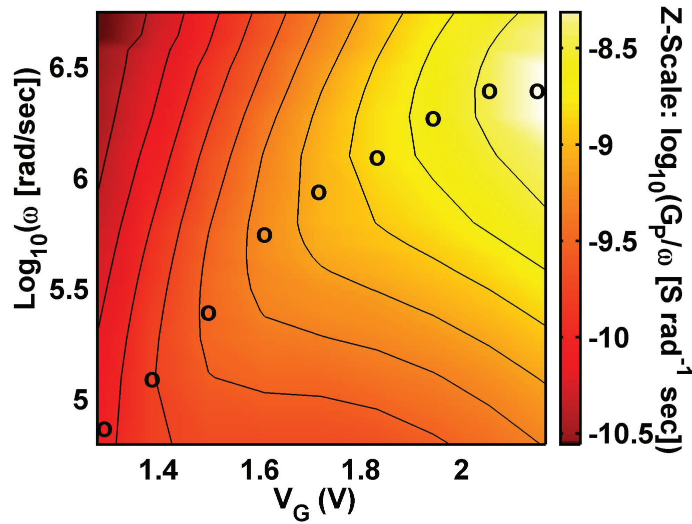
By sweeping ω the characteristic time constant at each energy level can be found via the relationship in Equation 5.12 and the associated capture cross section can be related to trap time constant by the following equation [73]

$$\sigma_n = \frac{1}{\tau_{it} v_{th} N_c} exp\left(\frac{E_C - E_T}{k_B T}\right) \tag{5.18}$$

where v_{th} is the thermal velocity of electrons in the semiconductor (v_{th} = 1.5x10^7 cm/s) [1], N_C is the density of states in the conduction band (N_C = 3.5x10^{18} cm^{-3}) [77], and $E_C - E_T$ is the energy below the conduction band, which we related to V_G as described previously. The time constants for these traps (Figure 5.14(b) [red]) determined from the peaks observed in G_P/ω data is in the range of $\tau_{it} = 0.7$ μsec - 50 μsec increasing as the Fermi level decreases below E_C. The capture cross section (Figure 5.14(b) [blue]) was calculated to be in the range of $1.2x10^{-19} < \sigma_n < 2.8x10^{-8}$ cm^2 from E_C to 0.8 eV below E_C. The range and trend of capture cross section data is comparable to other MIS systems, including data obtained for Si-SiO_2 via high-temperature A-S [44]. Variable temperature admittance measurements and related techniques will provide further insight on τ_{it} and σ_n in the ZnO/HfO_2 system. Integrated interface state density based on the D_{it} extraction results in a value of N_{it} =



(a)



(b)

Figure 5.13: Frequency dependent conductance G_P/ω data. (a) G_P/ω vs ω with a curve shown for each V_G value. (b) G_P/ω vs ω vs V_G contour plot. $(G_P/\omega)_{peak}$ values indicated by white 'O's.

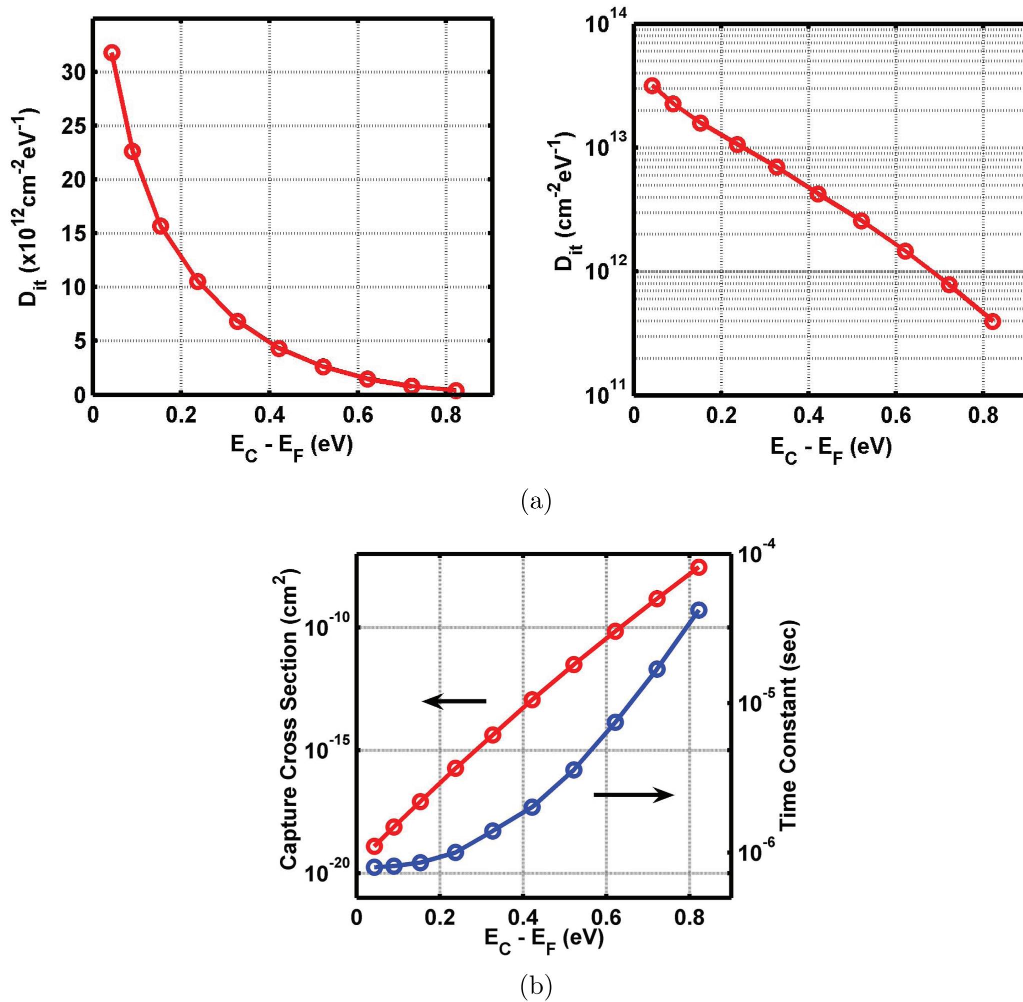


Figure 5.14: D_{it}, time constant, and capture cross section data extracted from frequency dependent conductance method. (a) D_{it} vs Energy. (b) Extracted time constants (red) and calculated capture cross sections (blue).

$5.6x10^{12}$ cm^{-2}, which is in reasonable agreement with our extraction from the TFT subthreshold slope in Section 5.2.1.

5.3.5 Admittance spectroscopy results

Cole-Cole plots of an ZnO/HfO_2 MIS-C at varying bias are shown in Figure 5.15, and result in excellent fits to the Debye behavior described in Equations 5.15 and 5.16 assuming negligible σ_s.

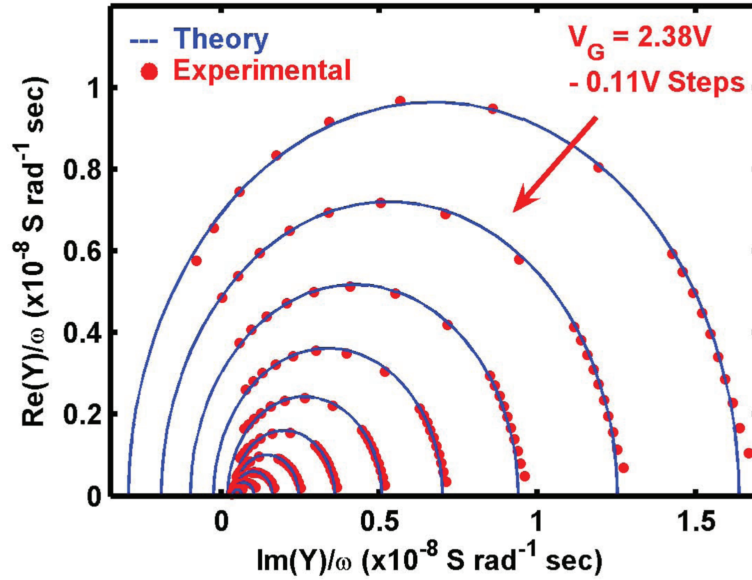


Figure 5.15: Cole-Cole plot of ZnO MIS-C with 30nm of HfO_2 dielectric

The D_{it} values obtained from Cole-Cole plotting indicate a distribution of interface states in the range of $3.0x10^{13}$ to $1.2x10^{12}$ cm^{-2}eV^{-1} from near E_C to $E_C - 0.9$ eV, as shown in Figure 5.16(a).

Integrated interface state density based on the D_{it} extraction results in a value of $N_{it} = 7.9x10^{12}$ cm^{-2}, which is in agreement with N_{it} extraction from the TFT subthreshold slope. The time constants of these states extracted from ω_{peak} are in the range of $\tau_{it} = 0.8$ μsec - 8 μsec, as shown in Figure 5.16(c). The range of capture cross section is $3.4x10^{-19} < \sigma_n < 8.6x10^{-6}$ cm^2 obtained via the method described in

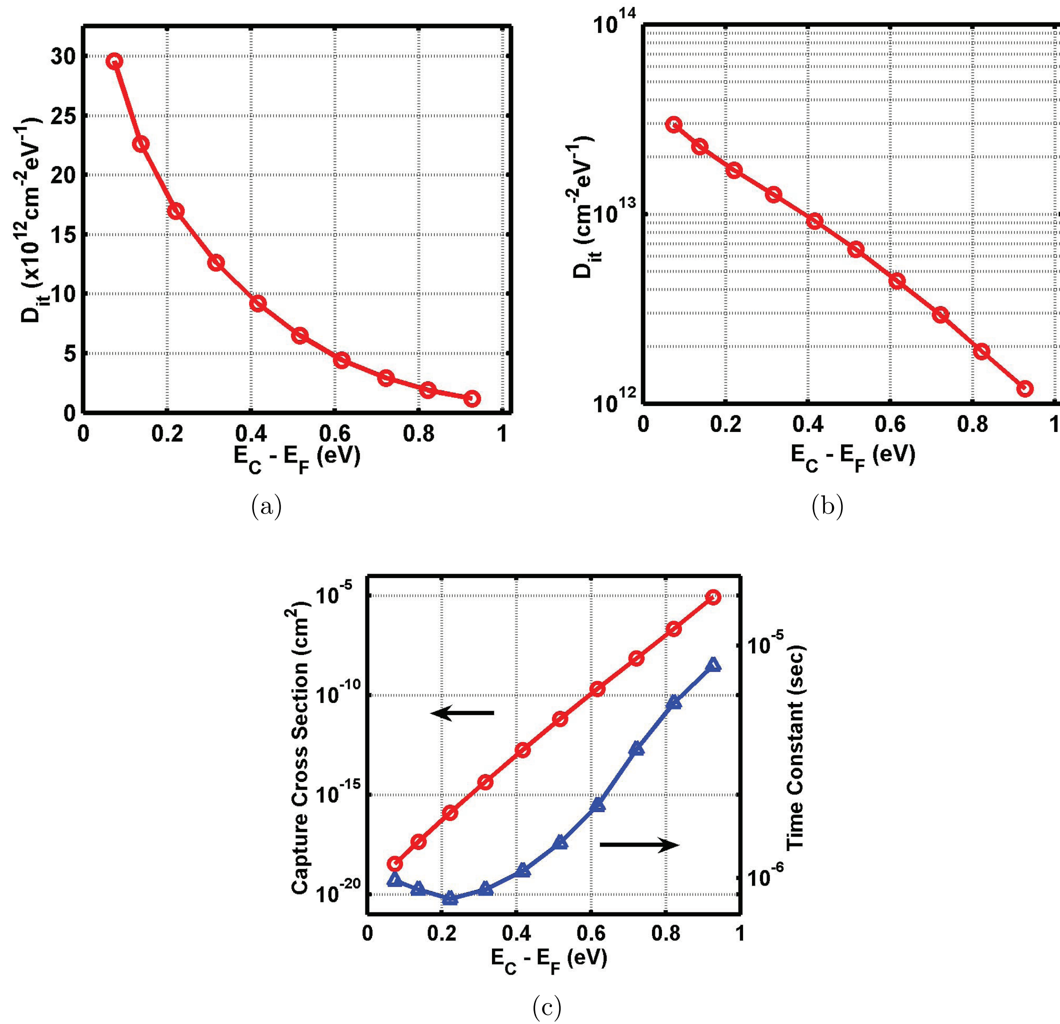


Figure 5.16: Admittance Spectroscopy Results. (a) D_{it} vs Energy. (b) Semi-logarithmic plot of D_{it} vs Energy. (c) τ_{it} and $\sigma_n$vs Energy.

Section 5.2.3 and Equation 5.18, from near E_C to E_C – 0.9 eV, as shown in Figure 5.16(c)[red].

5.4 Fermi level pinning / movement efficiency

Interface charge, if large enough, may cause the Fermi energy on the surface to be 'pinned' preventing changes of the surface potential in response to the changes of the voltage applied to the MIS-C device, which as a result, is rendered dysfunctional [72].

According to Ali et al. [2] "Fermi level movement efficiency is defined as the ratio of the change in the Fermi Level at the oxide-semiconductor interface in the presence of D_{it} to the change in Fermi level without D_{it}, for a unit applied gate voltage. Mathematically, it can be represented as follows:"

$$E_F^{ME} = \frac{1 + C_S/C_{OX}}{1 + (C_S + C_{it})/C_{OX}} \% \tag{5.19}$$

C_S is the depletion capacitance, which can be extracted from a MIS-C curve with no interface charge capacitance influence via the characteristic equation for an MIS-C [53] in Equation 3.1 and C_{it} is the interface charge capacitance, $C_{it} = q \cdot D_{it} \cdot Area$. A movement efficiency of 100% means that the Fermi Level is perfectly free to move in response to applied voltage on the gate and a value of 0% would mean there is absolutely no change in Fermi Level with applied voltage.

Reports on GaSb/Al_2O_3 MIS-C devices report E_F^{ME} that values from 60% to 90% in devices deemed acceptable for transistor applications. No reports of Fermi level movement efficiency on ZnO devices have been found in the literature.

Using the D_{it} found via frequency dependent parallel conductance in Section 5.3.4 and C_S extracted from 500 kHz C-V presented in Chapter III the Fermi Level Movement Efficiency was calculated and can be seen in Figure 5.17

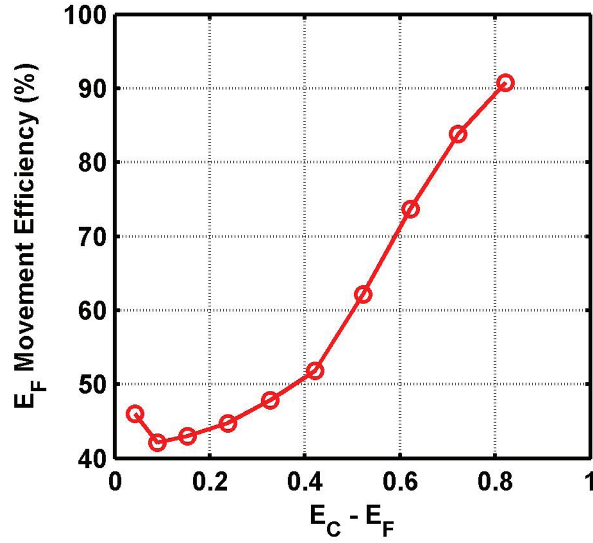


Figure 5.17: Fermi Level Movement Efficiency

where at energies near E_C movement efficiency is near 40% and increases to 90% at 0.8 eV below E_C due to the inverse trend with D_{it}. Based on the GaSb report and the fact that we have high-performance transistors with these interfaces, E_F^{ME} values shown are not low enough to significantly reduce device performance.

5.5 Discussion

In this Chapter complementary methods to characterize interface charge in ZnO/HfO_2 devices have been explored. Admittance Spectroscopy was found to be the most comprehensive technique and had the best agreement with N_{it} values obtained from TFT subthreshold slope. D_{it} values can be seen in Figure 5.18 ranging from values in the low 10^{13} to high 10^{11} cm^{-2}eV^{-1}, which is considered high for Silicon CMOS devices, but the ZnO interfaces presented in this work exhibit no fermi level pinning and are used in devices that show state-of-the-art performance as seen in Table 1.2.

Summary data can be seen in Table 5.1. The maximum values for capture cross section approach the cross sectional area of TFT devices used, which seems unusually large.

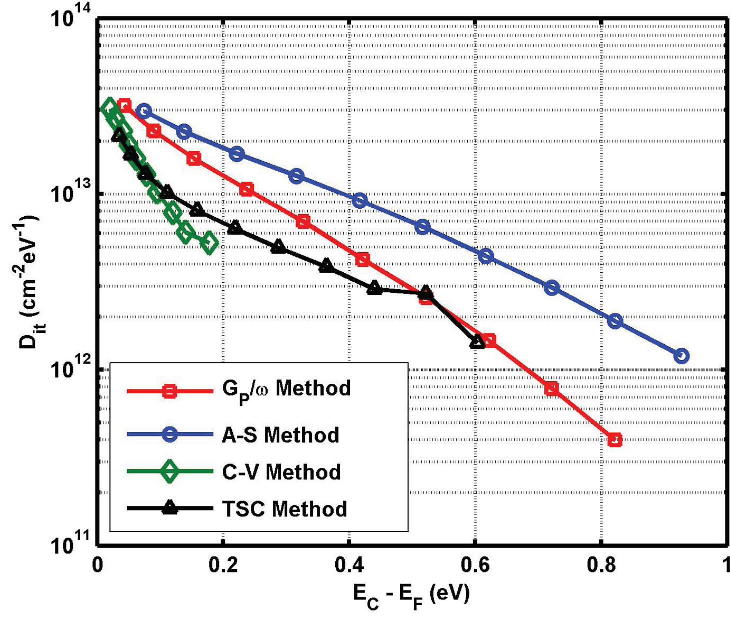


Figure 5.18: D_{it} vs Energy for techniques used in this work.

Parameter	Units	TFT S	C-V	$\left(\frac{G_P}{\omega}\right)_{Temp}$	$\left(\frac{G_P}{\omega}\right)_{freq}$	A-S
D_{it}^{max}	10^{12} $cm^{-2}eV^{-1}$		30	21	32	30
D_{it}^{min}	10^{12} $cm^{-2}eV^{-1}$		5	6	0.41	1.2
Energy^{max}	eV		0.02	0.03	0.04	0.07
Energy^{min}	eV		0.2	0.6	0.8	0.9
N_{it}	10^{12} cm^{-2}	7.2	1.9	3.3	5.6	7.9
τ_{it}^{max}	μS				50	8
τ_{it}^{min}	μS				0.7	0.8
σ_n^{max}	cm^2				2.8x10^{-8}	8.6x10^{-6}
σ_n^{min}	cm^2				1.2x10^{-19}	3.4x10^{-19}

Table 5.1: Summary data from interface charge investigation

Qualitatively, data shows fast interface traps with very large capture cross sections near the conduction band. These traps degrade TFT subthreshold slope and are likely responsible for elevated values of clockwise hysteresis observed in ZnO/HfO_2 devices [76].

For future low power and other applications that require low hysteresis, interface trapped charge will need to be reduced in order to achieve technology insertion. Possibilities for improving interface qualities via engineering include the following concepts:

- Insertion of a low D_{it} inter-layer between ZnO and HfO_2.
- Introduction of pre and/or post treatments during materials deposition.
- Use of deposition methods that introduce less damage. Deposition of ZnO via ALD rather than PLD may result in different interface characteristics due to the difference in kinetics between the two methods.

Finally, understanding D_{it}'s role in TFT performance will be important as this work advances to study thin-film transistor stability in the next chapter.

CHAPTER VI

Bias - Temperature - Stress Studies on High-k/ZnO Devices

6.1 Introduction

The advantages of ZnO as a semiconductor and ZnO/high-k structures have been illustrated in previous Chapters. One potential drawback illuminated in Chapter III is voltage profile instability. In this section Bias - Temperature - Stress (BTS) measurements are used to characterize the stability of ZnO/HfO_2 TFTs.

Stabilities of many figures of merit are important for TFT applications and much work has been done to characterize the stability of a-Si and poly-crystalline silicon (p-Si) TFTs. Extensive Bias-Temperature-Stress (BTS) studies have been carried out on a-Si and p-Si TFTs to track the temporal characteristics of threshold voltage (V_{TH}), subthreshold slope (S), mobility (μ_{FE}), grain boundary trap creation (N_{TG}), and to correlate TFT parameter instabilities with physical mechanisms that include charge trapping and charge state creation, which can both take place in the gate dielectric, interface, and grain boundaries [71, 13, 48]. It is of note that Powell [71] has reported devices with two regions, depending on the magnitude of V_{STR}, where a different mechanism is attributed to device instability. At higher V_{STR} values charge trapping in the oxide seemed to dominate BTS characteristics and at lower V_{STR}

values charge state creation seemed to dominate. Both these regions exist in the same a-Si devices and both mechanisms are used to explain the majority of voltage instabilities of TFTs reported in the recent past.

6.1.1 Charge trapping

Charge trapping occurs when carriers from the semiconductor channel are captured by electrically active traps located at or near the semiconductor-gate dielectric interface and throughout the dielectric. As a result, the charge of these carriers is fixed at these trap locations and thus alter the charge of the system, resulting in a change in threshold voltage (ΔV_{TH}. A figurative representation of this mechanism can be seen in Figure 6.1.

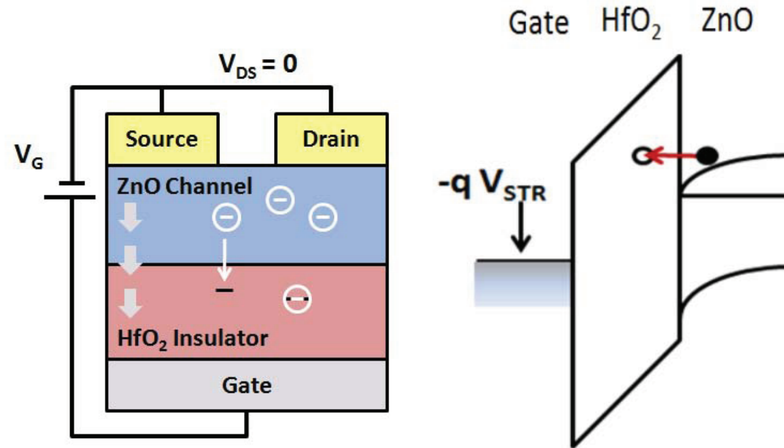


Figure 6.1: Left: Schematic TFT cross sectional representation of channel carriers tunneling into gate dielectric traps. Right: Band diagram representation of channel carriers tunneling into gate dielectric traps.

A model used to describe charge trapping in SiO_2 was proposed by Ross and Wallmark [20]. Based on the premise that the change in threshold voltage must be caused by a change in charge injected into the gate dielectric.

$$\Delta V_{TH}(t) = \frac{\Delta Q(t)}{C_{OX}} \tag{6.1}$$

$\Delta Q(t)$ can then be calculated by assuming a uniform distribution of traps in the dielectric and a classical tunneling function for the probability of carriers accumulated at the interface tunneling into the dielectric. The probability function takes the form

$$\omega(x) = \omega_0 e^{(-x/\lambda)} \tag{6.2}$$

where ω_0 is the carrier cross section at the interface, x is the distance into the dielectric, and λ is the tunneling parameter which is a function of the gate voltage and dielectric material properties. The relationship for $\Delta Q(t)$ is then [20, 79]

$$Q(t) = \int_0^t dt' \int_0^x N_{tr}\omega(x')e^{[-\omega(x')t']}dx \tag{6.3}$$

where N_{tr} is the volume trap density in the dielectric and the exponential function serves to limit the value of integrated charge to N_{tr} over all x.

One equation often used in literature to show data conforms to dielectric charge trapping is a solution to equation 6.3 of the form

$$\Delta V_{TH} \approx r_d \ln(1 + \frac{t_{STR}}{t_0}) \tag{6.4}$$

which assumes time-dependent tunnelling probabilty and interface states are included explicitly [20]. r_d is a decay rate constant which is proportional to the product of N_{tr} and λ [70].

Another commonly used equation assumes a distribution of trap energy levels, uniform spacial distribution of traps, and takes the form

$$\Delta V_{TH} \approx r_d \ln(\frac{t_{STR}}{t_0}). \tag{6.5}$$

Later in this chapter a refined technique for modeling charge trapping due to carrier tunneling (injection) into the dielectric will be presented that allows extraction

of N_{tr}. For now the understanding that ΔV_{TH}, due to charge trapping, characteristics include a linear increase with logarithmic time and temperature independence will suffice

6.1.2 Charge state creation

Charge state creation occurs when enough energy is given to the system to change the semiconductor, interface, or insulator materials in a way that electrically active states are created. In a-Si and p-Si devices, weak Silicon bonds in the semiconductor network can be broken leaving dangling bonds. In addition, hydrogen can thermally dissociate from Silicon atoms at grain boundaries leaving a negatively charged state behind. Both cases are examples of charge state creation. A figurative representation of interface state creation can be seen in Figure 6.2.

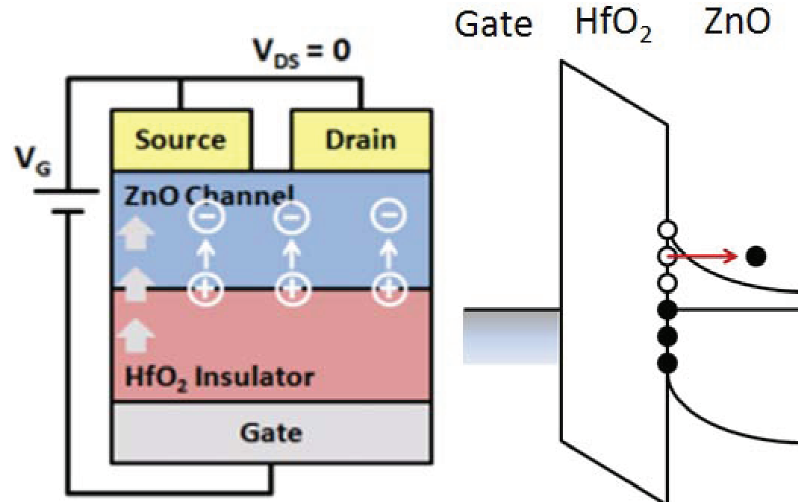


Figure 6.2: Left: Schematic TFT cross sectional representation of ions disassociating from interface resulting in interface state creation. Right: Band diagram representation of interface state creation.

The ΔV_{TH} dependence expected when charge state creation is the dominant mechanism has been shown to follow a power law relationship such as the form shown in Equation 6.6 [13], which was developed assuming diffusion limited interface state generation as hydrogen disassociates from an interface defect and diffuses into the gate

oxide [32].

$$\Delta V_{TH} \propto t^n e^{(-Ea/kT)} e^{(C|V_{STR}|)} \tag{6.6}$$

where n is found to be near 1/4 for the Silicon-SiO_2 system, C is a fitting parameter, and E_a is the activation energy extracted from an Arrhenius plot [13]. When ΔV_{TH} is dominated by state creation mechanisms the $\log_{10}(\Delta V_{TH})$ vs $\log_{10}(t_{STR})$ will exhibit linear behavior. At a given t_{STR}, ΔV_{TH} due to state creation will have an exponential dependence on V_{STR} and also $1/T_{STR}$ [13].

6.1.3 Prior Work

Past studies on the stability of ZnO TFTs have indicated threshold voltage shifts with the same polarity as the gate bias stress voltage (V_{STR}) that increase with time [18, 59, 22]. Reports on the trends of S with time (t_{STR}) and V_{STR} are varied, but indicate S is unchanged below a certain V_{STR} and will degrade with time above this value. Cross reports S values that initially increase with time, but above 10^3 seconds S decreases. Because S is strongly correlated to interface state charge, this result hints there is more than one physical mechanism at play governing interface characteristics. Ability to recover pre-stress characteristics with and without post-stress treatments has also been reported; In different cases ΔV_{TH} has been reported to spontaneously recover in ~1 hour [18], with 200 ^oC anneal for 2 hours [22], or not at all [59]. The ease in which pre-stress V_{TH} can be recovered has been used to attribute an instability mechanism. For example, spontaneous recovery requires no bias or temperature perturbation so the mechanism is thought to be carrier traps at or near the semiconductor-oxide interface that would require low energy to de-trap, but ΔV_{TH} where recovery is only achieved with long high-temperature anneals is thought to be caused by charge state creation in the semiconductor or oxide, a mechanism that requires much more energy. In addition, a number of studies focusing on stability with respect to elemental ratio have been reported [24, 36].

Only one reported study has investigated the instabilities of ZnO TFTs across a range of temperatures [17] and none have investigated ZnO TFTs with high-k HfO_2 dielectrics. Further investigation is desired to both understand the device instability behavior dependence on temperature and gate-bias and to determine the physical origins governing the instabilities in this important material system. In this Chapter, the instabilities of ZnO/HfO_2 TFTs are studied by BTS investigation.

6.2 Sample Preparation

The devices used in this study were described in Chapter IV [t_{ZnO} = 47 nm, t_{HfO_2} = 30 nm]. All of the TFTs used in this study were from the same fabrication sample. After TFT fabrication, as described in Chapter IV, the sample was coated with 3 μm of Shipley 1827 Photoresist, diced using a ADT 7100 Dicing Saw, and cleaned in Acetone and IPA. This was done so that TFTs from the exact same fabrication run could be compared at different temperatures and applied biases, without having to subject all TFTs to all temperatures.

6.3 Testing

BTS testing was carried out using a Keithley 4200 SCS attached to a Desert Cyrogenics Temperature Controlled Probe Station. Each die was brought to the desired temperature, pre-tested, and then gate bias stress voltage was applied for up to 10^4 seconds. Stress bias was periodically removed in order to obtain TFT parameters.

The BTS independent variables are applied gate bias (V_{STR}), sample temperature (T_{STR}), and time (t_{STR}). Three values each for V_{STR} and T_{STR} were chosen so that trends could be evaluated by more than two points. V_{STR} values were chosen to be ± 5, ± 7.5, and ± 10 V because shifts in voltage characteristics were witnessed at 5 and

8 volts in MIS-C devices of the same material stack. After a few devices failed during the 10^4 stress tests at V_{STR} =10 V, 9 V was chosen as a replacement. Initial T_{STR} values were chosen to be 300, 320, and 340 Kelvin because changes were witnessed at room temperature. t_{STR} was chosen to be 10^4 seconds due to overwhelming use of this value in reported BTS studies.

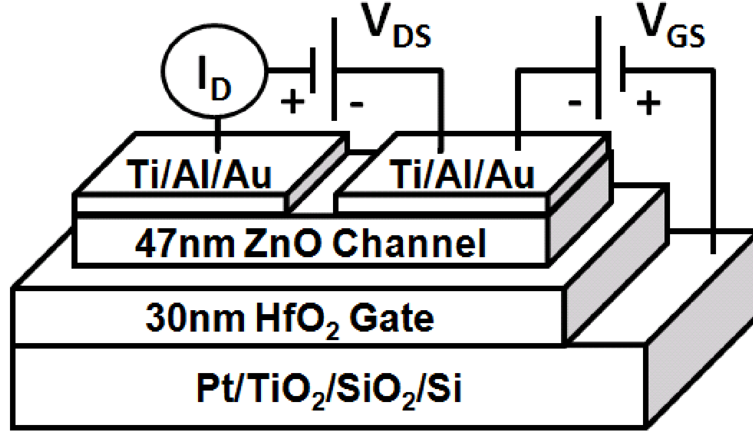
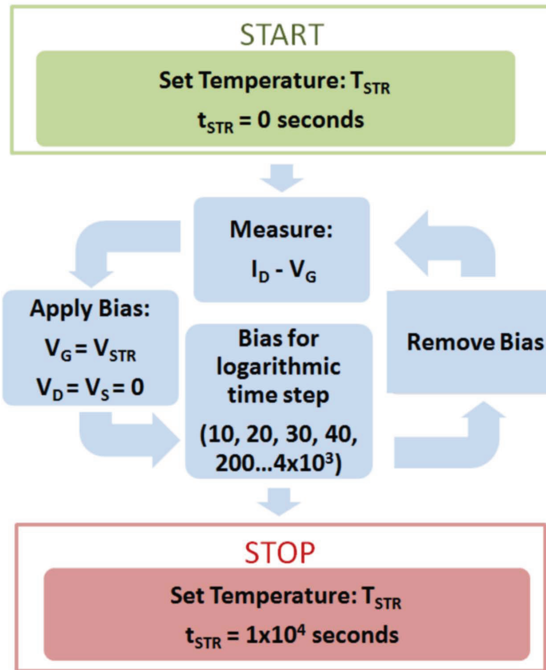


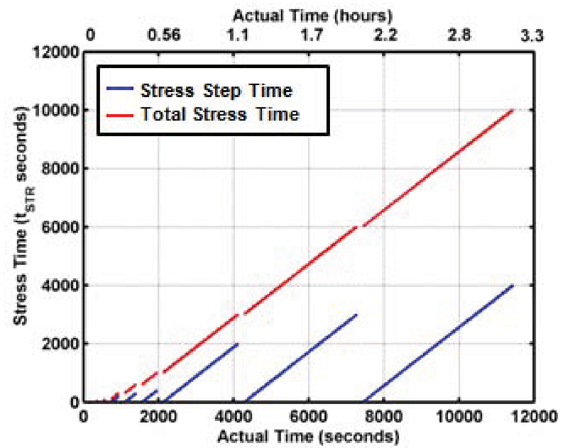
Figure 6.3: Schematic of HfO_2/ZnO TFT and biasing scheme for applied bias stress $V_{GS} = V_{STR}$ and $V_{DS} = 0$V.

The TFTs were first brought to T_{STR} and then a pre-test I_D-V_G transfer curve was measured, which served as the zero time case ($t_{STR} = 0$). The devices were then biased as seen in Figure 6.3 with $V_{GS} = V_{STR}$ and $V_{DS} = 0$ V for 10^4 seconds. Stress-bias was stopped at 10, 30, 60, 100, 300, 600, 1000, 3000, 6000, and 10000 seconds so that TFT transfer characteristics could be re-measured. During TFT transfer curve measurement, V_G was elevated to a to a magnitude greater than $|V_{STR}|$. A schematic flow chart of the BTS testing process can be seen in Figure 6.4(a). A graphical depiction of the accumulated stress time over the course of BTS testing can be seen in Figure 6.4(b).

V_{TH} and μ_{FE} were extracted from a linear fit of $\sqrt{I_{DS}}$ vs V_{GS} in the TFT saturation region. Typically a linear fit from 90% to 10% of $\sqrt{I_{DS}}$ is used to extract TFT parameters, but due to the shifting transfer curve and requirement to keep V_{GS} below



(a)



(b)

Figure 6.4: BTS Measurement Plan. (a) Schematic flow of BTS testing at one V_{STR}, T_{STR} value. Analyzing data over many V_{STR}, T_{STR} data pairs can help understand the mechanisms governing BTS instabilities. (b) Graphical depiction of BTS measurement plan. Each blue line represents the beginning and end of one step in the BTS process. The red lines represent the total stress time of the device (t_{STR}).

V_{STR}, a fixed $\sqrt{I_{DS}}$ window was used to extract all parameters so that they could be compared across variable t_{STR}, V_{STR}, and T_{STR} [22]. S was calculated by a linear fit to the subthreshold current from 0.6 to 3.6 decades of I_D above I_{D-min}. The change in a given figure of merit value over the course of BTS testing is signified by the Δ symbol which indicates the value is in reference to the pre-test value. An example can be seen for calculating ΔV_{TH} in Equation 6.7.

$$\Delta V_{TH}(t_{STR}) = [V_{TH}\,(t_{STR}) - V_{TH}\,(t_{STR} = 0)] \tag{6.7}$$

6.4 Positive (gate) Bias-Temperature Instability (PBTI)

ZnO TFTs with 30nm HfO_2 gate dielectrics were subjected to positive V_{STR} values to ascertain the positive bias-temperature instability (PBTI) characteristics.

Stress under positive gate bias results in a clear trend of transfer curves shifting along the voltage axis to more positive voltages over time. An example family of PBTI transfer curves can be seen in Figure 6.5 for T_{STR} = 300 K and V_{STR}= 5 V. The transfer curves shift monotonically with time, the rate of which has a dependence on both T_{STR} and with V_{STR}.

ΔV_{TH} increases linearly with logarithmic time [$\log_{10}(t_{STR})$], while no distinguishable trends are observed for extracted values of $\Delta\mu_{FE}$ or S. $\Delta\mu_{FE}$ and absolute value of S with t_{STR} can be seen along with ΔV_{TH} in Figure 6.6. The observed PBTI trends of V_{TH} will be further discussed in Section 6.4.2.

When PBTI data is analyzed across all stress conditions ΔV_{TH} is the only figure of merit exhibiting coherent changes. ΔV_{TH} data is linear vs $\log_{10}(t_{STR})$ indicating charge trapping is the dominant mechanism causing ΔV_{TH} rather than charge state creation as discussed in Sections 6.1.1 and 6.1.2.

There is no clear temperature dependence of ΔV_{TH} over the temperature range studied as shown in Figure 6.7. Examining ΔV_{TH} values at 10^4 seconds and analyzing

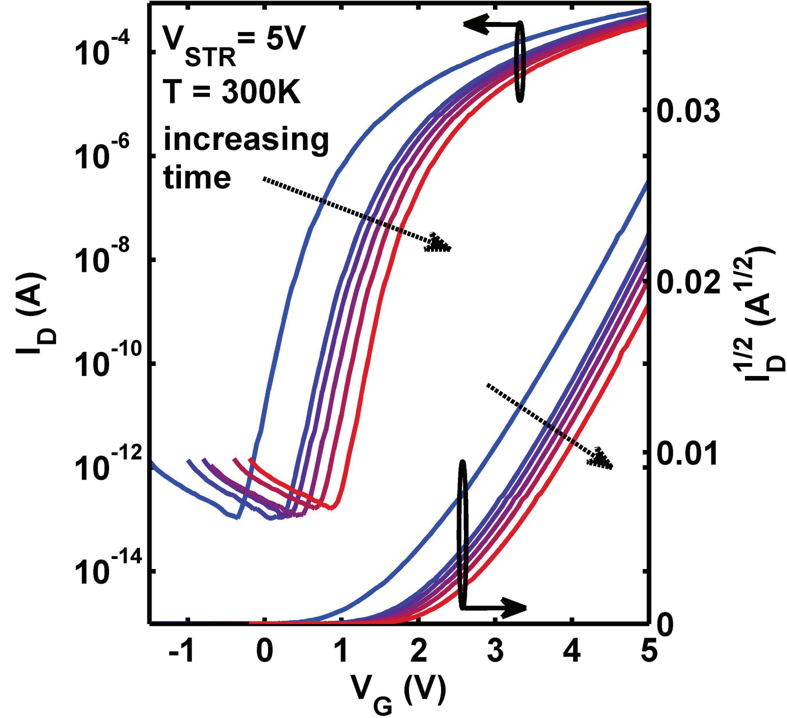


Figure 6.5: Series of transfer ($I_D - V_{GS}$) characteristics under $V_{STR} = 5$ V at $T_{STR} =$ 300 K.

the trends with temperature, the 9 and 7.5 volt cases show no trend with temperature and the 5 volt values increase less than a factor of 2 with temperature. This lack of temperature dependence supports the hypothesis of charge trapping as a cause for PBTI, as tunneling is a temperature independent process [71].

There is also a weak dependence of ΔV_{TH} on 1/V$_{STR}$ as shown in Figure 6.8. An exponential dependence of ΔV_{TH} on 1/V$_{STR}$ is expected for charge trapping in the oxide, but only a weak relationship can be seen from the results of this study, which perhaps lack the range and resolution for 1/V$_{STR}$ analysis. Future studies across a wider range of temperatures and stress bias will improve understanding of this relationship.

The data for ΔV_{TH} vs t$_{STR}$ across all positive stress values can be seen in Figure 6.9

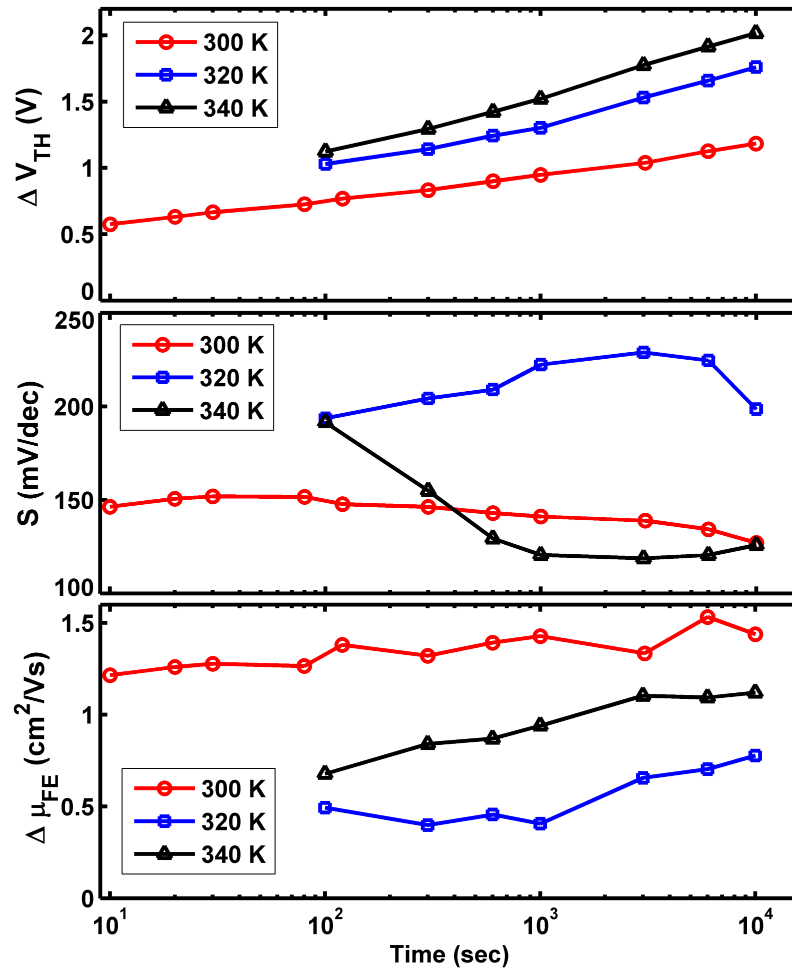


Figure 6.6: Change in ΔV_{TH}, S, and $\Delta\mu_{FE}$ over course of Positive BTS testing

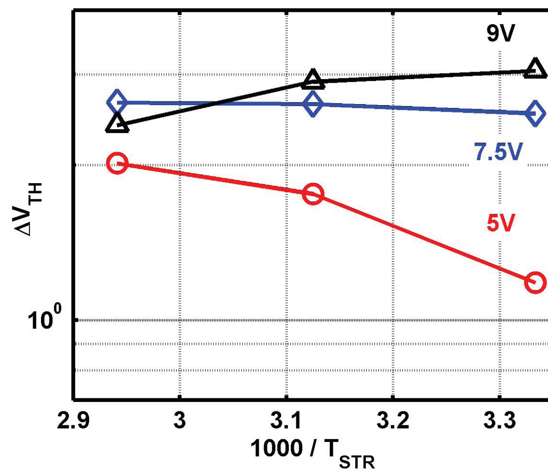


Figure 6.7: ΔV_{TH} $(t_{STR} = 10^4 sec)$ vs $^{1000}/_{T_{STR}}$

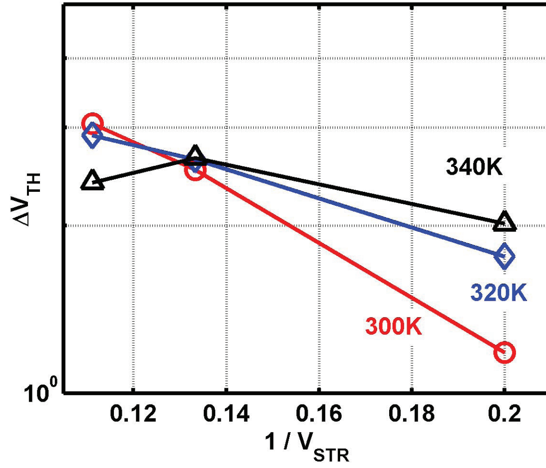


Figure 6.8: $\Delta V_{TH}\,(t_{STR} = 10^4 sec)$ vs $^{1000}/_{T_{STR}}$

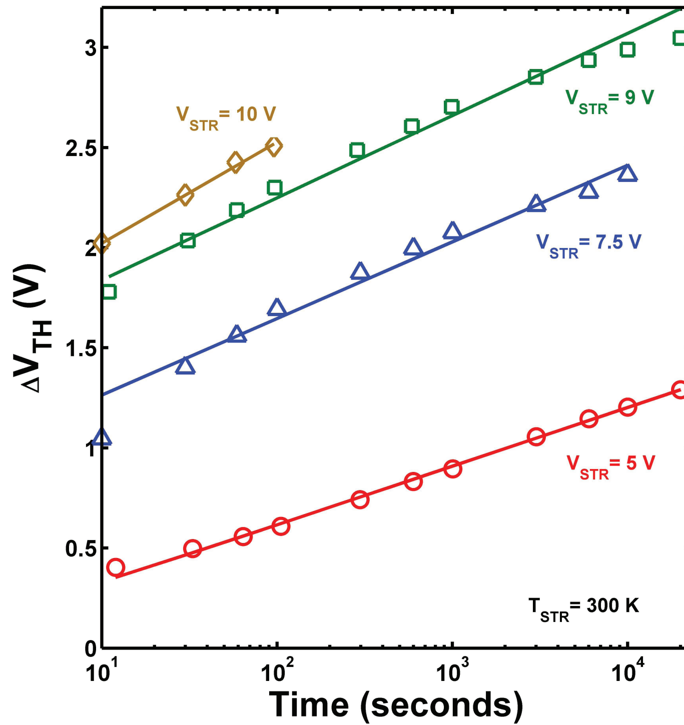


Figure 6.9: ΔV_{TH} vs t_{STR}. Trend typical of device influenced by charge trapping in dielectric. Trend-lines calculated via Equation 6.5

6.4.1 Recovery Results

Directly after a BTS measurement was complete, the device was left at temperature with the probes contacting the device and the SMUs disabled. A transfer curve was periodically measured to monitor how quickly the device performance returned to pre-test characteristics, termed 'recovery'. Recovery characteristics can reveal information about instability mechanisms as discussed in Section 6.1.3.

Typical PBTI recovery of ΔV_{TH} to a value of 50% was observed within several hours as seen in Figure 6.10.

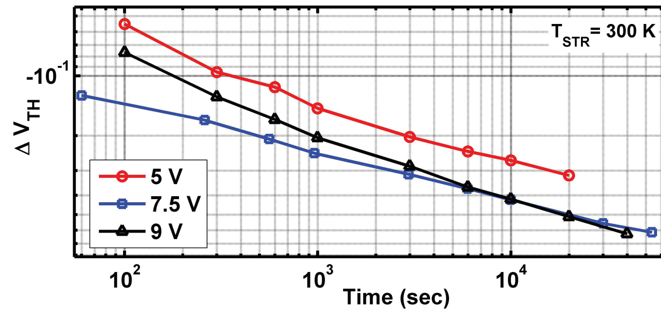


Figure 6.10: ΔV_{TH} recovery vs t_{STR}.

Here, recovery results for ZnO/HfO_2 indicate traps deep in the dielectric with long emission times are contributing to PBTI. A device suffering interface charge trapping would be expected to recover to near-original performance much faster than witnessed [17].

In order to investigate the temperature dependence of recovery, several devices were stressed at 10 volts for 100 seconds, at different temperatures. The recovery characteristics were then recorded for 10^4 seconds as shown in Figure 6.11.

From the temperature dependent recovery data, we see a trend where the slope of recovery becomes steeper with temperature. This could be explained by a two stage recovery process vs simply tunneling. Figure 6.12 shows such a process where a phonon could excite a trapped carrier to an energy level where tunneling into the conduction band is possible.

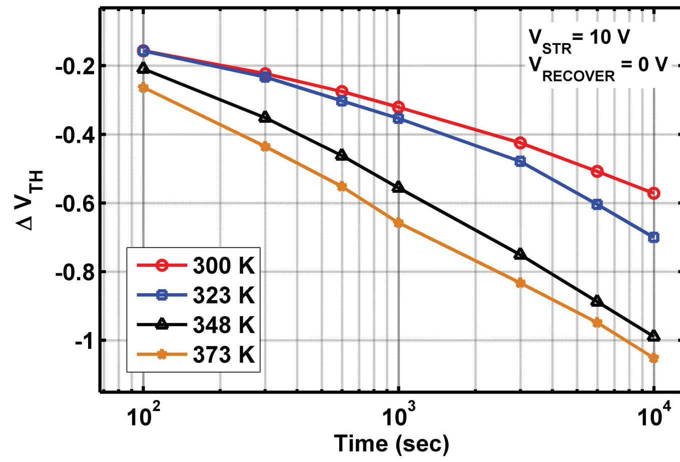


Figure 6.11: ΔV_{TH} recovery vs t$_{STR}$.

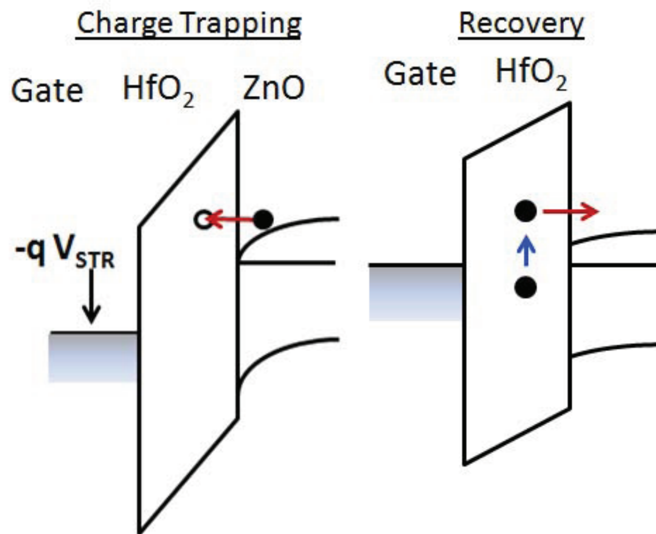


Figure 6.12: Band diagram representation of ΔV_{TH} stress tunneling (left) and two-stage thermally-assisted de-trapping (right).

6.4.2 PBTI Analysis

The only performance parameter trending with positive gate bias or temperature is V_{TH}. Lack of coherent trend with S or μ_{FE} leads to the conclusion that PBTI is not governed by mechanisms related to interface states, typically linked to changes in S, or charges in semiconductor band edge states typically associated with μ_{FE} [12, 48]. Analysis of ΔV_{TH} shows a logarithmic dependence on time, as shown in Figure 6.9. This trend has been linked to charge trapping in a semiconductor/dielectric system (Section 6.1.1).

As an added point of reference, PBTI testing was conducted on ZnO TFTs with SiO_2 gate dielectrics to discern the role of the dielectric. From the results, shown in Figure 6.13, there is negligible PBTI ΔV_{TH} in the ZnO/SiO_2 system, further pointing to the dielectric as the source in ZnO/HfO_2 devices.

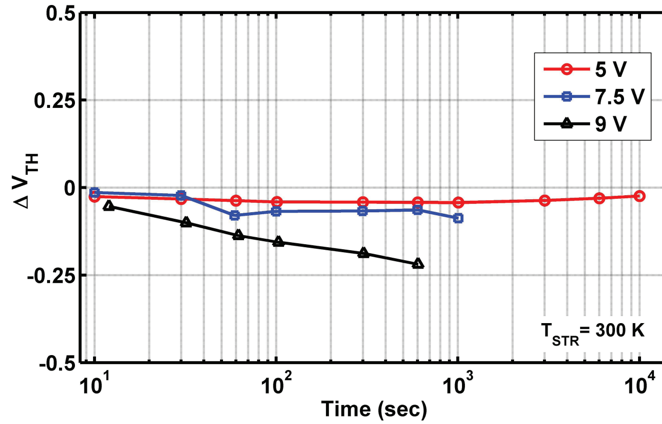


Figure 6.13: ΔV_{TH} vs t_{STR} for ZnO TFT with SiO_2 gate dielectric. Lack of ΔV_{TH} indicates gate dielectric is responsible for PBTI results reported in Section 6.4.

ΔV_{TH} PBTI is believed to be caused by charge tunneling into the gate dielectric, in this section we present a method that fully describes the experimental data, is based on real physical parameters, and allows the extraction of the dielectric trap density. A new method is necessary for several reasons:

- Cannot extract N_{TR} from popularly used Equation 6.5

- Existing model does not take into account that ΔV_{TH} is a function of the spacial characteristics of charge, Q(t,x), and charge distance from the interface, x.

- Popular solution is not based on physical parameters.

As a result we present a method that is based on Ross and Wallmark's work, but includes ΔV_{TH} dependance on spacial characteristics of gate oxide trapped charge, is a function of real physical parameters [carrier concentration at the interface, tunneling parameter (function of gate potential), and trap density], and allows the determination of N_{tr}.

As indicated, this method more accurately defines ΔV_{TH} according to Muller and Kamins [53]

$$\Delta V_{TH} = \frac{-1}{C_{ox}} \int_{0}^{x_{ox}} \frac{x}{x_{ox}} Q(x,t)dx \tag{6.8}$$

The next steps follow Ross and Wallmark.

1. Charge is assumed to have the time independent tunneling probability

$$Q(x,t) = \omega(x)dt = \omega_0 e^{(-x/\lambda)}dt \tag{6.9}$$

2. It is assumed that traps in the gate oxide are distributed uniformly throughtout its thickness at a single energy level.

3. It is assumed that if a trap is available at slice x' in the dielectric the charge will be trapped there according to $\omega(x)$

4. Once the trap occupation at a given slice of x, Q(x'), reaches the dielectric trap density per slice [$N'_{tr} = N_{tr}$/(slice thickness)] no more charge will accumulate in that slice.

$$Q(x') \leq N'_{tr}(x') = N_{tr}/(\text{slice thickness}) \tag{6.10}$$

5. At each time step, the calculation will compute the additional charge to be added along x and update Q(t,x).

6. Then ΔV_{TH} is calculated according to Equation 6.8.

7. In this way, Q(t,x) and ΔV_{TH} are each calculated over the duration of the stress

8. This method can then be used to fit experimental data with the input/fiting values:

   ω_0: Channel carrier concentration at the interface

   λ: Tunneling parameter, which is directly related to potential at interface and thus applied gate bias.

   N_{tr}: Gate dielectric volume trap density

The numerical method fit to experimental data can be seen in Figure 6.14.

The subtle breaks from linear vs $\log_{10}(t_{STR})$ can be seen as V_{STR} goes from 5 V (small tunneling parameter and supply cross section) to 9 V (large tunneling parameter and supply cross section). In the 9 volt case, the slope of the curve begins to visibly drop over time due to the fact that charge far away from the interface does not contribute equally to ΔV_{TH}. If the experiment were taken to longer times or higher V_{STR} values, we would see the slope of ΔV_{TH} go to zero as the tunneling charge eventually saturates the entire dielectric.

With good fits, we can use our experimental data to discover real attributes of our system. Table 6.1 shows fits for our tunneling parameters, supply cross section, and trap density.

As predicted, we find a constant N_{tr} which is expected because it is a material parameter. We find that λ and ω_0 scale with applied voltage which is expected

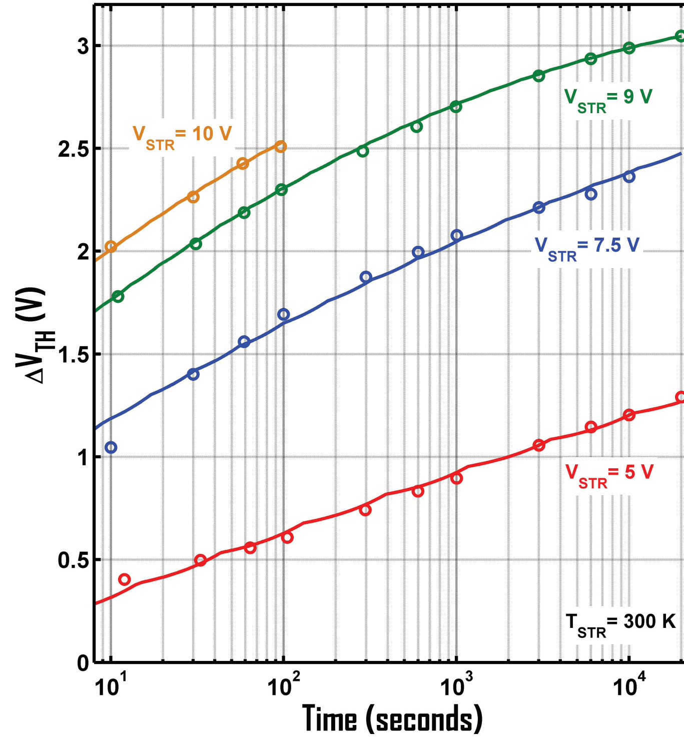


Figure 6.14: ZnO TFT with HfO_2 gate dielectric ΔV_{TH} vs t_{STR} data for different V_{STR} values.

Parameter	V_{STR} Values			
	5	7.5	9	10
N_{tr} (x10^{18} cm^{-3})	7.5	7.5	7.5	7.5
λ (Å)	7	13	19	21
ω_0 (x10^{11} cm^{-2})	1.2	21	37	56

Table 6.1: Electrical Properties of ZnO TFT with 30 nm HfO_2 gate dielectric

because tunneling parameter will increase with potential energy and more carriers will accumulate at the channel dielectric interface with higher positive gate bias.

It is important to note that since N_{tr} is 7.5 x 10^{18} cm^{-3} and the assumption of uniform charge distribution was made, the linear distance any trap is from another trap is $1/N_{tr}^{1/3} \approx 5$ nm. Evaluating the tunneling probability by the Wentzel-Kramers-Brillouin (WKB) approximation

$$T \propto \exp\left(-2L\sqrt{\frac{2mV_b}{\hbar}}\right) \tag{6.11}$$

where T is the tunneling probability, L is the distance into the potential barrier, m is the mass of an electron, and V_b is the barrier height [84] gives an extremely low tunneling probability for 5 nm. With this in mind electron tunneling into traps much farther than the tunneling parameter might require multiple 'tunneling actions' where carriers populate traps near the interface and then tunnel into successively farther traps with time. Making these assumptions about the system would change the source and tunneling functions such that a modification to the method above would result. Such a method will not be considered in this work.

In conclusion, PBTI results for ZnO TFTs with HfO_2 gate dielectrics have been shown. There is overwhelming evidence that PBTI is caused by charge tunneling into fixed traps within the HfO_2. Finally a method to model experimental data and extract real, physical parameters, such as dielectric trap density has been presented.

6.5 Negative (gate) Bias-Temperature Instability (NBTI)

Disclaimer: Most NBTI data presented in this section are extracted values from curves swept from some negative gate voltage to +1.5 volts. Early results showed that sweeping to higher gate voltages introduced PBTI effects which could confound NBTI results. Consequently, the value V_T is used to track shifts in I_D-V_G characteristics,

which is defined as the voltage at which I_D = 1 nA. Similarly μ_{FE} values were not extracted in this max(V_G) = 1.5 V case.

Stress under negative gate bias results in a shift of transfer curves to negative voltages over time as shown in Figure 6.15. In addition to shifts in V_T, the subthreshold

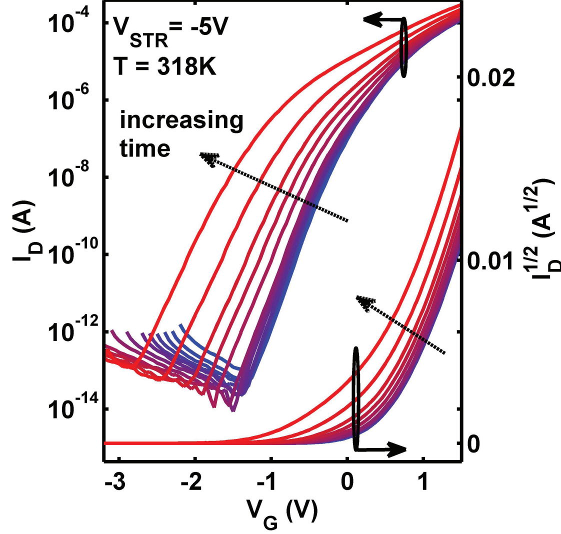


Figure 6.15: NBTI family of curves for V_{STR}=-7.5 V, T_{STR}=366 K case.

slope and channel mobility appear to have a recognizable NBTI. Extracted values of V_T, μ_{FE}, and S versus stress time at three different temperatures (V_{STR} = -5 V) are shown in Figure 6.16.

V_T shifts in the negative voltage direction with time. Initially V_T trends with a power law relationship, but for each curve, at some point in time, the slope breaks from power law and assumes less change per unit time than power law. The change is accelerated with increased T_{STR} and the power law 'break point' occurs in shorter times with increasing temperature. ΔS, similarly, shows temporal characteristics with two types of change. Initially, ΔS increases with $\log_{10}(t_{STR})$, but at some time (T_{pk}) values peak and begin to decline with additional time. ΔS also has peaking behavior with temperature. From a temperature standpoint, values rise until T_{STR} = 348 K and then drop. The bottom plot in Figure 6.16 shows μ_{FE} data from an

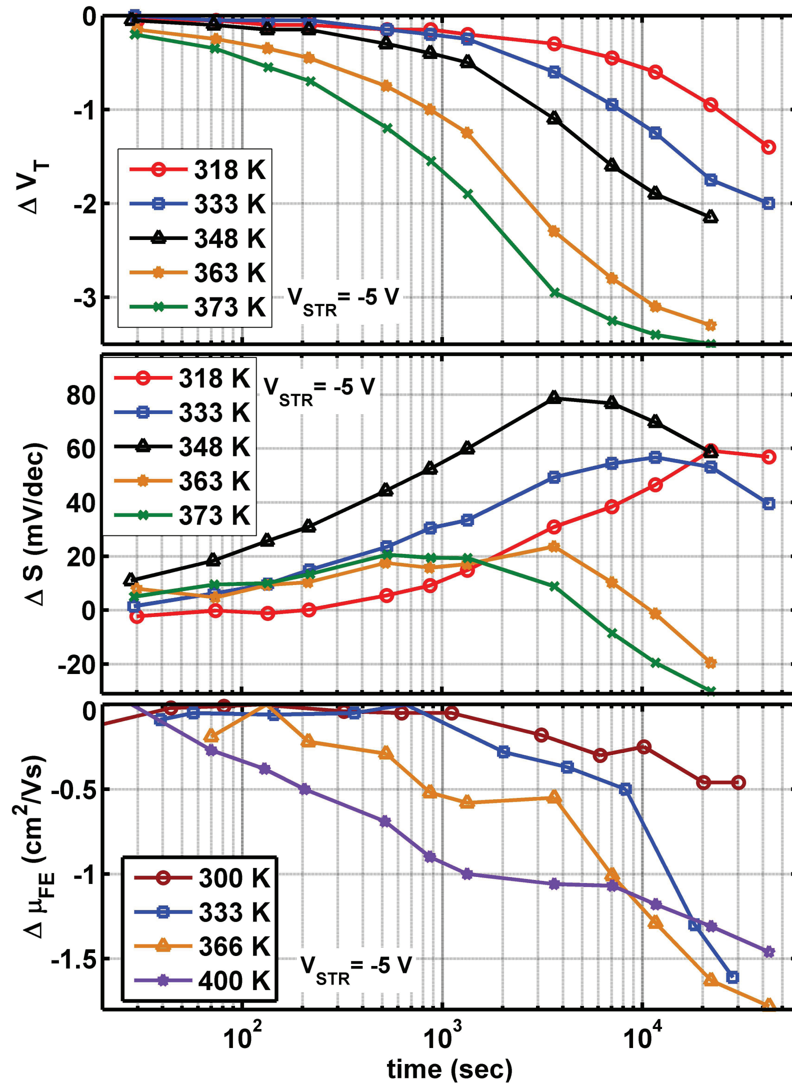


Figure 6.16: TFT performance parameters plotted vs t_{STR}. V_{STR}=-5 V, variable T_{STR}.

initial NBTI study where V_G was swept to 5 volts. It is important to note that μ_{FE} does decrease with time and temperature under NBTI conditions. Since this is not a trend witnessed in the PBTI case, it is likely a real effect and not the product of PBTI confounding. In the case of NBTI, there is clear temperature dependence. Figure 6.17 shows -ΔV_{TH} from an initial NBTI study showing a clear exponential relationship with $1/T_{STR}$. Not only is there a clear temperature relationship,there is no V_{STR} dependence whatsoever.

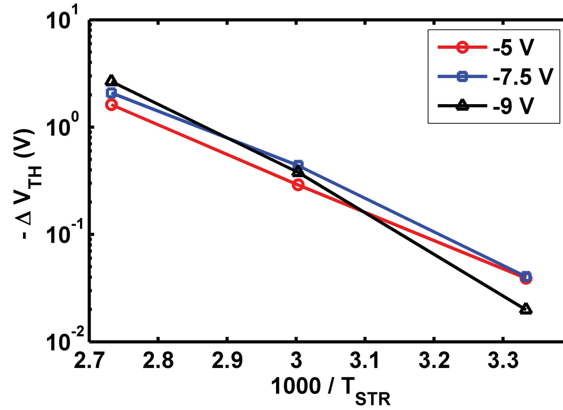


Figure 6.17: $-\Delta V_{TH}$(t_{STR}=1.4x10^4 sec) vs $1/T_{STR}$, variable V_{STR}.

6.5.1 NBTI Analysis

From NBTI results, ΔV_T is observed to initially follow an exponential trend with logarithmic time. This is indicative of a system under the influence of charge state creation. In this section the trends of various parameters with t_{STR}, T_{STR}, and V_{STR} will be analyzed to characterize and understand the sources of NBTI mechanisms.

6.5.1.1 ΔV_T

In order to characterize NBTI results, data will be analyzed via a model used to describe temperature and field dependent NBTI due to charge state creation in polycrystalline Silicon. As discussed in Section 6.1.2 the model developed takes the

following form

$$\Delta V_T \propto t^n e^{(-Ea/kT)} e^{(C|V_{STR}|)} \tag{6.12}$$

where ΔV_T time dependence is exponential with coefficient, n, temperature dependence has an arrhenius dependence on temperature with an activation energy, E_a, and an exponential dependence on stress voltage with a coefficient, C [13].

As shown in Figure 6.17 there is no dependence on V_{STR}. Plotting $\log_{10}(\Delta V_T)$ vs $\log_{10}(t_{STR})$ for various T_{STR} values it is easy to see that the exponential slope does not change with T_{STR} and thus a singular n value can describe the system (Figure 6.18). n was determined to be 0.6.

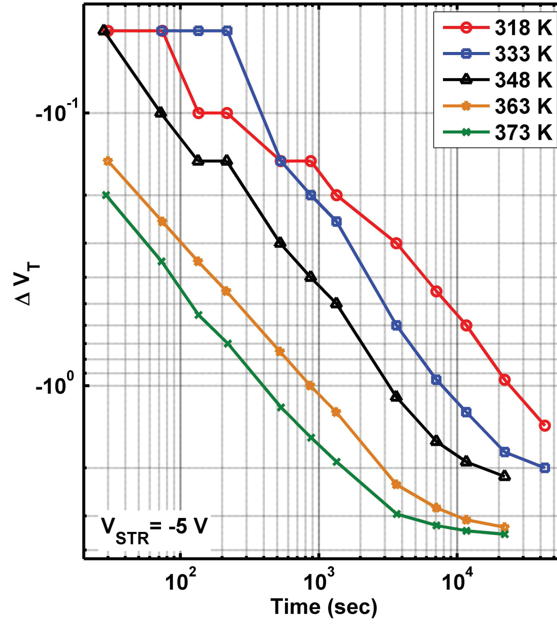


Figure 6.18: $-\Delta V_{TH}$ vs T_{STR}, variable T_{STR}.

The temperature dependence was found via a fit to the Arrhenius relation as described in Equation 6.13

$$-\Delta V_T = -\alpha e^{-Ea/kT_{STR}} = -\beta t^{0.6} e^{-Ea/kT_{STR}} \tag{6.13}$$

where α and β are pre-exponential fitting parameters and k is Boltzmann's constant.

Figure 6.19 shows the extracted E_a to be 0.47 eV.

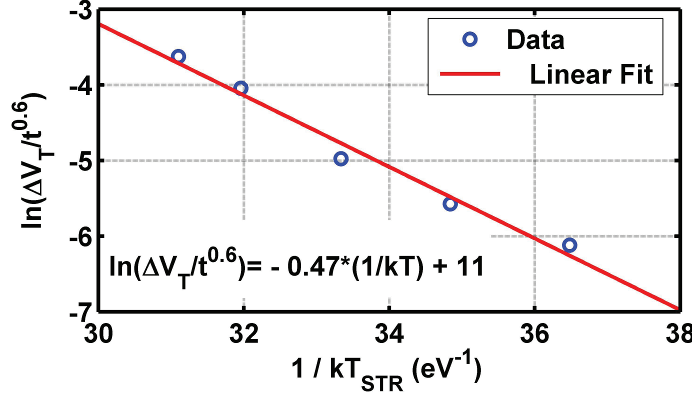


Figure 6.19: Arrhenius plot. $-\Delta V_T$ hold an Arrhenius relationship with T_{STR}

With temporal and temperature dependence revealed, Equation 6.14, based on charge state creation in a polycrystalline semiconductor system, describes the experimental data well as shown in Figure 6.20.

$$\Delta V_T \simeq \beta t^{0.6} e^{(-0.47/kT)}$$
$$\beta = 5.8x10^4 \text{V/sec} \quad (6.14)$$

6.5.1.2 ΔS

Figure 6.16 shows the unique qualities of the ΔS with time and temperature. With time ΔS initially rises, then peaks, and begins to decrease with additional time. With temperature, ΔS also appears to initially rise, with peak values occurring for the 348K curve and then values decreasing again. The time at which ΔS peaks for each temperature appears inversely proportional to temperature. This relationship seems to correlate with of the time relationship at which the slope of -ΔV_T begins to decrease. It must also be noted that both ΔS and -ΔV_T have temporal shapes with two regions of slope. Perhaps the two are related. Since ΔS is linked to interface charge and -ΔV_T showed charge creation characteristics, the theory that interface charge creation is playing a role in governing ZnO/HfO_2 NBTI is suggested.

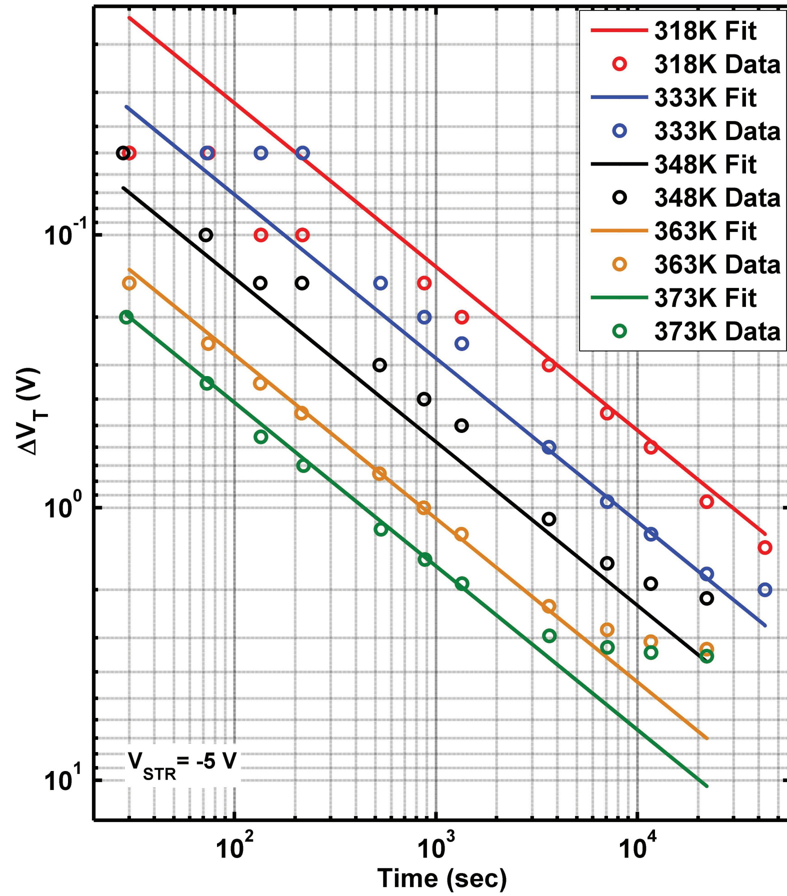


Figure 6.20: ΔV_T vs t_{STR} over range of T_{STR} values with fit to model based on charge state creation.