

**DESIGN TECHNIQUES FOR LOG BASED CLOSED-LOOP  
NEUROSTIMULATION SYSTEM-ON-CHIP**

by

Hyo Gyuem Rhew

A dissertation submitted in partial fulfillment  
of the requirements for the degree of  
Doctoral of Philosophy  
(Electrical Engineering)  
in The University of Michigan  
2012

Doctoral Committee:

Professor Michael P. Flynn, Chair  
Assistant Professor Parag G. Patil  
Assistant Professor David D. Wentzloff  
Assistant Professor Zhengya Zhang

© Hyo Gyuem Rhew

---

All rights reserved

2012

*To Mom, Dad, my sister and fianc é for their endless love...*

## **Acknowledgements**

I would like to express my sincere gratitude to my friends, colleagues, advisors and family for their care and support during my graduate study in Ann Arbor. First, I would like to thank my advisor Prof. Michael Flynn for introducing me to the research area and for guiding and encouraging me through the course of the research. I must confess that I am very fortunate to have an advisor like Prof. Flynn. Throughout the years of my graduate life he has not only been a good research advisor but also given me personal advice as a great mentor. I would also like to thank the rest of my committee members: Prof. Parag G. Patil for many discussions we had to design and refine this doctoral work, Prof. David D. Wentzloff for his invaluable feedback during all years of my graduate study and Prof. Zhengya Zhang for his interest and support for this research and helping me write a better dissertation.

I would like to thank Mr. Ram Sadhwani and Mr. Adil Kidwai from Intel for their great mentoring. I would also like to thank many people at Intel Corporation including Dr. Hasnain Lakdawala, Mr. Benjamin Jann, Mr. Sunny Sharma, Dr. Stephen Bruss, Dr. Satwik Patnaik, Dr. Ning Zhang, Dr. Thomas Brown, and Dr. Khartik Natarajan for sharing their time and expertise. I would also like to thank many people at Mediatek Incorporation including Mr. Michael Ashburn, Mr. Stacy Ho, Dr. Patrick Riehl, Dr. Jose Silva, and Dr. Ayman Shabra.

I would like to acknowledge the help of all EECS department staffs, especially Mrs. Beth Stalnaker, Mrs. Deborah Swartz and Mrs. Francis Doman. They provided tremendous amount of support while I was going through all kind of issues related to degree progress. I must express my gratitude to Joel VanLaven for supporting CAD systems. I would never be able to write these lines without their continuous support.

Much thanks must go to all of my former and current members of Prof. Flynn's group for their assistance in research and their heartfelt friendship: Dr. Sunghyun Park, Dr. Ivan Bogue, Dr. Dan Shi, Dr. JunYoung Park, Dr. Mark Ferriss, Dr. Joshua Kang, Dr. Jongwoo Lee, Dr. Shahrzad Naraghi, Andres Tamez, Dr. Chun Lee, Jorge Pernillo, Dr. David Lin, Dr. Li Li, Nick Collins, Jeffrey Fredenburg, Hyungil Chae, Mohammad Mahdi Ghahramani, Jaehun Jeong, Aaron Rocca, Chunyang Zhai, Yong Lim, and Batuhan Dayanik. I would like to thank especially Jaehun Jeong for his great work designing log-scale digital circuits. This thesis work could not be finished if it weren't for his invaluable help. I would also like to express my gratitude to my friends from all over the world I have made at Michigan for sharing their time with me which made my life in Michigan always happy and enjoyable. I would also like to thank people at the Eden Presbyterian Church of Oregon for their care and love.

I am very grateful to the Samsung Scholarship Foundation for providing me with a fellowship for my Ph.D. study. I also thank the Catalyst Foundation for supporting this work.

Most importantly, I want to say my thankfulness to my wonderful family and my fiancé My father, mother, sister, and Jiyeon believed in me with their endless love, support, encouragement and prayer. Above all I thank God for His grace and love.

## Table of Contents

<b>Dedication .....</b>	<b>ii</b>
<b>Acknowledgements .....</b>	<b>iii</b>
<b>List of Figures.....</b>	<b>vii</b>
<b>List of Tables .....</b>	<b>xi</b>
<b>List of Appendices.....</b>	<b>xii</b>
<b>List of Abbreviations .....</b>	<b>xiii</b>
<b>Abstract.....</b>	<b>xv</b>
<b>Chapter I.....</b>	<b>1</b>
<b>1. Introduction.....</b>	<b>1</b>
1.1. Essential Tremor .....	1
1.2. Dystonia .....	3
1.3. Parkinson’s Disease .....	6
1.4. Epilepsy .....	8
1.5. Deep Brain Stimulation (DBS).....	10
1.6. Closed-loop DBS .....	13
1.7. Dissertation outline .....	16
<b>2. Design techniques for recording front-end.....</b>	<b>18</b>
2.1. LNA .....	18
2.2. Pipeline logarithmic ADC .....	24

<b>3.</b>	<b>Design techniques for a log-domain digital processing unit.....</b>	<b>35</b>
3.1.	Logarithmic digital signal process.....	35
3.2.	Logarithmic digital filter.....	38
3.3.	Closed-loop stimulation controller .....	41
<b>4.</b>	<b>Design techniques for a power management block.....</b>	<b>44</b>
4.1.	RF-DC converter .....	45
4.2.	LDO .....	46
4.3.	Bandgap voltage reference .....	48
<b>5.</b>	<b>Design techniques for other building blocks: current stimulator, clock generator, and RF transceiver .....</b>	<b>50</b>
5.1.	Current stimulator.....	50
5.2.	Clock generator.....	52
5.3.	RF Transceiver.....	54
<b>6.</b>	<b>Prototype system and performance measurements.....</b>	<b>57</b>
6.1.	Proposed closed-loop DBS SoC architecture .....	57
6.2.	Prototype measurement results .....	61
<b>7.</b>	<b>Conclusions.....</b>	<b>70</b>
7.1.	Summary of the prototype performance .....	71
7.2.	Contributions .....	73
7.3.	Future work.....	74
	<b>Appendices.....</b>	<b>76</b>
	<b>Bibliography .....</b>	<b>101</b>

## List of Figures

Figure 1.1: A patient with essential tremor drawing the Archimedes spiral [6].....	2
Figure 1.2: A person with medication induced dystonia. ....	4
Figure 1.3: Muhammad Ali and Michael J. Fox.....	6
Figure 1.4: Diminished substantia nigra in a patient with Parkinson’s Disease [13]. ....	7
Figure 1.5: Woman with epileptic seizure. ....	9
Figure 1.6: Implantation of DBS system [23].....	11
Figure 1.7: Activa RC neurostimulator for Medtronic DBS therapy [25].....	12
Figure 1.8: Titrating stimulation using a handheld programmer from Medtronic [28]. ...	14
Figure 2.1: A single-ended representation of the schematic of a band-pass amplifier. ....	19
Figure 2.2: Simulated frequency response of the general band-pass amplifier. ....	20
Figure 2.3: A differential representation of the schematic of a two-stage band-pass amplifier.....	22
Figure 2.4: Simulated frequency response of the designed two-stage band-pass LNA....	23
Figure 2.5: Coding scheme of a 5-bit logarithmic ADC with $B=10$ (left) and output from sinusoidal input shown with dead-zone effect (right).....	26
Figure 2.6: Pre-conversion of input to eliminate the log dead-zone.....	27
Figure 2.7: Overall architecture of the 8-bit pipeline logarithmic ADC.....	28
Figure 2.8: Conceptual block diagram of the logarithmic 1.5-bit stage. ....	29
Figure 2.9: Residue plot of the logarithmic 1.5-bit stage with $B=10$ .....	29



Figure 2.10: Simplified schematic of SHA with $B=10$ .	31
Figure 2.11: Simplified schematic of a logarithmic 1.5-bit stage.	32
Figure 2.12: Schematic of bias circuits.	34
Figure 3.1: Lookup table usage decision.	37
Figure 3.2: Block diagram of digital logarithmic low-pass and high-pass filters.	38
Figure 3.3: Simulated output spectrums of the linear (left) and logarithmic (right) 15 <sup>th</sup> order FIR LPF.	39
Figure 3.4: Simulated output spectrums of the linear (left) and logarithmic (right) 15 <sup>th</sup> order FIR HPF.	40
Figure 3.5: Power consumption comparison of a linear-domain and a log-domain 10-bit FIR digital filters.	41
Figure 3.6: Flow diagram of the proposed closed-loop stimulation that uses LFP energy information as a feedback indicator.	42
Figure 3.7: Simulated transient input and output of the PI-controller with pre-recorded rat's neural data input.	43
Figure 4.1: Block diagram of the power management block of the closed-loop DBS system that generates both analog and digital supply voltages from a 915MHz carrier.	45
Figure 4.2: Schematic of the full-wave rectifier that generates unregulated $V_{DD}$ of 2.2 V from a 915MHz carrier.	46
Figure 4.3: Schematic of the LDO for analog domain voltage supply.	47
Figure 4.4: Schematic of bandgap reference circuits.	49
Figure 5.1: Simplified block diagram of 8-channel current stimulator.	51
Figure 5.2: Schematic of clock generator.	53

Figure 5.3: Block diagram of RF transceiver.....	55
Figure 5.4: Communication protocol for RF telemetry. ....	56
Figure 6.1: Overall system block diagram of the proposed log-based closed-loop DBS system. ....	58
Figure 6.2: Die micrograph of the prototype log-based closed-loop DBS system. ....	60
Figure 6.3: Measured DNL and INL of the designed AFE (4- <i>ch.</i> LNAs + log ADC). ....	61
Figure 6.4: Measured output spectrum of the designed AFE (4- <i>ch.</i> LNAs + log ADC)..	62
Figure 6.5: Measured frequency response of the designed recording path (AFE + digital log-filters). ....	63
Figure 6.6: Recorded output of the designed recording path (AFE + digital log-filters) with a pre-recorded neural signal from a rodent’s brain applied as input to the system. .	64
Figure 6.7: Measured stimulation current waveforms of low-current and high-current stimulation channels with 6.23 $k\Omega$ and 220 $\Omega$ respectively.....	65
Figure 6.8: Measured stimulation current waveforms of a high-current stimulation channel in closed-loop mode using LFP energy detection with a 220 $\Omega$ resistor load.....	66
Figure 6.9: Measured input impedance changed from backscatter modulation of the transceiver. ....	67
Figure 6.10: Measured output spectrum of the backscatter transceiver.....	68
Figure 6.11: Measured recovered data bit-stream from the backscatter transmitter.....	68
Figure A.1: IO pad of the closed-loop neurostimulation SoC prototype.....	78
Figure A.2: PCB schematic of the prototype. ....	82
Figure A.3: PCB photograph. ....	84

Figure B.4: Transceiver architecture with an on-chip transmission line link terminated with optimal resistance. ....	87
Figure B.5: Interleaved voltage-mode line drivers: A, B.....	88
Figure B.6: Block diagrams of 4b-to-1b serializer and 2b-to-1b serializer. ....	89
Figure B.7: Schematic of comparator of high-speed serial link. ....	90
Figure B.8: Schematic of comparator of low-power serial link.....	91
Figure B.9: Block diagrams of 1b-to-4b deserializer and 4b-to-1b deserializer.....	92
Figure B.10: Die micrographs of low-power type serial link (left) and high-speed type serial link (right). ....	94
Figure B.11: Measured energy-per-bit and data rates at 25°C.....	95
Figure B.12: Measured eye-diagram of the receive-end of the 10mm serial link with a GSG probe at 25°C.....	96
Figure B.13: Comparison of energy efficiency over bandwidth density with conventional bus schemes that utilize the same metal level (M9) at 1.2V <sub>DD</sub> and 25 °C. A crosstalk coefficient of 15% is assumed for the transmission line.....	98
Figure B.14: Comparison of energy efficiency over 16-bit transfer time with conventional bus schemes that utilize the same metal level (M9) at 1.2V <sub>DD</sub> and 25 °C.....	98

## List of Tables

Table 1.1: Treatment for essential tremor.....	3
Table 1.2: Treatment for dystonia.....	5
Table 1.3: Treatment for Parkinson’s disease.....	8
Table 1.4: Treatment for epilepsy.....	10
Table 2.1: Summary of the simulated performanc of the designed LNA at 40°C with 1.8V supply.....	24
Table 2.2: Voltage reference and gain settings in the logarithmic 8-bit ADC with $B=10$ .....	34
Table 4.1: Pass transistor dimensions and load capacitance values of the LDOs.....	48
Table 5.1: Summary of ranges of stimulation parameters.....	52
Table 6.1: Power breakdown of the prototype system.....	69
Table 7.1: Prototype performance summary.....	72
Table A.1: IO pad information of the closed-loop neurostimulation SoC prototype .....	78
Table A.2: Parts list for PCB .....	83
Table B.3: Designed transmission line characteristics .....	92
Table B.4: Designed transmission line characteristics .....	97
Table B.5: Performance comparison with recent works.....	100

## **List of Appendices**

Appendix A. Printed circuit board for the closed-loop neurostimulation SoC..... 77

Appendix B. A 22Gb/s, 10mm On-chip Serial Link over Lossy Transmission Line..... 85

## **List of Abbreviations**

ADC	Analog-to-digital converter
AFE	Analog Front-end
BER	Bit error rate
CMOS	Complementary metal-oxide semiconductor
CNS	Central nervous system
DAC	Digital-to-analog converter
dB	Decibel
DBS	Deep brain stimulation
DNL	Differential non-linearity
DSP	Digital signal processor
ENOB	Effective number of bit
ET	Essential Tremor
FET	Field Effect Transistor
GSG	Ground-signal-ground
HPF	High pass filter
INL	Integral non-linearity
I/O	Input/Output
ISI	Inter-symbol interference
LNA	Low-noise neural amplifier

LPF	Low pass filter
LSB	Least significant bit
MOS	Metal-oxide semiconductor (field-effect transistor)
MSB	Most significant bit
PCB	Printed circuit board
PD	Parkinson's disease
PRBS	Pseudo-random binary sequence
PWM	Pulse width modulation
QFN	Quad-flat no-leads
RF	Radio frequency
ROM	Read-only memory
SAR	Successive approximation
SerDes	Serializer/Deserializer
SHA	Sample and hold
SMA	Sub-miniature version A
SNDR	Signal to noise-plus-distortion ratio
SoC	System-on-Chip
TEM	Transverse Electro-Magnetic
UI	Unit interval
VGA	Variable gain amplifier

## Abstract

This thesis describes research on design techniques for a log-based closed-loop neurostimulation system-on-chip (SoC) for treatment of neurological disorders. Deep brain stimulation (DBS) has become one of the most effective therapies for numerous neurological disorders and epilepsy. A single-chip closed-loop neurostimulation system for treatment of neurological disorders is proposed.

The system is comprised of five major parts: a recording path, a stimulation path, a digital processing unit, a power harvester, and an RF transceiver. Unlike any previous work, the recording path and digital processing unit of this work operate entirely in the log-domain to represent neural signals effectively with fewer bits while consuming less power. The recording path incorporates four channel low-noise amplifiers (LNAs), a logarithmic 8-bit pipeline analog-to-digital converter (ADC), and two sets of a logarithmic digital low-pass filter (LPF) and high-pass filter (HPF). The stimulation path includes two high-current digital-to-analog converters (DACs), six general-purpose DACs, and dedicated stimulation controllers. The high-current DACs are capable of both electrical and optical stimulation.

Even though there has been over a decade of research on the mechanism of DBS, the algorithms of closed-loop DBS are still unclear. Recently, the energy of the local field potential (LFP) has emerged as an important and effective feedback indicator. In the proposed system, the digital processing unit detects the LFP energy and extracts optimal



stimulation parameters by analyzing the LFP energy information. The digital processing unit includes a generic PI-controller for analysis of the LFP energy.

The proposed system also includes a power harvester that converts a  $915\text{MHz}$  RF carrier to  $1.8\text{V}$  power supplies for the system, an RF transceiver to transmit recorded signals to an external device for further research. A backscatter scheme is chosen for the type of transmitter to minimize power consumption.

A prototype system is designed and fabricated in  $180\text{nm}$  CMOS technology. The prototype system occupies  $4\text{ mm}^2$  and consumes  $468\text{ }\mu\text{W}$  for recording and processing neural signals, stimulation, and RF communication. The proposed closed-loop neurostimulation system utilizes the LFP energy for closed-loop stimulation and log-domain computation for the first time, and achieves a single-chip operation requiring no external circuit components.

# **Chapter 1**

## **Introduction**

An estimated 42 million people in the United States suffer from neurological movement disorders including essential tremor, dystonia, and Parkinson's disease [1]. More than 10 million people in the United States and more than 50 million people worldwide suffer from epilepsy [2]. Deep brain stimulation (DBS) of the subthalamic nucleus with periodic, high frequency electric pulse trains has become one of the most effective therapies for epilepsy and aforementioned neurological movement.

In this chapter, we review the background of several important neurological movement disorders and epilepsy, and discuss DBS and closed-loop DBS. Following the discussion, we propose a log-based single-chip closed-loop neurostimulation system and give a brief description of the proposed system. At the end of the chapter, an outline of the dissertation is provided.

### **1.1. Essential Tremor**

Essential tremor (ET) is a progressive neurological disorder that causes a rhythmic trembling (4-12 Hz) of the hands, head, voice, legs or trunk [3]. In addition to the trembling, a variety of non-motor features appear such as anxiety, depressive symptoms and cognitive difficulty [4]. Patients with severe tremor have difficulty

performing many routine activities of daily living. ET is one of the most common neurological disorders, with a prevalence of approximately 4% of people in age 40 and older and considerably higher among people in 60s and older [5].

Although the underlying etiology is not clear yet, it is found that a genetic mutation is responsible for 50% of all cases, from observing its autosomal dominant transmission. It is estimated that the abnormal brain activity is processed through the thalamus and causes tremor. Figure 1.1 shows a patient with ET drawing the Archimedes spiral [6]. This is the most common way to diagnose ET assuming there are no other neurological or biological reasons to be found.



Figure 1.1: A patient with essential tremor drawing the Archimedes spiral [6].

The tremor tends to intensify as any physical or mental stress builds up. Other factors including fatigue, low blood sugar, caffeine, cold, and lithium salts also make tremor worse.

Table 1.1 gives summary of treatment for ET. When diagnosed with essential tremor there are several courses of action depending on the severity of the tremor. Most people with ET benefit from medication. A surgical approach to treatment is generally suggested for people with severe ET symptoms or those whose symptoms have not responded to the maximum acceptable dosages of medication.

Table 1.1: Treatment for essential tremor.

<b>Type</b>	<b>Name</b>	<b>Mechanism</b>	<b>Side Effects or Complications</b>
Medication	Propranolol	Blocks the receptor sites for Adrenaline.	Dizziness, fatigue, depression, diarrhea, nausea and vomiting, changes in blood sugar levels, difficulty breathing, sinus bradycardia, or hypotension.
	Primidone	Slows the central nervous system and helps to reduce seizure.	Nausea, vomiting, fatigue or sleepiness, confusion, ataxia, vertigo, unsteadiness, irritability, blurred vision, or loss of appetite.
Surgery	Thalatomy	A selected portion of the thalamus is ablated.	Contralateral weakness, confusion or dysarthria.
	DBS	High frequency electrical stimulation helps the thalamus rebalance the movement control.	Mild dysarthria, weakness on one or both sides of the body, or disequilibrium.

## 1.2. Dystonia

Dystonia is also a neurological movement disorder in which sustained muscle contractions cause twisting and repetitive movements or abnormal postures [7]. The movements are involuntary and sometimes painful, and may affect a single or group of muscles [8]. Dystonic spasms typically increase in intensity during stress, emotional

upset, or fatigue. Spasms tend to decrease in intensity during periods of rest or sleep. Secondary effects such as disturbed sleep patterns, mood swings, mental stress, blurred vision, digestive problems and short temper may accompany direct symptoms. Over a period of time, the symptoms may become more noticeable and widespread and be unrelenting. Figure 1.2 shows a person with medication induced dystonia. It is difficult to find a comfortable position for arms, legs, and a neck for the patient.



Figure 1.2: A person with medication induced dystonia.

Although the causes of dystonia are not known or understood, investigators believe that dystonia results from an abnormality in the basal ganglia. It is suspected that a defect in the body's ability to process neurotransmitters, environmental or disease-related damage

in the basal ganglia causes dystonia.

Unfortunately there are currently no known treatments that can reverse the course of dystonia. However, the symptoms can be reduced and managed with a combination of treatments. Table 1.2 gives summary of treatment for dystonia. Surgical intervention is generally suggested for those patients with severe dytonia or those whose symptoms have not responded to drug therapy. Recently, DBS has proven successful in many cases of severe dystonia [9].

Table 1.2: Treatment for dystonia.

<b>Type</b>	<b>Name</b>	<b>Mechanism</b>	<b>Side Effects or Complications</b>
Medication	Botulinum Toxin (BoNT)	Block the release of acetylcholine to decrease inappropriate or excessive muscle contractions.	Temporary muscle weakness.
	Benzo-diazepines	Interfere with chemical activities in the nervous system and brain.	Drowsiness, depression or psychosis.
	Anti-cholinergics	Block the action of acetylcholine to decrease inappropriate or excessive muscle contractions.	Confusion, drowsiness, hallucinations, forgetfulness, dry mouth, or blurred vision.
Surgery	Thalamotomy	A selected portion of the thalamus is ablated.	Contralateral weakness, confusion or dysarthria.
	Pallidotomy	Part of the globus pallidus (GPi) is destroyed to restore balance.	Stroke, or cognitive impairment.
	DBS	High frequency electrical stimulation helps the thalamus rebalance the movement control.	Mild dysarthria, weakness on one or both sides of the body, or disequilibrium.

### 1.3. Parkinson's Disease

Parkinson's disease (PD) is a degenerative disorder of the central nervous system (CNS) and is the second most common neurodegenerative disorder after Alzheimer's disease [10]. PD affects more than 1 million people in United States and approximately 50,000 Americans are diagnosed with PD every year [11]. PD gives rise to motor types of symptoms including tremor, bradykinesia, stiffness, and postural instability as well as non-motor types of symptoms such as sensory deficits, depression, anxiety, cognitive difficulties and sleep disturbance. Figure 1.3 shows Muhammad Ali and Michael J. Fox who are celebrity patients diagnosed with PD.



Figure 1.3: Muhammad Ali and Michael J. Fox.

For most cases with PD, patients are diagnosed with idiopathic PD meaning no specific causes are known or understood, and only a very small minority of cases can be attributed to known genetic factors such as the parkin gene, alpha-synuclein, DJ-1, PINK-

1, and UCHL-1. The main pathological characteristics of PD is that cells of the substantia nigra degenerate and become incapable of producing adequate dopamine as described in Figure 1.4. Since dopamine controls movement and balance for the proper functioning of CNS, PD gives rise to the aforementioned symptoms [12].

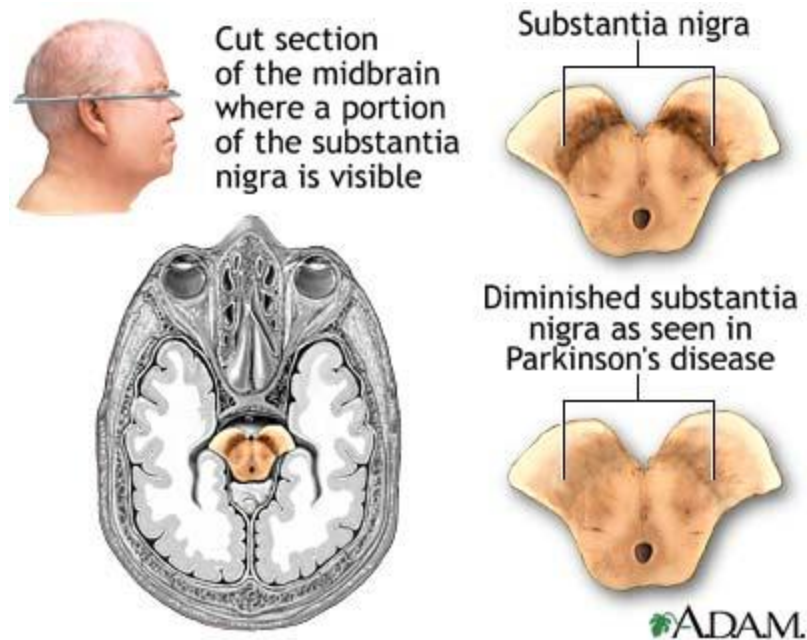


Figure 1.4: Diminished substantia nigra in a patient with Parkinson's Disease [13].

Although there is no known cure that can stop or reverse the progress of PD, there exists treatment that can provide relief from the symptoms of PD. Several types of treatment are summarized in Table 1.3. While levodopa continues to be the most effective treatment for motor symptoms, DBS has become the most commonly used surgical treatment for patients with advanced PD for whom medication is no longer sufficient [14]. Active on-going research direction includes the studies of cell transplants and gene therapy that are still at the experimental stage.



Table 1.3: Treatment for Parkinson’s disease.

Type	Name	Mechanism	Side Effects or Complications
Medication	Levodopa	Converted into dopamine in the brain.	Nausea, vomiting, drowsiness, orthostatic hypotension, and dyskinesia.
	Dopamine Agonists	Imitate or mimic the action of levodopa in the brain by directly stimulating dopamine receptors.	Drowsiness, sudden sleep onset, nausea, orthostatic hypotension, edema and psychosis.
	MAO-B Inhibitors	Slow the breakdown of dopamine in the brain.	Insomnia, hallucinations, and orthostatic hypotension.
	Anti-cholinergics	Block the action of acetylcholine to decrease inappropriate or excessive muscle contractions.	Confusion, drowsiness, hallucinations, forgetfulness, dry mouth, or blurred vision.
Surgery	Thalamotomy	A selected portion of the thalamus is ablated.	Contralateral weakness, confusion or dysarthria.
	Pallidotomy	Part of the globus pallidus (GPi) is destroyed to restore balance.	Hemorrhage, stroke, or cognitive impairment.
	DBS	High frequency electrical stimulation helps the thalamus rebalance the movement control.	Mild dysarthria, weakness on one or both sides of the body, or disequilibrium.

#### 1.4. Epilepsy

Epilepsy is one of the most common neurological disorder characterized by a tendency for recurrent seizures, which is defined as a transient symptom of abnormal excessive or synchronous neuronal activity in a part of the brain, in particular the cortex [15]. The intensity of epileptic seizure differs from person to person. Although some may experience a strange sensation, some experience violent shaking and lose consciousness

as shown in Figure 1.5. Epilepsy is estimated to affect approximately 3 million Americans of all ages and ethnic groups, and about 50 million people worldwide [16-17].



Figure 1.5: Woman with epileptic seizure.

Causes of epilepsy vary from a medical condition to injury that affects the brain, or even may be unknown. Many known common causes of epilepsy include hypoxic-ischemic encephalopathy, CNS infections, congenital defects, stroke, trauma, brain tumors, cerebrovascular disease, and dementia.

Epilepsy is usually treated with medication. Anticonvulsants may reduce the number of future seizures. If a patient's condition does not improve after adequate trials of different anti-seizure drugs, that epilepsy is diagnosed to be medically refractory. For people with refractory epilepsy, surgical treatments are recommended. Even though it is not clear which brain region is affected by DBS and the mechanism is not understood at the present time, DBS is shown to be effective in many uncontrolled studies. Table 1.4 summarizes treatments of epilepsy.

Table 1.4: Treatment for epilepsy.

<b>Type</b>	<b>Name</b>	<b>Mechanism</b>	<b>Side Effects or Complications</b>
Medication	Anticonvulsant	Favor inhibition over excitation by modifying processes that develop a seizure.	Mood changes, sleepiness, unsteadiness in gait, hepatitis, or aplastic anemia.
Surgery	Resection	Removes the area of the brain that causes seizures.	Paralysis, headache, nausea, or depression.
	Vagus nerve stimulation	Affects serotonin and norepinephrine neurotransmitters.	Dyspepsia, infection, nausea, paresthesia, or hoarseness.
	DBS	High frequency electrical stimulation helps the thalamus rebalance the movement control.	Mild dysarthria, weakness on one or both sides of the body, or disequilibrium.

### **1.5. Deep Brain Stimulation (DBS)**

DBS is a surgical treatment that involves the implantation of battery-operated medical device which delivers electrical stimulation to specific parts of the brain, blocking the abnormal nerve signals that cause movement or affective disorders [18-19]. Despite the long history of DBS and the fact that DBS in select brain regions has provided remarkable therapeutic benefits for refractory movement and affective disorders, its underlying principles and mechanisms are still not clear and are still under research [20].

The Food and Drug Administration (FDA) approved DBS as a treatment for ET in 1997, for PD in 2002, and dystonia in 2003, and a medical technology company named Medtronic has received European regulatory approval for its DBS system for patients with refractory epilepsy [21]. Medtronic has pioneered the use of DBS therapy in the

United States, a fast growing market that has attracted the interest of competitors like St. Jude Medical, Cyberonics, Advanced Bionics, and Boston Scientific [22]. Among those many companies, Medtronic is currently the only company selling FDA-approved rechargeable DBS devices in the country, and this distinction led the third quarter neurostimulation revenues of the company to \$394 million in fiscal year 2010 [23].

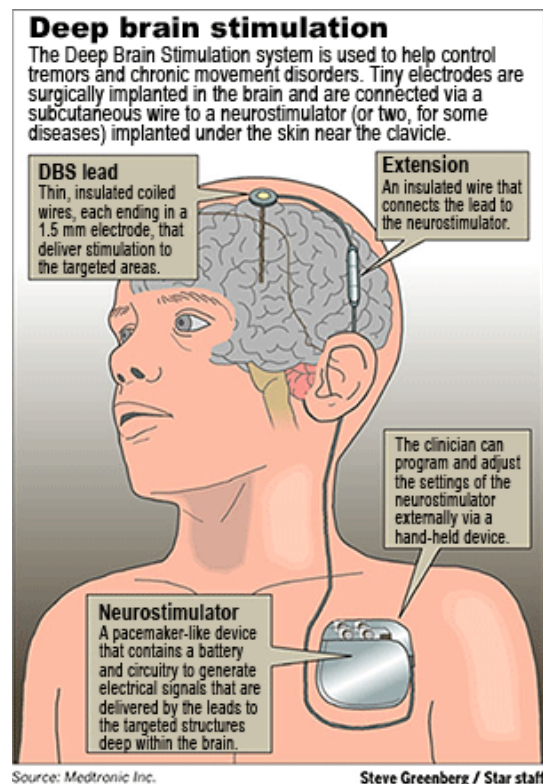


Figure 1.6: Implantation of DBS system [23].

The DBS system is typically comprised of three parts implanted completely inside the body by an experienced neurosurgeons, neurologists, and neurophysiologists: the power source to the system called neurostimulator, a set of thin wires called lead covered with a protective coating, and an insulated wire called extension that connects the

neurostimulator and the lead [24]. Figure 1.6 shows a placement of these components in a patient. DBS leads are placed in the target site of the brain according to the type of symptoms. The leads are placed in the ventrointermediate nucleus of the thalamus and in either the globus pallidus or subthalamus nucleus for cases with essential tremor and cases with dystonia or PD respectively. The neurostimulator is usually placed subcutaneously below the collarbone. The extension runs from the head, down the side of the neck and connects to the neurostimulator. The Activa RC neurostimulator shown in Figure 1.7, the most advanced device from Medtronic that operates with a rechargeable battery, has the size of  $54 \times 54 \times 9 \text{ mm}$  ( $2.1 \times 2.1 \times 0.4 \text{ in}$ ) and the weight of  $40\text{g}$  ( $1.6 \text{ oz}$ ).



Figure 1.7: Activa RC neurostimulator for Medtronic DBS therapy [25].

While DBS is proven to be effective to movement and affective disorders and to epilepsy, there exist potential side effects and complications. The potential side effects

commonly include stiffness or weakness of the limb, dizziness, imbalance, mood changes, and depression. These side effects are, however, usually temporary or reversible, and can be minimized by optimization of stimulation parameters in most cases. Post-operative complications include hemorrhage, and wound infection. Although the resulting complications from hemorrhage can be severe, complication rates after DBS surgery remain low when the procedure is performed by an experienced surgical team, proving that DBS is not only effective but also safe [26].

Unfortunately, complications related to hardware and its components can also occur, and these include fracture or breakage of the DBS lead or extension wire, battery failure, erosion of the device, and migration of the wire. From recent research, it has been reported that 9.8% of the patients with DBS procedure were affected by hardware related complications [27]. Improvement in powering scheme of DBS devices such as power harvesting or wireless powering that obviates the need for a large battery and an extension wire can reduce the number of incidents from hardware related complications as well as the number of surgeries only to replace a battery or a wire.

## **1.6. Closed-loop DBS**

Despite over a decade of clinical experience the underlying principles of DBS are still not clear. Because of this lack of knowledge, the only effective feedback indicator currently known for the optimal selection of stimulation parameters such as amplitude, pulse-width, and repetition rate (frequency) of the electrical stimulation signals is the visual sign of symptoms. In addition, every patient has a different set of signal amplitudes,

pulse widths and repetition rates that are effective to treat their disease symptoms. Thus a post-surgery process called programming is necessary for the best result from DBS.



Figure 1.8: Titrating stimulation using a handheld programmer from Medtronic [28].

After a DBS device is surgically implanted in a patient, the stimulation parameters are adjusted by a neurologist or a trained technician to optimize symptom management with minimum adverse effects. An external component that transmits instructions wirelessly to the neurostimulator is used to noninvasively tune the parameters [29]. Figure 1.8 shows a clinician programming the stimulation parameters of a patient using a programmer from Medtronic which communicates with the neurostimulator through the skin. Initial programming may take 2-3 hours and the patient

should not leave the doctors for at least 1-2 hours after programming to allow the observation of therapeutic changes with DBS and for any fine adjustments to be made. In general, programming is performed frequently for the first 3-6 month period to achieve good results, and the patients visit a neurologist or a trained technician periodically or on need basis to ensure the best control of symptoms as a patient's condition changes over time. This type of DBS can be named open-loop DBS.

If any internal information from the brain of a patient with a neurological disorder can be obtained, then it may be possible to find the proper stimulation parameters automatically with the help of a dedicated microprocessor or even a small digital signal processor. This type of DBS is called closed-loop DBS. While open-loop DBS, the only type of DBS currently available, requires patients to visit clinicians often for fine tuning and needs an external device for programming, closed-loop DBS does not require intricate visits of patients to clinicians nor external device for programming.

Although the underlying principles of DBS is not known yet, it is believed that the strongest candidate for the closed-loop feedback signal is an abnormal pattern change in spike or local field potential (LFP) signals. In general, spike signals, also known as action potentials, are said to have bandwidths from 100 *Hz* to 10 *kHz* and amplitudes up to 500  $\mu V$  [30], and LFP signals have bandwidths from 1 *Hz* to 100 *Hz* and amplitudes up to 5 *mV* [31]. Among them, neural spike signals have drawn more attention as a possible candidate for the feedback indicator. To this end, a biomedical multiprocessor system-on-chip (SoC) for closed-loop neuroprosthetic applications has been proposed [32]. This work performs real-time spike-sorting with principal component analysis. Another work on a closed-loop biomedical system has developed an activity-dependent intracortical



microstimulation SoC [33]. This SoC embeds a digital spike discrimination processor that triggers stimulation every time it captures a neural spike signal stronger than a preset threshold. Recently features of the LFP signals, in particular the energy of LFPs, have emerged as more effective feedback indicators for DBS [34]. An implantable closed-loop microstimulator targeted at titration therapy in DBS was proposed and developed to exploit the features of LFP signals with analog spectral analysis method [35]. The system incorporates a custom IC for recording and spectral analysis, an auxiliary microprocessor for extracting key bioelectrical signals, and an existing neurostimulator device.

### **1.7. Dissertation outline**

In this dissertation, a new architecture and new design techniques are proposed for closed-loop neurostimulation to exploit the logarithmic characteristics of neural signals, allowing efficient signal processing to extract the feedback information while operating from harvested or battery power. These techniques are verified with evaluation results from a prototype closed-loop DBS SoC. The prototype is fabricated in 180nm TSMC CMOS. The key design goals for the prototype are to implement and verify a log-based digital processing unit that receives the logarithmic output from a log-ADC directly and extracts the energy information of LFP signals, and a closed-loop feedback path that uses the energy of LFP signals, and to achieve the highest degree of integration to enable truly single-chip operation.

Design techniques for a low-power differential low-noise neural amplifier (LNA) and a pipeline log-ADC are proposed in Chapter II. These techniques include a two-stage cascade structure of band-pass amplifiers, power optimization of a folded cascode

amplifier, and elimination of a dead-zone inherent in a pipeline log-ADC structure. In Chapter III, design methods and techniques to build a digital processing unit that performs high-pass and low-pass filtering, and extracts the feedback information to set the stimulation parameters are explained. The processing unit performs calculation entirely in a logarithmic domain resulting in reduced power consumption. Circuit techniques for a power management block which incorporates a power harvester, low-dropout regulators, and bias circuitries are shown in Chapter IV. The power management block provides 1.8V supply to the whole system from a 915 MHz carrier. Design techniques for other important building blocks of the proposed system including a biphasic current stimulator, a source-coupled oscillator for clock generation, an RF transceiver based on a backscattering scheme, are described in Chapter V.

The prototype system and performance measurements are presented in Chapter VI. The dissertation concludes in Chapter VII that combination of logarithmic analog to digital conversion, logarithmic digital signal processing (DSP), and LFP energy based closed-loop DBS enables a power-efficient, fully implantable SoC for treatment of neurological disorders, and suggests some possibilities for future work to extend this research.

## Chapter 2

### Design techniques for recording front-end

As the extraction of accurate feedback information relies on the quality and accuracy of recorded neural signals, the performance of the recording front-end is one of the most critical specifications of closed-loop neurostimulation systems. Therefore, it is required to design the recording front-end to provide data that carry sufficient and accurate information to support the extraction of feedback indicators or to enable further analysis. In this chapter design techniques for LNAs and a log-ADC are presented to process both spikes and LFPs.

#### 2.1. LNA

Both the spikes and LFP signals carry unique information about the state of a brain [36]. Since these signals exhibit different characteristics such as bandwidth and amplitude, there have not been many IC systems that record both signals simultaneously. Due to the very different amplitude ranges of spikes and LFPs, LNAs should exhibit a high dynamic range, good noise performance, and wide bandwidth at the same time.

A general band-pass amplifier is shown in a single-ended fashion in Figure 2.1. Assuming the voltage gain of the op-amp is  $A$ , the transconductance of the op-amp is  $G_m$ , and the poles are far from each other, we have the following equations for the zero and

pole locations, and the pass-band gain. The frequency response of the general band-pass amplifier is shown in Figure 2.2 with the zero and pole locations assigned with the equations described below.

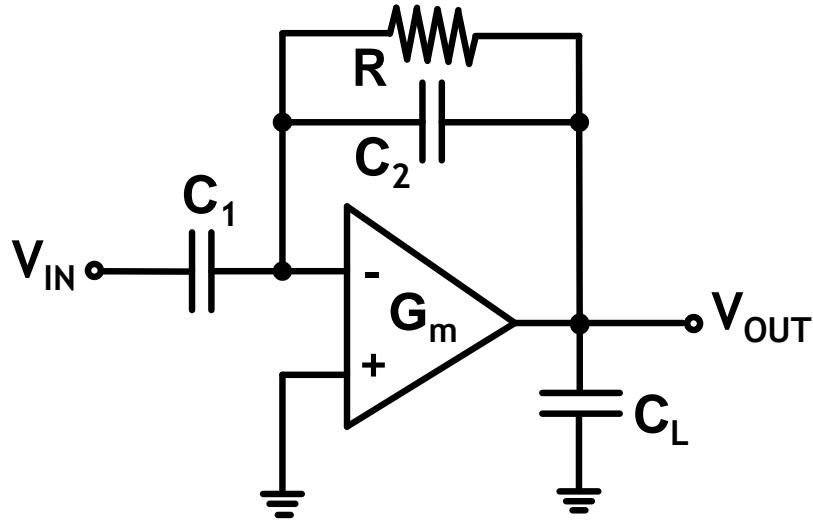


Figure 2.1: A single-ended representation of the schematic of a band-pass amplifier.

$$\omega_{z1} = 0 \quad (2.1)$$

$$\omega_{z2} = \frac{1}{C_2} \left( G_m - \frac{1}{R} \right) \quad (2.2)$$

$$\omega_{p1} \approx -\frac{1}{RC_2} \quad (2.3)$$

$$\omega_{p2} \approx -\sqrt{\frac{G_m}{R(C_1C_2 + C_2C_L + C_LC_1)}} \quad (2.4)$$

$$(Passband\ Gain) = \frac{C_1}{C_2} \quad (2.5)$$

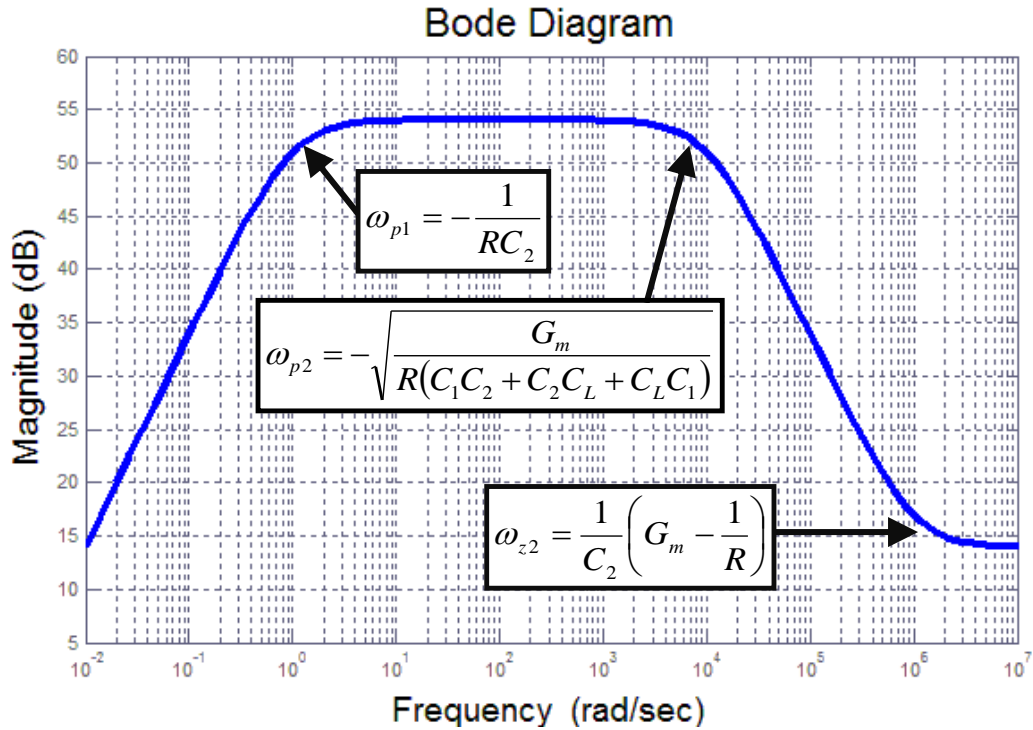


Figure 2.2: Simulated frequency response of the general band-pass amplifier.

As can be seen from the equations, the two poles tend to move in the same direction as the values of  $R$  and  $C_2$  change, except only that the second pole moves less because of the square root operator. The pass-band gain and the first pole are determined easily from the gain requirement to match the full scale input of the ADC and from the low cutoff frequency requirement (around 1 Hz) to be able to capture low frequency LFP signals. Therefore, the transconductance of the amplifier,  $G_m$ , and the load capacitance,  $C_L$ , are determined by equation 2.4 to achieve the second pole of around 10 kHz to capture high frequency spike signals.

Given that the full scale input range of the ADC is 600 *mV*, as explained in section 2.2, and that the input amplitude of the LFP signals is around 1 *mV* and rarely higher than 1.2 *mV*, a pass-band gain of 500 (= 54 *dB*) is appropriate for the front-end LNA. Moreover the feedback resistance *R* is on the order of  $10^{11}$   $\Omega$  which is described later. This level of gain and the feedback resistance makes it difficult to achieve both the first and second poles low and high enough respectively to be able to capture low-frequency LFP and high-frequency spike signals at the same time unless  $G_m$  is in the order of  $1\Omega^{-1}$ , which is not allowed in low-power biomedical applications.

Therefore, to address the large gain issue and to achieve the bandwidth requirement with a minimum overhead in power consumption, a two-stage cascade structure is chosen for the front-end LNA. The LNA with two-stage structure is shown in Figure 2.3. This two-stage structure also suppresses out-of-band signals more than the general one-stage band-pass amplifier with the same pass-band gain. The first stage and second stage are designed to have a pass-band gain of 50 and 10 respectively. The larger gain in the first stage reduces the effect from the second stage to the input-referred noise of the entire LNA. This two-stage structure also reduce the capacitor area compared to the general one-stage approach while meeting the same mismatch requirement which is directly related to the pass-band gain.

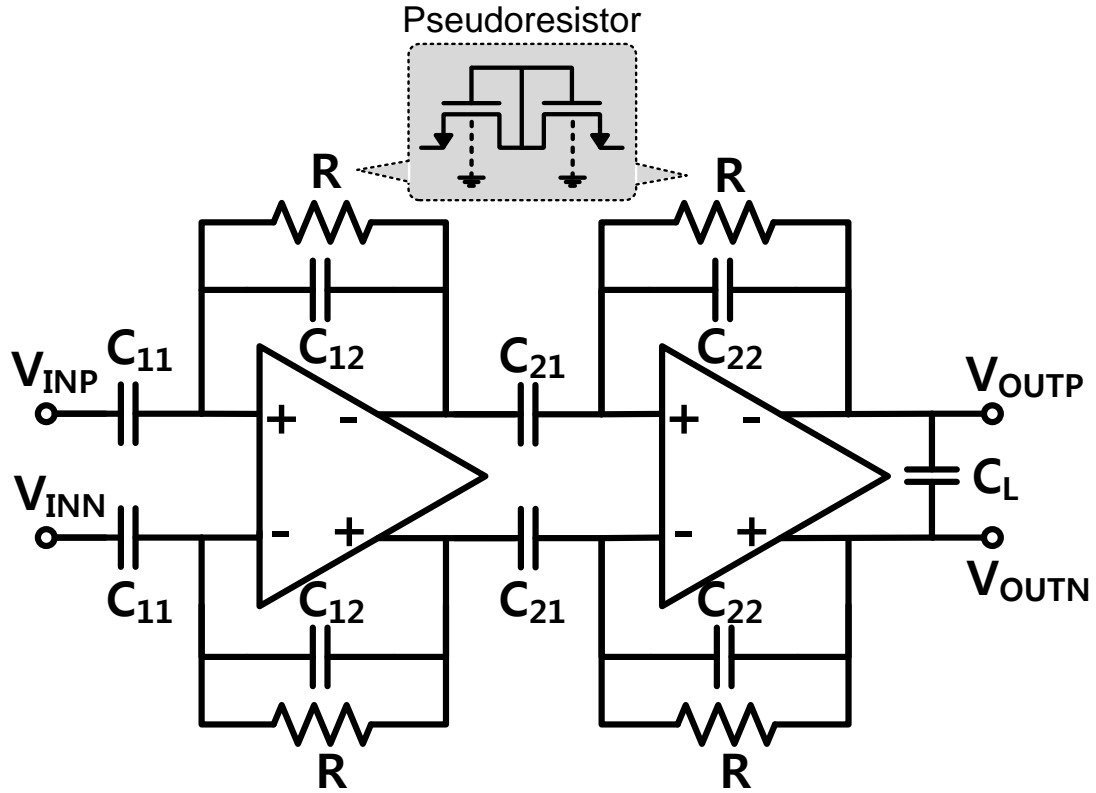


Figure 2.3: A differential representation of the schematic of a two-stage band-pass amplifier.

The amplifiers in the first and second stages are folded cascode amplifiers with an NMOS input pair to provide an enough gain. The lengths of all MOSFETs in the signal paths are  $20\mu m$ , the maximum channel length allowed in the used  $180nm$  CMOS technology, for large output resistance, since gain is a more important property than speed in this application. Since the input pair of an amplifier is the most significant source of flicker noise, the input pair of the amplifier is sized to  $W=20\mu m$  and  $L=20\mu m$  to reduce the total noise. A pseudoresistor comprised of two back-to-back diode-connected NMOSs are used to emulate high resistance as high as  $10^{11}\Omega$ . Compared to one used in

[37], this configuration reduces parasitic capacitance shown at the input and output nodes of the amplifier because the gates of NMOSs are connected within the pseudoresistor.

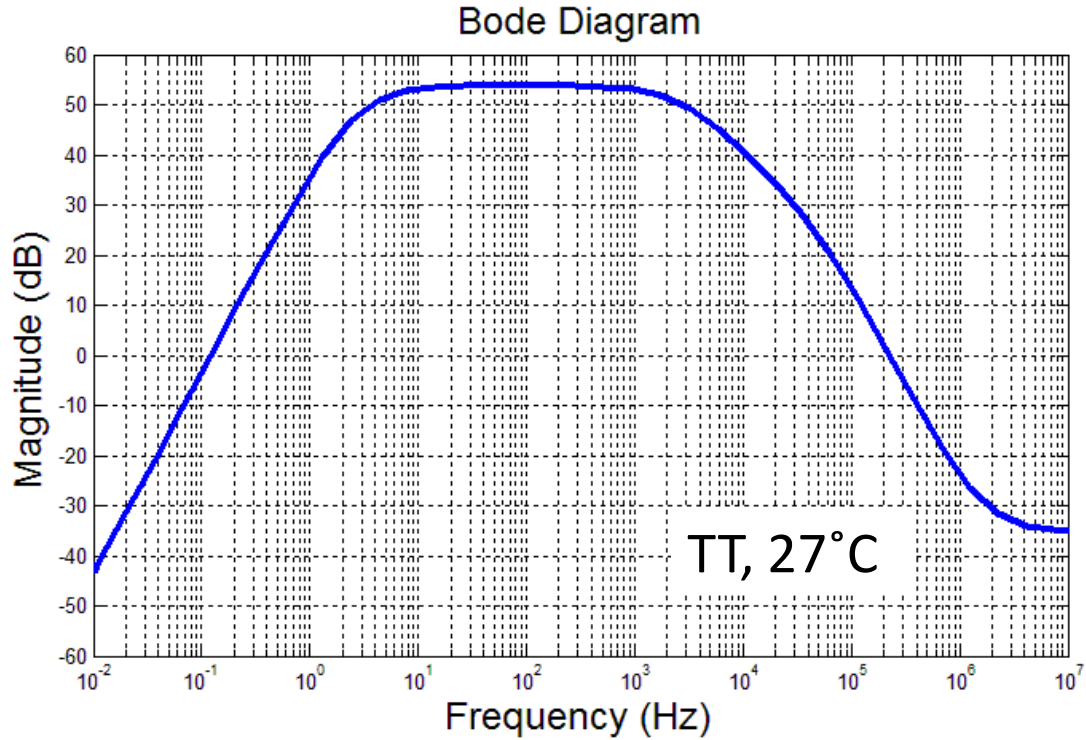


Figure 2.4: Simulated frequency response of the designed two-stage band-pass LNA.

The values of the circuit components in the LNA are chosen through calculation and simulation:  $C_{11} = 62.5 \text{ pF}$ ,  $C_{21} = 1.25 \text{ pF}$ ,  $C_{12} = C_{22} = 12.5 \text{ pF}$ ,  $C_L = 2.5 \text{ pF}$ , and  $R = 10^{11} \Omega$ . A simulated frequency response of the designed band-pass LNA at  $40^\circ\text{C}$  and  $1.8\text{V}$  supply is shown in Figure 2.4. The simulated input-referred noise is  $6.04 \mu\text{V}_{rms}$ , which is comparable to the microelectrode noise and background cortical activity noise ( $5 \mu\text{V}$ ) [38]. As the application of this system is an implant device in a human body, temperature variation is not a significant factor to affect the performance of LNA. Therefore, the



design of the system is considered at body temperature, 40°C. A summary of the simulated performance of the LNA at different process corners is given in Table 2.1.

Table 2.1: Summary of the simulated performanc of the designed LNA at 40°C with 1.8V supply.

<b>Process Corner</b>	<b>Power consumption</b>	<b>Low 3dB cutoff frequency</b>	<b>High 3dB cutoff frequency</b>
TT	12.4 $\mu W$	1.4 Hz	6 kHz
FF	12.8 $\mu W$	6.9 Hz	6.6 kHz
SS	12.4 $\mu W$	0.66 Hz	5.04 kHz

## 2.2. Pipeline logarithmic ADC

Once neural signals are recorded from a microprobe implanted in a specific part of the brain and amplified by LNAs, the signals need to be encoded into digital domain to facilitate digital processing of the recorded signals, including further filtering to separate LFP and spike signals and to extract feedback information.

In the real world, many signals such as light intensity, audio amplitude, as well as neural signals in the brain, are better represented in a logarithmic scale than in a linear scale. These signals exhibits a high dynamic range and require high resolution analog to digital conversion when conventional linear encoding is used. However, increasing the resolution of an ADC results in larger area consumption, higher power consumption, or slower conversion speed depending on the type of ADC structure. Alternatively variable gain amplifier (VGA) can be used to expand dynamic range. However, a VGA is generally slow and cannot respond rapidly to fast varying signals [39].

Instead we propose to use a logarithmic ADC directly [40]. Although a neurostimulator system with a logarithmic ADC was proposed in our previous work [37], the compatibility of the logarithmic ADC in the system with neural signal input was not fully demonstrated. The performance of the log-ADC designed in this work is presented in a later chapter. Compatibility of the log-ADC with sample neural signals prerecorded from the brain of a rodent is also shown.

First, we briefly introduce the concept of the pipeline log-ADC. With logarithmic scale quantization, assuming an  $N$ -bit logarithmic ADC with an input voltage,  $V_{in}$ , a full scale input range,  $V_{range}$ , output digital bits ( $b_{N-1}$ ,  $b_{N-2}$ , ...,  $b_0$ ), and the base of logarithm function,  $B$ , the transfer function of the ADC is given by [40]:

$$\left[ 2^N \cdot \log_B \left( B \cdot \frac{V_{in}}{V_{range}} \right) \right] = b_{N-1} 2^{N-1} + \dots + b_0, \quad (2.6)$$

where  $[x]$  is the maximum integer that is not larger than  $x$ . As illustrated in Figure 2.5, the LSB size increases as the input signal level increases. As the input amplitude increases, the quantization becomes coarser. The LSB size is described by:

$$LSB_j = V_{range} \cdot B^{\left(\frac{j}{2^N}-1\right)} \cdot \left( B^{\frac{1}{2^N}} - 1 \right), \text{ where } j = 0, 1, 2, \dots, 2^N-1. \quad (2.7)$$

According to equation 2.7, we also have the following equations for the maximum and minimum LSB size.

$$LSB_{\max} = V_{range} \cdot \left( 1 - B^{-\frac{1}{2^N}} \right). \quad (2.8)$$

$$LSB_{\min} = V_{range} \cdot \left( B^{\left(\frac{1}{2^N} - 1\right)} - B^{-1} \right). \quad (2.9)$$

The dynamic range (DR) is defined as the ratio of the input range to the smallest resolvable signal, and can be described with the next equation:

$$DR = \frac{V_{range}}{LSB_{\min}} = \frac{B}{B^{\frac{1}{2^N}} - 1}. \quad (2.10)$$

From this equation, it is shown that DR increases as the base of logarithmic function,  $B$ , and the resolution,  $N$ , increase. Because of this logarithmic scale coding, a log-ADC have a higher DR than a conventional linear ADC. For example, with  $B=10$  and  $N=8$ , we get  $DR=61 \text{ dB}$  and this is  $13 \text{ dB}$  larger than DR of a conventional linear ADC with 8-bit resolution.

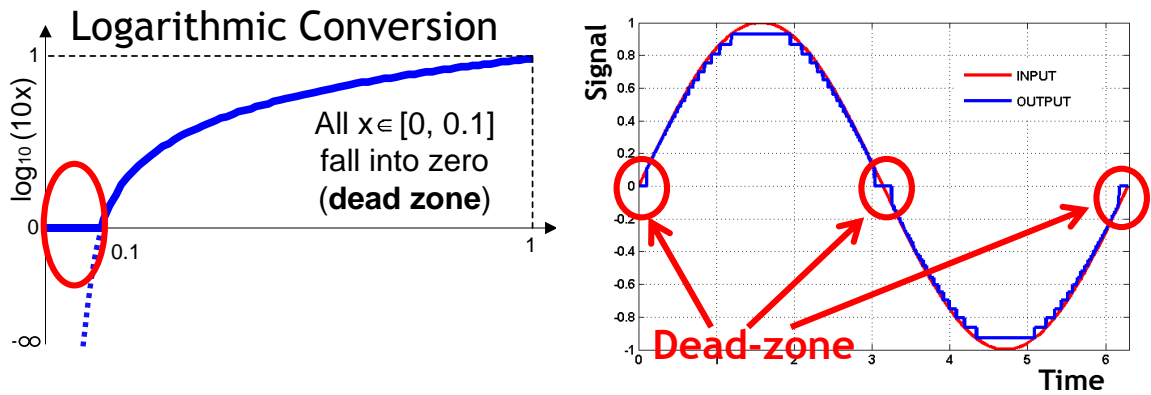


Figure 2.5: Coding scheme of a 5-bit logarithmic ADC with  $B=10$  (left) and output from sinusoidal input shown with dead-zone effect (right).

However, all inputs smaller than  $0.1 \times V_{range}$  result in a negative digital output and usually truncated to “0” as shown in Figure 2.5 leading to a practical DR of only 10. This logarithmic dead-zone and a technique to remove this dead-zone is briefly described in detail in Figure 2.6. Given that  $x = V_{in}/V_{range}$ , all inputs smaller than  $0.1 \times V_{range}$  are converted to a digital output 0 losing the benefit of high DR characteristic of logarithmic conversion. This problem can be overcome with a pre-conversion of input signal. With  $B=10$ , input  $x$  is pre-converted to  $y=0.9 \cdot x + 0.1$ , where,  $y$  is the input to logarithmic conversion. This pre-conversion scheme effectively eliminates the log dead-zone without losing significant DR. The pre-conversion scheme can be easily combined with the sample and hold circuits and this is explained later.

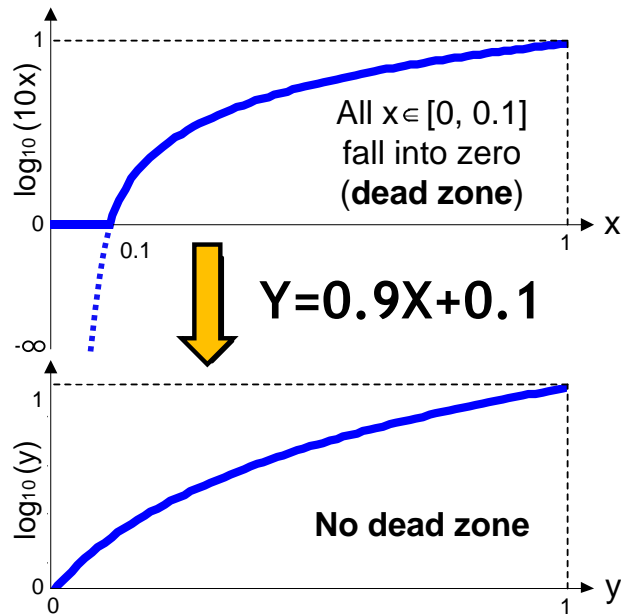


Figure 2.6: Pre-conversion of input to eliminate the log dead-zone.

Figure 2.7 shows the overall architecture of the 8-bit pipeline logarithmic ADC. Before the pre-conversion, the polarity of input signal is checked and sample and hold is performed. The output of sample and hold circuits is arranged in order to give positive inputs to the following logarithmic 1.5-bit stage, because of the nature of logarithmic function that assumes the input to be a positive number. After the sign decision with sample and hold, five logarithmic 1.5-bit stages and a 2-bit flash ADC process the signal and, finally, a digital logic block calculates out 8-bit digital output.

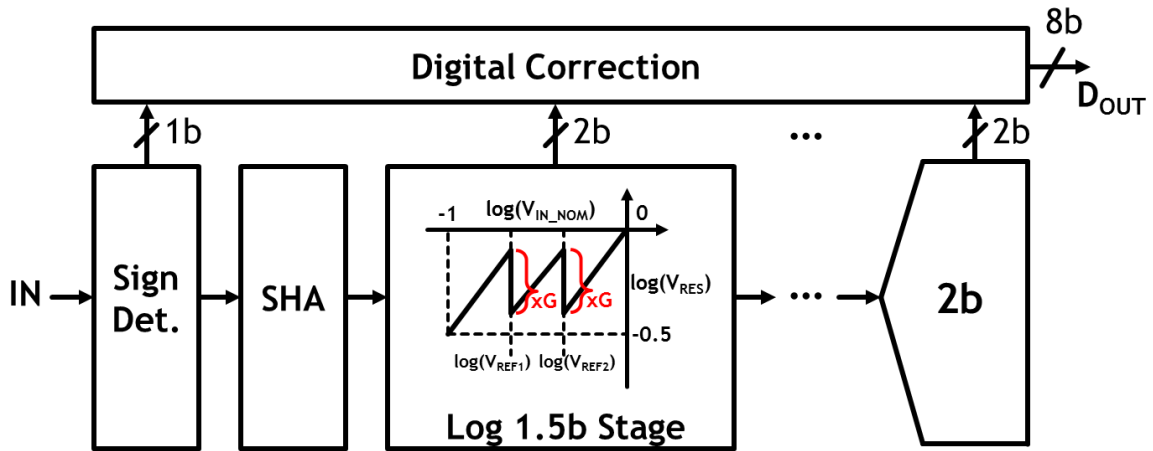


Figure 2.7: Overall architecture of the 8-bit pipeline logarithmic ADC.

Direct logarithmic conversion of a 1.5-bit stage in linear domain requires squaring operation to replace multiplication-by-2 operation in linear domain and conditional multiplication to replace the conditional addition or subtraction in linear domain. To avoid analog squaring, the reference voltages for the comparators and the gain settings for conditional addition are scaled in order to achieve the same result [40]. A conceptual

block diagram of the logarithmic 1.5-bit stage is described in Figure 2.8. The residue characteristic of the logarithmic 1.5-bit stage is also described in detail in Figure 2.9.

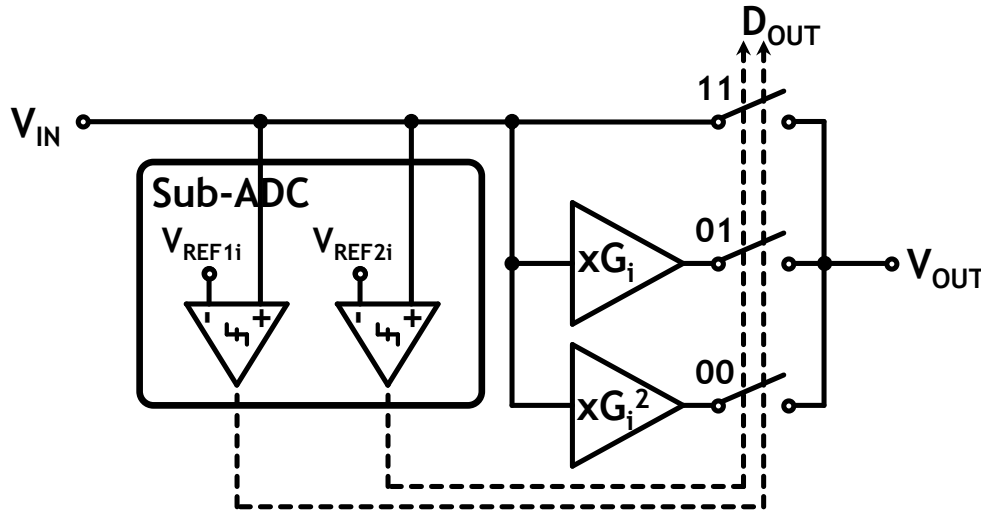


Figure 2.8: Conceptual block diagram of the logarithmic 1.5-bit stage.

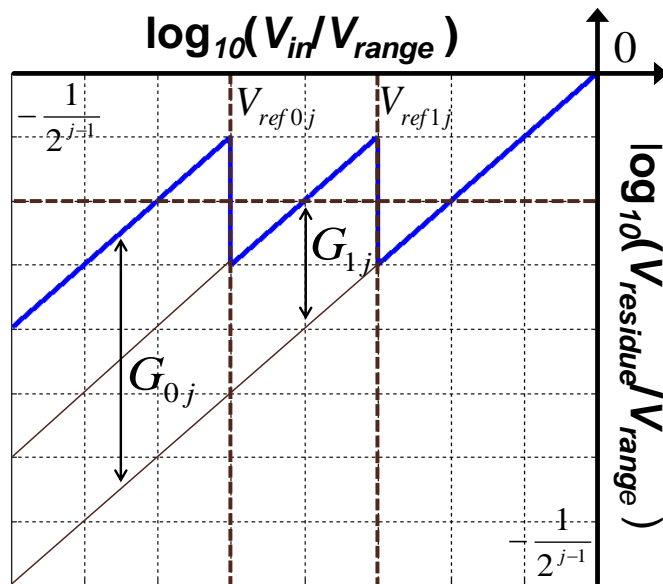


Figure 2.9: Residue plot of the logarithmic 1.5-bit stage with  $B=10$ .

The reference voltages for a  $j^{\text{th}}$  1.5-bit stage are given by:

$$\begin{aligned} V_{ref0j} &= V_{range} \cdot B^{-1.25/2^j}, \\ V_{ref1j} &= V_{range} \cdot B^{-0.75/2^j}, \end{aligned} \quad (2.11)$$

where  $V_{ref0j}$  and  $V_{ref1j}$  are the first and second reference voltages for a  $j^{\text{th}}$  1.5-bit stage, and  $V_{range}$  is the full scale input range. The gain settings for a  $j^{\text{th}}$  1.5-bit stage are given by [40]:

$$G_j(V_{in}) = \begin{cases} G_{0j} = B^{1/2^j}, & V_{in} \leq V_{ref0j} \\ G_{1j} = B^{1/2^{j+1}}, & V_{ref0j} < V_{in} \leq V_{ref1j} \\ G_{2j} = 1, & V_{ref1j} < V_{in} \leq V_{range} \end{cases} \quad (2.12)$$

where  $G_{0j}$ ,  $G_{1j}$ , and  $G_{2j}$  are gains for the first, second, and third input region for a  $j^{\text{th}}$  1.5-bit stage respectively, and  $V_{range}$  is the full scale input range. As shown from Figure 2.8, the input range of the next 1.5-bit stage is half of the current stage, and the reference voltages also scale accordingly.

For neural interface applications, an 8-bit logarithmic ADC with one sign bit and a base of 10 is implemented. A sampling rate of 100 *kSample/s* is chosen to process neural data from four recording channels simultaneously with some bandwidth margin. This configuration (7-bit resolution + 1 sign bit) provides a DR of 61 *dB*, which is high enough to cover the entire range of spike and LFP signals.

Figure 2.10 shows a fully differential sample and hold circuits that embeds the pre-conversion scheme. A common mode voltage of 800mV is chosen and used

throughout the entire ADC. Three clock signals  $\varphi_1$ ,  $\varphi_1'$ , and  $\varphi_2$  control the operation of the sample and hold circuits with the help of bottom-plate sampling [41]. When  $\varphi_1$  is high, the stage input is sampled and the output is reset. When  $\varphi_2$  is high, the input is amplified and the output is set by the following equation.

$$V_{out} = 0.9 \cdot V_{in} + 0.1 \cdot V_{range} \quad (2.13)$$

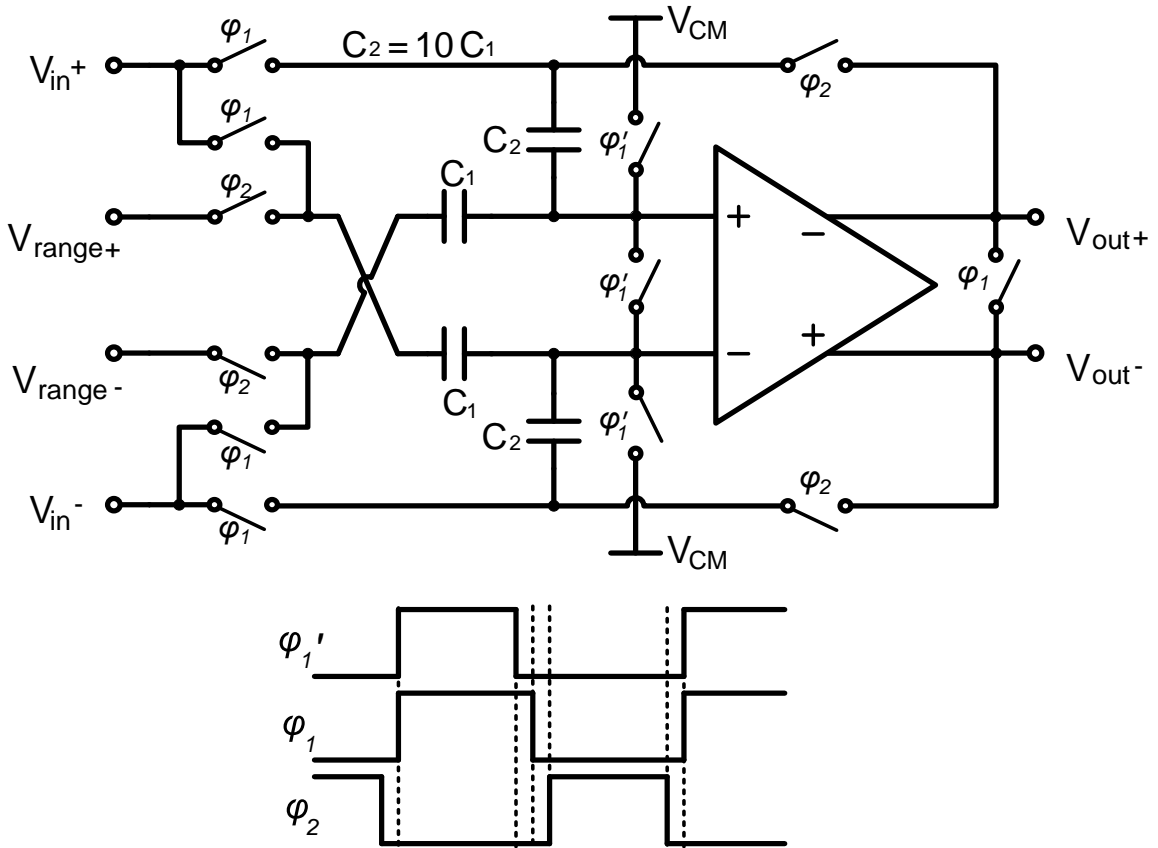


Figure 2.10: Simplified schematic of SHA with  $B=10$ .

For the op-amps in the SHA block and the 1.5-bit stages, a folded cascode amplifier topology with a PMOS input pair is chosen for its high gain and low power



consumption. The full scale input range,  $V_{range}$ , is set to 600 mV, which is the maximum achievable voltage swing that allows all MOS devices in the cascode amplifiers in saturation region. The op-amps are scaled through the stages to match the gain-bandwidth requirement.

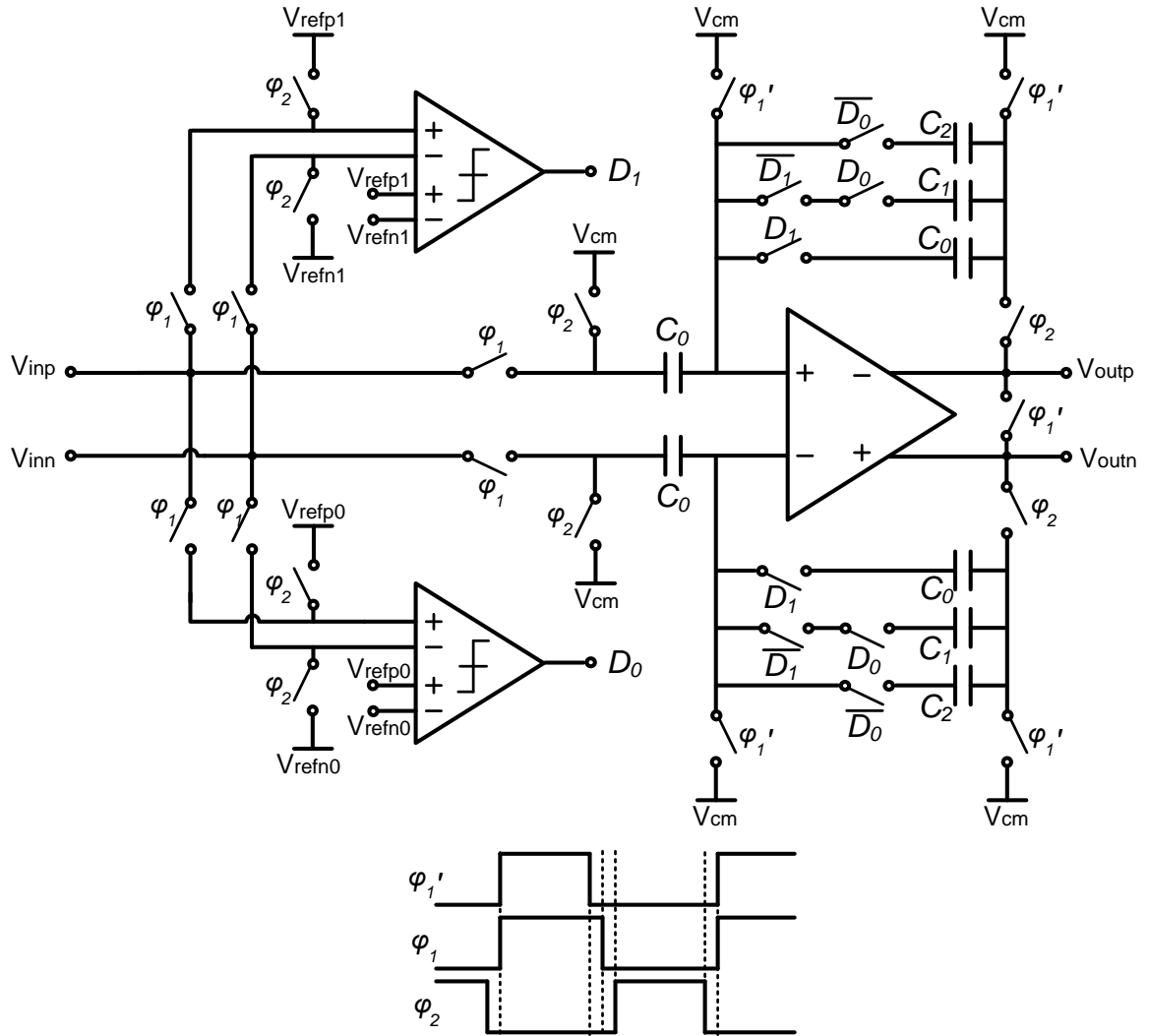


Figure 2.11: Simplified schematic of a logarithmic 1.5-bit stage.

A schematic of a fully differential 1.5-bit stage of the logarithmic ADC is illustrated in Figure 2.11. Similar to the SHA block, three clock signals  $\varphi_1$ ,  $\varphi_1'$ , and  $\varphi_2$  controls the operation of the sample and hold circuits with the help of bottom-plate sampling. When  $\varphi_1$  is high, the stage input is sampled and the output is reset. When  $\varphi_2$  is high, comparators decide the output bits and the residue is amplified with a gain depending on the bit decision. A two-stage regenerative comparator is used for the sign decision block and 1.5-bit stages, and the size of the input pairs of the comparators are scaled through the stages as the mismatch requirement becomes more strict due to the decrease of input range along the stages.

The bias circuit that generates reference voltages of the ADC is implemented entirely on-chip to enable the single-chip operation of the neurostimulation SoC. The schematic of the bias circuits is comprised of a two-stage amplifier with frequency compensation and a resistor ladder as shown in Figure 2.12. The common mode voltage and differential full scale input range voltages are generated, as well as the differential reference voltages, from the bias circuits. Reference voltage values and gains in each stage of the ADC are summarized in Table 2.2.

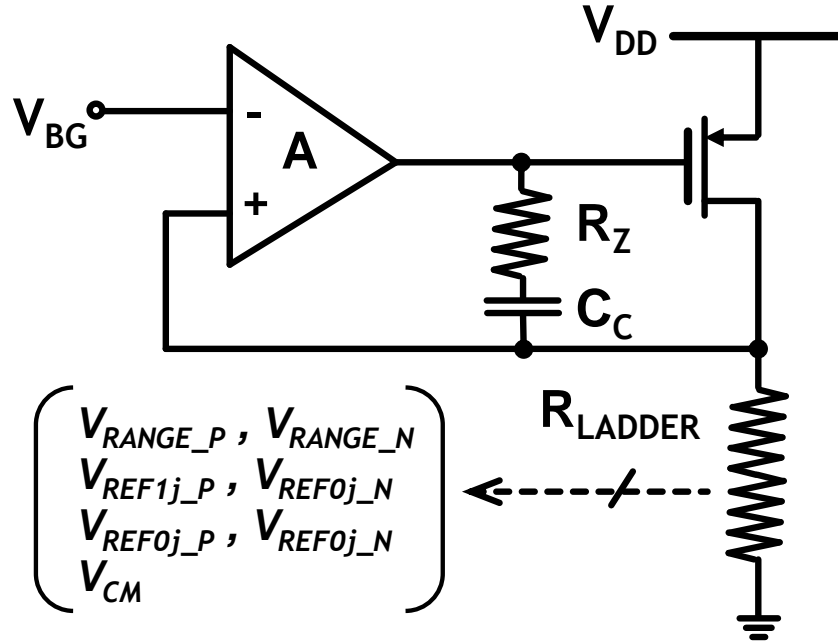


Figure 2.12: Schematic of bias circuits.

Table 2.2: Voltage reference and gain settings in the logarithmic 8-bit ADC with  $B=10$ .

Stage ( $j$ )	1 <sup>st</sup>	2 <sup>nd</sup>	3 <sup>rd</sup>	4 <sup>th</sup>	5 <sup>th</sup>	6 <sup>th</sup> (2-bit Flash)
$V_{ref0j}$	142 mV	292 mV	419 mV	501 mV	548 mV	568 mV
$V_{ref1j}$	253 mV	389 mV	484 mV	539 mV	568 mV	579 mV
$V_{ref2j}^*$	-	-	-	-	-	589 mV
$G_{0j}$	3.162	1.778	1.334	1.155	1.075	-
$G_{1j}$	1.778	1.334	1.155	1.075	1.037	-
$G_{2j}$	1	1	1	1	1	-

\*  $V_{ref2}$  is needed for the 6<sup>th</sup> stage because a 2-bit flash ADC needs three comparators.

## Chapter 3

### Design techniques for a log-domain digital processing unit<sup>1</sup>

To exploit the efficiency of logarithmic digitization, an analog front-end (AFE) with a logarithmic ADC is proposed in Chapter II to record neural signals with less number of bits while achieving the same DR compared to a conventional linear ADC.

We introduce complete log-domain digital filters and digital processing unit to implement closed-loop stimulation in this chapter. To further take advantage of logarithmically encoded signals, log-domain digital filtering is introduced in this work to directly process the logarithmic scale digital output from the ADC to reduce power consumption. LFP energy is also calculated efficiently from the filtered LFP signals using logarithmic arithmetic, and a programmable digital PI-controller uses the LFP energy information to set the optimal stimulation amplitude.

#### 3.1. Logarithmic digital signal process

There has been ongoing research on logarithmic digital signal processing for more than three decades because of the inherent high DR of logarithmic number system and the potentially low power consumption [42]. A logarithmic number system with a sign bit is proposed in early research to represent negative numbers as well as positive numbers

---

<sup>1</sup> The entire logarithmic digital processing unit is designed by Jaehun Jeong after the functionality and specifications of the unit are determined.

with minimal complexity, and this number system can be easily adopted in digital signal processing [43].

For a given DR requirement, fewer bits are needed for logarithmic number system compared to conventional linear number system. Furthermore, multiplication in linear-domain is equivalent to addition in logarithmic domain as described by the next equation.

$$\log(A \cdot B) = \log A + \log B, \quad (3.1)$$

where  $A$  and  $B$  are positive numbers. From this equation, it is expected that power consuming multipliers can be substituted with simple adders. The combination of the elimination of multipliers and the fewer number of required bits potentially leads to lower total power consumption for a digital processing unit. Although linear-domain addition is less intuitive in log-domain, a few methods are proposed in earlier studies [44-45]. The most popular way is to use a lookup table and this method is selected in our work for its simplicity.

$$\log(A + B) = \log\left(A\left(1 + \frac{B}{A}\right)\right) = \log A + \log\left(1 + 10^{\log B - \log A}\right), \quad (3.2)$$

assuming  $B$  is larger than  $A$ . In equation 3.2,  $\log(1+10^{\log B - \log A})$  needs to be determined. As the value of  $\log B - \log A$  increases,  $1+10^{\log B - \log A}$  approximates to  $10^{\log B - \log A}$  and, as a result,  $\log(1+10^{\log B - \log A})$  approximates to  $\log B - \log A$  which means that  $\log(A+B)$  simply approximates to  $\log B$ . In the case where  $\log B - \log A$  is not large enough, a lookup table is needed to find the value of  $\log(1+10^{\log B - \log A})$ . The decision to use lookup-table or not is also described in Figure 3.1. For a fixed resolution system (i.e. a fixed bit number),

there is a certain point for  $\log B - \log A$  beyond which  $\log(A+B)$  and  $\log B$  are the same. Therefore, a lookup table is needed only when  $\log B - \log A$  is smaller than the threshold.

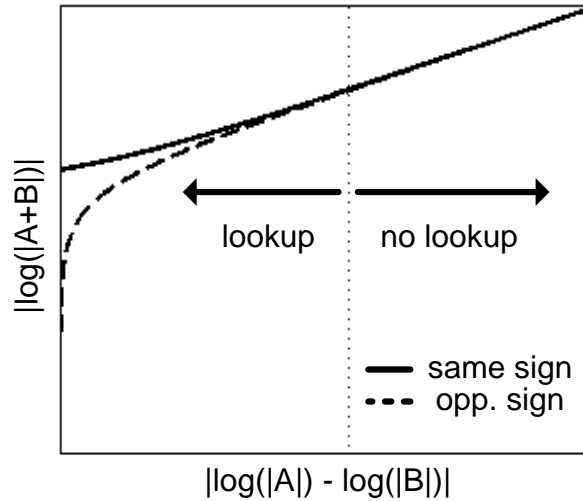


Figure 3.1: Lookup table usage decision.

Logarithmic arithmetic is first used in a digital filter in [46]. The work demonstrated that the designed log-domain digital filter consumes lower power than its linear counterpart, while maintaining a high DR. In other early research, a lookup table is used to calculate the sum of two numbers [47]. Recently, a 32-bit processor core based on logarithmic arithmetic was developed for low-power 3-D graphics systems [48]. Employing log-domain arithmetic enables the work to achieve performance improvements and lower power and area consumption simultaneously compared to other earlier works. Logarithmic digital signal processing is, therefore, proven to be efficient for applications that need high dynamic range with moderate accuracy as predicted from early theoretic studies.

### 3.2. Logarithmic digital filter

In this work, both a 15<sup>th</sup> order digital FIR low-pass filter (LPF) and a high-pass filter (HPF) are implemented in the system to separate the low-frequency LFPs and the high-frequency spikes from the digitized neural data and to provide those signals simultaneously.

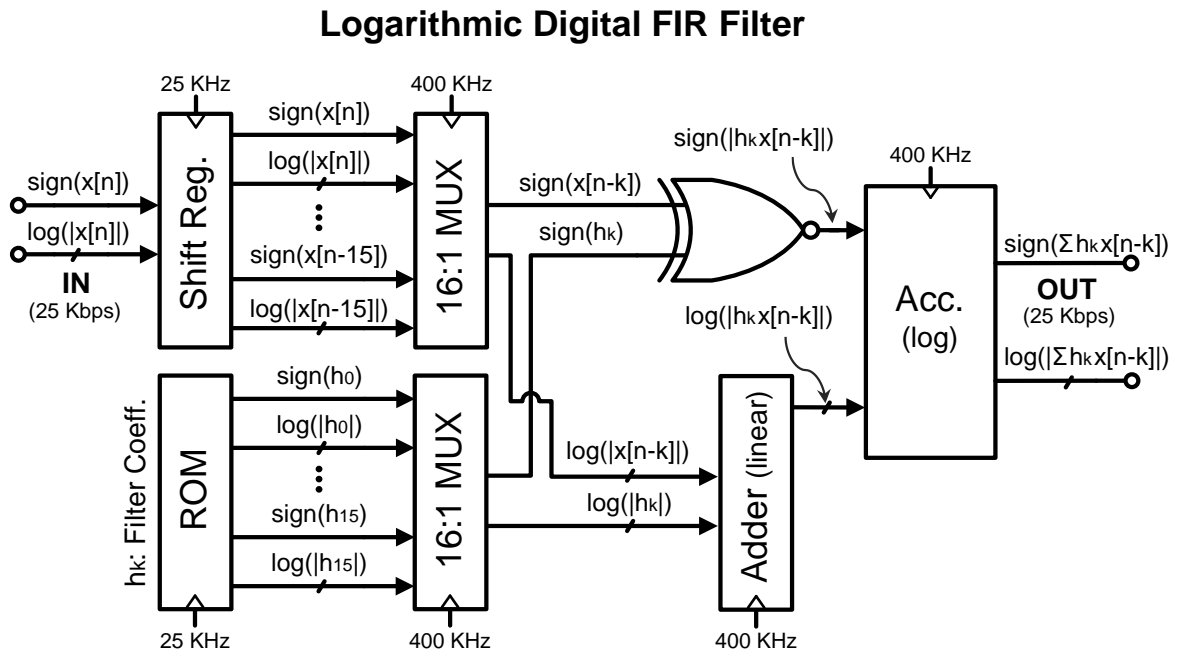


Figure 3.2: Block diagram of digital logarithmic low-pass and high-pass filters.

Figure 3.2 shows a block diagram of the logarithmic digital FIR filters. The entire digital filters run with a 400 kHz clock. Both the LPF and HPF have the same 3dB cutoff frequency of 700 Hz. As mentioned above, the log-filters do not require any multiplier since multiplication in linear-domain is equivalent to addition in log-domain. A simple linear adder multiplies the filter coefficients stored in the ROM and the input bits. A

selective look-up table method is used for logarithmic accumulation of the multiplied values of input and filter coefficients, and if the difference of the two inputs is larger than a threshold, which is 105 in this work, then the output of accumulation is approximated to the larger input, obviating the need for table look-up in this case.

Simulated output spectrums of both a linear 15<sup>th</sup> order FIR LPF and a logarithmic LPF are shown in Figure 3.3. The input signal for this simulation is sample data pre-recorded from a rat's brain. Both output spectrums show suppression of signals at frequency higher than 700 Hz, though the high frequency notches are less noticeable in the logarithmic LPF than the notches in the linear LPF.

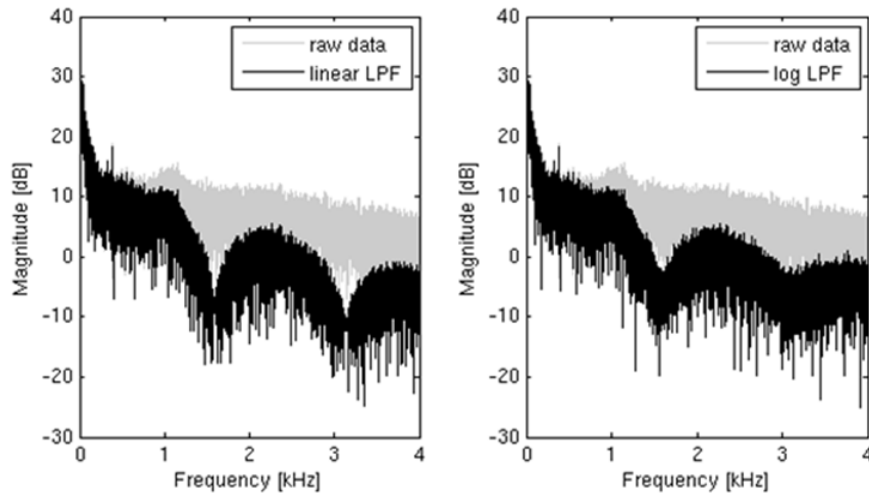


Figure 3.3: Simulated output spectrums of the linear (left) and logarithmic (right) 15<sup>th</sup> order FIR LPF.

In addition, the simulated output spectrums of both a linear 15<sup>th</sup> order FIR HPF and a logarithmic HPF are shown in Figure 3.4. Both output spectrums show suppression of signals at frequency lower than 700 Hz.



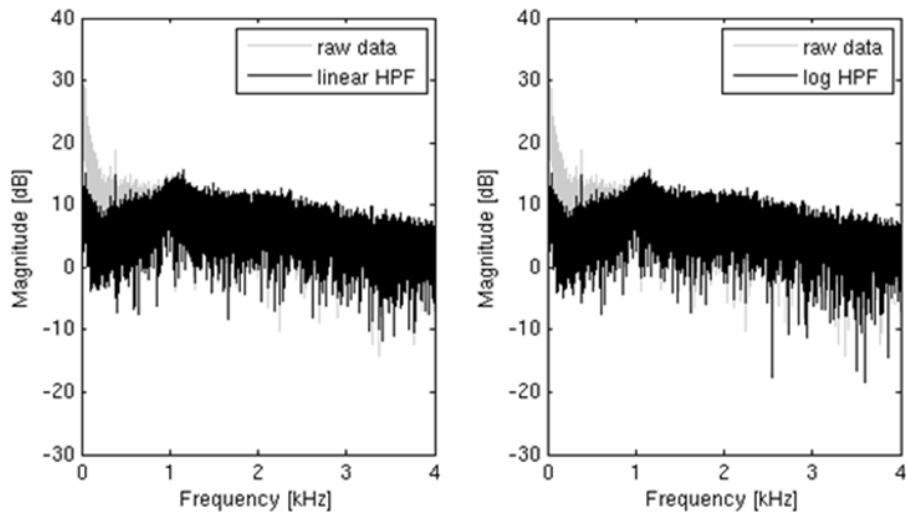


Figure 3.4: Simulated output spectrums of the linear (left) and logarithmic (right) 15<sup>th</sup> order FIR HPF.

A comparison of power consumption of a 8-bit linear-domain digital filter and a 8-bit log-domain digital filter is shown in Figure 3.5. The logarithmic filter consumes 48.5% less power than the linear filter in simulation mainly due to elimination of multipliers.

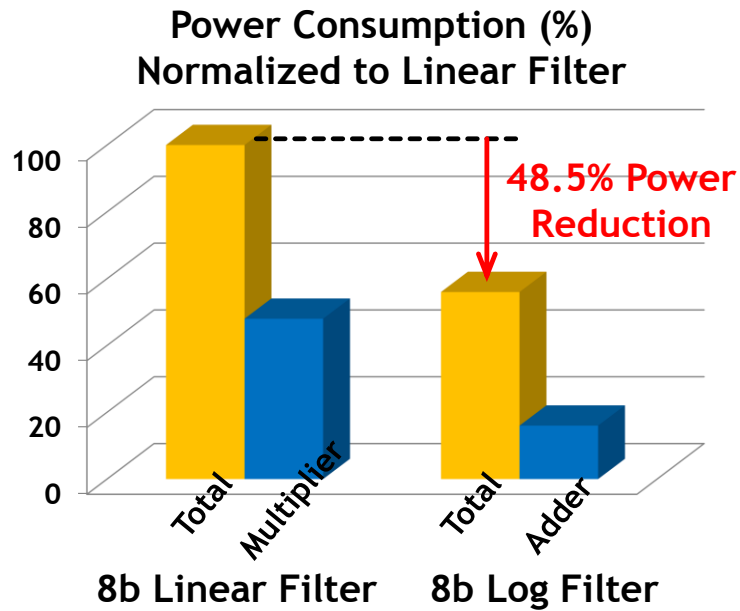


Figure 3.5: Power consumption comparison of a linear-domain and a log-domain 10-bit FIR digital filters.

### 3.3. Closed-loop stimulation controller

Neural signals such as spikes and LFPs have been considered to be the strongest candidate for an indicator of closed-loop DBS. Recently, features of the Local Field Potential (LFP), and in particular the energy of LFPs, have emerged as a more effective feedback indicator for DBS [34]. However, the mechanism of DBS for many neurological diseases is still not fully understood. Therefore, we propose a closed-loop stimulation controller embedded with a generic PI-controller to overcome the lack of understanding the DBS mechanism. The PI-controller determines stimulation parameters in order to optimally suppress abnormal activities in the brain using extracted LFP energy information.

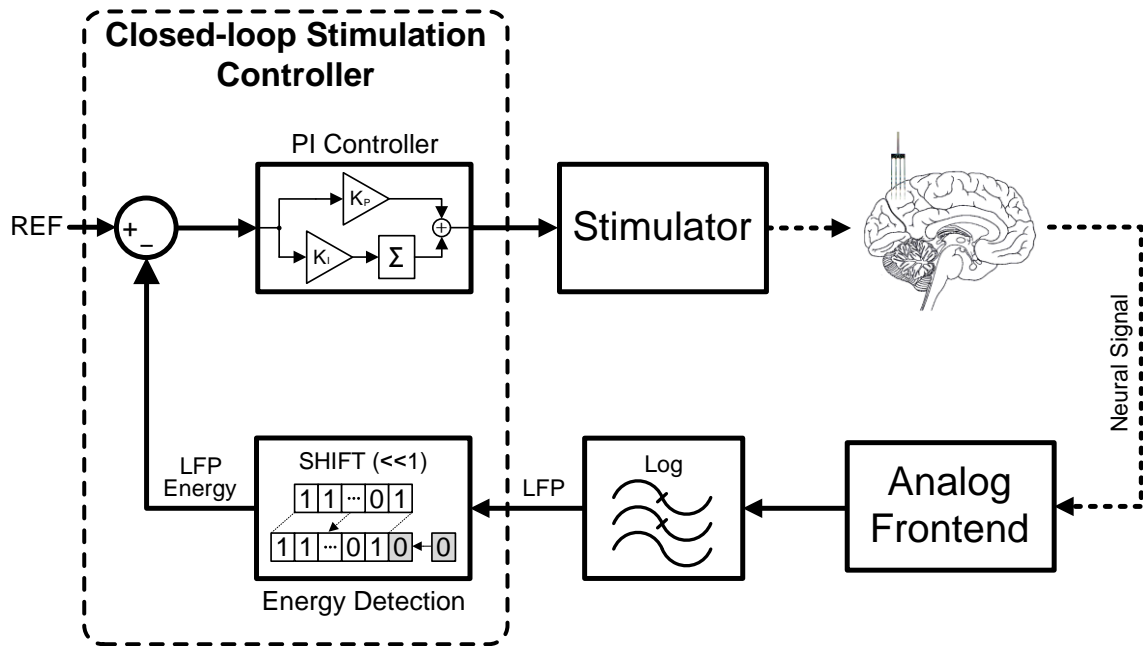


Figure 3.6: Flow diagram of the proposed closed-loop stimulation that uses LFP energy information as a feedback indicator.

A simplified signal flow diagram of the proposed closed-loop DBS system is shown in Figure 3.6. A programmable digital PI-controller optimizes stimulation amplitude based on the energy detected in the filtered LFP signal. Instead of squaring, simple logical 1-bit left-shifting calculates the energy of the log-domain LFP signals due to the logarithmic arithmetic. To generate controller output, the product of controller constants and input is also calculated in log-domain through simple addition.

Figure 3.7 shows simulated outputs of the closed-loop stimulation controller using the LFP signals filtered from a rat's neural data sample as an input. The LFP energy of input neural signals is calculated by the energy detection block and the energy value is compared to a manually set reference value to provide input to the PI-controller. In

summary, the stimulation controller sets the stimulation amplitude depending on the neural activities and a LFP energy reference. For example, as shown in the figure, the closed-loop stimulation controller adjusts stimulation amplitudes when the controller captures LFP energy abnormally different from the reference.

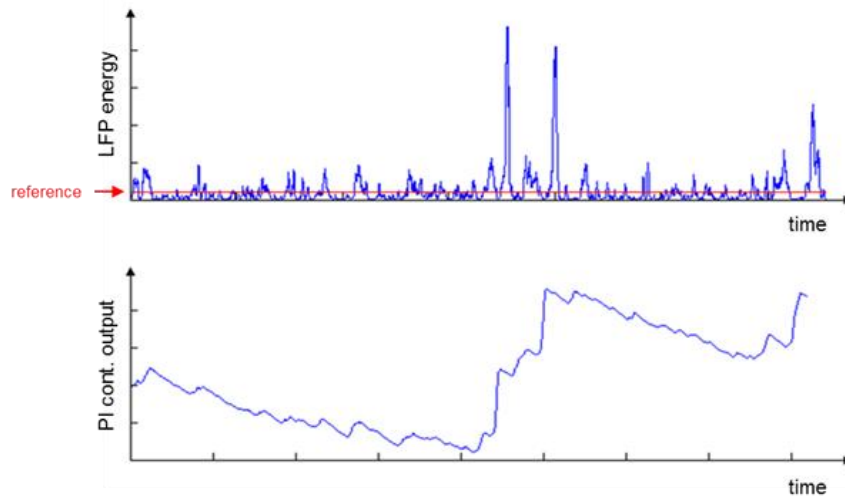


Figure 3.7: Simulated transient input and output of the PI-controller with pre-recorded rat's neural data input.

## Chapter 4

### Design techniques for a power management block<sup>2</sup>

All commercial DBS devices currently available are powered up from batteries. The battery installation inside a human body causes many problems including wire erosion, wire snapping, battery corrosion and periodic surgeries for battery replacement. To reduce the battery related risks, other means to deliver power that do not require a battery is desirable.

There has been a lot of research on delivering power wirelessly to implanted medical devices. Most research has focused to low frequency electromagnetic field in conjunction with inductive coupling to power up the implanted systems [47-51]. The power management block in these systems uses frequencies below 10 *MHz* with an intent to minimize power absorption from tissue. A few works, however, examined the range of frequencies that optimizes power transmission considering tissue absorption by modeling biological tissue as a dispersive dielectric and showed that the optimal frequency for wireless power transfer to implanted devices is in the *GHz* or sub-*GHz* range depending on the size of transmit antenna [52].

In this work, a power management unit comprised of a RF-DC converter (rectifier), two low-dropout regulators (LDOs), and a bandgap voltage generator is

---

<sup>2</sup> The power management block is an assistive but critical part of the system since it provides power to the system. This block is designed by Jaehun Jeong after the specifications of the block is determined.

proposed. A simplified block diagram of the power management unit is shown in Figure 4.1. The power management block is designed to supply  $1.8V$  from a  $915MHz$  carrier to both analog and digital domains of the entire DBS system. An optional  $5V$  battery can be used to operate high-current DACs, which is explained in section 5.1.

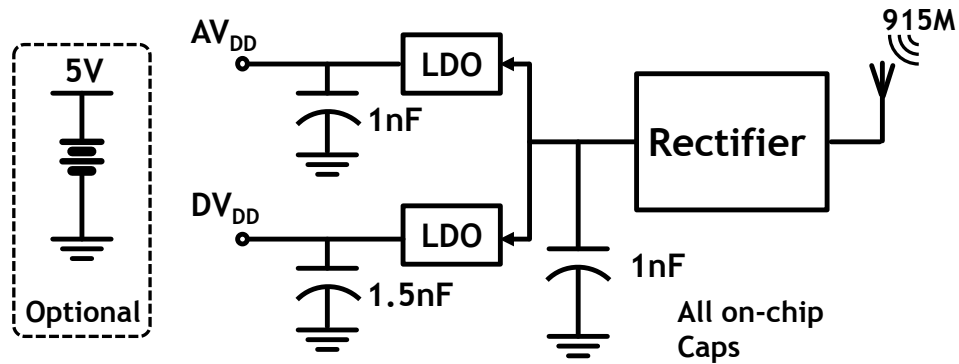


Figure 4.1: Block diagram of the power management block of the closed-loop DBS system that generates both analog and digital supply voltages from a  $915MHz$  carrier.

#### 4.1. RF-DC converter

An RF-DC converter is the first component of the power management block. Input of the RF-DC converter is connected to an antenna that receives a  $915MHz$  carrier. A schematic of the RF-DC converter is illustrated in Figure 4.2. A full-wave self-threshold-compensated rectifier [53] is chosen for its higher power conversion efficiency compared to that of a half-wave rectifier. In addition compared to [53], the body of each FET is tied to the drain for both lower on-resistance and less reverse-biased leakage in this work. The rectifier generates unregulated  $V_{DD}$  of  $2.2V$  and charges  $V_{DD}$  on an on-chip

1nF capacitor. The designed RF-DC converter exhibits a simulated power conversion efficiency of 52% when load current is 350 $\mu$ A.

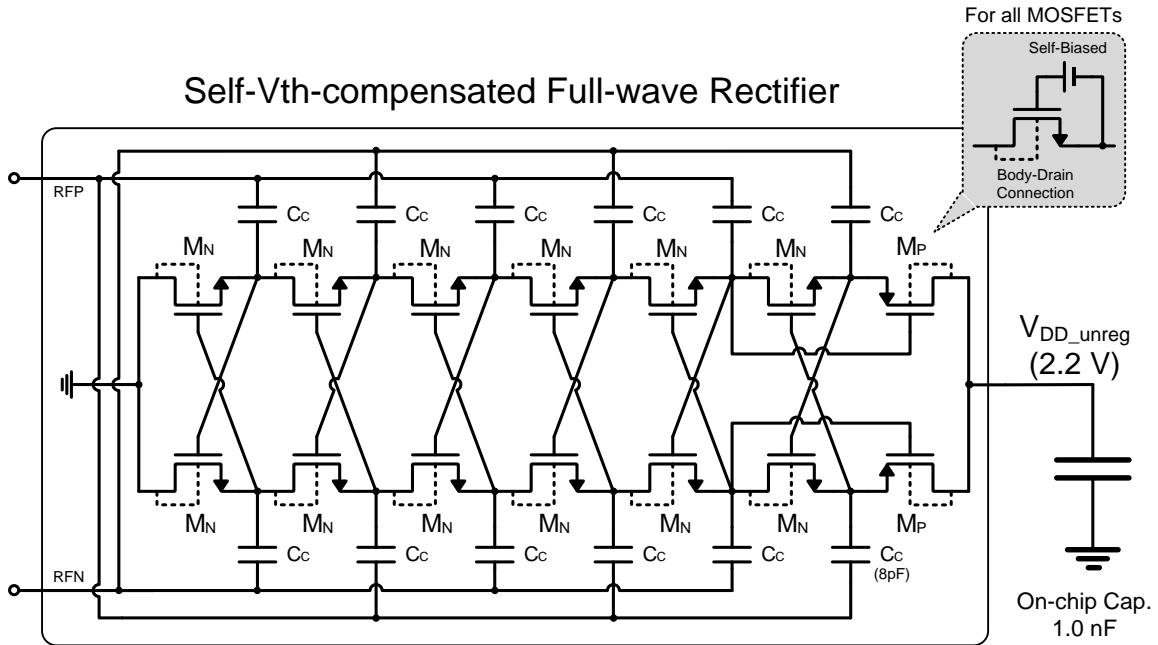


Figure 4.2: Schematic of the full-wave rectifier that generates unregulated  $V_{DD}$  of 2.2 V from a 915MHz carrier.

## 4.2. LDO

Two LDOs are implemented to provide analog  $V_{DD}$  and digital  $V_{DD}$  separately to minimize high frequency interference from digital circuits to analog circuits. A schematic of the LDO of the system is shown in Figure 4.3. The on-chip load capacitors,  $C_L$ , for the analog domain LDO and the digital domain are 1 nF and 1.5 nF respectively. The larger capacitance of digital domain LDO is to tolerate sharp ripples from clocks and digital

signals or any fluctuation in the supply voltage. Since digital circuits cause fluctuation in the supply voltage. Also a larger pass transistor is used in the LDO assigned to digital circuits than that used for the LDO assigned to analog circuits for the same reason. The output voltage,  $V_{DD}$ , is set by the diode ladder and bandgap reference voltage,  $V_{BG}$ .  $V_{DD}$  is set to 1.8 V in this work. The LDOs are designed to be fully on-chip requiring no external on-board passive components to achieve small size and single-chip operation capability of the proposed closed-loop stimulation system. An indirect compensation capacitor,  $C_C$ , is used to provide a high frequency path to stabilize the circuits.

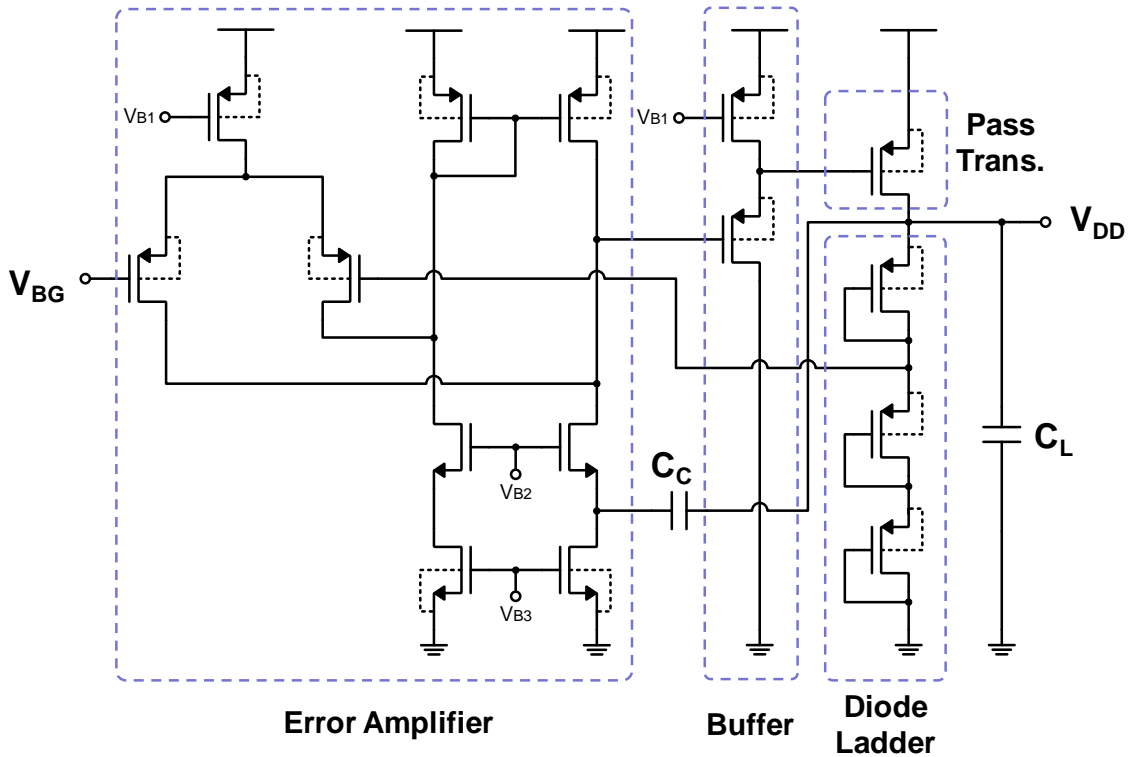


Figure 4.3: Schematic of the LDO for analog domain voltage supply.



The pass transistor dimensions and load capacitance value of the LDOs are given in Table 4.1.

Table 4.1: Pass transistor dimensions and load capacitance values of the LDOs.

	<b>Pass transistor dimension (<math>W/L</math>)</b>	<b>Load capacitance (<math>C_L</math>)</b>
LDO for Digital	$40\ \mu m / 180nm$	$1.5\ nF$
LDO for Analog	$20\ \mu m / 200nm$	$1.0\ nF$

### 4.3. Bandgap voltage reference

To enable a truly self-contained single-chip system for closed-loop DBS, the system needs an on-chip voltage reference that is highly stable and tolerable to process, voltage or temperature variations. Due to its superior tolerance of bandgap reference to any of these variances, a bandgap reference is implemented in our work to serve as the most stable voltage reference point throughout the entire system [54]. A schematic of the bandgap reference circuits is shown in Figure 4.4. The bandgap reference circuits consist of start-up circuitry, a simple active mirror-loaded amplifier and its replica bias, and bandgap core circuitry using substrate PNP BJTs. The bandgap reference block generates 1.3 V bandgap reference voltage,  $V_{BG}$ , insensitive to process, supply voltage, and temperature variations.

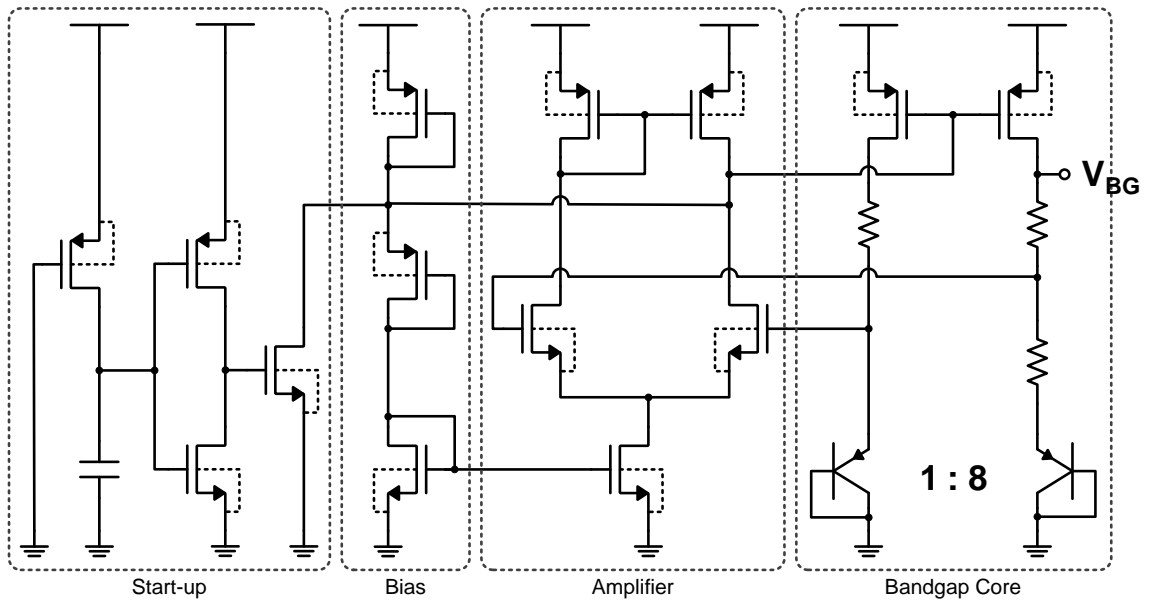


Figure 4.4: Schematic of bandgap reference circuits.

## Chapter 5

### **Design techniques for other building blocks: current stimulator, clock generator, and RF transceiver**

Other important functional blocks for the proposed closed-loop neurostimulation system are described in this chapter. First, a programmable current stimulator that generates biphasic pulse stimulation current is described. Design of an on-chip sub-*MHz* clock generator to provide low-jitter clock to the system while consuming small area and low power is also discussed. Lastly, an RF transceiver that communicates recorded data to external system to extend research and receives control signals and system variables is designed in this work and implementation of the RF transceiver is discussed.

#### **5.1. Current stimulator**

There are two different types of neurostimulation in general: voltage type stimulation and current type stimulation. The clinical efficacy of voltage type stimulation may decrease gradually as the impedance of implanted electrodes increases due to a reactive tissue response [55]. Therefore a current stimulation is selected for this work because of the stable amount of charge injection against fluctuation of load impedance. Also biphasic stimulation is chosen to avoid tissue damage caused by residual charge. These choices we made for the type of stimulation lead to a set of stimulation parameters

such as amplitude, pulse width and stimulating frequency (repetition rate) of stimulation current. In this work, those three parameters are controlled digitally with 6-bit resolution.

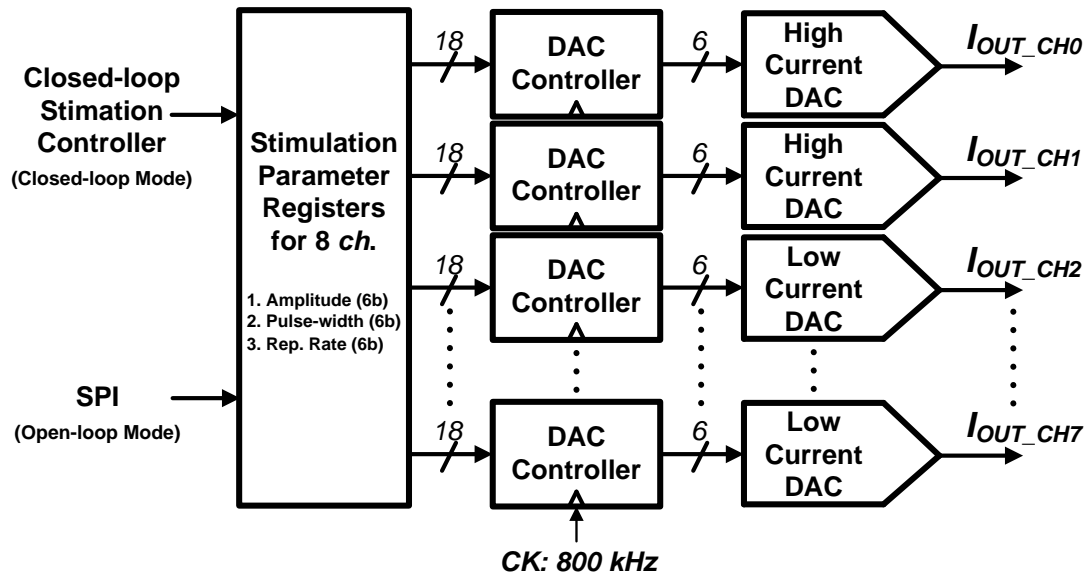


Figure 5.1: Simplified block diagram of 8-channel current stimulator.

Figure 5.1 shows a block diagram of the designed 8-channel current stimulator. The current stimulator is comprised of three parts: eight 6-bit current steering digital to analog converters (DACs), dedicated DAC controllers for each current DAC, and stimulation parameter registers. Stimulation parameters are either set by the closed-loop stimulation controller or manually by a user through an SPI interface or the RF receiver, depending on the stimulation mode (i.e. closed-loop mode or open-loop mode). DAC controllers control current DACs according to the stimulation parameter valued stored in the parameter registers to generate biphasic pulse current. In addition, to support a variety of stimulation probes, six general-purpose DACs are designed to drive current up to 116

$\mu A$ , and two high-current DACs can drive up to  $4.2\text{ mA}$ . The high current DACs is capable of driving miniature LEDs for optogenetic applications as well as DBS probes. Because of the high current drive capability, the high current DACs are designed to operate with a  $5V$  supply. A triple cascode current-steering DAC is chosen for its output impedance leading to high linearity and high supply rejection.

To span the range of clinical efficacy to variety of neurological disorders, the pulse width range is set between  $5\ \mu s$  and  $320\ \mu s$ , and repetition rate range is set between  $31\text{ Hz}$  and  $1000\text{ Hz}$  as suggested from an early study [56]. Ranges of stimulation parameters are summarized in Table 5.1.

Table 5.1: Summary of ranges of stimulation parameters.

	<b>Amplitude</b>	<b>Pulse-width</b>	<b>Repetition Rate</b>
High-current DAC	$0 - 4.2\text{ mA}$	$5 - 320\ \mu s$	$31 - 1000\text{ Hz}$
General-Purpose DAC	$0 - 116\ \mu A$	$5 - 320\ \mu s$	$31 - 1000\text{ Hz}$

## 5.2. Clock generator

For stand-alone operation of a small-sized implanted device, the system needs a low-power on-chip generated clock signal. An LC based oscillator doesn't suit this application because the size of inductor needed to achieve a clock speed of sub- $MHz$  is impractically large. On the other hand, a RC based relaxation oscillator can be designed with much smaller silicon area compared to the LC oscillator, but with a trade-off of degraded jitter performance.

A source-coupled multivibrator is one of the most popular relaxation oscillator in CMOS technology because of its simple structure and small number of circuit components. The source-coupled multivibrator has been used extensively in sub- $MHz$  digital electronics. However, as with all the other relaxation type oscillators, it usually suffers from its high phase noise. Thus, in this work, a source-coupled multivibrator is implemented to generate  $800\text{ kHz}$  on-chip clock signal for the entire system.

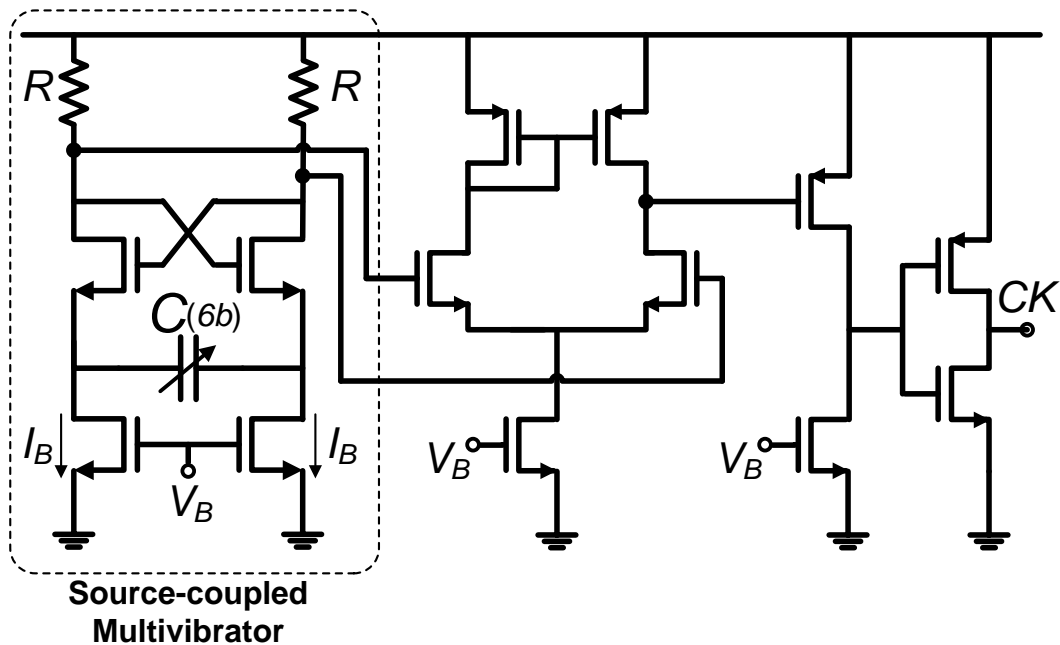


Figure 5.2: Schematic of clock generator.

Figure 5.2 shows a schematic of the clock generator. A two-stage amplifier and an inverter follow the source-coupled multivibrator to provide a rail-to-rail clock. To minimize the ADC performance degradation from jitter at minimal power consumption, the clock generator is designed to consume  $60\ \mu W$  from  $1.8\text{ V}$  supply. To provide an

accurate 800 kHz output, even with significant process variation, a 6-bit digitally controlled capacitor array is implemented in the design. A resistance value,  $R$ , of 34.8 k $\Omega$  and a nominal capacitance value,  $C$ , of 7.04 pF are chosen. The clock generator exhibits a cycle-jitter of 176 ps in simulation, which is good enough not to impact the ADC performance.

### 5.3. RF Transceiver<sup>3</sup>

In many biomedical devices, it is helpful to have a means to communicate with an external system wirelessly. The purpose of the communication can be sending recorded data to the external system for further research, or receiving system parameters to control the implanted biomedical system. However, power consumption for communication needs to be minimized in most cases where the system operates from a battery or wireless powering. Due to the power constraint of implanted neurostimulation systems, wireless communication for DBS system should not consume power too much to accelerate battery drainage. In many RFID applications where no dedicated power source is connected to an RFID transponder, backscatter type communication scheme is used for its extremely low power consumption and design simplicity on the transponder side [57].

In this work, a backscatter type RF transceiver is designed to broaden the utility of the closed-loop stimulation system for further research on recorded neural data. An 800 kbps power-efficient backscatter RF transmitter communicates recorded LFP, spike

---

<sup>3</sup> The layout of the RF transceiver block is done by Jeffrey Fredenburg.

or raw data wirelessly to a receiver outside a human body. The RF transceiver also enables manual setting of stimulation parameters and system parameters.

Figure 5.3 depicts a block diagram of the RF transceiver. The transceiver is a half-duplex type that works as a receiver or a transmitter depending on a digital mode control bit, RX\_EN. The transmitter simply consists of digital buffers and a switch transistor for impedance modulation. The receiver works based on pulse-width modulation (PWM) scheme. The transceiver is designed to give a power consumption of  $5 \mu W$  with  $1.8 V$  supply in both transmitter and receiver mode.

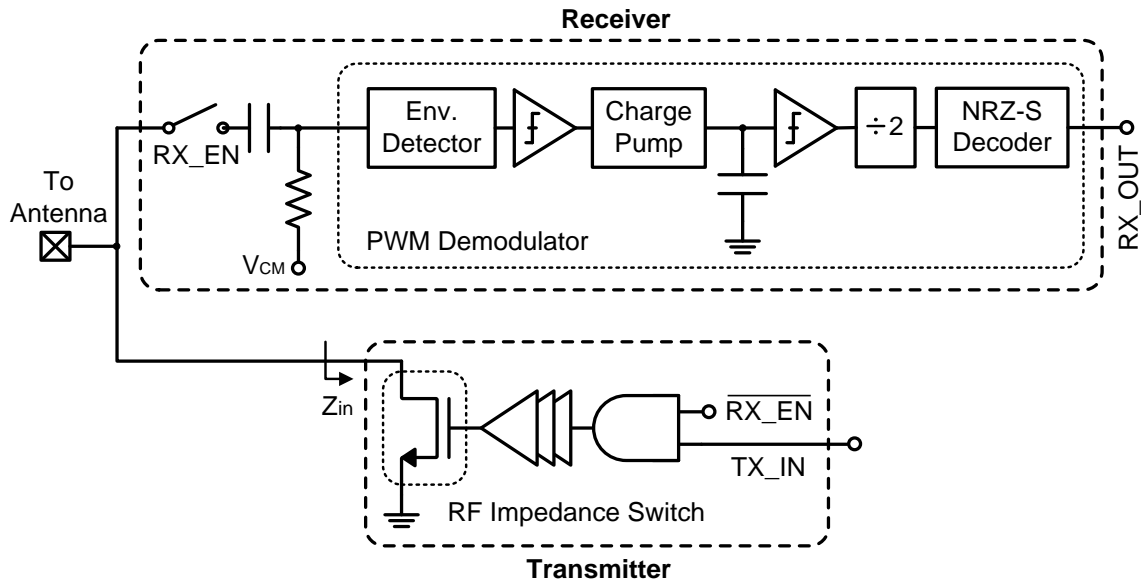


Figure 5.3: Block diagram of RF transceiver.

Communication protocol for the RF transceiver is implemented as shown in Figure 5.4. The receiver detects 6-bit address and 6-bit data after a 10-bit preamble. When the transmitter is set to send raw data, the transmitter sends 8-bit raw data from



two channels in one sequence of data stream. When the transmitter is set to send only LFP or spike signals, the transmitter sends 12-bit LFP or spike data from a single recording channel.

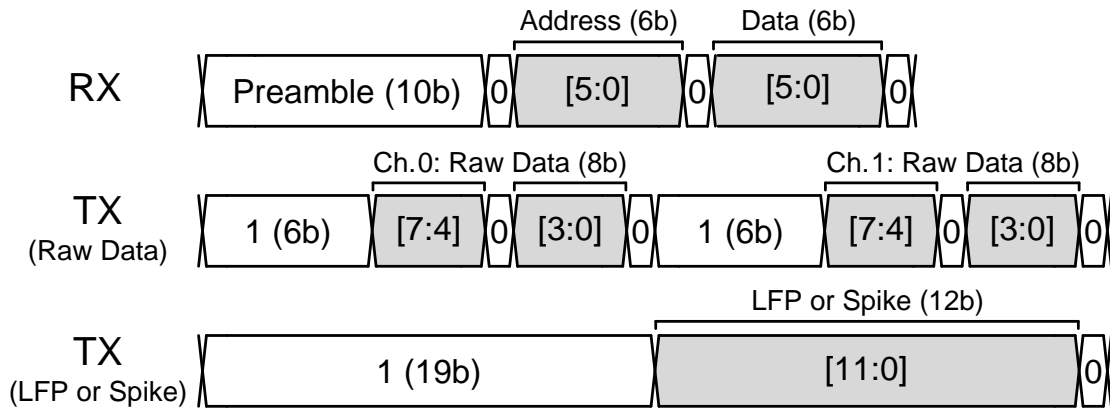


Figure 5.4: Communication protocol for RF telemetry.

## Chapter 6

### Prototype system and performance measurements

In this chapter, we present a single-chip log-based wirelessly-powered closed-loop DBS System with RF telemetry. The closed-loop DBS system optimizes stimulation parameters by analyzing measured LFP energy. To broaden the utility of this system for research, the platform also incorporates extensive two-way telemetry, filtering of spike and LFP signals, as well as support for electrical and optical stimulation for optogenetic research.

#### 6.1. Proposed closed-loop DBS SoC architecture

As shown in Figure 6.1, the prototype system incorporates more functionality and includes several design innovations compared to prior works. Since neural signals are efficiently expressed in logarithmic scale due to its high dynamic range, we introduce a complete log-domain neural recording and processing chain. Four band-pass LNAs filter and amplify neural signals before these signals are multiplexed to a 100 kSample/s 8-bit pipeline logarithmic ADC. A new log-ADC scheme eliminates the dead zone in earlier log-ADC architectures. Furthermore, log-domain digital filtering is introduced in this work to directly process the log scale digital output from the ADC, saving power

consumption by avoiding digital multiplication. Similarly, thanks to log-domain processing, the DSP calculates LFP energy by simple bit-shifting instead of squaring.

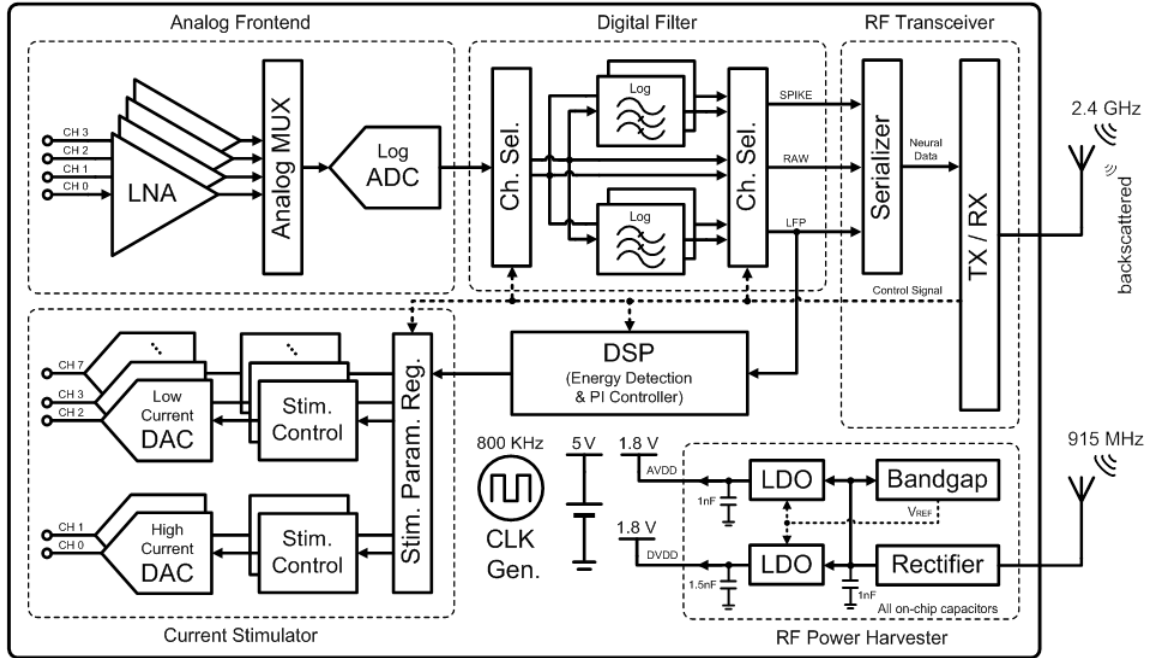


Figure 6.1: Overall system block diagram of the proposed log-based closed-loop DBS system.

This work also introduces a programmable closed-loop digital PI-controller that applies the LFP energy information to set the optimal stimulation amplitude. The stimulation parameters can also be set manually in open-loop mode via an on-chip RF transceiver. To further facilitate research, an 800 *kbps* power-efficient backscatter RF transmitter communicates recorded LFP, spike or raw data wirelessly to an external receiver for further analysis. Unlike most other integrated systems, the prototype supports a variety of stimulation probes. A stimulation controller sets the amplitude, phase and repetition rate of eight charge-balanced biphasic multi-function stimulation channels. Six

of these are 6-bit low-current ( $116 \mu A$ ,  $1.8 V$ ) channels to drive microelectrodes, while two 6-bit high-current ( $4.2 mA$ ,  $5 V$ ) channels support DBS probes. The high current channels can also drive miniature LEDs for optogenetic applications. Except for the high current high-voltage channels, which require battery power, the entire system is powered from energy recovered by an efficient RF-DC converter from a  $915 MHz$  carrier. The single-chip device incorporates two fully on-chip LDOs, a bandgap reference, bias circuitry and a low jitter clock generator for true standalone operation with no external circuit components.

The prototype log-based closed-loop DBS system is fabricated in  $180nm$  CMOS. Fig. 6.2 shows a die micrograph of the prototype system. The total area (excluding only I/O pads) is  $2 \times 2 mm^2$ . The prototype run from a  $915 MHz$  carrier signal generating  $1.8 V$  supplies to entire block of the system. This work was funded in part by the Catalyst Foundation.

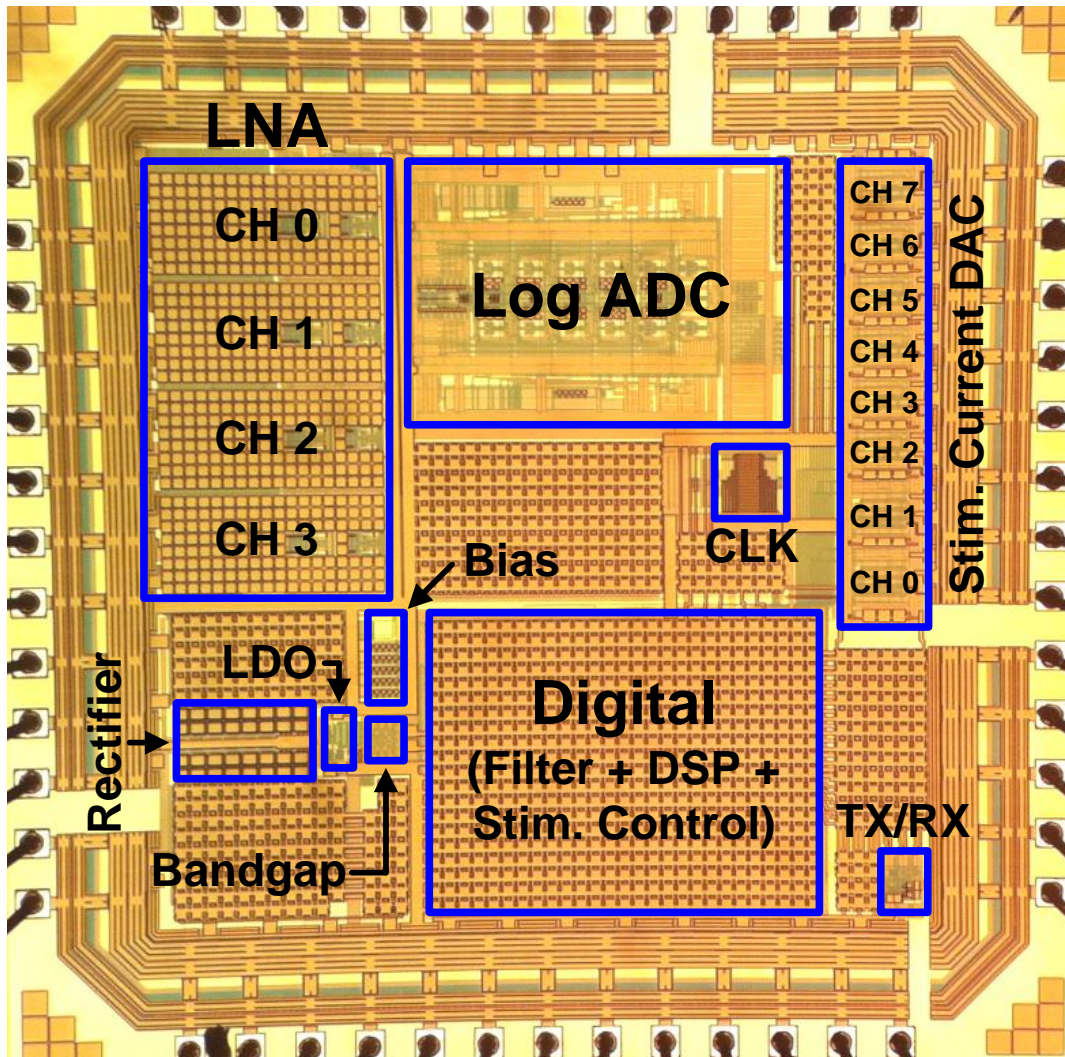


Figure 6.2: Die micrograph of the prototype log-based closed-loop DBS system.

## 6.2. Prototype measurement results

### 6.2.1. AFE: 4-channel LNAs and a log-ADC

The LNAs are comprised of a cascade of two active band-pass filters and achieve a measured gain of  $54\text{ dB}$  over a passband from  $0.64\text{ Hz}$  to  $6\text{ KHz}$ . The log-ADC improves on that in [40] by removing the dead zone, where small signals are compressed below the quantization range. The function  $Y = 0.9|V_{in}/V_{range}| + 0.1$  is applied within the SHA to remove this dead zone without losing DR.

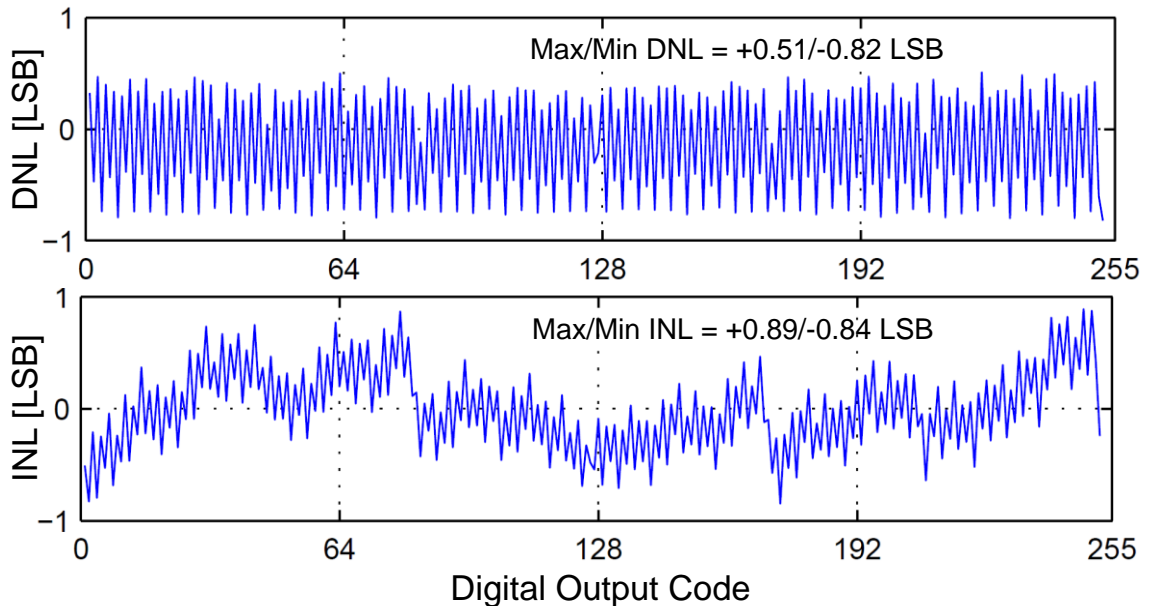


Figure 6.3: Measured DNL and INL of the designed AFE (4-ch. LNAs + log ADC).

The measured DNL/INL of AFE is shown in Figure. 6.3. For the DNL/INL and output spectral measurement of AFE, signals with amplitude of  $1.2\text{ mV}$  are applied. The

maximum DNL/INL is 0.82 *LSB*/0.89 *LSB*. The maximum SNDR of the AFE (4-*ch.* LNAs and log-ADC combined) is 35.5 *dB*.

The measured output spectrum of AFE is shown in Figure. 6.4. The SNDR of the AFE (4-*ch.* LNAs and log-ADC combined), is 35.5 *dB* at an input frequency of 170.898 *Hz*.

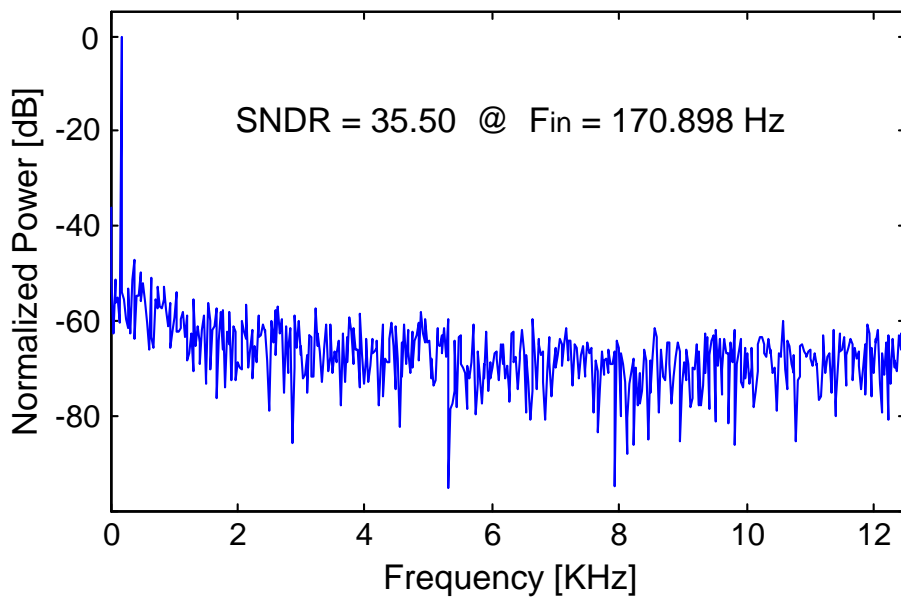


Figure 6.4: Measured output spectrum of the designed AFE (4-*ch.* LNAs + log ADC).

### 6.2.2. Logarithmic digital filters

Two sets of 15<sup>th</sup> order digital FIR low-pass and high-pass filters are implemented to separate the low-frequency LFPs and the high-frequency spikes from the digitized neural data of two channels simultaneously. We take advantage of the logarithmic output of the ADC to introduce efficient log-domain filtering.

An input signal with amplitude of  $1.2mV$  is applied for testing and Figure 6.5 shows the measured frequency response of the recording path (AFE and digital logarithmic filters combined). Both the LPF and HPF have the same  $3\text{ dB}$  cutoff frequency of  $700\text{ Hz}$ .

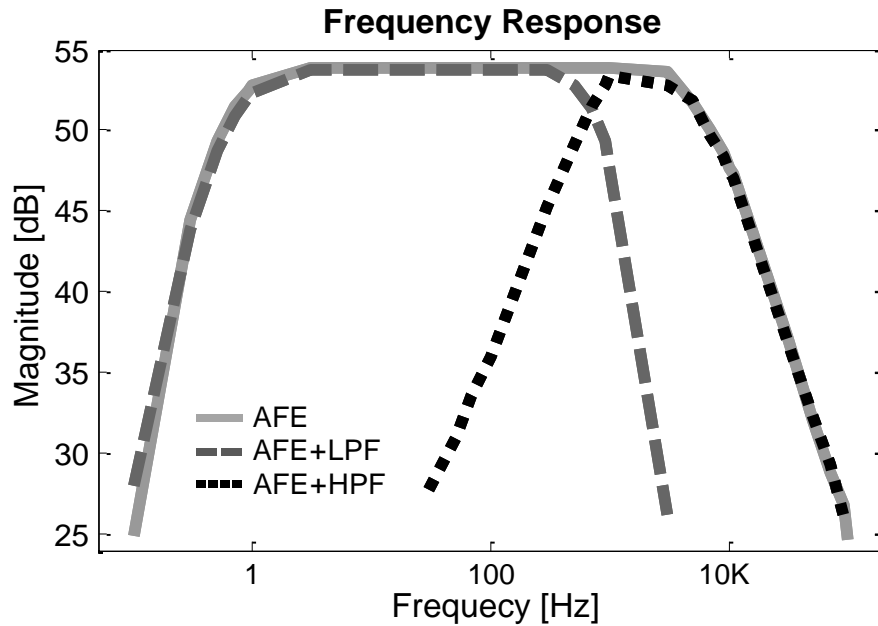


Figure 6.5: Measured frequency response of the designed recording path (AFE + digital log-filters).

As mentioned above, the log-filters do not require any multiplier since multiplication in the linear-domain is equivalent to the addition in the log-domain. A look-up table is used for logarithmic accumulation, and if the difference of the two inputs is larger than a threshold, then the output of accumulation is approximated by the larger input obviating the need for table look-up in this case.



Measured LFP and spike recordings of a (pre-recorded) neural signal from a rat's brain are also shown in Figure 6.6. The system demonstrated extraction of clean LFPs, spikes, and raw signals.

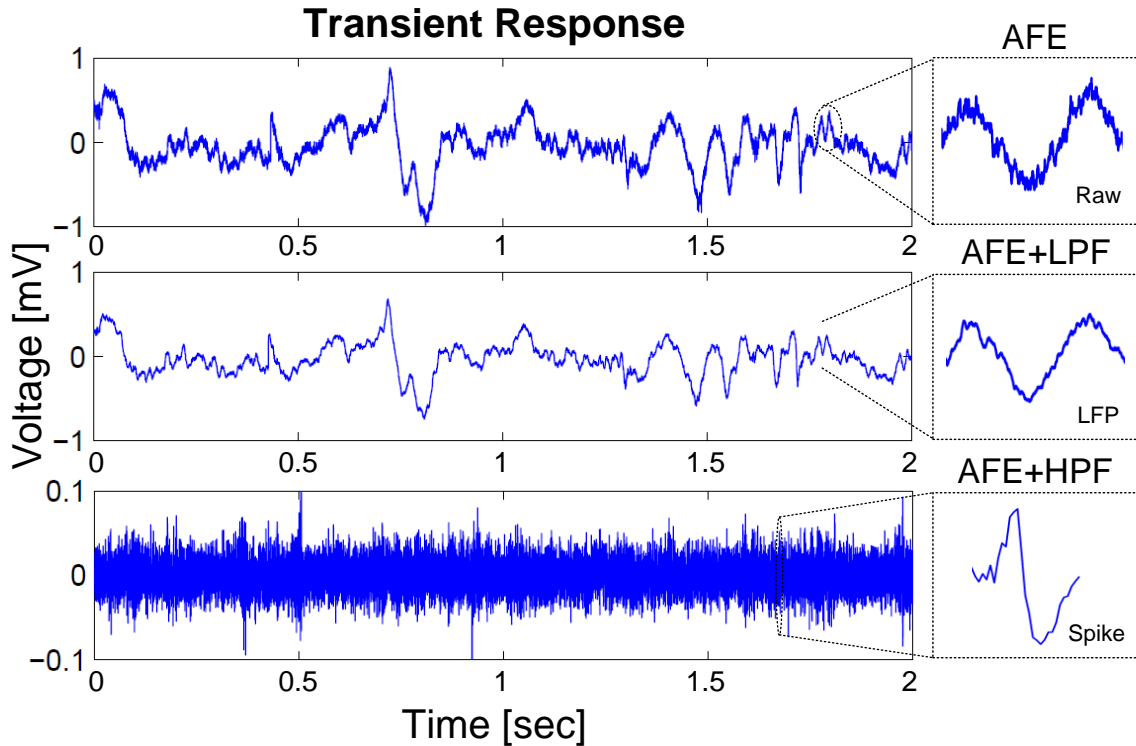


Figure 6.6: Recorded output of the designed recording path (AFE + digital log-filters) with a pre-recorded neural signal from a rodent's brain applied as input to the system.

### 6.2.3. Current stimulator

The proposed system has two modes for stimulation: open-loop and closed-loop mode. In open-loop mode, SPI interface or wireless communication sets the stimulation parameters (amplitude, duty cycle, and repetition rate) of eight charge-balanced biphasic

multi-function stimulation channels. In closed-loop mode, a stimulation controller sets the stimulation parameters. Six of these are 6-bit low-current ( $116\mu\text{A}$ ,  $1.8\text{V}$ ) channels to drive microelectrodes, while two 6-bit high-current ( $4.2\text{mA}$ ,  $5\text{V}$ ) channels support high-current probes. The high current channels can also drive miniature LEDs for optogenetic applications.

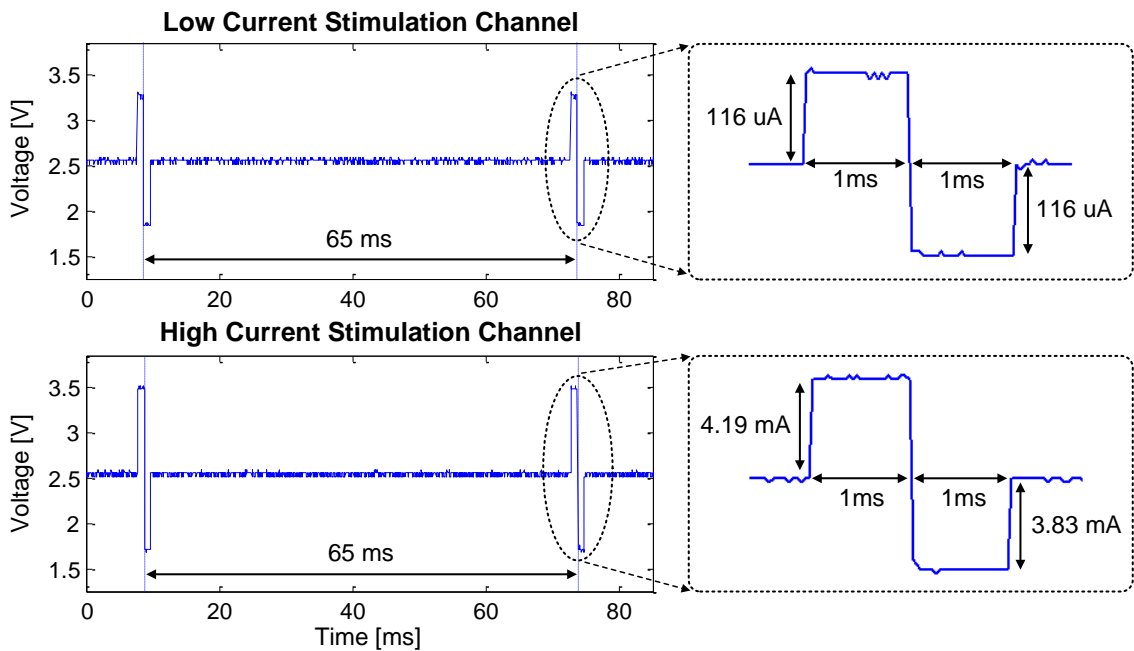


Figure 6.7: Measured stimulation current waveforms of low-current and high-current stimulation channels with  $6.23\text{ k}\Omega$  and  $220\ \Omega$  respectively.

Figure 6.7 shows measurements of a stimulation current pulse train in open-loop mode. Due to the coarse resolution of the testing oscilloscope, the accuracy of measured current waveforms is limited to  $4\ \mu\text{A}$ . Both current stimulation channels show a pulse-width of  $1\ \text{ms}$  and a repetition rate of  $15.4\ \text{Hz}$ . There was a design mistake in the DAC

controllers and the pulse-width and the repetition rate is not programmable and they can be set only to 1 ms and 15.4 Hz, respectively. Amplitudes of a low-current channel and a high-current channel are 116  $\mu\text{A}$  and 4.19 mA, respectively.

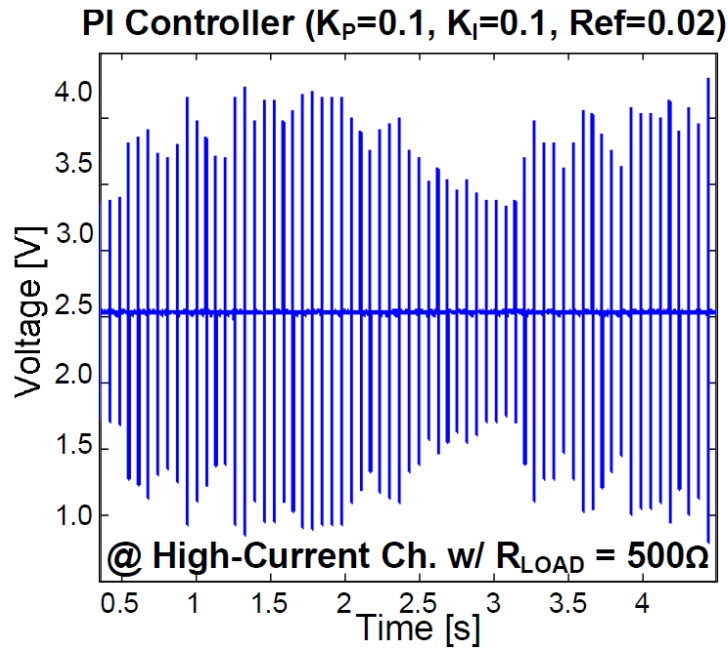


Figure 6.8: Measured stimulation current waveforms of a high-current stimulation channel in closed-loop mode using LFP energy detection with a 220  $\Omega$  resistor load.

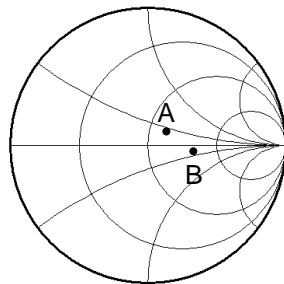
Figure 6.8 shows a measurement of a stimulation current pulse train of a high-current stimulation channel in closed-loop mode. The system in closed-loop mode adapts the stimulation current in real-time responding to the energy of input LFP signals.

#### 6.2.4. RF transceiver

Backscattering modulation is exploited to minimize power consumption of transmitted neural data. The receiver demodulates a PWM signal to set the PI constants of the PI-controller, stimulation parameters, and system parameters.

The measured modulated impedance of the backscatter transmitter is shown in Figure 6.9. Due to the large parasitic capacitance from a I/O pad and a lack of matching network on the testing printed circuit board (PCB), the impedance values for two different states differ by only  $45^\circ$ .

#### $Z_{in}$ Change by Backscattering Modulation



$$\text{A: } Z_{in} = 69 + 15j \\ (\text{TX\_IN} = 0)$$

$$\text{B: } Z_{in} = 109 - 13j \\ (\text{TX\_IN} = 1)$$

Figure 6.9: Measured input impedance changed from backscatter modulation of the transceiver.

Figure 6.10 shows a measured output spectrum of the backscatter transmitter with 2.4 GHz carrier signals incident on the transmitter with -15 dBm input power. Even with only angle difference of  $45^\circ$ , measured output spectrum of backscatter transmitter still clearly shows 800 kbps data transmission.

## Spectrum of Backscattered Signal

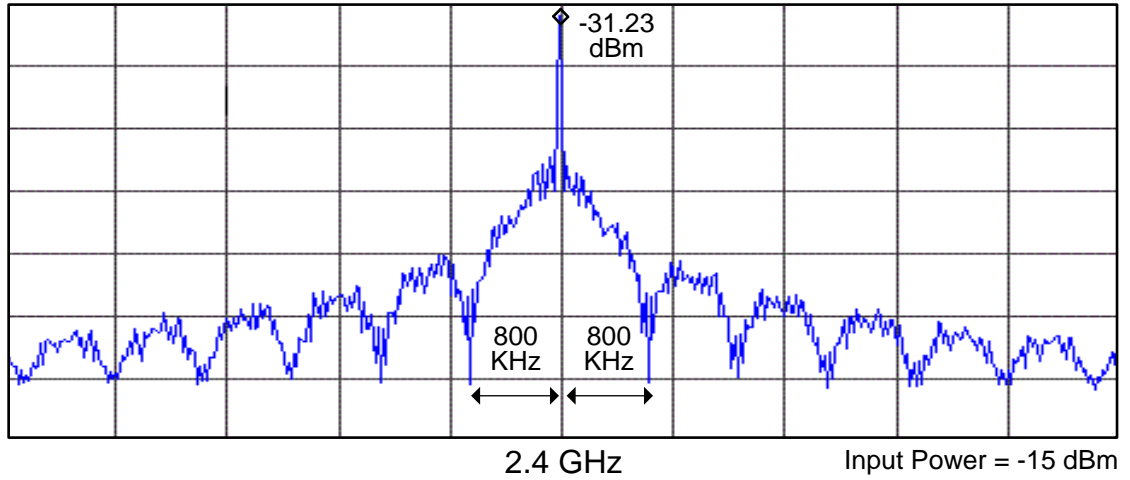


Figure 6.10: Measured output spectrum of the backscatter transceiver.

Reflected output signals from the transmitter are down-mixed with a 2.4 GHz carrier and recovered to a data bit-stream as shown in Figure 6.11. The output bit-stream clearly shows 800 kbps data transmission.

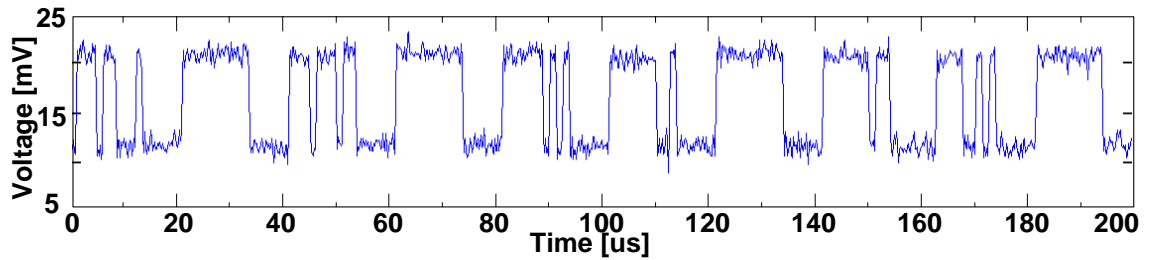


Figure 6.11: Measured recovered data bit-stream from the backscatter transmitter.

### 6.2.5. System power consumption

The system is entirely powered by RF power from a 915 MHz carrier using the power management block that consists of a full-wave rectifier, a bandgap reference and two fully on-chip LDOs except for the high-current DACs which require 5V battery.

The power consumption of each block is summarized in Table 6.1. The total power consumption of the system is 468μW.

Table 6.1: Power breakdown of the prototype system.

<b>Part</b>	<b>Power Consumption</b>	<b>Condition</b>
LNA	16 μW/ch.	-
Log-ADC	180 μW	-
High-Current Stimulation Ch.	50 μA/ch.	4.2 mA amplitude, 1 ms pulsewidth, 15.4 Hz repetition rate.
Low-Current Stimulation Ch.	3 μA/ch.	116 μA amplitude, 1 ms pulsewidth, 15.4 Hz repetition rate.
Digital (Filters+Stim. Controller)	138 μW	All four filters (two LPFs and two HPFs) are active.
RF Transceiver (TX/RX)	5 μW / 4.6 μW	One of TX and RX active at a time.
Clock Generator	60 μW	800 kHz clock output.
<b>Total</b>	<b>468 μW</b>	All 6 low current stimulators are active with 116 μA amplitude.

## **Chapter 7**

### **Conclusions**

In this thesis, the background of several important neurological movement disorders and epilepsy are reviewed and both DBS and closed-loop DBS as means of treatment of the neurological disorders are discussed. Following the discussion, a log-based single-chip closed-loop neurostimulation system is proposed.

Design techniques for a recording path that includes LNAs and a logarithmic pipeline ADC are described. A two-stage structure is adopted for LNAs to implement high gain band-pass amplifiers at minimum power cost. A logarithmic ADC is used to digitize neural signals in small number of bits while preserving the high DR characteristic of neural signals.

Subsequently, design techniques for a logarithmic DSP unit that includes logarithmic digital FIR filters and a closed-loop stimulation controller are presented. The logarithmic DSP unit does not require a power hungry multiplier to perform multiplication, which leads to significant reduction of power consumption. The closed-loop stimulation controller involves a PI-controller to set optimal stimulation parameters.

A power management unit is designed to gather power from a  $915\text{MHz}$  carrier signal. This wireless powering scheme obviates the need for battery and reduces the risk from battery implantation inside a human body. The power management unit includes an RF-DC converter and two LDOs, and it generates supply voltage to both analog and

digital domains of the entire system. Also the power management unit is fully on-chip and enables the fully self-contained SoC operation.

Lastly, design techniques for other important circuit blocks including current stimulators, RF telemetry, and a clock generator are presented. For low-power consumption, a backscatter type transmitter is proposed as a part of the RF telemetry, and source-coupled multivibrator is proposed for clock generation.

In this chapter, we conclude the work described in this thesis with a summary of the prototype performance and a list of contributions by this work. Finally, a few possible future works are suggested.

### **7.1. Summary of the prototype performance**

The system performance of the prototype is summarized in Table 7.1. We note good DNL/INL results of the AFE, the maximum of which is smaller than 1LSB even with 54 *dB* gain bandpass amplifiers placed in front of the log-ADC. The 4-channel AFE consumes 245  $\mu W$ . The current stimulators output maximum DAC currents as designed. The entire digital circuit blocks consume 138  $\mu W$  from 1.8 V supply. Given that the clock speed of the digital blocks is slower than 1MHz, even more reduction of power consumption would be possible by reducing the supply voltage while maintain the functionality of the digital processing unit. The RF transceiver consumes only a fraction of total power and avoids any overload of power to the implanted DBS system. The system is fabricated in 180nm CMOS technology to take advantage of the low leakage property of the technology.



Table 7.1: Prototype performance summary.

<b>AFE</b>	
LNA Gain	54 dB
LNA 3dB Passband	0.64 Hz – 6 kHz
Logarithmic ADC Sampling Rate	100 kSample/s
AFE Max DNL/INL	0.82 LSB / 0.84 LSB
AFE SNDR	35.5 dB @ 170 Hz
AFE Power Consumption	245 $\mu$ W
<b>Current Stimulator</b>	
Maximum Current of High/Low Current DAC	$\pm 4.18$ mA / $\pm 116$ $\mu$ A
Charge Unbalance of High/Low Current DAC	< 9% / < 0.1%
Amplitude Resolution	6-bit
Repetition Rate	15.4 Hz
Pulse Width	1 ms
<b>Digital Filters + Stimulator Controller</b>	
Clock Frequency	400 kHz
3dB Cutoff Frequency of LPF / HPF	700 Hz / 700 Hz
Power Consumption	138 $\mu$ W
<b>RF-DC Converter</b>	
Carrier Frequency for Power Harvesting	915 MHz
Simulated Rectifier Power Conversion Efficiency	52% @ $I_{Load} = 350$ $\mu$ A
<b>RF Transceiver</b>	
Communication Scheme of TX / RX	Backscatter / PWM
Carrier Frequency for RF Communication	2.4 GHz
Data Rate TX / RX	800 kbps / 100 kbps
Power Consumption TX / RX	5 $\mu$ W / 4.6 $\mu$ W
<b>Clock Generator</b>	
Output Frequency	800 kHz
Simulated Cycle Jitter	176 ps
Power Consumption	60 $\mu$ W
<b>Total Power Consumption</b>	<b>468 <math>\mu</math>W</b>
<b>Technology</b>	<b>180nm 1P6M CMOS</b>
<b>Die Size (excluding pads)</b>	<b>2 x 2 mm<sup>2</sup></b>

## 7.2. Contributions

This section summarizes the contributions of this work.

- First fully self-contained wirelessly-powered closed-loop DBS SoC that does not require any off-chip component other than two antennas for wireless-powering and RF communication is proposed and implemented. The wireless powering scheme eliminates the need for a battery and reduces the risk of implanted device.
- Closed-loop DBS based on the analysis of LFP signal energy is proposed and implemented. A PI-controller is implemented inside the closed-loop stimulation controller to best accommodate the current situation where no DBS mechanism has been clearly found yet.
- Logarithmic digitization of neural signals and log-domain digital signal processing is proposed and implemented. This technique improves power consumption of the system due to the reduced number of bits and elimination of multipliers.
- Low-power two-way wireless interface is included in the DBS system. The wireless transceiver adds flexibility to the device and extends the functionality of the system.

### 7.3. Future work

Due to the lack of understanding the mechanism of closed-loop DBS, a PI-controller with LFP energy information is implemented in this work. To overcome the lack of understanding even better, implementation of an on-chip micro-controller or FPGA in the system to store and execute an arbitrary algorithm for closed-loop DBS is proposed for future work. This will also enhance the flexibility of the system extending the system's applications to different kinds of neurostimulation beyond DBS.

It is also proposed to implement two complete different recording channels in the system for LFP and spike signals for future work. Since the LSB size of a logarithmic ADC becomes larger as input becomes larger, small-amplitude spike signals are recorded with very coarse LSB size when large LFP signals are incident on neural probes with the spike signals at the same time. Exploiting the two-stage structure LNAs, which is implemented already in the system, it would be easy to split to two recording paths with different AFE gains for LFP and spike signals. The separated recording paths will provide independence between the recorded LFP and spike signals.

Although a pipeline topology is exploited in the logarithmic ADC of this work, as in general, power consumption of the ADC was larger than that of the state of the art work [49]. The successive approximation (SAR) ADC has been dominant for slow to moderate speed, low power applications because of its superior low power consumption. Thus, for future work, a closed-loop DBS SoC embedded with a logarithmic SAR ADC is proposed. If a logarithmic scale architecture can be applied to the structure of the SAR ADC efficiently as in the case of the pipeline ADC, the logarithmic SAR ADC will

reduce the power consumption of the entire system. When accompanied by low supply voltage design of the digital block, power consumption of the entire system can be improved further.

An on-chip antenna is also another possible future work. If on-chip antennas are implemented, the RF performance will be enhanced to a great extent by elimination of performance degradation from impedance mismatch at I/O pads or package pads. This will also ease the system design flow since only the models of the antennas need to be added to the given technology libraries.

## **Appendices**

## **Appendix A. Printed circuit board for the closed-loop neurostimulation SoC prototype**

Figure A.1 shows the I/O pads of the closed-loop neurostimulation SoC prototype.<sup>4</sup> As indicated by different shading, there are four different power domains: analog, digital, optional battery, and testing buffer powers. Table A.1 describes functions of each pad. It is worth noting that there is no dedicated 3.3V pad supply voltage source since this SoC is intended for implanted device running from one RF carrier signal. Instead 1.8V analog and digital supplies generated inside the SoC and 2.2V supply voltage generated from the RF-DC converter are used for 3.3V pad supply voltage. The power domain for testing is only powered up when the system uses a output buffer to send out recorded neural signals for testing, and it is entirely turned off when the system is using RF transceiver to send out recorded data. The 5V battery power domain is only used when high-current DACs are active, and only 3.3V pad supply voltage is used even then.

---

<sup>4</sup> Many discussions with Jeffrey Fredenburg led to the final power planning of the chip that involves four different power supplies and their dedicated I/O pad 3.3V supplies.

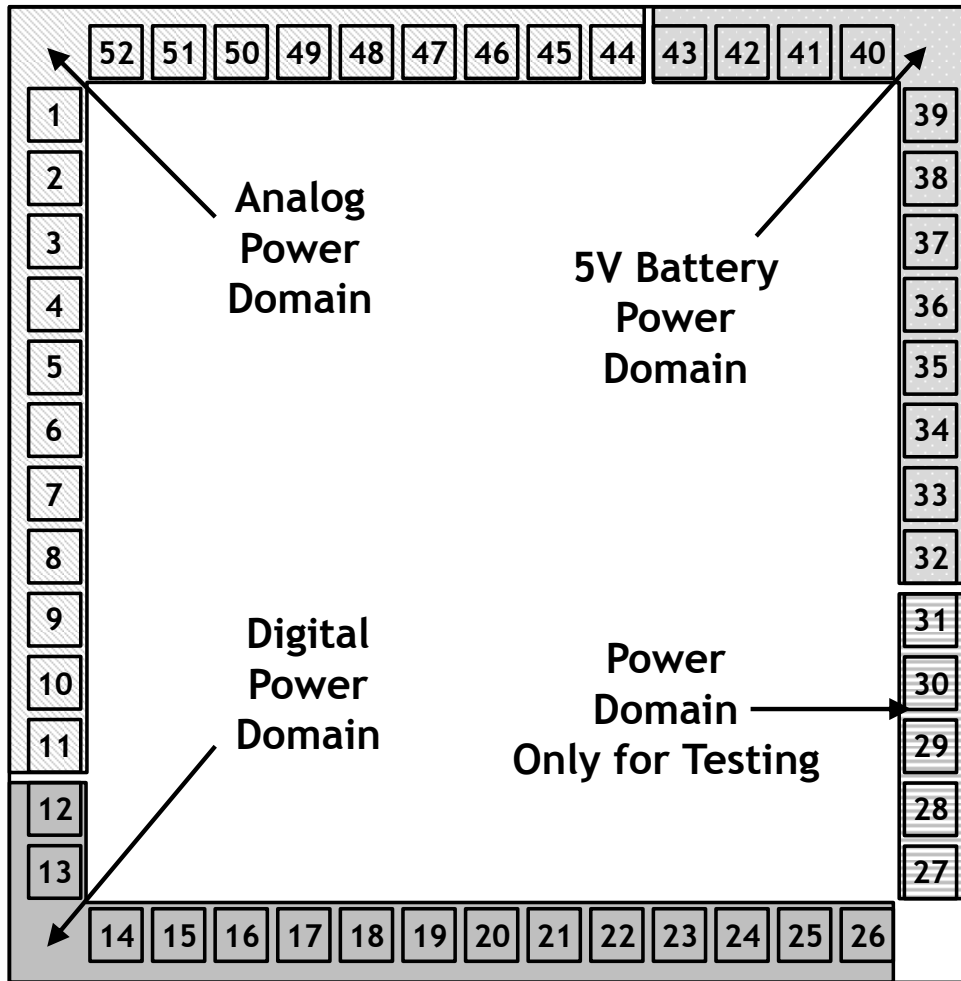


Figure A.1: IO pad of the closed-loop neurostimulation SoC prototype.

Table A.1: IO pad information of the closed-loop neurostimulation SoC prototype

Pin No.	Mnemonics	I/O	Description
1	AVDD	Power	1.8V analog supply (generated inside the chip)
2	IN3	Analog	Neural input: channel-3
3	AVSS	Ground	1.8V analog ground
4	IN2	Analog	Neural input: channel-2
5	INM	Analog	Neural input: common ground
6	IN1	Analog	Neural input: channel-1
7	IN0	Analog	Neural input: channel-0

<b>Pin No.</b>	<b>Mnemonics</b>	<b>I/O</b>	<b>Description</b>
8	CK_EXT	Digital In	External clock signal only for testing
9	AVDD33	Power	3.3V analog supply (supplied from 1.8V analog supply voltage)
10	RECT_INN	Analog	Negative input to RF-DC converter (connected to matching network for antenna)
11	RECT_INP	Analog	Positive input to RF-DC converter (connected to matching network for antenna)
12	DVDD33	Power	3.3V digital supply (supplied from 2.2V RF-DC converter output)
13	DVSS33	Ground	3.3V analog ground (connected to AVSS)
14	SEL_CK_EXT	Digital In	0: Use on-chip clock source, 1: Use external clock source (CK_EXT)
15	RSTB_DIG	Digital In	0: Reset all digital blocks, 1: Turn on all digital blocks
16	USE_CLOOP	Digital In	0: Open-loop stimulation mode, 1: Closed-loop stimulation mode
17	USE_DESER	Digital In	0: Use SPI to set system parameters. 1: Use RF receiver to set system parameters.
18	SCLK	Digital In	SPI clock 1
19	CS	Digital In	SPI chip-select
20	SIN	Digital In	SPI input
21	SPI_CLK	Digital In	SPI clock 2
22	RX_EN	Digital In	0: Transmitter mode, 1: Receiver mode
23	TX_USE_ANT	Digital In	0: Use output buffer to read recorded neural data. 1: Use RF transmitter to read recorded neural data.
24	DVSS	Ground	1.8V digital ground
25	DVDD	Power	1.8V digital supply (generated inside the chip)
26	ANT_DATA	Analog	In/out of RF transceiver (connected to matching network for antenna)
27	TX_OUT	Digital Out	Output buffer for testing
28	TVSS	Ground	1.8V ground for testing



<b>Pin No.</b>	<b>Mnemonics</b>	<b>I/O</b>	<b>Description</b>
29	TVDD33	Power	3.3V supply for testing
30	TVSS33	Ground	3.3V ground for testing (connected to TVSS)
31	TVDD	Power	1.8V supply for testing
32	IOUT0	Analog	Stimulation current output: channel-0
33	IOUT1	Analog	Stimulation current output: channel-1
34	IOUT2	Analog	Stimulation current output: channel-2
35	IOUT3	Analog	Stimulation current output: channel-3
36	IOUT4	Analog	Stimulation current output: channel-4
37	IOUT5	Analog	Stimulation current output: channel-5
38	IOUT6	Analog	Stimulation current output: channel-6
39	IOUT7	Analog	Stimulation current output: channel-7
40	BVSS33	Ground	3.3V ground for 5V battery power domain (connected to BVSS)
41	BVDD	Power	1.8V supply for 5V battery power domain (not used)
42	BVSS	Ground	1.8V ground for 5V battery power domain
43	BVDD33	Power	3.3V supply for 5V battery power domain (connected to 5V battery)
44	AVSS	Ground	1.8V analog ground
45	AVSS	Ground	1.8V analog ground
46	AVDD	Power	1.8V analog supply (generated inside the chip)
47	AVDD	Power	1.8V analog supply (generated inside the chip)
48	RSTB_LNA	Digital In	0: Turn off LNAs. 1: Turn on LNAs.
49	IBIAS	Analog	Optional bias current for fine tuning (never used for any measurement)
50	AVSS	Ground	1.8V analog ground
51	AVDD	Power	1.8V analog supply (generated inside the chip)
52	AVSS33	Ground	3.3V analog ground (connected to AVSS)

The closed-loop DBS SoC prototype is packaged with 56-pin QFN package grounding four left pins, and connected to corresponding pads of PCB through a 56 pin socket. A four-layered FR4 printed circuit board (PCB) is chosen for testing the chip. The top and bottom layers are mostly used for signal routing. They and middle two layers are used to provide four different power domains (analog, digital, testing, and 5V battery power domains) to the chip. The grounds of those power domains are connected through beads to share the same DC ground and to decouple disturbances at the same time.  $1nF$  ceramic capacitors are used near the socket area, and  $10\mu F$  tantalum capacitors are used near the SMA connectors for decoupling. It is worth noting that attenuators are used in front of LNAs because the minimum amplitude of waveform generators used to provide neural input signals was  $20mV$  which is too large for neural signal amplitude. Thus attenuators are placed in front of LNAs to generate signals with amplitude of  $1.2mV$ .

A schematic of the PCB for the closed-loop DBS SoC prototype is shown in Figure A.2. Table A.2 lists parts used to build the PCB for testing. Figure A.3 shows a photograph of the PCB.



Table A.2: Parts list for PCB

Description	Purpose
Antenna 916MHz 1/4 wave SMA	Antennae for wireless powering
Antenna 2.45GHz 1/4 wave SMA	Antennae for RF communication
6.23k $\Omega$ resistor	Load emulation for general-purpose DACs
220 $\Omega$ resistor	Load emulation for high-current DACs
0 $\Omega$ resistor	Jumper
Connector header 2pos gold	Connector to a logic analyzer
Terminal 12 port	Connection port for digital control signals including SPI connection
Bead	Decoupling
Capacitor 1nF 50V ceramic	Decoupling
Tantulum 10 $\mu$ F 50V ceramic	Decoupling
Balun	900 MHz balun to give differential input to RF-DC converter
30dB Attenuator	To generate small amplitude signals for LNA input
Slide swith spdt 2pos J hook	Switch for stimulation control

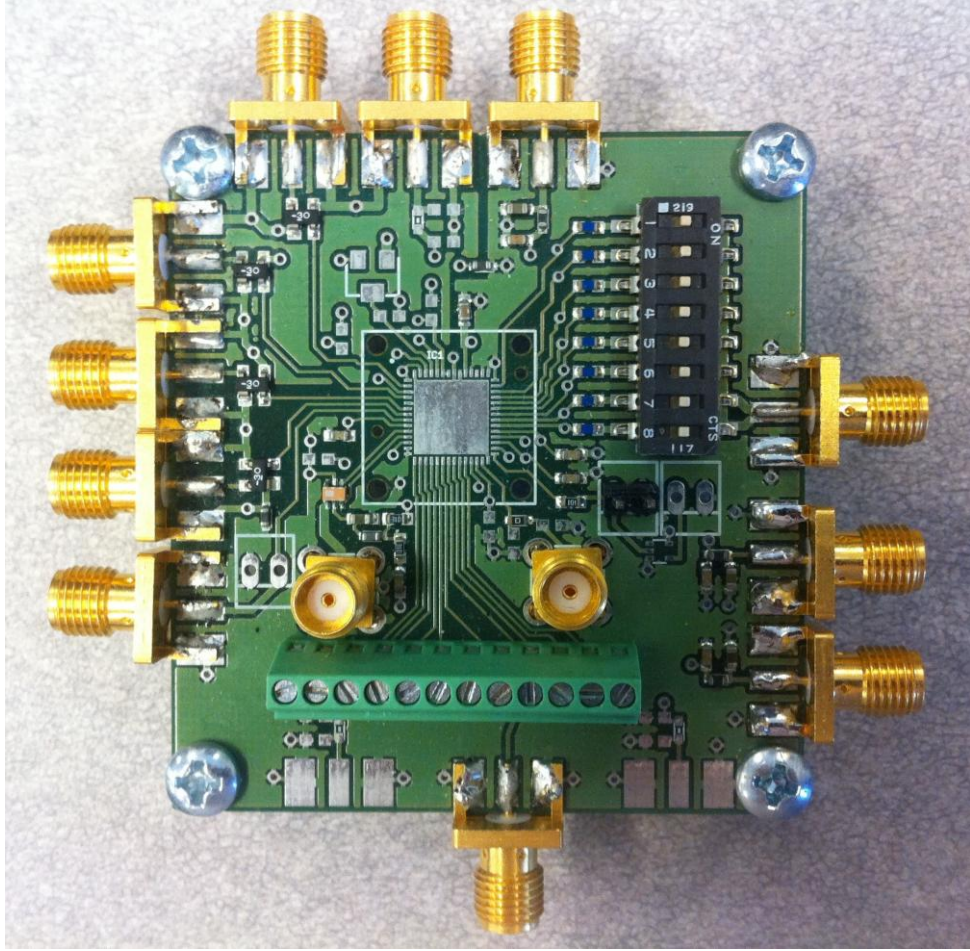


Figure A.3: PCB photograph.

## **Appendix B. A 22Gb/s, 10mm On-chip Serial Link over Lossy Transmission Line with Resistive Termination**

This section describes my other doctorate research work to investigate a simple yet efficient way for long distance on-chip communication. An on-chip serial-link scheme incorporating an interleaved voltage-mode driver, interleaved samplers and an optimally resistively terminated transmission line, enables an energy-efficient very-high-speed long-range data communication. The link is more than twice as fast and more than twice as energy efficient as the fastest reported on-chip link, yet has more than triple the communication range. A 10mm prototype link achieves a data rate of 20Gb/s with an energy consumption of 1.36pJ/b and a measured BER better than  $10^{-11}$ . A 10Gb/s prototype achieves an energy efficiency of 680fJ/b with a measured BER of better than  $10^{-13}$ .

### **B.1. Introduction**

Global interconnect has suffered from technology scaling in terms of latency, power consumption, bandwidth and the complexity of floorplanning. Several techniques have been presented to improve global signaling, but these suffer from high latency, limited bandwidth [58-61], design complexity of equalization circuits [60], and the need for placement of negative impedance converters along interconnect lines [62]. An on-chip transmission line with pulsed current-mode signaling offers higher bandwidth (8Gb/s),

but achieves much less bandwidth density than densely packed wires employing repeaters [63]. A resistively-terminated transmission line link reported in [64] achieves a data rate of  $9Gb/s$  but consumes  $600mW$ .

We present a global on-chip serial link scheme that achieves high data rates, low latency, and high bandwidth through serial communication over an optimally-terminated lossy transmission line. Optimum resistive termination eliminates dispersion in a lossy link to enable a single long ( $> 10mm$ ) wire bandwidth of more than  $20GHz$  and eliminate the need for transmit or receive equalization. Improved transmitter, receiver and link design improves the energy efficiency by a factor of 37 compared to the  $9Gb/s$  resistively-terminated link in [64]. An efficient interleaved voltage mode transmitter drives the line. Digital-like, interleaved, voltage mode drivers are used for simplicity, speed and energy efficiency. Interleaved  $10GS/s$  comparators sample the received signal at an optimum phase dictated by a digitally controlled sampling clock. Compared to [64-65], better link design enables a wire width reduction from  $8\mu m$  to only  $2\mu m$ . The prototype  $22Gb/s$  is fully self-contained and self-testing. We also present a  $10Gb/s$  prototype that is optimized for lower speed.

We present measured data from two prototypes implemented in  $65nm$  CMOS; one optimized for high-speed operation and the other optimized for low-power. The high speed  $10mm$  link achieves a measured energy-per-bit of  $1.36pJ/b$  at  $20Gb/s$  and an estimated latency of  $54ps$  over a  $10mm$  link. The  $10Gb/s$   $10mm$  link achieves a measured energy-per-bit of  $680fJ/b$  at  $10Gb/s$ . The total receiver and transmitter circuit area for the  $22Gb/s$  prototype is only  $2450\mu m^2$ .

## B.2. System Architecture

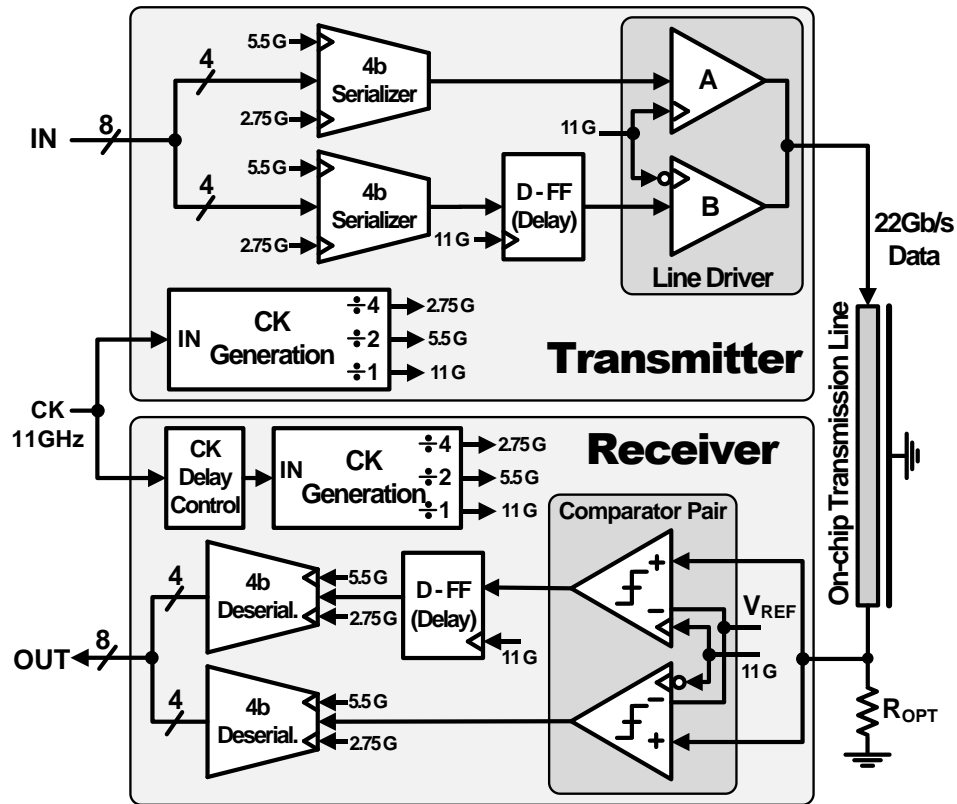


Figure B.4: Transceiver architecture with an on-chip transmission line link terminated with optimal resistance.

Figure B.4 illustrates the overall system. The transmitter, shown on top of Figure B.4, serializes 8b parallel input data and two interleaved drivers launch data over a lossy on-chip transmission line. Termination of the transmission line with optimum resistance permits signal transmission over the high frequency Transverse Electro-Magnetic (TEM) mode. This termination scheme eliminates dispersion and enables high bandwidth communication while suppressing inter-symbol interference (ISI) [65]. A digitally-controlled delay chain sets the optimal sampling time at the receiver. A pair of



interleaved comparators in the receiver samples the received signal. The recovered data is converted to CMOS logic levels and deserialized to an 8b parallel data stream.

The transmitter consists of a voltage-mode driver, two 4b to 1b serializers and a clock generation block. A pair of digital-like interleaved voltage-mode drivers (A and B in Figure B.5) launches serial data on to the transmission line. To simplify the driver circuitry and to allow the use of conventional static CMOS, two interleaved tri-state drivers, operating at 11GHz, feed 22Gb/s data to the lossy transmission line. A voltage-mode scheme is chosen to achieve a large voltage amplitude at the receive-end, enabling better noise immunity and easier decisions by receiver, compared to current mode schemes. The interleaved voltage mode driver requires only a single clock (i.e. CK and its complement CK\_B) running at half the total data rate. Driver A drives the line only while the clock is high and driver B drives the line when the clock is low.

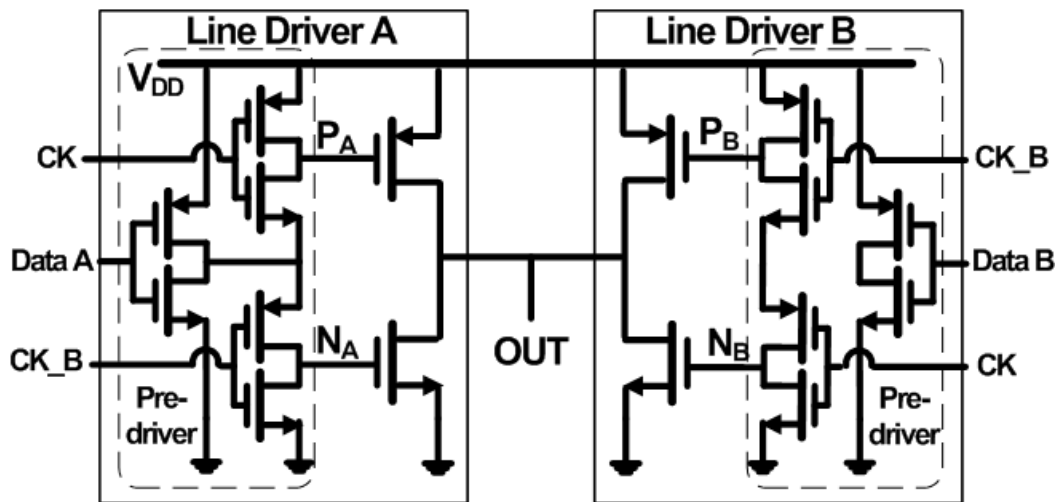


Figure B.5: Interleaved voltage-mode line drivers: A, B.

The pre-drivers (indicated in the dashed boxes in Figure B.5) enable just one of the four PMOS and NMOS driver devices depending on the polarity of the data.

As shown in the upper half of Figure B.4, the transmitter serializes 8b parallel data and launches the serial data onto the lossy on-chip transmission line. 8b 2.75Gb/s parallel data is first serialized to two interleaved 11Gb/s data streams by two 4b to 1b serializer. The voltage-mode line driver follows and serializes the two 11Gb/s streams to a single 22Gb/s data stream. To facilitate interleaved operation at the line driver, a half clock period delay is introduced in one of the 11Gb/s data streams.

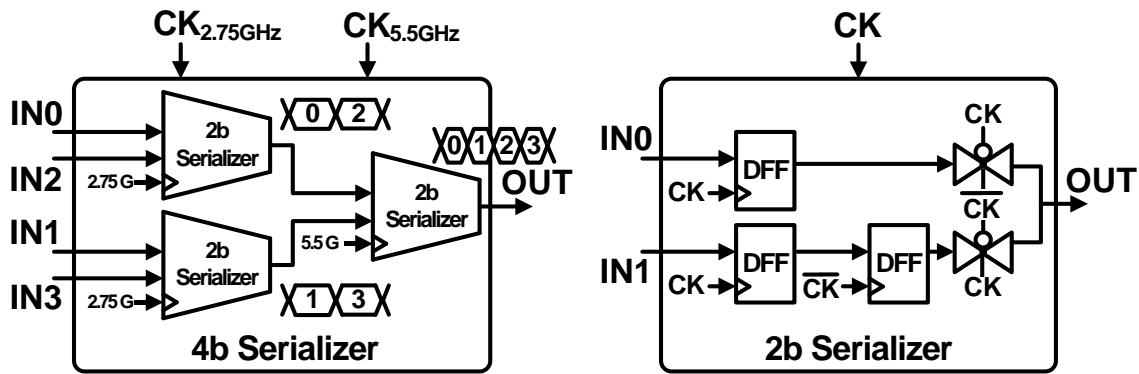


Figure B.6: Block diagrams of 4b-to-1b serializer and 2b-to-1b serializer.

A block diagram of the 4b to 1b serializer and a schematic of the 2b to 1b serializer are shown in Figure B.6. Two 2b to 1b serializers serialize parallel 4b 2.75Gb/s data to 2b 5.5Gb/s data streams with the help of a 2.75GHz clock, and then the next 2b to 1b serializer serializes them to a 11Gb/s bit-stream using a 5.5GHz clock.

The receiver consists of a comparator pair, two 1b-to-4b deserializers, and a clock generation block. A pair of comparators, at the end of the transmission line, samples the

22Gb/s data and deserialize to two parallel 11Gb/s data streams. Finally, two 1b to 4b deserializers deserialize these two interleaved data streams to a 2.75Gb/s 8b parallel bit stream.

The first stage of the receiver is a pair of comparators operating in an interleaved fashion to sample the received signal (see Figure B.4). One comparator of the pair samples the data at the rising edge of the 11GHz clock and the other at the falling edge of the clock. Figure B.7 and Figure B.8 show a schematics of the comparators used in the high-speed and low-power link prototypes respectively. In both prototypes, a dynamic comparator is adopted for high speed operation [66]. In the low-power system, a two-stage structure achieves low metastability and low power consumption at moderate speed. Each stage of this two-stage comparator is comprised of a preamplifier followed by a latch. A PMOS pair is added in the second stage preamplifier to reduce kick-back from the output. A 61% reduction in kick-back noise is observed in simulation.

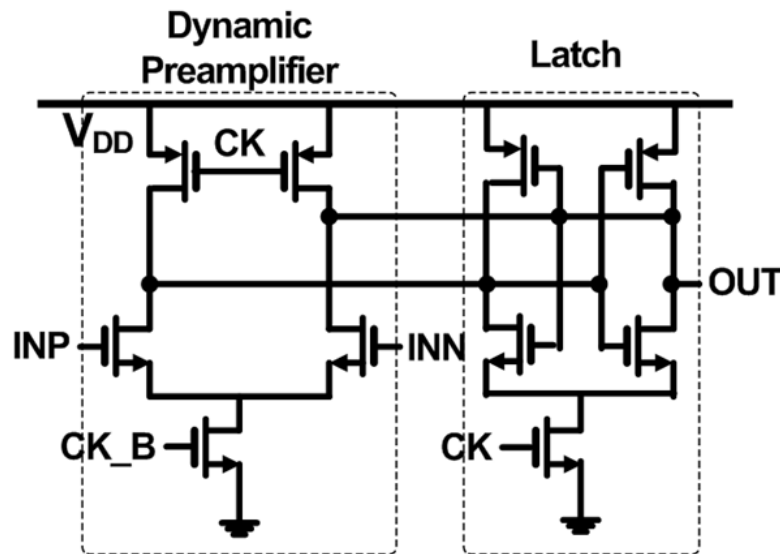


Figure B.7: Schematic of comparator of high-speed serial link.

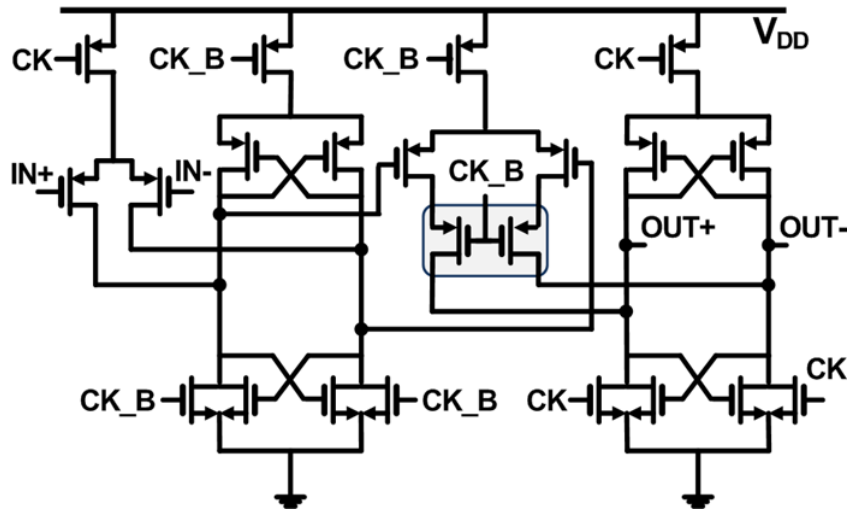


Figure B.8: Schematic of comparator of low-power serial link.

As shown in Figure B.4, since the two output data streams from the comparator pair differ in timing by half a clock period, one of the data streams is delayed by a half clock period to time align the two comparator outputs. Two 1b to 4b deserializers recover the original 8b parallel data. A block diagram of the 1b to 4b deserializer and a schematic of the 1b to 2b deserializer are shown in Figure B.9. In the 1b to 4b deserializer, a 1b to 2b deserializer deserializes  $11Gb/s$  data to two  $5.5Gb/s$  streams. Next two 1b to 2b deserializers deserialize the two  $5.5Gb/s$  data streams to a 4b  $2.75Gb/s$  parallel data stream.

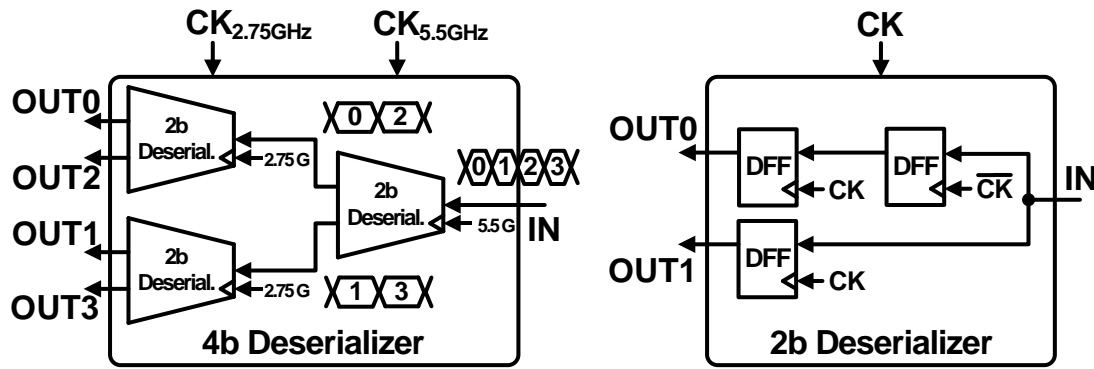


Figure B.9: Block diagrams of 1b-to-4b deserializer and 4b-to-1b deserializer.

The characteristics of the prototype, 10mm long, 2 $\mu$ m wide microstrip transmission line are summarized in Table B.3.<sup>5</sup> A 2 $\mu$ m line width is chosen to achieve both low driver power consumption and a large voltage amplitude at the receive-end. The estimated output voltage amplitude is 52% of the input voltage amplitude. The large receive amplitude means that comparator offset in the receiver is not a concern in this design.

Table B.3: Designed transmission line characteristics

Distributed Resistance	Distributed Inductance	Distributed Capacitance	Characteristic Impedance ( $Z_0$ )
9.9 k $\Omega$ /m	476 nH/m	61 pF/m	88 $\Omega$

Optimum resistive termination at receive-side of the lossy transmission line supports signal transmission over the high frequency TEM mode which enables signaling

<sup>5</sup> EM simulations for the on-chip transmission line are run with the help of Mohammad Ghahramani.

at the speed-of-light. This resistive termination eliminates dispersion due to the RC delay of low frequency components. The attenuated output voltage amplitude at the receive-end is [65]:

$$V_{OUT} = V_{IN} \exp\left(-\frac{R_L}{2Z_0}\right), \quad (\text{B.1})$$

where  $V_{IN}$  and  $V_{OUT}$  are the input and output voltage amplitudes, and  $R_L$  and  $Z_0$  are the total parasitic series resistance and characteristic impedance of the transmission line, respectively.

The optimum termination resistance at the receive-end of the transmission line,  $R_T$ , is chosen according to [65]:

$$\exp\left(-\frac{R_L}{2Z_0}\right) = \frac{R_T}{R_L + R_T}, \quad (\text{B.2})$$

Since, according to (B.1), a larger characteristic impedance leads to larger output voltage amplitude, a microstrip transmission line with the highest metal layer (M9) as a signal line and the lowest metal layer (M1) as a ground plane is chosen to achieve the maximum characteristic impedance for the given technology. The estimated parasitic series resistance of  $99\Omega$  for  $10\text{mm}$  line results in an optimum termination resistance of  $130\Omega$ , according to (B.2).

### B.3. Measurement Results

Both the  $20\text{Gb/s}$  and the  $10\text{Gb/s}$  transceivers, each with a  $10\text{mm}$  microstrip transmission line terminated with a poly resistor are fabricated in  $65\text{nm}$  digital CMOS

technology. Die micrographs are shown in Figure B.10. The total transceiver area, including clock network and clock drivers, but excluding the transmission line, is  $1580\mu\text{m}^2$  for the low-power prototype and  $2450\mu\text{m}^2$  for the high-speed prototype.

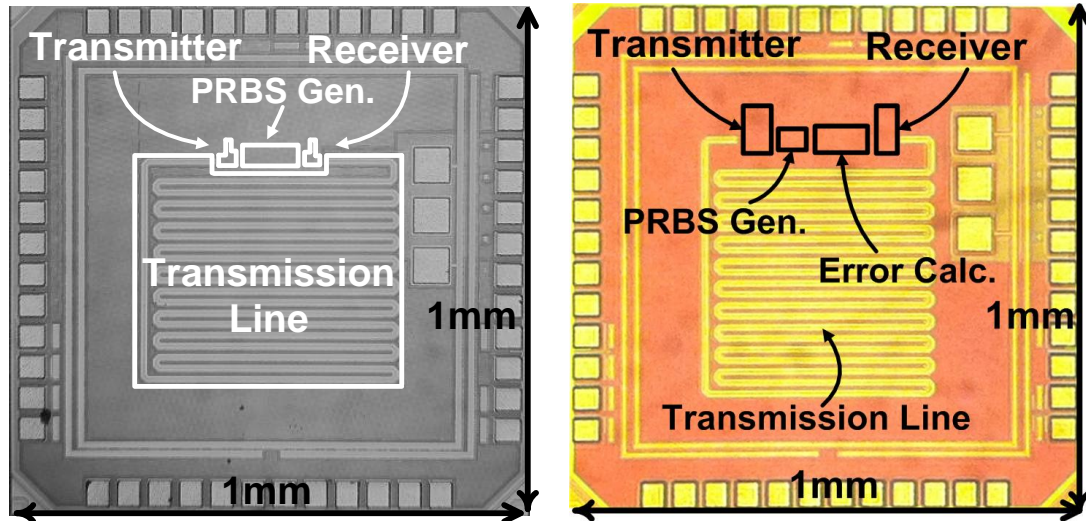


Figure B.10: Die micrographs of low-power type serial link (left) and high-speed type serial link (right).

Test data patterns are generated by an on-chip 16b PRBS generator. For the low-power prototype, the transmit and receive data streams are compared using a commercial BER tester. Because of limited bandwidth of this BER tester, BER measurements for the high speed prototype are made with an on-chip, custom, error calculation block. The energy consumption of the transmitter, receiver, and entire system (including clock drivers, but excluding the PRBS generator and error calculation block) are measured while maintaining a BER of less than  $10^{-13}$  and  $10^{-11}$  for the low-power and high-speed prototypes, respectively. As shown in Figure B.11, the high-speed type serial link

achieves a maximum rate of  $22\text{Gb/s}$  data rate, while the entire system consumes  $1.36\text{pJ/b}$  at  $20\text{Gb/s}$ . The low-power type consumes  $680\text{fJ/b}$  at  $10\text{Gb/s}$ . Although the latency cannot be measured directly from our test setup, EM simulations show the latency to be  $54\text{ps}$  for a  $10\text{mm}$  link, which corresponds to the speed of light latency in the  $\text{SiO}_2$  medium of this technology.

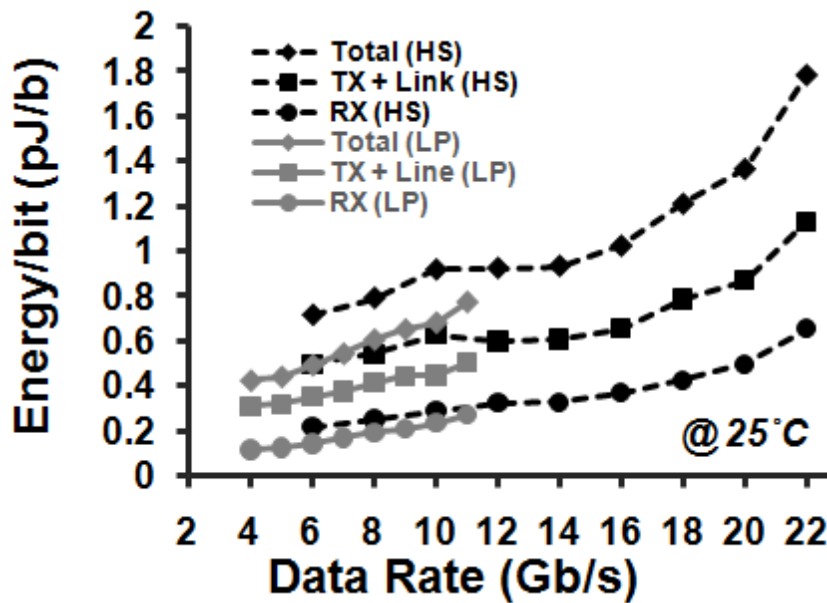


Figure B.11: Measured energy-per-bit and data rates at  $25^\circ\text{C}$ . HS: high-speed type serial link, LP: low-power type serial link.

Eye-diagrams at the receive-end of the transmission line, measured using dedicated probing pads and a  $50\Omega$  GSG probe, are shown in Figure B.12. Direct eye measurements were done for data rates up to  $18\text{Gb/s}$ , which is the limit of the  $15\text{GHz}$  GSG probes used. For the high-speed type serial link, the horizontal eye width is  $54\% UI$  and the vertical eye opening is  $152\text{mV}$  at  $18\text{Gb/s}$ . For the low-power type serial link, the



horizontal eye width is 91%  $UI$  and the vertical eye opening is 304mV at 10Gb/s. The large eye opening proves the noise immunity of the proposed scheme, and also demonstrates the effective elimination of dispersion and the suppression of ISI.

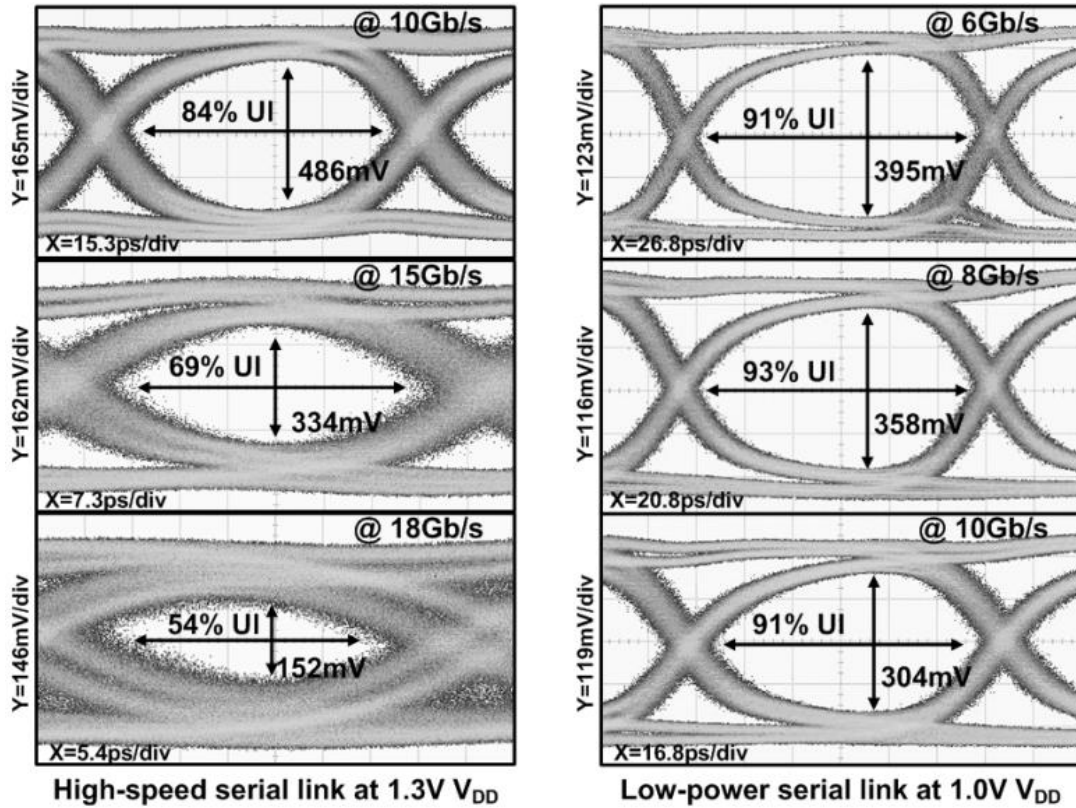


Figure B.12: Measured eye-diagram of the receive-end of the 10mm serial link with a GSG probe at 25°C.

The serial link achieves better energy efficiency than conventional parallel busses with the same bandwidth density and data transfer time. Several bus schemes are designed for performance comparison and they are listed in Table B.4. Figure B.13 compares the measured performance of the prototype to the simulated performance of conventional parallel busses in terms of energy efficiency over bandwidth density. For a

crosstalk coefficient of 15%, the spacing between the  $2\mu\text{m}$  wide M9 microstrip transmission lines is  $10.8\mu\text{m}$ . We compare the  $20\text{Gb/s}$  serial link with several 8-bit parallel bus schemes each with this same overall width and spacing, and each optimized in terms of energy-per-bit and bandwidth density. We also compared energy efficiency over 16b transfer time and the result is shown in Figure B.14. The transfer time of 16-bit data over link is considered for fairer comparison instead of directly using link latency. The 16-bit data transfer time is defined as link latency added to the clock cycles needed to transfer 16-bit data. The serial link shows a 75% improvement of (energy-per-bit)/(bandwidth density) and 3.7 times improvement of (energy-per-bit)/(16-bit data transfer time) compared to the most optimized parallel bus.

Table B.4: Designed transmission line characteristics

<b>8-bit Parallel Bus</b>	<b>Line Width</b>	<b>Line Space</b>	<b>Repeater Size (PMOS/NMOS)</b>	<b>Number of Repeater Insertion</b>
Bus Scheme 1	$0.4\mu\text{m}$	$0.4\mu\text{m}$	$19.8\mu\text{m} / 9.6\mu\text{m}$	13
Bus Scheme 2	$0.4\mu\text{m}$	$0.4\mu\text{m}$	$9.6\mu\text{m} / 4.8\mu\text{m}$	9
Bus Scheme 3	$0.8\mu\text{m}$	$0.8\mu\text{m}$	$9.6\mu\text{m} / 4.8\mu\text{m}$	9
Bus Scheme 4	$0.8\mu\text{m}$	$0.8\mu\text{m}$	$4.8\mu\text{m} / 2.4\mu\text{m}$	5

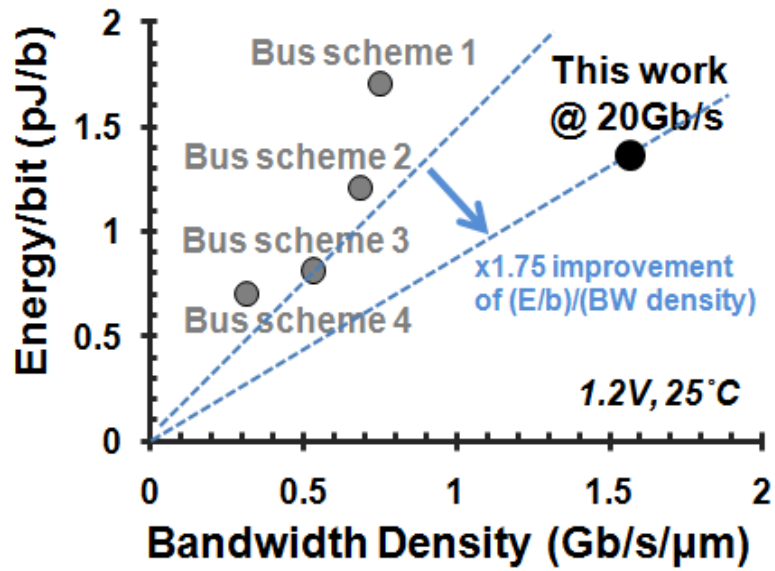


Figure B.13: Comparison of energy efficiency over bandwidth density with conventional bus schemes that utilize the same metal level (M9) at  $1.2V_{DD}$  and  $25^{\circ}C$ . A crosstalk coefficient of 15% is assumed for the transmission line.

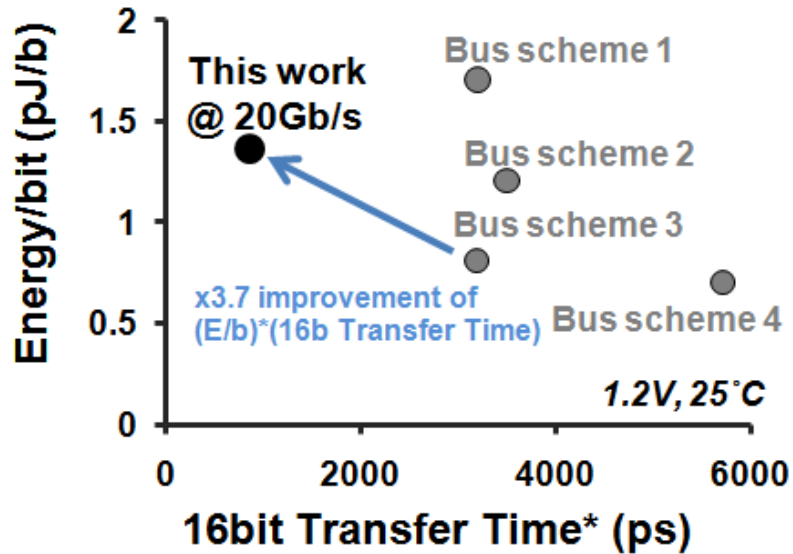


Figure B.14: Comparison of energy efficiency over 16-bit transfer time with conventional bus schemes that utilize the same metal level (M9) at  $1.2V_{DD}$  and  $25^{\circ}C$ .

\*16-bit transfer time = (link latency) + (two clock cycles)

#### **B.4. Conclusion**

An on-chip serial transceiver with an optimally terminated transmission line for global signaling is implemented in  $65nm$  CMOS technology. Table B.5 summarizes the measured performance of the prototype and compares it to recently published on-chip global link systems. The prototype achieves the fastest data rate and the lowest link latency.

The combination of voltage-mode line driver, optimum resistive termination, and SerDes techniques enables very low latency, high data rate and low ISI. The high-speed prototype device achieves a data rate of  $22Gb/s$  with a BER lower than  $10^{-11}$ . The  $10Gb/s$  prototype device consumes  $680fJ/b$  at a data rate of  $10Gb/s$  with a BER lower than  $10^{-13}$ . These links demonstrate the highest combinations of speed, energy efficiency and link distance of any on-chip serial link. Furthermore energy efficiency and bandwidth density are better than that of an optimized parallel bus in the same technology.

Table B.5: Performance comparison with recent works.  
 HS: high-speed type serial link, LP: low-power type serial link.

	<b>This Work: HS</b>	<b>This Work: LP</b>	<b>[3]</b>	<b>[4]</b>	<b>[5]</b>	<b>[6]</b>
Data Rate	20Gb/s	10Gb/s	4Gb/s	4.9Gb/s	3Gb/s	8Gb/s
BER	$< 10^{-11}$	$< 10^{-13}$	$< 10^{-6}$	$< 10^{-10}$	$< 10^{-14}$	$< 10^{-14}$
Eye Width (% UI)	54 at 18Gb/s	91	50	N/A	N/A	N/A
Energy/bit (pJ/b)	1.36	0.68	0.36	0.34	2.0	$> 3.4$
Energy/bit/link length (pJ/b/10mm)	1.36	0.68	0.36	0.68	1.43	$> 11.2$
Transceiver Area	2450 $\mu\text{m}^2$	1580 $\mu\text{m}^2$	1760 $\mu\text{m}^2$	N/A	N/A	N/A
Link Latency (ps/mm)	5.4 (from sim)	5.4 (from sim)	N/A	N/A	12.1	6.4
Link Length	10mm	10mm	10mm	5mm	14mm	3mm

## Bibliography

- [1] <http://www2.med.umich.edu/departments/md/index.cfm>
- [2] <http://www.epilepsyfoundation.org/aboutepilepsy/>
- [3] Benito-Leon J, Louis ED., "Clinical update: Diagnosis and treatment of essential tremor," *The Lancet*, Vol. 369, No. 9568, pp. 1152-1153, April 2007.
- [4] Tan EK, Fook-Chong S, Lum SY, et al., "Non-motor manifestations in essential tremor: use of a validated instrument to evaluate a wide spectrum of symptoms," *Parkinsonism & Related Disorders*, Vol. 11(6), pp. 375-380, September 2005.
- [5] Dogu O, Sevim S, Camdeviren H, Sasmaz T, Bugdayci R, Aral M, Kalegasi H, Un S, Louis ED, "Prevalence of essential tremor: Door-to-door neurological exams in Mersin Province," *Neurology*, Vol. 61(12), pp. 1804-1807, December 2003.
- [6] <http://findmeacure.com/2011/07/08/essential-tremor/>
- [7] [http://www.ninds.nih.gov/disorders/dystonias/detail\\_dystonias.htm](http://www.ninds.nih.gov/disorders/dystonias/detail_dystonias.htm)
- [8] Burda A, Webster K, Leikin JB, Chan SB, Stokes KA, "Nefazadone-induced acute dystonic reaction," *Vet Hum Toxicol*, Vol. 41(5), pp. 321–322, October 1999.
- [9] Bittar RG, Yianni J, Wang S, Liu X, Nandi D, Joint C, Scott R, Bain PG, Gregory R, Stein J, Aziz TZ, "Deep brain stimulation for generalised dystonia and spasmodic torticollis," *J. Clinical Neuroscience*, Vol. 12(1), pp. 12–16, January 2005.
- [10] de Lau LM, Breteler MM, "Epidemiology of Parkinson's disease," *Lancet Neurology*, Vol. 5(6), pp. 525–535, June 2006.
- [11] <http://www.parkinson.org/parkinson-s-disease.aspx>
- [12] Dickson DV, "Neuropathology of movement disorders," In Tolosa E, Jankovic JJ. *Parkinson's disease and movement disorders*. Hagerstown, MD: Lippincott Williams & Wilkins, pp. 271–283, 2007.
- [13] [http://www.umm.edu/patiented/articles/what\\_parkinsons\\_disease\\_what\\_causes\\_it\\_000015\\_1.htm](http://www.umm.edu/patiented/articles/what_parkinsons_disease_what_causes_it_000015_1.htm)

- [14] The National Collaborating Centre for Chronic Conditions, ed, "Surgery for Parkinson's disease," *Parkinson's Disease*. London: Royal College of Physicians. pp. 101–11, 2006.
- [15] Commission on Epidemiology and Prognosis, International League Against Epilepsy (1993). "Guidelines for epidemiologic studies on epilepsy," *Epilepsia*, Vol. 34(4), pp. 592–596, July 1993.
- [16] <http://report.nih.gov/NIHfactsheets/ViewFactSheet.aspx?csid=88>
- [17] World Health Organization, "Epilepsy: aetiogy, epidemiology and prognosis, World Health Organisation," <http://www.who.int/mediacentre/factsheets/fs165/en/>, February 2001.
- [18] [http://www.ninds.nih.gov/disorders/deep\\_brain\\_stimulation/deep\\_brain\\_stimulation.htm](http://www.ninds.nih.gov/disorders/deep_brain_stimulation/deep_brain_stimulation.htm)
- [19] M. L. Kringelbach, N. Jenkinson, S.L. Owen, and T.Z. Aziz, "Translational principles of deep brain stimulation," *Nature Reviews Neuroscience*, vol. 8(8), pp. 623-635, August 2007.
- [20] Gildenberg PL, "Evolution of neuromodulation," *Stereotactactic and Functional Neurosurgery*, Vol. 83(2–3), pp. 71–79, July 2005.
- [21] [http://wwwp.medtronic.com/Newsroom/NewsReleaseDetails.do?itemId=1284644553533&lang=en\\_US](http://wwwp.medtronic.com/Newsroom/NewsReleaseDetails.do?itemId=1284644553533&lang=en_US)
- [22] <http://www.neurotechreports.com/pages/publishersletterApr05.html>
- [23] <http://medcitynews.com/2010/03/fda-questions-medtronics-deep-brain-stimulation-device/>
- [24] <http://www.medtronicdbs.com/essential-tremor/about/how-it-works/index.htm>
- [25] <http://www.medtronic.com/health-consumers/essential-tremor/therapy/dbs-therapy/activa-rc/>
- [26] Boviatsis EJ, Stavrinou LC, Themistocleous M, Kouyialis AT, Sakas DE, "Surgical and hardware complications of deep brain stimulation. A seven-year experience and review of the literature," *Acta Neurochirurgica*, Vol. 152(12), pp. 2053-2062, December 2010.
- [27] Shahid M. Nimjee, "Complications of deep brain stimulation: Risks of placement vs. neurostimulator device issues," *Annual meeting of the North American Neuromodulation Society*, 2011.
- [28] Wesley Thevathasan, Ralph Gragory, "Deep brain stimulation for movement disorders," *Practical Neurology*, Vol. 10, pp. 16-26, February 2010.

- [29] <http://www.epda.eu.com/en/parkinsons/medinfo/neurosurgery/deep-brain-stimulation-dbs/>
- [30] Khalil Najafi and Kendal D. Wise, "An implantable multielectrode array with on-chip signal processing," *IEEE Journal of Solid-State Circuits*, Vol. SC-21, pp. 1035–1044, December 1986.
- [31] A. C. Metting van Rijn, A. Peper, and C. A. Grimbergen, "High-quality recording of bioelectric events," *Medical and Biological Engineering and Computing*, Vol. 28, pp. 389-397, 1990.
- [32] T. Chen, K. Chen, Z. Yang, K. Cockerham, and W. Liu, "A biomedical multiprocessor SoC for closed-loop neuroprosthetic applications," *IEEE International Solid State Circuits Conference (ISSCC'09) Digest of Technical Papers*, pp. 434-435, February 2009.
- [33] Meysam Azin, David Guggenmos, Scott Barbay, Randolph Nudo, Pedram Mohseni, "A battery-powered activity-dependent intracortical microstimulation IC for brain-machine-brain interface," *IEEE Journal of Solid-State Circuits*, Vol. 46, pp. 731–745, April 2011.
- [34] F. Yoshida, I. Martinez-Torres, A. Pogosyan, E. Holl, E. Petersen, C. Chen, T. Foltynie, P. Limousin, L. Zrinzo, M. Hariz, P. Brown, "Value of subthalamic nucleus local field potentials recordings in predicting stimulation parameters for deep brain stimulation in Parkinson's disease," *Journal of Neurology, Neurosurgery and Psychiatry*, Vol. 81(8), pp. 885-889, August 2010.
- [35] Al-Thaddeus Avestruz, Wesley Santa, Dave Carlson, Randy Jensen, Scott Stanslaski, Alan Helfenstine, Tim Denison, "A 5  $\mu$ W/channel spectral analysis IC for chronic bidirectional brain-machine interfaces," *IEEE Journal of Solid-State Circuits*, Vol. 43, pp. 3006–3024, December 2008.
- [36] T.C. Marzullo, J.R. Dudley, C.R. Miller, L. Trejo, D.R. Kipke, "Spikes, Local Field Potentials, and Electrocorticogram Characterization during Motor Learning in Rats for Brain Machine Interface Tasks", *IEEE 27th Annual International Conference of the Engineering in Medicine and Biology Society*, September 6, 2005.
- [37] Jongwoo Lee, Hyo-Gyuem Rhew, Daryl R. Kipke, Michael P. Flynn, "A 64-channel programmable closed-loop neurostimulator with 8-channel neural amplifier and logarithmic ADC," *IEEE Journal of Solid-State Circuits*, Vol. 45, pp. 1935–1945, September 2010.
- [38] K. S. Guillory and R. A. Normann, "A 100-channel system for real time detection and storage of extracellular spike waveforms," *Journal of Neuroscience Methods*, Vol. 91, 1999.



- [39] F. Serra-Graells and J. Huertas, "Low-voltage CMOS subthreshold logarithmic amplification and AGC", *IEEE Proceeding of Circuits, Devices and Systems*, Vol. 152, pp. 61-70, February 2005.
- [40] J. Lee, J. Kang, S. Park, J. Seo, J. Anders, J. Guilhereme and M. P. Flynn, "A 2.5mW 80dB DR 36dB SNDR 22MS/s Logarithmic Pipeline ADC," *IEEE Journal of Solid State Circuits*, Vol. 44, pp. 2755-2765, October 2009.
- [41] R. C. Taft and M. R. Tursi, "A 100-MS/s 8-b CMOS subranging ADC with sustained parametric performance from 3.8 V down to 2.2V", *IEEE Journal of Solid-State Circuits*, Vol. 36, pp. 331-338, March 2001.
- [42] V. Paliouras and T. Stouraitis, "Low-power properties of the logarithmic number system," *PATMOS 2000: International Workshop on Power and Timing Modeling, Optimization and Simulation, Gottingen, Germany*, pp. 285–294, 13-15 September 2000.
- [43] E. E. Swartzlander and A. G. Alexopoulos, "The sign/logarithm number system," *IEEE Transactions on Computers*, Vol. C-24, pp. 1238–1242, December 1975.
- [44] L. K. Yu and D. M. Lewis, "A 30-b integrated logarithmic number system processor," *IEEE Journal of Solid-State Circuits*, Vol. 26, pp. 1433-1440, October 1991.
- [45] O. Vainio and Y. Neuvo, "Logarithmic arithmetic in FIR filters," *IEEE Electronics Letters*, Vol. 41, pp. 580-581, May 2005.
- [46] N. G. Kingsbury and P. J. W. Rayner, "Digital filtering using logarithmic arithmetic," *Electronics Letters*, Vol. 7, pp. 56-58, January 1971.
- [47] J. H. Lang, C. A. Zukowski, R. O. LaMaire, and C.H. An, "Integrated Circuit Logarithmic Arithmetic Units," *Massachusetts Institute of Technical Report*, EE and CS Department, 1983.
- [48] Byeong-Gyu Nam and Hoi-Jun Yoo, "An embedded stream processor core based on logarithmic arithmetic for a low-power 3-D graphic SoC," *IEEE Journal of Solid-State Circuits*, Vol. 44, pp. 1544–1570, May 2009.
- [49] T. Akin, K. Najafi, and R. M. Bradley, "A wireless implantable multichannel digital neural recording system for a micromachined sieve electrode," *IEEE Journal of Solid-State Circuits*, Vol. 33, pp. 109–118, January 1998.
- [50] W. Liu, K. Vichienchom, M. Clements, S. C. DeMarco, C. Hughes, E. McGucken, M. S. Humayun, E. de Juan, J. D. Weiland, and R. Greenberg, "A neuro-stimulus chip with telemetry unit for retinal prosthetic device," *IEEE Journal of Solid-State Circuits*, Vol. 35, pp. 1487–1497, October 2000.

- [51] Kim Fung Edward Lee, "A timing controlled AC-DC converter for biomedical implants," in *IEEE International Solid-State Circuits Conference*, pp. 128–129, February 2010.
- [52] A. S. Y. Poon, S. O'Driscoll, and T. H. Meng, "Optimal frequency for wireless power transmission into dispersive tissue," *IEEE Transactions on Antennas and Propagation*, Vol. 58, pp. 1739-1750, May 2010.
- [53] G. Papotto, F. Carrara, G. Palmisano, "A 90-nm CMOS Threshold-Compensated RF Energy Harvester," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 1985-1997, September 2011.
- [54] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New Delhi: McGraw-Hill, 2001.
- [55] V.S. Polikova, P.A. Trescob and W.M. Reicherta, "Response of brain tissue to chronically implanted neural electrodes," *Journal of Neuroscience Methods*, Vol. 148, pp. 1-18, October 2005.
- [56] J. Volkmann, J. Herzog, F. Kopper, G. Deuschl, "Introduction to the programming of deep brain stimulators," *Movement Disorders*, Vol. 17, pp. S181-S187, 2002.
- [57] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7- $\mu$ W minimum RF input power," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 1602-1608, October 2003.
- [58] E. Mensink, D. Schinkel, E. Klumperink, E. van Tuijl, and B. Nauta, "A 0.28pJ/b 2Gb/s/ch Transceiver in 90nm CMOS for 10mm On-chip interconnects," *ISSCC Dig. Tech. Papers*, pp. 414-415, Feb. 2007.
- [59] R. Ho, I. Ono, F. Liu, R. Hopkins, A. Chow, J. Schauer, and R. Drost, "High-speed and low-energy capacitively-driven on-chip wires," *ISSCC Dig. Tech. Papers*, pp. 412–413, Feb. 2007.
- [60] B. Kim and V. Stojanović, "A 4Gb/s/ch 356fJ/b 10mm equalized on-chip interconnect with nonlinear charge-injecting transmit filter and transimpedance receiver in 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 66-67, Feb. 2009.
- [61] J. Seo, R. Ho, J. Lexau, M. Dayringer, D. Sylvester and D. Blaauw, "High-Bandwidth and Low-Energy On-Chip Signaling with Adaptive Pre-Emphasis in 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 182-183, Feb, 2010.
- [62] A. P. Jose and K. L. Shepard, "Distributed loss-compensation techniques for energy-efficient low-latency on-chip communication," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 1415-1424, Jun. 2007.

- [63] A. P. Jose and G. Patounakis, and K. Shepard, "Pulsed Current-Mode Signaling for Nearly Speed-of-Light Intrachip Communication," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 772-780, Apr. 2006.
- [64] J. Park, J. Kang, S. Park, and M. P. Flynn, "A 9Gbit/s serial transceiver for on-chip global signaling over lossy transmission lines," *IEEE Trans. Circuits Syst. I*, vol. 56, pp. 1807-1817, Aug. 2009.
- [65] M. P. Flynn and J. J. Kang, "Global signaling over lossy transmission lines," *Proc. IEEE/ACM ICCAD.*, 2005, pp. 985-992.
- [66] C. C. Lee and M. P. Flynn, "A 12b 50MS/s 3.5mW SAR assisted 2-stage pipeline ADC," *IEEE Symp. VLSI Circuits, Dig. Tech. Papers*, pp. 239-240, Jun. 2010.