Energy-efficient Reactive Radio Design in Body Area Networks

by

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To my family

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Abstract

A wireless body area network (WBAN) consists of several mobile devices worn on the human body. WBANs have enormous potential in health monitoring systems as it eliminates the inconvenience of having wires around the patient's body, offering more freedom of movement and comfort, enhanced monitoring, and the administration of at-home treatment. Low power consumption is crucial for such applications due to the limited capacity of portable batteries. The power consumption of wireless communication is especially important since the radio typically consumes the majority of the energy in such systems.

There are two ways to solve this energy constraint, which are reducing the power consumption or harvesting the energy from external sources. In this thesis, we approach this in both ways. First, we reduce the RF communication power by optimizing the radio for the wireless communication channel in a WBAN. The RF communication channel is measured using custom hardware with UWB and narrowband signals, and it is observed that the channel has periods of time when it is good enough for a low sensitivity, low power receiver to be used for communication. Second, we scavenge the energy from propagating radio waves with a subthreshold CMOS rectifier. Theoretical analysis of a subthreshold CMOS rectifier is presented, and used to maximize the sensitivity of a prototype rectifier.

Chapter I.
Introduction to the Study

I.1 Wireless Body Area Network (WBAN)

A wireless body area network (WBAN) is wireless communication between multiple Body Sensor Units (BSUs) and a single Body Central Unit (BCU) around the human body [1]. Fig. I.1 shows an example of a WBAN that consists of one BCU (cell phone) and four BSUs (pacemaker, pulse oximeter, pedometer and intraocular pressure sensor). These wireless sensor networks have enormous potential in health monitoring systems as it eliminates the inconvenience of having wires around the patient's body, offering more freedom of movement and comfort, enhanced

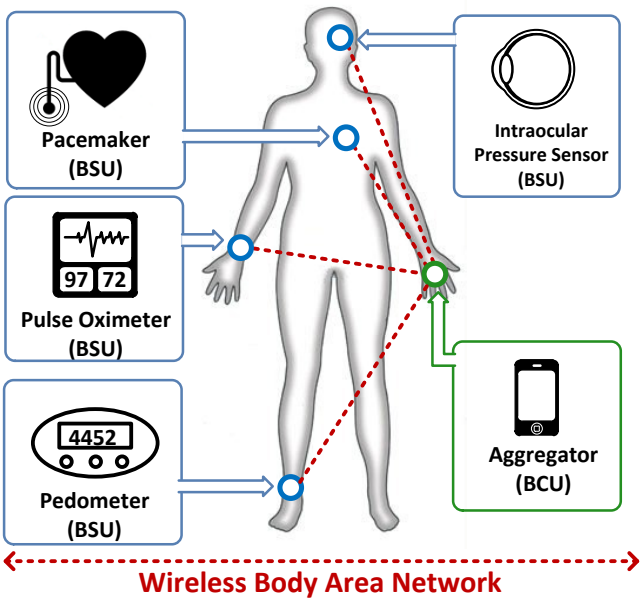

Fig. I.1. Example of wireless body area networks (WBAN)

monitoring, and the administration of at-home treatment [1]-[5]. Several BSUs on the human body work as health monitoring sensors, collecting biological information of the patient continuously. These collected data, saved in a local BSU memory, are sent to an aggregator (BCU) intermittently through an RF communication channel. The BCU processes these data and communicates with a doctor in a hospital or other experts via a cell phone or Wi-Fi network. In this way, the patient's health can be monitored anywhere in real time—without the need of wired devices—by experts in a remote location far away from the patient.

As low power radio frequency integrated circuits and biomedical sensors develop, WBAN becomes feasible and practical. An IEEE task group for WBAN (IEEE 802.15) was formed in 2007 has developed a communication standard for WBAN [6]-[7]. The quality of biological information and limited energy capacity of BSUs are the current bottlenecks of WBAN [3]. Especially, high power consumption and small battery size severely limit the operating time of BSUs.

I.2 Energy Constraint in WBAN

Fig. I.1 shows an example of a WBAN linking several health monitoring systems around a human body to the person's cellphone. The sensors are severely energy constrained, while the cellphone has a larger, rechargeable energy source. Low power consumption is crucial for such applications due to the limited capacity of portable batteries. The power consumption of wireless communication is especially important since it typically consumes the majority of the energy in such systems [8].

There are generally two ways to solve this energy constraint, which are reducing the power consumption or harvesting the energy from external sources. In this thesis, we approach this in

both ways. First, we reduce the RF communication power by optimizing for the dynamics of the wireless communication channel in WBANs. Second, we scavenge the energy from propagating radio waves. Since the first method is reducing the power consumption and the second method adapts power harvesting, these two methods can be applied concurrently. In section I.3, background research and the goals of power harvesting are provided, and detailed background and motivation for low power communication using channel modeling are provided in section I.4.

I.3 Power Harvesting Circuit

RF power harvesting using a CMOS rectifier is one of the most popular power harvesting methods for RFIDs and sensors, which converts an incoming RF signal into a DC voltage suitable for powering the node for brief periods of time. There are several ways to scavenge energy from an external source such as propagating radio waves, sunlight, mechanical vibration, or thermal gradients. The power densities, advantages and disadvantages of these sources are summarized in Table I. Power harvesting from RF waves has merits of small form factor and

Table I. Power harvesting methods

Source	RF wave [27]	Sunlight [9]	Mechanical vibration [10]	Thermal gradient [11]
Power density	36μW @ 8.5m distance with 4W EIRP	28μW/cm^2 @ Light soaked under 1W/m^2 (~1000 lux)	0.85mW @ 2600N force (knee during normal walking)	0.2-15mW @ 10-20º temperature gradients
Advantage	Small volume	Inexhaustible energy source	Energy from human movement	High power
Disadvantage	RF transmitter is necessary	Small power with indoor light	Time-varying energy source	Low efficiency (less than 10%)

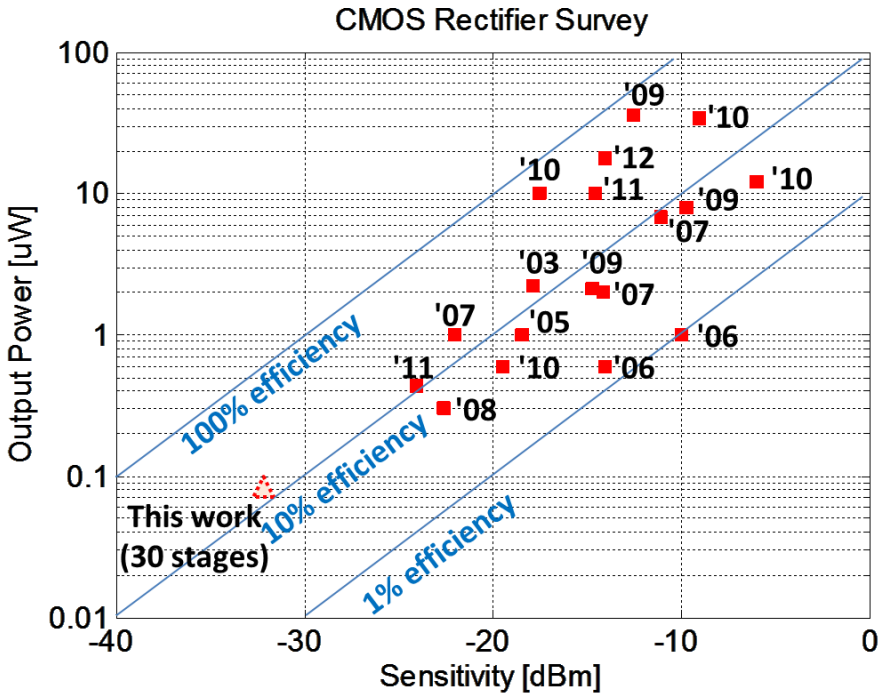

Fig. I.2. Sensitivity vs. output power

time-invariant power harvesting, although it requires a high power RF transmitter, such as a base-station in a star network.

Previous rectifiers focused on maximizing power conversion efficiency and output power rather than sensitivity [12]-[31]. The power conversion efficiency and output power are important when the system is continuously operating off harvested power. However, in some applications where the entire system does not need to be on all the time such as a human body physiological monitoring, the sensitivity is more important as it defines the maximum range. If output power consumption is minimized while charging and long charging time is acceptable, the sensitivity of the power harvester can be dramatically increased.

Fig. I.2 shows the harvested power versus sensitivity of previous work from 2003 to 2012 at 900MHz along with constant-efficiency lines [12]-[31]. As observed in this figure, the output

power is roughly proportional to the sensitivity, with most power harvesters operating around 10% efficiency. In this work, a power harvester is demonstrated with –32dBm sensitivity at 915MHz. This sensitivity is sufficient to power a device at a distance of 66m with a 4W EIRP source.

I.4 RF Communication Channel in WBAN

RF communication channel modeling in WBANs is necessary for power efficient RF communication. By producing a model that focuses on the periodic time domain behavior of the channel for a wireless body area network, we can analyze power/sensitivity tradeoffs at the circuit level as well as other system level design issues such as communication time and data rate. Therefore, robustly and accurately estimating WBAN channels is a crucial task in developing more efficient communication systems that optimally sense and exploit the unique channel dynamics [7]. The WBAN channel characteristics depend heavily on the surrounding environment, body posture, and movement, which all vary with time [32]. This is unlike the channel characteristics of long distance wireless networks (e.g. cellphone to WLAN or WWAN base station), which are relatively stable irrespective of the user's posture or movement. Furthermore, WBAN channels exhibit a periodicity due to the nature of body movements, yet this phenomenon hasn't been fully characterized or exploited to save energy in any WBANs. Many studies have been performed on WBAN channels [33]-[37]. Most of them use a vector network analyzer (VNA) or vector signal analyzer (VSA). These are accurate, but also bulky and expensive instruments, and require wired connections around the body and to a wall outlet for power. If we want to measure the channel characteristics where this equipment cannot be carried, a portable device is necessary. Furthermore, it is desirable to log channel data as a function of time in order to characterize the periodicity of the channel. Other groups have reported

implementing a portable WBAN channel estimator that relies on RSSI measurements at a fixed frequency [37][38].

I.4.1 Channel Model around the Human Body and its Usage

The channel for wireless body area networks involves the environment, and electromagnetic propagation, around the human body which is complicated due to the body's effect on antenna performance [39]. One reason the channel for a WBAN is unique compared to other channel models is the channel's dynamic characteristics due to the inherently limited motion of a person's body and the proximity of the sensors to the body itself. The distance and angle of antennas mounted to sensors worn on the body will constantly change in relation to one another as a person performs daily activities. For example, if a person has sensors on their belt and their wrist, then when their arm is in front of the body while walking, the channel will be line-of-sight (LOS) and the signal will be strong. In the back of their stride the channel will be non-line-of-sight (NLOS) and the signal will be weak, requiring more power to receive it. Intuitively, the channel should oscillate between strong and weak conditions as the person walks, runs, or performs other daily activities. Furthermore, these oscillations should be bounded by the physical limitations of the body's movement, or lack of movement (i.e. the human body is never perfectly still). Statistically analyzing such behavior using empirical data will allow us to effectively utilize the dynamics of the channel to reduce power consumption of the radio.

Radio power typically consumes the majority of the total power in a WBAN and is therefore a significant bottleneck in energy efficient design. This is because radio power is typically much higher than other components in a WBAN node, and the radio is not as easily duty cycled since it has to remain on when actively listening for packets. Often, as is the case with standards like

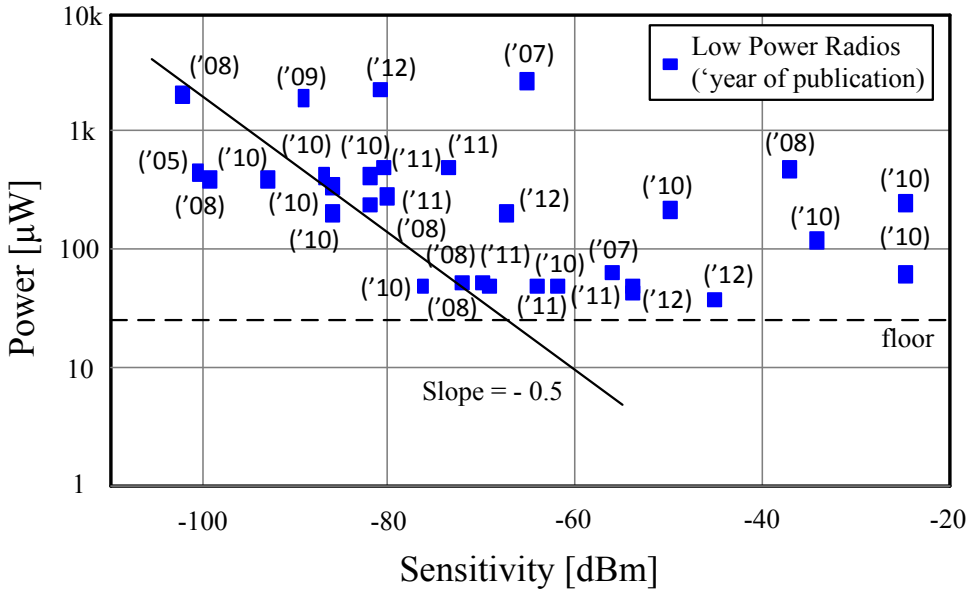

Fig. I.3. Low power radio survey

Bluetooth or Zigbee, radios are designed to have excellent sensitivity, defined as the minimum detectable power level of the receiver, so they can operate at a near worst-case path loss. This sensitivity level ensures reliable communication, but significantly increases the radio's power budget. Fig. I.3 shows a survey of published ultra-low power radios from 2006-2012 [40]-[63], comparing their power vs. sensitivity. Empirically, the survey shows a slope of -0.5 on a log graph between sensitivity and power consumption, with a floor around -40µW. The slope is influenced by several parameters, such as the variation in data rate, architecture, and non-linearity present in the radios. The survey only covers ultra-low power receivers, common in WBAN research, and Bluetooth or Zigbee receivers with higher power will sit well above this line. Using this survey one can estimate a squared relationship between power and sensitivity. For example, a 2X increase in power results in a 4X increase (improvement) in sensitivity.

Knowing the time domain response of a wireless WBAN channel allows us to make decisions based on design tradeoffs if we can tolerate periods of interrupted communication. By reducing

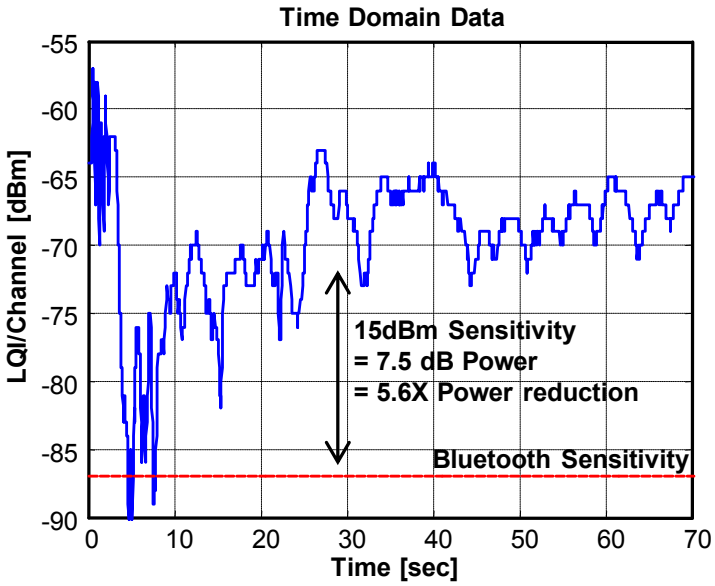

Fig. I.4. Channel path loss vs. Bluetooth sensitivity

the sensitivity of the receiver, square root power gains can be achieved at the cost of intermittent communication. Even so, the channel variability is slow enough that efficient packet transfer is possible.

To illustrate this tradeoff, Fig. I.4 shows the measured link quality indicator (LQI) vs. time of a person running with a receiver on the left hip and transmitter on the left wrist. Also shown is the sensitivity of a TI Bluetooth low energy radio [64] as an example. When LQI is above the sensitivity limit, reliable communication is achieved, and in this example, the majority of the time LQI far exceeds the sensitivity; therefore, the radio is overdesigned for the given channel. One could decrease the receiver sensitivity by 15dB in this case, which would give an estimated 5.6X power reduction by applying the empirical slope from Fig. I.3, but result in intermittent communication. Provided a WBAN sensor can tolerate some latency, we can make use of the fact that poor quality channels don't remain poor for long when a person is active.

I.5 Thesis Contributions

WBANs have enormous potential in health monitoring systems as it eliminates the inconvenience of having wires around the patient's body. Low power consumption is crucial for such applications due to the limited capacity of portable batteries. The power consumption of wireless communication is especially important since it typically consumes the majority of the energy in such systems. The goal of this research is to design a single chip solution for a low power reactive transceiver in WBAN. Three steps have been made to achieve this goal, and these are the key contribution of this thesis.

First, the RF communication channel in a WBAN is measured using custom hardware with UWB and narrowband signals in chapter II. It is observed that the RF communication channel periods of time when the channel is good enough that a low sensitivity, low power receiver can be used for communication.

Second, a -32dBm sensitivity CMOS RF power harvester is implemented and equations for the subthreshold rectifier are analyzed in chapter III. Sensitivity of the rectifier is maximized rather than efficiency, to maximize the communication distance. This rectifier is also used in a low power receiver, replacing the LNA.

Third, a 116nW multi-band CDMA based wake-up receiver with automatic interference rejection is implemented in chapter IV. This low power, low sensitivity receiver incorporates a full CDMA baseband processor operating in subthreshold to save power, as well as an automatic threshold compensation feedback loop to account for wireless interference.

Chapter II.
RF Channel Modeling in WBAN

II.1 Introduction

Developing accurate and sophisticated channel models for energy-constrained systems such as WBANs is a necessary step in understanding the key elements that factor into a channel model's behavior. By producing a model that focuses on the periodic time domain behavior of the channel for a wireless body area network, we can better analyze power/sensitivity tradeoffs at the circuit level and how they might impact communication goals at the system level. Similarly, accurate models can be used to develop WBAN-channel specific MAC protocols that more efficiently duty-cycle the radios.

In this chapter, RF communication channel modeling in a WBAN is provided. Section II.1.1 and II.1.2 provide a background of channel modeling in WBAN. Section II.2 proposes an UWB transmitter that can generate an impulse signal, which is essential when an impulse response of the channel is measured. Section II.3 discusses WBAN channel modeling using impulse response, and Section II.4 describes WBAN channel modeling using RSSI.

II.1.1 Channel Modeling Background

The 802.15.6 (WBAN) channel model document [65] is a collection of multiple experiments spanning different defined channels, including body-to-body or body-to-off body communication as well as line-of-sight (LOS) and non-line-of-sight (NLOS) variations. The purpose of these channel models is for evaluating potential physical layer proposals more than producing all-encompassing models. The ones included below describe WBAN CM3, which is body-to-body communication in the 900MHz and 2.4GHz bands for both LOS and NLOS communication. Three different experiments are described, resulting in the following two path loss modeling equations:

$$PL(d)[dB] = alog_{10}(d) + b + N \quad (1)$$

where a and b are coefficients of linear fitting, d is Tx-Rx distance in mm, and N is a normally distributed random variable with σ_n.

$$PL(d)[dB] = -10log_{10}(P_0 e^{-m0d} + P_1) + \sigma_p n_p \quad (2)$$

where P_0 is the average loss close to antenna, m_0 is the average decay rate in dB/cm for the surface wave traveling around the perimeter of the body, P_1 is the average attenuation of components in an indoor environment radiated away from the body and reflected back toward the receiving antenna, σ_p is the log-normal variance in dB, and n_p is a zero mean unit variance Gaussian random variable.

Equation (1) references Experiment A in the Channel Modeling document [66] which features a test subject in a hospital room in different stationary positions. S21 is measured between two antennas using a vector network analyzer in the 950-956MHz and 2.4-2.5GHz bands. A

transmitter antenna is placed at the waist, with a receiver antenna being placed on parts of the body, including head, ear, shoulder, wrist, waist, leg and ankle. Measurements in an anechoic chamber are also taken as a control experiment to remove the multipath effect. The path loss model is derived using a regression line through least square fitting for each frequency band.

Equation (2) references Experiment B [67] which is similar but includes signal fading in its experiments, covering the 915MHz and 2.45GHz frequency band. Antennas are placed horizontally around the torso as well as vertically along it and S21 is measured similar to Experiment A. The test subject is standing still during the experiments.

Experiment C [68] observes subject movement. Test subjects are observed standing, walking, and running in place in an office environment using BPSK modulated signals at 820MHz and 2360MHz. The channel response is captured on a vector signal analyzer in 40μs sets, with a 2.5ms gap before the next capture (sample rate of 0.4kS/s), totaling 10 seconds. Results show the most significant fading effects are due to movement and the change in distance and alignment of the antennas. Variation also increases with increased movement from the test subject. Finally, channel stability over time is observed and assigned a value, the channel variation factor, which is the ratio between the standard deviation and the RMS power of the sequence.

Papers published outside of 802.15.6 cover a spectrum of different approaches ranging from parallel finite-difference time-domain method (FDTD) simulations [69] to measurements from commercial MICAz motes using a Zigbee Radio [70]. Papers have also attempted to characterize the temporal characteristics of the channel [71].

II.1.2 Results from Channel Modeling Background Study

Many different distributions such as lognormal, normal, or Weibull, [72] fit different experimental scenarios within a WBAN. The most commonly used distribution for a static channel is lognormal, supported by both the S21 and RSSI data collection. Different experiments show different adjustment factors to the basic lognormal equation. The lognormal result is explained in [72] by the large number of contributing effects to the attenuation of the transmitted signal which are multiplicative, or additive in the log domain. In addition, movement was shown to increase the variability of the channel, which is an important observation for WBANs. Several papers cite the significant impact of antenna angles as well as influences from the environment (multipath) and the size and shape of the user [69].

There are several factors that these experiments lack that are critical to applying our knowledge of the channel to the design of an energy efficient WBAN. Most experiments do not attempt to characterize the time domain characteristics of the channel and are therefore not conducted with a high enough sample rate or for a long enough period of time to accurately see the influence time has on the channel.

Perhaps most important is that the resulting path loss equations erase time domain periodicity from the test results. Fig. II.1 illustrates how this periodicity is erased when using only path loss statistics. A measured time domain channel response is shown (left) with its respective distribution (middle), which is then reconstructed using equation (1) from the WBAN task group channel model (right). It is obvious that equation (1) does not reproduce the structured periodic channel response in the original measured data, nor is that its intention. The purpose of equation (1) is to give a single path loss estimate for a channel. The time domain information is lost.

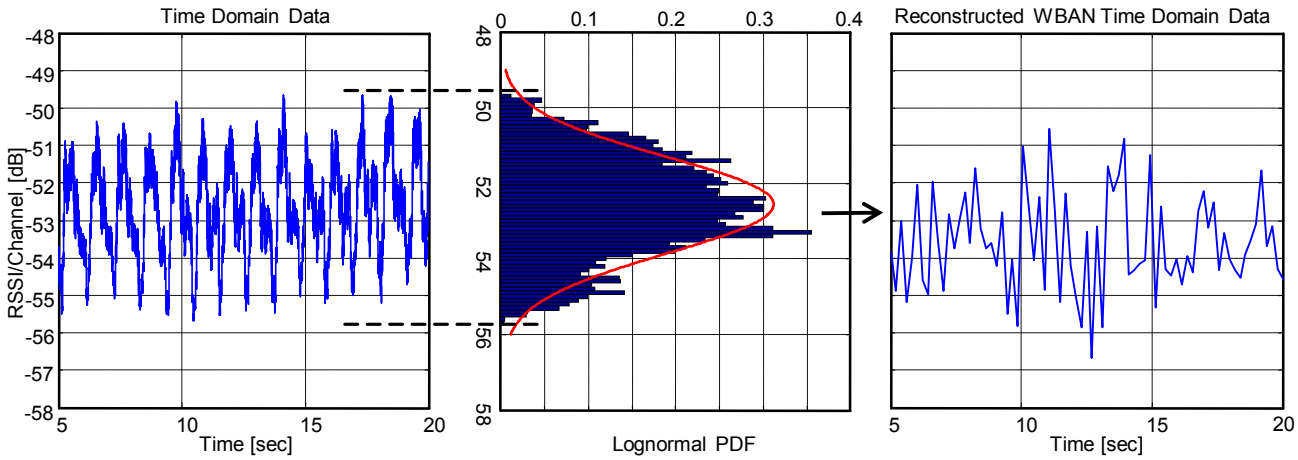

Fig. II.1. Time domain channel model with WBAN equation (1) reconstruction

Understanding this variability and being able to anticipate or accommodate for it is the key to our channel model and subsequent analysis. Our channel modeling will correct these shortcomings by using our custom hardware to measure impulse response or RSSI of the channel. Since the hardware is battery operated and portable, we can take data in different environments very applicable to peoples' normal lives or specific medical applications. Our statistical models will evaluate path loss of the channel in the time domain and will develop a policy to characterize the channel so it can be simplified and used to make design decisions that impact the performance and energy consumption of a WBAN node.

II.2 UWB Transmitter

When we want to measure the channel using an impulse response, a UWB transmitter can be the best option to generate impulses. Generally speaking, there are two ways to implement UWB transmitters. The first one is a design of UWB transmitter at a PCB level and second one is a design of a UWB transmitter with a custom IC.

In many cases, impulse radio-based UWB (IR-UWB) transmitters are fabricated as custom ICs in CMOS processes [74][75]. They have the advantage of system integration with processing and receiver electronics, etc., in a single-die. However, in some cases, full system integration is not required, and furthermore, some applications require only a UWB transmitter (e.g. channel sounding). In this case, it may be desirable to build a custom, high-performance impulse generator without the cost or complexity of fabricating a custom IC [76]. Moreover, if a pulse with high peak power is necessary, an IC may not be a good option. In particular for portable channel sounding in body area networks, we desire a UWB transmitter that is battery operated, is small enough to be worn on the body, and generates high power impulses to estimate the RF communication channel. In this application, the impulse generator only needs to excite the impulse response of a wireless channel so that it can be recorded by a higher-power receiver. Furthermore, the transmitter has low complexity and does not require compliance with a wireless standard. Therefore, a simple impulse generator is sufficient (no system integration with digital baseband processing is required). Designing a UWB transmitter on a printed circuit board (PCB) with discrete components is advantageous for these UWB applications.

On the other hand, the UWB transmitter with custom IC has benefits of low power consumption, BPSK modulation and system integration in a single die. In this research, we provide UWB transmitters with both design methods.

II.2.1 UWB Transmitter with SRD

There are several techniques to produce UWB pulses at the PCB design level [77]-[86]. These include avalanche transistors, tunnel diodes [77], nonlinear transmission lines (NLTLs) [78], photoconductive switches [79], bipolar transistors [80], FETs [81], and step recovery diodes

(SRDs) [82]-[86]. Avalanche transistors have high-power edge sharpeners, but the maximum pulse repetition frequency is limited, and the transistor lifetime is short [82]. Tunnel diodes have short transition times, but their output amplitude is relatively small [82]. NLTLs and photoconductive switches usually require monolithic microwave integrated circuits (MMICs). SRD based circuits are relatively easy to fabricate, cost effective and capable of generating pulses with less than 100ps of transition time. For this reason, SRD based circuits are suitable for low-cost, low-volume, and high performance UWB applications.

There are many researches which use SRDs to implement a UWB transmitter [82]-[86]. In most of these circuits, the power consumption is high (>300mW), and the supply voltage of the circuit is more than 7V, which is not compatible with a portable battery. This research presents a simple UWB transmitter with a supply voltage of 3V and also provides equations for estimating the pulse width and amplitude of the SRD pulse generator which are verified by experimental results.

II.2.1.1 Architecture

The architecture of the UWB transmitter is depicted in Fig. II.2. A microcontroller generates V_{DATA} which contains PPM information to be transmitted, and the UWB pulse generator produces the UWB pulses with SRDs according to the falling edges of V_{DATA}. A single 3V power supply is used for the entire circuit, and a 10MHz reference clock is used to produce the pulse repetition frequency

II.2.1.1.1 UWB Pulse Generator

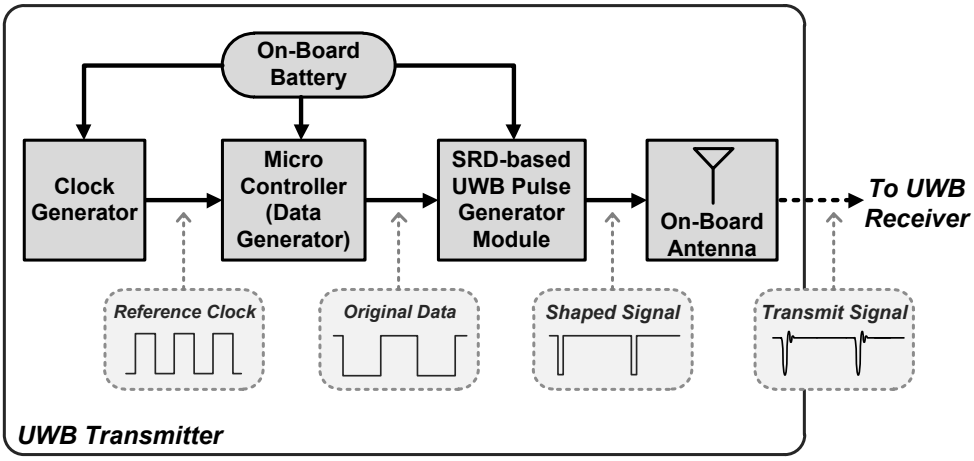

Fig. II.2. The architecture of the UWB transmitter

Fig. II.3 shows the schematic of the UWB pulse generator [86]. The core part of the pulse generator consists of two SRDs. To briefly explain its operation: SRD1 sharpens the falling edge of a negative pulse and SRD2 determines the width of the pulse and sharpens the rising edge of the pulse. Next we will examine the UWB pulse generator circuit in more detail.

The most important characteristic of an SRD is that it stores charge when forward biased. Once the SRD stores enough charge, it can use this stored charge at the beginning of reverse bias to temporarily maintain conduction and a forward bias voltage. Therefore, the SRD still functions like a short circuit with negative current during the initial time in reverse bias. However, when all stored charge is depleted, the SRD suddenly open circuits. At this time, the voltage across the SRD changes dramatically fast so that a sharp voltage edge can be generated. The pulse sharpening operation of the SRD is explained in [86].

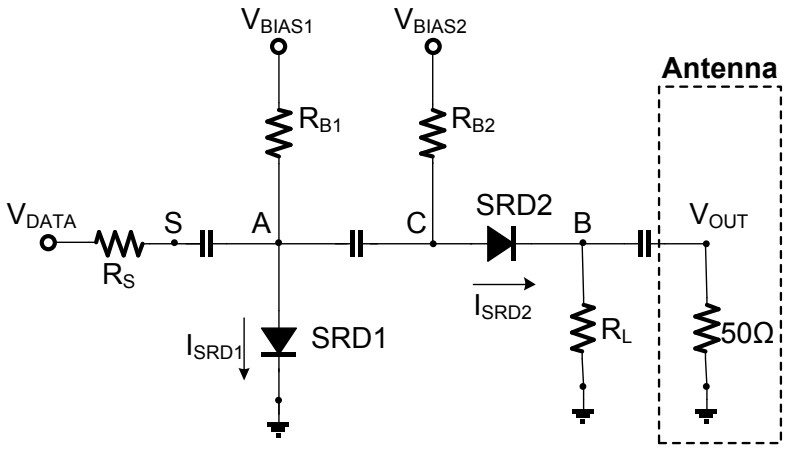

Fig. II.3. The schematic of the UWB pulse generator

The following equations summarize the output pulse.

$$T_{FALL} = \sqrt{T_T^{\,2} + ((R_S \,//\, R_L \,//\, 50)\cdot C_T)^2} \tag{3}$$

$$T_{RISE} = \sqrt{T_T^{\,2} + ((R_S + R_L \,//\, 50)\cdot C_T)^2} \tag{4}$$

$$pulse\ width = T_{FALL} + T_{RISE} + \ln(1+\frac{I_{F2}}{I_{R2}})\cdot\tau \tag{5}$$

$$amplitude = (\frac{V_{DD}}{R_S} - I_{F1})\cdot(R_S \,//\, R_{B1} \,//\, R_{B2} \,//\, R_L \,//\, 50) \tag{6}$$

Several design guidelines may be followed for selecting the values of the components. For faster rising and falling edges, and large pulse amplitude, small R_S and R_L are preferred. However, if R_L becomes too small, there is a ringing in the output pulse, and the output amplitude decreases. On the other hand, if R_L is larger than the 50Ω antenna impedance, it has a minimal effect on the pulse width and amplitude. Therefore, large R_L is desirable. Small I_{F1} and I_{F2} are better for lower power consumption, but I_{F1} and I_{F2} should be large enough to store sufficient charge in the SRDs during stages (II) and (III). R_{B1} and R_{B2} should be much larger than R_S and $R_L \parallel 50\Omega$ for high pulse amplitude.

II.2.1.1.2 Microcontroller

An ATtiny13A microcontroller is used to generate the data to be transmitted which is PPM modulated. A 10MHz oscillator is used for maximum data rate, which is the maximum frequency of the external clock for this microcontroller.

The pulse position modulation is used in this system. V_{DATA} is the output of the microcontroller and V_{OUT} is the output of the UWB pulse generator. One symbol period consists of four processor clock cycles. For the symbol '0', the value of V_{DATA} is '0111' and a UWB pulse of V_{OUT} exists at first clock edge. For the symbol '1', the value of V_{DATA} is '1101' and there is a UWB pulse at the third clock edge.

II.2.1.2 Experimental Results

Fig. II.4 is a photo of the UWB transmitter PCB with all the components. A single 3V supply is used for the entire circuit. A 2.7V regulator is used for the UWB pulse generator, the microcontroller and the buffer, and a 1.8V regulator for the 10MHz clock. For convenience, V_{BIAS1} and V_{BIAS2} were provided from an external power supply during the measurement. However, it could be replaced with voltage dividers using a potentiometer, since V_{BIAS1} and V_{BIAS2} are below 3V. The total size of the PCB is 4.3 cm x 2.9 cm.

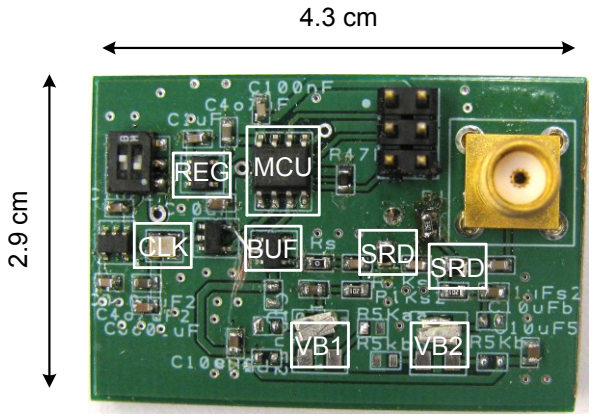

Fig. II.4. PCB of the UWB transmitter with SRD

Fig. II.5 shows the output UWB pulse measured with a Tektronix TDS6000C digital oscilloscope with R_S:20Ω. R_L:200Ω, I_{F1}:9.5mA, I_{F2}:2.5mA. The FWHM pulse width is 213ps and the pulse amplitude is 1.6V, which agrees with 227ps and 1.87V calculated from equations (5) and (6). When calculating equations (5) and (6), output resistance of the buffer should be considered as RS, which was 20Ω in our case. Fig. II.6 shows the power spectrum of the UWB

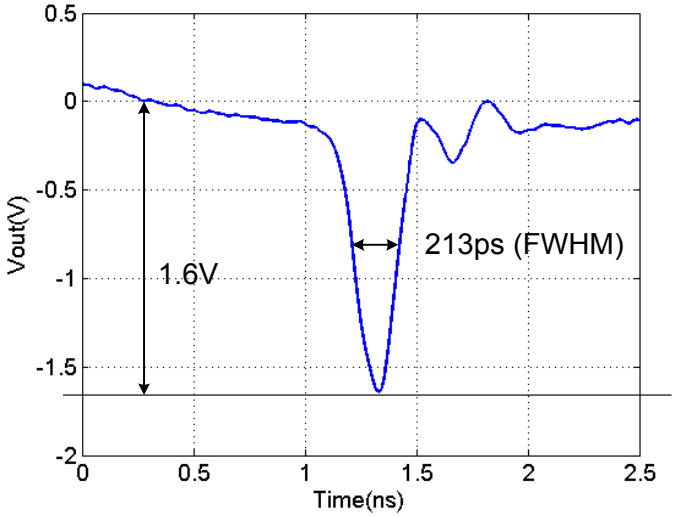

Fig. II.5. Measured UWB pulse at V_{OUT}

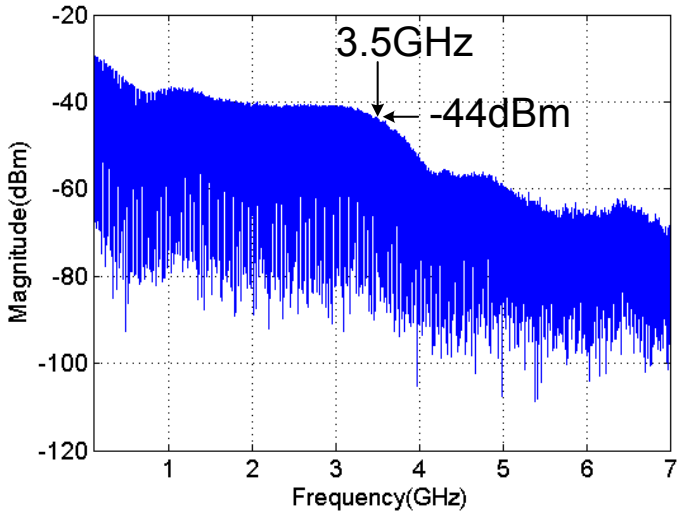

Fig. II.6. Measured UWB pulse power spectrum

pulse measured with an Agilent N9020A spectrum analyzer and resolution bandwidth is 3MHz. The 3dB bandwidth of the UWB pulse is 3.5GHz. The power consumption for the UWB pulse generator is 57mW and the total power of UWB transmitter is 70mW.

Table II shows the performance summary of the UWB pulse generator. The performances from other papers with different components are also provided. The power consumption of the IC based transmitter is the smallest, but the pulse amplitude is also relatively small. The pulse amplitudes of BJT and other SRD based transmitters are high. However, their supply voltage is greater than 7V, which precludes their use with single coin batteries. By comparison, this research demonstrates an SRD based transmitter that operates from a 3V supply, while generating pulse amplitude of 1.6V.

Table II. Performance summary of the UWB pulse generator

	Tech	Pulse Width	Pulse Amplitude	VDD	Power
Hu [74]	90nm CMOS	1ns	160mV	1.2V	225uW
Salameh [78]	NLTL	19ps	1.8V	-	>100mW
Gerding [80]	BJT	90-800ps	7V	-	-
Protiva [82]	SRD	110ps	7.5V	12V	>360mW*
Rueng. [83]	SRD	140ps, 100ps	2.5V, 1.1V	>7V	-
Han [84]	SRD	400-850ps	200-500mV	>7V	-
This work	SRD	213ps	1.6V	3V	70mW

*we calculate power consumption based on forward bias current

II.2.2 UWB transmitter with a custom IC

A UWB transmitter with a custom IC has benefits of low power consumption, BPSK modulation, and system in a single die than a UWB transmitter with SRD. For these reasons, the UWB transmitter with a custom IC is fabricated in IBM 130nm process.

II.2.2.1 Architecture

Fig. II.7 shows the schematic of the UWB transmitter with a custom IC. It consists of a custom IC fabricated in a 0.13μm CMOS process, an external power amplifier (ABA-54563 from Avago technology), and a 2.45GHz antenna (ANT-2.4-CW-RH from Antenna Factor). The IC generates BPSK-modulated, 350ps-wide pulses, and includes a gold code generator to modulate the pulses for CDMA. A 10MHz crystal oscillator is used as the clock source, and a single 9V battery is used to supply power to the entire transmitter.

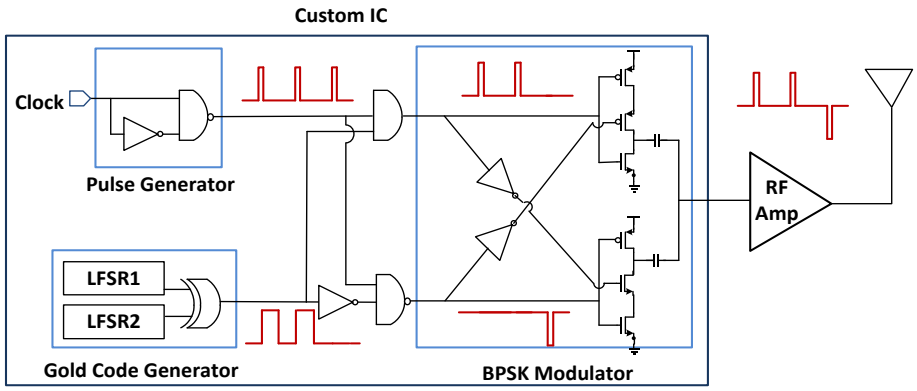

Fig. II.7. BPSK UWB transmitter architecture

The pulse generator generates pulses at each rising edge of the 10MHz clock. It consists of a NAND gate with an inverter to produce a delayed clock edge. The delay of the inverter determines the pulse width. The BPSK modulator generates a positive or negative pulse depending on the gold code bit sequence. Only one input path of the BPSK modulator is activated for each pulse, using the upper and lower paths for a positive and negative pulse, respectively. To decrease the output loading of the BPSK modulator and produce high pulse amplitudes, the output of the deactivated path is set to be floating while the activated path generates a pulse.

Gold codes are a set of binary sequences whose cross-correlation among the set is bounded into three values. Gold codes are commonly used when implementing CDMA as they allow the receiver to easily identify the corresponding transmitter which sent the signal of interest [87]. In this research, 4 different 31-bit gold codes are preset in the custom IC and can be selected by configuring external pins on the chip. Once enabled, the transmitter continuously repeats the selected code.

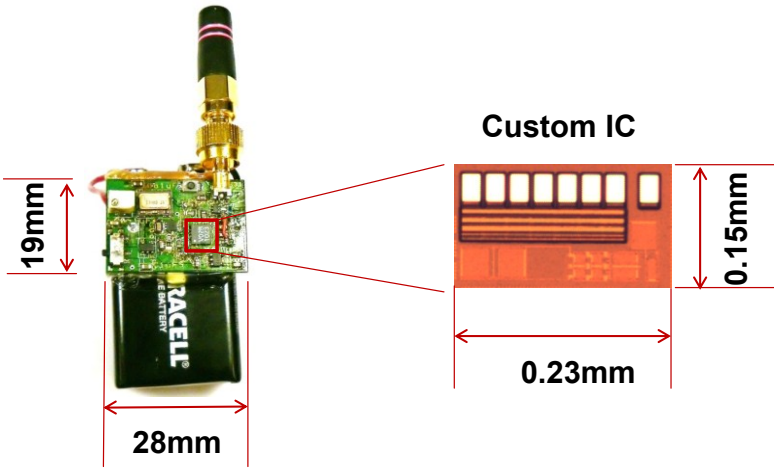

Fig. II.8. Picture of BPSK UWB transmitter

The peak output amplitude of the custom IC is 300mV, which is not sufficient to excite the channel with high SNR in a WBAN; therefore, an additional PA is used to increase the peak output amplitude to 2V. Because the signals are impulses with high peak-to-average ratio, a PA with high P1dB is necessary for matched positive and negative pulses.

II.2.2.2 Experimental result

The pictures of the transmitter along with the die photo of the custom IC, are shown in Fig. II.8. Fig. II.9 shows the transmitter output measured with a Tektronix TDS600C digital oscilloscope. Single positive and negative pulses with 2V amplitudes and 350ps widths are shown in Fig. II.9 (a). The positive and negative pulses are symmetric, which is essential for BPSK modulation. Fig. II.9 (b) shows BPSK pulses modulated by a repeated 31 bit gold code, with a pulse repetition frequency of 10MHz. Fig. II.9 (c) shows the frequency spectrum of the transmitter output measured with an Agilent N9020A spectrum analyzer.

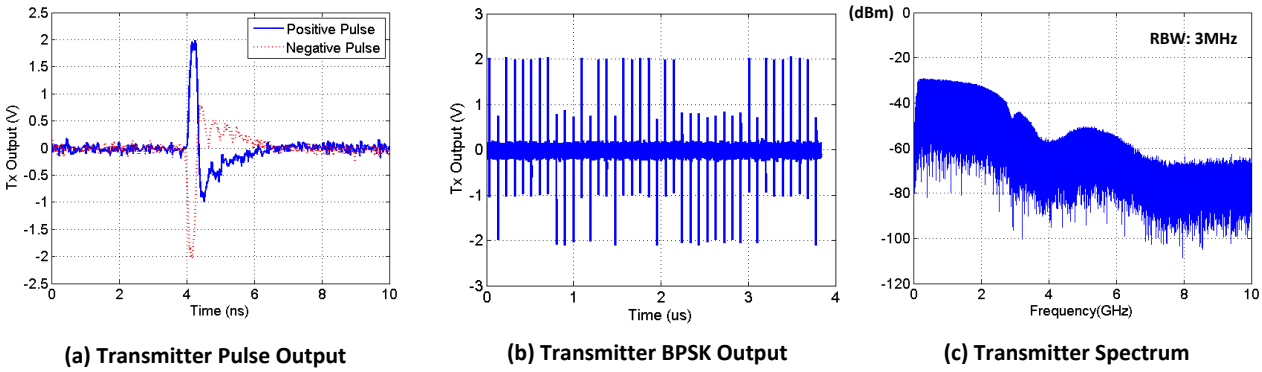

Fig. II.9. Transmitter output

The 3dB cut-off frequency is 2.0GHz; however, sufficient power for channel characterization is produced in the 2.45GHz ISM band. FCC compliance was not considered, as this is test equipment. The supply current of the custom IC, 10MHz oscillator, and RF amplifier is 27μA, 3mA, and 85mA, respectively. The supply current of the entire transmitter is 90mA, which can be powered continuously from a single 9V battery for 5 hours.

II.3 Channel Modeling using an Impulse Response

Fig. II.10 depicts the entire channel estimation system. Multiple transmitters are placed on the body that generate impulses to excite the channel response between each transmitter and a single receiver. The impulses are BPSK-modulated with unique CDMA codes so the receiver can identify them. The receiver down-converts and samples the received signal, and an FPGA implements a correlating receiver to recover an average impulse response. Snapshots of the channel are taken at a programmable rate, and the responses are saved in a local memory. When an experiment is complete, the responses are uploaded to a PC, where an FFT is performed on them to recover the frequency response of the channel vs. time. The hardware characteristics of

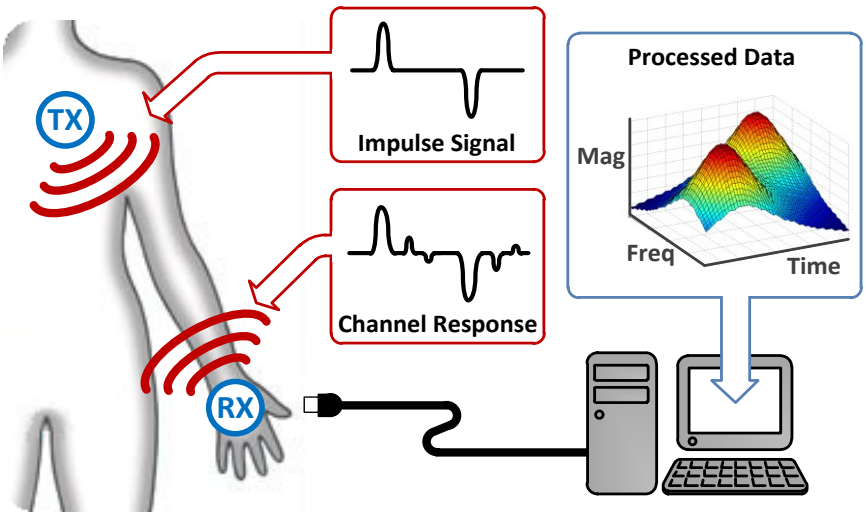

Fig. II.11. Channel estimation system

measured responses are de-embedded using a baseline response (with no multipath and at a known distance) in order to determine the impact of the time-varying channel.

II.3.1 Transmitter

BPSK UWB transmitter with a custom IC in section II.2.2 is used as a transmitter of this channel modeling system.

II.3.2 Receiver

Fig. II.11 shows the block diagram of the receiver. It consists of two LNAs (sky65047 from Skyworks), an I/Q down-conversion mixer with baseband amplifiers (AD8347 from Analog Device), a local oscillator (Si4136 from Silicon Labs), two ADCs (AD9288 from Analog Device), and an FPGA (Xilinx Spartan-3E). These components were chosen given considerations on the overall noise figure, conversion gain, frequency selectivity of the channel, and power consumption. An I/Q mixer is used to down-convert the received signal to baseband (direct-conversion receiver). A passive 5th order elliptic lowpass filter with a 50MHz cut-off

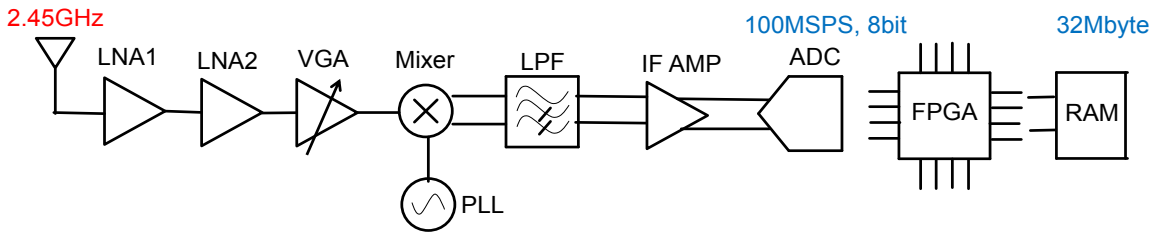

Fig. II.12. Receiver architecture

frequency is added between the mixer and the baseband amplifier to avoid aliasing and reduce high frequency noise. Finally, two 8-bit, 100 MS/s ADCs digitize the I and Q signals.

An FPGA performs all of the baseband processing on the received signals. A correlation-based receiver is implemented to correlate the incoming signal with all possible shifts of the 31-bit gold code, synchronizing the receiver to the transmitted sequence. After synchronization, 248 pulses are averaged (31 codes repeated 8 times) in order to reduce noise on the signal. The resulting signal is an average impulse response of the channel, and corresponds to one channel "snapshot." This result is sampled at a programmable rate and saved in a 32Mbyte SDRAM,

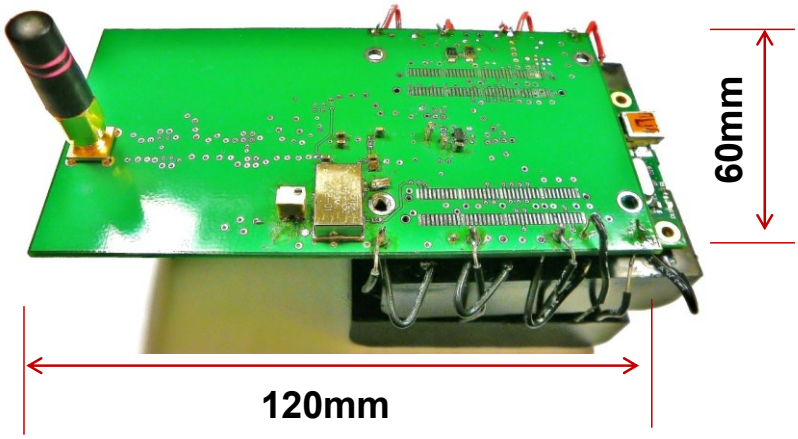

Fig. II.13. Picture of receiver

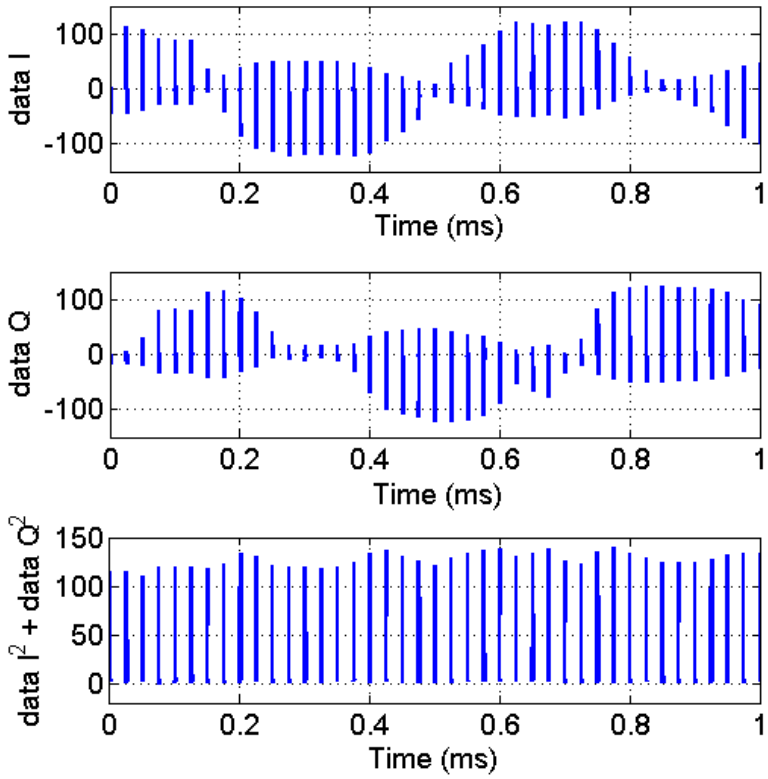

Fig. II.14. Receiver output

which can later be read by a PC over USB.

II.3.3 Experimental Results

The picture of the receiver is shown in Fig. II.12. To avoid performing operations on complex numbers on the FPGA, the receiver processes the I and Q signals separately, and saves the averaged channel responses on I and Q separately in the SDRAM. Once the values are read out, they are combined in Matlab. Fig. II.13 shows the recorded I and Q channel responses over a 1ms duration with a sampling rate of 40kS/s while the transmitter and receiver are 20cm apart in a lab environment. Each pulse is the result of 248 averaged pulses modulated by the gold code, and consists of 10 sample points. The amplitude of the I and Q data rotates due to the frequency difference of the transmitter and receiver clocks. When plotting the magnitude of (data I + j ·

data Q), only channel fluctuations are visible. The power consumption of the receiver is 1.8W, which can continuously operate off eight AA batteries for 30 hours.

II.3.4 Elevator Scenario

To demonstrate the capabilities of the hardware, a WBAN channel estimation experiment was performed in the EECS building at the University of Michigan. An experimenter held the receiver and transmitter in each hand, and walked into, rode, and walked out of an elevator. While this scenario seems routine, it produces highly dynamic channels and would be extremely difficult to measure with conventional equipment.

Fig. II.14 is the measured frequency domain data which is taken from the averaged pulse responses. The hardware characteristics are de-embedded using the -65dBm baseline response measured outside the EECS building. The frequency axis is relative to the LO frequency; therefore, 2.45GHz ± 30MHz data is shown. The FFT axis represents the magnitude of the FFT in dB of the measured impulse response; a higher number represents a stronger received signal at that frequency. The channel was sampled at a rate of 10kS/s over a total time of 35 seconds. In this experiment, we can observe that the average channel loss varies by more than 30dB. Fig. II.15 shows four 1-second intervals taken from Fig. II.14 for (a) standing in the hallway, (b) walking in the hallway, (c) walking in the elevator, and (d) standing in the elevator.

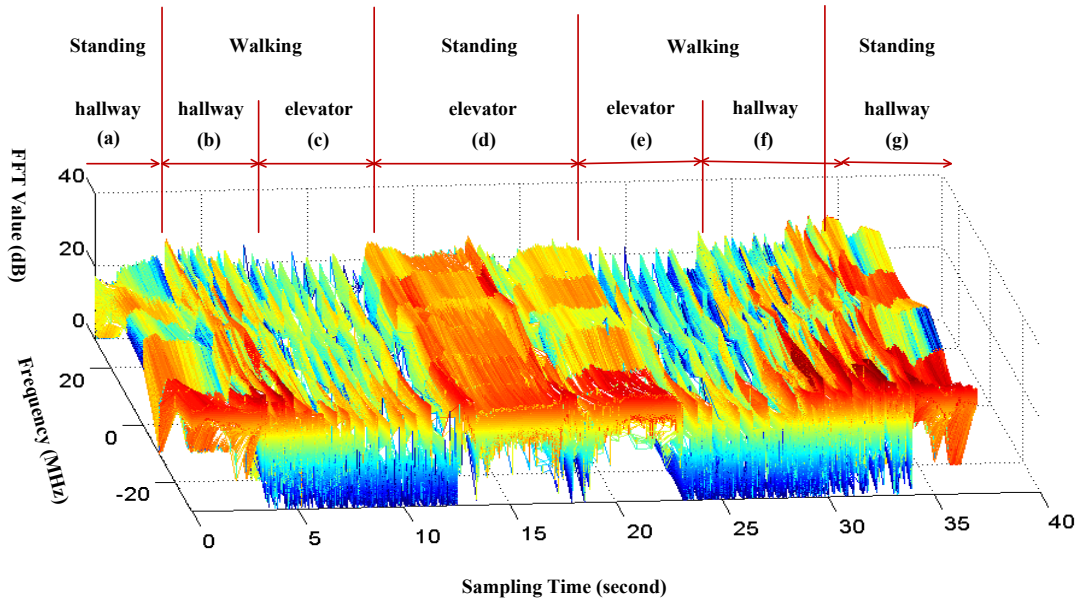

Fig. II.15. Frequency domain data of experiment scenario

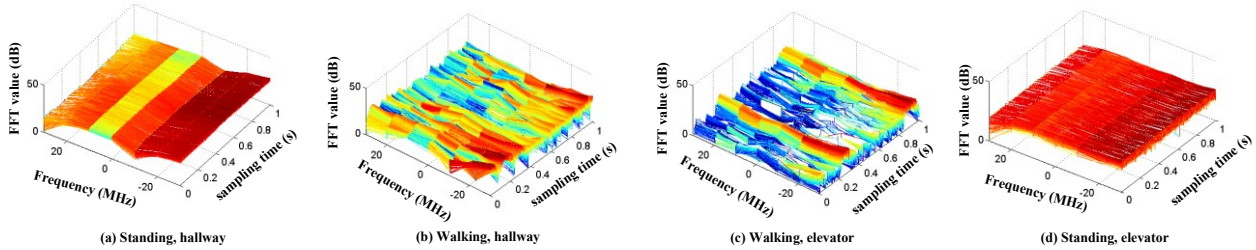

Fig. II.16. Frequency domain data of each scenario

Two major observations can be found in this data. First, the channel is stable, but shows multipath fading, when the experimenter is standing, and fluctuates when the experimenter is walking. The period of this amplitude change is approximately 0.5s, which matches the period of the experimenter's hand movement while walking. Second, the characteristics of the channel depend on the location of the experimenter; the channel inside the elevator (more multipath) is different from the channel in the hallway (less multipath). Table III summarize the specification of channel estimator using impulse response.

Table III. Specification of channel estimator using impulse response

Transmitter		Receiver	
3dB Bandwidth	2GHz	Frequency	2.4GHz±40MHz
Pulse Amplitude	2V	Gain	18 ~ 88dB
Pulse width	350ps	Storage	1.6M channels
Pulse Repetition Frequency	10MHz	Max Channel Sampling Rate	40kS/s
Modulation	31bit BPSK	Resolution	8 bits
Size	19 × 28 mm^2	Size	120 × 60 mm^2
Power	0.81W	Power	1.8W
Life Time	5 hours	Life Time	30 hours

II.4 Channel Modeling using RSSI

II.4.1 Dual-Band RSSI Recorder

Received signal strength indication (RSSI) was measured in the 900MHz and 2.4GHz bands to model channel characteristics. Multiple transmitters are placed on the body and broadcast simultaneous 900MHz and 2.4GHz tones. These tones are On-Off-Keying (OOK) modulated with unique CDMA codes so that the receiver can identify each transmitter. Multiple receivers are placed on the body and simultaneously record the RSSI of the 900MHz and 2.4GHz paths into local memory. When an experiment is complete, the RSSI data is uploaded to a PC, where post-processing is performed to correlate the data with the CDMA code, which will identify the transmitter and provide accurate RSSI measurements.

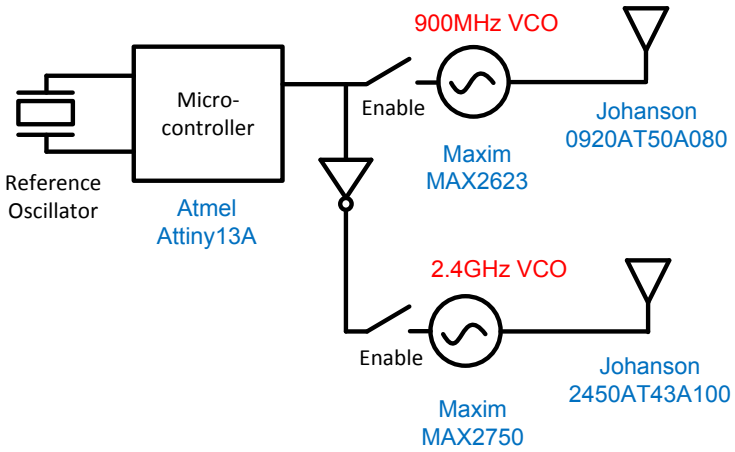

Fig. II.17. Schematic of the transmitter

The primary advantages of our hardware are that it is dual-band, portable, and has a sampling rate sufficient for Nyquist sampling of the channel response. The transmitter and receiver each have two antennas at 900MHz and 2.4GHz. Additionally, they can operate with a single portable battery. The sampling rate of the channel RSSI can be programmed up to 50 kS/s. In this work, a sampling rate of 1.34kS/s was chosen to increase sampling duration.

II.4.1.1 Transmitter

Fig. II.16 shows the schematic of the transmitter. It consists of a crystal oscillator, a microcontroller, a 900MHz oscillator (MAX2623 from MAXIM), a 2.4GHz oscillator (MAX2750 from MAXIM), a 900MHz antenna (0920AT50A080 from Johanson Technology) and a 2.4GHz antenna (2450AT43A100 from Johanson Technology). A 5MHz crystal oscillator is used as a reference clock, and a single 3V coin-sized battery is used to supply power to the entire transmitter.

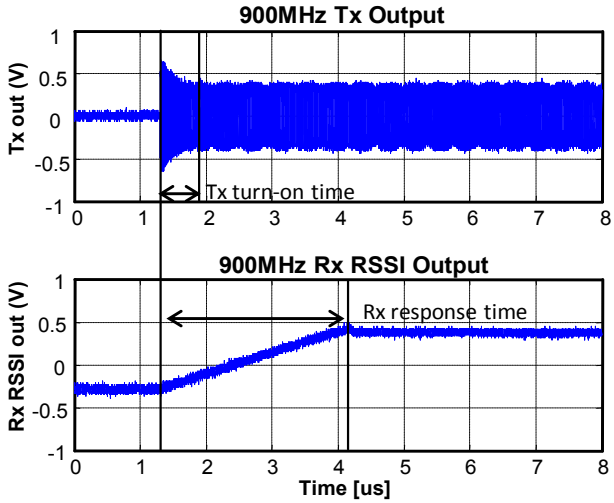

Fig. II.18. Transient response

The microcontroller generates a unique CDMA code for each transmitter and performs OOK by enabling the 900MHz and 2.4GHz VCOs with it. The enable signals for the VCOs are inverted to eliminate interference between the bands.

The one-bit time duration of the CDMA code is 24μs. As shown in Fig. II.17, this duration is much longer than the 1μs turn-on time of the VCO and the 3μs response time of the RSSI IC in the receiver. The supply current of the entire transmitter is 12.8mA, which can be powered continuously from a single 3V battery for 48 hours

II.4.1.2 Receiver

Fig. II.18 shows the schematic of the receiver. It consists of a 900MHz antenna (0920AT50A080 from Johanson Technology), a 2.4GHz antenna (2450AT43A100 from Johanson Technology), two RSSI detectors (LT 5534 from Linear Technology), two ADCs (AD7276 from Analog Devices), an FPGA (Xilinx Spartan-3E), and 32MB of SDRAM.

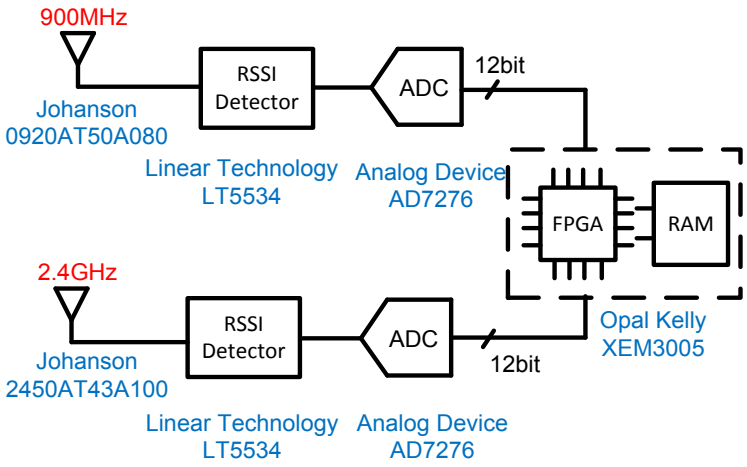

Fig. II.19. Schematic of the receiver

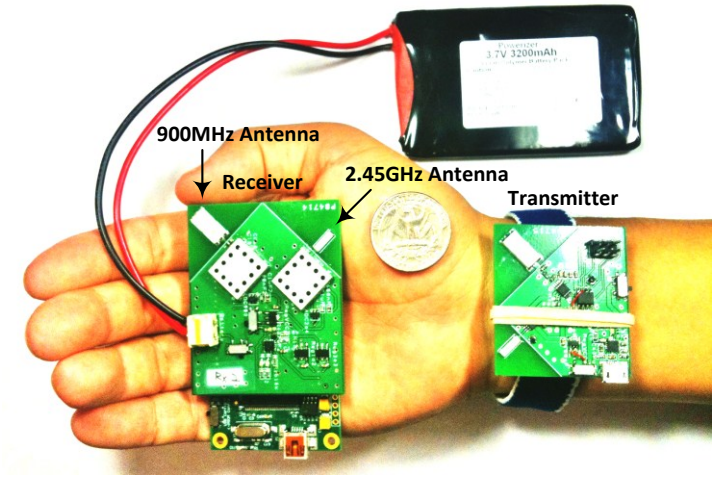

Fig. II.20. Photo of the transmitter and receiver

Each 900MHz and 2.4GHz signal is received through the antennas, and then RSSI detectors convert the received signal strengths to analog voltage outputs. The 12-bit ADCs convert these analog voltages to digital values at a programmable sampling rate. A 167kS/s sampling rate is chosen to ensure 4 sample points are recorded per CDMA bit. For a 31-bit CDMA code, this results in a sample rate of 167/31/4 = 1.3kS/s after averaging. The supply current of the whole receiver is 184mA, which can continuously operate with a rechargeable battery for 17.4 hours.

The receiver also has a power management chip, BQ24072 from Texas Instruments, so that it can charge the battery when it is connected to a USB cable.

Fig. II.19 shows a photo of the transmitter and receiver. The size of the transmitter and receiver printed circuit boards are 45mm x 40mm and 48mm x 60mm, respectively. A wrist strap is tied to the transmitter to make it easy to wear.

II.4.1.3 Support for Multiple Transmitters

To measure the correlation of multiple nodes on the body, each transmitter sends its unique Gold code. Gold codes are a set of binary sequences, where the cross-correlation of each sequence is bounded into three values. Gold codes are commonly used when implementing CDMA as they allow the receiver to easily identify the corresponding transmitter which sent the signal of interest [87].

Since RSSI values are not linear but logarithmic, an interval is required in which the received

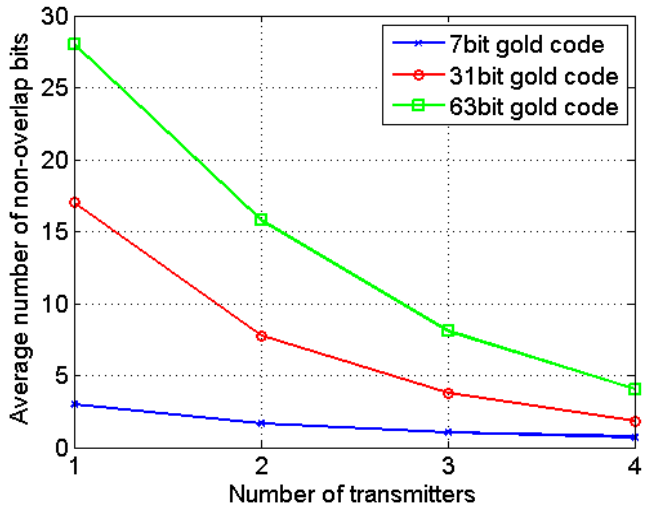

Fig. II.21. Number of transmitters vs. non-overlapping bits

power from only one transmitter is observed by the receiver in a given band in order to extract the RSSI value from that transmitter alone. As the length of the Gold code increases, the probability of having a non-overlapping bit also increases; however, the symbol duration will increase such that the channel sampling rate decreases. Therefore, a trade-off exists between the length of the Gold code and the number of transmitters supported. Fig. II.20 shows the number of transmitters versus the average number of non-overlapping bits of each Gold code, considering random shifts between all received Gold codes. In this work, the system is designed for a maximum of four transmitters; therefore, a 31-bit code is chosen.

II.4.2 Channel Measurements

The purpose of the measurement campaign was to collect data across enough controlled scenarios that we could generalize the results and compute various modeling factors. In addition we collected data correlation between bands and sensor locations. We did this in 2 stages: controlled experiments followed by measurements conducted in a real-life scenario. Each measurement was repeated three times for redundancy. Different locations on the body were targeted for each experiment.

II.4.2.1 Controlled Experiments

Fig. II. 21 shows the hardware's ability to simultaneously measure 900MHz and 2.4GHz bands at multiple locations at the same time. In this figure, path loss is shown between hip-to-wrist and hip-to-ankle in both RF bands, sampled at 1.3kS/s, for a period of 20 seconds. To calculate the path loss, including antenna gain, we subtracted the transmit power (-3dBm) from the RSSI

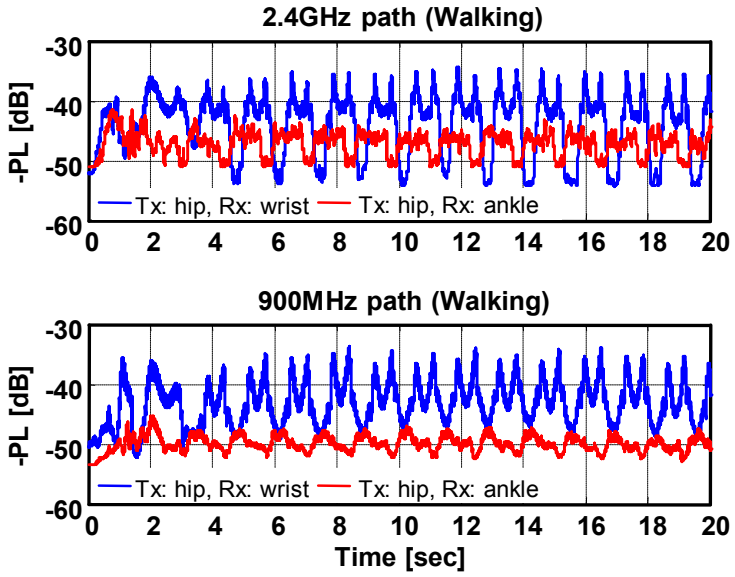

Fig. II.22. Data showing correlating band and location measurements

measurement. Fig. II.22 highlights variations in the channel periodicity for differing activity levels as well as the hardware's noise floor which is around a path loss of -54dB.

For different scenarios, the data that shows the most variability in the channel, as expected, comes from sensors on the body extremities that move the most, like the ankle or wrist. Somewhat unexpected is sensors on the body's core like the hip or chest also show a periodic response. Even with a person standing still, faint periodicity can be observed.

II.4.2.2 Observations

Some notable observations from controlled experiments are outlined in the following paragraphs.

Hip-to-chest and hip-to-wrist communication produces periodic signals with more frequency content than chest-to-chest or chest-to-write, which is due to the motion of the hip sensor. Hip to chest communication appears as a noisy sinusoid. When a person walks the hip will swing

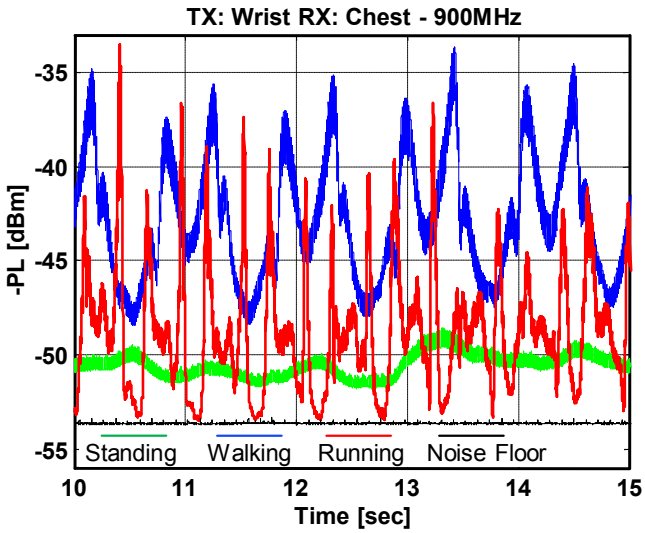

Fig. II.23. Data showing activity variations

between LOS and NLOS with the chest sensor, which creates the sinusoidal response and the frequency content appears due to the forward and backward motion between the hip and chest as the person lifts and lowers their leg. The movement of the hip and the swing of the wrist both contribute to the extra frequency content in that scenario.

The channel between the hip and ankle looks similar to a square wave when walking and the increased frequency when running makes it appear more sinusoidal. The channel between both wrists is poor due to the nearly constant NLOS condition, therefore relying mostly on multipath for communication. When running, if the user is leaning forward, small windows where the wrists pass by each other, yet are still in front of the body and therefore LOS, will produce pulse shapes in the path loss. Channel Measurement statistics are summarized in Table IV. The superscript numbers represent which sets of data were taken simultaneously. The frequency column is the fundamental frequency of the oscillations observed in the path loss. μ and σ are the mean and standard deviation of the path loss calculated in dB. The two numbers in each cell represent 900MHz and 2.4GHz data, respectively.

Table IV. Measured channel PL parameters

900/2400MHz	TX/RX	Freq [Hz]	μ [dBm]	σ [dB]
Standing	Hip/Ankle[1]	0.13/0.13	49.60/44.30	0.28/0.30
	Hip/Wrist[1]	0.28/0.17	50.34/48.74	0.90/0.99
	Wrist/Wrist[2]	0.15/0.15	53.40/53.66	0.08/0.08
	Wrist/Chest[2]	0.13/0.13	52.94/50.00	0.16/0.34
	Chest/Hip[3]	0.13/0.17	47.64/47.46	0.56/0.62
	Chest/Wrist[3]	0.15/0.15	52.75/50.70	0.20/0.93
Walking	Hip/Ankle[1]	0.99/0.99	50.24/47.55	1.13/1.85
	Hip/Wrist[1]	0.96/0.96	43.92/43.78	3.22/5.25
	Wrist/Wrist[2]	0.13/0.13	53.54/54.00	0.24/0.39
	Wrist/Chest[2]	0.97/0.97	52.13/49.68	1.51/0.80
	Chest/Hip[3]	0.68/0.92	47.24/45.92	1.20/1.43
	Chest/Wrist[3]	0.93/0.93	50.84/49.79	2.54/3.96
Running	Hip/Ankle[1]	1.78/1.78	50.70/49.77	1.48/1.24
	Hip/Wrist[1]	1.80/1.70	49.57/47.81	2.92/4.32
	Wrist/Wrist[2]	1.60/1.80	53.47/53.61	0.25/0.81
	Wrist/Chest[2]	1.76/1.74	51.37/46.45	2.28/4.33
	Chest/Hip[3]	1.71/1.72	46.93/47.16	1.62/1.93
	Chest/Wrist[3]	1.72/1.72	46.19/43.4	3.90/6.93

II.4.2.3 Scenario Experiment

The second set of measurements in Fig. II.22 targeted a real life scenario where the user does not conduct strictly repetitive motions, therefore creating a non-uniform channel. The scenario involved the test subject playing tennis outdoors which involves lots of fast, abrupt movements in an outdoor environment with the receiver on the left hip and transmitter on the left wrist. Since the channel is non-uniform, non-uniform windowing was also used to break the channel data into smaller segments that were analyzed for periodicity. The time domain channel response and resulting Activity Factors (defined in II.4.3) plotted across time are shown in Fig.

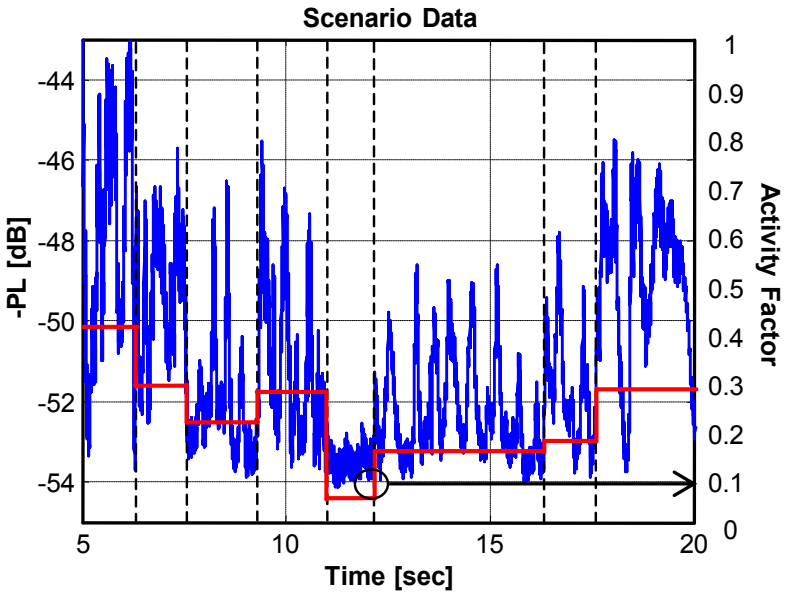

Fig. II.24. Channel waveform of a real-life scenario

II.23. The purpose of this experiment was to observe natural movement and the change in frequency and standard deviation across time. It is possible that a person will remain stationary for a given period of time in a way that restricts communication between sensors. However, the data shows that a person in motion will see periodic peaks and valleys in the channel response between sensors, therefore allowing communication in at least some periods of time.

II.4.2.4 Correlation among Sensor Locations and Bands

In addition to collecting data for the development of a model, we correlated the channel response of different sensor locations on the body as well as different frequency bands. This information is useful in WBAN applications that may want to use knowledge of one channel to predict the quality of another channel to a different location on the body or in a different band for asymmetric wireless links [73].

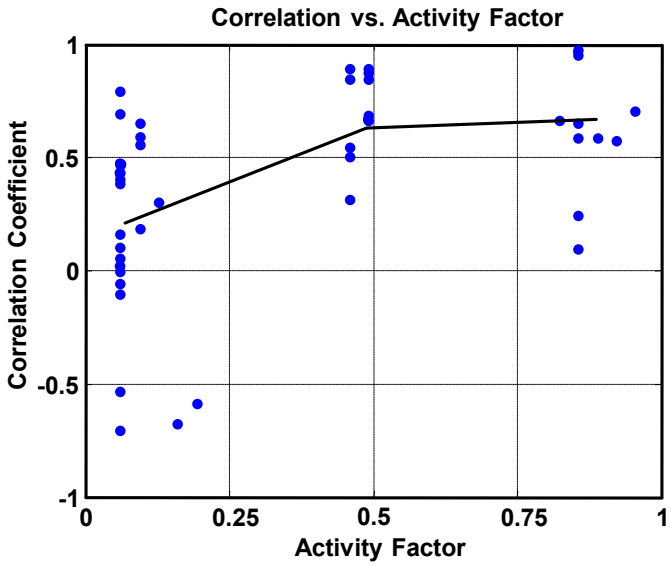

Fig. II.25. Correlation between bands

Frequency correlation is calculated by taking the correlation coefficient between the 900MHz and 2.4GHz bands of the same experiment. Results can be seen in Fig. II.24. Frequency correlation increases in relation to motion. The correlation coefficient while standing is difficult to predict, with values being essentially random, ranging from 0.78 to -0.72. Once the test subject starts moving, correlations increase significantly with gradual improvement between walking and running. One conclusion we can draw from this is that while a person is stationary, and a good channel is observed in one frequency band, it is no guarantee that another frequency band will be good. However, when the person is active, there is high probability that both bands will have good channels at the same time.

The correlation among sensor locations that was the strongest involved sensors from the wrist and hip communicating with a sensor on the chest. This scenario, shown in Fig. II.25, had a negative correlation coefficient of -0.73 and is a result of one sensor being placed on the upper half of the body (wrist) and lower half (hip). While the test subject was moving, the wrist would

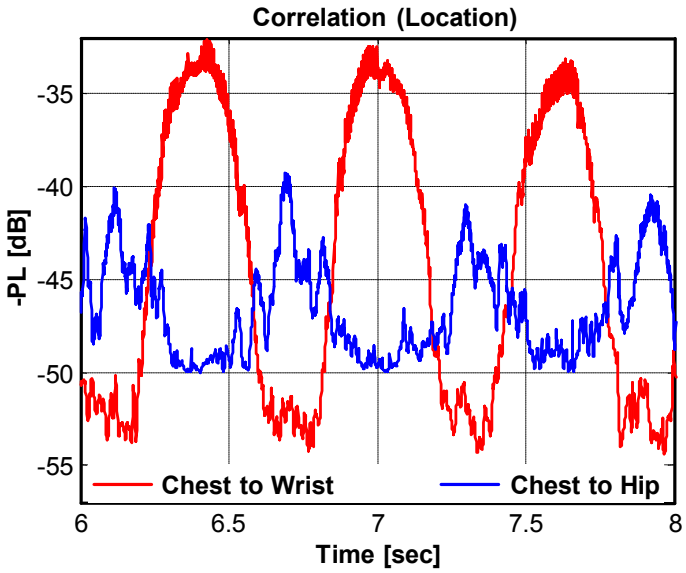

Fig. II.26. Correlation between locations

swing forward and into a LOS scenario with the sensor on the chest while the hip would be moving backwards and out of LOS communication. This type of location correlation can be exploited for multi-hop routing, or if sensors are on the same side of the body and placed on opposing extremities so that one sensor is always in good communication while walking or running. The communication location that had the least correlation was wrist to wrist.

II.4.3 Periodic BAN Channel Model

Our goal is to gain insight into the channel and develop simplified models that aid in the system level design of radios for WBANs. This includes observing path loss in different scenarios as well as developing correlations between multiple sensors at different locations on the body and between different frequency bands. The controlled experiments, shown in Table IV, are aimed to characterize the complex WBAN channel as simply as possible to allow for quick and effective design calculations.

The periodic behavior of the channel seen in the data is relatively sinusoidal and can be represented as such. The proposed path loss of the periodic WBAN channel model with respect to time is:

$$PL(t)[dB] = PL(d) + 2\sigma_{PL}\sin(2\pi \cdot f_{PL} \cdot t) \quad (7)$$

where PL(d) is the path loss in dB calculated from one of the 802.15.6 [65] models (e.g. equation (1) or (2) in section 1.4), and the second term adds the modeled channel periodicity where σ_{PL} is the standard deviation, in dB, and f_{PL} is the fundamental path loss repetition frequency.

This model complements the WBAN equations that calculate path loss, by adding a periodic dimension to the equation which accounts for the periodicity we measured in the channel. Using measured statistics, equation (7) closely models the channel as seen in the top plot of Fig. II.25, which represents someone walking with a transmitter on their wrist and receiver on their chest. Note the model drops below the hardware's noise floor.

II.4.3.1 Impact of Activity and Location

Numerous individual factors contribute to the path loss and periodicity of the channel including antenna placement and direction, multipath, and body shape. To integrate all these factors would produce a complicated model that would not be practical for WBAN design. To generalize the results of our channel modeling measurement campaign we will introduce two variables that will account for all the different factors in a simple and intuitive way. Even though extremely simple by design, these factors are shown to predict the channel response with accuracy sufficient for WBAN design. The two variables are Activity Factor (AF) and Location Factor (LF).

$$\text{Activity Factor (AF)} = \text{amount of user movement} \tag{8}$$

Activity Factor is a qualitative number between 0 and 1 that is approximated by knowing what a person is doing. If a person is completely still the Activity Factor is 0 and a full sprint is 1. Activity between these extremes is qualitatively assigned an intermediate number based on a best guess as to the relative level of activity. For example, AF=0.25 is someone working at a computer, AF=0.5 is someone walking, and AF=0.75 is someone jogging. The frequency component of the path loss in (7) is then calculated as:

$$f_{PL} = f_{max} \cdot AF \tag{9}$$

where f_{max} is the maximum capable frequency of the user's movement, which we assume is 2Hz which is a good general assumption. Under normal circumstances, it is highly unlikely that an average person would exceed a fundamental repetition rate greater than 2Hz. From (9) we back-calculate the activity factor for our measured results, which are reported in Table V.

σ_{PL} in (7) is dependent on Activity Factor as well as a Location Factor (LF). LF is a

Table V. Activity and location factors derived from data

Action	TX/RX	Activity Factor	Location Factor
STANDING	Hip/Ankle	0.07	0.24
	Hip/Wrist		0.70
WALKING	Wrist/Wrist	0.45	1.00
	Wrist/Chest		0.60
RUNNING	Chest/Hip	0.85	0.24
	Chest/Wrist		0.60

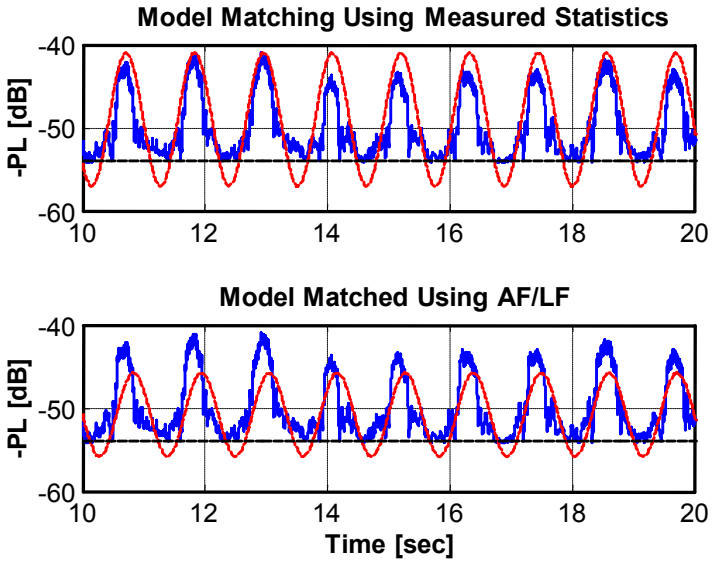

Fig. II.27. Model validation

qualitative measure of the relative motion between two sensors, normalized between 0 and 1. An LF of 1 represents sensor locations that have a lot of movement relative to each other, e.g. wrist to wrist communication. An LF of 0 represents sensor locations with little to no relative movement, e.g. two sensors on the chest. Location factor between these extremes is qualitatively assigned an intermediate number, e.g. LF=0.25 for hip to ankle, LF=0.5 for chest to wrist, and LF=0.75 is hip to wrist. σ_{PL} used in (7) is then calculated as:

$$\sigma_{PL} = k_{\sigma} \cdot LF \cdot \log_{10}(1 + f_{PL}) \tag{10}$$

where k_{σ} is a data fitting parameter. Based on our controlled experiments, ranging from standing to running with sensors at various locations, $k_{\sigma} = 15$ results in the best overall fit.

The bottom plot of Fig. II.26 shows the periodic model compared to the same walking data as the top of the plot, but this time using AF and LF. Using an AF and LF of 0.45 and 0.6

respectively, show a close match, which is also close to our estimates of an AF of 0.5 for walking and an LF of 0.5 for chest to wrist communication.

II.4.4 Impact on Radio Design

If we assumed that the transmitted power and antenna gain are 0dBm and 0dB, respectively, then we can claim that the sensitivity of the receiver is equivalent to the measured path loss. Using our developed channel model we can determine the tradeoff between communication time and receiver power using representative receivers from literature: a low power receiver [53] and a wake up receiver [45]. We will also include a commercial Bluetooth low energy radio [64] for comparison.

II.4.4.1 Power Savings

Using the same channel data plotted in Fig. II.27 with computed AF, LF and PL(d) values of 0.45, 0.6, and -52dB respectively, we can compare the performance of the two low power radios. A radio [53] with a power of 2.1mW and a sensitivity of -100dBm would be the primary receiver in the WBAN and always remain active. At 100% operation the total power would be 2.1mW and it can communicate 100% of the time. Using the wake-up receiver [45] with a sensitivity of -56dBm, one can turn off the main receiver to save energy while leaving the wake up receiver always listening for packets, or even utilize the wake up receiver for low speed communication. By applying variables determined from our channel model we calculate the percentage of time the wake up receiver can communicate as:

$$T_p = \frac{\pi/2 - \arcsin((S_{RX} - PL(d))/2\sigma_{PL})}{\pi} \quad (11)$$

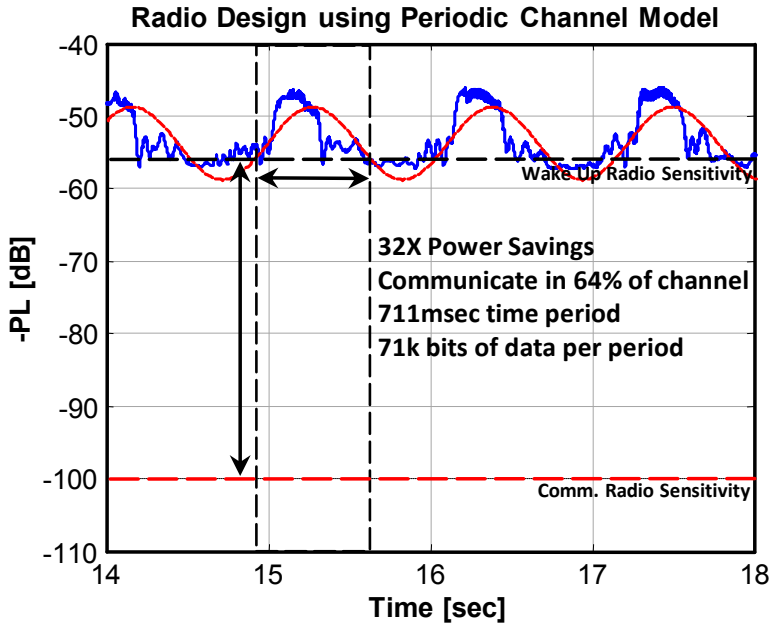

Fig. II.28. Radio design

where S_{RX} is the sensitivity of the receiver and σ_{PL} is calculated from equation (9) and (10), respectively. Using equation (11), we determine the wake up receiver will communicate 64% of the time at a power consumption of 65µW. Utilizing channel periodicity by reducing the receiver sensitivity results in a 32X power savings over the standard low power radio while being able to communicate in 64% of the channel compared to 100%. Comparing against the commercial Bluetooth radio, with a power of 58.6mW and a sensitivity of -87dBm, th is results in a 900X power savings.

II.4.4.2 Communication Performance

Assuming a MAC that reacts to the periodicity of the channel and knowing the percentage of time one can communicate, the time interval spent in the good channel region can be calculated. Continuing with our example; given 64% communication time and a frequency of 0.9Hz, we can

estimate the channel to be good for 711ms at a time. Knowing the wake up receiver has a data rate of 100kbps; one can transmit roughly 71kbits of information during these periods of good channel communication as seen in Fig. II.27.

II.5 Summary

UWB transmitters are introduced in section II.2. Section II.2.1 presents an UWB transmitter with SRD and section II.2.2 presents an UWB transmitter with a custom IC.

Section II.3 presented a portable WBAN channel estimator using an impulse response, with specifications summarized in Table III. The transmitter sends BPSK modulated pulses and the receiver records the averaged channel response. Experimental results of the channel response in an elevator scenario highlight the capabilities of this hardware. While the channel in this scenario appears to be highly dynamic, it also shows the periodicity and stable statistics of the channel. Ultimately, WBAN systems should exploit these properties to build better channel predictions and lower power radios.

In section II.4, we proposed a simplified channel model to complement the current WBAN path loss models by exploiting channel periodicity in a WBAN with dual band RSSI recorder. We introduced custom hardware used to collect the data needed for this analysis and the measurement campaign designed to develop the model. We introduced Activity and Location factors to allow computation of the model's parameters. We demonstrated this model by fitting it to data collected during the measurement campaign. Finally, by making informed decisions regarding these tradeoffs we were able to show a power efficient design improvement example.

Chapter III.
Theoretical Analysis of a -32dBm Sensitivity RF Power Harvester Operating in Subthreshold

III.1 Introduction

The goal of this chapter is to design a power harvester maximizing the sensitivity. In order for the rectifier to work with very low input power, all transistors of the rectifier should operate in the subthreshold region. In subthreshold, the calculation of output voltage of the rectifier is different from that in the saturation region; therefore, new equations using subthreshold transistors are derived as a contribution of this thesis. A voltage boosting circuit is implemented off-chip to further increase the sensitivity. An impedance matching network is the best for voltage boosting, if there is no power loss except from the rectifier [26]-[30]. This work provides a method of implementing this matching network while taking into account lossy components.

III.2 Sub-threshold CMOS rectifier

Fig. III.1 shows a schematic of the Dickson multiplier with diode-connected transistors [94]. The output voltage of the N stage CMOS rectifier, V_{OUT}, when the load current is zero, is:

$$V_{OUT} = 2N \cdot (V_A - V_{DROP}) \tag{12}$$

where V_A is the input voltage amplitude of the CMOS rectifier and V_{DROP} is the voltage drop across the diode-connected FETs. An accurate equation for V_{DROP} is presented in [23] when all

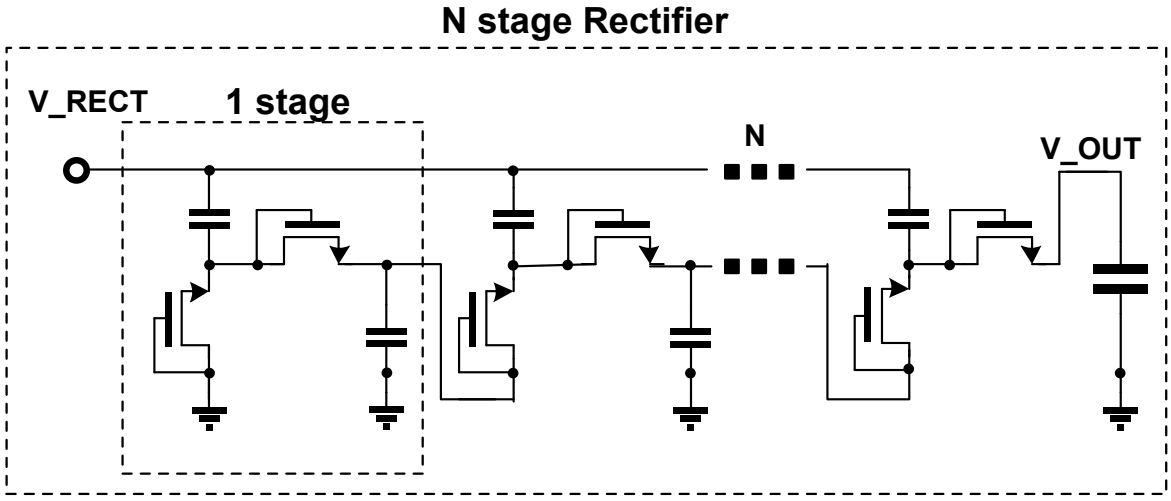

Fig. III.1. Schematic of N stage CMOS rectifier

transistors operate in the saturation region. In this work, V_{OUT} and V_{DROP} are calculated provided that all transistors operate in the subthreshold region.

Let us consider the one stage rectifier in Fig. III.2.(a). V_{RECT} is the input voltage of the rectifier, V_{FET} is the source voltage of FET1, and I_{FET1} is the current through FET1. The drain current of FET1, I_{FET1}, in subthreshold is [88]:

$$I_{FET1} = I_S \cdot e^{\frac{V_{GS}-V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}}\right) \tag{13}$$

where I_S is the zero-bias current for the given device, V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage, V_{TH} is the threshold voltage, n is the subthreshold slope, and V_T is the thermal voltage ≈ 26mV.

As it can be seen in Fig. III.2.(b), the direction of I_{FET1}changes during phase I and II as V_{FET} becomes positive or negative. That means the drain and source of FET1 are exchanged during

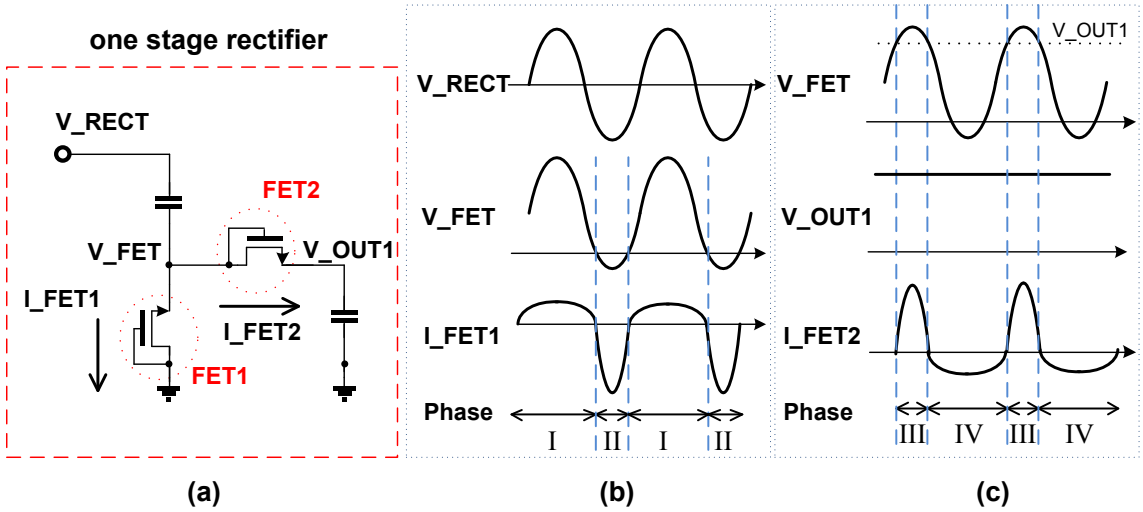

Fig. III.2. One stage rectifier (a) schematic (b) voltage and current of FET1 (c) voltage and current of FET2

phase I and II. In phase I when V_{FET} is positive, V_{GS} of FET1 is zero, and V_{DS} equals V_{FET}. In phase II when $V_{FET}$is negative, V_{GS} and V_{DS} equal $-V_{FET}$. Therefore, I_{FET1} in phase I and II is:

$$I_{FET1\,phase\,I} = I_S \cdot e^{\frac{-V_{TH}}{nV_T}}\left(1 - e^{-\frac{V_{FET}}{V_T}}\right) \quad \text{in phase I} \qquad (14)$$

$$I_{FET1\,phase\,II} = I_S \cdot e^{\frac{-V_{FET}-V_{TH}}{nV_T}}\left(1 - e^{\frac{V_{FET}}{V_T}}\right) \quad \text{in phase II} \qquad (15)$$

In steady-state, the average charge through FET1 for one cycle should be zero, since we assume that load current is zero.

$$Q_I = \int_0^{t1} I_{FET1\,phase\,I}\,dt = Q_{II} = \int_{t1}^{T} I_{FET1\,phaseII}\,dt \qquad (16)$$

where T is the period of the input voltage, and t_1 is the duration of phase I.

Applying equations (14) and (15) to equation (16) results in

$$\int_0^{t1} I_S \cdot e^{\frac{-V_{TH}}{nV_T}}\left(1 - e^{-\frac{V_{FET}}{V_T}}\right) dt = \int_{t1}^{T} I_S \cdot e^{\frac{-V_{FET}-V_{TH}}{nV_T}}\left(1 - e^{\frac{V_{FET}}{V_T}}\right) dt \qquad (17)$$

If we assume that $n = 1$,

$$\int_0^{t1} I_S \cdot e^{\frac{-V_{TH}}{V_T}} \left(1 - e^{-\frac{V_{FET}}{V_T}}\right) dt = \int_{t1}^{T} I_S \cdot e^{\frac{-V_{TH}}{V_T}} \left(e^{-\frac{V_{FET}}{V_T}} - 1\right) dt \tag{18}$$

$$\int_0^{T} I_S \cdot e^{\frac{-V_{TH}}{V_T}} \left(1 - e^{-\frac{V_{FET}}{V_T}}\right) dt = 0 \quad \Leftrightarrow \quad \int_0^{T} e^{-\frac{V_{FET}}{V_T}} dt = T \tag{19}$$

If V_{FET} can be expressed as $V_A \sin(\omega t) + V_{DC\,FET}$,

$$\int_0^{T} e^{-\frac{V_A \sin(\omega t)}{V_T}} dt \cdot e^{-\frac{V_{DC\,FET}}{V_T}} = T \tag{20}$$

As we know $\int_0^T e^{-\frac{V_A \sin(\omega t)}{V_T}} dt = T \cdot I_0\left({}^{V_A}/_{V_T}\right)$ where I_0 is the zero-th order modified Bessel function of the first kind, $V_{DC\,FET}$ can be derived as,

$$V_{DC\,FET} = V_T \cdot ln\left(I_0\left({}^{V_A}/_{V_T}\right)\right) \tag{21}$$

The same procedure can be used for FET 2 in Fig. III.2.(c) to calculate the output voltage of a one stage rectifier, V_{OUT1}. In phase III when V_{FET} is higher than V_{OUT1}, V_{GS} of FET2 is $V_{FET} - V_{OUT1}$, and V_{DS} is $V_{FET} - V_{OUT1}$. In phase IV when V_{FET} is lower than V_{OUT1}, V_{GS} is 0, and V_{DS} is $V_{OUT1} - V_{FET}$. Therefore, I_{FET2} in phase III and IV are:

$$I_{FET2\,phase\,III} = I_S \cdot e^{\frac{V_{FET} - V_{OUT1} - V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{FET} - V_{OUT1}}{V_T}}\right) \quad \text{in phase III} \tag{22}$$

$$I_{FET2\,phase\,IV} = I_S \cdot e^{\frac{-V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{OUT1} - V_{FET}}{V_T}}\right) \quad \text{in phase IV} \tag{23}$$

In steady-state, the average charge through FET2 for one cycle should be zero.

$$Q_{III} = \int_0^{t2} I_{FET2\ phase\ III}\, dt = Q_{IV} = \int_{t2}^{T} I_{FET2\ phaseIV} dt \tag{24}$$

If equation (22) and (23) are applied to equation (24),

$$\int_0^{t2} I_S \cdot e^{\frac{V_{FET}-V_{OUT1}-V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{FET}-V_{OUT1}}{V_T}}\right) dt = \int_{t2}^{T} I_S \cdot e^{\frac{-V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{OUT1}-V_{FET}}{V_T}}\right) dt \tag{25}$$

If we assume that $n = 1$,

$$\int_0^{t2} I_S \cdot e^{\frac{-V_{TH}}{V_T}} \left(e^{\frac{V_{FET}-V_{OUT1}}{V_T}} - 1\right) dt = \int_{t2}^{T} I_S \cdot e^{\frac{-V_{TH}}{V_T}} \left(1 - e^{\frac{V_{FET}-V_{OUT1}}{V_T}}\right) dt \tag{26}$$

$$\int_0^{T} I_S \cdot e^{\frac{-V_{TH}}{V_T}} \left(e^{\frac{V_{FET}-V_{OUT1}}{V_T}} - 1\right) dt = 0 \quad \Leftrightarrow \quad \int_0^{T} e^{\frac{V_{FET}-V_{OUT1}}{V_T}} dt = T \tag{27}$$

If $V_{FET} = V_A\, sin(\omega t) + V_{DC\ FET}$ is applied,

$$\int_0^{T} e^{\frac{V_A\, sin(\omega t)}{V_T}} dt \cdot e^{\frac{V_{DC\ FET}-V_{OUT1}}{V_T}} = T \tag{28}$$

$$V_{OUT1} = V_{DC\ FET} + V_T \cdot ln\left(I_0\left({}^{V_A}/_{V_T}\right)\right) = 2V_T \cdot ln\left(I_0\left({}^{V_A}/_{V_T}\right)\right) \tag{29}$$

The output voltage of an N-stage rectifier can be deduced from output of the one stage rectifier.

$$V_{OUT} = 2N \cdot V_T \cdot ln\left(I_0\left({}^{V_A}/_{V_T}\right)\right) \tag{30}$$

$$V_{OUT} \approx 2N\left(V_A - {}^{V_T}/_{2} \cdot ln\left({}^{2\pi V_A}/_{V_T}\right)\right) \quad if\ V_A \gg V_T \tag{31}$$

$$V_{OUT} \approx \frac{N \cdot {V_A}^2}{2V_T} \quad if\ V_A \ll V_T \tag{32}$$

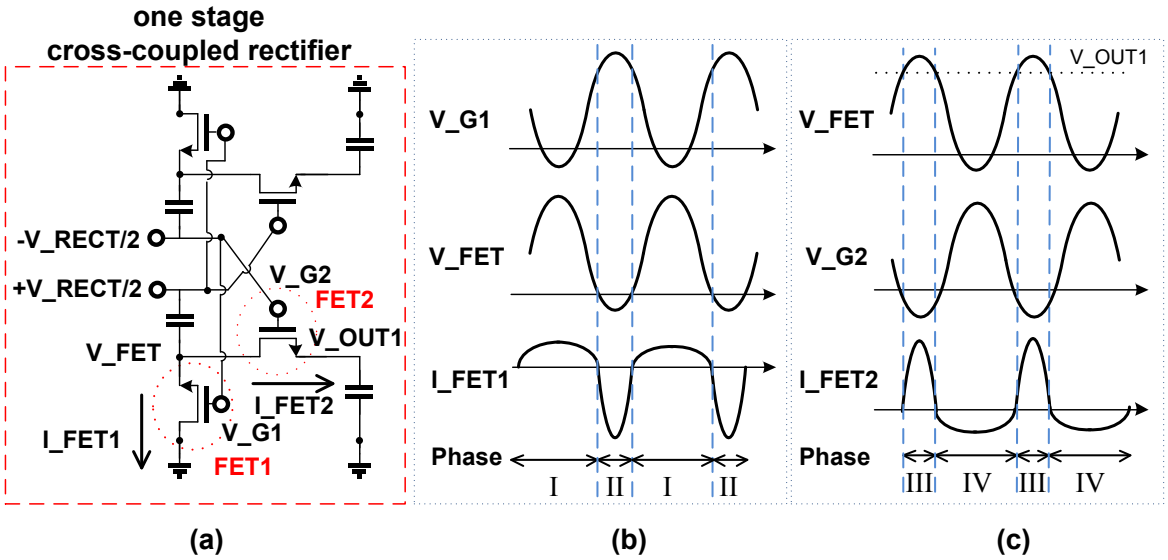

Fig. III.3. One stage cross-coupled rectifier (a) schematic (b) voltage and current of FET1 (c) voltage and current of FET2

where I_0 is the zero-th order modified Bessel function of the first kind

This equation (30) has a similar form including the modified Bessel function when diodes are used instead of FETs [26]. According to equation (30), transistor size and threshold voltage have no effect on V_{OUT}. The size and threshold voltage only effect the charging time and the equivalent input resistance of the rectifier.

A cross-coupled rectifier is another architecture of a rectifier that sometimes shows better power conversion efficiency that a single-ended rectifier [27]. In this paper, the output voltage of a cross-coupled rectifier in the subthreshold region is compared with the output voltage of a single-ended rectifier. Let us assume a cross-coupled rectifier is applied with differential input, $\pm V_{RECT}/2$, and the gates of FET1 and FET2 are connected to the opposite input, $-V_{RECT}/2$ with some DC levels $V_{DC\,G1}$, and $V_{DC\,G2}$ in Fig. III.3.(a). The same procedure used to analyze the single-ended rectifier can be used to calculate the output voltage of a cross coupled rectifier.

$$Q_I = \int_0^{t1} I_{FET1\ phase\ I}\, dt = Q_{II} = \int_{t1}^{T} I_{FET1\ phaseII} dt \tag{33}$$

$$\int_0^{t1} I_S \cdot e^{\frac{V_{G1}-V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{FET}}{V_T}}\right) dt = \int_{t1}^{T} I_S \cdot e^{\frac{V_{G1}-V_{FET}-V_{TH}}{nV_T}} \left(1 - e^{\frac{V_{FET}}{V_T}}\right) dt \tag{34}$$

$$\int_0^{T} I_S \cdot e^{\frac{V_{G1}-V_{TH}}{V_T}} \left(1 - e^{-\frac{V_{FET}}{V_T}}\right) dt = 0 \tag{35}$$

If $V_{G1} = -(V_A/2)\, sin(\omega t) + V_{DC\ G1}$, and $V_{FET} = (V_A/2)\, sin(\omega t) + V_{DC\ FET\ CC}$ are applied,

$$\int_0^{T} e^{\frac{-V_A/2\, sin(\omega t)}{V_T}} dt = \int_0^{T} e^{\frac{-V_A\, sin(\omega t)}{V_T}} dt \cdot e^{-\frac{V_{DC\ FET\ CC}}{V_T}} \tag{36}$$

$$V_{DC\ FET\ CC} = V_T \cdot ln\left(I_0\left(V_A/V_T\right) \Big/ I_0\left(V_A/2V_T\right)\right) \tag{37}$$

By calculating the charge during phase III and IV in Fig. III.3.(c), the output voltage of the cross-coupled rectifier can be derived.

$$Q_{III} = \int_0^{t2} I_{FET2\ phase\ III}\, dt = Q_{IV} = \int_{t2}^{T} I_{FET2\ phaseIV} dt \tag{38}$$

$$\int_0^{t2} I_S \cdot e^{\frac{V_{G2}-V_{OUT1}-V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{FET}-V_{OUT1}}{V_T}}\right) dt$$

$$= \int_{t2}^{T} I_S \cdot e^{\frac{V_{G2}-V_{FET}-V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{OUT1}-V_{FET}}{V_T}}\right) dt \tag{39}$$

$$\int_0^{t2} I_S \cdot e^{\frac{V_{G2}-V_{TH}}{V_T}} \left(e^{-\frac{V_{OUT1}}{V_T}} - e^{-\frac{V_{FET}}{V_T}}\right) dt = \int_{t2}^{T} I_S \cdot e^{\frac{V_{G2}-V_{TH}}{V_T}} \left(e^{-\frac{V_{FET}}{V_T}} - e^{-\frac{V_{OUT1}}{V_T}}\right) dt \tag{40}$$

$$\int_0^{T} I_S \cdot e^{\frac{V_{G2}-V_{TH}}{V_T}} \left(e^{-\frac{V_{OUT1}}{V_T}} - e^{-\frac{V_{FET}}{V_T}}\right) dt = 0 \tag{41}$$

If $V_{G2} = -(V_A/2)\,sin(\omega t) + V_{DC\,G2}$, and $V_{FET} = (V_A/2)\,sin(\omega t) + V_{DC\,FET\,CC}$ are applied,

$$\int_0^T e^{\frac{-V_A/2\,sin(\omega t)}{V_T}} dt \cdot e^{-\frac{V_{OUT1}}{V_T}} = \int_0^T e^{\frac{-V_A\,sin(\omega t)}{V_T}} dt \cdot e^{-\frac{V_{DC\,FET\,CC}}{V_T}} \tag{42}$$

$$V_{OUT1} = V_{DC\,FET\,CC} + V_T \cdot ln\left(I_0\left({}^{V_A}/_{V_T}\right) \Big/ I_0\left({}^{V_A}/_{2V_T}\right)\right)$$

$$= 2V_T \cdot ln\left(I_0\left({}^{V_A}/_{V_T}\right) \Big/ I_0\left({}^{V_A}/_{2V_T}\right)\right) \tag{43}$$

The output voltage of an N-stage cross-coupled rectifier can be derived as,

$$V_{OUT\,CC} = 2N \cdot V_T \cdot ln\left(I_0\left({}^{V_A}/_{V_T}\right) \Big/ I_0\left({}^{V_A}/_{2V_T}\right)\right) \tag{44}$$

Comparing equations (30) and (44), equation (30) is always greater than equation (44), meaning the single-ended rectifier is always better than the cross-coupled rectifier in the subthreshold region.

Power consumption of one stage of a single-ended rectifier is the sum of the powers consumed by FET1 and FET2.

$$Power = N \cdot \frac{1}{T}\int_0^T V_{FET} \cdot I_{FET1} + (V_{FET} - V_{OUT1}) \cdot I_{FET2} dt \tag{45}$$

$$\int_0^T V_{FET} \cdot I_{FET1} dt$$

$$= \int_0^{t1} V_{FET} \cdot I_S \cdot e^{\frac{-V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{FET}}{V_T}}\right) dt + \int_{t1}^T -V_{FET} \cdot I_S \cdot e^{\frac{-V_{FET}-V_{TH}}{nV_T}} \left(1 - e^{\frac{V_{FET}}{V_T}}\right) dt$$

$$= \int_0^T V_{FET} \cdot I_S \cdot e^{\frac{-V_{TH}}{V_T}} \left(1 - e^{-\frac{V_{FET}}{V_T}}\right) dt \qquad \text{(assume n = 1)}$$

$$= \int_0^T (V_A \sin(\omega t) + V_{DC\,FET}) \cdot I_S \cdot e^{\frac{-V_{TH}}{V_T}} \left(1 - e^{-\frac{V_A \sin(\omega t) + V_{DC\,FET}}{V_T}}\right) dt$$

$$= I_S \cdot e^{\frac{-V_{TH}}{V_T}} \left(T \cdot V_{DC\,FET} - T \cdot V_A \cdot I_1\left(-\frac{V_A}{V_T}\right) e^{\frac{-V_{DC\,FET}}{V_T}} - T \cdot V_{DC\,FET} \cdot I_0\left(\frac{V_A}{V_T}\right) e^{\frac{-V_{DC\,FET}}{V_T}}\right)$$

$$= I_S \cdot e^{\frac{-V_{TH}}{V_T}} T \cdot V_A \cdot I_1\left(\frac{V_A}{V_T}\right) \Big/ I_0\left(\frac{V_A}{V_T}\right) \qquad (46)$$

Where I_0 and I_1 are the zero-th and first order modified Bessel function of the first kind.

$$\int_0^T (V_{FET} - V_{OUT1}) \cdot I_{FET2} dt$$

$$= \int_0^{t2} (V_{FET} - V_{OUT1}) \cdot I_S \cdot e^{\frac{V_{FET} - V_{OUT1} - V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{FET} - V_{OUT1}}{V_T}}\right) dt$$

$$+ \int_{t2}^T -(V_{FET} - V_{OUT1}) \cdot I_S \cdot e^{\frac{-V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{OUT1} - V_{FET}}{V_T}}\right) dt$$

$$= \int_0^T (V_{FET} - V_{OUT1}) \cdot I_S \cdot e^{\frac{V_{FET} - V_{OUT1} - V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{FET} - V_{OUT1}}{V_T}}\right) dt \quad \text{(assume n = 1)}$$

$$= \int_0^T (V_A \sin(\omega t) - V_{DC\,FET}) \cdot I_S \cdot e^{\frac{V_A \sin(\omega t) - V_{DC\,FET} - V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_A \sin(\omega t) - V_{DC\,FET}}{V_T}}\right) dt$$

$$= I_S \cdot e^{\frac{-V_{TH}}{nV_T}} \left(T \cdot V_A \cdot I_1\left(\frac{V_A}{V_T}\right) e^{\frac{-V_{DC\,FET}}{V_T}} - T \cdot V_{DC\,FET} \cdot I_0\left(\frac{V_A}{V_T}\right) e^{\frac{-V_{DC\,FET}}{V_T}} + T \cdot V_{DC\,FET}\right)$$

$$= I_S \cdot e^{\frac{-V_{TH}}{V_T}} T \cdot V_A \cdot I_1\left(\frac{V_A}{V_T}\right) \Big/ I_0\left(\frac{V_A}{V_T}\right) \qquad (47)$$

If equation (46) and (47) are applied to equation (45),

$$Power = 2N \cdot V_A \cdot I_S \cdot e^{\frac{-V_{TH}}{V_T}} \frac{I_1\left(\frac{V_A}{V_T}\right)}{I_0\left(\frac{V_A}{V_T}\right)} \tag{48}$$

The effective input resistance of the rectifier, R_{RECT}

$$R_{RECT} = \frac{{V_A}^2}{2 \cdot Power} = \frac{V_A e^{\frac{V_{TH}}{V_T}}}{4NI_S} \frac{I_0\left(\frac{V_A}{V_T}\right)}{I_1\left(\frac{V_A}{V_T}\right)} \tag{49}$$

The input capacitance of the rectifier is the sum of the parasitic capacitance of the FETs, storage capacitors, input pad, and PCB. This depends on the transistor size, storage capacitor size, and the number of stages in the rectifier.

III.3 Voltage boosting circuit

Fig. III.4 shows a simplified schematic of the RF power harvester, where R_{RAD} is the antenna impedance. To increase the sensitivity of the system, a voltage boosting circuit between the antenna and the rectifier is proposed.

In the ideal case that the voltage boosting circuit is lossless, an impedance matching network results in the highest sensitivity, since it can deliver the maximum voltage V_{RECT} and power to the rectifier. For the ideal lossless matching network,

$$V_{RECT} = \sqrt{\frac{R_{RECT}}{R_{RAD}}} \cdot \frac{V_{IN}}{2} \tag{50}$$

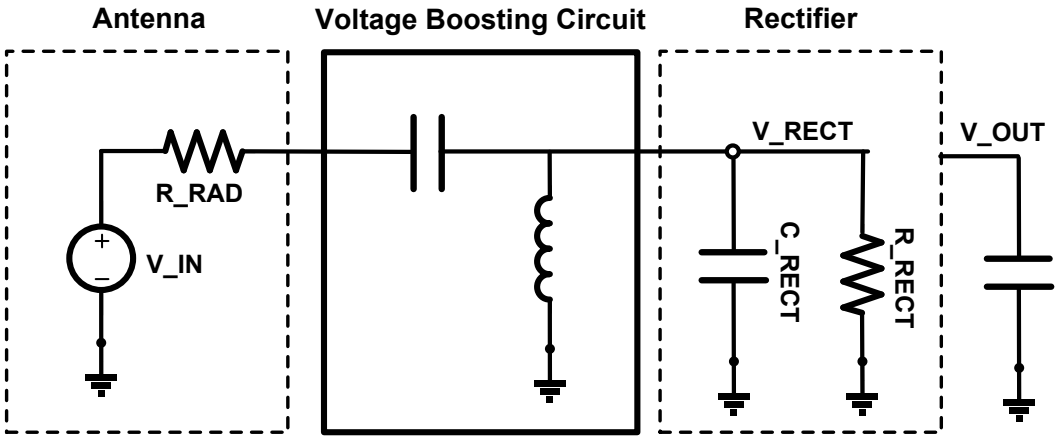

Fig. III.4. Antenna, voltage boosting circuit and rectifier

In realistic environments, the matching network is not lossless and limited by finite Q of e.g. inductors. Furthermore, if the input resistance of the rectifier is much larger than R_{RAD}, which is typically the case, then it becomes more difficult to implement the matching network with low-Q components. According to the Bode-Fano limit [30], [89], the bandwidth of the ideal matching network is limited by

$$BW \leq -\frac{\pi}{R_{RECT} \cdot C_{RECT} \cdot ln(|\Gamma|)} \tag{51}$$

where Γ is the reflection coefficient of the matching network. For a reasonable value of $\Gamma = 0.5$ with $R_{RECT} = 1\text{M}\Omega$ and $C_{RECT} = 1\text{pF}$, BW is less than 500kHz, which is also difficult to implement with low-Q devices.

Fig. III.5 shows the proposed voltage boosting circuit with a parallel inductor, where R_{LP} is the parasitic resistance of the inductor due to finite Q. To minimize the loss in the voltage boosting circuit, only one inductor is used. The equation of V_{RECT} in the lossy matching network is still

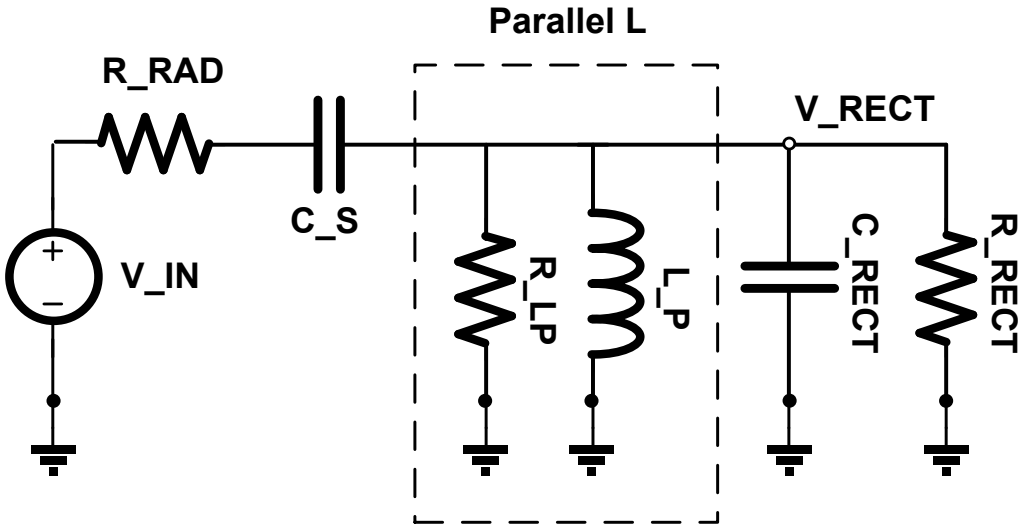

Fig. III.5. Voltage boosting circuit with parallel L

given by (50) if R_{RECT} is replaced with $R_{RECT} /\!/ R_{LP}$. In this work, high-Q air core inductors from Coilcraft Inc. are used to increase R_{LP}.

$$V_{RECT} = \sqrt{\frac{R_{RECT} /\!/ R_{LP}}{R_{RAD}}} \cdot \frac{V_{IN}}{2} \tag{52}$$

III.4 Experimental results

The custom IC is fabricated in an IBM 130nm CMOS process. Fig. III.6 shows the die photo of the fabricated chip. The total size is 1mm x 1mm, including all rectifier implementations. CMOS rectifiers with several types of transistors and different numbers of stages are implemented. Table VI summarizes the measurement results of ZVT (zero threshold voltage transistor), ZVTDG (zero threshold voltage transistor with thick oxide), LVT (low threshold voltage transistor), NFET (normal threshold voltage transistor) and NFET33 (3.3V I/O transistor with thick oxide) rectifiers with different numbers of stages. The input impedance at -25dBm

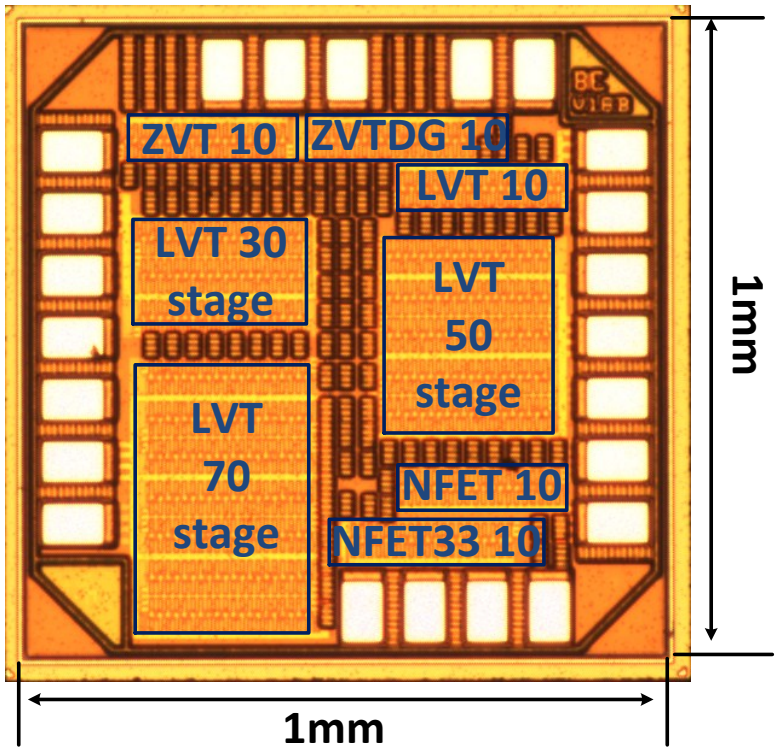

Fig. III.6. Die micrograph

input power, sensitivity for 1V V_{OUT}, and charging time (10% to 90% V_{OUT}) when the input is at the sensitivity level for a 1nF load capacitor are provided with and without a matching network.

The impedance of each rectifier is measured with an Agilent N5230A network analyzer at 915MHz. R_{RECT} and C_{RECT} are calculated based on the measured impedance value taking into account a 1.6nH inductance from the bondwire and PCB. The 70-stage LVT rectifier has the lowest R_{RECT}, and the 10-stage NFET33 rectifier has the highest R_{RECT}, which is expected given that higher power loss in the rectifier results in lower input resistance. C_{RECT} is similar for all types of transistors, but increases as the number of stages increases.

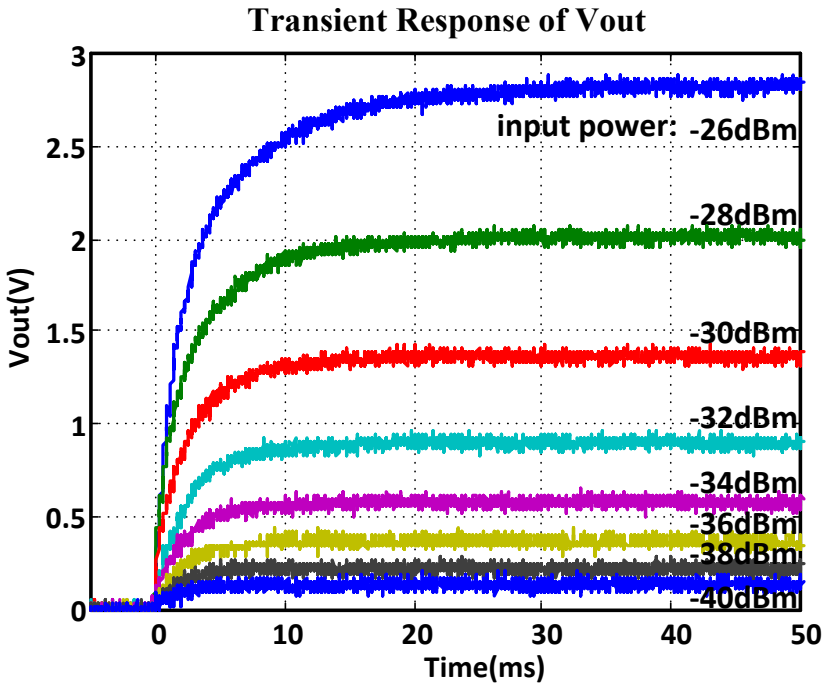

Fig. III.7. Transient response of 30-stage LVT rectifier

The sensitivity of a 10-stage rectifier without a matching network is around -14dBm, independent of the transistor type, which matches well with equation (30). Sensitivity increases

Table VI. Measurement results for each CMOS rectifier

		ZVT 10stage	ZVTDG 10stage	LVT 10stage	NFET 10stage	NFET33 10stage	LVT 30stage	LVT 50stage	LVT 70stage
without Voltage Boosting Circuit	Impedance	2.2-j39	1-j43	0.8-j31	0.8-j36	0.7-j50	1.2-j34	1.2-j24	1.3-j13
	RRECT(kΩ)	1.06	2.73	2.02	2.55	5.01	1.56	0.92	0.38
	CRECT(pF)	3.60	3.33	4.33	3.85	2.94	4.02	5.23	7.81
	1V VOUT Sensitivity	-14.0 dBm	-14.5 dBm	-13.6 dBm	-13.9 dBm	-13.2 dBm	-19.7 dBm	-21.5 dBm	-22.3 dBm
	Charging Time (1nF)	0.6ms	7.5ms	42ms	32s	285s	98ms	159ms	242ms
with Voltage Boosting Circuit	Impedance	21-j42	37+j10	19.6-j44	58-j27	110-j0.3	51-j6.5	40-j3	76-j2
	1V VOUT Sensitivity	-22.1 dBm	-27.1 dBm	-22.9 dBm	-22.6 dBm	-25.6 dBm	-31.7 dBm	-32.1 dBm	-31.8 dBm
	Charging Time (1nF)	2.2ms	1.4ms	4.8s	99s	370s	5.6ms	155ms	109ms

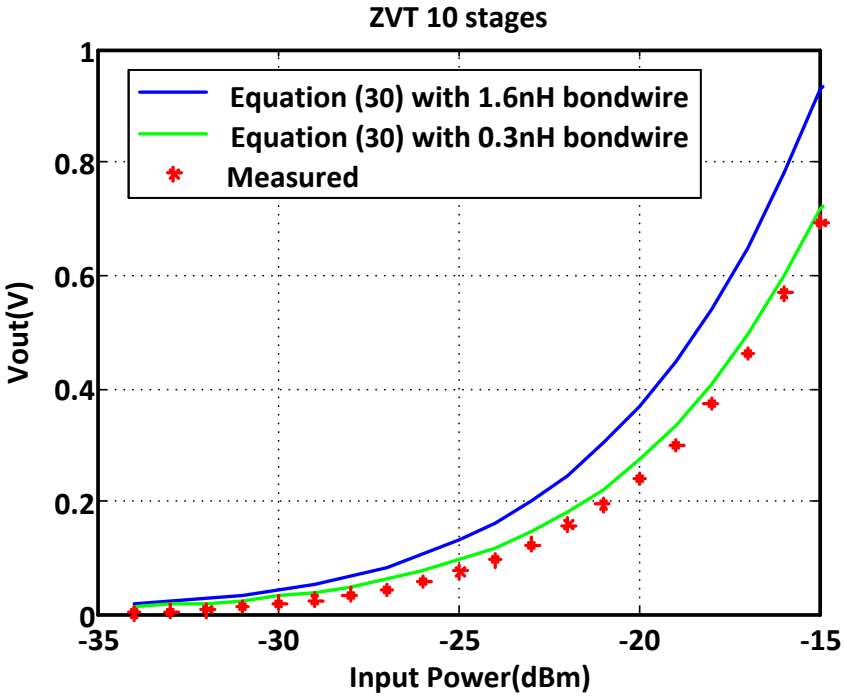

Fig. III.8. Equation (30) vs. measurement of 10-stage ZVT rectifier

as the number of stages increases. The sensitivity with a matching network is a function of both the number of stages and the transistor type, because the amount of voltage boosting from the matching network depends on the input impedance of the rectifier, and the low accuracy of the off-chip matching networks at 915MHz. The highest sensitivity of -32.1dBm is achieved with 50 stages, using LVT transistors and a matching network.

The charging time without voltage boosting increases with increasing V_{TH} and number of stages due to the small I_{FET} and large capacitance. Charging time also increases with the size of the final storage capacitor (1nF in our measurements). Fig. III.7 shows the transient response of the 30-stage LVT rectifier with off-chip matching network, as the input power is varied. Charging time increases as the input power increases because V_{OUT} increases faster than I_{FET}.

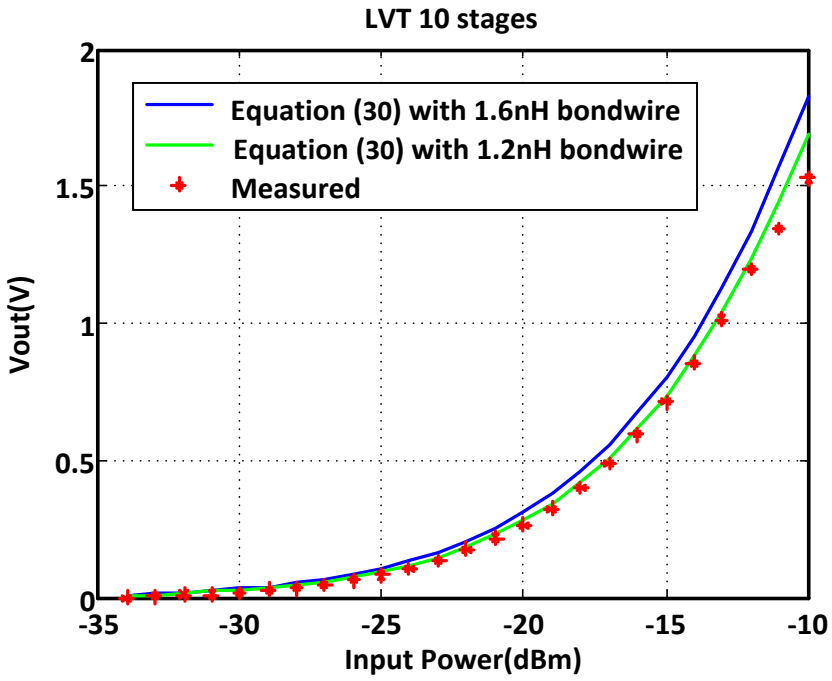

Fig. III.9. Equation (30) vs. measurement of 10-stage LVT rectifier

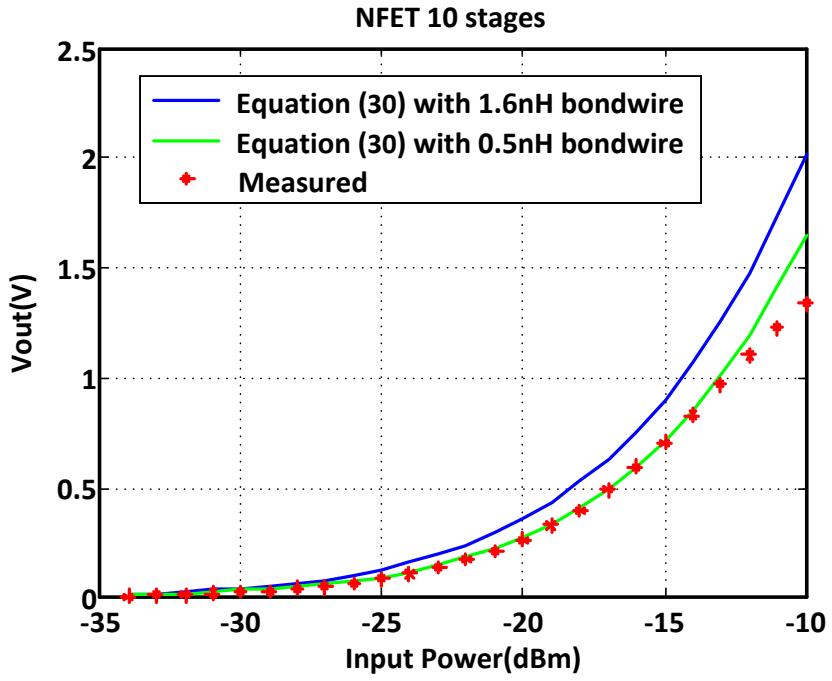

Fig. III.10. Equation (30) vs. measurement of 10-stage NFET rectifier

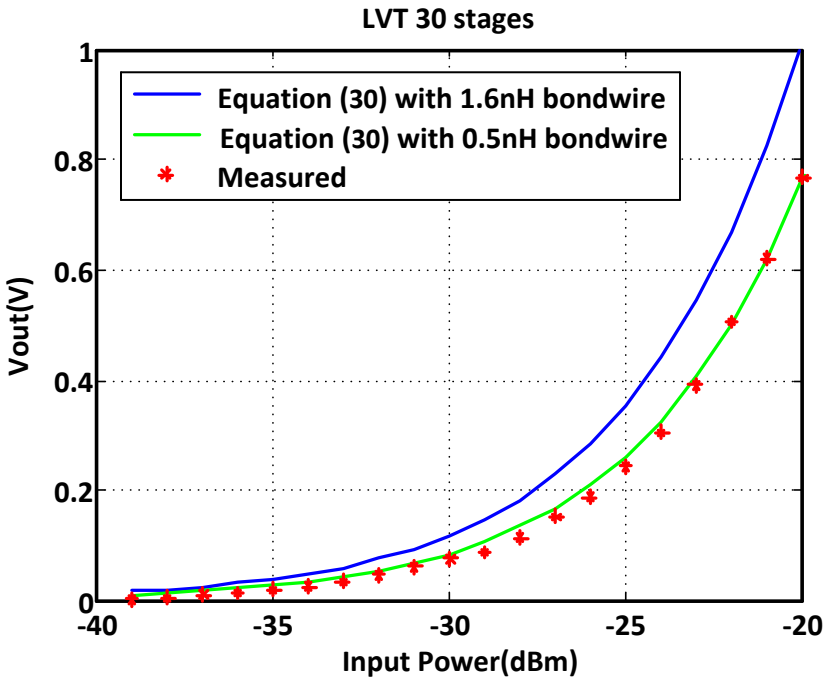

Fig. III.11. Equation (30) vs. measurement of 30-stage LVT rectifier

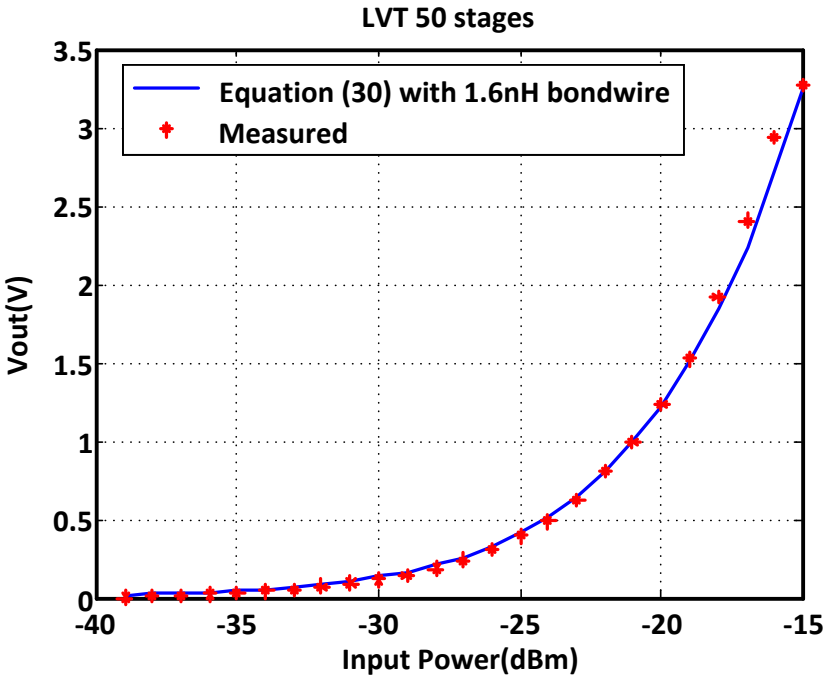

Fig. III.12. Equation (30) vs. measurement of 50-stage LVT rectifier

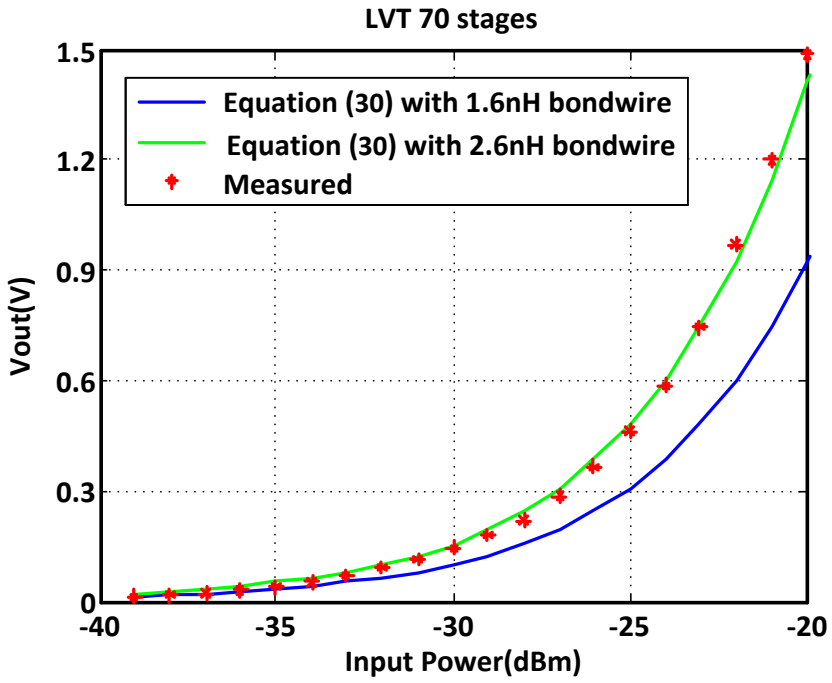

Fig. III.13. Equation (30) vs. measurement of 70-stage LVT rectifier

When voltage boosting is added, the charging time varies greatly due to the interaction between the matching network and the input impedance of the rectifier.

Fig. III.8-13 show the measured V_{OUT} and V_{OUT} from equation (30) of the 10-stage ZVT, 10-stage LVT, 10-stage NFET, 30-stage LVT, 50-stage LVT, 70-stage LVT rectifier. In this equation, voltage amplitude of the rectifier, V_A is a result of voltage divider of antenna voltage, V_{ANT} with the rectifier impedance, Z_{RECT} and 50Ω antenna impedance, R_{ANT}.

$$V_A = V_{ANT} \cdot (Z_{RECT} - jwL_{BOND})/(Z_{RECT} + R_{ANT})$$

Z_{RECT} is the measured result from table II, and the bondwire inductance, L_{BOND} is assumed as 1.6nH. These measurement results match with equation (30), however these results are sensitive to the value of bondwire inductance as shown in the figures.

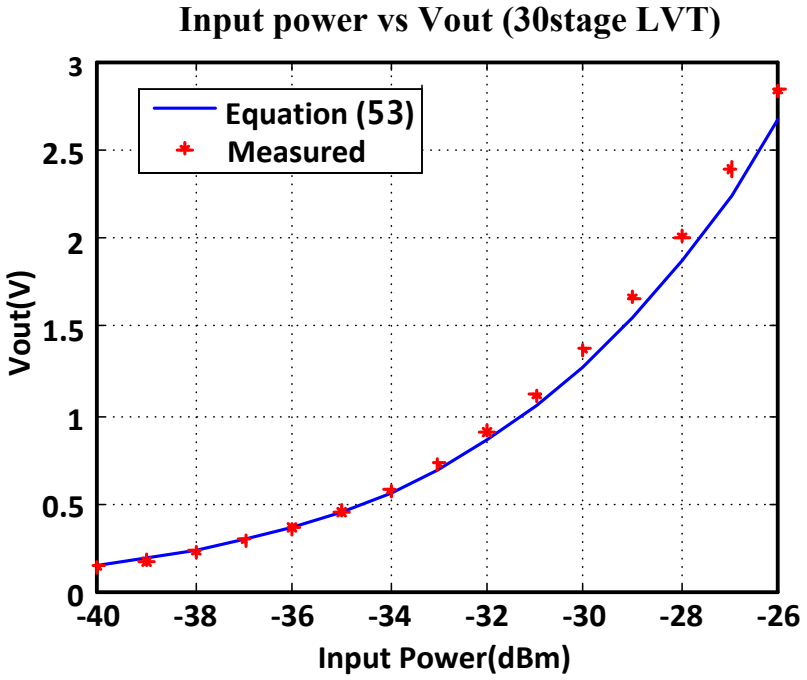

Fig. III.14. Equation (53) vs. measurement of 30-stage LVT rectifier

Fig. III.14 shows V_{OUT} of the 30-stage LVT rectifier with a matching network predicted from equation (53) and measurements where $R_{RECT} = 1560\Omega$ from Table VI, $L_P = 8.1\text{nH}$, and $Q_{LP} = 180$ from the Coilcraft Inc. datasheet. There is a slight discrepancy when V_{OUT} is large, likely because the transistors are no longer in the subthreshold region.

III.5 Design strategy

The final equation for V_{OUT} including the matching network is:

$$V_{OUT} = 2N \cdot V_T \cdot ln\left(I_0\left(\frac{1}{2}\sqrt{\frac{R_{LP} /\!/ R_{RECT}}{R_{RAD}}}\frac{V_A}{V_T} \right) \right) \tag{53}$$

For maximum sensitivity, large N, large R_{RECT} and small C_{RECT} are preferred, since R_{LP} is inversely proportional to C_{RECT} ($R_{LP} = \omega L_P Q_{LP}$, and L_P is inversely proportional to C_{RECT}). However, R_{LP} sets an upper limit on V_{OUT}, beyond which increasing R_{RECT} or reducing C_{RECT} is not helpful.

There are four design variables to consider for the CMOS rectifier. These are the number of stages, transistor type, transistor size and storage capacitor size. These affect V_{OUT}, R_{RECT}, C_{RECT}, and the charging time. More stages decreases R_{RECT}, and increases C_{RECT} linearly. The number of stages also linearly increases V_{OUT}. Therefore, there is an optimum N depending on the limit of R_{LP}. Increasing transistor size decreases R_{RECT}, and increases C_{RECT} with linear slopes. Higher V_{TH} of the transistor increases R_{RECT} exponentially, but has no effect on C_{RECT}. Therefore, if the charging time is not important, smaller transistor size and higher V_{TH} are preferred. The size of the load capacitor increases C_{RECT} linearly but has no effect on R_{RECT} so that a smaller capacitance is preferred. However, it should be relatively large compared to parasitic capacitance.

Chapter IV.
A 116nW Multi-band CDMA based Wake-Up Receiver with Automatic Interference Rejection in 0.13µm CMOS

IV.1 Introduction

Wireless sensors spend most of the time in an ultra-low-power sleep state with their radios off to conserve energy. This presents a problem for remotely waking up and synchronizing to these nodes. Wake-up radios (WRX) are a viable solution [40][41][42][61][95], but only if their active power is below the sleep power of the node, otherwise the WRX power dominates and dictates the lifetime of the node. With digital sleep power being reported in the nW range, this presents a significant challenge to WRX design. A simple method for reducing the power of a WRX is to reduce sensitivity, which is tolerable for short-range communication and when the primary goal is a lifetime of multiple years [95]. For example, with a receiver sensitivity of -40dBm, 6m communication at 400MHz is possible with only 0dBm transmit power. This is suitable for a broad range of medical and internet of things applications.

Most published WRXs use energy detection architectures to keep power low; however, any signal at the proper frequency can trigger a false wake-up of these radios, and false wake-ups result in significant amounts of wasted energy on the node. In order to prevent this, a WRX must have enough local processing to differentiate a wake-up event from interference without use of the node's main processor. This chapter presents a 116nW WRX complete with crystal reference,

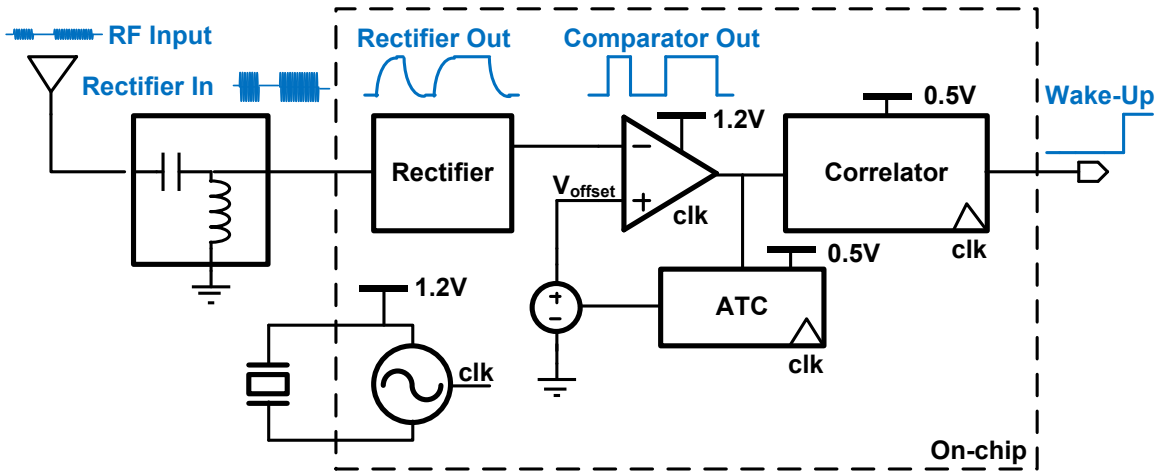

Fig. IV.1. CDMA WRX system architecture

interference compensation, and all the necessary baseband processing, such that a selectable 31-bit code is required to toggle a wake-up signal. The front-end operates over a broad frequency range, tuned by an off-chip band-select filter and matching network, and is demonstrated in the 403MHz MICS band, and the 915MHz and 2.4GHz ISM bands. Additionally, the baseband processor implements automatic threshold feedback to detect the presence of interferers and dynamically change the receiver's sensitivity, mitigating the jamming problem inherent to previous energy-detection WRXs.

IV.2 System Architecture

Fig. IV.1 shows a block diagram of the WRX. An OOK modulated RF signal passes through a passive input matching network that filters and boosts the signal before going on-chip. A 30-stage rectifier down-converts the RF signal to baseband, which is then sensed by the dynamic comparator clocked at 4X the chip-rate. The offset voltage of the comparator is controlled by the ATC (Automatic Threshold Controller) which compensates for interferers. A bank of 4 parallel,

bit-shifted 31-bit correlators continuously compare the received chip sequence with a programmable wake-up code, and toggles the wake-up signal only when a correlation result exceeds a programmable correlator threshold. The reference clock for the receiver is generated using an off-chip 50kHz crystal with an integrated oscillator. The oscillator and comparator operate from a 1.2V supply while all the digital logic operates in subthreshold at 0.5V. Because of the broadband design in the front end rectifier, the WRX can operate from the 400MHz to 2.4GHz bands, and can be tuned using a band-select filter and matching network off-chip. Sleep power was carefully designed using thick-oxide header devices on all the circuits.

IV.2.1 Circuit Description

In this section, the major circuit blocks of the WRX are explained in detail. All circuits use a thick-oxide PMOS header to improve sleep power.

IV.2.1.1 Off-chip matching network

For the WRX, a 2 element off-chip matching network was used and provided a passive 5dB voltage boost. The input impedance of the chip was measured on a network analyzer to be 23-j35 Ω at 400MHz so a 12pF series capacitor and a 15.7nH shunt inductor were used. Devices like BAW or FBAR resonators can also be used to tune to the desired frequency of operation.

IV.2.1.2 RF rectifier

Because the sensitivity has been reduced, an LNA is not necessary to amplify the received signal. Instead a zero-power RF rectifier replaces the LNA, saving significant power and allowing communication in the nanowatt range. As seen in Fig. IV.2, the rectifier's structure is

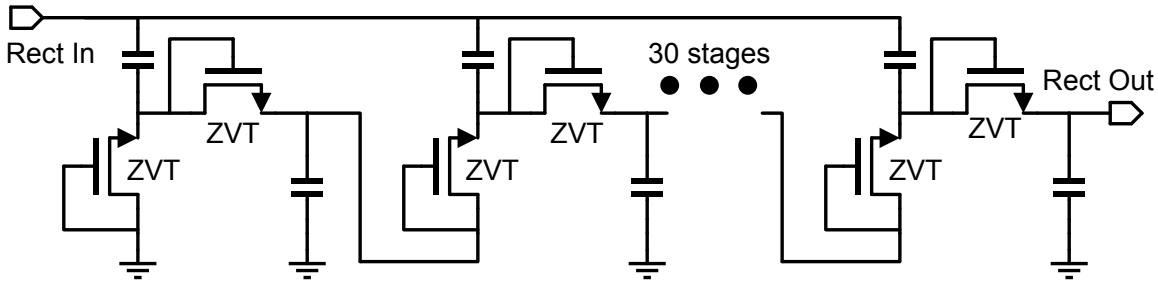

Fig. IV.2. RF rectifier used as the front end of the WRX

the same as the Dickson Multiplier [94], but the output voltage calculation is different because all transistors operate in subthreshold due to the small RF input same as in chapter III [96].

This subthreshold rectifier uses zero-threshold transistors and 30 stages to achieve sufficient RF gain with a fast charging time. The input impedance of the chip is 23-j35 Ω at 400MHz, 12-j13 Ω at 900MHz and 88-j5.8 Ω at 2.4GHz. The Q factor of the input impedance is low, due to a voltage limiter that prevents the rectified voltage from exceeding the breakdown voltage of the FETs, so a broadband matching network could be implemented.

IV.2.1.3 Comparator with ATC

The clocked comparator, shown in Fig. IV.3, applies regenerative feedback clocked by the 50kHz oscillator. Two separate current biases are each controlled by 4-bit binary-weighted current DACs. In addition, the comparator threshold can be programmed to a 4-bit binary-weighted value to tune the sensitivity of the receiver. The threshold of the comparator is controlled in a feedback look by the ATC which dynamically changes the comparator's offset voltage to overcome interference signals. A diagram showing operation of the ATC can be seen in Fig. IV.4. As RF input signal comes in, the RF rectifier outputs the signal for the comparator. The comparator compares this signal with its threshold. The ATC monitors the samples coming

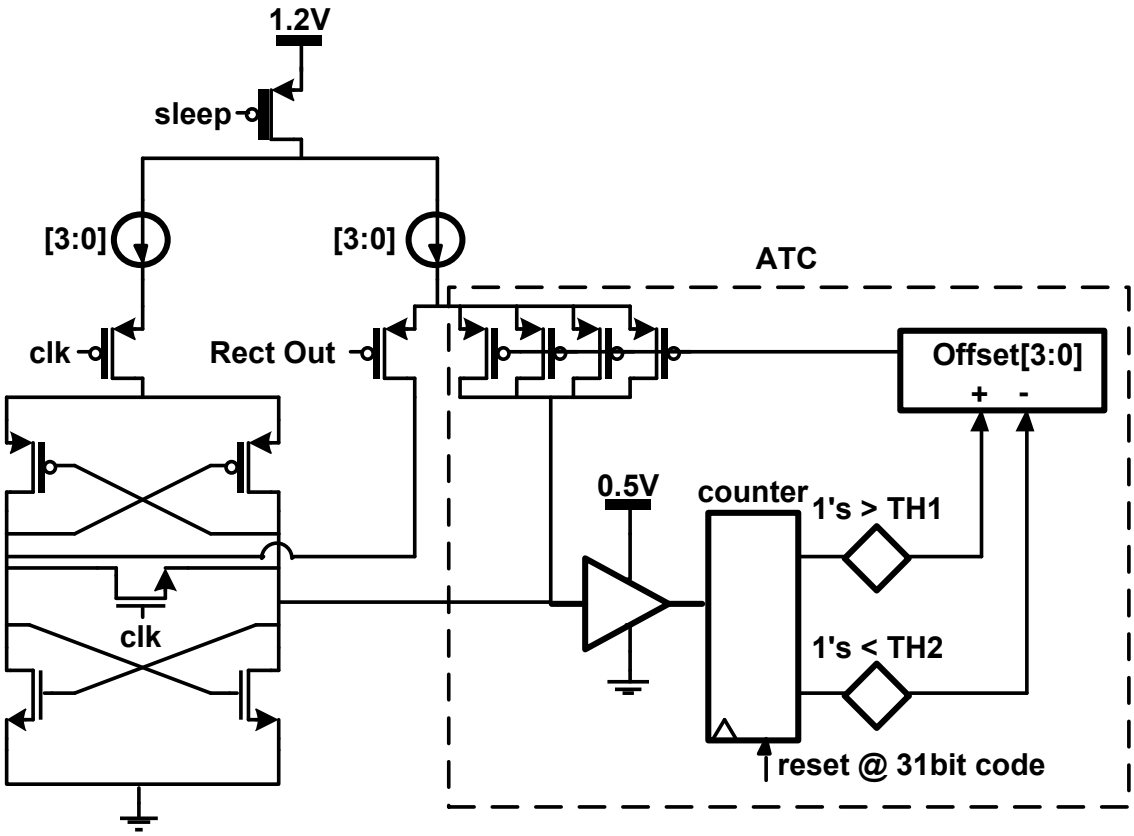

Fig. IV.3. Dynamic comparator with ATC

from the comparator output for one 31-bit code period. If the number of 1's is greater than a user defined value1 (indicating the comparator threshold is continuously exceeded by an interferer), then the ATC will increase the comparator threshold to bring the sensitivity of the receiver above that of the interfering signal. When the number of 0's at the output of the comparator reaches a separate, user defined value2 (indicating the interferer is gone and the comparator threshold is never exceeded), the ATC then reduces the threshold to increase the sensitivity of the receiver. Hysteresis is added between these values to eliminate limit-cycles. With this mechanism, the comparator can reject interference signals, and even if the interference signal is modulated by

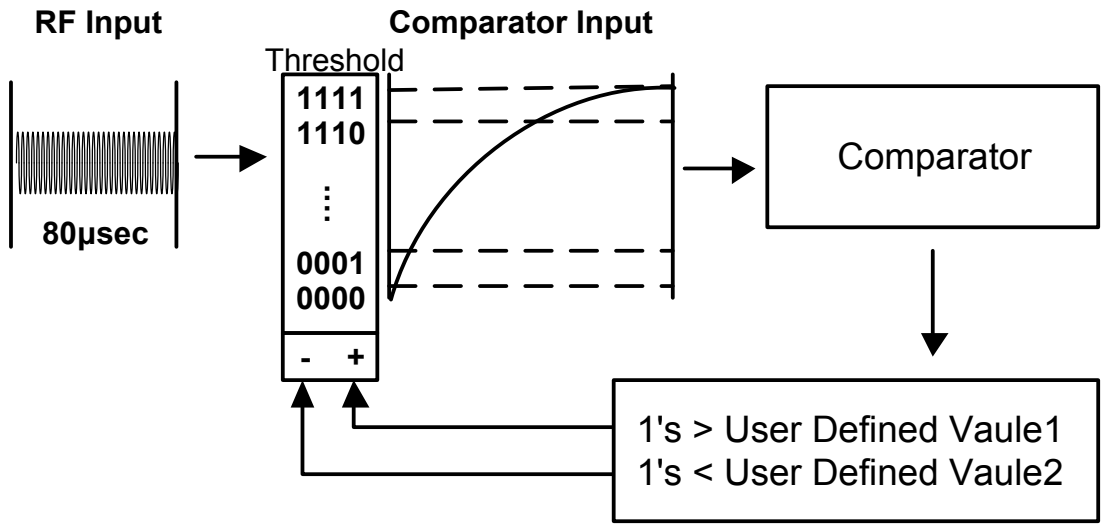

Fig. IV.4. Signal diagram of ATC

BPSK, or OOK, the comparator threshold is set to above the maximum level of interference so the comparator will produce the correct output.

IV.2.1.4 Correlators

A bank of four correlators continuously correlates the 4x-oversampled comparator bit-stream with a programmable, 31-bit CDMA code. This synchronizes to the transmitted code and only issues a wake-up output when the desired code is received. The digital baseband processor was synthesized in subthreshold in order to save power. Eight different Gold codes can be selected using control bits in a scan chain. This will allow for a single transmitter to uniquely wake up 8 possible WRXs. Gold codes are a set of binary sequences whose cross-correlation among the set is bounded into three values [87]. Gold codes are commonly used when implementing CDMA and they are easily implemented with 2 LFSRs (Linear Feedback Shift Register) and an XOR gate. In this work, 31-bit Gold codes with 3 configuration bits are implemented.

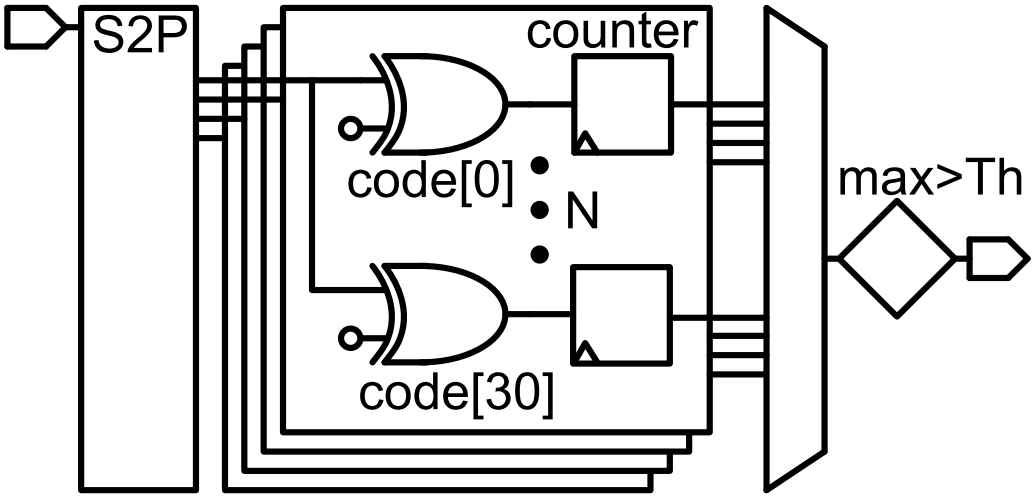

Fig. IV.5. Block diagram of correlators

The correlator compares the last two samples in each bit slice. Therefore, each 31-bit code results in a total of 62 comparisons. A programmable correlator threshold allows the user to define a value between 1 and 61 that must be exceeded in order to declare a code received indicating a valid wake-up event. A lower threshold value would mean fewer bits have to match the code, tolerating a higher BER and resulting in better sensitivity, but leads to more false wake-ups. A higher threshold would prevent false wake-ups, but also reduce the sensitivity of the receiver.

Fig. IV.5 shows a basic block diagram of the correlator. To synchronize the receiver to the transmitted code, 4 correlators operate at the same time and each correlator receives shifted samples of each bit slice since the receiver is 4x-oversampled. In each correlator, all possbile shifts of the 31bit Gold code are simultaneously correlated with the incoming bit stream, so that after a single 31bit sequence, the receiver is guaranteed to synchronize to the wake-up signal. Each parallel correlator will have a different number of correct comparisons based on the code shifts and phase difference between the WRX and the transmitter. If any of the 4 correlators

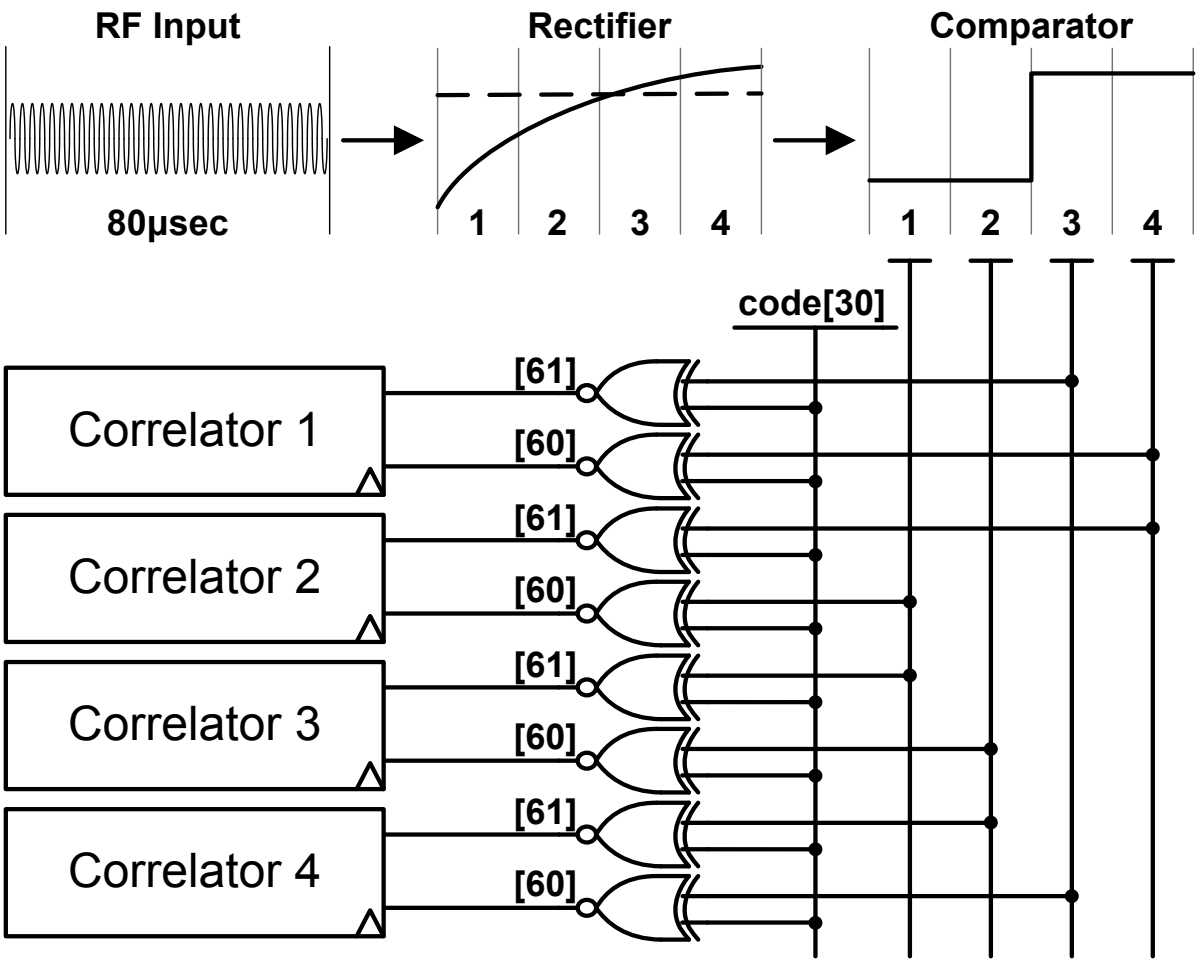

Fig. IV.6. Correlator signaling

results are greater than the correlator threshold, the wake-up signal will be asserted. An example showing how the correlator handles a single chip slice is shown in Fig. IV.6. This example shows what happens if the WRX receives a '1' as the last chip in the sequence. The OOK signal is gradually rectified during the chip window. The comparator, being 4X sampled by the crystal oscillator, captures 4 instances of each chip, with the last two being correct because those samples are taken after the RF rectifier has had the most time to rectify the signal. In this example, Correlator 1 receives the correct code. Since the comparator sampling is not

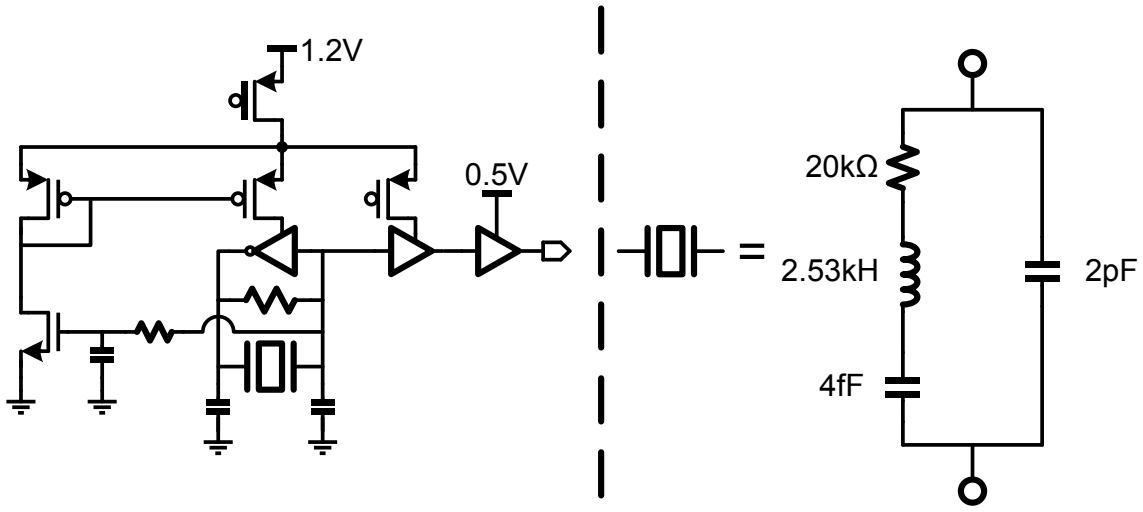

Fig. IV.7. Block diagram of 50kHz crystal oscillator

synchronized with the transmitter, the 4 different correlators span any possible shift between the two.

IV.2.1.5 Crystal oscillator

A 50kHz crystal oscillator serves as the reference clock of the radio [97]. As seen in Fig. IV. 7, an off-chip crystal is used, and the oscillator's primary amplifier is an inverter with resistive feedback. Fig. IV.7 also shows the intrinsic values of the 50kHz crystal. Using these values the critical g_m can be calculated using Equation (54), which is the transconductance of the amplifier that must be produced to achieve sustained oscillations. C and C_0 represent the motional and shunt capacitance of the crystal, ω and Q are the resonant frequency and Q factor of the crystal, and C_1 and C_2 are the load capacitance in the circuit. If the primary amplifier is biased in the near threshold region where the g_m/i_D ratio is around 10, then the current consumption to reach this critical g_m value is around 20nA.

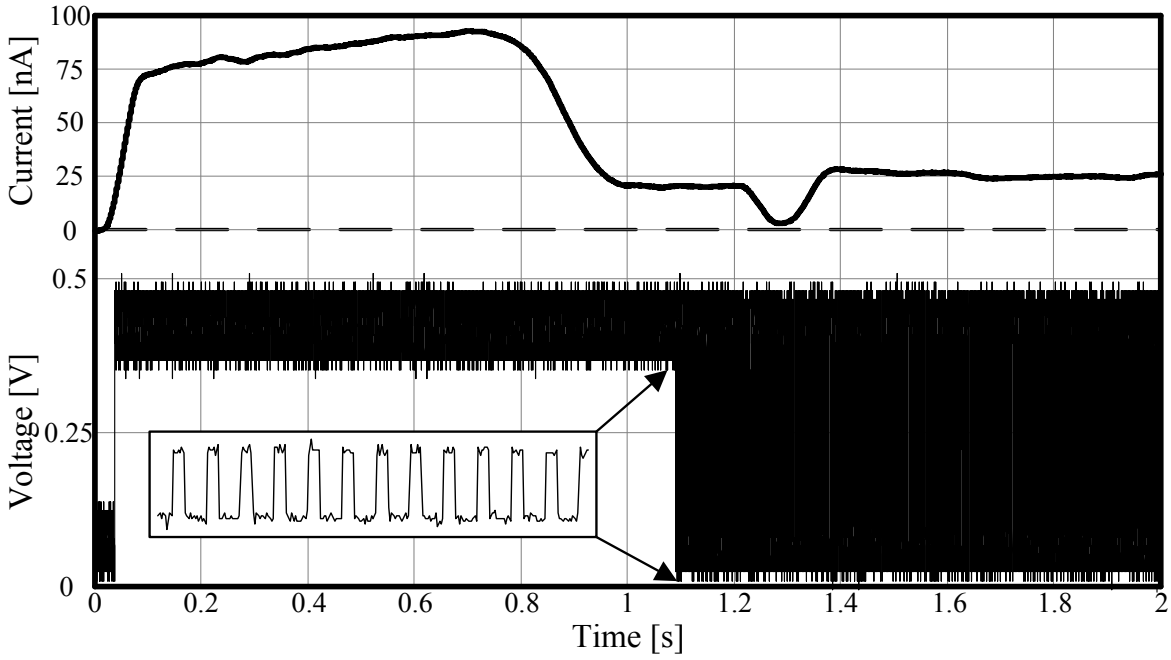

Fig. IV.8. Transient start-up time of crystal oscillator

$$Critical\ g_m = \frac{\omega}{QC} * \frac{(C_1C_2 + C_2C_0 + C_0C_1)^2}{C_1C_2} \tag{54}$$

Initially, the transconductance of the primary amplifier is much greater than the critical g_m of the crystal, which is needed to quickly increase the oscillation amplitude. However, as the oscillation amplitude increases, the DC level of the oscillation also drops and this common-mode signal is used in feedback to starve the primary amplifier until it settles with sustained oscillations. Measured results show the total power consumption is 30nW when sustaining oscillations using a 1.2V supply. The oscillation is then buffered to provide the reference clock for the WRX. Measured results show the oscillator has an RMS jitter of 6ns.

Fig. IV.8 shows the transient of the start-up time for the oscillator. The top of the figure shows the current consumption during start-up and shows that the current consumption peaks

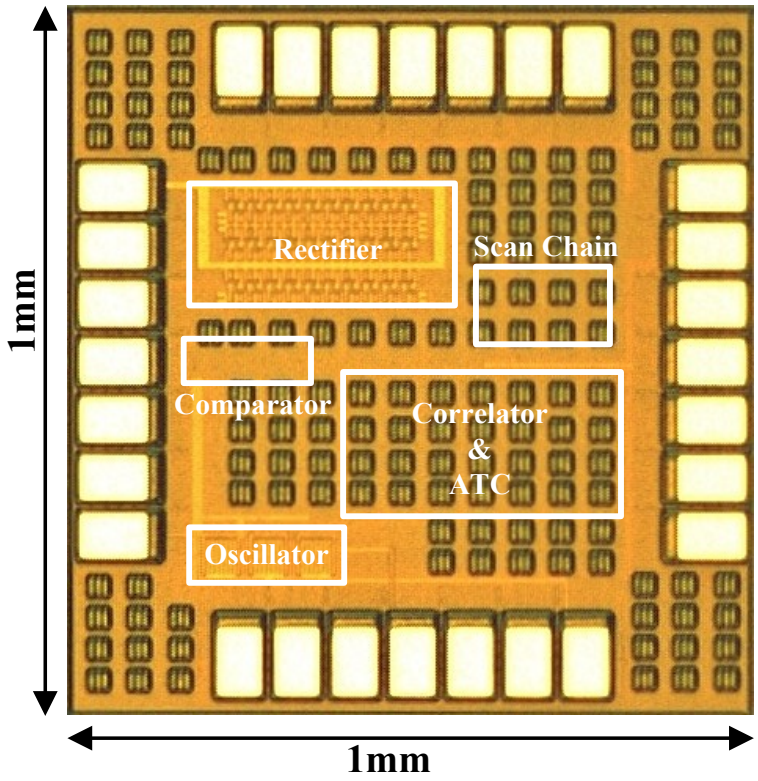

Fig. IV.9. Die micrograph

around 95nA before dropping as oscillations begin to increase. The current consumption finally settles to 25nA after a second has passed. While this start-up time is relatively long, the WRX can be left on continuously in a typical sensor node due to its ultra-low power consumption.

IV.2.1.6 Sleep power

Sleep power in the WRX was carefully considered during the design process to support a duty cycled wake-up strategy. To improve sleep mode energy, thick oxide power gating devices were used throughout the design. Wake up time is dominated by the slow start-up time of the crystal oscillator, which takes about 1.1 seconds to oscillate. Putting the WRX into a full sleep mode, where every circuit is power-gated, results in a sleep power of 18pW. Clock gating the

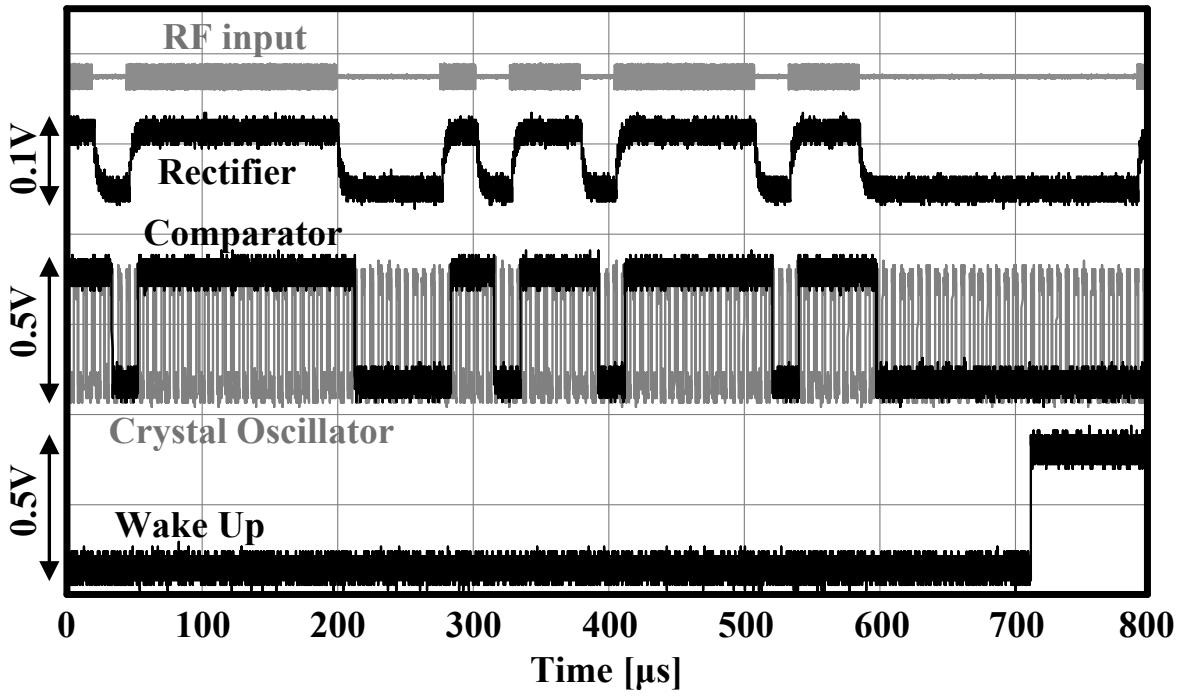

Fig. IV.10. Transient response of WRF

crystal oscillator, and putting all the circuits except the crystal oscillator into sleep mode, results in a sleep power of 30nW.

IV.3 Measurement Results

The WRX was fabricated in IBM's 130nm CMOS process and has an active area of 0.35mm^2 without pads. It uses 2 separate voltage supplies; a 1.2V supply for the crystal oscillator and demodulating comparator and a 0.5V supply for all baseband processing. A die micrograph can be seen in Fig. IV.9.

Transient operation of the WRX receiving a 31-bit code is shown in Fig. IV.10. Because of the bit-shifted parallel correlators, the WRX is able to automatically synchronize to the incoming bit stream upon receiving the first wake-up code. The top two traces show the RF input signal

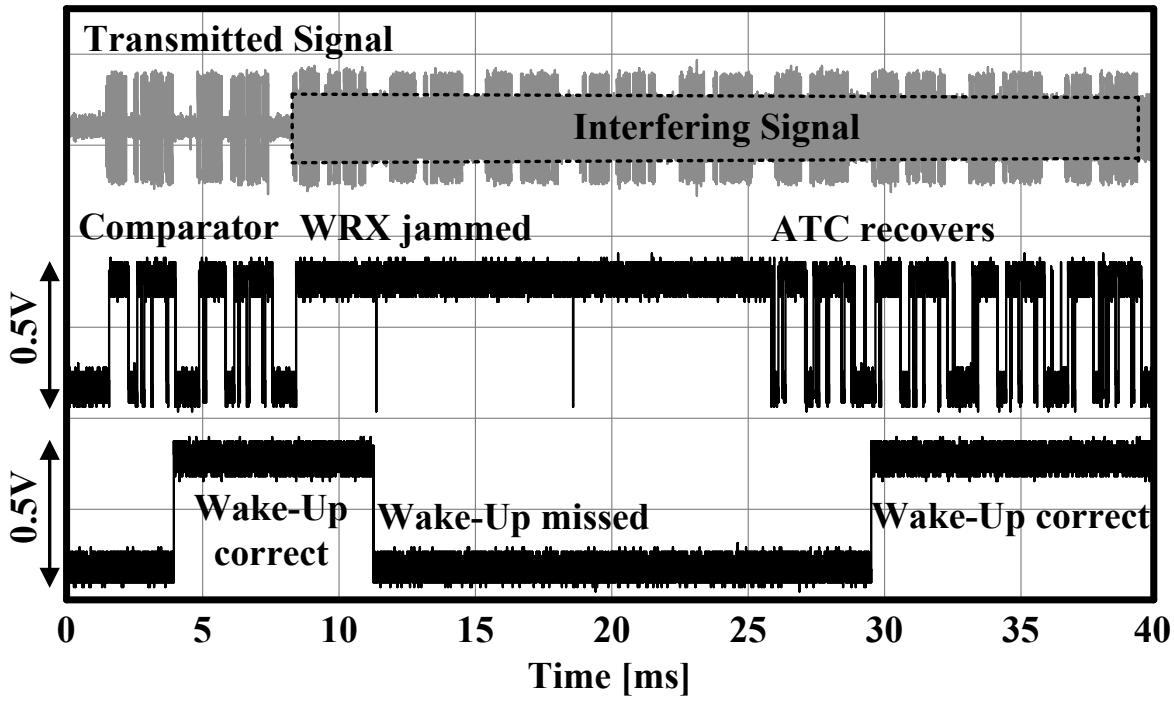

Fig. IV.11. Transient response in presence of interferer

and the RF rectifier converting the signal to baseband. The third trace shows the output of the comparator being clocked at 4X the data-rate by the oscillator and the final trace is the wake-up signal being toggled by the correlator. The WRX is capable of CDMA by selecting different codes used by the correlator block. If an interfering signal is strong enough to exceed the comparator threshold, then the ATC increases the comparator's threshold until it is above the interfering signal. A transient of this operation can be seen in Fig. IV.11. The top signal is the received RF signal, which is jammed by a 2.4GHz tone at 8ms. With the interferer present, the receiver cannot initially demodulate the code. After 15ms, the ATC has raised the threshold of the comparator above that of the interferer, and the WRX regains synchronization.

The WRX has an active power of 116nW with a sleep power of 18pW. It has a raw OOK chip-rate of 12.5kbps and a symbol rate of 50kbps and sensitivities of -45.5dBm, -43.4dBm, and

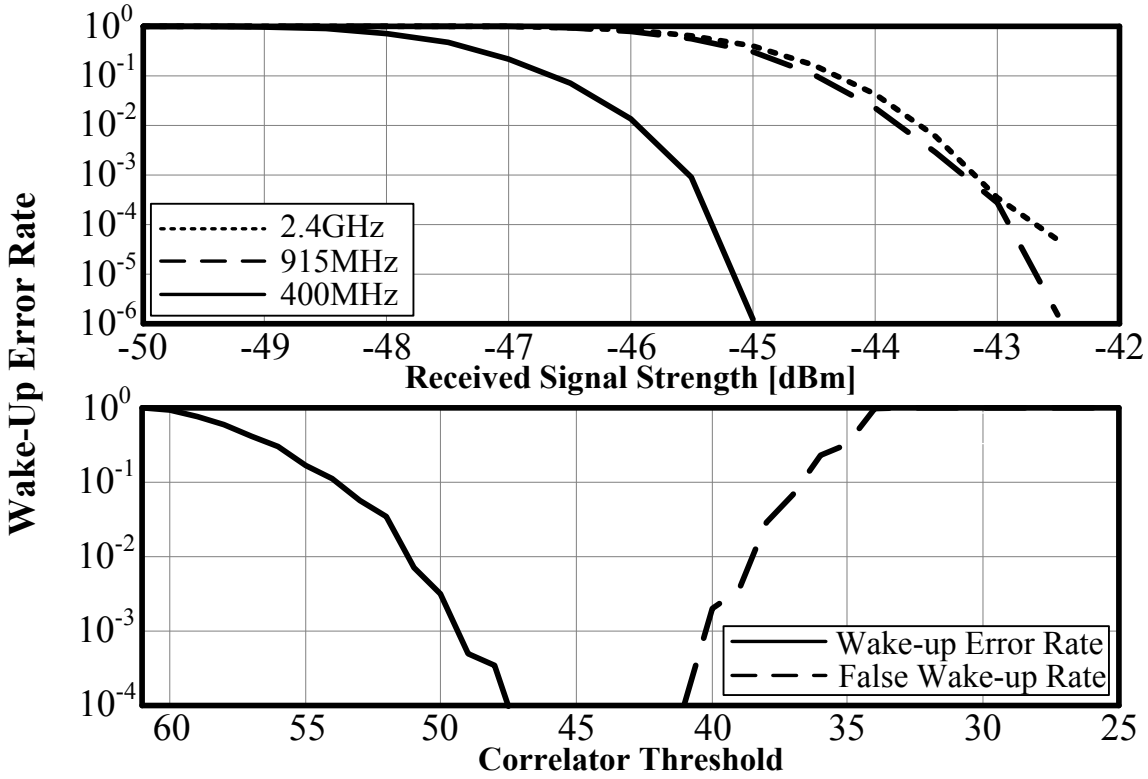

Fig. IV.12. BER vs. received signal strength and correlator threshold

-43.2dBm at 403MHz, 915MHz, and 2.4GHz, respectively. The top of Fig. IV.12 shows the chip error rate (BER) curves for the 403MHz, 915MHz, and 2.4GHz bands. The bottom of Fig. IV.12 shows the BER as the correlator threshold is varied. The measurements were taken using a -40dBm received signal in the 2.4GHz band. The figure also shows the impact this threshold has on false wake-ups. From these two data sets, the correlator threshold can be set to maximize sensitivity while minimizing the possibility of a false wake-up.

To demonstrate the ability of the WRX to be selective in its wake-up code, therefore allowing different codes to wake up different WRXs, Fig. IV.13 shows an experimental setup where the input signal was connected to two different WRXs, each with a different wake-up code programmed. The top of Fig. IV.13 shows that code 1 and code 2 were transmitted back to back

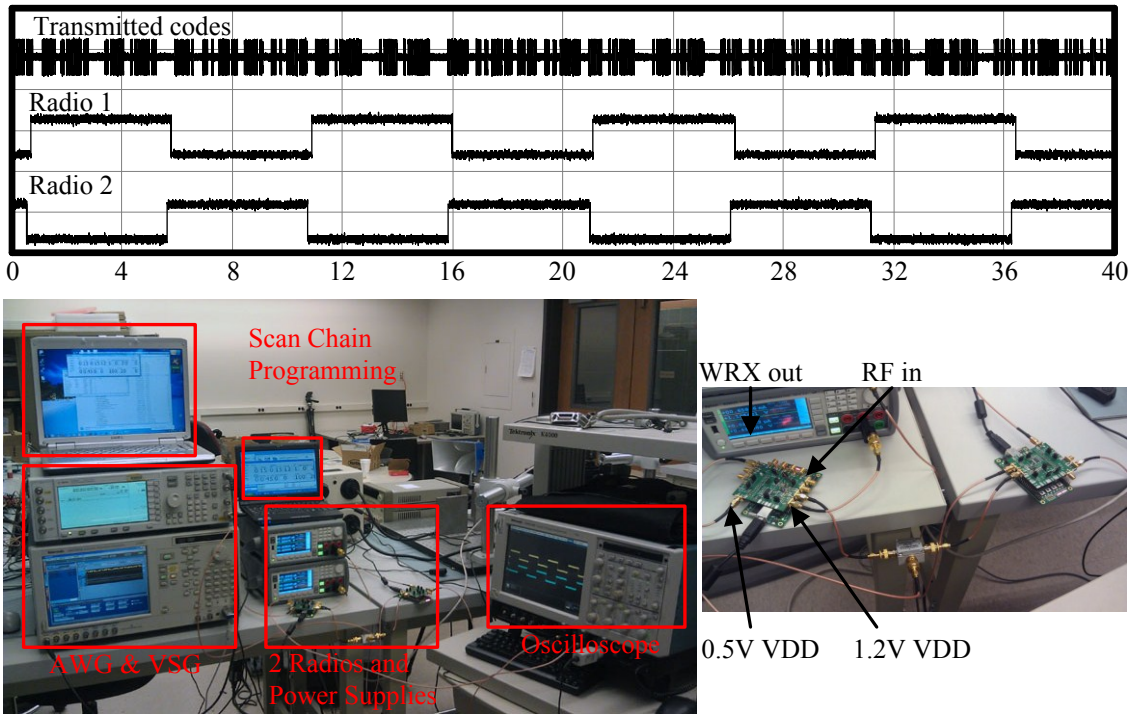

Fig. IV.13. WRXs measurement setup and result

and the resulting output from the WRXs correctly toggles when the proper code is sent, but ignores the incorrect code.

Table VII shows a power breakdown on the WRX on the left. Digital logic consisting of the 4 parallel correlators and a clock divider all synthesized in subthreshold consumes the bulk of the 116nW power. Second is the crystal oscillator consuming 38.4nW. The demodulating comparator consumes 8.4nW and the RF rectifier front end consumes no power, for a total of 116.3nW.

Table VII. Power breakdown and receiver specs

Power Breakdown [nW]		Receiver Specs	
RF Rectifier	0	Energy/bit	9.28pJ
Comparator	8.4	Energy/wakeup	287.7pJ
Digital Logic	69.5	Max signal level	-15dBm
Crystal Oscillator	38.4	Max interferer level	-20dBm
TOTAL	116.3	Code length	31
Sleep [pW]	20	# of pre-defined codes	8

Table VIII. Comparison with other state of the art work

	This Work			**[42]**	**[61]**	**[95]**
Power [µW]	0.116			52	45	0.098
Sleep [pW]	20			N/A	N/A	11
Frequency [MHz]	403	915	2400	2000	5800	915
Data-rate [kbps]	12.5/31			100	14	100
Sensitivity [dBm]	-45	-43	-41	-72	-45	-41
SIR [dB]	3.3	1.7	1.7	N/A	N/A	N/A
Die Area [mm^2]	0.35			0.1	N/A	0.03
VDD [V]	1.2|0.5			0.5	3.0 ~ 3.6	1.2
Process [nm]	130			90	130	130

The right side of Table VII shows the receiver's specs. It requires 9.28pJ/bit and with a 31-bit wake up code, the total energy to wake up the node would be 287.7pJ. The maximum signal level tolerable is -15dBm and the maximum interferer level is -20dBm. Table VIII shows a comparison versus the state of the art WRXs previously mentioned. It is apparent the design tradeoffs that are made to both reduce power and interference. In [42] the sensitivity is nearly 30dB better than this work, but the power is nearly 30dB greater. [61] blocks out-of-band interferers, but not in-band interferers and also has higher power. [95] uses the same sensitivity reduction technique to lower power, but does not have any way to compensate interferers.

Chapter V.
Conclusion

V.1 Summary

WBANs have enormous potential in health monitoring systems as it eliminates the inconvenience of having wires around the patient's body. Low power consumption is crucial for such applications due to the limited capacity of portable batteries. The power consumption of wireless communication is especially important since it typically consumes the majority of the energy in such systems. The goal of this research is to design a single chip solution for a low power reactive transceiver in WBAN.

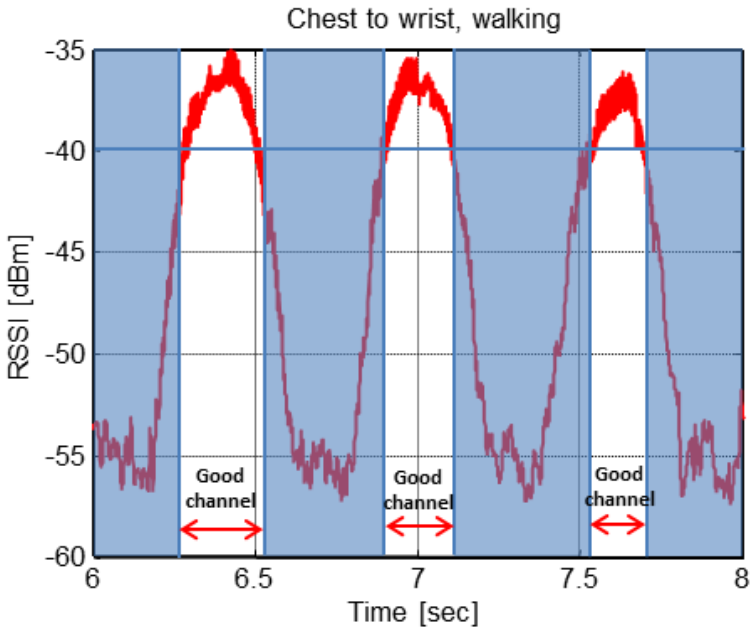

Fig. V.1. RF communication channel in WBAN

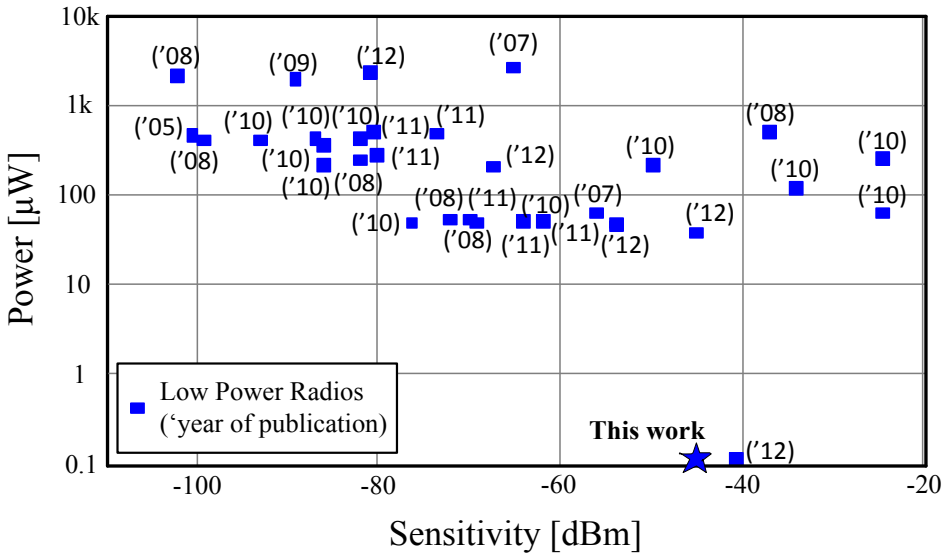

Fig. V.2. survey of low power radio

Fig. V.1 shows the RF communication channel in a WBAN measured with our custom hardware at 900MHz with 0dBm transmit power. As it can be seen in this figure, the received signal strength of the receiver is higher than -40dBm during 30% of period. Therefore, in applications that can tolerate intermittent communication, such as a human body physiological monitoring, a receiver with -40dBm sensitivity can communicate with very low power consumption.

Fig. V.2 shows a survey of low power radios from 2006-2012 [40]-[63]. In this thesis, a wake-up receiver with -45dBm sensitivity and 116nW power consumption was presented, which lies well under the reported prior work and is suitable for communication in the measured WBAN channels. A power harvester was also presented targeting maximum sensitivity rather than maximum efficiency, and achieving a similar sensitivity range.

V.2 Future work

The future work is to design a single chip solution for a low power reactive transceiver in WBAN. This chip has 2 receivers, a 100nW wake-up receiver and a 100µW communication receiver with high channel selectivity and 1 UWB transmitter as shown in Fig. V.3.

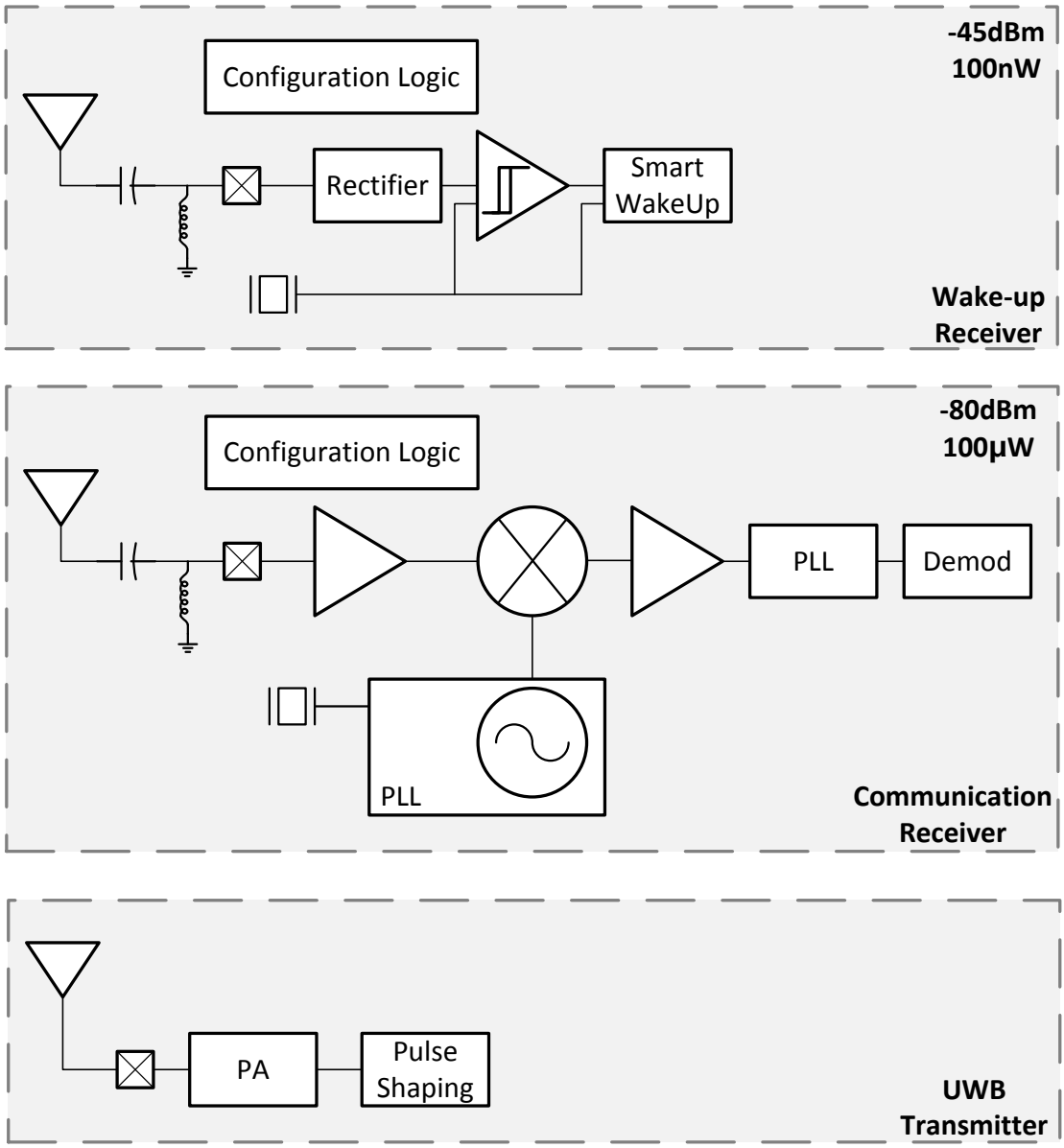

Fig. V.3. System architecture of a single chip solution

The wake-up receiver is always on and checks the received data, waiting for a 15bit unique wake-up code. Since it is on all the time, the power consumption of the wake-up radio should be as low as possible. When the unique wake-up code is received, the wake-up receiver wakes up the rest of the chip and the communication receiver starts to operate with higher sensitivity and higher channel selectivity. This duty cycle makes it possible to have ultra-low average power consumption for the whole chip.

Our target application has an aggregator with high power capacity and several sensor nodes with low power capacity. In order to reduce the power consumption in sensor nodes, an asymmetric communication link, comprised of a UWB uplink and narrow band down link will be implemented for low power radio, since energy per bit of a UWB transmitter (0.18nJ/bit [74] and 12pJ/bit [75]) are usually much less than energy per bit of a narrow band transmitter (3nJ/bit [90] and 60nJ/bit [91]). On the other hand, since energy per bit of a UWB receiver (2.5nJ/bit [92] and 0.5nJ/bit [93]) are usually greater than energy per bit of a narrow band receiver (510pJ/bit [41] and 830pJ/bit [40]), the UWB transmitter and the narrow band receiver are chosen for the sensor node. The target power consumption of the wake-up receiver, communication receiver and transmitter are 100nW, 100μW and 20μW, respectively, and the target sensitivity of the wake-up receiver and communication receiver is -45dBm and -80dBm, respectively.

Nathan E. Roberts and I worked together on this reactive transceiver. I focused on the wake-up receiver and UWB transmitter, and Nathan mainly works on the communication receiver. This chip was taped-out in November 2012 and will be back January 31th 2013.

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