FULLY INTEGRATED HIGH-PERFORMANCE MEMS LUMPED ELEMENT FILTERS FOR RECONFIGURABLE RADIOS

by

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To my parents

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LIST OF ABBREVIATIONS

ACP	Air coplanar probe
ADC	Analog-to-digital converter
ADS	Advanced design system
Ag	Silver
ALD	Atomic layer deposition
AlN	Aluminum nitride
Al_2O_3	Aluminum oxide
$BaTiO_3$	Barium titanate
BST	Barium strontium titanate
BW	Bandwidth
BW_{3dB}	3dB-bandwidth
BW_{30dB}	30dB-bandwidth
C	Capacitance
CDMA	Code division multiple access
CMOS	Complementary metal-oxide-semiconductor
CPD	Critical point dryer
Cr	Chromium
Cu	Copper
DC	Direct current
DSP	Digital signal processor
DRIE	Deep reactive-ion etching
EM	Electromagnetic

f_c	Center frequency
f_m	Mechanical resonant frequency
GeTe	Germanium tellurium
GPS	Global positioning system
GSG	Ground-signal-ground
GSM	Global system for mobile communications
GST	Germanium antimony tellurium
HFSS	High frequency structural simulator
HR-Si	High-resistivity silicon
IF	Intermediate frequency
IIP_3	Third-order input intercept point
ISM	Industrial, scientific, and medical
KOH	Potassium hydroxide
L	Inductance
LCP	Liquid crystal polymer
LNA	Low-noise amplifier
LPCVD	Low-pressure chemical vapor deposition
LTE	Long-term evolution
MEMS	Microelectromechanical systems
MIM	Metal-insulator-metal
NiCr	Nichrome
P_{1dB}	1dB compression point
PC	Phase change
PCB	Printed circuit board
PCM	Phase change material
PECVD	Plasma-enhanced chemical vapor deposition

PMMA	Polymethylmethacrylate
PNA	Programmable network analyzer
PRAM	Phase-change random-access memory
PSC	Parasitic surface charge
Pt	Platinum
PZT	Lead zirconate titanate
Q	Quality factor
RF	Radio frequency
RTA	Rapid thermal anneal
SAW	Surface acoustic wave
SDR	Software defined radio
SEM	Scanning electron microscope
SH	Sample and hold
SHF	Super high frequency
Si	Silicon
SiO_2	Silicon dioxide
SOLT	Short-open-load-through
SOI	Silicon-on-insulator
SRF	Self-resonant frequency
TCB	Tunable capacitor bank
TaN	Tantalum Nitride
Ti	Titanium
TiN	Titanium Nitride
UHF	Ultra high frequency
VHF	Very high frequency
W	Tungsten

WRAN	Wireless regional area network
XeF_2	Xenon difluoride
XRD	X-ray diffraction

ABSTRACT

FULLY INTEGRATED HIGH-PERFORMANCE MEMS LUMPED ELEMENT FILTERS FOR RECONFIGURABLE RADIOS

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In this research, we present RF MEMS filters which address the most challenging performance requirements of modern RF front-end systems, namely multi-band processing capability, low energy consumption, and small size. These filters not only provide a wide tuning range for multiple-band selection, but also offer low loss, high power handling capability, fast tuning speed, and temperature stability. Two different technologies are considered for tunable lumped element filter targeting UHF range. The first technology is a tunable RF MEMS platform based on surface micromachining, enabling fabrication of continuously tuned capacitors, capacitive and ohmic switches, as well as high-Q inductors, all on a single chip. The filter is in a third-order coupled resonator configuration. Continuous electrostatic tuning is achieved using three tunable capacitor banks each consisting of one continuously tunable capacitor and three switched capacitors with pull-in voltage of less than 40 V. The center frequency of the filter is tuned from 1 GHz to 600 MHz while maintaining a 3 dB-bandwidth of 13 to 14 % and

insertion loss of < 3.5 dB. The temperature stability of the center frequency from 223 K to 323 K is > 2 %. The filter occupies a small size (1.5 cm × 1.0 cm). This filter shows the best published performance yet in terms of insertion loss, out-of-band rejection, temperature stability, and tuning range.

The second technology is based on a new tuning mechanism utilizing phase-change (PC) materials. PC technology has been investigated and adopted in memory industry due to its fast transition time in nano second range, small size, and high resistance change ratio. Although PC materials offer several benefits, they have not been considered for RF applications because of their limited power handling capability and relatively higher on-resistance in their current form. In this work, germanium tellurium (GeTe) is considered as it offers a low on-resistivity and pronounced resistance change ratio of up to 10^6. To characterize RF properties of GeTe, different types of RF switches have been fabricated and compared. For improvement of reliability and power handling capability, new structural configurations are proposed and analyzed. Such PC switches can be monolithically integrated with other micromachined components to implement reconfigurable front-end modules, potentially offering high tuning speed, low loss, high linearity, and small size.

CHAPTER 1.

INTRODUCTION TO TUNABLE RF MEMS

1.1. Reconfigurable Radios

The largest commercial market in RF MEMS area is currently the wireless handset market, which includes smart phones and tablets, mobile phones, and portable computers. To provide high-end mobile services including video streaming and fast web browsing, frequency allocation and other regulations for wireless communications are constantly updated or amended for high-bit rate and energy-efficient data transmission. Future mobile handsets should support a number of wireless standards with different frequencies, such as WIFI [1], GSM [2], CDMA [3], LTE [4], BLUETOUTH [5], GPS [6], and any newly released standards (Table 1.1). Using existing technologies, a RF signal from each standard is processed separately by a dedicated RF front-end system. Therefore, a number of antennas, switches, phase arrays, and front-end filters are needed, increasing the overall size and cost of the system. This is well shown in Figure 1.1, which is the PCB layout of the iPhone 5 [7].

Recently, the National Broadband Plan [8] has been announced, calling for utilization of multiple channels within a wide range of frequencies (225 MHz – 3.7 GHz).

Table 1.1. Existing wireless standards in UHF and SHF range [1–6].

Standard	Classification	Allocated Frequencies	Channel Bandwidth	Spectrum Type
Wi-Fi	IEEE 802.11 (WLAN)	5.25, 5.6, 5.8 GHz	20 or 40 MHz	Unlicensed 802.11a and ISM band
Bluetooth	IEEE 802.15 (WPAN)	2.4 GHz	1 MHz	Unlicensed ISM band
WiMAX	IEEE 802.16 (WMAN)	2.3, 2.5, 3.5, 3.7, 5.8 GHz	20 MHz	Licensed
EV-DO, EV-DV	CDMA 2000	450, 850, 900 MHz, 1.7, 1.8, 1.9, 2.1 GHz	1.25 MHz	Licensed
UMTS W-CDMA	UMTS/3GSM	0.85, 1.7, 1.9, and 2.1 GHz	10 MHz	Licensed
UMTS TDD	UMTS/3GSM	450, 850 MHz, 1.9, 2, 2.5, 3.5 GHz	5 MHz	Licensed
GPRS, EDGE	GSM	850, 900 MHz, 1.8, 1.9 GHz	200 kHz	Licensed
LTE	3GPP	700, 750, 800, 850, 900 MHz, 1.7, 1.8, 1.9, 2.1 GHz	1.4, 3, 5, 10, 15, 20 MHz	Licensed
GPS	GPS	1.2276, 1.57542 GHz	10.23 MHz	Licensed

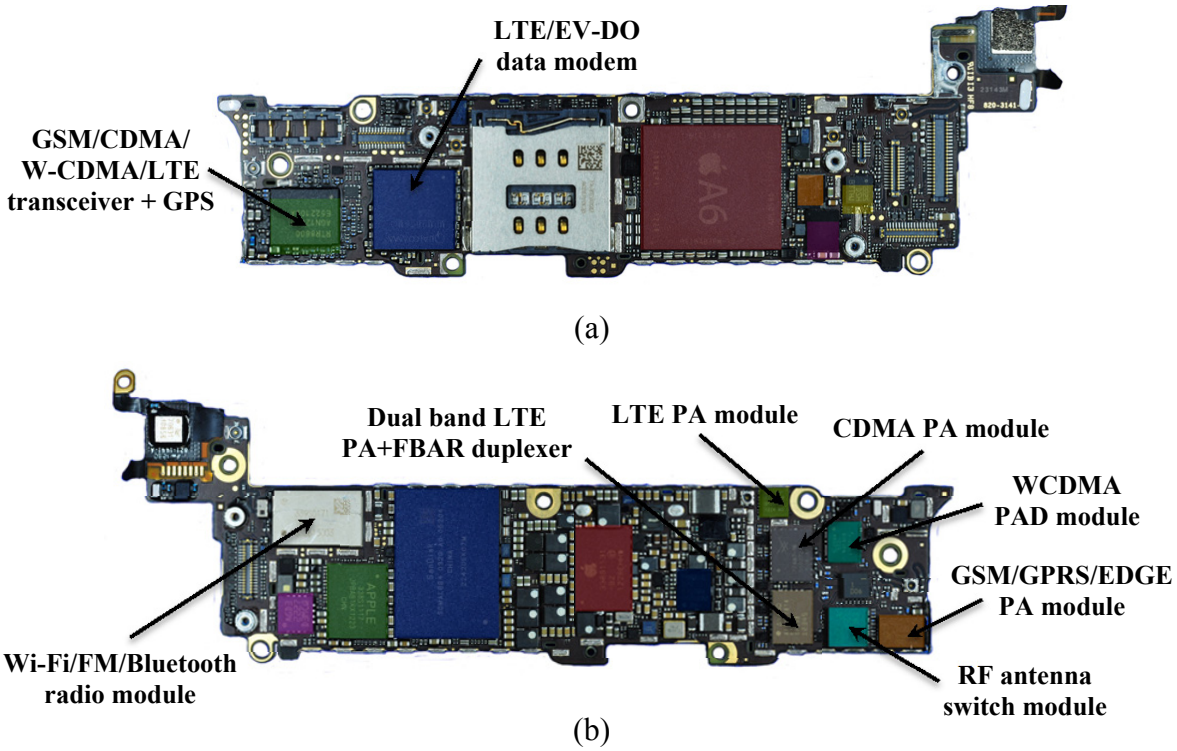


Figure 1.1. The PCB layout of the iPhone 5 [7]; (a) front side; (b) back side.

The purpose of this plan is to provide all Americans with access to the broadband wireless with high data rates exceeding one gigabit per second. To achieve this, a plan similar to the IEEE 802.22 standard [9], [10] for wireless regional area network (WRAN) could be utilized. The 802.22 standard uses cognitive radio techniques; any available channels in UHF/VHF TV bands between 54 and 862 MHz are processed with adaptable radios sensing the spectrum change. However, it is impossible to incorporate several tens of front-end filters for new wireless standards as the size and cost of the handset will increase significantly. This is where RF MEMS can play a unique role; tunable components implemented using the RF MEMS technology can decrease the number of necessary front-end components, reducing the overall handset size, cost, and energy consumption.

For multi-band transceiver implementation, a variety of architectures have been proposed. These architectures can be classified into several categories based on the type of the front-end filters and the topology of the transceivers. The most conventional approach uses multiple surface acoustic wave (SAW) filters and follows the superheterodyne, zero-IF, or low-IF transceiver [11], as shown in the RF transceiver architecture of a commercialized handset, LG GM730 (Figure 1.2 [12]). However, this approach is not applicable to flexible multi-band standards, such as IEEE 802.22, as the number of the required SAW filters will increase, enormously. To cope with this, SAW-less radios [13–15], or so called software defined radios (SDR), have been proposed.

SDR is based on wide-band signal processing in the digital domain after direct-conversion into the baseband (Figure 1.3) [13]. However, SDR requires high-bit rate analog-to-digital converters (ADC), and as such is power hungry and requires high-end, costly digital signal processors (DSP) as well as ADCs. It also suffers from blocking or saturation issues from strong interfering signals or jammers.

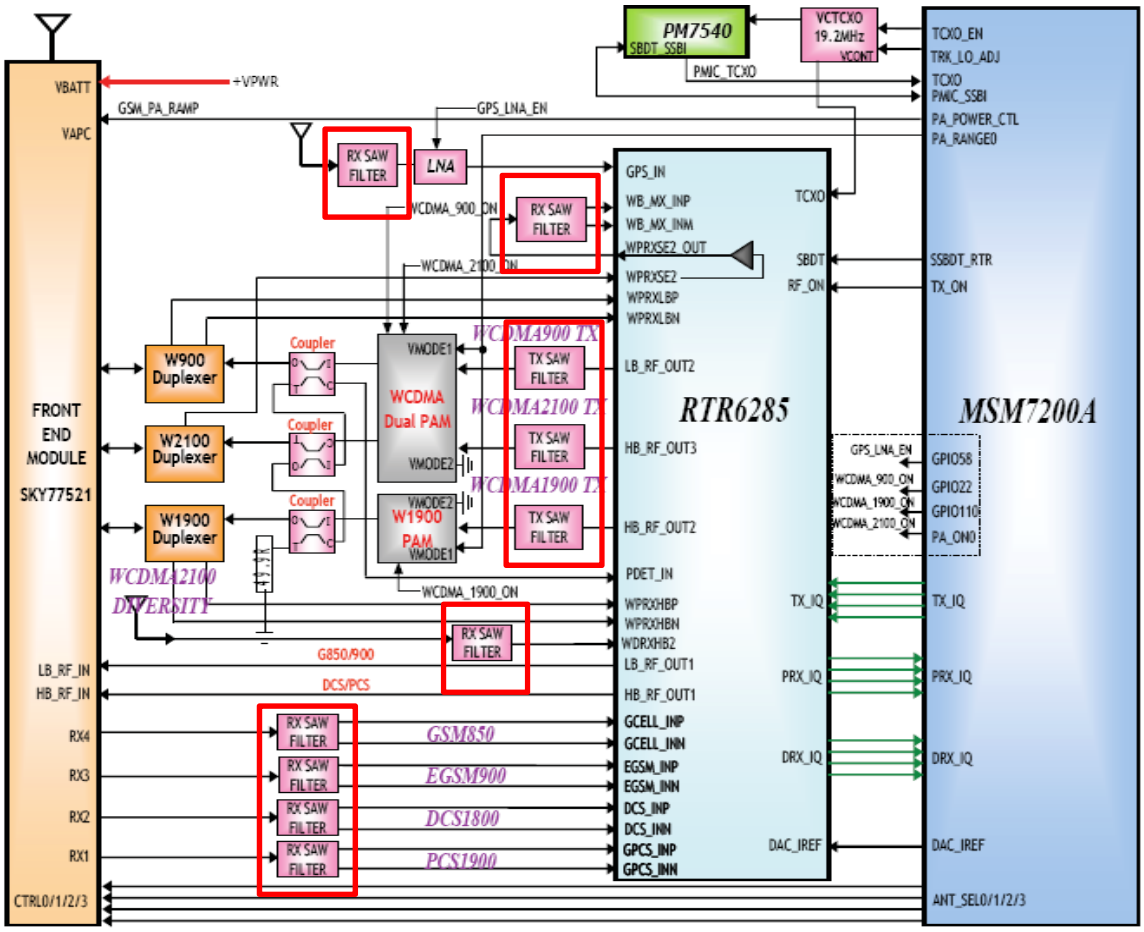


Figure 1.2. The transceiver architecture of LG GM730 [12].

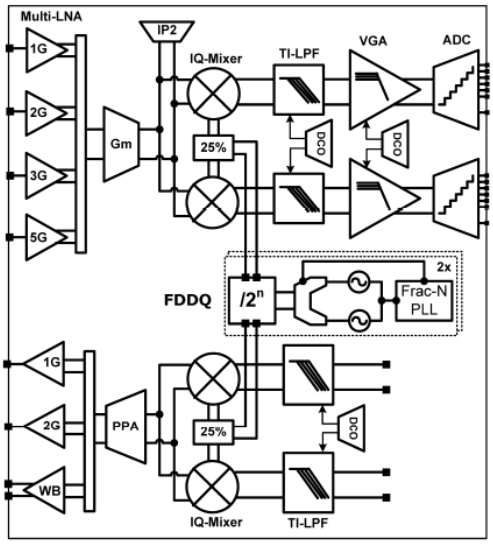
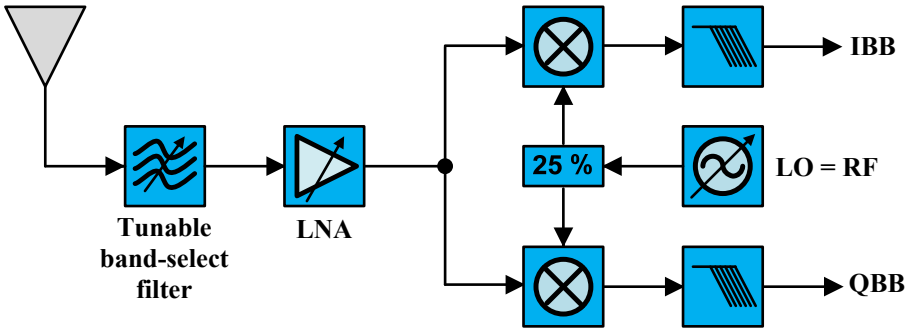


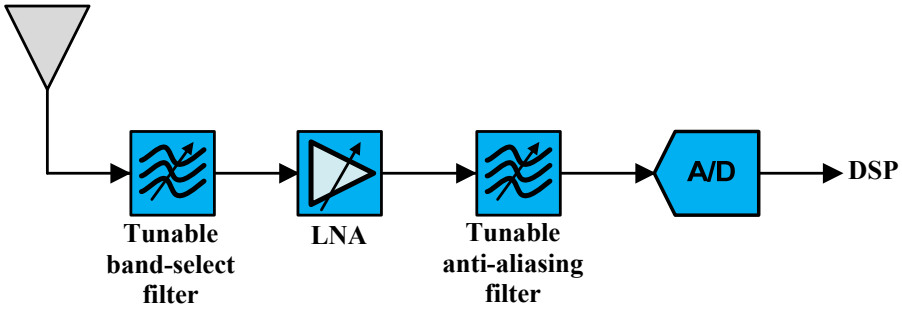
Figure 1.3. Transceiver block diagram of the multi-standard software defined radio [13].

Since SAW filters are hardly tunable and the tuning range is very limited if at all possible, a more practical approach to address the lack of reconfigurability is to integrate tunable passive filters in the transceiver front-end (Figure 1.4 (a)). Using this approach, strong interferences or blocking signals located near the target signal can be removed, to prevent the saturation of following RF circuits, such as the low noise amplifier (LNA) or mixer. This also reduces the stringent dynamic range requirement of the ADC. However, it is still challenging to generate a variety of local oscillators with different frequencies. Another candidate is the RF bandpass filtering transceiver shown in Figure 1.4 (b). In this technique, RF sampling replaces the down-conversion stage and multiple channels can be processed simultaneously. Depending on the bandwidth of the preselect filter, the ADC sampling rate can be from several tens to hundreds of MHz. Even though the required sampling rate is reduced compared to the original SDR architecture, this rate

is still challenging to accomplish since the analog bandwidth of the sample-and-hold (SH) should be more than the highest input RF frequency. Therefore, the power consumption of the SH stage becomes significant. Nevertheless, the later approach using tunable frontend filters is the most power-efficient approach and offers the highest versatility in terms of radio reconfigurability.



(a)



(b)

Figure 1.4. Candidate cognitive radio architectures with tunable preselect filters; (a) direct conversion architecture; (b) RF bandpass sampling architecture; reprinted from [16].

1.2. Tunable Passives

In reconfigurable RF front-end filters, tunable passives are key components which not only determine the tuning characteristics such as tuning range and tuning speed, but

also have dominant effects on the electrical properties such as insertion loss, bandwidth, and the operation frequency. Tunable passive modules use either or a combination of capacitive switches [17–23], continuously tuned capacitors (varactors) [24–32], metal ohmic switches [33–38], and tunable inductors [39–44]. Depending on the target application and the required tuning specifications, a number of tuning mechanisms such as electrostatic [1], [3], [7], electromagnetic [39], [45], electrothermal [28], [46], piezoelectric [35], [37], [47], [48], or ferroelectric tuning [21], [49], [50] can be utilized (Table 1.1). Among these, electrostatic transduction method is the most common technique used for tuning because of its simplicity and low power consumption. However, one practical limit using electrostatic tuning is the dielectric charging effect [51], [52], which results in inconsistent tuning characteristics and reduced reliability of the tunable device. To overcome this effect, a dielectric less structure was proposed [22], [53]. Applying bipolar control-voltage waveforms [54] can be another possible approach, but using this, a more complicated control would be necessary to minimize the charging effect.

Table 1.2. Comparison of different tuning mechanisms used to reconfigure RF passives.

Tuning Mechanism	**Voltage (V)**	**Current (mA)**	**Power (mW)**	**Size**	**Tuning Speed (μs)**	**Contact Force (μN)**
Electrostatic	20-100	0	0	Small	1-200	50-1000
Electromagnetic	3-5	10-100	0-100	Medium	300-1000	50-200
Electrothermal	3-5	10-200	0-200	Large	300-10000	500-4000
Piezoelectric	3-20	0	0	Medium	50-500	50-200
Ferroelectric	0-40	0	0	Small	< 1	-

Electromagnetic or electrothermal mechanism is adopted when strong actuation or restoring force is needed. For sufficient actuation force, springs or actuation electrodes become very large. Electrothermal mechanism also suffers from low tuning speed, exceeding 1 ms. Compared to electrostatic tuning that ideally consumes zero power for tuning control, these mechanisms consume significantly higher power. To reduce the power consumption, it is more desirable to implement bistable switches [55–57], which only consume power during transition periods. Bistable switches are, however, large in size and require complicated fabrication processes.

Piezoelectric actuation is another popular technique as it provides a bi-directional force, unlike electrostatic actuation which is always attractive. In addition, the actuation voltages for piezoelectric tuning are in general smaller than voltages required for electrostatic tuning. The problem with piezoelectric actuation is that common piezoelectric materials (e.g., PZT and BaTiO3) are not compatible with CMOS fabrication technologies. Therefore, only backend integration with CMOS chip is permitted with these materials. Aluminum nitride (AlN) [48], [58] has received increased attention as a CMOS-compatible piezoelectric material, as it can be sputtered and self-polarized at low temperatures. Relatively smaller piezoelectric constant, however, limits its applicability to RF MEMS tunable devices. Using a low piezoelectric constant material, longer actuation beams or larger actuation voltages are needed to implement switches with sufficient isolation at off state.

Ferroelectric tuning is normally achieved utilizing Barium-Strontium-Titanate (BST). Since this mechanism is solely an electric conversion, it has less mechanical reliability issues and faster tuning speed in ns range. However, as crystallization of BST requires very high annealing temperatures and it can only be deposited on certain substrates, such as single crystalline sapphire, complete integration with the CMOS process is not possible using this material.

1.3. State-of-the-Art Tunable Bandpass Filters for Lower UHF Range

As the frequency increases, the wavelength becomes smaller and the physical size and values of passives are reduced. At frequencies higher than 1 GHz, several reconfigurable passive filters have been demonstrated using microstrip lines [59–61], or cavity based structures [62–66]. At such high frequencies, because of relatively smaller passive component values, implementation with a single fabrication technology is easier. The entire size of a filter is also in a reasonable range, allowing low-cost and on-chip integration with silicon circuitry, even using distributed filter structures. On the other hand, tunable passive filters at the lower UHF band (< 1 GHz) have been implemented mostly using off-chip components as larger-value passive components are needed at low frequencies. Integration of passives at low UHF frequencies is very challenging; in this range the ohmic loss is dominant and the quality factor (*Q)* of the integrated passives is very low (*e.g.* inductor *Q* is less than 30). The low UHF band is receiving more attention

as new IEEE standards [10] are announced recently in this range and several bands will soon become available following the broadband plan announcement, discussed earlier [8]. To obtain small size, MEMS technology is the most promising approach as it could offer tunable lumped element passives with high *Q*s. Despite the promise and potential of MEMS technology, only a handful of work has been proposed so far [67–69] that offer fully integrated tunable filters. Most research instead focus on approaches to increase the *Q* of inductors using air-gap above substrates [70], [71], substrate patterning [72], [73], backside release of substrates [74], [75], and thick silver electroplating [76], [77].

Table 1.3 summarizes the performance of RF tunable filters in the lower UHF range below 1 GHz, built with different fabrication technologies. Tunability of filters is achieved using solid-state varactor diodes or MEMS tunable capacitors. The first two work [78], [79] integrated MEMS tunable capacitors, which have better linearity and power handling capability than semiconductor based varactors, on a PCB. Due to the large size of RF circuits on PCB, this type of integration has larger size than complete integration of MEMS technology [69]. The customized multi-layer PCB technology [80] can provide much smaller size than other technologies, but the filter implemented using this technique does not show a proper response across the entire tuned spectrum mainly due to the low *Q* of passives embedded in the lower PCB layers. The listed filters can be also classified into two categories based on their fractional bandwidths; wide-band filters with ~20 % of 3dB-bandwidth (BW_{3dB}) and narrow-band filters with ~5 % of BW_{3dB}.

Complete integration with MEMS technology is clearly more beneficial for the narrow-band filters that require higher Q passives. For wide-band filters, high-Q inductors can be soldered to the filter chip and still a reasonable insertion loss can be obtained. However, size reduction is still an issue when using off-chip elements. Therefore, more advanced MEMS solution is necessary in order to achieve both high performance and small size. More detailed discussion about each tunable filter technology, targeting lower UHF band will be discussed in the next sub-sections.

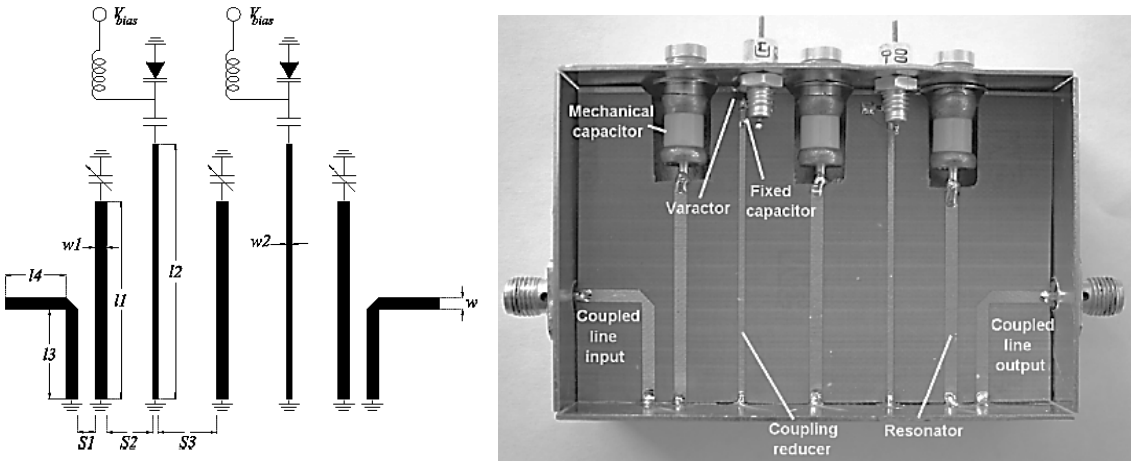
Table 1.3. Specifications of tunable front-end filters in the UHF range.

	Brown '00 [78]	**Borwick '03** [79]	**Lee '09** [80]	**Shim '09** [69]
f_c (MHz)	700-1330	225-400	510-910	516-638
Insertion loss	2.0-6.0	4.7-6.2	1.8-2.5	3.0-6.0
BW_{3dB} (% of f_c)	8-22	4	20	5-7
BW_{30dB}/BW_{3dB}	2.0-3.0	5.0-6.0	4.5-6.5	6.0-7.0
Tuning Speed	< 100 µs	< 600 µs	< 1 µs	< 1 ms
IIP_3 (dBm)	18-24 dBm	30-38 dBm	N/A	N/A
Technology	PCB (microstrip)	PCB (SMT) + MEMS	PCB (multilayer)	MEMS (single chip)
Size (mm^2)	31.0 × 41.0	30.0 × 44.5	4.4 × 3.4	6.1 × 8.1

1.3.1. Combline Filters with Continuous Control of Frequency and Bandwidth

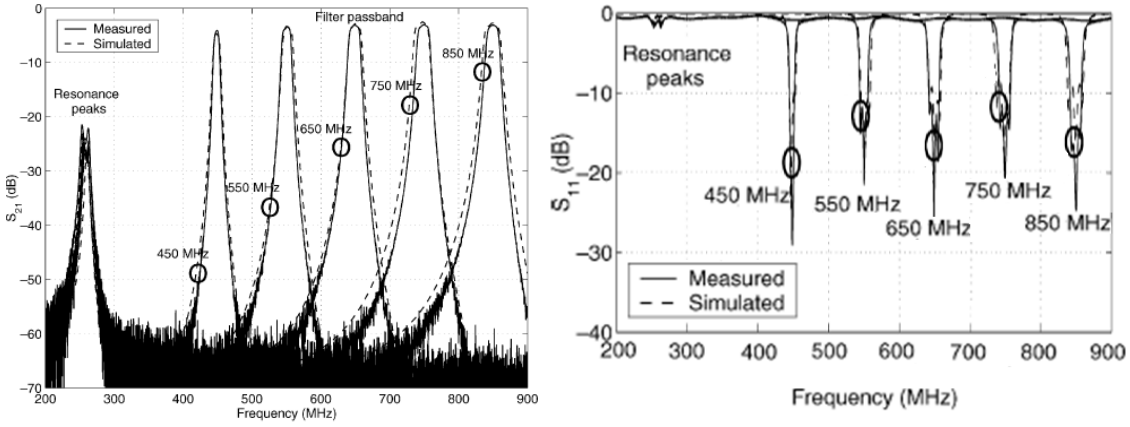
The most common tunable filter technology in the UHF and SHF range is based on stripline configuration implemented on a low RF loss substrate. This type of filters offer high performance and are usually reconfigured using semiconductor varactors. An exemplary third-order combline filter using suspended stripline technology is shown in Figure 1.5 [81]. The size of this filter is 50 × 65 mm^2, which is the largest of other state-

of-the art filters reviewed in this chapter. As shown in the measurement results (Figure 1.6 [81]), this filter provides wide frequency tuning range from 862 to 470 MHz with 5 to 15 MHz of bandwidth tuning. Using high-performance off-chip varactors, this filter design and technology provides low insertion loss and can be used for TV channel selection in the UHF–SHF band. However, as mentioned earlier, the size of the filter is relatively large, making it inapplicable for high-density integration.



(a) (b)

Figure 1.5. (a) a schematic and (b) photographic view of a combline bandpass filter [81].

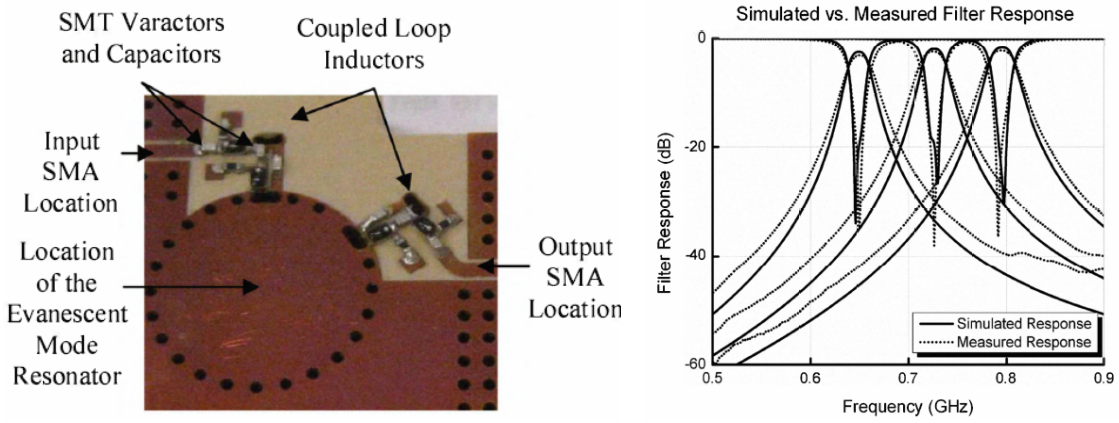


(a) (b)

Figure 1.6. Measured response in each tuned state; (a) insertion loss; (b) return loss [81].

1.3.2. Tunable Filter Using Vertically Integrated Evanescent Mode Resonator

Evanescent filter is another technology which enables low loss and narrow bandwidth filtering. A filter implemented using inductively coupled, vertically integrated cavity resonators is shown in Figure 1.7 [82]. The resonators provide Q of more than 300 at the target frequency range. The coupled inductor section is carefully designed using 3D electromagnetic simulation to achieve target coupling constant. The measured filter response is shown in Figure 1.7 (b) [82]. The filter center frequency is tuned from 650 to 800 MHz, while BW_{3dB} is tuned from 23 to 25 MHz. This filter technology can potentially offer very high Q and a low loss. The filter response can be further improved by increasing the order. However, this filter occupies a relatively large volume, especially in the lower UHF range and cannot be micro-fabricated.

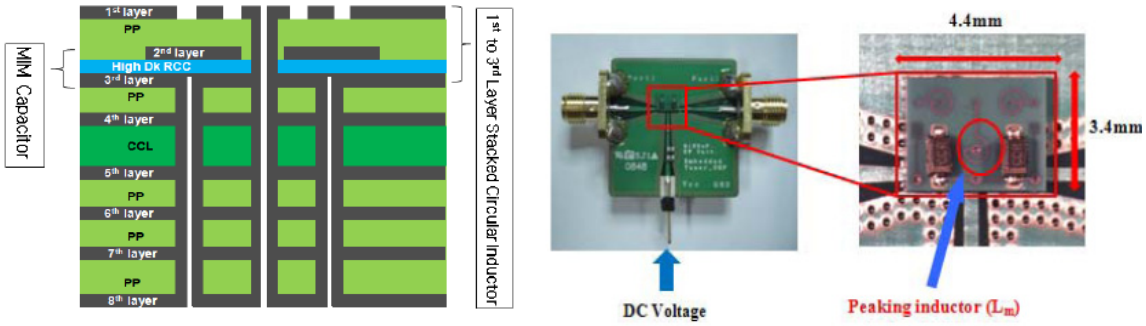


(a) (b)

Figure 1.7. (a) Photographic view, and (b) measured vs. simulated response of a tunable filter using vertically integrated evanescent mode resonator [82].

1.3.3. PCB-Embedded Tunable Lumped Element Filter

Small-size filters can be implemented using the PCB technology if lumped element components are embedded in different layers of the substrate. Figure 1.8 shows a tunable bandpass filter embedded into an eight-layered organic package substrate. Varactor diodes are assembled on the first layer of PCB to tune the frequency. Since this is only a second-order filter, the size is naturally smaller than other higher-order filters discussed earlier; however, this device is still impressively small, only about 4.4 × 3.4 mm^2 in size.



(a) (b)

Figure 1.8. (a) cross-sectional view of organic package substrate; (b) photographic view of the second-order coupled resonator with magnetic coupling [80].

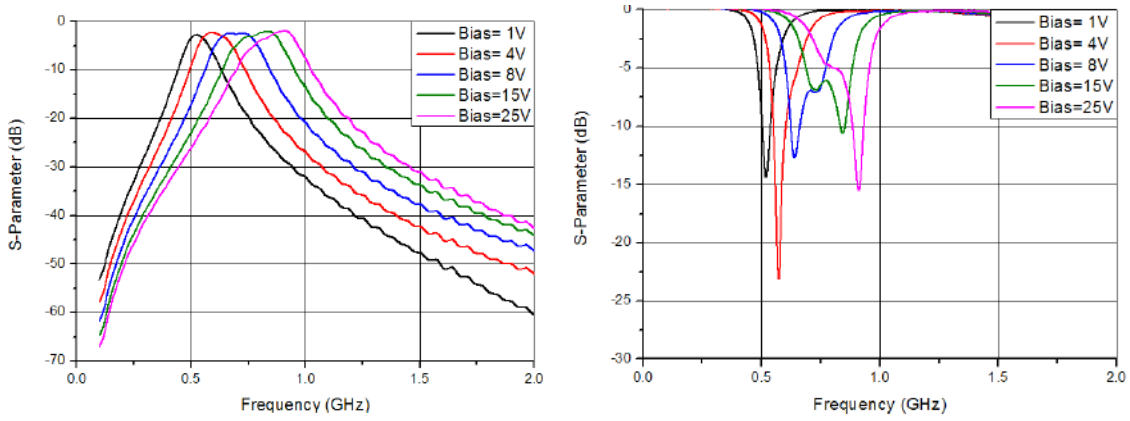
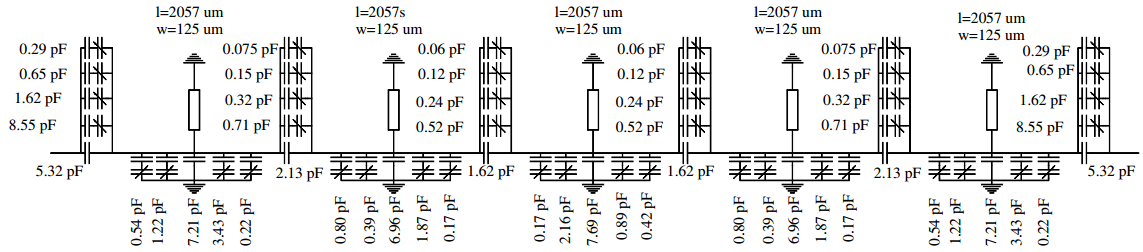


Figure 1.9. Measured filter response in each tuned state; (a) insertion loss; (b) return loss [80].

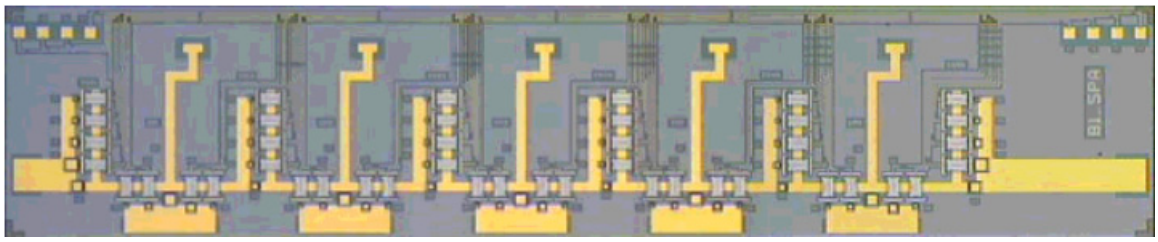
However, because the low order of the filter, the shape factor (30 dB-bandwidth (BW_{30dB}) to 3dB-bandwidth (BW_{3dB})) is high (Figure 1.9 [80]). Also, considering this is a relatively wide bandwidth filter with percentage bandwidth (BW_{3dB}/ f_c) of around 20%, the insertion loss is high. Although lumped element filter design using this technology has a potential to provide much smaller foot-print than other technologies, relatively long routing path from the top to bottom layer can derive additional loss, which makes it challenging to implement a narrow bandwidth filter with high performance.

1.3.4. Five-Pole Lumped Element Filter, Monolithically Integrated with MEMS Technology

To achieve both size reduction and high performance, monolithic integration of components on a single substrate is essential. The filter shown in Figure 1.10 is the first fully integrated tunable filter operating in lower UHF range below 1 GHz. This filter is designed using a combination of MEMS switched capacitor bansk and microstrip inductors and is capacitively coupled. It has five-poles and all inductances are 2.9 nH in value. As a result, the entire die size is 3.5×14.0 mm^2, substantially smaller than what would result if the inductor values were larger. The measurement result of the fabricated filter is shown in Figure 1.11. The center frequency is tuned from 986 MHz to 885 MHz while the bandwidth is maintained constant at 180 MHz. Within the tuning range, the insertion loss is ranged from 6.6 to 7.3 dB while return loss is above 10 dB.



(a)



(b)

Figure 1.10. (a) A schematic view and (b) a microscope image of a five-pole tunable bandpass filter [67].

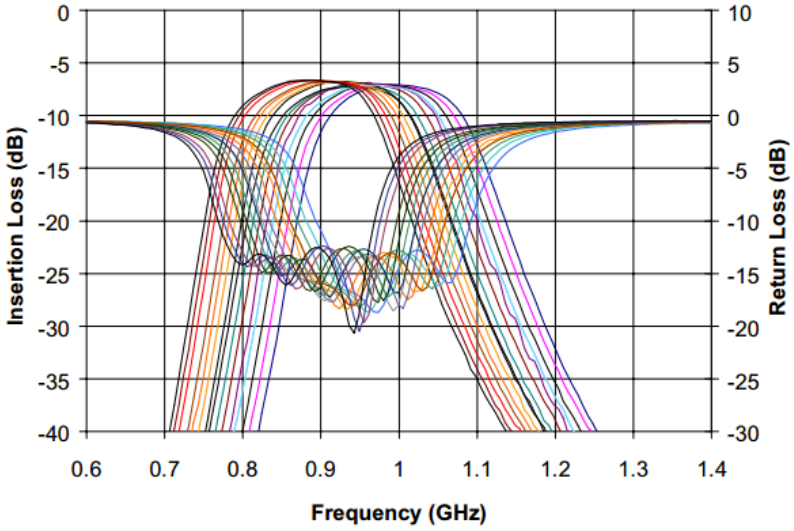


Figure 1.11. Measured frequency response of tunable bandpass filter in Fig. 1.10 [67].

Although this filter design and technology significantly reduces the size and provides high resolution frequency control, the tuning range of the filter is very limited. This is because the inductance of the microstrip resonators is relatively small, which demands large capacitance values in the resonator. The large MIM capacitance used to adjust the

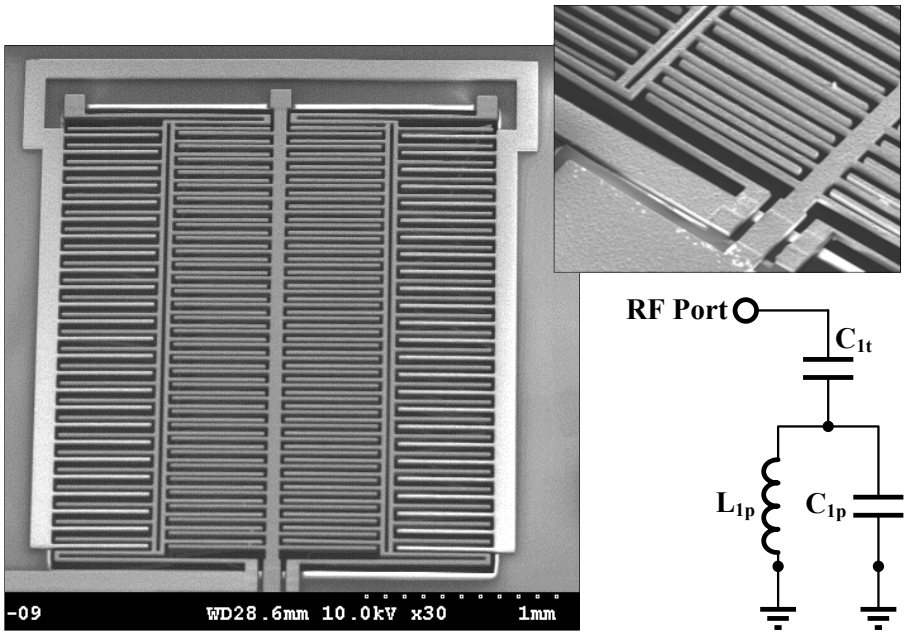
center frequency of the resonator limits the tuning range. The *Q* of capacitive switches is also not sufficiently high; resulting in a high level of insertion loss (*i.e.* above 6 dB) for this relatively wide bandwidth filter. Therefore, to extend the tuning range and improve the insertion loss level, a fabrication technology which provides more proper value of inductances and reasonably high *Q* is necessary.

1.4. Fully Integrated Tunable Filters using a Silver Micromachining Technology

Among reported work on tunable filters targeting lower UHF range, silver micro-machined tunable filters will be discussed in more detail here, to better understand the benefits of monolithic integration and the potential of the MEMS technology in implementing high-performance tunable modules.

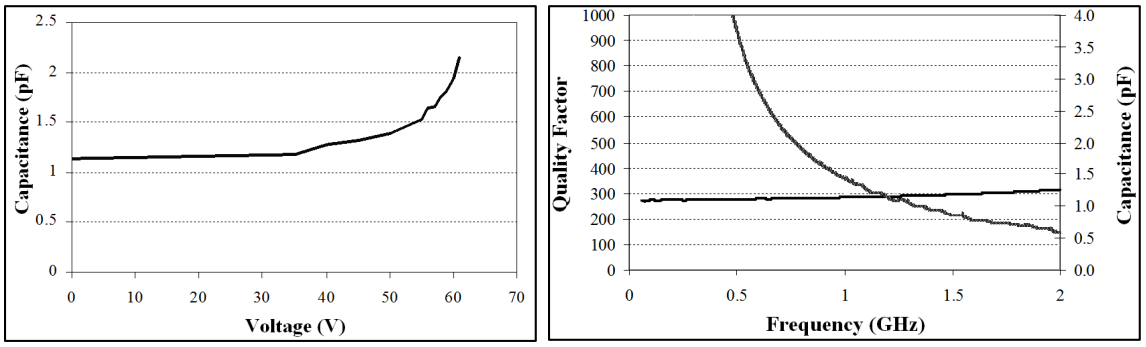
1.4.1. Design

These filters are deigned in lumped element configuration. The inductors and capacitors are fabricated simultaneously using a silver micromachining technology that offers high-*Q* and compact components [68]. To achieve frequency tuning, dual-gap MEMS lateral tunable capacitors are incorporated in the filter, as discussed in [83]. The electrical model and response of the tunable capacitors are presented in Figure 1.12 and Figure 1.13. The tunable capacitors are modeled as a sense capacitor (C_{1t}), in series with a parasitic inductor representing the spring (L_{1p}), and a parasitic capacitor representing the actuator (C_{1p}).



(a) (b)

Figure 1.12. (a) SEM view of the tunable capacitor, and (b) the electrical model of the tunable capacitor. The inset shows a close-up SEM view of the interdigitated fingers. The actuation gap is 20 μm and the sense gap is 10 μm.



(a) (b)

Figure 1.13. (a) Measured tuning and (b) embedded characteristic of the tunable silver capacitor. The trade-line of the measured data is shown for the quality factor.

The tunable filter is designed in the second-order coupled resonator configuration using capacitive coupling. Along with achieving continuous tunability at lower UHF band, the main design parameter of the filter is to push the quality factor and achieve a fractional bandwidth of less than 5 % with an insertion loss of better than 3 dB.

Capacitive coupling and matching are utilized as the size of the resulting filter is smaller and the insertion loss at the initial state is lower that inductively coupled filters.

Figure 1.14 shows the final electrical model of the filter, considering the parasitics. When designing the filters, values of the tunable capacitor (C_{1t} in Figure 1.13), fixed capacitor (C_{1f}), matching capacitor (C_2), and inductor (L_1) are selected with the following considerations: 1) the matched impedance of the filter is 50 Ω. 2) the 3dB fractional bandwidth is < 40 MHz; 2) The 50-dB rejection bandwidth is < 700 MHz; 3) the insertion loss is < 3 dB, and 4) the tuning range is > 100 MHz. To achieve the aforementioned requirement, a transmission zero is placed at the high frequency end of the filter. The frequency of the transmission zero is controlled by the value of C_{1t}, C_{1p} and L_{1p} (the parasitic inductance of the springs) with the following equation.

$$\omega_{tz} = \frac{1}{\sqrt{L_{1p}(C_{1f}+C_{1p})}}. \qquad \text{(Equation 1.1)}$$

To realize the required capacitance at each node, a fixed capacitor (C_{1f}) is placed in parallel with the tunable capacitor (C_{1t}).Using these guidelines several filters have been designed in the 220 MHz-640 MHz frequency range. Electrical simulations of the filters are first performed in Agilent ADS [84]. The optimizations of the physical layout of the filter and the individual lumped components are performed in Ansoft HFSS 3D modeler [85]. The thickness of the electroplated silver, the routing layer, and the silicon dioxide interlayer dielectric is assumed to be 30 μm, 4 μm, and 2 μm, respectively. The loss

tangent of silicon dioxide at 640 MHz is assumed to be 0.002. Figure 1.15 and Figure 1.16 show simulated responses of two filters centered at 480 MHz and 640 MHz, each having a bandwidth of ~40 MHz and insertion loss < 3 dB. The out-of-band rejection is >50 dB.

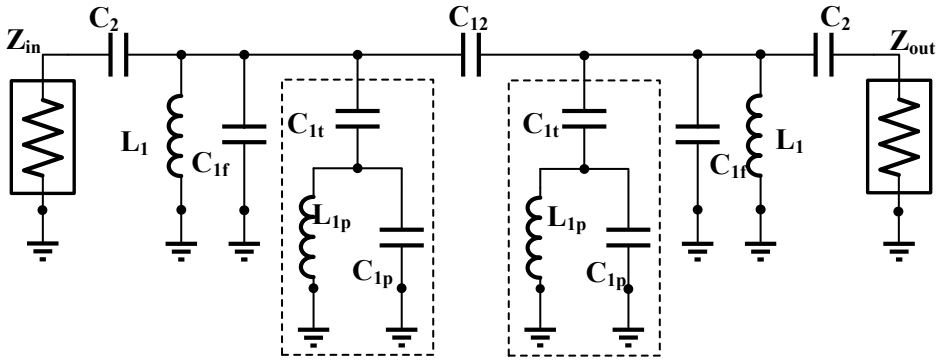


Figure 1.14. Electrical model of a tunable band-pass filter exploiting inductive parasitics for improved out-of-band rejection.

1.4.2. Measurement Result - Individual Filters

On-wafer S-parameter measurements of the fabricated devices have been carried out using an Agilent 8364B PNA and short-open-long-through (SOLT) calibration. The pad parasitics were insignificant and thus were not de-embedded. The measured out-of-band rejection of filters is better than 50 dB as shown in Figure 1.17 and Figure 1.18. In addition, filters exhibit a very high unloaded Q of > 44, the highest reported for UHF tunable filters on silicon. The unloaded Q is extracted from the measured frequency response using the following expression: $Q_u = \frac{f_0/BW}{1-S_{21}(f_0)}$. The tuning characteristic of a 640 MHz MEMS filter is shown in Figure 1.19. Continuous tuning is achieved by applying DC voltages to the isolated actuator port of the tunable capacitors. Tuning can

be significantly improved by increasing the thickness of the electroplated silver; thereby, increasing the tunable to fixed capacitance ratio.

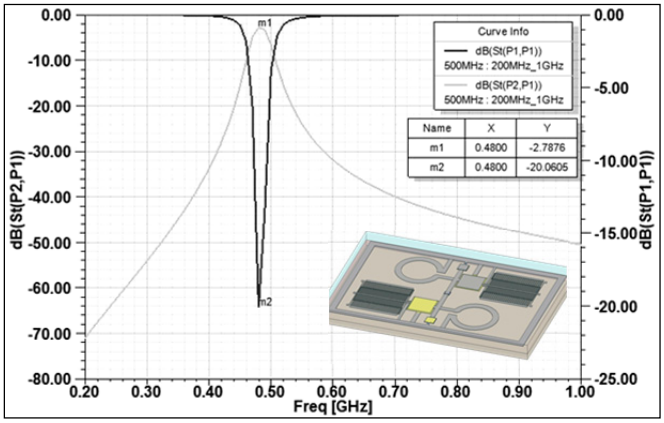


Figure 1.15. Simulated response and HFSS model of a filter at 480 MHz, showing an IL of 2.79 dB and out-of-band rejection of better than 50 dB.

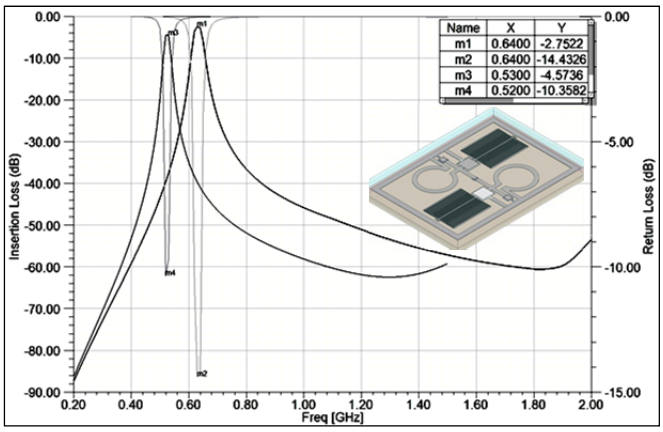


Figure 1.16. Simulated response and HFSS model of a filter at 640 MHz at the initial state and the maximum tuned state (520 MHz). The IL increases from 2.7 dB to 4.6 dB when the filter is tuned. The out-of band rejection is ~60 dB.

To demonstrate the importance of integration, the same filter is also implemented using off-chip inductors from coilcraft (Figure 1.20 (a)). Silver paste is utilized for integration of off-chip inductors as it requires much smaller interconnection area than other soldering technologies. The air-core off-chip inductor has a Q of 120 at 640 MHz

while the Q of the on-chip inductor in Figure 1.20 (b) is ~90. Although the off-chip inductors have higher Q than on-chip inductors, the filter response with off-chip inductors exhibits lower Q_u, and the initial f_c is also shifted. This is due to the loss of interconnects and additional parasitics from integration using the silver paste. The f_c of the filter can be further optimized by adjusting the value of on-chip capacitors, but the overall Q_u of the filter with off-chip inductors will be lower. This comparison well illustrates the benefits of monolithic integration which enables better Q_u and lower insertion loss (compare Figure 1.18 and Figure 1.21).

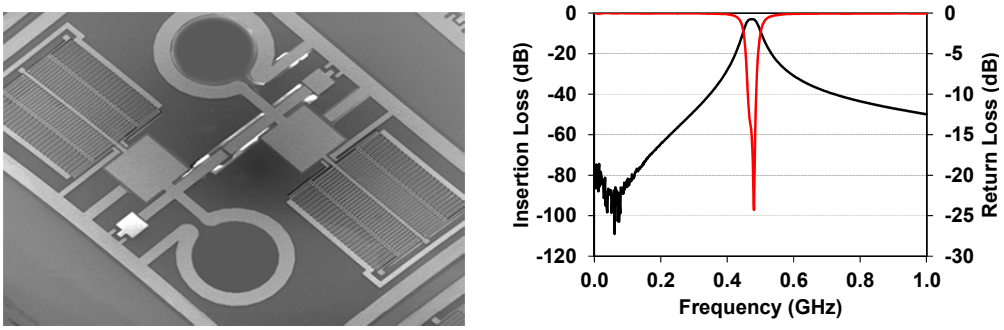


Figure 1.17. A SEM view (left) and measured response (right) of the filter, initially centered at 480 MHz. The transmission zero is at 1.5 GHz (not captured in this image). The unloaded Q of the filter is 44.

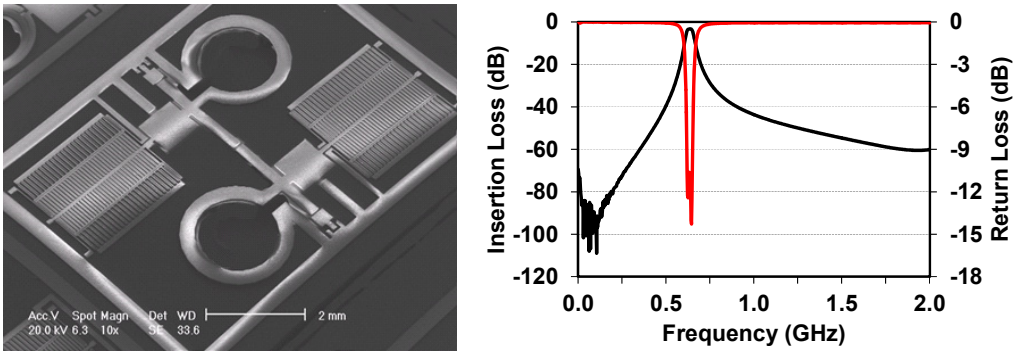
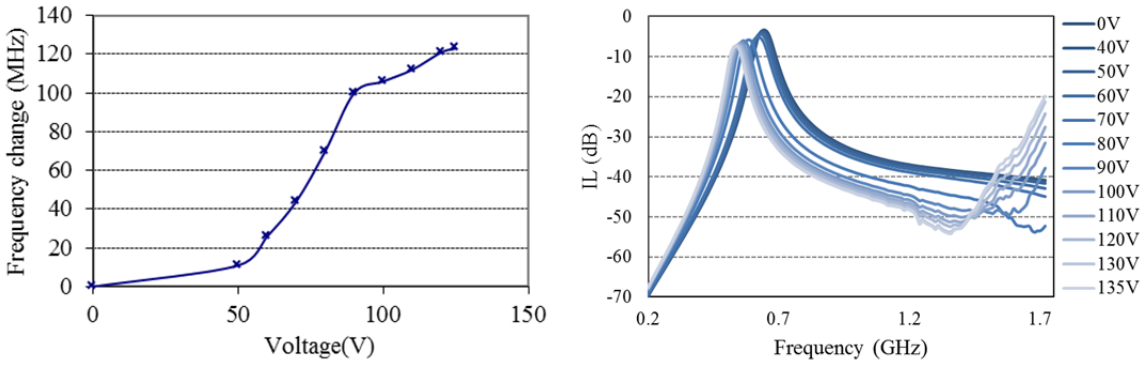


Figure 1.18. A SEM view (left) and measured response (right) of the silver filter at 640 MHz with out-of-band rejection of > 60 dB. The unloaded Q is 50, the highest reported for integrated MEMS filters on silicon.



(a) (b)

Figure 1.19. Measured tuning characteristic of a silver filter (coated with Parylene-C for improved tuning. The frequency of the transmission zero decreases as the filter is tuned.

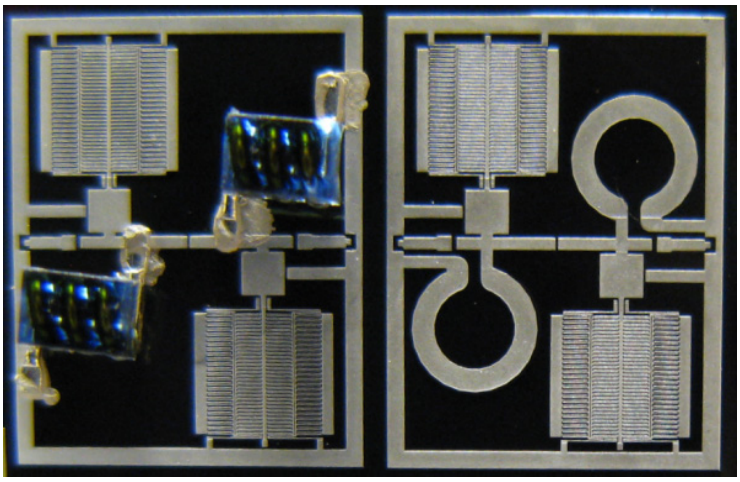


Figure 1.20. Micrograph images of the 640 MHz filter (a) using off-chip inductors and (b) fully integrated on silicon.

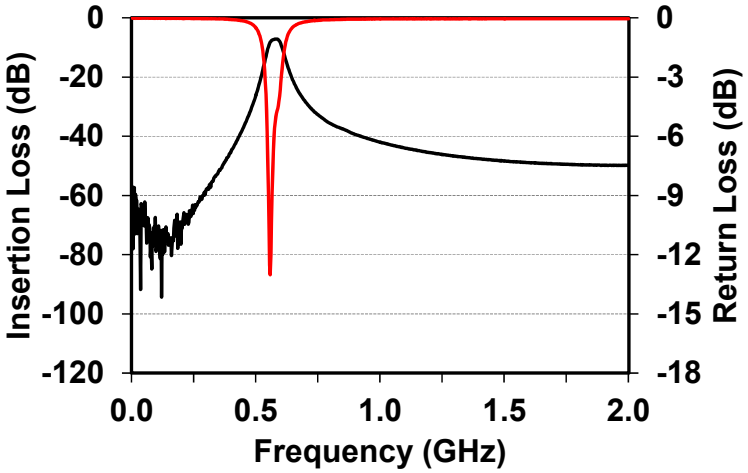


Figure 1.21. Measured response of the filter at 640 MHz using off-chip inductors from coil-craft, showing significantly lower performance compared to the integrated counterpart (compare to Fig. 1.18). This is due to the capacitive and resistive parasitics of the silver paste and the pads used to connect the off-chip inductors on the silicon die.

1.4.3. Measurement Result - Filter Array

Three filters with high out-of-band rejection are connected to the same input port to realize, for the first time, a three-way filter array fully integrated on silicon. The array can be used to receive and transmit signals in three different bands, simultaneously. Figure 1.22 shows the configuration and a SEM picture of the three-way filter with outputs centered at 208 MHz, 470 MHz, and 630 MHz. A passive matching network is designed at the input port as shown in Figure 1.22. The matching network provides 50 Ω matching between the input port of the filter array and each bandpass filter and minimizes the reflection at the input of the filters.

Simulated and measured responses of the three-way array are shown in Figure 1.23 (a) and (b). When placed in the array, the insertion loss of filters slightly increases and the bandwidth decreases due to the loss of the matching network and the minor cross-talk between the filters. The highest frequency filter suffers from the largest drop in the insertion loss since the parasitics of the long routing lines become more pronounced at higher frequencies. The performance of the filter array can be further improved by increasing the Q of matching components and reducing the length of interconnects. The matching network can be made tunable to provide proper matching across the entire tuning range of the filters.

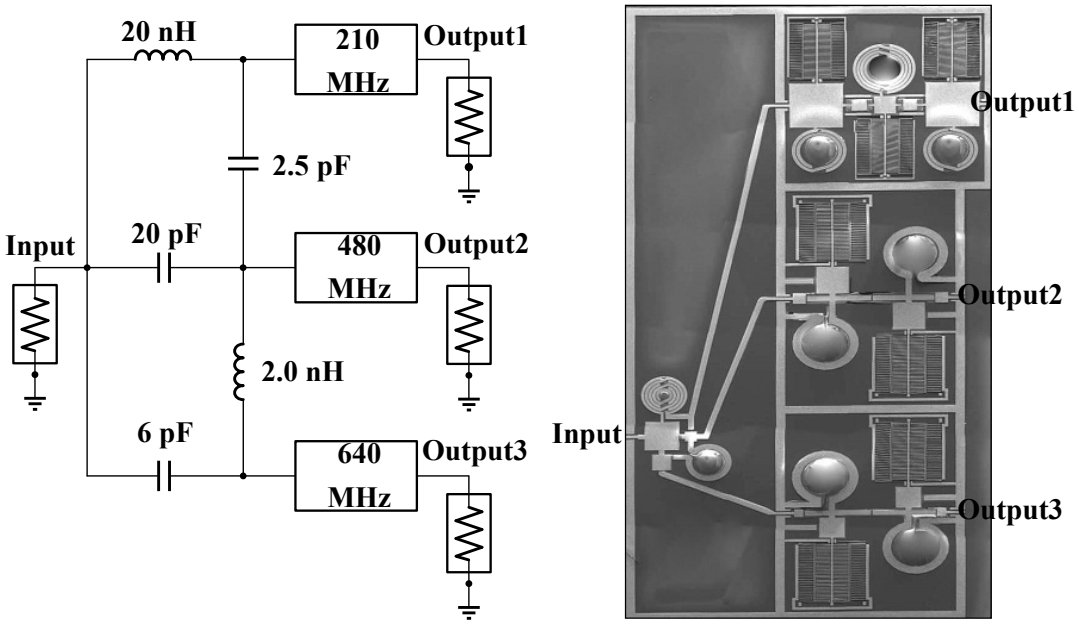
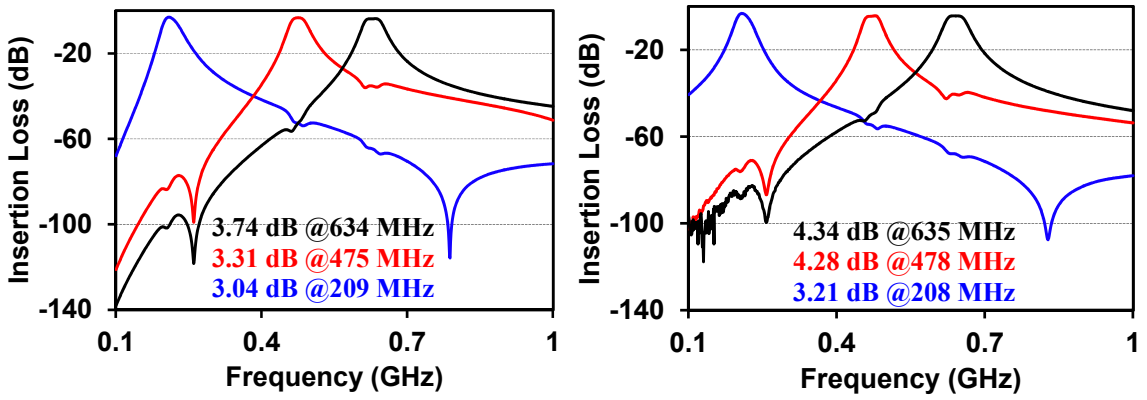


Figure 1.22. (a) Configuration, and (b) a SEM image of the three-way filter array.



(a) (b)

Figure 1.23. (a) Simulated, and (b) measured response of the three-way filter array showing the cross-talk between the filters is negligible thank to the high stop-band rejection of each filter.

1.5. Research Objectives

As shown in this chapter, previously reported filters at UHF range are either large in size (Figure 1.5, Figure 1.7), low in order (Figure 1.8), or have a limited tuning range (Figure 1.19). With the introduction of new frequency bands, the need for reconfigurable

and small-size front-end components has become more obvious. Our earlier work demonstrated the importance of integration; a fully integrated filter with moderate-*Q* inductors exhibits higher performance and is smaller in size/volume than a filter with high-*Q* post-assembled inductors due to the loss of interconnects and pad parasitics. The objective of this work is to address the critical need for reconfigurable RF front-ends by developing fully integrated, high-performance, small-form factor, tunable lumped filters, as the first step. As the newly released standards fall in the VHF–lower UHF range, frequency range of 500 MHz to 1 GHz is targeted for the filters. Two different tuning mechanisms and fabrication technologies are being considered. In the first approach, electrostatic actuation is used to tune the value of MEMS tunable capacitors and thus the frequency of bandpass filters. This technology is developed as tunable RF MEMS platform which can be utilized to implement various RF passives, including advanced reconfigurable front-end components. A filter was fabricated on a glass substrate and its frequency response was characterized, showing record low insertion loss of less than 3.5 dB across the entire tuning range (1 GHz to 600 MHz). In addition, good temperature stability (< 7%) and power handling (input third order intercept point (IIP_3) ~20 dBm) was achieved. However, the power handling and the tuning speed of the filter can be further improved using optimized designs for the tunable capacitors.

To demonstrate the versatility of the filter technology, similar filters have been implemented on a silicon substrate. The filters on silicon exhibit high performance

without the need for substrate micromachining. Other silicon-based passives and microsystems can be monolithically integrated on the same platform to realize all-silicon passive chip.

The packaging step is essential in RF tunable MEMS platform, for improved reliability and life time. The packaging process should not degrade the performance of the tunable filter, should be low cost, and preferably should be done at the wafer level process. As a proof-of-concept, the fabricated filters have been packaged using a low-temperature packaging technique. The filters show similar performance before and after the packaging process.

In the second approach, a different tuning mechanism based on PC material is considered. This technology is expected to provide better tuning speed and smaller foot-print than the filters tuned with MEMS capacitors. The fundamental RF performance, such as lumped element models, S-parameters, speed, and power handling capability of several PC switches is characterized. To improve RF power handling capability of the PC switch, a new type of switch structure is proposed. The frequency response of tunable phase change UHF filters has been simulated using the measured RF parameters of individual PC switches. These filters offer a faster tuning speed and are smaller in size than any other filter implemented at the UHF range.

1.6. Organization of Thesis

In Chapter 1, we introduced the concept of reconfigurable radios, tunable passives, and tunable filters, and presented the objectives of the proposed research. In Chapter 2, we will present the design and measurement results of temperature-stable, high-performance MEMS tunable capacitors fabricated using tunable RF MEMS platform. In Chapter 3, using the same fabrication technology, we will present the design and measurement results of a wide-band filter tuned using a bank of integrated electrostatically tunable capacitors. We will discuss other fabrication considerations such as the packaging process and use of Si as the substrate in Chapter 4. After that, we will introduce the principle of operation for phase-change materials in Chapter 5 and further present our preliminary work on RF switches using PC materials. Finally, we will discuss the future research goal and plans in Chapter 6.

CHAPTER 2.

HIGH PERFORMANCE, CONTINUOUSLY TUNED MEMS CAPACITOR

Electrostatically tuned MEMS capacitors can offer higher actuation speed and lower power consumption compared with piezoelectric, thermal, or magnetically actuated capacitors. Hence, there has been extensive work on electrostatically tuned capacitors and many wide tuning range devices have been reported. However, for successful insertion of the capacitor into RF systems, several other performance aspects of the device need to be simultaneously addressed; some or none of which is considered for in most reported tunable capacitors. These include tuning speed, initial capacitance value, Q, self-resonant frequency (SRF), and temperature stability.

In this chapter, we report on a tunable capacitor design which addresses all critical performance parameters that are discussed above. Specifically, a tunable capacitor is designed for stable operation over a wide temperature range. It is designed in a dual-gap configuration that offers fast tuning stabilization and a large tuning range. The mechanical design of the membrane and springs is optimized to overcome the warping issue due to residual stress and temperature variation, while maintaining a tuning voltage

of less than 40 V. The Q of the capacitor is maintained high (*i.e.* $Q > 100$) across the entire tuning range. Such capacitors can be directly integrated with high-Q inductors to implement continuously tunable filters for reconfigurable radio applications, as will be shown later in this thesis.

This chapter is organized in the following order. We will first introduce the design of springs and membranes, which have good temperature stability. Next, we will discuss the fabrication technology with emphasis on the choice of sacrificial layer and its release process. Finally, we will conclude the chapter by documenting the measurement results. In the following chapter, we will demonstrate the application of these components in tunable bandpass filters.

2.1. Design

For the design of tunable capacitors, the specifications listed in Table 2.1 were targeted. The capacitors are electrostatically tuned, temperature stable, and have separate RF and DC electrodes for better power handling as well as more convenient tuning. The layout of the tunable capacitor is shown in Figure 2.1, schematically. For continuously tuned capacitors (or varactors), a dual-gap configuration [86] is adopted (actuation to sense gap of 4:1) to overcome the pull-in limitation and achieve better linearity. The size of the entire membrane is decided by the center area for initial capacitance of 200 fF and the actuation area for maximum tuning bias of 40 V. The size of the center RF node is

145 μm × 145 μm, while the overall size of top membrane is 310 μm × 310 μm. The actuation air gap is designed to be 2 μm, considering the membrane size and the fabrication yield.

Table 2.1. Target specifications of the tunable capacitor.

Specifications	Target
Configuration	Series-type (1 port)
Tuning-type	Continuous / Switched
Initial capacitance (C_{IN})	200 fF
Tuning range (C_{FN} / C_{IN})	> 5
Quality factor (Q)	> 100 @ 1GHz
Operation range	up to 2 GHz
Mechanical resonant frequency (f_M)	> 20 kHz
Maximum tuning bias (V_T)	< 40 V
Temperature variation (C_{IN}, C_{FN}, V_T)	< 10 % (223 K ~ 333 K)
Dimensions	< 400 × 400 μm^2

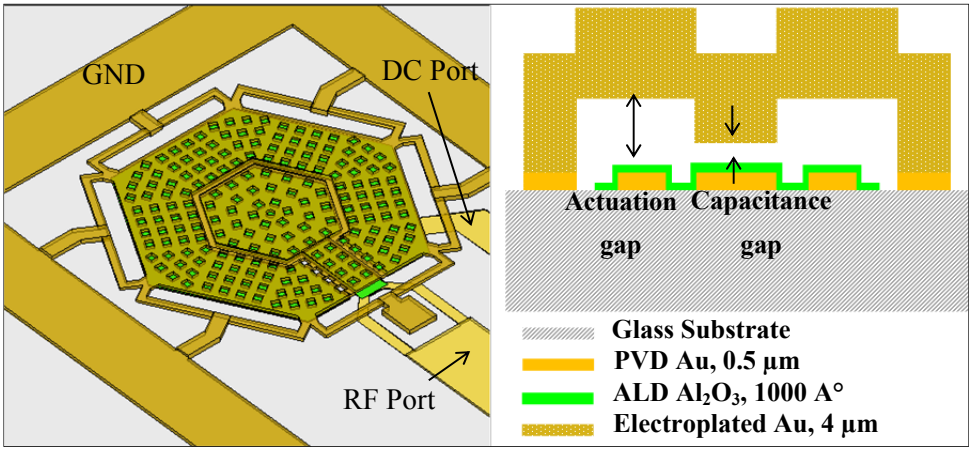


Figure 2.1. Layout of the tunable capacitor. Top-down view (left) and cross-section view (right).

For the mechanical design of the capacitor, ANSYS finite element simulation software [87] is used considering the residual stress (40 MPa) and stress gradient (2 MPa/μm) of

gold extracted from measurements. Other material properties of the gold layer is set as 45 GPa (Young's modulus), 19.30 g/cm^3 (mass density), and 14.7 ppm/°C (thermal expansion coefficient), according to the published values for electroplated gold. Two major specifications considered here are mechanical resonant frequency (f_M) and temperature stability of capacitance. For the springs, the geometrically compensated spring and anchoring design introduced in [88] was adopted. This structure releases thermally induced residual stress in the lateral direction, reducing the deformation in the vertical direction. Prior works using this compensation technique utilized a square-shape membrane. In this work, a hexagon-shape membrane is selected since it offers a higher mechanical resonant frequency for a temperature stable design. To compare characteristics of each structure, two square-shape and one hexagon-shape membranes with the same-size membrane and capacitance electrode are simulated. The springs of the square Membrane I are designed for f_M of 17 kHz, while the square Membrane II and the hexagonal membrane have f_M of 23 kHz, all within the target range of resonance frequency. Figure 2.2 shows the deformation of the top membrane in both square-shape membranes when 40 MPa of residual stress and 2 MPa/μm of residual stress gradient are applied at room temperature (300 K). The deformation of the hexagon-shape membrane under the same stress condition is shown in Figure 2.3. All designs show a maximum deformation of less than 80 nm, which is relatively small compared to the capacitance air gap of 0.5 μm. Next, the temperature stability is evaluated. As shown in Figure 2.4, larger deformation is observed

upon temperature variation for the square Membrane II since the wider springs do not relieve thermally induced stress as much as the narrow springs of square Membrane I. The square Membrane I shows comparable temperature stability as the hexagonal membrane, but f_M is limited to below 20 kHz. Therefore, the hexagonal membrane is selected as it provides small deformation, low temperature variation, and larger f_M.

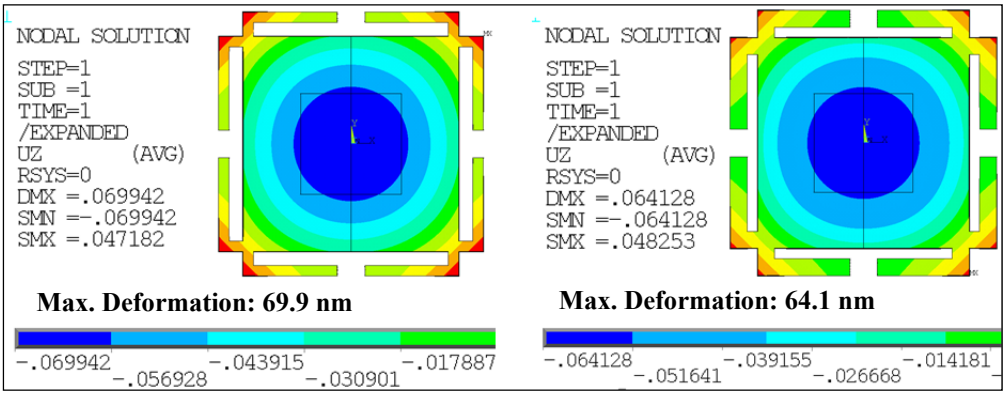


Figure 2.2. Deformation of the top membrane upon 40 MPa of residual stress and 2 MPa/μm of stress gradient; square Membrane I with f_M of 17 kHz (left) and square Membrane II with f_M of 23 kHz (right).

Other characteristics of the hexagonal membrane under different stress conditions are also analyzed. First, the deformation of the membrane with 50, 100, and 200 MPa of residual stress and no residual stress gradient is simulated over the same temperature range. As shown in Figure 2.5, the deformation is not affected by the residual stress and is less than 10 nm. Therefore, this hexagonal membrane design is very robust against residual stress and temperature variations. The second simulation is under 40 MPa of residual stress and different residual stress gradient of 2, 5, and 10 MPa/μm, respectively (Figure 2.6).

The deformation of the membrane is highly affected by stress gradient. Thus, the stress gradient in the electroplated gold should be carefully controlled.

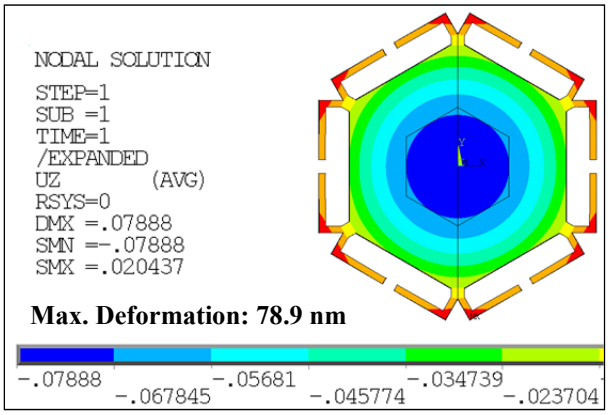


Figure 2.3. Deformation of the hexagonal membrane upon 40 MPa of residual stress and 2 MPa/μm of stress gradient at room temperature (300 K).

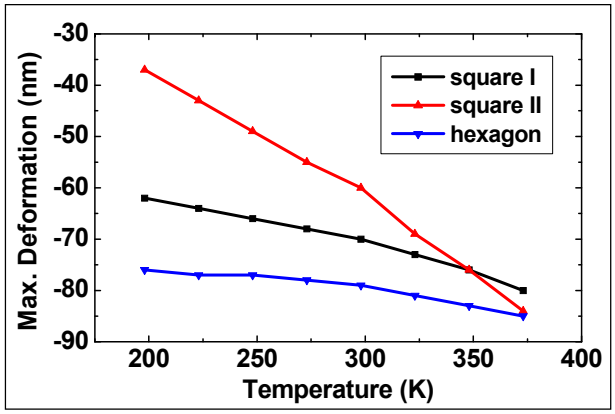


Figure 2.4. Maximum deformation of the square-shape membranes upon 40 MPa of residual stress and 2 MPa/μm of stress gradient when temperature is varied from 198 K to 373 K.

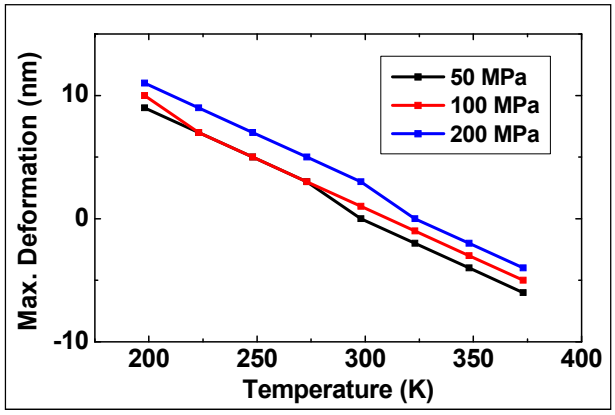


Figure 2.5. Maximum deformation of the hexagonal membrane upon 50, 100, and 200 MPa of residual stress when temperature is varied from 198 K to 373 K.

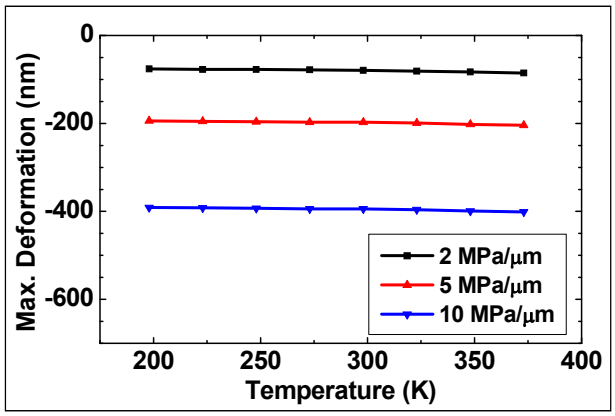


Figure 2.6. Maximum deformation of the hexagonal membrane upon 40 MPa of residual stress and 2, 5, and 10 MPa of stress gradient when temperature is varied from 198 K to 373 K.

The final membrane and spring design, including release holes is simulated under the same stress conditions over the temperature range from 223 K to 333 K, as shown in Figure 2.7. The temperature-induced change in the deformation of the central part, which defines the capacitive gap, is limited to 10 nm. The resulting change in the initial capacitance is thus less than 2.5%. The variation at larger stress gradient (4 MPa/μm) is

also simulated (Figure 2.8). As expected, maximum deformation increases with larger stress gradient, but the temperature variation of the capacitance gap is only around 10 nm.

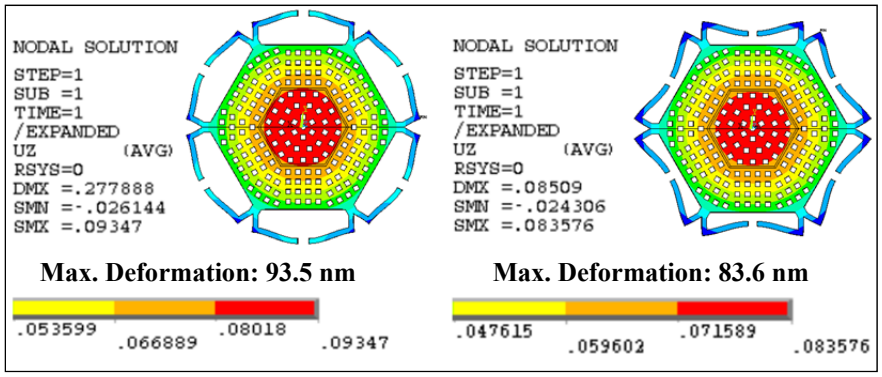


Figure 2.7. Deformation of the top membrane upon 40 MPa of residual stress and 2 MPa/μm of stress gradient at 223K (left) and 333K (right).

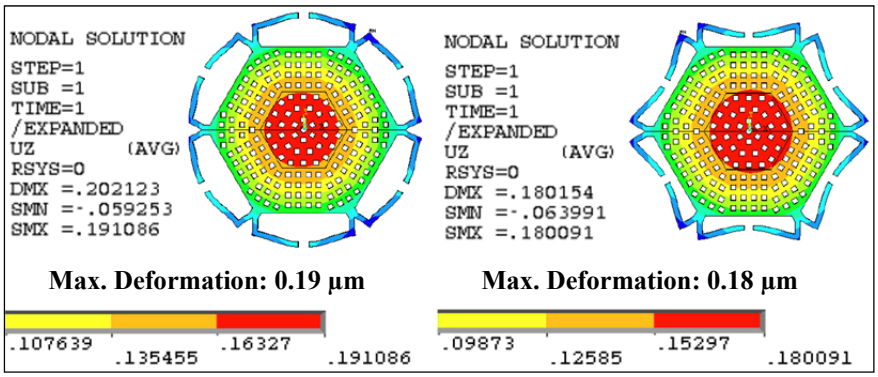


Figure 2.8. Deformation of the top membrane upon 40 MPa of residual stress and 4 MPa/μm of stress gradient at 223K (left) and 333K (right).

To simulate the electrical properties, such as C_{IN}, C_{FN}, and Q, the HFSS 3D electromagnetic tool [85] is utilized. The properties of the substrate are applied for accurate simulation of quality factor and self-resonant-frequency. Accurate simulation of C_{FN} during touch-down of the top membrane is difficult since there are various non-ideal factors, such as deformation of the top membrane, electrical properties and surface

conditions of the dielectric layer as well as non-uniform electrostatic force between the actuation electrodes. To reflect these non-idealities, C_{FN} is simulated using a reduced dielectric constant for the dielectric layer, around quarter of the bulk value. The simulated result in Figure 2.9 shows that Q is higher than 100 at 1 GHz at all tuned states; the initial Q is better than 500 and the final tuned value is around 130. The SRF at initial and final tuned states is 15 GHz and 7 GHz, respectively, which is sufficient for the target operation range, up to 2 GHz.

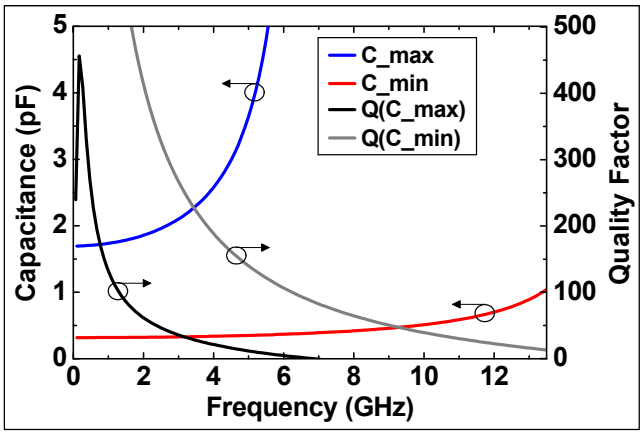


Figure 2.9. Initial capacitance, maximum capacitance, and Q at initial and final states extracted using the HFSS tool.

2.2. Fabrication Technology

The proposed tunable RF MEMS platform in Figure 2.10 is designed for simultaneous fabrication of capacitive switches, tunable capacitors, fixed MIM capacitors, high-Q inductors, transformers, and lumped element filters discussed in the following chapter. The fabrication process flow is schematically shown in Figure 2.11.

The only difference between the switches and varactors is the ratio of the actuation to sense gap. A reduced dual-gap ratio of 4:3 is used for switches to achieve better contact between the top center electrode and the bottom RF electrode. The inductors are fabricated out of the final thick electroplated layer and the layer used to implement the top membrane of the switches and capacitors.

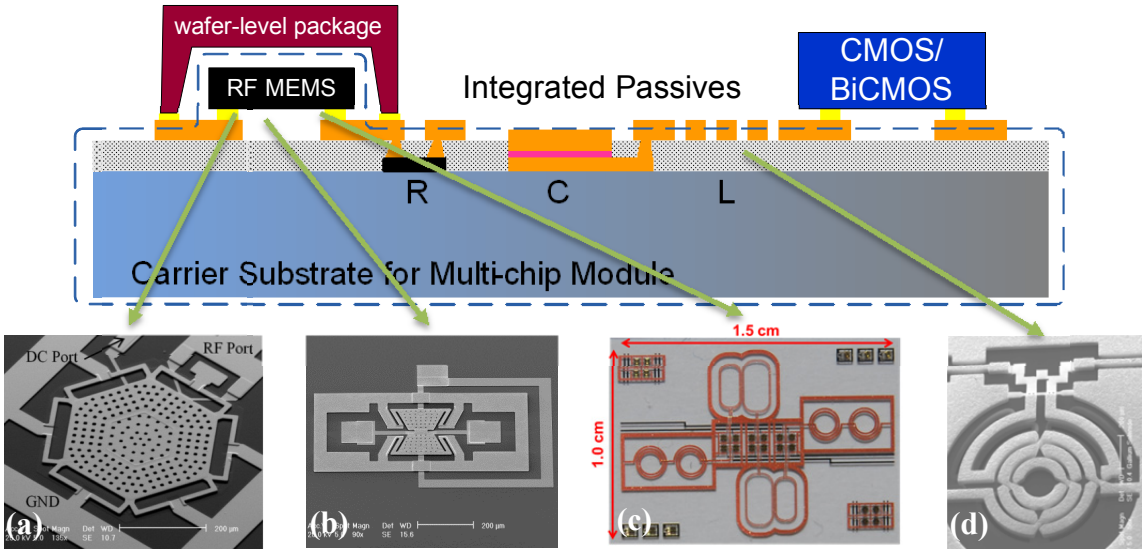


Figure 2.10. Schematic diagram of the tunable RF MEMS platform applicable for a variety of RF passive components; (a) tunable capacitor; (b) switch; (c) tunable filter; (d) high-*Q* inductor.

The fabrication starts with the deposition and lift-off patterning of the first metal layer consisting of 300 A° Cr / 5000 A° Au / 300 A° Cr on a Borosilicate glass substrate. This layer is used for bias lines and bottom electrodes of tunable capacitors. Borosilicate glass is chosen because it exhibits low loss at RF. Though, the same fabrication process can be applied to other substrates, such as high-resistivity silicon and or passivated CMOS-grade silicon. Next, a 1000 A° thick aluminum oxide (Al_2O_3) layer is deposited

using an atomic layer deposition (ALD) tool with water vapor at 250 °C. ALD Al_2O_3 is chosen as the inter-layer dielectric because of its high dielectric constant (ε_r) of close to 10 and uniform side-wall coverage. The Al_2O_3 is patterned using Transene aluminum etchant Type A at 50 °C.

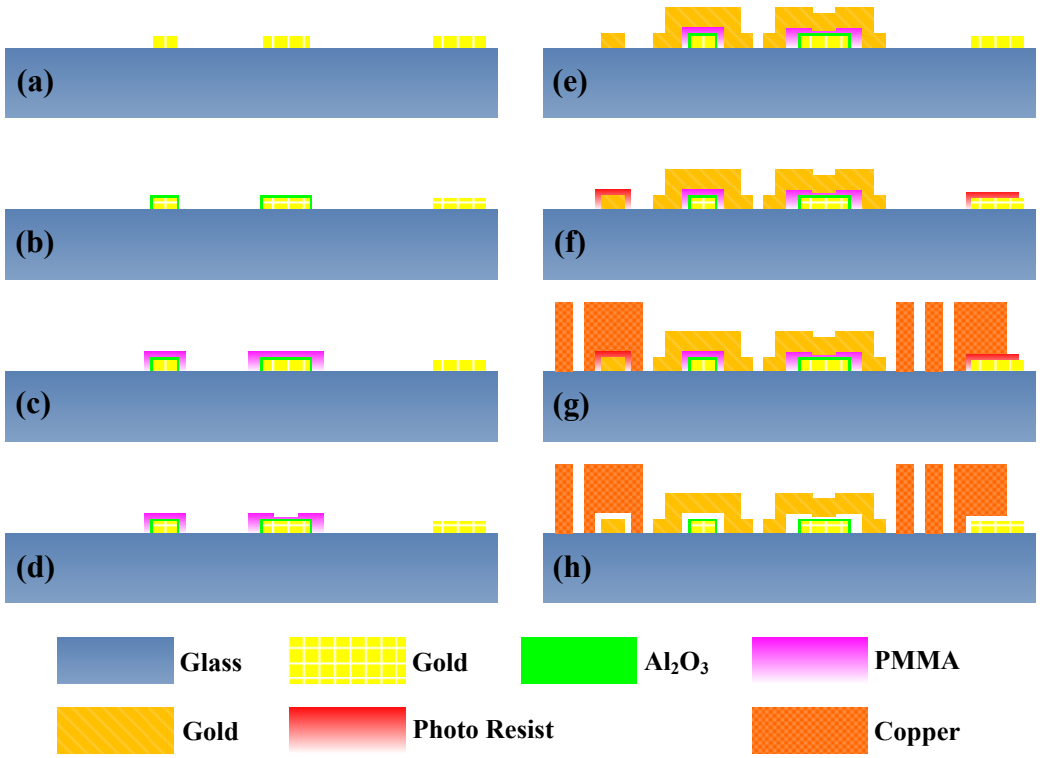


Figure 2.11. The fabrication process flow; (a) Au lift-off; (b) Al_2O_3 deposition; (c) PMMA patterning; (d) PMMA thinning; (e) Au electroplating; (f) S1813 lithography; (g) Cu electroplating; (h) release in Acetone followed by CPD.

Next, a sacrificial layer is deposited and patterned. For the selection of the sacrificial layer, the following factors should be considered: the sacrificial layer should not be deformed or attacked during the subsequent processing steps and its etchant during the release process should have a good selectivity against other layers. Some commonly used sacrificial layers are polymers [17], [89], metals [90], [91], silicon dioxide [71], and

amorphous silicon [92]. Amorphous silicon can be deposited with various methods such as plasma-enhanced chemical vapor-deposition (PECVD) or sputtering and it is not easily attacked or deformed during the post processing steps [94]. The main problem with PECVD amorphous silicon is that it is hard to remove with either wet etchants, such as KOH, or dry etchants, such as Xenon Difluoride (XeF_2) [95]. Sputtered amorphous silicon can be easily removed with XeF_2. However, the removal of sputtered amorphous silicon in XeF_2 is non-uniform; thereby, long etch time is needed to release the device. The long XeF_2 release step results in increased stress in other metal layers on the wafer (in our case when the release time is increased beyond 15 min). Figure 2.12 shows the stress distribution of a gold electroplated silicon wafer when 30 cycles (15 min) and 90 (45 min) cycles of XeF_2 is applied, respectively. Each XeF_2 cycle is composed of 30 seconds of gas flow. The stress in the gold layer clearly increases upon long exposure to XeF_2. Although the release condition is subjective to the deposition parameters and properties of the amorphous silicon layer as well as the XeF_2 etch process, and one might characterize a recipe for better release of amorphous silicon, the increased stress in metal layers is hard to avoid. The initial value and the tuning characteristic of capacitive devices are highly dependent on the stress in the released metal film and therefore, amorphous silicon was not chosen as the sacrificial layer in this process. Instead, uncured Polymethylmethacrylate (PMMA) is used as the sacrificial layer. The main advantage of using uncured PMMA is that it can be easily removed in a relatively short

time and without damaging other layers on the substrates. Alternatively, a metal could be used as the sacrificial layer. However, for a process consisting of three metal layers and several metal adhesions layers, it is unlikely to find a metal that its etchant is selective to all other metals on the wafer during release.

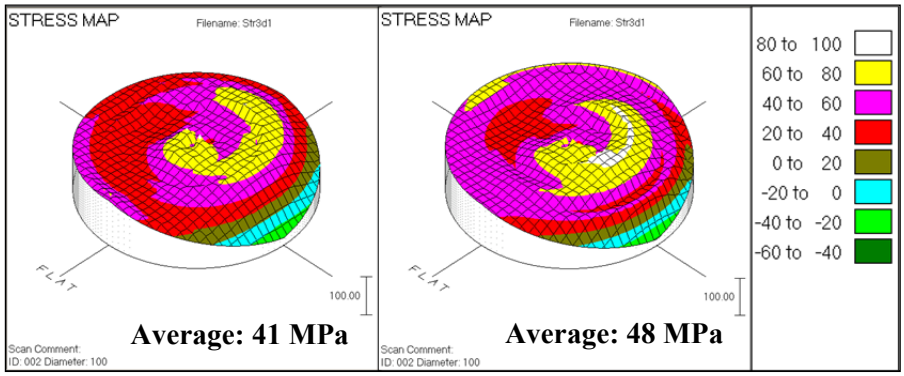


Figure 2.12. Residual stress distribution of a 2 µm thick gold layer electroplated on a silicon wafer after 30 cycles (left) and after 90 cycles of XeF_2 etch (right).

2.3. Measurement Result

Figure 2.13 shows the SEM view of the fabricated tunable capacitor. The RF properties of the tunable capacitor are measured using a N5241A Agilent PNA-X network analyzer and Cascade Microtech GSG Z-probes. The measured capacitance and *Q* at each tuned state is shown in Figure 2.14. The varactor has a continuous tuning of capacitance from 220 fF to 1.33 pF and *Q*s higher than 65 at 1 GHz at all tuned states. The measured tuning range is smaller, compared to the simulated range of 300 fF to 1.7 pF. The discrepancy between the measured and simulated initial capacitance values can be due to the warping of the top membrane, which itself might be the result of a larger

stress gradient in the electroplated gold layer. From the measured initial capacitance, around 0.2 μm of membrane warping is expected, which corresponds to a residual stress gradient of 4 MPa/μm (see Figure 2.8). The smaller touch-down capacitance value is due to the rough surface of the dielectric as well as the warping of the top membrane. The measured SRF of the varactor is more than 13.5 GHz at the initial capacitance state and 8.9 GHz at the final tuned state.

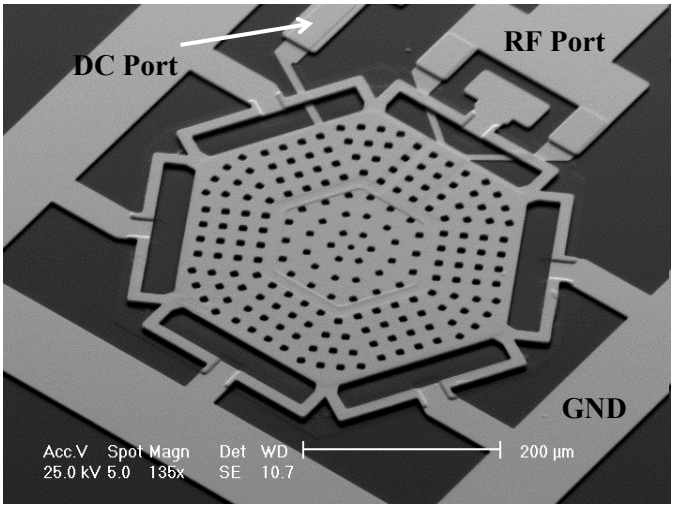


Figure 2.13. A SEM image of a fabricated tunable capacitor.

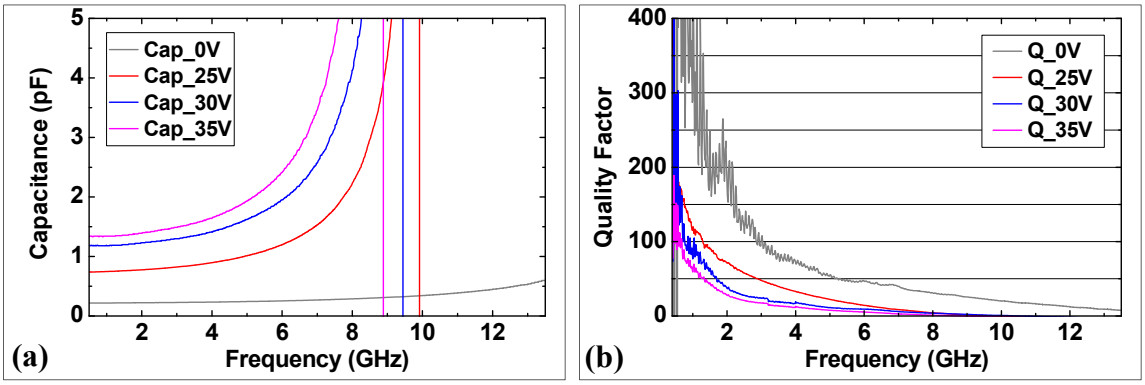


Figure 2.14. (a) Measured capacitance and (b) quality factor of the varactor at different tuning bias.

The tuning characteristics of the varactor and switched capacitor are compared in Figure 2.15 and Figure 2.16. Since both capacitors have the same springs and membrane design and only different in capacitance gap size, the tuning range of capacitance and Q is very similar. However, the C-V trend shows a clear difference; the largest transition slope of the varactor is 0.25 pF/V while that of the switched capacitor is more than 0.5 pF/V. This is due to the larger actuation to sense gap ratio for the continuously tuned capacitor. For both designs, the largest capacitance value is not achieved at the pull-in bias, but at larger bias voltages close to 35 V at which the membrane is flattened with larger actuation force. The warping in the membrane can be reduced with a more optimized gold electroplating process. The structural compensation can also be improved to allow better tolerance on the stress gradient.

Figure 2.17 shows variation of initial capacitance, maximum capacitance, and tuning bias over temperature range of 223 K to 333 K. Microtech KV-230 cryogenic station and GGB RF probes are used for these measurements. The initial and final capacitance values only show 5% and 7% variation, respectively, from the values at room temperature; whereas, the required tuning bias shows larger variation of 9%. These results are consistent with ANSYS simulations; the deformation of the top membrane as a result of temperature change is small as the uniformly induced stress is well relieved, laterally.

The tuning speed of the varactor is measured using the setup in Figure 2.18. A tuning bias is applied through a function generator while a high-power single-tone RF signal is injected from N5214A VNA. Since this varactor is a one-port device, the reflected power level from it is guided through a circulator and converted into voltage signal by a KRYSATAL 201A power detector. This voltage signal is detected by one port of an oscilloscope while the tuning bias is triggered in the other port of it. Figure 2.19 shows the response of the capacitor (the detected output of the power detector) when 15 V and 40 V of tuning bias is applied, respectively. The mechanical resonance frequency is extracted to be 25 kHz from the oscillation time, and the stabilization time is less than 80 μs. The mechanical response is in good agreement with the ANSYS simulation results.

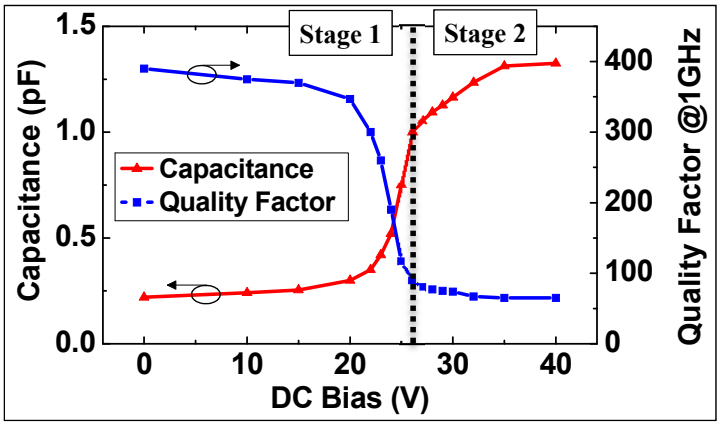


Figure 2.15. Tuning characteristics of the continuously tuned capacitor. At Stage 1 the air gap closes uniformly. At Stage 2 (after touch-down at 26 V) the membrane conforms to the substrate.

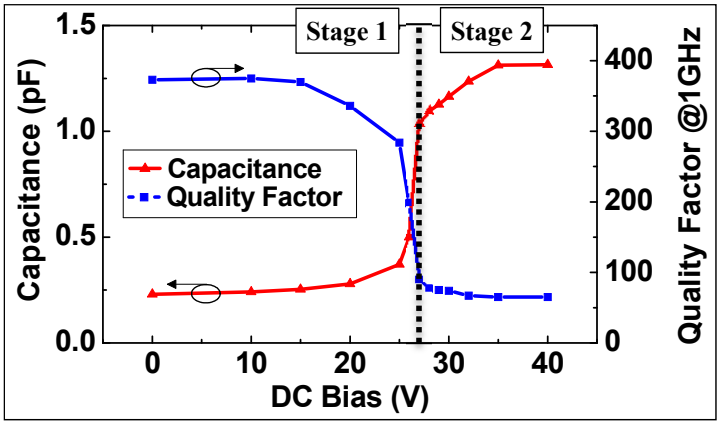


Figure 2.16. Tuning characteristics of the switched capacitor. At Stage 1 the air gap closes uniformly. At Stage 2 (after touch-down) the membrane conforms to the substrate.

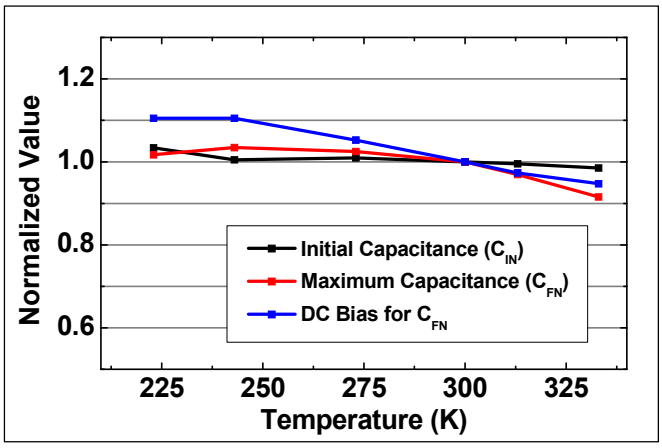


Figure 2.17. Measured initial and final capacitance values as well as the maximum DC bias are stable within 5%, 7%, and 9% of their room temperature values.

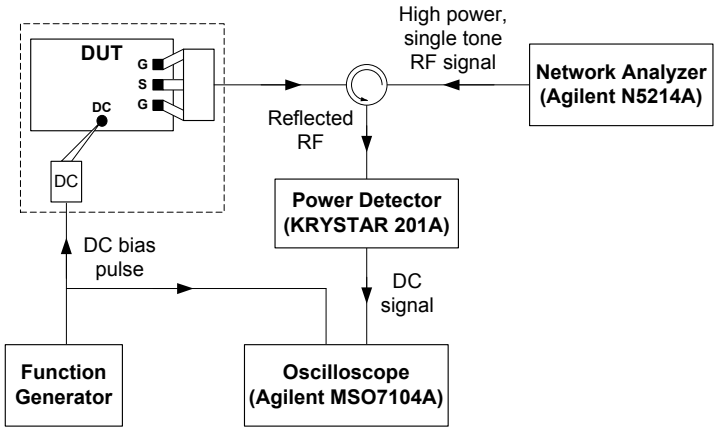
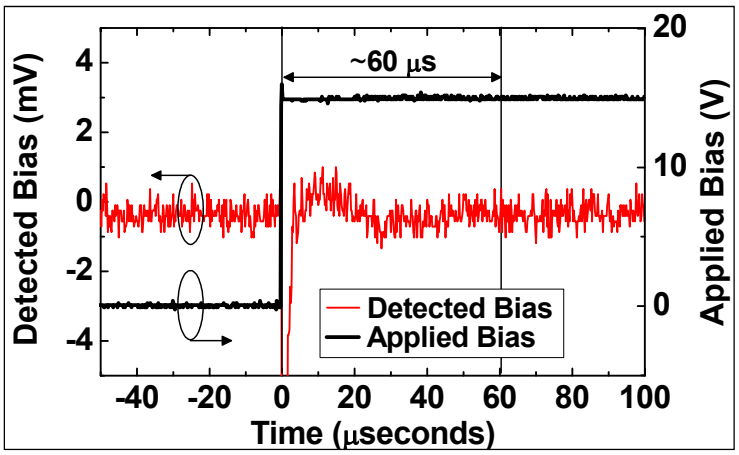
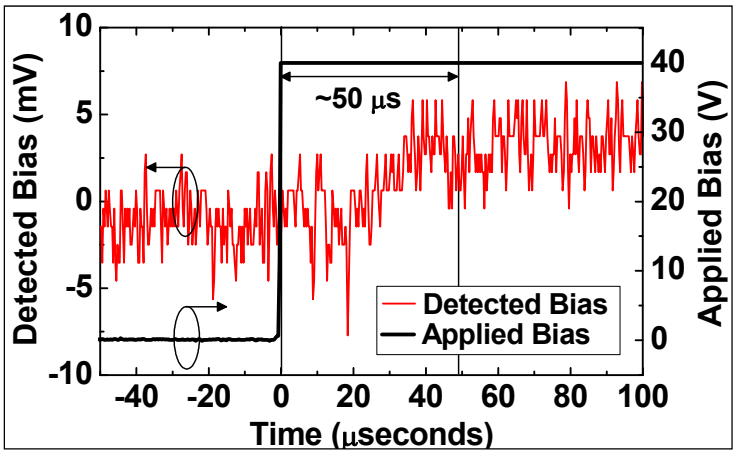


Figure 2.18. Measured initial and final capacitance values as well as the maximum DC bias are stable within 5%, 7%, and 9% of their room temperature values.



(a)



(b)

Figure 2.19. Tuning speed measurement; (a) with 15 V of tuning bias; (b) with 40 V of tuning bias.

The tuning speed of the varactor is measured using the setup in Figure 2.18. A tuning bias is applied through a function generator while a high-power single-tone RF signal is injected from N5214A VNA. Since this varactor is a one-port device, the reflected power level from it is guided through a circulator and converted into voltage signal by a KRYSATAL 201A power detector. This voltage signal is detected by one port of an oscilloscope while the tuning bias is triggered in the other port of it. Figure

2.19 shows the response of the capacitor (the detected output of the power detector) when 15 V and 40 V of tuning bias is applied, respectively. The mechanical resonance frequency is extracted to be 25 kHz from the oscillation time, and the stabilization time is less than 80 μs. The mechanical response is in good agreement with the ANSYS simulation results.

2.4. Analysis on Power Handling Capability

To analyze the power handling capability of the tunable capacitors, the Agilent ADS simulation tool is used. Non-linearity of the varactor and capacitive switches are taken into account using non-linear electro-mechanical models [96]. The simulation parameters such as initial capacitance, air gap, and mechanical properties of the varactor are summarized in Table 2.2. All values are carefully extracted from HFSS electromagnetic simulations and modal/displacement analysis in ANSYS. Since the integrated varactor has separate electrodes for actuation and capacitance sensing, the total force can be approximated as the sum of the actuation force from the DC bias applied to the actuation electrode and the RF self-actuation force from the capacitance sensing electrode. The following equations are applied to the electro-mechanical model of the varactor in Figure 2.20, in order to calculate the n^{th}-iterated total force applied to the top membrane and the sense capacitance, respectively.

$$F_n = \left(C_{S0} \cdot \frac{g_{S0}}{g_{S0} - \Delta g_{n-1}} \right) \cdot \left(\frac{V_{RF\ n-1}{}^2}{2(g_{S0} - \Delta g_{n-1})} \right) + \left(C_{A0} \cdot \frac{g_{A0}}{g_{A0} - \Delta g_{n-1}} \right) \cdot \left(\frac{V_{DC}{}^2}{2(g_{A0} - \Delta g_{n-1})} \right) . \quad \text{(Equation 2.1)}$$

$$C_{Sn} = C_{S0} \cdot \frac{g_{S0}}{g_{S0} - \Delta g_n} = C_{S0} \cdot \frac{g_{S0}}{g_{S0} - (F_n / k)} . \quad \text{(Equation 2.2)}$$

where Δg_{n-1}, $V_{RF\ n-1}$, and V_{DC} is the change of air gap and the equivalent RF bias from the $(n-1)^{th}$ iteration, and the DC tuning bias, respectively.

Table 2.2. Parameters of the varactor used in non-linear simulations.

Symbol	*Description*	*Value*
C_{S0}	Initial capacitance in sensing node	200 fF
C_{A0}	Initial capacitance in actuation node	220 fF
g_{S0}	Initial air gap in sensing node	0.5μm
g_{A0}	Initial air gap in actuation node	2.0 μm
f_m	Mechanical resonant frequency	22 kHz
k	Spring constant	163 N/m
Q_M	Mechanical quality factor	1

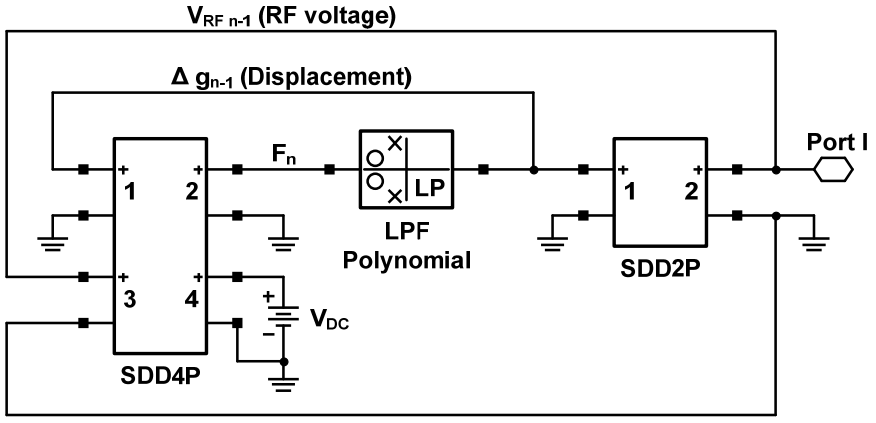
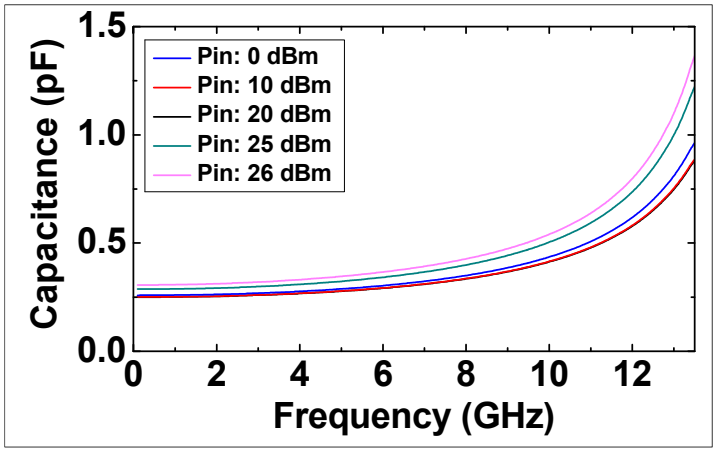
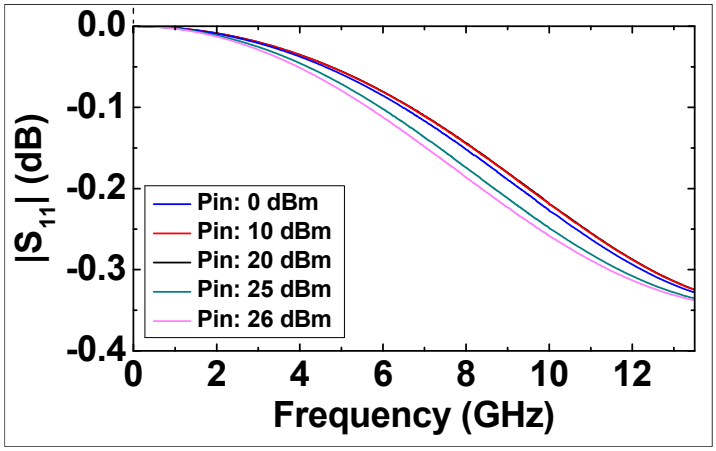


Figure 2.20. Schematic view of the non-linear electro-mechanical model for the varactor.



(a)

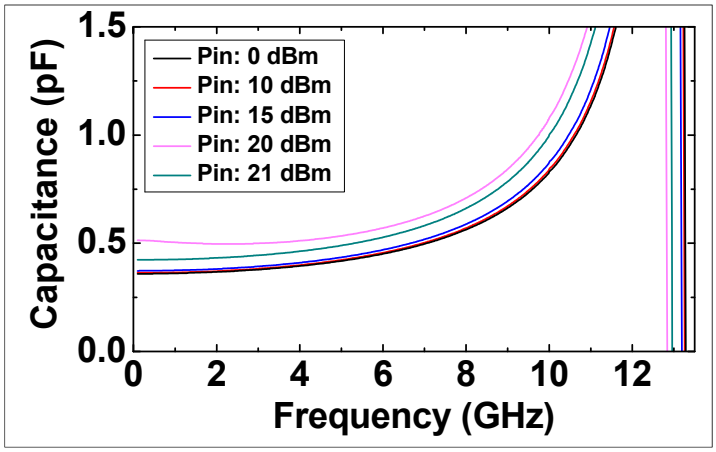


(b)

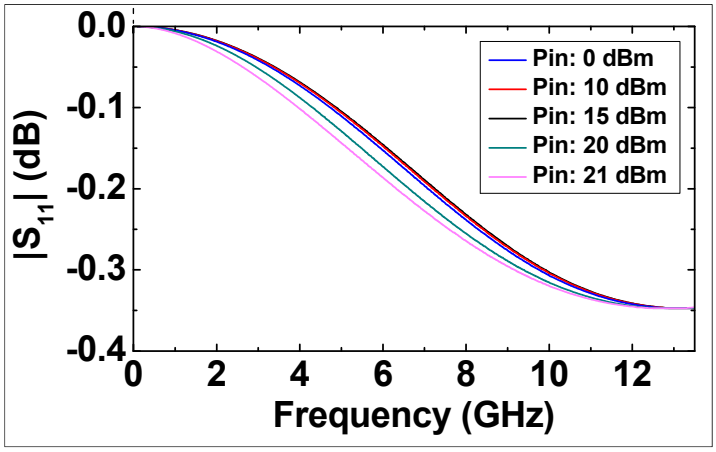
Figure 2.21. Simulated (a) capacitance and (b) S-parameters (S_{11}) at each RF power level when the varactor is at the initial state. The non-linear electro-mechanical model in Figure 2.20 is utilized for this simulation.

Using the non-linear model of the varactor in Figure 2.20, power handling capability of the varactor is simulated. Figure 2.21 shows the simulated capacitance and S_{11} at different input power levels when the varactor is at the initial state. The capacitance change is less than 10 % up to 25 dBm. However, the capacitance change is much more significant (~ 20%) when the power is increased above 25 dBm. When the varactor is tuned with 25 V of DC bias, less than 10 % of capacitance change is observed at 15 dBm

while 20 dBm of RF power results in more than 20 % of variation. Since the C-V curve has the sharpest slope at this point (see Figure 2.15), ~ 20 dBm of maximum power extracted from Figure 2.22 would be a pessimistic estimation of power handling capability when a DC bias is applied to the varactor.

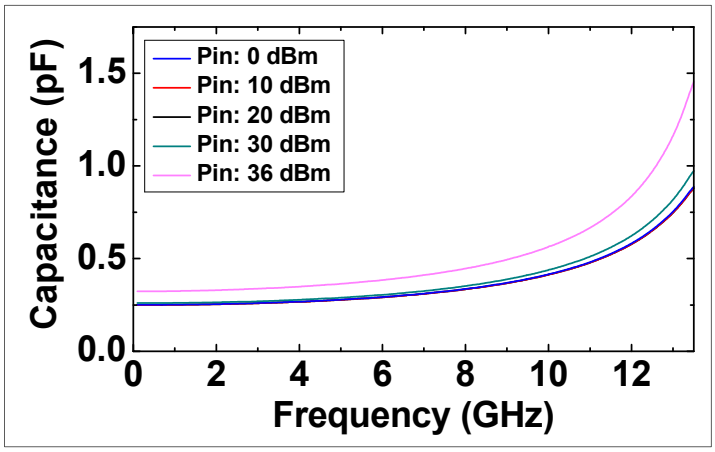


(a)

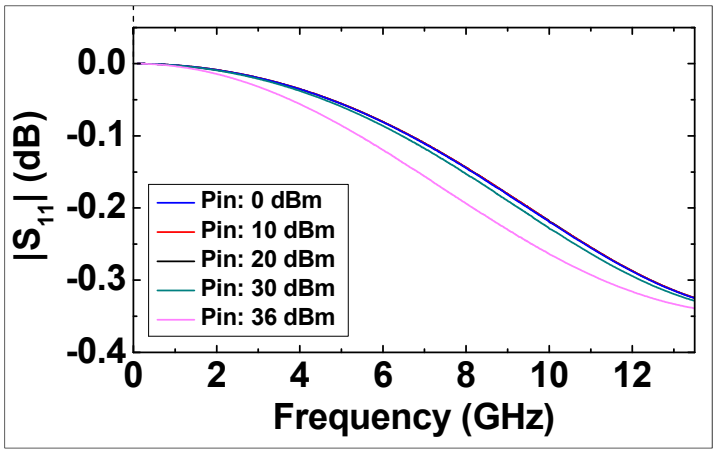


(b)

Figure 2.22. Simulated (a) capacitance and (b) S-parameters (S_{11}) at each RF power level when the varactor is tuned with 25 V of DC bias. The non-linear electro-mechanical model in Figure 2.20 is utilized for this simulation.



(a)



(b)

Figure 2.23. Simulated (a) capacitance and (b) S-parameters (S_{11}) at each RF power level when no DC bias is applied to the capacitive switch. The non-linear electro-mechanical model in Figure 2.20 is utilized for this simulation.

A similar analysis is also carried out using the capacitive switch model as shown in Figure 2.23. Since the capacitive switch only has ON and OFF states, the ON (initial) state is assumed with 1.5 μm of capacitance sensing gap for this simulation. As expected, the switch with larger capacitance sensing gap has less sensitivity to RF input signal, so it does not show significant change up to 36 dBm. Either increasing the stiffness of the

spring or increasing the actuation gap will enhance the power handling capability but at the cost of increased DC bias voltage for actuation. Therefore, while maintaining a similar DC bias level (or the actuation gap), adjusting capacitance sensing gap can provide either continuous tunability with lower power handling capability (varactor) or ON/OFF switching capability with better power handling capability (capacitive switch).

2.5. Discussion about Reliability and Tuning Control

Reliability and life cycles have been major concerns for RF MEMS switches or tunable capacitors, preventing their wide adoption in industry. Especially for MEMS varactors, mechanical degradation, dielectric charging, and temperature variation are the three main contributors to their relatively short life time. The problem with temperature sensitivity can be alleviated to some extent by a proper design for the springs and the membrane, as discussed earlier in this chapter. The dielectric charging issue can be reduced using contact-less and dielectric-less capacitive sensing [97]. However, tuning range of this type of varactors is greatly reduced at the same time since the maximum capacitance can be only three to four times larger than the initial capacitance. Instead of structural compensation, dielectric charging issue can also be mitigated by changing the polarity of the tuning bias or using more advanced circuits, which track the remaining charge and compensate for it (Figure 2.24 [98]).

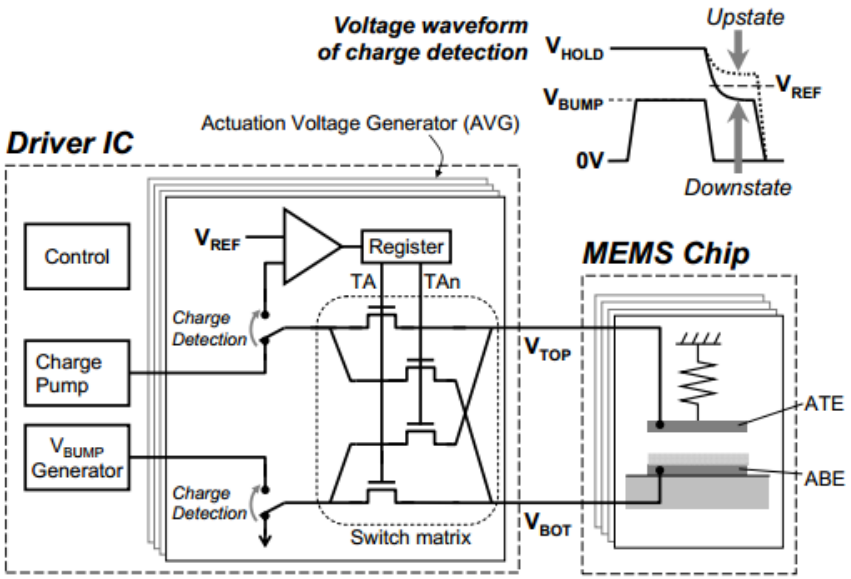
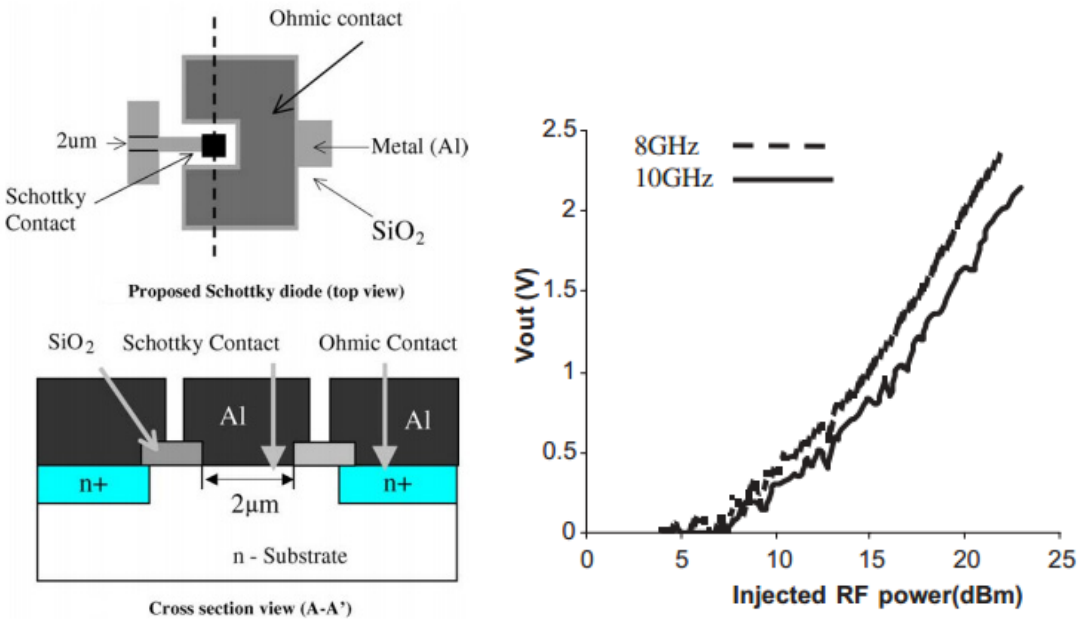


Figure 2.24. Block diagram of intelligent bipolar actuation circuit [98].



(a) (b)

Figure 2.25. (a) Schematic diagram of the Schottky diode; (b) Measured output voltage when power level is swept from 0 to 25 dBm at 8 and 10 GHz [99].

Using a similar technique, temperature variation or effect of high-power RF signal can be compensated by monitoring the capacitance value. These environmental effects will cause variations in the initial capacitance or the tuning bias required to achieve a specific capacitance value. The problem with this approach is that the control circuit gets more complicated as the number of varactors increases. Another indirect compensation method will be utilizing on-chip sensors such as power detectors (Figure 2.25 [99]) or temperature sensors (Figure 2.26 [100]) to monitor global change of environment and compensate it using a programmed lookup table. This lookup table should have pre-defined tuning bias conditions for each power and temperature condition. The varactor control circuits providing good reliability and sufficient repeatability will be one of the major future research topics in this area.

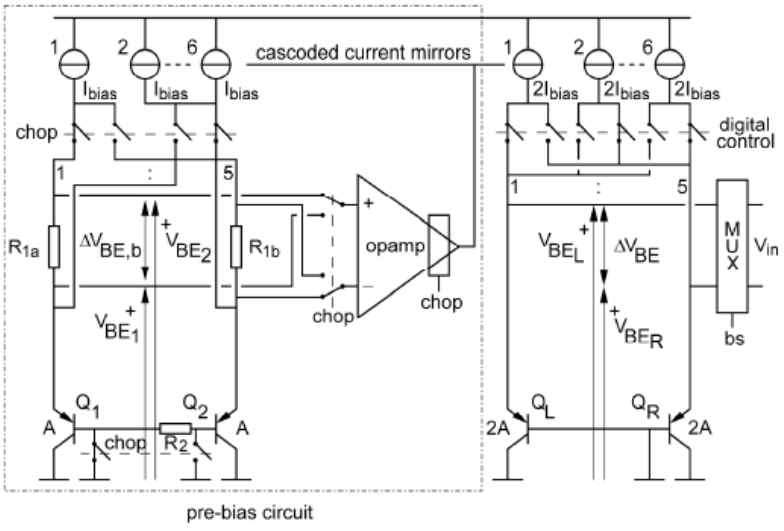


Figure 2.26. Circuit diagram of the sensor front-end, included in the integrated CMOS temperature sensor [100].

CHAPTER 3.

HIGH-PERFORMANCE CONTINUOUSLY TUNABLE MEMS BANDPASS FILTER

With the introduction of joint tactical radio as the next generation system in the U.S. military, ground mobile radios have to support various waveforms including VHF and UHF bands, requiring reconfigurable RF front-ends. As the key component of the RF front-end, the band-select filter needs to satisfy multiple frequency band coverage and good RF performance, all in a small form factor. This calls for a single fully-integrated frequency-tunable bandpass filter. As discussed earlier, there are only a few reports on tunable bandpass filters having all integrated components centered at frequencies below 1 GHz [69], [68]. The reported filters are designed in the second-order coupled resonator configuration. Because of the low order of the filter, the shape factor and out-of-band rejection of these filters were limited. In this chapter, a continuously tunable MEMS bandpass filter using a third-order coupled resonator configuration is presented. Using continuous tuning, the frequency of the filter can be tuned to select any desired frequency in the tunable frequency range or altered to account for fabrication inaccuracies. Continuous tuning is achieved using MEMS tunable capacitors presented in Chapter 2,

which exhibit high *Q*s (exceeding 100), fast tuning speed (less than 80 μs), wide capacitance tuning range (5:1), and good temperature stability.

The two-port capacitors are commonly used for matching or as the coupling elements in coupled resonator filters [86]. Using capacitive matching and coupling, it is hard to maintain a fixed bandwidth without tuning the value of the coupling capacitors. In this work, mutually coupled inductors and inductive matching are utilized to provide a wider band matching and avoid complicated tuning control. Using broad-band inductive matching and wide-range capacitive tuning in the resonator, a tunable filter is demonstrated with insertion loss of less than 4 dB and tuning range of 40%.

This chapter is organized in the following order. First, the design and tuning configuration of the filter are discussed. Next, the design of each passive component and their 3D electromagnetic simulation results are shown. The linearity analysis for IIP_3 is also described. Finally, the measurement and characterization results of the fabricated filter are presented.

3.1. Design

The target specifications of the pre-select tunable filter are listed in Table 3.1. The filter is aimed to achieve frequency coverage from 600 MHz to 1 GHz with 3dB percentage bandwidth of 13-14 %. The insertion loss of the filter is targeted to be less than 4 dB to achieve a small noise figure for the entire radio. To obtain a shape factor of

less than four, the order of the filter needs to be more than three [101]. A third-order Chebyshev filter with a 0.5 dB passband ripple is selected to achieve the desired shape factor. Using this configuration, the group delay is less than 10 ns, meeting all the specifications listed in Table 3.1.

The filter design procedure is as following. First, the lowpass prototype in Chebychev configuration is designed. The lowpass prototype values (g_1, g_2, g_3, g_4) of the third-order Chebyshev filter used here are 1.5963, 1.0967, 1.5963, 1.0000, respectively. The lowpass filter is then converted to a coupled resonator bandpass filter configuration using admittance inverters as shown in Figure 3.1 (a). With this configuration, values of the lumped components are easily realizable using MEMS surface micromachining technologies, such as the one shown in Figure 2.11.

Table 3.1. Target specifications of the tunable filter.

Filter Characteristics	**Target**
Center frequency range	600 MHz ~ 1000 MHz
Insertion loss	< 4 dB at ω_c
3dB-Bandwidth (BW_{3dB})	12 ~ 16 % of ω_c
Shape factor (BW_{30dB} / BW_{3dB})	< 4
Passband ripple	< 0.5 dB
Out-of-band rejection	> 40 dB
Group delay	< 10 ns
Impedance	50 Ω
IIP3	> 20 dBm
Tuning voltage	< 50 V
Tuning speed	< 100 μs
Temperature variation (ω_c)	< 5 %
Dimensions	< 1.5 × 1.5 cm^2

The parameters of the admittance inverters are derived using the following set of equations [102].

$$J_{01} = J_{34} = \frac{1}{2\pi f_c} \cdot \frac{1}{\sqrt{g_0 g_1 G_A L_{R1}}} \text{ , and} \qquad \text{(Equation 3.1)}$$

$$J_{12} = J_{23} = \frac{1}{2\pi f_c} \cdot \frac{BW_{3dB}}{f_c} \cdot \frac{1}{\sqrt{g_1 g_2 L_{R1} L_{R2}}} \text{ ,} \qquad \text{(Equation 3.2)}$$

where f_c is the center frequency of the bandpass filter at initial state, G_A is the input impedance, and $L_{R1,}$ L_{R2} are inductor values in each LC tank. To ease the characterization and tuning scheme, the initial value of all three capacitors (C_{R1}, C_{R2}, C_{R3}) are set to be the same. An initial value of 2.3 pF is chosen for the tunable capacitors, considering that the inductance value needs to be in the range of 1 nH to 15 nH to provide a high Q of more than 40. Using these values for the capacitors, the required inductance value for $L_{R1,}$ $L_{R2,}$ L_{R3} is 11 nH and the unloaded Q_0 of each resonator would be about 40. As shown in Figure 3.1 (b), the admittance inverter is implemented using inductive coupling with L_{12} = L_{23} = $1/(2\pi f_c J_{12})$. Values of L_{01} and L_{34} are not set at this step as they also depend on the matching condition. As shown in Figure 3.1 (c), L_1 can be approximated as L_{R1}//(-L_{12}). L_2 is split into both sides of the second resonator and converted into mutual inductive coupling; the value of L_2 is set to be equal to $2 \times L_{R2}$//(-L_{12})//(-L_{23}).

The inductive network of Figure 3.1 (c) is converted into mutually coupled inductors, as shown in Figure 3.1 (d). The matching inductance (L_M) is derived

considering the values assumed for g_1 and g_4, and the loaded Q_n of the resonator, as shown in Figure 3.1 (d). The mutual inductance (M) and resonator inductances (L_{C1}', L_{C2}') are

$$M = \frac{L_1 L_2}{L_1 + L_2 + L_K}, \qquad \text{(Equation 3.3)}$$

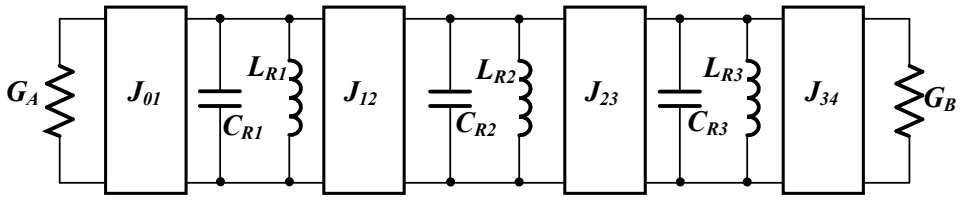
$$L_{C1}' = \frac{L_1(L_K + L_2)}{L_1 + L_2 + L_K}, \; L_{C2}' = \frac{L_2(L_K + L_1)}{L_1 + L_2 + L_K}. \qquad \text{(Equation 3.4)}$$

To obtain the effective impedance of g_1 and g_4 at input and output nodes and impedance matching to 50 Ω, impedance transformation using two inductors (L_{C1}, L_M) is obtained using the following expressions

$$L_{C1} = \frac{L_M L_{C1}' R_S}{R_S(L_M - L_{C1}') + R_T L_{C1}'}, \; L_M = \frac{\sqrt{R_S R_T}}{2\pi f_c}, \qquad \text{(Equation 3.5)}$$

$$L_{C2} \approx L_{C2}', \quad R_S = \frac{2\pi f_c \cdot L_{R1} Q_0 \cdot L_{R1} Q_n}{L_{R1} Q_0 - L_{R1} Q_n}. \qquad \text{(Equation 3.6)}$$

where R_T is the target input impedance (50 Ω) and R_S is the input impedance looking into the resonator. The extracted design values from the above equations are summarized in Table 3.2.



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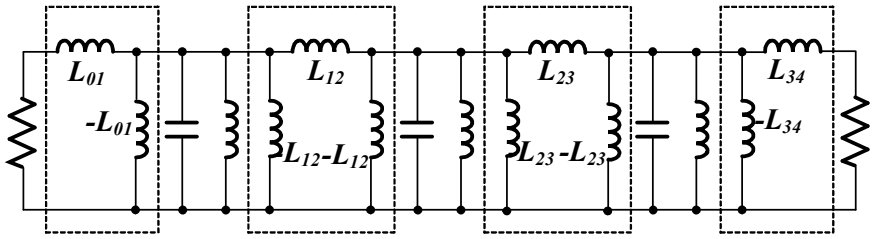

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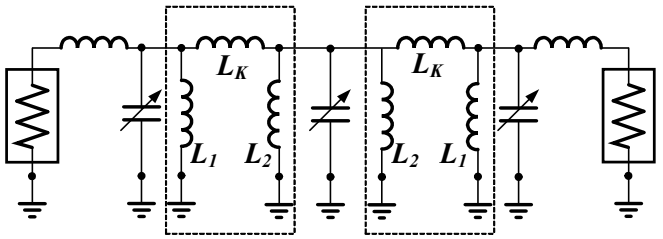
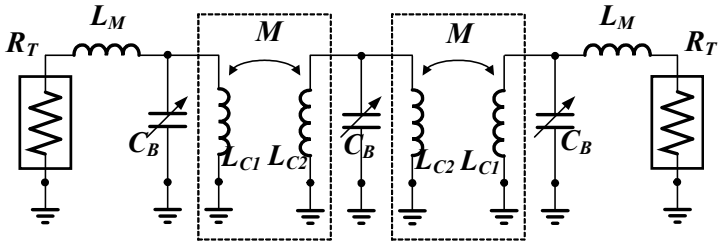


(c)



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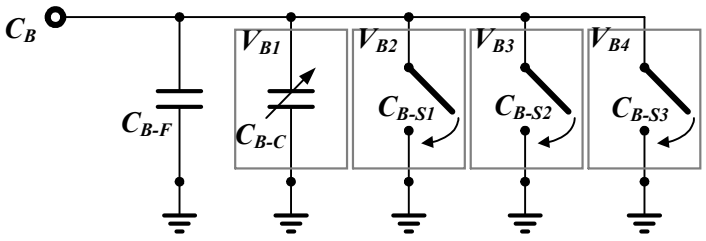


(e)

Figure 3.1. Schematic views showing the design procedure of the third-order bandpass filter in this work; (a) generalized bandpass filter using admittance inverter (b) conversion into inductive coupling (c) arrangement of inductance for mutual-inductive coupling (d) the final schematic view of the filter. Detail composition of the tunable bank included in each resonator (e).

Table 3.1. Tuning configuration of the filter.

Tuning Controls	Capacitance (C_B)	Center Frequency (f_C)
V_{B1} = 0-40 V	2.3-3.5 pF	811-1000 MHz
V_{B1} = 0-40 V V_{B2} = 40 V	3.4-4.6 pF	707-824 MHz
V_{B1} = 0-40 V V_{B2} , V_{B3} = 40 V	4.5-5.7 pF	635-715 MHz
V_{B1} = 0-40 V V_{B2} , V_{B3} , V_{B3} = 40 V	5.6-6.8 pF	582-640 MHz

Table 3.2. Design values of the proposed filter.

Symbol	Description	Value
J_{01}, J_{34}	Admittance inverter parameters	8.49×10^{-6}
J_{12}, J_{23}	Admittance inverter parameters	1.75×10^{-3}
L_1	Inductively coupled inductor 1	12.5 nH
L_2	Inductively coupled inductor 2	29.0 nH
L_K	Coupling inductor	90.9 nH
L_M	Matching inductor	32.0 nH
L_{C1}	Mutually coupled inductor 1	16.4 nH
L_{C2}	Mutually coupled inductor 2	22.6 nH
M	Mutual inductance	3.2 nH
R_T	Target Input / Output Impedance	50
C_B	Tunable capacitor bank (TCB)	2.3 pF ~ 6.8 pF
$C_{B\text{-}F}$	Fixed capacitor in TCB	1.5 pF
$C_{B\text{-}C}$	Continuous capacitor in TCB	0.2 pF ~ 1.4 pF
$C_{B\text{-}S}$	Switched capacitor in TCB	0.2 pF ~ 1.3 pF

To achieve frequency tuning, a tunable capacitor bank is employed in each resonator section which consists of one fixed capacitor (MIM capacitor), one continuously-tunable capacitor, and three capacitive switches. The tuning control is as following. First the continuously tunable capacitor is tuned. When this capacitor reaches its maximum value, a switch will be turned ON and the value of the continuously tunable capacitor will be reset to set the frequency as required. To further tune the center frequency, again the continuously tunable capacitor will be tuned to finally reach its maximum value. At this

state, another switch will be turned on. Therefore, to achieve continuous tuning, only one continuously tunable capacitor is required. Other capacitors are switched type to ease the tuning control. The initial capacitance value of all tunable capacitors is set to 200 fF with a tuning speed of less than 100 μs including the stabilization time.

The simulation result from the lumped circuit design reflecting the limited Q of each passive element is shown in Figure 3.2. Tuned State I indicates one set of tunable capacitors is completely tuned while Tuned State IV means all of capacitors are completely tuned. The detail filter specifications in each tuned state are summarized in Table 3.3. As shown, the filter satisfies all requirements including 3dB-bandwidth (BW_{3dB}) of 14 to 15 %, insertion loss of less than 4.0 dB and group delay of less than 10 ns at each tuned state.

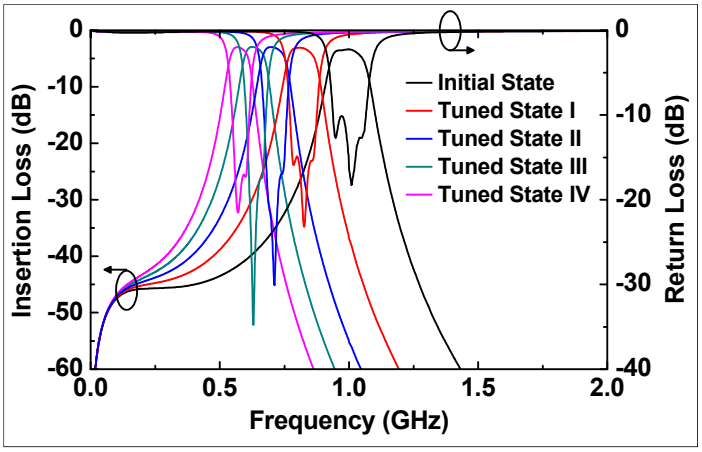


Figure 3.2. Simulated insertion loss and return loss of the third-order tunable bandpass filter at each tuned stage, based on the schematic view in Fig. 3.1 (d).

Table 3.3. Simulated filter specifications from 3D EM model.

Tuned Capacitors	Insertion Loss	3dB Bandwidth	Shape Factor	Group Delay
Initial State	3.4 dB @ 1000 MHz	143 MHz (14.3 %)	3.2	< 7 ns
Tuned State I	3.2 dB @ 824 MHz	118 MHz (14.3 %)	3.3	< 8 ns
Tuned State II	3.1 dB @ 715 MHz	102 MHz (14.3 %)	3.5	< 9 ns
Tuned State III	3.1 dB @ 640 MHz	91 MHz (14.2 %)	3.6	< 10 ns
Tuned State IV	3.2 dB @ 582 MHz	84 MHz (14.4 %)	3.7	< 10 ns

3.2. 3-D Electromagnetic Simulation

Filters are designed and fabricated using a multiple-metal surface micromachining process technique presented in Chapter 2. The performance of individual passive components as well as the tunable filter is simulated using the ANSOFT HFSS 3D electromagnetic simulation tool [85]. The material properties such as conductivity, dielectric constant, and loss tangent are characterized and the extracted values from measurements are used in simulations.

The integrated filter layout is shown in Figure 3.3. The length of the RF interconnecting lines is minimized and the ground connections are optimally placed to reduce loss and parasitics. The bias lines of the three tunable capacitors in each resonator tank are connected together. Also, one bias line controls all corresponding capacitive switches. Therefore, only one analog bias line and three digital (0 V / 40 V) bias lines are needed to tune the filter (instead of 12 control lines). The HFSS simulated insertion loss,

return loss, and group delay of the integrated filter at each tuned stage are shown in Figure 3.4. The group delay in Figure 3.4 (c) is derived from the formula suggested in [19]. The simulated RF performance of the filter is summarized in Table 3.4. As shown, the bandwidth of the filter is designed to be slightly wider than the specified bandwidth in Table 3.1. This is due to the fact that HFSS over-estimates the coupling between the inductors and thus the HFSS simulated bandwidth is wider that that achievable in fabrication. Measurements on stand-alone mutual inductor pairs have shown that the coupling constant is over-estimated by about 25% in HFSS, resulting in ~3% wider 3dB bandwidths at all tuned states in Table 3.4. The measured percentage bandwidth using this design is expected to fall within the specified range of 12-16%.

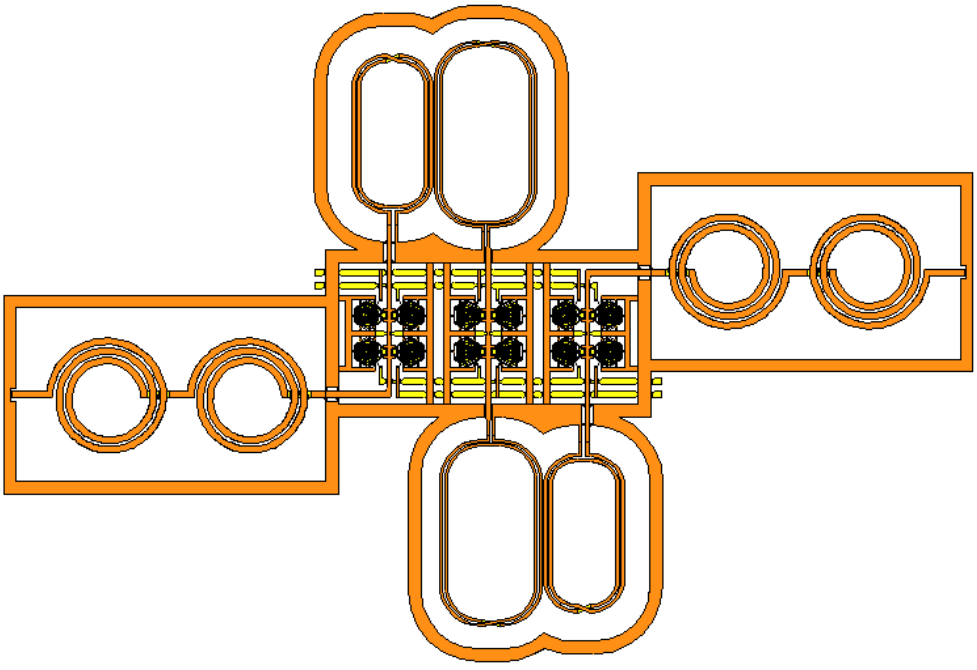
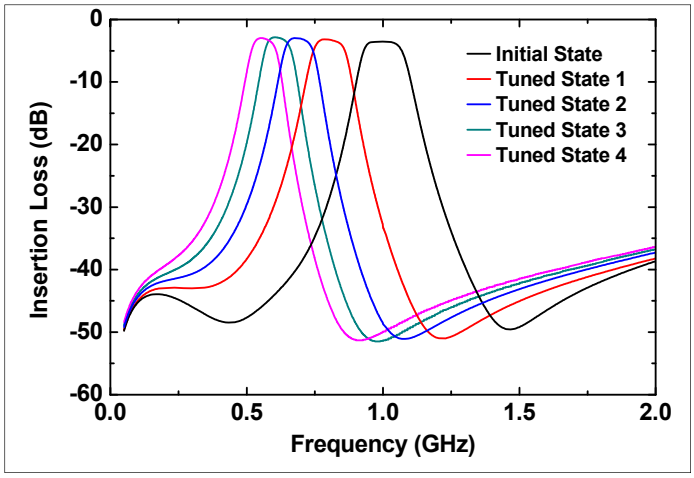
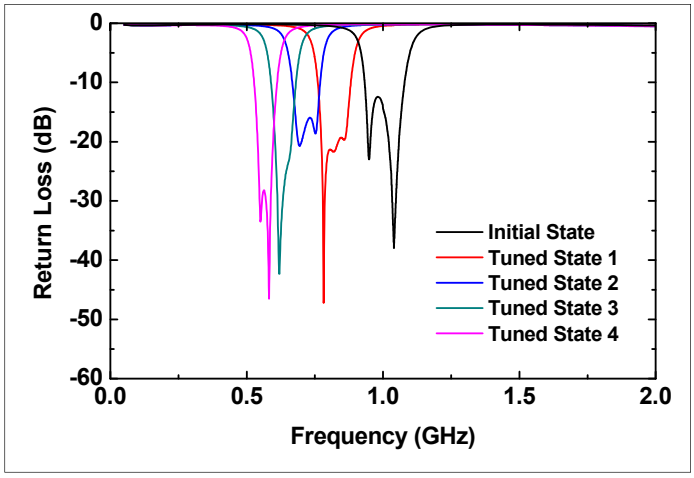


Figure 3.3. Layout of the MEMS tunable filter.



(a)



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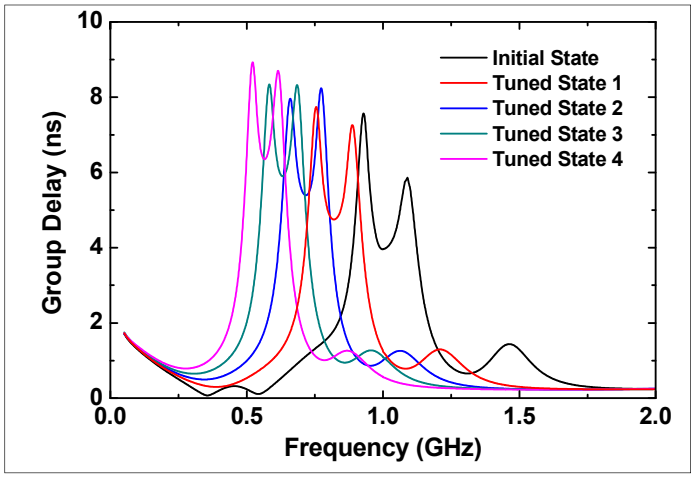


(c)

Figure 3.4. Simulation results of the MEMS filter. (a) Insertion loss; (b) return loss; (c) group delay.

Table 3.4. Simulated filter specifications using HFSS 3D EM tool.

Tuned Capacitors	Insertion Loss	3dB Bandwidth	Shape Factor	Group Delay
No tuning	3.5 dB @ 1010 MHz	172 MHz (17.0 %)	2.9	< 8.0 ns
Tuning_1	2.9 dB @ 817 MHz	141 MHz (17.3 %)	3.2	< 8.0 ns
Tuning_2	3.1 dB @ 719 MHz	123 MHz (17.1 %)	3.4	< 8.5 ns
Tuning_3	3.2 dB @ 638 MHz	111 MHz (17.4 %)	3.6	< 9.0 ns
Tuning_4	3.2 dB @ 573 MHz	102 MHz (17.8 %)	3.7	< 9.0 ns

3.3. Linearity Analysis

IIP_3 is a commonly used specification to indicate linearity and power handling capability of RF systems. The effect of nonlinearities in RF system is estimated with the following assumptions: Using a two-tone signal, the input signal can be expressed as

$$x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t. \quad \text{(Equation 3.7)}$$

The output of non-linear RF-system is assumed as

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots, \quad \text{(Equation 3.8)}$$

If the input signal in Equation 3.7 is inserted,

$$y(t) \approx \alpha_1 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) + \alpha_2 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^2 + \alpha_3 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^3 (t) + \cdots. \quad \text{(Equation 3.9)}$$

The output signal located at the fundamental frequency is

$$\omega = \omega_1, \omega_2 : \left(\alpha_1 A_1 + \frac{3}{4}\alpha_3 {A_1}^3 + \frac{3}{2}\alpha_3 A_1 {A_2}^2\right) \cos \omega_1 t + \left(\alpha_1 A_1 + \frac{3}{4}\alpha_3 {A_1}^3 + \frac{3}{2}\alpha_3 A_1 {A_2}^2\right) \cos \omega_1 t \quad \text{(Equation 3.10)}$$

For $A_1 \ll A_2$,

$$y(t) = \left(\alpha_1 + \frac{3}{2}\alpha_3 {A_2}^2\right) A_1 \cos\omega_1 t + \cdots \quad \text{(Equation 3.11)}$$

If $A_1 \cos\omega_1 t$ is the target RF signal, the weak signal (small A_1) may vanish if $\alpha_3 < 0$ and the gain drops to zero with sufficiently large A_2. This $A_2 \cos\omega_2 t$ is called blocking signal, and this effect is called desensitization or blocking effect.

The second and third order intermodulation harmonics are obtained as

$$\omega = \omega_1 \pm \omega_2 : \alpha_2 A_1 A_2 \cos(\omega_1 + \omega_2)t + \alpha_2 A_1 A_2 \cos(\omega_1 - \omega_2)t \text{ (Equation 3.12)}$$

$$\omega = 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 {A_1}^2 A_2}{4}\cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 {A_1}^2 A_2}{4}\cos(2\omega_1 - \omega_2)t \quad \text{(Equation 3.13)}$$

$$\omega = 2\omega_2 \pm \omega_1 : \frac{3\alpha_3 {A_2}^2 A_1}{4}\cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 {A_2}^2 A_1}{4}\cos(2\omega_2 - \omega_1)t. \quad \text{(Equation 3.14)}$$

If $\omega_1 \approx \omega_2$ and $A_1 \approx A_2 = A$, the output level at the fundamental frequency and third harmonic term have the same amplitude.

$$|\alpha_1|A + \frac{9}{4}|\alpha_3|A^2 = \frac{3}{4}|\alpha_3|A^3 \quad \text{(Equation 3.15)}$$

If $|\alpha_1|A \gg \frac{9}{4}|\alpha_3|A^2$, the input referred third-order intermodulation is

$$IIP_3 = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}. \quad \text{(Equation 3.16)}$$

To analyze the non-linear performance (IIP_3) of the filters, non-linearity of the varactor and the capacitive switches are taken into account using the non-linear electro-mechanical models provided in Chapter 2.

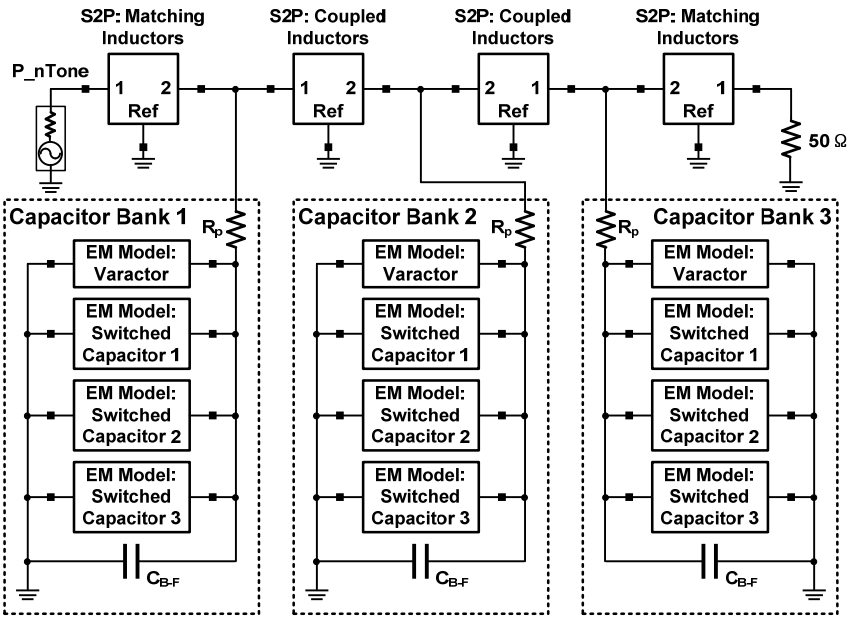


Figure 3.5. Schematic view of the non-linear electro-mechanical model for (a) the varactor, and (b) the entire filter.

The schematic including the filter configuration and non-linear models of the varactors and the capacitive switches is shown in Figure 3.5. The initial air-gap at the sensing node of the capacitive switch is set as 1.5 μm while the varactor is set as 0.5 μm. Figure 3.6 shows the harmonic simulation result at different input power levels. The frequency difference of the two input tones is 10 kHz. The extracted IIP_3 value is 30 dBm when no DC bias is applied to the varactors/switches. With the application of 25 V DC bias, the IIP_3 is reduced to 20 dBm. At this bias point, the capacitance value of varactors is most sensitive to the applied RF power as the C-V curve has the sharpest slope at this point (see inset of Figure 3.7). Therefore, 20 dBm is a pessimistic estimation of IIP_3 when a DC bias is applied. The extracted IIP_3 at different input frequency offset is shown in Figure 3.7. At both initial and tuned states, the IIP_3 value is better for larger

frequency offsets. This is due to the lowpass filtering behavior of the MEMS capacitors, which is taken into account in the non-linear electro-mechanical model of Figure 3.5 (a) by considering a cut-off frequency of 22 kHz (the mechanical resonant frequency (f_m) of the tunable capacitor). A similar trend is expected in the measured IIP_3.

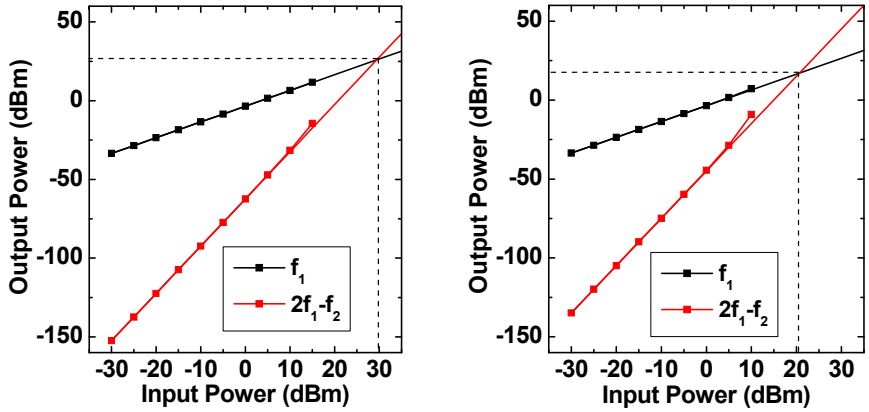


Figure 3.6. IIP_3 value extracted from the non-linear electro-mechanical model at frequency offset of 20 kHz (a) without DC bias (b) with 25 V of DC bias.

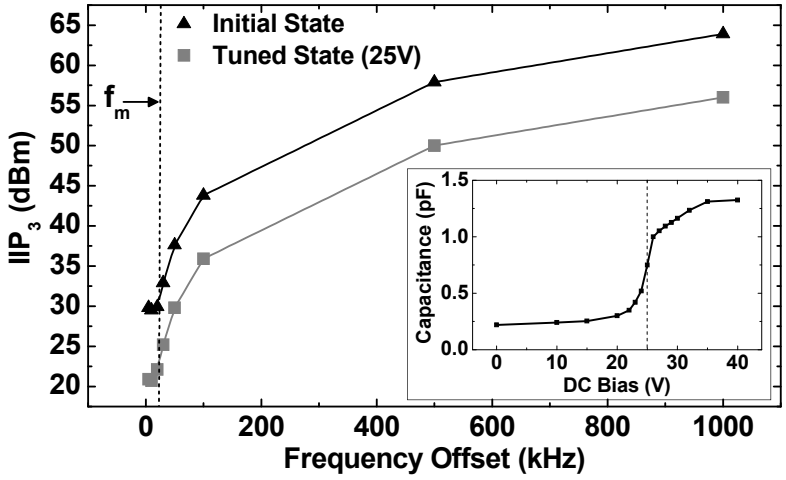


Figure 3.7. IIP_3 value extracted from the non-linear electro-mechanical model at different frequency offsets with and without DC bias. Tuning characteristics of the tunable capacitor is shown in the inset.

3.4. Measurement Result - Tunable Capacitor Bank

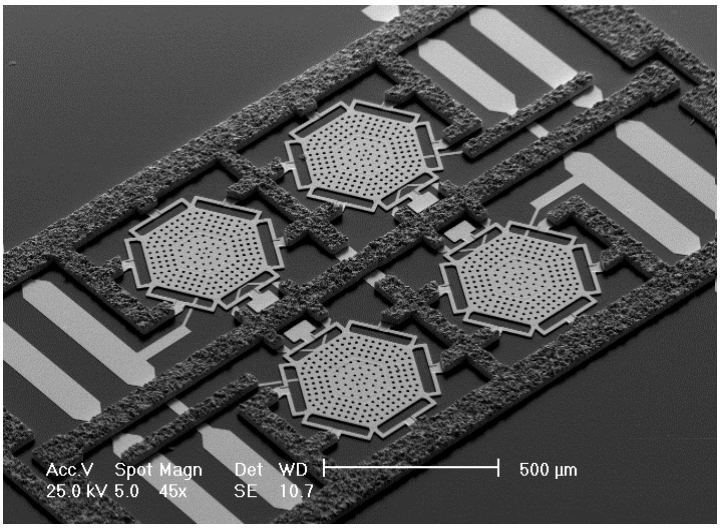


Figure 3.8. A SEM view of the fabricated tunable capacitor array.

To better understand the tuning characteristic of the filter, a sand-alone tunable capacitor bank (*i.e.* the tunable component of the filter) is also fabricated and measured. Figure 3.8 shows a SEM view of a fabricated tunable capacitor array. It consists of one varactor and three switched capacitors.

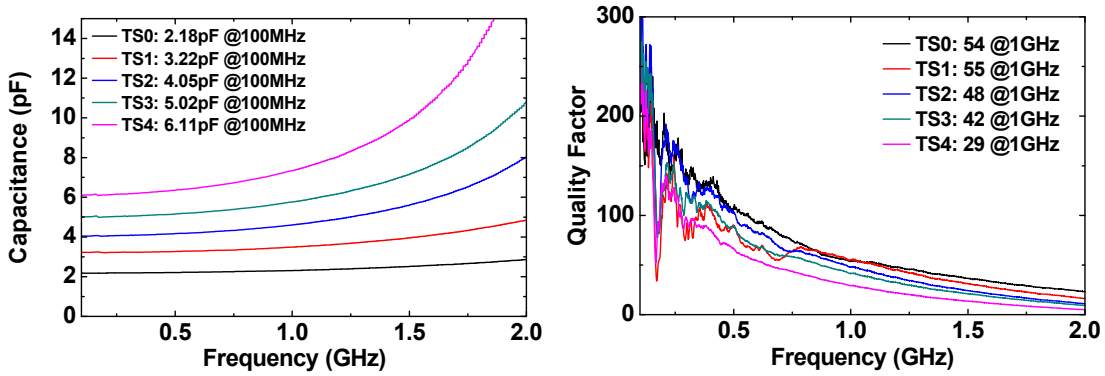


Figure 3.9. Measured capacitance (left) and *Q* of the tunable capacitor array (right).

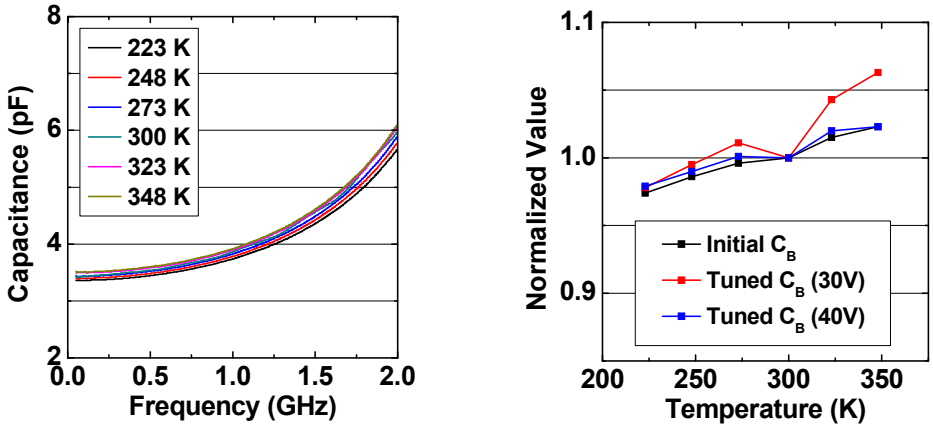


Figure 3.10. Temperature variation measurements of the tunable capacitor bank; measured capacitance under 40 V of DC bias (left); normalized value of the initial and tuned capacitance with 30 V and 40 V of DC bias (right).

The measured tuning range is from 2.2 pF to 6.1 pF (Figure 3.9), which is smaller than the simulated value. As described before, the membrane deformation and rough surfaces are the reasons for this discrepancy. The measured Q is also smaller than the simulated value. This is due to the lower conductivity of electroplated metals and higher dielectric loss of aluminum oxide compared to the values considered in the simulations. The temperature variation is performed at the different tuning state of the tunable capacitor bank (Figure 3.10). Compared to the initial and final tuned states of the varactor, the intermediate tuned state at DC bias of 30 V shows more temperature sensitivity of up to 8.5 % over temperature range of 223 K to 348 K.

3.5. Measurement Result - Tunable Filter

The frequency response of the filter is measured using Cascade Microtech GSG ACP probes and N5214A Agilent PNA-X network analyzer. The DC bias is applied to each

bias line using Microtech DC probes. The SEM and photo views of fabricated device are shown in Figure 3.11. The foot-print of the entire filter is around 1.5 cm × 1.0 cm, which is much smaller than other high-performance UHF filters that use micro striplines and SMT passives discussed earlier in Chapter 1 [78], [79], [81].

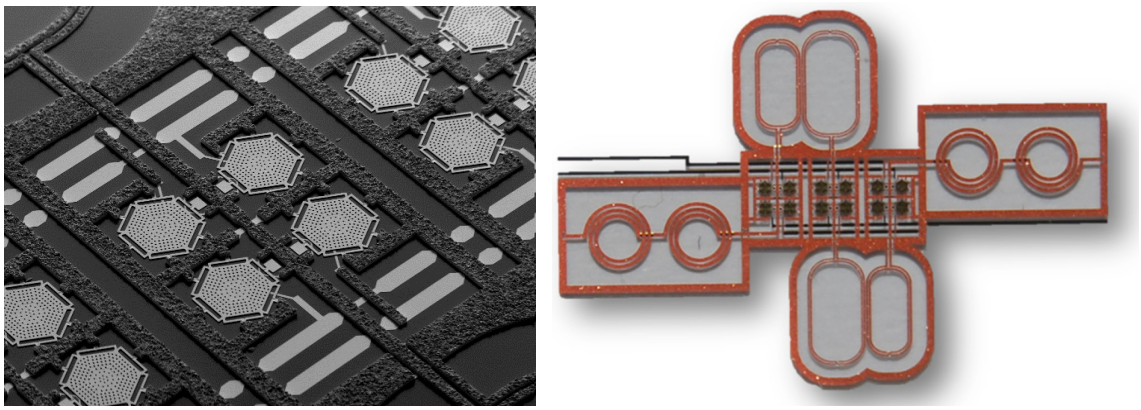
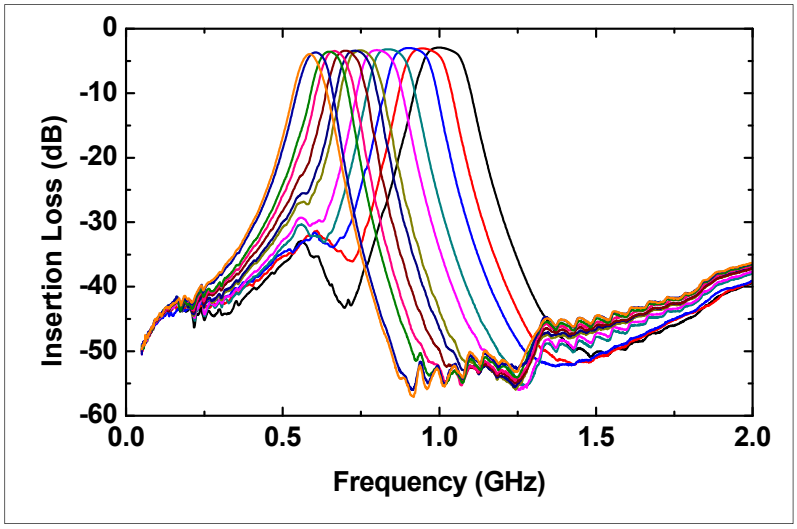


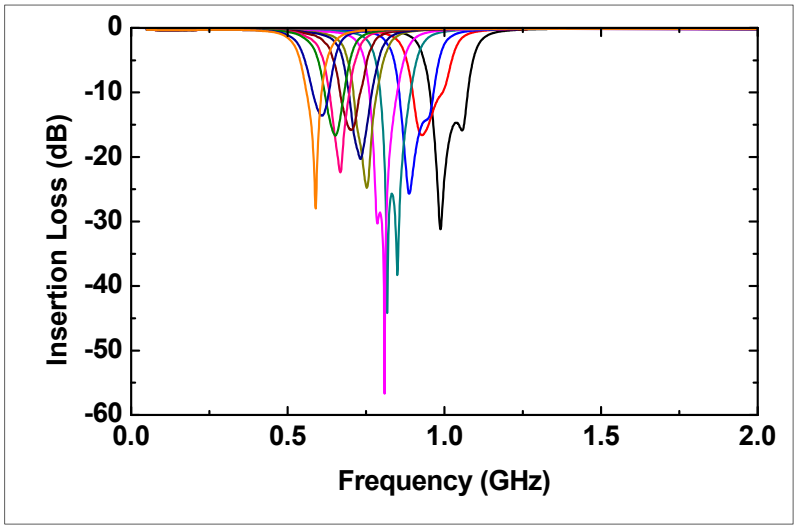
Figure 3.11. A SEM view (left) and a photo image (right) of fabricated filter.

Figure 3.12 shows the measured insertion loss and return loss at each tuned state when DC bias of 0 to 40 V is applied to the varactors and switched capacitors. The center frequency is tuned from an initial value of 1011 MHz to 602 MHz by applying a maximum of 40 V to the capacitors. Across the entire tuning range, the insertion loss is better than 4 dB and the return loss is better than 15 dB. The measurement results are summarized in Table 3.5. The 3dB-bandwidth shows good agreement with the electromagnetic simulation. However, the measured shape factor at most tuned states is slightly above four. This is caused by an unwanted resonance located at the lower side of

pass bands. This resonance is presumably due to the coupling between the substrate (*i.e.* 500 μm thick) and the inductors and can be reduced by increasing the thickness of the substrate.



(a)



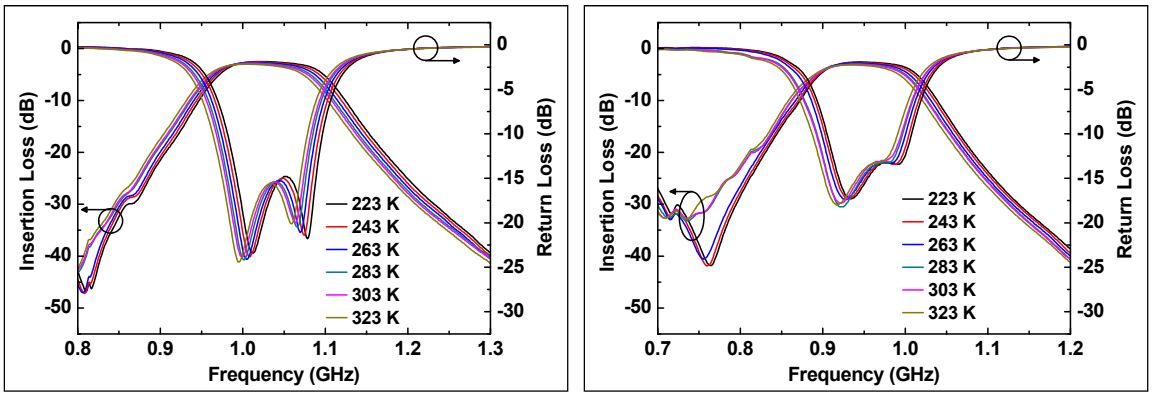
(b)

Figure 3.12. Measured filter response at each tuned stage; (a) insertion loss, and (b) return loss.

Table 3.5. Measured filter specifications at each tuned stage.

Tuned Capacitors	Insertion Loss	3dB Bandwidth	Shape Factor	Group Delay
No tuning	3.0 dB @ 1011 MHz	135 MHz (13.4 %)	3.2	< 7 ns
Tuning_1	3.3 dB @ 833 MHz	113 MHz (13.6 %)	4.5	< 8 ns
Tuning_2	3.4 dB @ 735 MHz	99 MHz (13.5 %)	4.6	< 9 ns
Tuning_3	3.6 dB @ 650 MHz	87 MHz (13.4%)	4.7	< 9 ns
Tuning_4	3.6 dB @ 602 MHz	81 MHz (13.5 %)	4.7	< 8 ns

Temperature stability of the filter is tested using Microtech KV-230 cryogenic station and GGB RF probes. SOLT calibration is done at each temperature. Figure 3.13 (a) shows the filter response from -50°C to 50 °C when no DC bias is applied. The center frequency of the filter is shifted from 1035 MHz to 1016 MHz, showing a variation of less than 2%. The frequency response of the filter when a DC bias is applied to one of the capacitors is shown in Figure 3.13 (b). Upon temperature change, the center frequency is shifted by 1.5% from 955 MHz to 941 MHz, which is considered small for a MEMS device [88], [103]. The temperature stability of the filter is better than the temperature shift of the varactor itself. As demonstrated in the previous chapter, the capacitance variation of individual varactors is less than 7 % over the same temperature range. Since the varactor is placed in parallel with a more temperature stable fixed capacitor, the temperature instability of the filter is improved at the initial state as well as tuned state of the varactors.



(a) (b)

Figure 3.13. Measured filter response at different temperatures; (a) at initial state; (b) when a DC bias of 25 V is applied to $C_{B\text{-}C}$.

The group delay of the filter at each tuned state is extracted from the measured S-parameters. As shown in Figure 3.14, the group delay at all tuned states is less than 10 ns, meeting the design requirement.

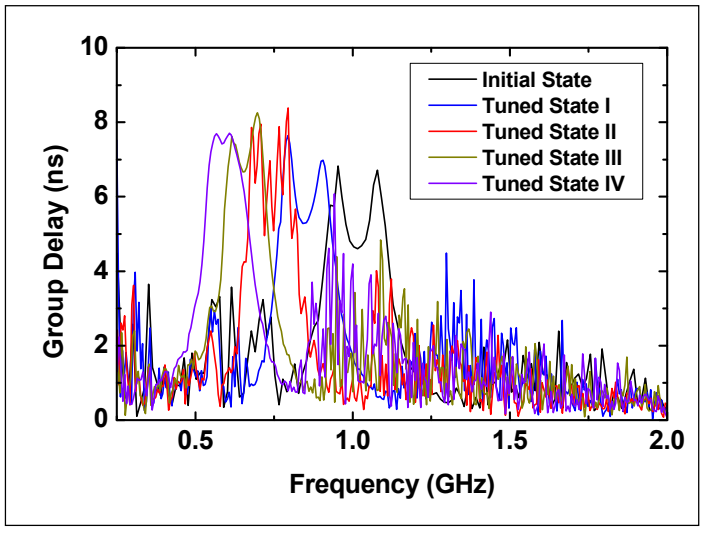


Figure 3.14. Measured group delay at each tuned stage.

The IIP_3 measurements are carried out using N5214A Agilent PNA-X network analyzer with two-tone source power mode. The harmonic measurement without DC

bias is shown in Figure 3.15. Figure 3.15 (a) shows output power spectrum when 4dBm of input power and 20 kHz of frequency offset is applied. The extracted IIP_3 at 20 kHz of frequency offset is around 20 dBm, as shown in Figure 3.15 (b). A larger frequency offset results in better IIP_3 values, as expected. As shown in Figure 3.15 (d), the extracted IIP_3 at a frequency offset of 500 kHz is about 35 dBm. When DC bias is applied to tunable capacitors, IIP_3 degrades as the smaller capacitance gap becomes more sensitive to the RF signal power. Figure 3.16 (a)-(d) show the linearity measurements when 25 V of DC bias is applied to the varactor. As shown, the IIP_3 value is the smallest at 20 kHz of frequency offset, which is simulated to be the mechanical resonance frequency of the varactor membrane. The measured IIP_3 value when no DC bias is applied is smaller than the simulated value (compare Figure 3.15 (a)-(d) to Figure 3.9). This is expected as at this state, the power level of the harmonics should be below -100 dBm. Since the noise floor of the PNA-X network analyzer is around the same value, the output power level could not be accurately measured. At 25 V of DC bias, measurements are in good agreement with simulations, validating the accuracy of the measurement method.

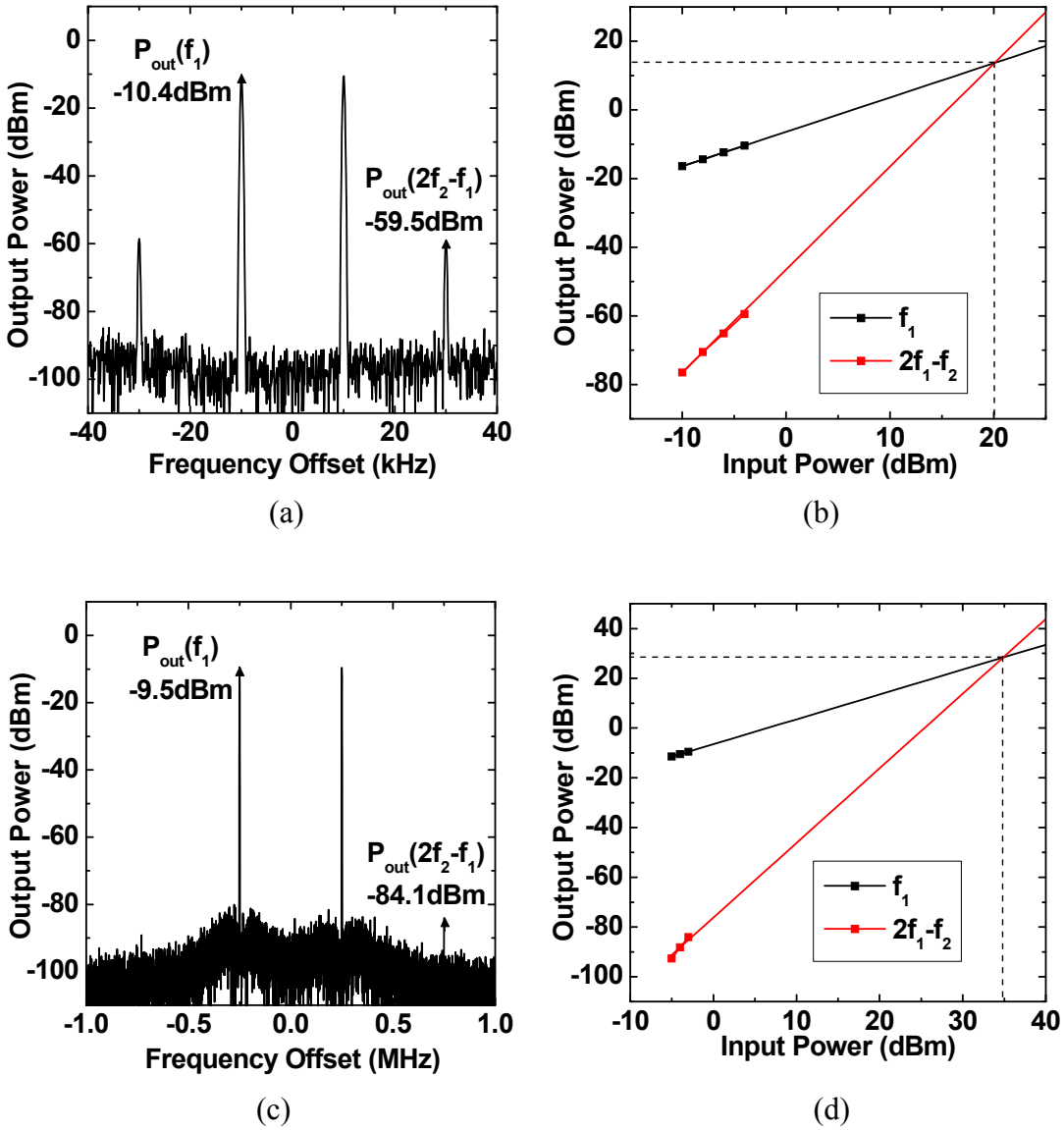


Figure 3.15. Measured power spectrum when all tunable capacitors are at the initial states; (a) output power spectrum with frequency offset of 20 kHz and input power of -4 dBm; (b) extracted IIP_3 with frequency offset of 20 kHz; (c) output power spectrum with frequency offset of 500 kHz and input power of -3 dBm; (d) extracted IIP_3 with frequency offset of 500 kHz.

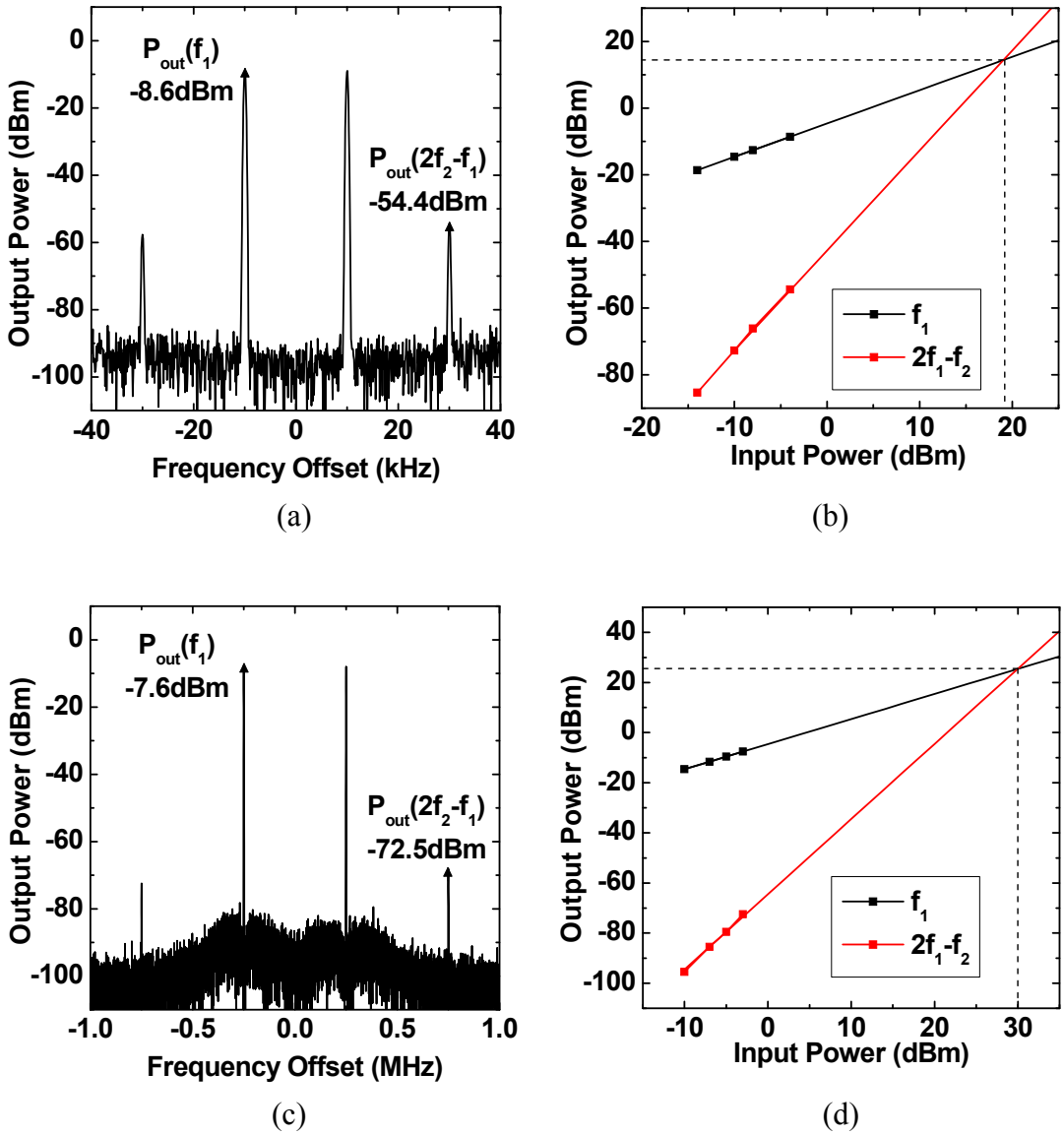
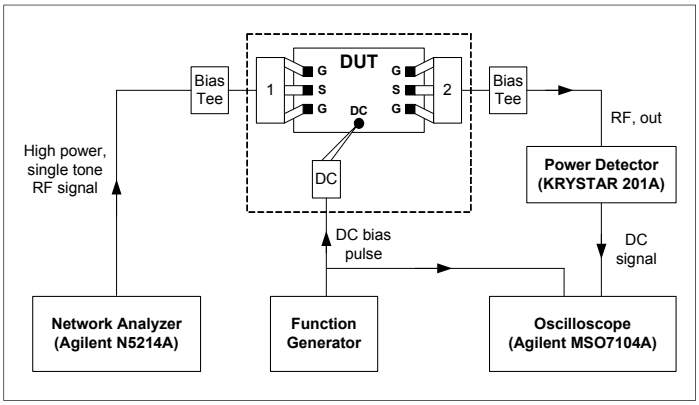
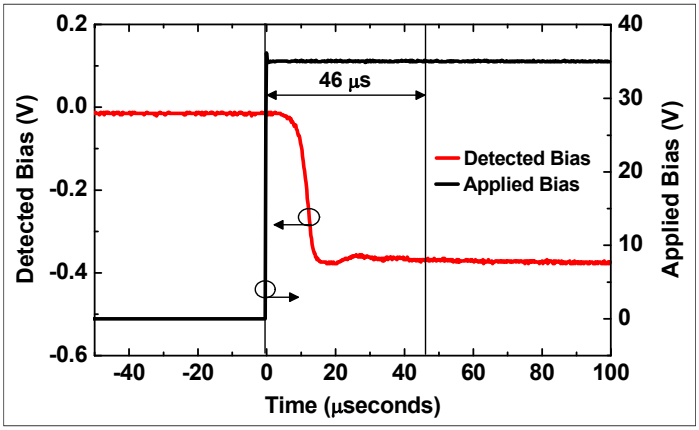


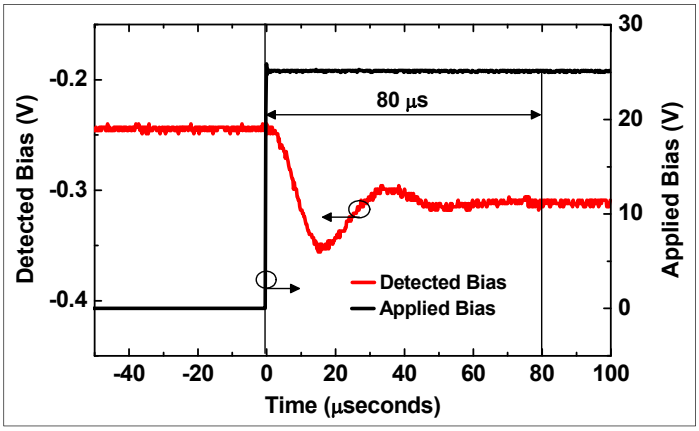
Figure 3.16. Measured power spectrum when 25 V of DC bias is applied to the continuously tunable capacitor; (a) output power spectrum with frequency offset of 20 kHz and input power of -4 dBm; (b) extracted IIP_3 with frequency offset of 20 kHz; (c) output power spectrum with frequency offset of 500 kHz and input power of -3 dBm; (d) extracted IIP_3 with frequency offset of 500 kHz.



(a)



(b)



(c)

Figure 3.17. (a) The setup used for tuning-speed measurements. The measured time response when (b) 40 V and (c) 25 V is applied to the tunable capacitor.

The tuning speed of the filter is measured using the setup shown in Figure 3.17 (a). A 10 dBm of single tone RF signal at the corresponding center frequency for the DC tuning bias is applied using the network analyzer. The RF signal at the output port is converted into DC voltage using a KRYTAR 201A power detector. The RF signal before applying the bias is zero; after application of bias, the filter tunes to the frequency of the input RF signal and a non-zero power is detected using the power detector. The tuning bias and power detector outputs are monitored with an Agilent MSO7104A oscilloscope to extract the tuning speed.

Table 3.6. Comparison between tunable front-end filters in the UHF range.

	Brown '00 [78]	**Sanchez-Renedo '05** [81]	**Rais-Zadeh '09** [68]	**Zhang '10** [104]	***This work***
f_c	700-1330 MHz	470-862 MHz	786-836 MHz	680-1000 MHz	602-1011 MHz
Filter configuration	5^{th} order discretely tunable combline filter	3^{rd} order continuously tunable combline filter	2^{nd} order continuously tunable lumped filter	2^{nd} order continuously tunable combline filter	3^{rd} order continuously tunable lumped filter
Insertion loss	2.0-6.0 dB	3.0-6.0 dB	4.0-6.0 dB	1.1-1.5 dB	3.0-3.6 dB
BW_{3dB}	8-22 % of f_c	1-3 % of f_c	5-6 % of f_c	8-12 % of f_c	13-14 % of f_c
BW_{30dB}/BW_{3dB}	2.0-3.0	3.0-5.0	> 7.0	5.0-6.0	3.2-4.7
Tuning Speed	N/A	< 1 µs	< 1 ms	< 1 µs	40-80 µs
IIP_3	18-24 dBm	N/A	N/A	13 dBm	20-30 dBm
Technology	PCB + MEMS switch	PCB + CMOS varactor	MEMS (single chip)	PCB + CMOS varactor	MEMS (single chip)
Size	< 31.0 × 40.0 mm^2	< 50.0 x 65.0 mm^2	< 5.0 x 6.0 mm^2	< 30.0 × 30.0 mm^2	< 11.0 × 15.0 mm^2

Figure 3.17 (b) shows transition of detected power level when a pull-in bias of 40 V is applied to the tunable capacitors. The measured transition time with this bias condition is better than 50 µs, which is the maximum tuning speed of the filter. As shown in Figure

3.17 (c), with 25 V of DC bias, the transition time is around 80 μs. At this bias, the membrane does not completely touch down and the stabilization time is longer.

Compared to the reported work, the filter presented in this chapter is the highest-performance single-chip filter in sub-GHz frequency band (Table 3.6). A significantly better performance is achieved for this filter using 12 wide-tuning range MEMS capacitors, high-Q integrated inductors, and a higher-order Chebychev design. In the next chapter, possible packaging technique and measure results of a packaged filter is discussed.

CHAPTER 4.

OTHER PROCESS CONSIDERATIONS FOR TUNABLE MEMS BANDPASS FILTERS

In the previous chapter, the design, and measurement results of an integrated tunable MEMS bandpass filter fabricated on a Borosilicate glass substrate were discussed. To be a practical solution for reconfigurable radios, there are other design and fabrication considerations that need to be addressed. First, packaging is essential for the protection of movable MEMS. Packaged devices show better reliability and improved life time. Therefore, in this chapter, possible packaging processes are discussed and a low-temperature technique is applied to package the filters. Second, silicon is a more attractive choice for the substrate, as it is low cost and can be used to implement a larger variety of passive elements, including bulk acoustic resonators and filters. For this reason trap-rich high-resistivity silicon is considered as an alternative low-loss substrate. Lumped element passives fabricated on high-resistivity silicon show promising performance. At the end of this chapter, the process variation of the tunable RF MEMS platform is also discussed, which should be considered in the design stage to satisfy target specifications of integrated passive components.

4.1. Packaging of Tunable MEMS Bandpass Filter

Reliability and life time of tunable micro-devices are significantly enhanced when they are packaged. Without proper packaging, migration of organic impurities can greatly degrade the performance of low-loss ohmic switches [33]. Also, humidity can be another major issue that could affect actuation characteristics of the movable membrane and derive non-steady operation of actuated devices. Therefore, we will first briefly discuss possible packaging technologies that could be employed for tunable RF MEMS, and then present a technology that we used to package our tunable MEMS filters. Finally, we present the measurement results of a packaged filter.

4.1.1. Packaging Technologies for RF Tunable MEMS Devices

Common packaging and interconnecting schemes used mainly for RF MEMS switches are illustrated in Figure 4.1 [105]. Anodic [106] and fusion [107], [108] bonding do not require additional bonding materials and provide clean and flat surfaces after the bonding process. However, the bonding temperature is relatively high (> 300 °C). Other metal-based bonding processes are eutectic [108], thermo compression [109], and solder [110] bonding. These bonding processes are relatively easier and do not require very strict cleaning processes. However, there is additional parasitic capacitance in the RF feed-through when signal line and bonding metal are insulated with a dielectric layer. Glass frit bonding in Figure 4.2 [111] does not have the RF feed-through issue, but

it also requires relatively high temperatures. Polymer bonding [112], [113] is a relatively low-temperature process and does not suffer from the RF feed-through issue either. However, out-gassing during the packaging process can damage delicate released membrane structures; thus, the polymer material used for packaging should be characterized carefully.

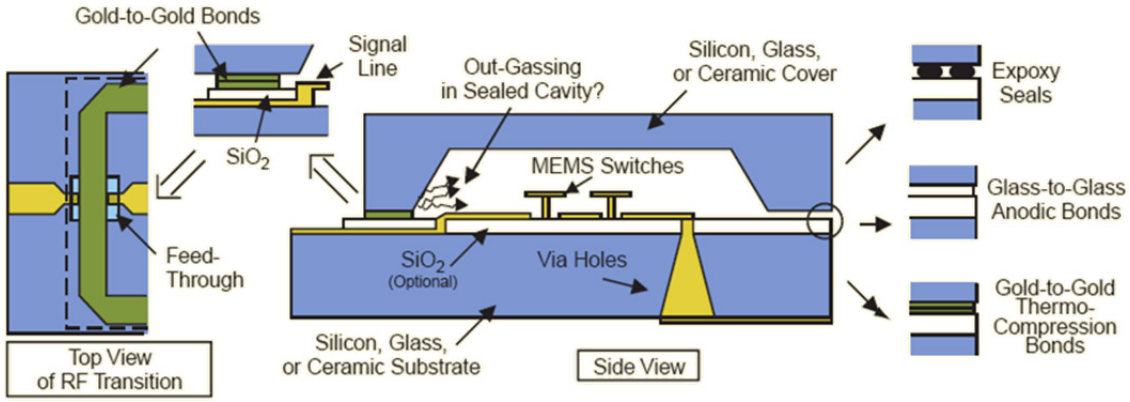


Figure 4.1. Packaging and interconnect schemes for RF MEMS switches [105].

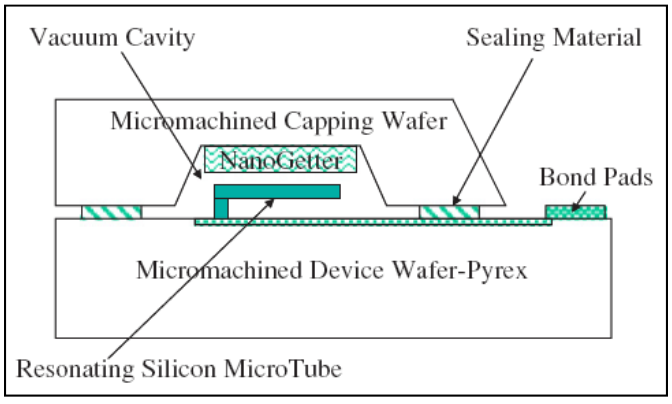


Figure 4.2. Schematic diagram of hermetically glass-frit sealed packaging approach [111].

Although the wafer-level bonding schemes presented in Figure 4.1 are very common, they cannot be employed after the device is released. Depending on the sacrificial layer and the nature of the device, the release step can be carried out after the wafer-level bonding step. However, it is still not practical to do a post-sealing step for larger-size devices. Therefore, surface micro-machining [114] is utilized to package each individual RF tunable component, providing a hermetic-level seal if necessary.

4.1.2. Hermetic Packaging with Surface Micromachining

To hermetically package our tunable MEMS bandpass filter, surface micromachining is the most suitable candidate. Since the fabrication process is based on multiple polymer sacrificial layers, high-temperature wafer-level bonding processes discussed earlier cannot be applied to package these devices. As shown in Figure 4.3, by adding two more fabrication steps to our existing technology platform, the tunable devices can be hermetically packaged. The process steps (a) to (d) are the same as the one presented in Chapter 2. The only difference is that the second sacrificial layer is also utilized to create a gap between the MEMS components and the lid. Before releasing the tunable devices, an additional low-loss dielectric layer is deposited and patterned with release holes. After the sacrificial layers are removed, release holes can be sealed with a second dielectric layer. For this step, sputtering is the most preferred deposition method, which can be used to uniformly cover the release holes and can provide a hermetic seal.

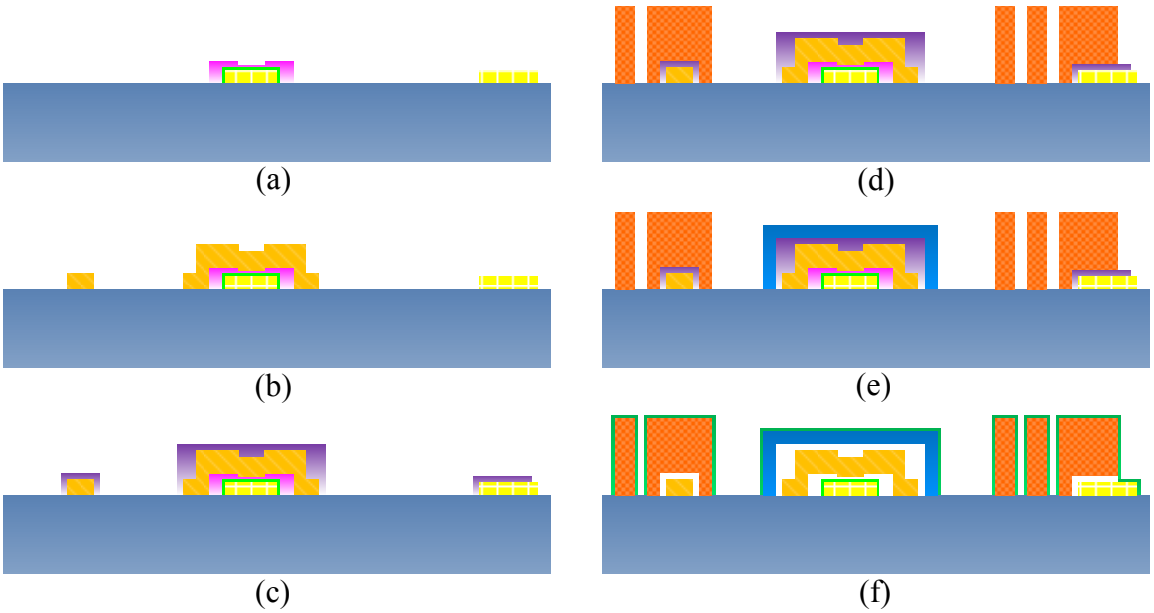
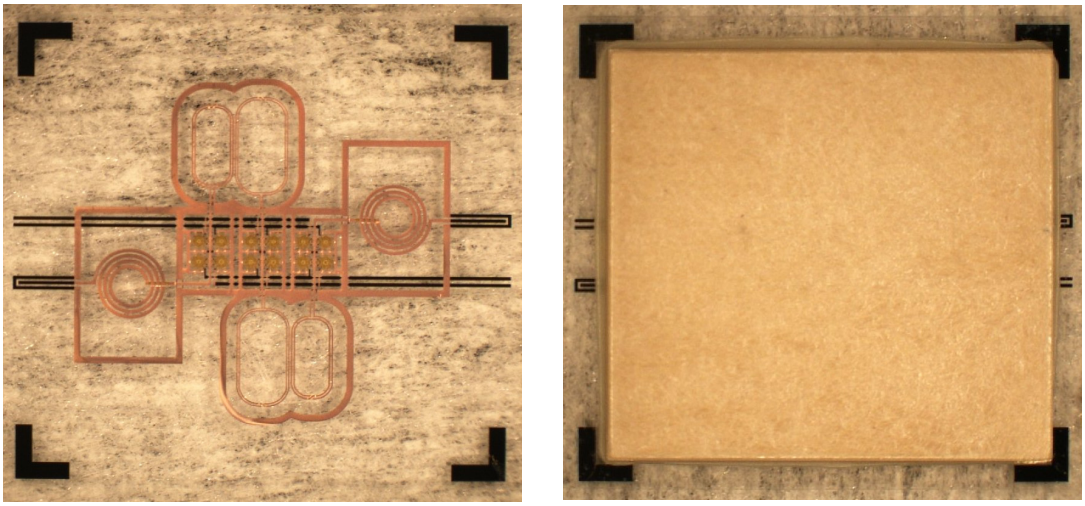


Figure 4.3. Surface micromachining process of tunable MEMS bandpass filter including the hermetic packaging steps; (a) bottom electrode, dielectric layer, and polymer sacrificial layer are processed; (b) top membranes of tunable MEMS devices are electroplated; (c) the second sacrificial layer used for hermetic packaging and interconnect insolation is processed; (d) inductor and routing layer are electroplated; (e) low temperature dielectric layer is deposited and patterned for packaging; (f) MEMS devices are released and subsequently sealed with a second dielectric layer.

4.1.3. Packaging Process Using a Liquid Crystal Polymer Lid

Besides the surface micromachining process shown in Figure 4.3, we considered a few other packaging techniques, each having their own advantages and disadvantages. A low-cost packaging process uses liquid crystal polymers (LCP) to cap the device [115], [116]. Low-temperature epoxy preform bonding is used to attach the polymer lid to the wafer. Since the process is low temperature and the polymer lid has a low loss at RF, the package does not degrade the frequency or tuning performance of the filter. The tunable filter in Figure 4.4 (a) is packaged using this bonding technique. The custom-designed

LCP lid having a with epoxy preform is provided by Stratedge [117]. The LCP lid is first aligned and clamped with a single tunable filter die using miniature spring clamps [118], which provides 3.5 N/cm^2 of clamping pressure between the LCP lid and the filter die. After that, the clamped filter is left in the oven at 80 °C with for the duration of 1 hour. The microscope image of the packaged tunable MEMS filter is shown in Figure 4.4 (b). Compared to the filter shown in Fig. 3.11, the size of the packaged filter shown in Figure 4.4 (a) is reduced by optimizing and sizing the matching inductors.

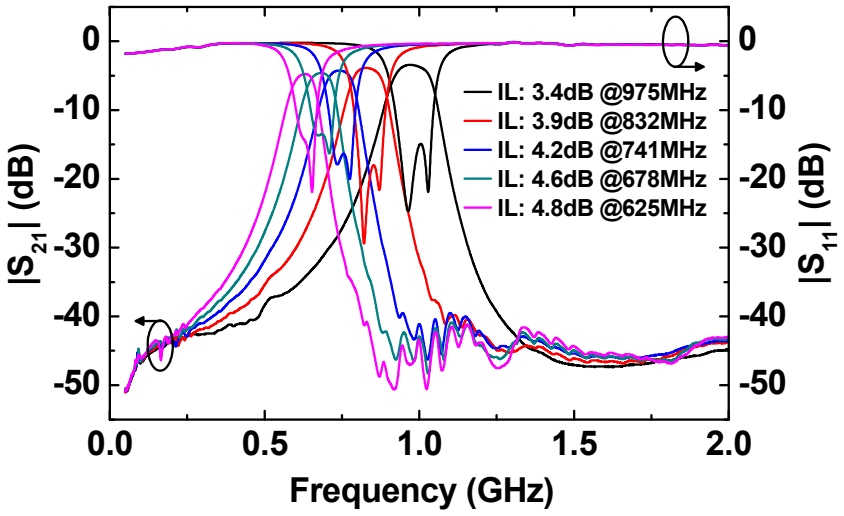


(a) (b)

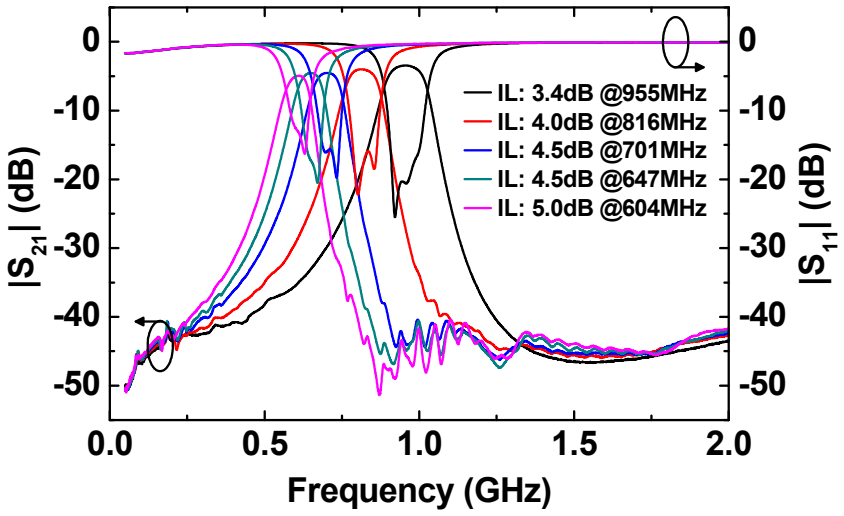
Figure 4.4. Microscope of tunable MEMS filter with optimization of matching inductors; (a) top-down view before packaging step; (b) top-down after packaging step.

Measurement results of the tunable MEMS filter before and after packaging are shown in Figure 4.5. Although the center frequency of the filter is shifted by about 20 to 40 MHz, no severe performance degradation is observed after the packaging step. The frequency shift is due to small bending of the stressed capacitor membrane during the

packaging process. By further optimizing the electroplating step for the membrane layer, the intrinsic stress and stress gradient can be further reduced and more optimized packaging results can be achieved.



(a)



(b)

Figure 4.5. Measurement results of tunable MEMS bandpass filter at each tuned state; (a) before packaging; (b) after packaging.

4.2. Trap-Rich High-Resistivity Silicon Substrates

Although the RF MEMS devices in the previous chapters are fabricated on glass substrates to achieve better RF performance, using Si substrate offers more fabrication options and compatibility with other MEMS or CMOS technologies. Preparing a trap-rich layer between a top passivation layer and a high-resistivity silicon (HR-Si) substrate is one of the most effective ways to improve RF loss in a standard HR-Si. To validate and investigate the effectiveness of the trap-rich layer in lowering the substrate loss, diverse RF MEMS passives such as capacitive switches, inductors, and tunable capacitor banks have been fabricated on standard HR-Si and trap-rich HR-Si substrates. The RF performance of devices is modeled using the equivalent lumped electrical models and compared with measurement results. Analysis using electromagnetic tool is also discussed and a simulation platform is proposed which can be utilized to predict the performance of integrated passive components on HR-Si and trap-rich RH-Si substrates.

4.2.1. Low Loss Substrates for RF Passives

Resistivity and dielectric loss are two of the most critical substrate parameters that need to be considered when designing high-performance RF MEMS. Commonly, quartz [119] or borosilicate glass [120], [121] substrates have been used for fabrication of RF devices as they offer both a small dielectric loss (loss tangent) and a high resistivity. However, compared to silicon, these materials show lower thermal conductivity resulting

in heating issues [122], are harder to bulk micromachine, and are not applicable as a common platform for implementing diverse MEMS structures and solid-state devices. Therefore, micromachined CMOS-grade silicon [123], [124], HR-Si [17], [125], or silicon-on-insulator (SOI) [126] substrates have been used when integration has been of the most importance.

Commonly, silicon dioxide is used as the passivation layer of the silicon-based substrates. The effective resistance of passivated HR-Si is lower than the bulk resistance value because of the accumulation of charges at the interface between silicon and the silicon dioxide passivation layer [127], [128]. This parasitic surface charge (PSC) induces additional coupling with the substrate and reduces the effective substrate resistivity by several orders of magnitude. As a result, Q and harmonic distortion of RF passives on HR-Si substrate are exacerbated [127], [128].

Formation of PSC degrades the Q of inductors more severely at higher frequency as the substrate loss is the limiting Q mechanism for inductors at high frequencies. On the other hand, for capacitors, PSC has a more dominant effect at lower frequencies as it substantially increases the effective series resistance; whereas, the ohmic loss of the metal plates has a more significant effect at high frequencies. In order to lower such losses in HR-Si, additional trap-rich layers such as poly-silicon or amorphous silicon can be deposited prior to the silicon dioxide deposition step [129], [130]. The PSC layer derived from the positive fixed charges at the Si/SiO_2 interface is reduced with the

introduction of a high-density trap-rich layer. The layer captures the free electrons attracted to the positive fixed charges, thus increases the effective substrate resistance.

4.2.2. Modeling for Trap-Rich High-Resistivity Silicon Substrates

To simulate RF properties of passive components on a single layer substrate, electromagnetic (EM) simulation tools such as SONNET [131] or HFSS can provide easy and comprehensive solutions. However, the effective resistance change, derived from PSC and trap-rich layers in passivated HR-Si substrates is not properly reflected in EM tools unless Si substrate is properly modified or divided into multiple layers with different properties, reflecting their effect on the overall substrate performance. Therefore, we first utilize the substrate lumped element model in [130], combined with passive component models, to analyze the effect of PSC and trap-rich layers. This model is also used to verify the importance of low metal loss in passive components in order to achieve high *Q*s. Since EM tools are still very effective for simulation of passive modules performance, such as phase shifters, filters, or matching networks, we also provide a setup that can be used to run accurate simulations without requiring heavy computation resources.

4.2.2.1. Lumped Element Model

The effect of PSC and trap-rich layers in HR-Si substrate is well modeled and compared with measurement results in [130]. This model is combined with lumped

element model of each passive component here. Figure 4.6 shows the complete models of an inductor and a one-port capacitive switch on trap-rich HR-Si, where C_1 is the coupling between the device and the SiO_2/Si interface, R_2 and C_2 are the resistive and capacitive coupling between the device and the wafer backside metallization, R_3 and C_3 are the coupling paths between the two ports through the silicon substrate.

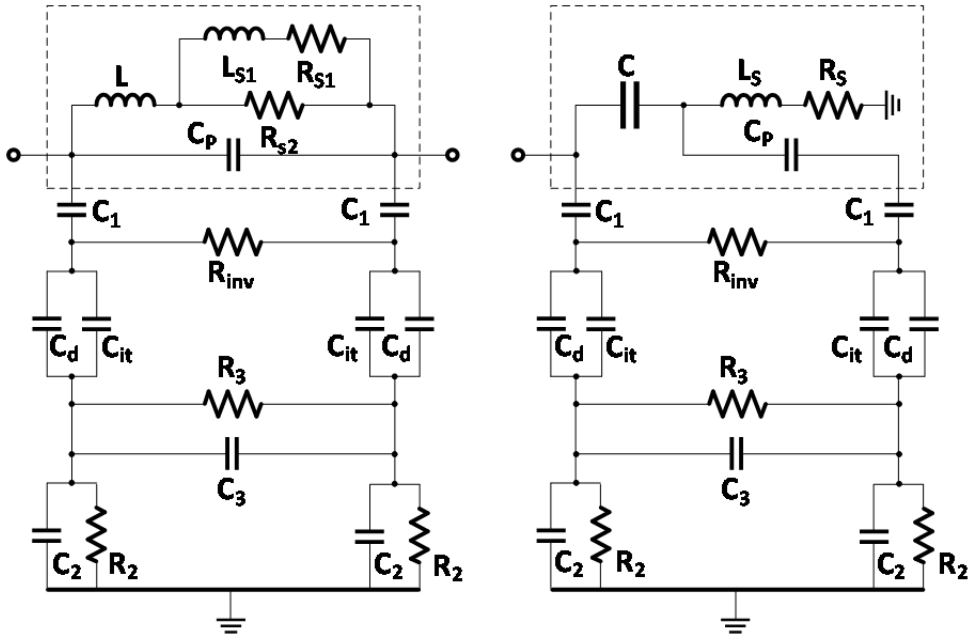


Figure 4.6. Lumped element equivalent model reflecting the effect of PSC and the trap-rich layers of (a) an inductor and (b) a one-port MEMS capacitive switch on a trap-rich HR-Si substrate.

The effect of PSC is modeled with C_d and R_{inv}, which are the depletion capacitance and resistance, respectively. With the addition of the trap-rich layer to the HR-Si substrate, the effective resistance increases and R_{inv} becomes ignorable. C_{it}, the small parasitic capacitance caused by the trapping mechanism, is also added, while C_d is

reduced significantly at the same time. However, at high frequencies above a few MHz, relaxation time of the carriers can no longer follow the AC signal and the substrate equivalent capacitance does not show much difference between HR-Si and trap-rich HR-Si substrates. Therefore, for the RF equivalent model, C_d and C_{it} are combined as C_{eq} and C_{eq} does not show much difference between HR-Si and trap-rich substrates.

To reflect the parasitics of inductors derived from the skin and proximity effects, the ladder circuit (L_{s1}, R_{s1}, R_{s2}) in [132] is adopted, as shown in Figure 4.6 (a). Here, C_p represents the parasitic capacitance, mostly due to the overpass or underpass layers in multi-turn inductors. The one-port MEMS capacitive switch model in Figure 4.6 (b) also reflects non-ideal parasitic components derived from springs (L_s, R_s) and actuation electrodes (C_p). The values of capacitors, C and C_p are changed according to the ON/OFF states of the capacitive switch. These lumped models are used to model and analyze the frequency response of inductors and capacitive switches on both trap-rich and standard HR-Si substrates. Where appropriate, the values of the components in the model are changed to reflect the substrate properties. The most dominant substrate parameter, R_{inv} varies depending on the accumulated charge (Q_{ox}) and the trap density (D_{it}) level, which should be carefully characterized first for accurate derivation of a lumped model. The equations for all passive component values in the equivalent model are provided in [130].

4.2.2.2. 3D Electromagnetic Simulation

As noted earlier, simply applying the original substrate properties in EM simulations does not provide a good estimate of passive device performance on HR Si. However, EM tool is very effective in modeling the metal loss and interconnects and can be an accurate simulation option if the effect of PSC and trap-rich layers is well reflected in the HR substrate model.

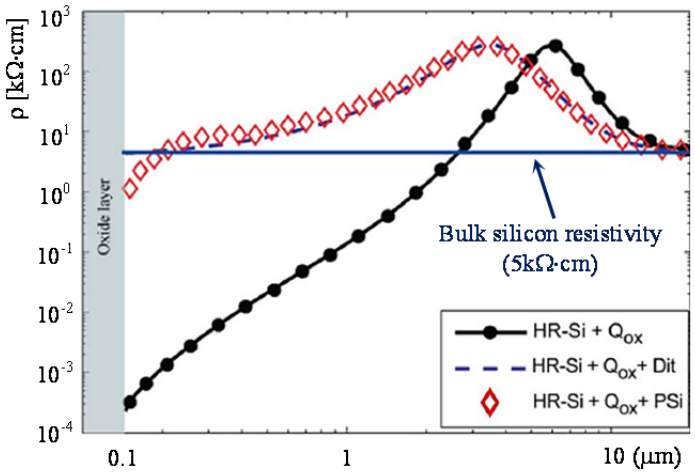


Figure 4.7. Lumped element equivalent model reflecting the effect of PSC and the trap-rich layers of (a) an inductor and (b) a one-port MEMS capacitive switch on a trap-rich HR-Si substrate [130].

Figure 4.7 shows the simulated resistivity distribution of 5kΩ·cm HR-Si substrates with and without a trap-rich layer [130]. It is estimated that PSC effect is dominant on the top most 3 μm layer, and it does not have a significant effect on the properties of deeper layers. Therefore, HR-Si substrates with and without the trap-rich layer can be modeled using the stack diagram in Figure 4.8 for accurate and simple EM simulations.

In HR-Si model with no trap-rich layer, a PSC layer is added between the bulk HR-Si and the silicon dioxide passivation layer (Figure 4.8 (a)). The resistivity and loss of HR-Si with a trap-rich layer is assumed to be similar to the bulk value and thus the stack in Figure 4.8 (b) is used for trap-rich HR-Si substrates.

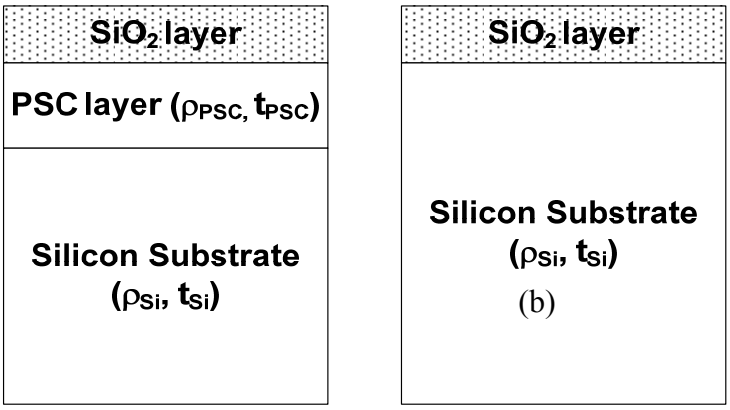


Figure 4.8. Approximated substrate assignment of HR-Si for RF simulation; (a) with a PSC layer; (b) with a trap-rich layer after PSC compensation.

To verify the accuracy of EM simulations using the substrate setup in Figure 4.8, SONNET EM simulation results are compared with those using the lumped element models and the measurement results of fabricated devices, as will be shown later in this paper. In SONNET simulations of devices on HR-Si, the parameters of the PSC layer are set as 4Ω·cm (ρ_{PSC}) and 4 μm (t_{PSC}) and the resistivity of the remaining 376μm (t_{Si}) thick silicon substrate is set as 4kΩ·cm (ρ_{Si}). HR-Si with a trap-rich layer is assigned with the nominal substrate parameters (*i.e.* t_{Si} =380μm and ρ_{Si}=4kΩ·cm) with the assumption that the trap-rich layer compensates all PSC effects. As shown in Figure 4.9, both lumped element and EM simulation show good agreement with the measurement result of a 1 nH

inductor (*IND1* in Figure 4.12 (a)); the maximum *Q*, peak *Q* frequency, and SRF are all in agreement with the measured results. Compared to the lumped element model, EM results using the setup proposed in Figure 4.8 are more accurate as SONNET EM tool also reflects some frequency dependent parasitic effects.

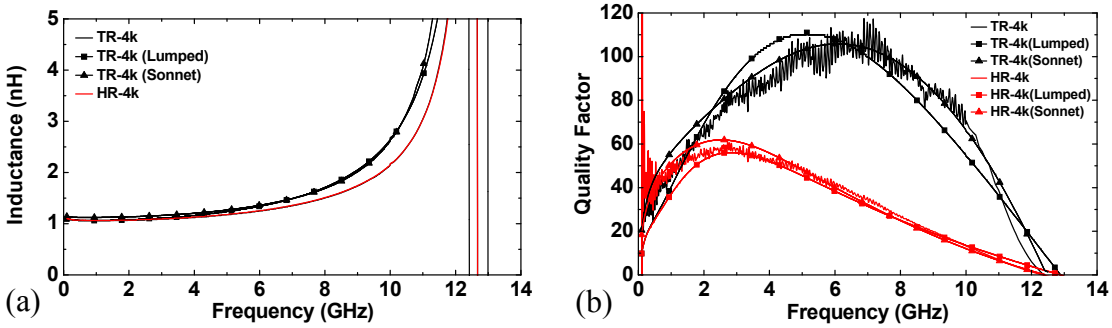


Figure 4.9. Comparison of measurement result with EM simulation and lumped element model. The measurement data is from IND1 on 4kΩ·cm HR-Si with and without a trap-rich layer; (a) inductance; (b) *Q*.

4.2.2.3. Substrate Loss vs. Metal Loss

The dominant loss mechanism limiting the *Q* of inductors is different depending on the frequency of operation. At lower frequencies, resistive loss of metal layers limits the *Q*. Metal loss can be reduced by using thicker metal layers or higher conductivity materials. As the frequency increases, the skin and proximity effects further increase the effective resistance and reduce the *Q*. At higher frequencies, because of the dielectric loss of the substrate and generation of eddy current, the substrate loss dominates the metal loss and reduces the *Q* [124], [133].

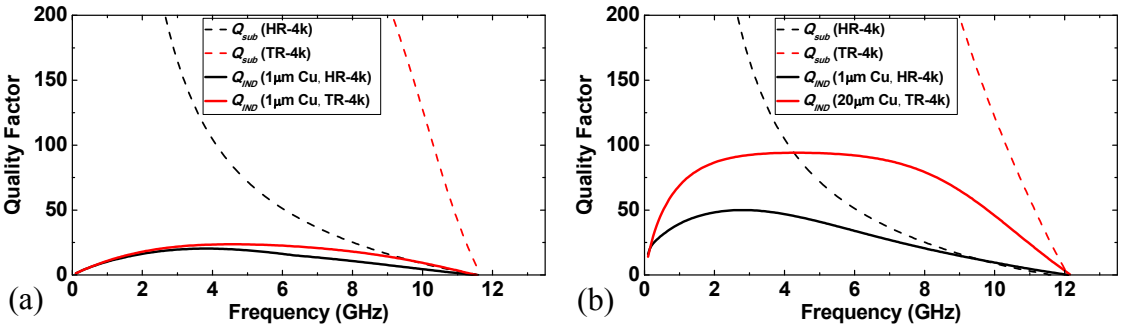


Figure 4.10. Illustration of quality factor difference as condition of loss mechanism is changed; (a) when substrate loss is improved (HR-4k to TR-4k); (b) when both substrate and ohmic loss are improved (1μm Cu to 20μm Cu).

In a previous work [134], the Q of an inductor on a trap-rich HR-Si did not show much improvement over that of an inductor on a standard HR-Si substrate. This was because the conductor was thin and the metal loss dominated the substrate loss. To prove this and show the true value of the trap rich layer in improving the Q, inductors are simulated and analyzed using SONNET. Two different substrates are assumed, one is a standard 4kΩ·cm HR-Si (HR-4k) and the other one is a 4kΩ·cm HR-Si with a trap-rich layer (TR-4k). The substrate setups in Figure 4.8 are used for these simulations. The layout of the simulated device is similar to *IND1* in Figure 4.12 (a), but the thickness of the metal layer is adjusted in each simulation. Figure 4.10 (a) shows the substrate loss (Q_{sub}) and the overall Q of the inductor (Q_{IND}) when the inductor is assumed to be composed of 1 μm thick copper (Cu) layer. For extraction of Q_{sub}, a lossless metal layer is assigned to the inductor. As shown in the result, Q_{IND} is limited by the ohmic loss even with the addition of the trap-rich layer. On the other hand, as shown in Figure 4.10 (b),

Q_{IND} can be significantly improved by increasing the thickness of the metal layer from 1 μm to 20 μm and using the trap-rich HR-Si substrate.

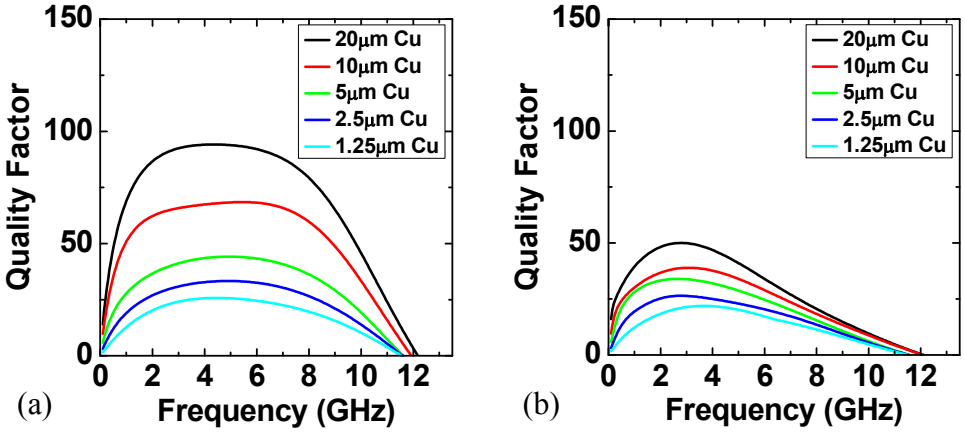


Figure 4.11. Simulation result of 1nH inductor on (a) trap-rich 4kΩ·cm HR-Si (TR-4k) and (b) standard 4kΩ·cm HR-Si (HR-4k) with different Cu layer thickness; 20μm, 10μm, 5μm, 2.5μm, and 1.25μm.

Table 4.1. Maximum Q of inductors with each Cu layer on HR-4k and TR-4k substrates.

Resistivity (mΩ/□)	Layer thickness with Cu (μm)	Max(Q) on TR-4k	Max(Q) on HR-4k	Max(Q) ratio
7.0×10^{0}	20.00	94.2	50.0	1.88
1.4×10^{1}	10.00	68.5	38.9	1.76
2.8×10^{1}	5.00	44.2	34.0	1.30
5.6×10^{1}	2.50	33.3	26.4	1.26
1.1×10^{2}	1.25	25.8	21.9	1.18

To study the thickness range and the conductivity required for the metal layer to appreciate the effect of the trap-rich layer, simulations were performed on *IND1* with different Cu layer thickness, ranging from 1.25 to 20 μm. The extracted Q plot and the

maximum Q value for each condition are shown in Figure 4.11 and Table 4.1, respectively. When a 1.25 μm thick Cu layer is used, the simulated Q is similar to the values reported in [134]. With the metal thickness of 20 μm (7.0×103mΩ/□), Q is improved by 88% using the trap-rich layer, while Q improvement is only 18% with the metal thickness of 1.25 μm (1.9×106mΩ/□). This calls for a fabrication process that offers thick high-conductivity metals, such as silver, gold, or Cu. In this work, inductors are fabricated using 35 μm thick electroplated Cu to achieve high Qs at a broader frequency range. 5 μm thick electroplated Au is utilized as an interconnection layer of multi-turn inductors. The metal thickness of MEMS capacitive switches can be also optimized for better Q following the same method. Since inductors are usually the Q limiting components, the electrical performance of capacitive elements is not discussed here in more detail.

4.2.3. Fabrication Process

For the preparation of substrates, a process similar to the one in [135] is utilized. The detailed specifications of each substrate are outlined in Table 4.2. Low-pressure chemical vapor deposition (LPCVD) was used to deposit a layer of polysilicon on TR-10k at 625 °C and an amorphous Si layer on TR-4k at 525 °C. The silicon was then crystallized by rapid thermal anneal (RTA) during 120s at 900 °C. For all wafers, a 150-

nm-thick covering oxide was deposited by PECVD at low temperature (350 °C) to avoid crystallization of the deposited amorphous Si.

Diverse inductors, capacitive switches, and capacitive switch banks are designed and fabricated on four different substrates using the fabrication process described in [136] and Chapter II. For the bottom electrode and dielectric layers of the capacitive switch, 5000A° of evaporated Au and 1000A° of ALD Al_2O_3 are utilized, respectively. 2 μm of PMMA A9 is spin-coated, baked, and patterned to build the sacrificial layer of air-suspended membranes. 5 μm of electroplated Au comprises the top membrane of the capacitive switches and the interconnection layer of inductors. 2 μm of S1813 photoresist is utilized as the sacrificial layer for air-gap insulation between the interconnection layer and the 35 μm thick electroplated Cu layer, which forms the inductor lines and the ground planes.

Table 4.2. Specifications of the HR-Si substrates

Substrate	ρ Si [Ω·cm]	SiO_2 [nm]	Intermediate trap-rich layer
HR-4k	> 4k	150	-----
HR-10k	> 10k	150	-----
TR-4k	> 4k	180	Amorphous Silicon (360 nm)
TR-10k	> 10k	150	Poly Silicon (330 nm)

4.2.4. Measurement Result

4.2.4.1. Inductors

Four inductors (*IND1*, *IND2*, *IND3*, *IND4*) targeting different operation frequencies are designed using the two electroplated metal layers, 5 µm Au and 35 µm Cu, to obtain sufficiently low ohmic resistance required to observe the effect of the trap-rich layer. To reduce parasitic capacitance and enhance the SRF, the bottom interconnection layer (electroplated Au) is separated from the top copper layer using an air gap of 2 µm, after removing the photoresist sacrificial layer. Microscope images of the fabricated inductors are shown in Figure 4.12.

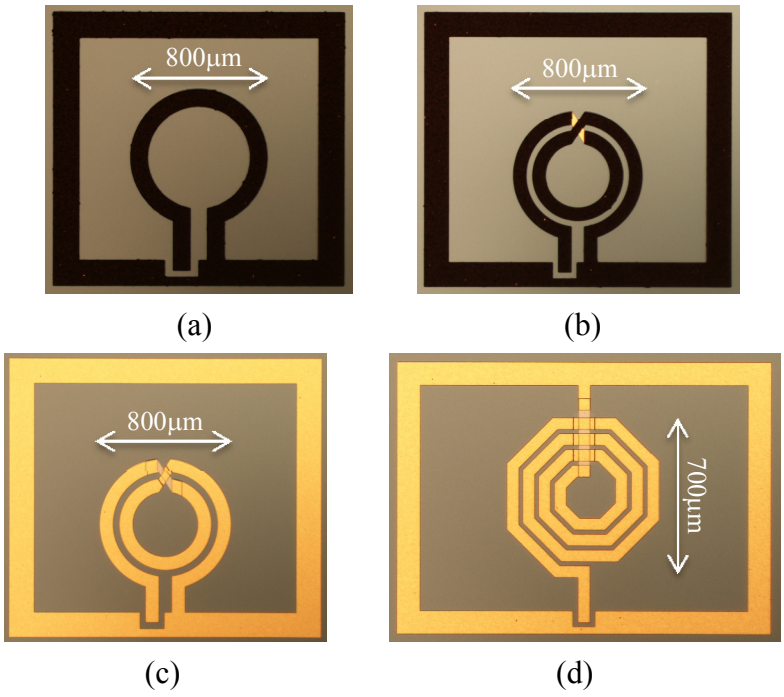


Figure 4.12. Microscope images of the fabricated inductors; (a) *IND1*, composed of a single-turn, 40 µm thick copper layer; (b) *IND2*, composed of a two-turn, 40 µm thick copper layer; (c) *IND3*, composed of a two-turn, 5 µm thick gold layer; (d) *IND4*, composed of a 3.5-turn, 5µm thick gold layer.

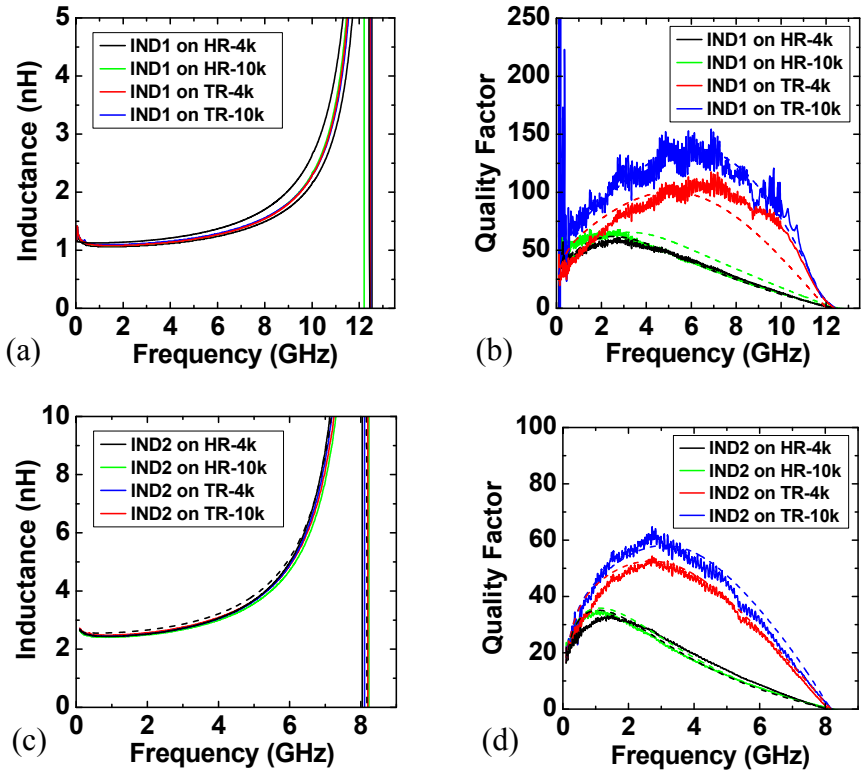


Figure 4.13. Measurement results of inductors on four different substrates listed in Table II; (a) inductance of *IND1*; (b) *Q* of *IND1*; (c) inductance of *IND2*; (d) *Q* of *IND2*.

Figure 4.13 show the measurement results of the four inductors in Figure 4.12 compared with the EM simulation results; the EM simulation results are shown with a dashed line using the same color as each measurement result. The first inductor, *IND1* is a single-turn circular inductor composed of 35 μm thick Cu layer. This inductor is designed to have its peak *Q* at frequencies higher than 6 GHz. As already estimated, trap-rich HR-Si provides a much higher *Q* than the standard HR-Si when a thick Cu layer is used. The maximum *Q* on 10 kΩ·cm trap-rich HR-Si is more than 130 at 6.0 GHz, while the corresponding value on standard HR-Si is only around 66.6 at 2.57 GHz. The difference in the substrate resistivity of 10kΩ·cm and 4kΩ·cm does not make as

prominent difference as does the inclusion of the trap-rich layer. Due to substantial reduction of losses, *IND1* on trap-rich HR-Si exhibits *Q* values similar in range to the inductors fabricated on other low-loss substrates or patterned silicon substrate [124], [133]. The measured Q presented in Figure 4.13 (b) is believed to be the best reported value for spiral inductors fabricated on a solid silicon substrate [124], [133].

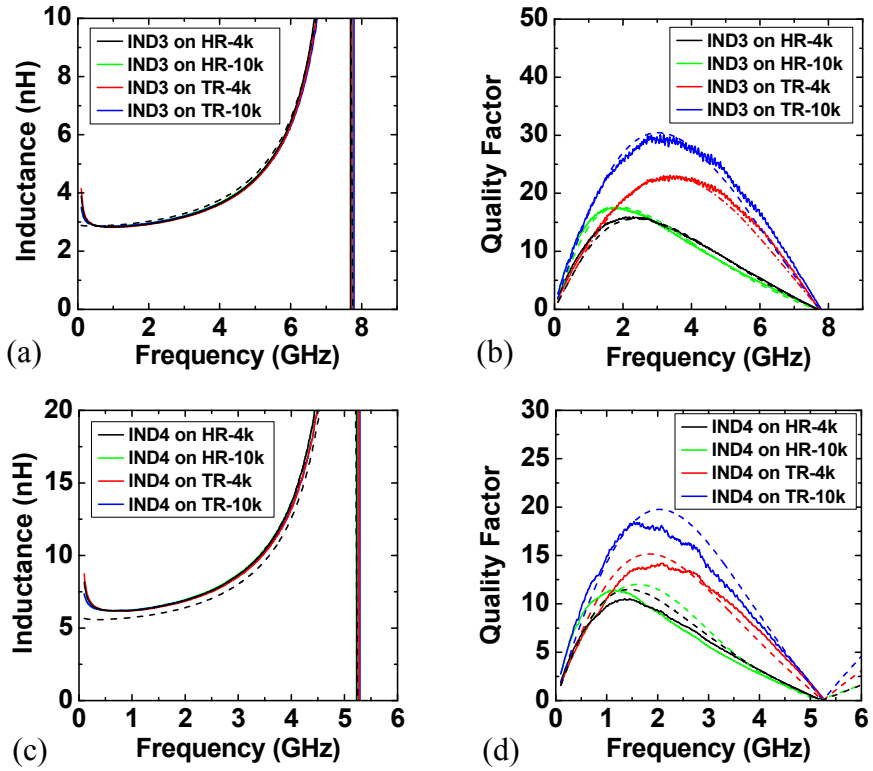


Figure 4.14. Measurement results of inductors on four different substrates listed in Table II; (a) inductance of *IND3*; (b) *Q* of *IND3*; (c) inductance of *IND4*; (d) *Q* of *IND4*; The dashed line is the EM simulation result using each inductor layout and the substrate models.

IND2 is a two-turn circular inductor composed of a 35 μm thick Cu layer. Similarly, using the trap-rich HR-Si one can get higher *Q*s than when standard HR-Si is used.

In order to verify the inductor performance when the metal line is thin, *IND3* is fabricated with 5 μm Au layer, which is the same two-turn circular inductor as *IND2*. Although the maximum Q is still better for inductors on trap-rich HR-Si than those on standard HR-Si substrates, its range is limited because of the substantial ohmic loss.

IND4, a 3.5-turn octagon-shaped inductor composed of 5 μm Cu, is designed for larger inductance value. This is to compare the overall Q of inductors on HR-Si with and without a trap-rich layer when the ohmic loss is even more dominant. As shown in the measurement result, the trap-rich HR-Si provides larger Q than the standard HR-Si. However, the improvement in Q is not as appreciable and significant as the thicker inductors with lower metal loss, which is expected from the previous analysis. These results demonstrate the feasibility of implementing diverse, high-performance inductors across a broad frequency range on a Si substrate.

4.2.4.2. Capacitive Switch

In order to verify the effect of trap-rich HR-Si on capacitive components, the capacitive switch in Chapter 2 is fabricated on the substrates listed in Table II. Detailed design and operation principle of this type of switch can be also found in [136] and [94]. The extracted capacitance and Q are shown in Figure 4.15 and compared with the simulation result using the lumped element model presented in Figure 4.6 (b) in order to prove effectiveness of this model for capacitor design as well. Each lumped element

value is summarized in Table 4.3 for both initial (OFF) and tuned (ON) states. The measurement results are in good agreement with the lumped model simulation results. As shown, the Q is improved by ≥200% using the trap rich layer. The peak Qs of the capacitors on trap-rich HR-Si substrates are similar and independent of the initial resistance of the substrate.

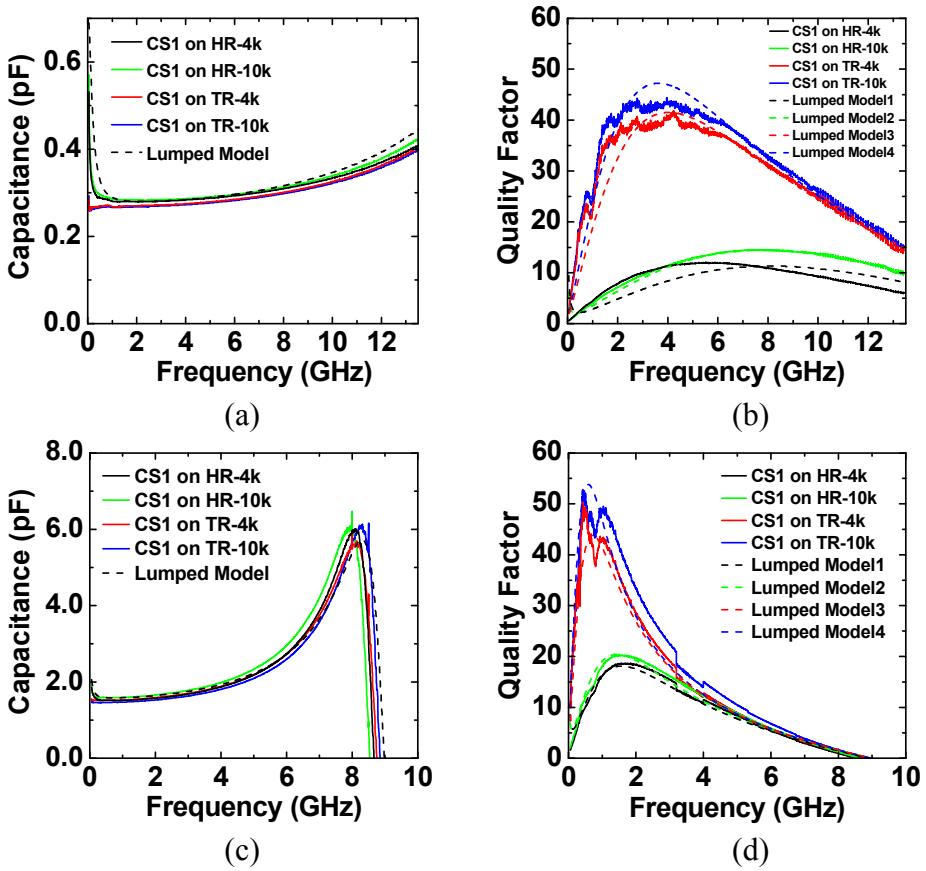


Figure 4.15. Measurement results when each capacitive switch is on four different substrates in Table II. (a) capacitance at initial state; (b) Q at initial state; (c) capacitance at touch-down state; (d) Q at touch-down state.

4.2.4.3. Capacitive Switch Bank

A capacitive switch bank, composed of four capacitive switches, is fabricated and measured to verify the effect of trap-rich layer on larger value capacitors. Detailed design of a similar tunable capacitor bank can be found in [136] and Chapter III; the only difference between the capacitive switch bank fabricated here and that in [136] is that here, all capacitors are digitally tuned versus one of the capacitors in [136] was continuously tuned to achieve a finer tuning resolution.

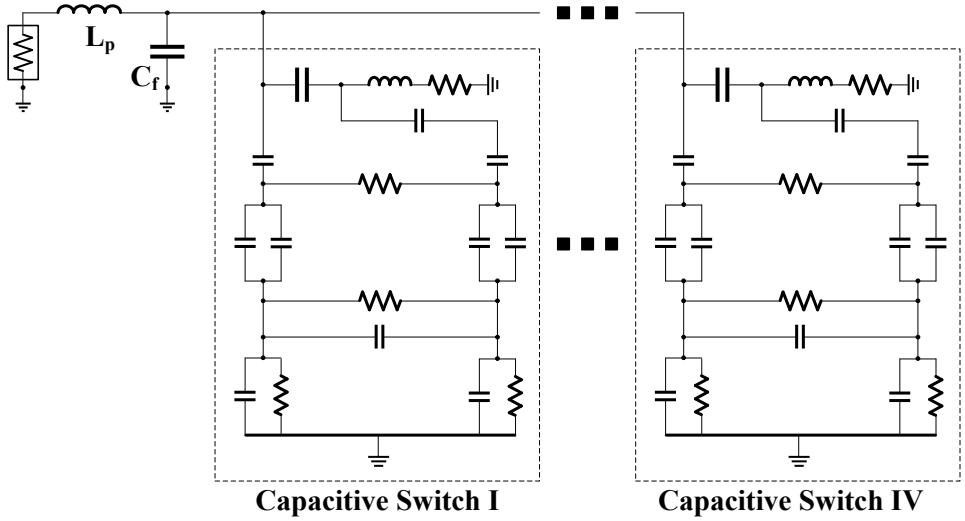


Figure 4.16. Equivalent lumped model of capacitive switch bank.

Measurement results from the initial state and the final tuned state of the capacitive switch bank are shown in Figure 4.17. The lumped element model in Figure 4.16 is utilized for modeling each of the tuned states. The model in Figure 4.16 includes L_p, parasitic inductance for routing, C_f, a fixed metal-insulator-metal (MIM) capacitor, and

four capacitive switches. The fitted values using lumped element models (Table III) show good agreement with the measurement results in Figure 4.17. The results of the capacitive switch bank at all tuned states are summarized in Figure 4.18. Even at larger capacitance values, the trap-rich layer works effectively and provides better Q than the standard HR-Si substrates. Since SRF is a function of capacitor value and inductive parasitics, SRF should not change significantly when capacitors are fabricated on trap-rich HR-Si substrates.

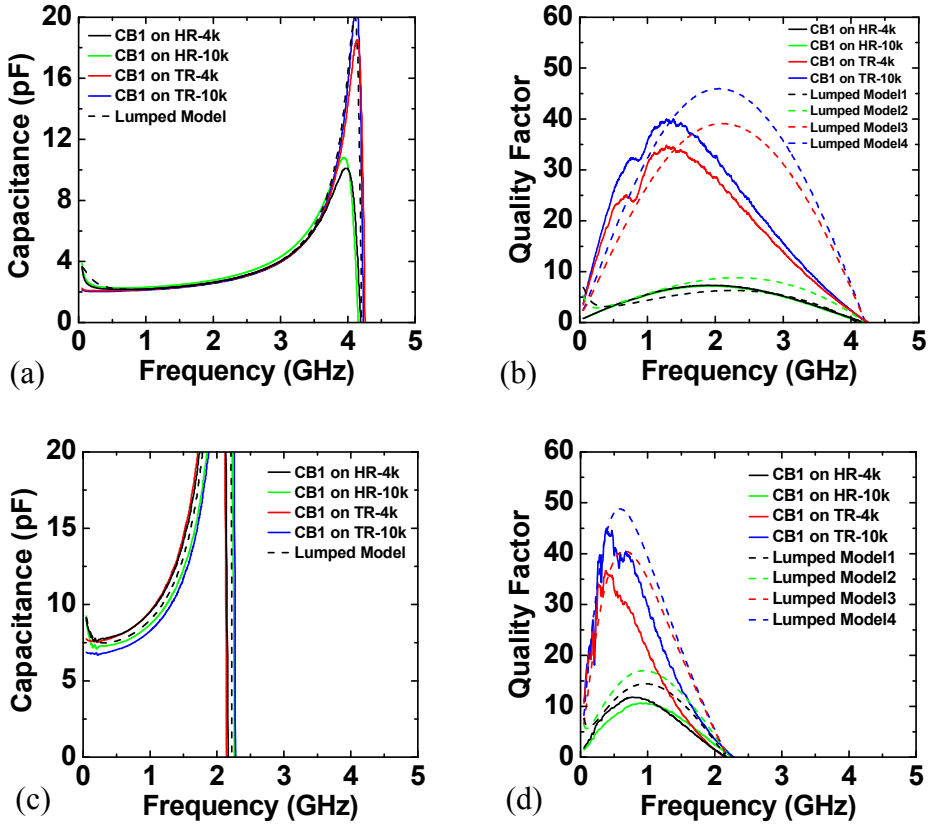


Figure 4.17. Extracted capacitance and quality factor of the capacitive switch bank, compared with the lumped model shown in Fig. 6; (a) capacitance at the initial state; (b) quality factor at the initial state; (c) capacitance when all switches are tuned; (d) quality factor when all switches are tuned.

Table 4.3. RF performance and lumped model parameters of capacitive switches

Substrate	Capacitance (fF) @500MHz	Maximum Q	SRF (GHz)	Lumped Model Parameters for Capacitive Switches										
				C (pF)	L_s (nH)	R_s (Ω)	C_p (pF)	C_{eq} (fF)	R_{inv} (kΩ)	C_1 (pF)	C_2 (fF)	R_2 (MΩ)	C_3 (fF)	R_3 (MΩ)
HR-10k	Initial: 295fF	14.5 @8.2GHz	21.5	0.26	0.20	1.6	0.8	20/60	1.8	1.4/4.0	10/10	1.0/1.0	100	1.0
	Tuned: 1.59pF	20.4 @1.6GHz	8.5	1.55	0.20	1.6	2.0	20/60	2.7	1.4/4.0	10/10	1.0/1.0	100	1.0
TR-10k	Initial: 266fF	44.4 @4.0GHz	22.3	0.26	0.20	1.6	0.8	20/60	14.0	1.4/4.0	10/10	1.0/1.0	100	1.0
	Tuned: 1.46pF	52.8 @0.4GHz	8.9	1.55	0.20	1.6	2.0	20/60	18.0	1.4/4.0	10/10	1.0/1.0	100	1.0
HR-4k	Initial: 289fF	12.0 @5.6GHz	21.8	0.26	0.20	1.6	0.8	20/60	1.1	1.4/4.0	10/10	0.5/0.5	100	0.5
	Tuned: 1.52pF	18.7 @1.5GHz	8.7	1.55	0.20	1.6	2.0	20/60	2.0	1.4/4.0	10/10	0.5/0.5	100	0.5
TR-4k	Initial: 270fF	41.8 @4.2GHz	21.8	0.26	0.20	1.6	0.8	20/60	11.0	1.4/4.0	10/10	0.5/0.5	100	0.5
	Tuned: 1.52pF	50.3 @0.4GHz	8.8	1.55	0.20	1.6	2.0	20/60	12.0	1.4/4.0	10/10	0.5/0.5	100	0.5

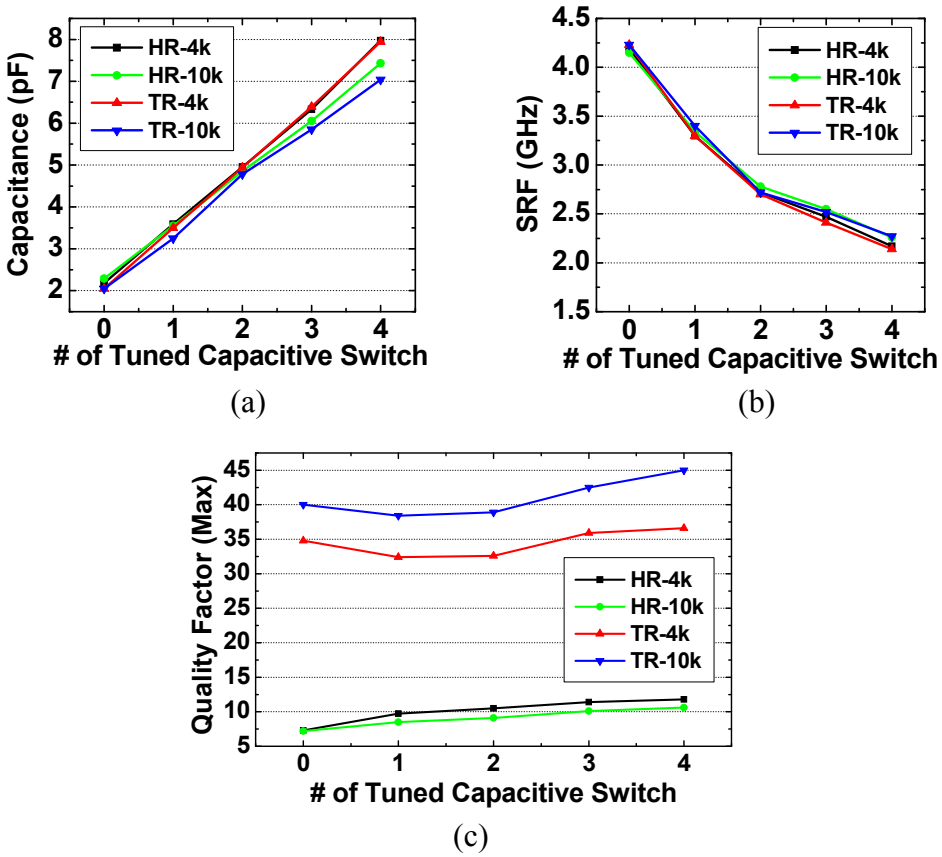


Figure 4.18. Extracted parameters of capacitive switch bank for the four different substrates; (a) capacitance vs. tuned state; (b) SRF vs. tuned state; (c) Q_{max} vs. tuned state.

4.3. Process Variation of Tunable RF MEMS Platform

Air-suspended tunable MEMS structure is an essential part of the presented RF tunable MEMS platform. Although reliability of this fabrication process is proved from the fabricated tunable filters, more quantitative analysis will be necessary in order to consider the process variation in the design stage. For this purpose, the measurement data of the capacitive switches and capacitive switch banks on four HR-Si substrates is compared (Table 4.4 and 4.5). No DC bias is applied for this measurement. From the measurement result, within-wafer variation is almost negligible, where the worst-case variation is still less than 2.3 %. However, wafer-to-wafer variation shows more than 6 %, larger than the within-wafer variation. This larger wafer-to-wafer variation of initial air-gap can be caused from thickness variation of the PMMA sacrificial layer or different residual stress in the electroplated gold layer. Especially, residual stress of electroplated gold can vary depending on the contact resistance during the electroplating process and the quality of the electroplating solution while the wafer-to-wafer variation of the sacrificial layer from the spinning and baking procedures is not significant. Therefore, it is important to design a structure that has a stress-insensitive membrane and springs. The variation of capacitive switch banks is comparable to individual capacitive switches since the less-sensitive MIM capacitor in the array compensates for the added variation from a larger number of capacitive switches in the bank.

Table 4.4. Average, standard deviation, and relative standard deviation of capacitance measured from initial state of capacitive switches on different HR-Si substrates.

	Average (C_{init})	**SD (C_{init})**	**RSD (C_{init})**
HR-4k	297.65 fF	2.44 fF	0.82 %
TR-4k	275.64 fF	6.15 fF	2.23 %
HR-10k	320.65 fF	5.09 fF	0.67 %
TR-10k	268.43 fF	1.79fF	1.59 %
Overall	284.87 fF	17.57 fF	6.17 %

Table 4.5. Average, standard deviation, and relative standard deviation of capacitance measured from initial state of capacitive switch banks on different HR-Si substrates.

	Average (C_{init})	**SD (C_{init})**	**RSD (C_{init})**
HR-4k	3.41 pF	0.05 pF	1.47 %
TR-4k	3.34 pF	0.06 pF	1.80 %
HR-10k	3.66 pF	0.01 pF	0.27 %
TR-10k	3.25 pF	0.04 pF	1.23 %
Overall	3.39 pF	0.15 pF	4.42 %

Although capacitance at down state is not compared here, it tends to show more variations due to the membrane warping and rough contact surface. More discussion about how to overcome these issues will be provided in the last chapter. *Q* of capacitive switch would be another parameter to use for the verification of the process variation, but it is not included here since the overall filter performance is dominated by the inductor *Q* and the absolute value of the capacitor *Q* is not important.

For more accurate extraction of variations in process parameters, larger number of devices should be fabricated and measured. However, the presented data in Tables 4.4

and 4.5 well indicate that the current tunable RF MEMS platform could potentially be a high-yield and high-uniformity technology once the process is carried out in a better optimized foundry facility rather than an academic facility used in this work for the fabrication of prototype devices.

CHAPTER 5.

RF SWITCHES USING PHASE-CHANGE MATERIALS

As mentioned earlier, electrostatic mechanism is commonly utilized to implement tunable passive components. However, conventional MEMS switches based on this mechanism exhibit relatively slow switching speed (tens of μs) and large foot-print, hindering their adoption in commercialized products. Electrostatically tuned passives also suffer from reliability issues from dielectric charging effect and have lower fabrication yield compared to semi-conductor technologies. To overcome these limits, a new tuning mechanism based on phase-change materials is considered in this chapter.

This chapter first introduces a brief overview of PC materials. Next, characterization result of a PC material (*i.e.* GeTe) is presented. The structures considered for phase-changing switches are discussed, subsequently, with emphasis on achieving high power handling capability. Finally, the design and simulation results of tunable filters using extracted values for GeTe switch parameters are presented.

5.1. Overview of PC Materials

Phase change materials are considered as one of the future alternatives in non-volatile memory industry. This is due to their fast transition time (ns range), small size (nm cell size), long life cycles ($> 10^{12}$), and the fact that their resistance can be changed

to set or reset the memory. Figure 5.1 shows SEM view of a highly integrated PC memory [137], and cycling performance of a single PC memory cell [138] .

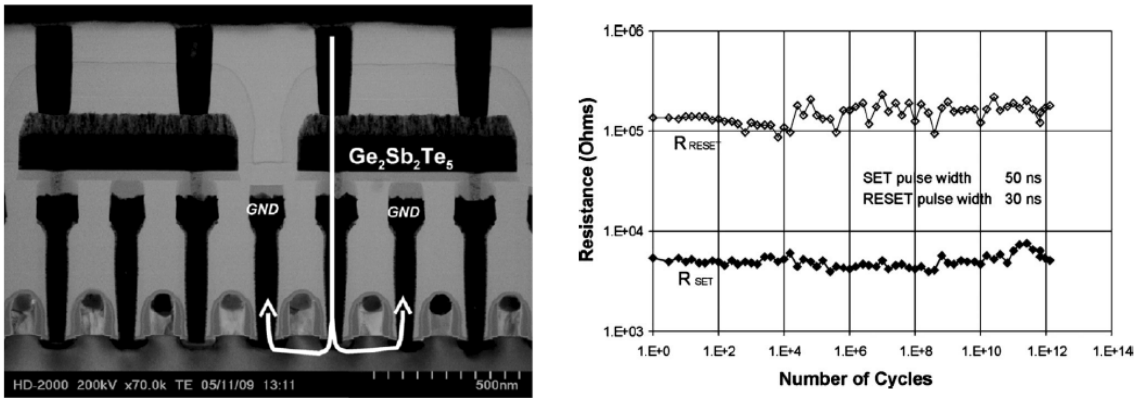


Figure 5.1. 256 MB PRAM using 100nm technology with a cell size of 0.166 μm^2 (left) [137]; cycling performance of the set and reset states of a single PC memory cell (right) [138].

As illustrated in Figure 5.2 [139], PCMs undergo transition between amorphous and crystalline phases, thermally, which is a characteristic of a charcogenide compound. For each transition, a well-controlled heat pulse should be applied either by a laser or using electrical pulses as shown in Figure 5.3. The most popular composition of phase change material is germanium, antimony, and tellurium alloys, $Ge_2Sb_2Te_5$. As an example, the temperature dependent sheet resistance of a 80 nm thick $Ge_2Sb_2Te_5$ is shown in Figure 5.4 [140]. Despite their unique properties, PC materials have not been utilized in RF applications because of their limited power handling capability using the structure used for memories and the relatively higher on-resistance of $Ge_2Sb_2Te_5$ at the crystalline phase.

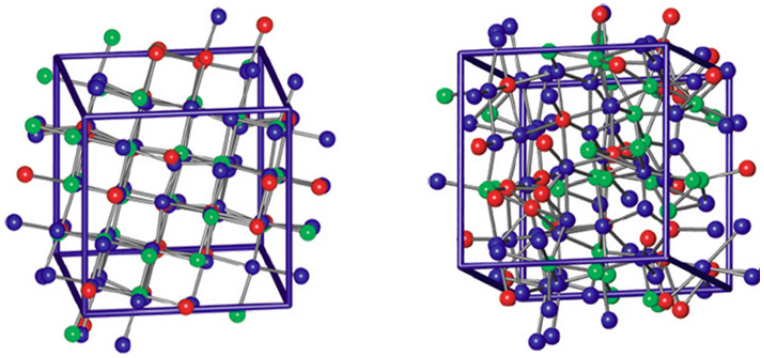


Figure 5.2. 63-atom models of crystalline $Ge_2Sb_2Te_5$ (left) and amorphous $Ge_2Sb_2Te_5$ (right) [139].

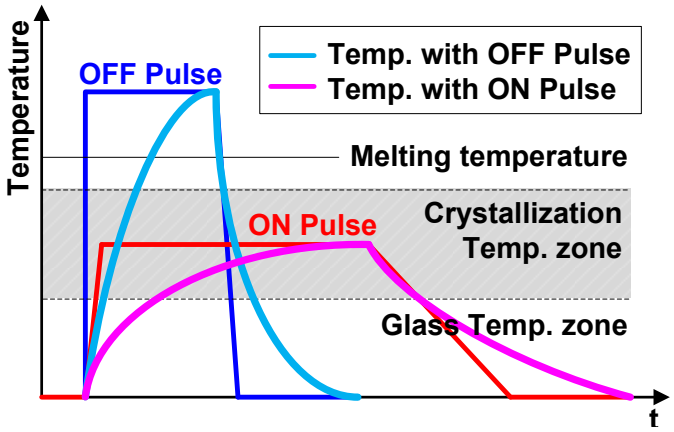


Figure 5.3. Transient temperature distribution of PCM when a required heat pulse for each transition is applied; OFF pulse is for amorphization and ON pulse is for crystallization.

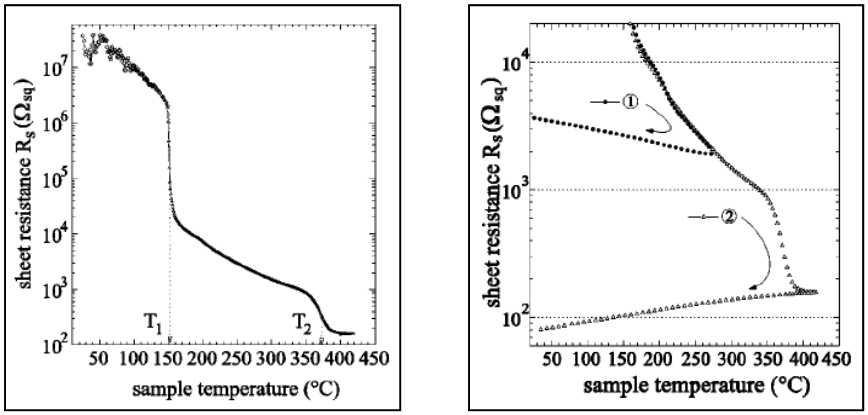


Figure 5.4. Temperature dependence of the sheet resistance in 80 nm thick $Ge_2Sb_2Te_5$ (left); sheet resistance change upon heating up to 270 °C and 420 °C, and subsequent cooling (right) [140].

In designing PC vias (or switches) for RF application, on/off resistance ratio, parasitic capacitances, and phase transition conditions need to be considered, simultaneously. The intrinsic parasitic capacitance and on-resistance of a PC switch at the ideal crystalline phase are defined as [141]

$$C_I = \varepsilon_r \varepsilon_0 \cdot \frac{wl}{t} \quad \text{(Equation 5.1)}$$

$$R_{I,ON} = \rho_{ON} \cdot \frac{t}{wl} \quad \text{(Equation 5.2)}$$

Where *w*, *l*, and *t* are the width, length and thickness of the effective PC area in contact with the electrodes, respectively, and ρ_{ON} is resistivity at the crystalline phase. Considering C_{max} as the maximum allowed parasitic capacitance for a target SRF and R_{max} as the maximum on-resistance to achieve the target level of loss, the conditions $C_I < C_{max}$ and $R_{I,ON} < R_{max}$ should be satisfied [141]. Re-writing these equations with respect to the PC via dimensions, the following expression is obtained [141].

$$\frac{\rho_{ON}}{R_{max}} < \frac{wl}{t} < \frac{C_{max}}{\varepsilon_r \varepsilon_0} \quad \text{(Equation 5.3)}$$

This indicates that larger area and smaller thickness will be beneficial to obtain low on-resistance, at the cost of increased parasitic capacitance. Simplifying Equation 5.3, we can obtain [141]:

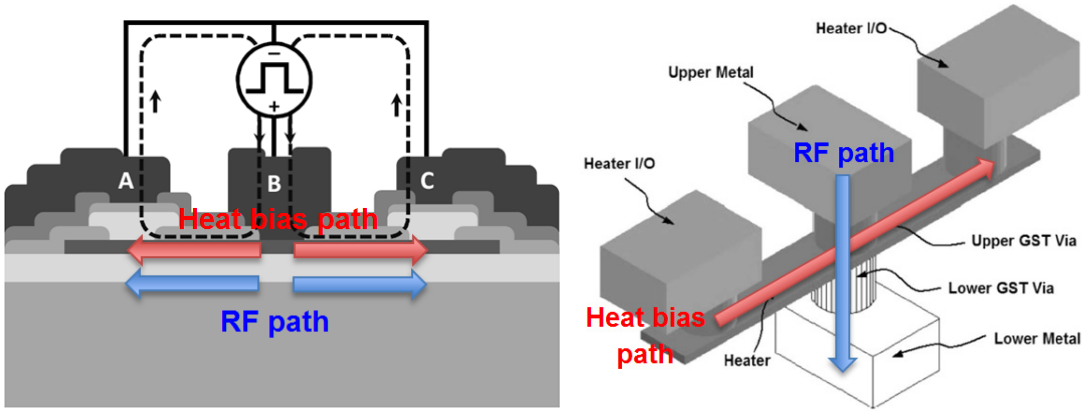
$$\rho_{ON} \varepsilon_r \varepsilon_0 < R_{max} C_{max}. \quad \text{(Equation 5.4)}$$

Depending on the stoichiometric composition of GST, ρ_{ON} varies significantly.

However, ε_r remains pretty constant at about 15. If the target values of R_{max} and C_{max} are 0.1 Ω and 100 fF, the reference value for $R_{max}C_{max}$ will be 10 fs. This value changes depending on the chosen material. As shown in Table 5.1 [140], [142], $Ge_{15}Sb_{85}$ has the smallest on-resistivity. However, the on/off resistance ratio of $Ge_{15}Sb_{85}$ is only around 10^3, which is not sufficient for good isolation at the amorphous phase. Thus, GeTe is the best material for RF switches due to its low on-resistivity and best on/off resistance ratio.

Table 5.1. Electrical parameters of different stoichiometric composition of GST [140], [142].

Material	ρ_{on} (Ω·cm)	ρ_{off}/ρ_{on}	ε_r	$\rho_{on}\varepsilon_r\varepsilon_0$
$Ge_2Sb_2Te_5$	1×10^{-1}	10^5	15	132.75 fs
$Ge_{25}Sb_{75}$	1×10^{-3}	10^3	15	1.33 fs
$Ge_{15}Sb_{85}$	1×10^{-4}	10^4	15	0.13 fs
$Ge_{30}Te_{70}$	1×10^{-1}	10^5	15	132.75 fs
GeTe	2×10^{-4}	10^6	15	0.27 fs



(a) (b)

Figure 5.5. (a) PC vias with direct heating structure [143]; (b) PC vias with indirect heating structure [144].

For phase transition of highly integrated PC vias, heat is mostly controlled by assigning electrical potential or current in the heat path and raising temperature of materials in the heat path by joule heating. If the PC layer is located within the heat path and directly heated up, it is called direct heating method. On the other hand, if PC layer is not directly located in the heat path, but indirectly heated by the heater layer, it is called indirect heating. Figure 5.5 shows a representative PC via structure using each heating method [143], [144]. Direct heating structure (Figure 5.5 (a) [143]) is more commonly used in the memory industry as it provides easier heat control and smaller foot-print. However, high current flow in the heat path can damage any circuits connected with PC via, so additional process steps would be necessary to protect the CMOS transistors. In indirect heating (Figure 5.5 (b) [144]), the heat bias path for phase transition is decoupled from a signal path by using an independently contacted heater electrode. Although indirect heating provides more reliable structure for signal path protection, the heater electrodes should be carefully designed considering effective heat transfer to the PC via.

To design the directly heated PC via, the following conditions need to be considered. As discussed earlier, the phase transition from crystalline-to-amorphous (C-A) phase demands more rigorous heating (bias) conditions whereas the reverse transition (A-C) easily occurs if the heating is sufficient enough to increase the temperature above the phase transition temperature, ~ 250 °C in GeTe. For the C-A phase transition, higher

heating power is necessary, and proper heating duration and quench time are required to prevent the PC material from remaining at the same crystalline phase. For transition to amorphous phase, the cooling time, τ_{th} should be shorter than the material transformation time, τ_{trans} [141],

$$\tau_{th} = R_{th}C_{th} = \rho_k \frac{t}{wl} \cdot c_p wlt \ . \qquad \text{(Equation 5.5)}$$

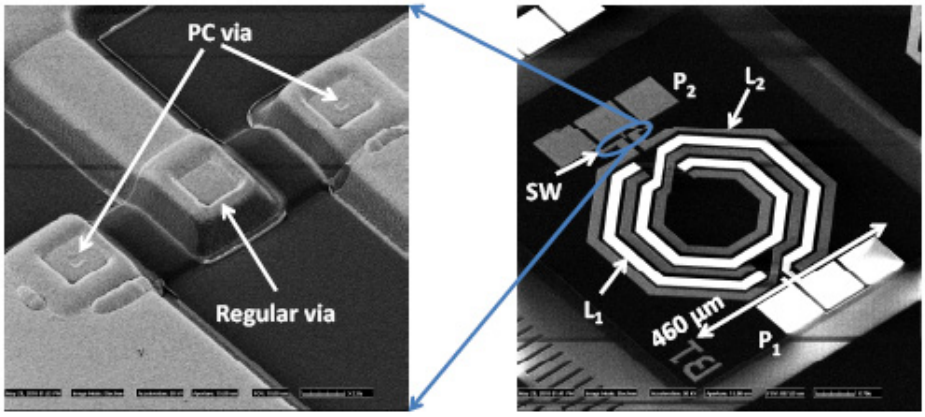
where R_{th}, C_{th}, ρ_k, and c_p are the thermal resistance, thermal capacity, thermal resistivity and heat capacity of the PC area, respectively. Therefore,

$$\tau_{th} = c_p \rho_k t^2 < \tau_{trans} \ . \qquad \text{(Equation 5.6)}$$

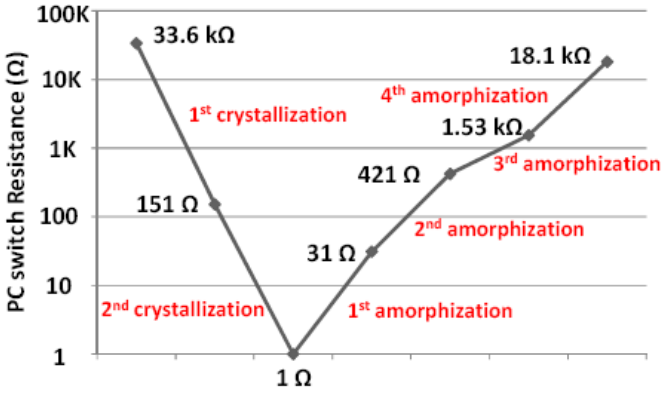
This implies that the maximum thickness of the PC material for the C-A transition will be limited. To design a PC switch, which has better isolation at the amorphous state, it would be more desirable to reduce the area than to increase the thickness in order to avoid large C-A transition time.

PC vias have been previously used to implement tunable inductors, as shown in Figure 5.6 [143]. The two PC vias were incorporated in locations A and C. The phase transition was controlled by GSG probe. Since RF signal and DC bias pulse for the phase transition were applied through the same port using a bias tee, this implementation is not practical for integration with other RF circuitry. As shown in the transition table, this switch requires longer transition time than other PC vias. This is mostly due to the thick PC layer used to reduce the parasitic capacitance; the area of each PC via was 1 μm × 1 μm, and the thickness was 100 nm. To improve the phase-transition time and maintain a

low parasitic capacitance, a thinner PC via with an additional oxide layer is necessary, as proposed herein.



(a)



		Amplitude	Width	Quenching time
Crystallization	1st	1 V	200 µs	200 µs
	2nd	2 V	1 ms	200 µs
Amorphization	1st	0.2 V	2 µs	5 ns
	2nd	3.8 V	2 µs	5 ns
	3rd	8.9 V	2 µs	5 ns
	4th	9.7 V	2 µs	5 ns

(b)

Figure 5.6. (a) SEM view of the tunable inductor with the PC switch; (b) resistance change of PC switch and voltage pulse conditions in crystalline and amorphous phases [143].

5.2. Characterization Result of Thin-Film GeTe

As mentioned earlier, among the variety of stoichiometric composition of PC materials, GeTe (GeTe 50:50) is chosen as it provides the largest on/off resistance ratio and reasonably low on-resistance, showing the best promise for RF ohmic switch application. The 3" GeTe sputter target was acquired from Mitsubishi Materials Corporation [145]. A 150 nm thick GeTe layer was deposited on the silicon wafer coated with 1 μm of silicon oxide, using the Kurt J. Lesker Lab 18-2 sputter [146]. The characterization results for the resistivity change of GeTe layer after heating up to each temperature and gradual cooling is shown in Table 5.2. The resistivity at crystalline phase is in the similar range as the published data in Figure 5.7 [142]. Once the material is crystalized, the on resistance is droped to less than $1/10^4$ of the off-resistance value and its crystalline strucure and resistance is maintained. Due to the measurement tool limit, the sheet resistance in the as-depostied amorphous state could not be measured precisely. The crystalline phase of the GeTe layer can be cleary verified from the X-ray diffraction (XRD) measurement, as shown in Figure 5.8. A clear peak is detected at 30° of 2Θ; this peak is not present at the amorphous state.

Table 5.2. Resistivity vs. maximum heating temperature in 150 nm thick GeTe.

Maximum heating temperature	Resistivity (Sheet Resistance)
180	$> 1.50 \times 10^{1}$ Ω·cm (1.000×10^{6})
200	$> 1.50 \times 10^{1}$ Ω·cm (1.000×10^{6})
220	4.71×10^{-1} Ω·cm (0.314×10^{5})
240	1.58×10^{-3} Ω·cm (1.055×10^{2})
350	1.12×10^{-3} Ω·cm (0.744×10^{2})

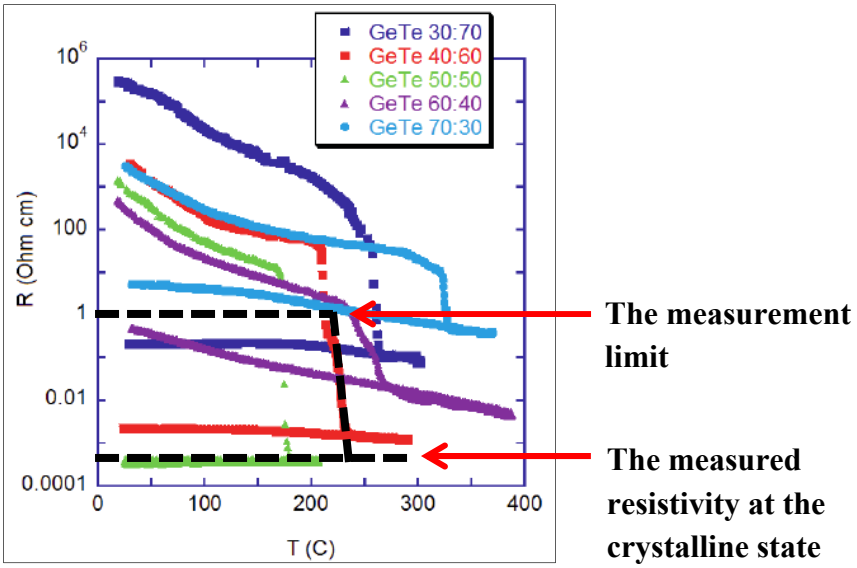
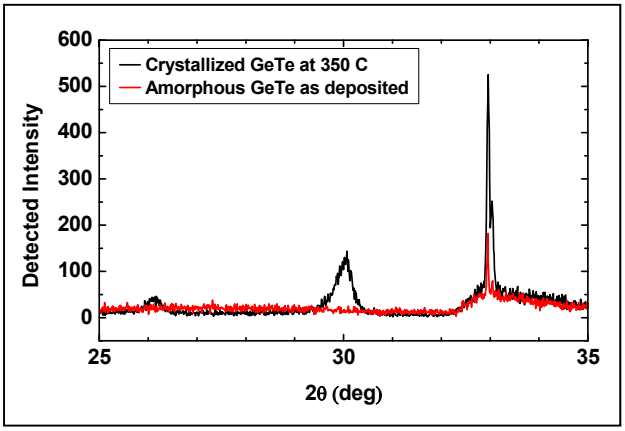
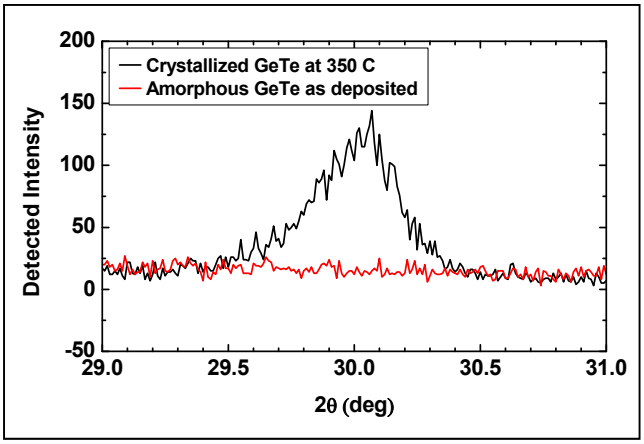


Figure 5.7. R vs. T for Ge-Te films of various stoichiometric composition [142]; the measured on-resistivity and the tool measurement limit are also indicated.



(a)



(b)

Figure 5.8. (a) XRD data scanned from 25° to 35° of 2Θ range; (b) enlarged XRD data from 29° to 31° of 2Θ range.

5.3. PC Switch Structure

To examine if PC materials can make a good RF switch, the RF properties of several PC vias based on GeTe are characterized. For characterization of RF properties of GeTe, PC ohmic switches are fabricated on a passivated silicon substrate. The cross-section view of a directly heated GeTe switch is shown in Figure 5.9. The PC switch stack consists of gold top and bottom electrodes, and thin chrome diffusion barrier layers connecting the electrodes to the GeTe layer through openings in silicon dioxide insulation layers. All metal layers are lift-off patterned. GeTe is sputter deposited with the same target and sputter, which are used for basic material characterization. Silicon dioxide is PECVD deposited at 200 °C, the highest temperature reached during the fabrication process. RF properties of GeTe are extracted from the two GeTe switch configurations shown in Fig. 5.10. The first switch is a single $3\times3\mu m^2$ via (Figure 5.10 (a)) and the second one uses five parallel-connected $2\times2\mu m^2$ vias (Figure 5.10 (b)). For all switches, phase transition is achieved using the direct heating scheme, where the required DC bias for phase transition is applied through the same electrodes as the RF signals.

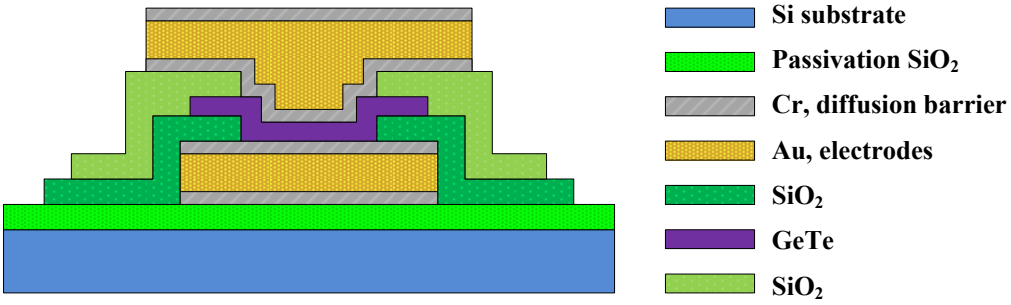
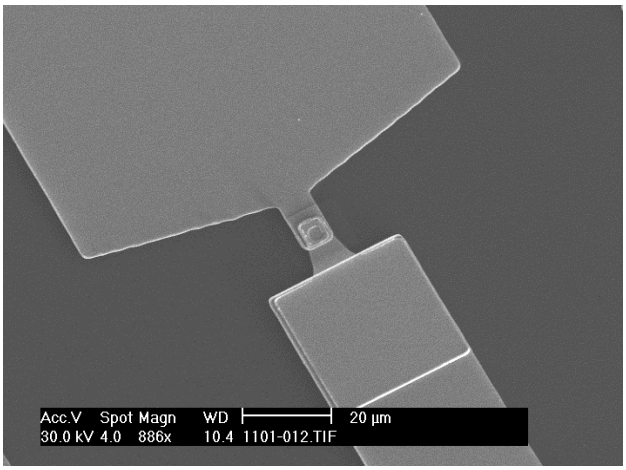
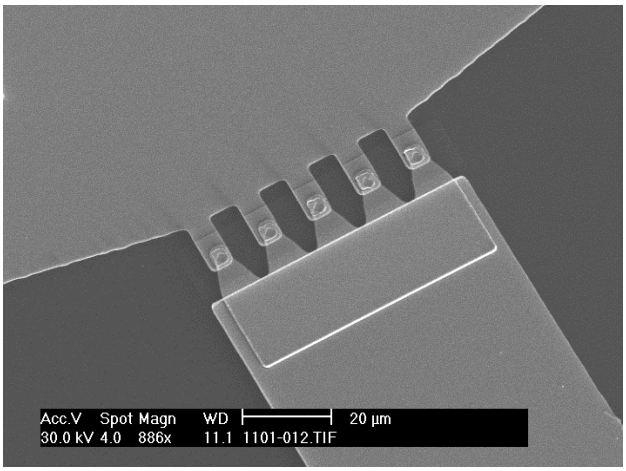


Figure 5.9. A schematic diagram showing the cross-section of a PC switch.



(a)



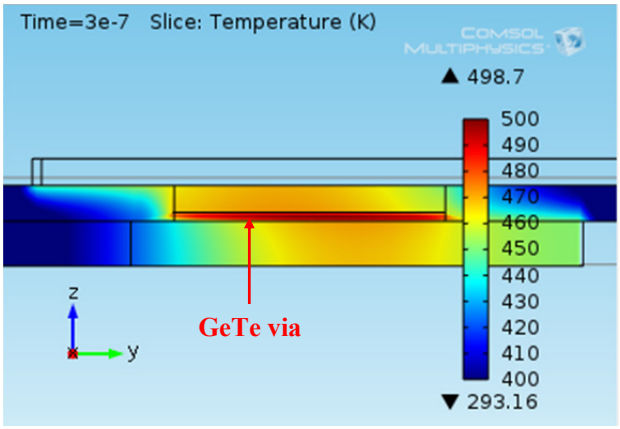
(b)

Figure 5.10. SEM views of (a) a single $3\times3\mu m^2$ via (Design 1) and (b) five parallel-connected $2\times2\mu m^2$ vias (Design 2).

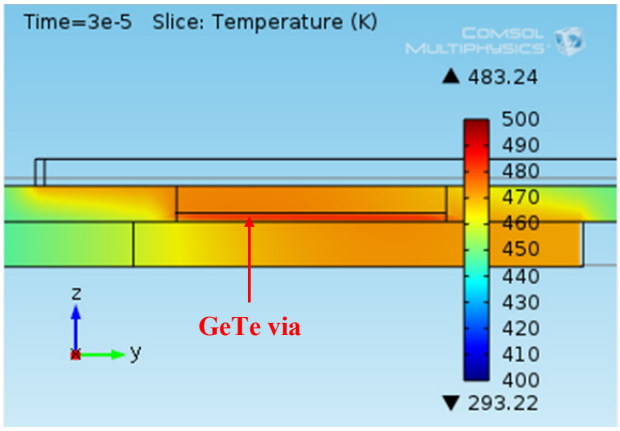
5.4. Phase Transition Analysis and Simulation

Joule heating simulations are performed using COMSOL finite element tool. In these simulations, the structure of the GeTe switch in Figure 5.9 is simulated reflecting the material properties extracted from the high-frequency measurements. Figure 5.11 shows the simulated heat distribution across the switch stack, indicating the bias conditions needed to reach crystallization or amorphization. As shown in Figure 5.11 (a), amorphization (switch OFF) can be reached by applying a 3.5 V DC pulse (~ 600 mW)

of 300 ns, reaching the melting point of GeTe (~ 480 K). As consistent with previous devices, crystallization (switch ON) needs a 2 V DC pulse (~ 100 μW) with longer duration of ~ 30 μs (Figure 5.11 (b)).



(a)



(b)

Figure 5.11. Temperature distribution across the PC switch stack when (a) 3.5 V is applied for 300 ns to amorphize and (b) 2 V is applied for 30 μs to crystallize the switch.

5.5. Measured RF Performance of GeTe Switches

Measured data of fabricated GeTe switches are extracted after building an equivalent lumped element model. Complete RF characterization including RF lumped elements, power handling capability, and switching speed is performed and analyzed.

5.5.1. Intrinsic RF Properties

The equivalent lumped-element model of a two-port GeTe switch is shown in Figure 5.12. Depending on the state of the GeTe via, two different electrical circuits could be used to model its performance (Figure 5.13). In general, the model in Figure 5.13 (a) is utilized to present both states of a properly transitioned GeTe via. R_I is the intrinsic resistance of GeTe, which experiences a large change between amorphous (OFF) and crystalline (ON) states. C_I models the parasitic capacitance of the PC layer. The model at the OFF state, which we newly propose, is shown in Figure 5.13 (b); here, R_{NI} and C_{NI} models the resistance and capacitance of the GeTe grains that undergo incomplete phase transition.

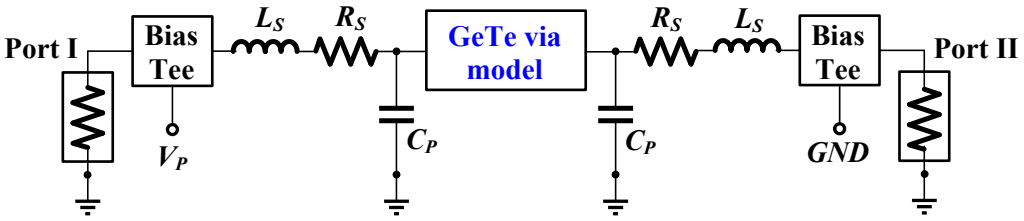


Figure 5.12. Equivalent electrical model of a GeTe switch; the entire model including electrodes and bias control.

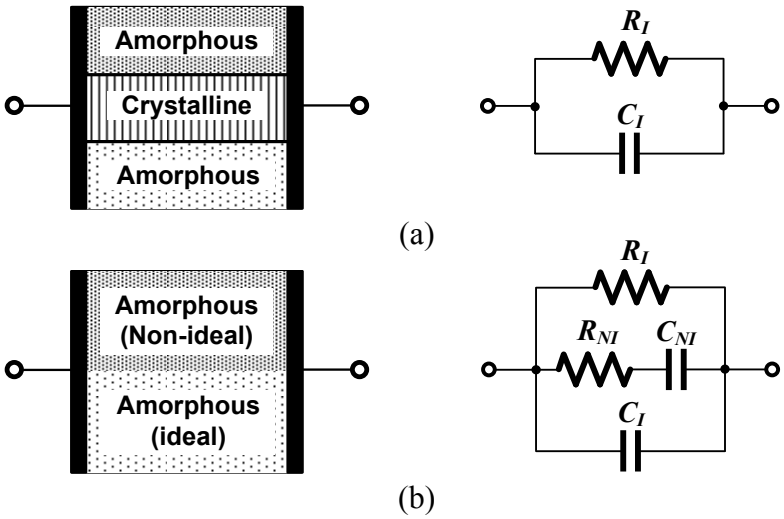


Figure 5.13. Illustrated diagram and equivalent model of GeTe via at (a) crystalline state and (b) amorphous state.

In Figure 5.12, C_P is the parasitic capacitance of the substrate, and L_S and R_S model the routing layer that connects the switch to the probe pads. GeTe is known to have a relatively high permittivity (ε_r >15). Therefore, reduction of the switch size is important to achieve good isolation at high frequencies. As GeTe has a small intrinsic ON resistivity compared to other stoichiometric composition of GST, the dimension of the via can be reduced for a better isolation without sacrificing the insertion loss. From Figure 5.12, the input impedance Z_{11} can be expressed as,

$$Z_{11} = [(Z_S \parallel Z_P) + Z_I] \parallel Z_P + Z_S \,, \qquad \text{(Equation 5.7)}$$

where $Z_S = R_S + j\omega L_S$, $Z_P = 1/j\omega C_P$, and Z_I is the intrinsic impedance of GeTe via. From Equation 5.9, parasitic impedance Z_S and Z_P can be de-embedded from Z_I, using open calibration fixture $Z_{11,O}$ and short calibration fixture $Z_{11,S}$ fabricated on the same substrate. At the ON state, intrinsic resistance R_I of GeTe via can be extracted as

$$R_I \approx re[1/(Y_{11} - Y_{11,O}) - 1/(Y_{11,S} - Y_{11,O})]. \qquad \text{(Equation 5.8)}$$

At the OFF state, the two most dominant lumped element values, R_{NI} and C_I, are extracted as

$$R_{NI} \approx re[Y_{11} - Y_{11,O}]/(im[Y_{11} - Y_{11,O}])^2 \,. \qquad \text{(Equation 5.9)}$$

$$C_I \approx im[Y_{11} - Y_{11,O}]/\omega \,. \qquad \text{(Equation 5.10)}$$

Two different configurations of GeTe switches in Figure 5.10 are fabricated and measured to extract these intrinsic properties. Design 1 is built as a single one-port GeTe

via (3×3 μm^2) while Design 2 is implemented as multiple GeTe vias with a smaller individual via size (2×2 μm^2). On-wafer measurements are performed using the Cascade ACP GSG probes, an Agilent E5061B ENA for low frequency measurement (< 3 GHz), and an Agilent N5242A PNA-X for high frequency (10 MHz–25 GHz) measurements. R_I, R_{NI}, and C_I are measured and extracted using Equations 5.10, 5.11 and 5.12, as shown in Figure 5.14 and Figure 5.15. As expected, Design 2 shows better ON resistance than Design 1, but also has a higher parasitic capacitance. An advantage of Design 2 is that phase transition could be more reliable, as smaller vias can be more uniformly heated and the state of the via is better controlled using the Joule heating method. At the OFF state, R_I is in the MΩ range; thus, R_{NI}, which models the resistance of areas that are not completely amorphized, becomes more dominant at higher frequencies, reducing the effective resistance (Figure 5.14 (b)). Figure 5.15 shows the measured S_{11} of Design 1 and Design 2, compared with the modeled response using the equivalent circuit in Figure 5.12 and Figure 5.13. Each lumped element value is listed in Table 5.3. The measured and modeled responses are in excellent agreement.

Table 5.3. Resistivity vs. maximum heating temperature in 150 nm thick GeTe.

Maximum heating temperature	Resistivity (Sheet Resistance)
180	$> 1.50 \times 10^{1}$ Ω·cm (1.000×10^{6})
200	$> 1.50 \times 10^{1}$ Ω·cm (1.000×10^{6})
220	4.71×10^{-1} Ω·cm (0.314×10^{5})
350	1.12×10^{-3} Ω·cm (0.744×10^{2})

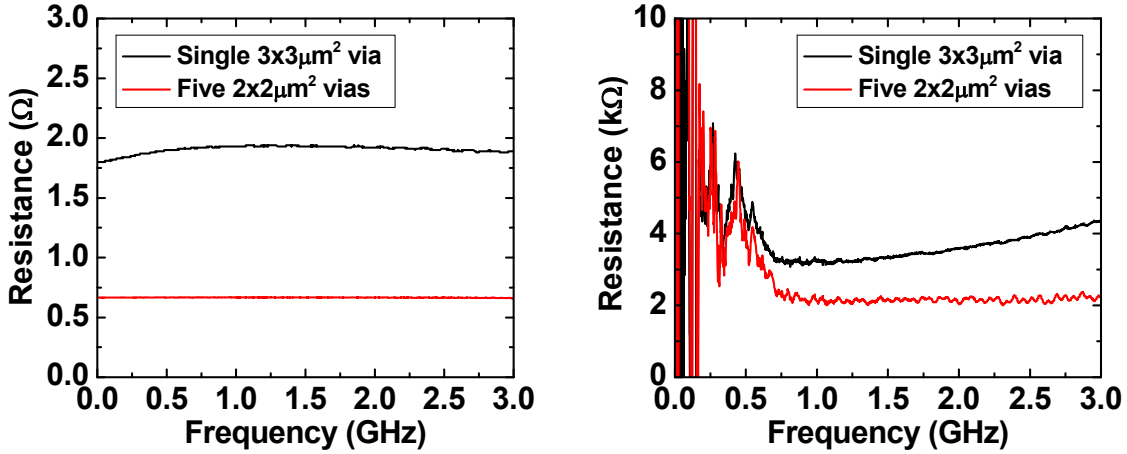


Figure 5.14. Measured resistance of a single 3×3μm^2 via (Design 1) and five 2×2μm^2 parallel vias (Design 2); R_I at the crystalline state (left); R_{NI} at the amorphous state (right).

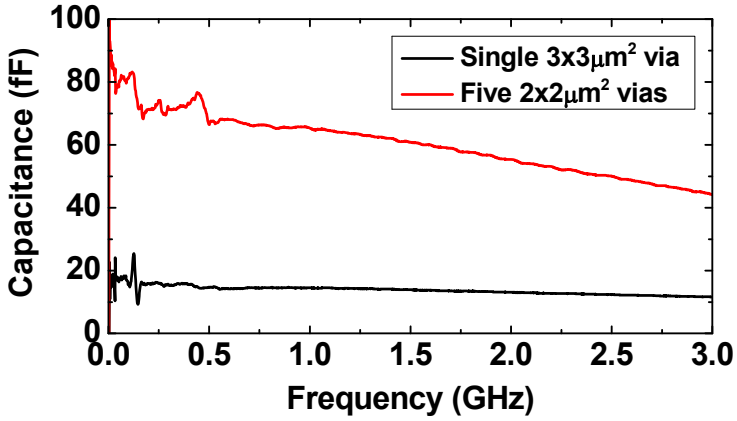


Figure 5.15. Measured intrinsic capacitance (C_I) of the single 3×3μm^2 via and five 2×2μm^2 vias at the amorphous state.

Figure 5.18 (a) and (b) show the measured and de-embedded S-parameters of a two-port 3×3 μm^2 switch (Figure 5.17). To extract intrinsic S-parameters of GeTe via, the contact resistance and pad parasitics are de-embedded using test fixtures fabricated on the same wafer. The de-embedded insertion loss is less than 1 dB while isolation is better than 18 dB up to 25 GHz. This switch exhibits comparable performance to that of MEMS- and solid-state-based switches.

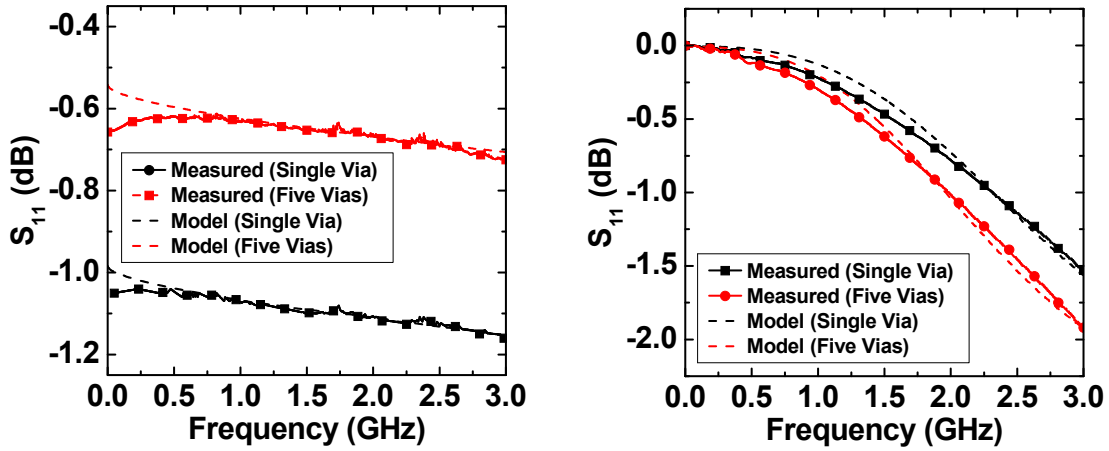


Figure 5.16. Measured S_{11} compared with simulation result using equivalent lumped element models; (left) crystalline state; (right) amorphous state.

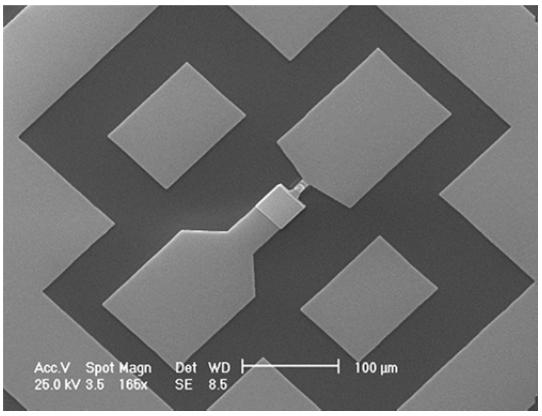


Figure 5.17. SEM view of a two port 3 × 3 μm^2 PC via.

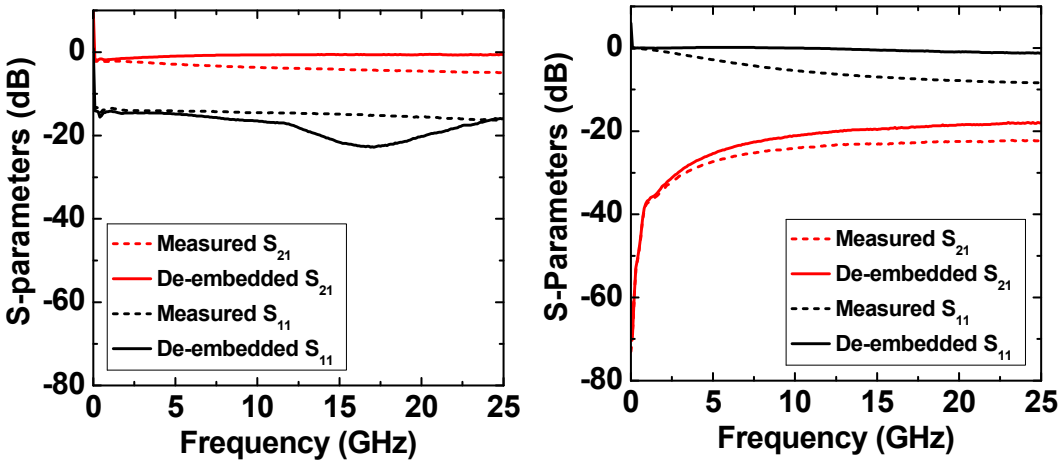


Figure 5.18. Measured and de-embedded S-parameters at the (left) crystalline and (right) amorphous state.

5.5.2. Power Handling Capability and Linearity

Due to the thermal transition mechanism of GeTe, the power handling capability can be a concern for phase change switches. To analyze IIP_3 and P_{1dB} of a GeTe switch, the Agilent ADS simulation tool is used similarly as in Chapter III. Since the purpose of this simulation is to analyze the frequency dependency of IIP_3 and P_{1dB}, simple one-dimensional transient conduction (Equation 5.13) is utilized without consideration of additional heating mechanism, dissipation factor, and nucleation behavior [147] of PC materials.

$$\frac{\partial T}{\partial t} = \frac{1}{\rho V c} \cdot \left(- hA_{surf} \right) \cdot (T - T_{\infty}) = - \frac{1}{C_{th} R_{th}} \cdot (T - T_{\infty}) \quad \text{(Equation 5.11)}$$

where C_{th} and R_{th} is thermal capacitance and thermal resistance, respectively. Thermal time constant, $C_{th}R_{th}$ decides the frequency response of thermal behavior in GeTe switch. For a typical GeTe switch considered in this work, this thermal constant is in the range between 2 and 4 ns, which corresponds to 250 MHz and 500 MHz in the frequency domain.

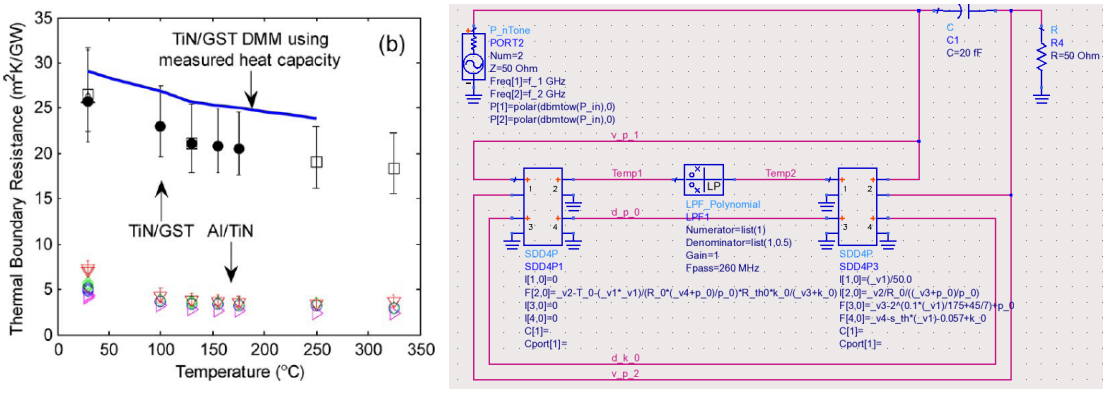
As shown earlier in Figure 5.7, the electrical resistivity of GeTe varies according to the temperature change although it is not as significant change as complete phase-transition. This temperature variation causes non-linearity in GeTe switches, and more variation is observed in the amorphous state. R_{th} is also known to show variation as temperature changes, as shown in Figure 5.19 (a) [148]. Therefore, the following

equations are applied to the electro-thermal model of the GeTe switch in Figure 5.19, in order to calculate the nth-iterated electrical resistance (R_{el}) and R_{th}, respectively.

$$T_n = T_0 + \frac{V_{RF}^{\ 2}}{R_{el,n-1}} \cdot R_{th,n-1}. \qquad \text{(Equation 5.12)}$$

$$R_{el,n} = R_{el,0} + a^{(bT_{n-1}+c)}, \quad R_{th,n} = R_{th,0} + dT_{n-1} + e \qquad \text{(Equation 5.13)}$$

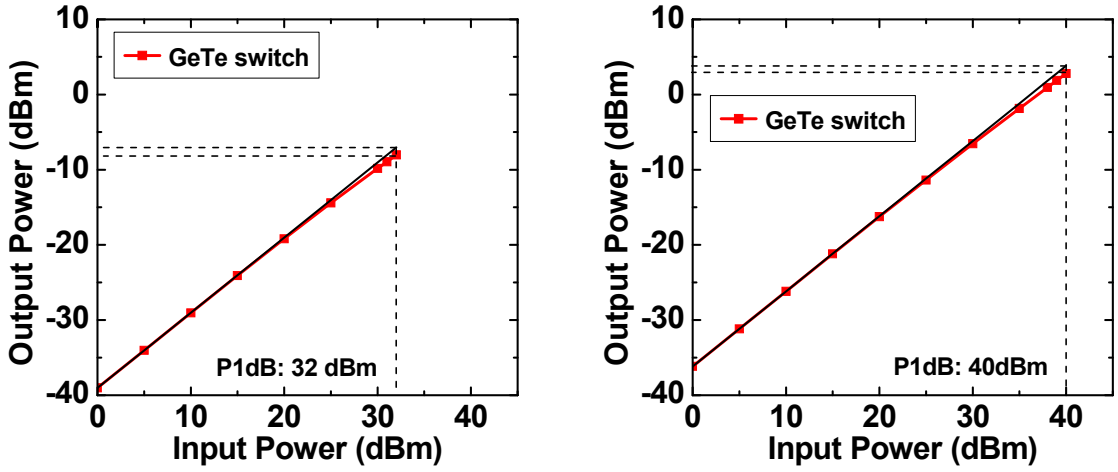
where T_n, $R_{el,n}$, and $R_{th,n}$ is temperature, electrical resistance, and thermal resistance at nth iteration, respectively. For more accurate simulation result, other constants (a, b, c, d, e) included in Equation 5.15 should be adjusted according to characterization result.



(a) (b)

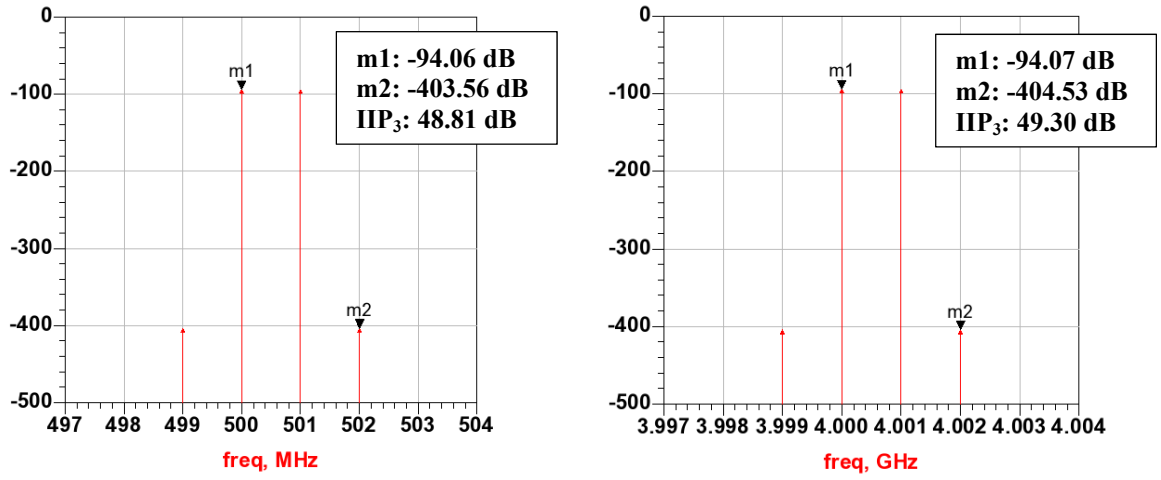
Figure 5.19. (a) Thermal resistance of GST vs. temperature [148]; (b) ADS schematic with electro-thermal model of a GeTe switch for non-linearity analysis.

P_{1dB} of a 3 × 3 μm^2 GeTe switch in the amorphous state is simulated, using the simulation setup in Figure 5.19. As shown in Figure 5.20, P_{1dB} with 1 GHz of RF input signal is better than P_{1dB} at 500MHz. This is because the cut-off frequency ($f_{cut-off}$) of the first order filter in Figure 5.19 is located at 500 MHz, mitigating a non-linear signal above this frequency.



(a) (b)

Figure 5.20. Simulated P_{1dB} of a 3 × 3 μm^2 GeTe switch in the amorphous state; (a) 500 MHz and (b) 1 GHz.



(a) (b)

Figure 5.21. Simulated IIP_3 of a 3 × 3 μm^2 GeTe switch in the amorphous state; (a) 500 MHz with 1 MHz offset and (b) 4 GHz with 1 MHz offset of two-tone input signal.

As shown in Figure 5.21, IIP_3 of a 3 × 3 μm^2 GeTe switch in the amorphous state is also simulated. As expected from P_{1dB} result, IIP_3 with RF input signal above $f_{cut\text{-}off}$ is better than IIP_3 below $f_{cut\text{-}off}$.

Both P_{1dB} and IIP_3 is measured from the fabricated 3 × 3 μm^2 GeTe switch. As shown in Figure 5.22, P_{1dB} of GeTe switch is above 20 dBm at both crystalline and amorphous states. Although P_{1dB} could not be accurately extracted due to tool limitations and it may be higher than 20 dBm, GeTe switch is proved to handle sufficiently high input power, suitable for use in reconfigurable RF front-ends. P_{1dB} could also be potentially improved by optimal choice of electrodes and diffusion barriers.

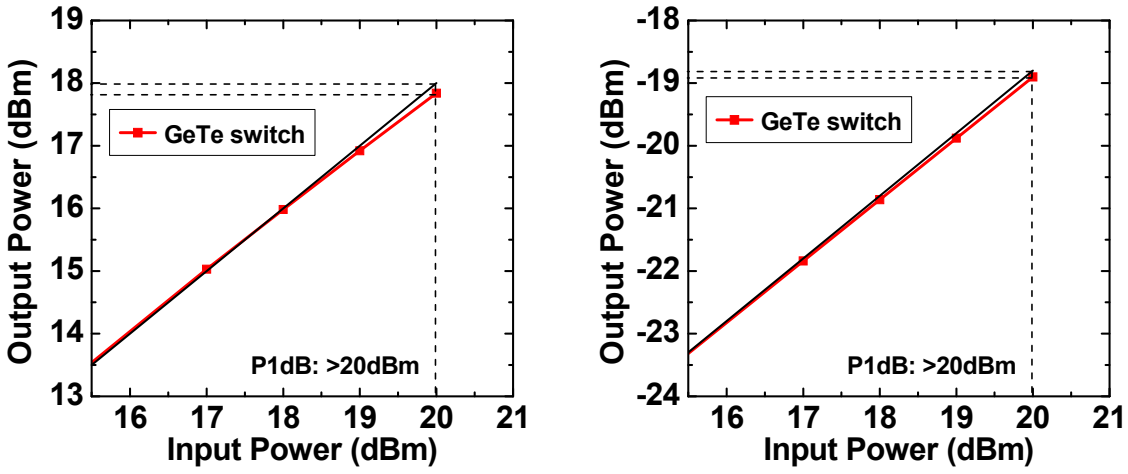


Figure 5.22. Measured P_{1dB} of a directly heated 3 × 3 μm^2 PC via; (a) crystalline and (b) amorphous states at 1GHz.

IIP_3 of the GeTe switch is measured using two RF sources, isolators, a power combiner, and a spectrum analyzer. As noted earlier, since the amorphous state has a larger temperature coefficient of electrical resistance, IIP_3 of the amorphous state is expected to be worse than the crystalline state. This is consistent with the measurement result in Figure 5.23 (a) and (b); IIP_3 at the crystalline state is extracted to be 37 dBm while the IIP_3 at the amorphous state is around 33 dBm.

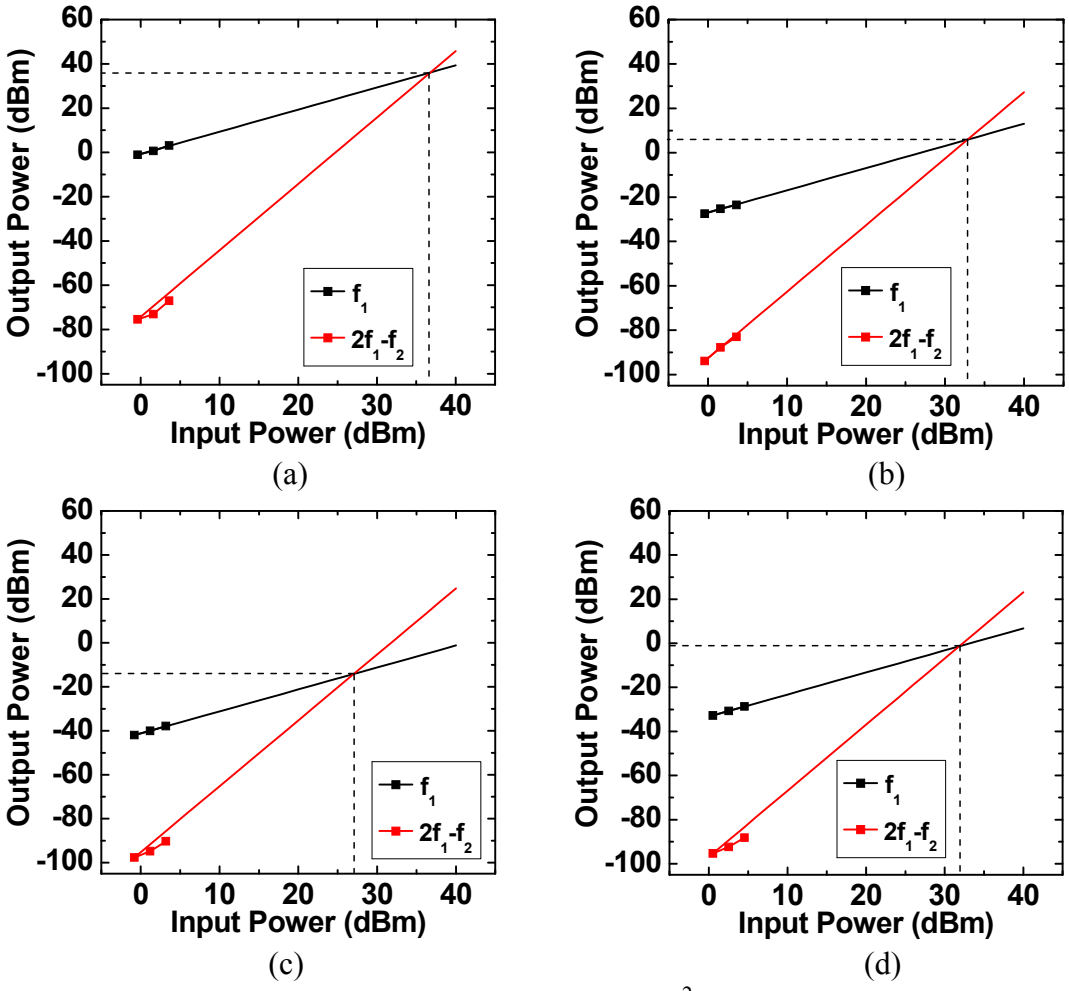


Figure 5.23. Measured IIP_3 of a directly heated 3×3 μm^2 PC via; (a) crystalline state with 50 kHz of frequency offset at 3.9 GHz; (b) amorphous state with 50 kHz of frequency offset at 3.9 GHz; (c) amorphous state with 50 kHz of frequency offset at 500 MHz; (d) amorphous state with 50 kHz of frequency offset at 2 GHz.

Also as expected in the simulation result using electro-thermal model, the switch linearity is worse at lower frequencies (Figure 5.23 (c) and (d)). At the amorphous state, IIP_3 at 500 MHz is limited to 27 dBm while IIP_3 at 2 GHz is around 32 dBm. At all states and frequencies, the measured IIP_3 of the GeTe switch is better than CMOS switches and comparable to high-performance MEMS switches.

5.5.3. Switching Speed

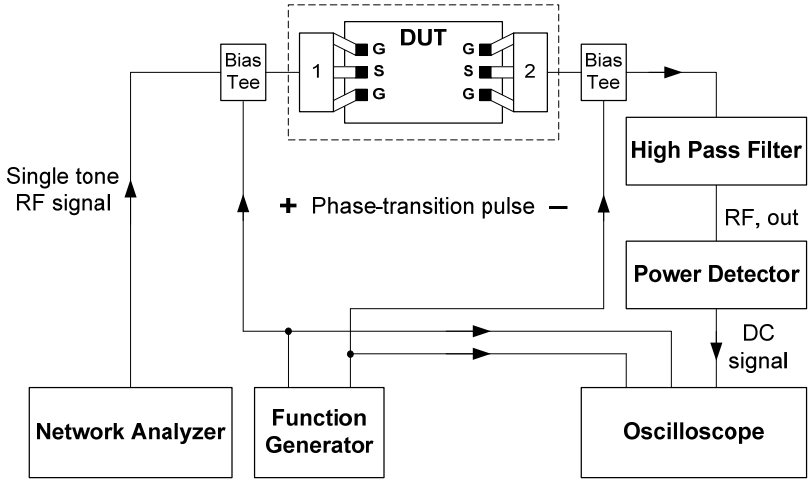


Figure 5.24. Equipment setup diagram for switching speed measurement of two-port GeTe switch.

The setup used for measuring the switching speed is shown in Figure 5.24. As explained earlier, crystallization requires moderate level of heating and gradual trailing of the heater bias. Figure 5.25 shows the crystallization timing diagram. The crystallization time including the stabilization time is less than 20 μs. As shown in Figure 5.26, the required pulse width for amorphization is less than 500 ns. The total switching speed of the GeTe via is thus limited by the crystallization time. With sizing the via and a better choice of electrodes and diffusion barriers, heat transfer to GeTe via can be made more efficient and the switching speed can be further improved.

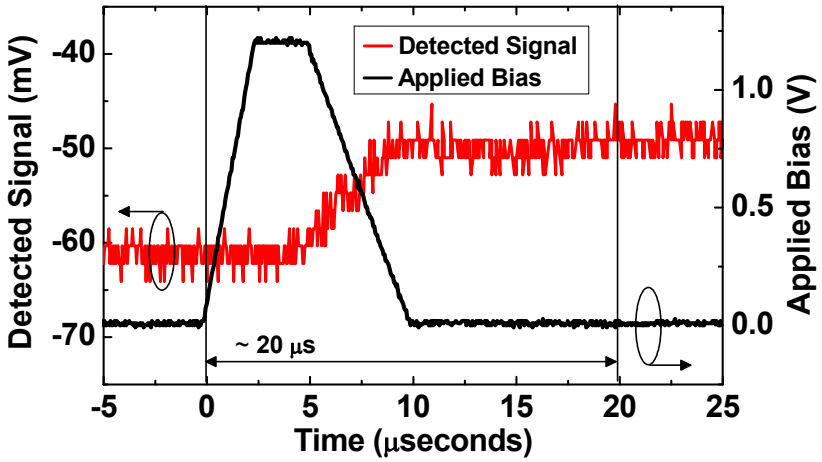


Figure 5.25. Timing diagram when a 1.2 V pulsed bias with duration of 5 μs and falling time of 5 μs is applied to the switch for crystallization; the total switching time including stabilization is around 20 μs.

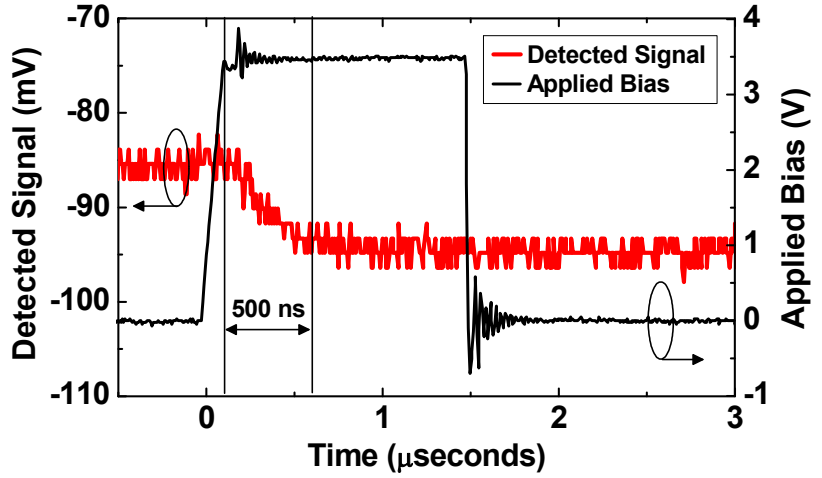


Figure 5.26. Timing diagram when 3.5 V bias with duration of 1.5 μs is applied to the switch for amorphization.

In this chapter, fundamental RF properties of phase change switches using GeTe were discussed. It was shown that the resistance ratio between the crystalline and amorphous states reaches 10^5, which is close to the bulk material property and sufficient for most switching applications. Overall, RF switches using GeTe can provide better

switching speed and higher integration density than conventional MEMS switches. When monolithically integrated with MEMS passive components, such as high-Q inductors and varactors shown in Chapter 2, this switch technology can be used to implement reconfigurable RF modules. To become a viable solution, the switch reliability should be further improved. Possible filter architectures using phase change switches are described in the final chapter of this thesis.

CHAPTER 6.

CONCLUSIONS AND FUTURE DIRECTIONS

6.1. Summary

In this thesis, a versatile tunable RF MEMS platform fabricated using a low-temperature and low-cost surface micromachining was described that offered high-performance RF fixed and tunable passive components. Several high-performance components were developed, including a temperature-stable wide tuning range MEMS capacitor, high-Q coupled inductors, and capacitive switches. The same fabrication technology was further used to implement a fully integrated MEMS tunable filter. The insertion loss of the fabricated filter at all tuned states (from 600 MHz to 1 GHz) is less than 3.5 dB, while the 3dB-bandwidth of the filter is maintained within 13 to 14 %. Shape factor of the filter is better than four and can be improved by optimizing the layout of the inductors and reducing the substrate coupling. Measured shift in the center frequency of the filter is less than 1.5 % across 100 °C of temperature change and its tuning speed is better than 80 μs. The IIP_3 is limited to 20 dBm when the capacitors are half tuned but is larger at the initial state. The filters were packaged using a low-cost polymer packaging process and the performance of the filters was not degraded after they were packaged. As future work, the design of the tunable capacitors will be further

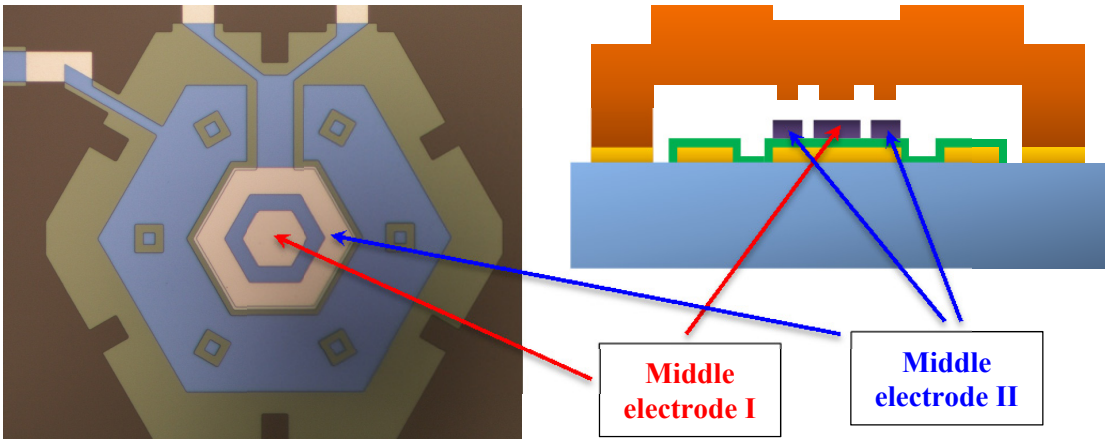
optimized and the fabrication technology will be extended to include a wafer-level hermetic packaging process.

Even though the presented tunable filter exhibited record high performance at UHF, better tuning speed and a more reliable tuning control are still necessary before these devices can be adopted in the commercial market. For this purpose, another tuning mechanism based on PC materials was proposed. Using this later approach, the size of tunable devices can be reduced significantly. GeTe is used as the phase change material as it provides the best conductivity and good resistance change ratio compared to other GST stoichiometric composition. The phase transition from as-deposited amorphous state to crystalline state was verified from resistance change and x-ray refraction measurement. Several GeTe switches were fabricated and tested for characterization of fundamental RF properties. The fabricated GeTe switch shows an ON resistance of < 0.7 Ω and the OFF resistance of > 100 kΩ, indicating the resistance change ratio of > 10^5. The measured 1dB compression point and IIP_3 of the switch are better than 19 dBm and 29 dBm, respectively. When integrated with MEMS passive components, this switch technology can be used to implement next-generation reconfigurable RF modules.

6.2. Future Work - Tunable RF MEMS Platform

The proposed tunable RF MEMS platform can be utilized for a variety of applications. The design of the tunable capacitor can be further improved for better reliability and performance. One of the possible improvements to the capacitive switches is the extension of the tuning range and resolution. The tunable bandpass filter can also be designed for other functionalities such as bandwidth tunability.

6.2.1. Capacitive Switch with Multiple Tuning Steps



(a) (b)

Figure 6.1. (a) Microscope image of capacitive switch after deposition of the middle electrode layer; (b) cross-section view of a capacitive switch with multiple tuning steps.

Tuning range of conventional capacitive switches is normally limited and is less than the designed value because of surface roughness and warping of the released membrane. With the addition of a floating middle electrode on the bottom dielectric layer, the capacitance value at the down state is simply decided by the layout of the middle and bottom electrodes, while ohmic contact resistance between the top and the middle electrode decides the Q [149]. Using this approach, a large capacitance on:off ratio can be achieved [149]. Additional tuning stage could be introduced, by patterning the middle electrode into separate parts, as shown in Figure 6.1. Using this design, the membrane contacts the middle electrodes in different stages controlled by the bias voltage and thus additional tuned states become available, achieving a much wider discrete tuning range than conventional designs.

6.2.2. Tunable Bandpass Filter with Bandwidth Tunability

Another useful feature that could be added to MEMS bandpass filters is bandwidth tunability. The 3D model in Figure 6.2 shows a possible implementation of a tunable bandwidth filter. This filter is designed in a third-order lumped-element configuration with capacitive coupling. The coupling value controls the bandwidth and can be tuned by changing the value of the MEMS capacitors. The expected filter performance simulated using the equivalent lumped element model of its subcomponents is shown in Figure 6.3. The center frequency of the filter can be maintained at 1 GHz, while the bandwidth is tuned from 100 to 400 MHz.

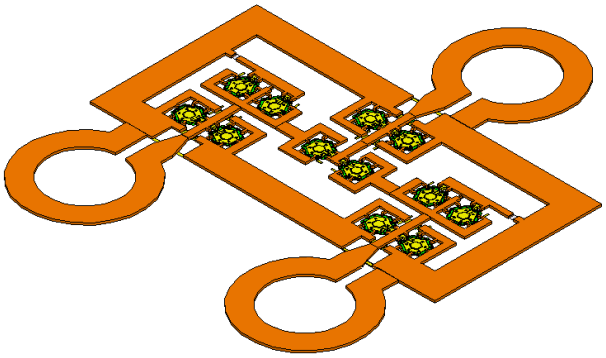


Figure 6.2. 3D view of a third-order tunable bandpass filter with bandwidth tunability.

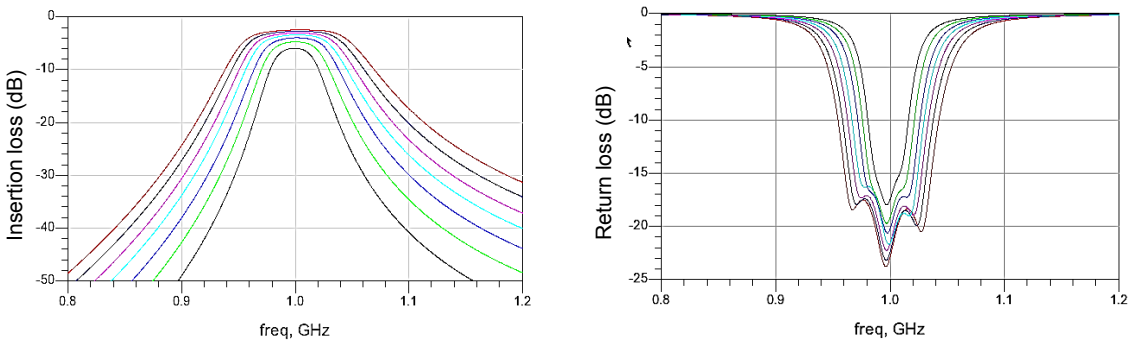


Figure 6.3. Simulated filter response using the lumped element model; insertion loss (left); return loss (right).

6.3. Future Work - PC Switches and Applications

In Chapter 5, characterization results of ohmic switches using GeTe as the resistance change layer have been presented and discussed. Although the measured RF performance of these switches is promising, the switch stack should be modified to include a separate heater layer. In this chapter, more advanced switch structures considering biasing issues will be discussed. Next, a tunable filter design using GeTe switches as the reconfigurable components will be presented. Extension of this work includes fabrication and characterization of the new switch structure and PC filters.

6.3.1. Phase Change Switch with Separate Heat Bias and Signal Electrodes

Figure 6.4 illustrates the cross-section view of a PC switch having separate control lines for the heater bias and the RF signal. In this new switch structure, the resistance of the RF path and the heater line can be independently assigned, while still benefiting from the advantages of the direct heating scheme.

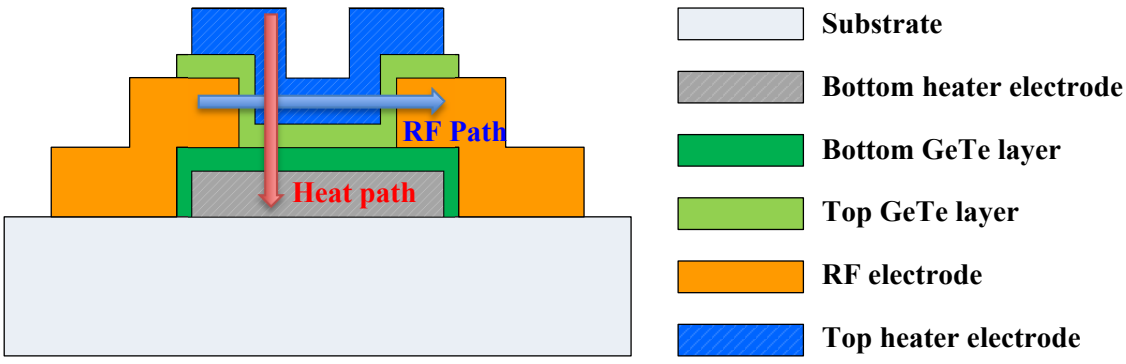


Figure 6.4. A schematic showing the cross-sectional view of a directly heated phase change switch with separate lines for the heater bias and RF signals.

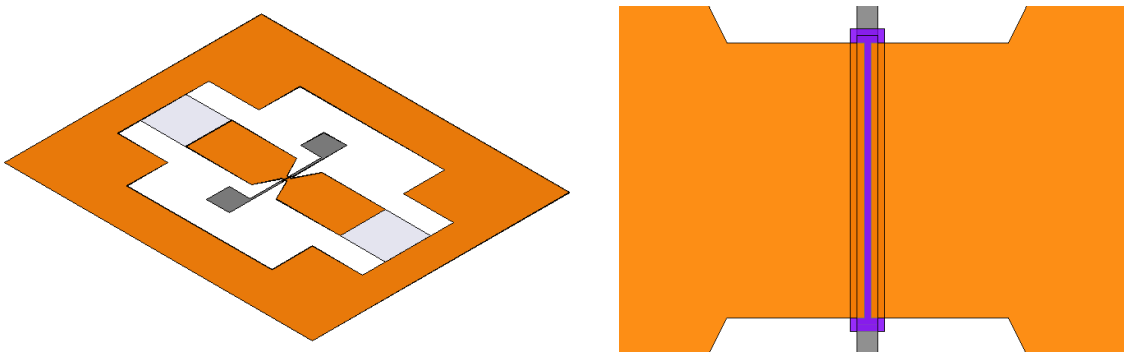


Figure 6.5. 3D layout of the phase change switch shown in Figure 6.4; 3-D view (left) and top-down view (right).

For phase transition of this switch, a DC bias is assigned between the top and bottom heater electrodes. Large resistance level, proper for the heating condition, can be maintained even when only one of the biasing electrodes (*e.g.* the bottom electrode) is composed of a high-resistivity material such as titanium nitride (TiN) [150] or tantalum nitride (TaN) [144]. If the top electrode is built with a higher-conductivity metal such as platinum (Pt) or tungsten (W), which have good thermal properties as well, low loss at crystalline state is also achievable. There is a trade-off between insertion loss and return loss, depending on the choice of materials and the overlap between the bias and RF electrodes. 3-D electromagnetic simulation results of possible configurations of this switch structure are shown in Figure 6.6. For proper choice of the electrode material, heat simulation and electrical simulations are performed and compared together. Heat simulation using W as the heater electrodes is shown in Figure 6.7.

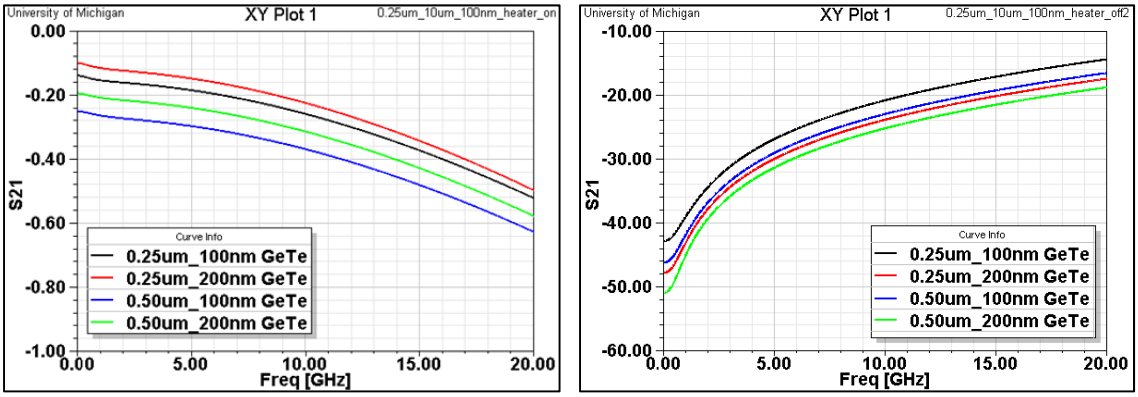


Figure 6.6. Simulation result with different overlapped size and GeTe layer thickness; insertion loss at crystalline state (left); isolation at amorphous state (right).

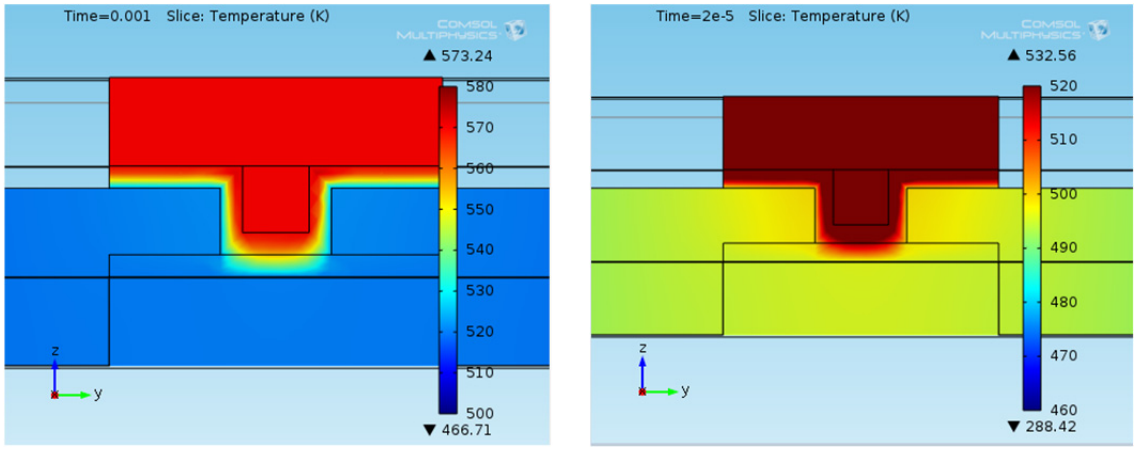


Figure 6.7. Heat simulation result of the PC switch; when 4 mA is applied for 1 ms in the amorphous state (left); 250 mA is applied for 20 μs in the crystalline state (right).

6.3.2. Design of Tunable Filters Using PC Switches

The equivalent switch lumped-element model shown in Figure 5.13 was used to design a tunable bandpass filter, tuned from 800 MHz to 660 MHz having 25 MHz of bandwidth (Figure 6.8). This filter is in a second-order capacitively coupled resonator configuration, where all coupling and matching capacitors as well as the capacitors in the resonator tanks are tuned for optimal performance at each tuned state. The insertion loss

and return loss of the filter is simulated using Agilent ADS and the result is shown in Figure 6.9. Detail filter specifications at each tuned state are summarized in Table 6.1. Considering the achievable Q of inductors and MIM capacitors integrated with PC switches, proper inductance and capacitance values were selected to achieve the maximum total Q for each resonator tank. This filter, if successfully implemented, will be the lowest-loss tunable filter at the UHF range. Needless to say, it will also be the first implementation of a filter using phase change materials.

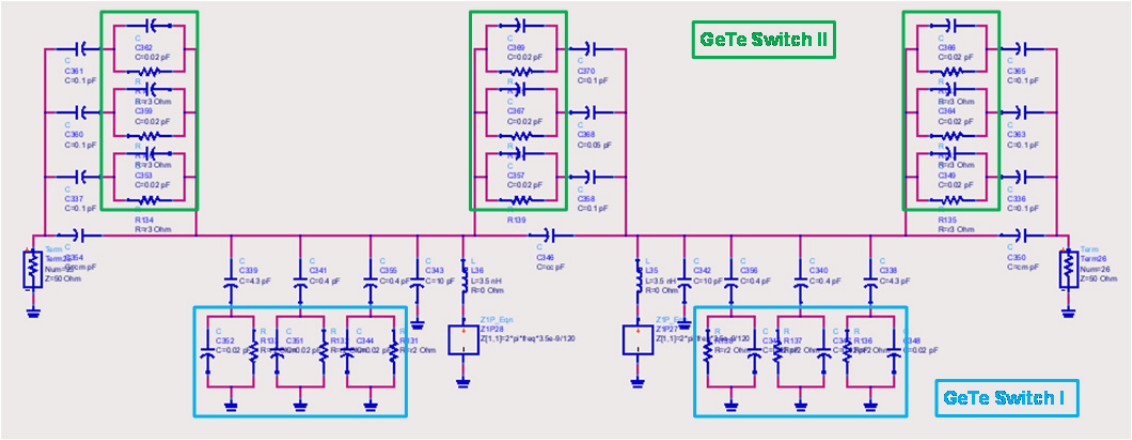


Figure 6.8. Equivalent circuit model for a 2nd-order coupled resonator filter initially centered at 800 MHz. Tuning is achieved using GeTe capacitive switches.

The layout and simulation results of another second-order tunable bandpass filter using PC switches are shown in Figure 6.10. This filter is tuned from 1 GHz down to 600 MHz, a similar tuning range as the MEMS tunable bandpass filter implementation discussed in Chapter 3. Due to the benefits of PC switches, the filter size can be significantly reduced compared to the similar filter design using tunable MEMS platform.

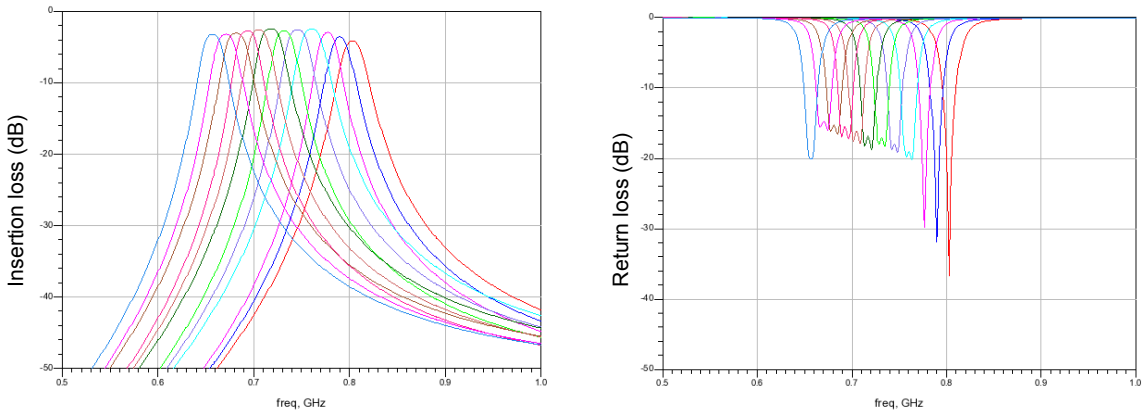
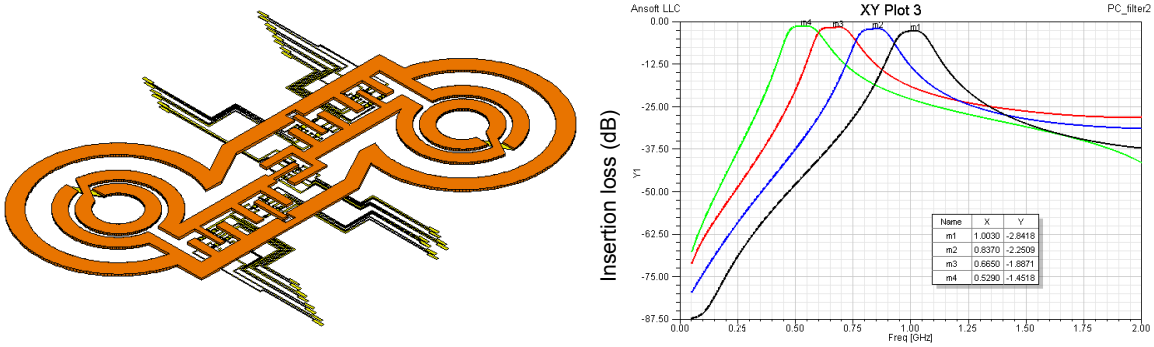


Figure 6.9. ADS simulation results for the insertion loss (left) and return loss (right) of a phase change filter.

Table 6.1. Simulated filter specifications at each tuned stage.

Center Frequency	Insertion Loss	3dB Bandwidth	C_C, C_M, C_R
804 MHz	4.2 dB	24 MHz	200 fF, 1.0 pF, 10.0 pF
790 MHz	3.6 dB	23 MHz	200 fF, 1.0 pF, 10.4 pF
776 MHz	2.9 dB	21 MHz	200 fF, 1.0 pF, 10.8 pF
760 MHz	2.5 dB	26 MHz	300 fF, 1.1 pF, 11.2 pF
746 MHz	2.6 dB	25 MHz	300 fF, 1.1 pF, 11.7 pF
733 MHz	2.7 dB	23 MHz	300 fF, 1.1 pF, 12.2 pF
719 MHz	2.5 dB	26 MHz	350 fF, 1.2 pF, 12.6 pF
706 MHz	2.6 dB	24 MHz	350 fF, 1.2 pF, 13.1 pF
694 MHz	2.7 dB	23 MHz	350 fF, 1.2 pF, 13.6 pF
682 MHz	3.1 dB	25 MHz	400 fF, 1.3 pF, 14.0 pF
671 MHz	3.2 dB	24 MHz	400 fF, 1.3 pF, 14.5 pF
659 MHz	3.4 dB	23 MHz	400 fF, 1.3 pF, 15.1 pF



(a) (b)

Figure 6.10. (a) 3D layout of a second-order tunable bandpass filter using phase change switches; (b) HFSS EM simulation result at each tuning stage.

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BIBLIOGRAPHY

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