Ultra-Low Power Optical Interface Circuits for Nearly Invisible Wireless Sensor Nodes

by

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To my parents,

my family in Korea,

and my late grandfather,

with love and gratitude

for precious memories

and sincere support

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CHAPTER 1

Introduction

1.1 Background

In the past few decades, technology scaling and economy of scale of semiconductor devices have led to rapid advances in the field of integrated circuits [1]. Driven by such progress, technologies that were once considered far-fetched imaginations have taken forms in many aspects of modern day lives. For instance, smartphones have undoubtedly reshaped our lives with shrinking size, increasingly versatile features, and more powerful computing capability. In fact, a typical smartphone being used these days is more powerful than a workstation from the 1980's, despite being several orders smaller in volume. In 1972, Gordon Bell formulated the Bells Law of Computer Classes [2], which described how the computing classes would evolve and create new markets and applications. Bells Law also correctly predicted that every decade, computing classes would shrink in volume by roughly 100$\times$ [3], which was confirmed by the introduction of small desktop PCs, laptop computers, and hand-held devices such as smartphones (Figure 1.1). According to this trend, the next class of computing will be cubic-millimeter-scale in volume and will be much more prevalent than smartphones are today, opening up yet another space of new applications.

One such computing platform that promises the future of electronics is miniaturized wireless sensor node. In 1999, the "Smart Dust" concept was proposed [4], envisioning a sensor node with the size of grain of salt, with focus on wireless communication and networking [5]. Since then, wireless sensor nodes have been a popular topic of research in the cyber-physical systems community, leading up to the concept of "Internet of Things" [6], in which every object and in-

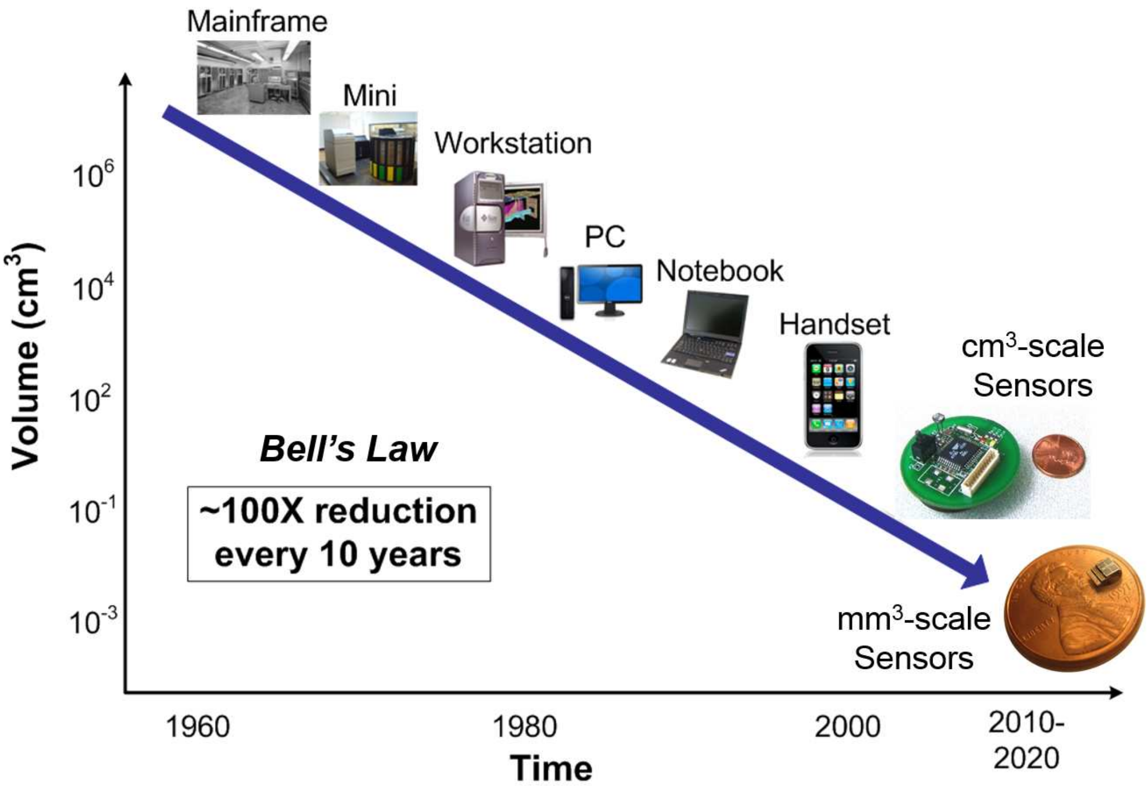


Figure 1.1: Bells Law predicted the evolution and miniaturization of computing classes.

formation surrounding our daily lives is electrically and wirelessly connected to offer ubiquitous object-identification and wireless sensing through massive networks of sensors. However, currently available wireless sensor nodes are limited to printed circuit board based designs that are 1 cm^3 or larger dimension [7], which is too bulky to be considered as "Dust." Furthermore, several wireless sensor node designs in literature often do not include battery as part of the system volume.

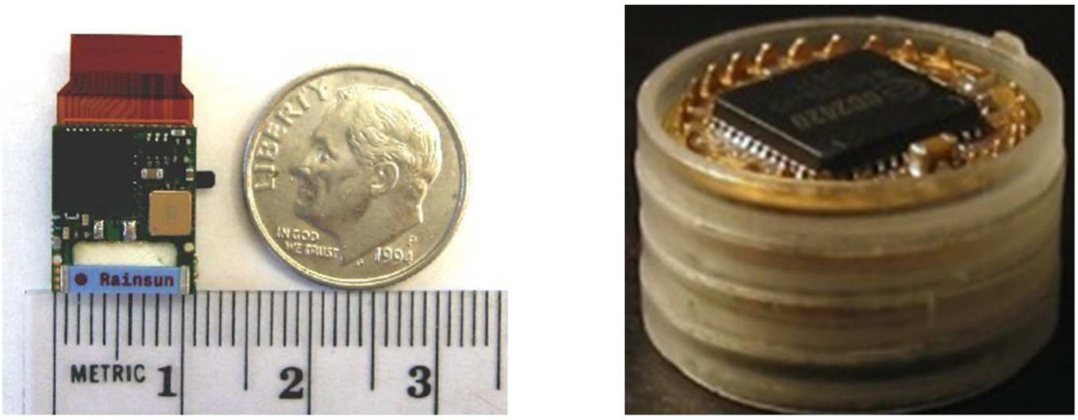
1.2 Prior Art

1.2.1 Centimeter-scale Wireless Sensor Nodes

The miniaturization of wireless sensor node began in the early 2000's with board-level systems. In 2005, the Eco node was proposed by researchers at UC Irvine [8], measuring $1 \times 1 \times 0.6$ cm^3, excluding battery. The system consists of two PCBs that are stacked, and uses commercial components for power management, processing, and sensing (Figure 1.2). A 2.5 GHz radio was also included to achieve 1 meter transmit distance. The total system sleep current is 2 μA without energy harvesting, which is a respectable number for a centimeter-scale system. However, for a millimeter-scale batteries with capacities around 10s of μAh, the Eco node will only survive for several hours, even during sleep mode.

In 2006, Philips Research proposed SAND (Small Autonomous Network Devices), which was a more systematical solution to building miniaturized wireless sensor nodes [9]. SAND is a modular platform targeted at 1 cm^3 volume, and uses stacked system-in-package technology to reduce the volume and also provides a fully encapsulated package, which is suitable for biomedical applications. Based on a coin-cell battery footprint, each module is a layer of circular PCB measuring 14 mm in diameter, which are stacked to form a cylindrical form factor. Available modules are transceiver, accelerometer, DSP, power converter, and serial flash. The modules are connected using a 24-pin interconnect embedded in the package. For an ECG (electrocardiogram) measurement applications, a proposed sensor using the SAND platform lasts 20 hours on a 144 mWh coin cell battery.

Both the Eco and SAND systems used commercial off-the-shelf (COTS) components, which clearly had limitations on the power reduction and hence the lifetime achievable in the miniaturized



EcoMote
UC Irvine (2005)

SAND
Philips (2006)

Figure 1.2: Centimeter-scale wireless sensor nodes.

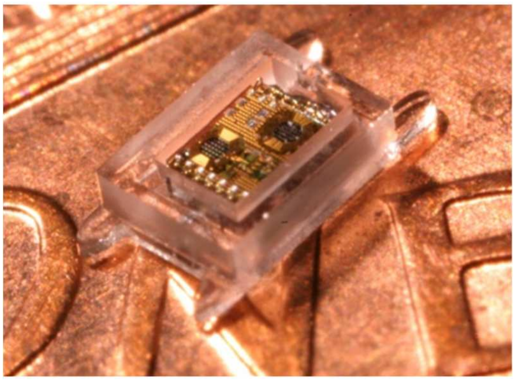
volume. Meanwhile, low-power circuit techniques and leakage reduction techniques started to emerge as the hot topic in the integrated circuit design research community mainly due to the “power wall” that was slowing down technology scaling [10] [11]. As a corollary, new applications to utilize the new circuit techniques were in demand, and wireless sensor nodes became a popular topic to motivate ultra-low power and ultra-low leakage circuits, which can extend the lifetime of the sensor and minimize the required battery volume. In 2007, a 1 cm^3 sensor node was proposed [12], which used a custom wireless transceiver chip. Even though the system integration was still done on the board level, the system achieved 0.98 μA of sleep current, and claimed 7 month life time using a 9 mAh coin cell battery.

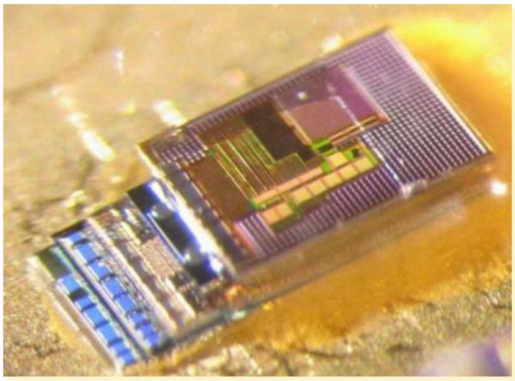
In 2010, a battery-less IOP (intra-ocular pressure) monitor was proposed [13], which consisted of custom MEMS and integrated circuit components. Instead of a battery, 24 μF off-chip capacitor array was used to store enough energy for 24 hours of operation, and wireless charging is required for continuous operation. The system measures 3 cm long, mainly due to a 2.7 cm antenna. By using custom circuits, and using duty-cycling of waking up for 1 ms every 5 min, the system achieves 675 pW of average current, inching closer to a millimeter-scale system.

1.2.2 Millimeter-scale Wireless Sensor Nodes

Continued research efforts to shrink the size of wireless sensor nodes while keeping the core functionality has led to realization of fully functional millimeter-scale systems (Figure 1.3). In 2010, a 8.75 mm^3 system with ultra-low power ARM Cortex-M3 CPU and solar energy harvesting was proposed [14]. This system was a proof-of-concept prototype consisting of two bare-die IC chips stacked and wirebonded, which laid a foundation for a more complete systems in the subsequent years, such as the IOP monitor introduced in 2011 [16]. Targeted for glaucoma patients, the IOP sensor was focused at minimizing the volume for convenient implant inside the eye. Using several ultra-low leakage circuit techniques such as the 10-T SRAM design in [14], the system power consumption is minimized to single-digit nanowatts. A MEMS capacitive pressure sensor [15] is used along with custom IC chips, and custom glass package is also designed for implantation. Compared to [13], the system volume was reduced to 1.5 mm^3, and the sensor lifetime is 28 days without energy harvesting. Solar cells are integrated on-chip, achieving energy-autonomy with 10 hours of indoor lighting per day. For both of these millimeter-scale systems, the key design aspect for achieving such small volume was in reducing the standby current and using duty-cycling to limit the average power consumption. For instance, the IOP system average power is 5.4 nW with 15 min pressure measurement interval and daily transmission of data.

In 2012, M^3 (Michigan Micro-Mote) millimeter-scale sensing platform was introduced [17], featuring a modular design and various system-level improvements over the previous designs. The system consists of custom IC chips that are stacked in a staircase fashion and connected via bond wires (Figure 1.3). With four IC layers and one battery layer, the overall dimension of the system is $2.2 \times 1.1 \times 0.4$ mm^3, resulting in a 1.0 mm^3 volume. The modular aspect of the system is similar to the SAND system, except the modules in this case are bare-die IC chips, allowing fully customized system architecture and tighter control of power consumption. More complete power management is implemented with features such as brown-out detection for preventing battery damage from over-discharge, and power-on-reset to bring up the system from assembly. A modified I^2C protocol is used for inter-layer communication, making it available to add additional layers or integrate with commercial components depending on the target application. The overall sleep mode power is 11 nW, and solar energy harvesting is implemented to extend the lifetime.





IOP Sensor (2011) **M3 Platform (2012)**

Figure 1.3: Evolution of millimeter-scale wireless sensor nodes.

1.3 Proposed Research

In this dissertation, a millimeter-scale wireless sensor node for visual sensing is described, with emphasis on the optical interface circuits that enable wireless optical communication and visual monitoring. The envisioned wireless sensor node is a nearly-invisible, yet a complete system with imaging, optics, wireless communication, CPU, memory, battery and energy harvesting. Such complete features in the unprecedented form factor can revolutionize the role of electronics in a broad range of applications, taking the "Smart Dust" concept from fiction to reality. Some examples include *in vivo* monitoring of tumor growth [18], non-invasive monitoring of eye pressure for glaucoma patients [19], infrastructure monitoring [20], monitoring the degradation of artworks or historic sites with minimal contact, studying the social network patterns of small insects, smarter home or office environment, and gathering information for surveillance.

Developing a millimeter-scale wireless visual sensor that is self-sustainable entails major design challenges arising from the physically small form factor and hence prohibitively small battery capacity. First, the standby power of the overall system must be minimized. Such battery-limited systems rely on heavy duty cycling - remaining in standby mode for most of the time and waking up intermittently to actively perform tasks - to ensure reasonably long lifetime. For the duty cycling to be effective, power consumed in standby mode, which includes the inherent leakage power of transistors, must be minimized. Therefore, every circuit component has to be designed with leakage power implications, especially for processors that has large number of gates [21] [22].

Furthermore, circuits that need to operate even during sleep mode, such as a wake-up receiver or motion detector, has to be carefully designed for ultra-low active power. To address this critical design challenge, low power design techniques are discussed throughout this proposal. Specifically, Chapter 4 discusses energy harvesting methods to achieve duty-cycled sensor operation with net energy gain.

Secondly, because of the small form factor, wired connections for testing the sensor node or transferring data is impractical. This is especially true once the sensor node is deployed, since retrieving the sensor node to make physical connections may not be possible. Also, any practical wired connection will be larger than the sensor node itself, defeating the purpose of achieving such small for factor. So a wireless method to control the sensor node and transfer data is desired. However, traditional RF receivers require standby power that easily exceeds the power budget of a millimeter-scale system. Chapter 2 describes an ultra-low power optical communication solution to address this issue.

Lastly, achieving visual sensing in a millimeter-scale form factor is extremely challenging. Implementing proper optics in such small volume has physical limitations and poses a significant challenge in the integration process. Furthermore, traditional images sensors consume relatively high power, making it difficult to conform to the strict power budget imposed by the small battery capacity. Because of these reasons, the smallest existing imaging systems are limited to centimeter-scale volume. To address these challenges, Chapter 3 discusses ultra-low power image sensor with built-in hardware motion detection feature that is suitable for power-constrained wireless sensor nodes. And Chapter 5 presents the first millimeter-scale wireless sensor node with visual imaging and motion detection capability as the end result of this research.

1.4 Contributions

In Chapter 2, an ultra-low standby power optical wake-up receiver with a novel front-end circuit and communication scheme is proposed. The optical receiver is intended to initially program, synchronize, or externally interrupt the sensor node, since wired connection may not be practical. Named "FLOW" for Free-space Low-Power Optical Wake-up, the receiver was consumes 695 pW in standby mode, which is $6000\times$ lower than previously reported RF and ultrasound wake-up radios. This extremely low standby power makes this receiver attractive for battery-limited mm^3-scale sensor nodes. After detecting a 16-bit passcode, the receiver enters active mode, during which it receives data at up to 91 bps consuming 140 pJ/bit. A pulse width modulated communication encoding scheme is used, and chip-ID masking enables selective programming and synchronization of multiple sensor nodes. The design was implemented in 180 nm CMOS technology and successfully tested.

In Chapter 3, a 128 $\times$ 128 resolution CMOS image sensor with ultra-low power in-pixel motion detection is presented. Visual monitoring and imaging with CMOS image sensors opens up a variety of new applications for wireless sensor nodes, ranging from surveillance to *in vivo* molecular imaging. In particular, the ability to detect motion can enable more intelligent power management through on-demand duty cycling and reduced data retention requirement. However, conventional motion detection schemes use digital signal processing, with power consumption levels too high for cubic-mm-scale sensor nodes. Aggressive power gating and clock gating schemes are used to minimize the power consumption. Furthermore, by implementing motion detection inside the pixel array in the analog domain, we avoid the need to use the ADC, achieving a significant power savings. Along with low power techniques, we also propose spatial aggregation of pixels and temporal averaging are implemented to minimize blindspots and increase sensitivity to slow motion. A test chip was fabricated in 130 nm CMOS technology and consumes 467 nW while performing motion detection, marking two orders of magnitude reduction over prior art, thereby bringing continuous motion detection within the realm of mm^3-scale sensor nodes. Full-frame still images with 38.5 dB dynamic range are captured at 6.4 fps while consuming 16 μW.

In Chapter 4, the harvesting aspect of the envisioned sensor node is discussed, via an experiment with microbial fuel cells (MFC). MFCs generate voltages of around 500 mV, which is A test chip was designed to include ARM Cortex-M0 CPU, 3 kB of SRAM memory, optical wakeup receiver and power management/harvesting unit. The chip as a whole consumes 11 nW in sleep mode. A small-scale micro-MFC with 21.3 cm^2 anode surface area is able to generate 5.4 μW of power at 700 mV, more than enough to power the chip in a duty-cycled usage. A 49.3-hour long-term experiment was performed with the micro-MFC connected to the chip's harvesting unit, demonstrating the sustainability of the sensor node with energy harvesting.

In Chapter 5, a complete millimeter-scale wireless imaging system is presented as the end result of this research. The proposed system is a complete wireless sensor node, including optics, battery, energy harvesting, imaging, motion detection, and two-way wireless communication. The proposed system builds on the M^3 millimeter-scale sensing platform [17], with improvements on the inter-layer communication scheme and adding two-way wireless communication. A modified version of the image sensor discussed in Chapter 3 is designed to achieve even lower power motion detection mode and more configurable thresholding, while increasing the imaging resolution to 160 $\times$ 160. Along with the improvement in the image sensor, the optical wake-up receiver described in Chapter 2 is implemented with improvements in faster data rate. During the assembly process, the solar cells are placed facing the opposite direction of the image sensor for energy harvesting. This way, the incoming light can illuminating both the solar cells and the target scene of the image sensor, creating an optimal environment for both imaging and harvesting. For optics, gradient-index (GRIN) rod lens is used for focusing, measuring 1 mm in diameter and 2.4 mm in height. The proposed system was successfully assembled with high yield and demonstrated on-demand operation with motion-triggered wake-up. With the bottom-facing solar cells, the system can harvest enough energy from 10 klux light source to sustain perpetual motion detection operation.

CHAPTER 2

Ultra-Low Power Optical Wake-Up Receiver

2.1 Introduction

In recent years, wireless sensor networks have been one of the main focus of low power circuit research, enabling a wide range of new application domains for semiconductor electronics. Wireless sensor nodes rely on limited energy stored in the battery, which becomes an increasingly difficult constraint as the nodes shrink in volume. To maximize sensor node lifetime, heavy duty-cycling is used under the premise that standby power is negligible compared to active power. Hence, minimizing standby power is critical, particularly when sensors find themselves in poor conditions for harvesting energy, such as indoor or night operation for solar cells.

One key component in a wireless sensor node is a wake-up receiver that stays on at all times to enable external interrupt, synchronization, and reprogramming. Given the miniature size of sensors and their inaccessibility after being deployed, wired connections are impractical. A wake-up receiver usually co-exists with a higher speed transceiver, which is too power-hungry to be continuously running. RF solutions are conventionally used [23] [24], exhibiting high throughput at the cost of high power consumption ($>$10s of μW). Recently, an ultrasound solution was proposed [25], but its 4.4 μW standby power remains high compared to the nW power budgets in small sensor nodes such as those in [14] [17]. This approach also requires a piezoelectric material to be bonded to the CMOS die, complicating system integration. Free-space optical solutions exist [26], but they are not integrated and consume hundreds of μW.

We propose Free-space Low-power Optical Wake-up (FLOW), a fully integrated sub-nW optical wake-up receiver and communication scheme. The FLOW receiver consumes 695 pW in standby mode and 12.7 nW in active mode. The role of FLOW in a wireless sensor node is two-fold:

- Initial programming after sensor node system assembly.
- Resetting a sensor node after catastrophic failure by re-programming and re-synchronizing timers.

The latter is required if 1) nodes become unsynchronized, effectively disabling timing-sensitive node-to-node RF communication, 2) the sensor node restarts from a power shutdown mode due to poor harvesting conditions, or 3) the CPU program encounters an unforeseen error and requires a hard reset. Hence, it is critical that the FLOW receiver remains on at all times and does not require a software stack, which is commonly needed in RF wake-up receivers.

FLOW was integrated in a wireless sensor node system [17] where it can directly load a program into the memory, trigger control signals to wake up the CPU, set configuration bits, and turn on an RF radio block to initiate high-speed communication. With FLOW, multiple nodes can be addressed in parallel using a global 16-bit access code while a programmable chip-specific ID code allows communication to a specific subset of nodes.

2.2 Proposed Design

The proposed optical wake-up receiver is comprised of a decoder, protocol controller, reference generator, clock generator, and front-end circuits (Figure 2.1). The FLOW receiver remains on at all times, whereas the protocol controller is power-gated in standby mode. CPU and SRAM are also implemented in the same design, and are used for system-level testing and BER (bit error rate) testing.

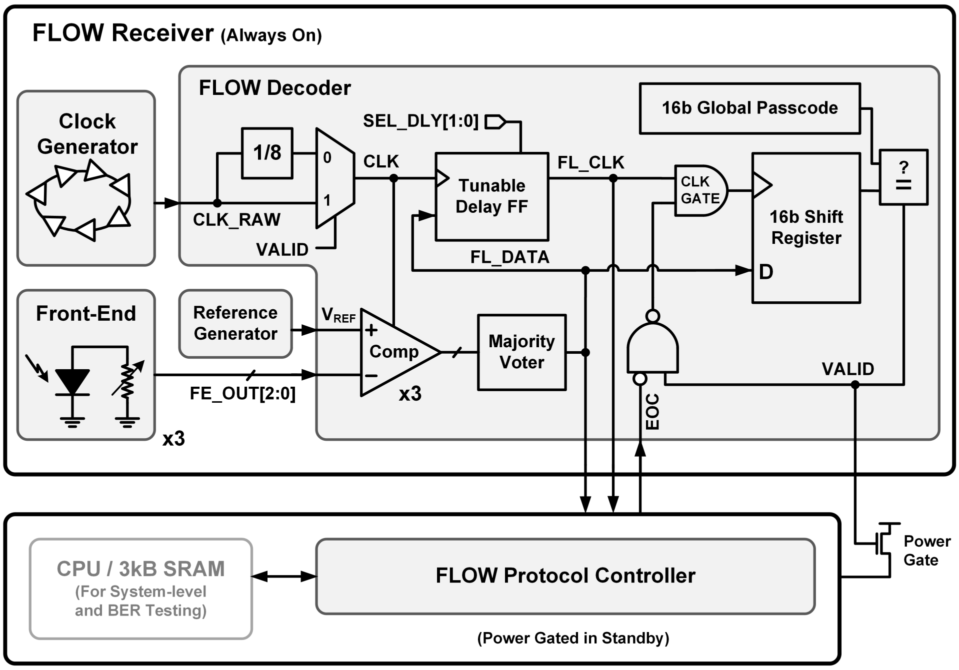


Figure 2.1: System block diagram of FLOW, Free-space Low-power Optical Wake-up.

2.2.1 Front-End Design

The front-end circuit uses an n+/pw/nw parasitic diode as a PV cell to convert incoming light to voltage. Figure 2.2 shows measured open circuit voltage of a PV cell in response to an LED light switching on/off. Even though the rising transition is fast at about 100 μs, the falling edge is much slower, taking about 100 ms to fully discharge. This is because instant photocurrent is responsible for charging up, but for discharge only diode current is responsible. As the voltage drops, the diode current decreases exponentially, resulting in a long discharge time. A pull-down resistor in parallel with the diode, provides a fast discharge path, as shown in Figure 2.3. However, the parallel resistor has a disadvantage of linearizing the open circuit voltage's dependence on illuminance.

Figure 2.4 shows simulation results for a 10 x 10 μm diode with different pull-down resistor values. Higher resistance value gives sharper slope, and lower resistance value of around 200 MΩ makes the open circuit voltage response completely linear, obscuring the definition of illumination levels. Hence, a trade-off exists here; lower resistance pull-down path is desired for faster response, but higher resistance is desired to provide a steep slope for easily distinguishing two levels of illuminance.

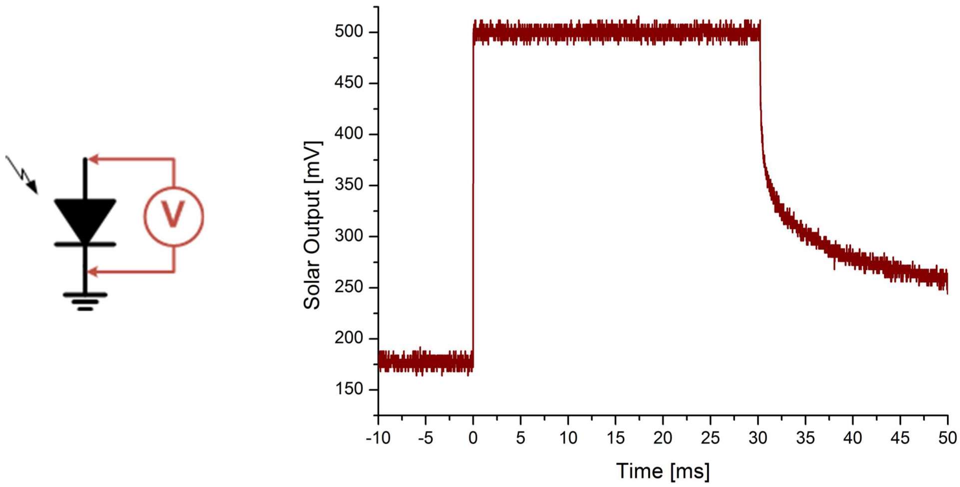


Figure 2.2: Measured open-circuit voltage of a PV cell in response to LED.

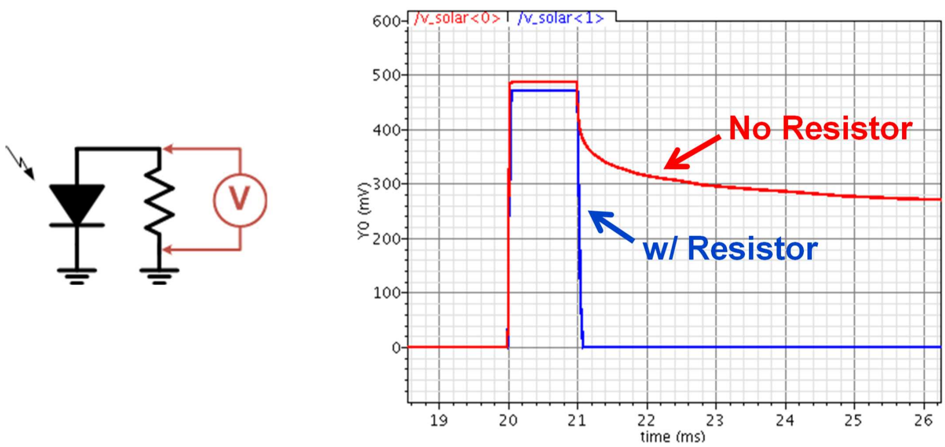


Figure 2.3: Simulated open-circuit voltage of a PV cell in parallel with a pull-down resistor.

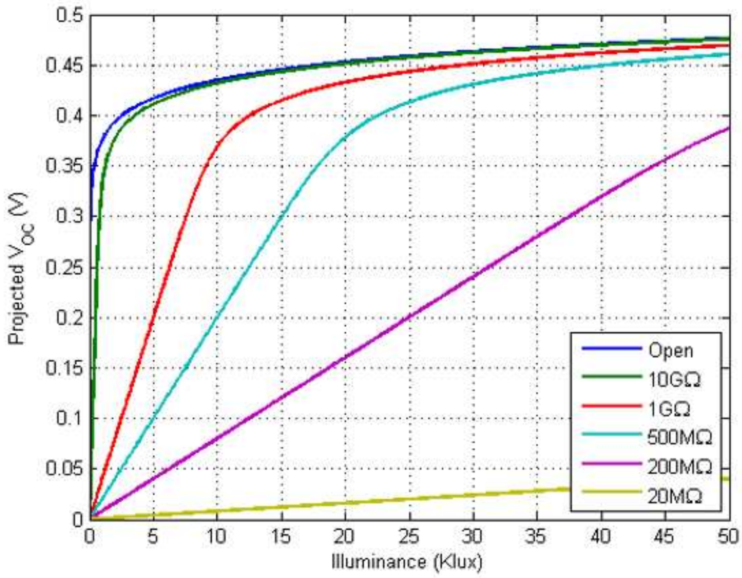


Figure 2.4: Open-circuit voltage of a PV cell in parallel with different value of resistance.

A solution to this problem is non-linear resistor. We propose the use off-state MOSFET to implement the pull-down resistor for two main reasons: 1) realizing 100s of megaohm to gigaohm-range resistor is impractical for area, and 2) the non-linear resistance characteristic of off-state transistor, which is an effect of DIBL (drain-induced barrier lowering), is beneficial in creating a sharp response to illumination. Figure 2.5 (top) shows resistance of an off-state MOSFET varying with drain to source voltage. This resistance characteristic translates into a sharp open circuit response of a PV cell in parallel with the off-state MOSFET (Figure 2.5, bottom). With this configuration, the location of the edge can be easily tuned for different background lighting conditions without compromising the slope.

The tuning range of the frontend circuit is shown in Figure 2.6. Since the range of the diode open circuit voltage is about 400 mV, the threshold used to determine light on/off is set to be 200 mV. For indoor usage, the frontend can be configured to toggle at illuminance of 1-2 klux. For outdoor usage, the toggling illuminance can be set much higher. Sensitivity is defined as the slope of open circuit voltage response to illuminance, and the proposed circuit improves the sensitivity by 220$\times$ compared to a linear resistor, significantly improving ambient light immunity and signal integrity.

Figure 2.7 shows the schematic of the tunable frontend. The resistors are implemented with

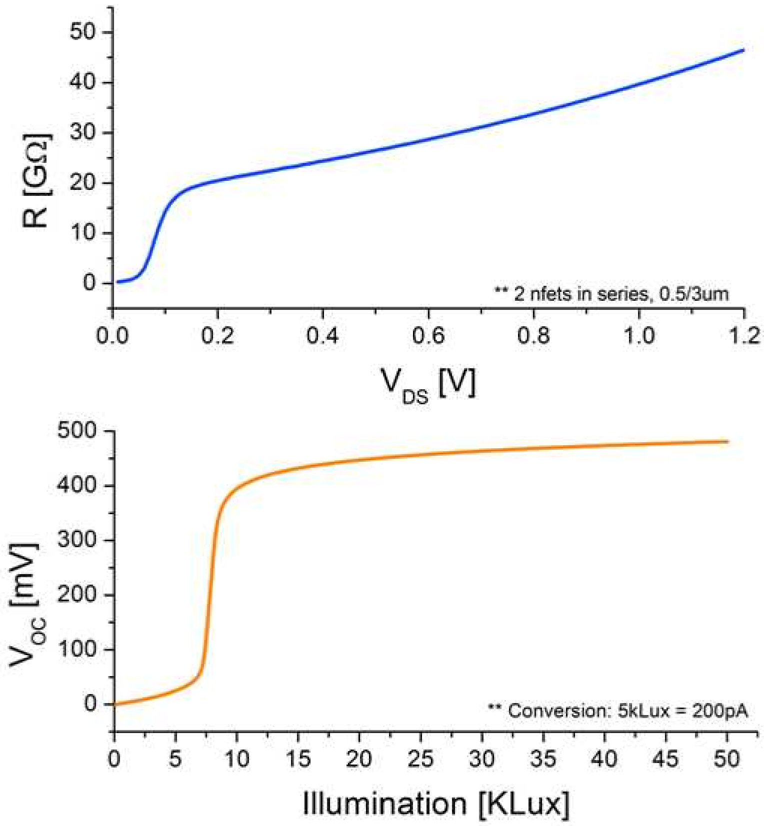


Figure 2.5: Resistance of an off-state MOSFET vs. drain to source voltage (top). Paired with a PV cell, the off-state MOSFET yields a sharp open circuit response (bottom).

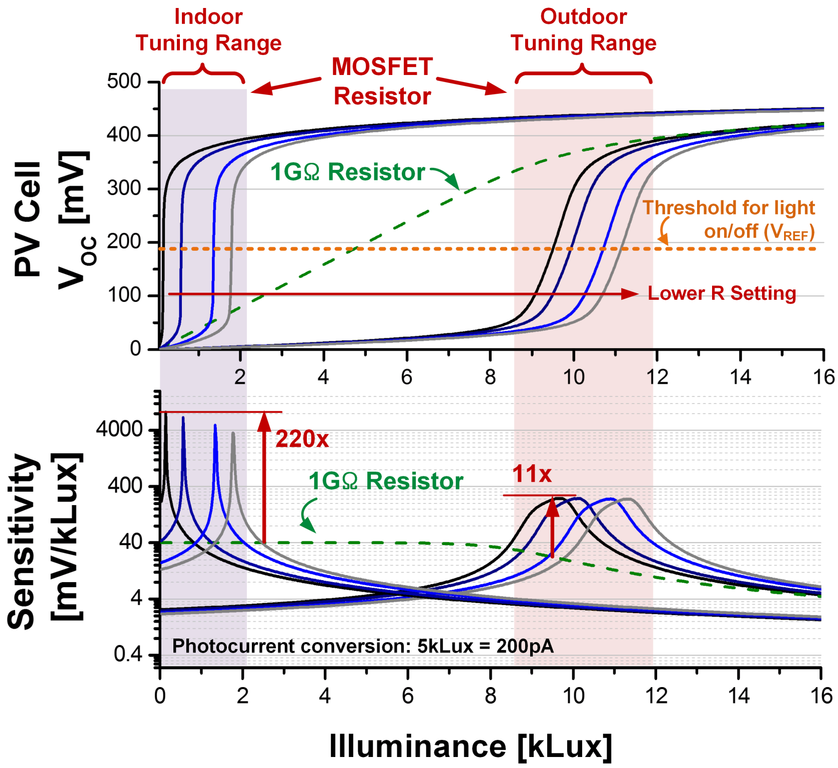


Figure 2.6: PV cell open circuit voltage and sensitivity to illuminance. The non-linearity of off-state MOSFET resistance improves peak light sensitivity of the front-end output by up to 220× compared to a linear resistor.

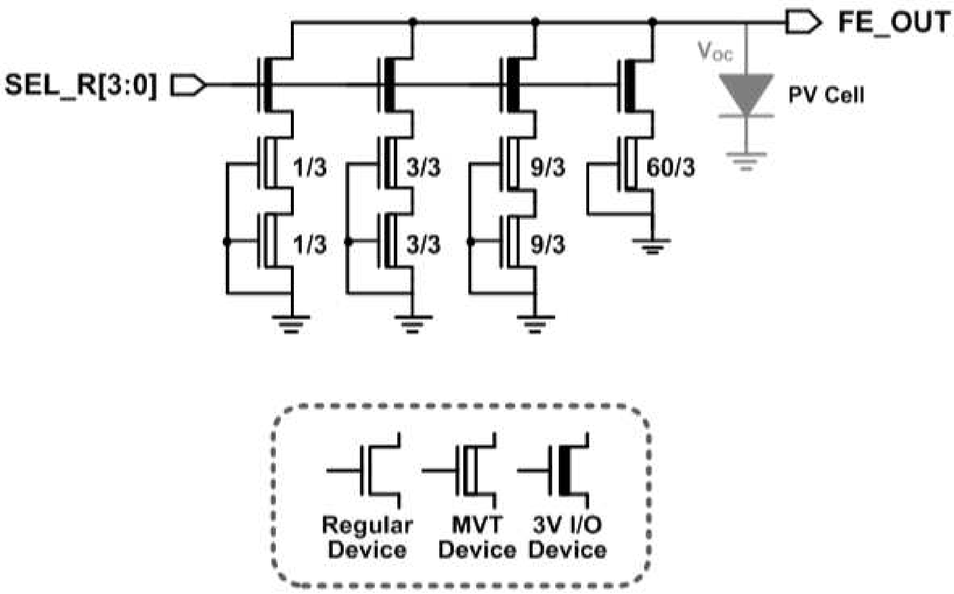


Figure 2.7: Schematic of the digitally tunable front-end circuit.

medium Vth devices and are sized in super-exponential steps to provide large tuning range. The tuning switches need to provide higher resistance than the resistors, so they are implemented with high Vth 3 V I/O devices. Default resistor tuning bits are hard-coded so that FLOW can initially program under indoor conditions after the sensor node is fabricated and assembled.

2.2.2 Light-to-Digital Data Conversion

The outputs of the three front-end circuits are digitized by the comparators and majority-voted to generate FL_DATA (Figure 2.1). This redundancy in the front-end circuit improves robustness against false triggers and provides immunity against possible structural problems such as a dust particle blocking the path of light to the front-ends. FL_DATA in turn is delayed by a tunable digital delay to generate FL_CLK. The incoming data stream is recovered when FL_DATA is latched at the positive edge of FL_CLK. A 2-T low power reference circuit [27] generates a temperature and supply voltage insensitive reference voltage of 190 mV with σ of 4.8 mV (1k Monte Carlo simulation result) to be used as the threshold for light level detection. A 2 kHz clock (CLK_RAW) is generated using a leakage-based oscillator [14] for reduced voltage sensitivity and low power.

2.2.3 Communication Scheme

The timing diagram in Figure 2.8 shows the pulse width modulated timing scheme of FLOW communication. The sampling clock is used for the front-end comparison and generating a digital delay. Illumination pulse widths of t_{short} and t_{long} determine data bit values of 0 and 1, respectively. The delay of the tunable delay flip-flop is $t_{delay} = n \cdot t_{clk}$, where the parameter n is set between 7 and 29. This delay serves two purposes: 1) it distinguishes long pulse from short pulse, and 2) serves as a margin to account for chip-to-chip process variation of sampling clock frequency. This margin is critical to accommodate for batch programming. Timing constraints on the length of short and long pulse is:

$$2 \cdot t_{clk} < t_{short} < n \cdot t_{clk} \tag{2.1}$$

$$n \cdot t_{clk} < t_{long} < t_{period} \tag{2.2}$$

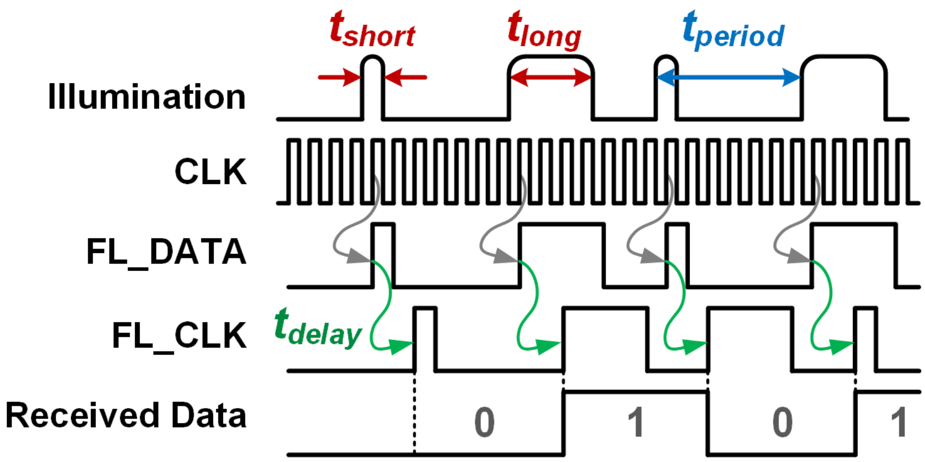


Figure 2.8: Timing diagram of FLOW's pulse-width modulated communication scheme.

To achieve batch programming of multiple chips, process variation of CLK_RAW must be considered in determining a common data rate, 1/t_{period}. Considering process variation in t_{clk}, the values of tshort and t_{long} have the following constraints:

$$2 \cdot t_{clk\_slow} < t_{short} < n \cdot t_{clk\_fast} \tag{2.3}$$

$$n \cdot t_{clk\_slow} < t_{long} < t_{period} \tag{2.4}$$

Hence the common data rate for FLOW batch transmission, 1/t_{period}, is limited by the clock frequency of the slowest chip and delay parameter n. If the chip-to-chip variation is small, n can be lowered from its default value and multiple chips can be programmed at a faster common data rate. When the chip is first powered on, the delay parameter n resets to its largest value at 29 to maximize the tolerance to process variation. This allows the sensor node to be safely programmed after system assembly without any prior tuning.

2.2.4 Ultra-Low Power Standby Mode

In standby mode, the FLOW receiver operates at 1/8 of the nominal clock frequency to minimize the standby power. The rest of the system, including the protocol controller, is power-gated during this mode. To prevent false triggers from ambient light, a 16-bit predetermined passcode is used as a global passcode to wake up the system. Once the incoming stream of FL_DATA matches this 16-bit code, the VALID signal wakes up the protocol controller and increases the clock frequency by 8× to enable full speed data transfer. During this ultra-low power standby mode, the majority of the switching power is consumed by the clocked comparators and the clock dividers. If the division ratio of the clock is larger than 8, the clock divider dominates the power consumption, resulting in a marginal reduction of power.

2.2.5 Communication Protocol

After VALID signal goes high, the protocol controller receives and interprets the subsequent FL_CLK and FL_DATA, according to the communication protocol summarized in Table 2.1. A FLOW message consists of header and data sections. 8-bit parity is implemented for both sections to validate the transmitted content. The header indicates the functionality of the message, chip ID, and program length, along with other control bits. The main functionalities of a FLOW message include: 1) resetting the system, 2) writing configuration registers of the system, 3) issuing an I^2C message through the system, and 4) loading program onto the memory. A local chip ID scheme is used to address groups of chips or individual chips, enabling selective batch programming. If the FLOW transmission completes or FL_DATA is idle for more than 21 seconds, the protocol controller asserts the EOC (End-Of-Communication) signal, resetting the FLOW receiver into standby mode. The protocol controller has direct access to memory, sends interrupt messages to the CPU to start executing code, and has the ability to reset the system, effectively taking full command of the wireless sensor node.

2.3 Measurement Results

The proposed optical receiver was fabricated in 180 nm CMOS technology and successfully tested with 695 pW standby power. The design was also integrated in a wireless sensor node [17] with an ARM M0 CPU and 3 kB SRAM, which were used for BER (bit error rate) testing and system-level testing.

Section	Byte	Description	Detail
Header	0	Control Field	Bit 3:0 = Chip ID Mask Bit 4 = Reset Request Bit 5 = Chip ID Enable Bit 6 = I2C Message Issue (8bit Addr, 32bit Data) Bit 7 = Run after programming
	1	Chip ID	16-bit Chip ID
	2		
	3	Memory Address (16 bit)	Word address (2'b00 padded at LSB)
	4		
	5	Programming Length (16 bit)	Data length in words (2'b00 padded at LSB)
	6		
	7	Bit-wise XOR Parity (BIP-8) (8 bit)	Parity for header section
Data	8	Bit-wise XOR Parity (BIP-8) (8 bit)	Parity for data section
	9~	Data Field	

Table 2.1: FLOW communication protocol.

2.3.1 Light Source & Optics

Three different light sources were used for communicating with FLOW: a 0.5 W 45 lm LED without focus, a 3 W 134 lm LED with manual focus, and a 3 mW green laser. Receiver performance depends on the illuminance received at the surface of the chip. As shown in Figure 2.9, the power and optics of the light source strongly impacts the illuminance. The same 3 W LED in focus shows 40× higher illuminance than when out of focus. With the laser, FLOW can be triggered from a distance of 50 m, with longer range measurements limited by the testing environment. This demonstrates the advantage of optical communication as it enables long distance transmissions with commonly available transmit sources.

2.3.2 Measured Performance

Figure 2.10 shows the relationship between maximum data rate and illuminance. If the illuminance is low, the frontend needs a high pull-down resistance, and limits data rate. As illuminance is increased, pull-down resistance setting can be reduced, resulting in faster pull-down of the diode voltage and increased data rate. The data rate eventually saturates at 91 bps, due to limitations

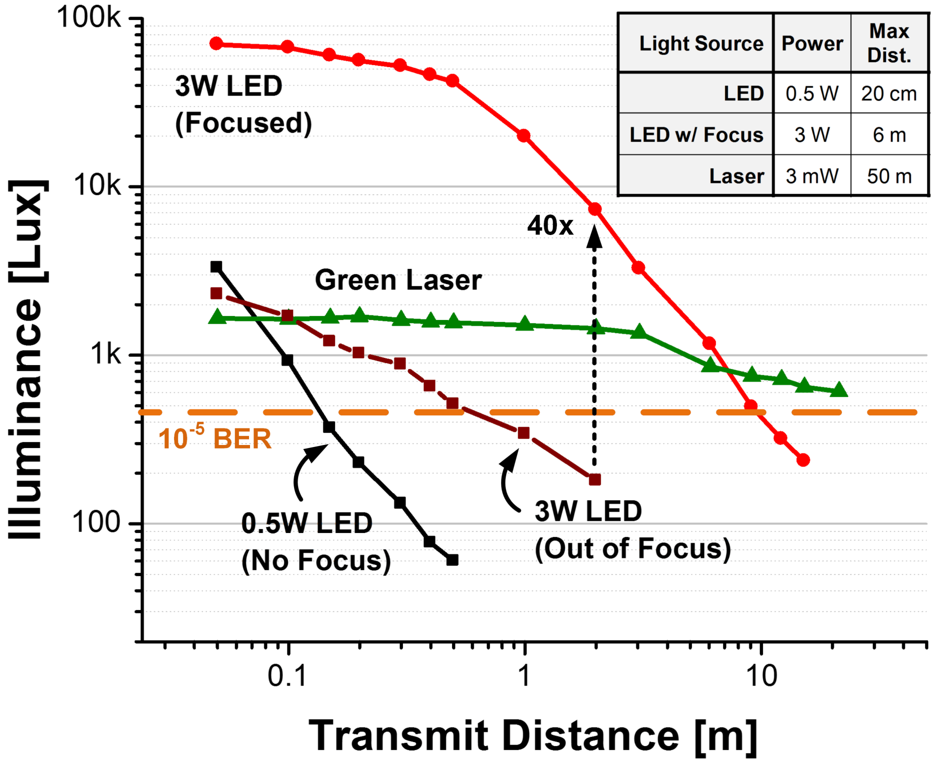


Figure 2.9: Illuminance measured at the receiver end versus light transmission distance for different classes of light sources. An off-the-shelf laser pointer can trigger FLOW from >50 m.

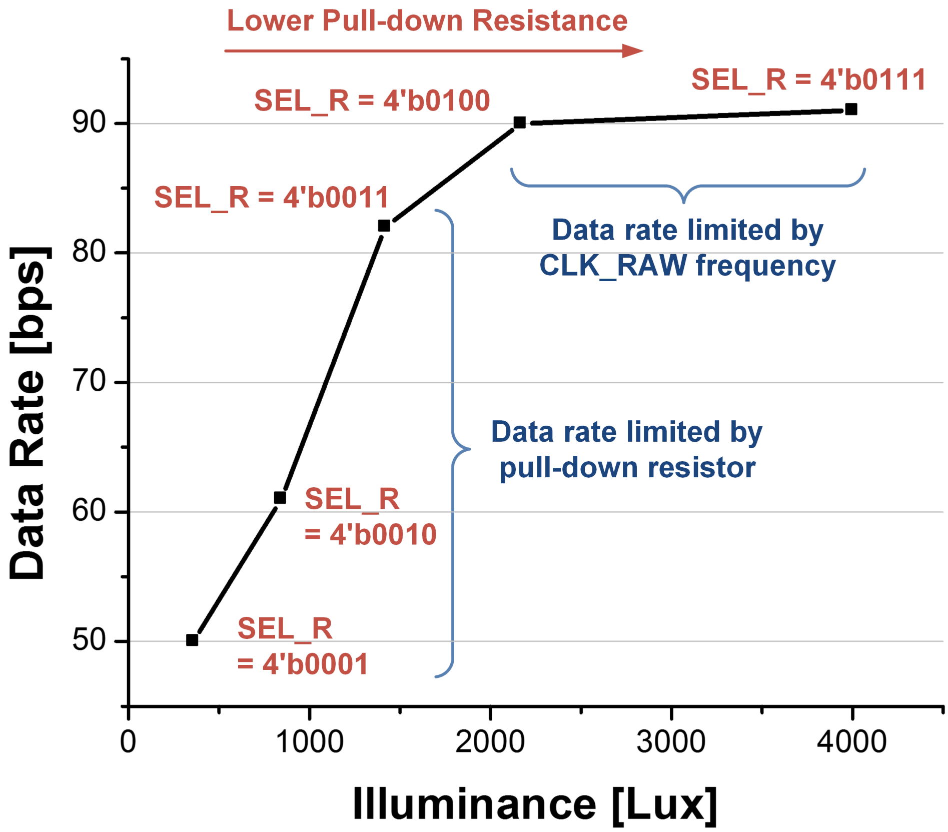


Figure 2.10: Data rate versus illuminance with optimal setting for resistor. High resistance is required for low light conditions, limiting data rate.

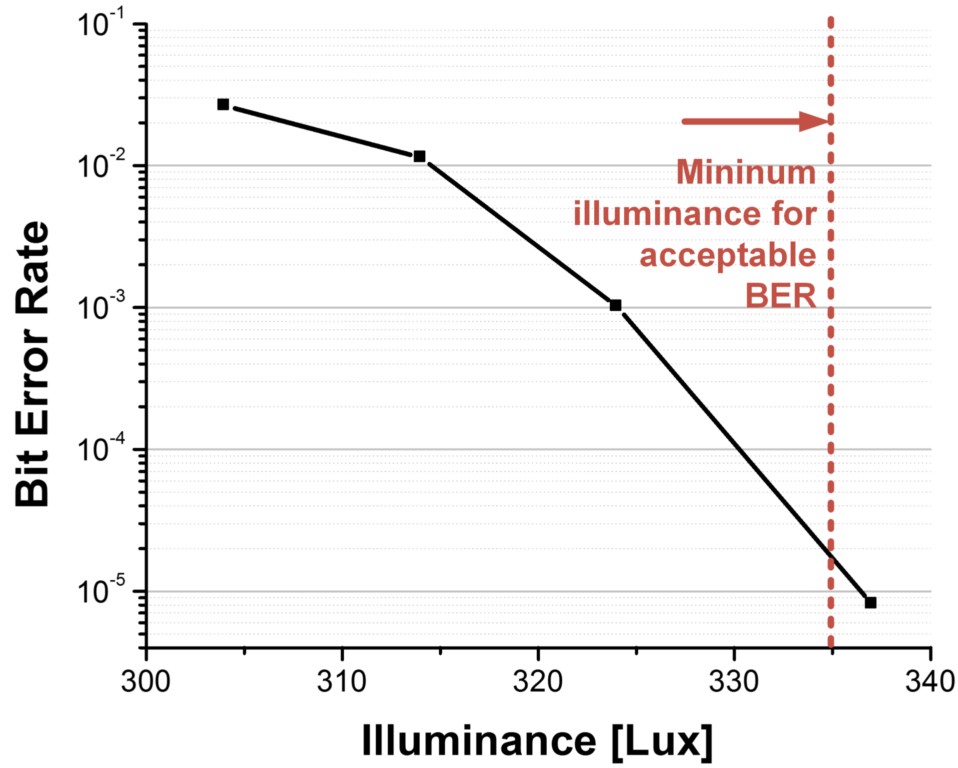


Figure 2.11: Bit error rate vs. illuminance. Lowest measured BER is 8E-6. A relatively low illuminance of 300 lux is required to achieve acceptable BER.

on sampling clock generator. This relatively low data rate is acceptable for a wake-up receiver because only a small amount of code is required for initial sensor setup and faster wireless transceiver can be activated afterwards. Data rate can be further increased by adding a faster clock generator while retaining low standby power by power-gating this fast clock in standby mode. BER was measured by repeatedly transmitting 1 kB code through FLOW onto the memory. Bit error rate also declines with higher illuminance; a minimum illuminance of 370 lux was required to obtain a BER of 8.1E-6 (Figure 2.11).

2.3.3 Clock Variation Considerations

To demonstrate batch programming, clock distribution among 28 chips was measured (Figure 2.12). At the default delay parameter of n=29, all 28 chips can be simultaneously programmed with a common data rate of 14 bps without prior tuning. Based on the measured CLK_RAW frequency σ of 159 Hz, the default delay setting can cover $\pm 3\sigma$ clock variation, resulting in 99.7% yield.

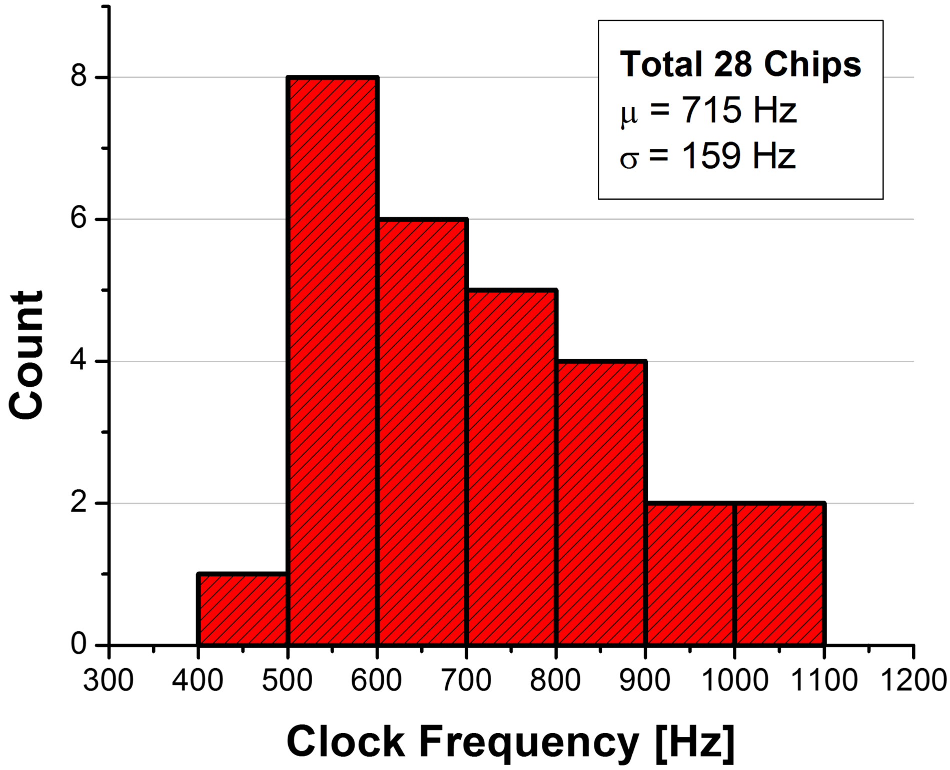


Figure 2.12: Measured clock frequency distribution of 28 chips. All 28 chips can be simultaneously programmed without prior tuning.

Both batch programming and chip-ID masking was verified with multiple chips.

2.3.4 System-Level Testing

Figure 2.13 shows the testing setup with a 0.5 W LED controlled by NI Labview, which is used to generate illumination patterns from digital code. Measured oscilloscope snapshot shows FL_DATA being triggered by light and VALID signal triggering after the 16-bit passcode is matched. Wireless sensor node system-level functionality was verified by transferring a 1 kB program through FLOW to the SRAM without any prior tuning, followed by successful program execution by the CPU. Figure 2.14 shows the die photo of the test chip. The three front-ends measures 32 x 19 μm each, and are placed between bonding pads. This allows the die containing FLOW receiver to be placed anywhere in a die-stacked system and ensures light exposure of the front-ends.

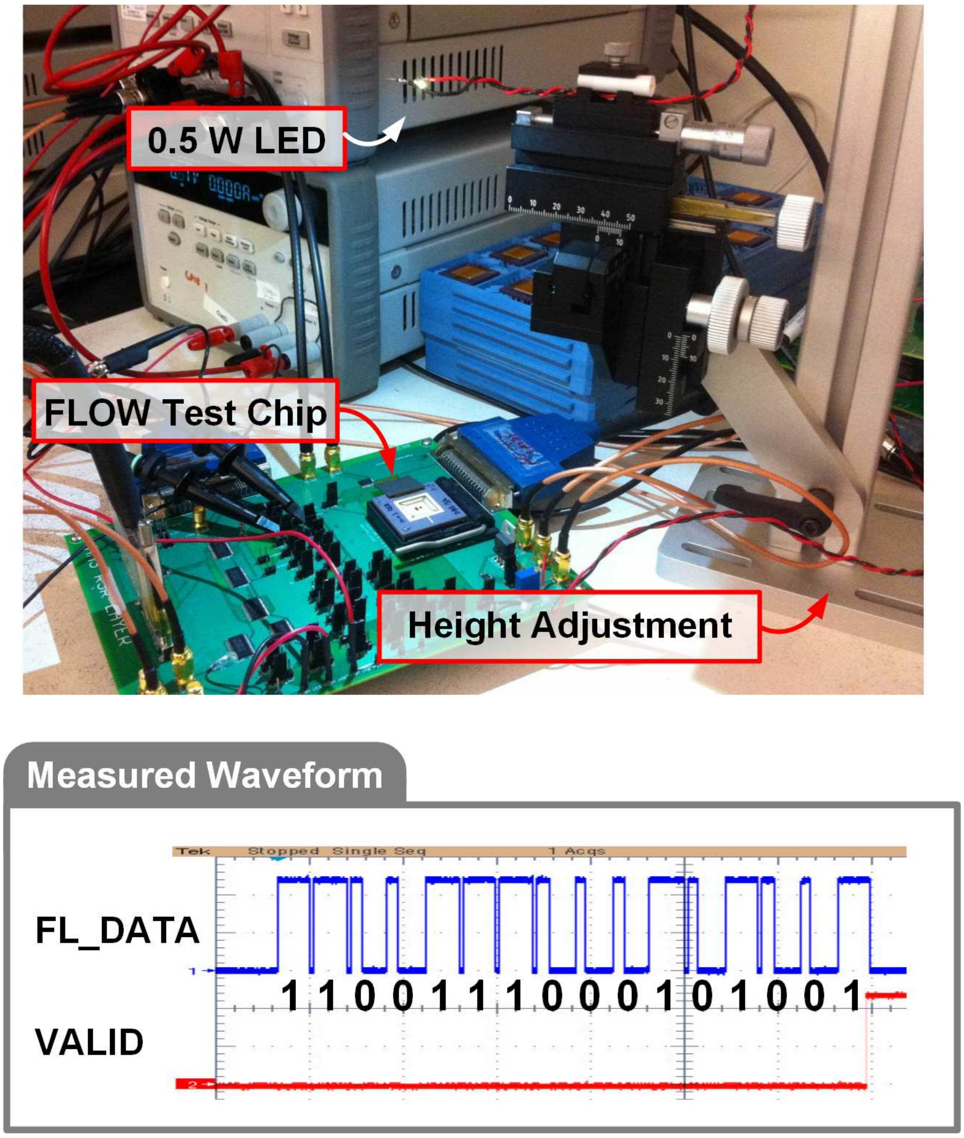


Figure 2.13: Test setup with 0.5 W LED controlled by NI Labview. Ambient office light interference does not affect FLOW operation.

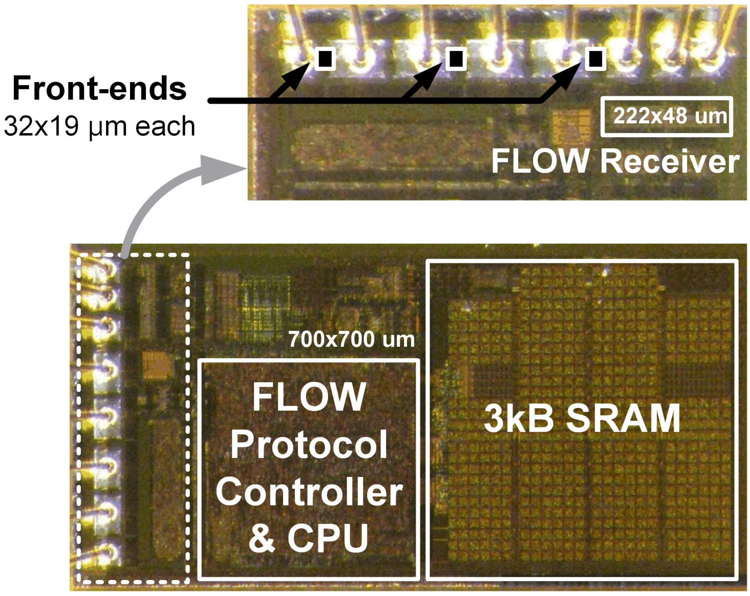


Figure 2.14: Die photo in 180 nm CMOS. The three front-end circuits are placed between bonding pads for light exposure in a stacked system.

2.3.5 Comparison to Prior Art

Table 2.2 compares FLOW with previously reported wakeup receivers. Compared to the RF and ultrasound solutions, the proposed design achieved more than three orders of magnitude smaller standby power at 695 pW, including clock generation. The measured clock generator consumes 520 pW, so if a clock is already available in the system, total FLOW power overhead would be only 175 pW, which is 3% of the 7 nW standby power of the wireless sensor node system in [17]. Data rate is on the same order as the ultrasound solution in [25], which consumes 4.4 μW.

2.4 Conclusion

In this chapter, we proposed a sub-nanowatt standby power optical wake-up receiver and communication scheme suitable for wireless sensor nodes. In its ultra-low power standby mode, the receiver only consumes 695 pW, while looking for the 16-bit passcode to wake it up. We have demonstrated stable system-level operation with excellent transmission distance. In the wireless sensor node system [17] in which the proposed design was employed, clock was already present, so the power overhead of continuous wake-up monitoring was only 3% of 7 nW total system sleep power.

	[Drago2010]	[Pletcher2009]	[Yadav2011]	This work
Transmission Method	RF (2.4 GHz)	RF (2 GHz)	Ultrasound (43 kHz)	Optical
Technology	65 nm	90 nm	65 nm	180 nm
Fully Integrated	Yes	No	No	Yes
Supply Voltage	1.2 V	0.5 V	0.6 V	1.2 V
Total Standby Power	415 μW	52 μW	4.4 μW	695 pW
Maximum Data Rate	500 kbps	100 kbps	250 bps	91 bps
Demonstrated Distance	-	-	8.6 m	50 m
BER	$<10^{-4}$	$<10^{-5}$	$< 10^{-3}$	$< 10^{-5}$
IC Area	0.2 mm^2	0.1 mm^2	1.24 mm^2	0.51 mm^2 *

Table 2.2: Measured performance summary and comparison.

CHAPTER 3

CMOS Image Sensor with In-Pixel Motion Detection

3.1 Introduction

Visual monitoring with CMOS image sensors opens up a variety of new applications for wireless sensor nodes, ranging from military surveillance [28] to *in vivo* molecular imaging [29]. CMOS image sensors have been widely used as an alternative to CCD imagers mainly due to its compatibility with other CMOS circuitry, among other benefits. There is a large amount of literature on CMOS image sensor designs, most of which focus on achieving higher resolution [30], frame rate [34], or dynamic range [35], often at the expense of power consumption, resulting in power levels that are prohibitive for battery-powered wireless sensor nodes such as reference [17]. Therefore, there is a clear need for a highly energy efficient image sensor.

In addition to capturing images, the ability to detect motion can enable more intelligent system-level power management through on-demand duty cycling and reduced data retention requirement. Motion detection capability can reduce the duty cycle of a distributed sensor node by triggering a response only when needed. One example scenario would be capturing images immediately upon motion detection, followed by processing the images and transmitting the results to a central location. This scheme would reduce the power budget compared to periodically capturing images and transmitting each, provided motion detection is performed efficiently. The key here is that power consumption required for motion detection needs to be minimized as much as possible, since it needs to be operating even during sleep mode of the duty-cycled scenario.

One of the more sophisticated algorithms of motion detection involves integration of multiple

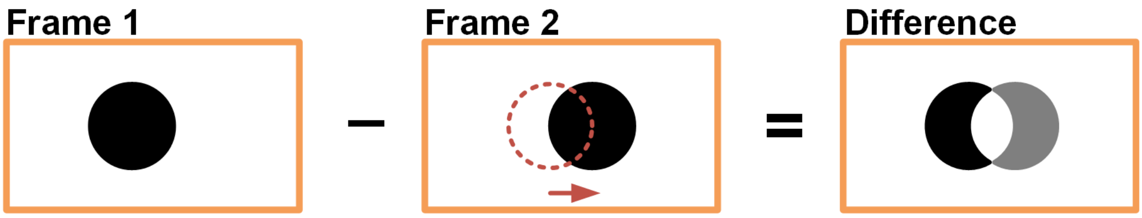


Figure 3.1: Frame differencing concept.

frames, followed by convolving with a Gaussian to smoothen the data, and applying the Laplacian (second derivative) to find zero crossings [32]. These operations involve digital signal processing and require memory element to store the multi-frame image data, both of which pose a large power and area overhead. There have been works on implementing Gaussian and Laplacian operators at the circuit level by using current-mode circuits [33], but the nature of current-mode design calls for high power consumption. Thus, the power requirements of these approaches are not suitable for our proposed mm^3-scale sensor.

A simpler method to perform motion detection is frame differencing [31], in which two consecutive images are subtracted from each other pixel by pixel and the result is compared to a pre-defined threshold value to provide movement information, as shown in Figure 3.1. Several in-pixel motion detection designs have been proposed [36] [37], in which the previous pixel value is stored on an in-pixel capacitor until the end of the next integration cycle for immediate frame differencing. This avoids the need for high power signal processing operations and digital memory. However, the in-pixel schemes are limited to frame differencing of two consecutive frames, reducing sensitivity to slow moving objects compared to more sophisticated digital signal processing approaches that operate on multiple frames. If the movement is slower than the frame rate, then the two consecutive frames will look identical, and the slow motion can escape detection. Also, because of the added circuitry inside the array, pixel fill factor is reduced, with some designs reporting less than 10% fill factor. And last but not least, existing designs consume at least 100s of μW, which is well above our power budget.

In this chapter, we address these issues by proposing an improved in-pixel frame differencing scheme using a sub-array of an image sensor, in which only a fraction of the pixels are used for motion detection and the rest of the pixels are only enabled for full-frame imaging. This reduces overall array power consumption, and also improve fill factor by distributing the motion detection circuitry in the imaging-only pixels. Along with the sub-array architecture, we propose two novel techniques to improve motion detection sensitivity. First, to compensate for the reduced detection resolution and possible blindspots introduced by not using the full frame, we propose pixel aggregation concept. Secondly, temporal averaging is proposed to address low sensitivity to slow motion, closing the gap between frame differencing and digital signal processing. With these techniques, we demonstrate a CMOS image sensor with in-pixel motion detection capability with less than 1 μW power consumption and close to 40% pixel fill factor.

3.2 Motion Detection Techniques

3.2.1 Pixel Aggregation

To reduce power consumption and limit the impact of added motion detection circuitry on pixel fill factor, only a subset of the pixels is instrumented with motion detection (3 of 64 in our implementation). As a result, power consumption is reduced by 20×, but so-called blindspots are created due to the presence of inactive pixels. To address this issue, we propose pixel aggregation (PA), where multiple pixels are combined and operate as one to increase coverage with no power penalty.

Figure 3.2 illustrates how pixel aggregation help eliminate blindspots in sub-array motion detection. In a baseline design, 1 out of 9 pixels are designated as detection pixels, shown as black dots, so the inactive pixels become blindspots for motion to escape. The red arrows indicate traces of motion, and the bottom motion escapes the field of view without triggering any detection pixels. With pixel aggregation, the number of detection pixels remain the same, but the photodiodes of neighboring pixels are merged together, providing tighter detection coverage. The same trace that escaped detection in the baseline case can be now detected with pixel aggregation.

3.2.2 Temporal Averaging

To capitalize on the low power aspect of in-pixel frame differencing without compromising sensitivity to slow moving objects, we propose temporal averaging (TA), in which certain pixels in the array are exposed to a longer integration time, resulting in a slower frame rate. The intuition

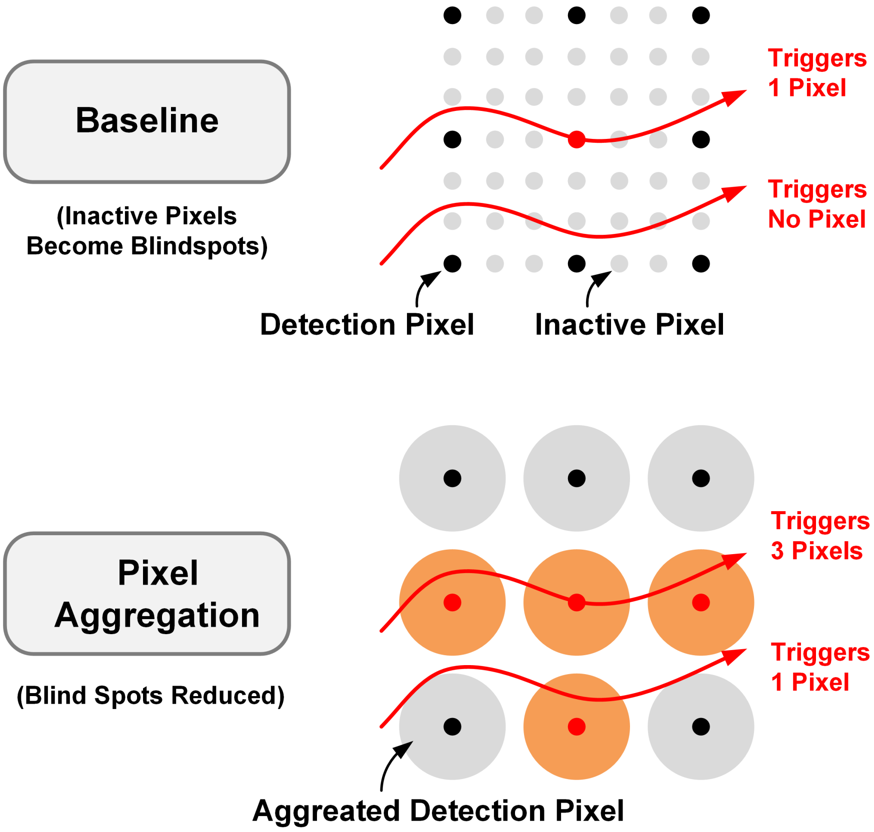


Figure 3.2: Pixel aggregation conceptual diagram.

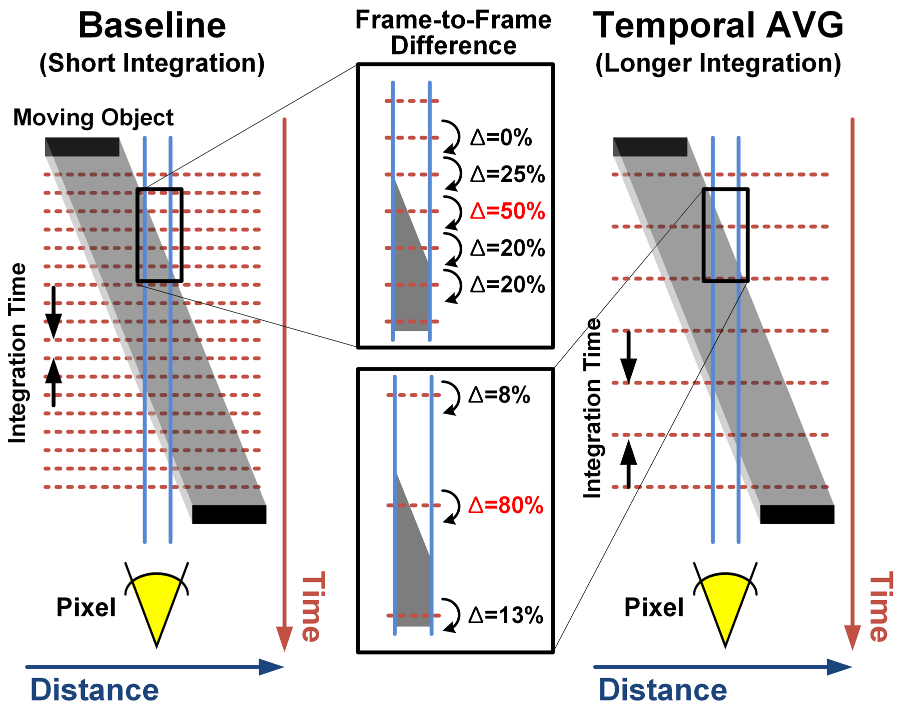


Figure 3.3: Temporal averaging conceptual diagram.

behind this is that slow objects make negligible differences at high frame rates but can be detected by slowing down the frame rate, as illustrated in Figure 3.3. As the object moves, the pixel sees different amount of movement in each frame, based on the integration period. In the baseline case, relatively short integration period is used, and the baseline pixel sees maximum frame-to-frame difference of 50%. Temporally averaged pixel has longer integration period than the baseline case, and sees a maximum of 80% difference. The implication of this bigger difference is that the accuracy requirement for the detection circuitry is relaxed, thus can be made lower power. This difference becomes more prominent for slower motions.

To verify this concept, a real-life video of a moving object was captured with a digital camera at 60 fps, and was post-processed in MATLAB with different temporal averaging factors. To quantify the sensitivity of motion detection, we define a term called motion intensity, which is given by:

$$MotionIntensity = \frac{\Delta V_{Pixel}}{Noise} = \frac{Max(Interframe\,\Delta V_{Pixel})}{AVG_{StaticFrames}(Max(Interframe\Delta V_{Pixel}))}. \tag{3.1}$$

Here, the noise level is defined by the average value of interframe pixel difference over mul-

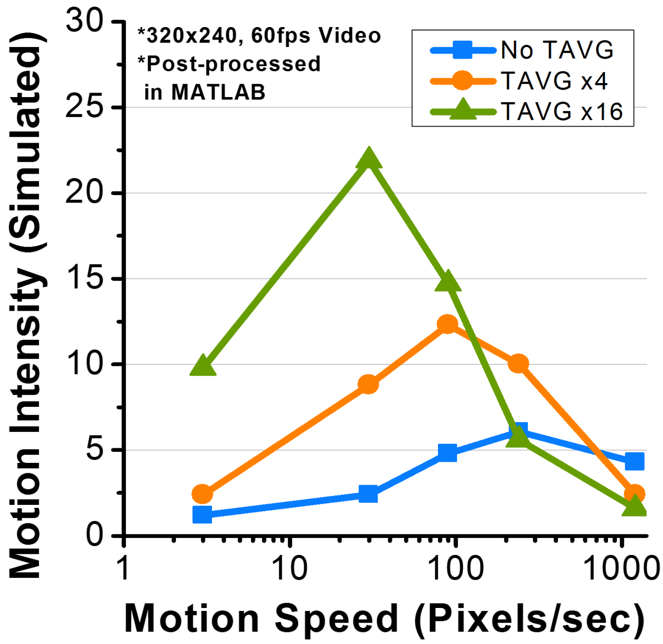


Figure 3.4: Motion intensity vs. speed with different temporal averaging factors.

tiple static images. Figure 3.4 shows motion intensity vs. moving object speed for three different temporal averaging settings. Compared to the raw data (no temporal averaging), temporally averaged frames show up to 10× higher motion intensity. Another observation is that depending on the speed of the object, there is an optimal temporal averaging factor that maximizes the motion intensity. The benefit of temporal averaging helps detection of slow motions, but if the integration period becomes too long, fast motions can escape detection, as its impact on the photocurrent integrated over the frame will be too short to be detected. Thus, more than one averaging settings should be implemented to maximize the detection coverage. We implement a dual mode operation, where two sets of detection pixels are simultaneously operated with short/long integration periods to ensure detection of slow/fast motions.

3.3 Design Implementation

The proposed techniques in Section 3.2 are implemented in an image sensor array consisting of 128 × 128 pixels, with groups of 8 × 8 pixels forming a motion detection (MD) cluster (Figure

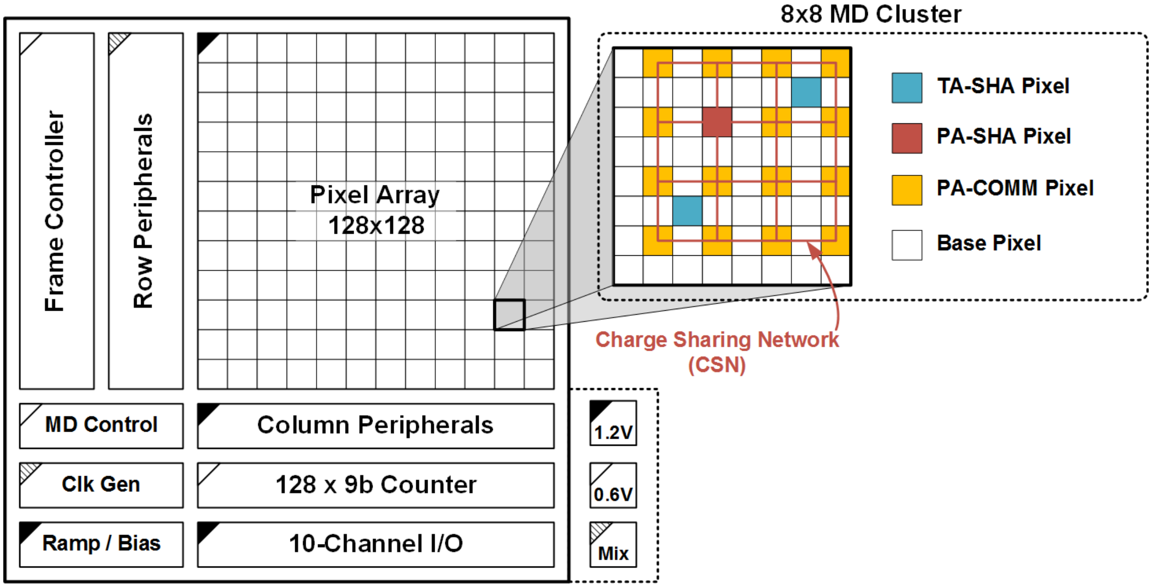


Figure 3.5: Block diagram of the image sensor, showing dual-supply power domains and pixel arrangements inside a motion detection cluster.

3.5). One approach in reducing the power consumption of an image sensor is to lower the supply voltage, which is a commonly employed technique in digital circuit design. However, supply voltage reduction de-grades signal to noise ratio (SNR) due to reduced signal swing, increased leakage noise, and increased sensitivity to process variation. To overcome this issue, we use dual-supply design, in which the analog components operate at 1.2 V, and the digital blocks operating at a near-threshold 0.6 V. Likewise, the frame controller operates in 0.6 V supply domain, and its control outputs to the pixel array is level converted.

3.3.1 Array Architecture

In each MD cluster, four different types of pixels are used and uniquely placed. Aside from the base pixels that are used for full-frame imaging only, there are two sets of motion detection pixels that operate independently. TA pixels employ temporal averaging, and PA pixels implement pixel aggregation. Since these three detection pixels sit on three different columns, TA and PA pixels can be independently controlled and read out, allowing concurrent dual-mode operation with two different integration period. Additionally, the photodiodes of PA-Base pixels can be selectively merged with PA detection pixel for pixel aggregation through the charge sharing network.

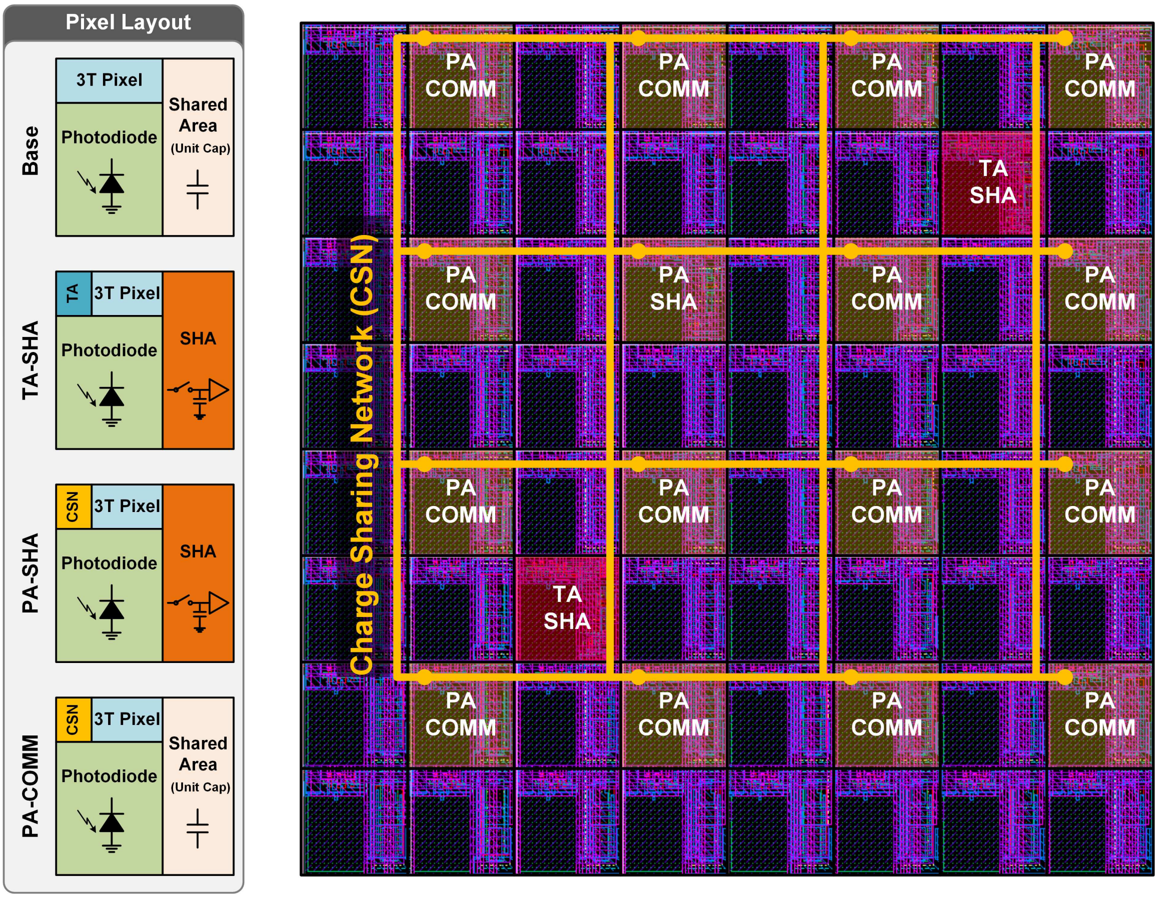


Figure 3.6: Simplified layouts of individual pixels (left) and actual layout of motion detection cluster in 130 nm CMOS technology.

To minimize the area overhead of in-pixel motion detection, the MD circuitry is distributed within the cluster across its 64 pixels, resulting in a pixel fill factor of 38%. Within each MD cluster, two TA pixels and one PA pixel are placed in an interleaved fashion for dual-mode operation, forming a 32 $\times$ 16 resolution TA array and 16 $\times$ 16 resolution PA array. TA is implemented by increasing the integration capacitance by 3$\times$ and extending the integration period in the frame controller. PA is implemented by charge-sharing photodiodes at the circuit level.

3.3.2 Pixel Schematics & Layout

There are four types of pixels in the array: base, TA-SHA, PA-SHA, and PA-COMM. Figure 3.6 shows the simplified layout of individual pixels. Pixel and column peripheral schematics are shown in Figure 3.7. The base pixel uses a conventional 3-T structure with reset device M0, source

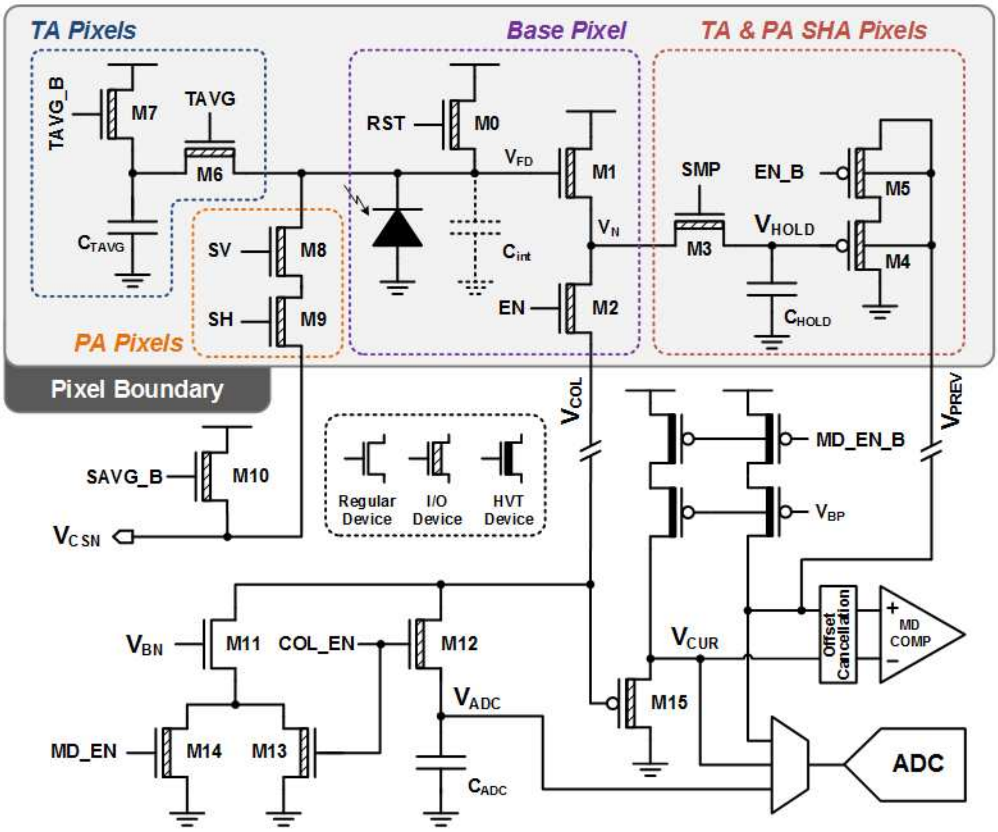


Figure 3.7: Pixel and column schematics. Different pixels have different add-ons to the base 3-T pixel.

follower input device M1, and column line access device M2. A 15.6 μm^2 psub/n+ diffusion diode is used as the photodiode. In the base pixel, the intrinsic parasitic capacitance of the diode is used as an integration capacitance. The base pixel is used only for regular imaging, and its spare layout area is shared for capacitance distribution. The TA detection pixel consists of a TA-SHA pixel, an explicit integration capacitor, C_{TAVG}, and another explicit capacitor C_{HOLD} for frame differencing. C_{TAVG} is required to adjust the integration capacity for longer exposure time. The PA detection pixel consists of a PA-SHA pixel, PA-COMM pixels, and C_{HOLD}.

TA-SHA and PA-SHA pixels include a sample-and-hold circuit consisting of M3-5 and C_{HOLD} to retain the previous frame's pixel value in the analog domain. Subthreshold leakage through M3 is the primary leakage source for V_{HOLD}; hence SMP is pulled low to -200 mV to super-cutoff M3. Simulation shows a maximum leakage-induced droop of 5 mV for 200 ms (<1% of signal range). C_{HOLD} for TA unit is 3× larger than in the PA unit, in accordance with the integration period ratio. All explicit capacitors are distributed in the cluster, with a unit capacitance value of 25 fF. Out of 61 (64 - 3 SHA pixels) available shared slots, 24 $\times$ 2 are used for TA C_{HOLD}, 3 $\times$ 2 for TA C_{TAVG}, and 7 for PA C_{HOLD}. M8-9 connect PA photodiodes to the cluster's charge sharing network, V_{CSN}. Up to 4 $\times$ 4 PA-COMM pixels can be selectively aggregated with PA-SHA per cluster. All devices in the pixel array, including capacitors, are thick-oxide I/O devices to minimize gate and subthreshold leakage.

3.3.3 Operational Modes

The frame controller is the main finite state machine that generates row and column control signals depending on the operational mode. It also triggers the ADC for a given row readout operation, by resetting the ramp generator and starting the column counter. There are three modes of operation: imaging (IMG), motion detection (MD), and an additional motion readout (MD Read) mode for testing purposes. The respective timing diagrams in each mode is shown in Figure 3.8. During IMG mode, all of the components are used. For delta-reset sampling, the ADC counts up during column readout and counts down during pixel reset. During MD mode, ADC is unused, minimizing the power consumption. Only the rows and columns that contain an MD detection pixel are enabled for readout. The output in this ultra-low power mode is 2-bit value per detection pixel: motion flag and direction. During MD Read mode, the ADC is used to read out the previous and current pixel values feeding into the MD comparators for debugging purposes. Therefore, the ADC is triggered twice per each row readout and its output can be used to verify the functionality of MD circuitry.

3.3.4 Clocking

A unique aspect of an image sensor is that the operational time is usually in tens or hundreds of milliseconds. So the time scale of system-level control signals, such as the integration time counter and signals for row-wise readout controls tend to be in milliseconds. At the same time, time scale of row/column signals enabling the analog circuits needs to be short to minimize the analog power consumption. A single fast clock could be used to control both the short and long time scale, but would result in excessively wasted switching power. For example, to turn on a column source

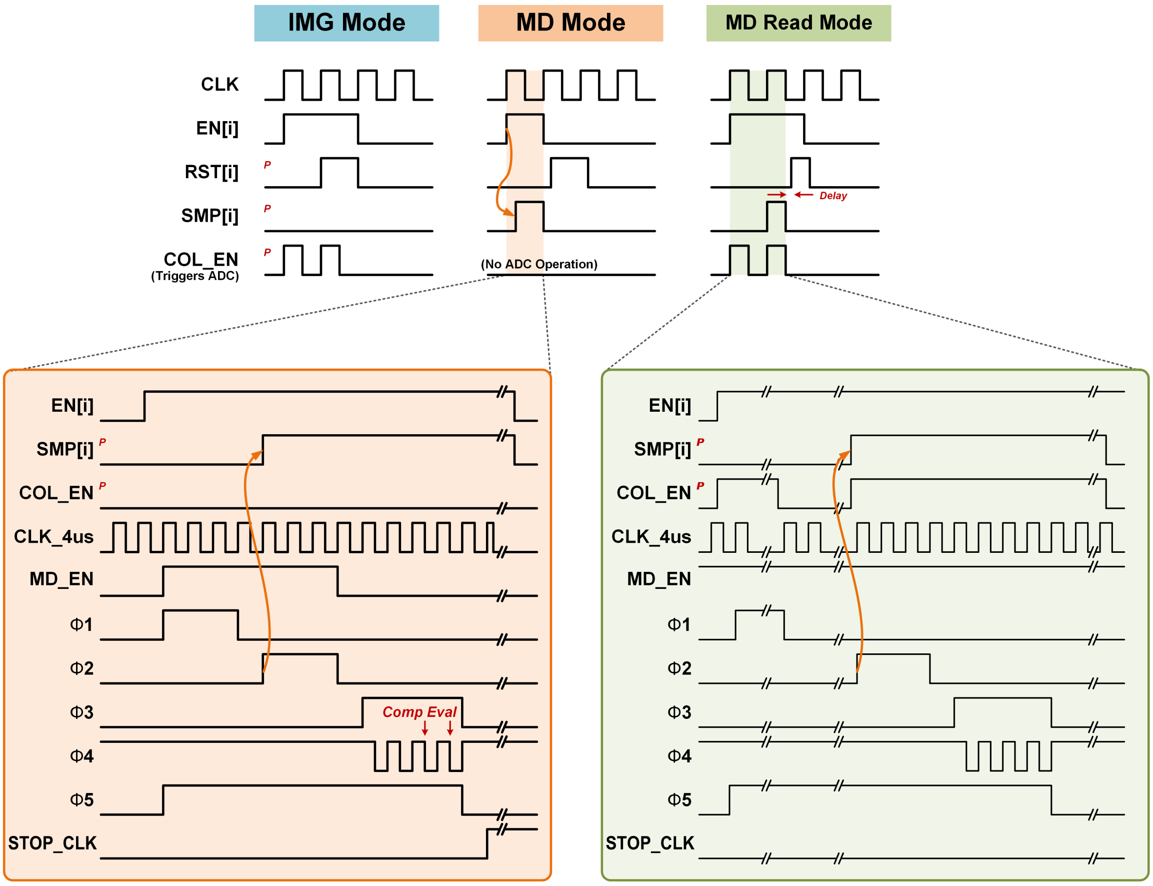


Figure 3.8: Timing diagram of three different modes of operation.

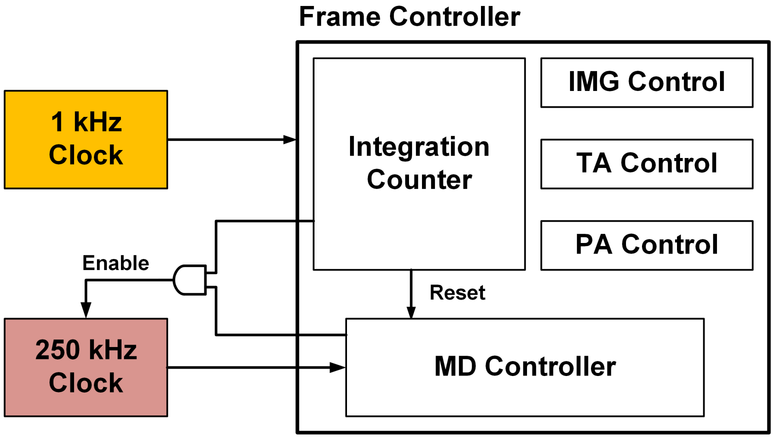


Figure 3.9: Clocking scheme of frame controller. The 250 kHz clock is only enabled during column readout of MD columns to minimize power consumption.

follower for a configurable 10 μs every 10 ms of integration time, a time scale of at least 5 μs is required, which means the controller would spend 2000 cycles consuming clock distribution power for anything but simple counting. To address this issue, two techniques are used to provide short time scale control signals with the main controller clocked at long time scale: pulse generation and clock-gating. There are three clock generators in the proposed design: 1 MHz clock for ADC, 250 kHz clock for ϕ generation by MD controller, and 1 kHz clock for frame controller (Figure 3.9). The ADC clock is always clock-gated during MD mode. The 250 kHz clock is only enabled 1 ms before the MD readout occurs, and is clock-gated by the MD controller itself. Digitally tunable pulse generators are placed after the row control signals generated by 1 kHz clock, only turning on analog tail currents for microseconds.

3.3.5 Column Readout Scheme

Column readout for both imaging and motion detection uses the n-type source follower M1, whose output is sampled by M12 onto C_{SMP} when COL_EN is high. For columns with MD detection pixels (3 per 8), additional column peripheral circuitry including M14-15 is added. During MD mode, the previous pixel value on C_{HOLD} is buffered through a p-type source follower M4, and the current pixel value is buffered twice through M1 and M15 to provide the same common mode. The resulting two analog signals, V_{PREV} and V_{CUR}, feed into the MD comparator to determine the presence of motion. The only mismatch that must be considered between V_{PREV} and V_{CUR}

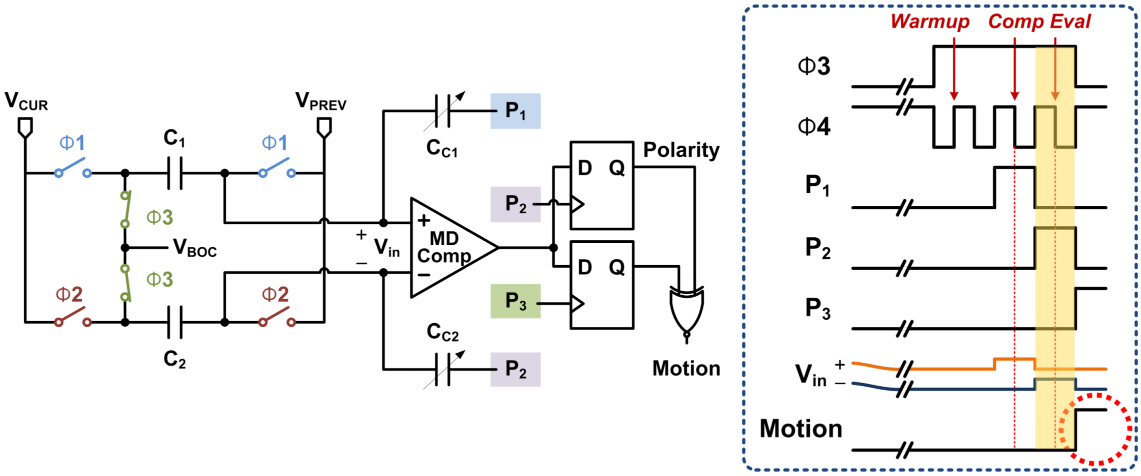


Figure 3.10: Offset cancellation and MD thresholding circuit schematics (left) and timing diagram (right). The example scenario shows motion being detected.

arises from process variation between M4 and M15, and is addressed with an offset cancellation scheme, described in Section 3.3.6. A 9-bit single-slope ADC with digital delta reset sampling is implemented per column to capture regular images and is only used during imaging mode.

3.3.6 Motion Detection Scheme

The schematics and timing diagram for offset cancellation scheme and MD thresholding are shown in Figure 3.10. When one integration period is complete, the MD controller and 250 kHz clock are enabled. The ϕ's are generated by the MD controller and the pulses P_1-P_3 are generated from $\phi 2$ and $\phi 4$. The source followers of Row [i] are enabled by EN[i] and MD_EN, after which the difference between V_{PREV} and V_{CUR} is sampled onto C_1 by $\phi 1$. When SMP[i] goes high, the previous pixel value is overwritten by the current pixel value, and V_{CUR}-V_{PREV} now represents the V_{th} mismatch between M4 and M15, which is sampled onto C_2. During $\phi 3$, the actual frame differencing occurs, with C_1 and C_2 in series subtracting out the V_{th} mismatch for motion detection comparison. During this phase, motion detection comparator fires three times. Since the comparator is only powered on during $\phi 3$, the first comparison serves as warm-up to make sure the bias voltages are stabilized and there is no hysteresis from waking up. The next two comparison occurs in accordance with a capacitive thresholding scheme.

Thresholding is implemented for two purposes. 1) It prevent against false trigger caused by small temporal noise. 2) Depending on the applications, it can be useful to have configurable levels of the detection threshold. During the first comparison after the warm-up, coupling capacitor C_{C1} raises the + terminal of V_{in}. In the second comparison, coupling capacitor C_{C2} raises the - terminal of V_{in}. The two comparison outputs are stored in the flip-flops, which are XNORed to generate motion detection flag. In the example of Figure 3.8, $|V_{CUR}$- $V_{PREV}|$ is smaller than the detection threshold, so motion flag stays low. If $|V_{CUR}$- $V_{PREV}|$ is larger than the detection threshold, the two comparator outputs agree, and motion is flagged. In this scheme, the detection threshold can be digitally tuned by changing the coupling capacitance value. After marching through 16 rows, $\phi 5$ cuts off static power through the MD comparator and the 250 kHz clock is disabled until the subsequent integration finishes.

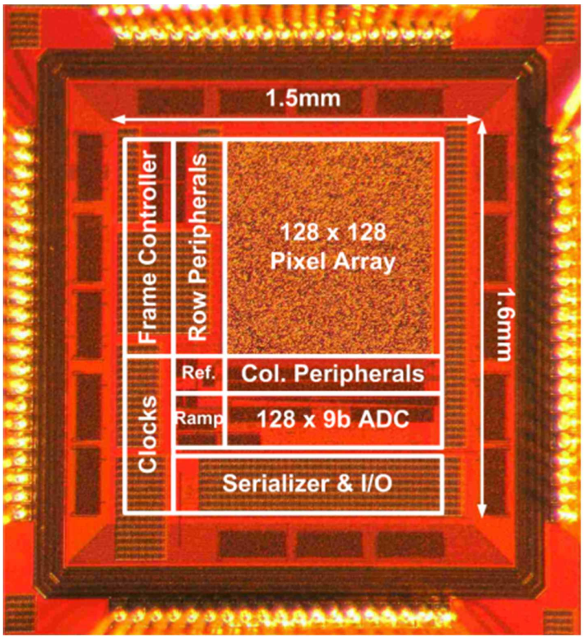
3.4 Measurement Results

The proposed design was fabricated in a logic 130 nm 8M1P CMOS technology. Figure 3.11 shows the die photograph along with technology information. A parasitic N+/Psub diffusion diode was used as photodiode, with fill factor 38%. Motion detection resolution is 48 $\times$ 16, but up to 64 $\times$ 72 pixels is used to provide coverage with pixel aggregation. The area of the chip not including bond pads is 2.4 mm^2.

3.4.1 Effectiveness of Motion Detection Techniques

To systematically experiment the motion detection capability, a program was written to display a moving object with configurable size and speed on an LCD screen, which was observed by the test chip. Figure 3.12 shows the effectiveness temporal averaging in detecting very slow motions. Temporally averaged pixels, shown in orange, sees up to 42% increase in motion intensity (as defined in Section 3.2) for objects moving slower than 70 pixels/sec. This enables easy detection of motion as slow as 3 cm/sec at 5 m observation distance (earthworms move at 2 cm/sec). Since the proposed design has two sets of detection pixels concurrently running at two different frame rates, it can effectively cover a wide range of motion speed.

Figure 3.13 shows the effectiveness of pixel aggregation. As we decrease the size of moving



Technology	0.13µm 8M1P CMOS
Photodiode Type	N+/Psub Diffusion
Pixel Size	6.4 x 6.4 µm^2
Photodiode Size	3.4 x 4.6 µm^2
Pixel Fill Factor	38%
Imaging Resolution	128 x 128
Motion Detect Resolution	48 x 16 (Up to 64x72 pixels w/ PA)
Area	2.4 mm^2(Core)

Figure 3.11: Die photograph of the fabricated test chip (left) and imager specifications (right).

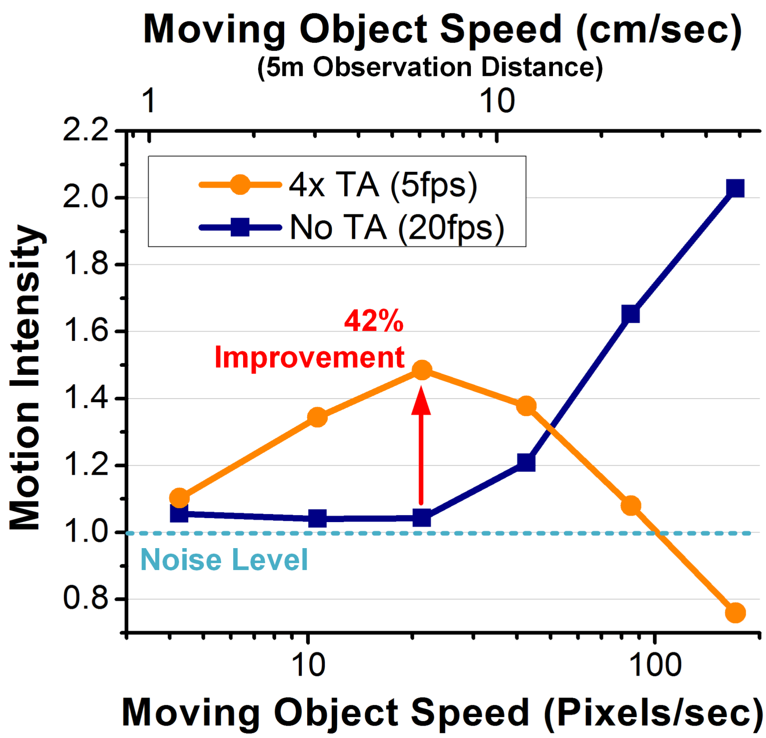


Figure 3.12: Measured motion intensity vs. speed of motion. Temporal averaging improves motion intensity by up to 42% for motions slower than 70 pixels/sec.

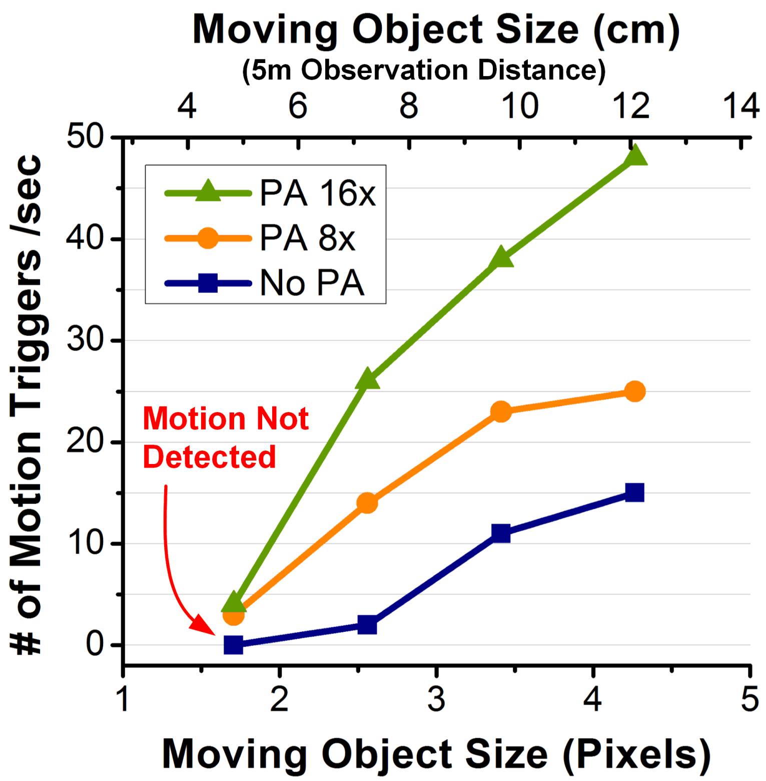


Figure 3.13: Measured results for pixel aggregation. Without pixel aggregation, objects smaller than 2.5 pixels can escape detection entirely.

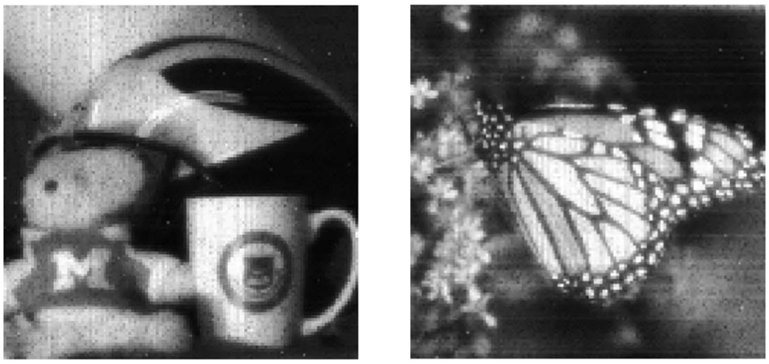


Figure 3.14: Sample images (128 $\times$ 128 resolution).

object in the program, fewer number of pixels detect motion. If we do not enable pixel aggregation, moving object smaller than 2 pixels can escape detection entirely. With maximum pixel aggregation, we can ensure nearly full frame coverage.

3.4.2 Imaging and Motion Detection Results

Figure 3.14 show full resolution sample images taken during imaging mode with the 9-bit ADC with delta reset sampling. The left image was taken with real objects, and the right butterfly image was shown on an LCD monitor. There is no systematic artifact from the added in-pixel motion detection circuitry.

The same ADC used to read out the full-frame image is used to read out the analog input of the motion detection comparator during MD Read mode for testing purposes. The set of images in (Figure 3.15) show the inter-frame difference of a hand moving across the field of view for PA and TA pixels. The motion detection comparator output matches the ADC image without any false triggers, confirming the functionality of frame differencing with detection thresholding.

3.4.3 Power Consumption

In MD mode, the sensor consumes 467 nW at 5 fps with both TA and PA enabled. In imaging mode, the chip consumes 16 μW at 6.4 fps. These numbers include every component in the chip such as clock and bias generators, except test harness such as scan chain and pads. At the slowest frame rate, leakage power dominates, at 75% (Figure 3.16). The pie chart shows power breakdown during motion detection mode and there is a balance between digital and analog components.

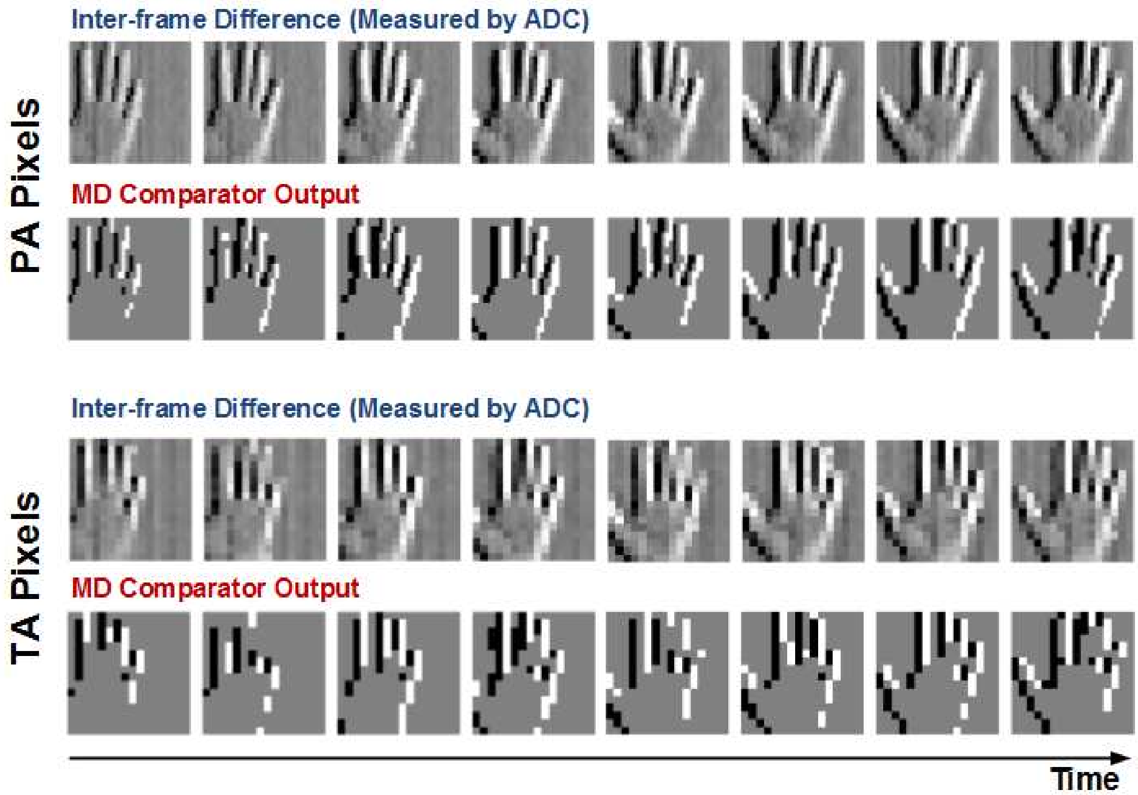


Figure 3.15: Motion detection output of a moving hand captured over 8 frames. The MD comparator outputs agree with the actual inter-frame pixel difference, which is measured by in MD Read mode for testing purposes. Both PA and TA pixels show clear detection of a moving hand.

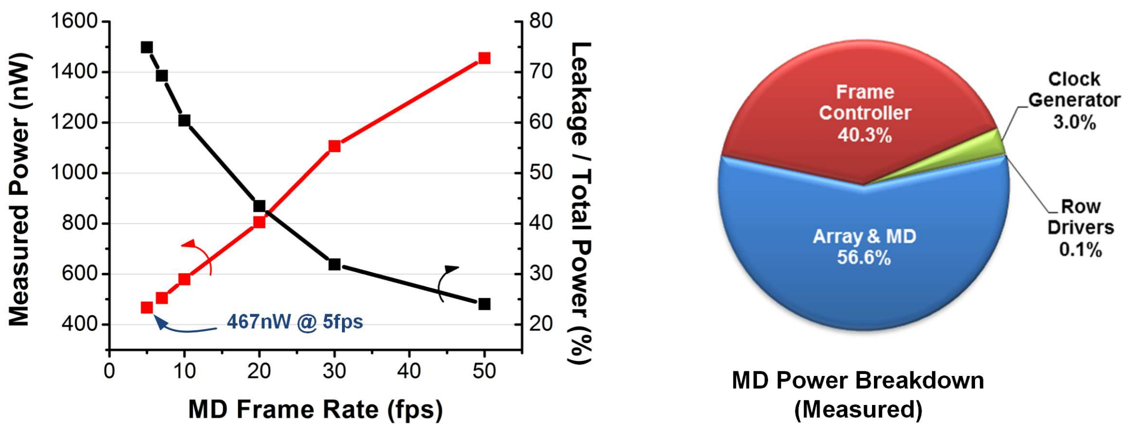


Figure 3.16: Measured power consumption vs. frame rate (left). Power breakdown shows a balance between analog and digital components (right).

	[Chi2007]	[Lichtsteiner2008]	[Hanson2010]	This Work
Technology	0.5μm CMOS 3M2P	0.35μm CMOS 4M2P	0.13μm CMOS 1P8M	0.13μm CMOS 1P8M
Array Resolution	90 x 90	128 x 128	128 x 128	128 x 128
MD Resolution	90 x 90	128 x 128	–	48 x 16
Pixel Size	25 x 25 μm^2	40 x 40μm^2	5 x 5 μm^2	6.4 x 6.4 μm^2
Fill Factor	17%	9.4%	32%	38%
FPN	0.5%	2.1%	6.6%	2.3%
Dynamic Range	51dB	120dB	23.4dB	38.5dB
Imaging Power	4.2mW @ 30fps	23mW, Asynchronous	1.2 μW @ 8.5fps	16μW @ 6.4fps
MD Power[2]	398μW @ 30fps	1.1mW, Asynchronous	–	467nW @5fps 1.1μW @30fps
Supply Voltage	3V	3.3V	0.5V	1.2V / 0.6V
Die Size	9mm^2	37.8mm^2	1.1mm^2 (Core)	2.4 mm^2(Core)

[1] Scaled for 128x128 imaging
[2] Scaled for 48x16 MD

Table 3.1: Comparison table to previously reported motion detectors and a low power imager.

3.4.4 Comparison to Prior Art

Table 3.1 summarizes the performance characteristics of the proposed image sensor and compares them against previous works. At 38%, the proposed design achieved more than twice the fill factor of previous motion detectors, and even higher than the low power imager presented at [38], which was an imager only design. Power consumption for motion detection scaled for the same number of motion detection pixels shows two orders of magnitude reduction. This huge reduction is in part due to technology scaling, as well as supply voltage reduction, in addition to various low power techniques such as biasing the analog amps in sub-threshold region and smart clock-gating of digital components.

3.5 Conclusion

In this chapter, we proposed CMOS image sensor with sub-μW motion detection, bringing continuous motion detection within the realm of mm^3-scale wireless sensor nodes. We use aggressive power gating and clock gating schemes to minimize the power consumption. Furthermore, by implementing motion detection inside the pixel array in the analog domain, we avoid the need to use the ADC, achieving a significant power savings. Along with low power techniques, spatial aggregation of pixels and temporal averaging were proposed to overcome the shortcomings of frame differencing and achieve significant sensitivity improvement.

CHAPTER 4

Energy Harvesting with Microbial Fuel Cells

4.1 Introduction

Benthic microbial fuel cells (MFCs) generate energy from the metabolic process of bacteria in marine sediment. For the MFCs to generate power, the anode must be in contact with bacteria in anaerobic conditions; the cathode floats in the water column where it is exposed to oxygen (Figure 4.1). Electrical current generation is related to the surface area of the electrodes. The anode tends to be the limiting factor because increasing its size makes it more challenging to maintain anaerobic conditions. When these fuel cells fail in the field, it is often attributed to a failure at the anode due to organism aeration of sediment, and incomplete anode burial and insertion. Burial of microbial fuel cells in the ocean surface requires divers or sophisticated deployment technologies, which limit the practicality of large-scale mass deployment.

MFCs on the cm^2 scale are more easily hidden, more conveniently deployed, and have lower failure rates. Space and Naval Warfare Systems Center (SSC) Pacific has successfully deployed and tested prototype MFCs [40] [41]. The voltage output level generated by MFCs is lower than most commercially available batteries at 0.4-0.75 V and offers power levels in the 1-100 μW range, which is not suitable for most commercial electronics. This voltage level is determined by the electrochemistry of the microbe system and cannot be easily changed. Additionally, because they operate as an open system in the marine environment, cells cannot be connected in series to increase voltage. Therefore, the electronics must be specifically designed to operate given these low voltage and power levels. In addition, the voltage level of an MFC cannot be assumed constant over a wide

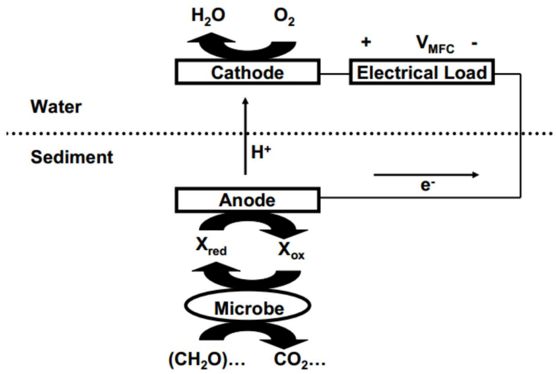


Figure 4.1: Operating principle of benthic microbial fuel cells [40].

range of current draw. This leads to added difficulties in MFC and electronics design. The anode surface area should be chosen large enough to dampen voltage fluctuations as load current changes.

Energy harvesting circuits with MFCs have been previously reported in literature, but reference [42] is an incomplete system without computational or storage capabilities, and [43] relies on commercial components with >10 mW power budget. In this chapter, a system coupling ultra-low power custom electronics with small scale (21.3 cm^2) and low power (5.4 μW) benthic microbial fuel cells is proposed, achieving a self-sustainable sensor system with user-programmable interface suitable for various underwater oceanic sensing applications. After a long-term experiment of 49.3 hours, the proposed system continues to operate with increasing battery voltage, demonstrating a stable system operation.

4.2 System Overview

4.2.1 Ultra-Low Power Electronics

A custom ultra-low power chip (CTRL chip) was designed to harvest energy from benthic MFCs and perform processor operations. Fabricated in a commercial 180 nm CMOS technology, this chip is part of a 1.0 mm^3 die-stacked sensor node system [17]. As the main processing and housekeeping chip of the system, the CTRL chip features an ARM Cortex-M0 processor, 3 kB of SRAM, I^{2}C interface with external sensor components, sleep controller, optical programming interface (FLOW), power-on reset detector (POR), brown-out detector (BOD) and a power-

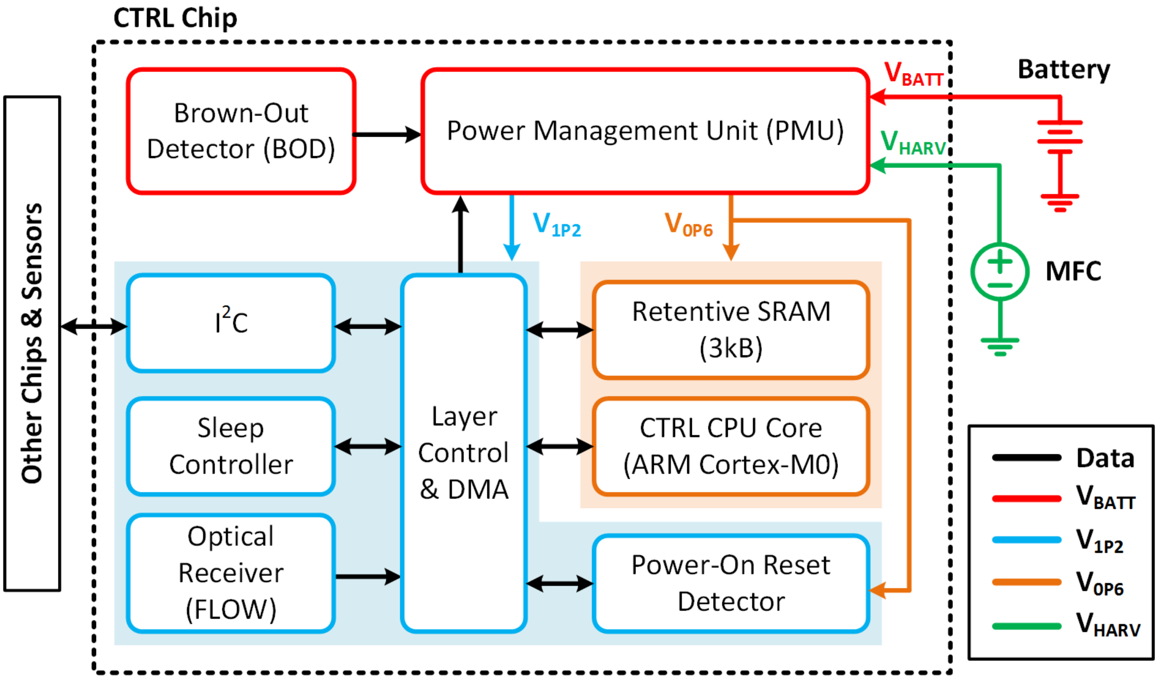


Figure 4.2: CTRL chip block diagram and external connections.

management unit (PMU) (Figure 4.2). Various leakage power reduction techniques limit the overall chip power consumption to only 11 nW in sleep mode, making it ideal for sensor applications with a duty cycled usage scenario.

The core operating at 400 kHz can configure the sleep controller to schedule sleep/wakeup cycles of the whole system. In sleep mode, I^2C block, layer controller, and the core are power-gated. The SRAM is used for storing both instructions and data. Since the custom 8-T SRAM cell has an ultra-low leakage power [16], the SRAM need not be power-gated. Hence, the custom SRAM retains its states as long as 0.6 V supply is present, avoiding the need of a non-volatile memory.

The main data interface of the CTRL chip is a modified I^2C protocol, which uses a time-divided pull-up/pull-down scheme that is still compatible with the standard I^2C protocol and yet avoids the use of conventional pull-up resistors that consume mWs of power [17]. The core can generate I^2C messages through the layer controller to talk to other off-chip I^2C-compatible components via a memory write instruction to a memory-mapped address. I^2C is also used to load the program instructions onto the memory. When wired I^2C connection is impractical, the optical receiver can be used to program the chip with light [44]. This option can be attractive for underwater operations,

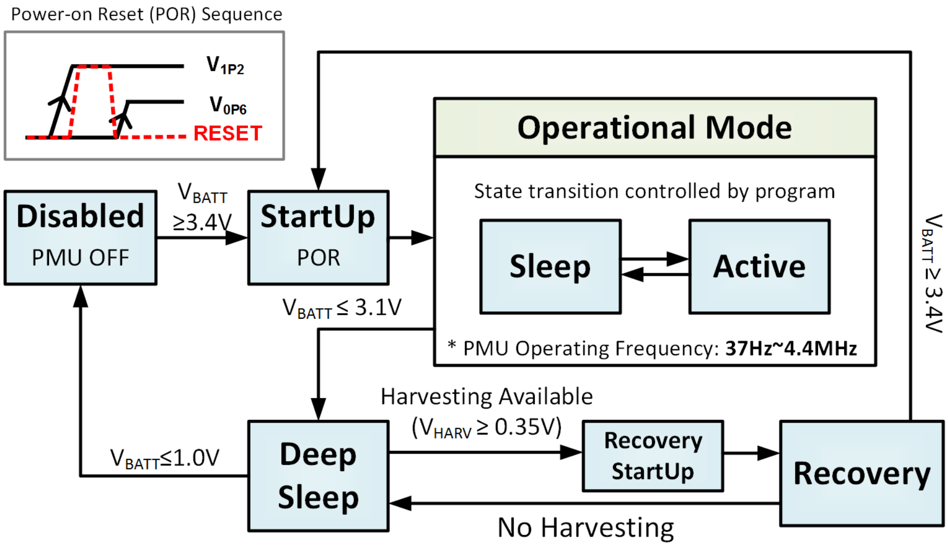


Figure 4.3: State transition diagram of PMU depending on harvesting conditions and battery voltage.

in which exposed wired connection can lead to corrosion or other physical damage.

The PMU takes a nominal battery voltage of 3.6 V and generates two supply voltages, V_{0P6} and V_{1P2} (nominally 0.6 V and 1.2 V, respectively), that are used to power different components of the chip [45]. The PMU is also responsible for harvesting from a source (V_{HARV}) and recharging the battery while in sleep mode. Figure 4.3 shows PMU state transitions in response to battery voltage fluctuation. When the battery voltage stabilizes above 3.4 V, the PMU enters Operational Mode and the system is activated. During Operational Mode, the system can switch between Sleep and Active Modes based on the user-defined program loaded on the memory.

The BOD continuously monitors the battery voltage, and when it detects that the battery voltage has dropped below 3.1 V, it signals PMU to enter Deep Sleep Mode to prevent the battery from over-discharging [46]. During Deep Sleep Mode, all supply voltages are turned off and the system only consumes 185 pW. Since SRAM is also powered down in this mode, its content is lost and the chip needs to be re-programmed. Harvested energy availability is monitored in while the system is in Deep Sleep Mode. The system enters Recovery Mode when sufficient power is detected. In this mode, the battery is recharged from the harvesting source until the battery voltage increases above 3.4 V. At this point, the system returns to its normal Operational mode.

4.2.2 Small-Scale Microbial Fuel Cell (MFC)

Six micro-MFCs were set up for experiments in the laboratory environment inside an aquarium of size 45 x 90 cm^2. Sediment from the Marine Corps Recruiting Depot marina in San Diego, CA was collected during low tide. The aquarium was filled with the 15-cm deep sediment. 25 cm of salt water above the sediment was continuously exchanged with surface water pumped from the San Diego Bay. The MFCs are comprised of graphite rod anodes and carbon fiber brush cathodes. The graphite rod anode was 1.9 cm in diameter. Three different anode lengths (2.5, 5.0, and 7.5 cm) with a respective surface area of 7.1, 15.2, and 21.3 cm^2 were evaluated as anodes for MFCs supplying power to the electronics. Electrical contacts for the anode were created by drilling a small hole (0.08 cm) located 1.3 cm from one end, through which titanium wire was threaded through the hole and tightly twisted for secure contact. The carbon-fiber brushes used as cathodes for each of the MFCs were identical (12 cm length x 12 cm diameter) and consisted of carbon fiber fixed in a titanium wire stem. The cathode was overdesigned to ensure that the device would be anode limited, in order to observe the limitations of $<$21.3 cm^2 anodes. Initially, the anodes were pushed into the sediment vertically with the titanium wire oriented towards the top of the sediment to emulate the deployment of a dart type MFC design. The cathodes were hung vertically in the overlying water. In order to condition the MFCs for use with the electronics, they were operated under varying conditions to maintain a cell voltage greater than 0.5 V. They were left under open circuit conditions for 24 hours followed by sequential loading of passive resistors. After 12 days, the MFCs were maintaining a voltage ranging from 0.6-0.7 V while generating 17-22 μW. A MFC with 21.3 cm^2 anode was selected for system integration testing because of its stability and performance compared to the smaller MFCs.

4.3 Experimental Results & Analysis

4.3.1 System-Level Experiment Setup

A PCB board was designed for system integration testing with two sections: SYSTEM and DEBUG (Figure 4.4). The SYSTEM portion was designed to mimic the die-stacked system in [17], by replacing the inter-layer bond-wire connections with PCB traces. It includes the CTRL

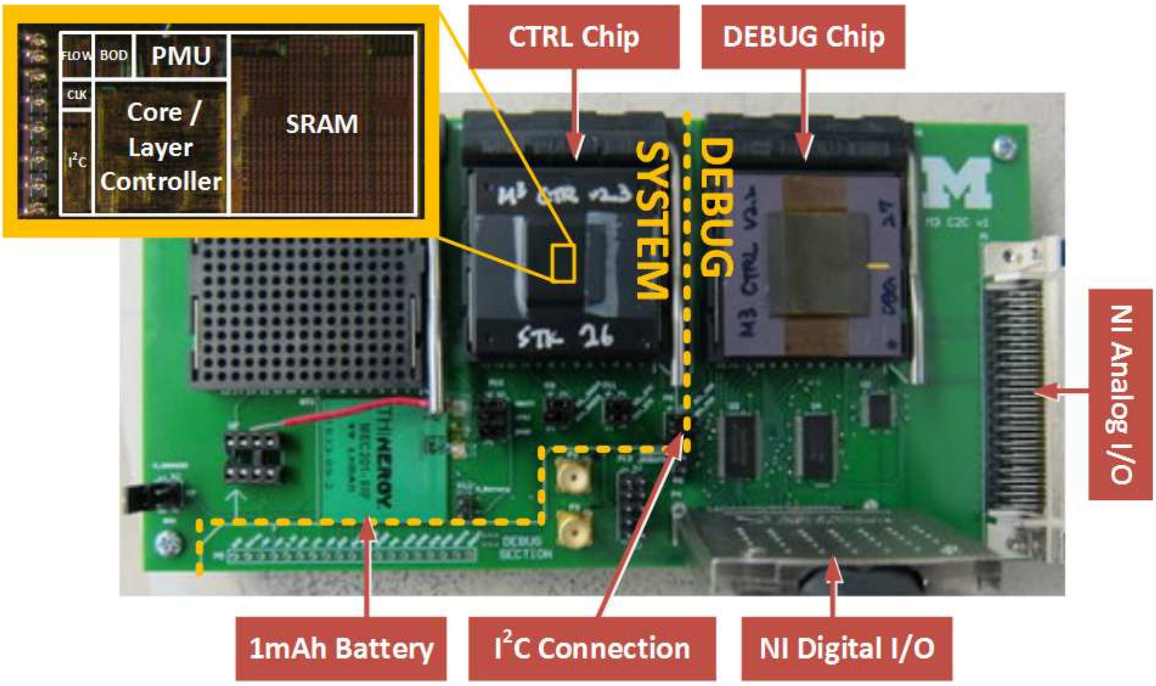


Figure 4.4: PCB board used for integration testing and die photograph of CTRL chip. Dashed line indicates boundary between SYSTEM and DEBUG sections.

chip, a commercial 4 V 1 mAh thin-film battery, and additional sockets for pressure sensor and other sensing modalities.

The DEBUG section of the board houses a DEBUG chip, which is a variant of CTRL chip that has additional peripheral circuitry for debugging purposes, such as a scan chain to override important system signals and observation blocks for I^2C and clock signals. The DEBUG chip interfaces through National Instruments (NI) digital and analog cards with a custom LabVIEW program and serves as the primary interface between the end user and CTRL chip. Its main role in this system is twofold: programming the CTRL chip and monitoring the I^2C wires to observe the status of the CTRL chip. The only electrical connection between the DEBUG and CTRL chips are the two I^2C wires and ground. Once the CTRL chip is programmed, the DEBUG section can be disconnected for field deployment of the system.

Figure 4.5 shows the system-level testing connections. MFC was connected to V_{HARV} terminal of the CTRL chip, allowing the PMU inside CTRL chip to up-convert the 0.7 V MFC output and charge the battery at 4 V. The DEBUG chip was used to transfer program code to CTRL chip via I^2C. The program writes a user-defined timer value to the sleep controller, and requests a "go to

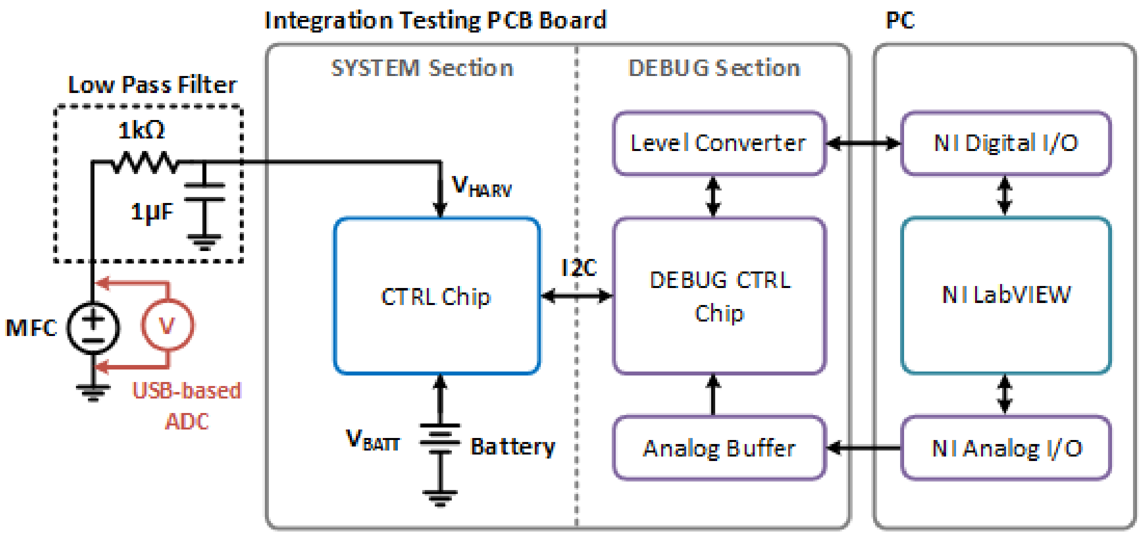


Figure 4.5: Block diagram of MFC + CTRL integration testing setup.

sleep" I^2C message at the end of program execution. The sleep controller then power-gates the core and I^2C block, entering sleep mode. After the internal timer expires, the sleep controller wakes up the core and the same program executes.

Prior to the long term experiment, an accelerated duty cycle test was performed with short sleep time of 7 sec. Intentional loop are inserted in the program to extend the wakeup time to about 1 sec, such that system operation could be easily verified by naked eye. After running the accelerated test for 2 hours, which corresponds to 900 repeated sleep/wakeup cycles, a long term experiment was set up with sleep time of 8 min. During the experiment, voltage and current in/out of the battery were monitored with a high impedance voltmeter and ammeter. With DEBUG chip being connected to LabVIEW, I^2C activity was also monitored, indicating proper program execution. A separate LabVIEW setup with USB-based ADC was used to record the MFC cathode voltage.

4.3.2 Long-Term Experiment

For the long-term experiment, a low-pass RC filter was placed on the output of MFC to decrease the impact of high frequency noise from the USB-based ADC on the stability of the CTRL chip. The RC values of 1 kΩ and 1 μF were used to give corner frequency of 1 kHz, which is fast enough to track the change in MFC voltage over time. The DEBUG section was also disconnected, emulating a field deployment environment. With this setup, the integrated chip-on-mud system

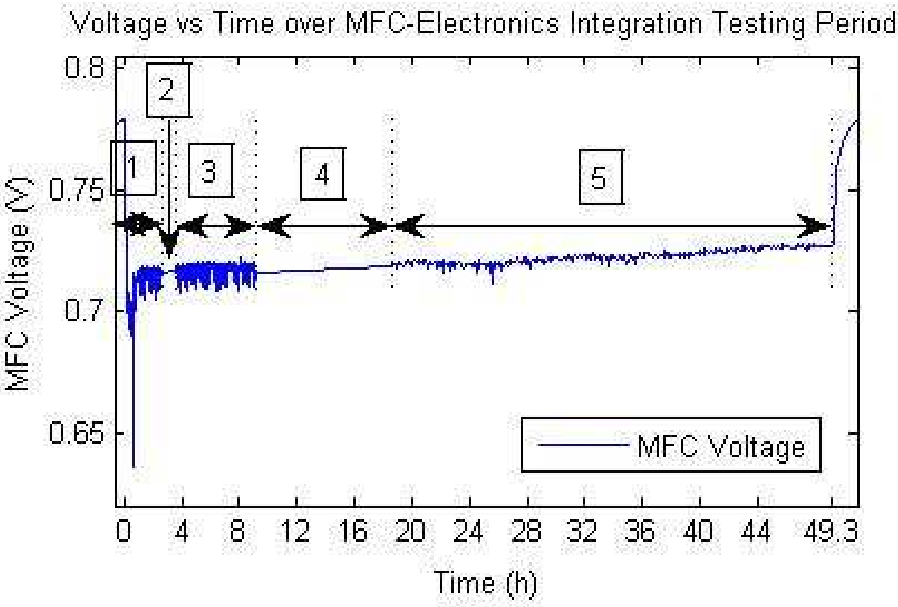


Figure 4.6: MFC voltage verses time (in hours). The electronics were connected with the MFC at hour 0 and disconnected at hour 49.3. The electronics remained in continuous operation during this period.

operated for 49.3 hours, demonstrating long-term stability and sustainability.

Figure 4.6 shows the measured MFC voltage vs. time over the 49.3 hour period, broken into five different regions. The MFC voltage was sampled at 2 samples per second in regions 1-4. Region 2 is a period of data acquisition failure that lasts for 1.5 hours. In Region 3 the data acquisition software is restarted and the sample rate continues to be 2 samples per second. Region 4 shows another data acquisition failure that lasts for 9.5 hours (overnight). In Region 5 the data acquisition software was restarted and the sample rate changed to 1 sample per 5 minutes to avoid further data acquisition failures. This region extends to the end of the integration experiment at hour 49.3, when the electronics are disconnected. The MFC voltage then begins to approach the open circuit voltage. The experiment was intentionally stopped by disconnecting the MFC from the chip, due to collaboration time constraints.

Figure 4.7 shows Region 1 in more detail, showing the loading effect of CTRL chip's PMU on the MFC, with the voltage dropping from 0.78 V to 0.7 V. When the DEBUG chip is used to initially program the CTRL chip, large current is drawn by the I^2C unit and layer controller, resulting in a further MFC voltage droop to 0.64 V. Upon completion of the initial programming,

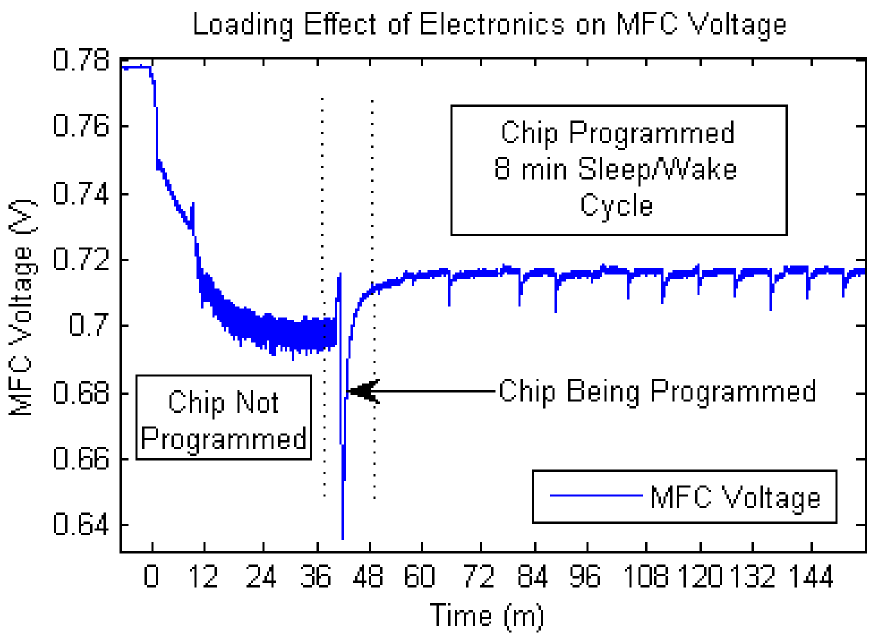


Figure 4.7: The MFC voltage verses time (in minutes) during the early period of electronics integration, Region 1. This figure more clearly shows the effects of loading the MFC and programming the electronics. The maximum peak to peak voltage difference is 20 mV after the electronics are programmed.

the chip goes into sleep mode and the MFC voltage rises to 0.72 V. Afterwards, voltage spikes begin to appear at uniform intervals, corresponding to the CTRL chip's duty cycle in which the chip wakes up every 8 minutes, executes the program for 1-2 seconds, and then goes back to sleep.

The voltage of the battery at the beginning of the long term experiment was 4.0908 V. At the end of the experiment, the battery voltage was recorded at 4.0932 V. This increase in energy stored in the battery over the course of the experiment confirms the capability of MFCs as a power source to keep the integrated system self-sustainable. The average current generated by the MFC during the integration period was 7.5 μA. With the average MFC voltage being 0.72 V during integration, this corresponds to 5.4 μW of power generation. The harvested current into the battery from the PMU harvesting circuit was 380 nA during sleep mode. With a usage scenario of waking up every 10 minutes for 10 ms to retrieve data from a sensor and storing it, the battery can supply 20 mA of current during the active mode without losing net energy.

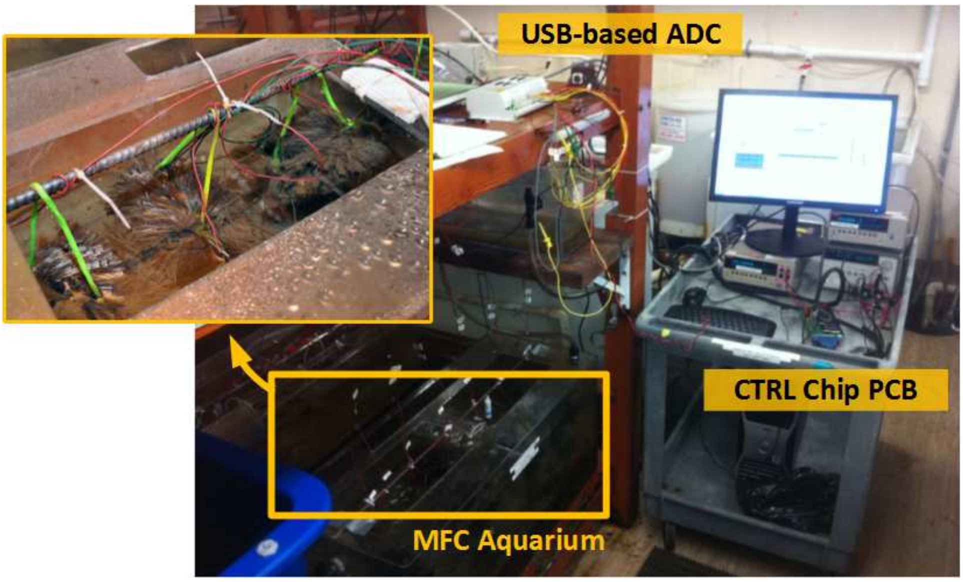


Figure 4.8: Experimental setup of chip-on-mud system integration testing.

4.4 Conclusion

In this chapter, microbial fuel cells was investigated and demonstrated as a means of energy harvesting for wireless sensor nodes. At the core of the system is the CTRL chip with ARM-based CPU, SRAM, I^2C interface and power management unit, with extremely low 11 nW standby power. The proposed system was able to harvest 380 nA net current from a small-scale MFC to charge the 4 V battery, offering a perpetual oceanic sensing solution. With commercially compatible I^2C interface and ARM-based core, the system offers user-friendly environment for third-party users.

CHAPTER 5

Millimeter-Scale Wireless Imaging System

5.1 Introduction

Visual sensing is a highly desired feature for wireless sensor nodes. Recent advances in low power circuit techniques and integration have resulted in self-sustaining wireless sensor nodes as small as 1 mm^3 [13] [16] [17] . However, achieving a complete visual sensing system in similar volume is challenging due to physical difficulties in integrating optics and the high power consumption of key components such as the image sensor and RF transmitter. Despite the challenges, a significant demand remains for achieving visual sensing in such small volume for many applications. One of the obvious applications is visual surveillance for both military and consumer uses [47]. Other applications include smarter home and office [48], environmental monitoring [49], and academic applications such as biological and social studies of insects or birds [50]. The common theme in these applications is that being able to visually monitor moving objects without being easily noticed can be extremely valuable.

In this chapter, a millimeter-scale wireless sensor node with visual imaging and ultra-low power motion detection is presented. The proposed visual sensing system measures merely $2 \times 4 \times 4$ mm^3 in volume, but features complete imaging and computing capability with optics, wireless communication, solar energy harvesting, and battery (Figure 5.1). Despite these comprehensive features, the overall power consumption of the proposed system in sleep mode is 304 nW with motion detection enabled, allowing energy-autonomous operation with typical daytime lighting condition on a window or on the surface of an indoor light source. The system also features on-

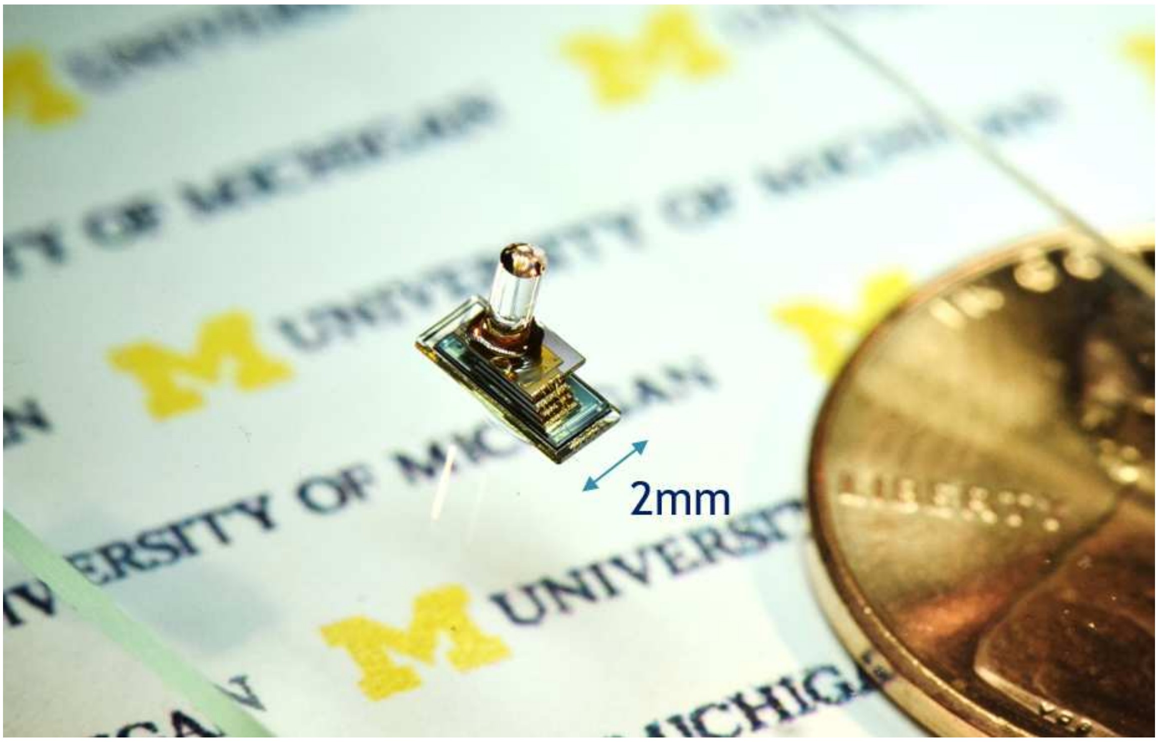


Figure 5.1: Proposed millimeter-scale wireless visual sensing system.

demand duty-cycling, in which the system wakes up when triggered by motion to capture an image and can restrict the read out to the portion of the image where motion was detected.

5.2 System Overview

The proposed visual sensing system consists of six layers of chips and battery that are die-stacked, optics and solar cells. The proposed system is based on the sensing platform described in reference [17], with an ARM Cortex M0 processor and 3 kB SRAM to store data and instructions. A new version of the image sensor discussed in Chapter 3 is designed for higher resolution and lower power, an improved version of the wake-up receiver discussed in Chapter 2 is included for faster data rate, and a robust low power digital interconnect scheme replaces the I^2C interface. A new inter-layer bus scheme is introduced, and an RF transmitter is also included with on-chip inductor coil to achieve two-way wireless communication along with the optical receiver. In the system assembly process, solar cells are placed facing the opposite direction of the imager, providing an optimal lighting condition for both imaging and harvesting.

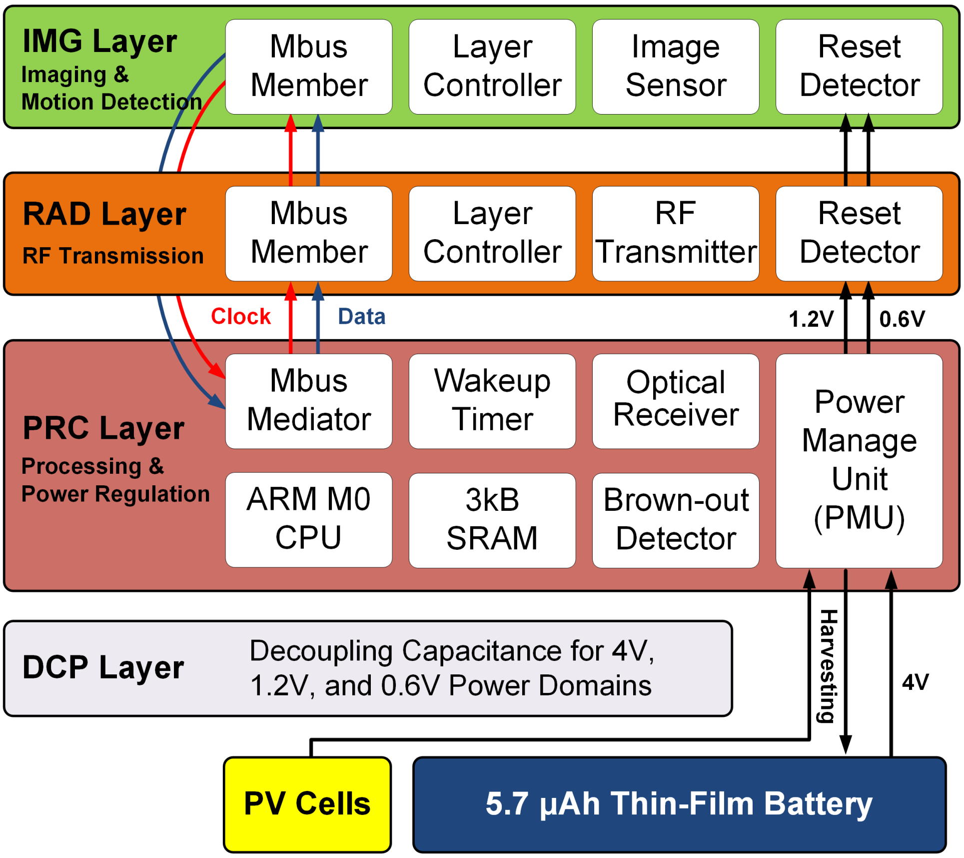


Figure 5.2: Block diagram of components of the proposed visual sensing system.

Figure 5.2 is a block diagram showing the key components of the system. The majority of the system components are placed in the three logic layers – IMG layer, RAD layer, and PRC layer. In addition, there is a layer dedicated to providing decoupling capacitance for the power domains, and photovoltaic cells for solar energy harvesting. A 5.7 μAh thin-film battery provided by Cymbet Corporation is used as the major energy storage of the system, and it measures $2 \times 4 \times 0.2$ mm^3 in size.

The logic layers communicate through Mbus, which is a new fully digital bus designed specifically for ultra-low power and robust operation. The details on Mbus will be discussed in Section 5.3. The PRC layer houses the ARM Cortex M0 CPU, retentive SRAM, and power management unit (PMU) that down-converts the 4 V battery voltage to generate 1.2 V and 0.6 V supply domains. The PMU also up-converts the solar cell output voltage to charge the battery. The 3 kB SRAM features ultra-low leakage bitcell, which limits the standby power of the whole SRAM to less than 100 pW, allowing it to remain powered on during system sleep mode and retain the data.

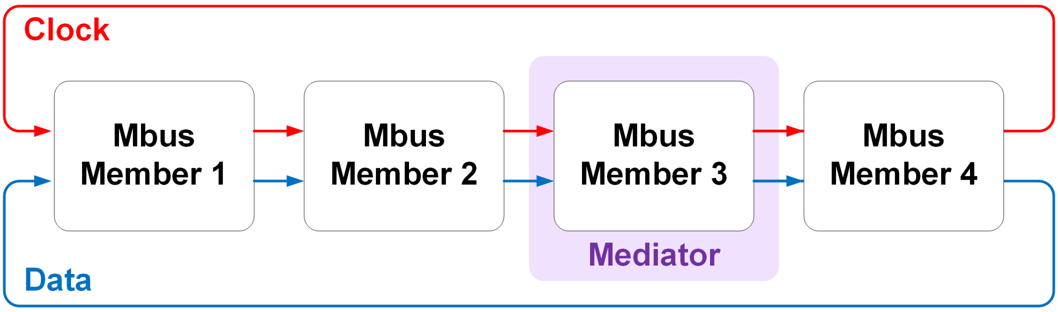


Figure 5.3: Mbus member nodes are connected in a daisy chain topology.

The processor layer also serves as the Mbus mediator, and generates Mbus clock. A wake-up timer and optical receiver is also implemented in this chip. And the brown-out detector ensures that the battery is not damaged from over-discharging.

In each layer, there is a reset detector, which uses 1.2 V and 0.6 V power signals to detect reset sequence generated by the PMU in the processor layer. The RAD layer houses the RF transmitter with Mbus member block to interface with the rest of the system. The IMG layer is home to the image sensor, which features a 80nA ultra-low power motion detection mode, allowing continuous motion detection while the rest of the system is in sleep mode.

5.3 Mbus: A Low-Power and Robust Interconnect Bus

One of the novelties in this work is a new interconnect bus named Mbus, which is used for inter-layer communication in the proposed system. Mbus was designed with particular emphasis on low power, portability, and robustness. Mbus has two unidirectional wires - clock and data - and the members are connected in a daisy chain fashion, as shown in Figure 5.3. Robustness and portability is achieved with fully digital and synthesizable design. One of Mbus members are designated as the mediator, which generates the Mbus clock, and performs arbitration. In the proposed design, the PRC layer is designated as the mediator node, but the location of the mediator node can be anywhere in the loop. And any member can initiate a transaction, which makes it suitable for an energy-constrained sensing system.

Figure 5.4 shows the components inside an Mbus member block, with the IMG layer as an example. The sleep controller, wire controller, configuration registers, and interrupt controller

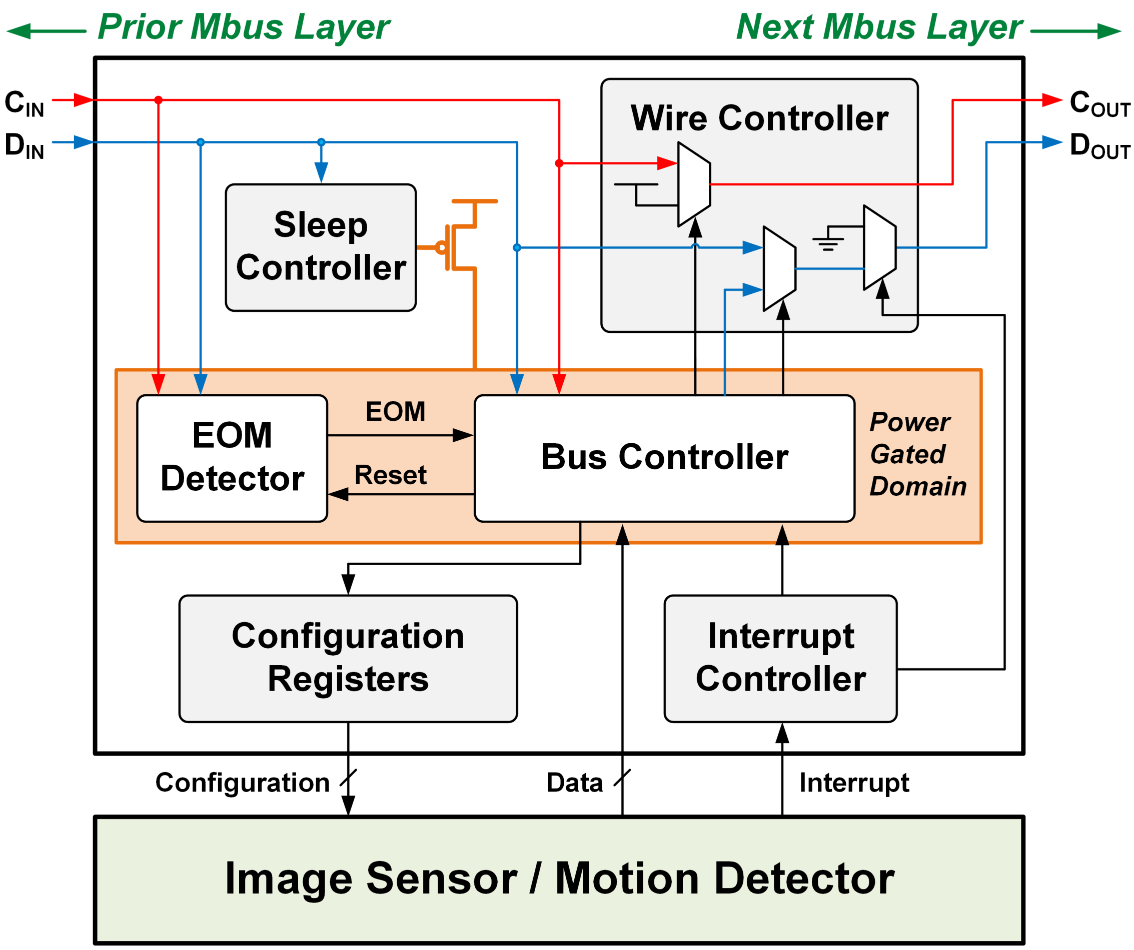


Figure 5.4: Components inside an Mbus member block.

remains powered on at all times. The bus controller and end-of-message detector is power-gated by the sleep controller during sleep mode, resulting in Mbus sleep power of 6 pW per layer.

The Mbus clock wires toggle only when there is bus activity, minimizing the active power. By default, Mbus clock and data lines are kept high and the member node forwards C_{IN} in and D_{IN} to C_{OUT} and D_{OUT}. This default forwarding mode allows accurate synchronization of layers since delay through the daisy chain is small and deterministic, and removes the need for a local clock on each layer, minimizing the power overhead of adding layers to the loop. While the Mbus controller remains in sleep mode, some blocks inside a layer can remain on, as long as the power consumption is within the PMU power budget. During sleep mode, the PMU can support up to 200 nA of load current. In the case of the IMG chip, the image sensor consumes only 100 nA in its lowest power mode, allowing continuous operation in system sleep mode.

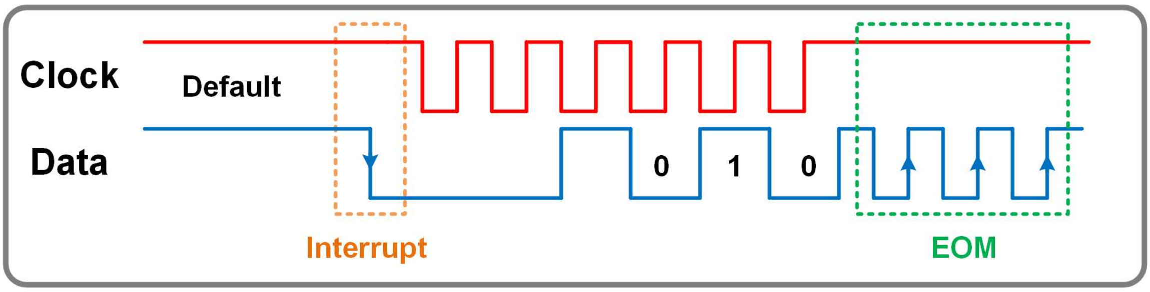


Figure 5.5: Timing diagram of an example Mbus message initiation.

A key feature of Mbus is its interrupt generation during system sleep mode. If a block inside a member node decides to interrupt the bus, which is the case when the imager detects motion, the interrupt controller sends a signal to the wire controller to pull down D_{OUT} to initiate an Mbus interrupt routine. This is shown in the example timing diagram (Figure 5.5). Key thing to point out is that the bus controller is still power-gated at this point, and discharging of the D_{OUT} line does not draw any power from the PMU. This is important because in sleep mode the PMU drive strength is limited, and the parasitic capacitance of the wires between Mbus nodes is unknown and could be large depending on the system implementation.

When D_{OUT} is pulled down, other member nodes forwards this value to the mediator, and the mediator node switches the PMU into active mode to start toggling Mbus clock. During active mode, the PMU can support 10s of uA of load current. Each clock tick is interpreted by the sleep controller of each Mbus layers and it subsequently releases the sleep, isolation, and reset signals to bring up the power-gated domain. Once the clock is running, the member node that initiated the interrupt starts sending an Mbus message. Data is changed at the negative edge of the clock and is read at the positive edge of the clock, easing setup/hold time constraints.

One additional neat feature of Mbus is end-of-message (EOM) detection, which allows flexible message length despite only having two wires. The end of message sequence is encoded as the data toggling three times while the clock stays high, which does not occur during normal message transmission. The EOM detector is also used to allow message interrupt. When a layer issues an interrupt while the Mbus is already active, it blocks the incoming clock (C_{OUT} held high), which is then recognized by the Mbus master. The master then sends the EOM sequence, allowing the interrupting layer to gain control. An EOM detector circuit is implemented with three D flip-flops, as shown in Figure 5.6.

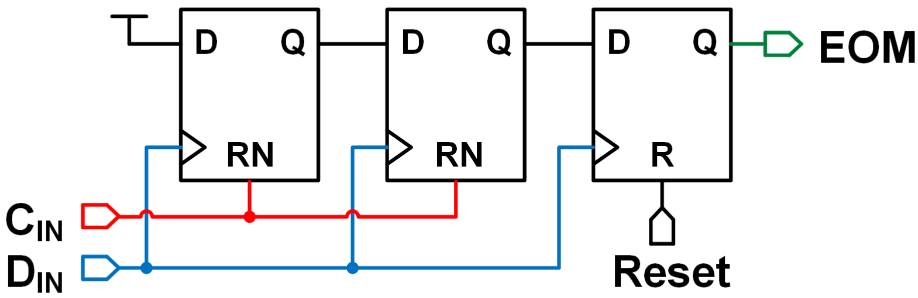


Figure 5.6: End-of-Message (EOM) detector circuit.

5.4 Image Sensor with Ultra Low Power Motion Detection

The image sensor in the proposed system is a new version of the work described in Chapter 3 [51], with higher resolution and even lower power in-pixel motion detection. During full-frame imaging mode, it produces 8/9-bit 160 $\times$ 160 resolution images with cropping and row/column skipping features to reduce data bandwidth and storage. Motion detection pixels of 10 $\times$ 10 resolution are built-in to the array, with temporal averaging to improve detection sensitivity to slow motions [51]. Figure 5.7 shows the block diagram of the image sensor. The pixel array is broken down into motion detection clusters, which consists of 16 $\times$ 16 pixels, and the additional circuits required to perform motion detection is distributed across the cluster. 1.2 V supply is used for the pixel array and comparators, and 0.6 V supply is used for the digital circuits to minimize the switching power.

5.4.1 Pixel & Column Readout Structure

Figure 5.8 shows the pixel & column readout structure. Base pixels have only the 3-T pixel structure for full-frame imaging, whereas the motion detection pixels have additional sample-and-hold circuit to perform frame differencing. The previous frame's pixel value is stored on a hold capacitor and is compared with the next frame's pixel value. A 14-level configurable detection threshold is used to determine if the inter-frame pixel difference is large enough to be flagged as motion. Offset cancellation circuit is implemented to compensate for the PMOS source follower mismatch. Details on the offset cancellation scheme is discussed in Section 3.3.6. By distributing the additional motion detection circuitry across 16 $\times$ 16 pixel MD cluster, 37% pixel fill factor

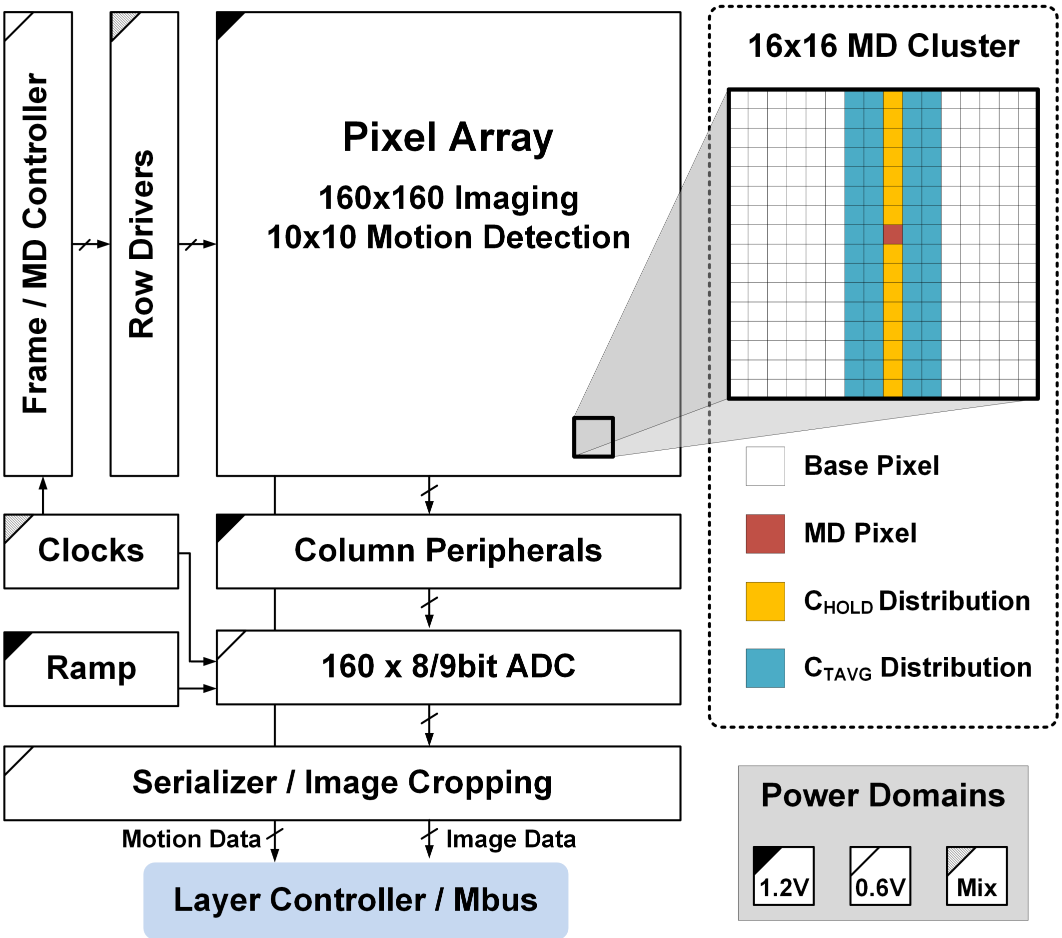


Figure 5.7: Image sensor block diagram.

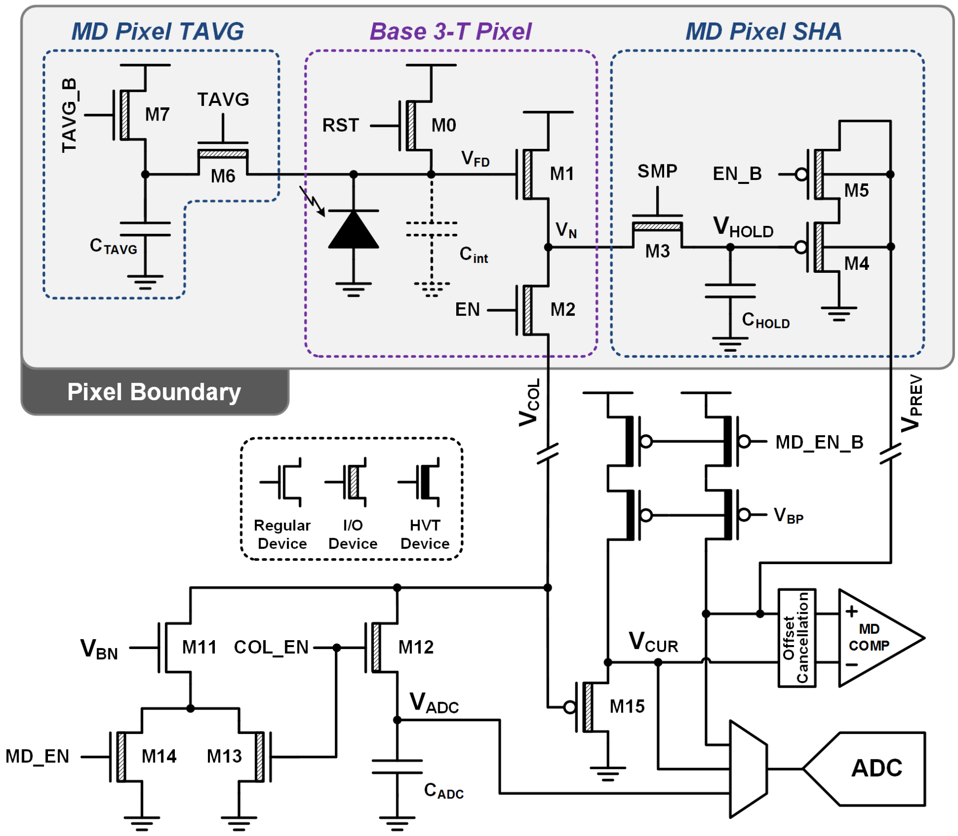


Figure 5.8: Schematic of pixel and column readout structure and motion detection comparator with offset cancellation scheme.

is achieved. The pixel pitch is 5.4 μm, and parasitic n+ diffusion to substrate diodes are used as photodiodes. Since NMOS devices are used for the reset and sample and hold switches, the control signals are bootstrapped to eliminate the threshold voltage drop.

5.4.2 Bootstrapping Circuit

A new bootstrapping circuit is designed to improve the image quality by eliminating reset hysteresis for boosted row control signals. In a practical usage scenario, a single image will be taken once motion is detected. So the very first image that is taken should be of the same quality as the subsequent images. In a conventional bootstrapping circuit (Figure 5.9a), internal node *n1* does not fully charge up to VDD, so the first boosted value after a long idle time is slightly lower than subsequent pulses. This is confirmed with Monte Carlos simulation results (Table 5.1), which show that in the conventional design, the first boosted voltage has a lower mean and higher variation than

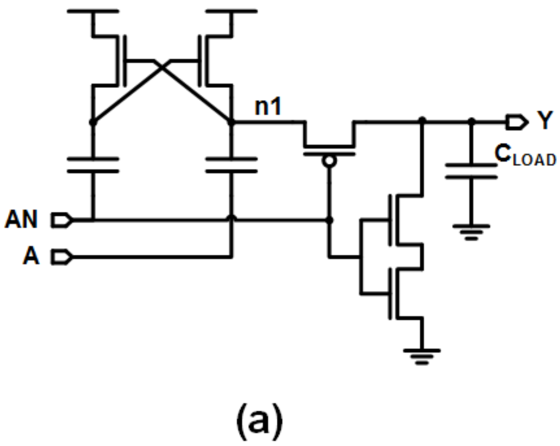


Figure 5.9: Schematics of (a) conventional bootstrapping circuit, and (b) proposed circuit.

		V_{A_first} (V)	V_A (V)
Conventional Design	μ	1.567	1.594
	σ	0.023	0.018
Proposed Design	μ	1.595	1.595
	σ	0.017	0.017

Table 5.1: Monte Carlos simulation results of conventional and proposed bootstrapping circuit.

the rest of the pulses. This larger variation has direct impact on the noise of the image, which is not desirable.

The proposed single-ended design (Figure 5.9b) uses low-V_{TH} NMOS device as a pull-up device and heavy body biasing is employed in the forward direction to make the device very leaky. This way, the internal node *n1* is ensured to be charged to VDD within tens of microseconds. In simulation, the proposed design shows no difference between the first pulse and the subsequent pulses. Figure 5.10 shows simulation results of input being boosted by the two circuits in time domain.

5.4.3 Ultra-Low Power Motion Detection

One of the new features in this version of the image sensor is an aggressive power-gating scheme. During the ultra-low power motion detection mode, the majority of the pixels used for full frame imaging and the ADC are completely power-gated, since the leakage through the photodiode

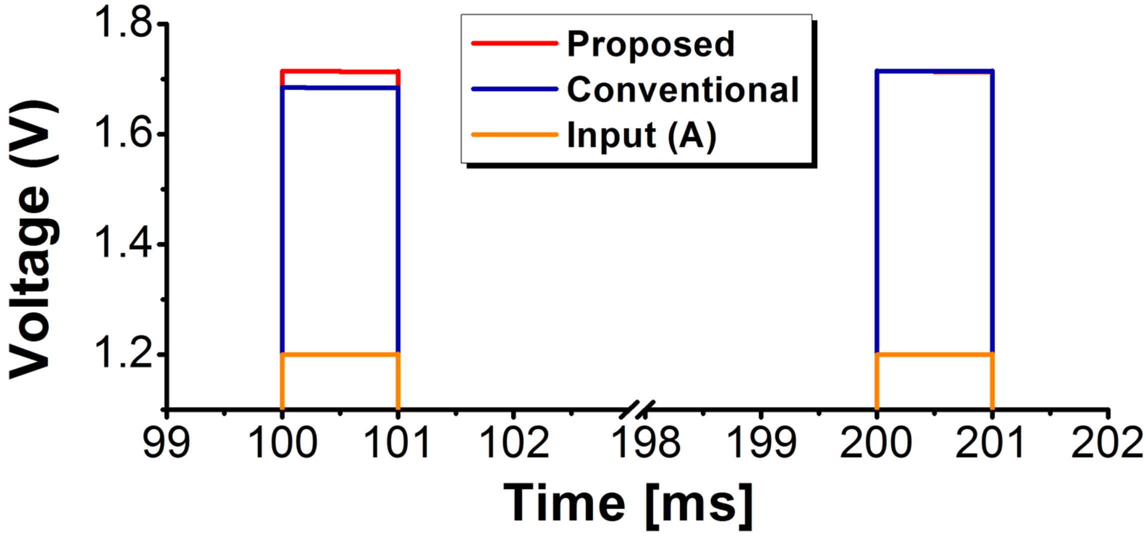


Figure 5.10: Simulation results of the boosted voltage.

can be significant if chip is facing a bright scene. So two separate supply lines are routed inside the pixel array. Figure 5.11 shows the hierarchy of the image sensor's power-gating scheme.

Since image readout may consume up to 1 mA instantaneous current, 100 pF decoupling capacitance is added for each power-gated domain. Dual-release power gates are used to limit the initial surge current when charging the explicit decoupling capacitors. This is required because the PMU can only sustain up to 10s of μA, and the current drawn to charge the 100 pF decoupling capacitor can reach mAs and crash the system if not limited. So when the power gate is released, a small header is turned on first to trickle charge the capacitors, followed by a large header, which ensures minimal IR drop during operation. To reduce leakage power of 0.6 V digital components, N-wells are biased at 1.2 V, reducing PMOS leakage by 60$\times$ in simulation.

Motion detection resolution can be configured to either 10 $\times$ 10 or 5 $\times$ 5 depending on the power requirements. Frame-wise thresholding of motion trigger count is implemented to prevent against false triggers or dead pixels. The location of the motion detecting pixel is also reported, which can be used to determine which portions of the image to store in SRAM. Fig. 5 shows state changes of each layer and Mbus activity for one of the tested usage scenarios of motion-triggered system wakeup and RF transmission.

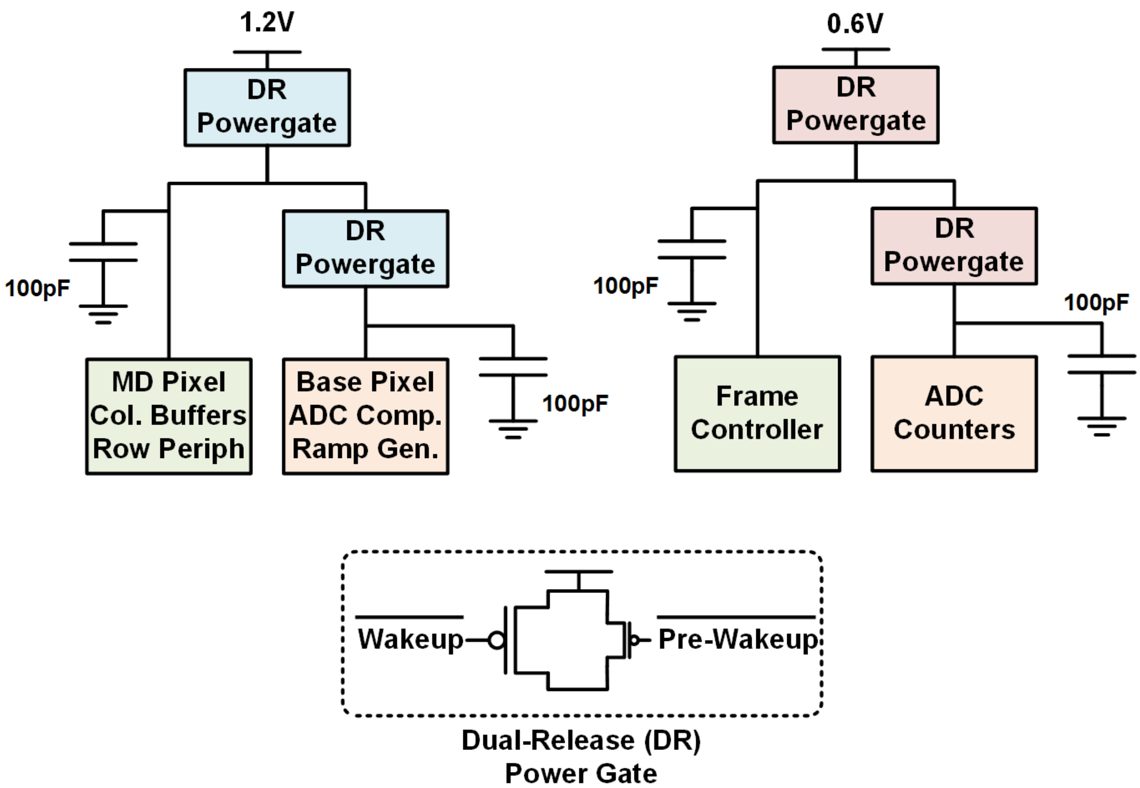


Figure 5.11: Hierarchical power domains within the image sensor block, and schematic of the dual-release power gate.

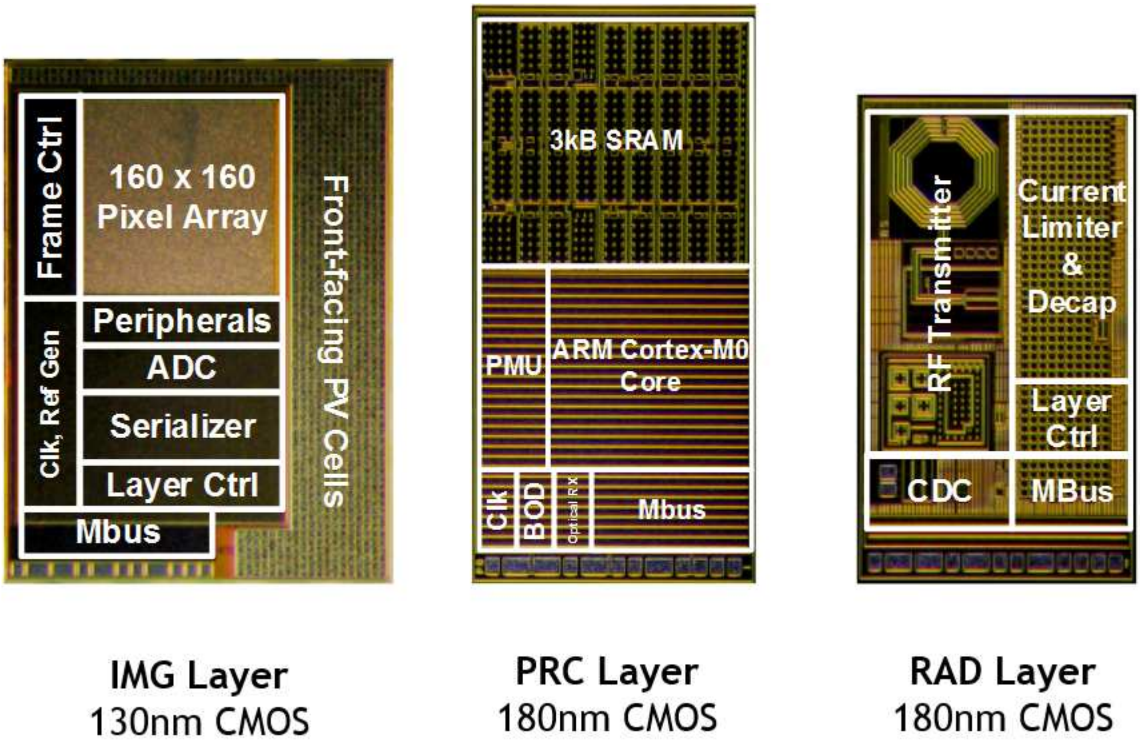


Figure 5.12: Die photographs of the three logic layers used in the proposed system.

5.5 Measurement Results

The imager layer and the photovoltaic cells were fabricated in 130nm CMOS technology, and the rest of the chips were fabricated in 180nm CMOS technology. All the chips used standard logic technologies. Figure 5.15 shows the die photos of the chips used in this project.

5.5.1 Optics

For millimeter-scale optics, a gradient-index rod lens was used. The GRIN lens is typically used for fiber optics, and has a varying index of refraction from the center of the cylinder to the outside (Figure 5.13). With a focal length of 0, it can be placed directly on top of the imager chip and glued with optical UV-curable epoxy (5.14). It measures only 1 mm in diameter and 2.4 mm in height. The small form factor and the optical quality was sufficient for the proposed imaging system.

Another candidate that was considered for optics was ball lens. Ball lens offers smaller form

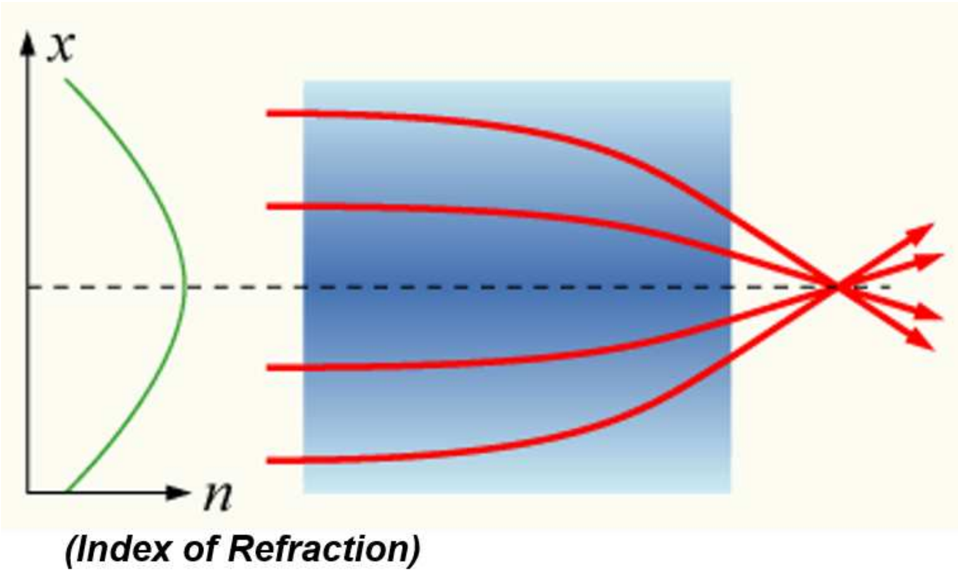


Figure 5.13: GRIN lens characteristics showing its varying index of refraction.

factor than the GRIN lens, but its optical quality is inferior to GRIN lens, with significant distortion towards the edges. In addition, because of the ball shape, mounting is another issue, requiring a much more sophisticated tool to position the lens and hold in place.

5.5.2 Sample Images

Figure 5.15 shows sample images taken by the imager chip with the GRIN lens. The image on the left was taken with real objects, whereas the face of Benjamin Franklin was projected on an LCD screen. The pixel array measures 900 μm on a side, and the lens measures 1 mm in diameter, hence the corners of the image are not covered by the lens. Both of these images were transmitted via Mbus at 1.1 Mhz. The signal-to-noise ratio is 51.7dB in 9-bit ADC mode, which is respectful for a non-CIS (CMOS Image Sensor) process.

5.5.3 System Assembly

The cross-sectional diagram of the overall system (Figure 5.16) shows the 5-layer stack placed inside a glass package with through-glass vias, which provides a connection between the top-facing chips and bottom-facing PV cells. This configuration creates optimal lighting conditions for both imaging and harvesting. Transparent protective epoxy covers the PV cells and bond wires

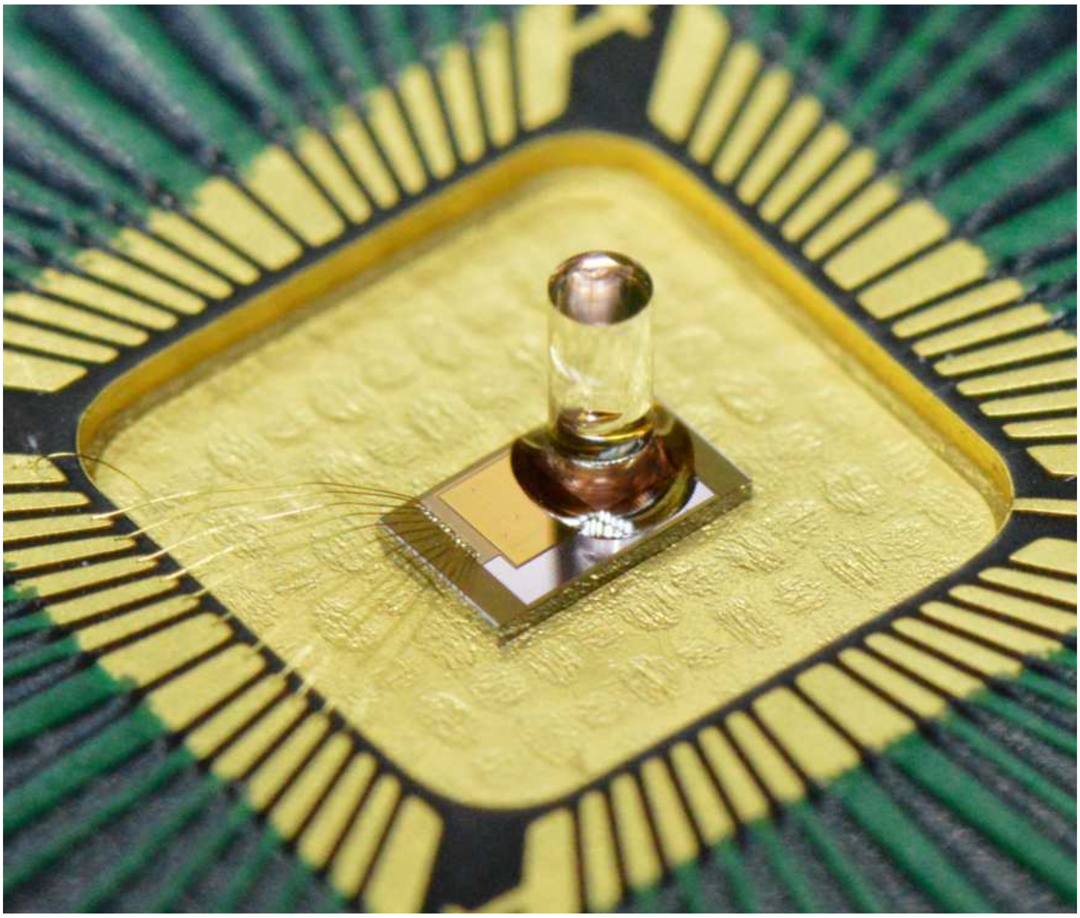


Figure 5.14: GRIN lens glued on chip with optical epoxy.

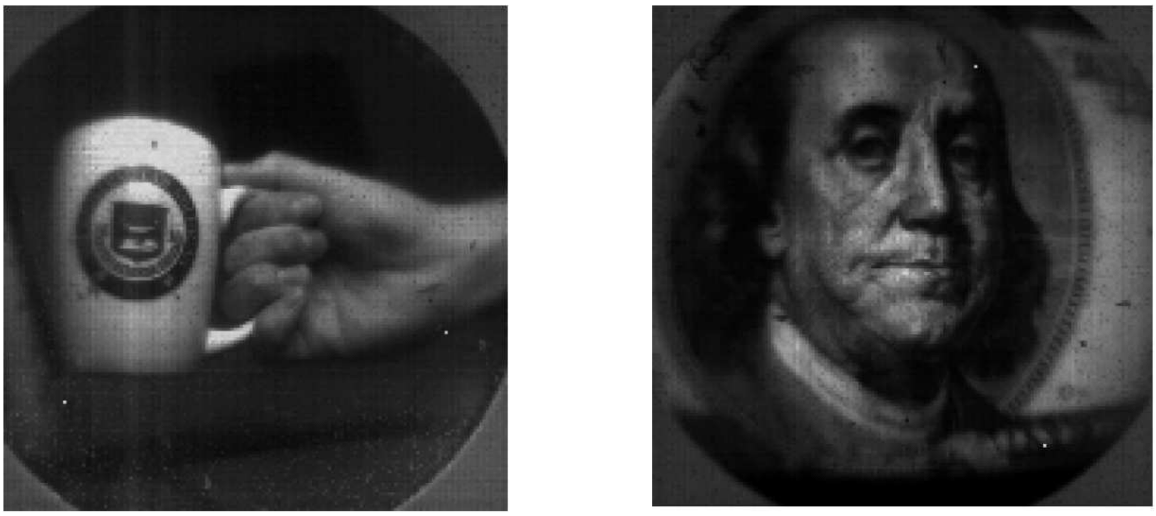


Figure 5.15: Sample 160×160 images transmitted via Mbus.

below the glass package. Since the ultra-low power circuits in the system exhibit high leakage when exposed to strong light, the cavity inside the glass package is filled with dark epoxy to shield non-imaging chips from light and complete the encapsulation.

For system assembly, the solar cells are first attached to the bottom side of a glass package module, wirebonded, and coated with transparent protective epoxy. The battery and remaining IC layers are then stacked and wirebonded on top of the glass package. Next, glass sidewalls are placed, and the cavity is filled with black epoxy to minimize light-induced leakage current. Finally, the lens is mounted with optical epoxy, which is UV-cured. Total of 10 systems with slightly different configurations were assembled for testing purposes. For instance, Figure 5.17 shows a side view of a fully encapsulated system on the left, and the stack shown on the right has the power wires attached to a PCB for power measurement testing.

5.5.4 Wireless Communication

Two-way wireless communication is achieved with optical wakeup receiver and RF transmitter. The optical receiver is an improved version of [44] consumes 695 pW standby power and is used for initial programming of the system or to externally send interrupt commands. With improvements on the front-end design and the clock generator, up to 800 bps data rate is achieved. The RF transmitter in the RAD layer uses an OOK-modulated scheme, with an LC oscillator tuned to the 915 MHz ISM band. The oscillator is turned on for 100 ns to transmit 1 bit and is otherwise power-gated. The transmitter sends data at 4 nJ/bit to an inductive receiver PCB board with -70 dBm of sensitivity positioned 15 mm away. Figure 5.19 shows the system being programmed with an LED through an interface PCB board that generates the encoded light pattern. Figure 5.20 shows the testing setup for RF reception.

5.5.5 Usage Scenario

In an example usage scenario, the proposed system will be running motion detection in its ultra-low power sleep mode, and wake up to perform radio transmission when motion is detected. The timing diagram in Figure 5.21 walks through this sample usage scenario. The clock and data wires of Mbus are shown, along with the status of each logic layers. Initially, the system is in sleep mode

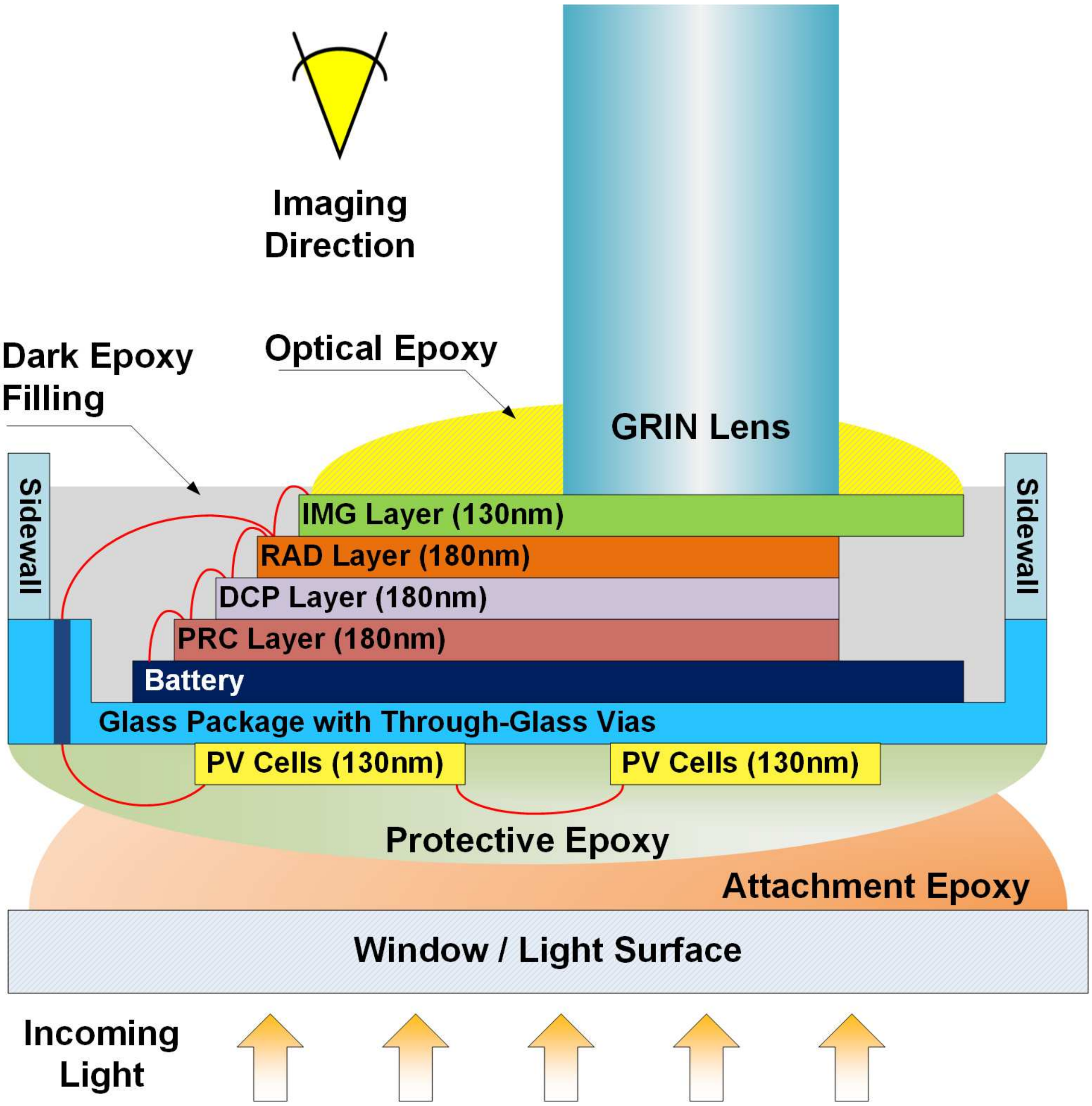


Figure 5.16: Cross-sectional view of the proposed visual monitoring wireless sensor node.

Figure 5.17: Side view of a fully encapsulated system.

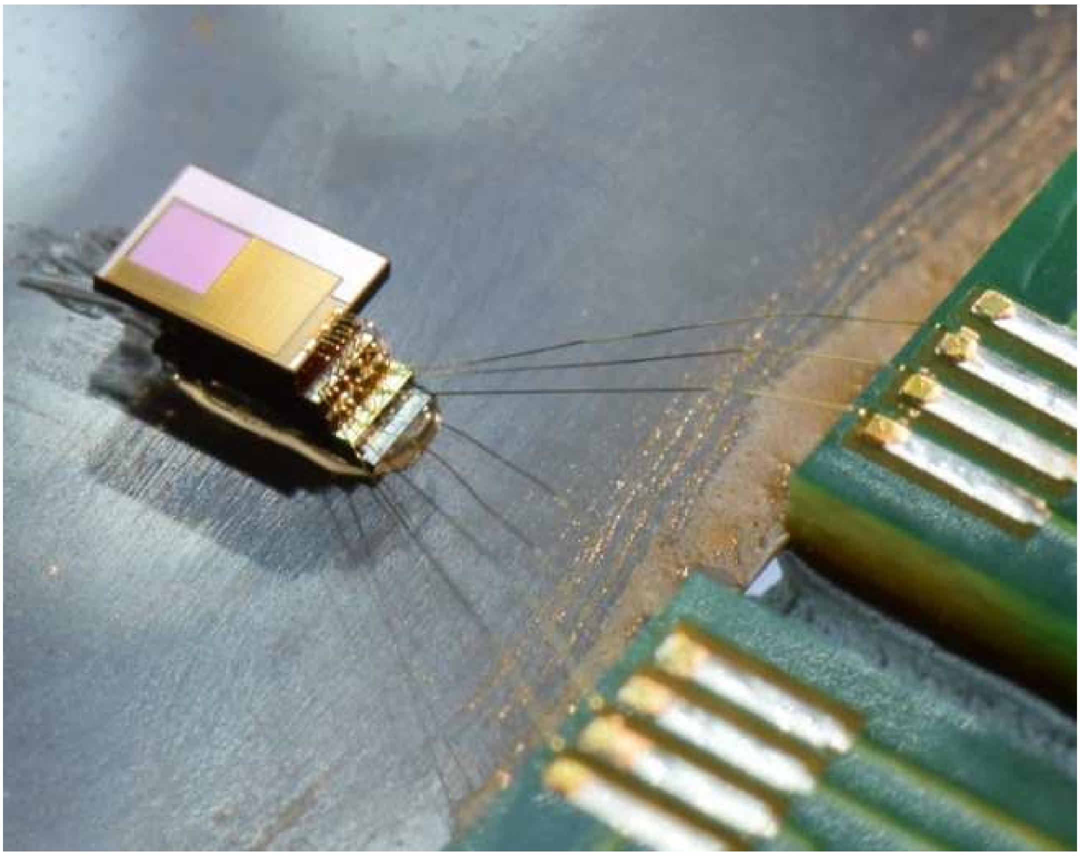


Figure 5.18: Power measurement testing setup.

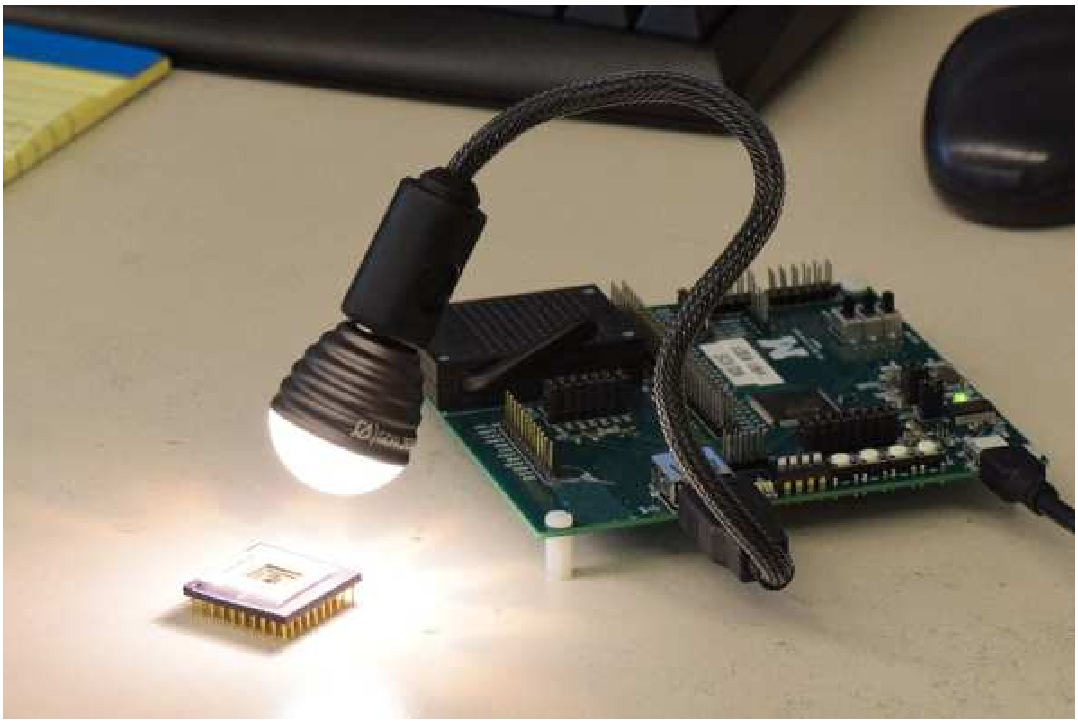


Figure 5.19: Proposed system being programmed via light.

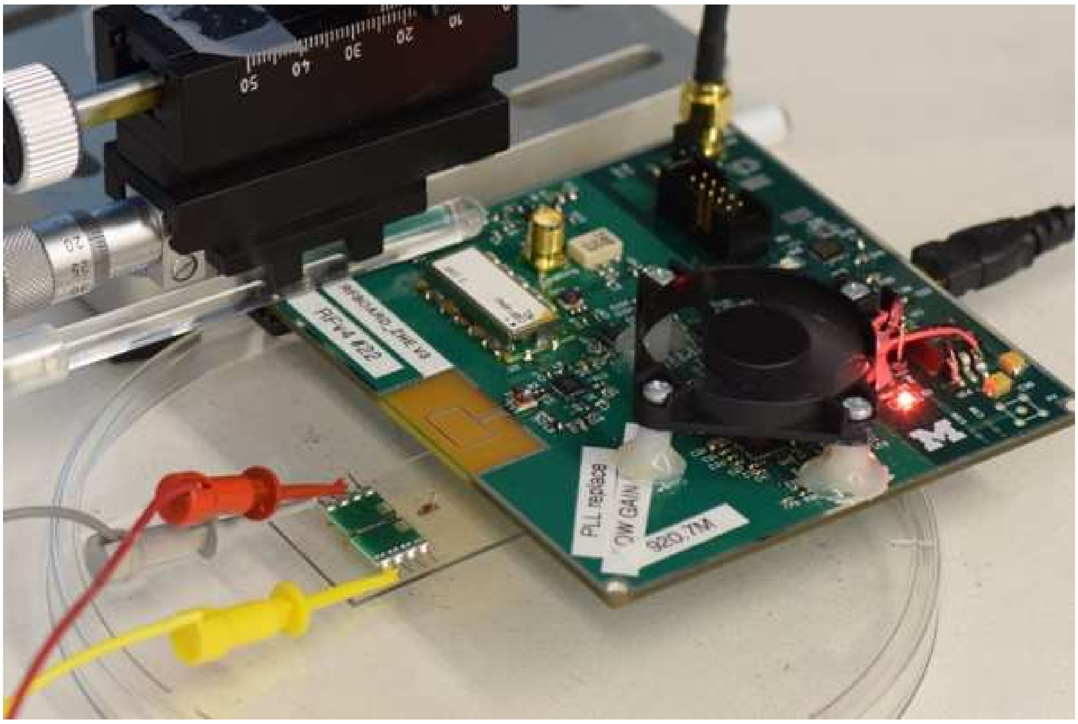


Figure 5.20: RF reception testing setup.

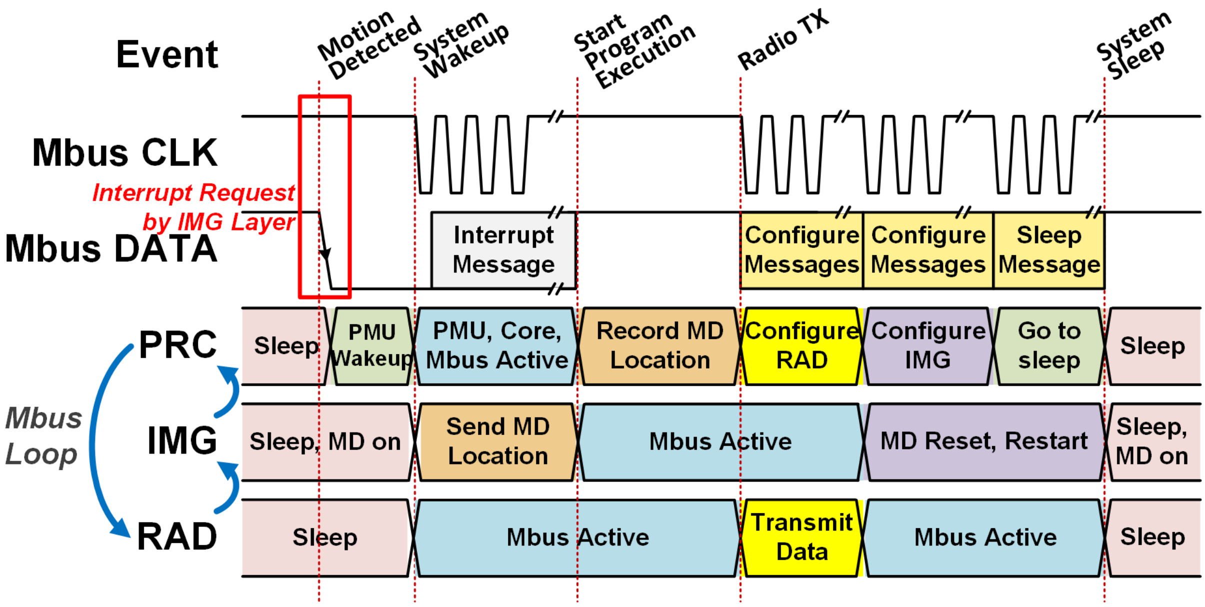


Figure 5.21: Example usage scenario of the proposed system.

with motion detection turned on. When motion is detected, the image sensor sends an interrupt signal to the IMG layer's Mbus interrupt controller, which pulls down the data wire to start Mbus interrupt routine. This pattern is recognized by the PRC layer's mbus sleep controller, which in turn switches the PMU to active mode to support subsequent Mbus activity. The PRC layer starts to generate the Mbus clock as the mediator node, and this wakes up all the Mbus controllers in each layer. With the incoming clock, the IMG layer sends the interrupt message, which contains information about the detected motion, such as the location within the pixel array, and the direction of motion. The CPU in the processor layer is woken up by this interrupt message, and starts to run the program stored in the retentive SRAM. If the program specifies radio transmission to an end user, the CPU sends Mbus messages to configure the radio layer and transmits data through the RF transmitter. At the end of the program, the system goes back to sleep.

5.5.6 System Power Consumption

Figure 5.22 shows measured current consumption out of the battery versus time in a usage scenario described in the previous section. The initial jump in current consumption corresponds to the system waking up after motion is detected, followed by radio transmission, and some processing. At the end of the program execution, the system enters sleep again.

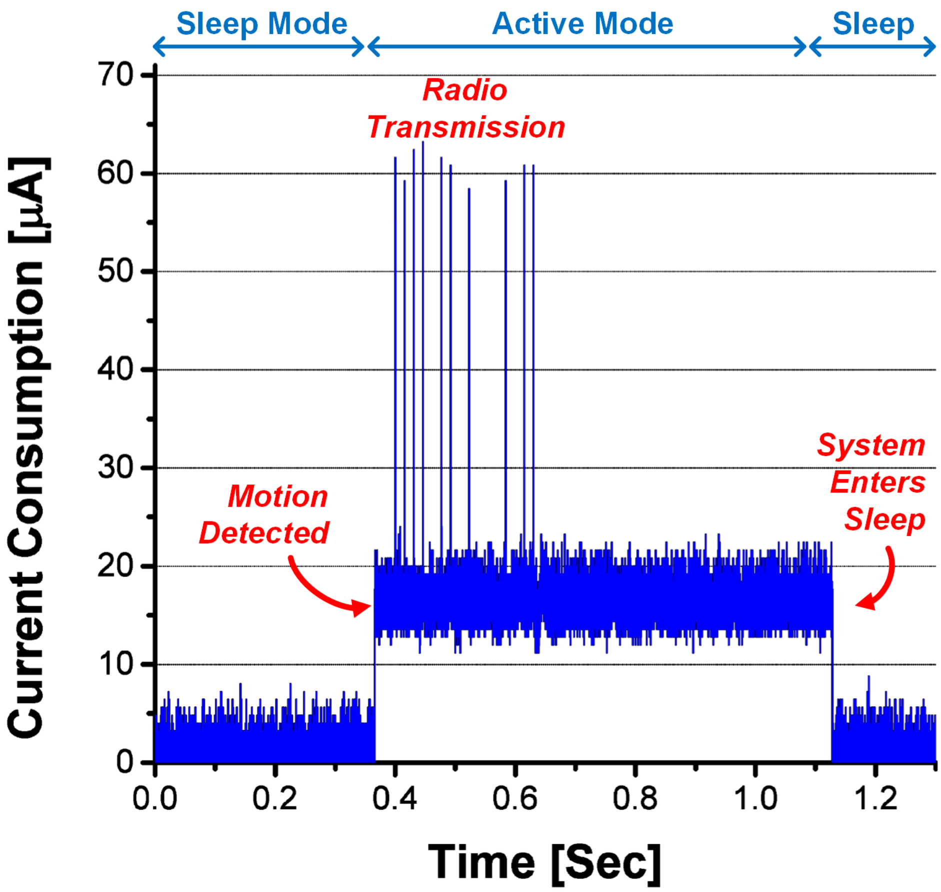


Figure 5.22: Measured current drawn from the battery vs. time of the proposed system.

The overall system standby power is 8 nW when it is in sleep mode, and with motion detection on, it consumes 304 nW from the 4 V battery. With the 5.7 μAh thin-film battery, the system can survive up to 60 days in sleep mode or perform continuous motion detection for 3.4 days without any harvesting. The battery was measured to be charged at 456 nW with 10 klux lighting, which is a typical daytime condition on a window or at the surface of an indoor light source. These power numbers indicate that the proposed system can perform continuous motion detection without losing net energy.

5.5.7 Comparison to Prior Art

Table 5.2 compares the proposed system to prior art. Compared to previously reported millimeter-scale wireless sensor nodes such as the IOP sensor [16] and M^3 [17], the proposed work is the first to include optics and two-way wireless communication to achieve complete visual sensing capability. Compared to other miniaturized cameras such as the eCAM [52] and INCA [53], the proposed system achieved orders of magnitude smaller volume at 32 cubic millimeters. eCAM is a centimeter-scale wireless sensor node with imaging capability but its lifetime is limited to 240 days without harvesting, and INCA is a miniaturized commercial-level camera for wired applications.

5.6 Conclusion and Future Directions

In this chapter, a complete visual sensing system in a nearly invisible millimeter-scale form factor was presented. The system features a 160 $\times$ 160 resolution image sensor with built-in motion detection, along with processor, memory, power management, two-way communication, optics, and encapsulation. The ultra-low power motion detection mode and energy harvesting using solar cells allows perpetual lifetime at 10 klux lighting condition. The sensor is designed to be placed at the surface of an indoor light source or on a window

As future work, a layer dedicated to storage can be added to the stack to store multiple full-frame images. Flash or embedded DRAM may be used for area density, but key challenges are the power requirements for writing and refreshing operations, respectively. Also, an RF transmitter capable of achieving longer distance should be considered for more practical applications.

Categories	Wireless Sensor Nodes		This Work	Miniaturized Cameras	
	IOP	M^3		eCAM	INCA
Imaging	N/A	9,216 Pixels	**25,600 Pixels w/ Motion Detection**	0.3 MPixels	2 MPixels
Optics	N/A	N/A	**GRIN Rod Lens**	Pinhole Lens	Regular Lens
Wireless	RF Transceiver	Optical Receiver	**Optical Receiver RF Transmitter**	2.4GHz Transceiver	LTE Module Optional
Processor	ARM Cortex M0	ARM Cortex M0	**ARM Cortex M0**	Nordic 8051	TI OMAP 4
Storage	0.5kB SRAM	3kB SRAM	**3kB SRAM**	4kB SRAM	Unknown
Battery Capacity	1μAh Thin-Film	1μAh Thin-Film	**5.7μAh Thin-Film**	170mAh Li-Poly	No Battery
Standby Power	3.7nW	11nW	**15nW idle, 304nW with MD**	>100μW	4W
Energy Harvesting	Solar, $0.07mm^2$	Solar, $0.54mm^2$	**Solar, $2.5mm^2$**	N/A	N/A
System Lifetime	Perpetual	Perpetual	**Perpetual**	<240days	Wired
Dimensions (Volume)	$0.5 \times 1.5 \times 2$ mm^3 (1.5 mm^3)	1 x 2.2 x 0.4 mm^3 (0.9 mm^3)	**2 x 4 x 4 mm^3** (32 mm^3)	23 x 32 x 18 mm^3 (13,248 mm^3)	20 x 20 x 80 mm^3 (32,000 mm^3)

Table 5.2: Comparison table to previously reported millimeter-scale wireless sensor nodes and miniaturized cameras.

CHAPTER 6

Conclusion

6.1 Summary

Technological advances in semiconductor industry and integrated circuits have resulted in electronic devices that are smaller and cheaper than ever, and yet they are more pervasive and powerful than what could hardly be imagined several decades ago. Nowadays, small hand-held devices such as smartphones have completely reshaped the way people communicate, share information, and entertain. According to Bell's Law, this trend of cheaper and smaller computers will continue, and the next generation of computing will be cubic-millimeter-scale in volume and will be much more prevalent than smartphones are today, opening up myriad of new applications.

In this dissertation, a millimeter-scale wireless sensor node for visual sensing applications was proposed, with emphasis on the optical interface circuits that enable wireless optical communication and visual monitoring. Visual monitoring and imaging with CMOS image sensors opens up a variety of new applications for wireless sensor nodes, ranging from surveillance to *in vivo* molecular imaging. In particular, the ability to detect motion can enable more intelligent power management through on-demand duty cycling and reduced data retention requirement. The proposed wireless sensor node is a nearly-invisible, yet a complete system with imaging, optics, wireless communication, CPU, memory, battery and energy harvesting. Such complete features in the unprecedented form factor can revolutionize the role of electronics in our daily lives, taking the "Smart Dust" concept from fiction to reality.

In Chapter 2, an ultra-low standby power optical wake-up receiver with a novel front-end circuit and communication scheme was proposed. The optical receiver provide the means for initially programming, synchronizing, or externally interrupting the wireless sensor node, since wired connection may not be practical. Named "FLOW" for Free-space Low-Power Optical Wake-up, the receiver was consumes 695 pW in standby mode, which is $6000\times$ lower than previously reported RF and ultrasound wake-up radios. This extremely low standby power makes this receiver attractive for battery-limited mm^3-scale sensor nodes. During active mode the receiver consumes 140 pJ/bit at up to 91 bps. A pulse width modulated communication encoding scheme is used, and chip-ID masking enables selective programming and synchronization of multiple sensor nodes. The design was implemented in 180 nm CMOS technology.

In Chapter 3, a 128×128 CMOS image sensor with ultra-low power in-pixel motion detection was proposed. Aggressive power gating and clock gating schemes are used to minimize the power consumption both during imaging and motion detection nmode. Furthermore, by implementing motion detection inside the pixel array in the analog domain, we avoid the need to use the ADC, achieving a significant power savings. Also, spatial aggregation of pixels and temporal averaging are implemented to minimize blindspots and increase sensitivity to slow motion. A test chip was fabricated in 130 nm CMOS technology and consumes 467 nW while performing motion detection, marking two orders of magnitude reduction over prior art, thereby bringing continuous motion detection within the realm of millimeter-scale wireless sensor nodes. Full-frame still images with 38.5 dB dynamic range are captured at 6.4 fps while consuming 16 μW.

In Chapter 4, the harvesting aspect of the envisioned sensor node was discussed, via an experiment with microbial fuel cells (MFC). MFCs generate voltages of around 500 mV, which is A test chip was designed to include ARM Cortex-M0 CPU, 3 kB of SRAM memory, optical wakeup receiver and power management/harvesting unit. The chip as a whole consumes 11 nW in sleep mode. A small-scale micro-MFC with 21.3 cm^2 anode surface area is able to generate 5.4 μW of power at 700 mV, more than enough to power the chip in a duty-cycled usage. A 49.3-hour long-term experiment was performed with the micro-MFC connected to the chip's harvesting unit, demonstrating the sustainability of the sensor node with energy harvesting.

In Chapter 5, a complete millimeter-scale wireless imaging system was described as the end result of this research. The proposed system is a complete wireless sensor node, including optics, battery, energy harvesting, imaging, motion detection, and two-way wireless communication. An improved version of the image sensor discussed in Chapter 3 is designed to achieve even lower motion detection power consumption and more configurable thresholding, while increasing the imaging resolution to 160 $\times$ 160. The optical wake-up receiver described in Chapter 2 is included with improvements in faster data rate, reaching as high as 800 bps. During the assembly process, the solar cells are placed facing the opposite direction of the image sensor for energy harvesting. This way, the light is illuminating both the solar cells and the target scene of the image sensor, creating an optimal environment for both imaging and harvesting. For optics, gradient-index (GRIN) rod lens is used for focusing, measuring 1 mm in diameter and 2.4 mm in height. The proposed system was successfully assembled with high yield and demonstrated on-demand operation with motion-triggered wake-up. With the bottom-facing solar cells, the system can harvest enough energy from 10 klux light source to sustain perpetual motion detection operation.

6.2 Future Works

As future work, there are several improvements that can be made to the millimeter-scale imaging system discussed in Chapter 5. First, the image storage can be improved from the current 3 kB SRAM, which cannot hold a full 160 $\times$ 160 image. A dedicated layer for data storage using non-volatile memory such as flash can be used to store multiple frames of images. Secondly, the optical receiver can be augmented with an infrared-sensitive frontend to help skin penetration for use in medical implants. This will also ease the line-of-sight constraints posed by visible light communication, making the optical receiver more attractive for many practical applications. Lastly, more diversified sources of harvesting should be explored, such as infrared-sensitive photovoltaic cells or inductive wireless charging. All of these improvements are feasible within the millimeter-scale form factor, and will significantly enhance the usability of the proposed system.

6.3 Concluding Remarks

The research described in this dissertation shows a glimpse of what the future miniaturized computers may look like, and the technology that will enable such devices. In the near future, very small computers - perhaps too small to be easily visible - will surround our daily lives, on the premise that they will provide substantial benefit and convenience to the human society. With the technology aside, however, there is still a lot of uncertainty as to how exactly these small computers will be used, as well as some open ethical discussions as to what extent should their capability be allowed. Undoubtedly, there is a plenty of benefits from using these nearly invisible computers to augment the natural senses and intelligence of humans, but there are also foreseeable security and privacy risks associated with distributing such small devices in mass volume. Hence the commercial development of such small and powerful devices should be accompanied by proper rules and regulations to prevent unnecessary outcomes from this remarkable technological achievement.

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