Millimeter-scale RF Integrated Circuits and Antennas for Energy-efficient Wireless Sensor Nodes

by

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To My Family

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Abstract

Recently there has been increased demand for a millimeter-scale wireless sensor node for applications such as biomedical devices, defense, and surveillance. This form-factor is driven by a desire to be vanishingly small, injectable through a needle, or implantable through a minimally-invasive surgical procedure. Wireless communication is a necessity, but there are several challenges at the millimeter-scale wireless sensor node. One of the main challenges is external components like crystal reference and antenna become the bottleneck of realizing the mm-scale wireless sensor node device. A second challenge is power consumption of the electronics. At mm-scale, the micro-battery has limited capacity and small peak current. Moreover, the RF front-end circuits that operates at the highest frequency in the system will consume most of the power from the battery. Finally, as node volume reduces, there is a challenge of integrating the entire system together, in particular for the RF performance, because all components, including the battery and ICs, need to be placed in close proximity of the antenna.

This research explores ways to implement low-power integrated circuits in an energy-constrained and volume constrained application. Three different prototypes are mainly conducted in the proposal. The first is a fully-encapsulated, autonomous, complete wireless sensor node with UWB transmitter in 10.6mm^3 volume. It is the first time to demonstrate a full and stand-alone wireless sensing functionality with such a tiny integrated system. The second prototype is a low power GPS front-end receiver that supports burst-mode. A double super-heterodyne topology enables the reception of the three public GPS bands, L1, L2 and L5 simultaneously. The third prototype is an integrated rectangular slot loop antenna in a standard 0.13-μm BiCMOS

technology. The antenna is efficiently designed to cover the bandwidth at 60 GHz band and easily satisfy the metal density rules and can be integrated with other circuitry in a standard process.

Chapter 1 Introduction

1.1 The Evolution of Computer Classes

1.1.1 The Limits of Moore's Law

According to Moore's law, the number of transistors on an integrated circuit (IC) doubles every 18-24 months [1]. Since the 1960s, the continual improvement in IC semiconductor manufacturing has led the density evolution of the transistor. Integrating more and more transistors onto a single IC has resulted in miniaturized computing devices that are low cost, achieve high data rates, with a shrinking form factor.

However, smaller transistors are becoming increasingly more difficult to make, and manufacturing at a constant cost per unit area is a result of a concerted engineering effort to make it so. Considerable effort is devoted to the continuation of Moore's Law because there is a strong

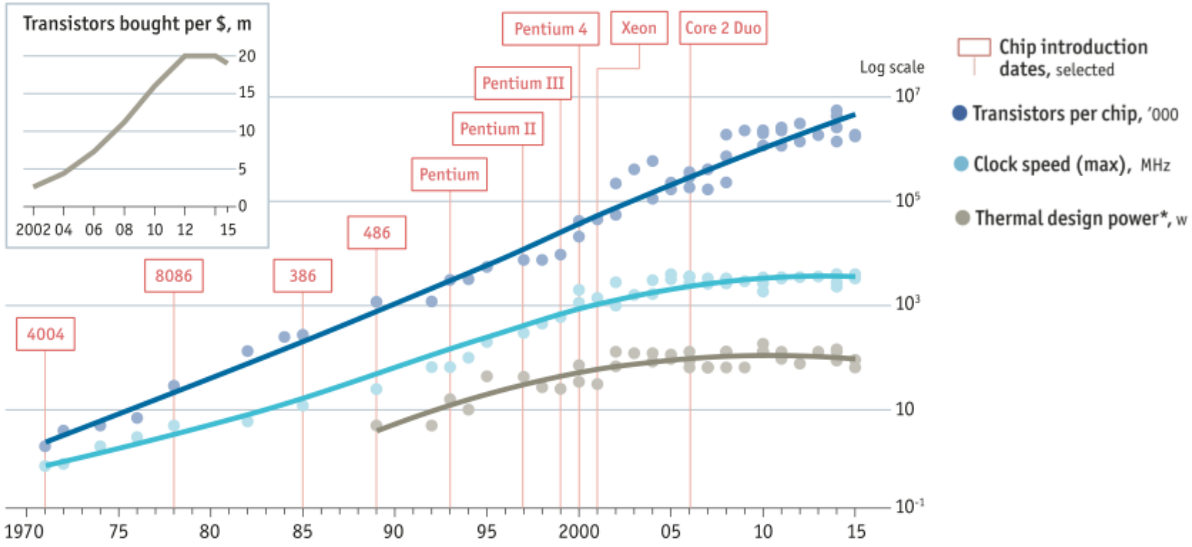


Figure 1.1. Stuttering of transistors per chip, clock speed and thermal design power [3]

economic incentive to do so [2]. However, as shown in Figure 1.1, the number of transistors bought per dollar had saturated from 2012 to 2014, and decreased since 2015. Because the average area per transistor declined at a slower rate than the processing costs per area has increased, the net transistor cost is increasing.

Furthermore, as the power density in ICs increases, the thermal design power and maximum clock speed becomes an issues. The maximum safe power limit prevents the increasing numbers of smaller cores squeezed into a multicore chip, all operating at their optimal clock speed. The result is multicore chips need to turn off power to unused circuitry and reduce the clock speed to remain within the safe power limits. For some time, making transistors smaller has no longer been making them more energy-efficient; as a result, the operating speed of high-end computing has been on a plateau since the mid-2000s [3]. While the benefits of making transistors smaller have been decreasing, this has presented an opportunity to improve performance in other layers of the computing stack.

1.1.2 The Advent of a New Class of Computer

Bell's Law described approximately every decade a new computer class forms as a new "minimal" computer either through using fewer components or use of a small fractional part of the state-of-the-art chips. A class may be the consequence and combination of a new platform with a new programming environment, a new network, and new interface with people and/or other information processing systems, where each successive class has had a 100x reduction in physical volume [1], [4].

The continual scaling of the size of computing systems has resulted in a diverse range of computing platforms. In Figure. 1.2, following the advent of personal computers in 1980s and wireless portable devices such as laptops and smartphones in 1990s and 2000s, wireless sensor

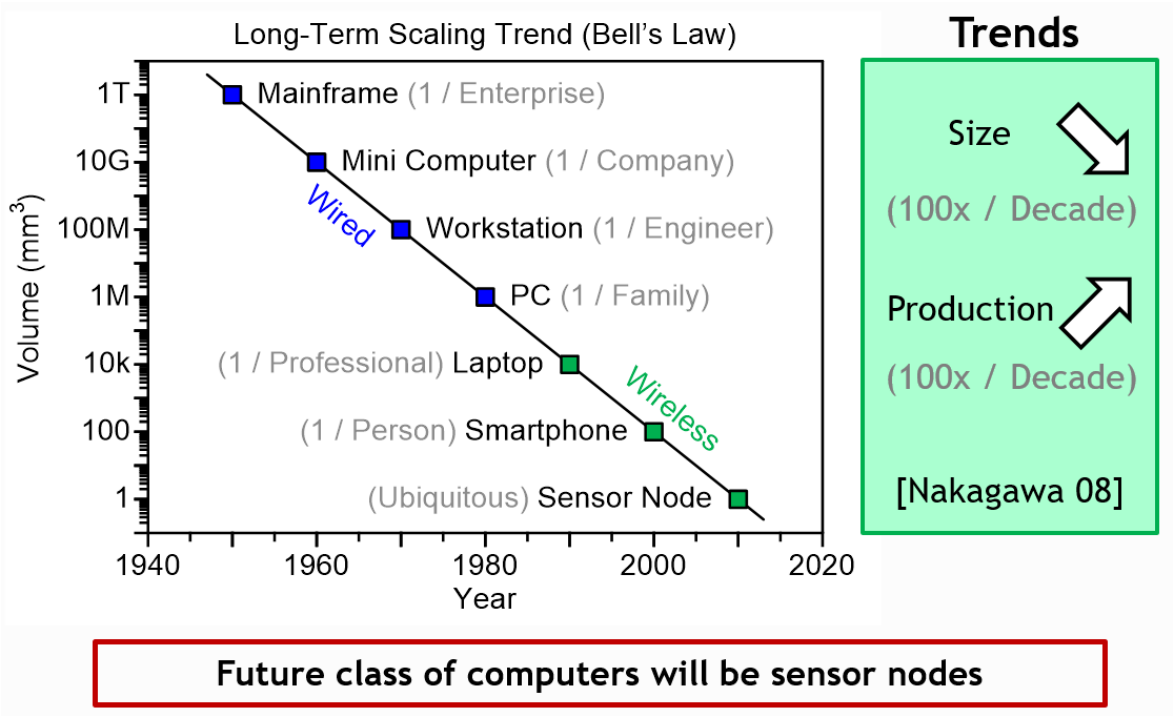


Figure 1.2. Long-Term scaling trend of computing devices over years

networks (WSNs) take center stage as the next trend of computing devices toward more compact, lower cost, more ubiquitous computing [5]. Ubiquitous sensing was projected to reach volumes of 100 sensors per person by 2017, and is currently on a path to reach 10s of Billions of devices in the early 2020s. With this trends in Bell's law, the next computer class is projected to be even smaller and more pervasive, which is the class of cubic-mm-scale devices.

In the face of the slowing of fundamental scaling, we can expect significant change and more diverse options in the underlying process technology, upward to the circuit, system, and applications software levels. This dynamic will increase the value of co-optimization for emerging applications. Combining the platform, wireless network, and interface into one to integrate with other systems is clearly a new class that are offering wireless deployments, and hence reduced cost for existing applications, such as process, building, home automation, and control. New applications will be needed for wireless sensor networks to become a true class. If, for example,

these chips become part of everything that needs to communicate in the whole IT hierarchy, a class will be established.

The new class of wireless sensor networks could record the state of a person or object (things such as scales, appliances, switches, thermometers, and thermostats) including its location and physical characteristics with communication to e.g. WiFi or some other infrastructure network for reporting. The Internet of Things (IoT) is a part of this potential for very large class of trillions of devices. Just as billions of clients needed millions of servers, a trillion dust-sized wireless sensing devices will be coupled to a billion other computers [1].

1.2 Wireless Sensor Networks

In recent years the efficient design of a wireless sensor network has become a leading area of research. A wireless sensor network can be defined as a network of devices that can communicate

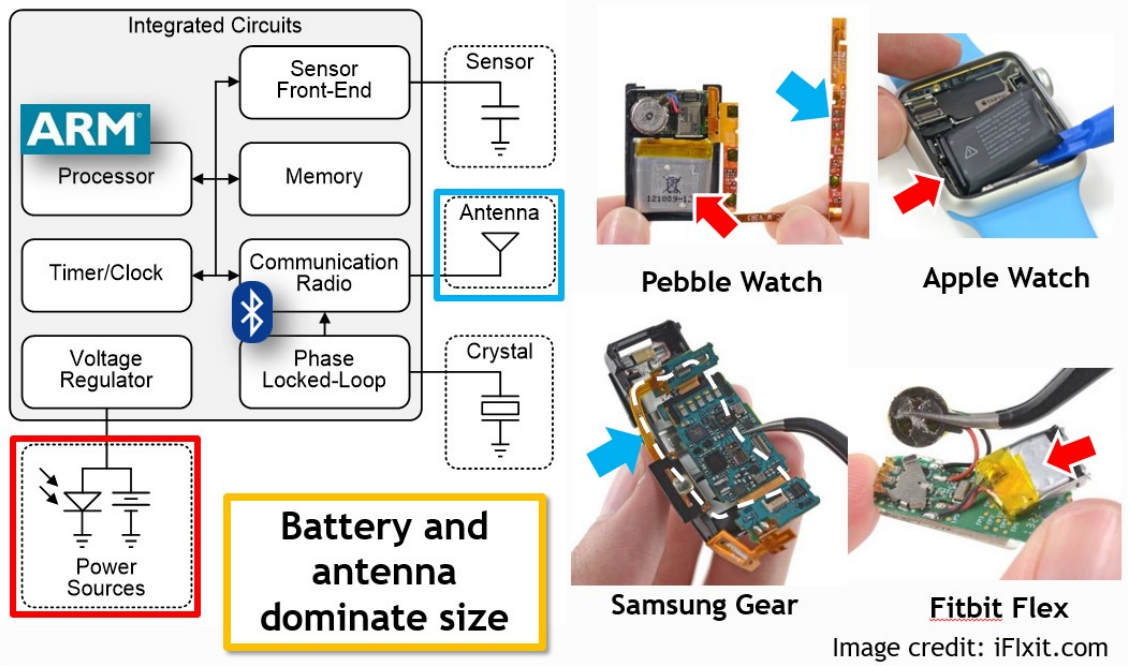


Figure 1.3. Anatomy of a wireless sensor node

the information gathered from a monitored field through wireless links. The data is forwarded through multiple nodes, and with a gateway, the data is connected to other networks like wireless Ethernet [6]. A wireless sensor network consists of base stations and numbers of wireless sensor nodes (WSNs). These networks are used to monitor physical or environmental conditions like sound, pressure, temperature and co-operatively pass data through the network to a main location [7].

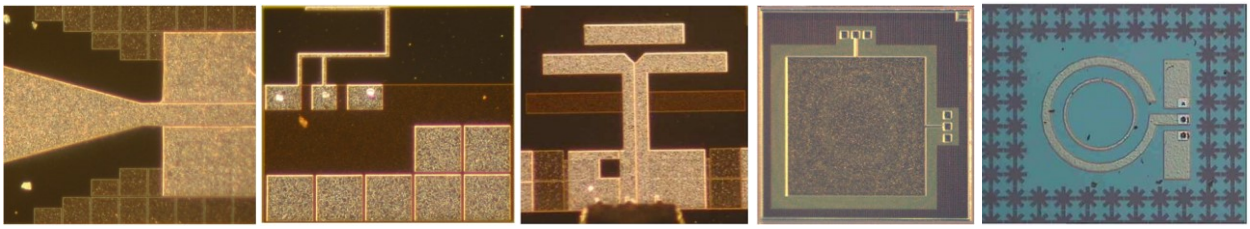
Today's wireless sensors are composed of multiple components such as microcontroller, power management, sensor, transceiver, timer/clock, battery, and antenna. These components tend to be commercial off-the-shelf (COTS) components, which could be bought individually then put together on a printed circuit board in Figure 1.3. It has a great advantage that could afford a designer flexibility, but doesn't look like the new class of computer in future sensor nodes. In most of these applications, the bulky battery takes a significant fraction of the total volume and the antenna for the radio sticks out several centimeters. The result is this system increases up to centimeters or tens of centimeters in at least one dimension. Due to these problems, the integration of battery and antenna are two major issues for realizing integrated cubic mm-scale wireless sensor nodes.

1.3 Antenna-on-Chip (AoC)

Recently, the wireless communications community has become increasingly interested in the unlicensed 60-GHz band where there is 9GHz of unlicensed spectrum available. The IEEE 802.15.3c Wireless personal area networks (WPANs) standard, which requires high data-rate and low-cost chipsets for wireless short-range communications, has been advancing technologies in this frequency band since 2003 [8]. The scaling down of transistors pushes up the high-frequency

Type of Antenna	Technology	Frequency	Antenna Gain	Antenna area	Chip area
Monopole [9]	0.13um CMOS	60 GHz	-9.4 dBi	0.81 mm^2	0.81 mm^2
Invert-F [10]	0.18um CMOS	60 GHz	-15.7 dBi	0.57 mm^2	0.57 mm^2
Yagi [11]	0.18um CMOS	60 GHz	-10.6 dBi	1.05 mm^2	1.05 mm^2
Patch [12]	0.13um CMOS	60 GHz	-3.32 dBi	1.92 mm^2	5.06 mm^2
Loop with AMC [13]	0.18um CMOS	65 GHz	-4.4 dBi	0.627 mm^2	3.24 mm^2

Table 1.1. Comparison table of the state-of-the-art integrated antennas



[7] [8] [9] [10] [11]

Figure 1.4. Die photos of the state-of-the-art AoC

capability of the active devices in a complementary metal oxide semiconductor (CMOS) technology, which has made supporting the 60-GHz band in CMOS possible.

However, the implementation of Antenna-on-Chip (AoC) has been challenging because the antenna structure should be a reasonable size compared to the wavelength of the RF field and can be integrated with the circuitry. Reducing the size below the natural resonant length could cause low efficiency. At high frequencies around 60 GHz, the electrical wavelength is on the mm-scale which allows the integration of the antenna on the chip. Although the size is amenable to implementing the AoC in a standard CMOS process, there are still many issues to consider in CMOS manufacturing such as routing, density rule, keep-out areas, coupling with the actives.

In recent research, several state-of-the-art CMOS integrated antennas have been proposed to meet the demand of WPANs in 60-GHz band [9]-[13]. While most antennas perform poor radiation efficiency because of the limited area, low resistivity and high permittivity of lossy silicon substrate used for CMOS technology, the removal of all connections between RF circuits and the antenna offers substantial cost reduction and flexibility in circuit design for low-cost consumer electronics, especially at millimeter-wave frequencies. Table 1.1 shows a comparison table for the state-of-the-art antennas 60GHz CMOS antennas. In Figure 1.4, the die micrograph of the state-of-the-art AoC is shown.

1.4 Frequency References

1.4.1 Timing Devices

A timing device generates a reference signal that oscillates at a constant frequency. They mainly consist of a resonating element providing an oscillating output with a specific frequency. Their ability to maintain a determined frequency in a specified period of time is the most important parameter limiting their implementation [14]. It provides the timing cues to synchronize with the

Type of OSC	Frequency	Stability	Power	Area
Quartz-crystal OSC [15]	52 MHz	5 ppm	6 mW	5.0 mm^2
Ceramic OSC [16]	30-280 MHz	50 ppm	40 mW	35 mm^2
MEMS OSC [17]	1-150 MHz	50 ppm	9 mW	5.0 mm^2
SAW based OSC [18]	315-1000 MHz	150 ppm	66 mW	37.5 mm^2

Table 1.2. Comparison table of the state-of-the-art timing devices

peripheral controller. As a resonate device, a quartz-crystal and a ceramic are well-known as mechanical resonators. RC and LC oscillation circuits are also used to produce electrical resonance. The mechanical resonator has higher stability of the oscillation frequency because it is rarely affected by external circuits or by perturbation of the supply, but it is incompatible with CMOS processes, meaning the resonator is implemented as a separate device. As its dimension shrinks to the microscale, most mechanical resonators exhibit nonlinearities that considerably degrade the frequency stability of the oscillator. On the other hand, the electrical resonator can be used in monolithic integration in a CMOS process, but the RC and LC resonator in CMOS has relatively Low-Q which could lead instability and frequency offset.

For many wireless sensor network applications, maintaining accurate time information is crucial. This requires an accurate timing references. For the wireless sensor nodes (~ cm-scale) in the public bands below the 60-GHz band, the mechanical resonators such as a quartz-crystal [15], ceramic [16], MEMS [17] or saw-filter [18] have been used widely. However, when it comes to mm-scale wireless sensor nodes (WSNs), the dimension of the timing devices does not relatively small compared to the integrated antenna and micro-battery. The mechanical OSC also requires high power consumption and cannot be integrated in a standard CMOS technology. The performance comparison table of the state-of-the-art timing devices is shown in Table 1.2.

1.4.2 Q Factor of Integrated Passive Devices (IPDs)

For mm-scale WSNs, designing integrated passive devices (IPDs) such as an LC resonator in CMOS is plausible, but the Q factor of IPDs is limited, which impacts the stability resonance frequency. For instance, the Q factor of the integrated spiral inductor (150pH) and MIM capacitor (180fF) in 130nm BiCMOS technology is presented in Figure 1.5. The size of the components has chosen to have a resonance frequency at 30 GHz.

At low frequency, the capacitor has very high Q factor, but, due to the poor Q factor from the inductor, the combined Q factor of this LC resonator is mostly dominated by the inductor. The metal turns of a spiral inductor experience significant loss mechanism; skin effect loss and magnetic field induced proximity effect loss. On the other hand, at high frequency (above ~ 10 GHz), the Q factor of the capacitor got degraded exponentially and even got worse than the inductor when it comes closer to its self-resonance frequency. Due to this characteristic of IPDs, the Q factor of the LC resonator is degraded in one way or another and the optimal combined Q

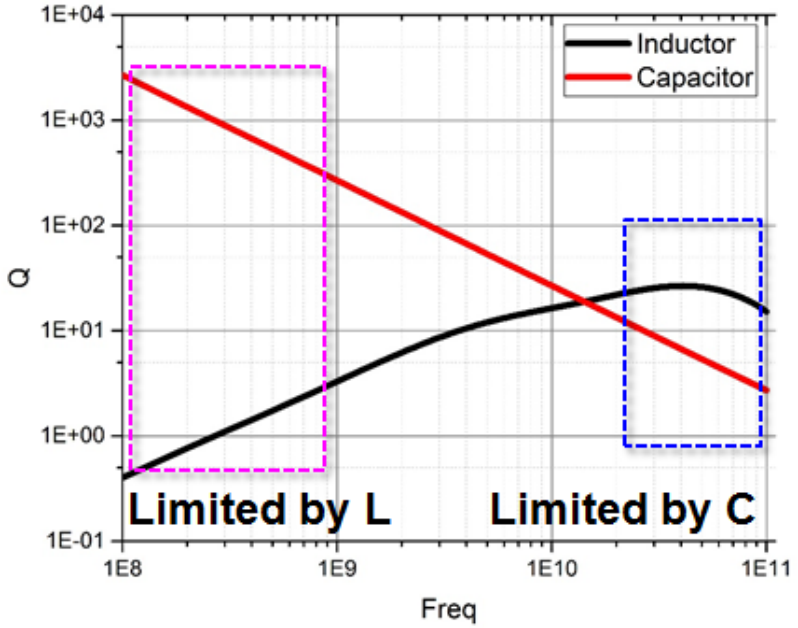


Figure 1.5. Simulated Q vs Freq of the integrated inductor and capacitor

factor would be around 20-30 above 10 GHz. Moreover, the MIM capacitor is built between the thin layers of the metal and it has relatively large tolerance (± 10%) of area capacitance which is not suitable to use as a frequency reference.

1.5 Micro-batteries

Advances in ICs and low-power circuits have reduced the power consumption of WSNs to well below 1mW [19]. One of the main challenges of powering WSNs is a battery that is meant to last the entire life of the device. This is particularly a problem for mm-scale devices, that take advantage of micro-batteries that fit in this form-factor. The maximum current output of a battery depends on the surface area of the electrodes [20]. When reducing the size of micro-batteries, it limits maximum output power due to the surface area limitations of micro-scale device. For instances, as shown in Figure 1.6, the maximum current output of a 5µAh thin-film Li battery from Cymbet is 20 - 30µW at 3.8V, which cannot directly support wireless transmission [21]. To prevent

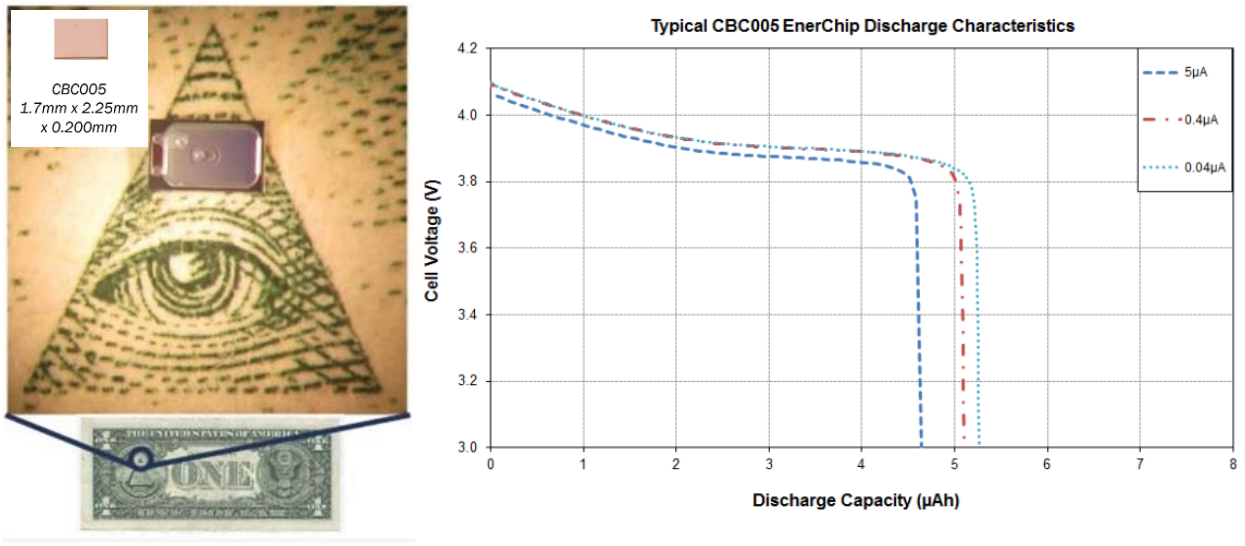


Figure 1.6. The cymbet EnerChipTM bare die and discharge characteristics [20]

catastrophic VDD droop, by placing a capacitor in parallel with the battery, this problem can be alleviated.

In the wireless network system, the radio circuitry consumes the largest portion of power. In order to save power as possible, radios should be heavily duty-cycled, because the de-cap cannot pull such high current from battery all the time. Also, current limiter is necessary to protect battery from high current at the radio.

1.6 Thesis Contributions

1.6.1 A Fully-Integrated Wireless Sensor Node in a 10.6mm^3

A 10.6mm^3 fully-integrated, wireless sensor node with 8GHz UWB transmitter has been demonstrated. The wireless sensor node includes solar energy harvesting with an integrated 2μAh battery, optical receiver for programming, PMU, microcontroller and memory, 8GHz UWB transmitter, and miniaturized custom antennas. The WSN operate autonomously from harvested energy, initially powered and programmed optically, and broadcast UWB messages of sensed data at a fixed time period. The communication range for the dipole was 7 meters with a peak SNR of 10dB which is the highest reported distance to volume ratio. My main contribution of this wireless sensor node is to design external antennas, top-level integration of the WSN and system-level verification. It is the first time to demonstrate a full and stand-alone wireless sensing functionality with such a tiny integrated system.

1.6.2 A Fully-Integrated GPS Logger Co-Designed Receiver/Antenna

The fully integrated GPS logger co-designed receiver and antenna is presented. An ultra-low-power (ULP) GPS logger system that features a custom miniaturized antenna co-designed with a

GPS analog front-end (AFE) optimized for heavy duty-cycling and a 10x10x6mm^3 form-factor. The GPS logger can sample 115K fixes from the 12mAh Li-ion battery before recharging. The flash is sufficient to hold ADC samples for 37 fixes before retrieval. After post-processing by streaming over 10ms, the 10dB SNR required for the GPS logger is -125dBm. In the sleep mode, the processor and the timer only consume 50nW and in the active mode the total power jumps up to 12.5mW. My main contribution of the GPS logger is to design GPS AFE in 65nm CMOS, top-level integration of the GPS logger and system-level verification.

1.6.3 A Tri-band GPS Receiver in 65nm CMOS

The GPS analog front-end (AFE) is specifically designed for receiving the GPS tri-band signals by using passive mixers. The main contribution of the RF front-end is comprised of a signal path which support the tri-band mode (L1, L2, L5) which can be sampled the three bands onto a single IF channel simultaneously. The AFE is able to fold the tri-band GPS signals onto a low-IF thanks to the orthogonality of the pseudo-random (PRN) codes. The radio draws 9.6mW from a 1.2V/1.4V supply, with a passive RF front-end and a startup time of 20μs.

1.6.4 A 60-GHz Band Integrated Slot Loop Antenna and Field Distribution in 0.13-μm BiCMOS

An integrated rectangular slot loop antenna in a standard 0.13-μm BiCMOS technology is presented. By using the slot loop antenna, it can easily satisfy the metal density rules without dummy metal fill and can be integrated with other circuitry. The total area of the antenna including the ground plane is 0.883mm^2 and the loop antenna only occupies 0.24mm^2. The antenna resonates at 59.2 GHz and the bandwidth at VSWR 3.0 is 2.77 GHz from 57.95 GHz to 60.72 GHz with 300-ohm load. The measured peak gain at 59 GHz is about 0dBi.

Chapter 2 A Fully-Integrated Wireless Sensor Node in a 10.6mm^3

This chapter presents a complete, autonomous, wireless temperature sensor, fully encapsulated in a 10.6mm^3 volume. The sensor includes solar energy harvesting with an integrated 2μAh battery, optical receiver for programming, PMU, microcontroller and memory, 8GHz UWB transmitter, and miniaturized custom antennas. Because of its millimeter-scale, the 2 μAh micro-battery has a maximum discharge current of <100μA which places new challenges on the power management of this mm-scale wireless sensor node. The WSN is consisted of 8-layer stack of heterogeneous dies which are designed and collaborated with numerous colleagues in Univ. of Michigan [22]-[23], [25]-[32], [35]. My main contribution of this wireless sensor node is to design external antennas, top-level integration of the WSN and system-level verification. The active power consumption of the IR-UWB transmitter far exceeds the peak discharge current of the battery. As a result, a fully-integrated modem is included to duty-cycled the RF circuits at the bit-level. Likewise, the temperature sensor is also duty-cycled, and keep in a low power standby mode the majority of the time. Current limiters on multiple ICs in the sensor protect the battery from over-current conditions. In this system, an optical wake-up receiver is implemented for external triggering and programming without any physical connections required. Two types of miniaturized custom antennas, a monopole and dipole, on a glass substrate are demonstrated, which are co-designed to the IR-UWB transmitter to optimize its communication range, achieving 7 meters. This system consumes 8nA in sleep mode and 36 μA in active mode. Full, stand-alone operation was demonstrated for the first time for a system of this size and functionality.

2.1 Introduction

Wireless personal area networks (WPANs) demand for a millimeter-scale wireless sensor node. These miniature wireless sensors will enable new applications in fields such as biomedical devices, infrastructure monitoring, defense and un-obstructive surveillance. This form-factor is driven by a desire to be vanishingly small, injectable through a needle, or implantable through a minimally-invasive surgical procedure. Wireless communication and energy harvesting are necessities, however to date the range of communication has been limited to only a few centimeters, limited by the peak power available from the battery and poor radiation efficiency of millimeter-scale antennas [21-22].

Power management is a primary challenge at mm-scale form factors, due to severely limited harvested power and energy storage capacity. The mm-scale battery technology with limited capacity and peak current [23] requires efficient integrated power conversion, heavy duty-cycling of high-power modules, ultra-low standby leakage power, and under-voltage/over-current battery-protection circuitry. Heterogeneous die stacking helps to alleviate these challenges, by enabling components to be designed in their optimal processes. However, seamless interaction across dies is essential, in particular at the interface circuits, for sustained operation with long lifetimes.

In order to meet the power requirements of the mm-scale battery, each of wireless sensor components in this system are designed to achieve robust ultra-low power operation [24]. For communication among layers, an ultra-low power interconnect bus (MBus) is implemented. MBus employs a unidirectional ring topology to avoid the high power of shared wires, bus arbitration, and bi-directional drivers. The system includes an integrated wakeup scheme which is compatible with PMUs with a special low power standby mode. The radio is designed for a high supply voltage to operate directly from the battery through a current limiter, and low sleep power. The current-

limiting at the battery supply prevents it from exceeding the peak current of the battery, which would degrade capacity and lifespan. Integrated decoupling capacitors are used on the PMU, radio, and processor layers to provide higher peak currents for a short amount of time when e.g. the RF front-end is enabled to transmit one bit, which is then recharged between bits. IR-UWB communication was selected because the pulse-based modulation scheme naturally provides the smallest duty-cycling ratio.

The limited antenna size is another primary challenge for a millimeter scale wireless sensor node. The wavelength at 8GHz is much longer than the millimeter form factor of the system, therefore electrically small antennas are required. As a result, the antenna and UWB transmitter are co-designed in order to miniaturize the size, and eliminate the need for an off-chip matching network. The primary goal is to maximize the radiated power by reducing the mismatch between the transmitter and antenna, and minimizing the impact of the die stack. This work introduces a

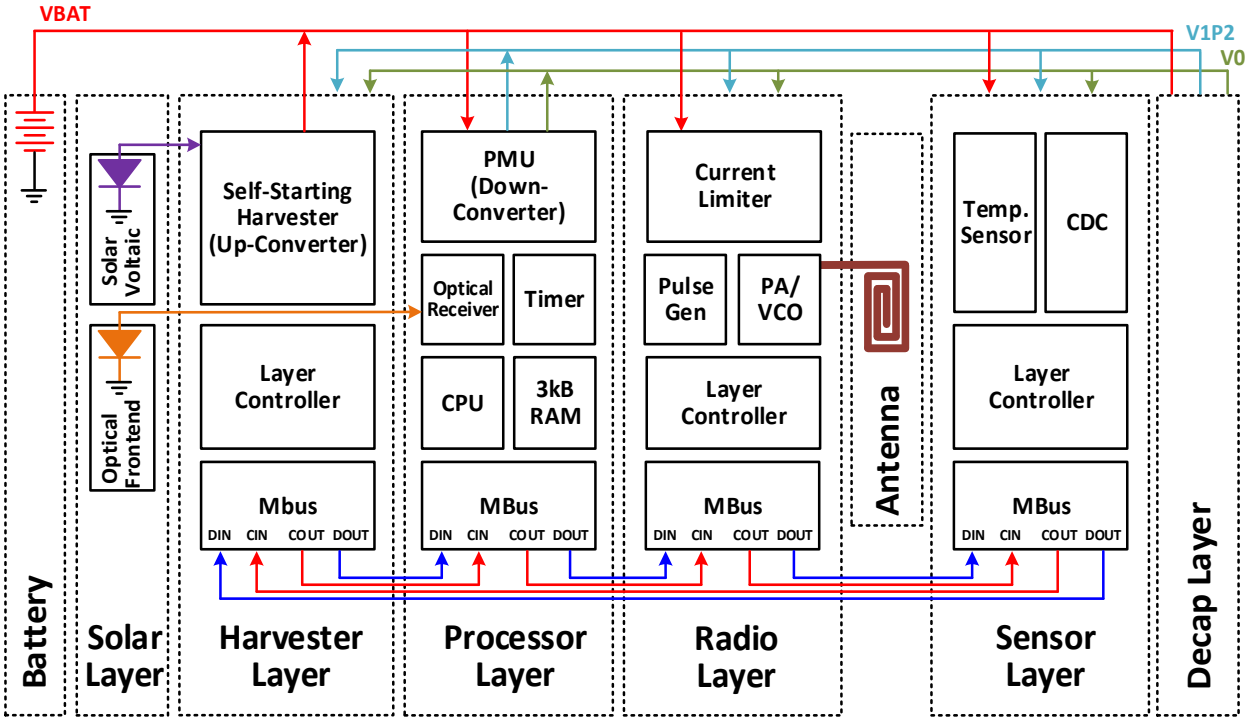


Figure 2.1 Overall system block diagram of the 8GHz WSN

fully integrated wireless sensor that enables meter-range communication with a base station using two custom antennas, a monopole and dipole, co-designed with the UWB transmitter to optimize radiated power.

2.2 System Overview

The overall system block diagram is shown in Figure 2.1. The circuits are implemented in a heterogeneous 8-layer stack of thinned die, which communicate via MBus, a fully digital interconnect bus scheme suitable for energy-constrained sensing systems [25]-[26]. The processor layer contains an ARM Cortex-M0 microcontroller along with a power management unit which down-converts the battery voltage to generate 1.2V and 0.6V power domains distributed across the stack [27]-[31]. A 3 kB SRAM serves as instruction and data memory. The battery is a 2µAhr solid state thin film Li rechargeable battery (2.21 x 1.00 x 0.25 mm^3) supplied by Cymbet that operates between 3.6-4.2V. A sensor layer contains the temperature sensor and a 13-bit CDC that can be used for optional pressure measurements. A self-starting energy harvester [32] can up-convert the solar cell output with a configurable conversion ratio to charge the battery. Energy

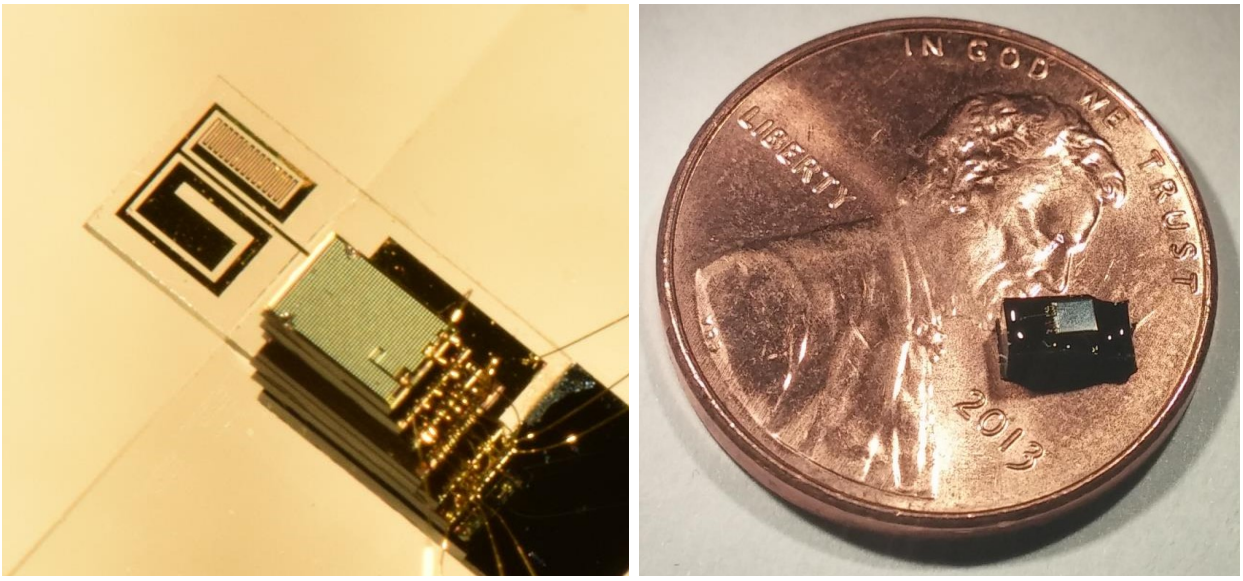


Figure 2.2 Photo of proposed stack system and encapsulated stack

harvesting is implemented and serves two main purposes: initial charging of the battery after assembly and re-charging of battery for extending the lifetime of the sensor node.

For initial programming of the system, an ultra-low power optical receiver was integrated in the wireless sensor node where it can directly load a program into the memory, trigger control signals to wake up the CPU, set configuration bits, and turn on an RF radio block to initiate high-speed communication.

One of the key elements in the wireless sensor node system is a wake-up receiver which has to remain on even during sleep mode, since accurate time synchronization with the access point is not affordable from either a power or size perspective. Traditional RF wake-up receivers have standby currents that are too high for the proposed system [33], or use low-frequency narrowband signaling that require large antennas. An ultrasonic solution has been proposed [34], but it requires an off-chip piezoelectric element and its standby power of 4uW still remains high.

In this system, an optical wake-up receiver is implemented [35]. The wake-up receiver's role in the proposed system is three-fold: 1) Initial programming after system assembly and boot-up, 2) user-specified external triggering for system operation, and 3) re-programming the system after software failure. A pulse-width modulation encoding scheme is used, in which bit 1 is encoded as a long pulse, and bit 0 is encoded as a short pulse. The receiver consists of an optical front-end, analog front-end, decoder, and protocol controller.

The radio layer contains an IR-UWB transmitter with a tunable output frequency from 8 to 11GHz and a current limiter to protect the battery from over-current when the radio is on [36]. Finally, the dies are stacked on a low loss glass substrate including a printed, 8GHz wideband antenna co-designed with the UWB transmitter. The entire system including the glass substrate is

encapsulated with epoxy for physical protection (Figure 2.2), which raises unique challenges for the initial battery charging and system boot up of the fully encapsulated system.

2.3 Wireless Start-up Sequence

The WSN presents the first fully-wireless startup of a system of this size, including battery charging. The solid-state battery is initially uncharged after fabrication, and must remain so during the assembly process to endure the high temperature epoxy curing. With exposure to light of ~200 lux (dim indoor light) the harvester is able to self-start and commence battery charging, with a minimum solar cell output voltage of 140mV and power of 1.6nW. Figure 2.3 shows a measured battery charging curve when energy is harvested under 25kLux light which requires 15.5 hours to fully charge the integrated battery. As the charged battery voltage rises beyond 3.6V, the system automatically initiates a boot sequence. Initially, the PMU raises the 1.2V supply and holds the

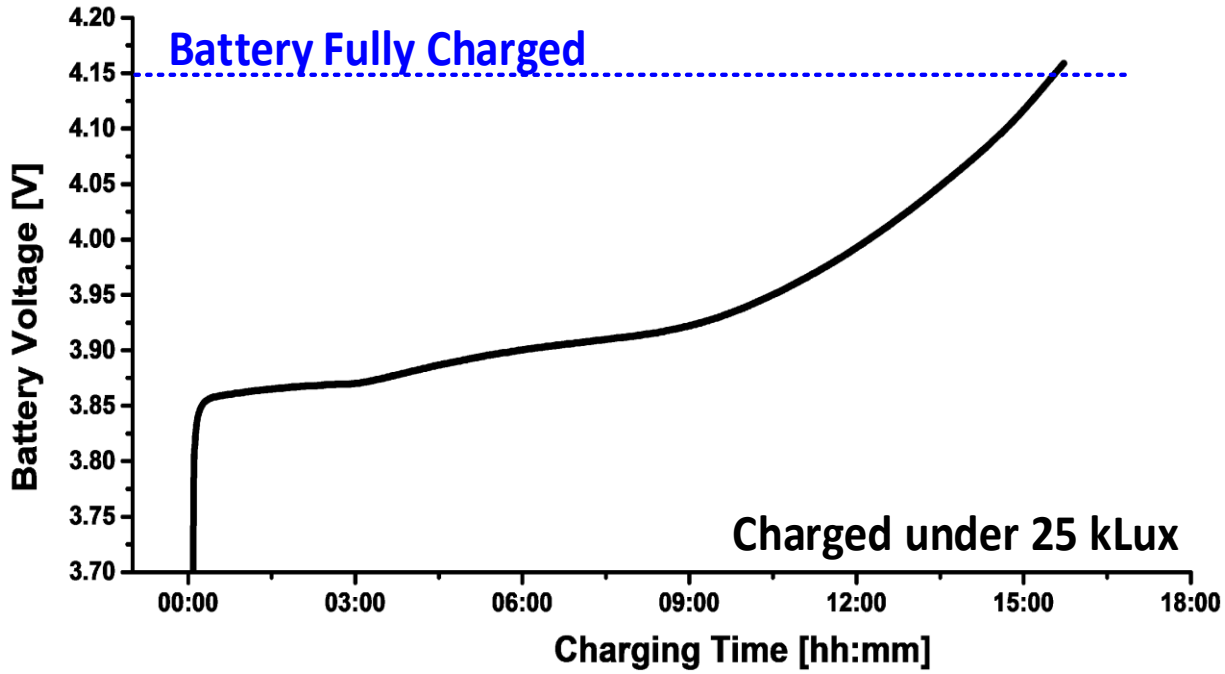


Figure 2.3 Battery charging characteristic under 25Klux light

0.6V supply to ground. This state is detected by reset detectors in each layer to generate clean reset signals for critical blocks such as the configuration registers. This is critical to ensure that no layers are accidentally started up in an active or invalid mode, pulling high current. Subsequently, the 0.6V supply is raised, and the system enters a sleep mode, in which the core is still power-gated and the SRAM has no content. The reset values of configuration registers ensure that the circuit components are either power-gated or in an ultra-low power state.

Once the battery is fully charged, the system is programmed via optical communication to load the SRAM with a program [37]. The front-end photodiodes of the optical receiver are placed in the SOLAR layer located at the top of the stack for light exposure through clear epoxy, such that the rest of the stack can be encapsulated with black epoxy to minimize light-induced leakage current in the ICs. Optical communication can also directly change the configuration register settings or send interrupts. Once the SRAM is loaded, system operation commences, switching between sleep and active modes and communicating with blocks in different layers via MBus. Figure 2.4 shows the current consumption of the sensor system programmed to transmit data once

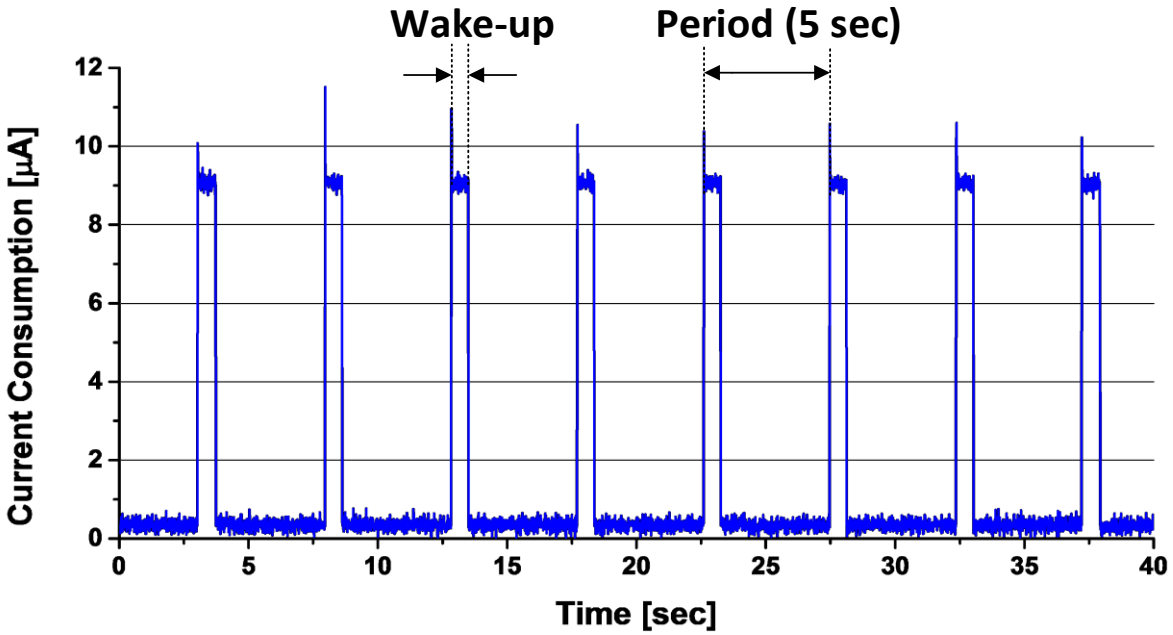


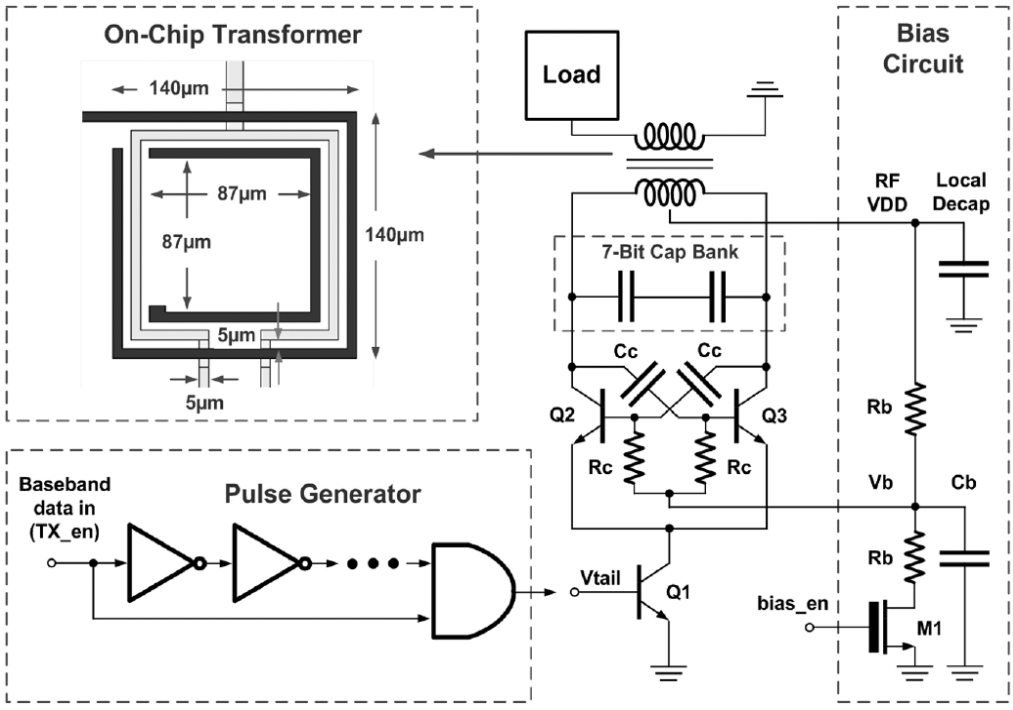
Figure 2.4 Current consumption in sleep and active mode

every 5 seconds. In sleep mode, it consumes 2nA and in active mode current jumps to ~9µA for 700ms. The initial current peak upon wake up is due to the charging of decoupling caps on power-gated supplies and no overcurrent is observed during radio transmission due to the current limiter in the Radio layer.

2.4 Antenna and UWB Transmitter

2.4.1 UWB Transmitter

An ultra-low power IR-UWB transmitter [22] is used with a modified, non-coherent pulse position modulation scheme (Figure 2.5). Transmit data is first loaded in a local buffer over MBus. Then, using a local oscillator for bit-timing, pulses are generated at either an early or late edge of the clock, depending on the data bit. These nanosecond pulses then turn on the VCO-PA which



*J Brown, et al. ISSCC, Feb 2013

Figure 2.5 Schematic of the ULP IR UWB transmitter

drive the antenna through a transformer. The center frequency may be tuned from 8 to 12 GHz by tuning caps at VCO through control bits programmed over MBus. The frequency is tuned according to the antenna it is connected to, and the frequency that produces the largest output power is selected. At a 30 kb/s data rate, the average power of the TX is only 22.4 μW at 3.6 V. The current limiter is included, also digitally tuned through MBus, to protect the battery from high current at the radio.

2.4.2 Antenna Design

This system demonstrates the sensor node operating with two antennas; a monopole and dipole. Both antennas are fabricated on glass substrates with lower substrate loss than silicon or printed circuit boards (PCB), to achieve higher antenna efficiency. The dimensions of both antennas are only 0.05 λo x 0.11 λo which includes the antenna ground plane on which the stack of chips sit. Compared to the lengths of a typical monopole and dipole of 0.25 λo and 0.5 λo, the antennas are electrically small in order to achieve mm-scale dimensions.

The first antenna is a dual-resonance monopole which provides sufficient bandwidth for the UWB signals. Each arm in the antenna has a slightly different length in order to produce two

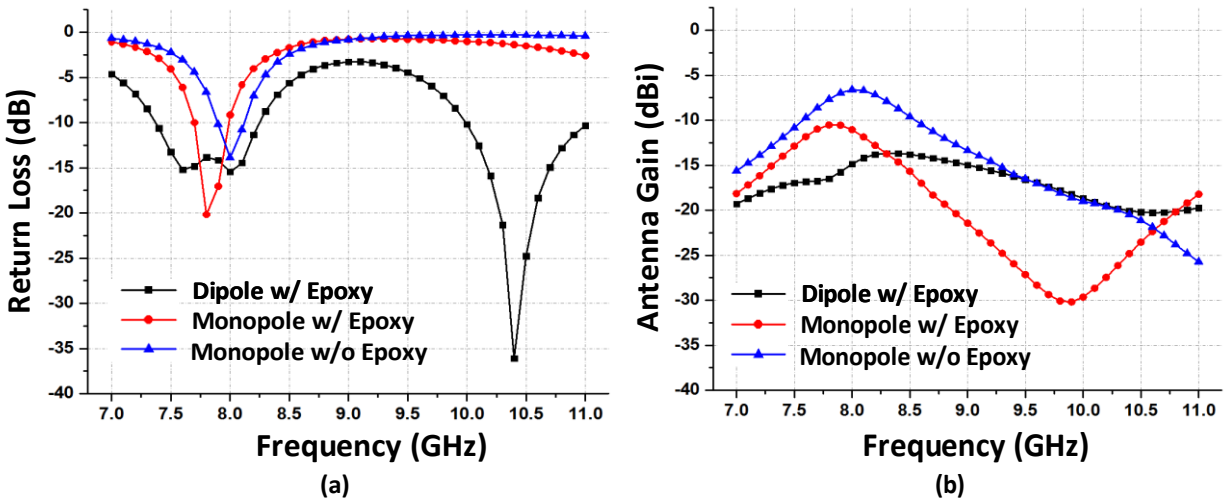


Figure 2.6 (a) Return loss (S11) (b) antenna gain variation

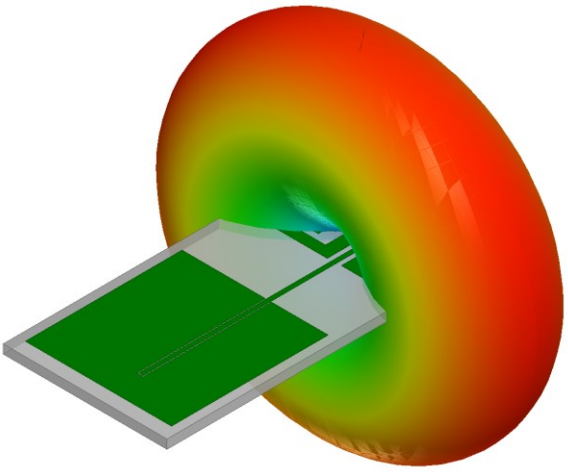


Figure 2.7. Radiation pattern of monopole

nearby resonant frequencies. The return loss and antenna gain of the antennas are summarized in Figure 2.6. It achieves a fractional bandwidth of 9% and -7.5dBi peak gain at 8 GHz. The radiation pattern of the monopole is plotted in Figure 2.7. A monopole has an advantage that it could save the physical antenna area by using its ground plane as reflector. This provides an area to place the

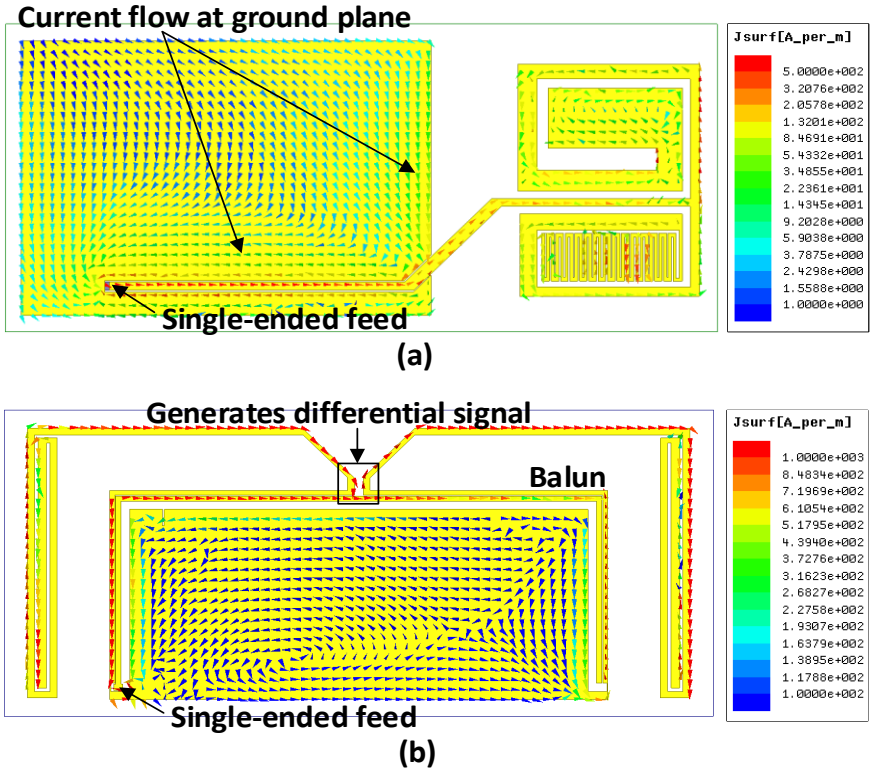


Figure 2.8 Surface current distribution (a) monopole (b) dipole

die stack on the antenna substrate. However, when the monopole is considered as an electrically small antenna, much smaller than the wavelength, the antenna gain is not determined from antenna element itself, but by its ground plane and environment, which in this case also includes the sensor node die stack (Figure 2.8(a)). The ground effect on the monopole degrades the antenna gain and shifts the resonance frequency, which leads to a shorter communication distance compared to free-space.

To isolate these environmental and ground plane effects, a dipole antenna with a merchant balun is proposed (Figure 2.8(b)). The single-ended output at the transmitter is converted to a fully differential signal through the merchant balun at the feed point of the antenna. Although the dipole has lower antenna gain compared to the monopole because it requires 2x more space than a monopole, its radiation performances are much more reliable, with much less impact from the die stack.

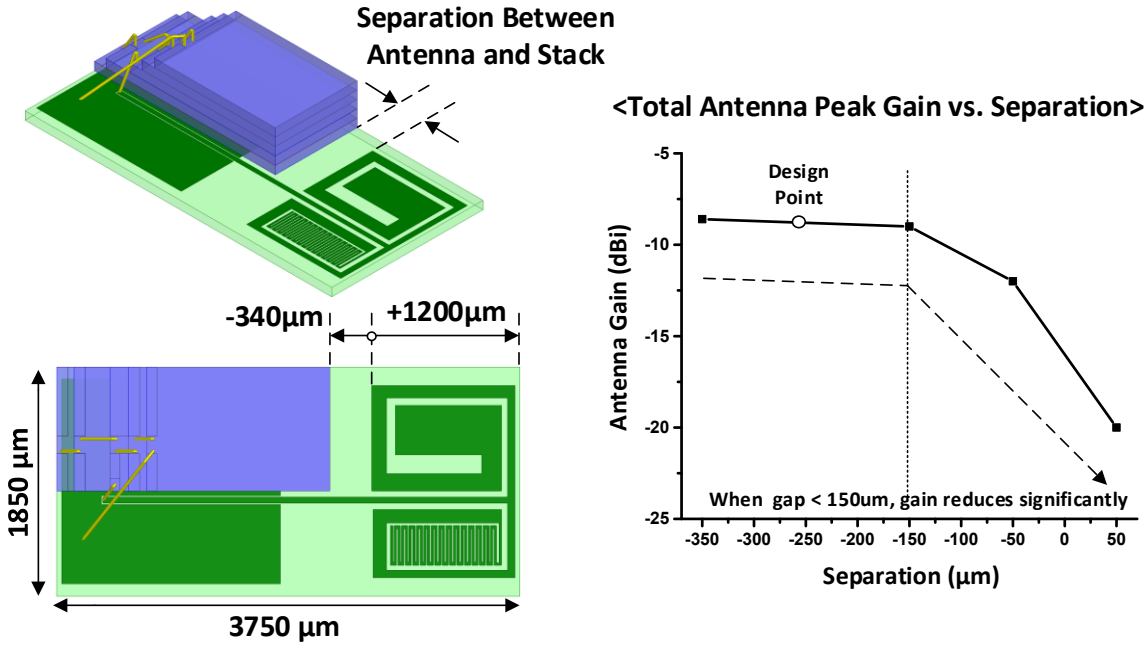
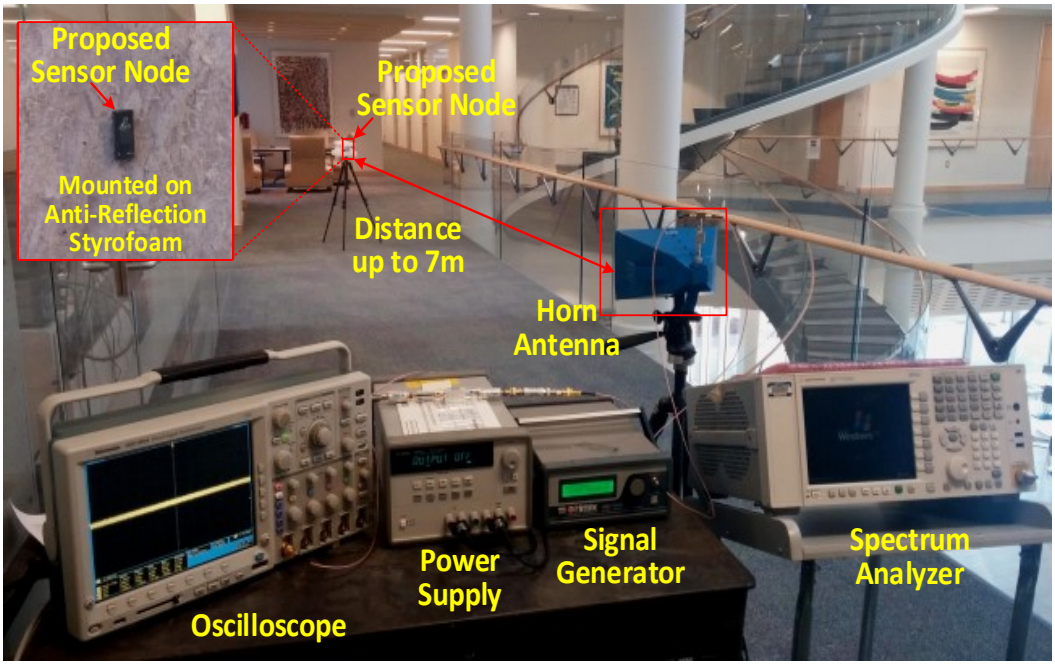


Figure 2.9 Total antenna gain reduction by separation between antenna and stack

2.4.3 Co-designed Antenna and UWB Transmitter

The antenna and UWB transmitter are co-designed in order to miniaturize the antenna size, and eliminate the need for an off-chip matching network. The primary goal is to maximize the radiated power by reducing the mismatch between the transmitter and antenna, and minimizing the impact of the die stack which is placed in close proximity to the radiating element. Figure 2.9 shows the mutual relation between the die stack and the antenna. When the separation is less than 150μm, the antenna gain reduces significantly due to the reflection from the IC layers and the discontinuity in dielectric constants of the materials. The lossy epoxy used for encapsulation also degrades the gain and shifts the resonance frequency of both antennas, which leads to a shorter



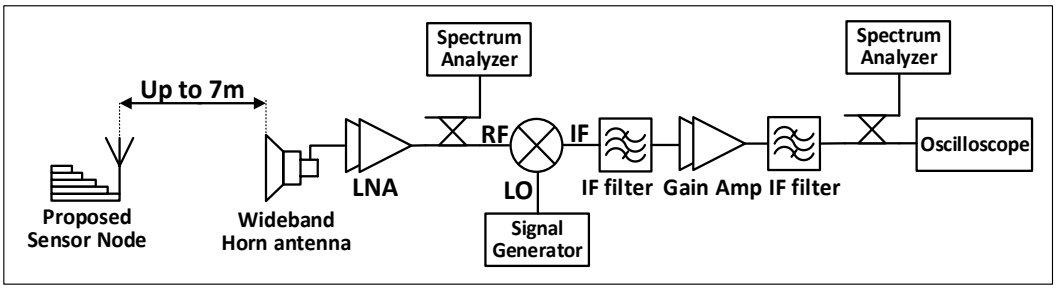
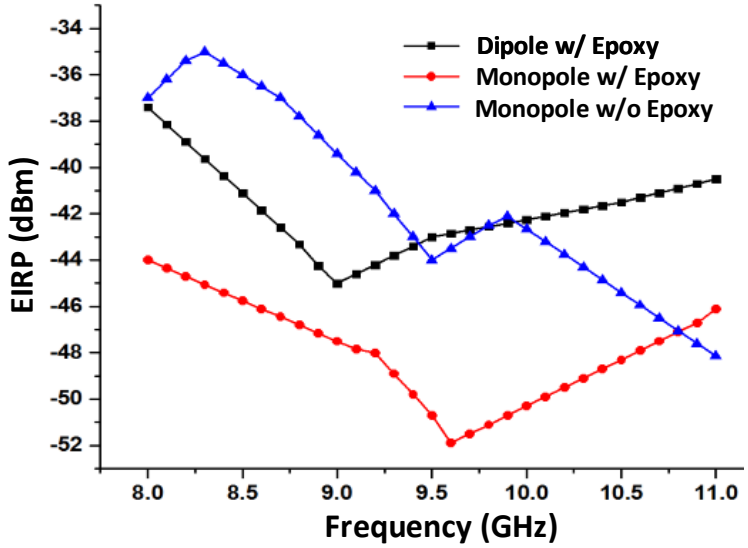


Figure 2.10 Test setup between the die-stacked sensor node and a base station

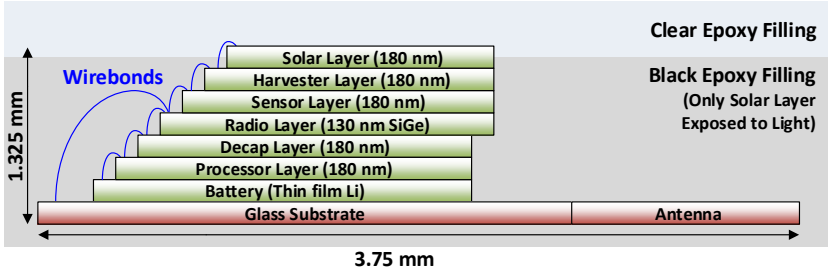
communication distance compared to free-space. To simultaneously minimize the antenna dimensions and electrical mismatch, the output of the transmitter and the input of the antenna both are matched to 50 Ohms without using an off-chip matching network. The transmitter and antenna both have a measured VSWR less than 3:1.

2.5 Measurement Results

Figure 2.10 shows a test setup between the die-stacked sensor node and a base station, and the equivalent isotopically radiated power (EIRP) at the transmitter as a function of center frequency.



(a)

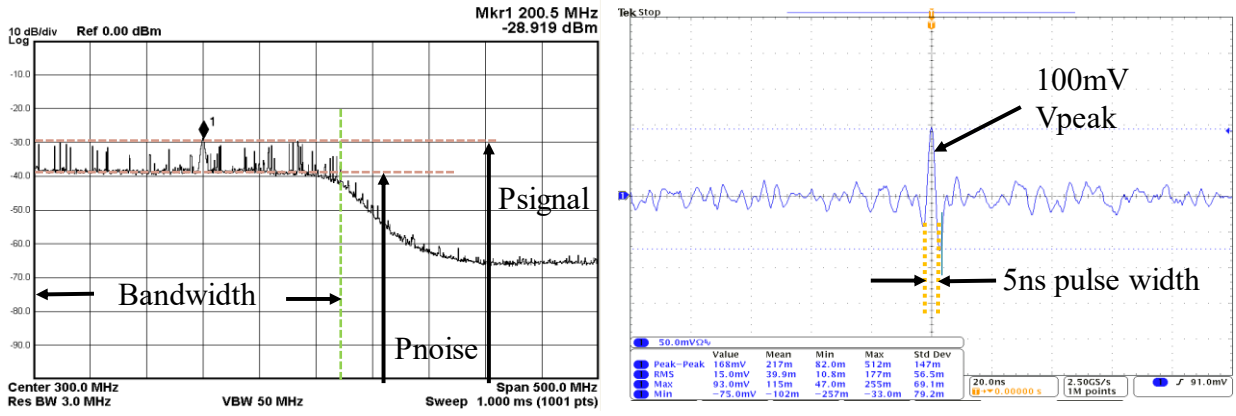


(b)

Figure 2.11 (a) The measured EIRP by sweeping VCO (b) Encapsulation of the entire system

This EIRP can be used to determine the base-station sensitivity for a target distance. The proposed stack is apart from 7m away in aisle and the stacks is mounted on anti-reflection Styrofoam. At the receiver, it has consisted with 10dBi wideband horn antenna and mini-circuit components. The whole system is encapsulated with two types of epoxy for physical protection (Figure 2.11(b)). The front-end photodiodes of the optical receiver are placed in the SOLAR layer located at the top of the stack for light exposure through clear epoxy, such that the rest of the stack can be encapsulated with black epoxy to minimize light-induced leakage current in the ICs. In Figure 2.11(a), the EIRP of the stack with monopole indicates 6dB less than the one with a dipole even though the gain of the monopole is 4dB higher than the dipole. Thus, when it comes to encapsulation for mm-scale sensors, the monopole is much more sensitive on the environmental variations compared to the dipole, and the dipole is therefore preferred.

For the distance test, the received signal was amplified and down-converted to an IF (150MHz) before being observed on an oscilloscope to verify functionality. The base-station has 52.8dB gain and 10dB noise figure at IF and -99dBm sensitivity including the receiver antenna gain. The measured communication range for the dipole was 7 meters with a peak SNR of 10dB (Figure



(a) (b)

Figure 2.12 Measurement between the wireless sensor node and a base station
(a) Received UWB signal at spectrum analyzer (b) Received pulse at oscilloscope

2.12). Table 2.1 summarizes the measured performances of the wireless sensor node with comparison to the state of the art. A figure of merit of communication distance per volume is introduced, which highlights this work compares to stat of the art. It would show that this work achieved not only low power and small volume, but also a long distance communication. The die micrograph of the stack is shown in Figure 2.13.

2.6 Conclusions

A 10.6mm^3 fully-integrated, wireless sensor node with 8GHz UWB transmitter has been demonstrated to operate autonomously from harvested energy, initially powered and programmed optically, and broadcast UWB messages of sensed data at a fixed time period. This sensor node

		This work			VLSI 2014 [35]	VLSI 2007 [36]	MTT 2011 [37]
		Dipole w/ Epoxy	Monopole w/ Epoxy	Monopole w/o Epoxy			
Dimension [mm^3]		1.85 x 4.1 x 1.4			2 x 4 x 4	10 x 10 x 10	40 x 22 x 1.1
Power	Active	36 µW			40 µW	36 mW	5.4 mW
	Standby	8 nW			15 nW	1.8 µF	7.2 µW
Distance		7.0 m	3.8 m	13.4 m	15 mm	10 m (10.7 Mbps)	60 m
Distance/Volume [Normalized]		1	0.54	1.91	0.0007	0.015	0.094
Wireless		8.0 GHz			Optical Receiver RF Transmitter	Original UWB	3.6-4.1 GHz
Battery Capacity		2 µAh Thin-Film			5.7 µAh Thin-Film	150 mAh	-

Table 2.1 Measurement summary and performance comparison

has total volume of 10.6mm^3, while achieving microwatt power consumption and meter-range communication. The communication range for the dipole was 7 meters with a peak SNR of 10dB which is the highest reported distance to volume ratio. This system consumes 8 nA in sleep mode and 36 µA in active mode. Full, stand-alone operation was demonstrated for the first time for a system of this size and functionality.

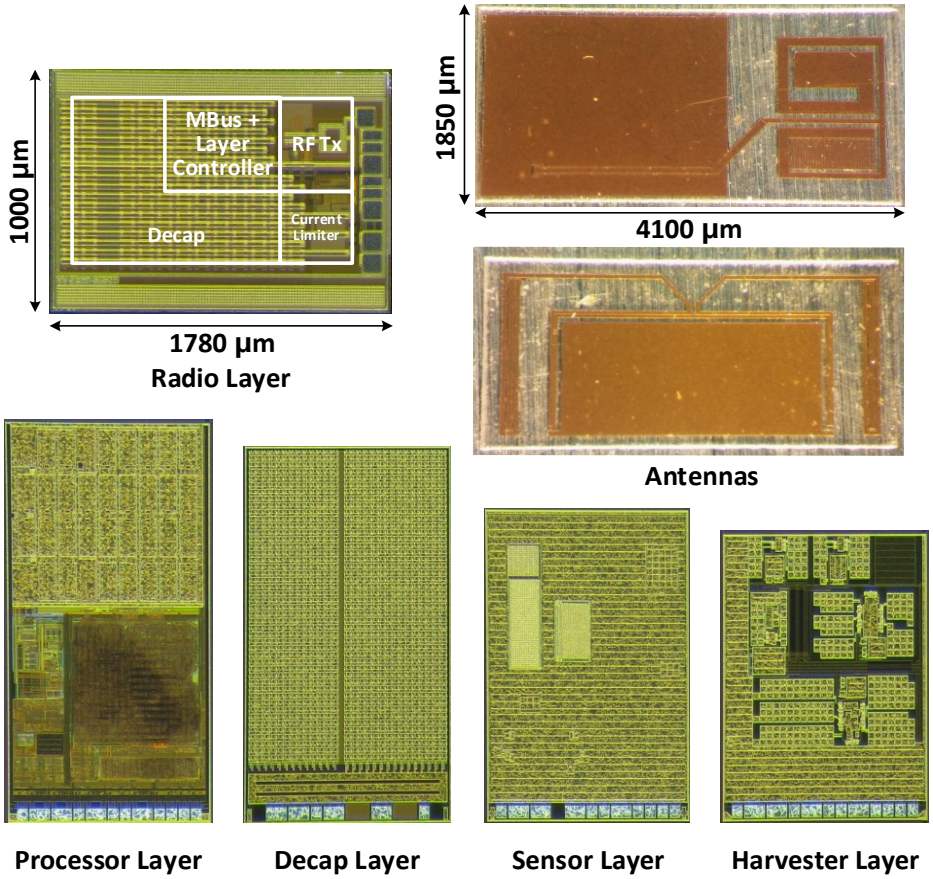


Figure 2.13 Die micrograph of the stack

Chapter 3 A Fully-Integrated GPS Logger Co-Designed Receiver/Antenna

This chapter presents an ultra-low-power (ULP) GPS logger system that features a custom miniaturized antenna co-designed with a GPS analog front-end (AFE) optimized for heavy duty-cycling in a 10x10x6mm^3 form-factor. The complete system includes a GPS AFE, processor, two custom 8Mb flash memory chips, custom antenna, and a 12mAh polymer Li-ion battery. An electrically small differential loop antenna is designed, and all components are integrated on the top and bottom of the antenna in close proximity without degrading the antenna efficiency. In the sleep mode, the processor and the timer consume 50nW and in active mode it draws 12.5mW from a 1.2V supply. The AFE achieves a maximum conversion gain of 72dB, a noise figure of 3.5dB, and P1dB of -46dB. The blocker level that desensitizes the gain by 1dB is -6.1dBm at 1710 MHz, one of the closest blockers near the GPS bands. The GPS logger achieves a 10dB SNR after correlation at an input power level of -125dBm. The logger is capable of storing data for 37 position fixes by streaming 10ms of received signal per fix to dual flash memories for later egress and post-processing.

3.1 Introduction

The Global Positioning System (GPS) is consisted of a constellation of 32 satellites. Every GPS application ultimately involves the determination of platform position, velocity, and/or time and it requires an unobstructed line of sight to four or more GPS satellites [40]. Typically, outdoor

signal is -125dBm which is below the thermal noise level in its bandwidth. The satellites transmit to the user in the form of binary data over the ranging signal via a spread-spectrum communication technique; BPSK phase modulated signal with 1ms duration of a complete coarse/acquisition (C/A) code [41]. Typically, the amplitude of the outdoor GPS signal is -125dBm which is below the thermal noise level in its bandwidth. By running the correlation with the expected pseudo-noise (PN) sequence of captured ADC samples, it could produce the processing gain for the post-processing SNR.

There is a growing demand for GPS tracking systems with low-power consumption, millimeter scale form factor, and high performance. Interest in these systems is driven by the desire for small form factor and long lifetime for applications such as wearable devices, asset trackers, and drones. Many of these applications do not require a high rate or real time position-tracking, so the power requirement is significantly reduced by heavily duty-cycling. The power of the GNSS signal is lower than the channel noise, and the small form factor makes it even smaller due to the small radiation efficiency [42].

One of the main challenges when miniaturizing GPS tracking systems is power consumption. Millimeter-scale batteries have limited capacity and low peak current levels, both of which present challenges for powering a GPS analog front-end (AFE) for acquiring signal and flash memory for storing sampled data. A second challenge is the antenna design. At millimeter-scale, a GPS-band antenna is electrically small, and as a result efficiency can suffer. Finally, there is the challenge of integrating the entire system together, in particular for the RF performance, because all components, including the battery and ICs, need to be placed in close proximity of the antenna. This paper presents a complete GPS logger system that features a custom antenna co-designed with a GPS AFE optimized for heavy duty-cycling and a 10x10x6mm^3 form-factor. The complete

stack is modeled and incorporating into a differential loop antenna design, which allows integration of components on the top and bottom of the antenna without impacting of antenna efficiency. Furthermore, the antenna and AFE are co-designed to maximize sensitivity. The GPS logger is capable of storing data for 37 position fixes by streaming 10ms of received signal per fix to dual flash memories for later egress and post-processing.

3.2 System Overview

The proposed system is specifically designed for an ultra-low-power (ULP), fully integrated, and miniaturized GPS logger. As shown in Figure 3.1, this GPS logger includes a GPS AFE, ARM

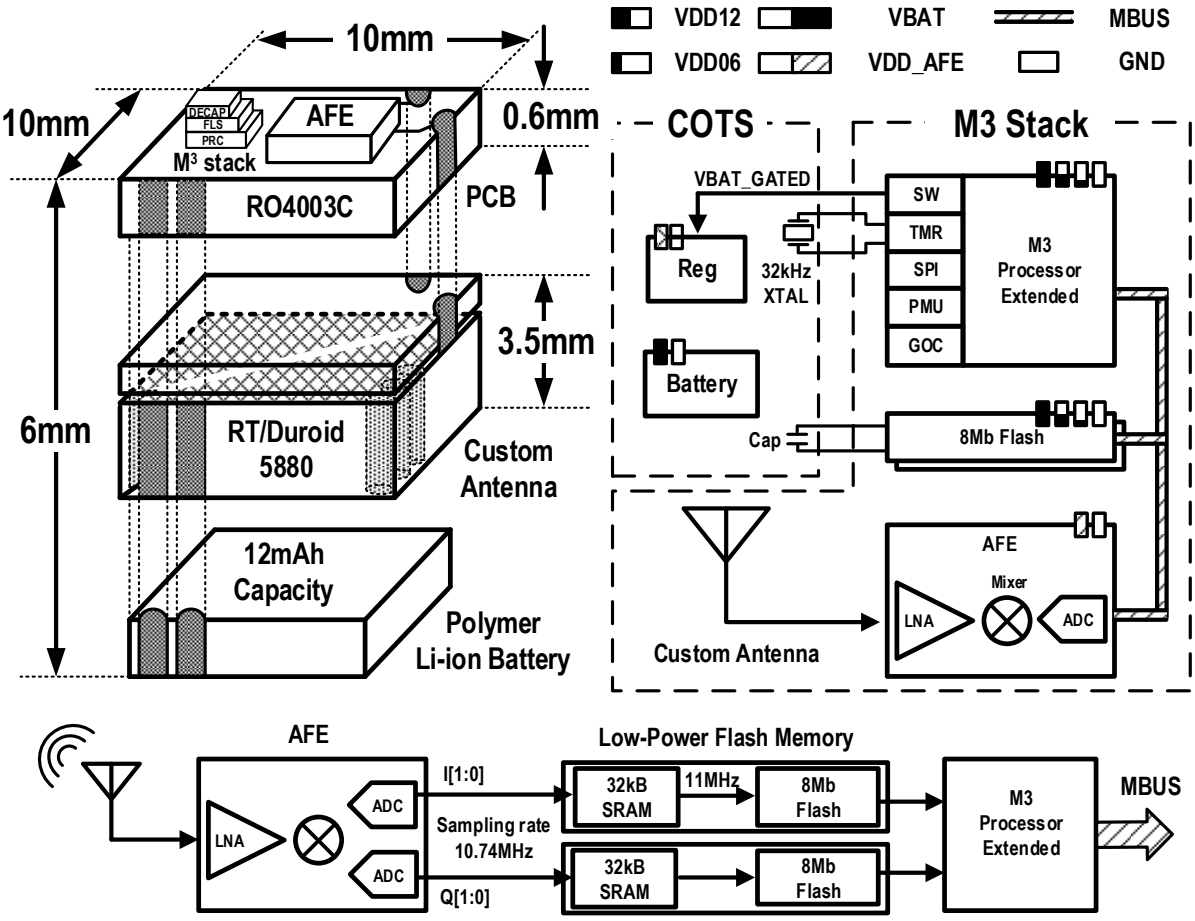


Figure 3.1. Conceptual diagram and overall system block diagram of the proposed GPS logger for 10x10x6mm^3

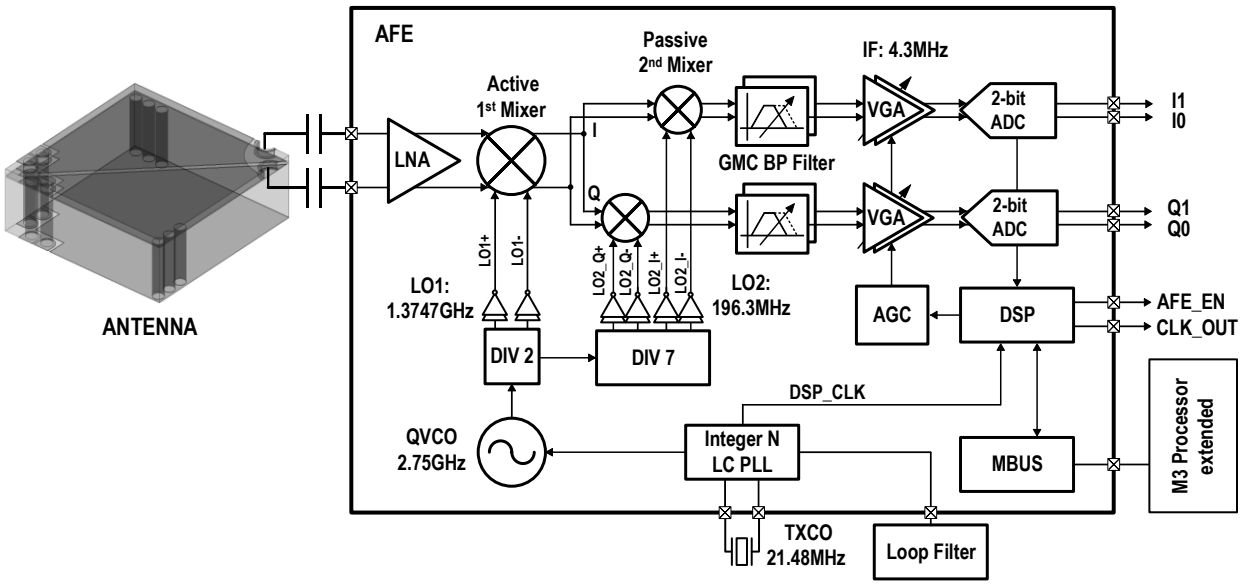


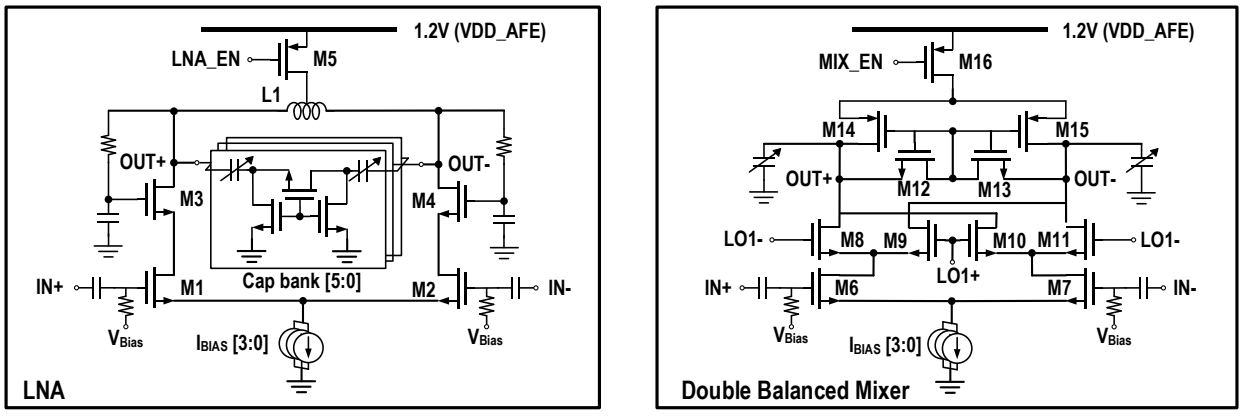
Figure 3.2. Overall block diagram of the AFE

Cortrx-M0 processor, two custom 8Mb flash memory chips, custom antenna, and a 12mAh polymer Li-ion battery with a total system volume of 10x10x6mm^3. The AFE turns on for 10ms intervals, sufficient to capture one GPS fix. The AFE boots up and shuts down in 20us, minimizing the energy overhead from startup. Since highly accurate time is kept, the AFE can also turn on precisely when new satellite ephemerides are broadcast and sleep during the rest of the transmission. When the AFE is operating, the quantized 2 bits I/Q signals at the ADC are captured for 10ms at a 10.74MHz sampling rate. The off-line correlation is performed with the expected PN sequence of the GPS satellite signal. An electrically small GPS antenna has an overall size of 0.05λo x 0.05λo x 0.018λo. For better efficiency, the inter-connection between the AFE and antenna is through castellated holes in the PCB, with a 0.6mm thickness board.

3.3 GPS Analog Front-End (AFE) Receiver

The overall block diagram of the GPS AFE is shown in Figure 3.2. It includes a low noise amplifier (LNA), an active double balanced mixer, passive mixers, IF filter, a VGA, a 2 bits ADC, digital baseband with an automatic gain control (AGC) loop, frequency synthesizer, DSP and MBus interface connecting the chip with the system processor. When the AFE is powered, the MBus interface and DSP blocks are always-on, while the rest of blocks are in stand-by mode until receiving an enable signal from the processor.

The entire receiver employs fully differential quadrature signals. The signal path includes an internal LNA, a gilbert type double balanced mixer for a 1st down-conversion stage, and an IQ passive mixer for a 2nd down-conversion. Figure 3.3(a) depicts the schematic of the cascode CS LNA covering a range from 1.1GHz to 1.6GHz and the active mixer. The output of the LNA is AC-coupled to a gilbert type double-balanced quadrature mixer which realizes 1st down-conversion to IF1 (200.7MHz) as shown in Figure 3.3(b). An I/Q passive mixer, driven by a differential quadrature LO, performs the 2nd down-conversion to IF2 (4.3MHz). The low-IF path is comprised of an IF filter and VGA with an AGC loop. The AGC loop controls the amplification



(a) (b)

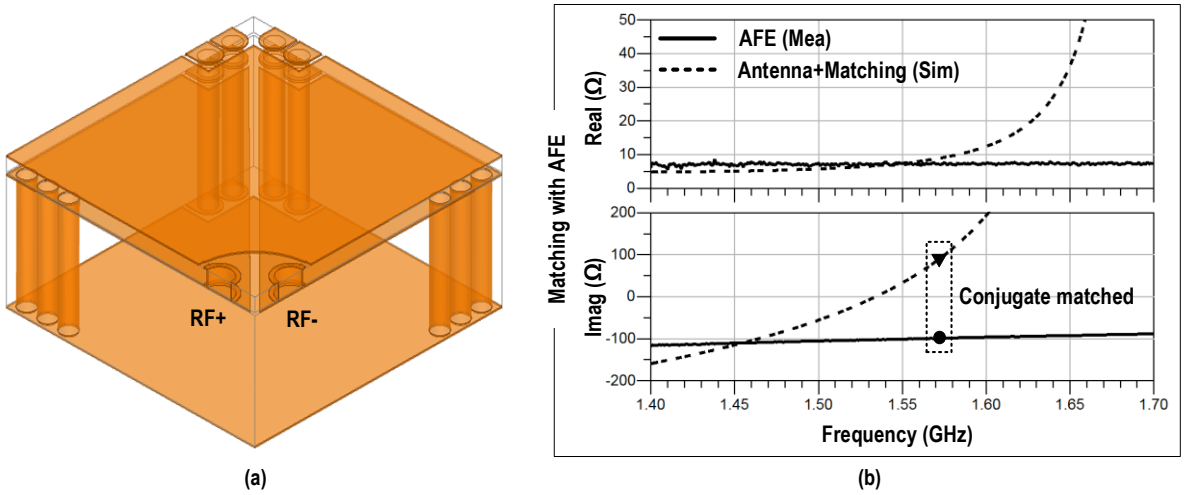
Figure 3.3. Simplified schematics (a) LNA (b) Active mixer

of VGA based on the histogram of the ADC codes to maintain the desired signal level at the ADC input. The ADC quantizes in 2 bits outputs at a sampling rate of 10.74MHz.

An integrated Integer-N PLL is used to provide differential and quadrature signals. The differential LC VCO oscillates at 2.749GHz while LO1 and LO2 are at 1374.7MHz and 196.3MHz, respectively. The LO signal is divided further to provide the sampling clock for the ADC and DSP. It has an external loop filter with a 100kHz bandwidth and a reference clock of 21.48MHz, all integrated within the system depicted in Figure 3.1.

3.4 Custom Designed GPS Antenna

A custom antenna has been developed for the GPS logger presented here. Nikolaos Chiotellis from Prof. Grbic group in Univ. of Michigan designed this custom antenna for the GPS logger. The GPS antenna is a linearly polarized, differentially-fed single-turn loop antenna. It consists of two Rogers 5880 RT/duroid® 5880 PCBs with dimensions 10x10x3.175mm^3 and 10x10x0.381mm^3. The thicker board is responsible for reception, while the thinner one shields the antenna from the AFE and provides the necessary routing. As a result, the antenna occupies a 10x10x3.556mm^3 volume and exhibits a *ka* value of 0.24, where k is the wavenumber at the



(a) (b)

Figure 3.4. (a) Miniaturized GPS antenna (b) input impedance and matching with AFE

frequency of operation (1.575GHz) and α is the radius of the smallest sphere that encircles the antenna. A *ka* value of less than 1 indicates an electrically small antenna [43].

The antenna, shown in Figure 3.4(a), sits under the PCB that contains the AFE and is connected to it through two castellated holes, to which the differential signal (RF+ and RF-) is applied. The four holes on the opposite side provide conducting paths in case another PCB or system (e.g. a PV cell) is attached on the bottom side of the antenna. The RF current travels through the holes to the right, traverses the bottom metal plane, and returns through the holes on the left, forming a loop. Alternatively, the current can jump over the thin gap. Hence, the antenna's equivalent circuit comprises an inductor and a capacitor in parallel. The inductance can be tuned by adjusting the right and left holes' number and radius, and the capacitance by adjusting the gap. The antenna's self-resonant frequency can thus be easily tuned. The design is simulated and optimized in ANSYS Electronics Desktop (formerly HFSS). The antenna operates below resonance at the GPS frequency. This allows it to be subsequently conjugate matched to the AFE using only lumped capacitors in order to maximize the sensitivity of the system. The input impedance of the antenna prior to matching is presented in Figure 3.4(b). As expected, Figure

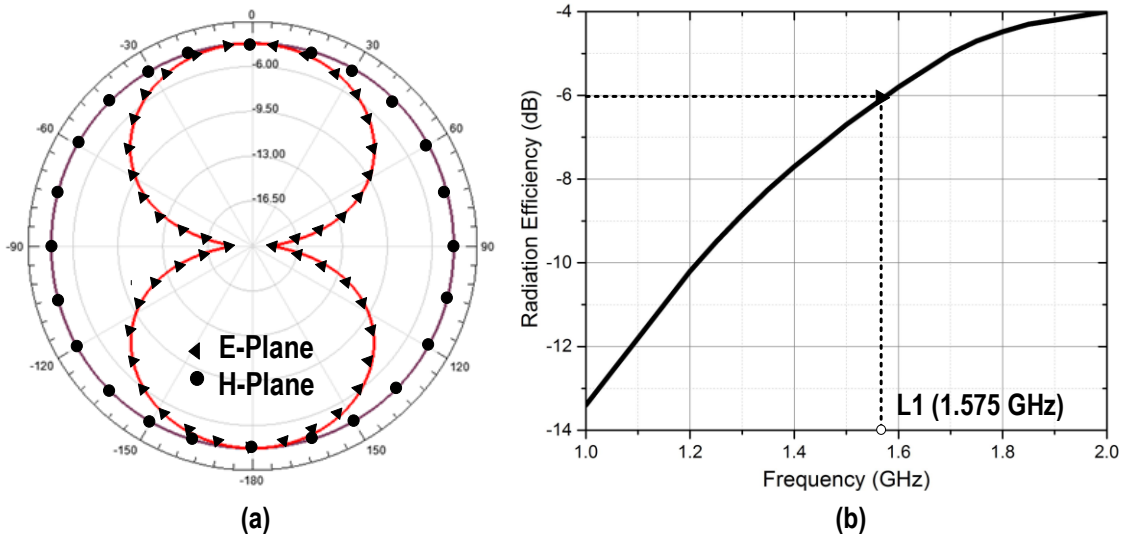


Figure 3.5. (a) Radiation pattern (b) radiation efficiency

3.5(a) show its radiation pattern corresponds to that of an electrically small loop and its radiation efficiency (-6dB at 1.575GHz) as a function of frequency are shown in Figure 3.5(b).

3.5 Off-line Correlation of Captured AFE Signals

The performance of integrated AFE and antenna is evaluated by running the off-line GPS signal correlation of captured ADC samples. The off-line correlation is performed in Matlab where the captured ADC sample sequence is correlated with the expected PN sequence of the actual GPS satellite signal. The correlation code can handle arbitrary ADC sampling rate which is typically 2x of the intermediate frequency (IF) of the AFE. Intentional narrowband jamming signals also can be added for evaluating AFE's resilience against interferences. The PN sequence of any 32 satellite

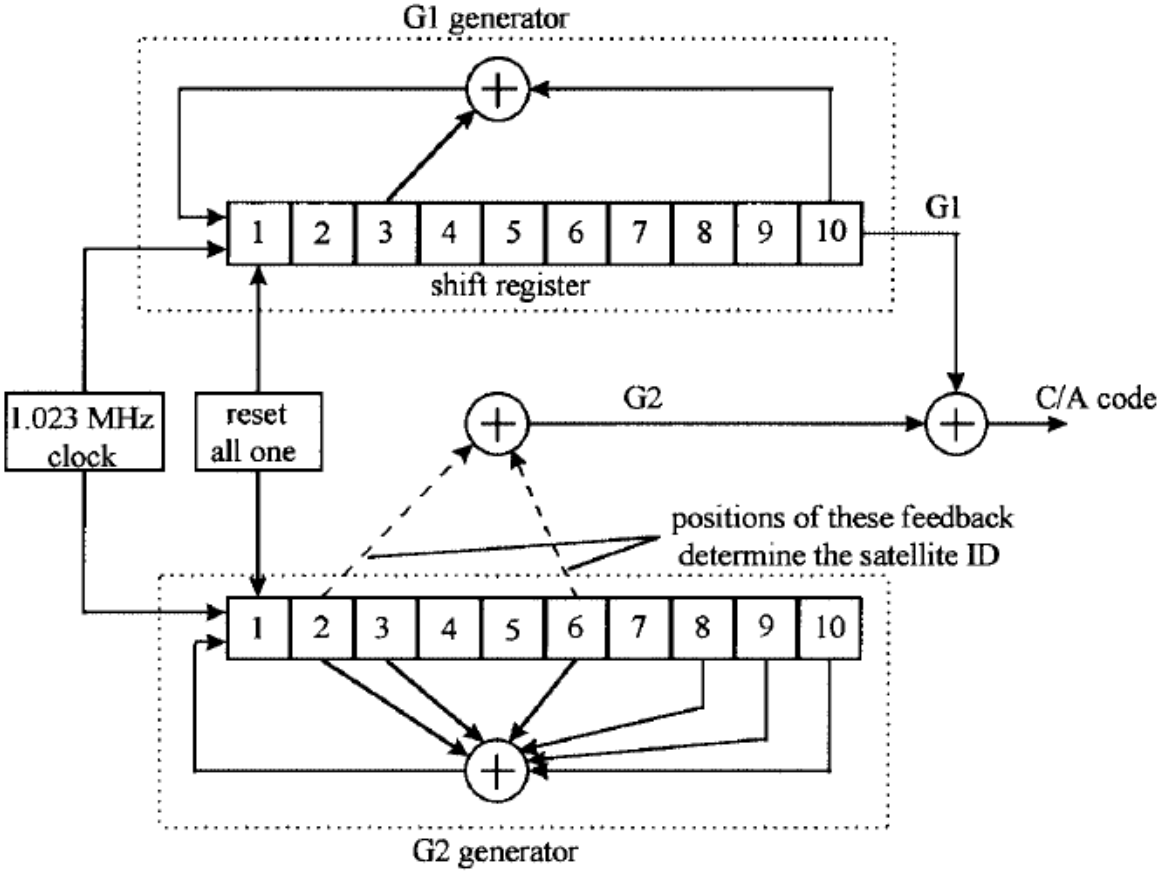


Figure 3.6. GPS PN sequence generation structure [44]

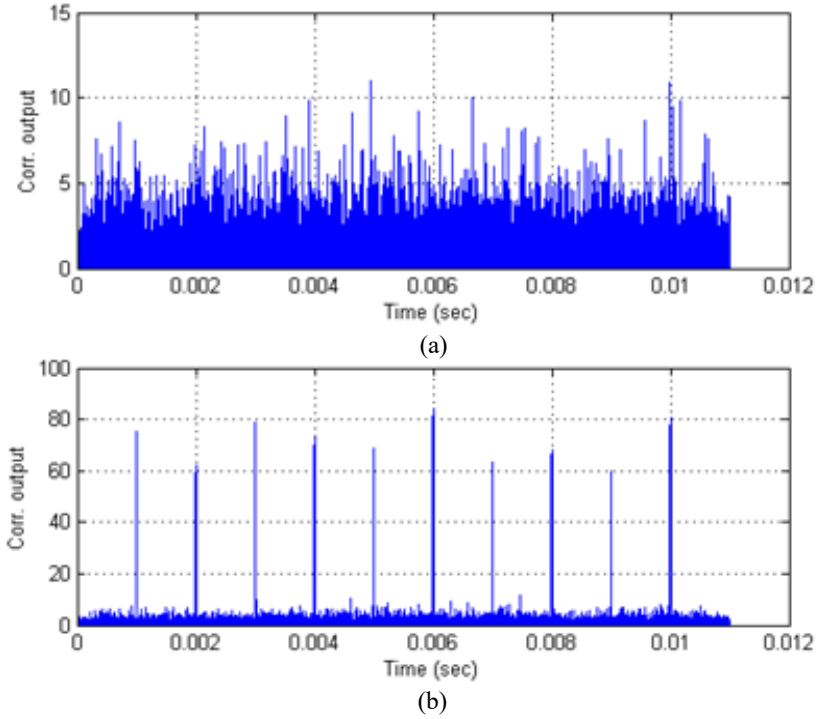


Figure 3.7 (a) PN seqeunce mismatch (correlated with an incorrect satellite ID) (b) Output from the matching PN sequence and satellite ID

IDs can be tested for correlation. The correlation length for the PN sequence is 1023 chips. Therefore, the maximum processing gain attainable for the post-processing SNR is 30dB. The correlation process can be represented by $corr[n] = \left|\sum_{k=1}^{1023} s[n-k]e^{-j2\pi n f_{IF}/f_S} p[k]\right|$ where $s[n]$ is the complex valued ADC samples with sampling rate of f_S, f_{IF} is the IF frequency, and $p[k]$ is the target satellite PN sequence of ±1 (Figure. 3.6) [44]. Correlation output for -10dB SNR input captured signal over 10ms time period. 10 correlation peaks are observed in Figure 3.7.

The post processing SNR is defined by the equation (1). With 30dB theoretical coding gain, the post-processing SNR S[dB] is translated to approximately S-30[dB] pre-processing signal SNR when non-ideality factors such as the frequency offset is ignored.

$$post\ processing\ SNR = \frac{\text{mean power of the correlation peak}}{\text{mean power of the correlation at non peak positions}} \quad (1)$$

3.6 Side-by-side Wireless Testing of Custom AFE and COTs AFE

The performance of the custom integrated AFE and antenna is compared with an off-the-shelf COTS GPS AFE (MAX 2769) and antenna to compare them side-by-side. The 8-channel logic analyzer simultaneously captures the quantized 2-bits outputs (I and Q) from both the custom AFE and COTS AFE for 100ms. The two AFEs have different IF frequencies and ADC sampling rates, which are accounted for in the post-processing of the data in Matlab. The COTS GPS AFE uses a -6dBi monopole antenna, which is placed next to the custom AFE so that the two systems have similar path loss from a single GPS transmitter 2m away Figure as shown in Figure 3.8.

After post-processing, the sensitivity acquired for 10dB SNR of the integrated AFE with antenna and the COTS GPS AFE are about -125dBm and -129dBm, respectively. It is measured at 2m away from the GPS signal generator and the input power at 10dB SNR is estimated by de-embedding the antenna loss, path loss and mismatch. Table 3.1 summarizes the specifications and results from the side-by-side measured comparison. After post-processing, the sensitivity required

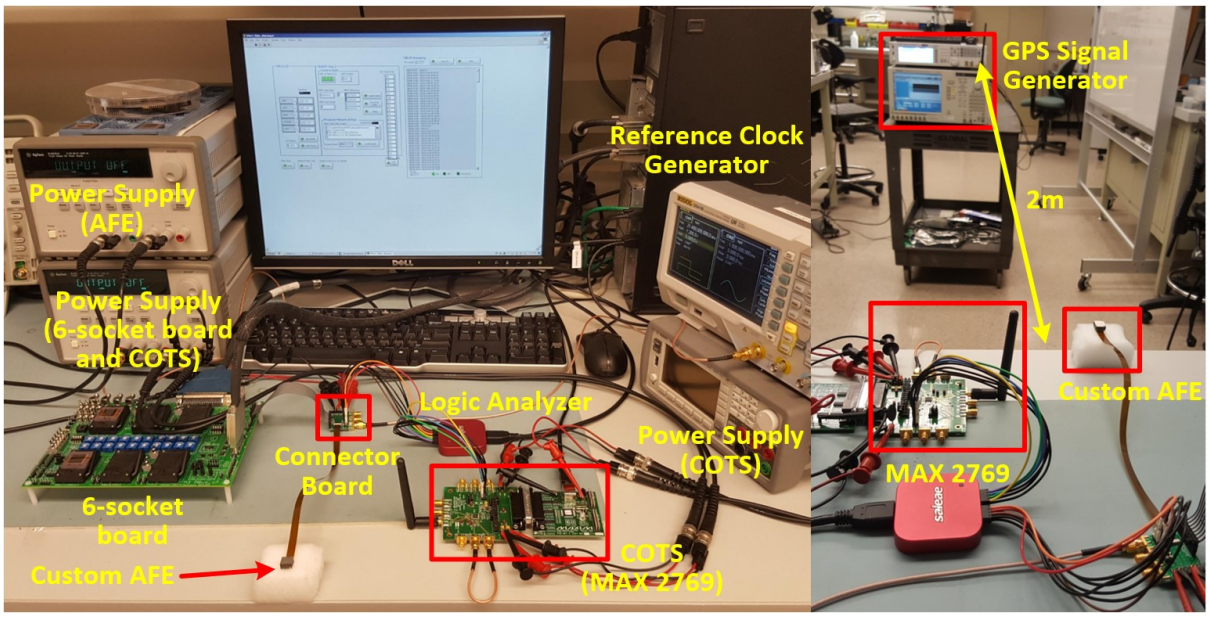


Figure 3.8. Test setup of a side-by-side comparison

for 10dB SNR of the integrated GPS logger and the COTS GPS receiver are about -125dBm and -129dBm, respectively.

	UM AFE with Antenna	MAX2769
Power	12.1 mW	51.3 mW
Gain	72 dB	96 dB
Noise figure	2.2 dB	1.4 dB
Input impedance	9-j*130 ohm (Differential)	50 ohm (single-ended)
Matching	Conjugate matching	50 ohm matching
IF frequency	4.3 MHz	4 MHz
Bandwidth	6 MHz	8 MHz
ADC sample rate	10 MHz	50 MHz
Reference frequency	21.4 MHz	16.3 MHz
Measured Sensitivity	-125 dBm	-129 dBm

Table 3.1 Comparison of custom AFE to COTS GPS AFE

3.7 Measurement Results

Figure 3.9 shows a test setup between the GPS logger and the GPS signal generator. The signal generator transmits the L1 C/A-coded GPS signal with PN sequence of any 32 satellite IDs. The

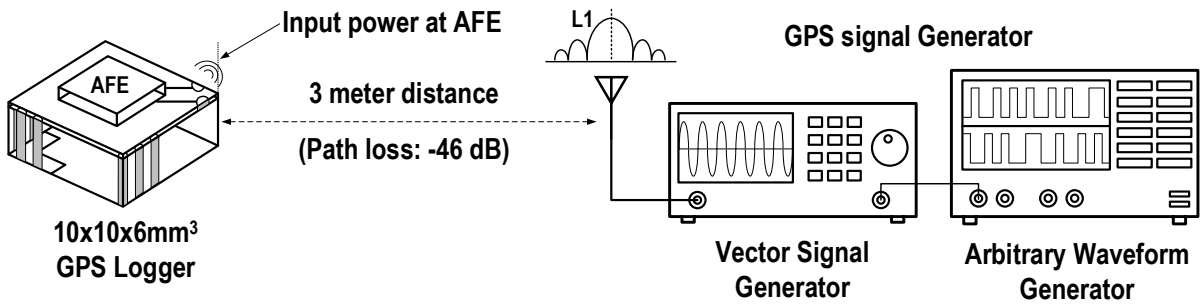


Figure 3.9 Measurement setup of the GPS logger

antenna, PCBs, and AFE were assembled at mm-scale and verified stand-alone, and receiver performance is reported from these stacks. Control signals to the M3 stack and flash connected to a separate PCB, verifying full functionality of the GPS logger recording fixes. Various GPS signal power levels were tested by adjusting EIRP of the transmitter at a distance of 3 meters (-46dB path loss) where ensured radiating at the far field distance in a wireless setup. The AFE and other layers are controlled via MBus, a fully digital energy efficient interconnect bus scheme.

The timing diagram of initial control waveform of MBus and power consumption are presented in Figure 3.10. For initialization, with a wake-up signal, the processor, AFE, and flash are initialized in sequence and then flash start erase operation. This step happens one-time at the initialization. The AFE turn on and off for 10ms and the captured data store in SRAM and transfer to flash memory. The GPS logger get back to the sleep mode when the storing data into the flash

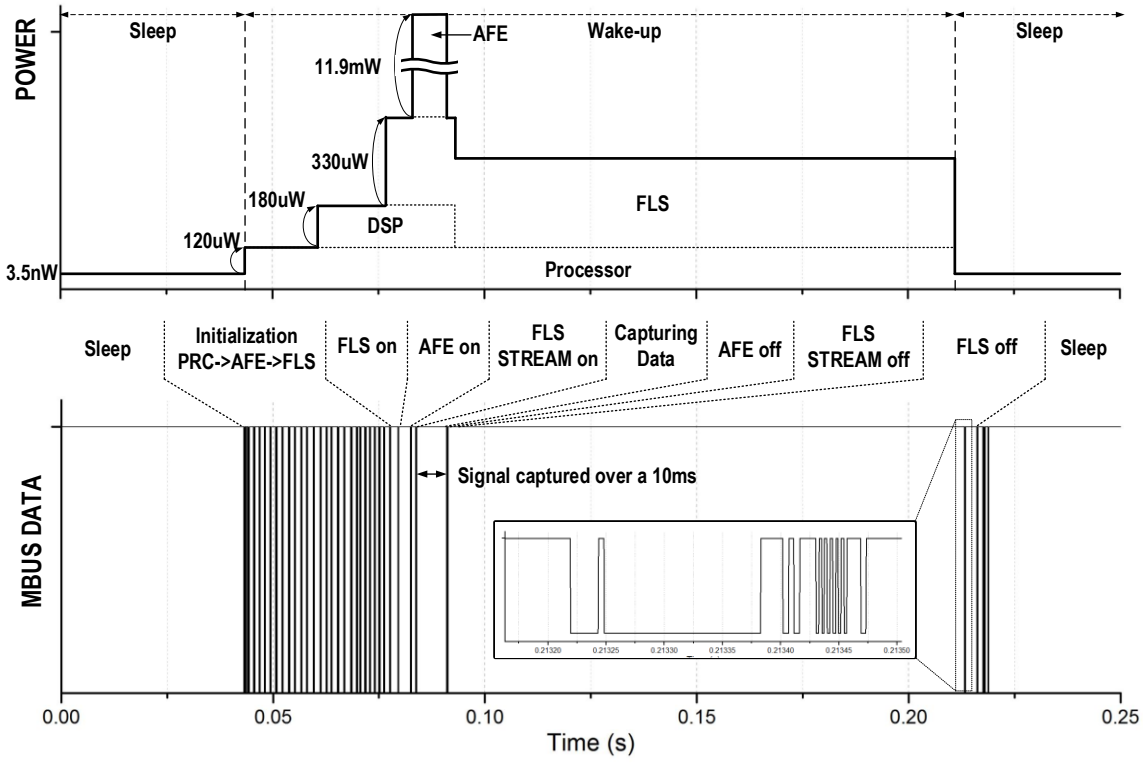


Figure 3.10 Timing diagram of MBUS data and power consumption for a fix

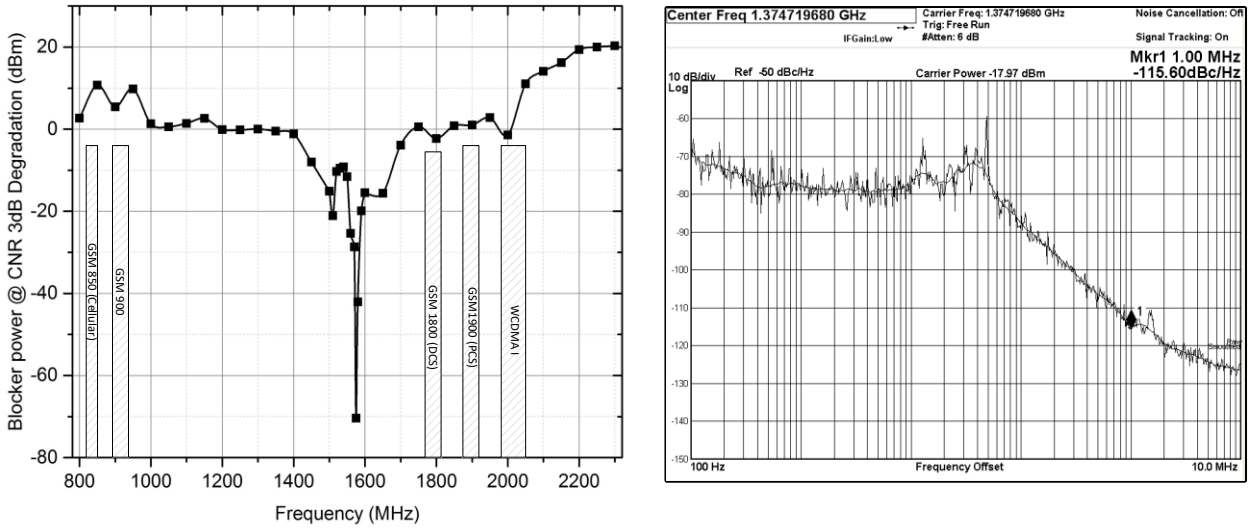


Figure 3.11 (a) Out-of-band blocking performance (b) PLL phase noise at LO1 (1374.7 MHz)

is completed. In the sleep mode, the processor and the timer only consume 50nW and in the active mode the total power jumps up to 12.5mW which is dominated by the power consumption from the AFE. From the 12mAh Li-ion battery, the GPS logger can sample 115K fixes and the flash is sufficient to hold ADC samples for 37 fixes before retrieval.

The AFE achieves a maximum conversion gain of 72dB, a noise figure of 2.2dB, and P1dB of -46dB. The blocker level that desensitizes the gain by 1dB is -6.1dBm at 1710MHz, one of the closest blockers near the GPS bands. The measured 3dB CNR degradation level with the CW out-of-band blockers is shown in Fig 3.11(a). The measured phase noise of the VCO is -115.6dBc/Hz at 1MHz offset frequency from the LO1 at 1374.7MHz (Figure 3.11(b)). The AGC loop is implemented in the controller and regulates the 5-bits VGA control code varying the gain from -13 to 22dB (Figure 3.12(a)). The ADC outputs are captured over a 10ms and off-line correlation is performed where the captured ADC sample sequence retrieved from flash is correlated with the expected PN sequence of the GPS satellite signal. The GPS logger achieves a 10dB SNR after correlation at an input power level of -125dBm with capturing over a 10ms. The results of the post-

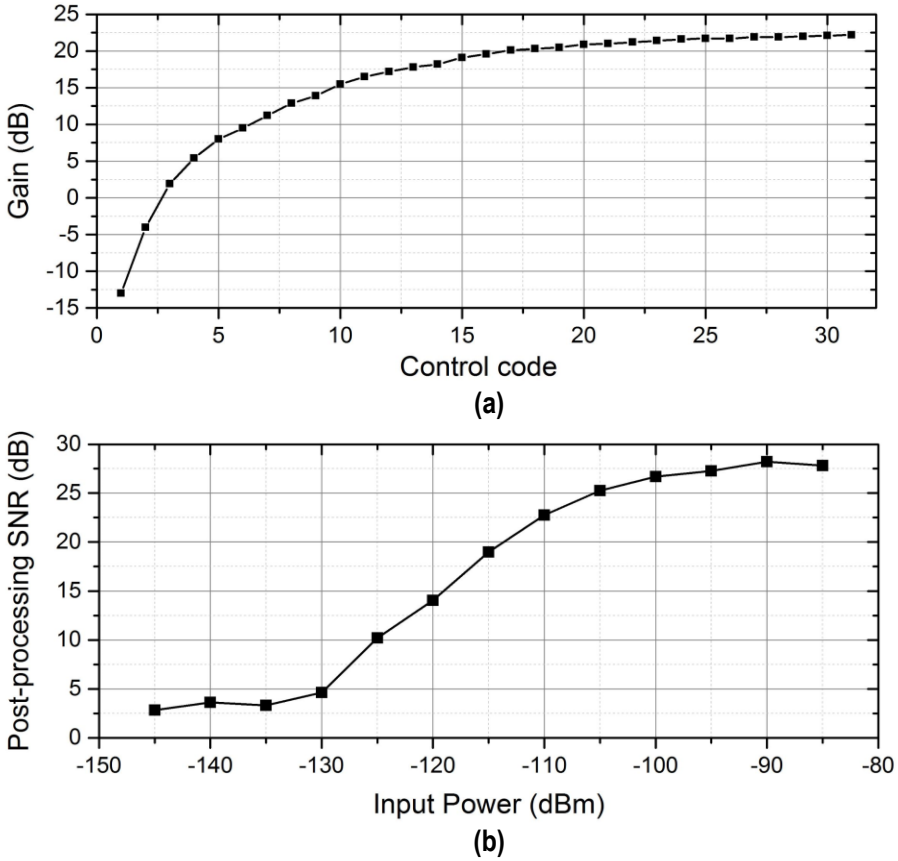


Figure 3.12 (a) VGA gain tuning range (b) Post-processing SNR in L1

processing SNR depending on the input power is shown in Figure 3.12(b). Table 3.2 summarizes the measured performance of the GPS receiver with comparison to the state-of-the-art.

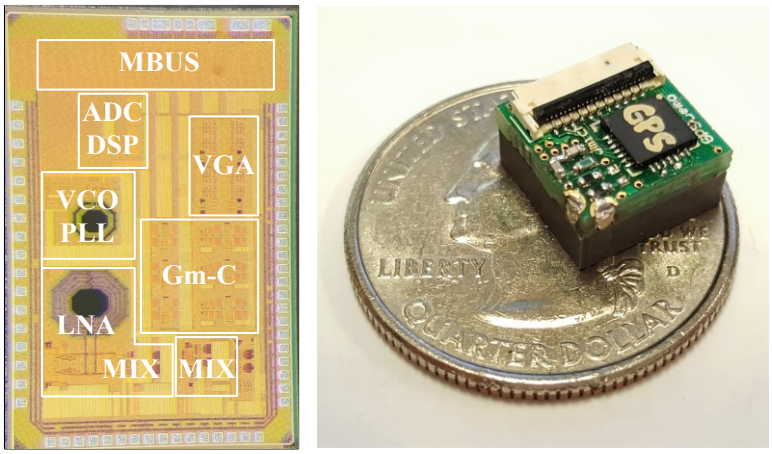
3.8 Conclusions

The fully integrated GPS logger co-designed receiver and antenna is presented. The proposed GPS logger has total volume of 10x10x6mm^3 while achieving 1.5mJ energy per fix. The GPS logger can sample 115K fixes from the 12mAh Li-ion battery before recharging. The flash is sufficient to hold ADC samples for 37 fixes before retrieval. After post-processing by streaming over 10ms, the 10dB SNR required for the GPS logger is -125dBm. In the sleep mode, the

processor and the timer only consume 50nW and in the active mode the total power jumps up to 12.5mW. The AFE is fabricated in a 65nm CMOS process and occupies 2.35x1.5mm^2. The die micrographs of the system and the photo of the proposed GPS logger are shown in Figure 3.13.

	This work	CICC 13 [45]	CICC 13 [46]	ISSCC 13 [47]	ISSCC 11 [48]	ISSCC 10 [49]	ISSCC 09 [50]
Application	GPS Logger	GPS receiver	GPS receiver	GPS receiver	GPS receiver	GPS receiver	GPS receiver
Captured time	10ms	Contiguous	Contiguous	Contiguous	Contiguous	Contiguous	Contiguous
System	GPS L1	L1/Compass /Galileo/ GLONASS	GPS L1	GNSS	L1/Galileo	GPS L1	GPS L1
RX NF (dB)	2.2	2.2	2.4	2.1	2.0	2.3	6.5
RF-IF Gain (dB)	72	64	>100	-	-	42	42.5
LO Phase noise @ 1MHz offset (dBc/Hz)	-115.6	-118	-115.8	-94	-118	-114	-110
1dB Gain de-sense @1710MHz blocker (dBm)	-6.1	-	-	-18	-	-15	-
System Integration	Complete GPS w/ Antenna	GPS AFE	GPS AFE	GPS AFE	GPS AFE	GPS AFE	GPS AFE
Power (mW)	12.5 (System)	31	41.4	20	18	23	7.2
AFE Area (mm^2)	3.52	10.5	1.2	0.25	1.4	2.5	3.05
Technology	65nm CMOS	65nm CMOS	55nm CMOS	40nm CMOS	65nm CMOS	65nm CMOS	130nm CMOS

Table 3.2 Measurement summary and performance comparison



(a) (b)

Figure 3.13 (a) Die micrograph of the system (b) Photo of the proposed GPS logger

Chapter 4 A Tri-band GPS Receiver in 65nm CMOS

This chapter presents a quadrature fully integrated tri-band GPS receiver implemented in 65nm CMOS. This GPS analog front-end (AFE) is specifically designed for receiving the GPS tri-band signals by using passive mixers. The main contribution of the RF front-end is comprised of a signal path which support the tri-band mode (L1, L2, L5) which can be sampled the three bands onto a single IF channel simultaneously. The AFE is able to fold the tri-band GPS signals onto a low-IF thanks to the orthogonality of the pseudo-random (PRN) codes. The radio draws 9.6mW from a 1.2V/1.4V supply, with a passive RF front-end and a startup time of 20μs. The measured conversion gain and noise figure are 59.3dB and 0.7dB including external LNA. The receiver is implemented in a standard 65nm CMOS process occupying 2x1mm^2 by the core circuitry.

4.1 Introduction

The proliferation of location-based applications in the Internet of Thing (IoT) increases the demand for GPS tracking systems with low-power consumption, small form factor and higher position accuracy [51]-[52]. This recent large demand and potential market of GPS tracking systems is driven by location based services (LBS) applications such as smartphone, health-tracking wearables, drone, asset tracker and security systems. Despite the interest in GPS tracking systems with small form factor and low-power consumption, one of their main limitations is reliable visibility of satellites.

Band	L1	L2	L5
Frequency (MHz)	1575.42	1227.60	1176.45
Bandwidth (MHz)	2.046	2.046	20.46
Modulation	BPSK	BPSK	BPSK
Code Frequency (MHz)	1.023	10.23	10.23

Table 4.1 Summary of the tri-band GPS signals

The GPS tracking system determines the absolute location, time information and derived velocity from the GPS signals including ranging signals and navigation messages, and it requires at least four satellites for obtaining this information. However, the received GPS signals are buried under the thermal noise floor. To retrieve the navigation message, a significant amount of correlation is performed in the baseband processor. The spreading of the GPS signal by the PRN code not only distinguishes each signal from the others, but also protects against interference (or other bands). Immunity against interferences is highly dependent on the processing gain of the system. The higher the processing gain, the wider the GPS signal is spread. By spreading the signal over a wide bandwidth, only a fraction of the desired signal can be corrupted by narrow-band interference [53].

By utilizing spreading of the GPS signals, more satellites are visible at GPS multi-bands which enables faster signal acquisition, enhanced reliability, and greater operation range. Prior published multi-band GPS receivers require additional channels or need to select one band at a time which leads to higher energy consumption to cover all 3 bands and increased design complexity [54], [55]. This works introduces a tri-band GPS receiver folding the three GPS bands (1.57542 GHz L1, 1.2276 GHz L2 and 1.17645 GHz L5), listed in Table 4.1, into a single low-IF so that they can be sampled simultaneously by a single baseband path. This has minimal impact on the sensitivity

and increases the possibility of reception because the signals in different GPS bands are already below the thermal noise floor, and each transmission across the bands uses a unique pseudo-random (PRN) code. The PRN codes are highly orthogonal to one another, and therefore can be recovered in the digital domain after being folded on top of each other.

4.2 Overall System and Frequency Planning

The GPS AFE is specifically designed for supporting tri-band operation simultaneously and employs fully differential quadrature signals. A two-step down-conversion process with a passive front-end is used to fold the three GPS bands onto a single low-IF. The overall block diagram of the GPS receiver is shown in Figure 4.1. It includes two consecutive passive mixers, IF filter, a VGA, an 2-bit ADC, digital baseband with AGC loop, frequency synthesizer and MBUS serial interface. The entire receiver employs fully differential quadrature signals. The RF front-end is comprised of two passive mixers and adopts a dual down-conversion architecture. The following

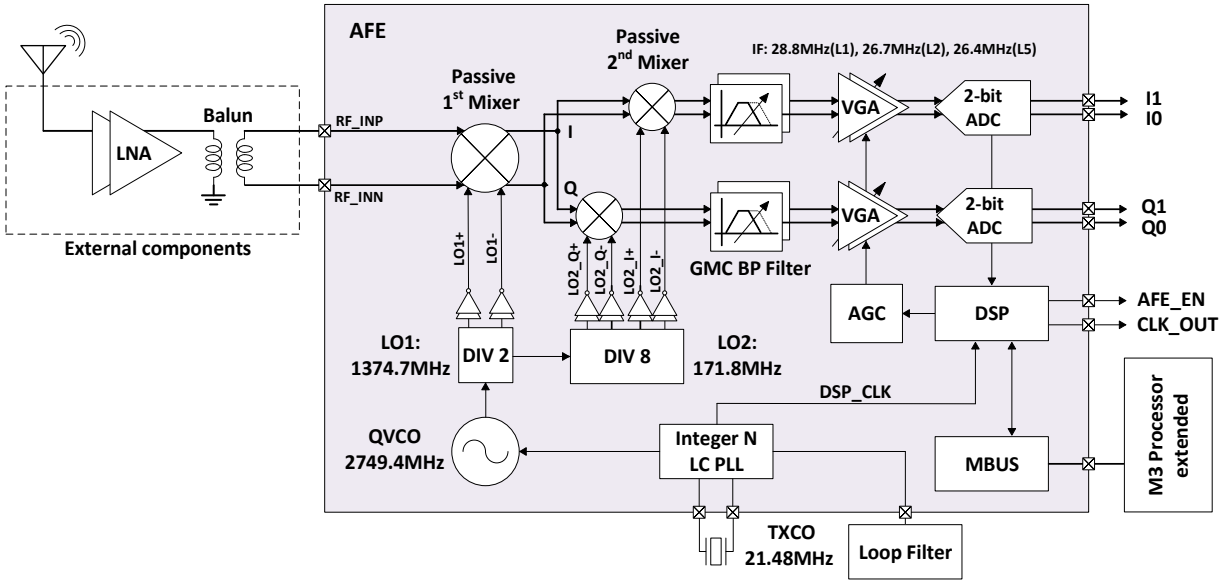


Figure 4.1 Overall block diagram of the GPS AFE

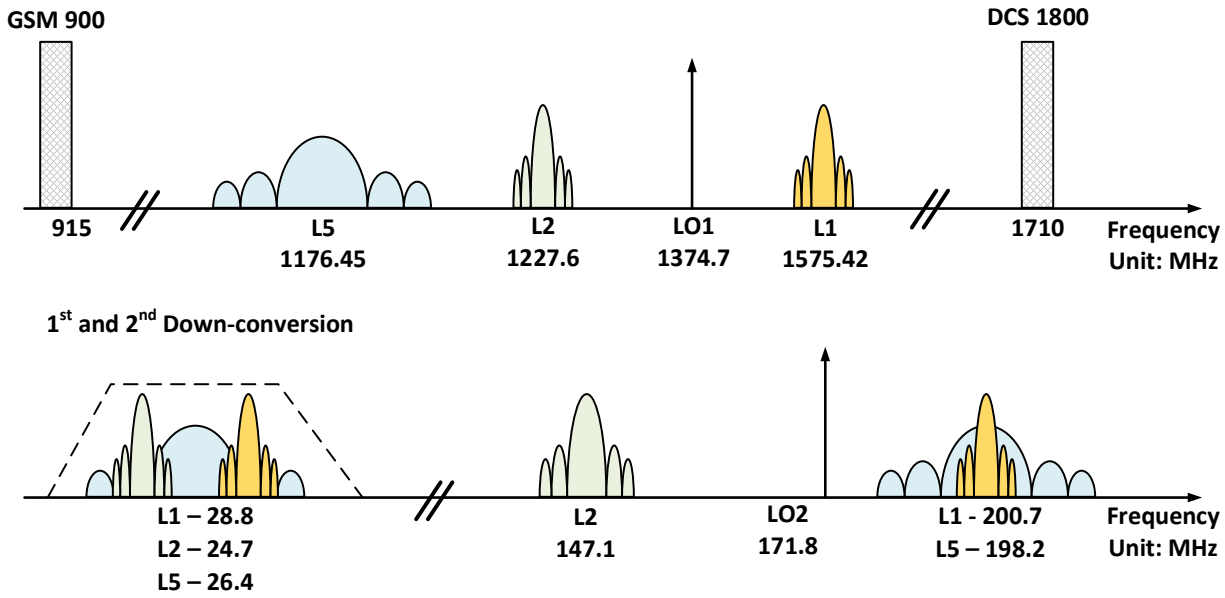


Figure 4.2 Spectrum allocation for GPS bands

IF chain performs filtering and amplification at low IF. The AGC (automatic gain control) loop controls the amplification of VGA based on the histogram of the ADC codes to keep the signal strength at the ADC input. The ADC quantizes in 2 bits outputs of I/Q and the sampling rate is 57.2MHz. The I/Q differential LO signals are generated by the frequency synthesizer with the Integer-N PLL. The MBUS and DSP blocks are always-on, while the rest of blocks are in stand-by mode until receiving an enable signal from the off-chip correlator.

Figure 4.2 illustrates the frequency plan for the dual down-conversion receiver in the tri-band. The LC VCO oscillates at 2749.4MHz which is 2x frequency of LO1 (1374.7MHz). The LO1 is divide by 8 to select the appropriate LO2 (171.8MHz) so that could fold the three bands into a single IF. This results in IF frequencies of 28.86MHz, 24.72MHz and 26.42MHz for L1, L2 and L5 bands, respectively. Note that in tri-band mode, L1 and L2 both fold onto the wider L5 band, however because of the orthogonal PRN codes this has a minimal impact on the receiver sensitivity.

4.3 Circuit Design

4.3.1 RF Front-end

The RF signal path includes external LNA, balun, a differential passive mixer at the 1st down-conversion and an I/Q passive mixer, driven by a differential quadrature LO2, performs the 2nd down-conversion to IF2 as shown in Figure 4.3. The voltage-driven passive mixer is implemented to save the power of the transimpedance amplifier (TIA). Two consecutive I/Q passive mixers and external wideband LNAs are used because of the wide RF bandwidth needed to capture all three bands. A tunable RC bank filters out the interferers after the 1st down-conversion.

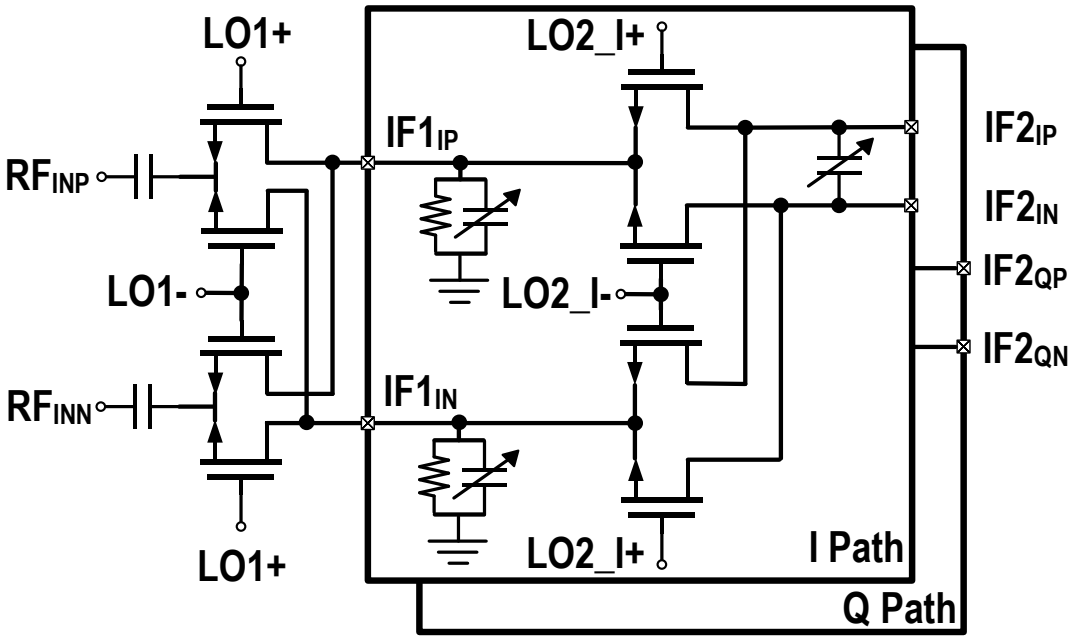


Figure 4.3 I/Q quadrature passive mixers at RF front-end

4.3.2 IF Path

As shown in Figure 4.4, the low-IF path is comprised of an IF filter and VGA with an AGC loop. The IF filter consists of 3 stages of fully-differential biquads and its output could be selected between the band-pass or low-pass outputs. The long channel NFETs, M3 and M4, provide common-mode feedback. At each gm stage, there are 4-bits for gm tuning. The cut-off frequency and Q of the filter are determined by C1 and Gm4. The VGA has 4th-order gm-C stages and the gain is tuned by Gm1. The AGC loop is implemented in the controller, and regulates the 5-bits VGA control code of Gm1 based on a target sigma value of the histogram of ADC codes.

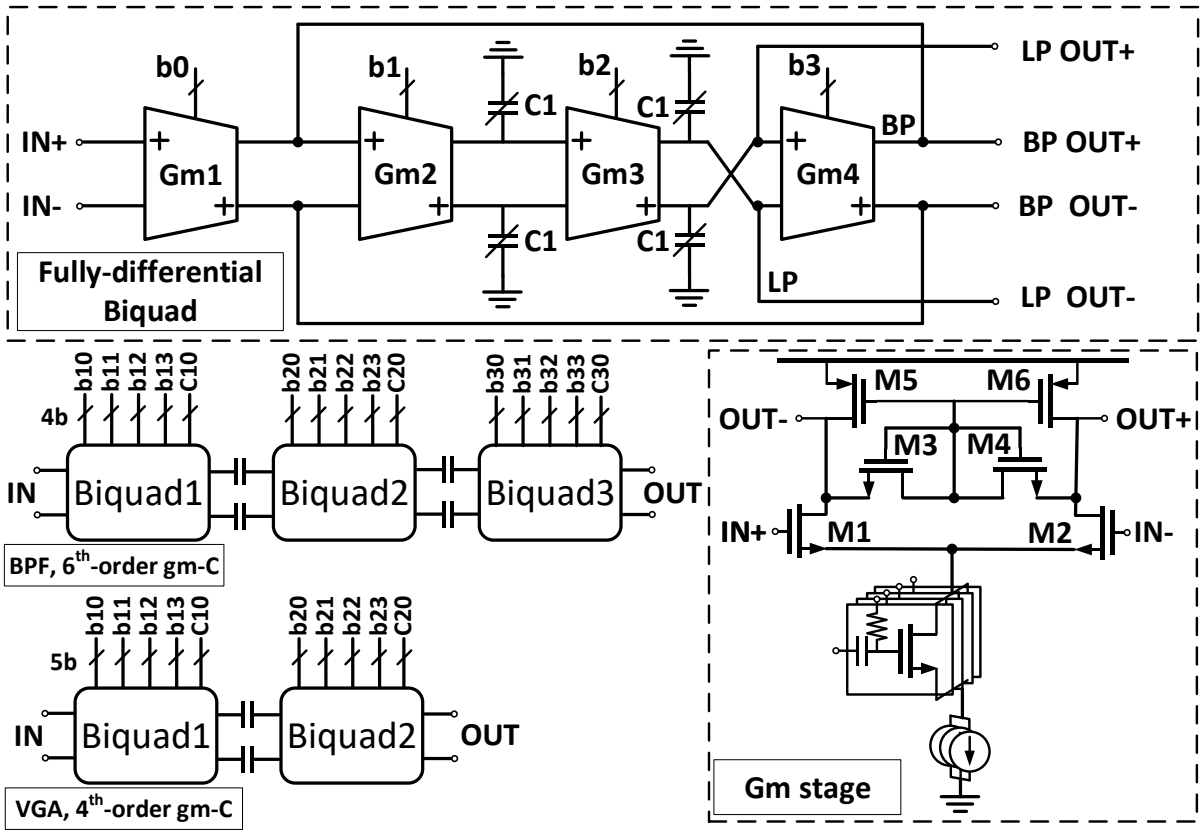


Figure 4.4 Simplified schematics of the IF path

4.3.3 Frequency Synthesizer

An integrated integer-N PLL is used to provide differential and quadrature signals, and the LO2 frequency is selected through a divider to enable simultaneous reception in tri-band. The differential LC VCO oscillates at 2.749GHz, twice the LO1 frequency, for improved inductor Q and providing IQ differential LO signals. The LO signal is divided further to provide the sampling clock for the ADC and DSP. It has an external loop filter with 100kHz bandwidth and a reference clock frequency of 21.48MHz.

4.4 Measurement Results

The quadrature fully integrated tri-band GPS receiver is implemented in a 65nm CMOS process and packaged in a QFN 64 package. The AFE is able to fold the GPS tri-band signals into one channel simultaneously. The IF frequency for L1, L2 and L5 bands are 28.8MHz, 24.7MHz and 26.4MHz, respectively. The Figure 4.5(a) represents the measured IF frequency response and the 3dB bandwidth is ~10MHz from 21MHz to 31MHz which cover all bands effectively. The output spectrum with a -100dBm input signal of three bands is shown in Figure 4.5(b).

The GPS receiver draws total power of 9.6mW and the AFE only consumes 3.5mW. The AFE achieves a maximum conversion gain of 59.3dB, a noise figure of 0.7dB including external LNA. The measured phase noise of the VCO achieves -86.7dBc/Hz at 100KHz and 114.9dBc/Hz at 1MHz offset frequency from the LO1 frequency at 1374.7MHz. The VCO ensures sufficiently fast turn on time of 20μs.

A custom GPS PRN sequence was implemented to evaluate the performance of the integrate AFE by running the off-line GPS signal correlation of captured ADC samples. The off-line correlation is performed in Matlab where the captured ADC sample sequence is correlated with

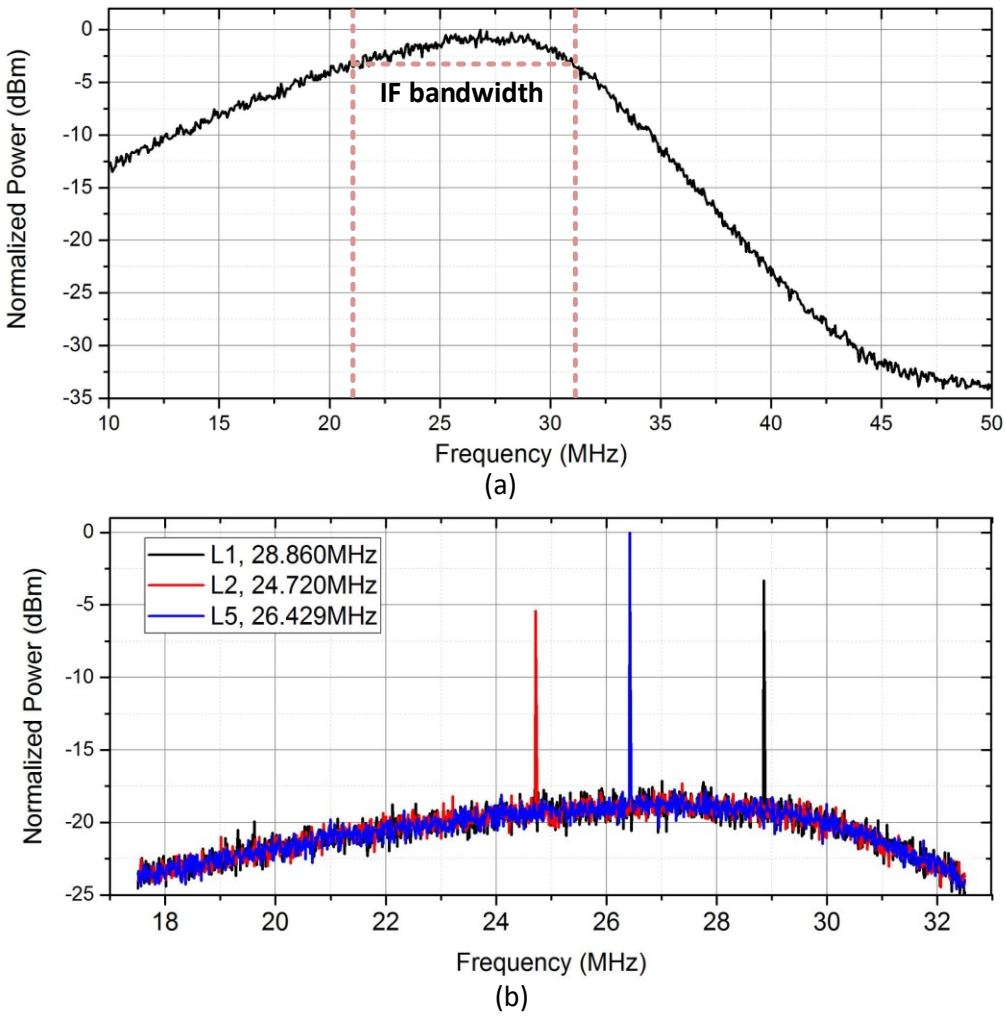


Figure 4.5 (a) IF frequency response (b) IF output spectrum with input power of -100dBm at L1/L2/L5

the expected PN sequence of the actual GPS satellite signal. The analog and digital output signals for both I and Q channels are captured at the sampling rate of 57.2 MHz in 50ms. The correlation length for the PN sequence is 1023 chips. Therefore, the maximum processing gain attainable for the post-processing SNR is 30dB. The results of the post-processing SNR after the correlation is shown in Figure 4.6(a). The intentional narrowband jamming signals are added for evaluating the AFE's resilience against interferences thanks to the orthogonal PRN codes. The SNR of L1 without narrowband jammer is ~13dB and, as shown in Figure 4.6(b), it is not degraded with a jammer 40 dB greater power. Exceeding the level, the IF path got saturated by the jammer. Hence, the tri-

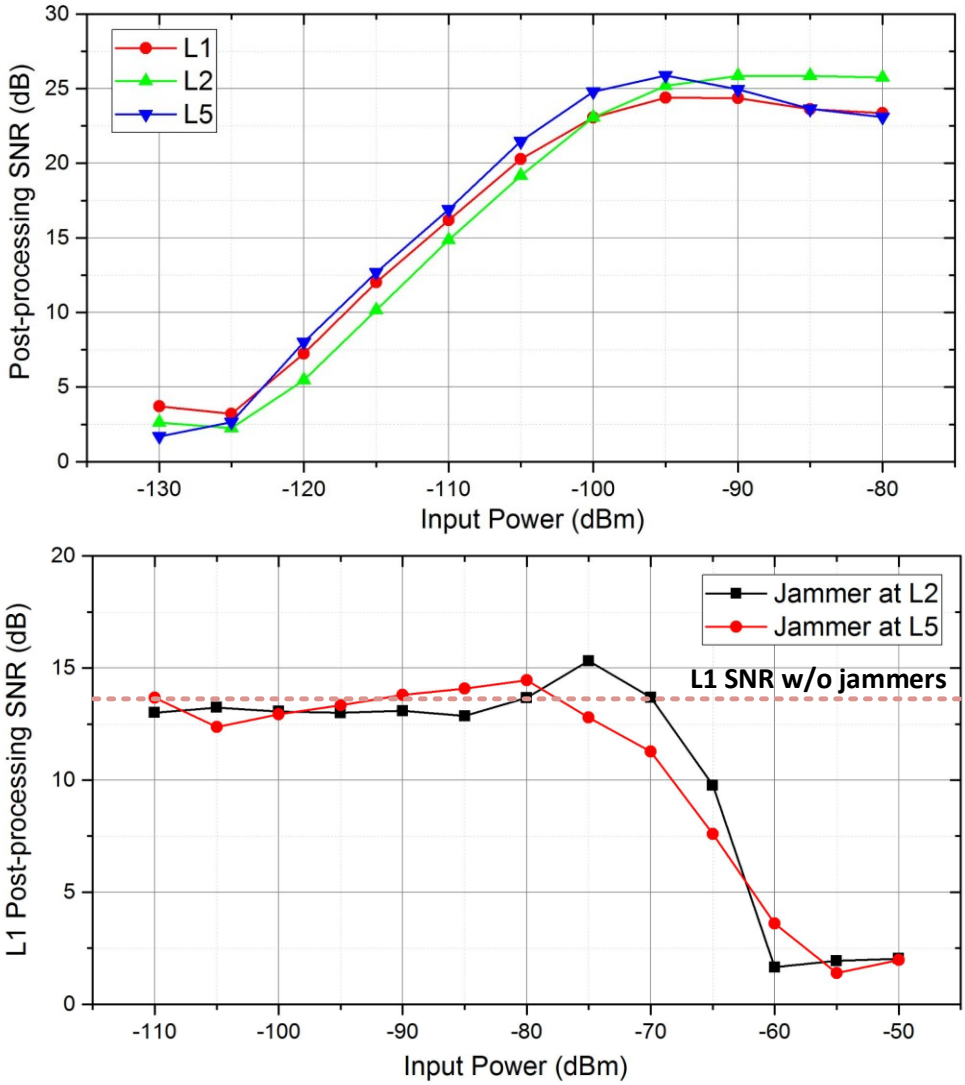


Figure 4.6 (a) Post-processing SNR in the tri-band L1/L2/L5 (b) L1 (at -115dBm) SNR variation with jamming signal at L2/L5

band folding has a minimal impact on the receiver sensitivity and enhance the signal acquisition. Table 4.2 summarizes the measured performance of the GPS receiver with comparison to the state of the art.

4.5 Conclusions

This paper describes a fully integrated tri-band GPS analog front-end receiver is fabricated in a 65 nm CMOS process. The energy efficient GPS AFE designed for extreme duty cycling to reduce average power with a startup time of 20us. The AFE supports the GPS tri-band (1.57542 GHz L1, 1.2276 GHz L2 and 1.17645 GHz L5) operation simultaneously and all three bands share one IF channel. the receiver dissipates 9.6mW with a passive front-end with a 1.2V/1.4V supply. It exhibits a conversion gain of 59.3dB and a noise figure of 0.7dB including the external components. The die area of the GPS receiver (including bond pads) is 2.35x1.5mm^2, of which 2x1mm^2 is occupied by the core circuitry.

Multiband GNSS RX	This work	JSSC05 [54]	ESSCIRC13 [55]	ESSCIRC13 [56]	ISSCC13 [57]	ISSCC11 [58]
System	GPS L1/L2/L5	GPS L1/L2	GPS L1/ Compass B1	GPS L1/ Compass B1/ Galileo E1/ GLONASS L1	GPS L1/ Galileo	GPS L1/ Galileo
# of concurrent RF channel (IF path)	3 (1)	2 (1)	2 (2)	2 (2)	2 (1)	2 (1)
IF Frequency(MHz)	28.8/24.7/26.4	1.279	4.092/10.23	3.9-13.29	4.092-13.1	4.092
RX NF (dB)	0.7(Rx)/17.1(chip)	8.5	1.8	2.5	2.1	2.0
RX-IF Gain (dB)	59.3(Rx)/29.7(chip)	95	110	64-125	-	-
LO Phase noise @ 1MHz offset (dBc/Hz)	-114.99	-109	-112	-115.23	-94	-118
Power consumption (mW)	9.6	19	24	41.4	20	18
Chip Area (mm²)	3.52	2.6	2.1	7.2	6.4	1.4
Technology	65nm CMOS	180nm CMOS	55nm CMOS	180nm CMOS	65nm CMOS	65nm CMOS

Table 4.2. Measurement summary and performance comparison

Chapter 5 A 60-GHz Band Integrated Slot Loop Antenna and Field Distribution in 0.13-µm BiCMOS

This chapter presents an integrated rectangular slot loop antenna in a standard 0.13-µm BiCMOS technology. By using the complementary structure of loop antenna, the slot loop antenna can easily satisfy the metal density rules without dummy metal fill and does not necessary the keep-out region (except the slot area) which integrate with a circuitry. The loop antenna only occupies 0.24mm^2 and the total area of the antenna including the ground plane is 0.883mm^2. Furthermore, the field distribution of the antenna is analyzed to present its resonance characteristic as a frequency reference. From the measurement, the antenna resonates at 59.2 GHz and the bandwidth at VSWR 3.0 is 2.77 GHz from 57.95 GHz to 60.72 GHz with 300-ohm load.

5.1 Introduction

The 60-GHz band, a global unlicensed band at 57-64 GHz, has a wide spectrum of up to 9 GHz and four allocated bands of 2160MHz bandwidth. In recent year, the wireless communication at the 60-GHz band has become more interested thanks to its spacious and uncongested spectrum availability compared to other public bands [59]-[62]. In particular, the propagation characteristics of the 60-GHz band provides the promise of high spatial frequency reuse with low-power transmitters [63]. As shown in Figure 5.1, over-the-air (OTA) transmission losses at 60 GHz is greater due to absorption of the radio signal by water vapor (H_20) and oxygen(O_2), therefore, short propagation distance [64]. Although the absorption reduces the communication distance, the

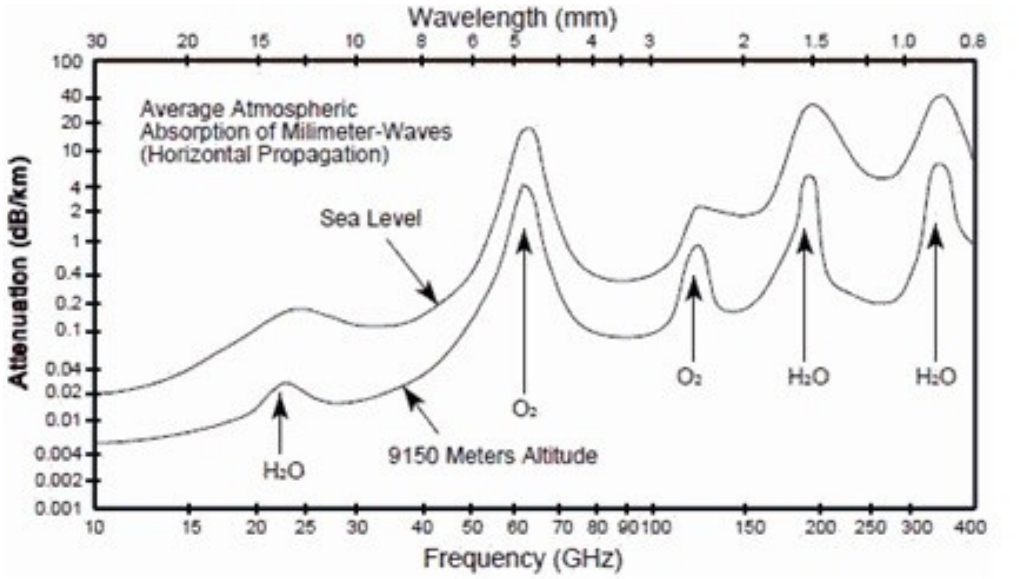


Figure 5.1 Atmospheric absorption of millimeter waves [64]

absorption peak around 60-GHz gives high security and interference resistance so that make the 60-GHz band suitable for the application of low power indoor networking system [61]-[62].

There is a growth demand for integrated antennas for wireless personal area networks (WPANs) thanks to its wide bandwidth, high capacity, and interference resistance [9]-[13], [65]-[68]. Implementation of an integrated antenna in a CMOS standard process are particularly beneficial for mm-scale wireless sensors used in short-range IoT applications [69]-[70]. If these devices integrate all components of a sensor node into a cubic-mm volume, a great deal of cost savings would be realized. The design of integrated antennas for the more typical <10GHz ISM bands at mm-scale often result in <1% radiation efficiency. Therefore, the 60GHz band tends to be a better match for the size of these devices. The integrated antenna at mm-scale which has moderate gain (~0dBi) and broad beamwidth would be suitable for this application.

For mm-scale wireless sensor nodes, having the antenna integrated in a CMOS process along with the RF circuits enables compact, low-cost, and short-range wireless communication. However, an on-chip antenna co-designed with the circuitry must conform to the CMOS design

rules, in particular meeting metal density rules. This can be problematic for many antenna designs that use large blocks of metal, such as patch, or large open areas without metal, such as a loop and a monopole [9],[12],[13]. For example, if the antenna is designed either under or over density, dummy metal fill or metal slots must be added in and around the antenna, which inevitably degrades antenna performance. This work presents a slot loop antenna which can easily satisfy the density rules without requiring dummy metal fill, which can also be integrated with other active circuits underneath the antenna except the slot area.

5.2 Comparison Loop Antenna and Slot Loop Antenna

The loop antenna is one of the popular type of the antenna because of its simplicity in design and versatile design such as rectangle, triangle, and circle. In 60-GHz band, the size of the loop tends to be mm-scale so that easily implement for low profile applications. The loop circumference are the main factors to determine its far-field function and directivity. The equation (2) shows the radiated power and radiation resistance of the large loop antenna. ($C \geq \lambda/2$) [71]:

$$P_{rad} = \frac{\pi(a\omega\mu)^2|I_o|^2}{4\eta(ka)} \qquad R_r = \frac{2P_{rad}}{|I_o|^2} = 60\pi^2\left(\frac{C}{\lambda}\right) \qquad (2)$$

where I_o is the current distribution, a is the radius of the loop, C is the circumference of the loop.

When the *ka* (=C/λ) is <0.1, it is a poor radiator due to small radiation resistances. The directivity versus the circumference of the loop is shown in Figure 5.2. In order to achieve positive gain, the circumference need to be larger than ~ 0.5 λ. An electrically small loop antenna has same radiation pattern as an infinitesimal magnetic dipole.

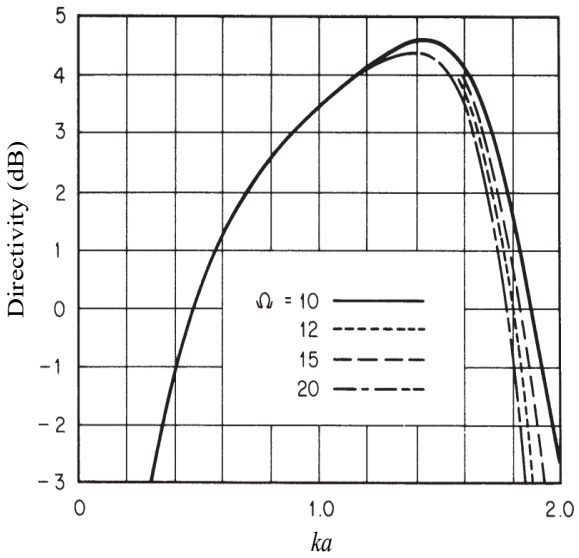


Figure 5.2. Directivity of circular-loop antenna for θ=0 [71]

The Figure 5.3 represents input impedance of square-loop antenna on 130nm BiCMOS. The loop antenna has resonances around 0.5 λ, 1 λ and 1.6 λ. The simulated total gain at 0.5 λ and1 λ is -1.63 dBi and 1.53 dBi, respectively. The resonance at 0.5 λ has the highest impedance and narrow band contrast to the one at 1 λ which has low impedance and gradual slope in resistance

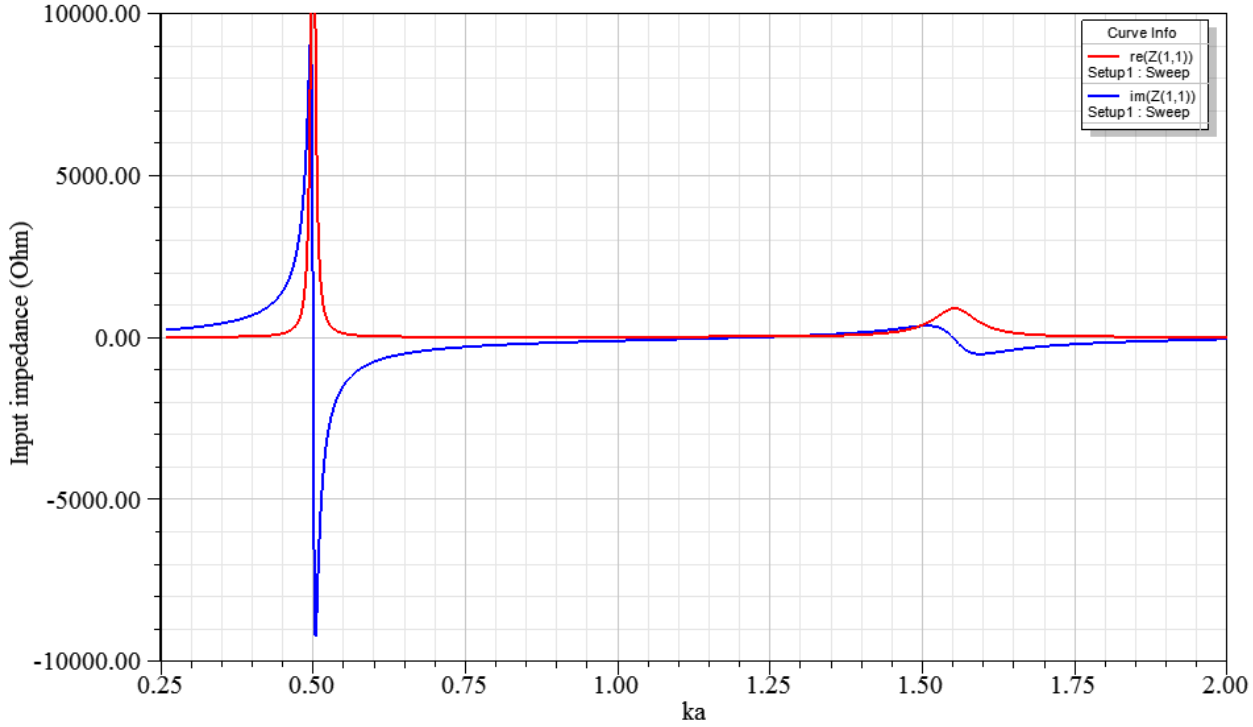


Figure 5.3 Input impedance of loop antenna on 130nm BiCMOS

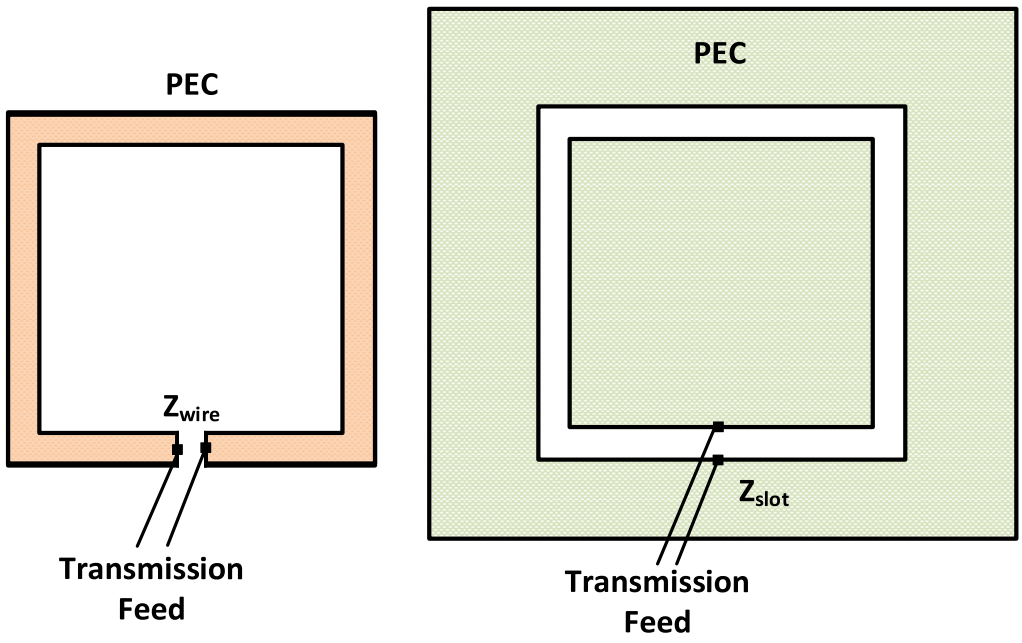


Figure 5.4 Loop antenna and its complemenrary slot loop antenna

and reactance. To cover spacious frequency spectrum of 60-GHz, the circumference of loop antenna is desired to be around 1 λ. However, the resistance at the resonance is ~ 20 ohm which is too low matching from the power amplifier output. To implement with circuitry at the 60-GHz band, the antenna with high input impedance and wide bandwidth is necessary.

To find complementary impedance of the loop antenna, Babinet's principle, which states the diffraction pattern from an opaque body is identical to that from a hole of the same size, can be used. Figure. 5.4 shows the complementary structure of the loop antenna. The relationship between the wire and slot antenna as shown in equation (3) [72].

where Z_{wire} and Z_{slot} are input impedance of wire and slot antenna, and η is the intrinsic

$$Z_{wire}Z_{slot} = \frac{\eta^2}{4} \tag{3}$$

impedance of the media. The slot loop antenna can be made to resonate by choosing the dimension of the complementary structure which is loop antenna. The radiation pattern of the slot loop antenna is identical to the loop antenna except that E and H-field are interchanged.

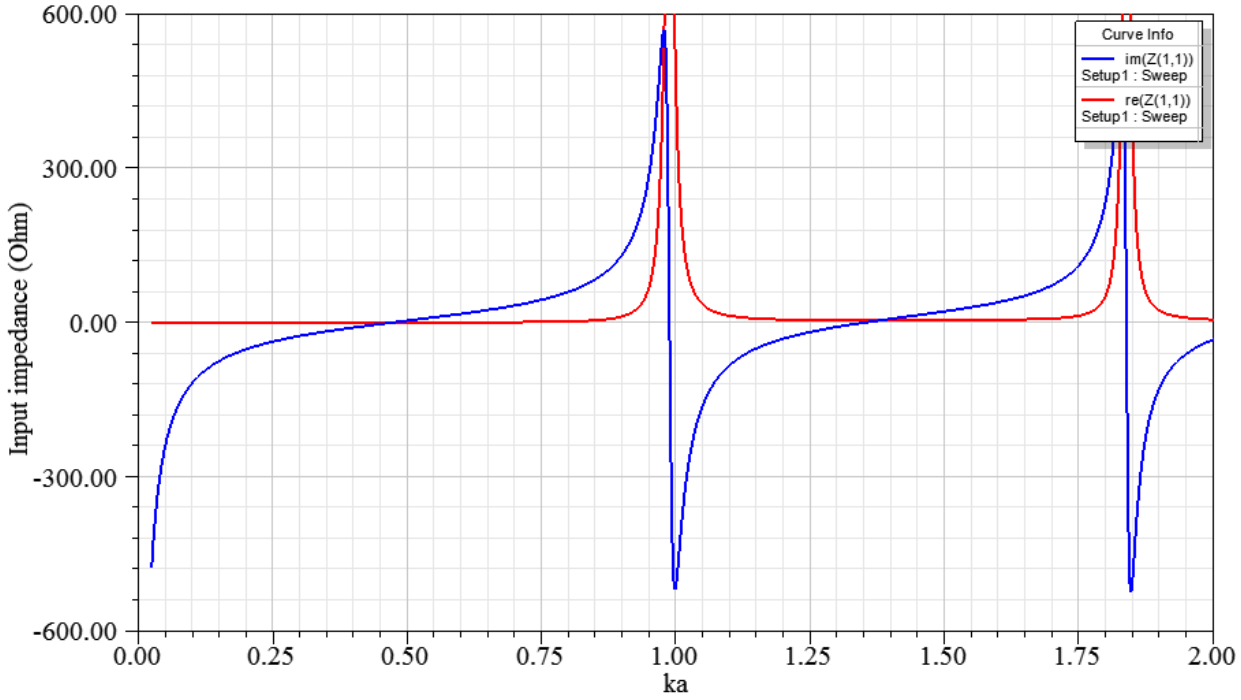
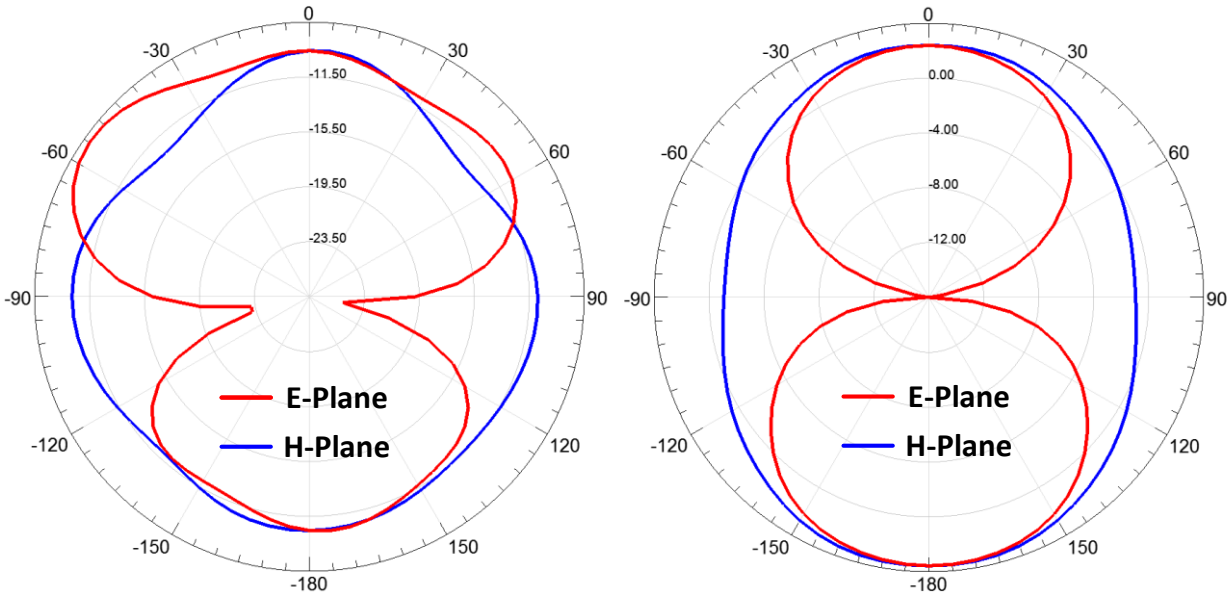


Figure 5.5 Input impedance of slot loop antenna on 130nm BiCMOS

The input impedance of the slot loop antenna with finite conductor and substrate is shown in Figure 5.5. By comparing the impedance with Figure. 5.3, the resonance at 0.5 λ change to low impedance and the one at 1 λ become high resistance around 500 ohms. The simulated total gain



(a) 0.5 λ **(b) 1 λ**

Figure 5.6 The radiation pattern (a) C = 0.5 λ , (b) C = 1 λ

at 0.5 λ and 1 λ is -7.8 dBi and 3.56 dBi, respectively. The total gain at 0.5 λ has degraded from wire to slot type antenna, because of finite the outer metal plane and substrate in mm-scale application. The radiation pattern is plotted in Figure 5.6. Thanks to its high impedance and wide bandwidth, the slot loop antenna is beneficial to use as an integrated antenna with the circuitry. As another advantage of the slot type antenna, it can be fabricated and concealed it within metallic objects which could be power or ground plane in circuit design. Once the circuit is carefully designed along with the slot, the antenna can be incorporated efficiently with the active devices without degradation.

5.3 Field Distribution of Loop Antenna and Slot Loop Antenna

The field distribution of a loop antenna can be analyzed using a short transmission line model which has a length of λ/2. As shown in Figure 5.7(a), the λ/2 short transmission line has a zero E field and maximum H field at the end and maximum E-field and peak current at λ/4. In standing

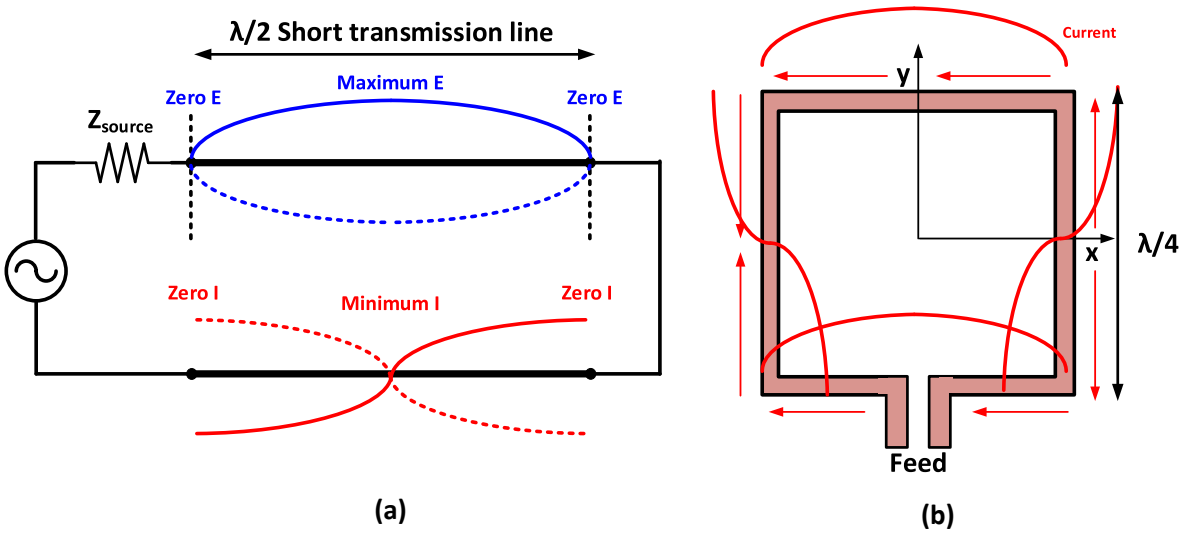


Figure 5.7 (a) Voltage and current distribution of λ/2 short transmission line, (b) Current distribution loop antenna (C = 1 λ)

wave, the null point of the standing wave where the incident and reflected waves cancel each other never change position. The field distribution of the loop antenna (C = 1 λ) is identical with the λ/2 short transmission line (Figure 5.7(b)).

Figure 5.8 represents the E-field distribution of the integrated loop antenna (1mm x 1mm) within $2mm^2$ substrate in standard 130nm BiCMOS processes. As similar as Figure 5.7(a), the shorted end always has a null of E-filed, then peak and null of E-field appear consecutively in every λ/4. However, the second null of the loop (C = λ) does not appear clearly, due to the fringing field at the feed (Figure 5.8(b)). When the C > λ, the second null is conspicuous. This null

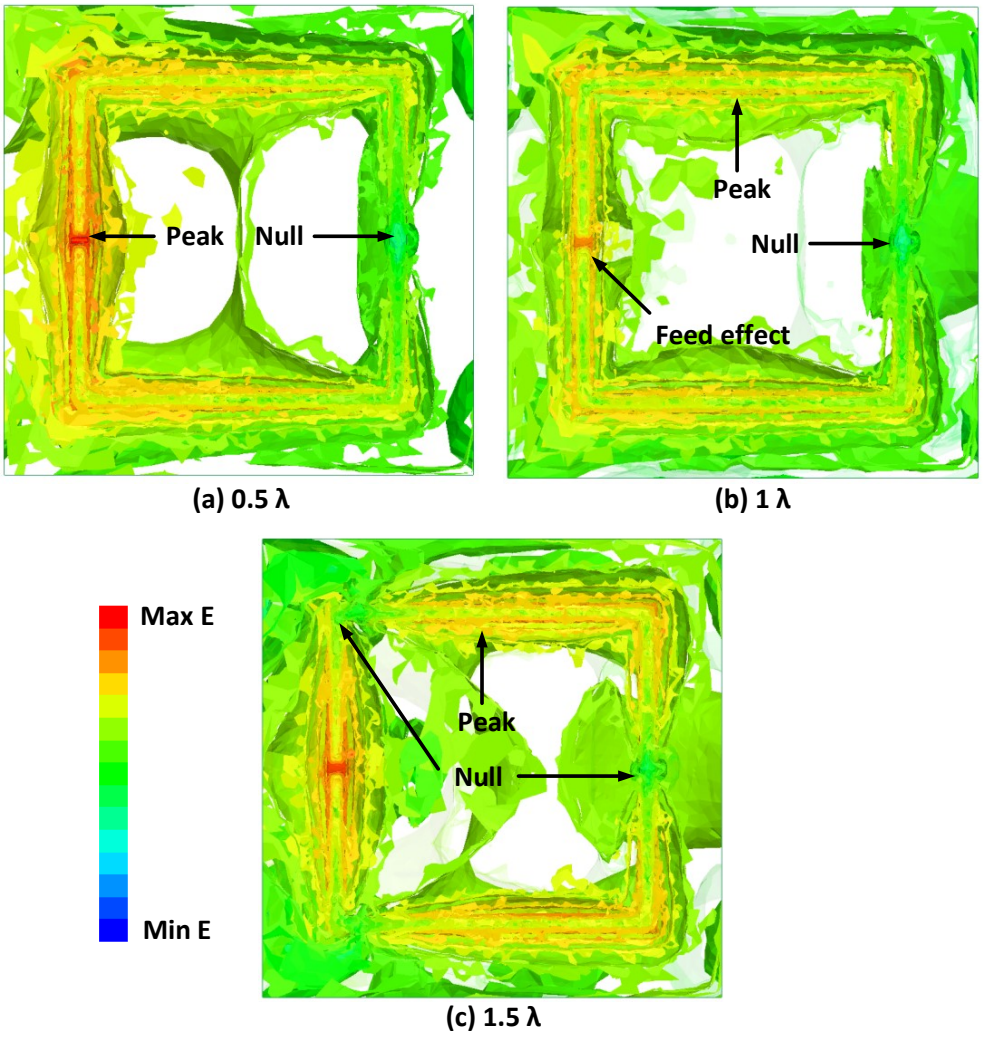


Figure 5.8. E-field distribution of the loop antenna (a) C = 0.5 λ (b) C = 1 λ (c) C = 1.5 λ

movement is unique characteristic mainly depending on the size of the loop so that could be a candidate as a reference resonator for replacing timing device.

Figure 5.9 shows the E-field distribution of the slot loop antenna with same conditions as loop antenna, but only its complementary structure. The E and H-field of a slot loop antenna and a loop antenna are interchanged and the radiation pattern is identical. Contrary to the loop antenna, the shorted end always has a peak of E-filed, then null and peak of E-field appear consecutively in every λ/4. The moving null appears around feed when C > 0.5 λ and it moves linearly to the shorted end by increasing the circumference of the slot loop up to 1 λ. After that, the movement is gradually

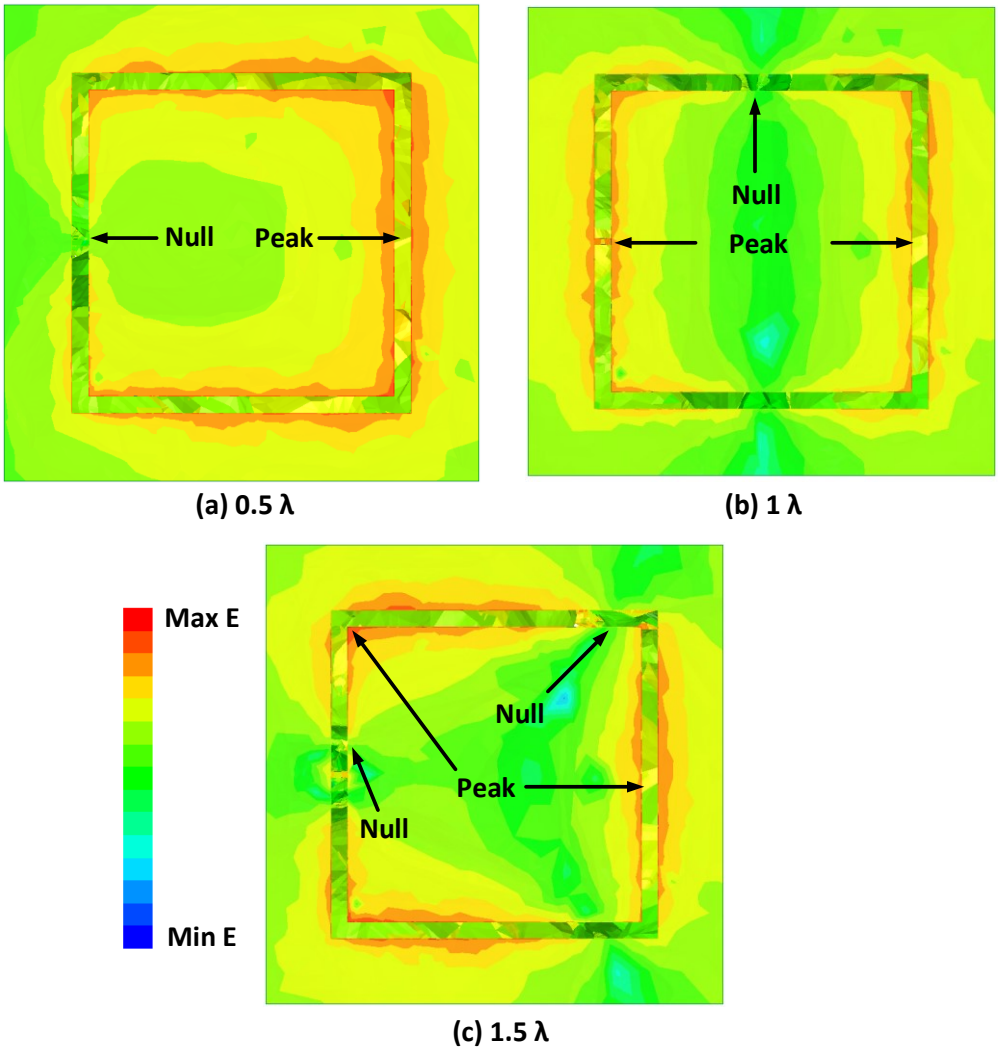


Figure 5.9 E-field distribution of the slot loop antenna (a) C = 0.5 λ (b) C = 1 λ (c) C = 1.5 λ

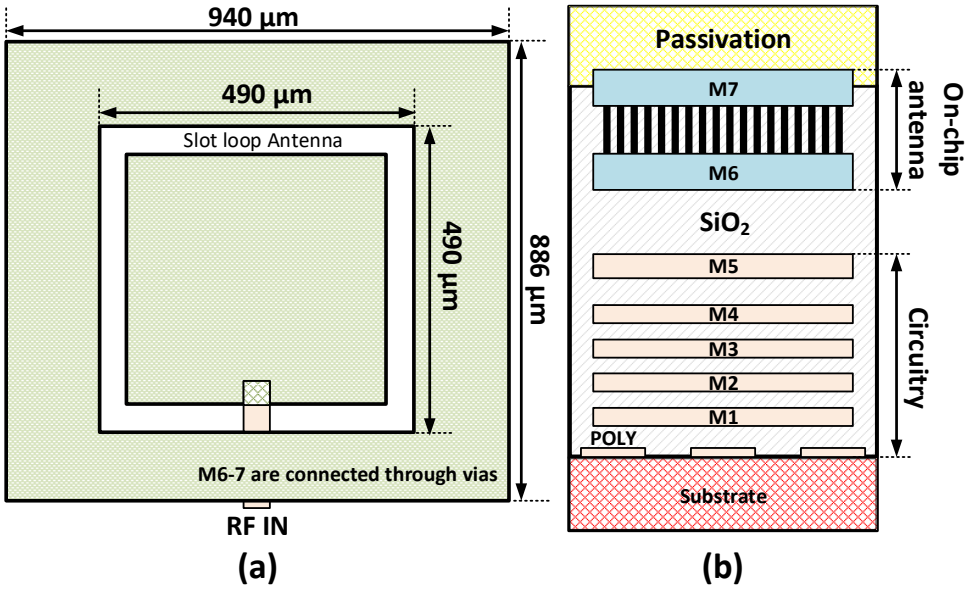


Figure 5.10 (a) The designed 60-GHz on-chip slot loop antenna, (b) cross section view in a standard 0.13-µm BiCMOS process

slow down and it would no longer move linearly (Figure 5.9(C)). For these reasons, the ideal circumference of the slot loop for null detection would be in a range of $0.5\ \lambda < C < 1\ \lambda$. Compared to the loop antenna, the slot loop can be more effective design to detect the null movement thanks to its smaller size and less interference with fringing field at the feed.

5.4 Slot Loop Antenna Design

Figure 5.10(a) shows the geometry of a slot loop antenna using the layer profile of 0.13-µm BiCMOS technology. The loop antenna is designed on the two top metals (M7 and M6) in a dimension of 0.883 mm^2 including the ground plane. The size of the loop antenna is only 0.24 mm^2, 490 µm x 490 µm, which corresponds to 0.098 λo at each side (Figure 5.11). The two layers are connected using an array of vias for better reliability and for reducing the conductor loss (Figure 5.10(b)). The center frequency of the antenna is mainly determined by the dimension and gap of the loop. The tolerance of the conductor is one of the limitations impacting variation of the

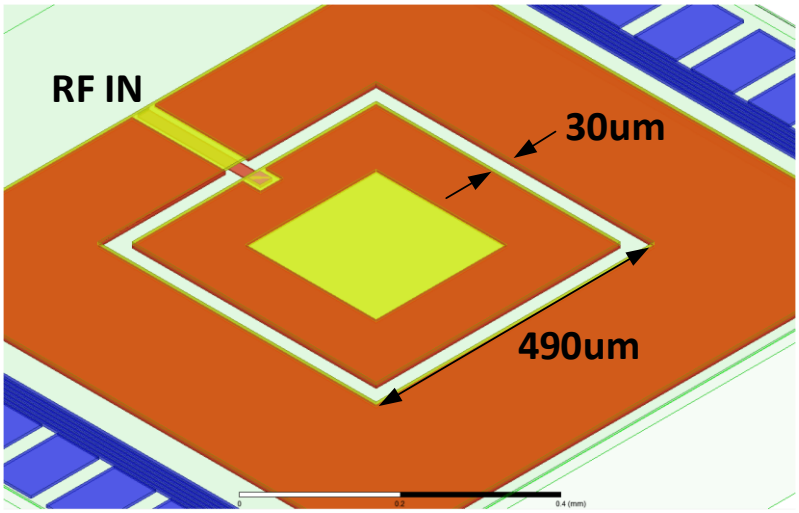
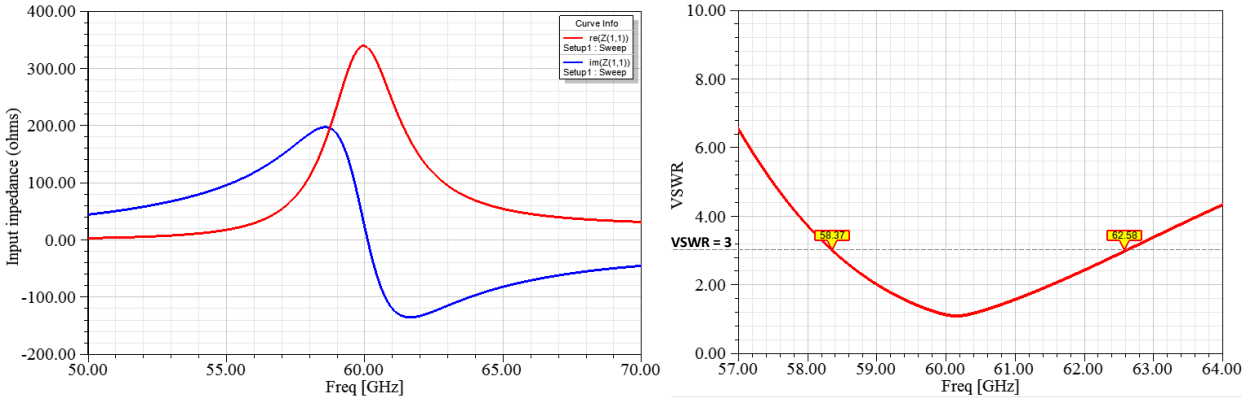


Figure 5.11 A 3-D EM simulation model of the slot loop antenna

center frequency. By connecting the top metal to the M6 layer, which has better tolerance, the frequency variation can be reduced.

This antenna is specifically designed for integration with the RF front-end and baseband circuitry. The baseband circuitry operating at a much lower frequency can be placed anywhere underneath the antenna except the slot loop area. The RF input of the antenna is directly connected to the power amplifier, and the input impedance is carefully designed including the feed line for accurate matching with it.



(a) (b)

Figure 5.12 (a) Simulated Input impedance of the slot loop antenna, (b) VSWR with 300 ohms input impedance

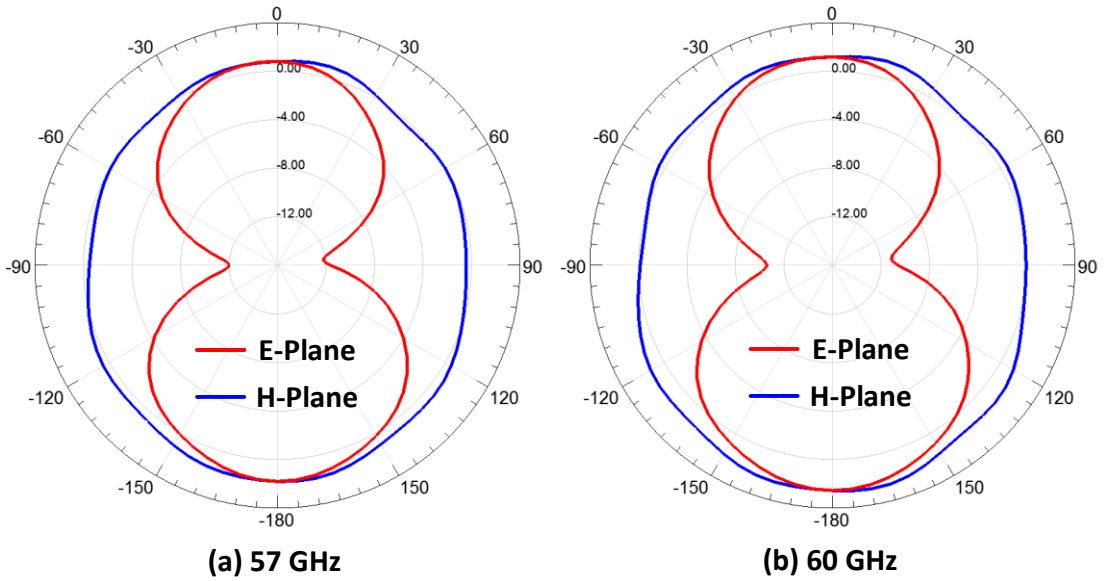


Figure 5.13 Radiation patterns (a) at 57 GHz (b) at 60 GHz

Figure 5.12 shows the input impedance of the slot loop antenna. The design is simulated and optimized in ANSYS Electronics Desktop. The antenna resonates at 60.0 GHz and the bandwidth (at VSWR 3.0) is 4.21 GHz from 58.37 GHz to 62.58 GHz. At the resonance frequency, the input impedance matches to a relatively high impedance of 300 ohms, which is designed intentionally to match with a power amplifier.

Figure 5.13 represents the radiation pattern at 57GHz and 60 GHz. The simulated peak gain at 60 GHz is 2.69 dBi, and the efficiency is 86%. In the 60 GHz band, 57-64 GHz, the radiation efficiency is better than 74% as shown in Figure. 5.14. This omni-directional radiation pattern and its high efficiency over the band make it suitable for the application of short-range communication systems.

Prior published integrated antennas are mostly designed as wire radiators, but their efficiency and bandwidth suffer due to the design limitations of standard CMOS technology, such as thin metal layers and, metal density rules, and coupling with other routes and circuitry [9]-[13]. By using the slot type antenna, the slot mainly radiates an electromagnetic wave and is not impacted

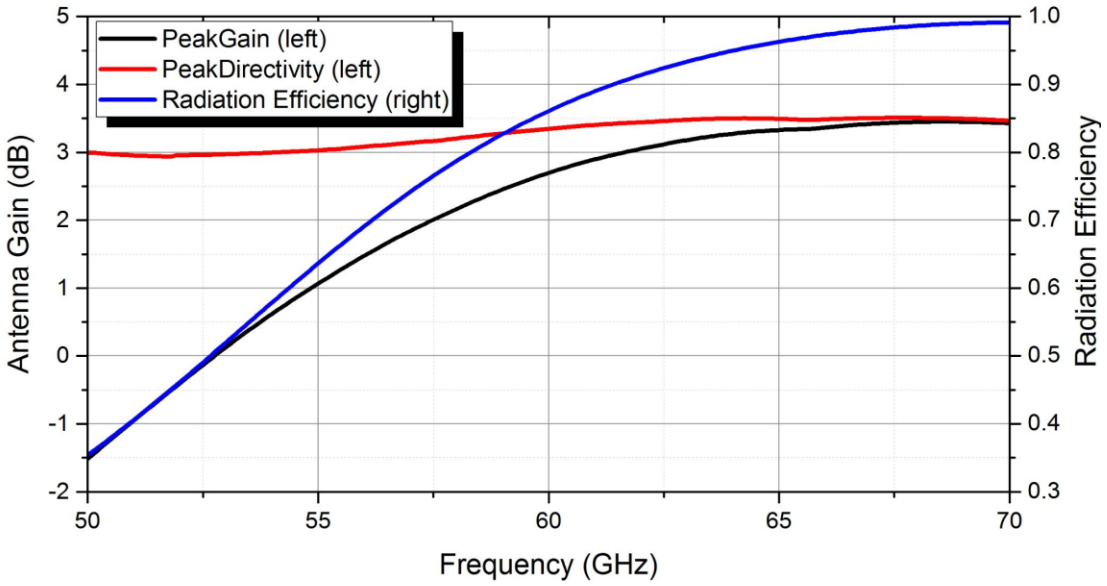


Figure 5.14 Simulated radiation performance; Peak directivity, peak gain and radiation efficiency

by design rules and coupling issues. The outer dimensions of the loop and the gap are controllable to satisfy the density rule, which eliminates unwanted metal filling dummy. However, because the slot radiates, the actives devices and routes need to be carefully designed near the slot area so that it does not degrade the radiation performance.

5.5 Measurement Results

The 60-GHz band slot loop on-chip antenna were performed at the probe station with the Infinity GSG probe (100um pitch), an Agilent E8361A vector network analyzer (VNA) and an Keysight E440A PSA spectrum analyzer. Figure 5.15 represents the measurement setup of the slot loop on-chip antenna. The on-chip antenna is placed on a probe station and fed through the microwave probe, which is connected to a 60-GHz millimeter-wave signal generator or vector network analyzer. The S-parameters with VNA were measured up to 67 GHz and the peak gain was measured with spectrum analyzer in V-band from 50 to 75 GHz.

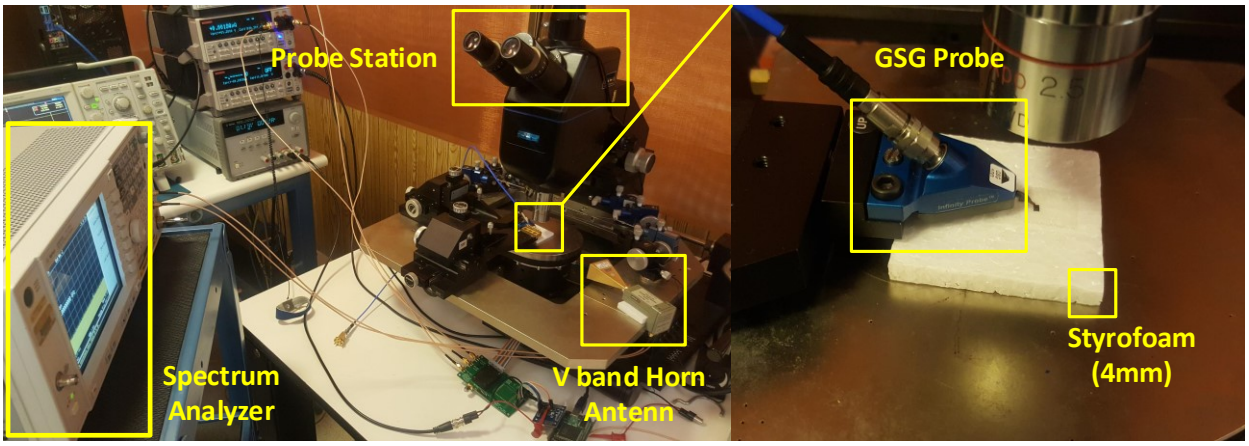


Figure 5.15 Slot loop on-chip antenna measurement setup

To rule out the radiation effect from the microwave probe, the radiation of the probe without any DUT has been measured over frequency for both polarizations in all three measurement planes to ensure that the main radiation comes from the on-chip antenna [73]-[74]. The measurement of the on-chip antenna at the probe station has several factors that could degrade the radiation performances. The probe station has consisted of lots of metal that could reflect the signal and generate multipath interference. Also, the accessories such as cable, connectors and probes could degrade the antenna characteristic. The performance of the antenna is quite susceptible to metal. Especially, when an integrated antenna is placed on the vacuum metal chuck at a probe station, the input impedance and radiation pattern would be changed significantly. To minimize the proximity effect from the metal chuck, a 4mm thickness Styrofoam is placed on top of the chuck which is could be separated by about one wavelength.

Figure 5.16(a) shows the measured input impedance of the slot loop antenna. The measured resonance frequency of the antenna is at 59.2GHz and the bandwidth at VSWR 3.0 is 2.77 GHz from 57.95 GHz to 60.72 GHz in Figure 5.16(b). Compared to the simulation results, the resonance frequency has shifted down from 60.0 GHz to 59.2 GHz and the bandwidth at VSWR 3.0 (300Ω load) got reduced from 4.21 GHz to 2.77 GHz. The variations of frequency and bandwidth are

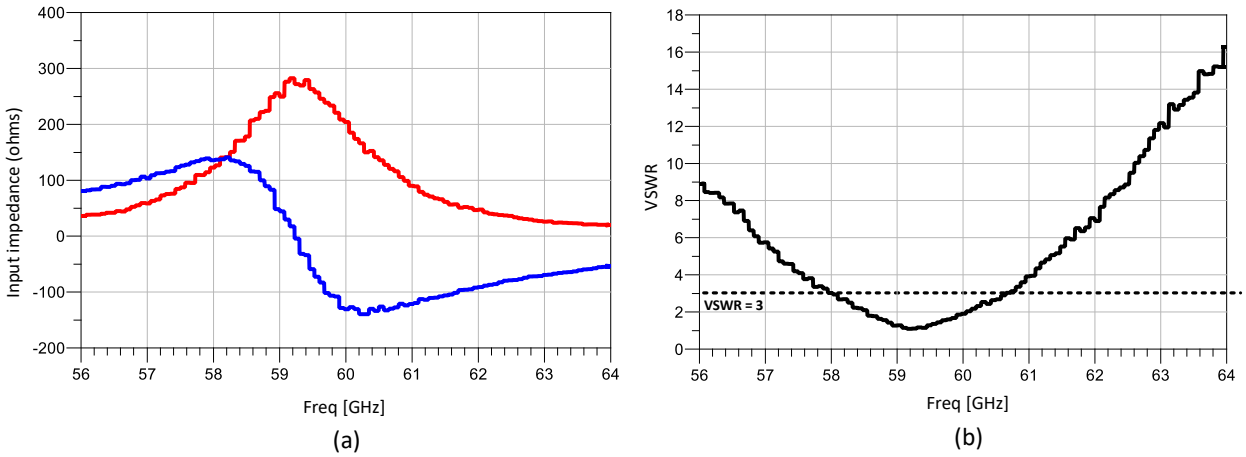


Figure 5.16 (a) Measured Input impedance of the slot loop antenna (b) VSWR with 300 ohms input impedance

mainly caused by the feed line which got extended by 400um in order to connect to the pad for the test purpose. This could add more inductance at the input of the antenna resulting in frequency shift and reduce the bandwidth. The peak gain of the antenna was measured by using the deembedding technique [75]. As a reference antenna, a V-band horn antenna with 23dBi gain is used. The losses from the cables, connectors, and probes had considered at calibration. The measured peak gain at 59 GHz is about 0dBi. Table 5.1 summarizes the performances of the integrated slot loop antenna with comparison to the state of the art.

5.6 Conclusions

The slot loop on-chip antenna is implemented using a standard 0.13-µm BiCMOS process. The chip micrograph of 60-GHz band transmitter is shown in Figure 5.21. The slot loop which in a range of $0.5\,\lambda < C < 1\,\lambda$ can be more effective design to detect the null movement thanks to its smaller size and less interference with fringing field at the feed. The slot loop antenna can easily satisfy the density rules without requiring dummy metal fill, which can also be integrated with other active circuits underneath the antenna. The antenna is beneficial for mm-scale wireless

sensors used in short-range IoT applications due to its wide bandwidth, high efficiency, and small area. The loop antenna only occupies 0.24mm^2 and the total area of the antenna including the ground plane is 0.883mm^2. The die micrograph of the slot loop antenna is shown in Figure 5.17.

Type of Antenna	Technology	Frequency	Antenna Gain	Antenna area	Chip area
Monopole [9]	0.13um CMOS	60 GHz	-9.4 dBi	0.81 mm^2	0.81 mm^2
Invert-F [10]	0.18um CMOS	60 GHz	-15.7 dBi	0.57 mm^2	0.57 mm^2
Yagi [11]	0.18um CMOS	60 GHz	-10.6 dBi	1.05 mm^2	1.05 mm^2
Patch [12]	0.13um CMOS	60 GHz	-3.32 dBi	1.92 mm^2	5.06 mm^2
Loop with AMC [13]	0.18um CMOS	65 GHz	-4.4 dBi	0.627 mm^2	3.24 mm^2
Slot Loop (This work)	**0.13um CMOS**	**60 GHz**	**0 dBi**	**0.24 mm^2**	**1.96 mm^2**

Table 5.1 Measurement summary and performance comparison

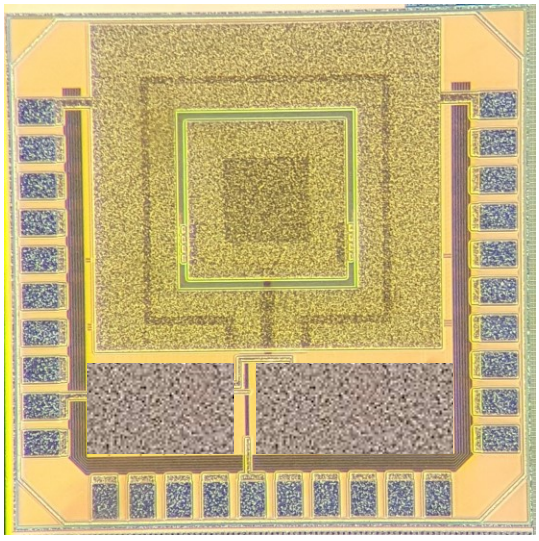


Figure 5.17 Chip micrograph of the slot loop antenna

Chapter 6 Conclusions and Future works

6.1 Conclusions

According to the Bell's Law, a new computer class advent approximately every decade as a new "minimal" computer either through using fewer components or use of a small fractional part of the state-of-the-art chips. The continual scaling of the size of computing systems has resulted in a diverse range of computing platforms. Nowadays, wireless sensor networks (WSNs) take center stage as the next trend of computing devices toward more compact, lower cost, more ubiquitous computing.

Today's wireless sensors are composed of multiple components such as microcontroller, power management, sensor, transceiver, timer/clock, battery, and antenna. These components tend to be COTS components, which could be bought individually then put together on a printed circuit board. It has a great advantage that could afford a designer flexibility but doesn't look like the new class of computer in future wireless sensor nodes. In most these applications, bulky battery and timing devices takes significant fraction of volume and the antenna sticks out at least several centimeters. The result is this system increases up to centimeters or tens of centimeters in at least one dimension. Due to these problems, the integration of battery, timing device and antenna are the major issues for realizing integrated cubic mm-scale wireless sensor nodes. This research has been focused to miniaturize the total volume of the WSN and to reduce the average power consumption that could survive with micro-battery.

In chapter 2, a 10.6mm^3 a complete, autonomous, wireless sensor node with 8GHz UWB transmitter has been demonstrated. The wireless sensor node is fully encapsulated with epoxy includes solar energy harvesting with an integrated 2μAh battery, optical receiver for programming, PMU, microcontroller and memory, crystal-less 8GHz UWB transmitter, and miniaturized custom antennas. The WSN operate autonomously from harvested energy, initially powered and programmed optically, and broadcast UWB messages of sensed data at a fixed period. The communication range for the dipole was 7 meters with a peak SNR of 10dB which the highest reported distance to volume ratio is. This system consumes only 8nA in sleep mode and 36 μA in active mode. Full, stand-alone operation was demonstrated for the first time for a system of this size and functionality.

In chapter 3, the fully integrated an ultra-low-power (ULP) GPS logger co-designed receiver and antenna is presented. A GPS logger system that features a custom miniaturized antenna co-designed with a GPS analog front-end (AFE) optimized for heavy duty-cycling in a volume of 10x10x6mm^3 form-factor. An electrically small differential loop antenna is designed, and all components are integrated on the top and bottom of the antenna in close proximity without degrading the antenna efficiency. The GPS logger can sample 115K fixes from the 12mAh Li-ion battery before recharging. The logger can store data for 37 position fixes by streaming 10ms of received signal per fix to dual flash memories for later egress and post-processing. After post-processing, the 10dB SNR required for the GPS logger is -125dBm. In the sleep mode, the processor and the timer only consume 50nW and in the active mode the total power jumps up to 12.5mW. The proposed GPS logger has total volume of 10x10x6mm^3 while achieving 1.5mJ energy per fix.

In chapter 4, the GPS analog front-end (AFE) is specifically designed for receiving the GPS tri-band signals by using passive mixers. The main contribution of the RF front-end is comprised of a signal path which support the tri-band mode (L1, L2, L5) which can be sampled the three bands onto a single IF channel simultaneously. By utilizing spreading of the GPS signals, more satellites are visible at GPS multi-bands which enables faster signal acquisition, enhanced reliability, and greater operation range. The AFE is able to fold the tri-band GPS signals onto a low-IF thanks to the orthogonality of the pseudo-random (PRN) codes. The radio draws 9.6mW from a 1.2V/1.4V supply, with a passive RF front-end and a startup time of 20μs.

An integrated rectangular slot loop antenna in a standard 0.13-μm BiCMOS technology is presented. By using the complementary structure of loop antenna, the slot loop antenna can easily satisfy the metal density rules without dummy metal fill and does not necessary the keep-out region (except the slot area) which could integrate with the active devices. As another advantage of the slot type antenna, it can be fabricated and concealed it within metallic objects which could be power or ground plane in circuit design. Thanks to its high impedance, small size, high gain and wide bandwidth, the slot loop antenna is beneficial to use in short-range IoT applications. The loop antenna only occupies 0.24mm^2 and the total area of the antenna including the ground plane is 0.883mm^2. From the measurement, the antenna resonates at 58 GHz and the bandwidth at VSWR 3.0 is 2.67 GHz from 55.61 GHz to 58.28 GHz with 300-ohm load.

6.2 Future Work

The presented integrated slot loop antenna at chapter 5 is not only designed as an efficient radiator could cover wideband but can be used as an electrical resonator working with the circuity. At the 60 GHz band, the integrated antenna acts as a resonator with a relatively high Q factor compared to the passive devices. Therefore, a 60GHz bands low-power transmitter with an integrated antenna referenced frequency-locked loop (FLL) that eliminate the need for a crystal reference and ensures channel selectivity in 57-64 GHz.

The block diagram of the 60GHz bands transmitter with FLL is shown in Figure 6.1. The transmitter is mainly comprised of two part; RF Front-end and frequency-locked loop. At RF front-end, the 60-GHz band signal is generated and amplified to the integrated antenna. The FLL has two sets of the envelope detectors, MUXs, an error amplifier, an integrator, and a loop filter. By

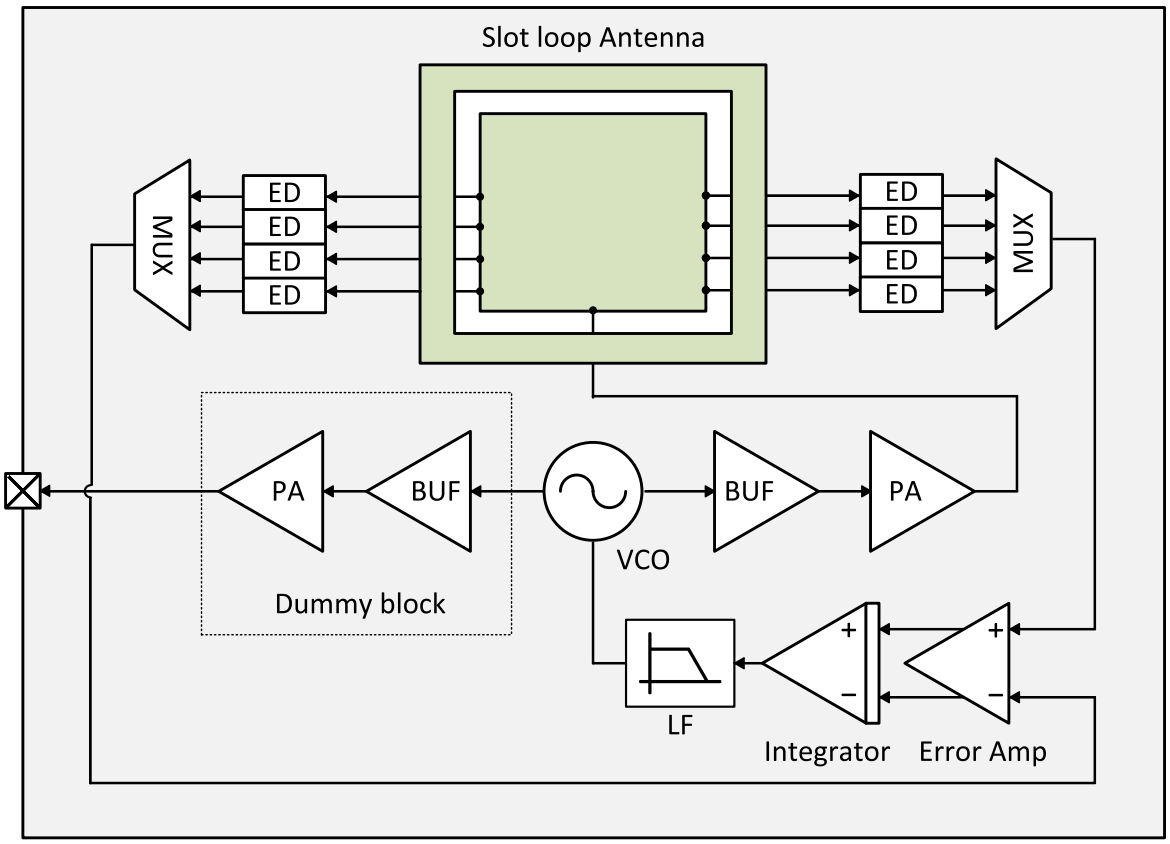


Figure 6.1 Block diagram of the 60 GHz bands transmitter

using null detection, the feedback signal through baseband circuitry control the VCO frequency for FLL.

The RF front-end is consists of a LC differential VCO, a buffer, a power amplifier (PA). The transmitter supports on-off keying (OOK) modulation by power gating at PA with header device, so that the FLL can serve as a simple low-rate OOK transmitter. The VCO uses a cross-coupled LC oscillator. The frequency tuning is realized by three differential pair of NMOS varactors and the range is 57 to 64 GHz. The buffer and power amplifier are designed for maximum power gain. The integrated inductor and transmission lines are used as matching components. At the resonance frequency, the input impedance of the antenna matches to relatively high impedance of 300 ohms that could minimize loading effect to VCO and induce larger voltage swing at the envelope detectors.

The frequency-locked loop is comprised of the slot loop antenna, 2 sets of envelope detectors, error amplifier, integrator and loop filter. To get the symmetrical field distribution, 4 envelope detectors are located at each side for the same loading on the antenna. The input impedance of the envelope detector need to be high impedance to prevent pulling too much power into detectors and shifting the input impedance of the antenna. Depends on the frequency interest, two detector outputs are chosen through multiplexer. At the error amplifier, any voltage difference from detectors generates a compensating error voltage. The integrator introduces a pole at DC, minimizing the steady state error between the FLL and the resonator. The loop filter stabilizes the FLL and is realized by a distributed resistive transmission line with metal comb capacitor units with a self-resonant frequency above 60GHz.

The four envelope detectors are located at both side to monitor the voltage magnitudes (Figure 6.2(a)). In 57-64 GHz, the null moves around the envelope detectors and it generate several points where the difference of voltage magnitude from two envelope detector equal to zero. Figure 6.2(b)

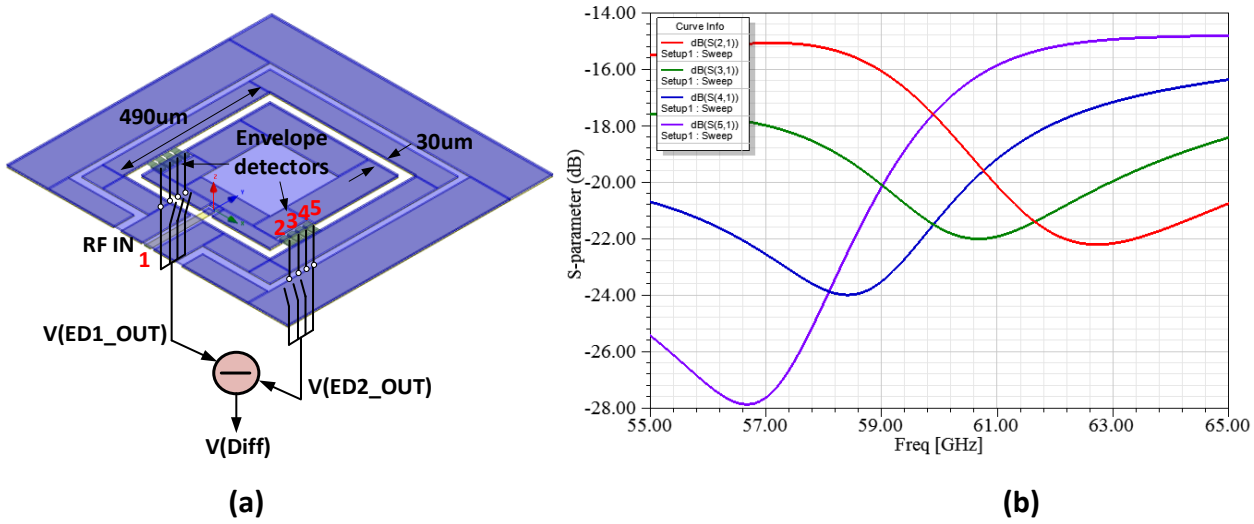


Figure 6.2 (a) Simplified model of resonance detection (b) S-parameter from the antenna and envelope detectors

shows the power delivered ratio from the input to envelope detectors. Each envelope detector has one electric null at the unique frequency based on the location at the slot. The 6 monotonic curves are derived from the combination of 4 envelope detectors. The zero crossed points are in the 60GHz bands and the FLL can be locked on the desired frequency by tapping any of two envelope detectors. The difference in magnitude on two different envelope detectors are plotted in Figure

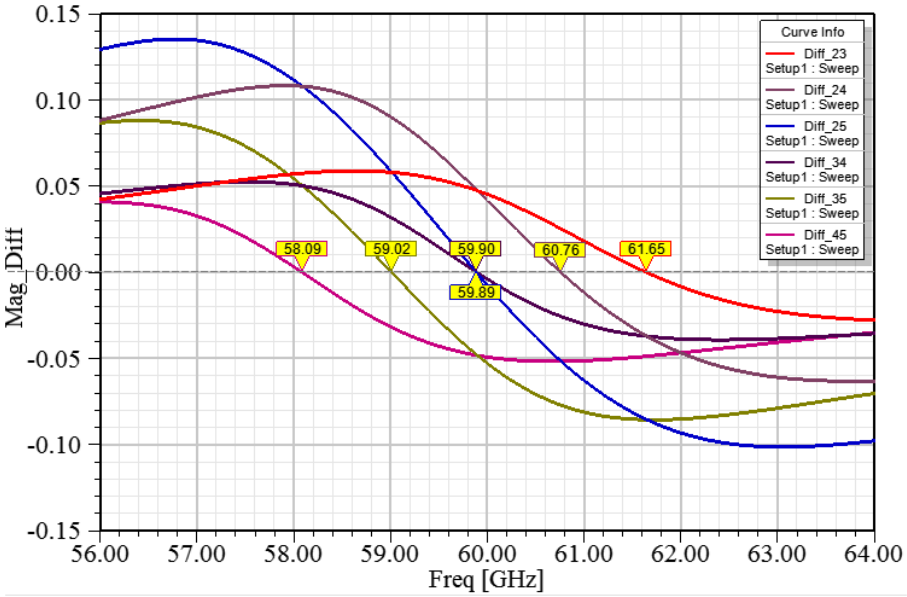


Figure 6.3 Difference in magnitude on two different envelope detectors

6.3. The crossing points where the difference equal to zero are equally spaced (~900MHz) thanks to the location and gap of the detectors. Depending on the gap between envelope detectors, the gap of the crossing points is controllable. However, it can be increased too much because the resolution of the null detection is mainly limited by the frequency variation of the antenna and VCO tuning range. Therefore, the gap and number of the detectors need to choose carefully.

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