High Aspect-ratio Biomimetic Hair-like Microstructure Arrays for MEMS Multi-Transducer Platform

by

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DEDICATION

To my parents, Hong Liping 洪莉萍 and Tang Jianfa 唐建法.

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ABSTRACT

Many emerging applications of sensing microsystems in health care, environment, security and transportation systems require improved sensitivity and selectivity, redundancy, robustness, increased dynamic range, as well as small size, low power and low cost. Providing all of these features in a system consisting of one sensor is not practical or possible. Micro electro mechanical microsystems (MEMS) that combine a large sensor array with signal processing circuits could provide these features.

To build such multi-transducer microsystems we get inspiration from “hair”, a structure frequently used in nature. Hair is a simple yet elegant structure that offers many attractive features such as large length to cross-sectional area ratio, large exposed surface area, ability to include different sensing materials, and ability to interact with surrounding media in sophisticated ways. In this thesis, we have developed a microfabrication technology to build 3D biomimetic hair structures for MEMS multi-transducer platform. Direct integration with CMOS will enable signal processing of dense arrays of 100s or 1000s of MEMS transducers within a small chip area.

We have developed a new device structure that mimics biological hair. It includes a vertical spring, a proof-mass atop the spring, and high aspect-ratio narrow electrostatic gaps to adjacent electrodes for sensing and actuation. Based on this structure, we have developed three generations of 3D high aspect-ratio, small-footprint, low-noise accelerometers. Arrays of both

high-sensitivity capacitive and threshold accelerometers are designed and tested, and they demonstrate extended full-scale detection range and frequency bandwidth.

The first-generation capacitive hair accelerometer arrays are based on Silicon-on-Glass (SOG) process utilizing 500 μm thick silicon, achieving a highest sensor density of ~100 sensors/mm^2 connected in parallel. Minimum capacitive gap is 5 μm with device height of 400 μm and spring length of 300 μm.

A custom-designed Bosch deep-reactive-etching (DRIE) process is developed to etch ultra-deep (> 500 μm) ultra-high aspect-ratio (UHAR) features (AR > 40) with straight sidewalls and reduced undercut across a wide range of feature sizes. A two-gap dry-release process is developed for the second-generation capacitive hair accelerometers. Due to the large device height at full wafer thickness of 1 mm and UHAR capacitive transduction gaps at 2 μm that extend > 200 μm, the accelerometer achieves sub-μg resolution (< 1μg/√Hz) and high sensitivity (1pF/g/mm^2), having an area smaller than any previous precision accelerometers with similar performance. Each sensor chip consists of devices with various design parameter to cover a wide range. Bonding with metal interlayers at < 400 °C allows direct integration of these devices on top of CMOS circuits.

The third-generation digital threshold hair accelerometer takes advantage of large aspect-ratio of the hair structure and UHAR DRIE structures to provide low noise (< 600 ng/√Hz per mm^2 footprint proof-mass due to small contact area) and low power threshold acceleration detection. 16-element (4-bit) and 32-element (5-bit) arrays of threshold devices (total chip area being < 1 cm^2) with evenly-spaced threshold gap dimensions from 1 μm to 4 μm as well as with hair spring cross-sectional area from 10^2 μm to 30^2 μm are designed to suit specific g-ranges from < 100 mg to 50 g.

This hair sensor and sensor array technology is suited for forming MEMS transducer arrays with circuits, including high performance IMUs as well as miniaturized detectors and actuators that require high temporal and spatial resolution, analogous to high-density CMOS imagers.

Chapter 1 INTRODUCTION

Researchers have continued to explore new approaches to develop miniaturized sensors and actuators with improved performance, enhanced functionality, smaller size and lower cost. Innovations are made possible with significant advances in design/analysis techniques, integrated circuits, micro/nano fabrication and packaging technology. One of the many approaches is based on a multi-transducer platform and microsystem which takes advantage of co-fabricated sensor arrays and integration with signal conditioning circuitry. Taking inspiration from one of the most commonly occuring structures in nature, large arrays of biomimetic hair sensor systems are a promising candidate for a multi-transducer platform that can potentially provide many advanced features: improved sensitivity and selectivity, redundancy, enhanced robustness, increased dynamic range and enhanced functionality.

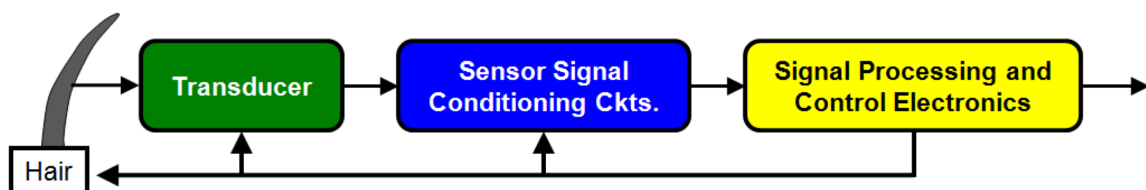


Fig. 1.1. Biomimetic hair sensor system [1].

Our group has proposed the basic elements of a highly functional, sensitive and selective biomimetic hair sensor system as shown in [1]. These elements are: 1) the core high aspect-ratio small-footprint hair-like structure with large surface-volume ratio configured with an array to

effectively interact with external environment; 2) the transduction elements which efficiently converts the external physical parameters to electrical signals; 3) local interfacing circuits to improve sensitivity and selectivity, and 4) signal processing and control electronics.

This chapter starts with the motivation for developing a biomimetic hair multi-transducer microsystem. Potential benefits of such sensor system include providing both high accuracy and high frequency selectivity measurement over wide dynamic range. We also present a discussion of existing MEMS biomimetic hair sensors and sensor arrays, and concludes by presenting the contribution and organization of this thesis.

1.1 Motivation for Biomimetic Hair Multi-Transducer Microsystem

There are many types of sensors and actuators found in biological systems and among them, hair-like structures are used extensively to achieve a myriad of functions including: air/fluid flow sensing for aerodynamic control of wing structures, temperature sensing for insulation or temperature control, acoustic or vibration sensing, tactile sensing, chemical sensing etc. Cilia interact with neural cells when stimulated by specific physical movements which are electromechanically converted into electrical potentials enabling the sensing of mechanical motion.

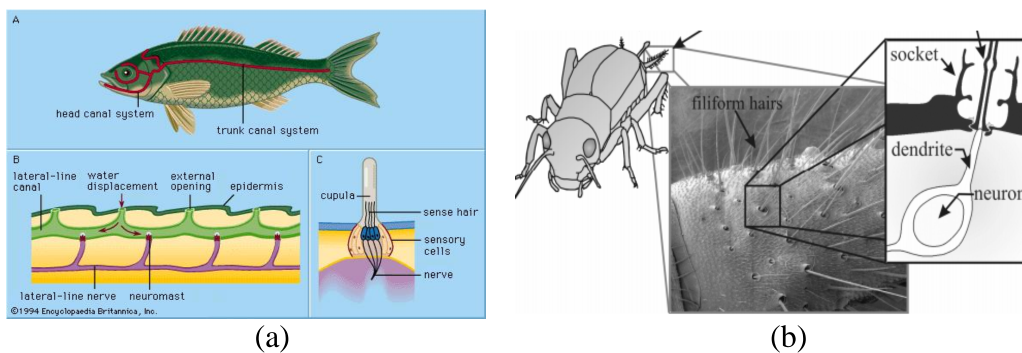


Fig. 1.2. Hair in nature: (a) Neuromast called cupula going down the side of the fish [2]; (b) Air flow sensing in crickets by appendages call “cerci” [3].

Examples include the lateral line hair in aquatic vertebrates [2], cerci in crickets [3] and the cochlear hair cells in human and other mammals [4]. The neuromasts called cupula going

down the side of the fish bends in response to the water flow. The cluster of sense hairs embedded in protective, gel-like domes within the cupula converts the fluid-flow to electrical potentials. Air flow sensing in crickets is achieved by appendages called “cerci” where different hair lengths and directions provide frequency selectivity and directivity. In humans and other mammals, the vestibular system that detects gravity, linear motion and rotary motion and cochlear in the auditory system both rely on the phenomenal speed and sensitivity of the hair cells [4].

Sound can be represented as the sum of a set of sinusoidal components of different frequencies and amplitudes. The cochlear can separate the acoustic frequencies along its length like an acoustic prism. The 35 mm-long basilar membrane in human cochlear responds to frequencies from less than 100 Hz to 20 kHz, with logarithmic frequency mapping such that each decade occupies an equivalent distance (Figure 1.3(a)).

Sound waves are initially relayed by the middle ear bones and set in motion the tapered basilar membrane. Upward displacement of the basilar membrane stimulates the hair cells by bending their stereociliary bundles against the acellular tectorial membrane. Submicron deflections of the stereociliary bundles on the inner hair cells in the cochlear are detected by the outer hair cells and forces are generated to augment the signal, with the outer hair cells functioning as both sensor and motor. The cochlear transmits signals to the auditory nerve and eventually to the auditory cortex in the brain.

Researchers have different theories that explain the remarkable frequency selectivity ability of the auditory system. It partly relies on mechanical resonances of the basilar membrane. Sound of different frequencies excite localized patterns of vibration at different positions along

the membrane, with the resonant frequency of each section determined by the average mass, stiffness, and damping of the basilar membrane (Figure 1.3(b)).

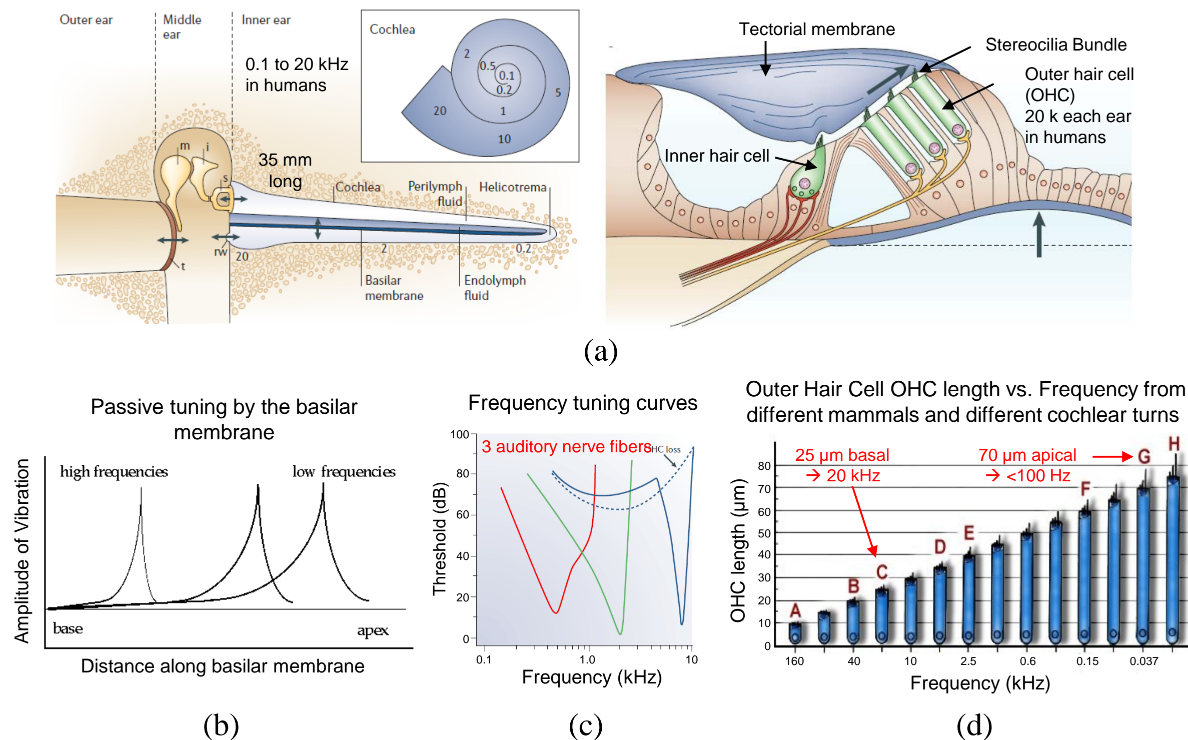
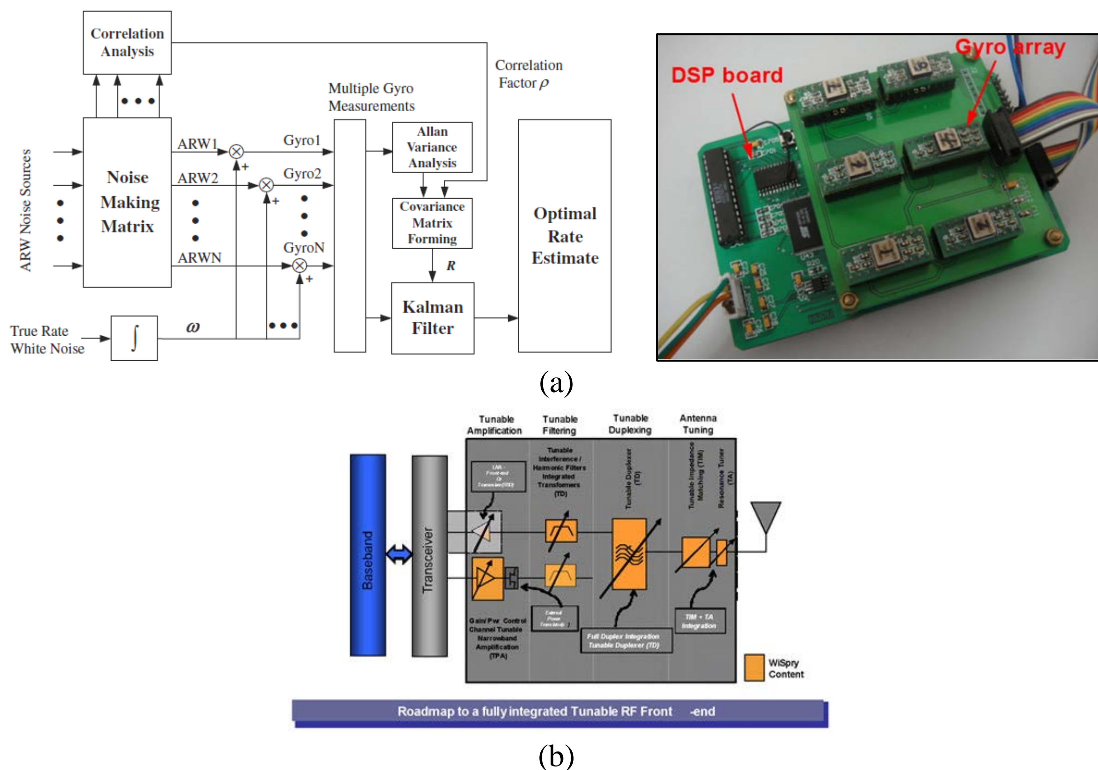


Fig. 1.3. Hair cells in the vestibular system and cochlear: (a) Inner and outer hair cells interact with basilar membrane excited by sound wave;(b) (c) (d) Auditory frequency selectivity [4].

Frequency selectivity is also by the change in morphology of outer hair cells (OHCs) located in the organ of Corti within the cochlear. The OHC morphology changes along the length of the cochlear duct, with shorter OHCs at the base and longer OHCs at the apex. OHC have a cylindrical shape and are about 9 µm in diameter. They vary in length from ~20 µm at the basal end of the cochlea to approximately 90 µm at the apex. Figure 1.3(c) shows an example of the V-shaped “tuning curves” of 3 nerve fibers. For each one, the characteristic frequency (CF) represents the frequency at which least energy is needed to stimulate it and elicit a response from a central auditory neuron. Different nerve fibers have different CFs and different thresholds. The CF of a fiber is roughly the same as the resonant frequency of the part of the basilar membrane

that it is attached to. Figure 1.3 (d) shows OHCs from different mammals and different cochlear turns, with two human OHCs highlighted, one 20 μm at the basal and another one 70 μm at the apex. There are more than 20,000 OHCs with afferent nerve fibers in each ear in human, and with CFs that span the entire auditory range.

There are many emerging transducer applications [5-12] that would desire these nice features of the biological systems: improved sensitivity and selectivity, redundancy, enhanced robustness, increased dynamic range and enhanced functionality. Biomimetic hair sensors can have small footprint and high integration density thus arrays of sensors can be integrated monolithically.



(a)

(b)

Fig. 1.4. Examples of potential applications of the proposed hair multi-transducer platform: (a) Synthetic Gyroscope [7], (b) Fully integrated tunable RF front-end [8].

Some examples are: 1) High performance inertial measurement units that requires large dynamic range, high resolution, as well as providing robustness and system redundancy [5-7]; 2)

RF front-end models where multiple standards for wireless communications and multiple antenna switches need to be integrated while size needs to be kept small [8-9]; 3) Large arrays of miniaturized detectors and actuators with high temporal resolution and high spatial resolution for pattern recognition, analogous to high-density CMOS imagers [10-11]; 4) Flexible and expandable smart acoustic sensor array system with powerful real-time signal processing capability [12].

For high-performance inertial measurement unit, one can take advantage of large arrays of individual sensors. For example, optimally combining measurements from N sensors into a single estimate by Kalman filtering proves to be significantly improving the performance over individual elements. Xue et al. [7] demonstrated reduced Allan variance, bias instability and reduced noise density (0.03°/s/√Hz for the combined rate signal from the six-gyroscope array compared to 0.11°/s/√Hz single). Since a single-chip gyroscope array with a different correlation was not available, they had to take six separate MEMS gyroscopes ADXRS300 chips to form the gyroscope array.

In addition, the bandwidth and dynamic range of typical MEMS based single-sensor IMU are usually fixed and only allows for limited tuning. They use one mechanical sensor for single or multiple axis detection and the bandwidth is predetermined by the mechanical resonant frequency of a single spring-mass-damper system. Existing wide-band inertial sensors demand intensive computation by the control algorithms implemented by microprocessor for further filtering and processing, and thus are very power hungry and slow down the control loop. Thus, using large array of individually tunable mechanical sensors with modulated performance can enable band-selective and large dynamic range inertial measurements. Redundant, reconfigurable and programmable mode of operation may also be realized.

For RF front-ends design, the radio design is required to work with different wireless standards implemented on many frequency bands. The front-end complexity is driven higher at the needs to have separate RF chains for each band. The preferred implementation has been a combination of parallel front-ends and several tunable broadband antennas to select the desired signal path [8].

Common requirements of these arrayed microsystems are: high performance discrete element, large arrays of individual element with modulated specifications, and signal processing ability. Biomimetic multi-transducer platform is thus a perfect candidate for these applications. Utilizing the third dimension is necessary to build these devices in dense array, small area and at a lower cost.

1.1.1 High Accuracy Over Wide Full-Scale Range

The multi-transducer platform that mimics hair sensor arrays in nature we proposed in this research falls in the realm of what is known as ‘smart sensor' [13]. The fundamental idea of a smart sensor system is that the integration of silicon microprocessors with sensor technology not only provide customized outputs and interpretive power, but also significantly improve sensor system performance and capabilities.

Once the behavior of the sensing elements is well studied and output has been defined, the electronic interface can be designed. For example, a Universal Transducer Interface (UTI) [14] from Smartec is available to provide interfacing for many types of application nodes: capacitors, platinum resistors, thermistors, resistive bridges and potentiometers.

One of the major challenges for a smart microsystem has been to realize both high accuracy and wide dynamic range from a single-chip microsystem. The demand for the measurement to be linear, well characterized, and highly-accurate poses challenges when the

signals to be measure covers wide dynamic range (frequency, amplitude, etc.). For example, for a Wheatstone bridge sensor readout configuration, in order to generate outputs at the same order of magnitude for a wide range of inputs, the bridge output will need to be amplified by a scaling factor (SF) for small-amplitude signals, while being divided by SF for strong signals. This will yield better linearity and extend full-scale-range.

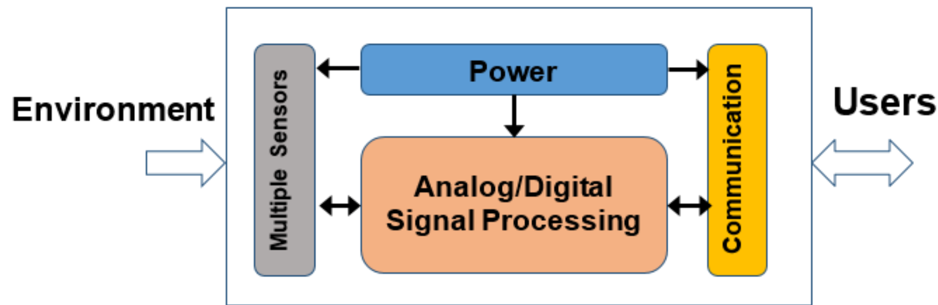


Fig. 1.5. Components of smart sensors.

Application mode	Resolution in slow mode	Resolution in fast mode	Accuracy in slow mode	Condition
Capacitors in (0 to 2) pF range	50 aF	150 aF	14 bit	$C_p = 30$ pF
Capacitors in (0 to 12) pF range	0.3 fF	0.9 fF	14 bit	$C_p = 30$ pF
Platinum resistors	7 μV or 9 mK	20 μV or 26 mK	15 bit	Pt100, $I_{pt} = 2$ mA,
Thermistors	7 μV or 1 mK	20 μV or 3 mK	15 bit	$R_{th} = 1$ kΩ, 4 %/K
Resistive bridge, 200 mV range	7 μV	20 μV	11 bit	
Resistive bridge, 12 mV range	700 nV	2 μV	10 bit	

Fig. 1.6. Measurement results of some of the 16 application nodes of a Smartec UTI [1.14].

Two methods are typically employed: single-sensor/multi-processing-paths and multi-sensor/multi-processing-paths. The latter has the potential to reduce processing circuit complexity and enables a more balanced system approach.

Some examples of the single-sensor/multi-processing-paths approach is to design high precision variable gain amplifier by integration of the output of one sensor in the time domain

[15-17]. In [15], a low-drift variable gain amplifier is realized by a rotating chain of resistors where the effect of mismatch of these resistors is minimized by averaging outputs from multiple samples. Small signals are amplified by a larger scale factor by adjusting resistor ratio. The same dynamic element matching (DEM) amplifier concept was also realized by using banks of switched capacitors to reduce the effect of component mismatches [16]. In [17], a combined resistive/capacitive divider network is built to scale down the larger signals. In these cases, the sensing element remains the same while the circuit block cycles through each state in time. The system memorizes, integrates the outputs, and calculates the average value.

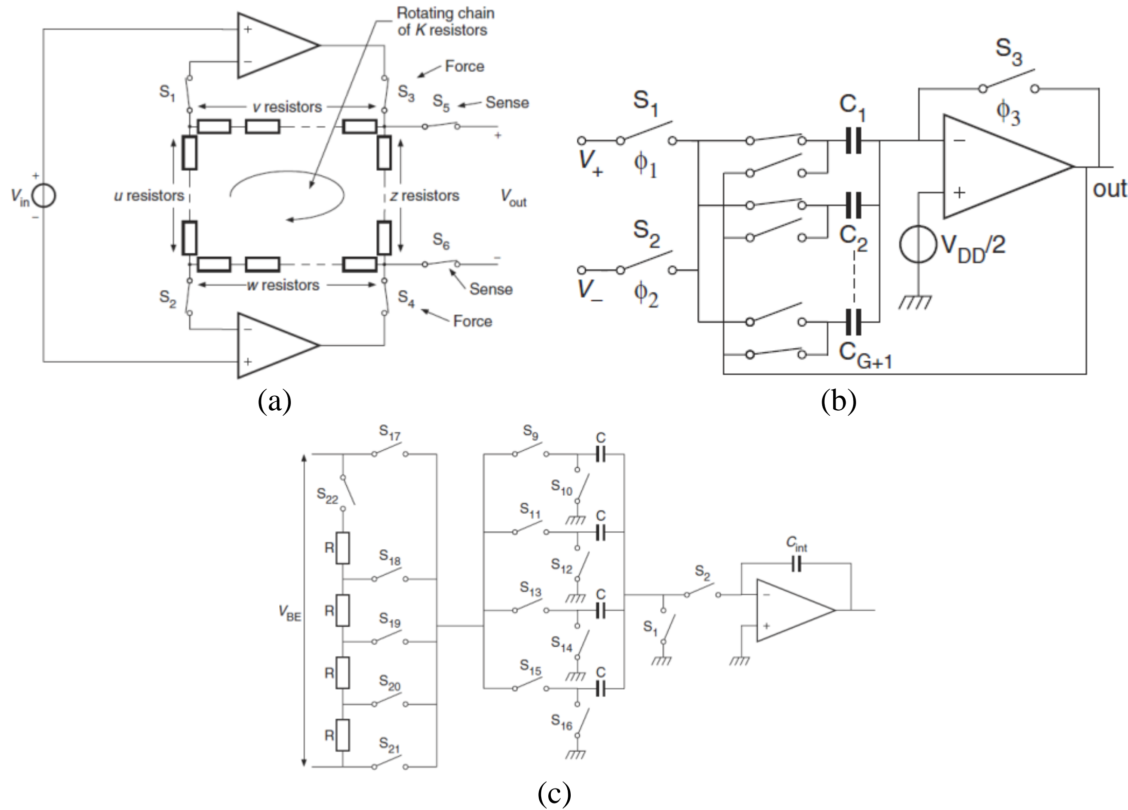
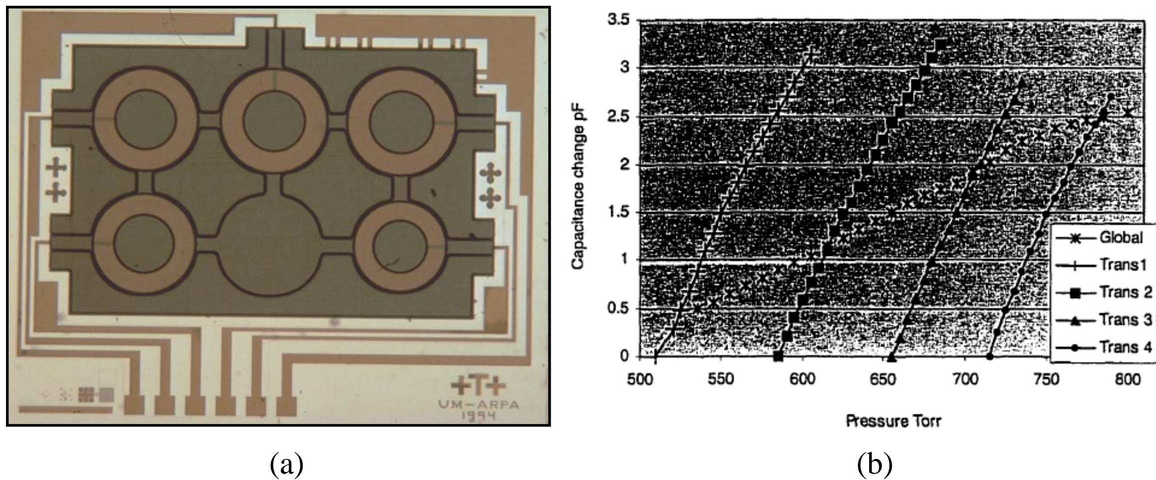


Fig. 1.7. Single-sensor/multi-processing-paths approach with dynamic amplification of sensor output by circuit: (a) Rotating chain of K resistors as a dynamic-feedback instrumentation amplifier [15]; (b) A dynamic element matching (DEM) switched capacitor amplifier [16]; (d) A dynamic voltage divide [17].

However, switching through the all the programmed states slows down the overall processing speed. For example, the Smartec UTI has internal frequency at 50 kHz.

On the contrary, multi-sensor/multi-processing-paths approach is faster and provides additional functionalities (spatial resolution, robustness, redundancy, etc.) because arrays of devices are used and outputs are readily selected. However, the increase in the number of sensors for each application node in the smart sensor system will greatly affect the overall size and thus cost. It is not feasible without developing new technology.



(a) (b)

Fig. 1.8. An integrated high resolution barometric pressure sensing system [18-19]: Measured output voltage of global range selection transducer and four segment transducers.

One noteworthy work in literature targeted to achieve both high accuracy and large dynamic range is by utilizing a course-to-fine or segmented sensing system with an array of devices with various designs. The pressure sensor chip proposed by A. V. Chavan et al. [18-19] is composed of an array of modulated dimension pressure sensors as shown in Figure 1.8. One of the transducers is a lower-sensitivity global range-checking device, while the other four devices have higher sensitivity but smaller ranges. The global device spans the entire range of 300 Torr. Its response is exponential in the lower half of the span and changes to being logarithmic in the upper half. It is not linear over its entire range thus it is more challenging to find an analytic

expression for this response over temperature and for calibration. For the segment devices, the nominal sensitivity for each one of them is 39 fF/Torr (3800 ppm/Torr) and they each has a short operational span of 70 Torr, with considerable overlap in their ranges. Their response thus is fairly linear. By using programmable transducer selection provided on the readout circuit, the global device is sampled to determine what range the ambient pressure is in, followed by switching to the appropriate higher-sensitivity transducer for a high-resolution measurement.

Another noteworthy work by Hudson et al. [5] investigated in the use of controlled multiplexed arrays of MEMS accelerometers to provide full dynamic performance ranges, improved harsh environment tolerances, and improved reliability for miniature sensing systems, especially for inertial applications.

An acceleration fusion algorithm to effectively expand the performance range is tested on both an array of three commercially-available Colibrys MS8000 series accelerometer chips, and an array of in-house co-fabricated SOI accelerometers on a single chip. The calculated extended acceleration and weight factor W_i are as followed:

$$A = \frac{\sum_i W_i(C_i V_i)}{W_i} = \frac{\sum_i W_i A_{measured}}{W_i} \quad (1.1)$$

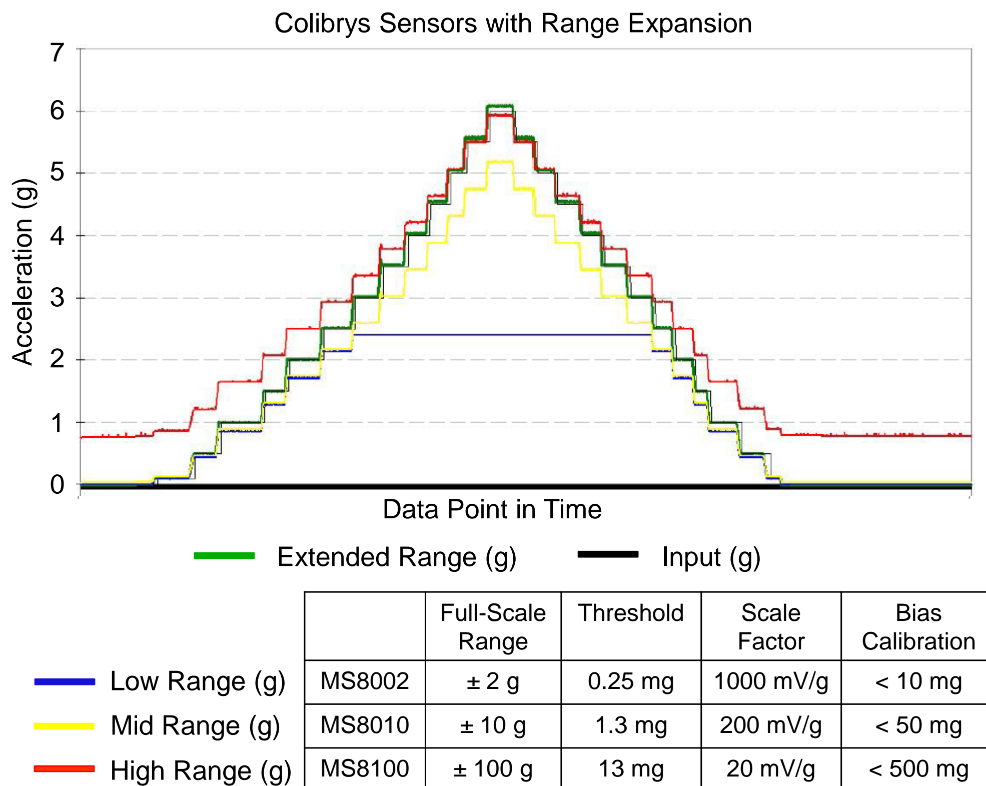
$$W_i = |V_i| \; if \; |V_i| < M_i, = 0 \; else, \; \forall i. \quad (1.2)$$
$$C_i = 1/SF$$

The weight factor W_i assigned to sensor i readout is determined by its zerod acceleration voltage V_i and the voltage at full specified acceleration M_i. If the readout saturates ($V_i \geq M_i$), the factor is assigned as zero.

Compare similar devices in the Colibrys MS8000 series, MS8002 with a smaller full-scale range ±2 g and large scale-factor (SF) of 1000 mV/g, and MS8100 with a higher full-scale range ±10 g and small scale-factor (SF) of 20 mV/g, the weight factor W_i(the zeroed voltage output V_i)

for greater-range MS8100 is much smaller at lower g-range. Thus, using this algorithm, the large bias (500 mg) of MS8100 will be compensated by MS8002 that provides more accurate readout. However, it is also true that the noise performance at lower g-range is compromised by including the readout from the high-range device, when compared with the single low-range device MS8002.

Figure 1.9 shows all three accelerometers' data, the extended range readout and the original input acceleration on the same plot. The extended range readout more closely follows the actual acceleration than any of the three accelerometers, and it is obvious that at the lower end, error of the high-range accelerometer was overcome by the extended-range algorithm. However, the mid-range sensor that has a smaller bias deviates more from the actual inputs at 4-6 g when the low-range device already saturates, so this plot may not be accurate according to the algorithm.



	Full-Scale Range	Threshold	Scale Factor	Bias Calibration
MS8002	± 2 g	0.25 mg	1000 mV/g	< 10 mg
MS8010	± 10 g	1.3 mg	200 mV/g	< 50 mg
MS8100	± 100 g	13 mg	20 mV/g	< 500 mg

Fig. 1.9. Extend the full-scale range by using multiplexed Colibrys MS800 series accelerometer arrays [5].

Measurements are also presented on custom-designed silicon-on-insulator SOI MEMS accelerometer arrays with the expansion algorithm applied. The extended range measurement from the three accelerometers array also more closely follows the actual input acceleration, and the algorithm is able to compensate for the noisy acceleration measurements of the "high-g" and "mid-g" accelerometers. The resolution of the three accelerometers are 10 mg, 100 mg and 1000 mg respectively from the "low-g" to "high-g" device.

However, the overall chip area and footprint of each device is relatively large for the acceleration resolution they can achieve: each of them are > 2 mm on the side due to the thickness of device silicon layer in the SOI stack being only 100 μm.

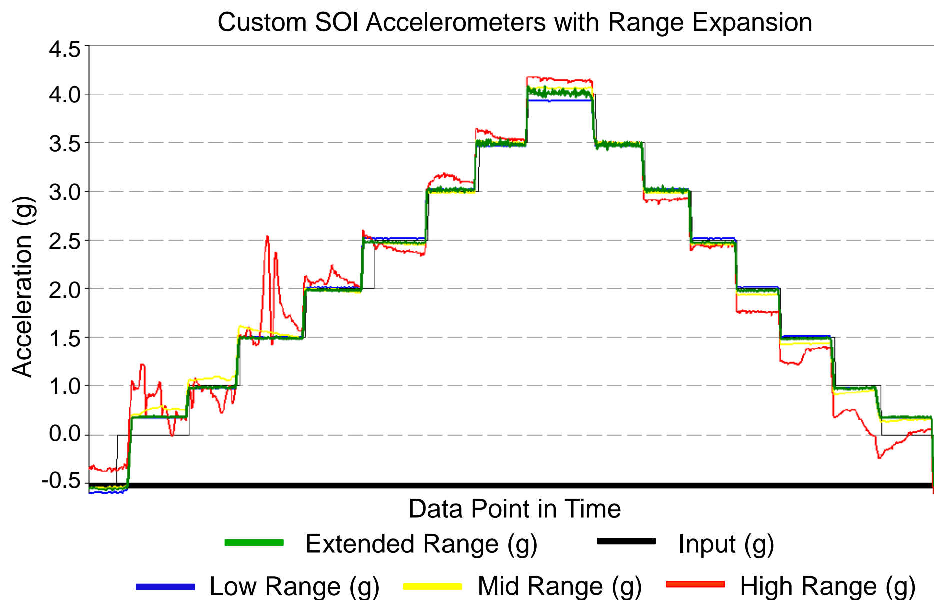


Fig. 1.10. Extend the full-scale range by using of multiplexed accelerometer arrays co-fabricated on custom SOI substrates [5].

These previous works on single-chip pressure sensor arrays and accelerometer arrays have proven the efficacy of extending dynamic range while preserving relatively high measurement resolution and accuracy by implementing modulated designs within an array of devices co-fabricated on the same chip.

However, limitations occur as sensor array size scales up as the number of devices increases. To realize high-density arrayed-sensor microsystems on a single chip, new microfabrication technologies need to be developed both on high aspect-ratio MEMS fabrication techniques as well as efficient MEMS-electronics integration technology.

1.1.2 Micromechanical Frequency Processer over Wide Frequency Spectrum

Another key challenge in addition to achieving high accuracy over wide full-scale range by a sensing system with a single sensor is realizing high frequency selectivity over wide frequency spectrum. Instead, sensing system that consists of massive array of mechanical sensors with modulated frequency spectrum lines can provide such function.

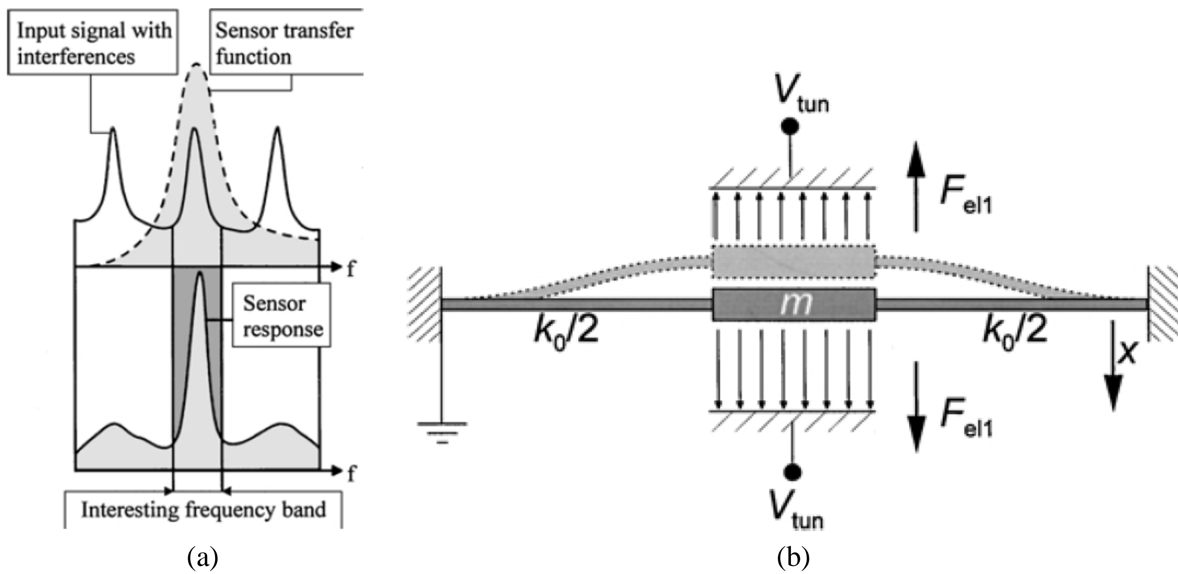


Fig. 1.11. (a) Signal selective principle, and (b) stiffness modulation of the resonance frequency of the spring-mass pair by electrostatic forces. [20].

An array of mechanical resonators can be used to construct a vibration monitoring system. For example, in the scenario of vibration monitoring of engines, gears and bearings, their wear state frequencies or vibration signature cover a wide range from several Hertz to 10 kHz [6]. Wide-band output from a single sensor is processed by sophisticated electronics to analyze and separate the frequency components. Wibbeler et al. [6] suggests that future development of

vibration monitoring equipment will be carried out by smart sensors with fully-digital interface, self-test functionality and onboard storage, all at lower cost for permanent monitoring in safety related applications or at extremely expensive machinery.

Mechanical signal processor is built based on the mechanical resonance of a spring-mass structure with direct electrostatic stiffness tuning ability as shown in Figure 1.11. An incoming spectrum is only amplified at the resonance frequency of a particular sensor. The advantage of resonance pickup compared to processing wide-band output signal by electronics is its higher signal-to-noise ratio (high SNR) due to the high quality factor (high Q) of the sensor structure. The approach will also simplify the signal conditioning circuit.

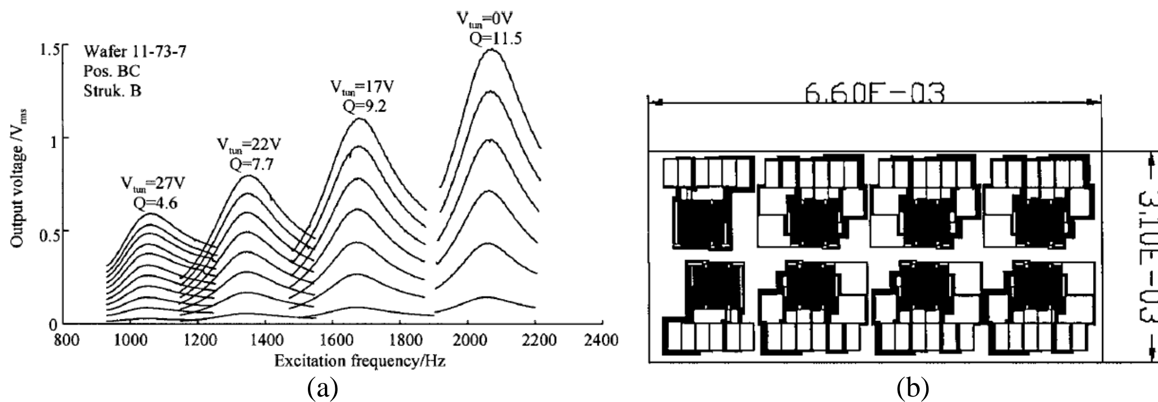


Fig. 1.12. (a) Measurement of one sensor structures that covers 1 to 2 kHz with various tuning voltage, and (b) Layout of eight-sensor array that covers 1 to 10 kHz. [20].

To characterize the wear state of several spectrum lines, an array of sensor structures with stepped base frequencies can be designed to match the spectrum lines. They fabricated and tested one-sensor structure that can achieve resonance frequency from 1 kHz to 2 kHz by applying various tuning voltages as shown in Figure 1.12(a). The lines at the same frequency share the same tuning voltage V_{tun}. The slight shift (~1%) of the frequency shift is due to different ac excitation amplitudes.

Since higher tuning voltage will reduce the Q-factor (from >11 to <5 with higher V_p) and

limit the frequency range, the researchers designed an eight-sensor array to match desired frequency range from 1 to 10 kHz and with tuning voltages of 35 V.

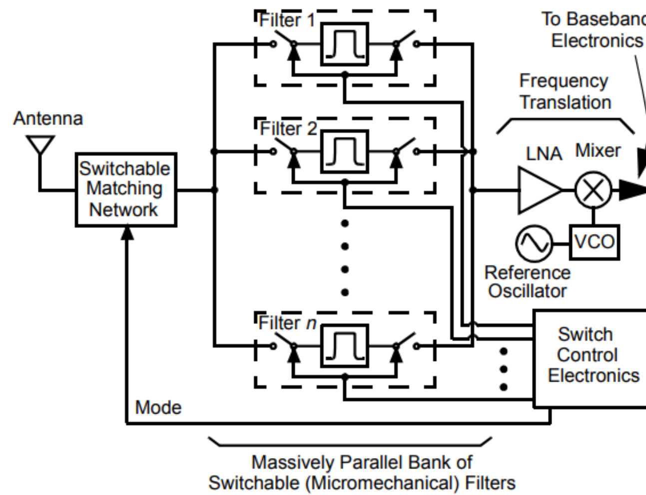


Fig. 1.13. Simplified block diagram of highly selective filters proposed for communications subsystems, where each filter switch combination corresponds to a single micromechanical filter [21].

Nguyen [21] has proposed back in 1998 that with quality factor (Q's) in the tens to hundreds of thousands, micromachined vibrating resonators can be used as IC-compatible tanks for use in the low phase noise oscillators and highly selective filters of communications subsystems as shown in Figure 1.13. Hundreds or thousands of a massively parallel bank of switchable micromechanical filters can be fabricated within smaller area to select one of several channels over a large frequency range thanks to the tiny size and zero dc power dissipation, rather than using a single tunable filter. The desired frequency bands can be switched in when needed. Figure 1.13 presents the simplified block diagram for such a front-end architecture, where each filter switch combination corresponds to a single micromechanical filter. Such system has high switching flexibility such that very resilient frequency-hopping spread spectrum transceiver architectures can be built that take advantage of simultaneous switching of high-Q micromechanical filters and oscillators.

1.1.3 High Frequency Stability and Accuracy by Resonator Array

Array of mechanically-coupled resonator can also be used to build stable MEMS-based oscillators against supply noise and acceleration. Wu et al. [22] constructed s 215-MHz polysilicon capacitive-gap transduced micromechanical resonator array employing 50 mechanically coupled radial-contour mode disks. The fluctuations in the dc bias voltage (V_P) applied across the electrostatic gaps results in frequency instability due to electrical stiffness variation. The arrayed resonator achieved 3.5 times better frequency stability than single stand-alone disks against V_P fluctuations.

To model the effectiveness of arrayed resonator on frequency stability, the classic equivalent electrical circuit of the 215-MHz radial-contour mode polysilicon disk resonator in a two-port excitation and sensing configuration in Figure 1.14(a) is transformed to a negative capacitance equivalent circuit of a disk array-composite with N resonators in Figure 1.14(b). In (a), the electrical stiffness is lumped into the variable capacitance C_r ($1/(k_m-k_e)$). To study the effect of impact of electrical stiffness on the overall circuit performance, the mechanical stiffness is represented through the transformers on both sides to outside the core LCR loop in (c) as negative capacitors $-C_{on}$. If the C_{on} is designed such that the load impedances $Z_{Ln} \gg \frac{1}{\omega_o C_{on}}$, C_{on} will pass most of the current flowing through C_{on} in parallel with Z_{Ln}, and almost same current will flow through C_{on} and $-C_{on}$, negating the electrical stiffness represented by $-C_{on}$.

Coupled-array increases C_{on} by N times thus leading toward better frequency stability against variations in electrical stiffness introduced by variations of the supply voltage. Figure 1.14 (d) validates that this method reduces the frequency dependence on dc-bias voltage as the number of resonators used in an array increases.

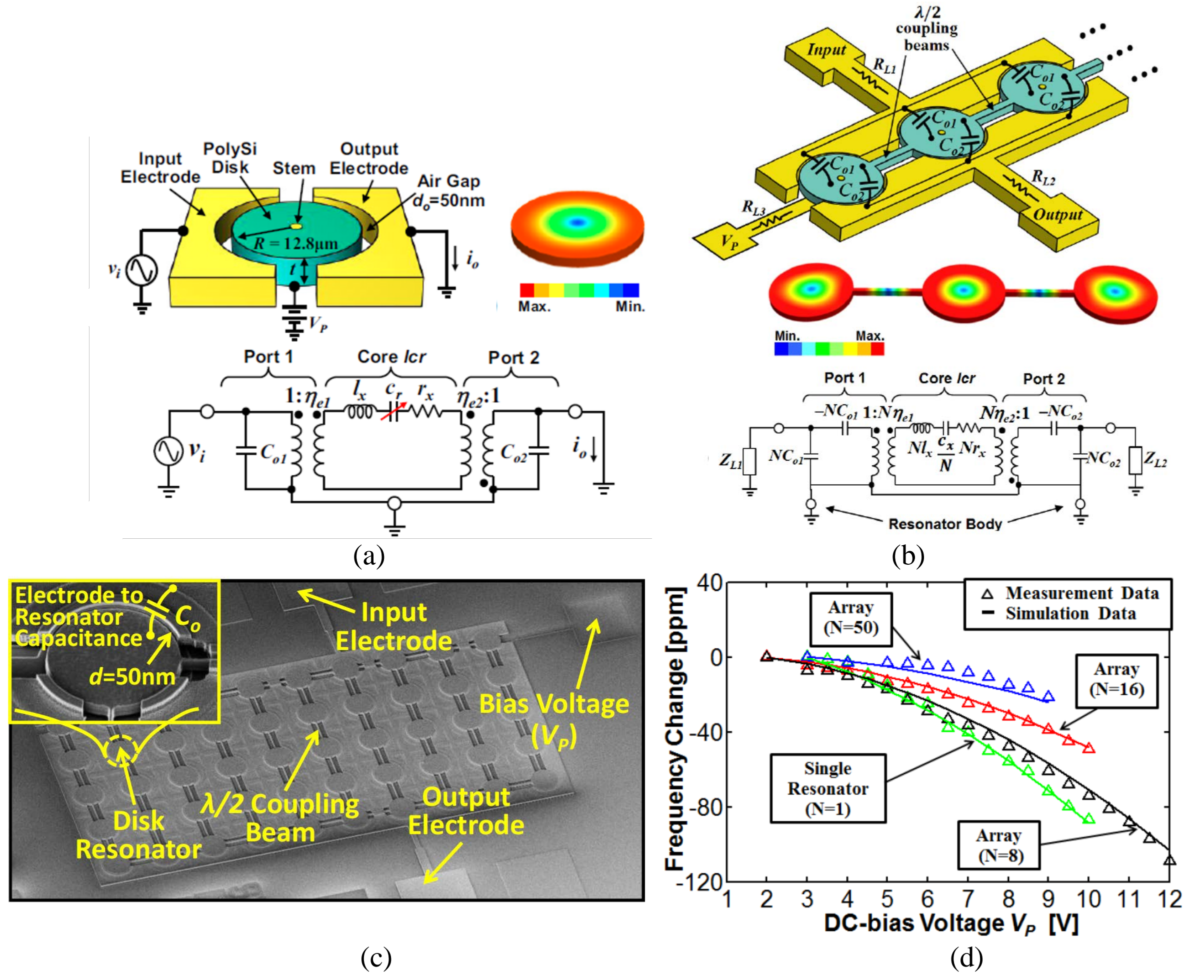


Fig. 1.14. (a) Schematic of a 215-MHz radial-contour mode polysilicon disk resonator in a two-port excitation and sensing configuration with the classic equivalent electrical circuit that has the electrical stiffness lumped into the variable capacitance C_r; (b) Schematic of a disk array-composite resonator with disks linked by λ/2 coupling beams to enforce in phase vibration of each individual resonator. Negative capacitance equivalent circuit of a disk array-composite with N resonators based on element values of the single resonator equivalent circuit; (c) SEM of a 215-MHz 50 nm capacitive-gap transduced contour mode disk array employing 50 mechanically coupled resonators; and (d) Measured curves of resonance frequency versus dc-bias voltage V_P plotted against simulation using negative capacitance equivalent circuit models for disk arrays with N=1, N=8, N=16, and N=50. [22]

1.1.4 Technology Development: 3D Vertical Integration

Batch fabrication of a wide range of MEMS transducers have been realized by microfabrication technologies that were initially developed for making ICs. Potential reduction

in chip size/pinout and improvement in signal transduction motivate integration of MEMS and electronics to construct a complete microsystem. Co-fabrication of MEMS and CMOS circuits has become a trend in IC design and researchers have worked on various integration methods to meet the specific requirements imposed on the process sequence, thermal budget and material selection [23-33].

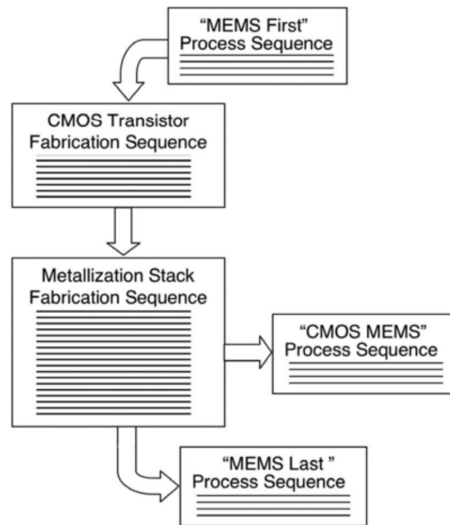


Fig. 1.15. Options for process integration of MEMS and electronic fabrication sequences: i) interleaved steps, ii) MEMS-first, and iii) MEMS-last, including formation of microstructures from the metallization stack layers [23].

In [23], the authors reviewed the major approaches in modular co-fabricating MEMS and electronics and divided them into two major categories as shown in Figure 1.15: 1) "MEMS first" where most of device fabrication are carried out prior to circuit fabrication, except potential DRIE or plasma release step involved in SOI substrates; and 2) "MEMS last" where MEMS layers are deposited and patterned with tight thermal budget post-CMOS fabrication.

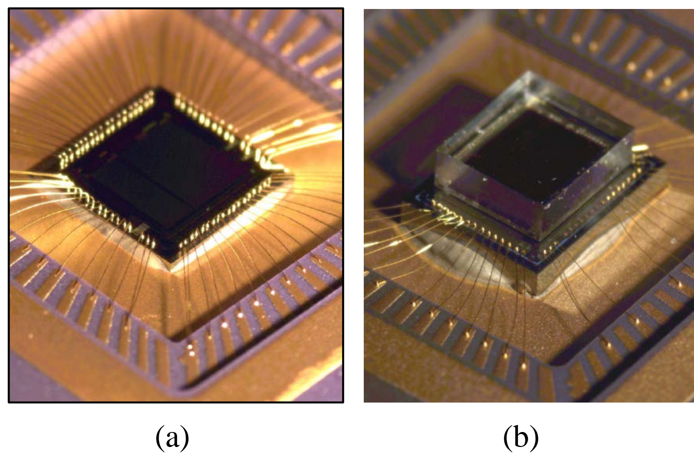
Some of the existing methods are not suitable for building arrays of 3D, tall and high-aspect-ratio MEMS devices. For example, metallic structural layers that are available in the CMOS process or readily deposited at CMOS compatible temperature have been applied to

inertial MEMS [25-26], RF demodulators [27] and pressure sensors [28]. It is done by defining the MEMS structure in metal interconnects layers and performing postprocessing etch steps on the dielectric passivation layers. However, the structures typically have limited height and aspect-ratio which is not optimal for high-performance MEMS Inertial Measurement Units (IMUs) [25-26]. In addition, the structure could be very sensitive to the unwanted deformations induced by thin-film residual stress and coefficient of thermal expansion (CTE) mismatch of metal-dielectric films. MEMS-first approaches where the microstructures are released and encapsulated prior to transistor fabrication impose constraints on the transducer design. Lateral integration requires at least twice the size of the device or circuit for the integrated sensor chip. Parasitics are also added if signal path is disturbed or additional wire-bonding is needed.

The best method for integrating arrays of hair sensors with CMOS is by vertical integration, analogous to vertically-integrated (VI) CMOS image sensors that date back to as early as the late 1970s. Vertical stacking allows increased pixel-level data processing and device optimization. One advantage is that resistance and capacitance contributed by wirebond or long traces on PCB are replaced by shorted interconnections between the vertically-stacked dies, thus reducing RC delay as well as transmission power loss. The second advantage is that the number and density of signals passing between the CMOS and sensor dies is no longer limited by the perimeter or pad, but is rather limited by the technology in making reliable metallic interconnects with fine pitch, thus 3D stacked-integration has the potential to substantially increase the information flow. In addition, both the MEMS devices and CMOS chips/wafers can be optimally designed and fabricated in the mostly suitable technology [26].

For example, Skorka et al. [30] presented the design of vertically-integrated (VI) CMOS image sensors that are fabricated by flip-chip bonding where the sensor chip is composed of a

CMOS die and a photodetector die. Figure 1.16 shows two images of a CMOS chip compared with a VI-CMOS chip. VI-CMOS facilitate ADC per pixel to convert the readout to digital signals. Digital signals are more immune to noise while travelling outside the pixel to the output buffers and busses. There are also more degrees of freedom in photodetector design in a flip-fashion such as the depth of vertical photodetectors can be varied rather than being fixed by the doping profiles of the CMOS process.



(a) (b)

Fig. 1.16. CMOS image sensors (a) a CMOS die and (b) VI-CMOS prototype with a photodetector die stack on top of a CMOS die [30].

The performance gain and feasibility of implementing local signal conditioning circuitry in a 3D vertically-stacked sensor array-CMOS chip configuration depends on the suitable CMOS technology chosen and the needed footprint of the pixel sensor. Although for the VI-CMOS image sensor, due to more complex local circuitry, the spatial resolution of image sensor arrays may be degraded.

Flip-chip bonding for vertical integration can also provide high alignment accuracy and reliability with top surface metallurgy (TSM) patterned on the CMOS die post-CMOS fabrication using the aluminum bond pads from the CMOS process (with native aluminum oxide etched before metal stack deposition), and under bump metallization (UBM) on the

photodetector die. Each pixel has a bond pad (BP) and its area is limited by the pixel dimension. Two VI-CMOS image sensor prototypes with two different pixel dimension at $100 \times 100\ \mu m^2$ and $10 \times 10\ \mu m^2$ are shown in Figure 1.17.

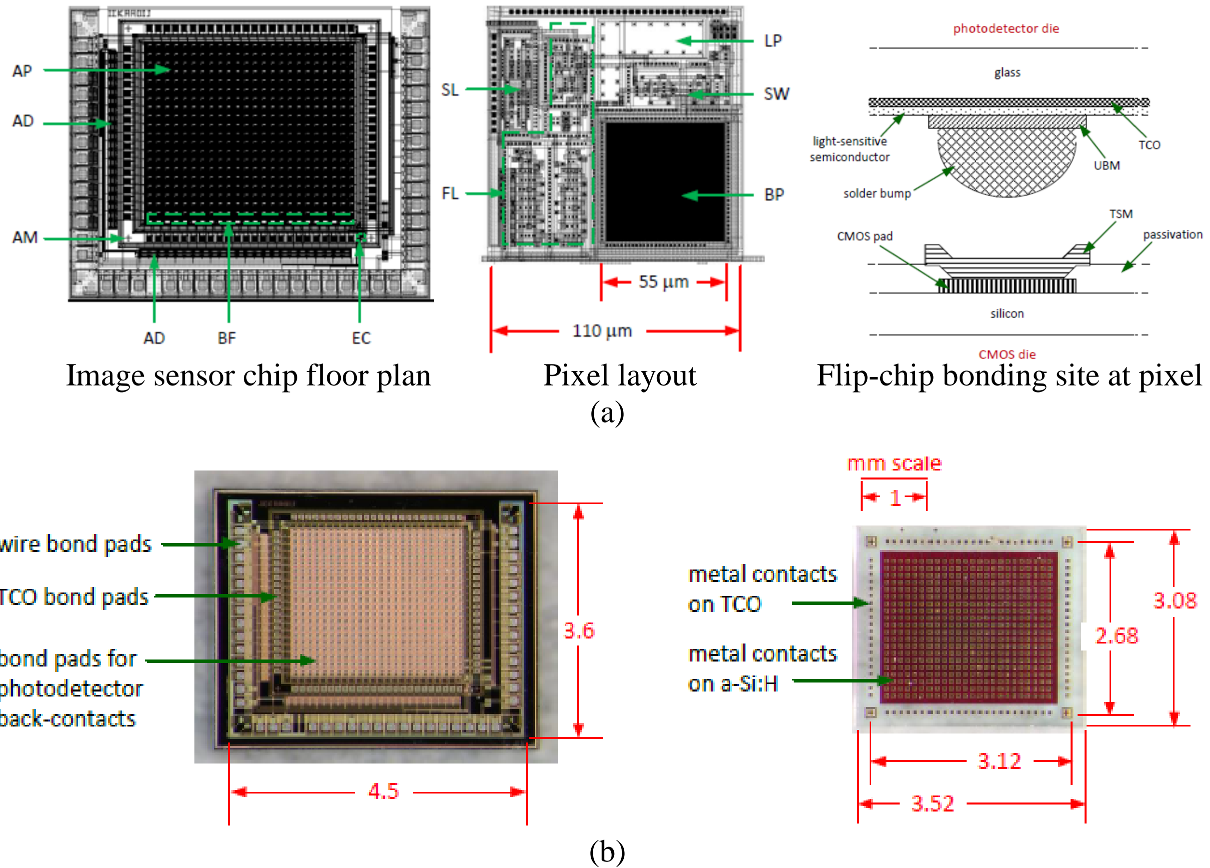


Fig. 1.17. VI-CMOS prototypes: (a) pixel dimension of $100 \times 100\ \mu m^2$; (b) pixel dimension of $10 \times 10\ \mu m$ pixel dimension of $100 \times 100\ \mu m^2$ [30].

1.2 Literature Reviews on MEMS Biomimetic Hair Sensors and Sensor Arrays

Previous works on bio-inspired hair-like sensors mostly focused on measuring drag force and velocity of flow either in air or water. It is most intuitive for engineering designs because the idea is to mimic hair in nature for similar functionalities.

These flow sensor designs (Figure 1.18) incorporate various mechanisms, enable directional sensitivity, use different transduction principles, and integrate myriads of materials for

operating in desirable environments. The out-of-plane tall hair-mimicking structures are realized either by curled up cantilevers, polymer manual assembly or multi-step lithography [34-39].

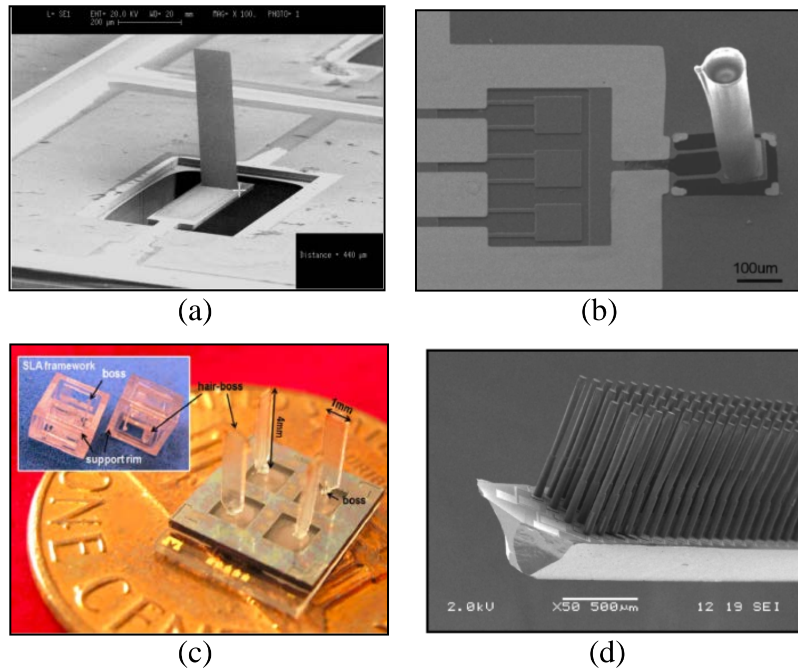
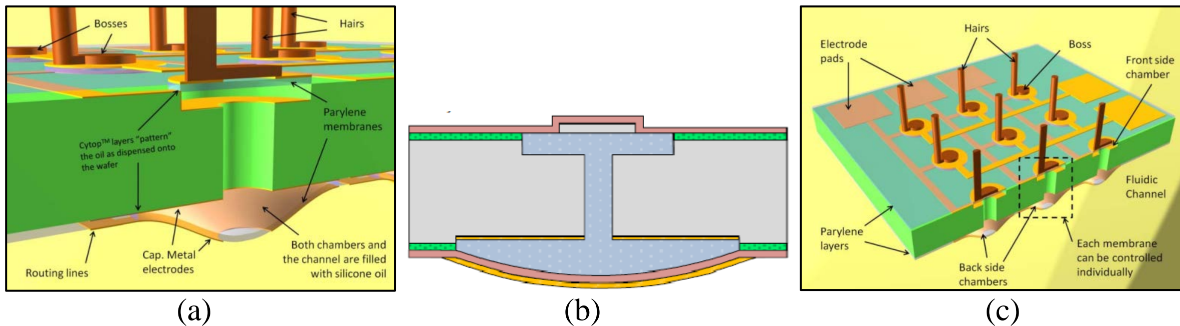


Fig. 1.18. Micromachined hair sensors in literature: (a) 820-µm tall cilium is curled up by plastic deformation magnetic-assembly with strain gauge attached [34] to mimic lateral line sensors in fish; (b) 700-µm tall SU-8 hair and strain gauges at their base [35]; (c) Directional air flow sensor array by stereo-lithography and MEMS micro-hydraulic structures [36-37]; (d) Arrays of SU8 hair by lithography. Capacitive sensing is at the base [38-39].

Both cantilever-based sensor and piezoresistive strain gauge embedded in the substrate plane occupy large surface area and limit the use of high-density arrays. Polymer hair manual attachment require separate assembly processes for the hair and transducer thus increase the overall process complexity and limits its potential integration with signal processing circuitry which is desirable for highly dense arrays.

Recent advancements in biomimetic hair sensors utilizing capacitive transduction at the base proved to be more effective [36-39]. Sadeghi et al. [36-37] reported a hair-based air flow sensor that converts drag force to pressure and uses microhydraulic structure for hydraulic

amplification of the signal and capacitive transduction. 2-D directional sensing is realized by hair appendages made using stereo-lithography. Two sensors perpendicularly positioned can quantify the air flow direction in the wafer plane.



(a) (b) (c)

Fig. 1.19. Micro-hydraulic structure with hair attached to bossed membrane. The base structure consists of top and bottom chambers and a pair electrodes for electrostatic actuation and capacitive sensing [36-37].

Researchers at Universe of Twente [38-39] have also developed an artificial hair flow sensor and interfaced arrays of these sensors with frequency-division modulation (FDM) circuits for flow pattern recognition (Figure 1.20). For each sensor, capacitive sensing relies on the tilting of a membrane by drag forces acting on the SU-8 receptive hair of the sensor, fabricated by surface micromachining technology. The 900 µm tall SU-8 hair is made by a sequential exposure procedure of two 50 µm-thick SU-8 layers. The thickness limitation of each layer is imposed by the maximum exposure thickness of only 700 µm due to UV light adsorption. The diameters of the ranges from 25-50 µm and capacitive gap is 0.6-1.0 µm. The 1 µm-thick SiRN (Silicon rich Nitride) torsional beams have lengths ranging from 75-100 µm and widths ranging from 5-10 µm. Superposition of the acoustic measurements at three different frequencies (10 Hz, 100 Hz and 400 Hz) on the flow-sensor are presented in Figure 1.20(b).

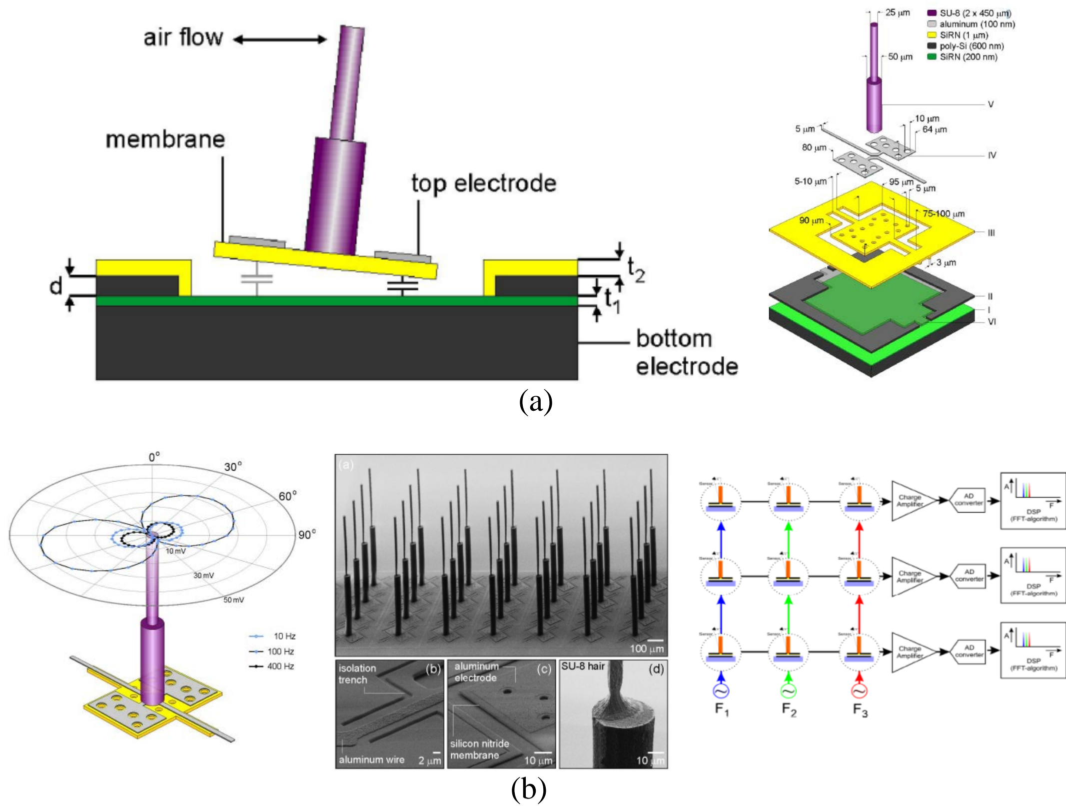


Fig. 1.20. Biomimetic flow sensor array with sensitivities on the order of 1 mm/s. (a) Operation: Capacitive transduction relies on the tilting of a membrane by drag forces acting on the SU-8 receptive hair of the sensor; (b) Superposition of the acoustic measurements at three different frequencies (10 Hz, 100 Hz and 400 Hz) on the flow-sensor. An array of sensors uses frequency-division modulation (FDM) circuits for flow pattern recognition [38-39].

1.3 Thesis Contributions and Organization

Thesis Contributions

The main technological contributions of this thesis are summarized as follows:

1) Design and analytical modeling of the 3D biomimetic high aspect-ratio hair-like microstructure as the basic sensing element for high density MEMS multi-transducer platform. Vertically anchored micromachined cantilever spring is introduced for the first time. It reduces single device footprint and enables dense transducer array formation. The 3D hair structure with increased aspect-ratio and device height can achieve competitive/superior performance compared

with traditional planar devices.

2) Develop and characterize an advanced Bosch deep-reactive-ion-etching (DRIE) process for realizing ultra-deep (1 mm) ultra-high aspect-ratio (UHAR) silicon structures with straight sidewalls across a wide range of feature sizes, and apply this well-characterized Bosch DRIE process to the microfabrication 3D high aspect-ratio hair structure.

3) Develop a two-gap double-sided silicon microfabrication process that takes advantage of the ultra-deep UHAR Bosch DRIE. The process allows the 3D hair structure design to be optimized for applications in MEMS inertial sensor fabrication.

4) Develop a CMOS-compatible wafer-level microfabrication technology for integration of MEMS device wafer with arrays of 3D hair sensors and CMOS circuit/interconnect wafer to realize multi-transducer microsystems.

5) Design, fabricate and test high performance capacitive accelerometer based on the 3D hair structure. Effective high aspect-ratio capacitive transduction along the direction normal to the wafer plane is embedded within the hair structure, resulting in a silicon MEMS accelerometer with low mechanical noise floor and high capacitive sensitivity per unit footprint.

6) Design, fabricate and test threshold accelerometer based on the 3D hair structure that achieves high threshold resolution and low power consumption within a small footprint. Effective contact-mode detection is formed at the top between the proof-mass and stationary electrodes.

7) Demonstrate the use of MEMS sensors arrays to extend full-scale range and introduce frequency selectivity. We build arrays of both capacitive hair accelerometers and threshold hair accelerometers consisted of devices with tailored structural dimensions in order to cover wide performance specifications in terms of full-scale acceleration levels and frequency spectrum.

Thesis Organization

This thesis is organized into eight chapters. Chapter 2 introduces the novel 3D high aspect-ratio biomimetic hair structure as the basis to build high performance hair sensor array. Both theoretical analysis and COMSOL FEA simulation are used to optimize the critical structural dimensions. This section also includes a discussion on two major design constraints imposed by critical microfabrication steps: 1) high aspect-ratio anisotropic deep-reactive-ion-etching (DRIE) process and 2) different bonding methods to provide both electrical connections as well as mechanical anchoring. Methods to overcome these constraints and analysis on the fabrication results will be discussed for every generation of hair accelerometer arrays in later chapters. Chapter 3 detailed a custom-developed deep-reactive-etching (DRIE) process that can be applied to the fabrication of the high aspect-ratio biomimetic hair structure introduced in Chapter 2. The new process can etch ultra-deep (> 500 μm) ultra-high aspect-ratio (UHAR) silicon structures ($AR > 40$ for 1 mm through-trench etch, $AR \approx 80$ for 500 μm through-trench etch, and $AR > 20$ for 500 μm through-hole etch), with straight sidewalls across a wide range of feature sizes. We overcome the challenges in Bosch DRIE by continuously ramping critical DRIE parameters throughout the process, including the 380-kHz bias power during etch step, the etch/passivation step duration, and the chamber pressure.

In Chapter 4, we applied the ultra-high aspect-ratio (UHAR) DRIE of 2-10 μm wide trench features to the first-generation uniform-gap capacitive hair accelerometer made from standard 500 μm thick silicon wafers based on a modified silicon-on-glass (SOG) process including 2-10 μm trench DRIE, metal interconnects patterning and anodic bonding. Proof-mass footprint varies from $200^2 \mu m^2$ to $500^2 \mu m^2$, and singe spring cross-section varies from $30^2 \mu m^2$ to $50^2 \mu m^2$. One array consisting of 25 identical elements (500 μm wide mass and 50 μm wide

spring) is measured to have 0.25 fF/g single-ended capacitive sensitivity.

Chapter 5 discusses the constraints of the uniform-gap devices from Chapter 4 and introduces a two-gap hair structure. Analysis and simulation verifies that narrow gap near the top of a tall device is sufficient to increase capacitive sensitivity. The device height (H) is not limited by DRIE etch and can be further increased. The two-gap design allows all the critical structural dimensions to be independently optimized. Major fabrication steps of the two-gap structures include ultra-deep (> 500 µm), ultra-high aspect-ratio DRIE and silicon-gold eutectic bonding.

Based on the two-gap hair structure, Chapter 6 presents the design, optimization and characterization of the second-generation low-noise high-sensitivity capacitive accelerometer arrays. Critical fabrication results regarding ultra-deep DRIE and silicon-gold eutectic bonding are discussed in detail. To further incase capacitive sensitivity per unit footprint, interdigitated electrodes and vertical spring thinning technique by isotropic plasma etch are proposed. We verify the arrays of accelerometer with various dimensions by resonance testing from 1 µTorr to 100 mTorr. The last section of the chapter presents the electromechanical testing results when devices are subjected to shaker motion. The device performance is compared with the state-of-the-art, achieving < 1 µg/√Hz noise floor and > 1 pF/g capacitive sensitivity by design.

Chapter 7 introduces the third-generation low-power wide-range threshold hair accelerometer arrays. The chapter starts with the motivation behind developing low-power microsystems and a review of existing works on threshold accelerometer arrays and acceleration switches. The interactive design optimization of the third-generation digital threshold hair accelerometer arrays considers both process capability (including critical gap defining steps and structural layers involved), and performance specifications (including acceleration threshold range, resolution, and bandwidth). The low noise and frequency selectivity nature of the hair

structure and arrays is inherited, and more importantly, the new designs aim to address power consumption since it is one of the limiting factors in the state-of-the-art wireless world of Internet of Things (IoT). Low power consumption is realized by switching from capacitive sensing to switch-mode detection, along with a low-power circuit block that can sense and capture the sensor arrays switching without affecting their operation. The micro-power consumption allows it to continuously monitor environmental shocks or vibrations in power limited systems, and is extremely critical when the sensor array size is expected to be scaled from less than 10 to 100s or even 1000s.

Chapter 8 summarizes the milestones and contributions of this research. Directions on future technology development, as well as suggestions for further development on both single hair sensor design and sensor array implementation are presented.

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Chapter 2 HIGH ASPECT-RATIO BIOMIMETIC HAIR STRUCTURE

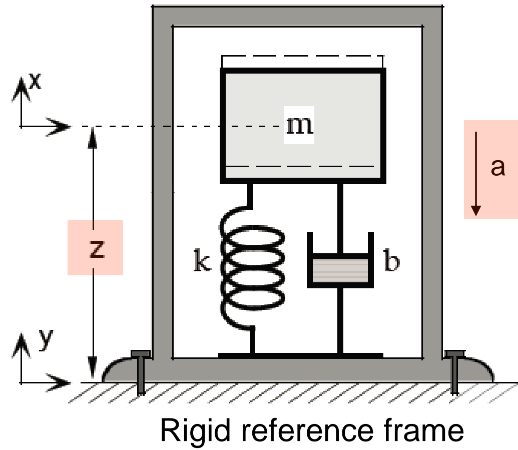
2.1 MEMS Accelerometer and Hair Structure Description

In this chapter, we proposed a biomimetic hair structure as the basis to build high performance hair sensor array. Its implementation as a micro-accelerometer will be presented.

Accelerometers are devices that measure the instantaneous change in platform velocity. To use accelerometer as motion sensors, the distance travelled can be calculated by integrating the acceleration output twice over time.

MEMS accelerometer typically has a proof-mass supported by a compliant spring. The spring is fixed to a rigid reference frame, where the acceleration of this rigid frame is to be measured as shown in Figure 2.1(a). When the rigid y-frame is going south under an acceleration a, the proof-mass will move north relative to the y-frame due to inertial force such that the acceleration can be calculated by measuring the relative motion of the proof-mass with respect to the rigid frames ($z = x - y$). In order to measure the relative motion z with a transducer design, with higher accuracy and lower mechanical noise floor, MEMS accelerometer requires large proof-mass and large transduction area to capture this change.

For a single mass-spring pair, it has a fixed resonant frequency $\omega_n = \sqrt{\frac{m}{k}}$ and the device is operated or usable at certain $\frac{\omega}{\omega_n}$ ratio below this frequency as a static accelerometer, determined by the damping ratio $\zeta = \frac{D}{\sqrt{km}}$ or quality factor Q.



$$z = x - y$$

$$z = \frac{m}{k} a = \frac{a}{\omega_n^2}$$

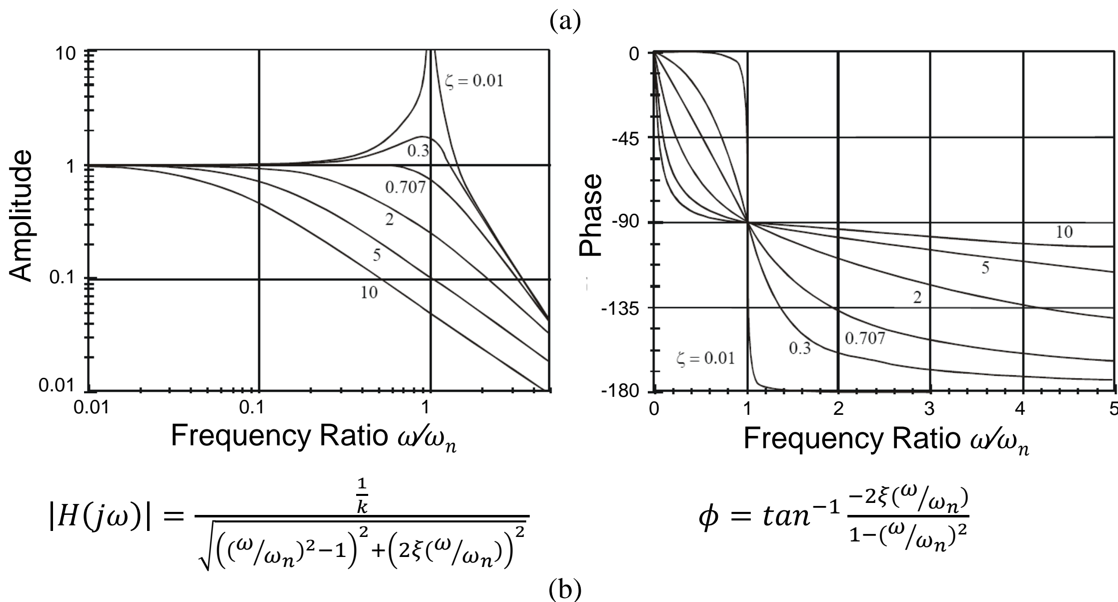
$$\omega_n = \sqrt{\frac{k}{m}}$$

Proof-mass Motion: $m\frac{d^2x}{dt^2} + D\left(\frac{dx}{dt} - \frac{dy}{dt}\right) + k(x-y) = 0$

Rigid Frame Motion: $y(t) = Ycos(\omega t)$

Acceleration: a

(a)



$$|H(j\omega)| = \frac{\frac{1}{k}}{\sqrt{\left(({}^{\omega}/_{\omega_n})^2 - 1\right)^2 + \left(2\xi({}^{\omega}/_{\omega_n})\right)^2}}$$

$$\phi = tan^{-1}\frac{-2\xi({}^{\omega}/_{\omega_n})}{1-({}^{\omega}/_{\omega_n})^2}$$

(b)

Fig. 2.1. (a) MEMS accelerometer: second order mass-spring-damper system. (b) Amplitude and phase response of the second order mass-spring-damper system.

As shown in the frequency response plot of the second-order system in Figure 2.1(b), above the resonant frequency ω_n, the proof-mass no longer moves relative to the rigid frame, acting as a vibrometer rather than an accelerometer; or it moves by orders of magnitude smaller distance than at frequencies lower than ω_n. Bandwidth (BW) is typically specified in dBs

(±1 dB, ±3 dB) with respect to the flat band-amplitude. For example, if the BW is specified for -3 dB, the $\omega_{-3\,dB}$ represents the frequency at which the output magnitude drops to about 70% (–3 dB) of the actual magnitude of movement that the accelerometer is experiencing. For example, if the damping ratio $\zeta = \frac{D}{\sqrt{km}}$ equals 0.707, the magnitude drops to –3 dB at the resonant frequency $\frac{\omega_{-3dB}}{\omega_n} = 1$; while for $\zeta = 2$ the magnitude drops to –3 dB at $\frac{\omega_{-3dB}}{\omega_n} = 0.267$.

However, since the accelerometer sensitivity $z = \frac{m}{\omega_n^2}$ decreases with larger ω_n, there's a fundamental tradeoff between ***sensitivity*** and ***BW*** for a single spring-mass-damper system. Table 2.1 listed the accelerometer selection criteria based on various applications, and these criteria cover a wide range of sensitivity and BW.

Table 2.1 Accelerometer Selection Based on Applications [1]

Measuring	Applications	Criteria	Operation
Motion	slow-moving, integrated to calculate velocity or displacement;	DC-response / zero offset error / SNR/ Thermal Zero Shift (TZS)	Piezoresistive; Variable Cap.;
High Frequency Vibration	gear noise analysis, turbine or high-speed rotating machinery monitoring;	high-speed rotating machinery monitoring / high resonance (several kHz to >10kHz / low sensitivity	Piezoelectric;
Low Frequency Vibration	modal analysis, building and bridge monitoring	no phase shift at low frequency / base strain sensitivity	Piezoresistive; Variable Cap.; Force-Balance Servo;
Shock	package drop-testing, automotive crash-testing, and pyroshock/simulation	zero shift/ localized material responses / usable output / survivability.	Piezoresistive;
Micro-G Vibration	vibration in space on the Hubble telescope, monitoring noise in a nuclear submarine;	High sensitivity / low noise floor / direction of earth's gravity / limited dynamic range	Variable Cap.; Force-Balance Servo;
Vibration on Small Objects	test articles are small	Light weight / Mass-Loading Effect / weight ratio <10:1 / mounting/ surface curvature	Piezoelectric;

Mass-spring-damper type MEMS accelerometers typically have the springs defined in the wafer plane. This approach has the advantage of precisely defining the width and length of the springs by layout, and precisely defining the thickness of springs by the thickness of substrate or deposited layers to adjust the spring stiffness. However, although meandered springs can be designed to reduce the footprint, the longest in-plane spring dimension increase the overall device footprint or chip area. For example, the Bosch BGA64 z-axis accelerometer defines both the torsional spring and proof-mass in the several-micron thick poly-silicon layer [2] in Figure 2.2.

Although current trend for commercial consumer-grade accelerometer chips is to target the thickness of the whole package at ~ 0.5 mm, extending the device thickness in the third dimension has the potential to improve performance and lower cost within smaller footprint.

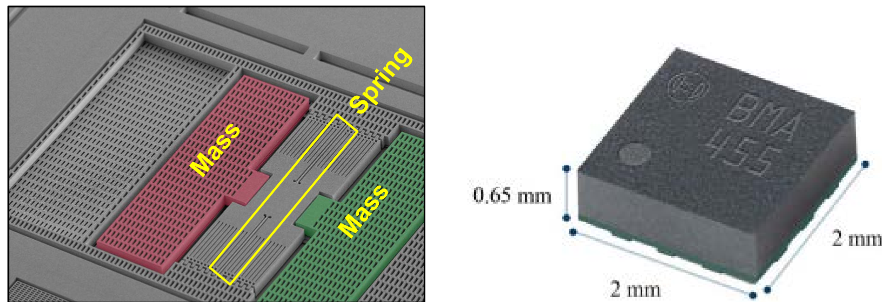


Fig. 2.2. Bosch BMA455 Accelerometer [2].

To overcome the limitations imposed by a planar spring and, we design a new device structure with the mechanical spring normal to the wafer surface. As shown in Figure 2.3(a), the vertical hair-like spring is anchored at the bottom end and supports a proof-mass at its center. The proof-mass also extends out of the wafer plane. The proof-mass is further surrounded by multiple electrodes, separated by a gap for capacitive transduction of motion. Critical design parameters of this structure implemented as a capacitive accelerometer include: device height (**H**), proof-mass footprint (**a**×**b**), spring length (**L**) and cross-sectional dimension (**c**×**d**), and the

nominal transduction gap (**g_0**).

Capacitive transduction is chosen because it can utilize the large area without increasing the footprint. This is because the hair-like transducer structure can have a larger dimension on the planes normal to the wafer surface than in the wafer plane, thus the taller the hair structure, the more transducing area there will be. Consider a planar mass (500 μm × 500 μm × 10 μm)–spring (5 μm × 500 μm × 10 μm) system where the 10 μm thick structural layer determine both the spring thickness and proof-mass thickness: if this system is implemented by the hair structure in Figure 2.4 where H = 1000 μm, a / b = 50 μm / 50 μm, and c / d / L = 5 μm / 10 μm / 500 μm, the overall footprint is reduced by 100 x.

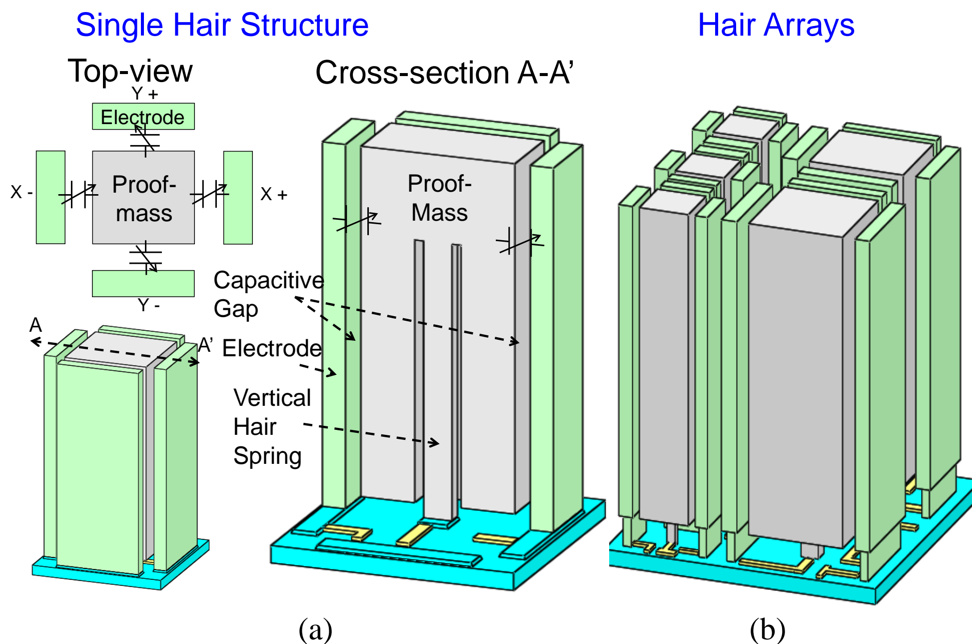


Fig. 2.3. Proposed biomimetic hair sensor structure: (a) Single biomimetic hair structure with vertical hair-like spring, tall proof-mass, and electrodes for capacitive sensing and actuation; (b) An array of hair structures with various dimensions.

2.2 Optimization of Hair Structure Design

The hair accelerometer structure in Figure 2.3 is studied as a vertical cantilever beam fixed at the bottom with a proof-mass attached to the other end. Finite element analysis (FEA) is

performed using COMSOL Multiphysics® version 5.1 combining the solid-mechanics module and the electrostatic module to study the sensor response to in-plane lateral acceleration (Figure 2.5). Since the spring cross-section is designed to be rectangular, for the first bending mode, the spring-mass bends along one of the two orthogonal axes toward one of the electrodes. The side electrodes are stiffer than the hair spring by > 100 x.

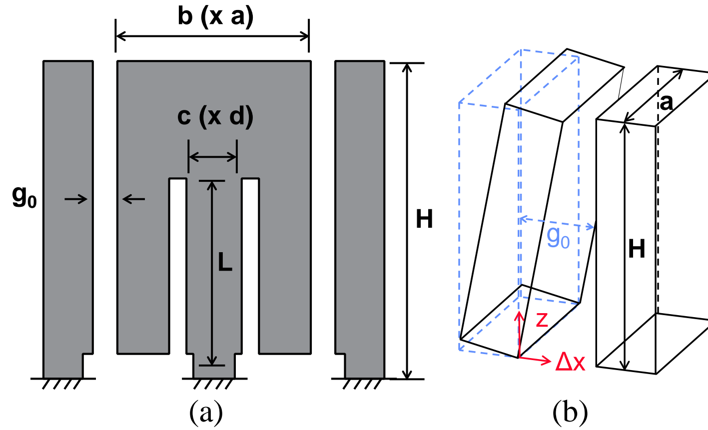


Fig. 2.4: (a) Critical design parameters of the hair structure; (b) Gap profile when lateral acceleration is applied.

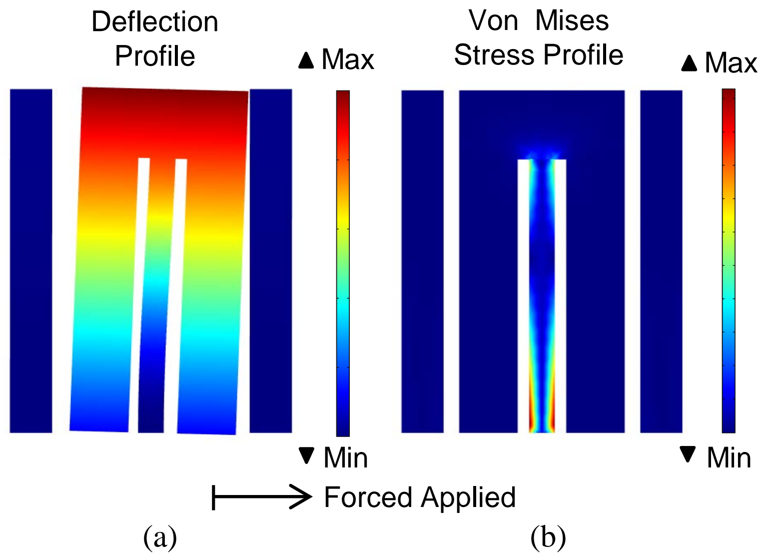


Fig. 2.5. COMSOL simulation results showing: (a) Deflection profile and (b) von Mises stress profile of the hair structure along the axis of acceleration applied under in-plane lateral force. Maximum stress is at the anchor of the vertical hair spring.

Since the top of a vertical inverted pendulum (proof-mass) undergoes the maximum deflection, the gap profile between the proof-mass and electrode can be approximated as a trapezoidal shape. When the proof-mass is displaced under external acceleration (*Accel.*), the displacement, $\Delta x_{max}(z)$, along the side of the proof-mass is derived as a simple mass (*Mass*) attached to a spring of stiffness (*k*), and the maximum displacement, $\Delta x_{max}(H)$, at the top along the mass sidewall are:

$$\begin{aligned}\Delta x_{\max}(z) &= \Delta x(L) + \Delta x'(L)(z-L) \\ &= \frac{m \times Accel.}{k}\frac{1}{2L^2}[3(2h-L)z-(3h-2L)L],\ \mathrm{h}=\frac{\mathrm{L+H}}{2}\end{aligned} \tag{2.1}$$

$$\Delta x_{\max}(z) = \frac{m \times Accel.}{k}\frac{1}{2L^2}(12h^2-15Lh+5L^2) \tag{2.2}$$

The displaced gap dimensions at the top and at the bottom are:

$$g_{top}(H) = g_0 - \Delta x_{\max}(H),\quad g_{bot}(0) = g_0 - \Delta x_{\max}(0) \tag{2.3}$$

Thus, the capacitance when acceleration is applied compared to the initial capacitance are:

$$\begin{aligned}C_1 &= \varepsilon \times Area \times \frac{1}{g_{top}(H)-g_{bot}(0)}\ln\left(\frac{g_{top}(H)}{g_{bot}(0)}\right) \\ C_0 &= \varepsilon \times Area \times \frac{1}{g_0}\end{aligned} \tag{2.4}$$

When the displacement is small, the change in capacitance can be approximated by Taylor expansion as:

$$\Delta C = C_1 - C_0 \approx \frac{1}{2}\varepsilon \times Area \times \frac{m}{k} \times \frac{1}{g_0^2} \times Accel. \tag{2.5}$$

$$S = \frac{\Delta C}{Accel.} \propto \frac{1}{2}\varepsilon \times (a \times H) \times \frac{abH}{dc^3/L^3} \times \frac{1}{g_0^2} \tag{2.6}$$

From Equation (2.6), we can see that the sensitivity (S in Farad/g) is inversely proportional to $1/g_0^2$ and scales with the proof-mass size (a, b, H), the sensing area (a, H) and the

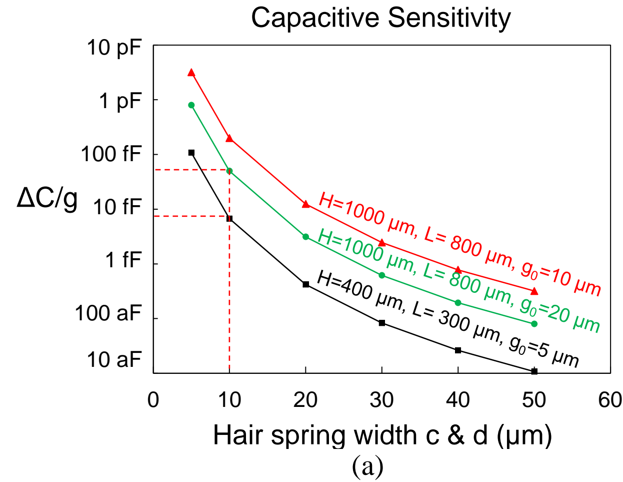
spring dimensions (c, d, L). A taller H also allows for longer vertical spring L. For example, a 1000 μm tall device can have a spring with L > 800 μm, while a 400 μm can only have a spring with L > 300 μm. Thus, device height H plays a critical role in improving the sensitivity for this design by utilizing the third dimension.

Figure 2.6 presents the effect of varying different design parameters. For example, a 1 mm thick device can have 800-900 μm long spring, while a 400 μm thick device can only have a 300 μm long spring. Thus, a thicker device with larger H will increase sensitivity. When the device height H is varied, the achievable minimum uniform sensing gap size will also change due to deep reactive ion etching (DRIE) limitations. As shown in Figure 2.6(a), for a 500^2 μm^2 footprint (a = b = 500 μm) hair structure with various spring diameter (for example, c = d = 10 μm), within a quarter of a mm-squared footprint, the 1mm thick device has more than 5 times higher sensitivity than the 400 μm thick device, even with a 20 μm air gap (4 times larger than a 5 μm gap).

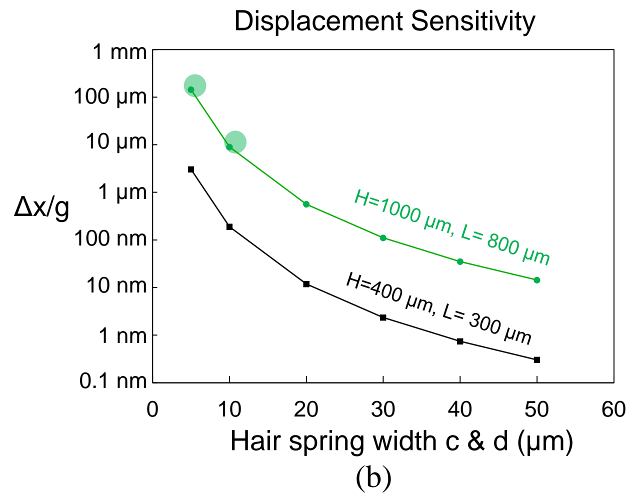
Due to the tradeoff between BW and sensitivity, the 1 mm thick device has f_n around 166 Hz while the 400 μm device has f_n around 1143 Hz since the resonant frequency of a mass-spring system is,

$$\omega_n = \sqrt{\frac{k}{m}}. \tag{2.7}$$

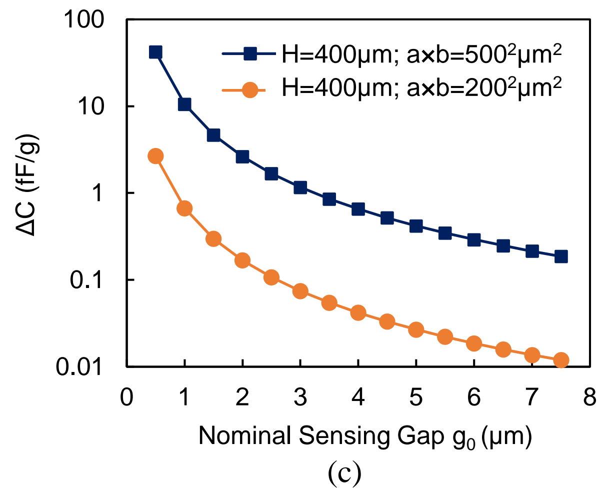
In addition, the thinner the spring, the more compliant it is and the higher the displacement sensitivity (Figure 2.6(b)) as well as capacitive sensitivity for the same proof-mass. If the spring is 10 μm wide, even with 20 μm air gap, this device has very high sensitivity of 50 fF/g. It can achieve even higher sensitivity at almost 800 fF/g if the spring can be further reduced to 5 μm wide.



(a)



(b)



(c)

Fig. 2.6. Sensitivity: (a) $\Delta C/g$ for $500^2\ \mu m^2$ footprint with various device height H, spring dimensions, and nominal sensing gap; (b) Displacement sensitivity; and (c) Comparison of $200^2\ \mu m^2$ and $500^2\ \mu m^2$ proof-mass footprint devices for various nominal sensing gaps as small as $0.5\ \mu m$.

Sweeping the capacitive gap from 0.5 μm to 7.5 μm, we show that a smaller sensing gap (<1 μm) can greatly increase the sensitivity per unit footprint by comparing a 200^2 μm^2 footprint (a = b = 200 μm) and a 500^2 μm^2 footprint (a = b = 500 μm) hair structure (Figure 2.6(c)).

However, since the Brownian noise associated with the squeeze film damping effect in air (Equation (2.8) BNEA is the Brownian noise equivalent acceleration in g/√Hz) increases significantly with reduction of the gap opening, we should not reduce the gap indefinitely.

$$BNEA = \sqrt{\frac{4k_B TD}{M^2}} = \sqrt{\frac{4k_B T\omega_0}{MQ}} \propto \frac{1}{gap^{3/2}} \tag{2.8}$$

Therefore, the proof-mass size is a more effective design parameter since both sensitivity and Brownian Noise Equivalent Acceleration (BNEA) are improved with a larger proof-mass.

2.3 Design Constraints Imposed by Critical Fabrication Steps

2.3.1 Nominal Sensing Gap and Device Height Constraints Imposed by DRIE

To build the 3D high aspect-ratio biomimetic hair structure, critical in-plane dimensions are precisely defined by photolithography. Creating 3D structure into the depth of the silicon wafer heavily relies on 3D microfabrication techniques. Challenge arises when both tall structure and high aspect-ratio electrostatic transduction gaps are desired.

Researchers have developed several fabrication methods for making small transduction gaps for MEMS devices [4-22]. For effective gaps of several microns, the gap height is typically less than 150 μm [6-8]. HAR submicron gaps are achievable for gap height at a few tens of microns [6, 8, 12, 13], while other submicron [9] or sub-100 nm gaps [10] are only found in thin (several microns) RF resonators that are surface micromachined. Table 2.2 summarizes these various methods.

Among these methods, sacrificial material is most frequently chosen to precisely define HAR gaps at 1 - 2 μm or submicron range [6, 8, 12, 13]. Timing in gas or liquid phase release etching is sensitive and limit the proceeding or subsequent process steps. In addition, the processes result in larger total chip area than the active device to ensure structural integrity. Fabrication process in [6] combines two-sided surface micromachining, bulk micromachining and sacrificial oxide patterning. Full wafer thickness is achieved with the 1.5 μm sensing gap and thickness of 70 μm. Silicon dioxide is used as sacrificial layer and the device is released in HF after anisotropic wet etching of the SCS proof-mass in EDP. Another example is the submicron gap SCS resonators/accelerometers/gyroscopes made by HARPSS or HARPSS-SOI process [8, 12, 13] where sacrificial oxide is also used to define the gap dimensions. The effective thickness is bonded in the range of 30 - 150 μm with corresponding gap dimensions definable in the range of 0.1-2 μm. Timing in gas or liquid phase release etching limits the maximum thickness achieved for a minimum gap dimension. Although the device thickness may be increased by back-side processing of the substrate silicon in SOI wafers [8], effective sensing/actuation areas are limited to few tens of microns because of the device layer thickness and back-filling limitations.

Work has also been done toward the possibility of enhancing the etching properties of photo-assisted electrochemical etching in hydrofluoric acid to create HAR gaps and to replace DRIE. Sub-200 nm gaps with ultra HAR of 125:1 has been demonstrated but the height is limited to less than 25 μm [15]. Most literature to date only tested uniformly patterned bars, circles or rectangles [14-17]. Factors including composition of electrolyte, applied bias and photo-intensity of the light source combined affect the etching profile, repeatability and reproducibility.

These existing methods are complicated and not applicable to or optimal for 3-D, small-footprint, thick devices. Wet processing also limits the process window for integrating with other parts of MEMS structure and potential integration with CMOS circuits.

Over the last few decades, deep reactive ion etching (DRIE) has become one of the key processes in making high aspect-ratio MEMS [3]. The widely-recognized Bosch process alternates between passivation step and etching step to create almost vertical sidewalls.

Table 2.2: Various methods of making small high aspect-ratio capacitive transduction gaps

Methods of Making Gaps	Gap	Gap Height	Applications	Reference
Modified SOG	5 µm	400 µm	Inertial Sensors	[4]
Sacrificial HTO, electroplated Au electrodes and poly-silicon structure.	0.6 µm	6 µm	RF Resonators	[9]
Minimum width PR by i-line lithography, and further reduced by O2 plasma	50 nm minimum	1.5 µm	RF Resonators	[10]
SCREAM	Several microns	10 - 20 µm, < 100 µm	Inertial Sensors	[11]
DRIE CMOS-MEMS	1.8 - 2.1 µm	4.9 µm gap 10 - 100 µm backside SCS membrane	Inertial Sensors	[21-22]
SOG	3.2 µm, 5 µm	35 - 140 µm	Inertial Sensors	[18-20]
HARPSS	0.1 - 2 µm	30 - 150 µm	RF Resonators, Inertial Sensors	[6, 9, 12, 13]
Photo-assisted electrochemical etching in electrolyte	Submicron to several microns	10 - 300 µm	Uniformly patterned bars and trenches	[14-17]

We have developed an advanced Bosch DRIE process for etching ultra-high aspect-ratio (UHAR) trenches in silicon [4-5], this process has also been applied to the fabrication of a single-crystal-silicon vibratory cylindrical rate integrating gyroscope (CING) [25]. In order to achieve large proof-mass height (H) and gap g_0, this Bosch DRIE process ramps several critical process parameters including chamber pressure, etch power, passivation time and etching time.

Due to aspect-ratio-dependent etch (ARDE) and etch limitation, there is a direct correlation between the trench opening and etch depth. Further improvements of this Bosch DRIE process will be described in detail in Chapter 3.

An aspect ratio of 80 was achieved for a 400 μm deep trench with 5 μm originally defined on the mask, and 300 μm deep for 2 μm gap originally defined on the mask. This process is optimized for trench opening from 2 -6 μm as presented in Figure 2.7 (blue dots).

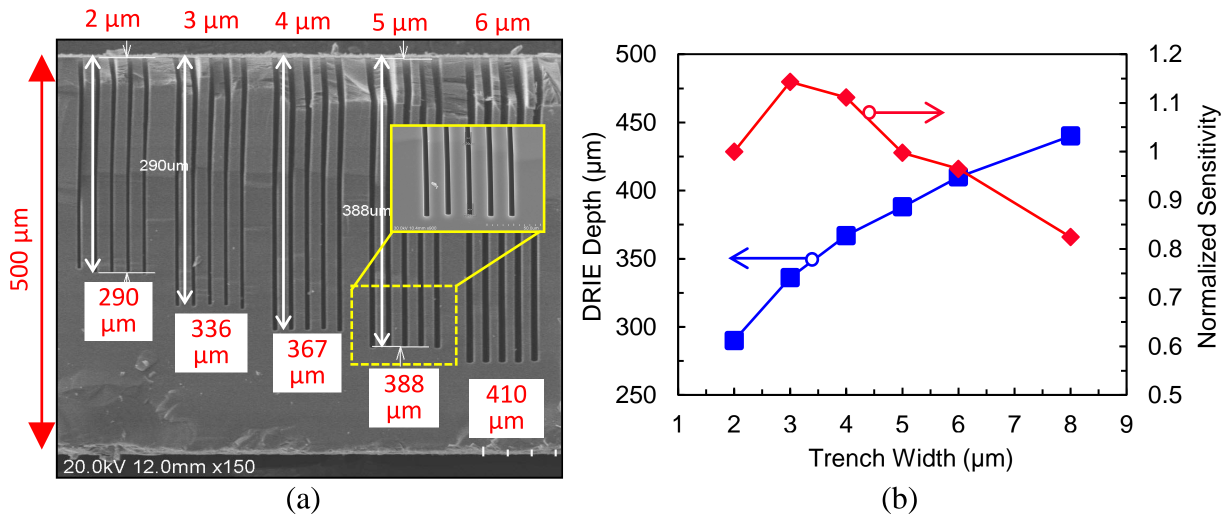


Fig. 2.7. Ultra-HAR DRIE characterization: (a) SEM cross-section of UHAR DRIE for 2 μm – 6 μm gaps; (b) DRIE depth vs. gap width (red) and the normalized capacitive sensitivity when this width/depth combination is used as the capacitive sensing gap.

We apply these HAR silicon DRIE etching results of narrow trenches from 2-10 μm to the hair accelerometer design [5]. Ideally a uniform narrow gap is desired to achieve very high capacitive sensitivity. Compare a sensor with H = 500 μm / L = 400 μm to a sensor with H = 1 mm / L = 900 μm, the latter has sensitivity of more than 45x assuming the same g_0, the same footprint, and the same spring cross-section according to Equation (2.6). However, it is very challenging to produce a 2-5 μm gap to a depth of 1 mm. If the DRIE width/depth data (blue dots) in Figure 2.7(b) are applied to g_0 and H (with L = H – 100 μm), and are assumed to be the only design variables, it is shown that the capacitive sensitivity will be reduced for a larger H.

This is because the increases in H and L are compromised by the wider sensing gaps that are needed to etch a greater depth.

2.3.2 Shock Survival Constraints Imposed by Hair Spring Bonding Strength

When in-plane lateral bending force (x-axis and y-axis) is applied, von Mises stress analysis by COMSOL shows that the maximum compressive and tensile stress is present near the bonding site where the hair spring is anchored to the lower substrate (Figure 2.5(b)).

During a high-g-shock event in the in-plane directions, the maximum distance traveled is limited by the initial transduction gap g_0, although in some cases, a different shock-stop gap distance less than g_0 can be included to further contain the motion. Thus, the maximum stress a design can possibly experience before failure is the greater of either the maximum stress when full-gap distance is traveled (Equation (2.11)), or the yield bond strength of a specific bonding method.

$$\Delta x_{max_bending} = \frac{FL^3}{3EI} = \frac{(m \times Accel) \times L^3}{3E(dc^3/12)} \tag{2.9}$$

$$\sigma_{max_bending} = \frac{FLt}{2I} = \frac{(m \times Accel) \times L \times c}{2(dc^3/12)} \tag{2.10}$$

$$\sigma_{max_bending}(\Delta x_{max_bending} = g_0) = \frac{3E g_0 c}{2L^2} \tag{2.11}$$

The von Mises stress profile along the length of the hair spring is simulated and presented in Figure 2.8(a). Using Equation (2.11), we plot the maximum stress at the spring anchor vs. different spring width (c = 10 – 30 μm, d = 30 μm) when full-gap distance (2 μm) is traveled (Figure 2.8(b)) for two device dimensions: H = 1 mm / L = 600 μm and H = 500 μm / L = 400 μm, and with typical device footprint at 500^2 μm^2.

40 MPa yield/fracture strength is assumed for a specific bonding method and the materials' tensile/fracture strength near the bonding interface. For H = 1 mm / L = 600 μm

(Figure 2.9(a)), if the spring width is smaller than c = 28.75 μm, even when the full-gap distance is traveled, the maximum stress will not exceed 40 MPa. The structure can survive very high-g shock with the counter-electrode as a shock stop. However, if the width is set to c = 30μm, the bond will fail before it reaches the counter-electrode. Either a separate shock stop gap needs to be included or the maximum acceleration must be much smaller than 55.8 g. If the yield/fracture strength of the bonding method and the materials' tensile/fracture strength near the bonding interface is less than 20 MPa, the springs will need to be much thinner (< 15 μm) otherwise they should not be subject to acceleration greater than 10 g.

Similarly, for H = 500 μm / L = 400 μm (Figure 2.9(b)), when the spring width c < 12.5 μm, the structure can survive very high in-plane g-shock.

Comparing Figure 2.9(a) and (b), a longer spring will allow for a wider spring, which will also enable the design to withstand larger z-axis g-shock and increase the available bonding area.

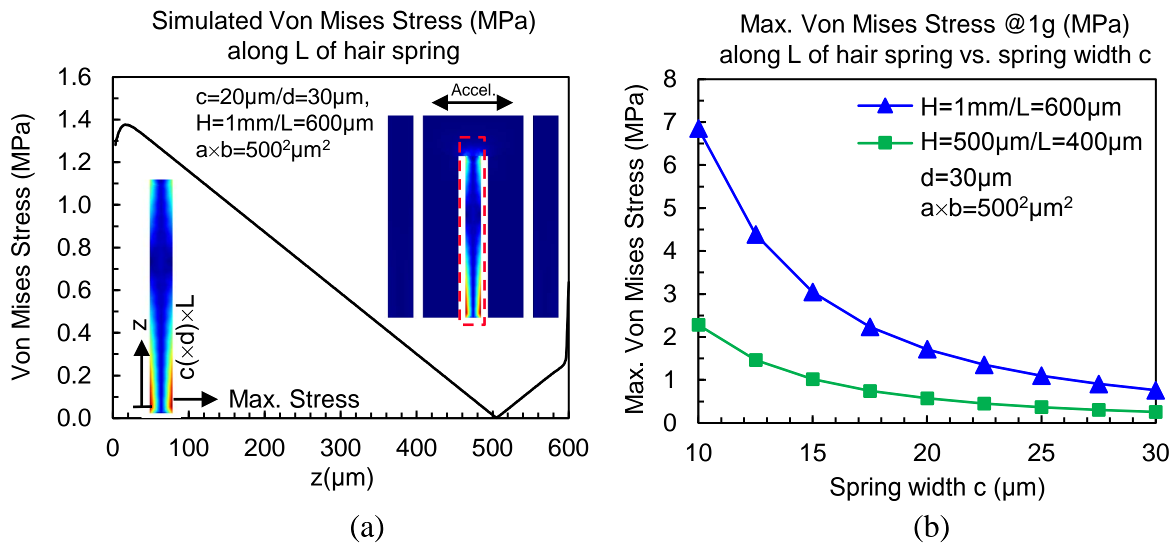
The greater vulnerability is due to out-of-plane z-axis high g-shock unless constraints were also designed to limit the out-of-plane motion. The bond strength is also bounded by the yield bond strength of the bonding method being used. For the same tensile longitudinal load F, a thinner vertical hair spring (smaller cross-section) will lead to great normal stress. For a device with c = 10 μm, d = 30 μm, L = 600 μm and H =1000 μm, at 1000g acceleration, $\sigma_{longitudinal}$ is calculated as 19 MPa.

$$\sigma_{long.}(z) = \frac{F}{A_{bonding}} = \frac{Mass \times Accel.}{d \times c} \tag{2.12}$$

If a larger proof-mass and a more compliant spring is needed for reduced noise and higher sensitivity, the maximum g-shock will be further reduced because the z-axis loaded stress

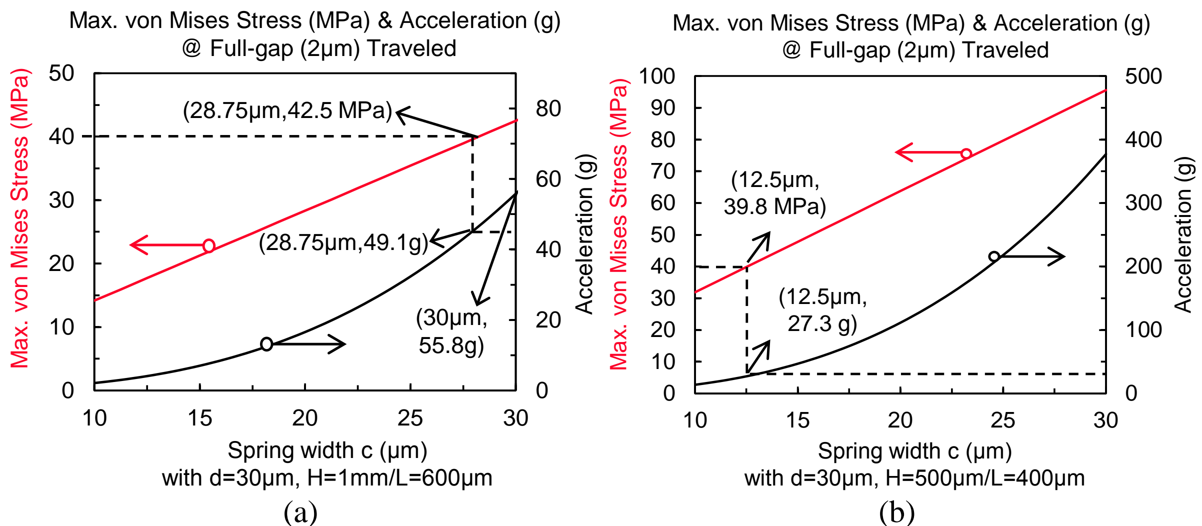
will be increased for the same input out-of-plane acceleration. Whereas the in-plane shock limit is independent of the proof-mass size.

Therefore, the in-plane g-shock requirement sets an upper limit on the spring width c (Equation (2.11)). And the out-of-plane g-shock requirement sets the minimum spring width c (Equation (2.12)).



(a) (b)

Fig. 2.8. Maximum von Mises stress analysis for in-plane motion for proof-mass footprint $a \times b = 500^2\ \mu m^2$. (a) von Mises stress profile along the deflected hair spring; (b) Max. stress for different spring design.



(a) (b)

Fig. 2.9. Maximum stress and the corresponding acceleration at full gap $g_0 = 2\ \mu m$.

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Chapter 3 ULTRA-HIGH-ASPECT RATIO DEEP REACTIVE ION ETCHING IN THICK SIILICON

In order to realize the high aspect-ratio biomimetic hair structure introduced in Chapter 2 and extend the device height beyond standard 500 μm thickness, new enabling technology must be developed in fabricating 3D high aspect ratio features in silicon.

The development, experimental results, and analysis of the ultra-high-aspect ratio deep reactive ion etching (UDRIE) recipe presented in this chapter have been submitted to the Journal of Microelectromechanical Systems (JMEMS) for peer review in December 2017. The experiments were done in collaboration with Amin Sandoughsaz and Kevin Owen in the Lurie Nanofabrication Facility (LNF) at the University of Michigan.

3.1 Enabling Technology: Deep Reactive Ion Etching (DRIE)

Deep reactive ion etching (DRIE) has become a cornerstone of microfabrication technologies since its introduction in the 1990s [1]. The most prevalent DRIE processes are the Bosch DRIE process [1,5,6] and the Cryogenic DRIE process [1-4]. Bosch process is a time-multiplexed dry plasma etching process [1], and is based on a sequential recipe alternating between a passivation sub-cycle and an etching sub-cycle to achieve deep and high aspect-ratio (HAR) anisotropic etching. The passivation step isotropically deposits a polymeric layer on the bottom and sidewalls of the etched structures, serving as a protective layer against the following

etching step. In the next sub-cycle, the directional ion bombardment first removes the passivation layer at the bottom and then the fluorine radicals etch the underlying silicon, while the sidewalls remain protected. Two fluorine-based chemistries such as SF_6 and C_4F_8 gas species are switched on and off during each step. For nanoscale structures less than 100 nm etched up to several microns to tens of microns deep, cryogenic process is generally preferred over the Bosch process [1-4]. This is because the cyclic nature of the Bosch process forms undulating sidewalls called scallops that measure tens of nanometers wide from peak to valley; whereas the sidewall passivation mechanism of the cryogenic etch relies on the formation of 10-20 nm thick oxide/fluoride (SiO_xF_y) on the sidewalls. This passivation is not easily attacked by the fluorine radicals at cryogenic temperatures (around -110 $^{\circ}$C). The other advantage is that lower temperature yields lower sidewall etch rate and increases dry etch resistance of masks (organic, oxide, etc.). Issues with cryogenic etch include cracking of standard mask materials at low temperatures and deposition of etch by-products on the cold substrate. These shortcomings restrict usage of this technique [2-3]. Other DRIE processes are reported using alternative reacting gas species including a non-sequential plasma-based DRIE process [7-10]. Among these different DRIE processes, Bosch process is an industrial standard etching process.

There exist a broad range of applications that can benefit from ultra-deep (>500 µm) silicon DRIE with ultra HAR: 1) capacitive inertial MEMS transducers that have reduced mechanical noise floor and increases sensitivity [11-13]; 2) micrometer to millimeter scale devices that can better emulate their macroscopic counterparts [16-18, 22-24]; and 3) through-silicon-via (TSV) as well as plasma dicing for IC integration [19-21]. For inertial MEMS, Tang et al. [11] concluded that DRIE beyond standard 500 µm silicon allows realization of a taller thus larger proof-mass per unit footprint. This greatly reduces the thermal mechanical noise floor thus

reducing the minimum detectable signal. Apart from inertial MEMS, DRIE can also be applied to making myriad of physical devices of sizes ranging from hundreds of microns, to several millimeters such as miniaturized optical instruments [16-17], micro-motors and micro-turbines [22-24], antimatter trap arrays [25], thick and HAR silicon molds for biotechnology applications [26-27]. For example, Narimannezhad et al. [25] built very deep (10 cm) and HAR micro-Penning-Malmberg trap arrays to store antimatter by stacking two hundred 500 μm-thick silicon chips patterned with 100 μm diameter tubes DRIE etched through the thickness. Smaller-diameter tubes etched through thicker silicon wafers would be preferred since trapped positron density is proportional to the inverse square of the trap radius. As for through-silicon via (TSV) fabrication, the current trend is to increase the via depth for the same diameter, because adopting thicker substrate helps addressing thermal dissipation and warp issue [19-21]. TSVs are widely demanded in both MEMS device and IC fabrication for hybrid packaging and three-dimensional die stacking. Deep DRIE is the best choice for forming TSVs due to its patterning accuracy, controlled etch profile, and high selectivity to masking materials. Other than TSVs, DRIE can also be applied to wafer dicing during IC packaging. Traditional blade dicing can cause silicon chipping that results in lower yield. The dicing streets width is determined by the blade thickness thus removing valuable "real estate". Dry plasma DRIE dicing has the advantages of improved throughput, narrower widths, clean edge, and can take advantage of deep and HAR silicon trench etch.

The depth of silicon DRIE in literature is typically limited to <500 μm. Our goal in this research is to achieve ultra-deep (>500 μm) etch in silicon wafers with HAR and vertical sidewall profile.

However, obtaining these features is challenging due to several shortcomings of the

standard Bosch DRIE process with fixed etch and passivation sub-cycle parameters. These shortcomings include: 1) aspect-ratio dependent etch (ARDE) induced sidewall tapering ($\theta<90°$ defined as positive and $\theta>90°$ defined as negative), etch termination (instantaneous etch rate equals zero), and DRIE-lag ($W_1>W_2>W_3 \rightarrow h_1>h_2>h_3$); 2) pattern dependency, i.e., trenches with the same width as the diameter of circular holes etch faster ($W_{trench}=\Phi_{hole} \rightarrow h_{trench}>>h_{hole}$), as illustrated in Figure 1(a); and 3) mask selectivity. These shortcomings are observed even when the depth of silicon DRIE is limited to <500 μm [1, 5, 6].

To address these DRIE shortcomings, we develop an advanced Bosch DRIE process: ultra-deep and ultra-high aspect-ratio (UHAR) etch with straight sidewalls are achieved by continuously ramping various process parameters including the 380 kHz bias power during etch step, the etch sub-cycle and passivation sub-cycle duration, and the chamber pressure during both sub-cycles.

Efficacy of the developed recipe is verified by fabrication results and schematically illustrated in Figure 3.1. Trenches with width as small as 2-5 μm are etched in 500 μm thick silicon with reduced undercut, achieving AR exceeding 80:1. Through 1 mm thick silicon etches are demonstrated with trenches with width as small as 25 μm, equivalent to AR of 40:1. 10-20 μm wide trenches are also etched to depths of 600-800 μm in 1 mm thick silicon wafers, with greatly suppressed ARDE effect. Sidewall slopes of narrower trenches (<10 μm) are slightly positive (>89.50 °) whereas those of wider trenches are readily tuned by adjusting process parameters to achieve either positive or negative slopes. The sidewall profiles (≈90 °) and flat trench bottoms indicate the etching recipe has not reached its limits and greater etch depth exceeding 1 mm is feasible. Furthermore, circular holes with various diameters as small as 25-35 μm are etched through 550 μm thick silicon wafers with slight positive sidewalls (AR≈20).

This advanced Bosch DRIE process offers new opportunities for applications ranging from through-silicon via (TSV) in 3D CMOS integration to emerging micro and meso-scale MEMS devices that demand ultra-deep and ultra HAR DRIE with precise feature control.

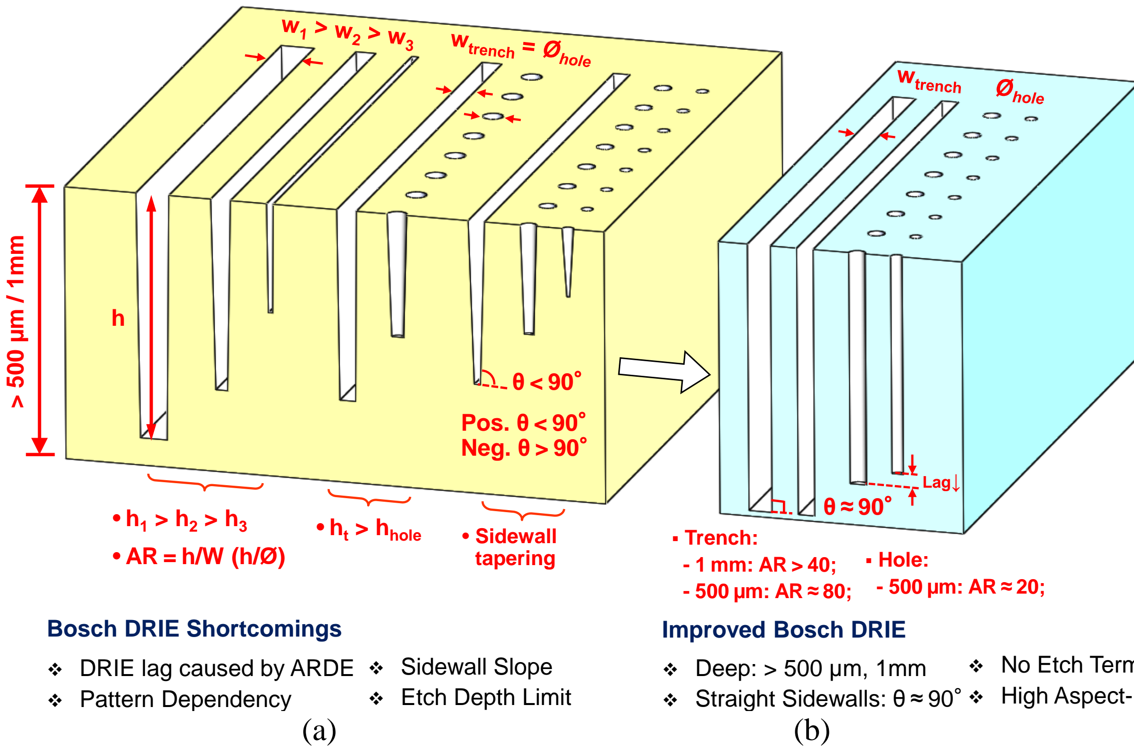


Fig. 3.1. Ultra-deep ultra-high aspect-ratio etching of thick silicon wafers (≥ 500 µm) with straight sidewalls across a wide range of feature sizes and patterns using an improved Bosch DRIE process. Shortcomings of the standard Bosch DRIE process with fixed etch and passivation sub-cycle parameters include:1) sidewall slope ($\theta < 90°$ defined as positive and $\theta > 90°$ defined as negative), etch termination (instantaneous etch rate equals zero), and DRIE-lag ($W_1 > W_2 > W_3 \rightarrow h_1 > h_2 > h_3$), all caused by ARDE; and 2) DRIE pattern dependency ($W_{trench} = \Phi_{hole} \rightarrow h_{trench} > h_{hole}$). These shortcomings are addressed by continuously ramping the Bosch DRIE etch and passivation sub cycle parameters (plasma power, step duration, and chamber pressure) throughout the process. The achieved aspect-ratios (W/h for trenches, Φ/h for holes) are greatly increased and sidewall slopes approach 90 °. No etch termination is observed.

3.1.1 Shortcomings of Standard Time-Multiplexed Bosch DRIE

In this section, we will briefly review shortcomings of the standard Bosch DRIE process including ARDE induced defects (tapered sidewall, etch termination, DRIE lag) and pattern

dependency. Selectivity of etching mask materials will also be discussed.

A. Aspect-Ratio Dependent Etch (ARDE)

Aspect-ratio (AR) is typically defined as the ratio of the etched feature depth into the wafer plane and the feature width or opening size. ARDE in silicon DRIE is a well observed phenomenon where the etch rate significantly decreases as the etch depth or the AR of the feature increases. It is generally caused by the depletion of reactive species at the bottom of the etched feature due to the limited Knudsen transport of the gas species, as well as by the reduction of ion bombardment.

ARDE results in: 1) tapered sidewall profiles, 2) etch termination, and 3) DRIE lag. These artifacts limit the maximum achievable etch depth and maximum AR.

Due to ARDE, sidewall becomes tapered at higher AR, and eventually the trench sidewalls converge to a point and etch terminates. The sidewall, whether positive ($\theta < 90\,°$ as shown in Figure 3.1) or negative ($\theta > 90\,°$), will degrade the performance of certain microfabricated devices. For example, in capacitive MEMS devices, the critical capacitive gaps defined by DRIE are required to have straight ($\theta = 90\,°$) and smooth sidewalls for high capacitive sensitivity and efficient tuning [29-30]. For TSVs, although positively tapered sidewalls by through-wafer DRIE may ease the deposition of a seed layer for subsequent Cu electroplating [31], slope sidewalls are not desired for creating high density HAR TSV arrays since the pitch of the vias must accommodate the tapered etching profile.

Etch termination happens when the etched feature tapers to a point at a critical AR and the etch rate becomes zero. Yeom et al. [32] analytically defined the maximum achievable AR for a given trench width as the AR at which the instantaneous etch rate of a given cycle in the DRIE process reaches zero. At this critical AR, the instantaneous polymer etch rate equals the

product of the instantaneous deposition rate and the set time ratio between the polymer deposition and etching phases. The underlying silicon cannot be exposed. They verified their model by DRIE experiments and showed that tapering happens at AR ranging from 10:1 to 15:1 until the etched feature tapers to a tip at the critical AR. The analysis is based on the process parameters being fixed throughout each DRIE experiment, although the effects of different process parameters on the critical AR are also analyzed in separate etches.

To compensate for ARDE induced sidewall tapering and etch termination, Owen et al. [5] ramped critical Bosch DRIE process parameters during a 150 min etch and demonstrated record-high AR of ~ 80:1 for 5 μm trenches etched to depth 400 μm. However, DRIE beyond standard 500 μm and with HAR has remained challenging.

ARDE also causes DRIE lag where smaller features are etched slower than larger features under the same process conditions. For TSV application, the multiplicity of final applications creates a wide range of specifications for TSV diameters from sub-micron to tens of microns [21]. It evolved from the medium-density interconnects for CMOS image sensor (d=70 μm, AR=1:1) to high performance computing applications (d=10 μm, AR=10:1) and to today's very dense logic stack (d=1 μm, AR<10:1). Due to ARDE induced DRIE lag, these vias of different diameters with the desired depths are fabricated in separate processes for different chipsets. Tian et al. [19] reported an improved method of fabricating TSVs with arbitrary ARs by adopting an aluminum etch-stop layer both to provide excellent etch selectivity, and to avoid notching for simultaneously fabricating TSVs and large cavities.

MEMS devices require an even wider range of feature sizes from sub-micron to tens or hundreds of microns. Unlike TSVs, the different feature sizes in MEMS devices are usually fabricated during the same process. For example, in the widely adopted SOI (silicon-on-

insulator) and SOG (silicon-on-glass) processes, DRIE lag results in features of different sizes being etched through and reaching the dielectric layer at different times. This causes notching at the silicon/oxide interface where the charged dielectric layer can re-direct the etching plasma ions and the ions will attack the sidewalls.

Researchers have found ways to reduce ARDE induced DRIE lag and effectively control the sidewall slope by adjusting process parameters. Lai et al. [28] demonstrated that a normal ARDE induced DRIE lag can be changed to an inverse lag under optimized conditions for trenches sizes from 2.5 μm to 10 μm using SF_6 and C_4F_8 gases. This is mainly achieved by adjusting step times and rates to offset the different efficiencies in polymer deposition, polymer removal and spontaneous silicon etching based on experimentally measured etch rate. Although reduced DRIE lag at < 2 % and inverse ARDE lag (-5 %) was shown, the etched trench depth tested was < 25 μm. Chung et al. [34] attributes the cause of RIE lag in ICP etching to the formation and removal of passivation film at the bottom of the trench, together with feature geometry. They fixed the factor of feature area to decrease the extra geometry contribution to RIE lag, and found that lag exists at a low pressure of APC (auto pressure control) 30 % while APC 75 % resulted in an inverse lag where smaller features etch faster. Pressure determines the density of radicals and ions dissociated from C_4F_8 and SF_6 reacting gasses thus governing the competition between two contrary reaction mechanisms: 1) the formation and removal of C_4F_8 passivation film that impedes etch depth; and 2) the arrival of SF_6 etching gas that enhances etch depth. Higher pressure leads to thinner passivation in smaller features due to reduced mass transport and scattering of C_xF_y. It also leads to lower ion density of S_xF_y. However, the difference in the effects of lower ion density of S_xF_y on different features is small, and can be improved by higher bias to increase the ion directionality. Although lag-eliminated and inverse

lag are achieved, the etch depth are tested up to only < 70 μm after 30 min etch of 2 - 100 μm wide trenches, indicating low overall etch rate even for the larger features (< 2.5 μm/min).

Results by Lai et al. [28] and Chung et al. [34] indicate that adjusting one process parameter (step times or pressure) could mitigate ARDE induced lag effect, however, the overall etch rate for both small and larger features are greatly reduced. Deeper etch thus will require much longer time and the etch depth will plateau.

B. Pattern Dependency

3D MEMS devices are fabricated by transferring 2D images on a mask to the desired substrate such as silicon and other materials. 3D devices are characterized by the feature resolution both in the plane of the wafer surface, and in the planes normal to the wafer surface that are etched deep into the bulk of the substrate. Using DRIE to define the critical parameters and boundaries of 3D MEMS devices, extra care is needed to study the etch characteristics of not only a wide range of feature sizes, but also the crossings and intersections of these features [33-35]. Kiihamäki et al. [33] showed that the RIE lag is related to the feature length-to-width ratio (L/W ratio) where long narrow features (L/W > 16) are etched faster than square holes of the same width, as well as the absolution width W. For example, after 80 min etch, the lag between holes and long lines with W = 5 μm is >100 %; the lag between holes and long lines with W = 50 μm is >20 %. Lag is also related to pattern shape. The intersections of multiple lines experience an enhanced etch rate. Chung et al. [34] verified through experiment that a transition point exists between the feature length-sensitive and feature length-insensitive area in relation to the etching rate of trenches at constant width and is related to the feature dimensions.

C. Selectivity of Etching Mask Materials

Selectivity is a measure of the ratio between the silicon etch rate and the mask materials

etch rate under the same conditions. Etching of mask materials is mainly due to physical sputtering. If the mask material is depleted the patterned features will be destroyed at the top surface. This is exceptionally critical for our ultra-deep Bosch DRIE since the target depth are approaching or exceeding 1 mm that requires significantly extended etching duration.

Oxide and aluminum are the most commonly used hard mask for DRIE, and photoresist (PR) is most widely used soft mask. Oxide generally has a higher etch selectivity (from 120:1 to 200:1) to silicon than typical photoresist (PR) (~50:1). For PR, the oxygen or fluorine content in the plasma will erode the mask and decrease the selectivity, with the rising temperature due to the exothermic reaction aggravating the effect. Lo et al. [36] has shown that with certain chemistries, PR has better selectivity and improved anisotropy than oxide due to polymer deposition caused by the PR mask. However excessive polymer deposition is not preferred since it will promote “black silicon” or “grass” formation (the formation of micro-columns) due to re-sputtering of the nonvolatile mask materials onto the exposed silicon [37]. Photoresists with higher selectivity are used to endure longer DRIE processing with higher plasma power. During DRIE of fused silica, Cao et al. [38] reported higher selectivity at 3.4 by using negative photoresist KMPR compared to very poor selectivity at ~1:1 of regular photoresists, even under bombardment of high-energy ions during the process. Deep etching of large features can also take advantage of new developments in ultra-thick PR such as dry film resist to achieve a greater etch depth [50-51].

The selectivity of low-chemical-reactivity metal masks is generally higher than oxide and PR, although it is not infinite due to ion bombardment in the process. Yeom et al. [32] reported that 1000 Å aluminum mask was used in a 180 min DRIE using a time-multiplexed DRIE process with SF_6 for etching and C_4F_8 for sidewall passivation, with silicon etch rate at 1-

2 μm/min. Ganji et al. [39] have shown that Al have 1000x higher selectivity than AZ1500 PR at cryogenic temperature. Marty et al. [6] used 2000 Å aluminum mask to etch 0.374 μm wide and 40.1 μm deep trenches. Parasuraman et al. [40] used 500 nm evaporated aluminum mask for etching 250 nm wide trenches with Bosch DRIE, and achieved >120:1 high AR using cryogenic DRIE.

However, the results with aluminum mask from submicron trench DRIE are not compatible with feature sizes in the tens of micrometer range. This is because in these submicron-feature etching, sputtering and re-deposition of nonvolatile metal compound were naturally suppressed by the high AR, whether cryogenic or Bosch DRIE. For larger feature, surface roughness caused by metal masks was reported by Oehrlein et al. [41]. Nonvolatile AlF_3 is formed in CF_4 reactive ion etching, which deposits on the exposed silicon and masks against subsequent etch resulting in formation of silicon grass. Ganji et al. [39] reduced substrate bias to laterally etch the silicon grass in its initial formation stages, resulting in increased sidewall damage.

This micro-masking may be avoided by preventing metal sputtering in the first part of the DRIE and, if prevented, it will not take place in further etching, after a given depth/AR is reached, as suggested by Bagolini et al. [42] and Mu et al. [43]. In [42], silicon etch rate measures 2.5 μm/min for 100 μm features and aluminum etch rate is measured at <0.05 nm/min. Photoresist as thick as 2 μm is necessary on top of the aluminum film to sustain 18 min of Bosch DRIE etched to a depth of 45 μm, and thus avoiding the formation of micro-masking during DRIE. Beyond this depth, the AlF_3 compounds have a limited mobility to reach the cavity bottom and re-sputter. To pattern smaller features, 100 nm titanium mask replaces the PR mask to sustain 17 min DRIE, where titanium mask does not generate re-sputtering of titanium

fluorides.

Jansen et al. [24] suggested that Cr, Cu and Ni are good candidates as DRIE masking materials. Nickel masks endured up to 10-hour DRIE of Pyrex Glass [45]. Dowling et al. [26] also reported SF_6/O_2 ICP etch of silicon carbide (SiC) with a Ni mask (selectivity=60:1). Despite high mask selectivity, Ni and Cr are not CMOS compatible and hardly fit into a semiconductor environment [47].

We will discuss the mask materials used in our deep ultra-high aspect-ratio silicon DRIE process in the next section.

We have developed a modified DRIE process to minimize the standard DRIE process shortcomings (ARDE induced tapered sidewall/etch termination/DRIE lag, and pattern dependency) presented in the previous section. Ultra-deep ultra-high AR features with controlled sidewall slope are obtained by dynamically ramping the Bosch DRIE process parameters. This section will present detailed description of this modified DRIE process with ramped process parameters and comparison with the standard fixed-parameter recipe.

3.1.2 Standard Fixed-Parameter Bosch DRIE Process

We use an inductively coupled plasma (ICP) Surface STS Pegasus etcher to conduct all the experiments. Standard DRIE recipes have fixed process parameters throughout the etching. The etcher is operated at 13.56 MHz ICP power level of 2800 W and 380 kHz RF bias power at 60 W in the etch sub-cycle and 2000 W ICP power in the passivation sub-cycle. C_4F_8 and SF_6 gas species are alternated between the passivation and etching steps at 24 mTorr and 30 mTorr chamber pressure, respectively.

1 - 35 μm wide trenches (> 1000 μm in length) are patterned and etched by the standard fixed-parameter DRIE process for various durations of 90 min, 110 min and 150 min. Since real-

time in-situ, process monitoring tool is not available, cross-sectional SEM images are used to characterize the process. Figures 3.2 & 3.3 show DRIE results of trenches with various widths.

Although the DRIE recipe used is designed for etching relatively small features (1 - 100 μm) with vertical, smooth sidewalls and minimal undercut, the depth of straight sidewalls is limited to < 250 μm even for trenches wider than 30 μm wide in Figure 3.2.

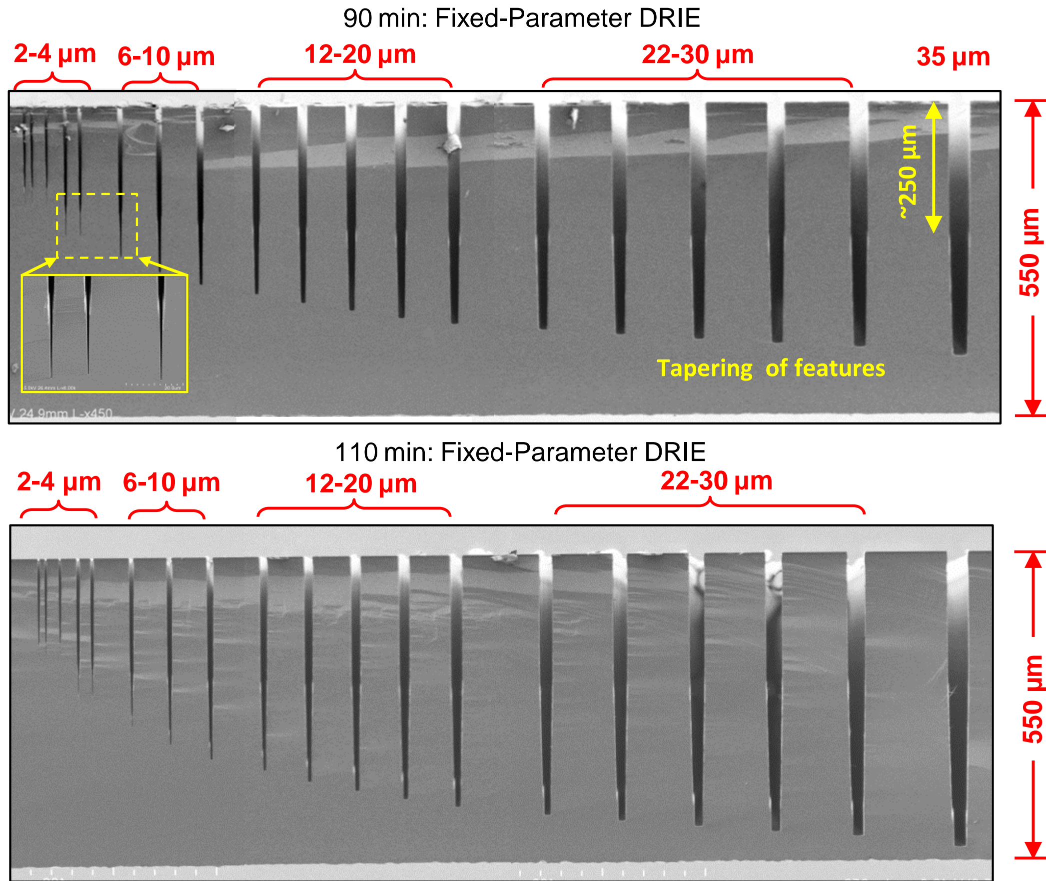


Fig. 3.2. Standard fixed-parameter DRIE results: 90 min and 110 min DRIE on 2 - 35 μm wide trenches. Sidewalls of trenches < 6 μm wide converge to a point and the etching is terminated within the 90 min DRIE. Although the apparent etch rate of trenches > 6 μm wide does not reach zero, sidewall tapering of all feature sizes is observed.

The sidewalls of trenches of all the feature sizes taper toward the bottom after certain AR is reached (>10:1 and <20:1), and the etch rate slows down significantly, especially for trenches that are <10 μm wide. These results are consistent with the AR suggested by Yeom et al. [32] at

which sidewalls start to taper.

This standard recipe has an etch rate of around 3 µm/min for 2 µm wide trenches and 5.62 µm/min for 10 µm wide trenches, given the etched feature does not exceed certain AR. During the last 30 min of the 150 min etch, we measure etch rates of <1 µm/min for the 1-2 µm features and <2 µm/min even for 5 µm features. The 5 µm trench closes at a depth of <290 µm as shown in Figure 3.3.

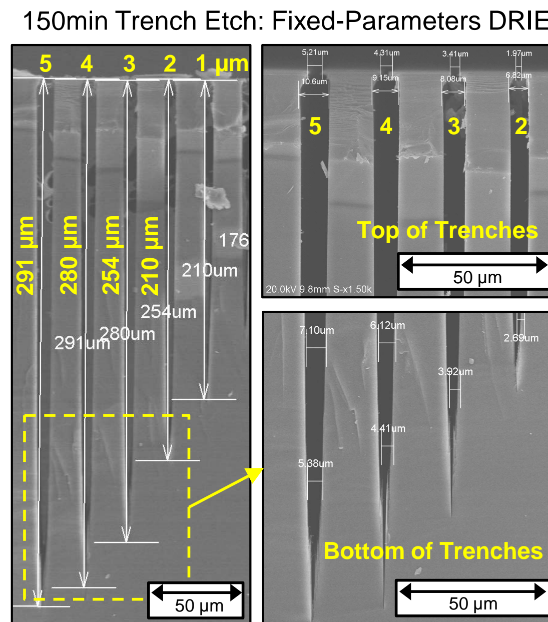


Fig. 3.3. 150 min DRIE of 1-5 µm wide trenches using standard fixed process parameters. SEM images show major sidewall tapering and convergence to a point at the bottom.

Holes with different diameters ranging from 15–35 µm are also etched with the standard fixed-parameter recipe. As shown in Figure 3.4, 15 µm holes are etched to <400 µm within 210 min. The apparent etch rate is close to that of 5 µm trenches at ~2 µm/min. The 35 µm holes however are beyond being etched all the way through the wafer (~550 µm). Tapering and convergence of sidewalls are observed at the bottom of the holes. Since the holes converge to submicron points at the very bottom, sharp points are not observed by cleaving the silicon wafers. Due to the ion flux and ion energy dependency on in-plane aspect-ratio (Ø/Ø for holes and L/W for

trenches), obtaining HAR in hole/via etching is more difficult than etching trench with the same width as the hole diameter.

This standard fixed-parameter recipe is used as a baseline recipe to develop and tune the dynamic recipe with ramped process parameters to achieve straight sidewalls and flat feature bottom.

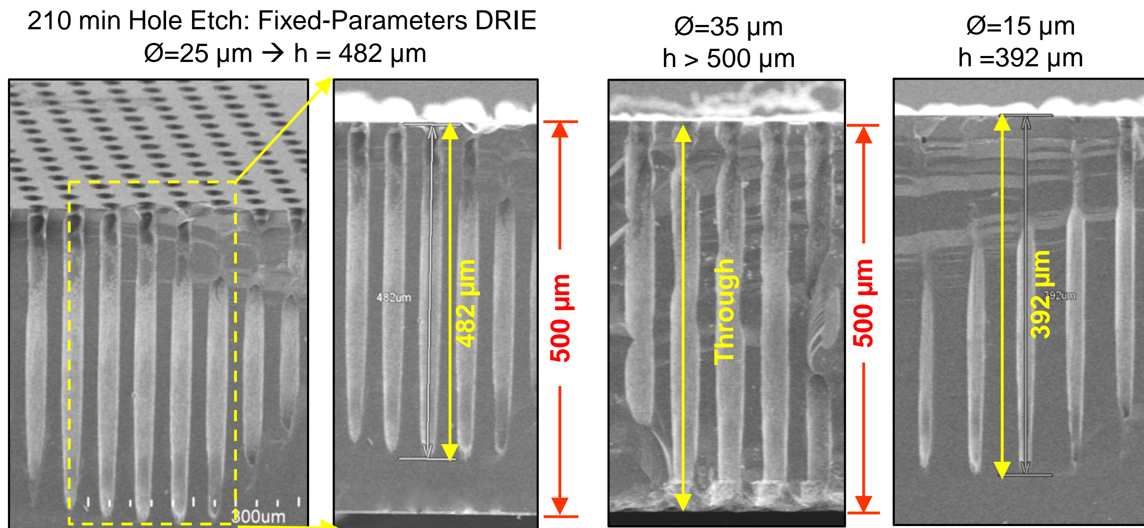


Fig. 3.4. SEM images of holes with various diameter etched for 210 min with the standard fixed-parameter DRIE process. The bottom of the holes converge to a sharp point and etching is terminated. Due to the ion flux and ion energy dependency on in-plane aspect-ratio (length to width), obtaining HAR DRIE in hole/via etching is more difficult compared to etching trench with the same width as the hole diameter.

3.2 DRIE with Ramped Process Parameters for High Aspect-Ratio Deep DRIE

To address ARDE and create desired structure, instead of adjusting a single process parameter [32-38] as discussed in Section II-A, combinations of recipes can be used in sequence by modern plasma etching tools. For instance, one can perform an anisotropic RIE etch, an isotropic etch and a Bosch DRIE by programming the etching sequence [5, 48,49].

Wang et al. [48] reduced undercut by over passivating at the beginning of the etching process. To do so, C_4F_8 passivation gas was introduced to the chamber during the etch sub-cycle

and the gas flow was ramped down from 10 sccm to 2 sccm while the SF_6 gas flow was kept constant at 450 sccm. This method resulted in reduction of undercut from 468 nm to 306 nm. Continuous adjustment of process parameters has also been proposed to address ARDE issue. For example, Teixeira et al. [49] proposed programming a governing function that determines the initial parameters as well as how the parameters are to be transitioned.

In this work, we attempt to address the key DRIE shortcomings (ARDE induced sidewall tapering, etch depth limitations and DRIE lag; and pattern dependency) in order to achieve ultra-deep ultra-high AR silicon etch by further developing and characterizing a modified Bosch DRIE process initially proposed by Owen et al. [5]. Since these issues mainly originate from the reduction in transport of etchant agents and ion bombardments at the bottom of deep features as the AR increases, Bosch DRIE process parameters are continuously ramped to optimize the DRIE conditions at each depth as the etch proceeds.

The STS Pegasus ICP DRIE etcher allows process parameters to be ramped from a start value to an end value. The ramp rates of different parameters are set in order to maintain as constant and high etch rate as possible as AR increases. Then the overall etch time (recipe duration) is set to reach a desired etch depth. The start and end values of the various parameters are calculated from the product of ramp rate and etch duration.

Three parameters of the DRIE process are ramped: 380kHz RF bias platen power, etching and passivation sub-cycle duration, and chamber pressure. It should be noted that the start and end values need to be characterized for specific feature sizes, etch patterns and target depths. For example, for 2-10 μm trench width, the following set of ramped parameters are found to best compensate the reduced etch rate and result in deep HAR structures by enhancing the etching agents effect during the total 150 min DRIE duration: the 380-kHz bias power during etch step is

increased from 60 W to 140 W; the etch sub-cycle duration starts at 2.6 s and is ramped up to 5.6 s; and the passivation step duration is increased from 2 s to 3.5 s. The chamber pressure is also changed throughout the process: the passivation step chamber pressure is ramped up from 24 mTorr to 34 mTorr whereas the etch step chamber pressure is ramped down from 30 mTorr to 15 mTorr. The relevant parameters for the fixed and ramped processes are compared in Table 1. The effect of these different parameters will be further discussed.

Table 3.1: DRIE process parameters oprimized for 150-min etch optimized for 2 - 10 μm trenches: fixed-parameter recipe vs. ramped-parameter DRIE recipe.

Recipe	Etch			Passivation	
	380 kHz Bias Power	Step Time	Pressure	Step Time	Pressure
	(Watt)	(s)	(mTorr)	(s)	(mTorr)
Fixed	60	2	30	2.6	24
Ramped	60→140	2.6→5.6	30→15	2→3.5	24→34

This is optimizaed for 2-10 μm trench etch.

3.2.1 DRIE Process Parameters

A. 380kHz RF Platen Bias Power

The plasma is generated by an inductively coupled coil generator at 13.56 MHz and is kept constant at 2000 W and 2800 W during the passivation and etching steps respectively.

A 380 kHz RF platen power is applied to bias the substrate which generates a high voltage sheath between the plasma and the wafer. This voltage drop accelerates the ions across the sheath to strike the substrate. The STS etcher allows us to set this 380 kHz RF platen power during the etch step as well as a higher boost power for a fraction of the etch step time. The main power is set to 60 W and the boost power during the first one second of the etch step is set to ramp from 60 W to 140 W. Ramping the boost power improves ion directionality as AR increases as well as improving passivation breakthrough at the bottom of the deep trenches.

However, higher boost power reduces mask material etch selectivity drastically even for thermally-grown SiO_2 mask. Thermal SiO_2 mask etch rate is measured to be > 30 nm/min at 140 W boost power whereas < 18 nm/min at 60 W.

B. Etch step duration and chamber pressure

Increasing the etch step time from 2.6 s to 5.6 s throughout the process provides more time to the gas species to diffuse through the depth of the trench as it gets deeper. To further improve the etchant agents' transport to the bottom of deep structures, chamber pressure during the etch step is decreased from 30 mTorr to 15 mTorr to increase the mean free path of gas species, which is achieved by reducing the gas molecules and ions collisions. These adjustments throughout the recipe improves breakthrough of the passivation layer at the bottom and promotes etching the silicon in deep high AR trenches.

Increasing the etch step time from 2.6 s to 5.6 s throughout the process provides more time for the reactive gas species to diffuse into and for the reaction products to get out of the narrow trench as it gets deeper. To further improve the gas transport to the bottom of deep structures, the chamber pressure during the etch step is decreased from 30 mTorr to 15 mTorr which increases the mean free path of gas species, by reducing the gas molecule and ion collisions. These adjustments improve the breakthrough of the passivation layer at the bottom and promote etching the silicon in deep high AR trenches. However, lowering the chamber pressure will decrease the etch rate slightly due to the lower concentration of reactive radicals in the chamber.

C. Passivation step duration and chamber pressure

Ramping up the bias power and duration of the etch step to compensate for high AR small features increases the undercut at the top of the features by consuming the passivation

polymer along the sidewalls of the etched features near the top. Passivation step parameters need to be adjusted to reduce lateral etching. This is compensated by ramping the passivation step chamber pressure from 24 mTorr to 34 mTorr, and duration from 2 s to 2.6 s. Increasing the duration of the passivation step results in a thicker passivation layer. Increasing the pressure provides more reactant in the chamber, reinforcing the passivation layer on the sidewalls near the top. At the same time, the polymer deposition rate at the bottom of deep trenches is suppressed with reduced gas species transport due to shorter mean free path of gas species.

3.2.2 Microfabrication process

For testing and charactering our ramped-parameter silicon DRIE process, experiments were carried out on 4-inch lightly doped p-type silicon wafers, and on 4-inch highly doped p-type silicon wafers. The silicon wafers are patterned with a wide range of patterns and feature sizes: trenches (L>>W) with widths ranging from 1-100 μm and circular holes with diameters at 10, 15, 25, 35 μm. 500 μm thick silicon wafers are used to characterize narrow-width trenches (2-10 μm wide) and holes (15-25 μm in diameter), whereas 1 mm thick wafers are used to characterize wider features (10-100 μm wide).

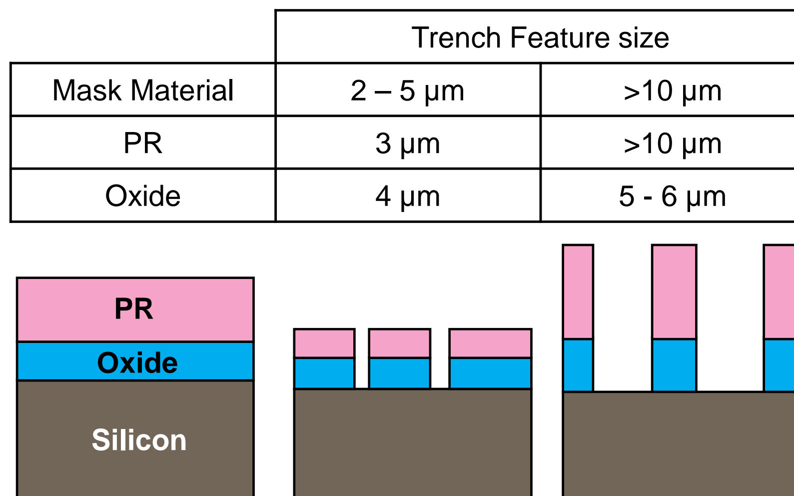
Since mask erosion rate increases throughout the process where dynamic process control with ramped-up RF bias power and etch step duration is employed, a thick oxide hard mask along with a thick photoresist film is needed to provide sufficient masking materials for the long DRIE process. In addition, lithography resolution will limit how precise the small-feature patterns can be transferred to a thick mask layer, whether it is thick oxide or thick PR.

As shown in Figure 3.5, for >150 min DRIE with the ramped-parameter process, ~3 μm SPR220 (7.0) photoresist in addition to 4 μm LPCVD SiO_2 is used as DRIE mask materials for

feature sizes of 1-10 µm, and >10 µm SPR220(7.0) photoresist along with 5-6 µm thick SiO_2 is used as mask materials for feature sizes >10 µm.

1 - 2 µm wide trench patterns need to be precisely transferred to the oxide mask with vertical sidewalls, thus they are patterned using a GCA AS200 AutoStepper with 5:1 reduction and etched using SPTS APS Dielectric Etcher for high sidewall verticality.

In future, high selectivity metal masks may be used to long DRIE with extended times for the small features [42-47]. Whereas ultra-deep etching of relatively large features can take advantage of new developments in ultra-thick PR such as dry film resist to achieve a greater etch depth [50-51].



	Trench Feature size	
Mask Material	2 – 5 µm	>10 µm
PR	3 µm	>10 µm
Oxide	4 µm	5 - 6 µm

Fig. 3.5. DRIE masking materials used for ultra-deep ultra-high aspect-ratio (UHAR) long DRIE processes: 5 - 6 µm LPCVD SiO_2 and thick photoresist layers are used as hard and soft masking material respectively. Thinner resist (~ 3 µm) is used for 1 - 10 µm feature sizes due to lithography limitations.

3.3 Ultra-High-Aspect-Ratio Deep DRIE Results

3.3.1 DRIE of Trenches: Etch Rate and Etch Profile

Trenches (>1000 µm long and 2-10 µm wide) are patterned and etched in 500 µm thick <100> wafers using both the fixed-parameter recipe and ramped-parameter recipe (DRIE parameters presented in Table 3.1). Table 3.2 presents the 150-min ramped-parameter DRIE

recipe results with all the depths and lateral dimensions measured at cross-sections after cleaving the 500 μm thick silicon wafers.

Table 3.2: Final trench profiles for 150 min drie with ramped parameter process.

Mask Opening (μm)	Measured Trench Width (μm)			Trench Depth (μm)	Aspect Ratio	Sidewall Slope (°)	Under-cut (μm)
	Top	Mid.	Bottom				
2.5	6.3	3.0	1.7	290	98	89.95	1.90
3.5	7.4	3.9	2.5	336	87	89.59	1.95
4.5	8.8	4.7	3.4	367	77	89.58	2.20
5.5	10.2	5.7	4.7	388	69	89.58	2.35

Ramped DRIE results demonstrate increased etch rate, reduced undercut, suppressed ARDE, flat trench bottom even after 150 min etch and ARs exceeding 90:1 for trenches as small as 2 μm as shown in Figure 3.6, in contrast to the fixed-parameter process that results in tapered sidewall and converged trench bottom (Figure 3.3).

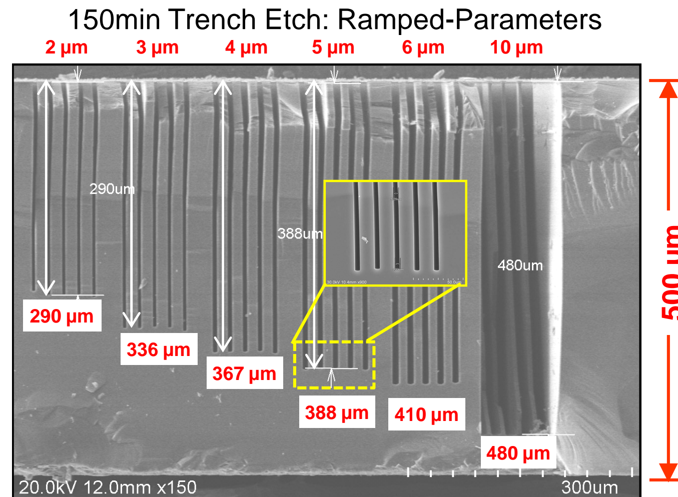


Fig. 3.6. DRIE of 2-10 μm wide trenches by the ramped-parameter process for 150 min. Deeper trenches with straight sidewalls and flat bottom is obtained compared to the results of fixed-parameter DRIE shown in Fig. 3.3.

The DRIE depths of various trench sizes after 150 min DRIE are compared for two

processes in Figure 3.7. The overall etch rate is increased by over 25 % for all feature sizes >2 µm compared to the fixed-parameter process. The widths at the bottom of the trenches are reduced by only 10-15 % from the original feature sizes on the mask. By measuring the depth at the deepest point, one might argue that the ramped-parameter recipe produces more ARDE induced DRIE lag, i.e., comparing the etch depth of the 5 µm wide trenches to that of 2 µm wide trenches, the lag is at 30 % with the ramped-parameter process compared to 28 % with the fixed-parameter process. However, well-controlled vertical sidewall profile with much less tendency of etch termination is more important.

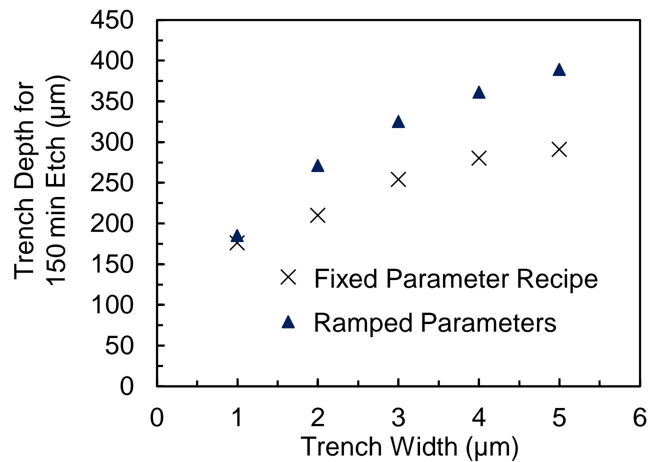


Fig. 3.7. Comparison of DRIE results of 1-5 µm wide trenches using the fixed-parameter and the ramped-parameter process for 150 min: for all feature sizes, deeper depth is obtained by using the ramped-parameter DRIE process.

Time-lapse depth measurements are made at 60 min, 90 min, 120 min and 150 min of DRIE to monitor the progress of the etch rate and AR dependency. Figure 3.8 depicts the obtained trench depth at different time intervals for 1-5 µm wide trenches. Figure 3.9 presents the calculated average etch rate at different time intervals: 0-60 min, 60-90 min, 90-120 min, and 120-150 min.

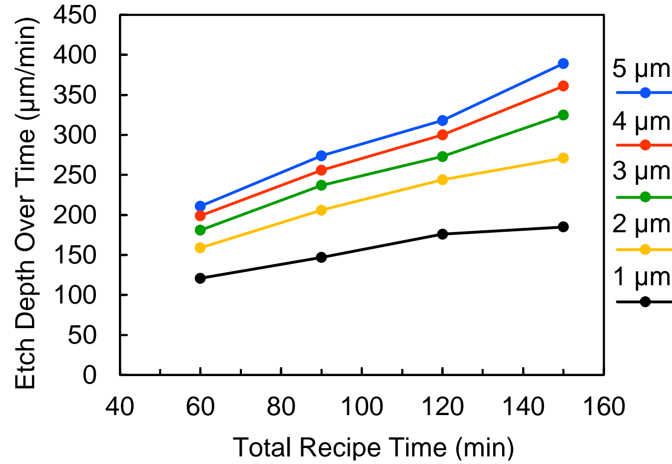


Fig. 3.8. Trench depth obtained at different time intervals for 1-5 μm wide trenches using the ramped-parameter DRIE process. Time-lapse depth measurements are made at 60 min, 90 min, 120 min and 150 min of DRIE to monitor the progress of the etch rate and aspect-ratio dependency.

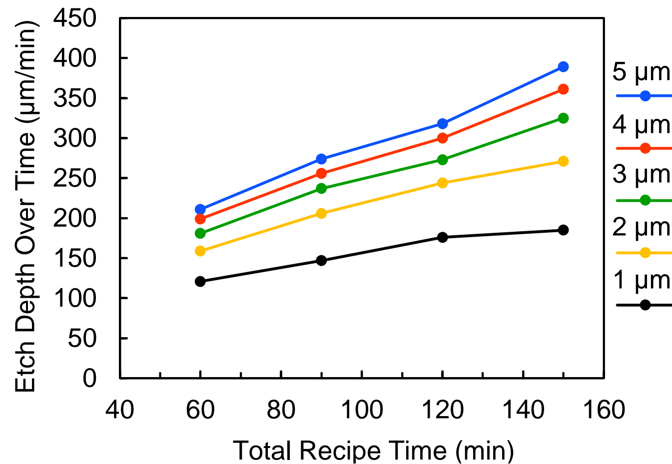


Fig. 3.9. Trench depth obtained at different time intervals for 1-5 μm wide trenches using the ramped-parameter DRIE process. Time-lapse depth measurements are made at 60 min, 90 min, 120 min and 150 min to monitor the progress of the etch rate and aspect-ratio dependency.

In a standard fixed-parameter DRIE process, a negative incremental etch rate is usually observed as the features are etched deeper due to ARDE effect. With the ramped recipe that applies higher bias power, longer etch step duration and reduced etch step chamber pressure, we obtained a positive incremental etch rate toward the end of the process, i.e. the etch rate during 120-150 min are higher than the etch rate during 90-120 min for 3-5 μm wide trenches. The

overall etch rate for the entire duration (150 min) is still reasonably high: greater than 1.5 µm/min for 4-5 µm wide trenches. For all 2-5 µm features ARDE effect is efficiently suppressed to achieve deeper etch.

Figure 3.10 show the final etched profiles all the way along the trench depth for 120 min and 180 min etch with the ramped recipe. The trench bottoms are relatively flat and the widths at the very bottom of the trenches are reduced by only 10-15 % from the original feature sizes defined on the mask.

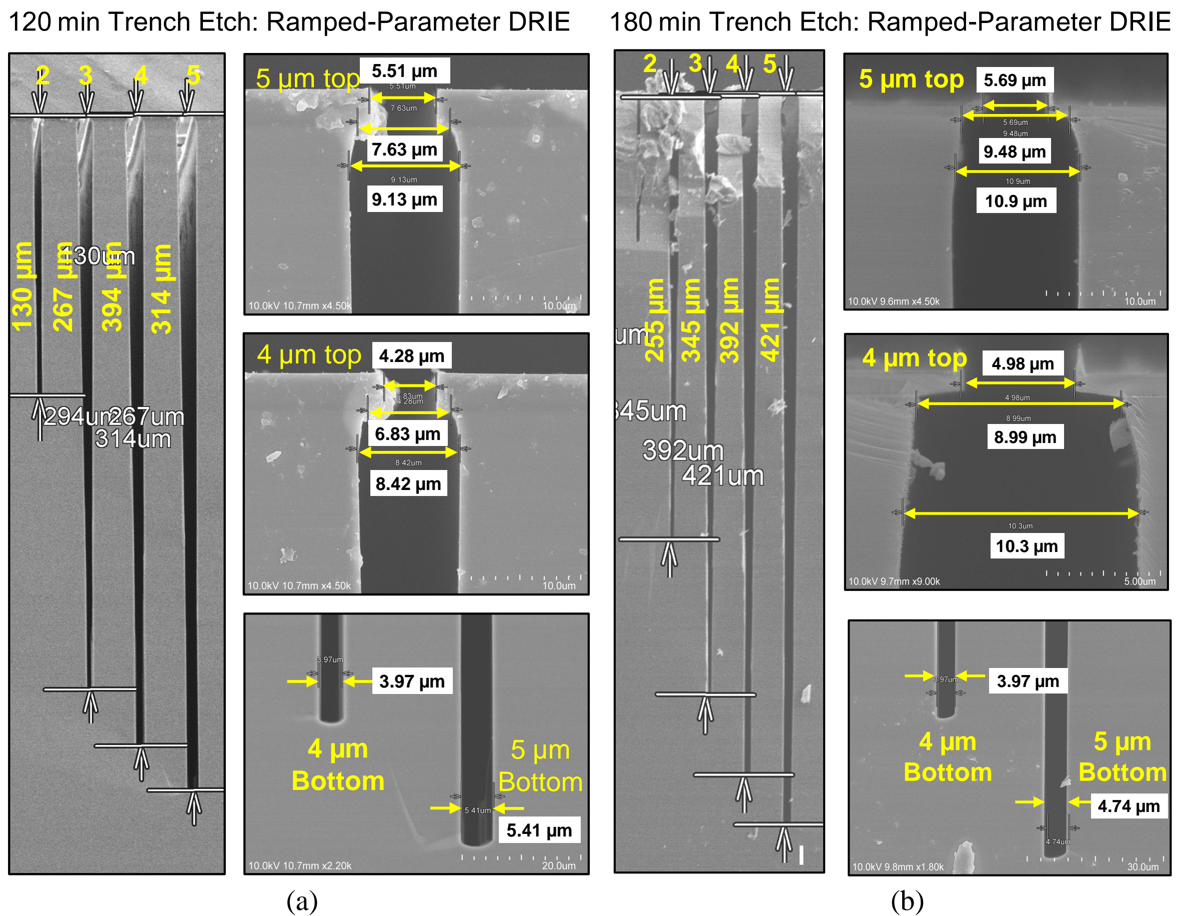


Fig. 3.10. 2-5 µm wide trenches etched for (a)120 min and (b) 180 min with ramped-parameter DRIE process. Final etch profiles are shown by highlighting the trench openings at both the bottom of the trenches and underneath the oxide mask near the top. The trench bottoms are relatively flat, and the widths are almost the same as the original feature sizes defined on the mask. The upper half of the trench is tapered slightly due to DRIE undercut and lateral etch.

The upper half of the trench is also tapered slightly due to DRIE undercut and lateral etch. The 180 min etch results in larger undercut (>2.5 µm on each side) compared to the 120 min etch (<2 µm on each side). This is because the increased power has the side effect of more easily breaking through the passivation layer at the top and enhances lateral etch. The ramped-up passivation step pressure and sub-cycle time duration provide more reactant to form thicker passivation layer on the trench sidewalls, reducing this undercut, but not completely.

3.3.2 DRIE of Circular Holes: Etch Rate and Etch Profile

In contrast to the converged bottoms shown in Figure 3.4, the ramped parameter process can create flat bottoms even for etching circular holes as shown in Figure 3.11. Etch rate is also increased compared to the fixed-parameter recipe. 25 µm diameter holes are etched to >500 µm within 150 min using the ramped process while 210 min of the original fixed-parameter process only obtained maximum depth of <400 µm.

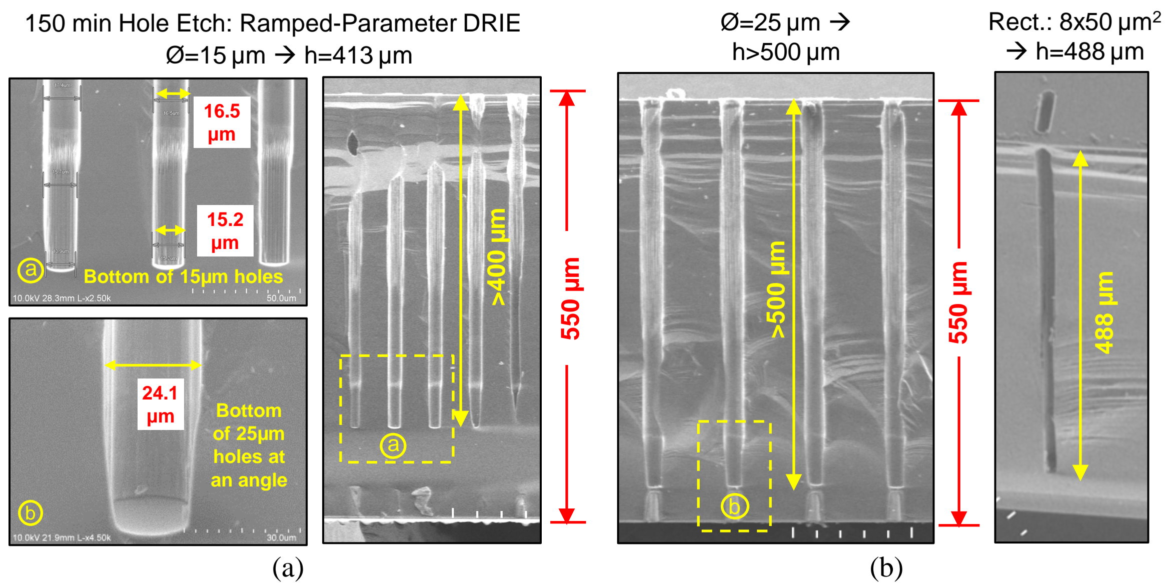


Fig. 3.11. (a) Holes and (b) small in-plane aspect-ratio rectangles at 8 µm×50 µm are etched for 150 min with the ramped-parameter DRIE recipe.

The in-plane AR (length /width, L/W) of the etched features also play an important role on the etch rate. 15 µm wide trenches reach a depth of more than 520 µm whereas the 15 µm

diameter circular holes only reach a depth of ~400 μm with the same 150 min ramped DRIE process. A rectangular pattern (8 μm×50 μm) is also etched deeper than 15 μm diameter circular holes. This verifies that etch rate is also in-plane AR (W/L) dependent. Long lines etch considerably faster than circular holes of the same width, or of even larger width as shown in Figure 3.11.

3.3.3 Ultra-Deep and Through-Wafer DRIE

In another test, 10-100 μm wide and >1000 μm long trenches are patterned on a 1mm thick silicon wafer and etched for 140 min. The wafers are then diced prior to taking cross-sectional SEM images. The sidewall slopes are slightly positive (89.50°<θ<90°) for relatively narrow trenches (1-10 μm in Figure 3.6 and 12-25 μm in Figure 3.12), and slightly negative (θ>90°) for wider trenches (25-100 μm) as shown in Figure 3.12.

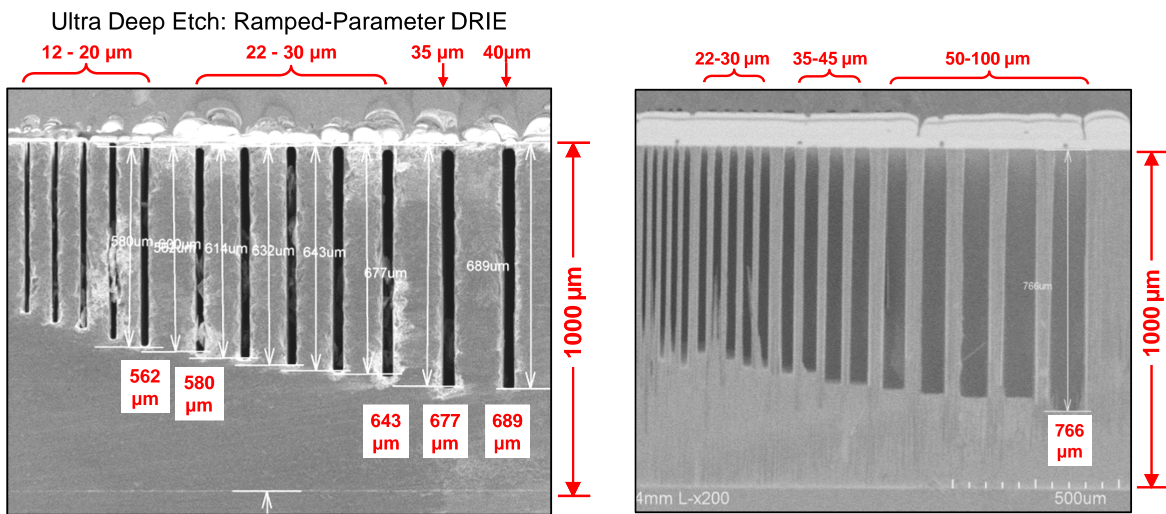


Fig. 3.12. Ultra-deep DRIE of 12–100 μm wide trenches in 1 mm thick silicon wafer by the ramped-parameter recipe for >130 min. The sidewall slopes are slightly positive (89.50 °<θ<90 °) for relatively narrow trenches (1 - 10 μm wide as shown in Fig. 6, and 10-25 μm wide), and slightly negative (θ > 90 °) for wider trenches (> 25 - 100 μm).

ARDE is effectively suppressed for trenches > 20 - 25 μm wide and are easily etched to more than 600 μm deep. The flat trench bottom and slightly negative sidewall profiles indicate

the etch has not been tested to its limit and can go all the way through 1 mm wafer thickness by increasing the DRIE process time.

Figure 3.13 illustrates DRIE results of 15 µm, 20 µm, 35 µm, and 40 µm wide trenches etched simultaneously. For 35 µm and 40 µm wide trenches, the bottom is widened by >5 µm while the 15 µm trenches bottom measure 15.9 µm and preserves the original mask dimensions. The slight negative tapering (θ>90°) of the larger features contrasts with the positive tapering (θ<90°) of narrower trench etch results using the fixed-parameter DRIE recipe shown in Figure 3.10.

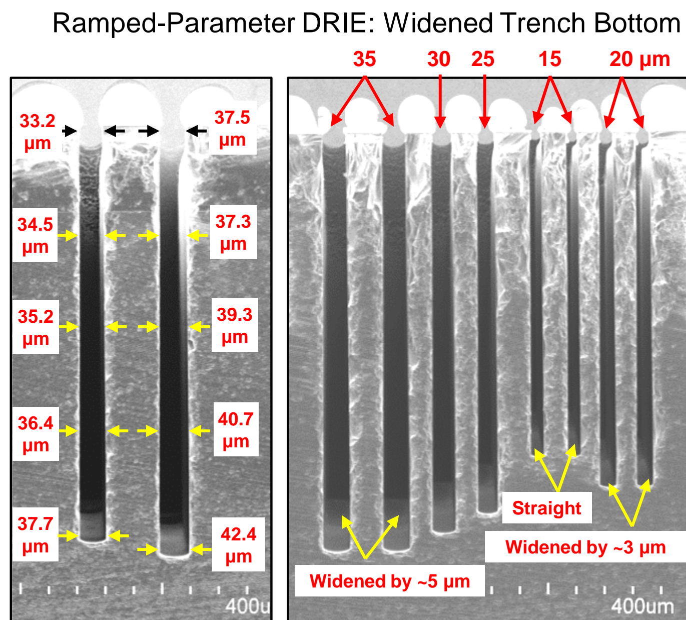


Fig. 3.13. Widening of trench bottoms is observed in > 20 µm wide trenches caused by the ramped DRIE process parameters (increase biased power, longer etch duration, and lower etch step chamber pressure), while 15 µm features has very straight sidewalls.

Widening of the trenches bottoms for larger trench width are expected due to the ramped-up bias power, increased etch step duration and ramped down chamber pressure. This can be accounted for by adjusting these ramped parameters, as discussed in the next section, although this will also impact the profile for smaller trenches.

By adjusting the ramped process parameters and overall DRIE process time, specific range of features sizes could be designed to have perfectly straight sidewall slopes, or tailored to obtain either positive or negative slopes.

Based on the slightly negative sidewall profiles for trenches wider than 25 µm, we cascaded several DRIE recipes to test the limit of our ramped-parameter DRIE process. In one experiment, the end conditions of the process parameters in Table 3.1 (optimized for 2-10 µm trench features) are modified and the overall duration of a continuously-ramped recipe is increased from 150 min (2.5 hours) to 240 min (4 hours). As shown in Table 3.3, the final 380 kHz boost power during the etch sub-cycle is set to 180 W and the final etch step chamber pressure is set to 10 mTorr, with the other parameters kept the same as in Table 3.1. The trench etch results are shown in Figure 3.14.

Table 3.3: DRIE process parameters set for 240-min etch with ramped-parameter DRIE recipe.

Recipe	Etch			Passivation	
	380 kHz Bias Power	Step Time	Pressure	Step Time	Pressure
	(Watt)	(s)	(mTorr)	(s)	(mTorr)
Ramped	60→180	2.6→5.6	30→10	2→3.5	24→34
Time	240 min				

This recipe produces very straight sidewalls for trenches wider than 18 µm. However, trenches narrower than ~16 µm wide are tapered and terminated before the end of the 4-hour DRIE. Thus, the setting is not sufficient to compensate the DRIE shortcomings for trenches narrower than 18 µm. This means that constant ramp rates for DRIE parameters are not optimal for a wide range of features sizes.

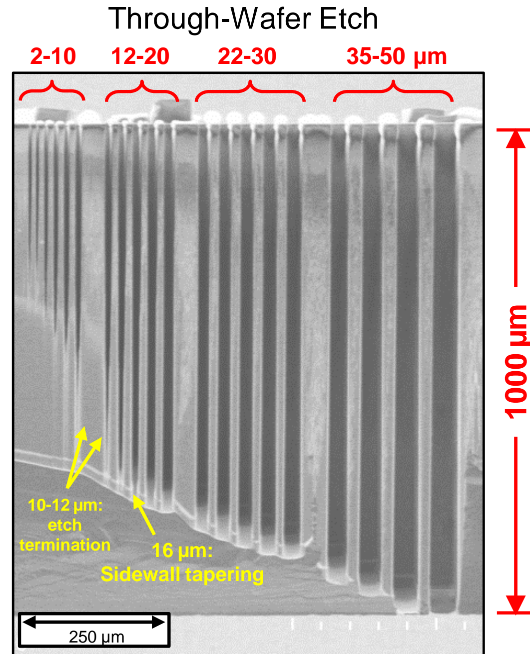


Fig. 3.14. Ultra-deep DRIE in 1 mm thick <100> silicon substrate using 240 min of continuously-ramped DRIE process. This recipe produces very straight sidewalls for trenches wider than 18 µm. However, although final boost power is increased from 140 W in Table 2 to 180 W, and final etch step chamber pressure is reduced to 10mTorr from of 15 mTorr, trenches smaller than ~16 µm wide are tapered and converged before the end of the 4 hour DRIE.

In another experiment, several DRIE processes are conducted back to back with the end conditions of one section determining the start conditions of the next section, unless noted otherwise, as shown in Table 3.4. It started with a 180 min (3 hours) recipe with an increased 380 kHz boost power to 160 W toward the end of the section; followed by a 60-min section with constant 380 kHz boost power at 160 W; and concluded by another 60-min section in which both the boost power ramped up from 160 W to 180 W as well as the etch step chamber pressure ramped down from 15 mTorr to 10 mTorr.

To prepare for a 5-hour-long through-wafer DRIE of 1 mm thick silicon substrate, 13-15 µm photoresist along with more than 6 µm LPCVD SiO_2 masks are patterned. The trench etch results are shown in Figure 3.15. After the 5-hour DRIE process, 1.5 µm oxide was remained; vertical sidewall profile and flat trench bottoms are achieved. No etch termination is observed.

Trench depth of >900 µm with width <20 µm (AR>40:1), and trench depth of >700 µm with width ~10 µm (AR>70:1) are obtained. Trench depth versus trench width is plotted in Figure 3.16. Further optimization of all process parameters is needed to achieve perfectly straight sidewall profiles all the way along the etch features.

Table 3.4: Through-wafer drie process parameters set for 5-hour etch with ramped-parameter DRIE recipe.

Segmented Recipe	Time	Etch			Passivation	
		380 kHz Bias Power	Step Time	Pressure	Step Time	Pressure
	(min)	(Watt)	(s)	(mTorr)	(s)	(mTorr)
1st	180	60→160	2.6→5.6	30→15	2→3.5	24→34
2nd	60	160	5.6	15	3.5	34
3rd	60	160→180	5.6	15→10	3.5	34

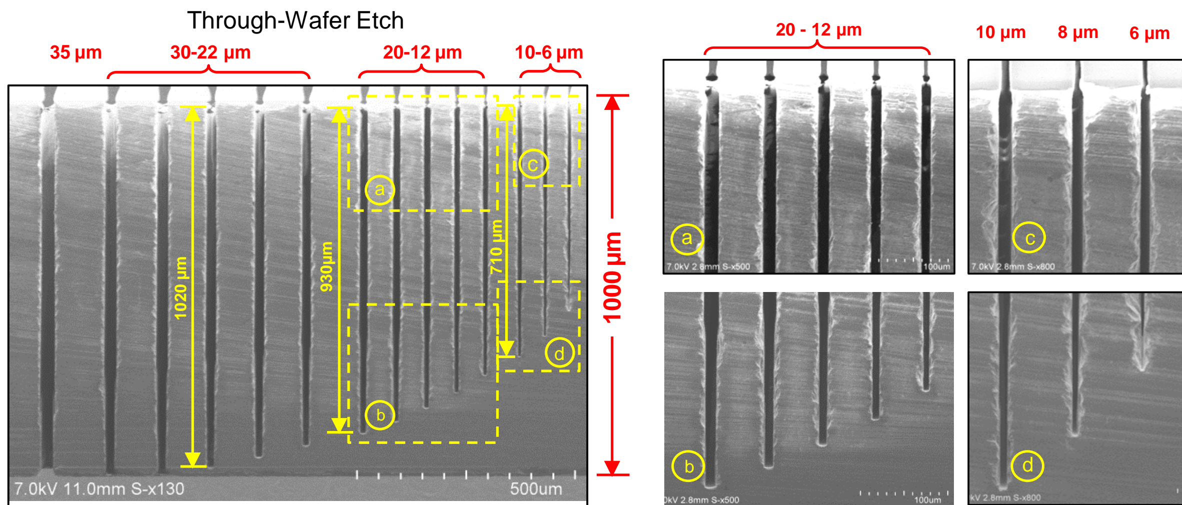


Fig. 3.15. Ultra-deep ultra-high aspect-ratio DRIE in 1 mm thick <111> silicon substrate. Trench depth of >900 µm with width <20 µm (AR > 40:1), and trench depth of >700 µm with width ~10 µm (AR>70:1) are obtained. After the 5 hour DRIE process, 1.5 µm oxide remains. Vertical sidewall profile and flat trench bottoms are achieved and no etch termination is observed.

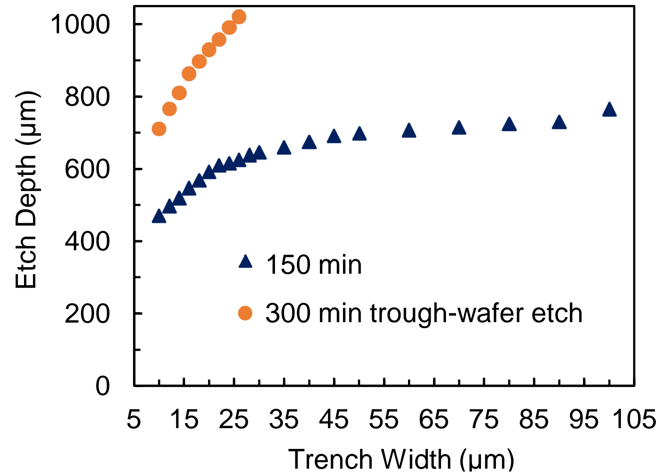


Fig. 3.16 Etch depth of ultra-deep ultra-high aspect-ratio DRIE for >130 min with the ramped-parameter recipe, compared to 300 min (5 hour) through wafer etch results from Fig. 3.15.

3.3.4 Pattern Dependency

To study the effect of DRIE pattern dependency, in our experiment, a 15 µm wide trench is etched to target depth >700 µm with crossing trenches of different widths from 20-45 µm in 1mm thick silicon wafer. Figure 3.17 shows that the 15 µm trench is etched more than 60 µm deeper near the 20 µm crossing trenches compared to the same feature size near the 40 µm crossing trenches, while both are etched deeper than where no crossing is present.

The etch rate and profiles at the junctions of narrow and wide features are very sensitive to abrupt widening/narrowing of features and sharp corners. In another experiment, 500 µm thick silicon wafer is patterned with 5-10 µm trenches that intersect at multiple points. It is etched using the ramped-parameter DRIE process followed by blanket thinning from the backside. The complicated artifacts at the trench bottoms where wide and narrow trenches intersect at 90-degree corners are shown in Figure 3.18: the etched depth on the narrow side near the junctions are greatly reduced compared to the flat trench bottoms farther away from the junction.

These artifacts are likely caused by the distorted trajectory of the incoming ions by the local electric fields created by the sharp corners along the sidewalls, such that the etch rate will

be altered for both wide and narrow features. In addition, when there is an abrupt change in feature size-induced etch depth, the artifacts could be exacerbated by a passivated “wall” across the different etch depths.

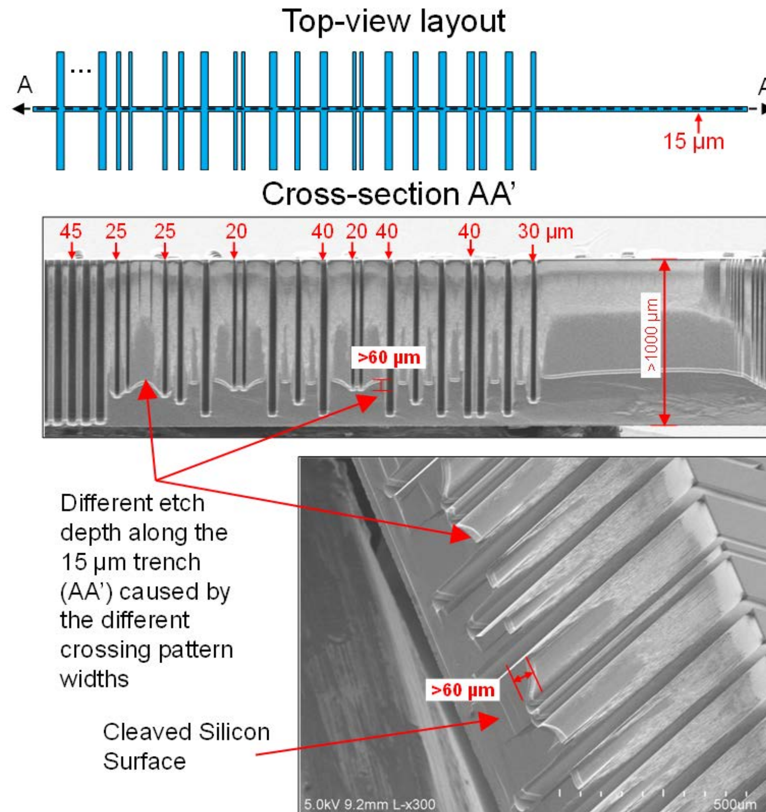


Fig. 3.17. Effect of crossing patterns on the etch depth: one 15 µm wide trench with crossing trenches of different widths from 20 - 45 µm is etched to a depth > 700 µm. The 15 µm trench is etched more than 60 µm deeper near the 20 µm crossing trenches compared to the one close to the 40 µm crossing trenches and both are etched deeper than where no crossing is present.

Rounding the corners where the different features intersect has been found to mitigate the effect and assist the etching of the narrow side. Narrow trenches connected to a large pattern with rounded corners etch faster than trenches of the same width standing alone. When we apply this customized deep HAR DRIE to a HAR MEMS accelerometer design in Chapter 4 through Chapter 7, the sharp corners at the wide and narrow feature intersections are all replaced with

rounded features. The accelerometers are successfully released, proving that the etch has reached the desired depth for all different feature sizes.

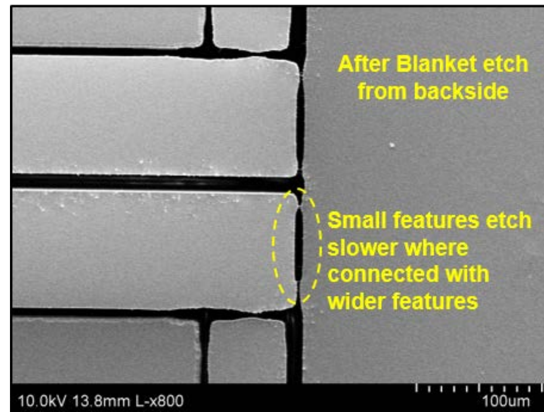


Fig. 3.18. Etch profile at junctions of narrow and wide features: Bottom of deep trenches are revealed by thinning down the wafer from backside: etch depth on the narrow side near the junctions are greatly reduced.

3.4 Summary

This chapter describes an advanced deep-reactive-ion-etching (DRIE) process for realizing ultra-deep (> 500 µm) ultra-high aspect-ratio (AR) silicon structures (AR > 40 for 1 mm through-trench etch, AR ≈ 80 for 500 µm through-trench etch, and AR > 20 for 500 µm through-hole etch), with straight sidewalls across a wide range of feature sizes.

The challenges of making such structures are overcome by continuously ramping critical parameters of the Bosch DRIE process throughout the process, including the 380-kHz bias power during etch step, the etch/passivation step duration, and the chamber pressure. The masking material capable of enduring the long DRIE process is also discussed. 10 µm and 25 µm wide trenches are etched to a depth of > 750 µm and > 1000 µm respectively, both in 1 mm-thick silicon wafers with straight sidewall profiles and flat trench bottoms. Deeper trenches are expected to be etched beyond a 1mm thick wafer with thicker and/or higher selectivity masking materials. We have also demonstrated etching of circular holes of diameters as small as 25 µm to

a depth of $> 500\,\mu m$, and potentially with $10 - 15\,\mu m$ diameter holes. This advanced DRIE process offers opportunities for applications ranging from through-silicon via (TSV) in 3D CMOS integration to emerging micro and meso-scale MEMS applications that demand ultra-deep and ultra-high aspect-ratio (UHAR) DRIE.

The results will be applied to the fabrication of the proposed 3D HAR biomimetic hair accelerometer made from silicon. Chapter 4 will describe devices with one uniform sensing gap that mainly utilize the UHAR DRIE of 2-10 μm trenches. Chapter 4 through Chapter 6 will focus on employing the ultra-deep and ultra-high aspect-ratio (UHAR) DRIE to the fabrication of a two-gap hair structure that greatly extend the device height as well as preserving small and well-controlled electrostatic transduction gaps to achieve high performance.

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Chapter 4 UNIFORM-GAP HAIR ACCELEROMETER BY SILICON-ON-GLASS (SOG) PROCESS

In the previous chapter, we described an advanced deep-reactive-ion-etching (DRIE) process for realizing ultra-deep (> 500 µm) ultra-high aspect-ratio (AR) silicon structures (AR > 40 for 1 mm through-trench etch, AR ≈ 80 for 500 µm through-trench etch, and AR > 20 for 500 µm through-hole etch), with straight sidewalls across a wide range of feature sizes (2 - 100 µm). We overcome the challenges in Bosch DRIE by continuously ramping critical DRIE parameters throughout the process, including the 380-kHz bias power during etch step, the etch/passivation step duration, and the chamber pressure.

The first-genration uniform-gap hair accelerometer prototype mainly utilizes the ultra-high aspect-ratio (UHAR) DRIE of 2 - 10 µm wide trench features.

4.1 Technology Development and Microfabrication

4.1.1 Applying Ultra High Aspect-Ratio DRIE

As shown in Figure 4.1, the spring length L of the uniform-gap device is determined by 2 µm wide trenches surrounding the spring (L≈ 300 µm). Our first-generation hair accelerometer utilize standard 500 µm thick silicon wafers thus 5 µm wide trenches are chosen as the capacitive sensing and actuation gap g_0 separating the proof-mass and electrodes. Referring to Figure 2.1, although g_0 at 3 µm or 4 µm may lead to a higher normalized sensitivity, the first DRIE etch

depths are less than 400 μm such that the release DRIE must be longer.

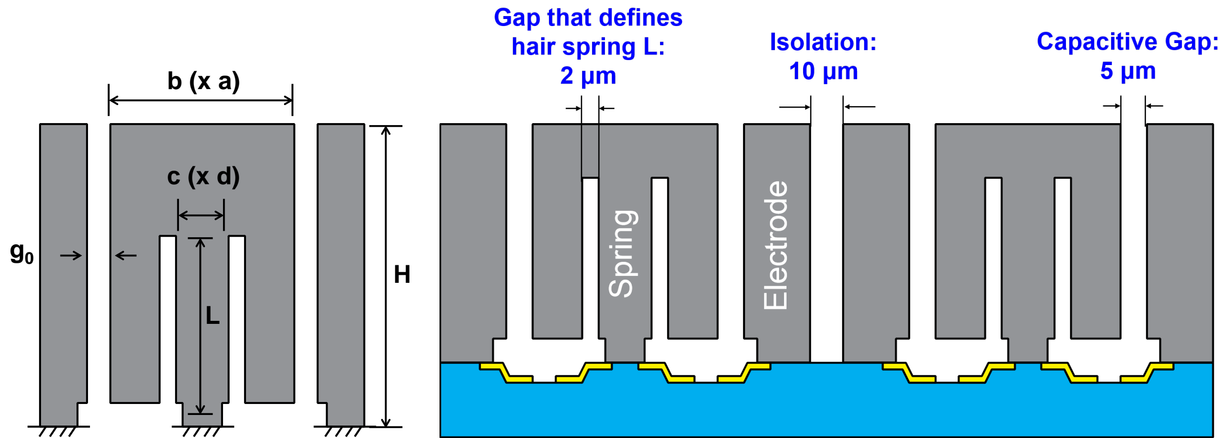


Fig. 4.1. Uniform-gap hair accelerometer: ultra-high aspect-ratio DRIE of trenches defines the device height, vertical hair spring length and isolation between neighboring electrodes.

5 μm sensing gap is optimal in achieving maximum device height (H) at almost full thickness (H < 500 μm), maximum spring length L (L < H) and large enough isolation gap between neighboring electrodes (10 μm). To increase the array layout density, the positive and negative axes along the same axis of two devices side by side are separated only by the 10 μm isolation gaps. Larger isolation gaps ($g_{isolation} = k \times g_0$) are desired to reduce the feedthrough between the positive and negative axis (Figure 4.2). However, $g_{isolation} = 10$ μm ($k = 2$) is the maximum dimension we can set due to DRIE lag: with large $g_{isolation}$, the wafer will be etched-through in step (a) in Figure 4.4.

The proof-masses are designed to have footprint (a × b) ranging from 200^2 - 500^2 μm^2 and hair spring cross-section (a × b) ranging from 30^2 - 50^2 μm^2. Four electrodes are arranged along two perpendicular sensitive axes and form four capacitors (X+, X-, Y+, Y-). To increase the capacitive sensitivity, arrays of 25 hair accelerometers are connected in parallel, i.e., the sensing capacitor from the same direction (X+, X-, Y+, or Y-) are connected in parallel (Figure 4.3). All the proof-masses within the array are electrically connected through the metal traces contacting

the conductive silicon hair spring at the spring bonding site.

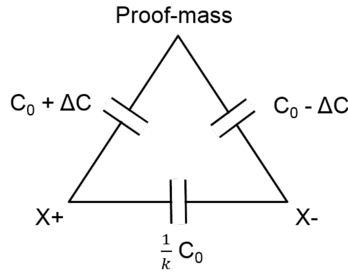
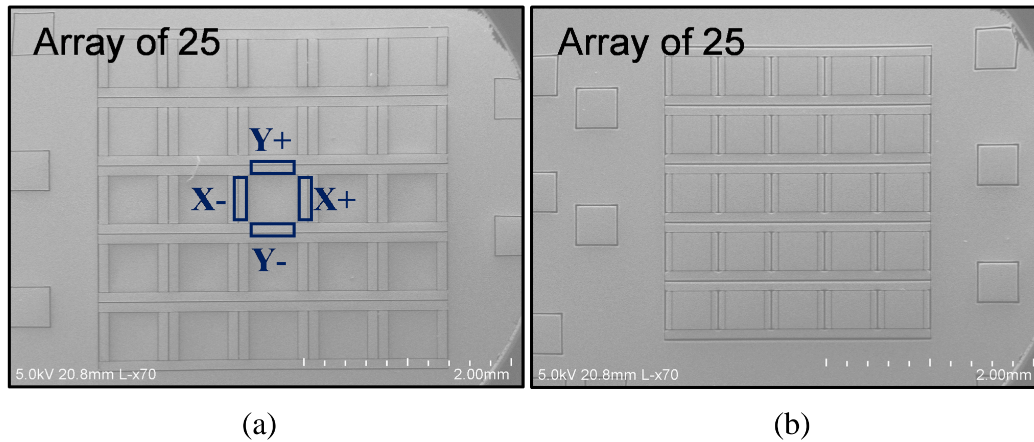


Fig. 4.2. Capacitive feedthrough due to the maximum separation gaps that can be realized by the SOG process in Fig. 4.4.



(a) (b)

Fig. 4.3. SEM of 25 (5×5) arrays of hair accelerometers: (a) Proof-mass footprint (a×b) equals 500×500 μm^2; (b) Proof-mass footprint (a×b) equals 400×400 μm^2.

The prototype 3D hair structure proposed in Figure 4.1 is fabricated using a silicon-on-glass (SOG) process (Figure 4.4).

(a) The process starts with a p-type double-side-polished 500 µm thick silicon wafer with 0.005 - 0.020 Ω-cm resistivity. A shallow recess of 2 µm is etched in the silicon wafer followed by a long deep reactive ion etching (DRIE) step to define the small capacitive gaps (5 µm) and the gaps surround the vertical hair spring within the proof-mass (2 µm), while simultaneously etching more deeply to separate neighboring electrodes (10 µm) by exploiting aspect ratio dependent etching (RIE lag).

(b) A Pyrex 7740 glass wafer is then patterned to define the anodic bond pads. A 3 μm deep recess is wet-etched by buffer hydrofluoric acid (BHF). The electrical interconnections are realized by a first metal layer (Ti/Pt of 200 Å /1500 Å) patterned by liftoff. These interconnections are in direct contact with the silicon springs that are later anodically bonded to the glass substrate. An optional second metal stack (Ti/Al of 200 Å /1500 Å) can protect the first metal layer from being sputtered during final DRIE step.

(c) The Si and glass wafers are aligned and anodically bonded at 400 °C.

(d) Finally, the bonded wafer stack is flipped and mounted on a 4-inch silicon carrier wafer. Without additional masking and patterning, blanket DRIE from the silicon side thins down the silicon and releases the proof-mass.

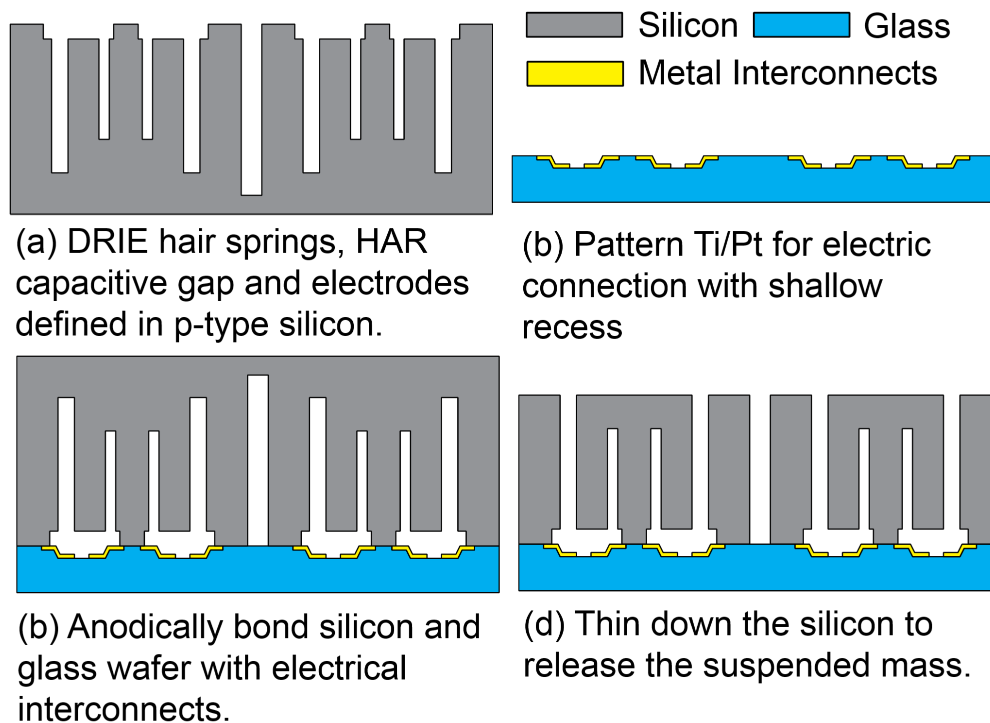


Fig. 4.4. Silicon-on-Glass (SOG) fabrication process for fabricating uniform gap hair accelerometer. The sensing gap g_0, mass height H and spring length L are defined by a single DRIE step.

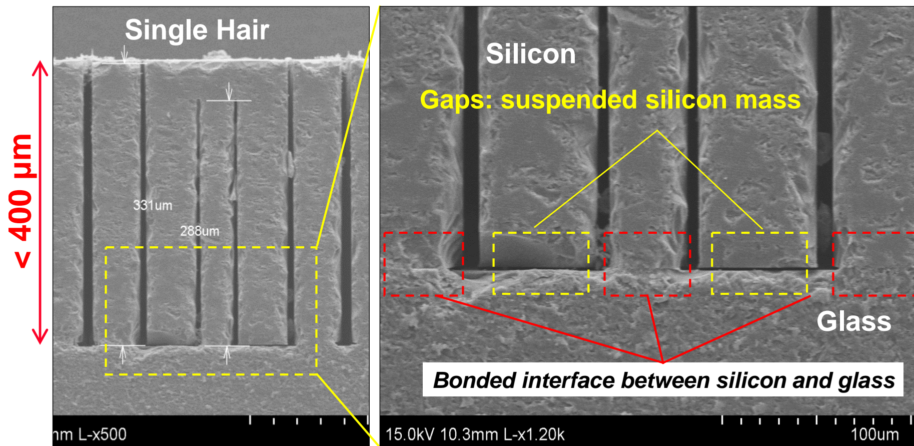


Fig. 4.5. Bonded silicon-glass interface: SEM of single hair structure cross-section and close-up of the silicon-glass interface.

Figure 4.5 shows the cross-section of a single hair structure and the close-up of the bonded silicon-glass after dicing the bonded wafer. The grain size of the two materials and the separation gaps between the proof-mass and glass substrate can be seen at the interface.

4.1.2 Silicon-Glass Anodic Bonding with Metal

Anodic bonding is a one of the key integration technologies in making 3D MEMS structures. It was first introduced in 1969 by Wallis and Pomerantz [1]. During a typical anodic bonding process, the glass wafer is usually placed on top of the silicon wafer. The cathode electrode is in contact with the glass wafer from the top. Temperature is risen to 350 - 400 °C before a bond voltage between 500 - 1000 Volt is applied to cause the diffusion of sodium ions (Na^+) away from the interface to toward the cathode. The temperature increases the mobility of the positive ions in glass. However, it should not exceed the glass transition temperature. As a result, in the glass wafer in contact with silicon a few micrometers thick high-impedance depletion region is formed. The potential drop across the few micrometers such that the electrical field intensity in the depletion region is very high, causing the oxygen ions to drift to the bond interface and react with the silicon to form SiO_2. The voltage is typically retrieved after the

current drops to certain percentage of the initial value I_0 (ex. 5%, 10%). After that slow cool down is preferred due to coefficient of thermal expansion (CTE) mismatch.

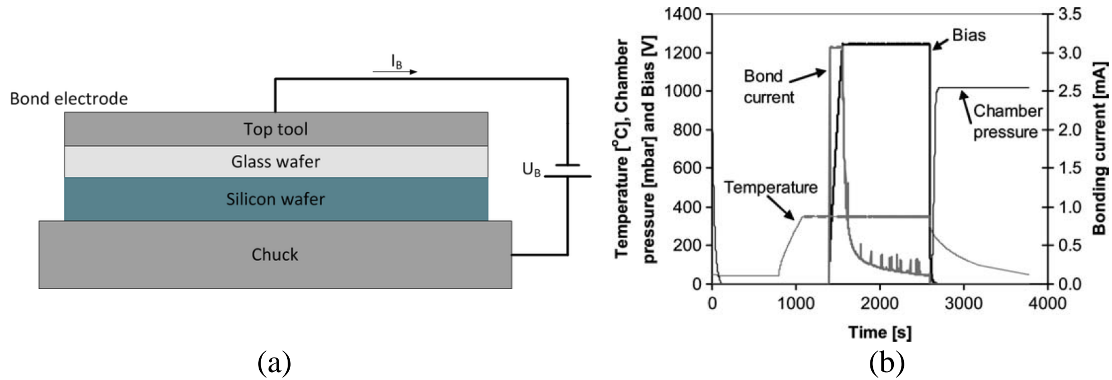


Fig. 4.6. Anodic bonding principle and plot of bonding parameters vs. time for a typical anodic bonding process.

Anodic bonding can provide hermetic seals and thus has been applied to a wide range of devices from inertial sensors, pressure sensors to microfluidic devices. Anodic bond can be formed between alkali-rich glass and semiconductor, as well as any metal. Among the different combinations, bonding of glass to silicon has been the most extensively investigated, although bonding to aluminum [2-3], polysilicon [4], thermal SiO_2 [5], and Si_3N_4[6].

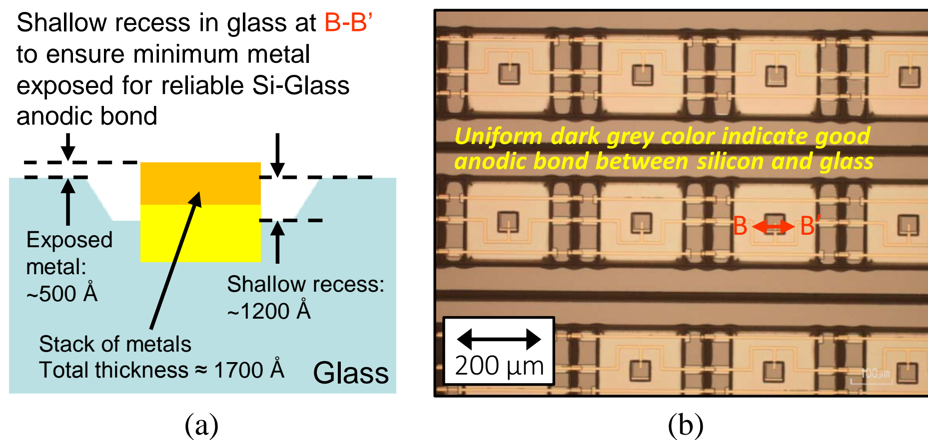


Fig. 4.7. Bonded silicon-glass interface: SEM of single hair structure cross-section and close-up of the silicon-glass interface.

In order to increase sensitivity, we should reduce the cross-sectional area of the hair

spring to make the it more compliant. Anodic bonding is chosen for its high bond strength and simplicity. However, it requires a minimum surface area for a successful bond and any material present between the silicon and glass substrate will prevent good contact between the two wafers. Thus, a shallow recess of 1200 Å is etched by BHF before the 1700 Å thick metal deposition. As shown in Figure 4.7(a), only ~500 Å of metal will breach the surface the glass substrate.

To minimize the spring cross-section area, we also ensure efficient pre-bond cleaning and apply plasma activation to the wafer surfaces to enhance the bonding strength. Good pre-bond alignment and optimization the anodic bond recipe (voltage, temperature, and annealing process) helps to ensure reliable bonding as well. For Si wafer pre-bond cleaning, we use H_2SO_4–H_2O_2 (1:1 Piranha) and HF solutions. In our case Piranha is necessary because polymers such as photoresist and CF_6-induced compounds can stick to the walls of the deep trenches during DRIE. Oxygen plasma activation is also used to treat both wafers before bonding. For both silicon and glass surfaces, the total surface energy increases even at low power or short plasma exposure times.

We pre-bond by applying - 500V at 250 °C for 30 minutes. Then we perform the second bonding step by applying -1300V at 350 °C. After the second bonding step is complete, we anneal the wafers at 350 °C for 1.5 hours and slowly ramp down to room temperature over 2 hours. With these settings, we achieve almost 100 % yield for posts with cross-sections larger than $30\,\mu m \times 30\,\mu m$ with the metal contact fingers (~500 Å higher than the glass substrate surface) between the silicon and glass substrates.

The anodic bonding quality is assessed visually as shown in Figure 4.7(b). The darker grey color indicates well-bonded areas while the light-colored areas represent the recess in the glass where the two substrates are separated. There are no visible particles at the interface.

A close-up of an array of hair accelerometer structures and their cross-section are presented in Figure 4.8, revealing the metal electrical interconnections on the glass substrate and the vertical silicon hair spring anchored securely to the glass bond pads by anodic bonding.

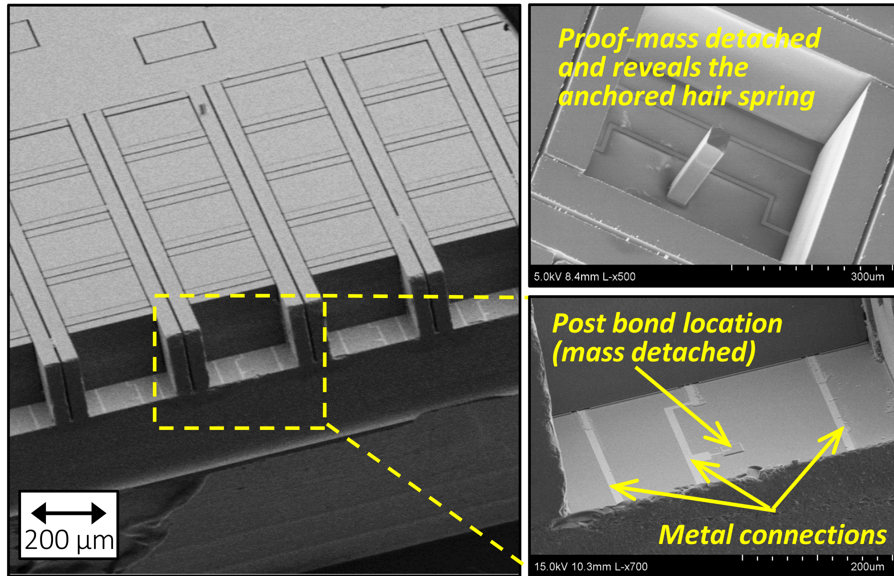


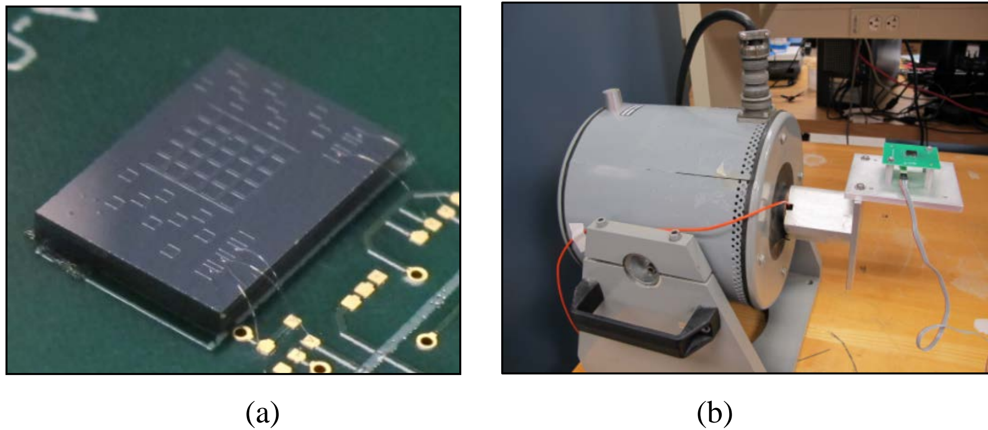
Fig. 4.8. Close-up of an array of hair accelerometer structures and their cross-section: vertical silicon hair spring is anodically bonded to the glass substrate and makes electrical contact with the metal fingers patterned on the glass substrate.

4.2 SOG Accelerometer Testing Results

Two-axis 25-element arrayed hair accelerometer chips with different design parameters are fabricated by the SOG process presented in Figure 4.4 and their electro-mechanical response is tested. Standard 500 μm thick highly-doped p-type silicon wafer is used such that the final device height H equals 400 μm. The single hair accelerometer footprint ($a \times b$) is varied from $200 \times 200\ \mu m^2$ to $500 \times 500\ \mu m^2$, whereas the spring cross-section area ($c \times d$) is varied from $30 \times 30\ \mu m^2$ to $50 \times 50\ \mu m^2$.

An Unholtz-Dickie 400ATE/C Transducer Calibration System is used to characterize the device under test (Figure 4.9).

We set the maximum acceleration and frequency of the shaker vibration motion and monitored the capacitance readout from an Analog Devices Capacitance-to-Digital Converter chip AD7746 CDC output. Since we connected the capacitors directly to the CDC inputs on the PCBs, parasitics are avoided as much as possible. The PCB was mounted in a way that one of the two sensing axes is aligned with the motion of the shaker.



(a) (b)

Fig. 4.9. Fabricated sensor chip mounted on PCB and then mounted on shaker table for electromechanical testing.

The testing was carried out by sweeping the maximum acceleration from 1 g to 24 g at an excitation frequency of 40 Hz. The motion follows a sine wave. The shaker can output acceleration ranging from 0.1 g to 100 g with a resolution of 0.01 g. It has a wide frequency range from 2 Hz to 10 kHz. COMSOL was also used to simulate the device sensitivity based on the measured fabricated device dimensions. However, the limit in the vibration amplitude means it is not feasible to apply high acceleration at very low frequency. In addition, the CDC chip had a sampling frequency at 90.9 Hz. This sampling rate is too low to reconstruct the sine waveform expected for the capacitance change at the vibration frequency of 40 Hz. Since it is above the Nyquist rate, we capture the envelope of the capacitance change and read the peak to peak values as we swept the acceleration magnitude. An example of the time domain measurement is shown in Figure 4.10.

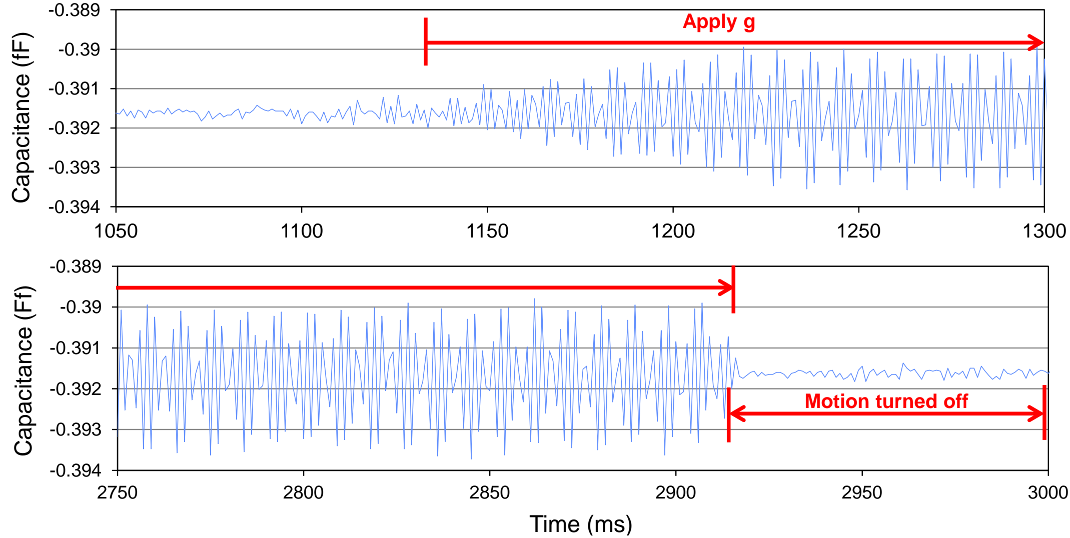


Fig. 4.10. Time domain capacitance change when shaker motion is turn on and off.

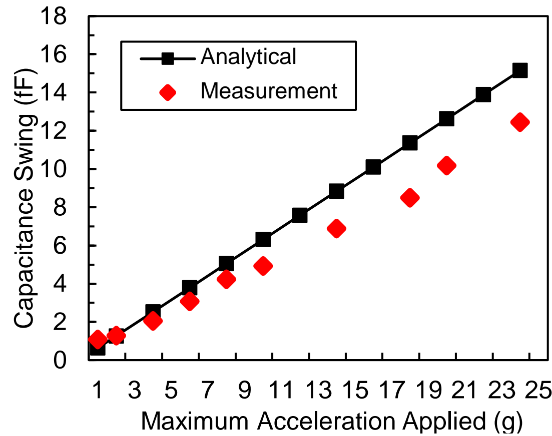


Fig. 4.11. Differential capacitance changes in X-axis of an array of 25 hair accelerometers connected in parallel when subjected to peak acceleration from 1 g to 24 g on Unholtz-Dickie shaker table. Each hair accelerometer in the array is composed of: 1) a 380 μm tall proof-mass that has footprint at $500 \times 500\ \mu m^2$; 2) a ~300 μm long spring that has a cross-sectional area of $50 \times 50\ \mu m^2$, and 3) nominal sensing gaps at 5 μm.

Figure 4.11 presents the differential capacitance change in the X-axis of one of the hair accelerometer arrays tested when subjected to peak acceleration from 1g to 24 g on the shaker table. We show the measured result compared with the analytical result of an array of 25 400-μm-tall SOG sensors ($500^2\ \mu m^2$ proof-mass, $50^2 \times 300\ \mu m^3$ spring and 5 μm g_0) when different levels of acceleration are applied. The differences are due to process variation from the designed

dimensions and parasitic capacitance. The differential mode measurement shows a more linear curve than the single-ended measurement. Due to the symmetry of the structure, common-mode noise is canceled in differential mode measurement.

Differences in the measured and simulated data are due to the discrepancies between the exact spring/gap profiles of the fabricated devices and the dimensions assumed in the COMSOL simulation based on the SEM measurement. Parasitics associated with electrical routing and wire bonding will also degrade the capacitive sensitivity.

The frequency response of the sensor array is measured using a standard bias-drive-sense method for the first bending mode. An AC signal is applied to one electrode and the resulting signal is picked off at the other side, 180˚ offset. Table 4.1 lists the simulated resonant frequencies for the first bending mode. A narrower spring (i.e., a smaller bond area) leads to more compliant springs, while a larger mass decreases the resonant frequency. The DC bias applied to the proof mass creates a force which softens the spring, thus decreasing the vibration resonant frequency of the hair structures.

Table 4.1: Measured vs. simulated resonant frequencies (in kHz) for different mass and post sizes for 5x5 hair accelerometer arrays.

Mass Size (a×b) ⇓	Spring Area (c×d) ⇒	Resonant Frequency (kHz)		
		30^2 μm^2	40^2 μm^2	50^2 μm^2
400^2 μm^2	Simulated	15.76	27.85	43.13
	Measured	16.5	27.6	41.5
500^2 μm^2	Simulated	12.57	22.29	34.55
	Measured	11.7	20.6	32.6

Figure 4.12 compares the frequency response of two different arrays having different proof-mass sizes (a × b) and the same spring (c × d): The 400^2 μm^2 array has resonant peak at 16.5 kHz and the 500^2 μm^2 array has resonant peak at 11.7 kHz. Multiple peaks are observed due

to variation in mass/spring dimensions across the array as well was asymmetric electrical routings at each accelerometer in the array.

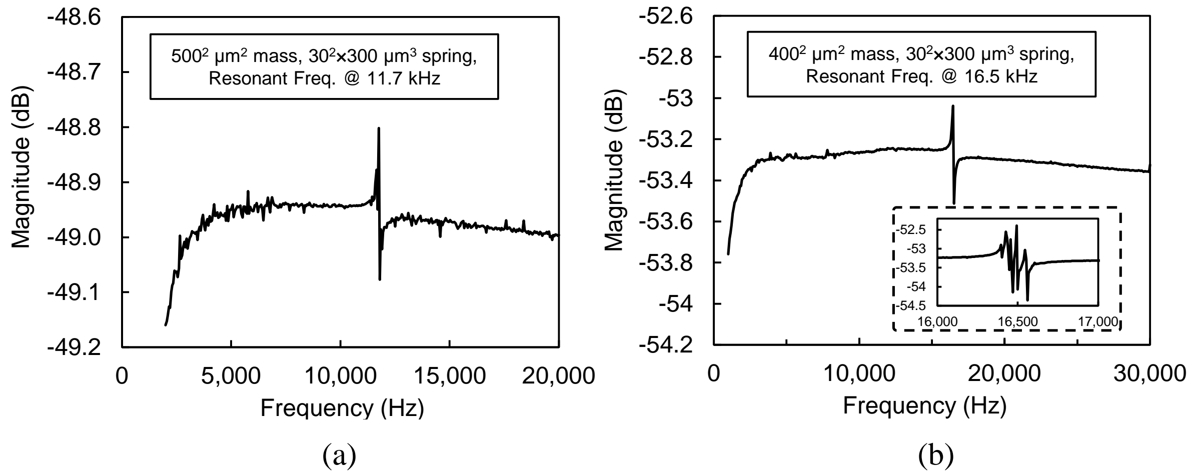


Fig. 4.12. Frequency response of two different hair accelerometer arrays both with $30^2 \times 300\,\mu m^3$ hair springs: (a) Proof-mass footprint ($a \times b$) equals $500 \times 500\,\mu m^2$; (b) Proof-mass footprint ($a \times b$) equals $400 \times 400\,\mu m^2$.

4.3 References

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Chapter 5 TWO-GAP HAIR STRUCTURE

5.1 Design Objectives

In Chapter 4 we present the first-generation uniform-gap biomimetic hair-like accelerometer arrays using a Silicon-on-Glass (SOG) process. Each accelerometer is composed of a proof-mass supported by a vertical hair-like spring and surrounded by four silicon electrodes. Each electrode is separated from the proof-mass by a capacitive transduction gap. The spring is vertical and located in the center of the proof mass. For the first bending mode, the spring-mass bends along one of the two orthogonal axes toward one of the four electrodes (x+, x-, y+, y-) when inertial force is applied, closing the gap between the proof-mass and the electrode.

In the SOG process, the minimum gap must be > 5 μm for a maximum achievable device height H of only 400 μm and spring length L of less than 300 μm. Although these numbers were quite impressive, more compliant spring and taller proof-mass are needed for higher performance sensing systems.

To achieve higher performance sensing systems, we need to overcome the limitations in device fabrication. In the SOG device design, the gap between the proof mass and the electrodes is defined using a single DRIE step performed on one side to the maximum height achievable by DRIE (Figure 4.4). Even with an advanced DRIE process for etching ultra HAR in silicon, due to DRIE lag and etch limitation, there is a direct correlation between the maximum device height, the maximum vertical spring length, and the minimum sensing gap. Deeper etches require a

larger gap, and this limits sensitivity. Thus, to achieve narrow gap for higher sensitivity, device height and spring length had to be reduced.

Ideally, a narrow gap, long vertical spring and tall device are needed for improved sensitivity. This can be achieved by using the 2-gap structure as shown in Figure 5.1, highlighting all the critical design parameters (device height **H**, spring length **L** and width **b**, two-part sensing gap (**g_{top}, g_{top}**, and top gap height **h_{top}**). Since the sensing area **A** is defined by the gap height h_{top} and the width of the capacitive plate **a** ($A = h_{top} \times a$), we also need to increase **h_{top}** in addition to increasing **H**, **L**, and reducing **b**, **g**.

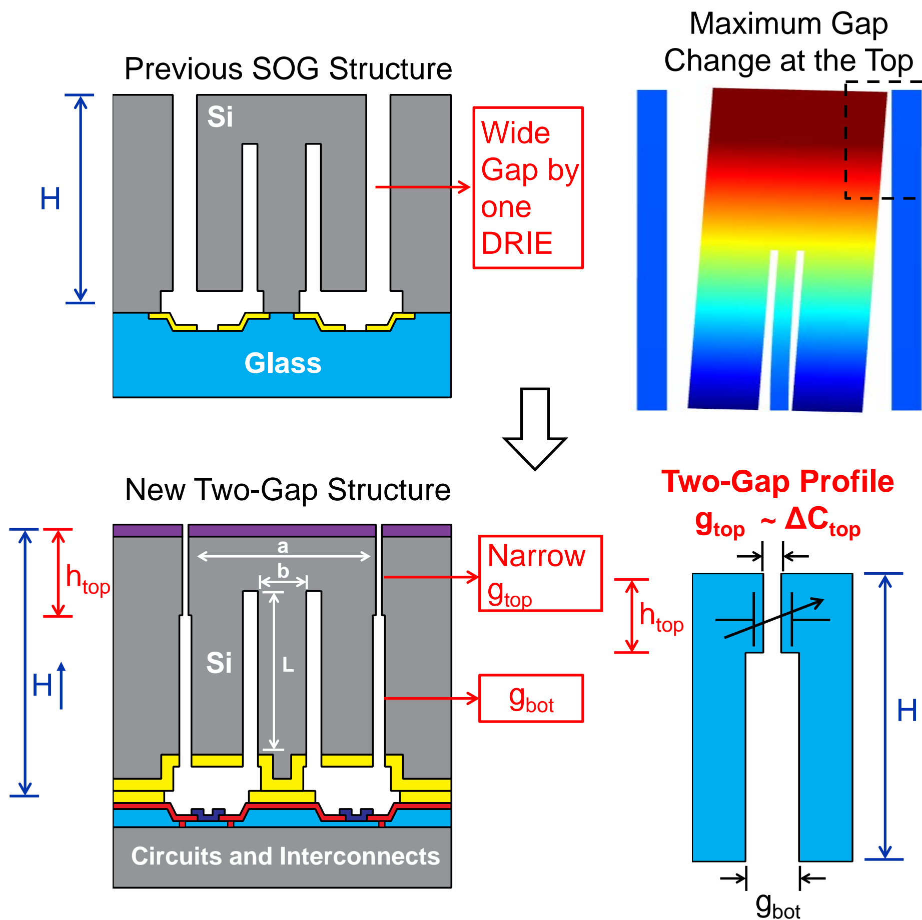


Fig. 5.1. 2-gap structure compared with SOG structure with uniform capacitive gap: Deflection of the proof mass under applied force is maximum at the top where the top gap g_0 (g_{top} / h_{top}) contributes to ΔC_{top}.

The top of a vertical inverted pendulum (proof-mass) undergoes the maximum deflection under applied lateral (in plane) inertial force. Thus, the capacitive sensing gap near the top of a vertical capacitive transducer contributes a larger fraction of the total change in capacitance, ΔC. This is verified by COMSOL simulation of various gap profiles (Figure 5.2). The total vertical sensing gap consists of two parts, g_{top} that extends h_{top} and g_{bot} that extends h_{bot}. For a uniform gap ($g_{top} = g_{bot} = 5$ μm) device, the top 40 % ($h_{top} / H = 0.4$) of the gap contributes > 60 % of ΔC_{total} (C). For $g_{top} = 2$ μm, $g_{bot} = 10$ μm and $h_{top} / H = 0.2$, $\Delta C_{top} / \Delta C_{total}$ is > 90 % (A).

Therefore, to achieve high sensitivity, one does not need to etch a narrow gap through the entire device height. A narrow gap near the top of a tall device is sufficient to improve sensitivity.

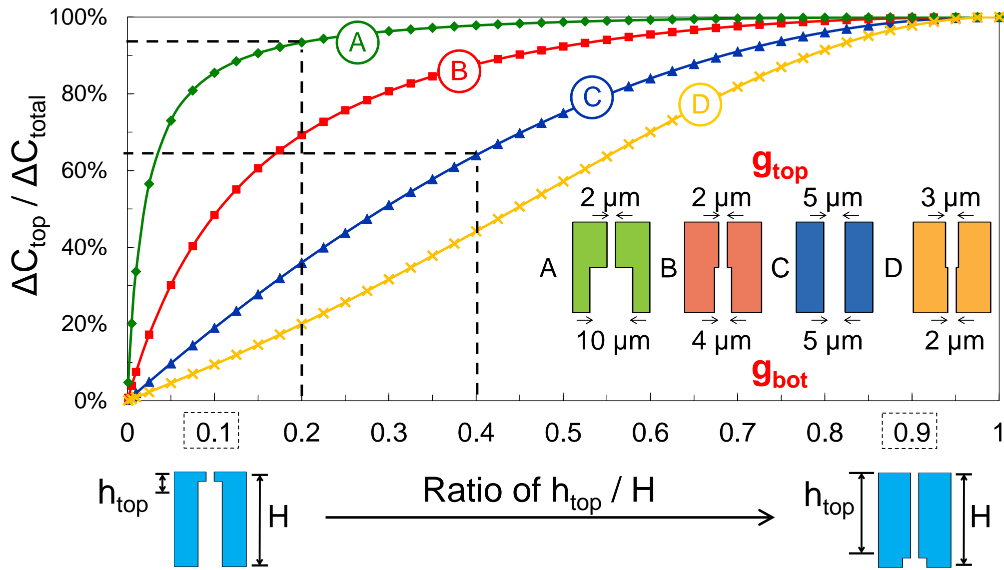


Fig. 5.2. ΔC_{top} contributes to most of total ΔC_{total}.

The proposed new 2-gap structure allows g_{top} to be made very narrow and tall, and removes limitation on device height due to DRIE lag. This high-sensitivity 2-gap process is achieved primarily by creating a narrow gap through the top ~ 40 % of the device height, and a wider gap (which is much easier to etch) through the rest of device height.

The device height (H) is not limited by DRIE etch and can be further increased. The new design allows all the critical structural dimensions to be independently varied. More detailed analysis on the application this structure to the hair accelerometer design will be presented in the next Chapter 6.

5.2 Two-Gap Process

The CMOS-compatible two-gap dry-release all-silicon fabrication process is shown in Figure 5.3. One silicon wafer with arrays of 3D MEMS accelerometers and a second silicon wafer with electrical interconnects (or circuits) are fabricated separately and eutectically-bonded together. Silicon-Au eutectic bonding at 400 °C is used in the current process, which can be replaced by CMOS-compatible Al-Ge at 450 °C.

(a) A 4 μm recess is created in a 1 mm thick highly-doped silicon wafer by deep reactive ion etching (DRIE). These recessed areas mainly suspend the proof-mass over the 2nd silicon substrate so that when the proof-mass tilts toward the contact electrodes, the bottom of the proof-mass will not touch the bottom substrate. After the recessed is formed, > 4 μm of LPCVD silicon oxide (SiO_2) is deposited. This oxide layer serves as the hard-mask against long DRIE during both the front-side and back-side etching. The front-side is the side that will be in contact with and eutectically-bonded to the 2nd silicon wafer patterned with gold. The oxide on the front-side is patterned to defined the boundaries of the vertical hair spring, the proof-mass and electrodes.

(b) Deep, high aspect-ratio DRIE masked by the front-side oxide is controlled by the different opening sizes as well as the total etch duration. After DRIE, the wafer is cleaned by oxygen plasma at 150 °C and 800 W followed by Piranha clean. The remaining front-side oxide hard mask is then removed by BHF while the back-side oxide mask is protected by hard-baked

photoresist. 5000 Å gold is blanket deposited to prevent the silicon from being oxidized, as well as to serve as the silicon-gold eutectic bonding inter-layer.

(c) The next step is carried out on the 2nd silicon substrate. 4 µm of LPCVD silicon oxide (SiO_2) is deposited as passivation layer before 3 µm deep recess is plasma etched. In-situ doped polysilicon of 0.6 µm serves as the electric interconnections over the passivation oxide. The poly-silicon is deposited in LPCVD furnace, patterned and etched by RIE. Since the polysilicon traces will be exposed to plasma during release DRIE, another passivation oxide is patterned and etched, covering the polysilicon traces where they will be exposed.

(d) After that, 1 µm thick gold for gold-silicon eutectic bonding is patterned by lift-off and evaporation.

(e) The 1st silicon wafer and 2nd silicon wafer are aligned and eutectically bonded. Detailed analysis of silicon-gold eutectic bonding principles and results will be presented in the next Chapter 6 on the fabricated hair accelerometer array chips.

(f) After the 4-inch wafer stack (1 mm silicon device wafer + 500 µm silicon) are diced ~1.1 mm deep from the top of the 1 mm silicon slide. The process is completed with a release DRIE step from top of the bonded wafer stack that defines the narrow 2 µm capacitive sensing gap.

The device height is not limited to 1 mm and the process can be applied to any full-wafer thickness. By taking advantage of ultra-HAR DRIE presented in Chapter 3, g_{bot}, the wide gaps can be etched even deeper than 1mm (1.5 mm, 2 mm, etc.) by using masking layer thickness or material that can withstand the long etch to achieve a greater device height. For example, we use ~4 µm of silicon dioxide in the current process. The size of the top gap, g_{top} of 2 µm at 300 µm can also be further narrowed if needed by further optimizing the DRIE process, or by narrowing the gap through deposition of additional films.

Since this process can build high performance devices within a small footprint, it can be applied to high-density sensor arrays where hundreds or thousands of sensors will be addressed simultaneously.

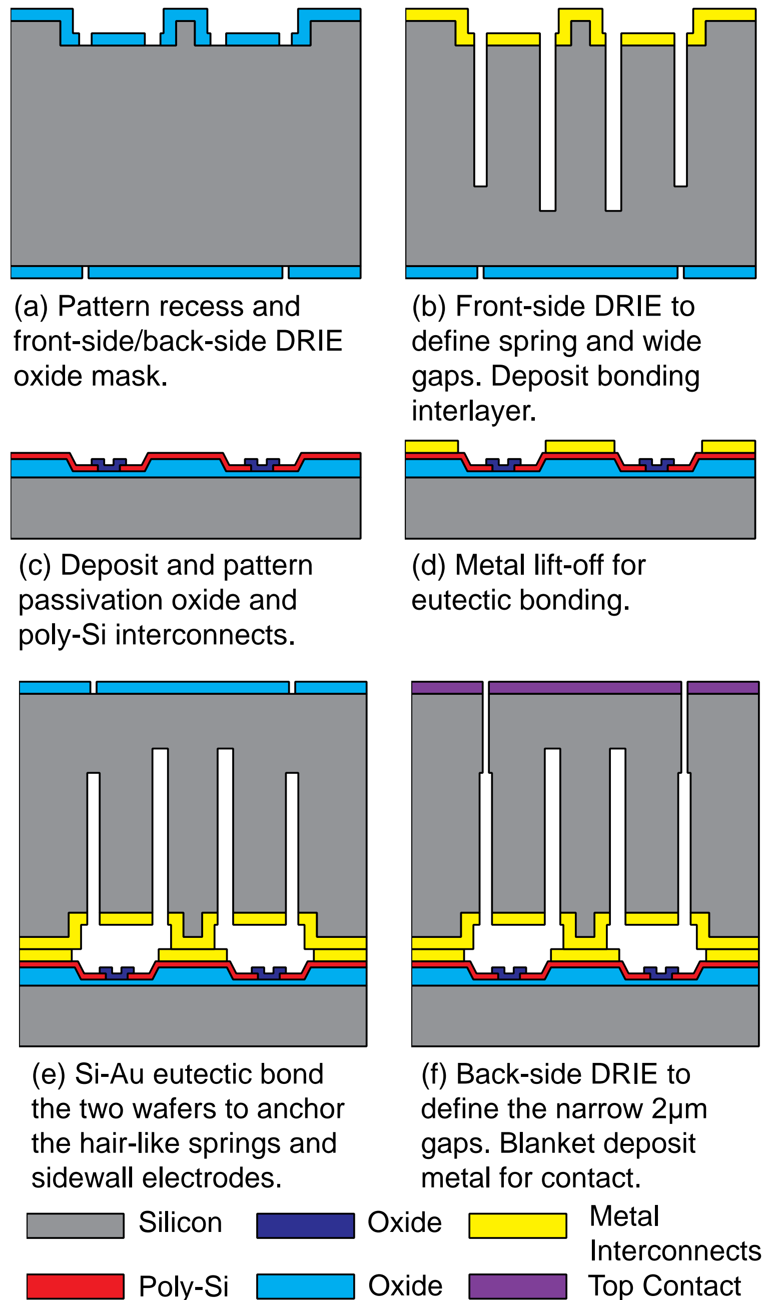


Fig. 5.3. Two-gap CMOS compatible dry-release all-silicon fabrication process.

This process also enables bonding of the HAR MEMS sensor array on top of signal processing CMOS circuits necessary to realize the various sensor arrays' functions. Since MEMS sensors with HAR transduction gaps and CMOS circuits can be fabricated separately, this process removes the constraints in temperature, materials, chemicals and transducers' design that an integrated MEMS-CMOS process imposes. Compared to metallic structural layer that are available in the CMOS process that have limited height and aspect-ratio, the HAR 2-gap structure is more desirable for high performance MEMS Inertial Measurement Units (IMUs).

All the layout dimensions are determined experimentally by adjusting DRIE parameters and total etch duration on 1 mm thick silicon wafers. The two gaps g_{top} and g_{bot} are designed so that they will connect after the final DRIE of the smaller g_{top} to ensure successful device release (Figure 5.4). The oxide hard mask for both the front-side and back-side DRIE have to survive the total etch duration respectively.

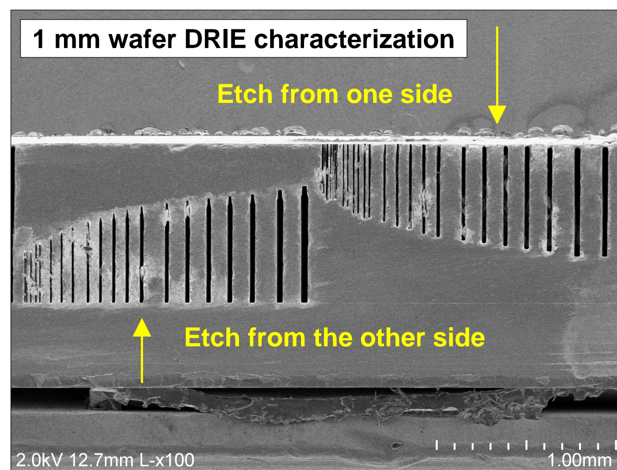


Fig. 5.4. DRIE characterization to determine the gap dimensions and etch depth to ensure the release of the capacitive hair accelerometer.

Figure 5.5 presents the SEM cross-sections of the fabricated 2-gap structure: two neighboring 1 mm tall structure with $g_{top} = 2$ µm extending 300 µm and spring length L = 700 µm

etched by a g_{bot} opening at 35 µm. The majority of the device height is also defined by 35 µm trench openings.

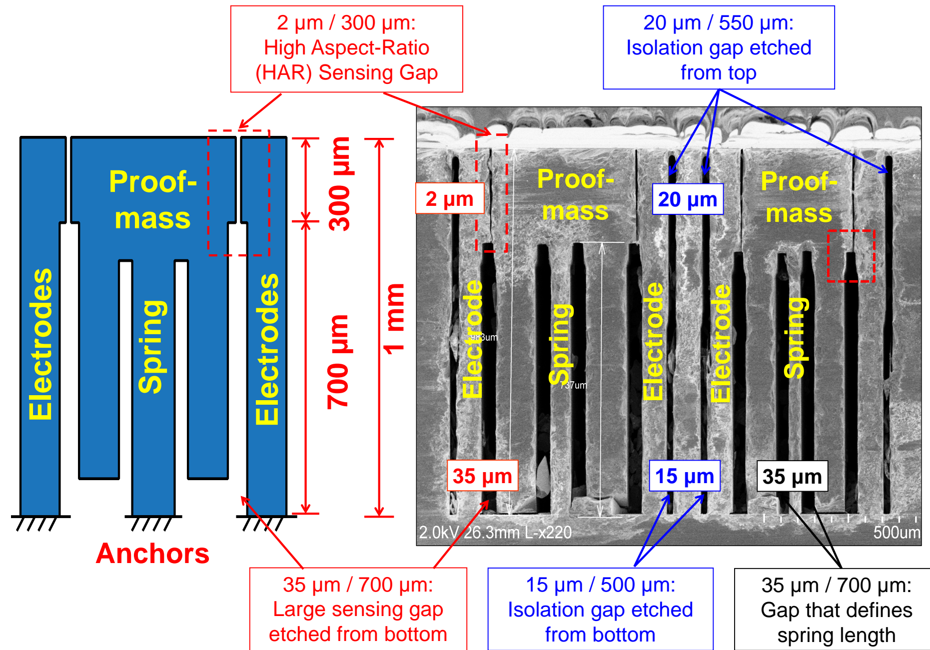


Fig. 5.5. SEM cross sections of fabricated 2-gap devices: two neighboring 1 mm tall devices with $g_{top} = 2$ µm extending 300 µm and spring L = 700 µm.

Close-up of the small and large gap junction is highlighted in Figure 5.6. The 5-6 µm misalignment is attributed to the 4-inch wafer-level contact exposure procedure.

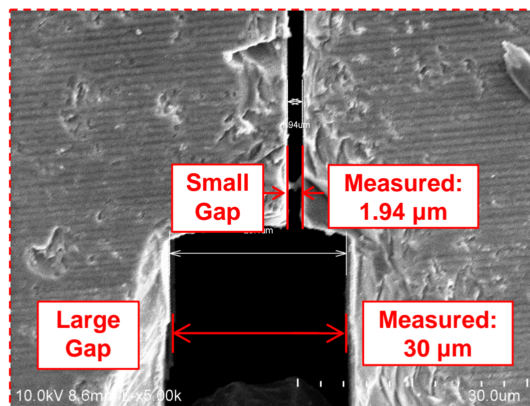


Fig. 5.6. Junction of g_{top} and g_{bot}.

The misalignment of the top and bottom gaps will cause imbalance of the proof-mass between the positive and negative directions along the sensing axis. If the misalignment is 5 μm, one side will have (h_{top}×10 μm) more mass per unit width of electrode.

Since the device sense in-plane lateral acceleration by capacitors along the sidewall, the mass-imbalance does not contribute to offset error or scale-factor error.

Chapter 6 LOW-NOISE HIGH-SENSITIVITY MULTI-AXIS CAPACITIVE HAIR ACCELEROMETER

To build high performance capacitive MEMS accelerometer, we need to optimize the hair structure and transducing element design targeting both high capacitive sensitivity (>1 pF/g/mm^2) and low Brownian noise floor (sub-μg/√Hz). With 1 pF/g capacitive sensitivity, if the front-end readout circuit can resolve $\Delta C = 1$ aF, we can detect 1 μg change in acceleration.

The dominant mechanical noise source for micromachined capacitive accelerometers at atmosphere or higher pressure is mainly limited by the thermos-mechanical noise associated with the Brownian motion of the gas molecules surrounding the device within the package [1]. To achieve thermomechanical noise below 1 μg/√Hz and high sensitivity per unit area for capacitive MEMS accelerometers, efforts have been made toward realizing both large proof-mass and narrow and high aspect-ratio (HAR) sensing gaps. Increasing the proof-mass size has proven to be the most effective way to reduce mechanical noise [1-3], while reducing the sensing gap is the most effective way to increase sensitivity. The former increases the device area, which is not desirable due to cost, while the latter contributes to gas damping that increases Brownian noise.

Using existing technologies, the MEMS device footprint has to be increased to allow for large proof-mass and sense area because the device height is typically limited to $\leq 500\,\mu m$ (Table 6.1). SOG [1] and CMOS MEMS [3] capacitive accelerometer that demonstrated

$< 10\ \mu g/\sqrt{Hz}$ noise floor have limited proof-mass thickness, typically $< 150\ \mu m$ and $5\ \mu m$ respectively. Thus, the device footprint must be increased. A HARPSS-SOI process has also been explored to increase proof-mass by utilizing the silicon mass on the backside of the SOI handle wafer (400 µm) [2]. Although a noise floor of $< 200\ ng/\sqrt{Hz}$ is reported, the device footprint is large (49 mm^2) due to the limited gap height and device height.

It is desired to achieve 1 pF/g capacitive sensitivity by capacitive type sensor since 1 µg change in acceleration can be detected (navigation grade) if the front-end readout circuit can resolve $\Delta C = 1$ aF.

Table 6.1: Low-noise high-sensitivity capacitive accelerometer in literature.

	[1]	[2]	[3]	This Work
Technology	SOG	SOI MEMS	CMOS MEMS	3D Vertical Hair
Mass Footprint	1.3 mm × 3 mm	5 mm × 7 mm	160 µm × 350 µm	4 mm × 250 µm
Overall Area	2.2 mm × 3 mm	7 mm × 7 mm	350 µm × 500 µm	4 mm × 350 µm
Sensor Height	120 µm	500 µm	5 µm	1 mm
Res. Freq.	2.14 kHz	8.9 kHz	200 Hz	627 Hz
Sensing Gap	2.0 µm	4-5 µm	1.5 µm	2–2.7 µm
Gap Height	120 µm	100 µm	< 5 µm	> 250 µm
Sensitivity	0.8 fF/g	> 30 pF/g	0.13 fF/g	> 1 pF/g
Sensitivity / mm^2	0.091 fF/g/mm^2	> 0.6 pF/g/mm^2	0.74 fF/g/mm^2	~ 1 pF/g/mm^2
BNEA*	10 $\mu g/\sqrt{Hz}$	< 200 $ng/\sqrt{Hz}$	6.9 $\mu g/\sqrt{Hz}$	< 1 $\mu g/\sqrt{Hz}$
*BNEA: Brownian Noise Equivalent Acceleration				

In this work, by utilizing thick silicon wafers of more than 500 µm (1-2 mm, etc.), we can greatly increase the proof-mass size per unit area, thus providing higher sensitivity and lower mechanical noise floor. This is realized by the unique vertical 3D hair-like capacitive structure we present in Chapter 2 [4] and a robust 2-gap fabrication technology we present in Chapter 5 [5] facilitated by well a characterized ultra-high aspect-ratio Bosch DRIE presented in Chapter 4. A wide range of device performance can be designed based on this structure.

6.1 Objectives: High Sensitivity (>1pF/g/mm^2) and Low Noise Floor (sub-µg/√Hz)

Each hair-like accelerometer structure (Figure 6.1) has a thick silicon proof-mass supported by two (or one on the center) vertical hair-like spring, and located on the two ends of the proof-mass along the axis normal to the sensing axis direction. Small spring constant can be achieved while reducing cross-axis sensitivity. The proof-mass is surrounded by multiple sense/feedback electrodes that are separated from the proof-mass by narrow capacitive transduction gaps. Multiple electrodes are implemented to enable fully symmetric differential readout, and provide force feedback for closed-loop operation.

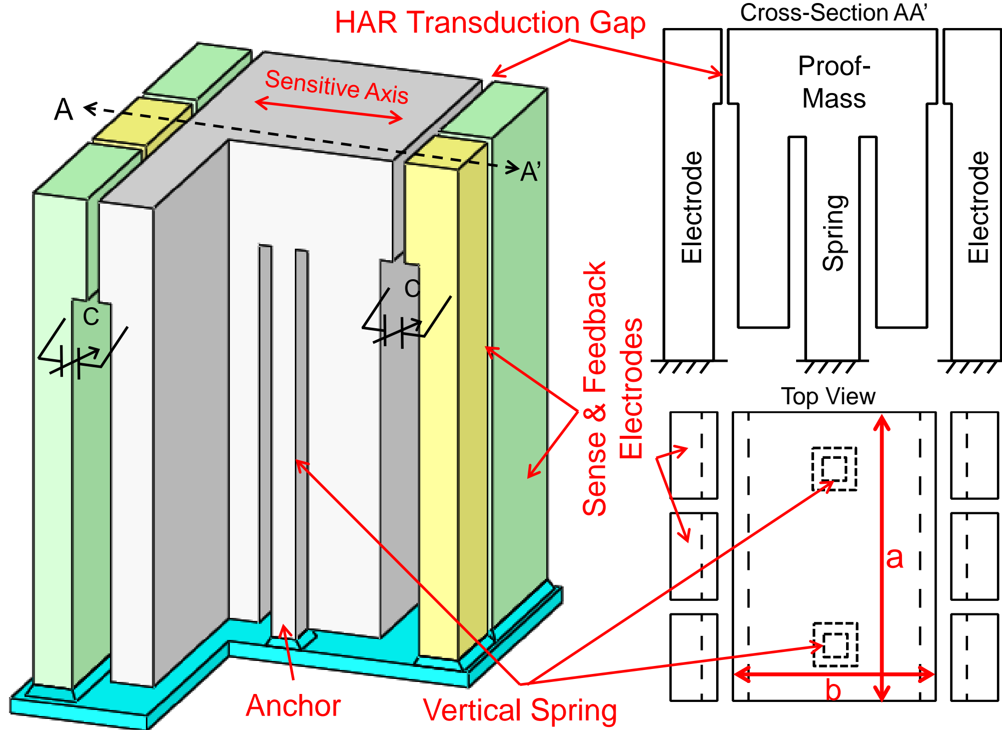


Fig. 6.1. High aspect-ratio two-gap hair-like accelerometer: tall proof-mass (1 mm), vertical spring, sense/feedback electrodes, and high aspect-ratio capacitive transduction gaps.

Critical design parameters are: proof-mass height H and footprint area (a × b), spring length (L) and cross-section (c × d), and the two-part transduction gaps. The top gap g_{top} extends a height of h_{top} and the bottom gap g_{bot} extends a height of h_{bot} (Figure 6.2).

Since the top of a vertical inverted pendulum (proof-mass) undergoes the maximum deflection under applied lateral (in plane) inertial force, the gap profile can be approximated as a trapezoidal shape. When the displacement is small, the change in capacitance can be written as:

$$\Delta C = C_1 - C_0 \approx \varepsilon A \frac{m \cdot accel./k}{2g_0^2} = \frac{1}{2}\varepsilon \times WH \times \frac{m_{eff}}{k_{eff}} \times \frac{1}{g_0^2} \times accel. \quad (6.1)$$

$$m_{eff} \propto H, \quad k_{eff} \propto \frac{1}{L^3} \propto \frac{1}{H^3} \quad (6.2)$$

$$\frac{\Delta C}{\Delta accel.} \propto H \times \frac{H}{1/H^3} \times \frac{1}{g_0^2} = H^5 \frac{1}{g_0^2} \quad (6.3)$$

The capacitive sensitivity (S) of the two-gap accelerometer is highly dependent on the gap dimensions, the proof-mass size and spring dimensions.

$$S = \frac{\Delta C_{total}}{\Delta accel.} \propto \frac{1}{2}\varepsilon \times (h_{top}\frac{m_{eff}}{k_{eff}}\frac{1}{g_{top}^2} + h_{bot}\frac{m_{eff}}{k_{eff}}\frac{1}{g_{bot}^2}) \quad (6.4)$$

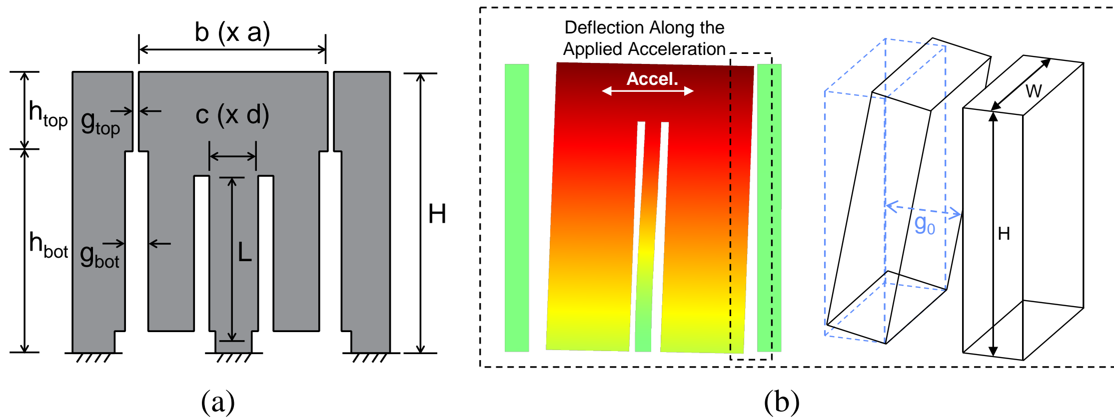


Fig. 6.2. (a) Critical design parameters of the two-gap hair-like accelerometer (Cross-section AA' in Figure 6.1); (b) Deflection profile of the hair structure and sense gap profile of the inverted pendulum design with applied acceleration.

From Equation (6.1) through (6.4), it is shown that the sensitivity scales with $\boldsymbol{1/g_{Initial}^2}$ and $\boldsymbol{H^5}$. The device height plays a critical role in improving the sensitivity for this accelerometer

design by utilizing the third dimension. H = 1 mm provides large proof-mass (> 2.33 milligram/mm^2) and can be further increased by using thicker silicon wafers than 1 mm.

COMSOL simulation of capacitive sensitivity verified that the capacitive sensing gap near the top of a vertical capacitive transducer (**g_{top}**) contributes a larger fraction of the total change in capacitance, **ΔC_{total}** since the proof mass undergoes the maximum deflection at the top. As shown in Figure 6.3, for a uniform gap ($g_{top} = g_{bot} = 2$ μm), the top 30 % ($h_{top} / H = 0.3$) of the gap contributes about 50 % of ΔC_{total} (black). It does not matter what ratio of is h_{top} / H evaluated along the height, the sensitivity ΔC_{total} per unit acceleration is fixed and is normalized to 1 in Figure 6.3(a).

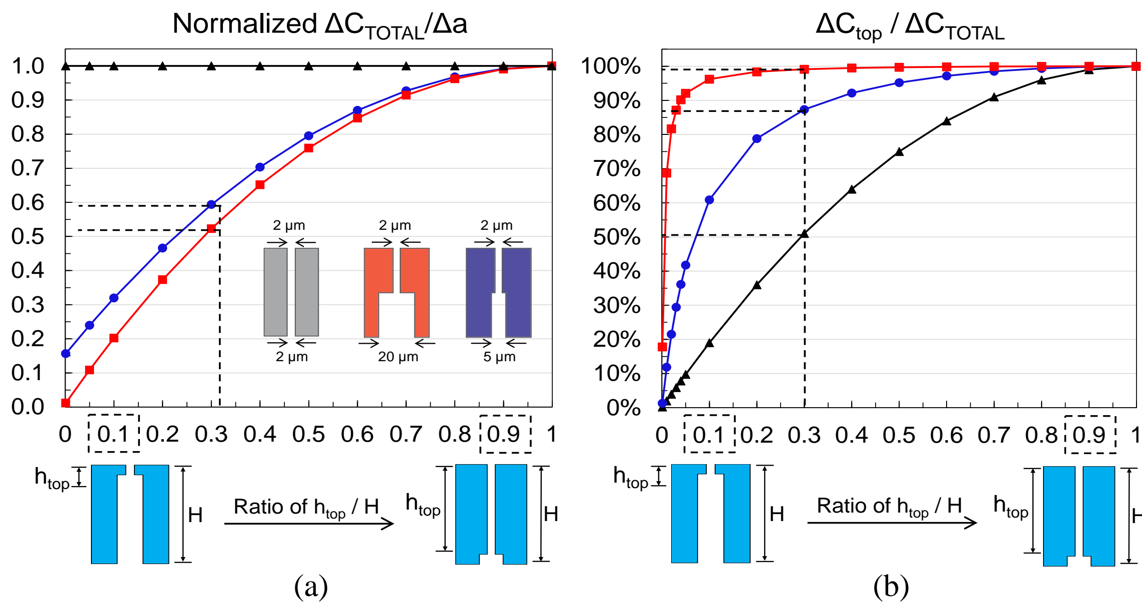


Fig. 6.3. (a) Sensitivity ΔC per unit acceleration and (b) Contribution of ΔCtop to the ΔCtotal for different gap profiles (g_{top}/h_{top} and g_{bot}/h_{bot}).

For $g_{top} = 2$ μm, $g_{bot} = 5$ μm and $h_{top} / H = 0.3$, $\Delta C_{top} / \Delta C_{total}$ is > 85 % (blue) and ΔC_{total} per unit acceleration is almost 60 % of the sensitivity of a 2 μm uniform narrow gap profile device. For $g_{top} = 2$ μm, $g_{bot} = 20$ μm and $h_{top} / H = 0.3$, $\Delta C_{top} / \Delta C_{total}$ is > 90 % (red) and ΔC_{total} per unit acceleration is greater than 50 % of the sensitivity of a 2 μm uniform narrow gap profile device.

Thus, to achieve high sensitivity, one does not need to etch a narrow gap through the entire device height. A narrow gap near the top of a tall device is sufficient to improve sensitivity.

The Brownian noise associated with the squeeze film damping effect in air increases significantly with reduction of the gap opening. There's tradeoff between sensitivity and noise floor. The nominal gap (g_0) should be reduced and sensing area ($A = W \times L$) should be maximized to increase the capacitive sensitivity. While the damping factor D increases with the parallel plate capacitor width (W) and length (L), and is inversely proportional to g_0 as in Equation (6.5). For the two-gap hair structure, $h_{top} = 200\,\mu m$ is typically smaller than the longer edge (dimension a in Figure 6.1) of the proof-mass footprint, thus $W = h_{top}$ a and $L = a$. Viscosity of air μ is assumed to be 18.76×10^{-6} [Pa·s] and $f(W/L) \approx 0.99$. Thus, we should not reduce the gap indefinitely.

$$D \approx f\left(\frac{W}{L}\right)\mu\left(\frac{W}{g_0}\right)^3 L \tag{6.5}$$

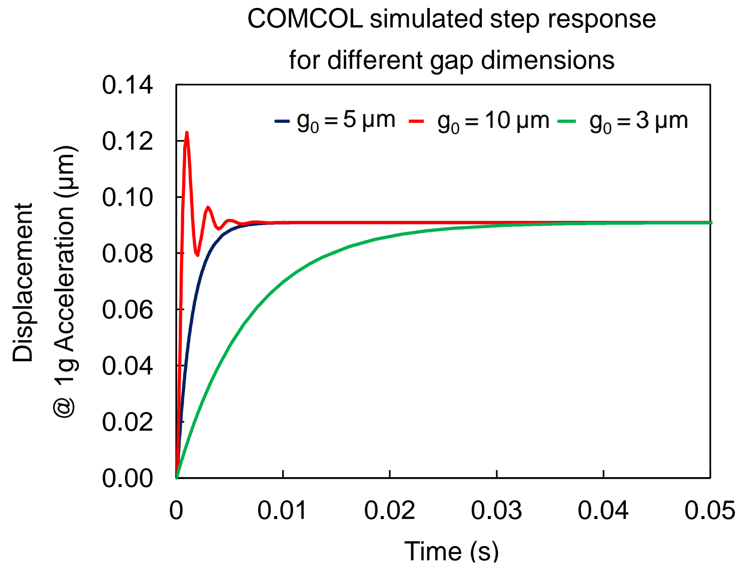


Fig. 6.4. COMSOL solid mechanics model including squeeze film damping effect for different sensing gap dimensions of 3 µm, 5 µm and 10 µm at 100 mTorr.

The effect of reducing the gap is shown in Figure 6.4 by COMSOL simulation combining solid mechanics module and squeeze film damping for different sensing gap dimensions of 3 µm, 5 µm and 10 µm at 100 mTorr. The proof-mass footprint is 500 µm×200 µm with

500 μm×200 μm sensing area on both sides of the proof-mass. The spring dimensions are 20 μm×20 μm×80 μm. We can see that the smaller the gap, the higher the damping.

Furthermore, the proof-mass size is more effective design parameter since both sensitivity and Brownian Noise Equivalent Acceleration (BNEA) are improved with large mass.

$$BNEA = \sqrt{\frac{4k_B TD}{M^2}} = \sqrt{\frac{4k_B T\omega_0}{MQ}} \propto \frac{1}{gap^{3/2}} \tag{6.6}$$

In this design, the gap and proof-mass size are weakly dependent. Tall device, narrow gap, and long/thin vertical springs are needed for improved sensitivity and reduced BNEA. Both $\mathbf{g_{top}}$ and **H** can be optimized without compromising the sensitivity or the mechanical noise floor, realized by the two-gap process presented in Chapter 5.

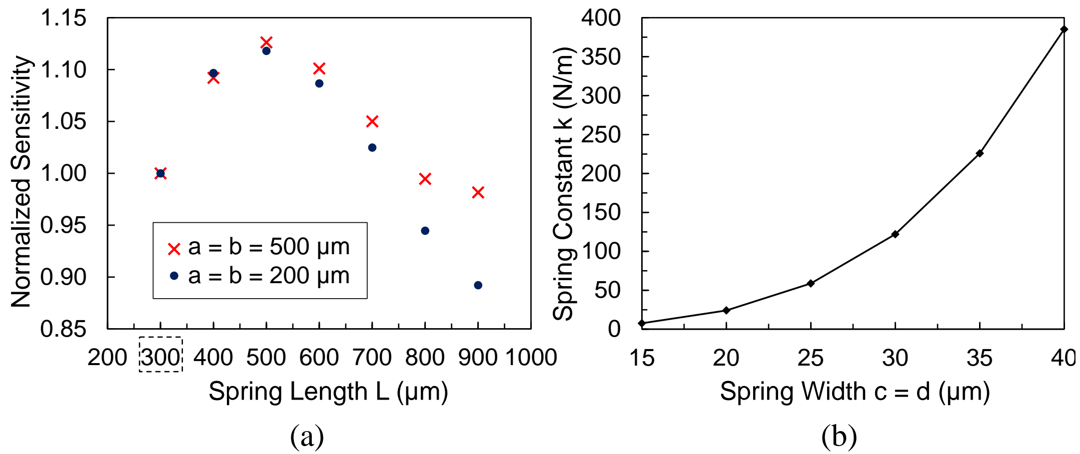
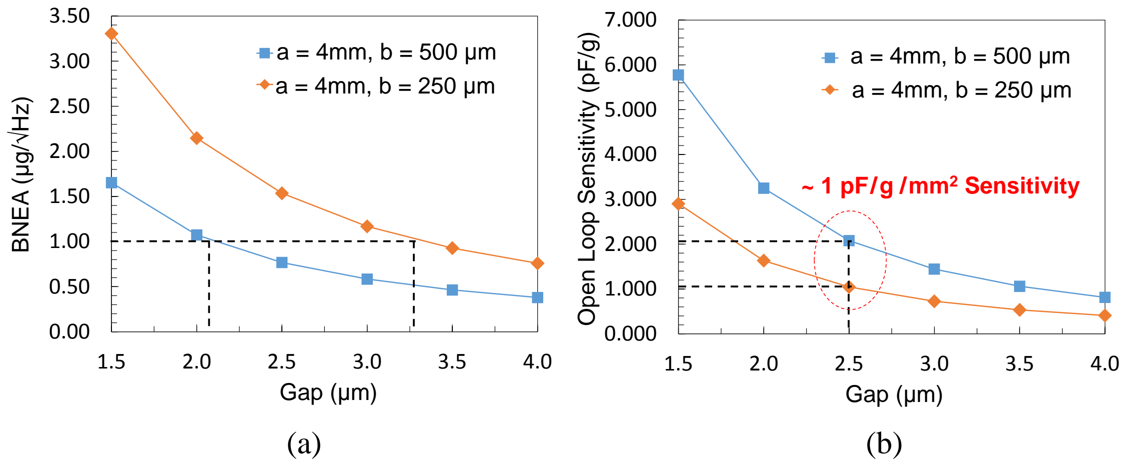


Fig. 6.5. (a) Optimize spring length: L ≈ 500-600 μm gives the maximum sensitivity for two different proof-mass sizes; The sensitivity is normalized to L = 300 μm; (b) Setting L = 600 μm and reducing the spring width (c and d) to < 25 μm lower the spring constant to < 50 N/m.

The different spring lengths L can be easily achieved by utilizing DRIE lag. Setting L ≈ 500-600 μm (Figure 6.5(a)) places the anchor point of the spring midway along the height of the proof-mass, thus increasing displacement near the top where the changes in the narrow gap g_{top} contribute the most to total ΔC and increasing sensitivity.

We optimized various design parameters, targeting high capacitive sensitivity (S) and sub-μg/√Hz BNEA for a sensor footprint at 1 mm^2 and 2 mm^2 as shown in Figure 6.6.



(a) (b)

- H = 1 mm, a is the electrode width, b is the mass width along sense axis;
- Sense area A = a × h_{top}, h_{top} = 250 μm;
- Single spring: c = 20 μm, d = 30 μm, L = 600 μm;

Fig. 6.6. COMSOL simulation to optimize the capacitive gap size for minimizing BNEA and maximizing capacitive sensitivity (S) for a sensor footprint of 1 mm^2 and 2 mm^2.

The 1 mm^2 footprint sensor is designed to have a proof-mass area of 4 mm × 250 μm while the 2 mm^2 footprint sensor has a proof-mass area of 4 mm × 500 μm. With the spring dimensions listed in Figure 6.5, The 1 mm^2 footprint accelerometer has resonant frequency at 627 Hz and the 2 mm^2 footprint sensor has resonant frequency at 443 Hz.

In both devices, 4 mm is the sense capacitor width. Figure 6.5 presents the calculated BNEA based on squeeze film air damping and COMSOL simulated sensitivity (S) for these two designs. A gap opening less than 2 μm will defeat the purpose to achieve BNEA of < 1 μg/√Hz. 2-3 μm is favorable for the 2-mm^2 sensor and 3.3-4 μm is desired for the 1 mm^2 sensor to achieve sub-μg noise performance. In the meantime, a 2.5 μm gap allows both sensors to achieve high capacitive sensitivity of greater than 1 pF/g per 1 mm^2 footprint.

As shown in Figure 6.7 and Table 6.2, we design and layout an array of 1mm thick high sensitivity and low noise capacitive hair accelerometers with various design parameters. The top small gaps are 2 to 2.5 µm and extend 250 µm. We cover a wide range of proof-mass sizes to target different sensitivity levels and full-scale ranges. Within the same chip, the spring dimensions are fixed. The higher sensitivity devices can achieve micro-g resolution.

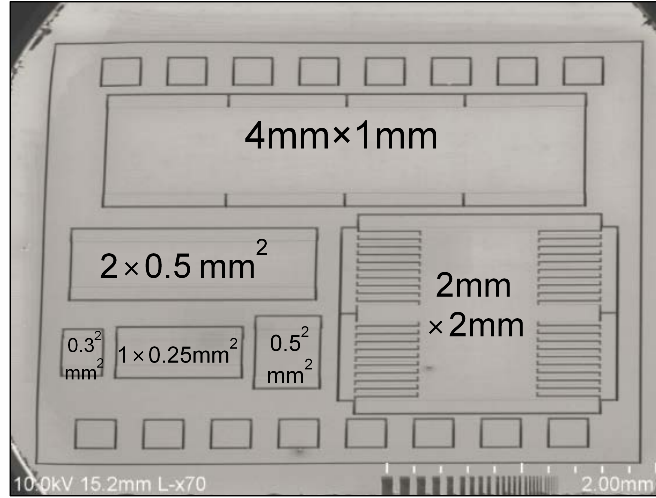


Fig. 6.7. SEM of a sensor chip consisting of an array of 1mm thick high sensitivity and low noise capacitive hair accelerometers with various design parameters.

Table 6.2: high sensitivity and low noise capacitive hair accelerometer design specifications of an array of devices with various design parameters

Device Footprint		k	Simulated and Calculated Specifications					G-Range @ 1/3 g_0		g-range @ ΔC=1pF
a	b	k	C_0 (pF)	$\Delta C/g$ (fF/g)	f_{res} (kHz)	Displacement Sensitivity	BNEA (µg/√Hz)	Accel. @ 1/3 g_0	ΔC @ 1/3 g_0	
4 mm	1 mm	$2k_0$	4.080	156	1.256	0.157 µm/g	0.384	5.3 g	826.8 fF	6.4 g
2 mm	500 µm	$2k_0$	2.187	19.2	2.512	0.0393 µm/g	1.086	21.2 g	195.0 fF	52.1 g
500 µm	500 µm	k_0	0.510	2.40	3.553	0.0196 µm/g	2.172	42.5 g	102.2 fF	416. g
300 µm	300 µm	k_0	0.305	0.52	5.921	7.079 nm/g	4.674	117.7 g	61.2 fF	1923 g

- H = 1mm
- Gap: 2.5 µm / 250 µm
- Spring: c ≈ 35 µm, d ≈ 45 µm, L = 600 µm

For example, a $4 \times 1\,\text{mm}^2$ footprint device has about $400\,\text{ng}/\sqrt{\text{Hz}}$ noise floor and has capacitive sensitivity at >100 fF/g. Another $2 \times 0.5\,\text{mm}^2$ footprint device has almost 20 fF/g sensitivity while providing a larger g-range considering the same maximum change in capacitance that can be handled by the readout circuit. Resonant frequencies of these structures are all above 1 kHz and the usable BW should be at least 500 Hz.

6.2 Fabrication Results

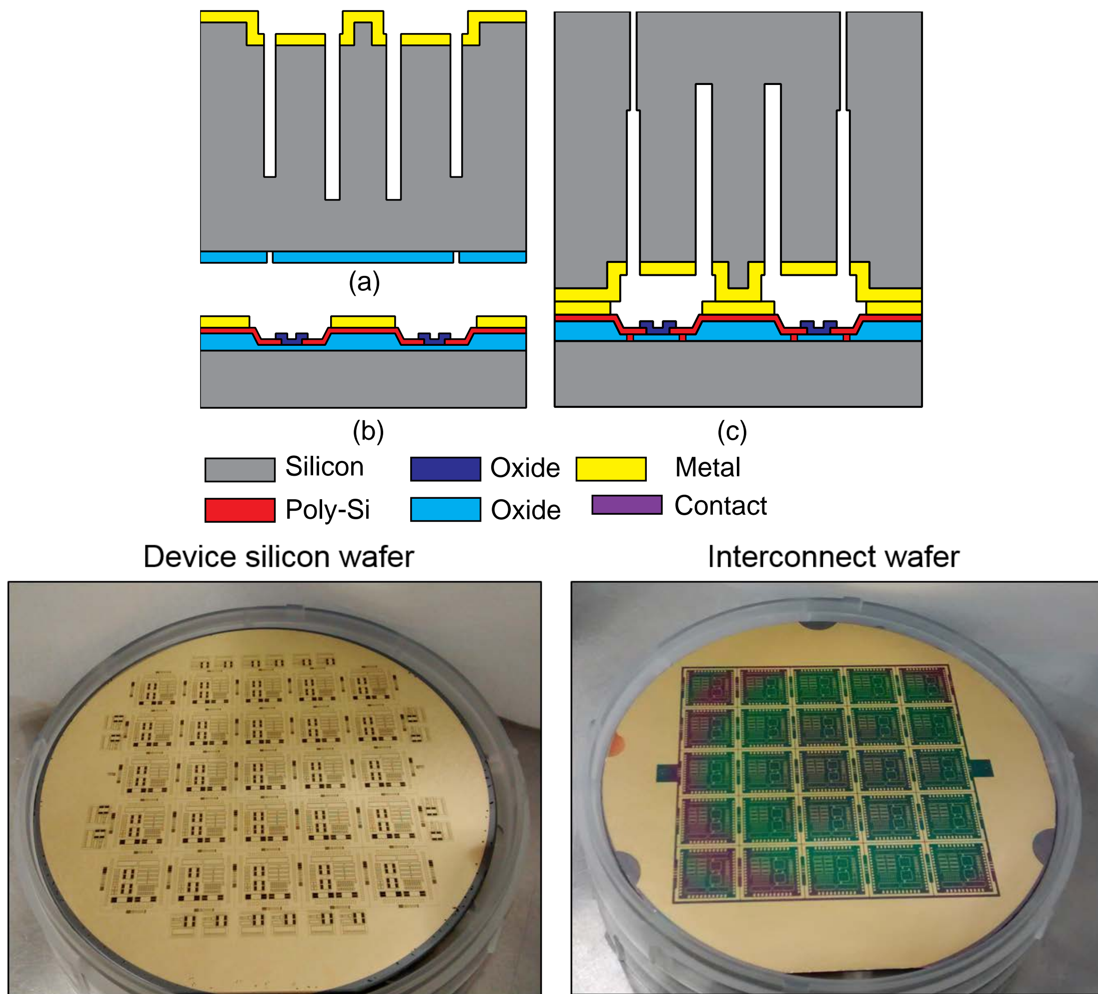


Fig. 6.8. CMOS-Compatible two-gap fabrication process: (a) MEMS devices wafer patterned with the spring, mass, narrow and wide gaps; (b) Interconnect wafer patterned with electrical connections and eutectic bonding metals; (c) Released bonded wafer.

This 3D vertical hair-like accelerometer with HAR transduction gap is fabricated by a well-characterized CMOS compatible two-gap microfabrication process introduced in Chapter 5. Sensor chip fabrication starts with HAR DRIE etching from one side of a 1 mm thick silicon wafer to define the proof-mass, vertical hair spring, and electrodes, is followed by bonding this wafer to an interconnect/circuit wafer, and is completed with a second HAR DRIE release step to define the 2-μm sensing gap g_{top} from the other side (Figure 6.8).

6.2.1 Ultra-Deep DRIE

This two-gap structure approach removes any limits due to DRIE on the maximum device height and minimum sensing gap that other fabrication approaches impose, and allows all the critical structural dimensions to be independently varied. The device height (H) can be greatly increased by allowing a reasonably wider g_{bot}. An ultra-high aspect-ratio (UHAR) DRIE process was developed for achieving > 100:1 aspect-ratio for gap sizes down to 2 μm for etching g_{bot} [6].

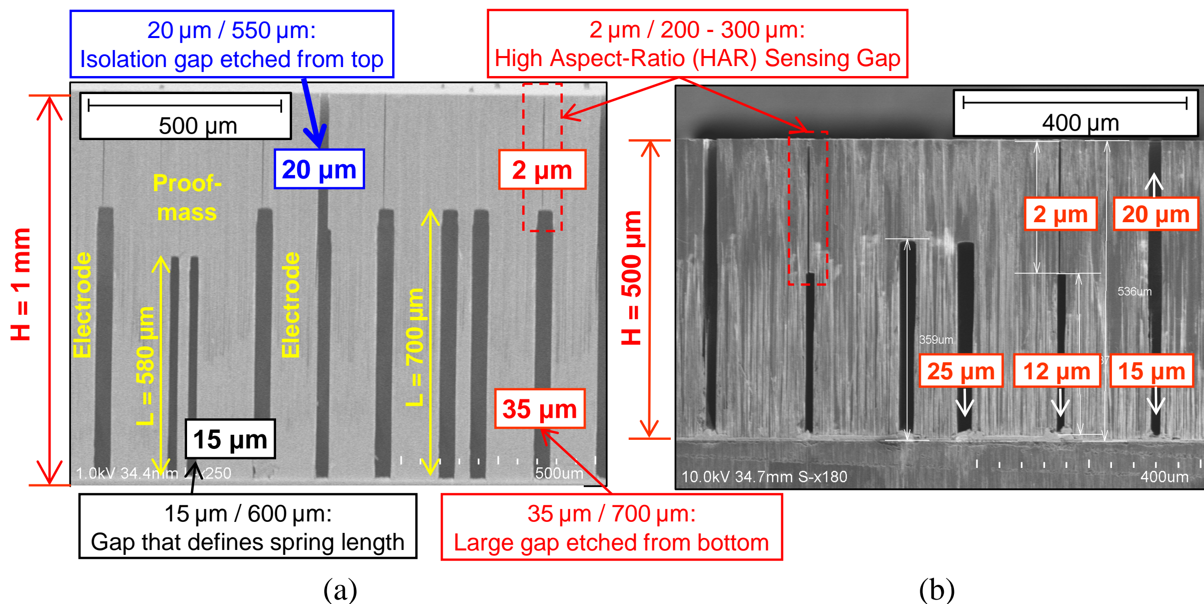


Fig. 6.9. SEM cross-section of fabricated 3D vertical hair-like accelerometers by the two-gap process: (a) Two 1-mm tall devices side-by-side. The left device has L = 580 μm and the right one has L = 700 μm; (b) Cross-section of a 500-μm tall device.

We implement the two-gap process and structure both with 500 μm and 1 mm thick silicon wafers. Figure 6.9(a) shows the cross-sectional SEMs of two fabricated 1mm tall accelerometers with different vertical spring lengths, measuring 580 μm and 700 μm respectively. Figure 6.9(b) represents 500 μm tall accelerometers cross-section. Both devices have top gaps that are 2 μm wide, extending > 250 μm in height.

In this generation of hair accelerometers, to reduce the cross-axis sensitivity, two springs are placed parallel to the electrode plate ($k = 2k_0$). The spring anchor dimensions are also designed to be at least 35 μm × 45 μm to ensure reliable silicon-gold eutectic bonding of the vertical hair springs to the substrate with electrical connections.

Various devices were designed. The proof-mass sizes range from 300^2 μm^2 to 4×1 mm^2, and the spring cross-sections range from 30^2 μm^2 to 50^2 μm^2, thus covering a broad range of performance specifications. Shaker table testing on the fabricated accelerometers will be presented in the next section.

Figure 6.10 compares the optical and SEM images of a fully released accelerometer (4 mm^2 footprint, 9.32 milligram), with < 2.5 μm average g_{top} (h_{top} = 233 μm), > 30 μm g_{bot} (h_{bot} = 762 μm) and sense/feedback electrodes. The aspect-ratio of the critical transduction gap g_{top} is almost 100:1. The proof-mass is intentionally detached to show the two-part gap along the proof-mass sidewall formed by two DRIE steps.

The HAR transduction gap, g_{bot} is measured along h_{top}. (Figure 6.11). g_{bot} is initially 2 μm defined on the mask layout: after the release DRIE the gap near the top increases to 2.69 μm due to release DRIE undercut, the gap in the midway measures 2.36 μm and the gap at the junction of g_{top} and g_{bot} is slightly less than 2 μm.

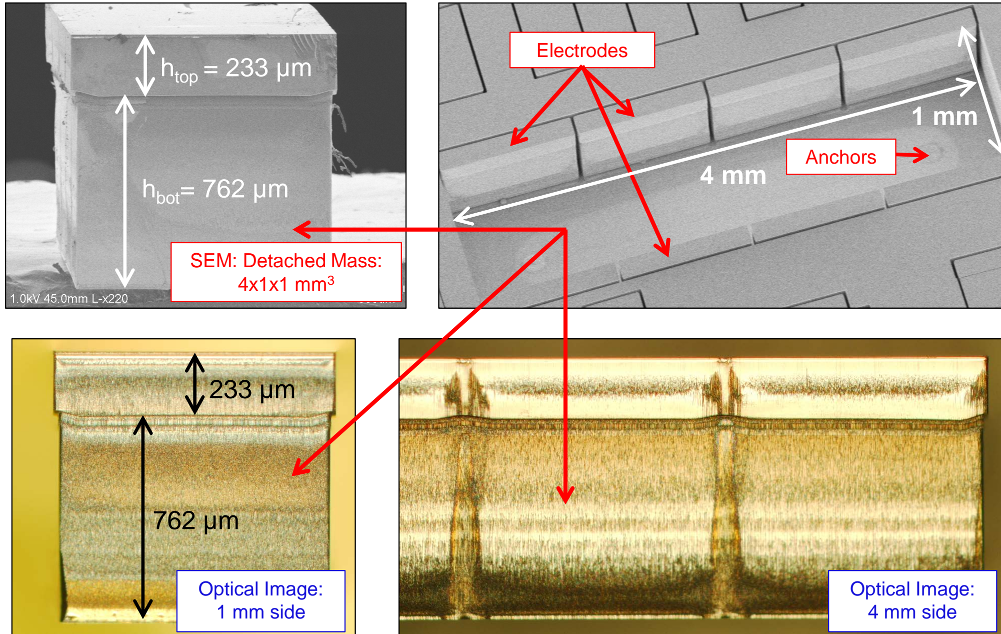


Fig. 6.10. Fully released accelerometer (4×1×1 mm^3 proof-mass): optical and SEM images of detached proof-mass sidewalls formed by DRIE. The device is fully released when gtop is etched through and joined with gbot. The two-part gaps along the height are htop = 233 µm DRIE-ed from the top and hbot = 762 µm DRIE-ed from the other side.

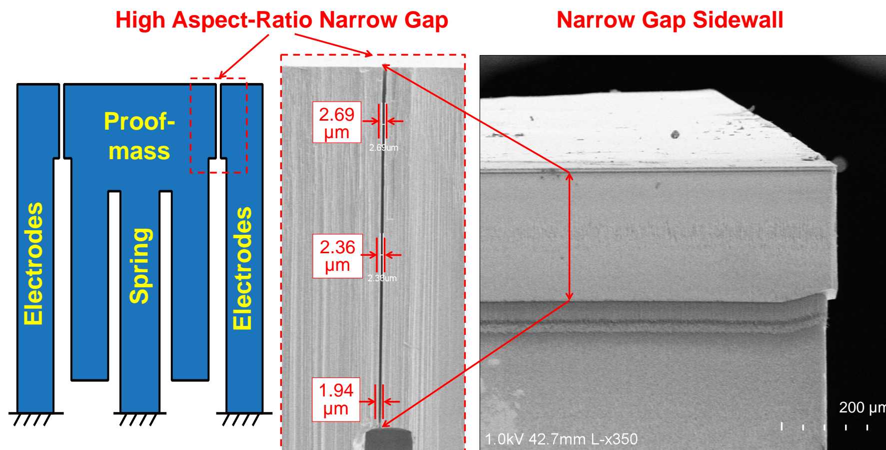


Fig. 6.11. HAR transduction gap profile with gap dimension measured along htop for 2 µm initial capacitive transduction gap defined on the mask.

6.2.2 Silicon-Gold Eutectic Bonding

Due to the large number of devices to be integrated. our proposed hair accelerometer array sensing system is not viable without vertical stacking of multiple wafers to form complex heterogeneous microsystems where functions are distributed over the different wafers in the

stack. Mechanical functions are realized in one or multiple wafers/layers in the stack while at least one of the wafers is dedicated to the readout circuits.

There are two main disadvantages with silicon-on-glass (SOG) process used in fabricating the uniform-gap capacitive hair accelerometer: 1) It is not compatible with processes where one of the constituent wafer to be integrated is CMOS IC chip or wafer because the high voltage apply during anodic bonding may destroy the underlying circuit; and 2) It does not provide electrical connections: although glass can be anodically-bonded to any conductor including metal, the oxidized bond interface is not electrically conductive. Patterning metal contact fingers between silicon and glass limit the minimum achievable bonding area thus result in a minimum hair spring diameter.

Thus silicon-gold eutectic bonding is implemented in the fabrication of high-sensitivity capacitive hair accelerometer array chips, to both mechanically anchor and electrically conduct the vertical high-doped springs as well the electrodes [6, 7]. It is also chosen for its relatively high bonding strength and low processing temperature at 350 - 400 °C. Li et al. [8] reported bonding strength of 66.8 MPa when bonding temperature has been raised to 400 °C.

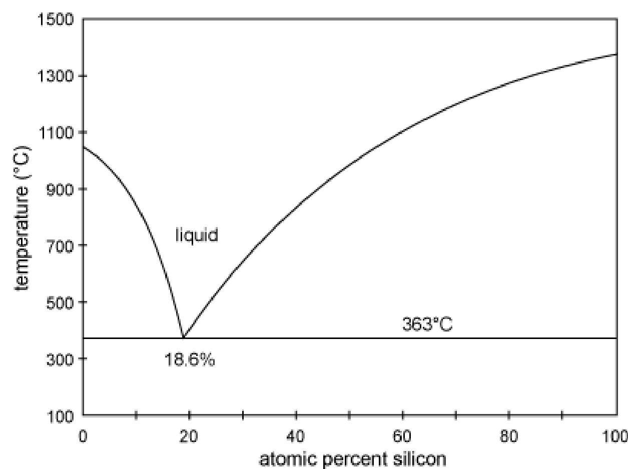


Fig. 6.12. Silicon-gold phase diagram.

The gold-silicon binary system reveals the most dramatic reduction of the melting

temperature: 19 at. % (3 wt %) silicon is dissolved in the eutectic silicon-gold compound at 363 °C compared to the 1063 °C melting temperature of pure gold or to the 1412 °C melting temperature of silicon as shown in Figure 6.12. For example, silicon substrate and thin-film gold in direct contact act as a solder. The thickness ratio of gold and silicon layers is 3.9 to 1 calculated from the atomic ratio. Bonding is typically carried out at a temperature slightly above the eutectic temperature of 363 °C. Before the saturation composition is reached silicon keeps being dissolved. After a set time, the wafers are slowly cooled and reliable bonds are obtained.

$$\frac{t_{Au}}{t_{Si}} = \frac{m_{Au}/\rho_{Au}}{m_{Si}/\rho_{Si}} = \frac{3.9}{1} \quad (6.7)$$

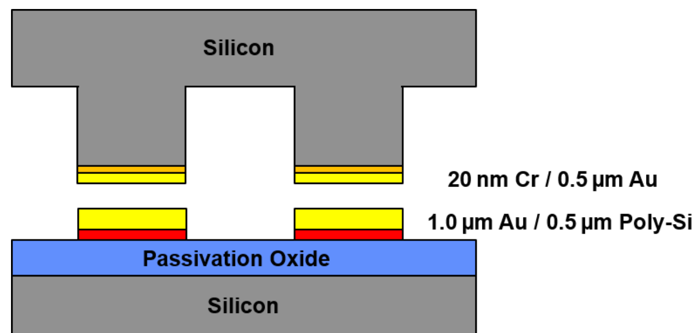


Fig. 6.13. Patterned eutectic bonding stack in the fabrication of capacitive hair accelerometer.

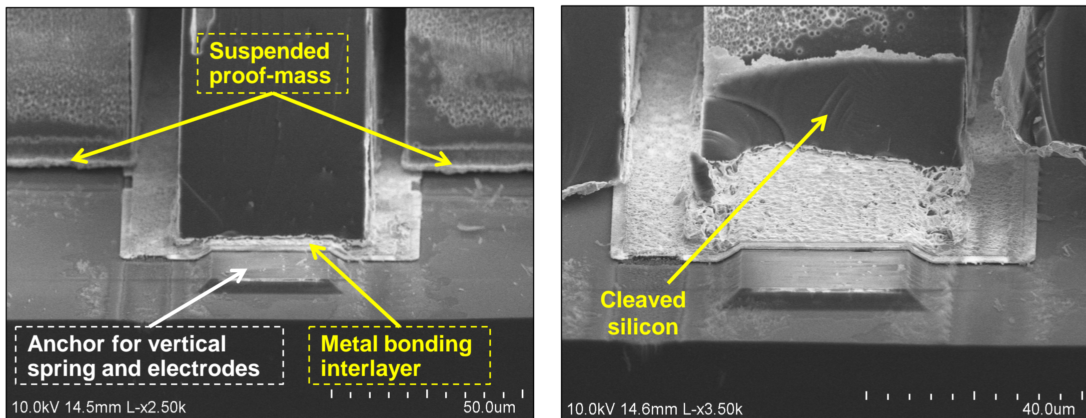


Fig. 6.14. Silicon gold eutectic bonding sites showing recess in the bottom silicon substrate and the suspended structure from device wafer.

Figure 6.13 illustrates the eutectic bonding stack used in the fabrication of our two-gap

capacitive hair accelerometer arrays: poly-silicon is patterned over the passivation oxide on the bottom silicon substrate followed by at least 1 µm Au thin film deposition. The poly-silicon layer supplies the silicon atom that can diffuse into the thick Au layer. The bonding sites (spring and electrode anchors) on the bottom surface of the top silicon substrate is covered with Cr as adhesion layer as well as diffusion barrier and 0.5 µm Au to prevent the silicon spring being oxidized. The total Au stack thickness of 1.5 µm needs 0.38 µm silicon to form eutectic composition. Since Au has both high ductility and malleability, thicker Au layer helps with forming good atomic contact at the bonding sites of the two wafers when high bond contact force is applied to compensate for wafer warping from previous processing steps.

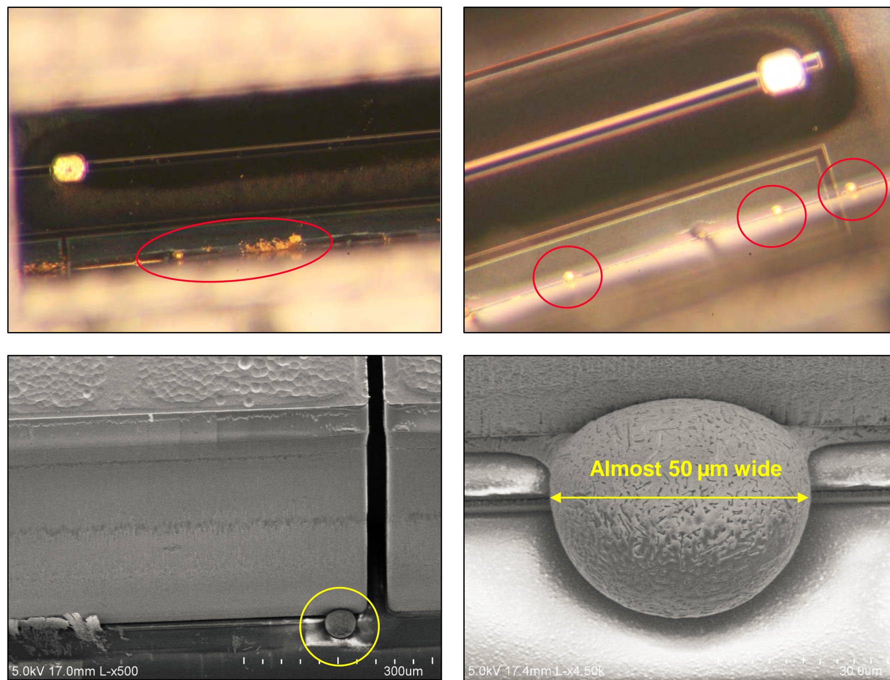


Fig. 6.15. Au-Si alloy squeezed out during bonding due to high contact force to ensure atomic contact of the two wafers: they can be seen on almost all the devices since the electrodes have larger bonding area (more Au-Si alloy formed).

The bonding results and interfaces were observed and analyzed with optical microscope, scanning electron microscope (SEM), and a related energy dispersive spectrometer (EDS).

A minimum force must be applied to ensure good atomic contact of the two wafers because unlike anodic bonding, there's no large electrostatic force pulling the wafers into good contact. However, a thick gold stack along with the larger contact force result in eutectic stack being squeezed out under large compressive force. There will also be nonuniformity in the final alloy thickness across the wafer.

Due to warping of both the silicon wafers being bonded, we apply a high contact force to flatten the wafers and to ensure local bonding pressure is at least 1 MPa based on the percentage bonding area out of the 4-inch diameter. However, the high contact force causes Si-Au alloy in its liquid transition phase being squeezed from the edges of the bonding pads and results in reduced thickness of the bonding interlayer as shown in Figure 6.15. They can be seen on almost all the devices since the electrodes have larger bonding area (more Au-Si alloy is formed). Although squeeze-out from the edge of the bonded wafer pair is a good indication of good atomic contact, these alloy balls may short neighboring electrodes, or short the electrodes and proof-mass. The alloy balls measures 30-50 μm in diameter.

To effectively minimize the effect of the eutectic alloy squeeze-out, the large DRIE-ed gap g_{bot} separating the proof-mass and electrode is designed to be greater than 35 μm. In addition, recessing both the bottom surface of the top substrate by > 5 μm, and the top surface of the bottom silicon substrate passivation oxide layer by > 3 μm creates more space along the vertical axis.

We analyze the bond interface after the silicon spring with the proof-mass is broken-off from the lower silicon substrate. Figure 6.16 (a) and 6.17 (a) show bond sites where the springs broke off at the silicon spring. Figure 6.16 (b) and 6.17 (b) show locations where the they broke off at the gold layer, and surface texture due to the formation of fine silicon microstructures on top of the gold surface can be observed, indicating that 100% bonded area was not achieved.

The fine microstructure formation is due to heating of the wafer beyond the eutectic temperature. This effect is already known from die bonding and studied by WoHenbuttel et al. [7]. They experiment with p-type (100) Si wafers thermally oxidized and deposited with 300 Å Ti and 1200 Å Au, and concluded that the microstructure formation. is almost time and temperature independent: the effect occurs after 60 s at 400 °C, 100 s at 390 °C, 5 min at 370 °C and 10 min at 365 °C. The mixing of Si into Au is due to solid-state diffusion. Clusters of silicon are formed rather than taking place uniformly until the eutectic composition is reached (19 at. % Si). Shiny eutectic alloy can be seen in Figure 6.13 and 6.17(c). Different bonding results across the wafer may be caused by temperature and bonding force nonuniformity.

The bonding quality may also be degraded by the formation of silicon oxide over the gold layers on silicon substrate [9]. This oxide layer could inhibit the Silicon-Gold eutectic alloy from the two wafers to join and form reliable bonds. They observed that a 1000 Å silicon-oxide could readily be grown on top of a gold layer on a silicon substrate by heat treatment at a far lower temperature (~250 °C) in air or oxidation atmosphere when silicon atoms already migrate through the gold film to reach the top of the thin gold film. In our bonding process, since the bonder process chamber is not purged with forming gas to ensure the removal of this potential oxide layer, bonding quality may be degraded. The authors also pointed out the importance of the Si-metal interface in the formation of oxide by slightly oxidizing the silicon wafer in hot nitric acid before vacuum evaporation of an Au film, oxide formation on top of the Au was not detected following anneal in oxidizing atmospheres at temperatures as high as 300°C for up to 1 hour. We cannot adopt this method since we do not want to inhibit the diffusion of Silicon.

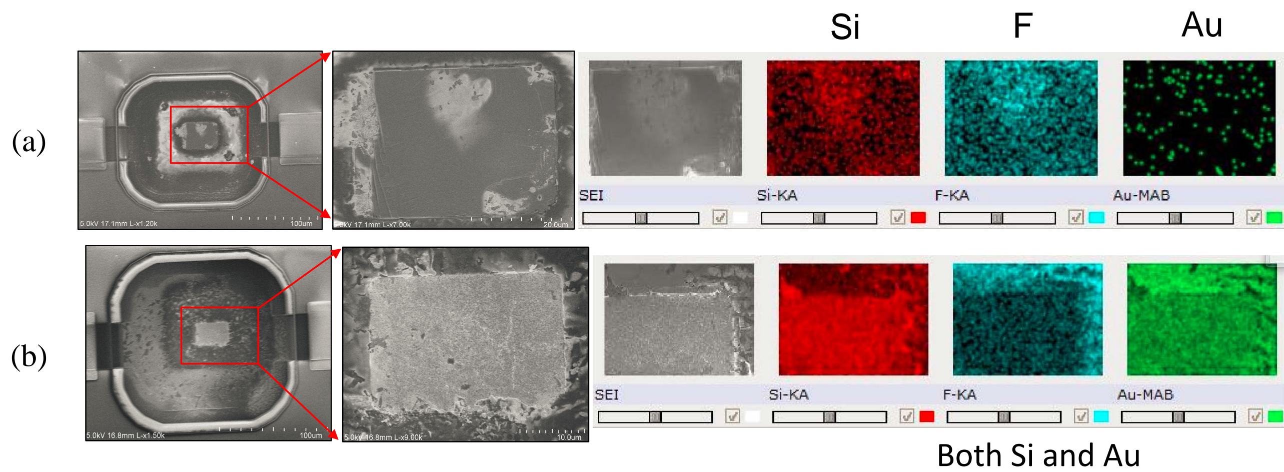


Fig. 6.16. EDX analysis of silicon-gold eutectic bonding interface.

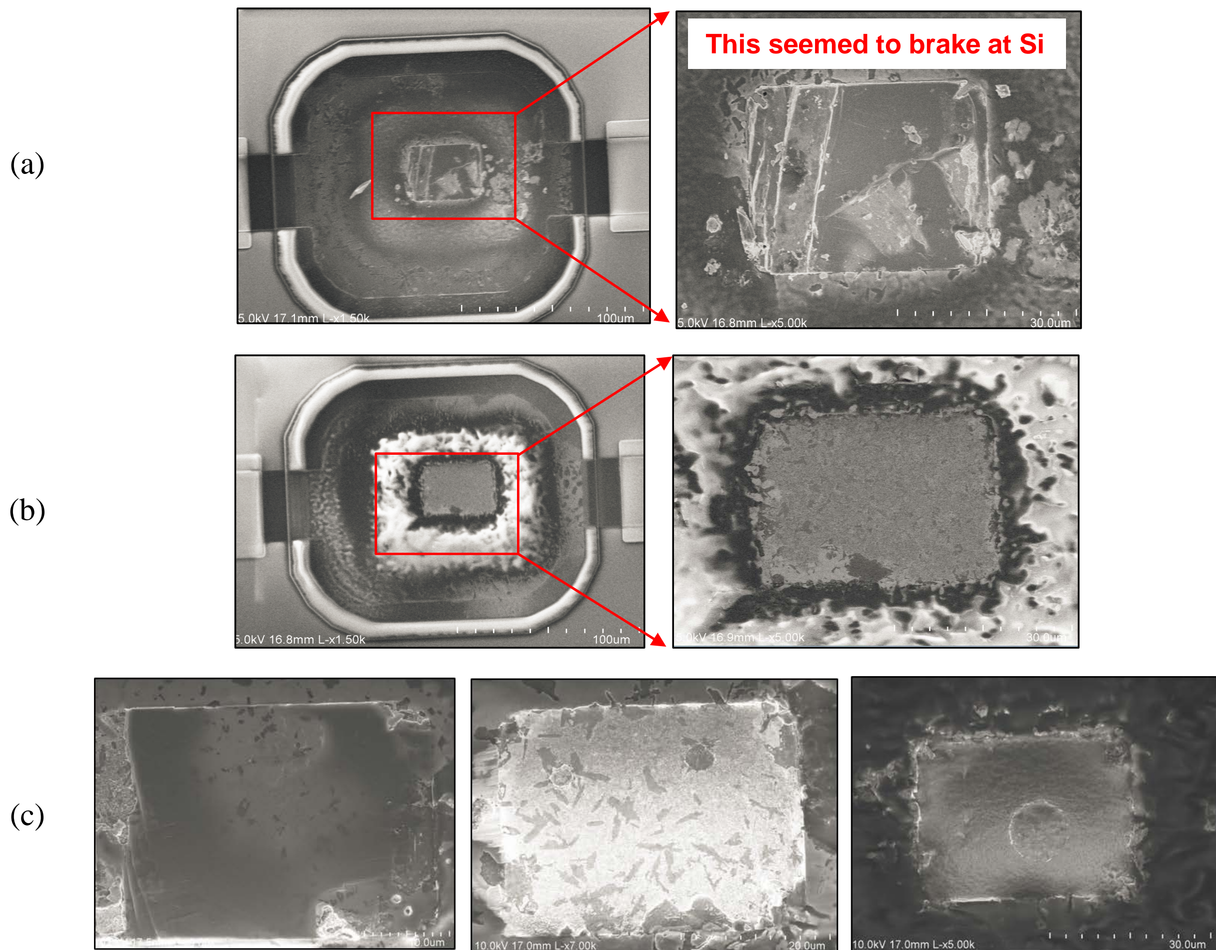
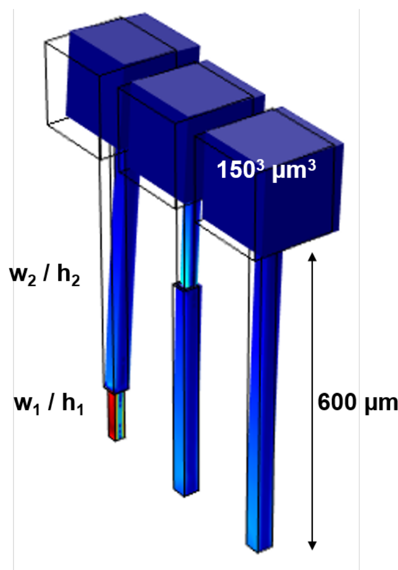


Fig. 6.17. (a) Silicon peeled off from the hair spring indicates that the bonding strength is higher than the silicon fracture strength; (b) The hair spring broke off at the alloyed interlayer. (c) Other bonding locations.

6.2.3 Thinning Hair Spring by Isotropic RIE

The other major challenge lies with achieving minimum hair spring width (bond area) while maintaining reliable bonding quality. However, whatever bonding method is adopted it requires a minimum bonding area: Chapter 4 shows silicon-glass anodic bonding with metal fingers only yield if the bond area is greater than 30 µm wide, and this Chapter shows silicon-gold eutectic bonding is reliable for similar bond area.



w_1 / h_1	30 µm/600 µm	20 µm/600 µm	20 µm/100 µm	20 µm/200 µm	30 µm/400 µm
w_2 / h_2	30 µm/600 µm	20 µm/600 µm	30 µm/500 µm	30µm/400 µm	20µm/200 µm
Displ. @ 1g Accel.	0.83 nm	4.1 nm	2.1 nm	3 nm	1.1 nm

Fig. 6.18. Hair spring composed of different width sections are simulated to study the effectiveness of narrowing the spring: narrowing the spring width from 30 µm to 20 µm for a length of 200 µm out of the entire 600 µm spring length from the anchor point increases the displacement sensitivity by more than three times (> 3x).

One technique to achieve a more compliant spring is to narrow the spring originally defined by DRIE while preserving a minimum required bonding area. COMSOL simulation is used to study the effect of different widths along a 600 µm long hair spring supporting a

600^3 μm^3 proof-mass. Ideally a uniform thin spring is desired: a 20 μm diameter spring results in five times displacement sensitivity compared to a 30 μm spring (Figure 6.18).

Isotropic SF_6 dry plasma etch can be used to thin the springs after the deep DRIE. As shown in Figure 6.19, conformal oxide deposition produces thick oxide both on the top and on the sidewall of the step at the spring anchors, thus protecting the anchor from being etched in isotropic SF_6 plasma. The sidewalls of the trenches surrounding the vertical springs should be thoroughly cleaned by oxygen plasma to remove any polymer on the sidewall that will present subsequent SF_6 etch. Ideally, the sidewalls of should also cleaned by HF to be free of native oxide but it is difficult when the masking oxide hard mask is to be preserved. Inefficient sidewall polymer and oxide removal may stop the spring thinning etch.

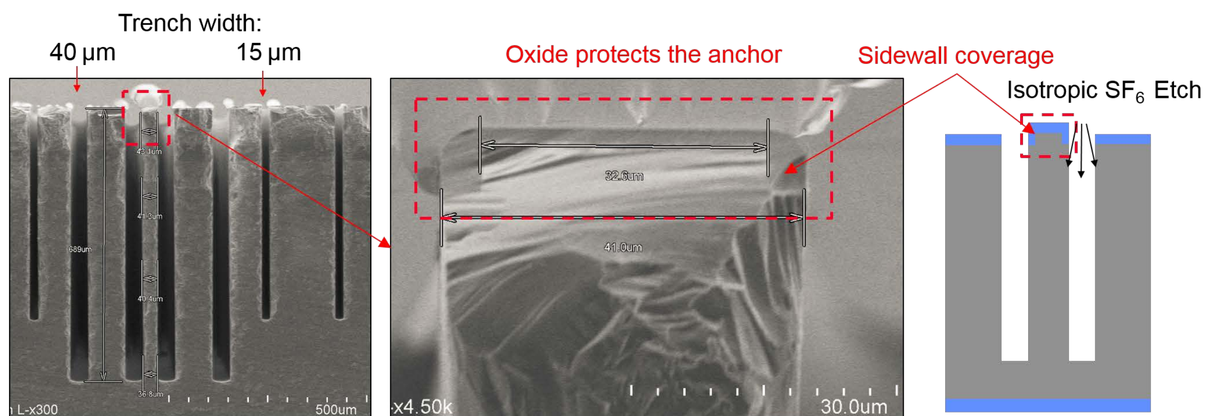


Fig. 6.19. Spring width after 130 min DRIE on 1 mm thick silicon wafer: oxide patterned around the spring anchor protect it from being etched during isotropic SF_6 etch.

In addition, there's also a limit on how far the reactive species can migrate into the narrow trenches surrounding the spring (20 μm), even with reduced chamber pressure (10 mTorr) and increased platen power (30 W). We increase the platen power to increase both the density and the energy of the free electrons. The DC voltage becomes more negative with increasing power thus driving the reactant normal to the wafer surface and into the etched HAR trenches.

With all these measures, there is still limit on how deep into the trenches we can narrow

the spring, so springs composed of different width sections are simulated in COMSOL as shown in Figure 6.18. Narrowing the spring width from 30 µm to 20 µm for a length of 200 µm out of the entire 600 µm spring length from the anchor point increases the displacement sensitivity by more than three times (> 3x).

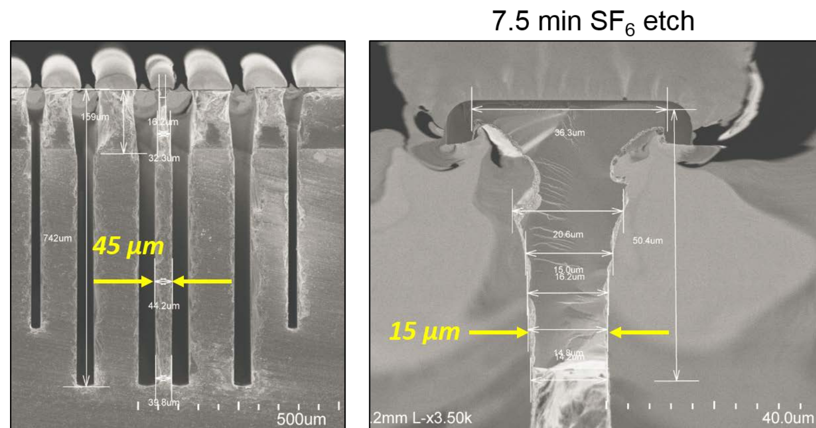


Fig. 6.20. Spring profile after 7.5 min isotropic SF_6 etch experimented on 1 mm thick silicon wafer (trenches are DRIE-ed for 130 min).

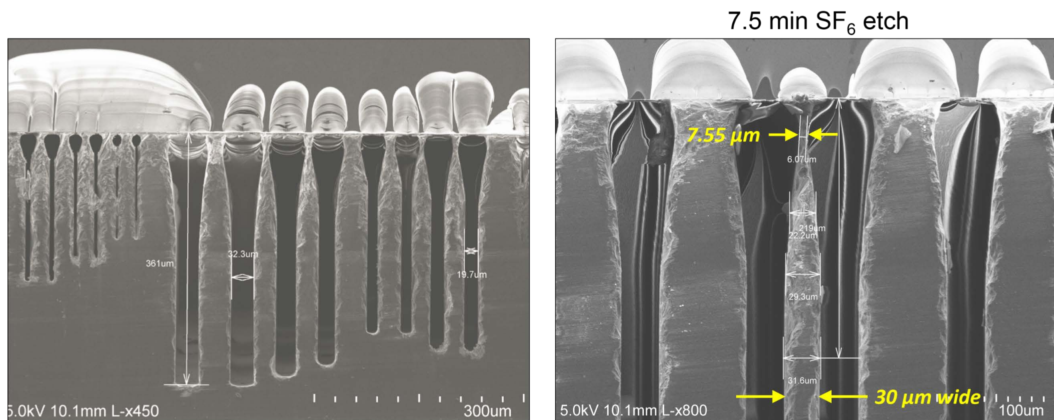


Fig. 6.21. Spring profile after 7.5 min isotropic SF_6 etch: experimented on 500 µm thick wafer (trenches are DRIE-ed for 70 min). Different openings result in different etch depth.

Figure 6.20 shows the spring profile after 7.5 min isotropic SF_6 etch on a 1 mm thick silicon characterization wafer patterned with different trench widths and DRIE-ed for 130 min (Figure 6.18) for. For a 40 µm wide spring surrounded by 40 µm wide trenches, SF_6 etch reaches a depth about 150 µm from the top. The silicon at the anchor is intact. However, in this example,

undercut makes the anchor very thin. The narrowest continuous portion of the spring is ~ 15 μm. Another 30 μm wide spring originally defined by DRIE has the narrowest continuous portion at 8 μm (Figure 6.21).

Different trench openings result in different SF_6 etch depth and lateral etch rate. Applying the trench etch results to hair spring fabrication, the lateral etch rate may be higher and more lateral etch will occur since all four faces of the spring are defined by the DRIE gaps thus the plasma angle increases.

6.3 Interdigitated-Electrode Device by Two-Gap Process

Interdigitated electrodes are employed extensively in planar devices to increase the sensing and actuation area [1-3]. The electrodes typically have the same thickness as the proof-mass formed simultaneously with the proof-mass in a single DRIE step (or DRIE followed by sacrificial layer refill).

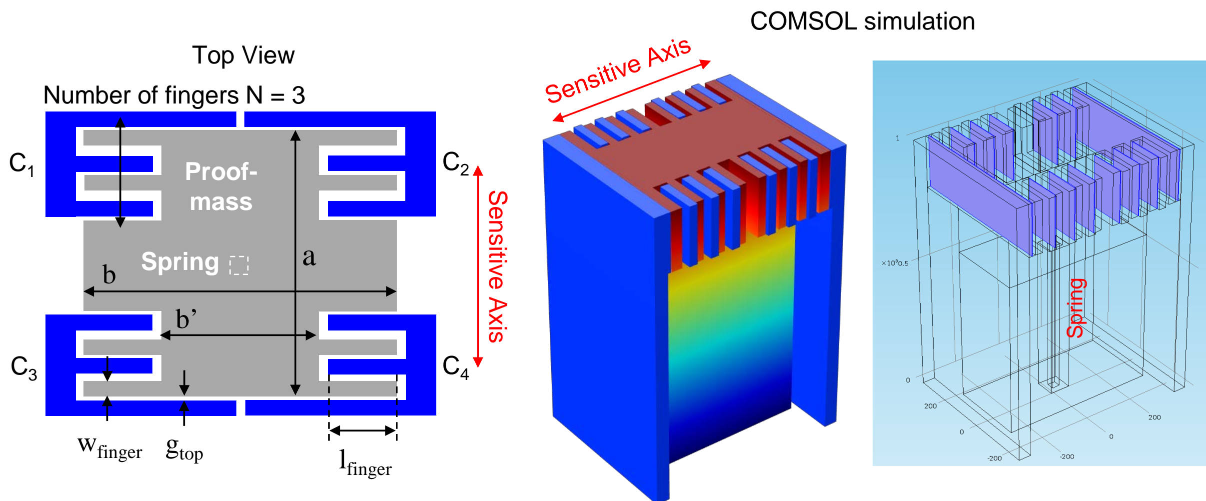


Fig. 6.22. Increasing the capacitive sensitivity per unit footprint by optimization of the gap dimension g_{top}, and interdigitated electrode width w_{finger} and length l_{finger}.

To further increase the capacitance change per unit footprint of the capacitive hair accelerometer, interdigitated parallel-plate type electrodes can be formed instead of one capacitor

on each side of the proof-mass along the sensitive axis. With optimization of the gap dimension and interdigitated electrode width and length with respect to the solid portion of the proof-mass, the capacitive sensitivity per unit footprint may be further increased from a solid proof-mass design. It is also easier to implement fully differential operation without reference capacitor.

As shown in Figure 6.22, effective capacitor plate area can be increased for the same device footprint by implementing the interdigitated electrodes. Since the interdigitated electrodes are formed by the top gap g_{top} and the bottom gap g_{bot} is much wider than g_{top}, adding the interdigitated fingers will reduce the effective proof-mass width from b to $b' = b - 2 \times l_{finger}$. The key is to increase the density of interdigitated fingers to increase the total ΔC per unit footprint. However, the electrodes density is limited by DRIE capabilities: etching closely-spaced long and narrow trenches (2 μm) introduces micro-loading and etch rate nonuniformity along the long trenches and at the junctions of various openings that define the contours of the proof-mass and different electrodes. Due to DRIE undercut, the interdigitated fingers should have a minimum width w_{finger} and maximum length l_{finger} to avoid flexing. These criteria determine the electrodes density N. Through analytical analysis and COMSOL simulation, we found that maximum ΔC_{total} for a given footprint $(a \times b)$ can be achieved with $b > a$, and with finger length $l_{finger} = 1/4\ a$. Compared to a solid proof-mass with a single electrode, ΔC_{total} is scaled by approximately $(1 + N/4)$.

As shown in Figure 6.23, we set $l_{finger} = a/4$, $w_{finger} = 15$ μm (denser fingers that results to 10 fingers within 500 μm) or 30μm (less dense electrodes that results to 10 fingers within 1 mm), $g_{top} = 2$ μm, and $g_{top_isolation} = 20$ μm for the interdigitated electrode designs. However, within the same footprint, sensitivity is traded-off with noise performance since the squeeze film damping effect increases with larger sensing area and reduced effective proof-mass ($BNEA \propto \sqrt{Area/Mass^2}$).

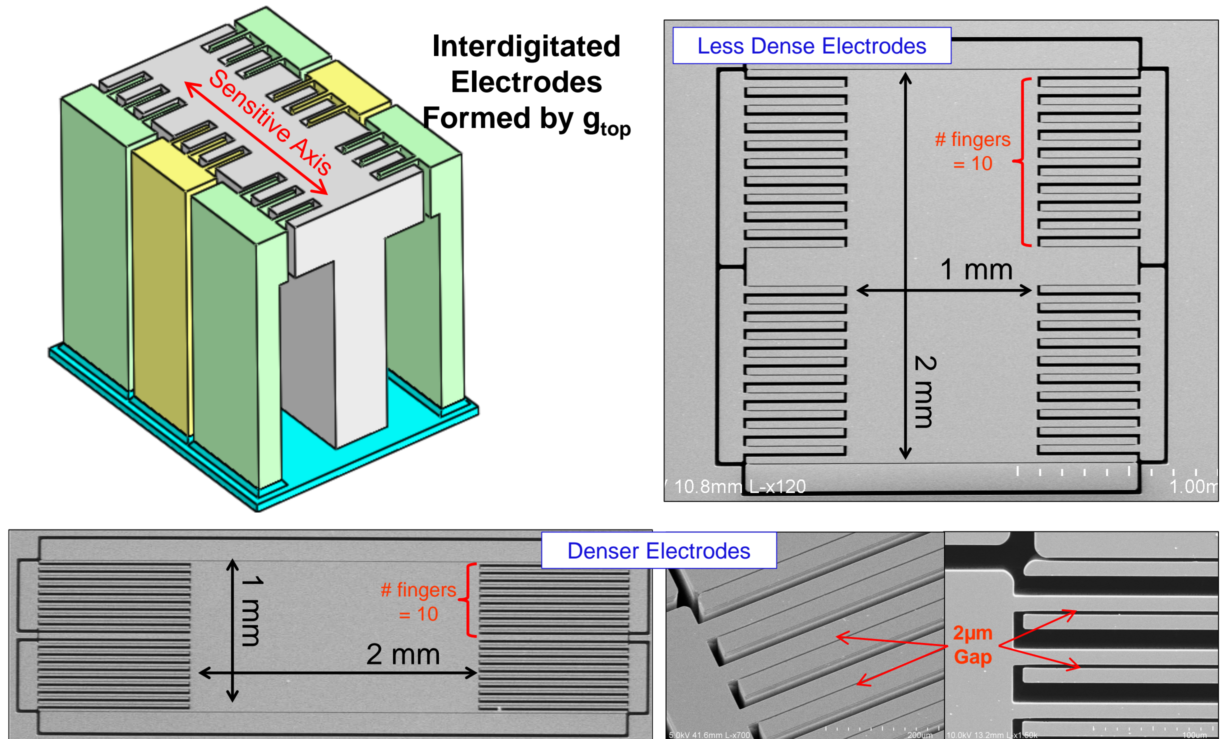


Fig. 6.23. Hair accelerometer with interdigitated electrodes form by the top gap: schematic and two devices with different electrodes density.

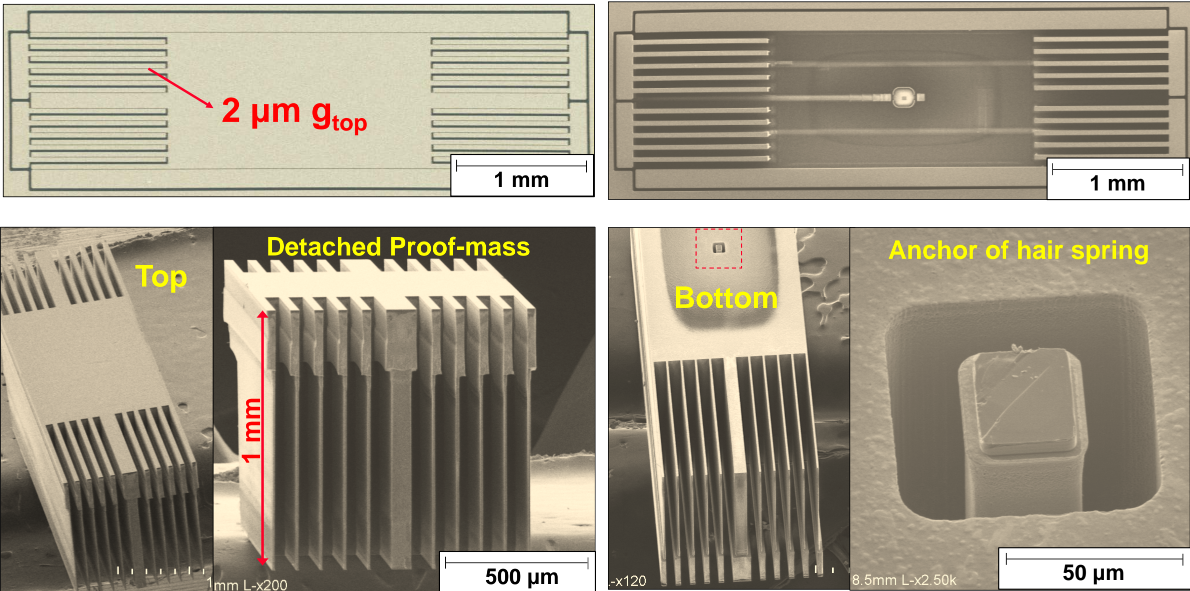


Fig. 6.24. Interdigitated devices successfully released.

The solid proof-mass device in Figure 6.10 (4x1 mm^2 footprint) is modified to include the interdigitated electrodes. There are 10 interdigitated electrodes for each orthogonal axis and the

proof-mass is > 50 % of that a solid mass design and the capacitive sensitivity is increased by 2x. If the finger density is increased such that 20 electrodes are placed in each orthogonal axis, the capacitive sensitivity is increased by 3x (Figure 6.22 Denser Electrodes).

6.4 Capacitive Hair Accelerometer Testing Results

6.4.1 Electromechanical Testing

The fabricated chips are mounted on a printed circuit board (PCB) with an Analog Device 7746 Capacitance to Digital Convertor (CDC) chip. We tested the accelerometers on Unholtz-Dickie 400ATE/C Transducer Calibration System. This shaker table outputs acceleration as low as 0.1 g over a wide frequency range. We tested both the 500 μm-thick and 1 mm-thick capacitive hair accelerometer arrays.

500 μm Tall Device

Figure 6.25 compares the capacitance testing results of arrays of 25 devices in parallel (500^2 μm^2 proof-mass and 500 thick device silicon wafer) between the two-gap devices and the uniform-gap devices by silicon-on-glass (SOG) process in Chapter 4. The single-ended measurement of one of the axis of a 5×5 array with 500^2 μm^2 footprint proof-mass, 50^2 μm^2 posts achieved a sensitivity of 2.1 fF/g, corresponding to about 80 aF/g per hair device. The SOG device with the same footprint and array size has single-ended sensitivity of 0.25 fF/g. The results show that even starting with the same 500 μm thick silicon substrate the two-gap devices have 8x improvement in capacitive sensitivity.

1 mm Tall Device

Multiple devices with different design parameters (Figure 6.25) are fabricated on the same chip. Since 1mm thick devices has much higher capacitive sensitivity than 500 μm thick devices, all devices are individually readout. COMSOL is also used to re-simulate the device

sensitivity based on the measured fabricated device dimensions by SEM or optical microscope. The electro-mechanical testing results are presented in Table 6.3, compared to the simulated data.

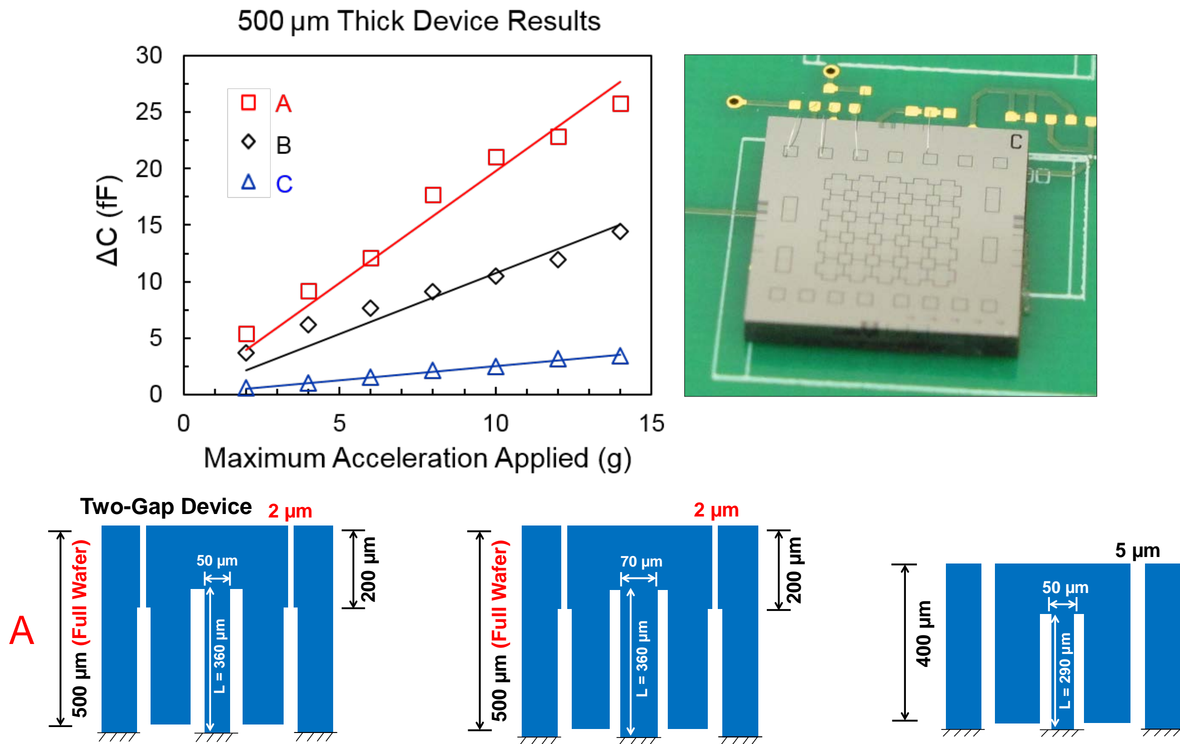
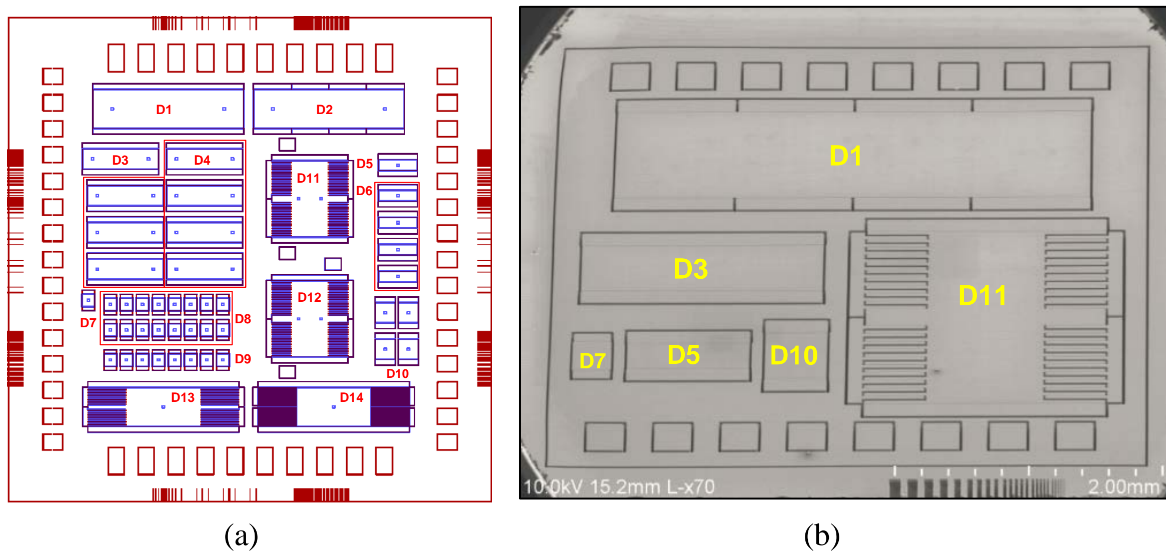


Fig. 6.25. Vibration table electromechanical testing of the second-generation two-gap device compared to the SOG devices, showing an improvement of 8x in capacitive sensitivity.



(a) (b)

Fig. 6.26. Layout of 1mm thick devices: (a) Single chip layout including multiple devices with different designs; (b) SEM of another fabricated chip highlighting the single devices.

Table 6.3: Measured capacitive sensitivity compared to comsol simulation for various accelerometer designs

Device ID	Footprint			Simulated		Measured	
Single Devices	a	b	k	C_0	$\Delta C/g$	C_0	$\Delta C/g$
D1/D2	4 mm	1 mm	$2k_0$	4.080 pF	156 fF/g	3.187 pF	105 fF/g
D3	2 mm	500 µm	$2k_0$	2.187 pF	19.2 fF/g	1.478 pF	12.46 fF/g
D5	1mm	250 µm	k_0	510 fF	2.40 fF/g	728 fF	1.33 fF/g
D7	300 µm	300 µm	k_0	305 fF	0.52 fF/g	257 fF	0.36 fF/g

- Dimensions are measured post-fabrication (Figure 7 & 8);
- Sense area $A = a \times h_{top}$, g_{top} = 1.94-2.69 µm, h_{top} = 233 µm; g_{bot} = 40 µm, h_{bot} = 767 µm;
- Double spring: H = 1 mm, c ≈ 35-40 µm, d ≈ 45-50 µm, L = 600 µm → $k = 2k_0$;

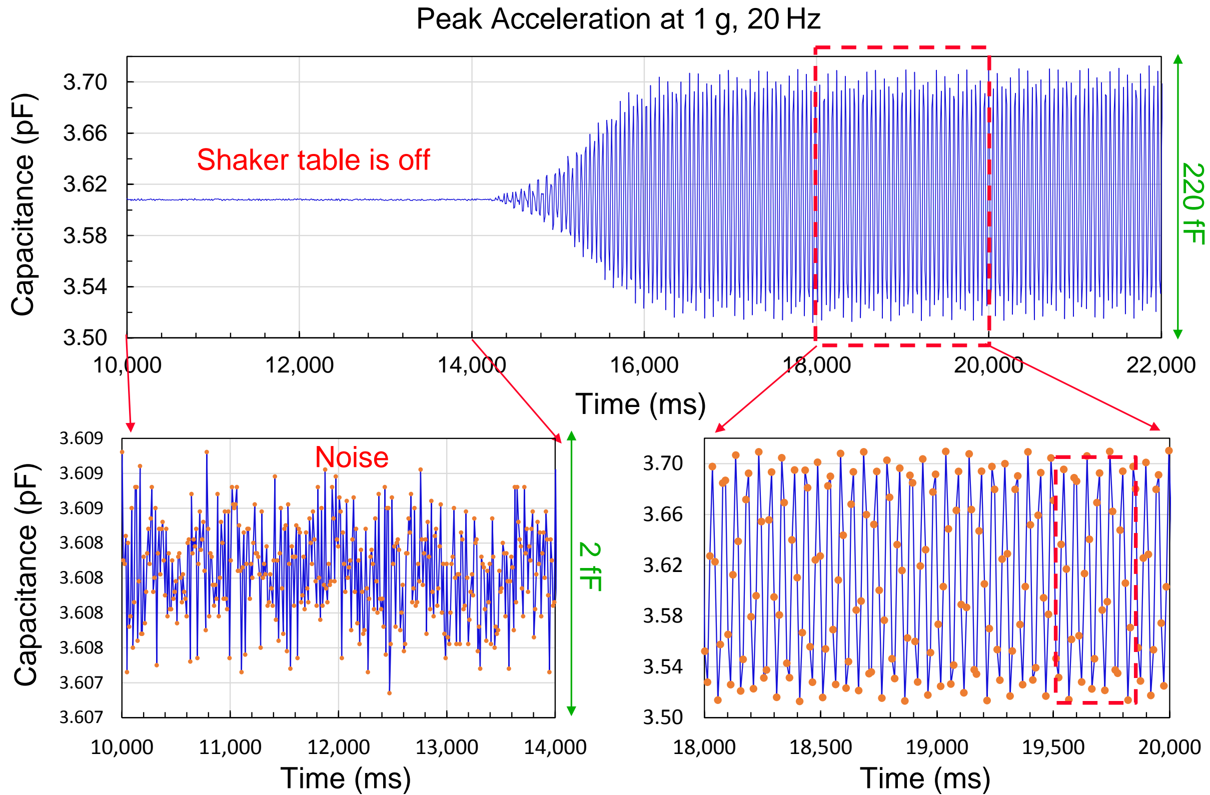


Fig. 6.27. Time-domain response of a 4×1 mm2 footprint hair accelerometer to 1 g acceleration at 20 Hz. The capacitance change ramped up after shaker table is turned on. At 90.0 Hz sampling frequency, the noise envelope is less than 1.5 fF.

Figure 6.27 shows the time-domain response of a 4×1 mm^2 footprint hair accelerometer to 1 g acceleration at 20 Hz. The capacitance change ramped up after shaker table is turned on. At

90.0 Hz sampling frequency, the noise envelope is less than 1.5 fF. Measured ΔC_{ppk} is 196 fF, which corresponds to single-ended sensitivity of 98 fF/g. The y-axis is minus a DC capacitance of 3 pF.

Zooming-in on the response in Figure 6.27, the response is fit with a 20 Hz sine wave as shown in Figure 6.28. Differences in the measured and simulated data are due to the discrepancies between the exact spring/gap profiles of the fabricated devices, and the dimensions assumed in the COMSOL simulation based on the SEM measurement. Parasitics associated with electrical routing and wire bonding will also degrade the capacitive sensitivity.

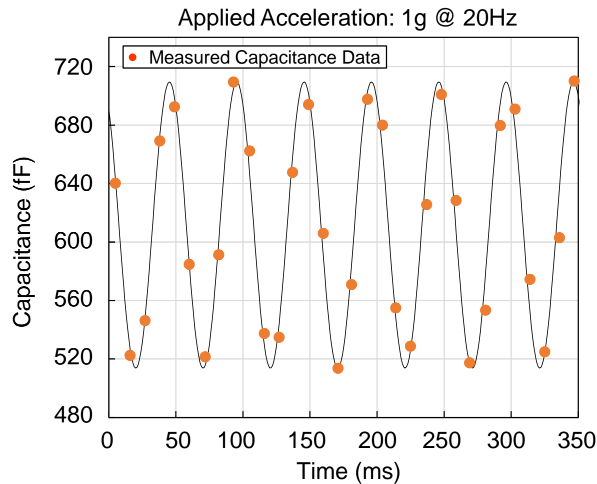


Fig. 6.28. Time-domain response of a 4x1 mm^2 footprint hair accelerometer to 1 g acceleration at 20 Hz and zoom-in on the response in Fig. 6.25. It is fit with a 20 Hz sine wave.

The fabricated accelerometers are also tested on a turntable for DC response. Figure 6.29 presents the open-loop response of this 4×1 mm^2 proof-mass footprint hair accelerometer to input acceleration from 0 g to1 g. ΔC at 1 g measures 105 fF.

Process variations in MEMS fabrication cannot be avoided even within the same 4-inch wafer area, especially when experiments are done at a research environment where production-grade tools are not available. Other deviations from the designed dimensions and specifications are inherent to the process. Figure 6.30 presents the measured change in capacitance of another

4×1 mm^2 footprint hair accelerometer measured over a frequency range, sampled at 90.9Hz. Results are shown at two acceleration levels, 0.1 g and 1 g. The extracted acceleration is greater than 300 fF/g.

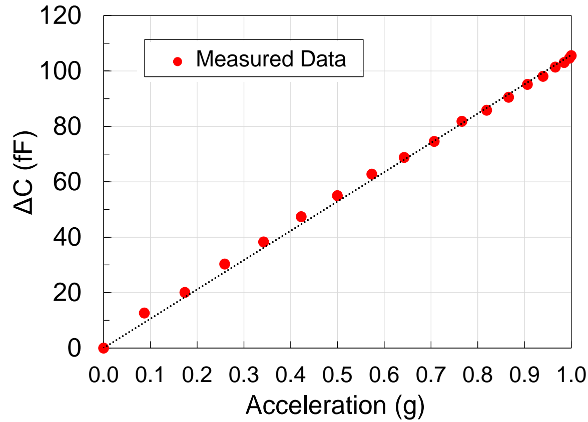


Fig. 6.29. Measured ΔC vs. acceleration for a 4×1 mm^2 footprint hair accelerometer. The acceleration ranges from 0 g to 1 g.

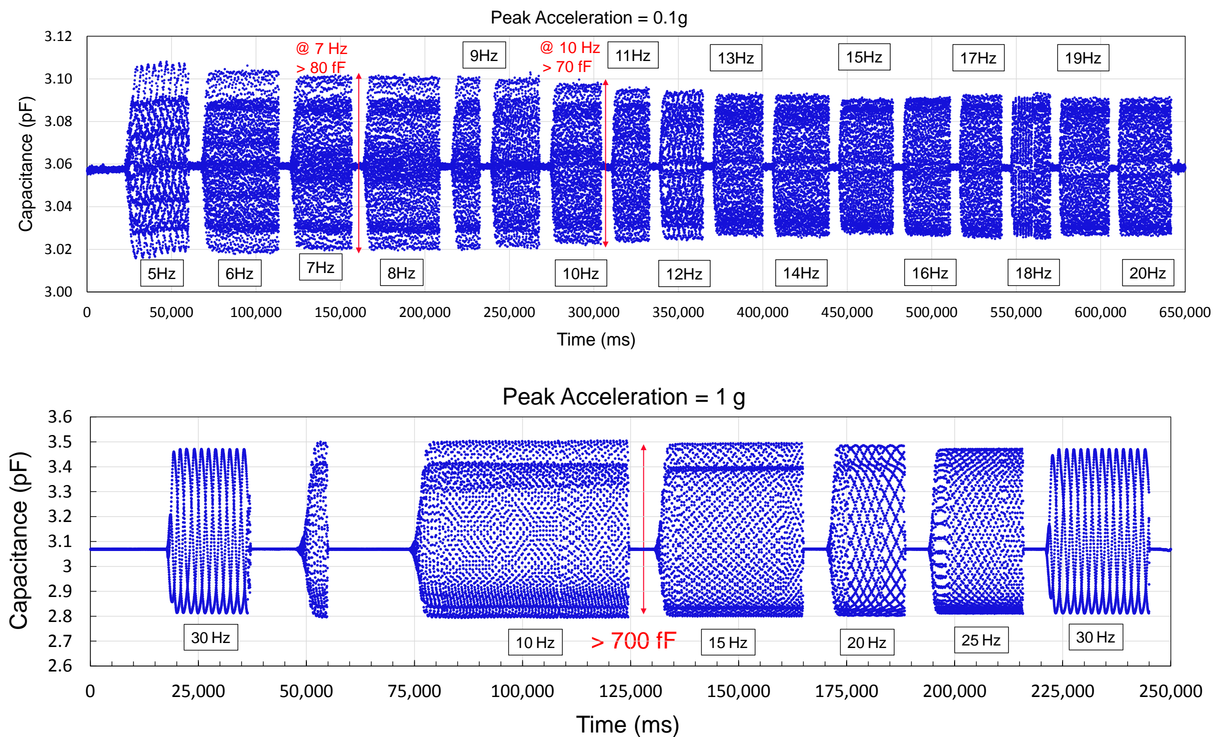


Fig. 6.30. Measured ΔC in time domain for another 4×1 mm^2 footprint hair accelerometer over a frequency range.

DIRE undercut and etch depth non-uniformity across a 4-inch wafer and between different batches cause the critical sensing gap dimensions (g_{top}, g_{bot}, h_{top}, h_{bot}) to vary over a specific range. The gap opening at the junction of the small top gap and large bottom gap is close to 2 μm ($g_{top1} \approx 2$ μm in Figure 6.29) however g_{top2} can could vary over a wider range from >2 μm to 5 μm due to DRIE undercut. At the same time, the exact vertical spring width and length are also affected by DRIE undercut and etch depth non-uniformity.

Figure 6.31 tabulates the estimated capacitive sensitivity for a device with 4×1 mm^2 proof-mass footprint, with h_{top} fixed at 233 μm, spring length (L) fixed at 600 μm and g_{bot} fixed at 40 μm, showing the effect of process-variation induced spring width variation and top gap variation on the change in capacitive sensitivity.

Proof-mass Footprint	Spring Cross-seciton		Top Gap Dimension		Sensitivity
a × b	c	d	gtop1	gtop2	
4×1 mm^2	20 μm	30 μm	2 μm	3 μm	2.12 pF/g
4×1 mm^2	30 μm	40 μm	2 μm	2 μm	704 fF/g
4×1 mm^2	35 μm	45 μm	2 μm	2 μm	392 fF/g
4×1 mm^2	30 μm	40 μm	2 μm	3 μm	464 fF/g
4×1 mm^2	35 μm	45 μm	2 μm	3 μm	256 fF/g
4×1 mm^2	35 μm	45 μm	2 μm	4 μm	192 fF/g
4×1 mm^2	35 μm	45 μm	2 μm	5 μm	153 fF/g
4×1 mm^2	40 μm	50 μm	2 μm	3 μm	152 fF/g
4×1 mm^2	40 μm	50 μm	2 μm	4 μm	115 fF/g
4×1 mm^2	40 μm	50 μm	2 μm	5 μm	91 fF/g

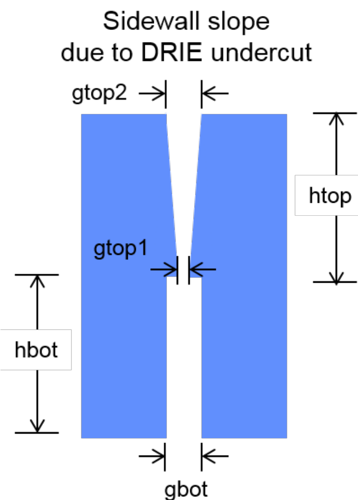


Fig. 6.31. DIRE undercut and etch depth non-uniformity across a 4-inch wafer and between different runs cause the critical sensing gap dimensions and spring cross-sections to vary from the designed values, thus resulting in variation in the capacitive sensitivity.

6.4.2 Resonance Testing and Quality Factor

The frequency response of each single hair accelerometer or an array of accelerometers is measured using a standard bias-drive-sense method for the first bending mode. An AC signal is applied to one electrode and the resulting signal is picked off at the other side, 180˚ offset. Single device D1, D3 and D5 (Table 6.2) have resonant frequencies around 1 kHz, 2 kHz, and 3 kHz at 100 mTorr (Figure 6.32).

Figure 6.33 presents the resonant responses of a single device D3 with footprint $a \times b = 2 \times 0.5\ mm^2$. The resonant frequency f_{res} is measured around 2.1 kHz. The resonant responses are measured at different vacuum levels while sweeping the bias voltage applied. At 100 mTorr and 1 mTorr, Δf_{-3dB} for this device measures > 5 Hz and < 2.5 Hz, which gives $Q \approx 400$ and $Q \approx 800$. At 100 µTorr, Δf_{-3dB} for this device measures < 900 mHz, which gives $Q > 2000$. At 50 µTorr, we zoom-in near the resonant peak with span = 2 Hz, $f_{center} = 2.022146$ kHz and $\Delta f_{-3dB} < 40$ mHz, which gives a $Q > 50k$ (Figure 6.34).

However, the ringing during the frequency sweep may distort this peak at 50 µTorr. For a MEMS resonator, the quality factor Q typically scales inversely with logarithmic of the package pressure P, and plateaus at high vacuum level (low pressure) as measured in [9] when pressure damping is dominant over intrinsic losses such as thermoelastic dissipation (TED) (Figure 6.35).

Resonant peak measurements verified that an array of hair accelerometers can be designed to cover a wide frequency range by simply modifying several key structural parameters. Such an array can be used to construct a MEMS-based mechanical spectrum analyzer more effective and less complex than proposed by Rocha et al. [11]. In [11], the frequency of the drive voltage is swept over a selected range, the mechanical (vibration) spectrum is analyzed in the mechanical domain.

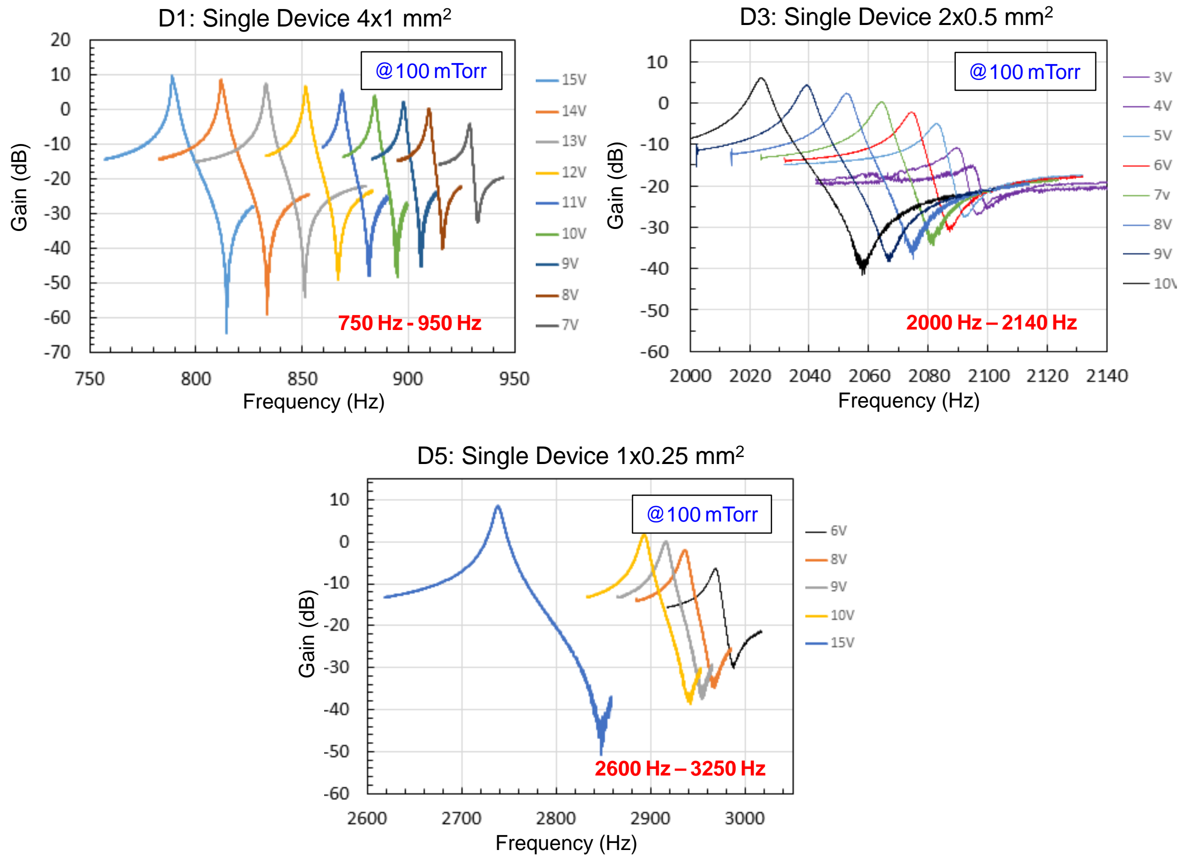


Fig. 6.32. Single devices with different resonant frequencies fres around:1 kHz (Device D1), 2 kHz (Device D3), and 3 kHz (Device D5) at 100 mTorr.

Table 6.4: Quality factor at different vacuum level of device D3

Vacuum Level	Quality factor (Q)
100 mTorr	400
1 mTorr	800
100 µ	> 2000
50 µTorr	> 50000

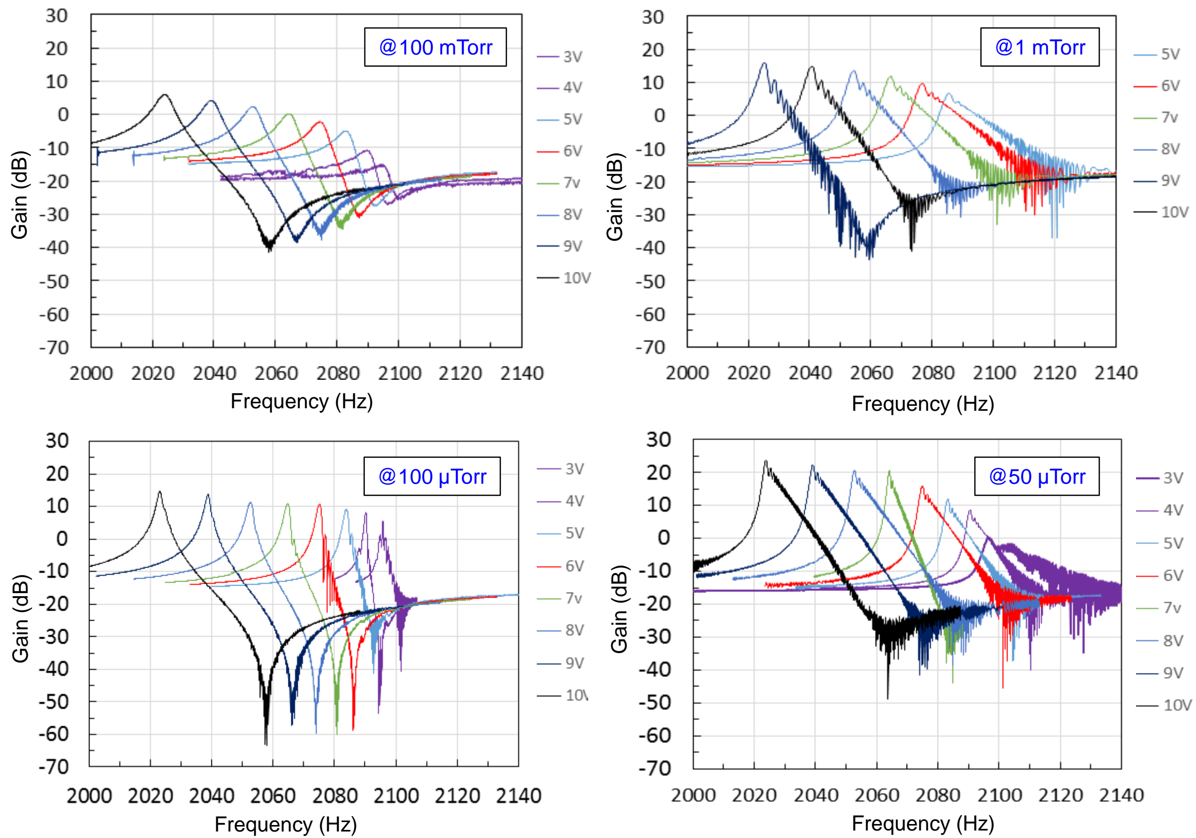


Fig. 6.33. Resonance testing of device D3: single device with footprint a × b = 2000 × 500 μm^2. The resonant frequency f_{res} is measured around 2.1 kHz. The resonant responses are measured at different vacuum levels with different bias voltage applied.

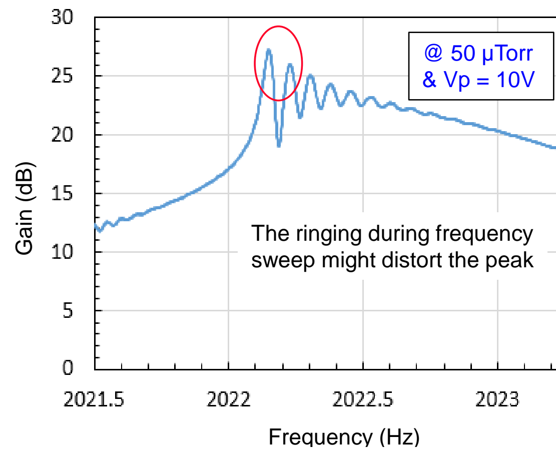


Fig. 6.34. Zoom-in on resonant peak of device D3 single device with footprint a×b = 2 × 0.500 mm^2. The ringing during the frequency sweep may distort the peak. At 50 μTorr, it is zoomed-in near the resonant peak with span = 2 Hz, f_{center} = 2.022146 kHz and Δf_{-3dB} = < 40 mHz, which gives a Q > 50k.

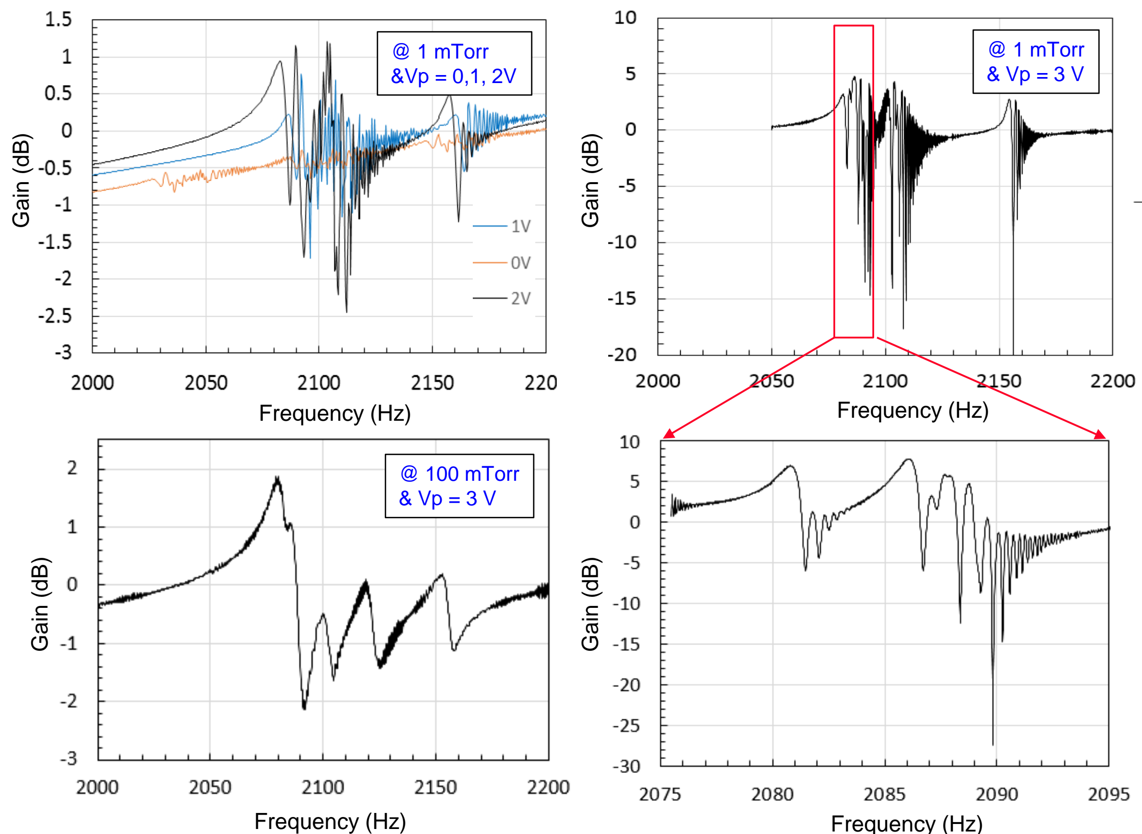


Fig. 6.35. Zoom-in the resonant response of an array of seven D3 in parallel (D4 in Figure 6.24). Multiple peaks are observed. At 100 mTorr, we can track the resonant peak shifts between the multiple devices in the array.

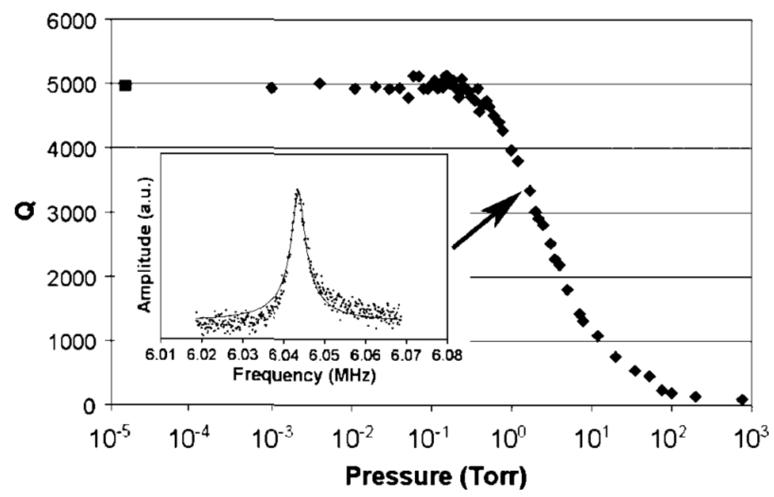


Fig. 6.36. Quality factor vs. pressure curve [10].

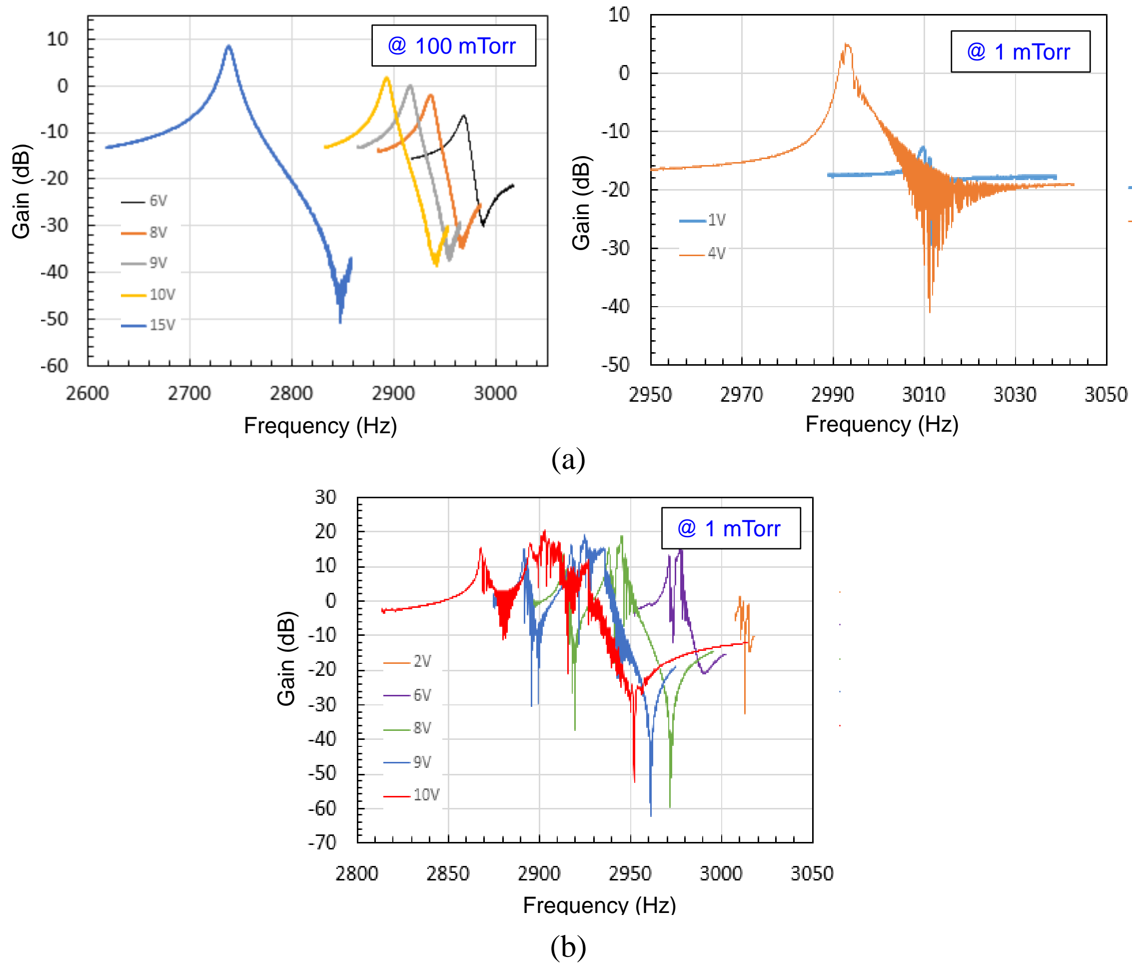


Fig. 6.37. Comparison between the resonant responses around 3 kHz of (a) D5: single $1000 \times 250\ \mu m^2$ and (b) an array of four D5 in parallel (D6 in Figure 6.24).

6.5 References

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Chapter 7 CAPACITANCE READOUT FRONT-END

7.1 Precision Readout Circuits for Capacitive MEMS Accelerometer

In section 6.4, the noise envelop from the Analog Device CDC chip is 1.5-2 fF when sampled at 90.9 Hz. For a capacitive MEMS accelerometer that has sub-μg resolution and is tested to have 100 fF/g sensitivity, it is difficult to resolve less than 20 mg acceleration. High precision measurement is not possible without a front-end capacitive readout interface closely integrated with the sensor output, either by wire-bonding or direct 3D stacking.

The three most commonly adopted readout circuits for capacitive MEMS accelerometers are AC-bridge with voltage amplifier, transimpedance amplifier (TIA) and switch capacitor (SC) circuit as shown in Figure 7.1 [11]. The voltage output V_{out} and the capacitance readout resolution $\Delta C_{min\ rms}$ are listed for each readout scheme.

Similar to our hair accelerometer structure (Figure 2.3 and Figure 6.1) for which there are at least one electrode on each side of the proof-mass along the sensitive axis that form a differential pair, in most cases, capacitive MEMS accelerometers are designed to provide a differential capacitance output. The reference capacitors C_r in in Figure 7.1 has the same rest capacitance as C_{S0} and change in opposite polarity (+ΔC and – ΔC).

The design goal is to increase V_{out} and improve the capacitance readout resolution, i.e. minimizing $\Delta C_{min\ rms}$.

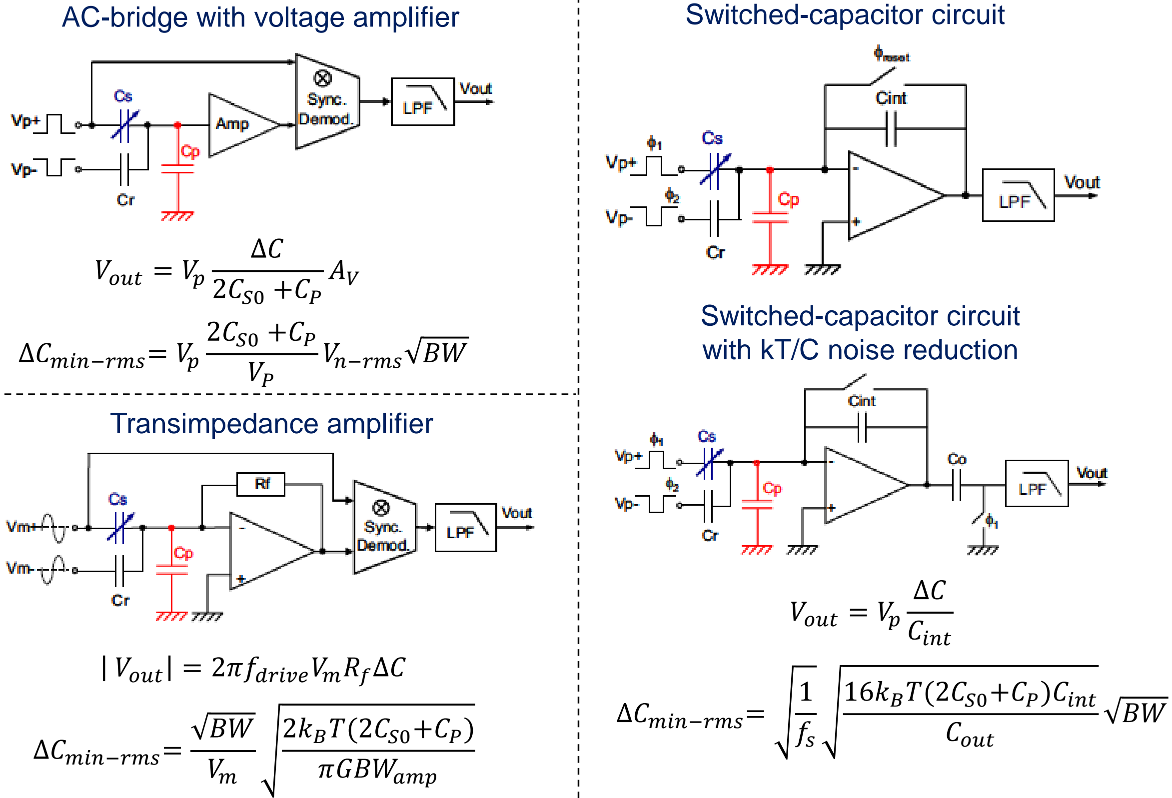


Fig. 7.1. Simplified block diagram of various capacitive readout circuits: AC-bridge with voltage amplifier, transimpedance amplifier (TIA), and switch capacitor circuit (SC) [11].

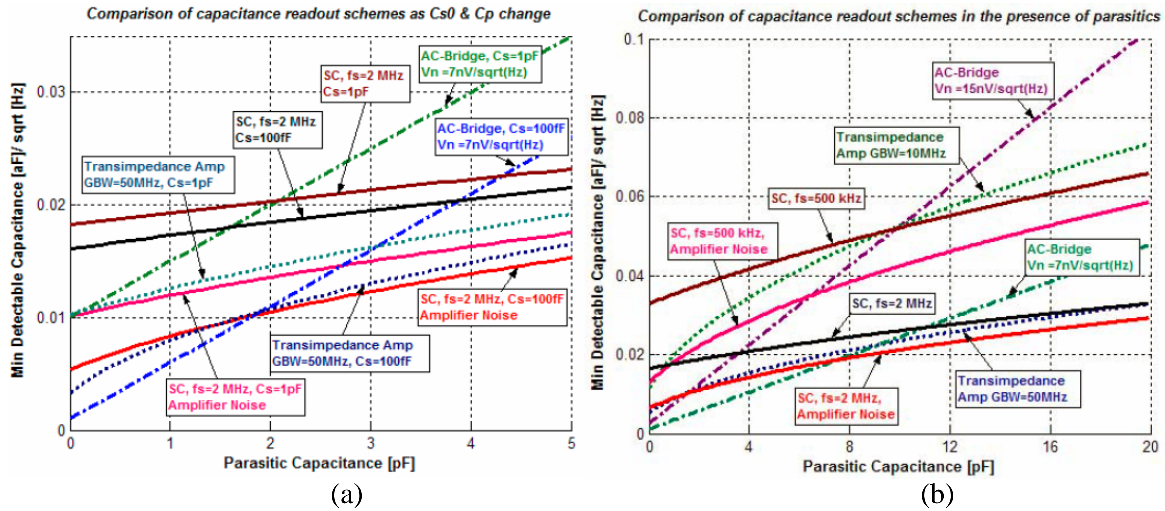


Fig. 7.2. Minimum detectable $\Delta C_{min\ rms}$ for different capacitance readout schemes [11]: (a) Comparing C_{S0}=100 fF and C_{S0}=1 pF shows that a larger C_{S0} will result in larger $\Delta C_{min.}$; and (b) Capacitance resolution for various readout schemes with C_{S0}=250 fF.

For capacitive MEMS, as the rest/nominal electrostatic gap g_0 is reduced and sensing area A is increased to achieve larger capacitance change ΔC, the sensor rest capacitance C_{S0} also increases. For AC-bridge with voltage amplifier, the correlation between ΔC and has an inverse effect on increasing V_{out}, while for TIA and SC configuration, V_{out} is not dependent on C_{S0} so that ΔC can be optimized by reducing the nominal sensing gap.

At the same time, a larger C_{S0} will result in a larger minimum detectable $\Delta C_{min.}$ for all readout schemes as shown in Figure 7.2(a), comparing C_{S0}=100 fF and C_{S0}=1 pF. Figure 7.2(b) presents the capacitance resolution for various readout schemes: AC-bridge offers the best resolution if parasitics are small; the virtual ground at the input of both TIA and SC circuits reduce the input parasitic capacitance C_P; SC circuit resolution improves with higher sampling frequency (thus it consumes more power) and efficient cancellation of kT/C noise, and it is also suitable for large input C_P.

Since the SC scheme is more suitable for non-monolithic integration that has relatively large parasitic capacitance, in the next sub-sections, we will first discuss the implementation of switched-capacitor charge amplifier front-end and the feasibility of monolithic integration of hair accelerometer arrays of front-end CMOS circuit. It is also the basic building block in a ΣΔ architecture which we will investigate in the future for high resolution readout [2].

7.2 Pixel-Level Differential Switched-Capacitor Charge Amplifier Front-End

Switched-capacitor front-end is investigated as the capacitance to voltage convertor for readout of our capacitive hair accelerometer arrays. As shown in Figure 7.3, each hair sensor has its own front-end switched-capacitor block. The output from each channel are multiplexed in time. The amplifier offset and 1/f noise, charge injection, and kT/C noise can be cancelled by correlated double sampling (CDS) [3]. CDS is performed at the preamplifier output so the errors

from both amplifiers are cancelled. The virtual ground at the input of SC readout reduces the effect of input parasitic.

Implementing pixel-level switched-capacitor circuit has the advantage of being able to adjust the circuit gain to accommodate a wider range of ΔC since our accelerometer array covers a wide range of capacitive sensitivity (ΔC/g) and nominal capacitance (C_{S0}). It also has the advantage of parallel processing of each sensor and achieving a higher sampling rate. However, it is done at a cost of the overall power consumption scaling with the number of sensor in the array. In order to reduce the power consumption, several sensors can share the same SC circuit as will be shown later in Figure 7.5.

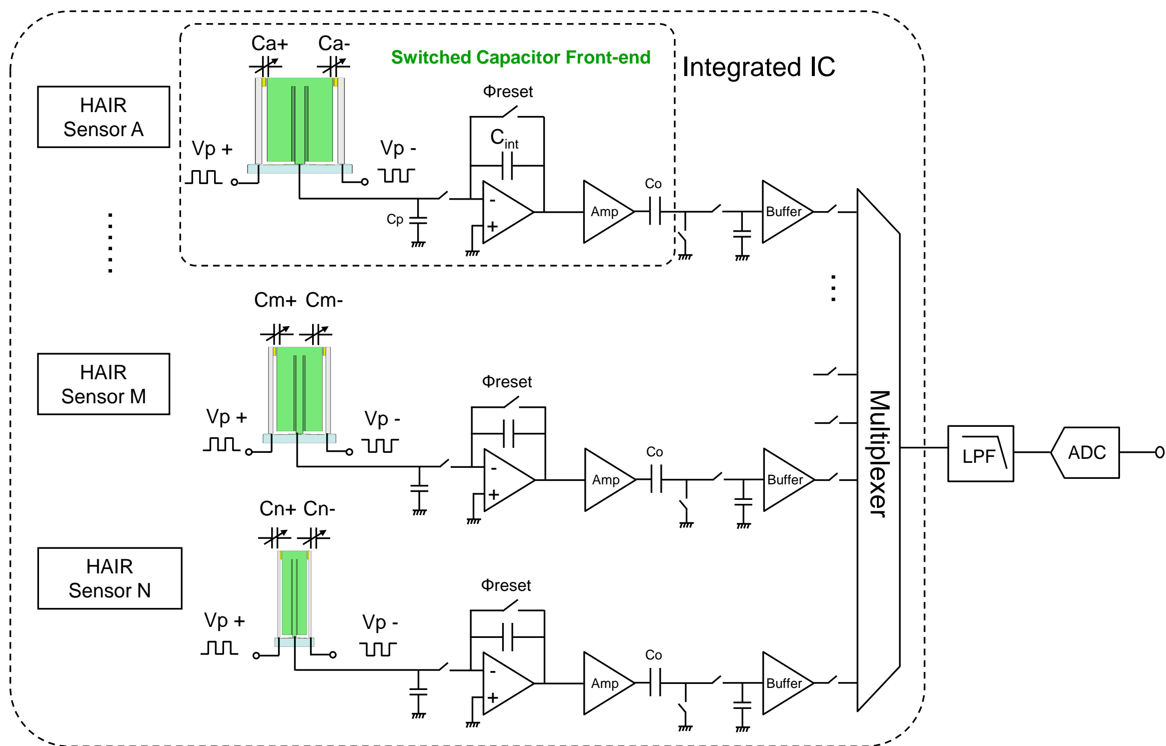


Fig. 7.3. Hair sensor array with integrated IC block diagram: switched-capacitor front-end and multiplexing of sensor array.

A switched-capacitor charge amplifier front-end is designed and layout in TSMC 0.18μm technology as shown in Figure 7.4. The design specifications of this core rectangle block front-end is tabulated in Table 7.1 and it can be repeated to incorporate multiple sensors in future runs.

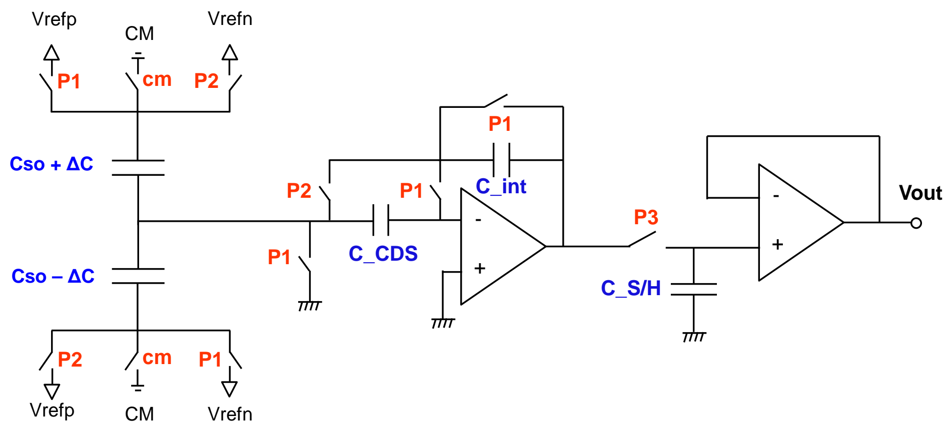
Table 7.1: Interface IC with MEMS

Technology	TSMC 180 nm CMOS
Supply voltage	0, 1.8 V
V_{cm}	0.9 V
V_{refp}, V_{refn}	0.3 V, 1.5 V
Sampling clock (f_S)	Desired Data Rate × N Eg: 2 kHz × 16 = 32 kHz 1 kHz × 1024 = 1 MHz
C_{int}	0.5 pF
$C_{S/H}$	3 pF
C_{S0}	Wide range: 300 fF to < 4 pF
Circuit Gain	4.8 mV/fF
Max Output Swing	±800 mV
Open-loop max. ΔC	0.167 pF
Opamp design specifications:	
Open-loop gain (AOL)	>100 dB
Phase margin (φM)	42°
Power consumption of two amplifiers	1.8V × (2 × 440μA) = 1.584mW

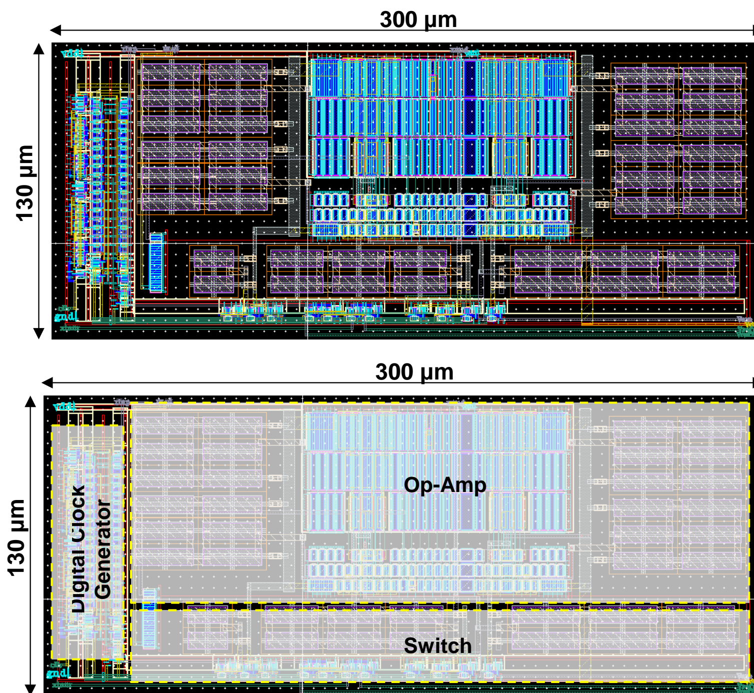
Figure 7.5(a) shows the schematic of four sensors with different sensitivity (ΔC/g) sharing a common readout block from Figure 7.4. The proof-mass terminal of each sensor is connected to one common node and connected to the inverting input of an op-amp, bypassing a correlated-double-sampling capacitor (C_{CDS}) [3]. The time-domain transient simulation results by Cadence of the four-sensor array is presented in Figure 7.5(b). The non-overlapping clock cycles/phases (P1, P2 and P_{CM}) for the four sensors are multiplexed in time. The clock signals are generated by the on-chip digital clock generator from an off-chip clock signal.

When one sensor is selected for readout, during phase P1, the differential capacitor pair C_{S+} (C_{S+}=C_{S0}+ΔC) and C_{S-} (C_{S-}=C_{S0}+ΔC) are charged with opposite polarity voltages, V_{refp} and

V_{refn} respectively. During the delayed and complementary P2, V_{refn} and V_{refp} are applied respectively such that a packet of charges proportional to the capacitance change ΔC are integrated on the integration capacitor C_{int}. During the active readout cycle of one of the N sensors, the two electrode-terminals of the other (N-1) sensors are connected the common mode potential (CM) thus they appear as a lumped parasitic capacitor $C_p = (N-1)\ C_S$.

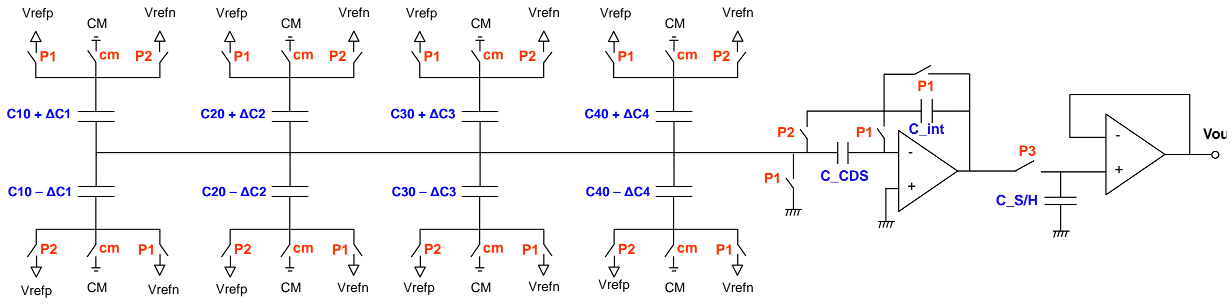


(a)

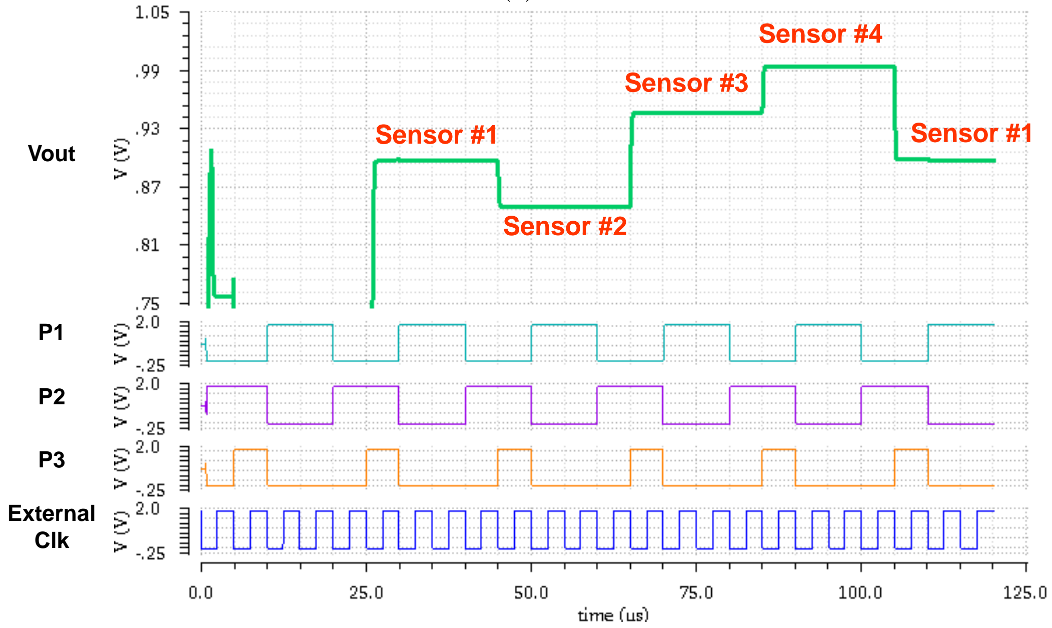


(b)

Fig. 7.4. Switched-capacitor front-end core: (a) schematic, (b) layout including both digital and analog block.



(a)



(b)

Fig. 7.5. Cadence transient simulation showing multiplexing of four sensors.

Interface Circuit Noise

The circuit thermal noise that limit the performance of the SC circuit should be evaluated and compared with the mechanical noise in order to determine the overall system performance, assuming correlated-double-sampling (CDS) technique is incorporated and larger input PMOS devices are used to effectively reduce the 1/f noise.

We mainly focus on the sampled thermal noise as a function of frequency (f_{sample}), sensing capacitor (C_1), sampling capacitor (C_2) and load capacitor (C_3) in Figure 7.6(a). The

circuit's thermal noise sources in our system can be categorized into: 1) front-end amplifier noise, 2) kT/C switch sampling noise, and 3) sensor charging reference voltage noise of V_{ref}.

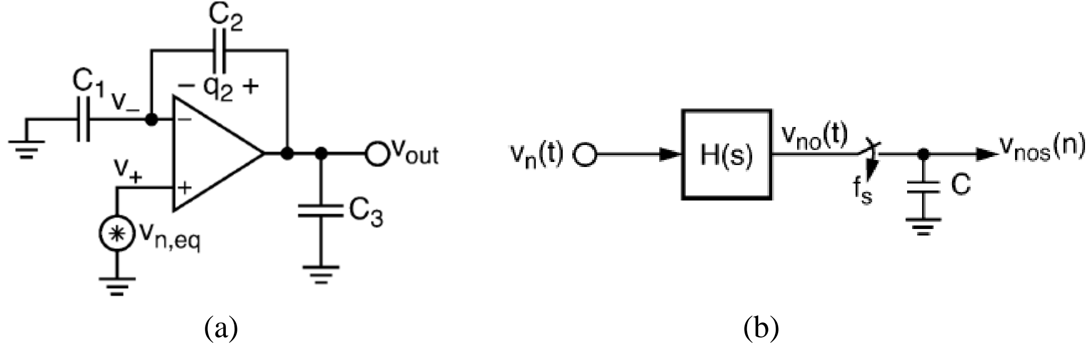


Fig. 7.6. Calculation of equivalent noise of continuous and sampled data [12].

In our op amp implementation, we study the effect of the thermal noise of the input differential pair [12]. The total thermal noise of the stage is represented by a single equivalent noise voltage source $v_{n,eq}$ in Figure 7.6(a) and it has PSD $S_{vt}(f) \approx \frac{16KT}{3g_{m1}}$.

The closed-loop transfer function H(s) of the input stage is:

$$H(s) = \frac{Go}{1+s\tau} \approx \frac{\frac{1}{\beta}}{1+s\tau} = \frac{1+\frac{C_1}{C_2}}{1+s\tau}$$

$$\tau = RC = \frac{\beta C_{out}}{g_{m1}} = \frac{\left(1+\frac{C_1}{C_2}\right)\left(C_3 + \frac{C_1 C_2}{C_1 + C_2}\right)}{g_{m1}}$$

Under negative feedback $v_{n,eq}$ is shaped by H(s) and produce an output noise component:

$$\overline{v_{out}^2} = \int_0^\infty S_{vt}(f)|H(j2\pi f)|^2 df = \frac{16KT}{3g_{m1}}\frac{Go^2}{4\tau} = \frac{4KT}{3\beta C_{out}}$$

The sampled system (Figure 7.6(b)) will magnify the noise PSD due to aliasing (if used without oversampling) by a factor of $1/(2\tau fs)$. The power of the noise being shaped by H(s) and then sample at fs is:

$$\overline{v_{no}^2} = \overline{v_{out}^2}$$

$$S_{nos}(f) = \frac{\overline{v_{no}^2}}{fs/2} \approx \frac{Go^2 Svt}{2\tau fs}$$

Thus, the sampled thermal noise at the output is:

$$v_{out_thermal} = \sqrt{\frac{8kT}{3C_{out}}\left(\frac{C_1 + C_2 + C_P}{C_2}\right)\frac{1}{fs}} = \sqrt{\frac{8kT}{3C_{S/H}}\left(\frac{C_{S0} + C_{int} + (N-1)C_{S0}}{C_{int}}\right)\frac{1}{fs}}\left(\frac{V}{\sqrt{Hz}}\right)$$

Our implementation of the switch-capacitor front-end shown in Figure 6.39 has the following components:

- $C_1 = C_{S0}$: the rest sensing capacitors C_{S0} that covers a wide range across the array depending on the sensor design;
- $C_2 = C_{int} = 0.5pF$, is the sampling capacitor;
- $C_P = (N-1)\ C_{S0}$, during the active cycle of one of the sensors and appears as parasitics;
- $C_{out} = C_{S/H} = 3pF$, $C_{S/H}$ is the sample and hold capacitor;
- f_S: the sampling frequency of P3.

Since $C_{S/H}$ and C_{int} are integrated on-chip, they cannot be modified post-fabrication. However, the C_P can be modified post-fabrication to study the effect of the scaling of the sensor arrays.

kT/C switch sampling noise and reference voltage noise can be expressed as followed:

$$vout_{kT/C} = \sqrt{\frac{4kT}{fs\ C_{int}}}\left(\frac{V}{\sqrt{Hz}}\right)$$

$$vout_{Vref} = \sqrt{\frac{2Vn^2 Cs}{fs\ R_{SW}\ {C_{int}}^2}}\left(\frac{V}{\sqrt{Hz}}\right)$$

These two noise sources all have strong dependence on two parameters: C_{int} and f_S. The transmission gate switches' equivalent switching resistance R_{sw} is simulated by Cadence to be

1kΩ. For an array of four sensors (N=4), with C_{S0} = 2 pF and v_{ref} with PSD = 10nV/√Hz, the contributions from the three circuit noise sources are listed in Table 7.2. The resolution improves as the sampling frequency increases.

Table 7.2: Interface circuit noise of switched-capacitor front-end

	Amplifier Noise	kT/C	Vref Noise	Total Noise
fs = 100 kHz	0.791 μV/ √Hz	0.575 μV/√Hz	4 μV/√Hz	5.366 μV/√Hz
fs = 500 kHz	0.354 μV/ √Hz	0.257 μV/√Hz	1.79 μV/√Hz	**2.401 μV/√Hz**
fs = 1 MHz	0.259 μV/ √Hz	0.182 μV/√Hz	1.27 μV/√Hz	1.711 μV/√Hz

The overall system resolution would be limited by the circuit noise if it is greater than the mechanical noise floor. With V_{refp} - V_{refn} = 1.2 V and C_{int} = 0.5pF (4.8 V/pF), the output voltage gain is calculated as a function of capacitive sensitivity.

Table 7.3: Circuit Gain

Sensitivity	Circuit Gain	Sensitivity	Circuit Gain
0.1 fF/g	0.48 μV/mg	**1 pF/g**	**4.8 mV/mg**
1 fF/g	4.8 μV/mg	2 pF/g	9.6 mV/mg
10 fF/g	48 μV/mg	10 pF/g	48 mV/mg
100 fF/g	0.48 mV/mg		

The ratio of circuit thermal noise floor and voltage/acceleration gain is the circuit equivalent noise acceleration (CNEA). For example, for an interface with output noise floor at 2.4 μV/√Hz from Table 7.3 and voltage/g gain of 9.6 mV/mg (for a device with 1 pF/g capacitive sensitivity in Table 7.4), the resolution limited by circuit performance can be calculated as 500 ng/√Hz. If this sensor having capacitive sensitivity at 1 pF/g has a mechanical thermal noise floor <500 ng/√Hz, the resolution of the system (sensor and front-end circuit) is limited by the interface circuit.

7.3 CMOS MEMS Integration

To integrate large arrays of hair sensors, CMOS-MEMS chip-to-chip or wafer level integration process need to be developed specifically to incorporate the 2-gap hair structure fabrication process.

As we have discussed in Chapter 1, the best method for integrating arrays of hair sensors with CMOS is by vertical integration since it allows increased pixel-level data processing and device optimization. Both the MEMS devices and CMOS chips/wafers can be optimally designed and fabricated in the mostly suitable technology. Resistance and capacitance contributed by wirebond or long traces on PCB are replaced by shorted interconnections between the vertically-stacked dies, thus reducing RC delay as well as transmission power loss. In addition, the number and density of signals connecting the CMOS and MEMS sensor chip is not limited by pad numbers on the perimeter, but is rather limited by the technology in making reliable metallic interconnects with fine pitch, thus 3D stacked-integration has the potential to substantially increase the information flow.

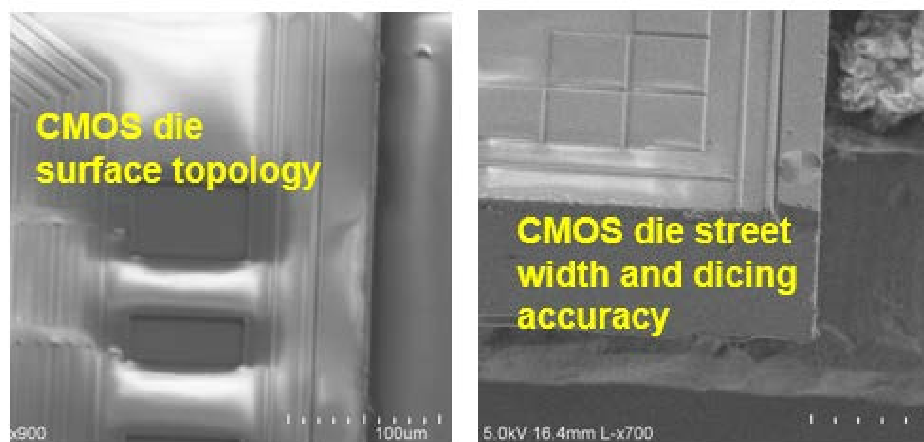
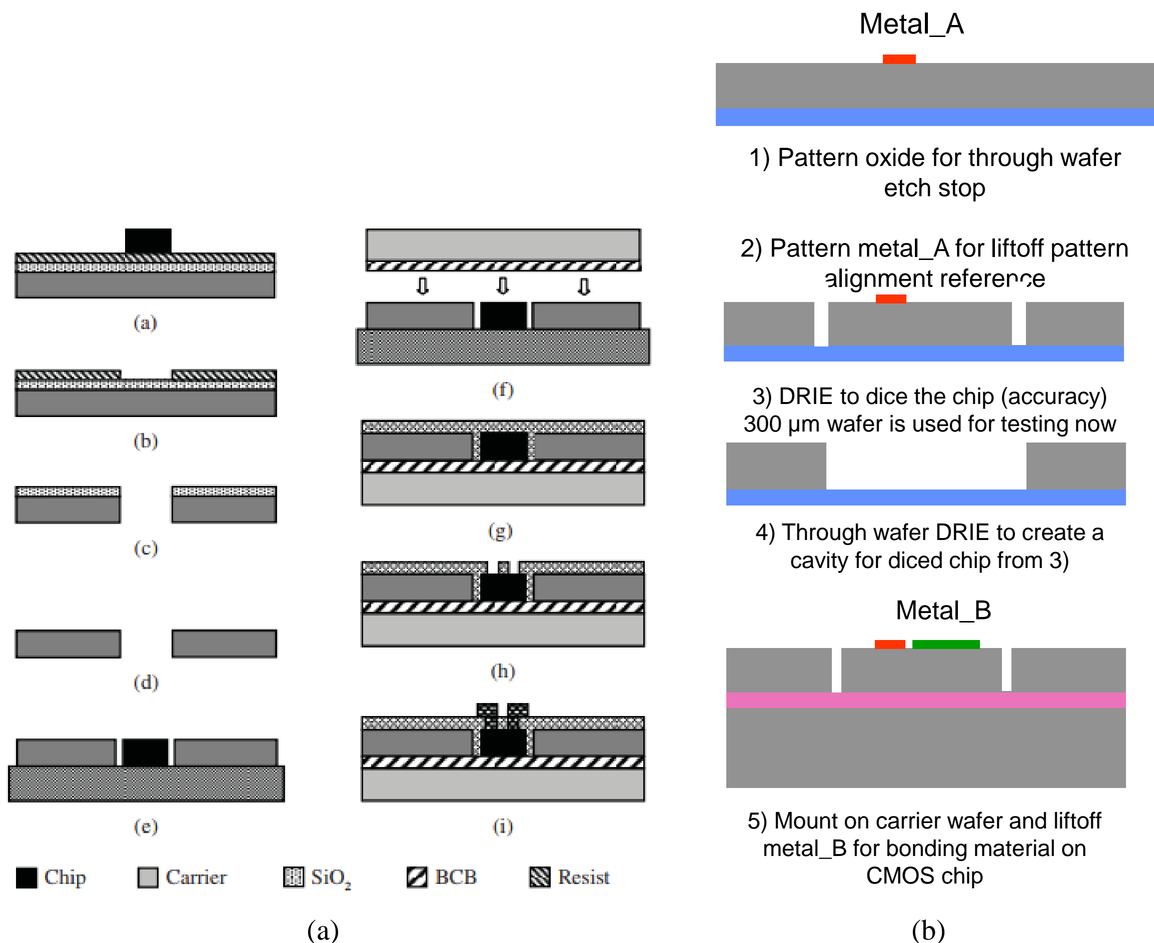


Fig. 7.7. CMOS chip from 180nm process: bond pads for post-CMOS processing and integration and die edge.

Figure 7.7 shows SEMs of CMOS chip from 180nm process highlighting the bond pads and chip edge. To process the IC chip, top surface metallurgy (TSM) needs to be patterned on aluminum bond pads from the CMOS process after removing the native aluminum oxide. CMOS die street width and dicing accuracy should also be well characterized to ensure successful patterning and subsequent CMOS-MEMS integration. In addition, CMOS chip surface topology will be different for different IC processes.



(a) (b)

Fig. 7.8. (a) CMOS chip and microfluidic chip self-aligned (accuracy can be within 5 μm) integration process includes placing the CMOS die in a silicon socket and patterning metal lift-off on CMOS chip for electrical connections; (b) Testing procedure to verify the alignment accuracy of process in (a): metal A represents the original patterns on CMOS chip and metal B will be lift-off when the chip is placed in the socket.

Figure 7.8(a) presents the process steps to package a CMOS chip with a microfluidic chip proposed by Uddin et al. [5]. This process allows for the fabrication of sockets in wafers that are at most 5 μm larger than the chip on each side. After patterning the cavity to place the chip inside, the cavity and the chip are placed face-down on a carrier substrate. BCB-coated carrier is then bonded with the backside of the chip and the holder. During the bonding, the gap between the chip and the cavity is filled and the top surface is planarized with Spin-on-Glass SOG. Vias to the contact pads of the chip are created by patterning the spin-on-glass (SOG) layer followed by making the metal interconnects from the chip to the cavity.

This method provides us inspiration on post-processing of CMOS dies for integration with MEMS chips with sensor arrays which include three major steps in addition to the original hair structure 2-gap process: (1) Pattern bonding interlayers on the foundry CMOS chip (Figure 7.8(b)); (2) Bond the MEMS hair array chip fabricated in-house with the patterned CMOS chip, and (3) DRIE release the MEMS devices arrays (Figure 7.9).

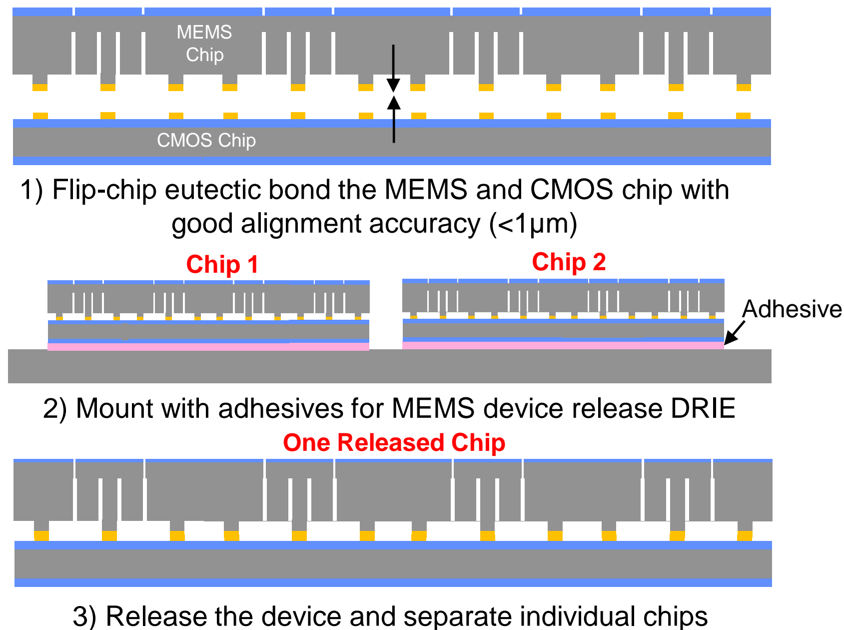
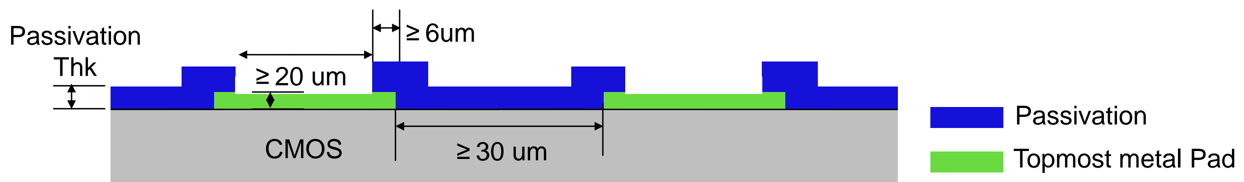


Fig 7.9. CMOS-MEMS chip-scale integration and hair sensor array release process.

Since every CMOS technology has different parameters for its conductive layers and dielectric layers, choosing the suitable and cost-effective IC technology for integration of MEMS and CMOS is critical. For the hair sensor array chip, the width or length of each sensor in the wafer plane (including the sensor and electrodes) could vary from several tens of microns, to several hundreds of microns, up to several millimeters. For the smaller footprint devices, the bond-pad density available for 3D-stack integration of the MEMS chip on top of the CMOS chip is limited by the minimum bond pad / passivation opening, pad metal overlap of passivation, and minimum pad spacing to unrelated metal (metal-to-metal or M2M). For example, as shown in Figure 7.10, the electrode pitch for this technology is at least:

$$\mathit{nin.\ pad\ opening} + 2\times \mathit{overlap} + M2M = 20\ \mu m + 2\times 6\ \mu m + 30\ \mu m = 62\ \mu m$$

In addition, the finished chip surface is not flat. For example, as shown in Figure 7.11 using the TSMC 0.35-µm technology (2015) surface topology scan, the passivation openings are the lowest points on the chip, 1.5 µm below the uniform passivation level. Additional topology is present where UTM (ultra-thick-metal) is patterned.



Rule	Description	Microns (*not* lambda)
10.1	Minimum bonding passivation opening	60
10.2	Minimum probe passivation opening	20
10.3	Pad metal overlap of passivation	6
10.4	Minimum pad spacing to unrelated metal	30
10.5	Minimum pad spacing to active, poly or poly2	15

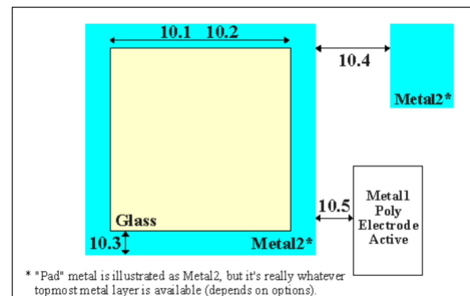
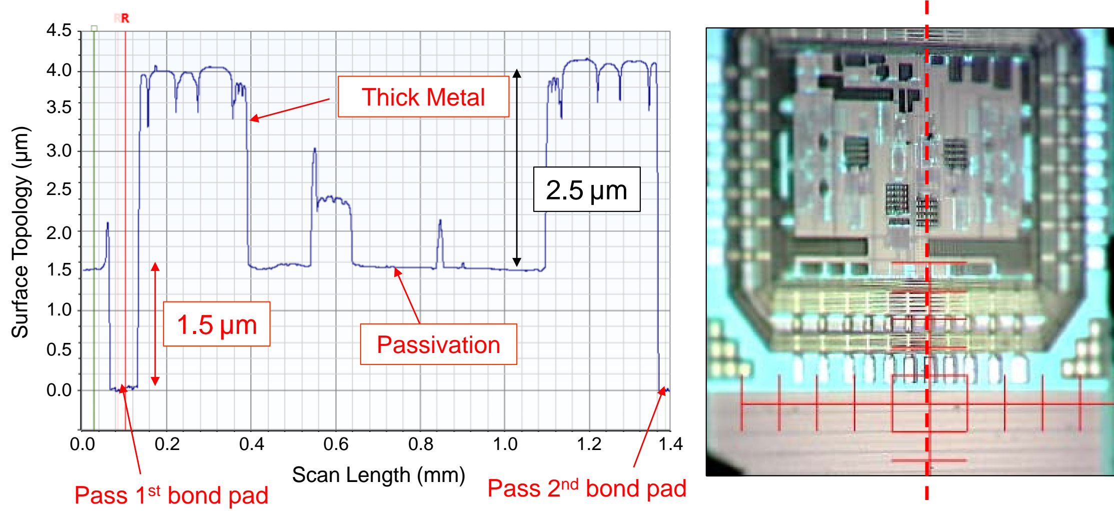
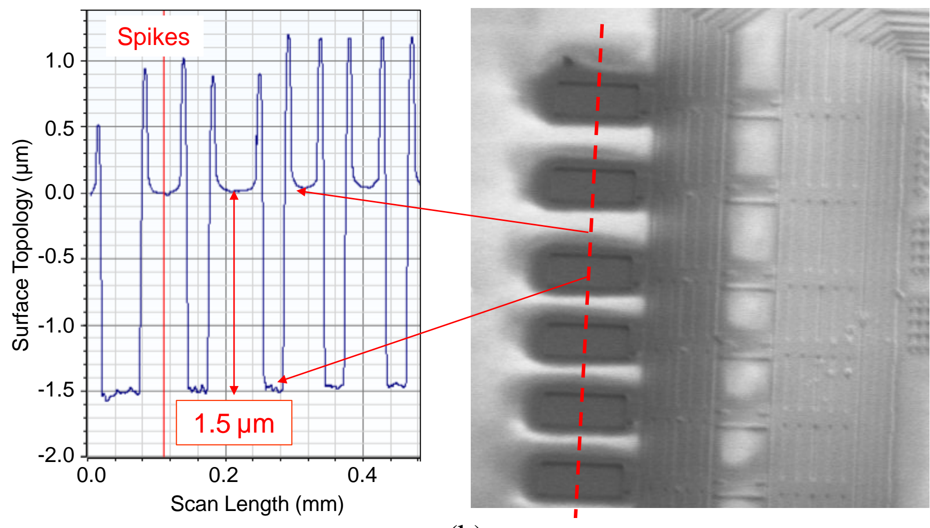


Fig 7.10. Technology parameters of top metal and passivation layers of an IC technology.



(a)



(b)

Fig 7.11. TSMC 0.35-µm technology (2015) surface topology scan: passivation openings are the lowest points on the chip, 1.5 µm below the flat passivation level. Additional topology is present where UTM (ultra-thick-metal) is patterned.

When bonding the vertical hair springs of width w to the exposed bond pad openings (passivation openings), we need to take into consideration the misalignment m_1 produced by different bonding methods: die-to-die (D2D), wafer-to-wafer (W2D), or die-to-wafer (D2W) as shown in Figure 7.12. If no tolerance is designed, i.e. the spring width w is exactly the same as the bond pad openings, the flat bottom of the spring may land on the step boundary of the bond

pad openings and pad metal- passivation overlap when there's misalignemtn. The bond pad openings (passivation openings) thus should be at least $w + 2m_1$:

$$nin.\ pad\ opening \geq w + 2m_1$$

The state-of-the-art Finetech Flip Chip Bonder at LNF can achieve $m_1 = 1$ µm alignment accuracy die-to-die or die-to-wafer, while at least 10-20 µm alignment error is expected if a mechanical alignment jig is designed to perform the alignment.

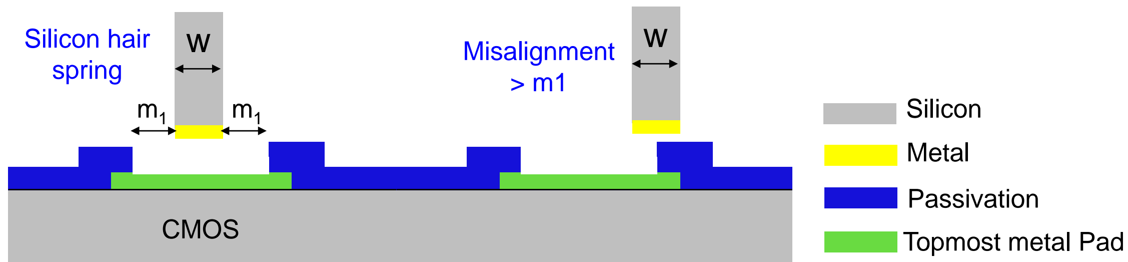


Fig 7.12. CMOS-MEMS chip-scale integration and hair sensor array release process.

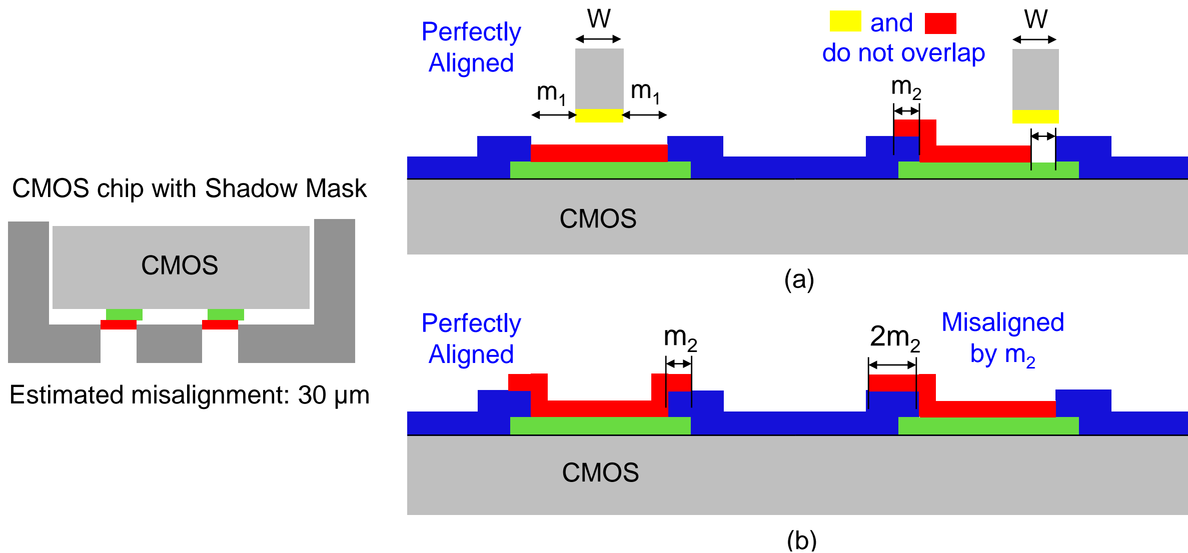


Fig 7.13. Pattern additional metal by shadow mask. (a) Width designed the same as the bond pad opening cannot cover the bond pad with misalignment m_2; (b) The metal pattern extended by m_2; to cover the exposed bond pad.

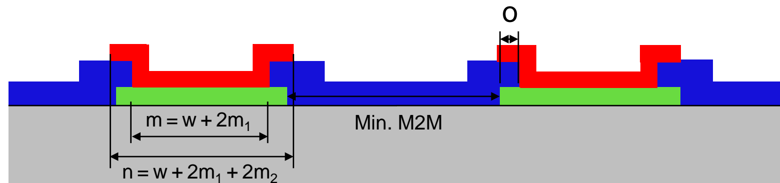
To electrically contact the exposed Al pad and to assist bonding of silicon hair spring to the CMOS die at the pad, a gold layer (Au) with diffusion barrier can be patterned on top of exposed Al. m_2 is the misalignment when patterning this metal layer by shadow mask or

lithography. To ensure this metal covers the exposed bond pad metal, the metal pattern has to be wider than $w + 2m_1 + 2m_2$ as shown in Figure 7.13:

Metal pattern width: $n \geq w + 2m_1 + 2m_2$

The minimum electrode spacing/pitch is the greater dimension of $m + 2\times overlap + M2M$ and $n + 2m_2$. Figure 7.14 shows that when the misalignment m_1 and m_2 are small, the minimum electrode pitch is bounded by the sum of the bond pad passivation overlap and the minimum metal-to-metal (M2M) spacing.

Min. electrode pitch $= max\ (m + 2\times overlap + M2M,\ w + 2m_1 + 4m_2)$



w: spring width		20	20	20	20	20	20	20	20
m_1:bond misalign.		20	20	10	10	5	5	5	1
m_2: metal pattern misalign.		20	10	20	10	20	10	5	1
m: $w + 2m_1$		60	60	40	40	30	30	30	22
n: $w + 2m_1 + 2m_2$		100	80	80	60	70	50	40	24
o: Metal Pass. overlap		6	6	6	6	6	6	6	6
Min. M2M		30	30	30	30	30	30	30	30
Min Electrode Pitch	m + o + M2M	96	96	76	76	66	66	66	58
	$n + 2m_2$	140	100	120	80	110	70	60	26

- Unit: micron (μm)
- Small bonding misalignment by flip-chip bonding (<1μm)
- Metal pattern accuracy increases by lithography instead of shadow mask

Fig 7.14. Minimum electrode pitch determined by technology parameters and alignment capability.

Further applying the analysis to integration of the MEMS hair array chip with a CMOS chip, the minimum hair pixel is at least three times (3x) the electrode pitch when two countering electrodes are needed on opposite sides of the spring-mass pair as shown in Figure 7.15.

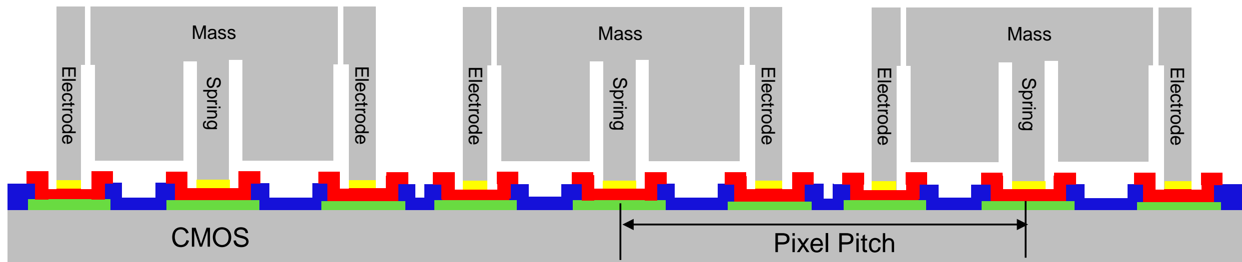


Fig 7.15. Minimum hair sensor pixel pitch is determined by the electrode layout and minimum achievable electrode pitch.

Instead of directly bonding to the exposed top metal bond pads, the electrical leads can be redistributed on the surface of the die outside the original pad region as shown in Figure 7.16 by a redistribution layer (RDL) [6]. It is an extra metal layer on a chip that makes the IO pads of an IC chip available in other locations. For example, when performing flip-chip bonding, this method can be applied to spread the contact points around the die so that solder balls can be applied and the stress of mounting can be spread.

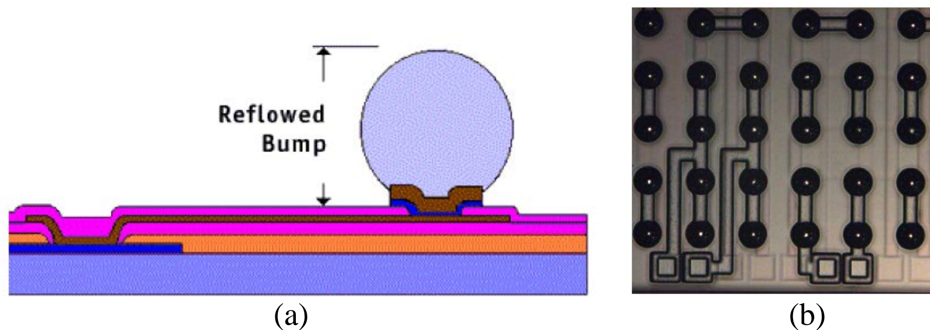


Fig 7.16. Bond Pad Redistribution Layers (RDL): (a) Polyimide dielectric layer is deposited and patterned to open bond pads while sealing fuse openings. Conductive metal layer connects old bond pads to new pad locations. The second layer of polyimide protects the metal trace. New bond pad location is opened for solder bumps reflow. (b) Optical image of old bond pads patterned with RDL and solder bumps. [6]

When applied to MEMS-CMOS stack integration, RDL helps with mapping the electrical leads on the MEMS die to the bond pad on the IC die. For example, as shown in Figure 7.17, the patterned metal can run over the passivation and bond to the hair springs. The minimum electrode pitch considering the topology and accumulated misalignment is about the same as in

Figures 7.12-7.14. Although Figure 7.17 shows the bonding site close to the IC bond pads to calculate the minimum electrode pitch, with the redistribution layer (RDL), we are provided with more flexibility in designing the locations of the CMOS-MEMS bonding sites.

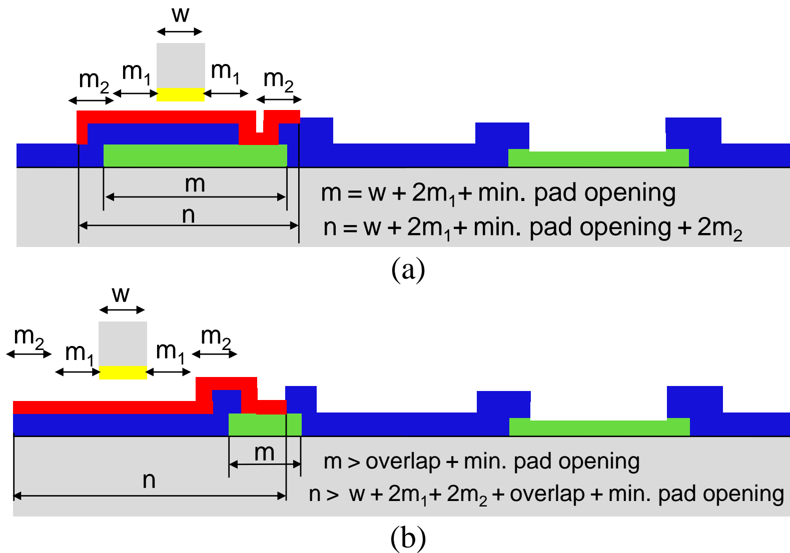


Fig 7.17. Patterned metal runs over the passivation and bond to the hair springs, similar to bond pad redistribution Layers (RDL) method.

Other than redistibution layers, interposers can also be designed as an intermediate substrate between IC chips and MEMS substrates. Integration with interposers is referred to as heterogenous integration method and usually involved a specially-desinged thin or thick substrates with through-silicon-vias (TSVs) [7-10]. It can lower the cost by dis-integrate different technologies: bond pitches in IC continue to decrease whereas the bond pitches in MEMS devices remains what it needs to be.

For our application, each hair sensor within the array have different footprint, ranging from several mirons, to several tens of microns, to several hundreds of mirons on the side. As shown in Figure 7.18, the interposer intermediate substrates assists mapping of MEMS devices' electircal leads to the finer-pitch IC chips. The overall chip size of the MEMS and CMOS chips can also be different.

In addition, the stringent alightment and surface topology requirements assiciated with direct interface between MEMS and CMOS chips can be released by the interposer substrates. Chemical mechanical posiishing (CMP) and wet etching create smooth and flat surface for bonding on both sides of the interposer substrates.

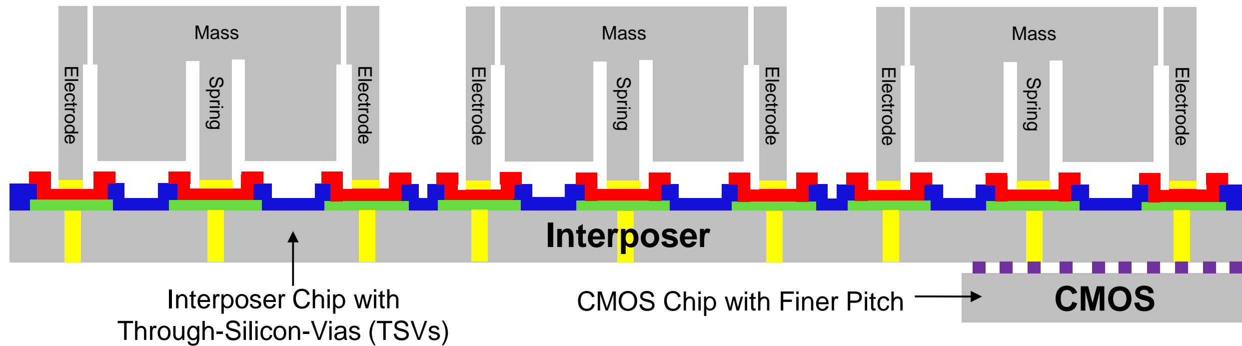


Fig 7.18. Heterogeneous integration with intermediate interposer substrates assists mapping of MEMS devices leads to the finer-pitch IC chips.

7.4 References

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Chapter 8 LOW-POWER WIDE-RANGE DIGITAL HAIR ACCELEROMETER AND ACCELEROMETER ARRAYS

For some applications of accelerometers such as airbag deployment and micro-relays, it requires that the sensors will switch states when a preset threshold level is detected. It is critical that the sensor system has high precision, fast response time, and reliability since human life is at stake. In addition, many autonomous platforms such as the micro air vehicles such as Quadrotors typically have many inertial sensors integrated for assisting simultaneous localization and mapping (SLAM) but have limited power supplies, which necessitates low power consumption of all the instruments and sensors onboard. Switch-mode operation also offers the ease of interface with the host microprocessor.

In this chapter, we introduce the digital threshold hair accelerometer array that can take advantage of the low noise and frequency selectivity nature of the hair structure and arrays. Low power consumption is realized by switching from capacitive sensing to switch-mode detection. This is extremely critical when we scale the sensor array size from less than 10 to 100s or 1000s.

8.1 Motivation

Compared to the many effort dedicated to measuring continuously varying acceleration, there are limited number of work on accelerometers measuring shock or threshold accelerations [1-6]. In contrast to the installation of a single device, threshold devices typically employ an

array of devices of various features (for example, geometrical dimensions) due to its digital nature.

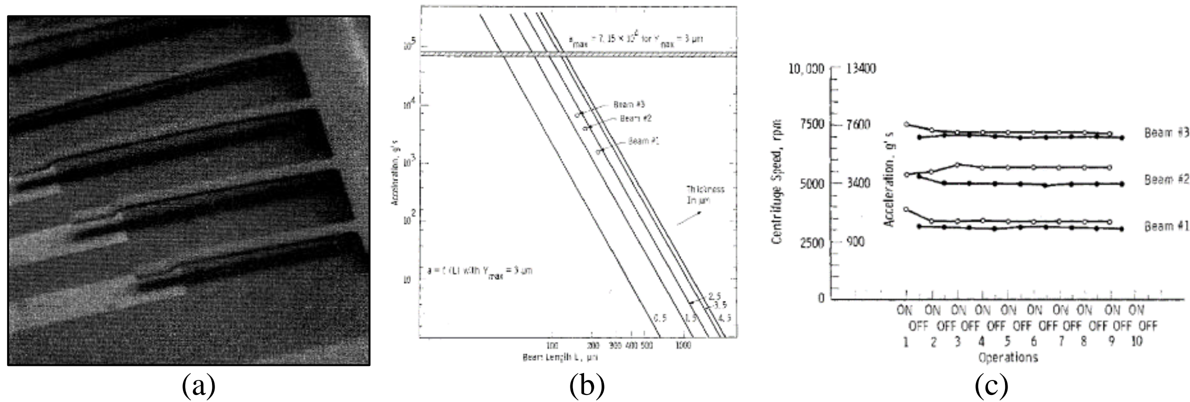


Fig. 8.1. Microminiature threshold accelerometers [2]: (a) SEM of a seven-cantilever module; (b) Design curves; and (c) Acceleration test results of a three-beam module accelerated in a 24-cm diameter biochemical centrifuge.

Earlier works on threshold accelerometers dates to the time when piezoresistive accelerometers were most widely adopted. Back in 1978, Peterson et al. [1] proposed arrays of electrostatically deflectable thin SiO_2 membranes for applications in light modulator arrays as well as in voltage controlled switches (>10^{10} cycle lifetime). Frobenius et al. [2] presented threshold accelerometers covering a wide range from few tens of g's up to 8000 g by constructing flexible metal beam and contact pairs as shown in Figure 8.1. The axis of inertia detection is in a direction normal to the contact plane. The temperature sensitivity of this device is merely the temperature coefficient of the modulus of elasticity for electroplated gold. Since the fabrication process is surface micromachining and the tip of beam deflection is given by $Y_{max} = 3\rho L^4 a/2Et^2$, the design strategy was to fix the gold beam thickness $t = 1.5$ µm as well as the tip deflection $Y_{max} = 3$ µm. The beam length L suffices to adjust the acceleration threshold levels. In addition, maximum bending stress σ_{max} in a beam is given by $\sigma_{max} = 3\rho L^2 a/\text{t}$. For a known material (E, σ_{max}, ρ) and maximum deflection Y_{max}, the maximum

obtainable acceleration level a_{max} will be $a_{max} = 1/6\ (E/\rho)\ (\sigma_{max}/E)^2(1/Y_{max})$. The upper limit for the acceleration threshold of the shortest beam (minimum L) turns out to be 7.15×10^4 g. The chip was tested in a 24-cm diameter biochemical centrifuge. As can be seen from Figure 8.1(c), after two operations the threshold values remained well within 2 %.

More recent works on threshold accelerometers aim to address one of the limiting factors in the state-of-the-art wireless world of Internet of Things (IoT): power consumption [4-5]. Since many sensors may be deployed in locations that may not have power available and will be operating on battery, minimizing power consumption is crucial in lowering the service costs and is directly affecting the dependability of the distributed sensor nodes.

Piezoelectric, piezoresistive and capacitive type MEMS accelerometers whether in academic or commercially available all require an analog front-end circuit to amplify and digitize the output (by an analog to digital converter). The power consumption for these chips are in the range of tens of μWatt to a few mWatt. For example, with a coin cell battery that has 200 mAh capacity and a nominal voltage supply of 1.5 V, for a sensor node that consumes 30 μW and relies on this 1.5 V supply, the battery can last slightly more than 1 year. At the same time, there has been aggressive power reduction in digital electronics, which makes most MEMS sensors one of the most power-hungry components in the integrated systems.

Table 8.1: Examples of battery type and leakage

Battery	I (leakage) A	I (sensor) A	I (total) A	Power (W)	Capacity (mAh)	Voltage (V)	Life Time (Year)
L92	1.10E-05	6.67E-09	1.10E-05	1.64E-05	1200	1.5	12.5
Alkaline	2.05E-06	6.67E-09	2.05E-06	3.09E-06	150	1.5	8.31

If sensor nodes' power consumption can be reduced to nW range, considering the characteristics of coin cell or AAA batteries for example, they can provide a lifetime of at least several years and limited only by self-discharge.

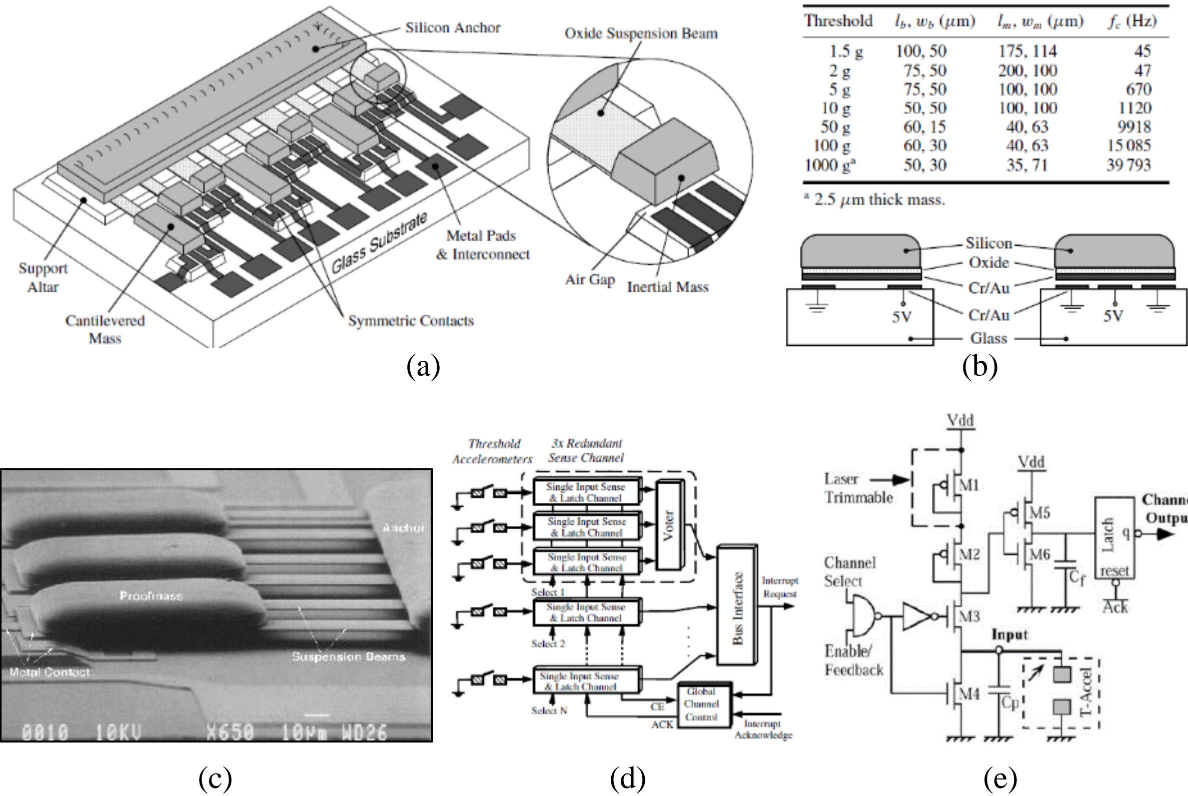


Fig. 8.2. Microminiature threshold accelerometers [4]: (a) Illustration of threshold acceleration sensors employing redundancy (three identical sets, each set containing three different thresholds); (b) Top: Threshold accelerometer designs and Bottom: Front view of the threshold switch: asymmetric pull down with double contact configuration vs. balanced pull down with triple contact layout with well-defined contact gap at 0.25 μm; (c) SEM micrograph of a triple array with threshold of 1.5 g with 100 μm long 25 μm wide and 0.75 μm thick oxide beams and 175 μm long, 114 μm wide and 15 μm thick inertial mass; (d) Functional circuit block diagram showing the input redundant channels and the logic voting of the majority function; (e) Schematic diagram of a sense channel.

Selvakumar et al. [4] presents a complete threshold acceleration detection microsystem comprising an array of threshold accelerometers and a low power interface circuit. A wide latitude in acceleration threshold levels from 1.5-1000g (with bandwidths of 45 Hz to 40 kHz

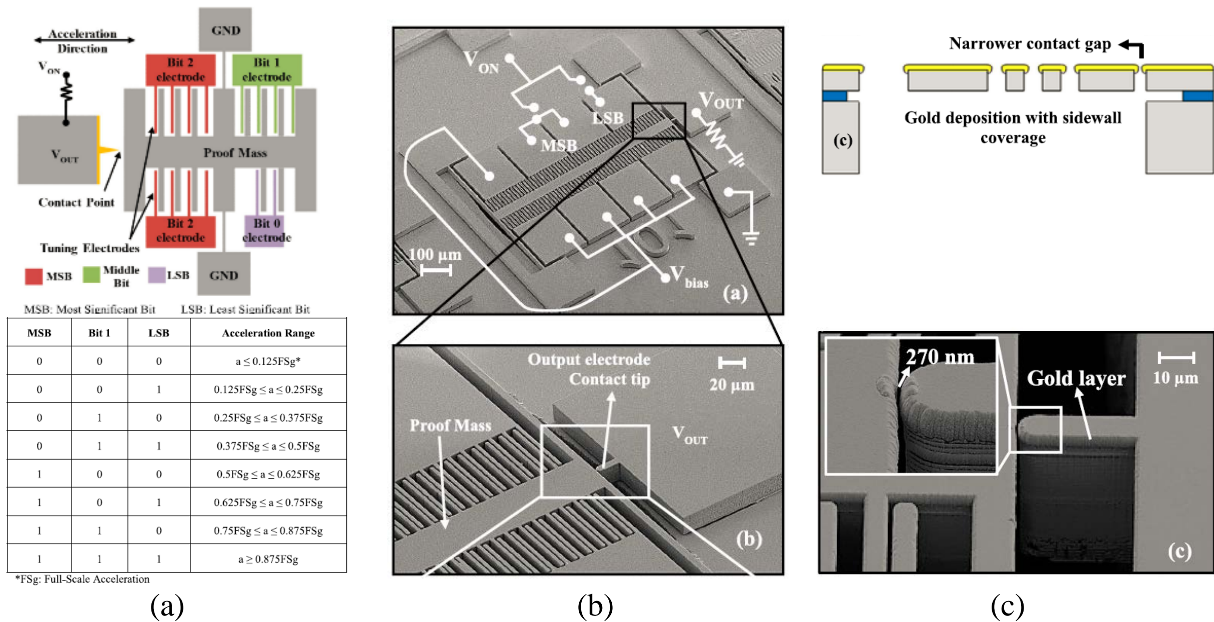
and mass sizes ranging from 0.015 μg to 0.7 μg) is demonstrated realized by the bulk-silicon dissolved-wafer process. The sensible axis is normal to the wafer/chip plane. Low-resistance gold–gold contacts are used for the switch. An upward acceleration greater than the threshold of the device causes a gold pad under the deflected mass to short the gold leads on the glass substrate. Referring to Figure 8.2, all beams are 0.75 μm thick and all mass are 15 μm thick except for the 1000 g device (2.5 μm thick). The separation between contacts is 0.25 μm. The contact gap is very well defined by using a 1.5 μm KOH recess that is eventually reduced to the design gap value by the metal and LPCVD oxide structural layers.

The interface circuit dissipates less than 300 μW by the circuit shown in Figure 8.2(e). A pull-up chain consisting of M1 and M2 for the channel input is designed to be weak in order to limit the current flow through the input switch. The input high-to-low transition is amplified by a CMOS inverter (M5–M6) and latched at the channel output. The ultra-low power operation of the interface is obtained by designing for virtually no static current flow in the circuitry, and using an asynchronous design approach. Most of the circuit blocks are digital CMOS, which do not draw static current. The power dissipation of the circuit designed to operate from a 5 V power supply was less than 10 μW from transient current flow during switching events. Higher reliability and fault tolerance is achieved by using channels with triple redundancy.

In the next seciton, we propose a circuit that implements the latch at the front end to further reduce the power consumption compared to Selvakumar [4]. The circuit is designed and simulated with 0.13 μm CMOC technology to achieved nano-Watt power cinsumption.

Another noteworthy work is presented by Kumar et al. [5] in 2016 that aims to significantly decrease the power consumption of digital accelerometers as shown in Figure 8.3. Instead of having an array of devices, this accelerometer chip consists of a single proof mass and

a number of parallel plate electrostatic actuators that can be turned on and off in a sequential manner by a digital controller. A simple 2-bit version of such accelerometers has been successfully fabricated and operated in the 0-1 g range. The same device concept and the configuration can be enhanced to higher number of bits.



MSB	Bit 1	LSB	Acceleration Range
0	0	0	a ≤ 0.125FSg*
0	0	1	0.125FSg ≤ a ≤ 0.25FSg
0	1	0	0.25FSg ≤ a ≤ 0.375FSg
0	1	1	0.375FSg ≤ a ≤ 0.5FSg
1	0	0	0.5FSg ≤ a ≤ 0.625FSg
1	0	1	0.625FSg ≤ a ≤ 0.75FSg
1	1	0	0.75FSg ≤ a ≤ 0.875FSg
1	1	1	a ≥ 0.875FSg

*FSg: Full-Scale Acceleration

(a) (b) (c)

Fig. 8.3. 3-bit digitally operated accelerometer [5]: (a) Mapping of the acceleration binary output; (b) SEM view a fabricated digital accelerometer also showing device electrical connections; (c) Zoomed-in side view of the gap between the proof mass and the output electrode showing the gap narrowed down by gold deposition.

Contact lithography and plasma etch constraints restrict the gap size between the proof mass and the metallic tip to ~1.5μm. They deposit a thick layer of gold with side wall coverage to reduce the gap sizes to as small as 270 nm. However, although the device was design to resolve 3-bit, some electrodes are used as tuning electrodes to set acceleration threshold limit to 1g. The applied the bias voltage is set to be 47.2V to further reduce the gap to ~12 nm to enable full-range at 1 g acceleration.

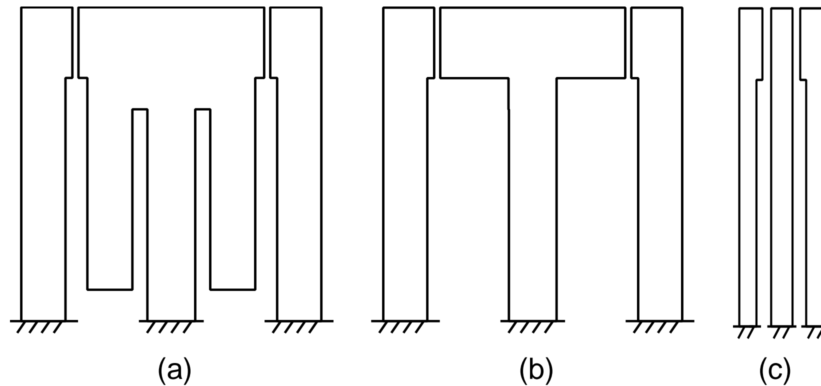
Like any other threshold acceleration switch, the device itself is a passive switch. They claimed 10.8 nW power consumption at 100Hz assuming the total capacitance to be charged up

to the system operating voltage at 5V and eventually depleted during each measurement cycle is 8.62 pF.

8.2 Digital Threshold Array Design Objectives

The threshold accelerometer arrays by Selvakumar et al. [4] covers a wider acceleration full-scale range (1.5-1000 g) and the single-device approach by Kumar et al. [5] achieves higher precision within 0-1 g.

In this research, we aim to achieve both large full-scale and high resolution across an array of devices. The threshold acceleration level is essentially a function of the proof-mass size (**m**), the spring constant of the vertical hair spring (k)**,** and the air-gap dimension separating the proof-mass and the two contact electrodes (**g_0**). By changing the design parameters, different threshold levels can be achieved for specific applications.



Lower-g threshold levels → Higher-g threshold levels

Structure	(a)	(a)	(c)
Fixed threshold gap (g_0)	4 μm		
Fixed spring width (c×d)	20 μm×20 μm		
Spring length (L)	600 μm	600 μm	1000 μm
Desired threshold levels	1 g	100 g	1000 g
Estimated proof-mass footprint (a×b)	~2 mm×2 mm	~200 μm×200 μm	~20-30 μm Spring is mass

Fig. 8.4. Different designs cover low-g to high-g threshold levels. Examples are given for fixed threshold gap and spring cross-sections, while adjusting the proof-mass footprint.

As shown in Figure 8.4, the two-gap process can easily define these structures with both small and large proof-mass with footprint from 20 μm on one side (the vertical hair spring being the proof-mass as shown in Figure 8.4(c)), to several millimeters on one side, which suffices to adjust the acceleration threshold levels. Further modulating the gap (**g_0**) to tune the threshold acceleration levels will be analyzed later. Without exceeding the maximum bending stress σ_{max} of the spring, for a known material (E, σ_{max}, ρ) and maximum deflection $Y_{max} = 4$ μm, the maximum obtainable acceleration levels from 1 g, 100 g to 1000 g for different proof-mass footprints are listed in Figure 8.4. Tradeoffs for a single device still exist: although a higher g-range is achieved, the noise also increases. In this chapter, we focus on the design, fabrication and characterization of low-noise arrays, but with a relatively smaller g-range.

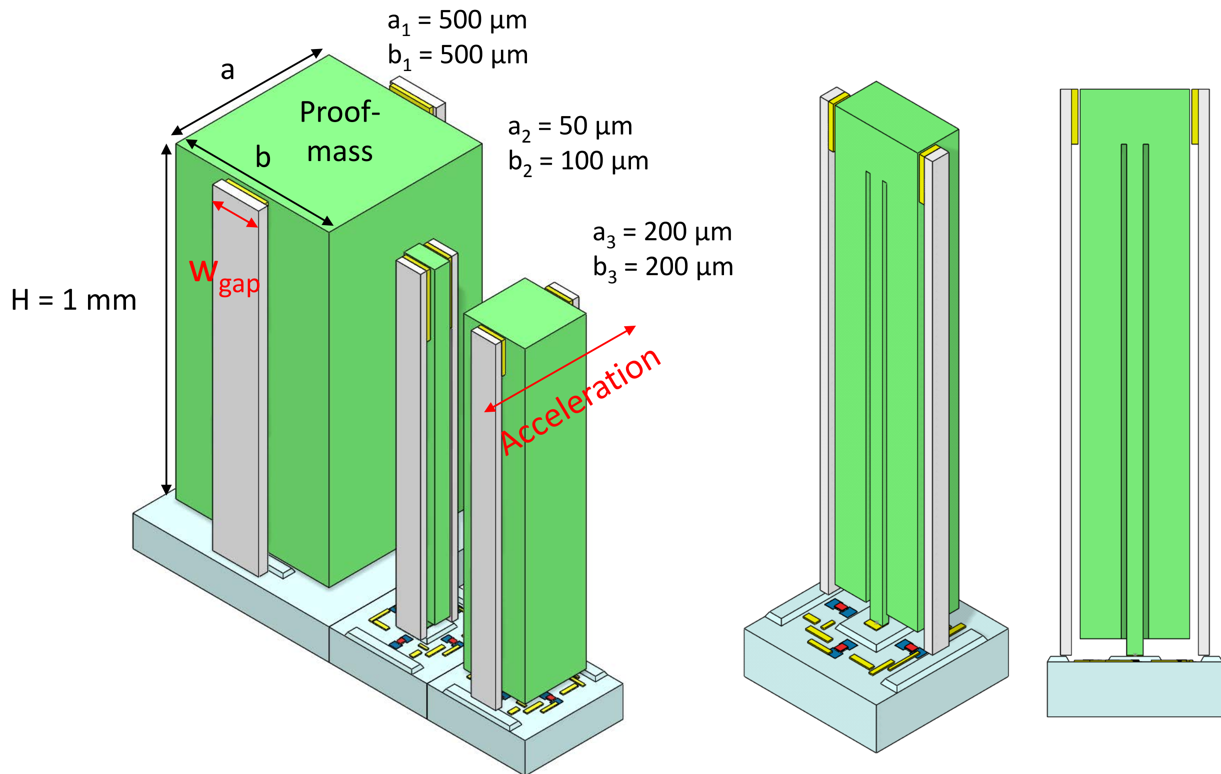


Fig. 8.5. Perspective drawing (showing three different threshold sensors each with different proof-mass dimensions), and cross-sectional views of a single sensing unit. The contact gap width w_{gap} can be designed small enough to reduce squeeze film air damping.

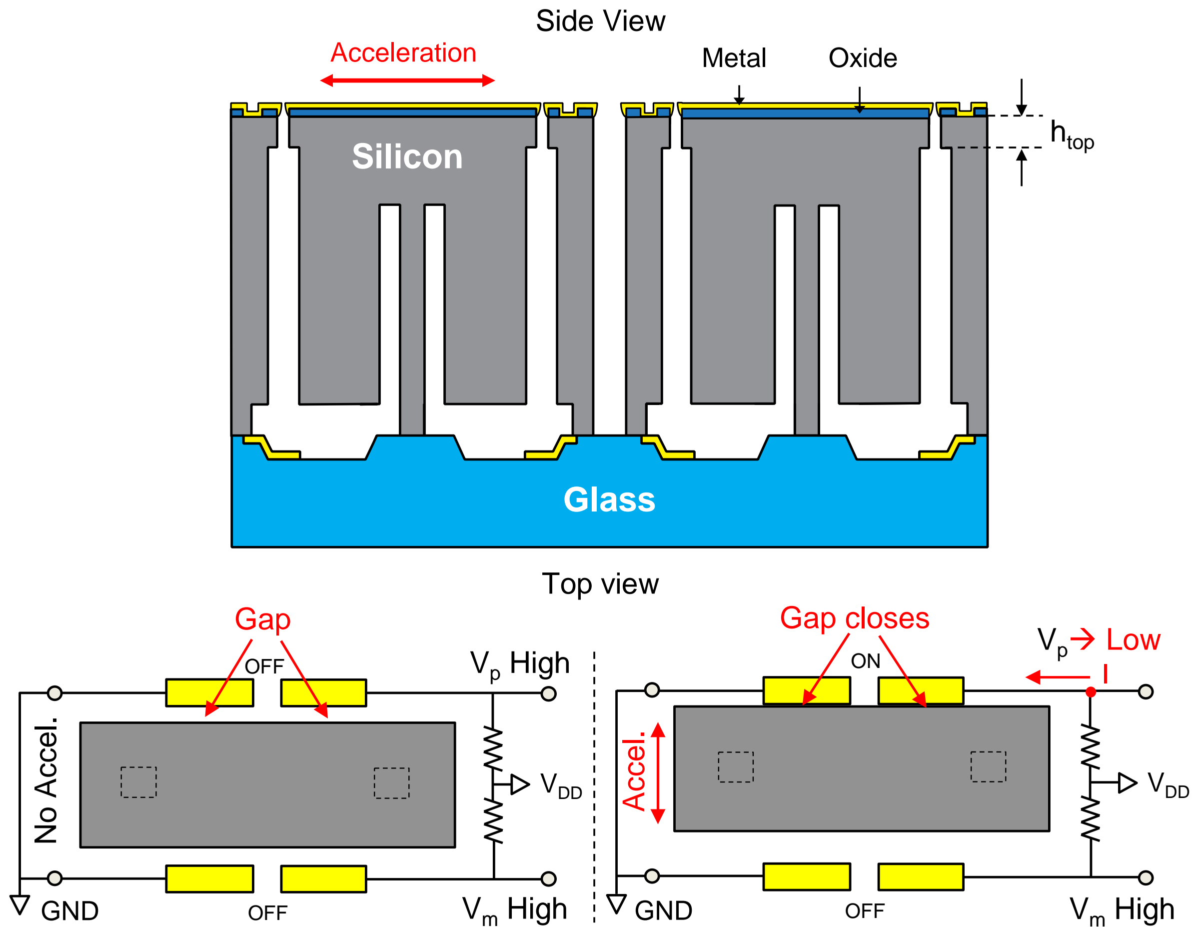
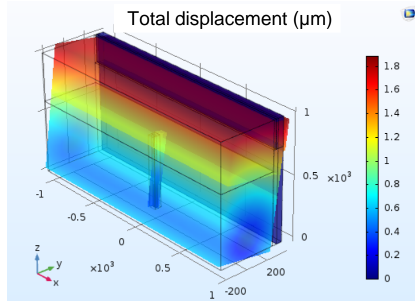


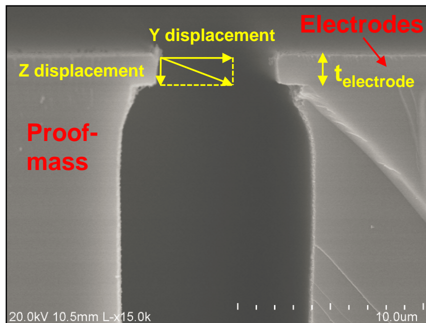
Fig. 8.6. Operation of threshold hair accelerometer: when the proof-mass travels toward the two electrodes and close the air gap due to external acceleration > threshold of the device, the metal on the proof-mass shorts the metal contacts on the two electrodes and closes a sensor circuit.

The threshold hair accelerometer is derived from the two-gap hair structure and consists of a tall and high aspect-ratio inertial mass. The tall inertial proof-mass is supported by one or two vertically anchored compliant spring. Two pair of electrodes are located along the sensitive axis of the spring-proof mass, and are separated from the proof-mass by an air-gap. As shown in Figure 8.6, when the proof-mass travels toward the two electrodes on the same side and close the air gap due to external acceleration greater than the threshold of the device, the metal on the proof-mass shorts the metal contacts on the two electrodes and closes a sensing circuit. This signal can be used as event trigger.



Single device with single spring	
Spring length L	600 μm
Spring width	20 μm x 30 μm
Mass footprint	2 mm x 500 μm
Mass height H	1 mm

@ Acceleration = 1g in Y-Axis → ΔZ / Max ΔY = 1: (3.4)



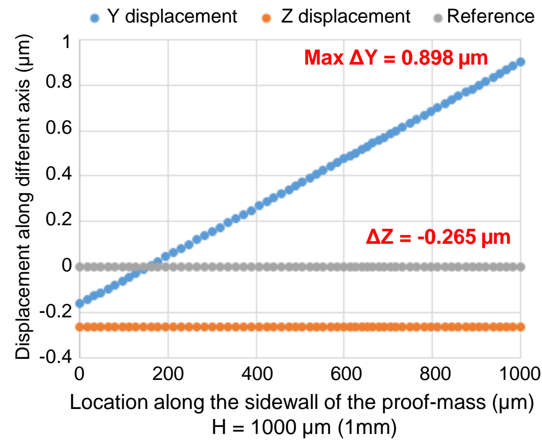


Fig. 8.7. COMSOL simulation of a device that consists of a 600 μm long and 20×30 μm2 wide spring that supports a 1 mm tall and 2 mm×500 μm footprint proof-mass under 1-g acceleration in the Y-axis. The height the electrodes in the Z-axis electrodes must be greater than 0.265 μm so that the proof-mass will make good contact with the stationary electrodes.

For example, as shown in Figure 8.7, a 600 μm long and 20 ×30 μm^2 wide spring supports a 1 mm tall and 2 mm×500 μm footprint proof-mass, 1-g acceleration in the sensitive axis (Y-axis) results in ΔY = 0.898 μm and ΔZ = -0.265 μm, with ΔY/ΔZ ≈ 3.4:1. The displacement filed in all three axes are shown in Figure 8.8. If this device is designed to have an air gap of 0.898 μm, the switch closes at 1-g acceleration. For this device, the height of the electrodes in the Z-axis $t_{electrodes}$ must be greater than 0.265 μm (since ΔZ = -0.265 μm) so that when the metal covered electrodes on the proof-mass will be able to not miss but and make good contact with the stationary electrodes. The ratio of ΔY/ ΔZ is approximately the ratio of the device height (H) and half of the proof-mass width (b/2), 2H/b. If the acceleration threshold is

desired to be 8-g, which means the sensing gap equals 7.148 μm (8×0.898 μm), the oxide/metal stack thickness must be at least 2.125 μm (7.148 μm divided by 3.4). The thickness of the electrodes is determined by the thickness of the oxide hard mask after the top-gap DRIE as well as the thickness of the metal stacks deposited on the top the oxide. Details on how we realize such precise control over the dimensions in microfabrication will be discussed in the next section.

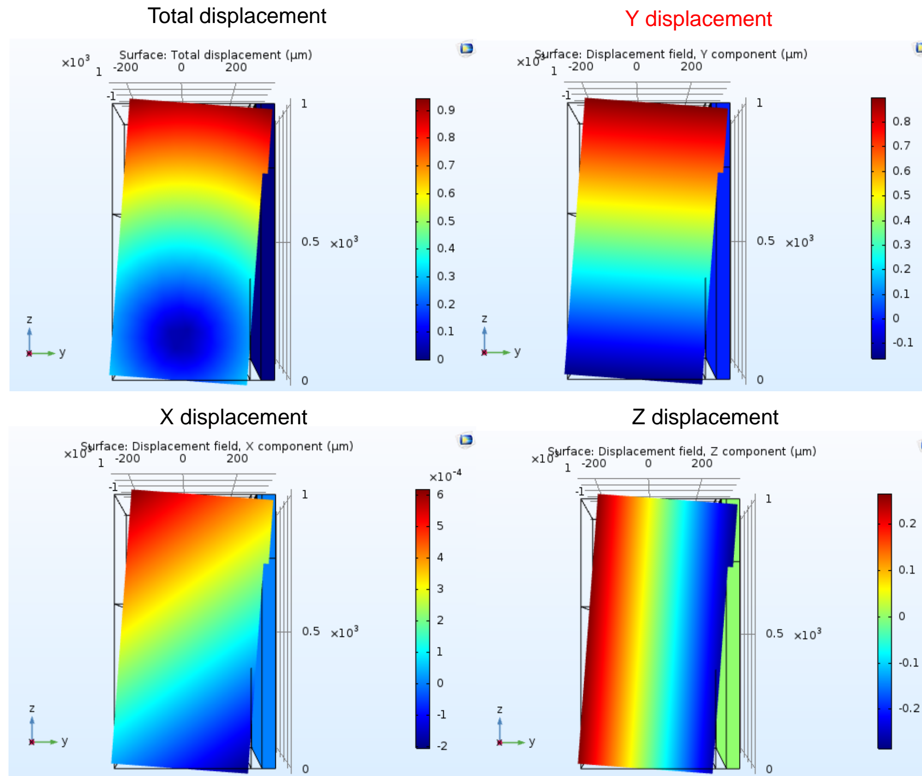


Fig. 8.8. Displacement filed in all three axes from the simulation in Fig.8.7.

An array of N devices can provide threshold acceleration detection resolution of $(a_{N-1} - a_0)/(N-1)$, or log_2N bit. The mass-spring can be modulated to cover different frequency spectrum and dynamic range. For example, an array of 4 (N = 4) devices that can resolve acceleration level from a_1 to a_4 by varying the air gap (Figure 8.9 (a)). The threshold acceleration detection resolution is $(a_3 - a_0)/(N-1)$. Similarly, an array of 32 devices having gap from 1 μm to 4.1 μm and Δgap = 0.1 μm can be constructed to cover 32 different threshold levels from a_0 to

$a_0 + 31\Delta a$ as shown in Figure 8.9 (b). By further varying the spring width (c & d), we can cover different range of threshold levels as well as different incremental acceleration levels that can be detected within the same array. The spring width ranges from 10×10 μm² to 30×30 μm², only limited by the bonding strength for mechanically anchoring the vertical hair spring.

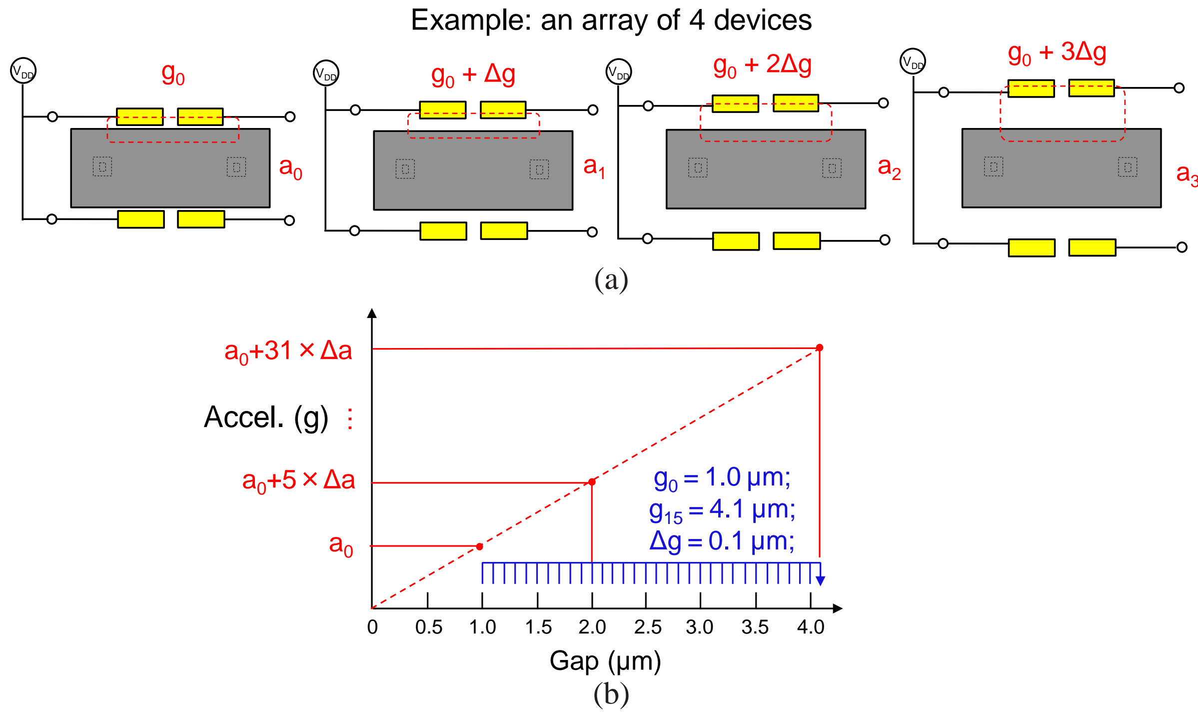


Fig. 8.9. Threshold hair accelerometer arrays: (a) an array of N=4 devices that can resolve acceleration level from a_0 to a_3 by varying the contact gaps; (b) 32 different threshold levels from a_0 to $a_0 + 31\Delta a$.

We layout two different chips with various proof-mass footprint and spring dimensions. The 16-array chip measures 4×0.5 mm² for each device: the gaps range from 1 μm to 4 μm with an increment of 0.2 μm. The 32-array chip measures 2×0.5 mm² for each device (Figure 8.10): the gaps range from 1 μm to 4.1 μm with an increment of 0.1 μm. The spring diameter ranges from 10×10 μm² to 30×30 μm², only limited by the bonding strength for mechanically anchoring the vertical hair spring. The design specifications for these two chips occupying total active chip area of less than 1 cm² are also summarized in Table 8.2.

The width (Wgap) and height (h_{top}) of the top small gap are 50 µm by 50 µm. Even with the minimum threshold gap of 1 µm, compared to the capacitive device in Chapter 6 with $W/g_0 = 2$ mm/2.5 µm, BNEA contributed by squeeze film damping can be reduced by 10 times since it is proportional to $(W/g_0)^{1.5}L^{0.5}$. For a device with 4×0.5 mm^2 footprint, the calculated BNEA is about 300 ng/√Hz, or 600 ng/√Hz per 1 mm^2 footprint of proof-mass.

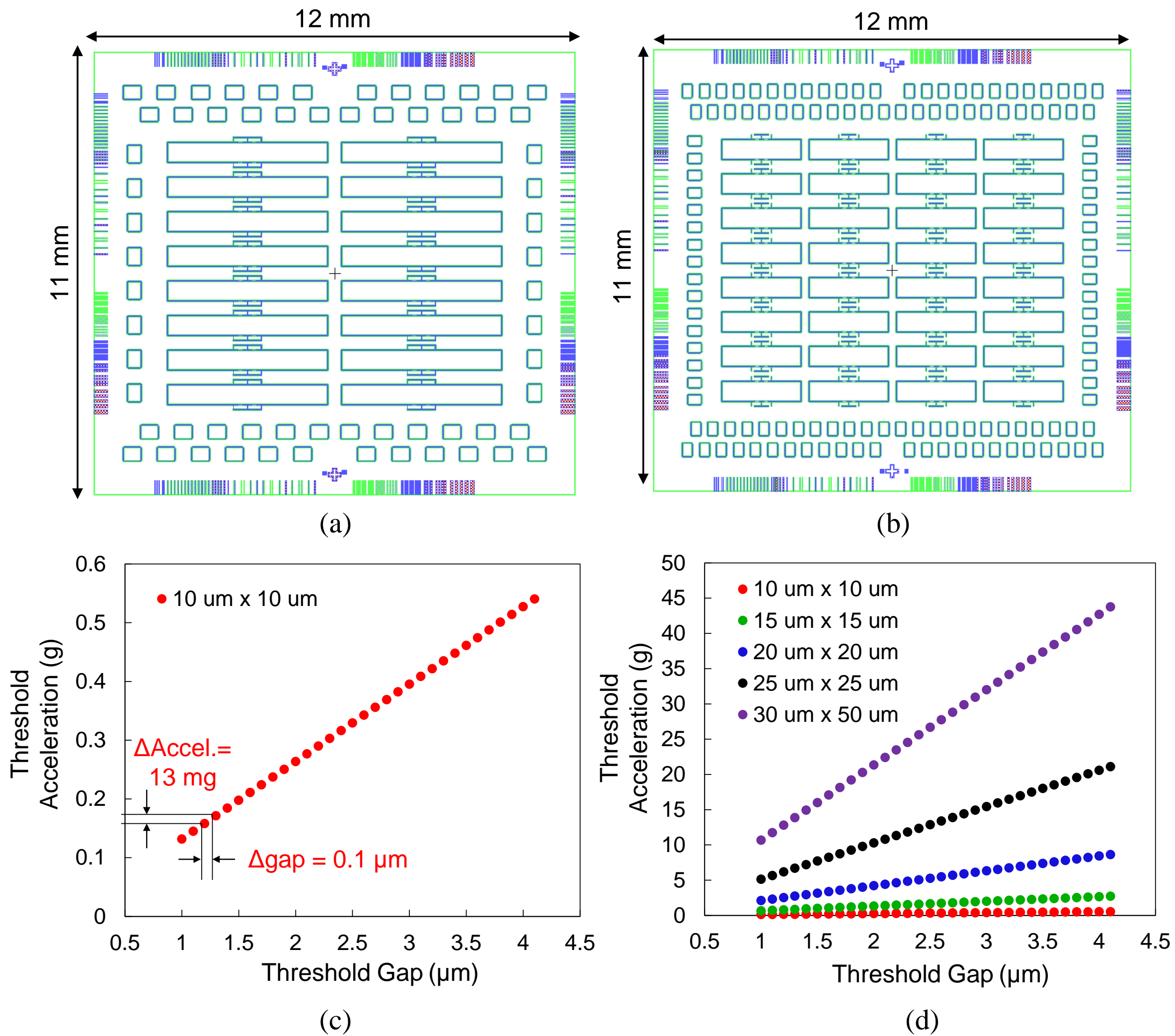


Fig. 8.10. (a) 16-array chip measures 4×0.5 mm^2 for each device; (b) 32-array chip measures 2×0.5 mm^2 for each device, with the same spring design within the same chip; (c)&(d) Threshold levels vs. gap and different spring designs for the 32-array chip: Increment gap $\Delta g = 0.1$ µm is equivalent to an increment acceleration $\Delta Accel = 13$ mg when the spring is 10 µm wide; and different threshold ranges realized by varying the spring dimensions.

Table 8.2: Design parameters and specifications of the 4×0.5 mm^2 and 2×0.5 mm^2 mass footprint threshold accelerometers layout in the 16- and 32-element arrays.

Proof-mass			Spring			Resonant Frequency	Displacement Sensitivity	Threshold @ gap = 1 µm
a	b	Mass	c	d	k			
mm	mm	µ-gram	µm	µm	N/m	Hz	µm/g	g
4	0.5	4.66	10	10	3.01	127.89	15.176	0.0659
2	0.5	2.33	10	10	3.01	180.87	7.588	0.132
4	0.5	4.66	15	15	15.23	287.77	2.998	0.334
2	0.5	2.33	15	15	15.23	406.96	1.499	0.667
4	0.5	4.66	20	20	48.15	511.58	0.948	1.054
2	0.5	2.33	20	20	48.15	723.49	0.474	2.109
4	0.5	4.66	25	25	117.55	799.35	0.389	2.574
2	0.5	2.33	25	25	117.55	1130.45	0.194	5.148
4	0.5	4.66	30	30	243.76	1150.56	0.187	5.347
2	0.5	2.33	30	30	243.76	1627.85	0.0937	10.69

- Device height H = 1 mm; Spring length L = 600 µm;
- Double spring: $k = 2k_0$;

8.3 Fabrication Process and Results

The sensor was fabricated using a modified silicon-on-glass (SOG) process combining the two-gap process presented in section V. SOG process is a well-studied and reliable process that allows for flexibility in the sensor design [12]. The air-gap dimensions are precisely defined by photolithography to suit different acceleration levels.

The process consists of six major steps as presented in Figure 8.11:

(a) A 4 µm recess is created in a highly-doped silicon wafer by deep reactive ion etching (DRIE). These recessed areas mainly suspend the proof-mass over the glass substrate so that when the proof-mass tilts toward the contact electrodes, the bottom of the proof-mass will not touch the bottom substrate. In addition, during the anodic bonding step, less mirrored charge will be built up when a large voltage is applied across silicon and glass. After the recessed is

formed, > 4.5 μm of LPCVD silicon oxide (SiO_2) is deposited. This oxide layer serves as the hard-mask against long DRIE during both the front-side and back-side etching. The front-side is the side that will be later be in contact with and be anodically bonded to the glass wafer. The oxide on the front-side is patterned to defined the boundaries of the vertical hair spring, the proof-mass and electrodes.

(b) A two-mask sequence is used to define the small sensing and switching gaps from the back-side of the silicon wafer from (a). The first mask is to be used with stepper lithography and it can resolve from <1 μm features to 1 μm features as the threshold switching gaps. Wherever the photoresist is exposed and developed, the oxide will be etched to expose the silicon. The thickness and selectivity of the photoresist is critical to precisely define the air gap openings. The second mask is to thin down the un-etched oxide from the initial 4.5 μm to 2 μm where contact needs to be made between the highly-doped silicon electrodes /proof-mass and the metal deposited on the very in step (f). The 2 μm should be thick enough to survive the back-side DRIE from the top on the silicon-glass wafer stack. Any residual oxide will be stripped by dry plasma etch after the devices are all release. The difference of 2.5 μm defines the contact electrodes thickness before metal is deposited. The oxide thickness being deposited and removed in this two-mask sequence needs to suit a range of gap dimensions.

(c) Deep, high aspect-ratio deep reactive ion etching (DRIE) masked by the front-side oxide. The etch depth are tuned by the different opening sizes as well as the total etch duration. After DRIE, the wafer is cleaned by oxygen plasma at 150 °C at 800 W followed by Piranha clean. The remaining front-side oxide hard mask is then removed by BHF while the back-side oxide mask is protected by hard-baked photoresist.

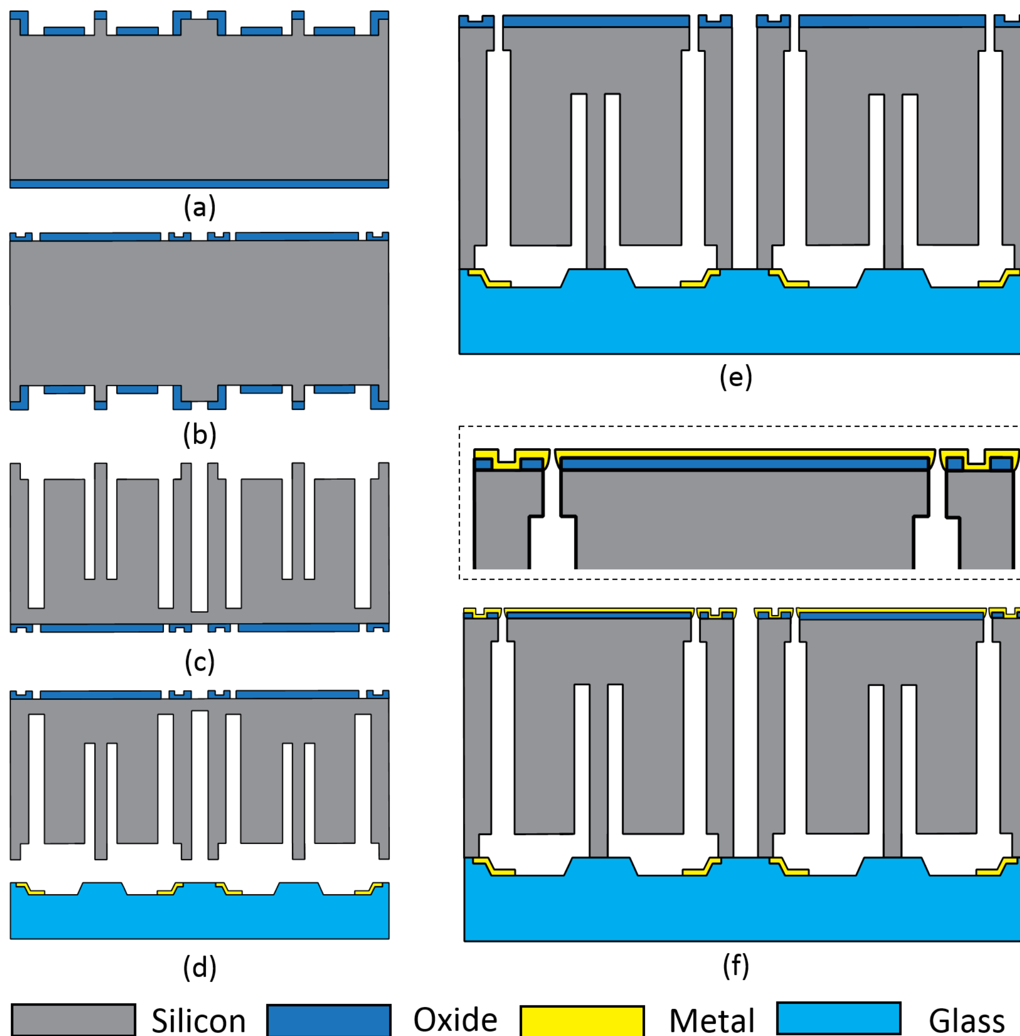


Fig. 8.11. Modified silicon-on-glass (SOG) process combining the two-gap process: (a) Recess formation and front-side DRIE hard mask patterning; (b) Two step back-side DRIE and contact pads hard mask patterning; (c) Front-side deep high aspect-ratio DRIE; (d) Recess formation and metal lift-off on glass wafer, followed by anodic bonding of the silicon wafer and the glass wafer; (e) Small top gap DRIE to release the proof-mass; (f) Blanket metal evaporation for electrical contact.

(d) The next two steps are carried out on the glass substrate. The first step is to etch recess on the glass surface by 3 µm except in the anchoring and contact regions by BHF wet etching. This further reduces the squeeze-film damping between the inertial proof-mass and the glass substrate. After that, photoresist is patterned to lift off and evaporate Titanium/Platinum (200/1500 Å) stack

as contact fingers as well as routings on the glass substrate. Before the deposition, 1000 Å recess is further wet etched by BHF to allow for this thick stack of metal, while not compromising anodic bonding quality. The second step is anodic bonding: the processed silicon and glass wafers are aligned and electrostatically bonded together at 400 °C at 1500 V.

(e) After the 4-inch wafer stack (1 mm silicon + 500 μm glass) are diced 1 mm deep from the glass slide, the stack is mounted on a carrier wafer and the final DRIE is performed. This etch defines the small gaps from the top. The oxide mask defined in step (b) ensures that oxide hard mask remains after the release DRIE and serves to more precisely define the threshold air gaps.

(f) The final metallization consists of two angled metal evaporation runs to ensure good coverage of metal on the vertical contact planes of the >2 μm thick oxide on top of both the proof-mass and electrodes. Each time 5000 Å metal is deposited thus the electrodes stack height will be increased by 1 μm.

Figure 8.12 and 8.13 presented partial view and overall chip view SEM of fabricated threshold hair accelerometer arrays. The charging effects in SEM indicates that all the devices are released.

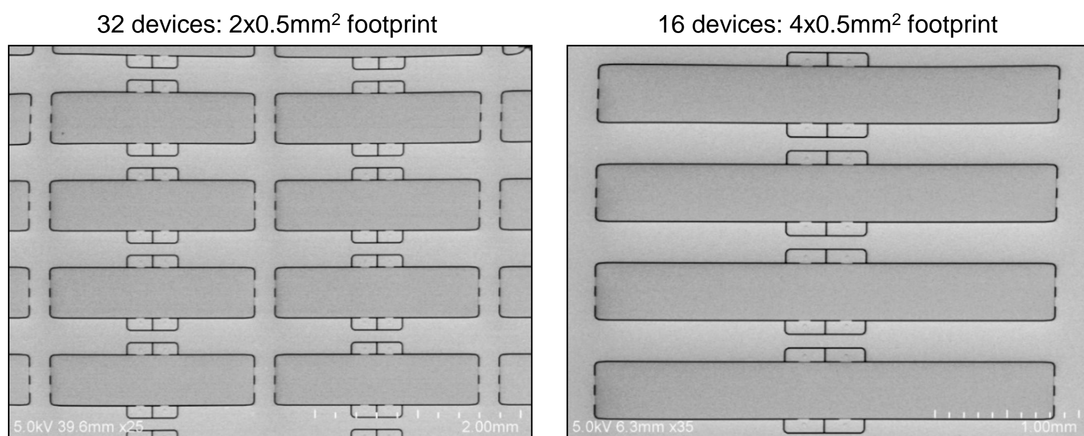


Fig. 8.12. SEM of fabricated threshold hair accelerometer arrays: partial view.

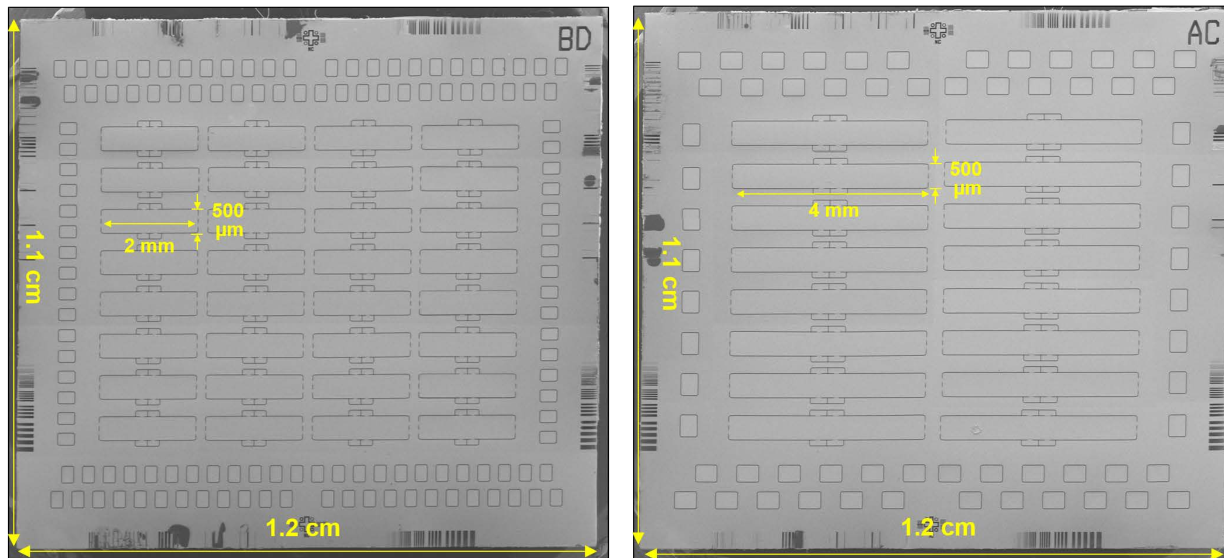


Fig. 8.13. SEM of fabricated threshold hair accelerometer arrays: chip overview of 32 element array and 16 element array.

8.3.1 Release DRIE

One of the common process issues involved in microelectromechanical system (MEMS) devices release by plasma etch such as DRIE is severe silicon undercut caused by overheating of suspended microstructures [13]. For capacitive devices, small transduction gaps (parallel-plate capacitors or comb fingers) normal to the silicon wafer planes are typically defined by DRIE, thus yielding large sensing and actuation areas if thick single crystal silicon wafers are used. Electrical isolation between electrodes at different potentials may also be etched simultaneously. Large proof-mass for higher sensitivity are usually supported by silicon beams defined using the same DRIE step that creates the sensing gaps, or by thin-film isolation beams defined by isotropic silicon undercut etching. As a result, the gap between sensing plates will be increased, the proof-mass boundary will be etched, and the support springs will be thinned, which decreases sensing capacitance, reduces proof-mass size, and decrease the spring constant in an unpredictable manner.

Over-etching is necessary to ensure electrical as well as mechanical isolation. However, lateral etch cannot be avoided: rapid silicon lateral undercut occurs after most of the suspended structures are etched-through. According to Equation 8.1 undercut is mainly attributed to the rapid temperature rise on the suspended MEMS structures: as temperature T rises the surface reaction rate also rises.

$$r \propto A \times T^{\frac{1}{2}} \times \exp\left(-\frac{E}{kT}\right) \qquad (8.1)$$

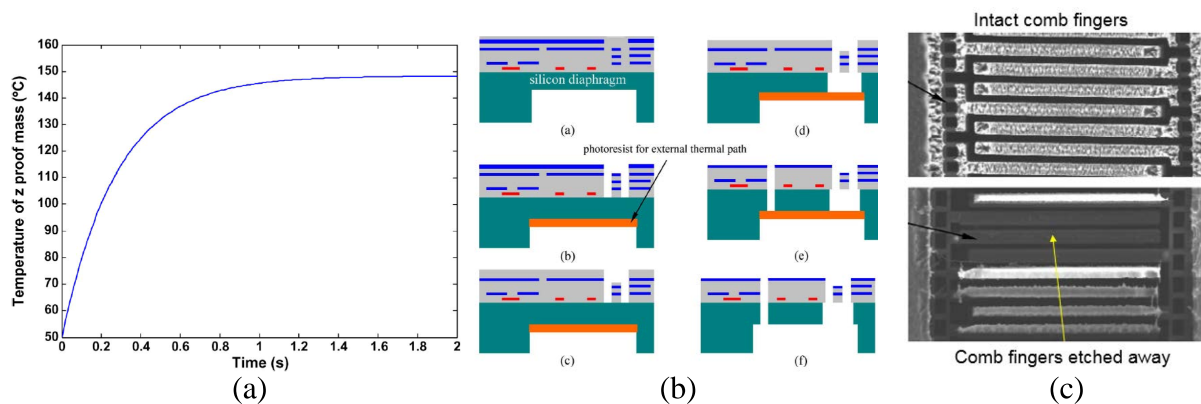


Fig. 8.14. Solutions to reduce lateral undercut caused by overheating of released microstructure [13]: (a) Calculated temperature rise on z proof mass: in less than 1s, the temperature is increased by 100 °C; (b) Modified process flow to include 10 μm PR coating on the backside of processed wafer before the final release DRIE. This reduces the thermal resistance when the proof-mass is almost released; (c) Comparison between backside-coated and uncoated samples showing the intact and etched-away.

The energy influx of ions is considered the major source that causes the substrate temperature rise: the kinetic energy of the impinging ions will convert to heat completely. Thus, the key is to estimate the temperature of the suspended microstructures. Qu et al. [13] calculated that in less than 1 s, the temperature of their z proof-mass design is increased by 100 °C, assuming the microstructure is assumed to be approximately 50 °C before release (Figure 8.14). They modified the accelerometer fabrication process to include photoresist (PR) coating step on backside of the wafer. The thick PR reduces the overall thermal resistance by almost 60 times.

10 μm AZ 9260 photoresist with thermal conductivity of 0.2 W/mK. By using backside photoresist coating, the release of the sensing fingers is well controlled with slight footing effect without being etched away (Figure 8.14 (c)).

In our case, due to the trenches being high-aspect ratio as well as the bonded silicon-glass wafer stack, it is not feasible to apply backside PR coating directly in contact with the features being etched to reduce the thermal resistivity.

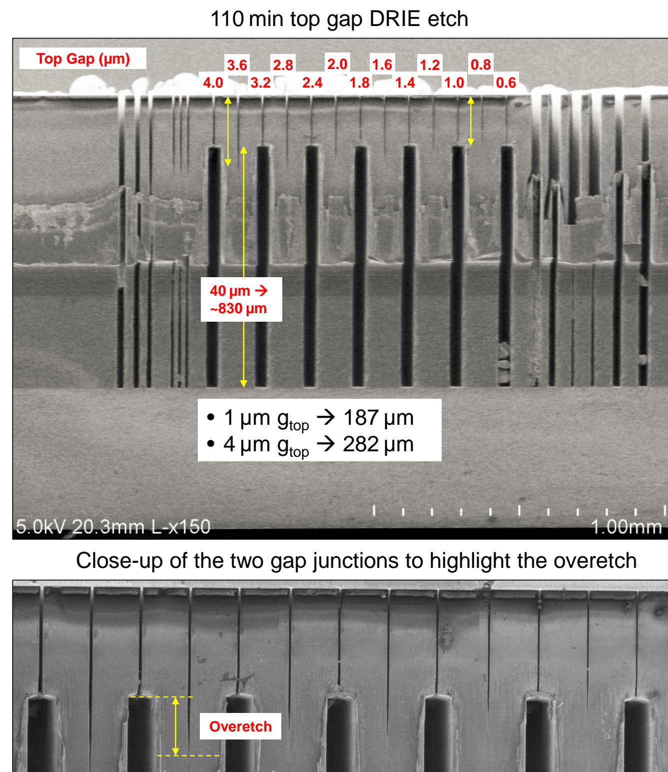


Fig. 8.15. Junctions of the top and bottom gaps: 40 μm wide bottom gaps connect with top gaps from 1-4 μm. The 4 μm top gap is etched pass the height of the 40 μm gaps.

The main challenge lies in the different threshold gaps designed for different threshold acceleration levels. As shown in Figure 8.15, for top gap sizes from 1 to 4 μm and bottom gap sizes of 40 μm etched to 830 μm, 110 min ramped-parameter DRIE over-etches the 4 μm gaps by over 50 %, which means the 4 μm threshold gap devices are released much earlier than the 1 μm threshold gap devices. This is caused by DRIE lag: larger features etch deeper than smaller

features with a fixed etch duration. The ramped-parameter recipe was design to etch small trenches with high aspect-ratio, however, lag-free DRIE is not achievable. In addition, there will be etch rate variations across one wafer.

When the proof-mass is already released, it will only be supported by one or two vertical hair spring(s) to the glass substrate: undercut right underneath the oxide hard mask can be seen in the optical images (Figure 8.16) since the etch needs to continue to ensure the release of all devices. The undercut is more than 60 μm maximum. The oxide mask is rigid and does not collapse.

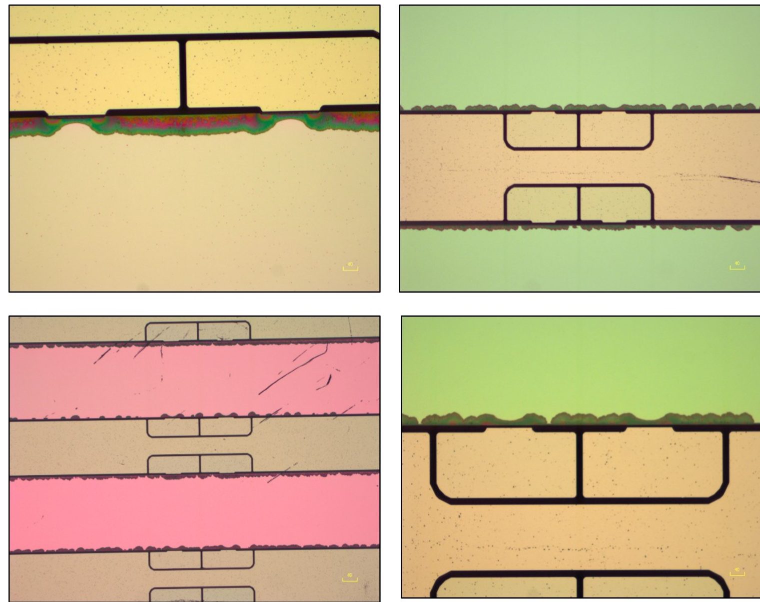


Fig. 8.16. Overetch creates large undercut due to overheating of the suspended structures.

Since we cannot entirely compensate for DRIE lag and undercut, the better option is to use the remaining oxide hard mask to more precisely define the contact threshold gap. However, DRIE undercut should still be reduced as much as possible. In the layout, we add dummy gaps $g_{dummy} = g_{minimum}$ to each device in order to delay the release of the devices with larger threshold gaps. For example, if the threshold gaps across an array is from 1-4 μm, then $g_{dummy} = 1\ \mu m$. Arranging the dummy gaps along the sensitive axis will limit the motion of the

proof-mass as shown in Figure 8.17 (a) (left). In this design, we place the dummy gaps along the axis normal to the sensitive axis as shown in Figure 8.17 (a) (right) so that g_{dummy} can match the minimum gap across the array as well as be much smaller than g_{sense}. After metal deposition, both the dummy gaps and sense gaps are very smooth.

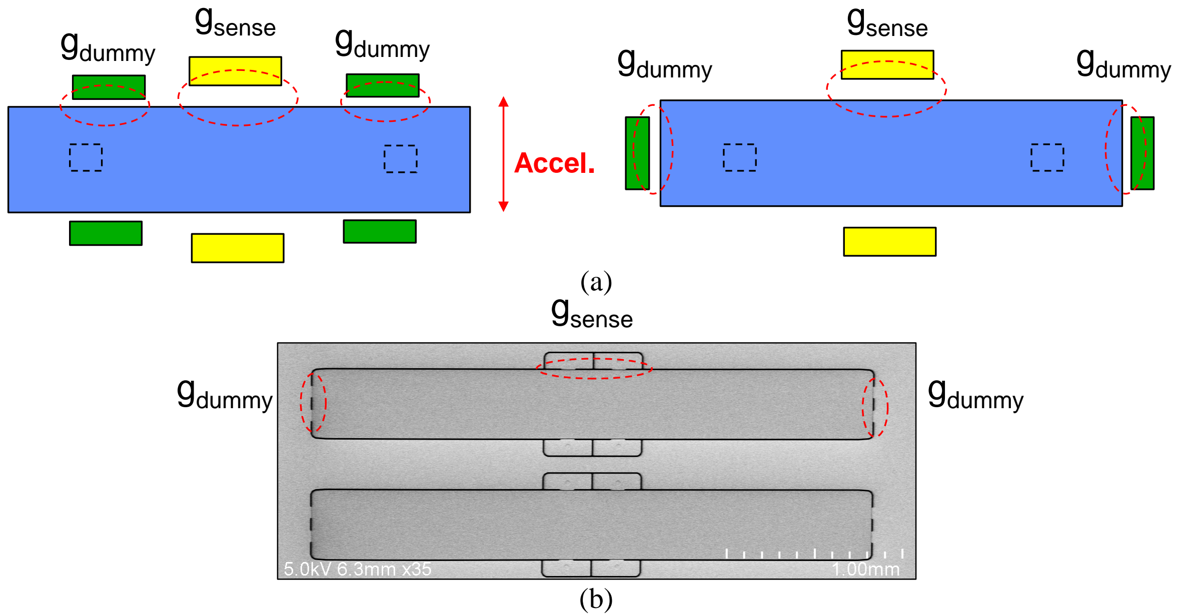


Fig. 8.17. Add dummy gaps to delay the release of devices with larger threshold gaps: (a) The dummy gaps are located along an axis perpendicular to the sensitive axis such that they do not limit the motion of the proof-mass; (b) Fabrication results of the devices with dummy gaps after top metal deposition.

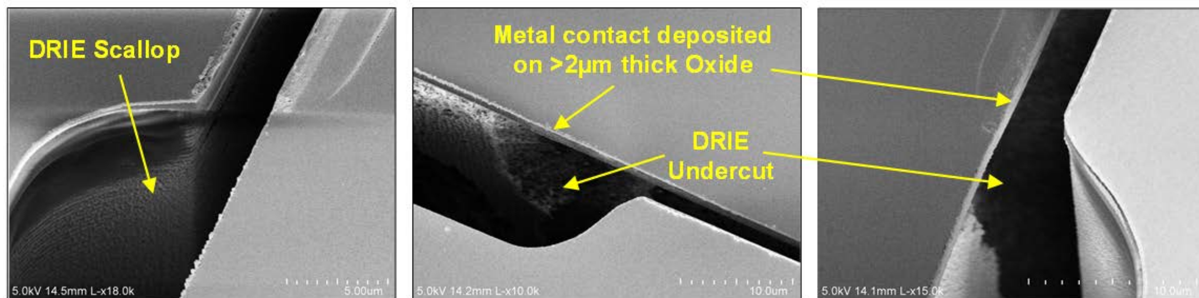
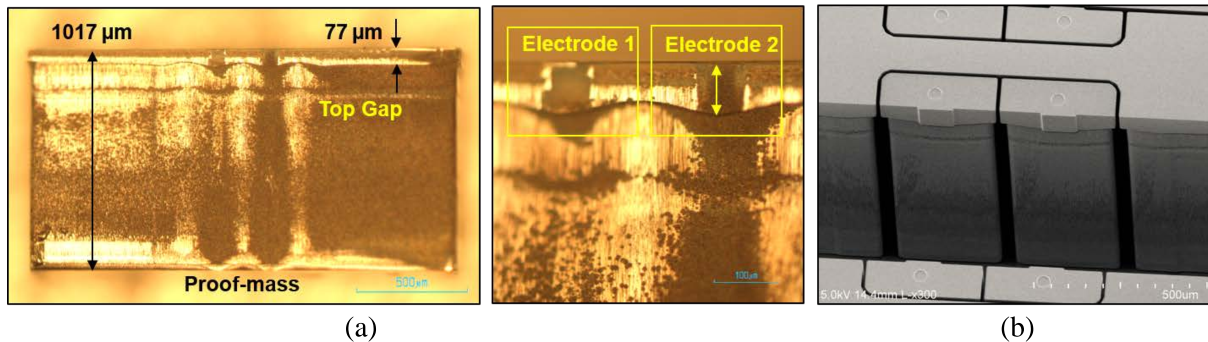


Fig. 8.18. DRIE scallop and DRIE undercut right underneath the > 2 µm thick oxide hard mask left after the release DRIE.

Undercut still exist but it will not affect the operation of the threshold devices. Figure 8.18 shows the DRIE scallop and DRIE undercut right underneath the >2 µm thick oxide hard mask left.

The overall small-gap etch time is reduced from 110 min to 50 min. This means the deep gap by front-side DRIE needs to by deeper than 900 µm, which is more challenging. Figure 8.19(a) shows optical images of the DRIE-ed sidewall of the released proof-mass: the top gap measures 77-84 µm due to DRIE non-uniformity caused by pattern geometry and density. The darker brown color in the images, especially at the electrodes location, indicates DRIE undercut caused by the overheating of the proof-mass when the proof-mass is mostly released. SEM of the electrode (Figure 8.19 (b)) proves that the device is cleaned very well and free of residues from DRIE or wet chemical cleaning steps.



(a) (b)

Fig. 8.19. Optical images of the DRIE-ed sidewall of the proof-mass: the top gap measures 77-84 µm due to DRIE non-uniformity caused by pattern geometry and density. The darker brown color in the images, especially at the electrodes location, indicates DRIE undercut caused by overheating of the proof-mass when the proof-mass is mostly released.

After the final metal evaporation, the threshold gap dimensions are measured by SEM to verify the gap dimensions. The 1 µm gap originally defined on the layout increases to 1.43 µm, and the 4 µm gap originally defined on the layout increases to 4.32 µm as highlighted in Figure 8.20. The smooth edge/sidewall of the oxide hard mask left after the small-gap DRIE

ensures good contact between the metal thin-films deposited on the electrodes and the proof-mass as shown in Figure 8.21.

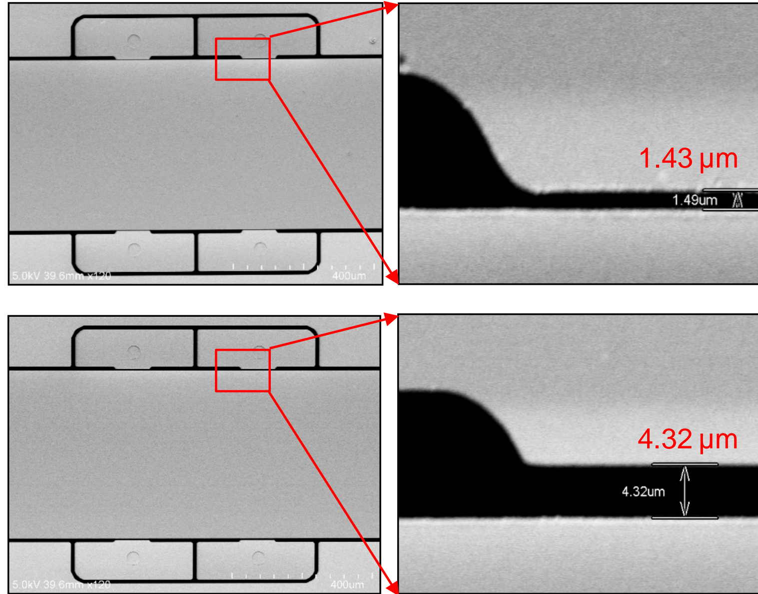


Fig. 8.20. Gap dimension after bonding, release DRIE and metal deposition: 1 μm gap originally defined on the layout increases to 1.43 μm, and the 4 μm gap originally defined on the layout increases to 4.32 μm.

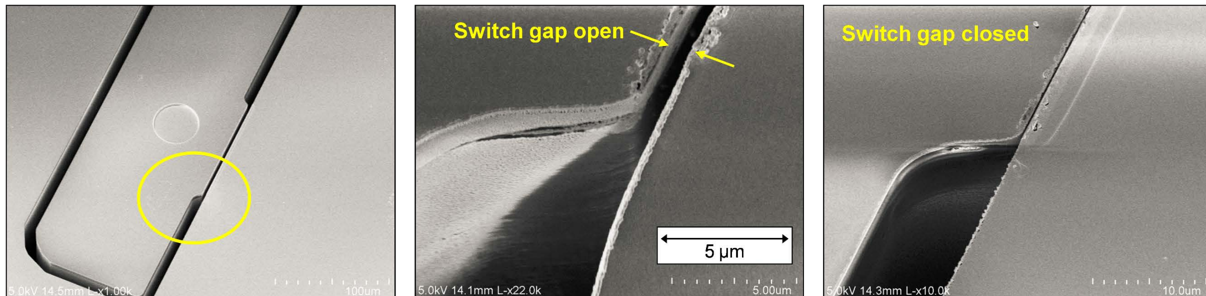


Fig. 8.21. Gap open and gap closed.

8.3.2 Silicon-Glass Anodic Bonding Quality and Strength

The other major challenge of the process lies in anodic bonding with small bonding area. Compared to capacitive hair accelerometers, the proof-mass supported by the hair spring does not need to be connected electrically to a certain potential, thus no metal fingers are sandwiched between the bottom of the vertical silicon hair spring and the islands on the glass substrate as

with the uniform gap capacitive devices by SOG process in section IV. Reliable bonding was only achieved for spring cross-section greater than 30 × 30 μm^2 when metal fingers are present.

In this design, the minimum spring cross-section area we experiment with is 15 × 15 μm^2, and the maximum spring cross-section area we experiment with is 30 × 30 μm^2. We pre-bond by applying -500 V at 250 °C for 30 minutes. Then we perform the second bonding step by applying -1300 V at 350 °C. After the second bonding step is complete, we anneal the wafers at 350 °C for 1.5 hours and slowly ramp down to room temperature over 2 hours. Pyrex glass has a similar CTE to silicon in the temperature range up to 400 °C.

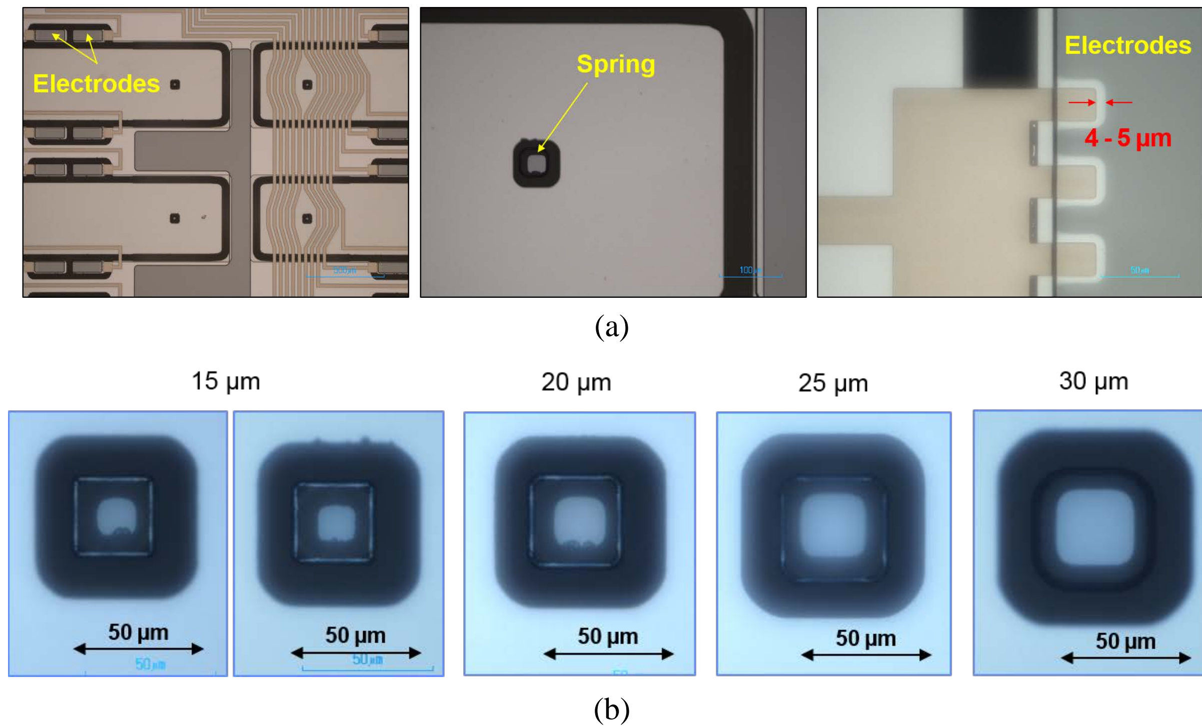


Fig. 8.22. After anodic bonding: (a) Dark grey color in the larger bonding areas, electrodes and hair spring locations all indicate good anodic-bonding quality. (b) Silicon springs of different cross-section areas are all in good contact and are bonded well to the glass substrate.

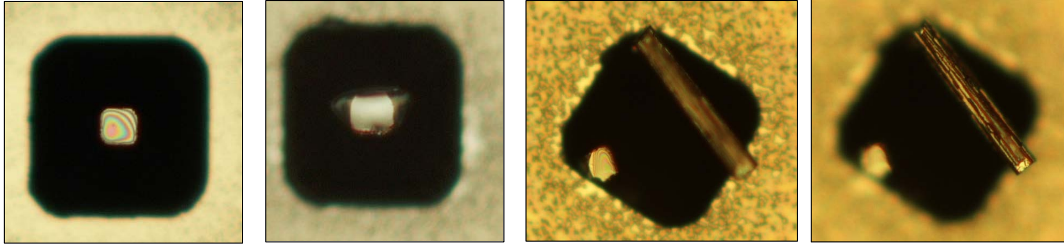
Figure 8.22 optically analyze the anodic bonding quality. The darker grey color indicates very good bonding quality. Both the silicon and glass surfaces are free of particles thanks to the thorough cleaning process before bonding. The silicon electrodes are bonded to the glass

substrate that is patterned with metal fingers. Shallow metal recess (>1500 Å) is etched by BHF before 2000 Å thick metal stack is evaporated so that the silicon electrodes can make good contact with the glass substrate. Variation of the etch rate of glass in BHF caused by lack of circulation of etchant or other factors may result in the final metal thickness breaching the surface being in the range of 400-600 Å. As shown in Figure 8.22 (a), rings of un-bonded regions of finite width can be seen at the edges of the metal fingers. They extended about 4 - 5 μm from the edge of the metal deposited until the two sides make good contact and are well-bonded. This distance may be reduced by more precisely controlling the metal thickness breaching the glass surface to less than 100 Å such that the un-bonded ring width can be less than 1 μm. Without metal fingers, the silicon springs of different cross-section areas are all in good contact and are bonded well to the glass substrate.

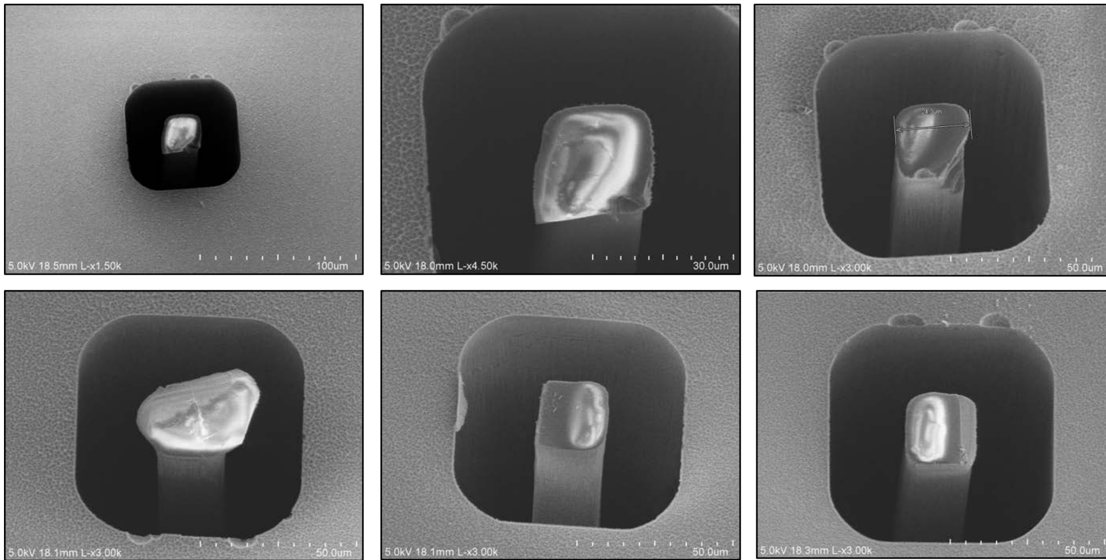
After the devices are bonded and released, the hair spring-mass could be broken to analyze the bonding interface. Chunks of glass attached to the silicon spring are verified by both SEM and optical images for hair springs of different diameters. The 15 μm wide springs sometimes not only got pull off from the substrate, they also broke in the middle (Figure 8.23) since they are very compliant (k <10 N/m) and large proof-masses are attached. The sidewalls of the vertical springs are not very smooth after deep DRIE and may also cause the spring to break more easily.

The glass fringe is good indication of descent anodic-bonding quality since typical bond strength of anodic bonding is higher than the tensile strength of glass before it fractures. The tensile strength of Borosilicate (Pyrex 7740) Glass could vary considerably about a mean value commonly found to occur at about 6.9 MPa (1000 psi). The lack of ductility of glass prevents the equalization of stresses at local irregularities or flaws.

15 μm hair spring: glass pieces on top of the detached silicon spring



25 μm hair spring: glass pieces on top of the detached silicon spring
Glass charged up in SEM



30 μm hair spring: glass pieces on top of the detached silicon spring

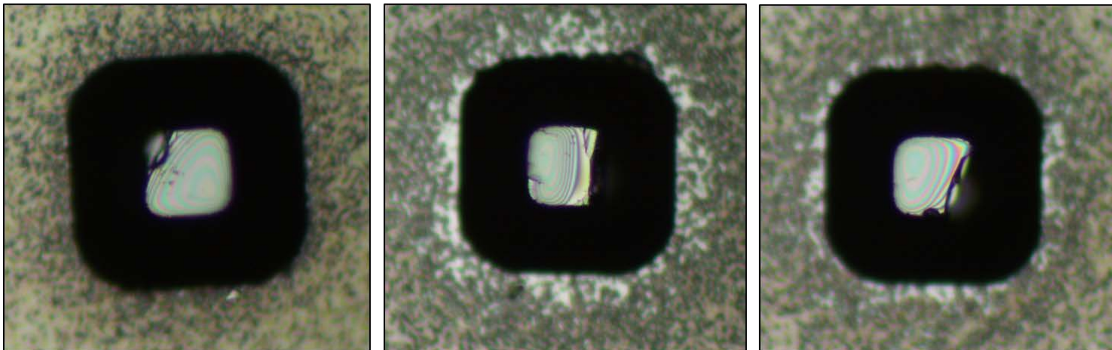


Fig. 8.23. Anodic bonding fracture morphology analyzed after the released hair spring-mass pairs are broken off from the glass substrate. Chunks of glass attached to the silicon spring are verified by both SEM and optical images, indicating good initial anodic bonding quality.

8.4 Electromechanical Testing Results

The fabricated threshold hair accelerometer array chip is glued and wire-bonded to a PCB. The PCB is mounted on Ulholtz-Dikkie voice coil shaker table for electromechanical testing of the threshold accelerometer arrays as shown in Figure 8.24. Each accelerometer in the array has four electrodes accessible, two for the positive axis and two for the negative axis.

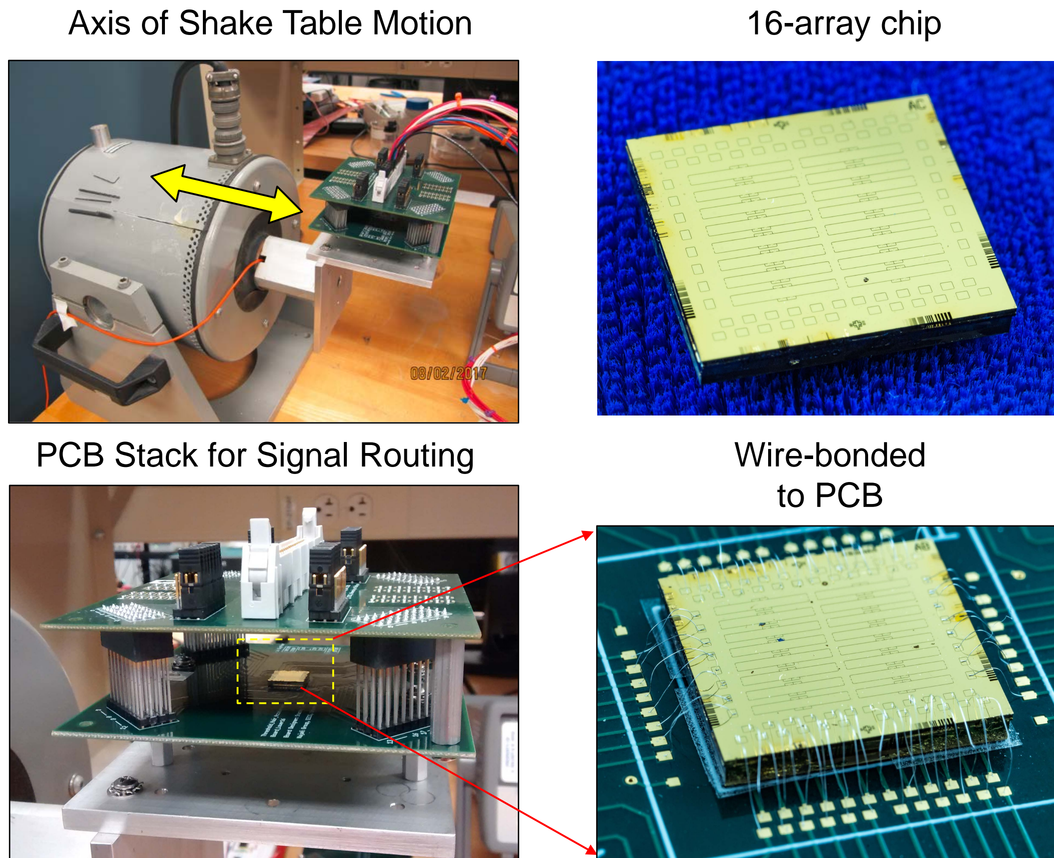


Fig. 8.24. PCB mounted on Ulholtz-Dikkie voice coil shaker table for electromechanical testing of the threshold accelerometer arrays. The sensor chip is glued and wire-bonded to the PCB.

For analog readout, each acceleration acts as a switch. The output ports V_{p_out} and V_{m_out} are initially charged to V_{DD} through a bias resistor as shown in Figure 8.25. When one of the switches is closed due to external acceleration, V_{p_out} or V_{m_out} will be pulled down through a discharging path. The resistor should be large enough to limit the current passing through the switch when it is on. Resistance welding [10-11] is observed (Figure 8.26) as a result of the

localized heating generated by the excessive current flow, leading to contact material melting when current measures around 130 μA. Thus V_{DD} is set to 5 V and R_{bias} is pick such that the discharge current is less than 5 μA. No welding is observed.

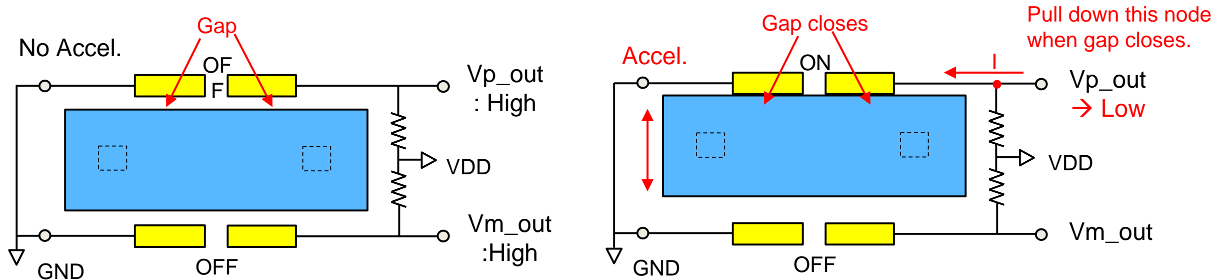


Fig. 8.26. Analog readout setup.

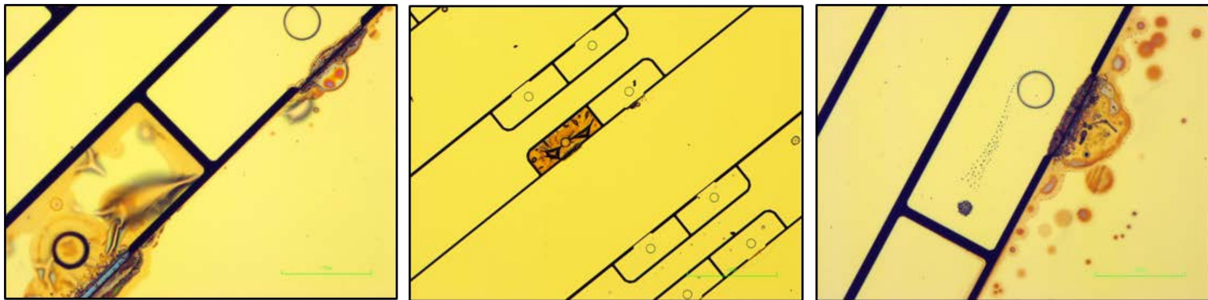


Fig. 8.28. Micro-welding at the electrodes due to excessive current flow.

The outputs from the array are routed through the PCB to the analog input channels of the National Instrument DAQ board NI PCI-6070E. The input impedance of the analog input channels is 100 GΩ resistance in parallel with 100 pF capacitance. We control the shaker table to operate at different frequencies and peak acceleration levels to test if the proof-mass and countering electrodes will make good contact to discharge the output nodes. The analog channel captures the threshold hair accelerometer contacting events that match with the input motion frequencies.

The sensor chip being tested has 4×0.5 μm^2 proof-mass footprint and 20×20-25×25 μm^2-wide > 600 μm-long double supporting springs. The outputs nodes are pulled down from the

initial 5 V at 20 Hz and 40 Hz. At 40 Hz, it is pulled down to ~ 3 V and at 20 Hz it is pulled down to 4.6 V as shown in Figure 8.27.

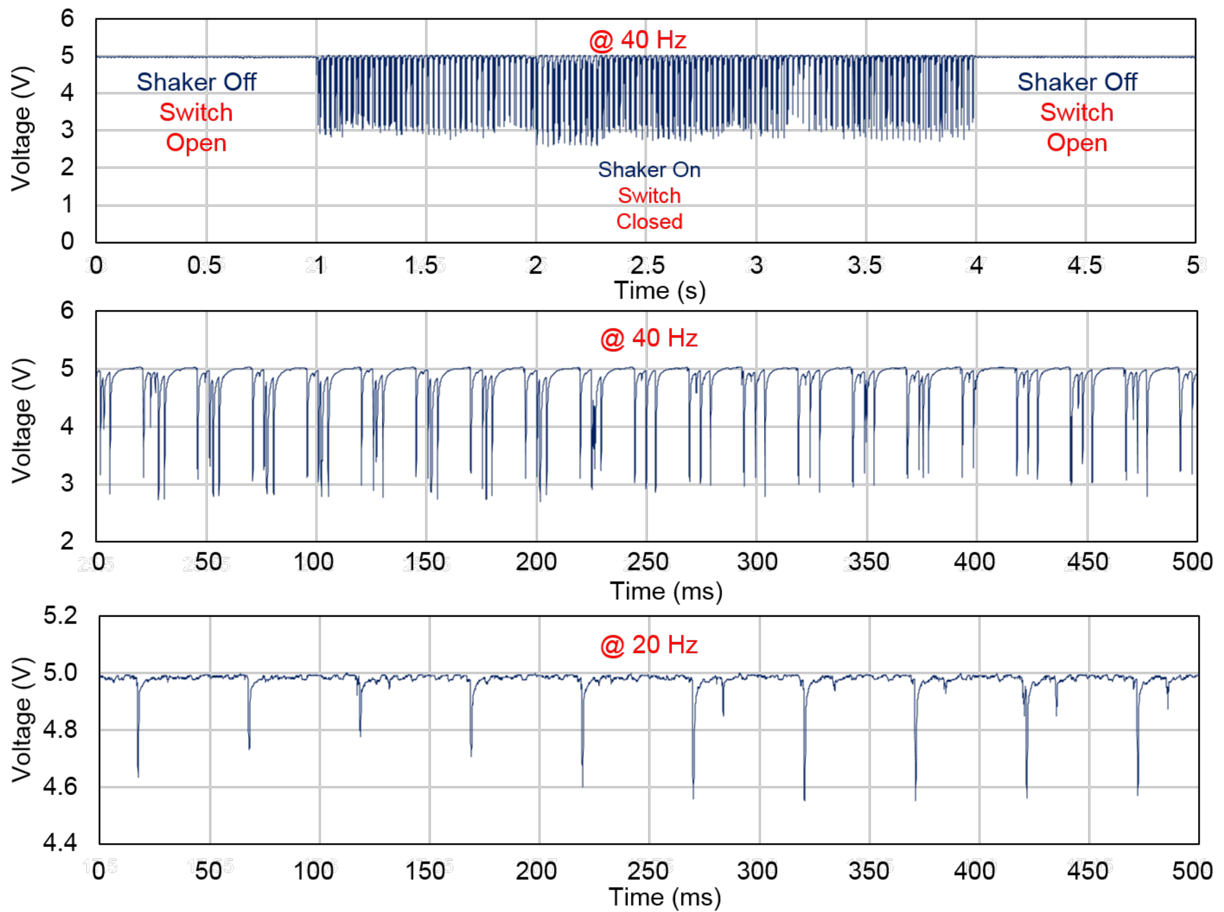


Fig. 8.27. Analog outputs from one threshold hair accelerometer: the outputs nodes are pulled down from the initial 5 V at 20 Hz and 40 Hz. At 40 Hz, it is pulled down to ~ 3 V and at 20 Hz it is pulled down to 4.6 V.

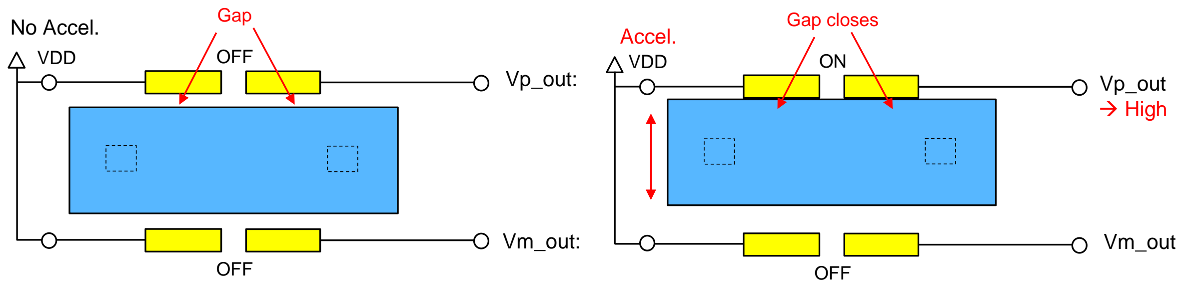


Fig. 8.28. Digital output setup.

We also feed the output ports (V_{p_out} and V_{m_out} in Figure 8.28) to the Keysight Technologies MSOX3054T Mixed Signal Oscilloscope's digital input channels to capture the

switching events of multiple threshold accelerometers simultaneously. The input impedance of the digital input channels is 100 kΩ R_L in parallel with 8.5pF C_L. V_{DD} is set to 0.5V so that I_{max} is less than 5 μA. The step response time $\tau = (R_S//R_L)C_L < 1$ μs.

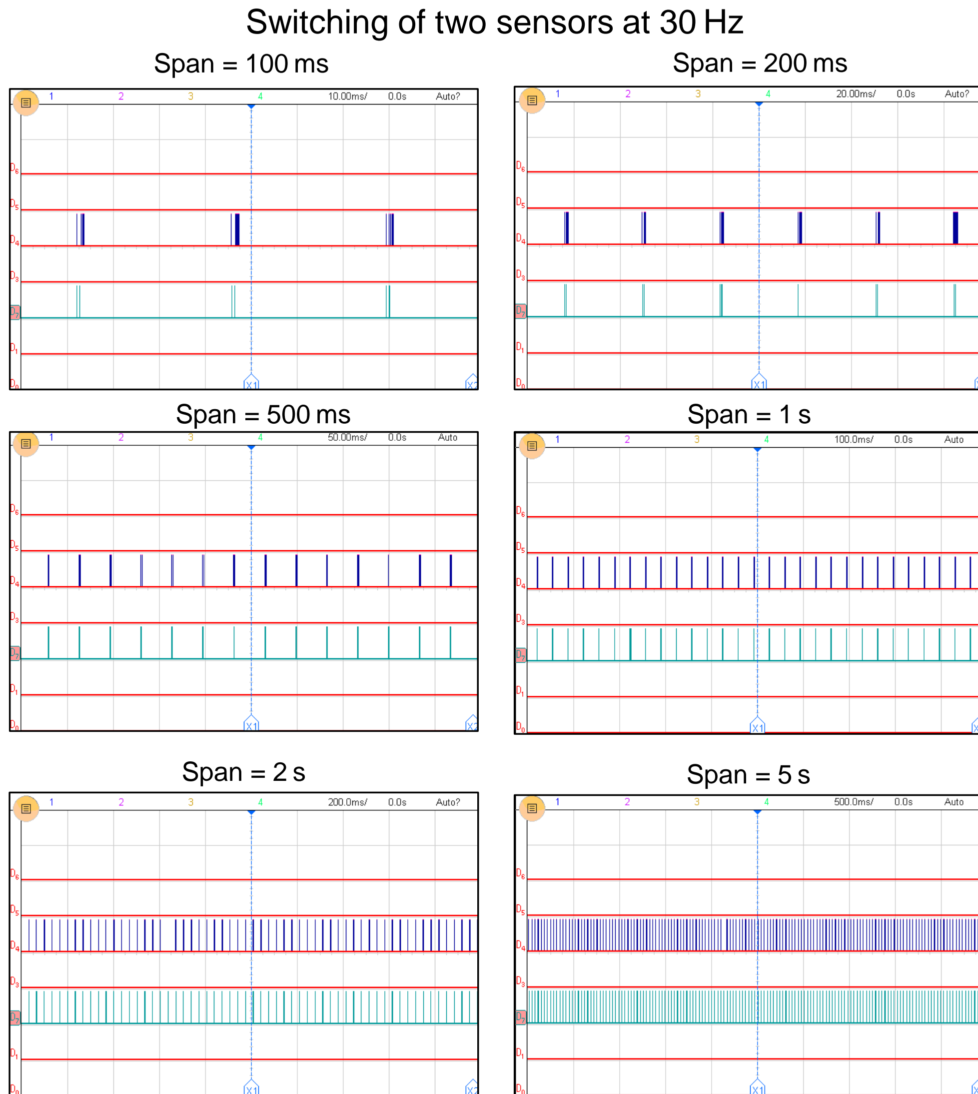


Fig. 8.31. Two threshold accelerometers are switched simultaneously with 6 g peak acceleration at 30 Hz.

Figure 8.29 and 8.30 present two threshold hair accelerometers are switched simultaneously with 6 g peak acceleration at 30 Hz, and with 8 g peak acceleration at 40 Hz. Since these two devices in the array have the same proof-mass and spring design, and differ only in the threshold gaps, their responses are almost synchronized.

Figure 8.31 presents the switching responses from two sensors in the array as the shaker motion was ramped up from rest. Missing bits were observed at the beginning. There’s also offset (approximately 0.5 ms) between the two sensors’ responses.

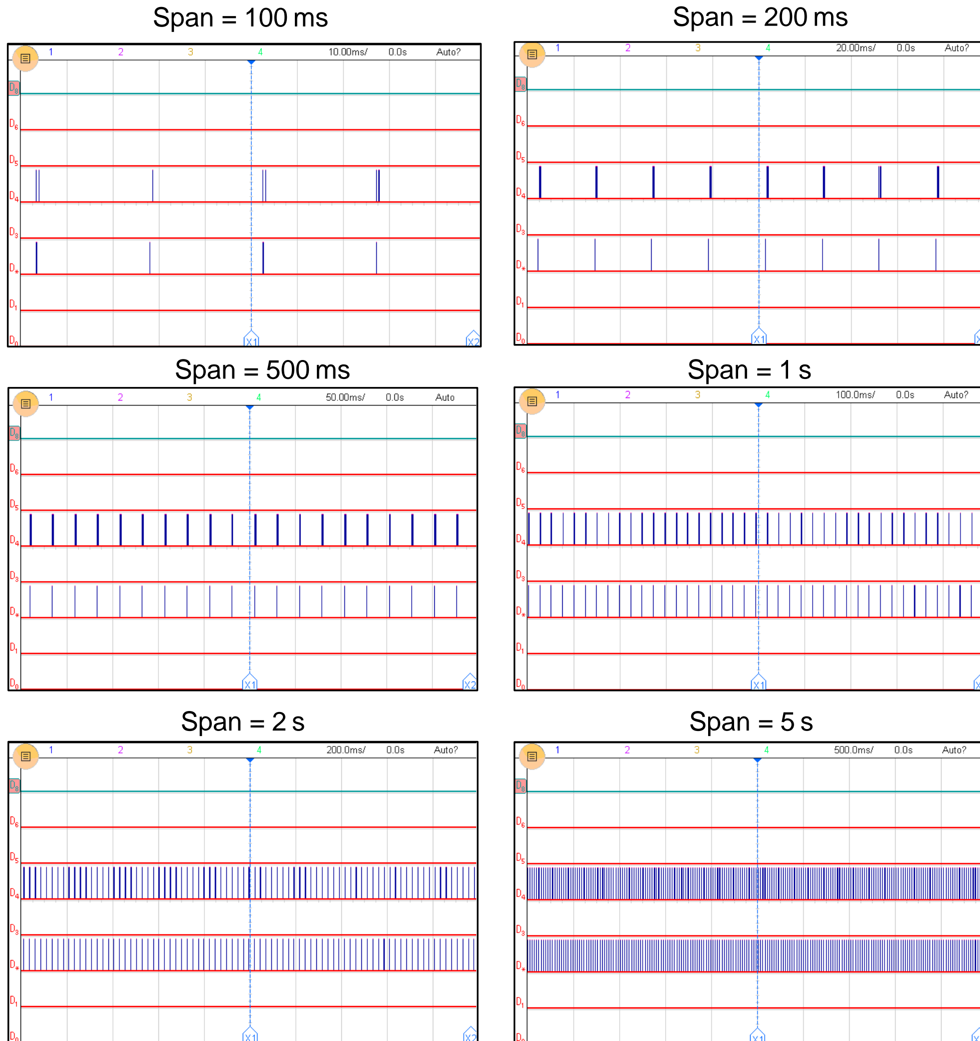


Fig. 8.32. Two threshold accelerometers are switched simultaneously with 8 g peak acceleration at 40 Hz.

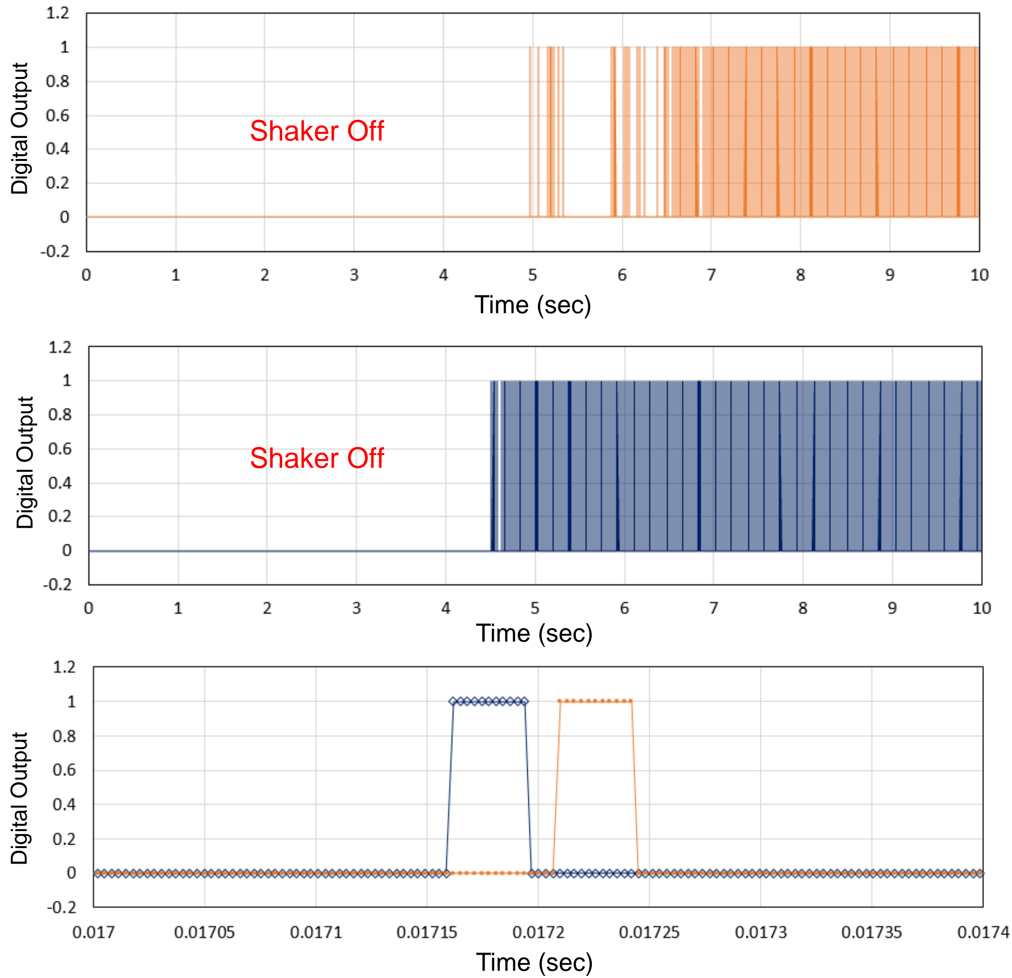


Fig. 8.31. Switching responses from two sensors in the array as the shaker motion was ramped up from rest. There's also offset (approximately 0.5 ms) between the sensors' responses.

8.5 Low-Power Digital Resonant Array for Micromechanical Frequency Processer

As introduced in Chapter 1.1, an array of micromechanical resonators can be used to construct a vibration monitoring system, performing mechanical FFT based on the mechanical resonance of a spring-mass structure in the range of from several Hertz to 10 kHz.

In this sub-section, we discuss the feasibility of building micromechanical signal processer using our proposed hair structure in dense array. Figure 8.32 presents the schematic of a large array of digital hair structures that can cover a wide frequency range by adopting single vertical cantilever beams structure for high frequencies, and vertical cantilever beams with

proof-mass for lower frequencies. For each accelerometer, there is a pair of contact/switch electrodes along the sensitive axis and digital outputs can be registered when the switches are closed due to vibration or acceleration at the designed resonant frequency of the sensor.

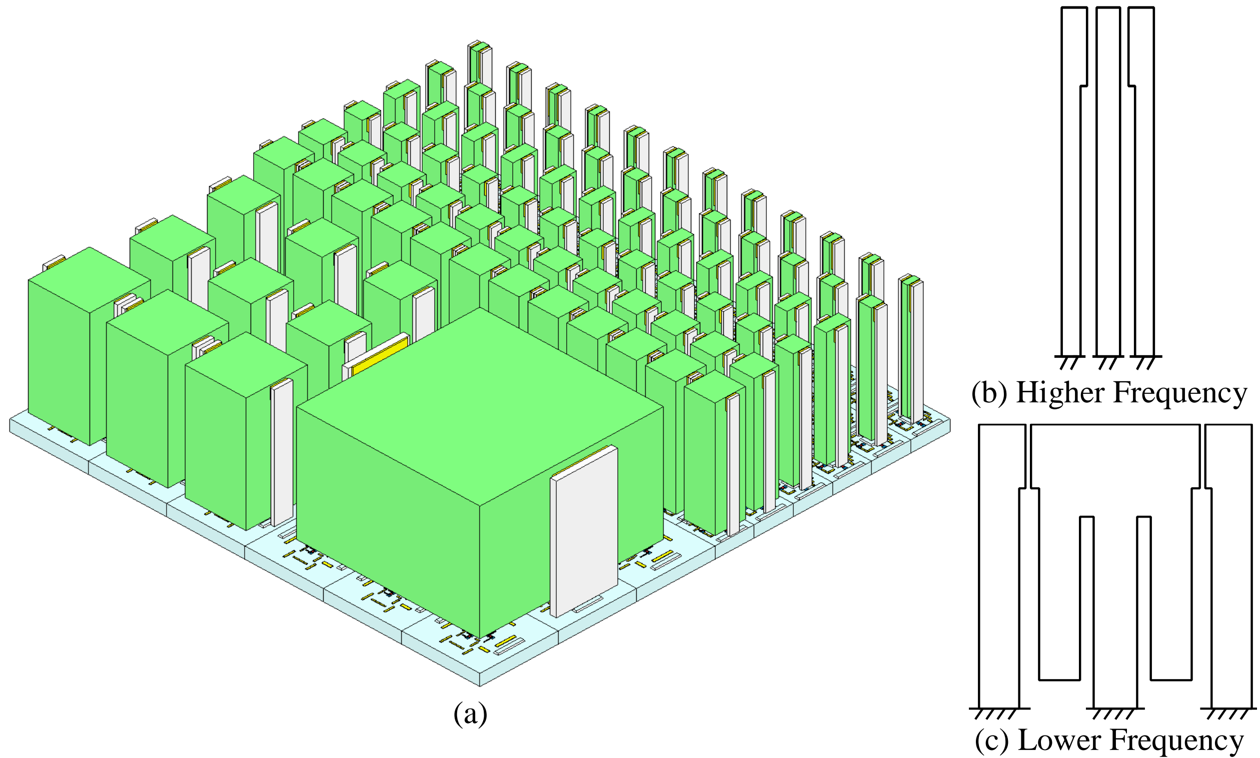


Fig. 8.32. High density MEMS transducer arrays based on the 3D biomimetic hair structures.

For single cantilever beams in Clamped-Free (C-F) configuration, the flexural resonators operate at their best at frequency ranges from several kHz to 100 MHz.

Blom et al. [14] in their 1992 article [14] gave theoretical design rules for the geometry of resonant silicon beams in order to achieve a high quality-factor at atmospheric conditions. Expressions are derived for the damped resonance frequency and the Q-factor of a damped vibrating beam considering only air damping (not squeeze film damping from small sensing gaps), as well as for the pressure dependence of both parameters.

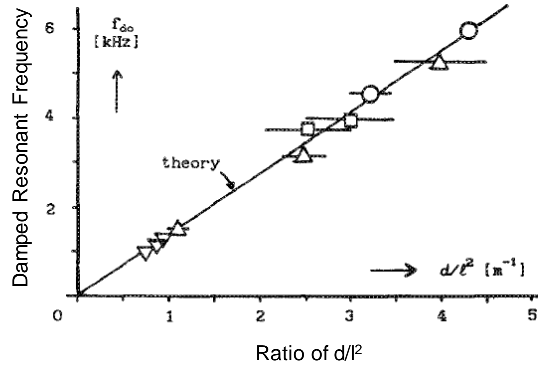
For a single cantilever design of length L, width b, and thickness d vibrating in its flexural mode when fixed on one end and placed in a fluid medium, the nth order undamped

angular resonance frequency is given by equation 8.2 [14]. For the first-order resonance mode $k_0 = 1.875$.

$$\omega_n = 2\pi f_n = k_n^2 \frac{d}{L^2}\sqrt{\frac{E}{12\rho_S}}, with\, k_0 = 1.875 \tag{8.2}$$

Sample	l (mm)	b (mm)	d (μm) ($\pm$1)	f_0 (Hz) ($\pm$1)	R (μm) ($\pm$40)	p_c (Pa) ($\pm$40)
7-3	1.5	0.5	9	5259	165	35
7-4	3.0	0.5	10	1491	310	55
7-5	2.0	0.5	10	3163	255	25
85-1	4.0	0.5	15	1310	370	30
85-3	4.0	0.5	15	1242	390	25
85-4	4.0	0.4	14	1193	355	35
85-6	4.0	0.4	14	1223	360	30
85-9	4.0	0.3	12	1005	230	100
85-10	4.0	0.2	11	915	160	210
85-12	4.0	0.2	12	1017	155	200
89 B2	1.4	0.2	5	3751	80	195
89 B5	1.4	0.4	6	3995	120	90
89 B6	1.4	0.4	6	3978	140	65
89 B8	1.4	0.6	6	3832	160	50
90 F5	2.0	0.4	13	4537	175	35
91 C5	2.8	0.4	34	5952	300	10

(a)



(b)

Fig. 8.33. (a) Dimensions of the beams used (length I, width b, and thickness d), their first-order resonance frequency f_0. It also presents the calculated results of the curve fitting for the radius R of a sphere (model the beams by discs→spheres) and the critical pressure p_c in order to maximize Q at higher pressure; (b) the damped resonance frequency f_{d0} as function of the dimensional parameter d/l^2 for the cantilever beams. [14]

In the hair array design, with the current fabrication technique of fabricating the vertical hair structures from a thick wafer of fixed thickness, it is not possible to modify the beam length L on the same chip as in reference [14] and [15].

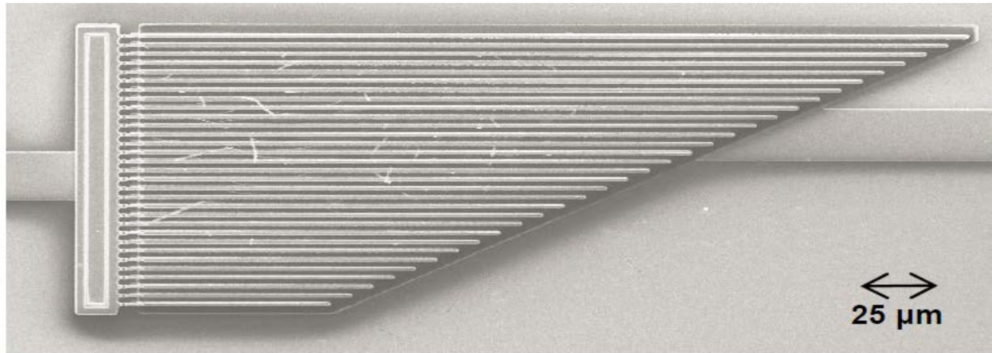


Fig. 8.34. SEM image of the array of cantilever beams in [15].

However, we can modify the width the spring to target different resonant frequencies for the 1st flexural mode from 1 to 100 kHz (Figure 8.35(a)) and from 1 kHz to 10 kHz (Figure 8.35(b)).

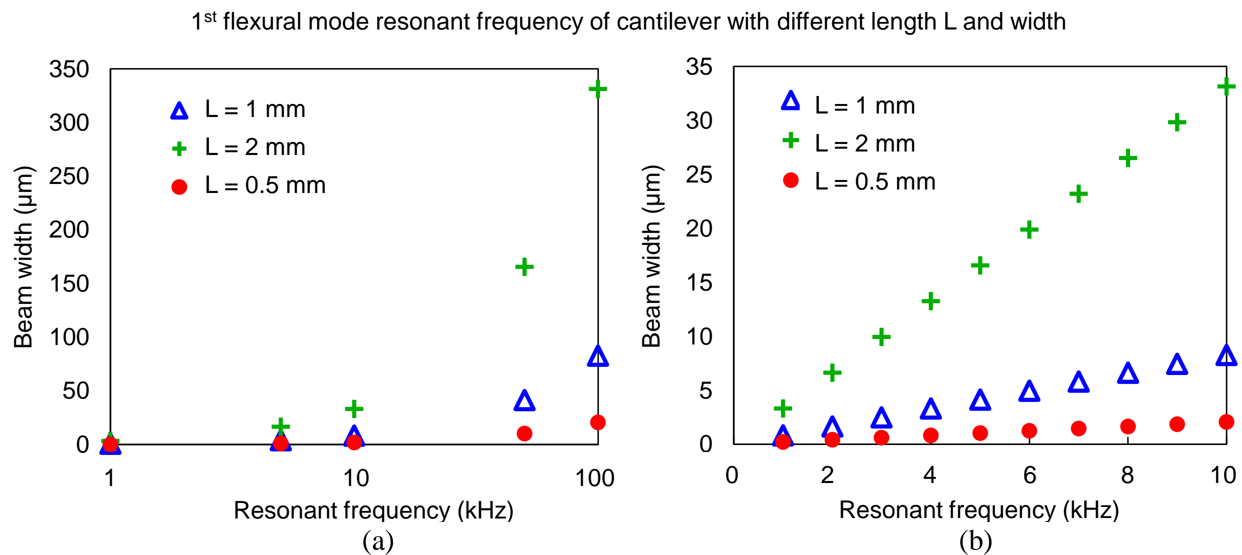


Fig. 8.35. For a single cantilever hair spring with fixed beam length L, different beam width can be designed to target the desired resonant frequencies for the 1st flexural mode targeting (a) 1 to 100 kHz and (b) 1 to 10 kHz.

For resonant frequencies from 100 to 1000 Hz, the hair structure with both the vertical

hair spring and proof-mass can be implemented. Figure 8.36 shows that by varying the proof-mass footprint, the resonant frequencies above 200 Hz can be realized by proof-mass that is less than 400 μm on the side, and 100 Hz can be realized by proof-mass that is less than 850 μm on the side.

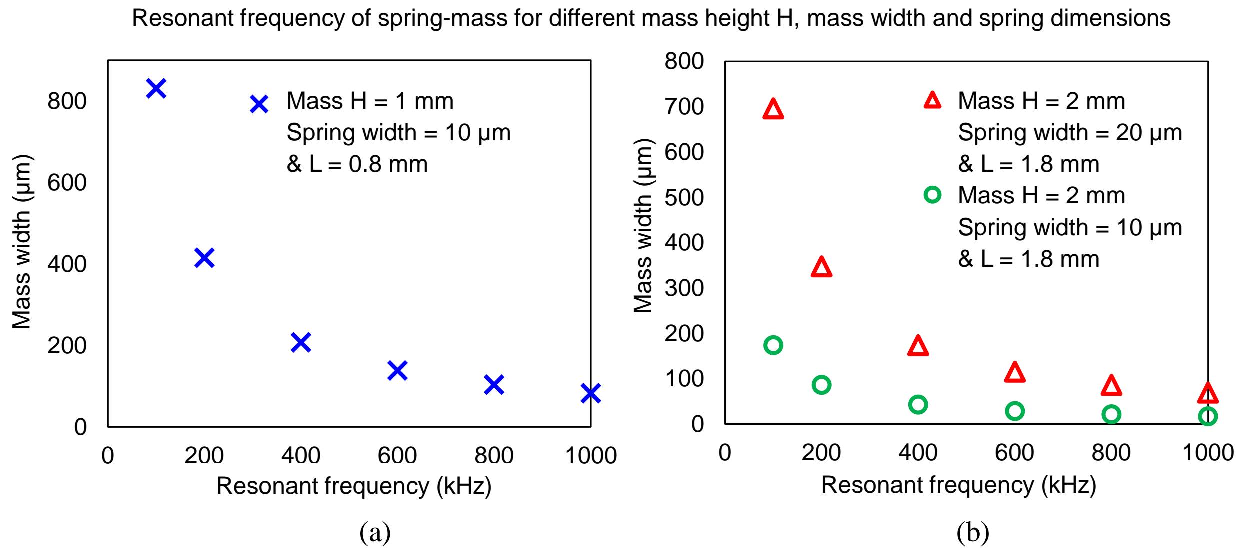


Fig. 8.36. Resonant frequency of spring-mass hair structure targeting 100 Hz to 1000 Hz.

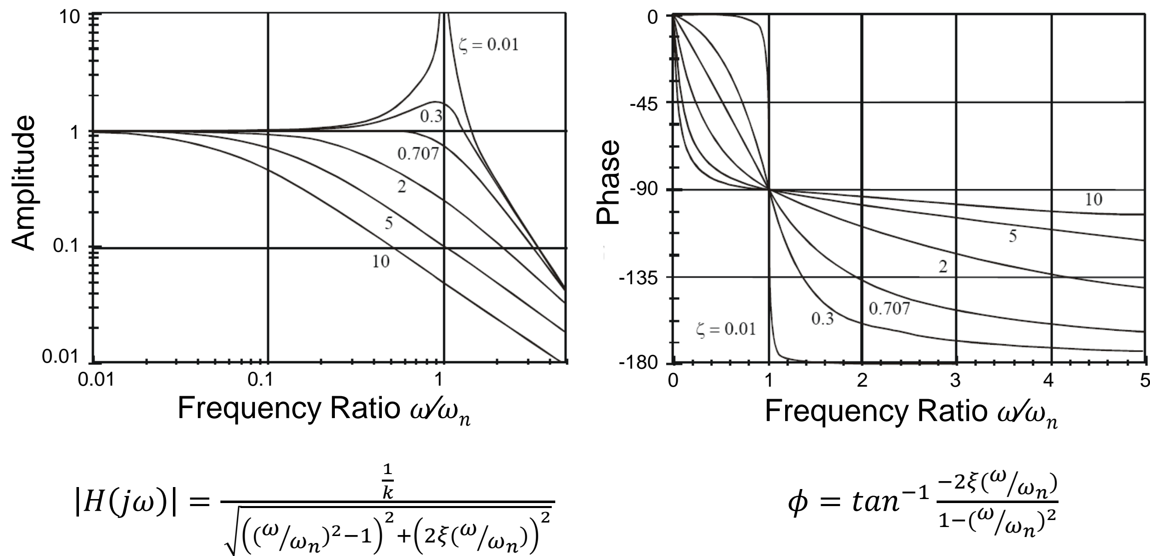


Fig. 8.37. Frequency response of second-order mass-spring-damper system.

Amplitude amplification at resonant frequency by quality factor (Q) requires packaging at specific pressure (affecting the damping ratio ζ in Figure 8.37) to ensure enough displacement for the proof-mass to contact the stationary electrodes.

Based on the resonant testing results in section 6.4.2, the digital array sensor chip needs to be packaged below 1mTorr. Due to the tradeoff between resonant frequency and displacement sensitivity, achieving Q that is high enough for higher frequency resonant mode is more challenging.

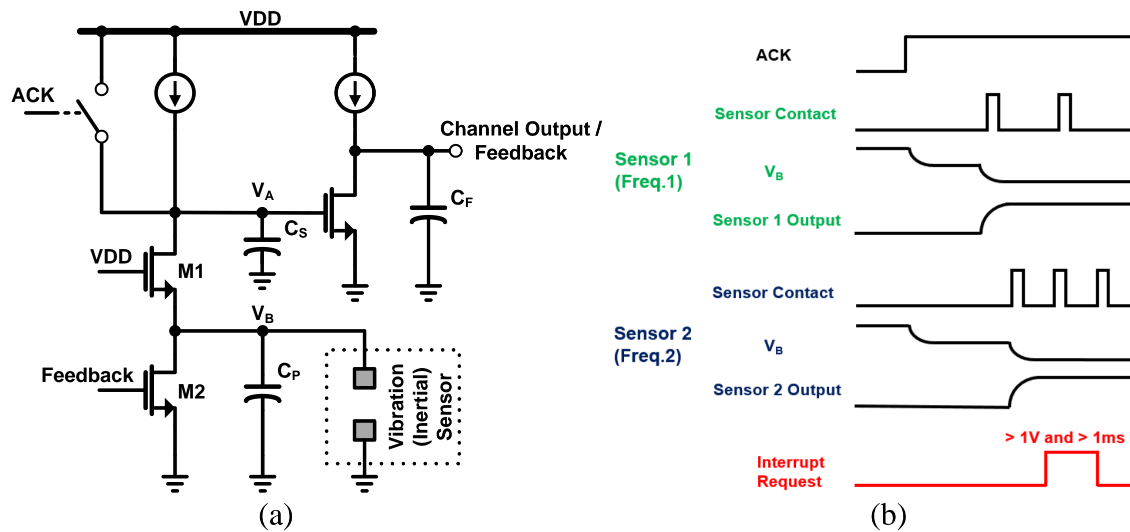


Fig. 8.38. Proposed circuit block for threshold detection and latching.

Readout architecture similar to the interface circuit previously developed in our group for threshold sensor arrays can be implemented with latest technology for our hair accelerometer arrays [4].

This circuit (Figure 8.38) can sense and capture the sensor arrays switching without affecting its operation. The micro-power consumption allows it to continuously monitor environmental shocks or vibrations in power limited systems. Furthermore, multiple channels can address large switch arrays and provide higher reliability and fault tolerance.

The schematic diagram of a sensor detection circuit is shown in Figure 8.38(a). Compared to [4], this circuit merges a latch at the front end that further reduces power. Before the normal mode of operation, the internal node V_A is pre-charged to V_{DD}. Transistor M_3 is on and the output capacitor, C_F, discharges. The output signal is fed back to the gate of transistor M_2 and this also pre-charges V_A to V_{DD}. When the switch is off, the limited current (the leakage current of the transistors) for both nodes reduce the overall chip power dissipation.

When the proof-mass touches the two electrodes capacitor Cp is grounded. The input of high-to-low transition is amplified by a common source amplifier (M_3 right to capacitor C_S). The output signal will be latched because the pulses of the MEMS switch contacting will be short and will have different duty cycles.

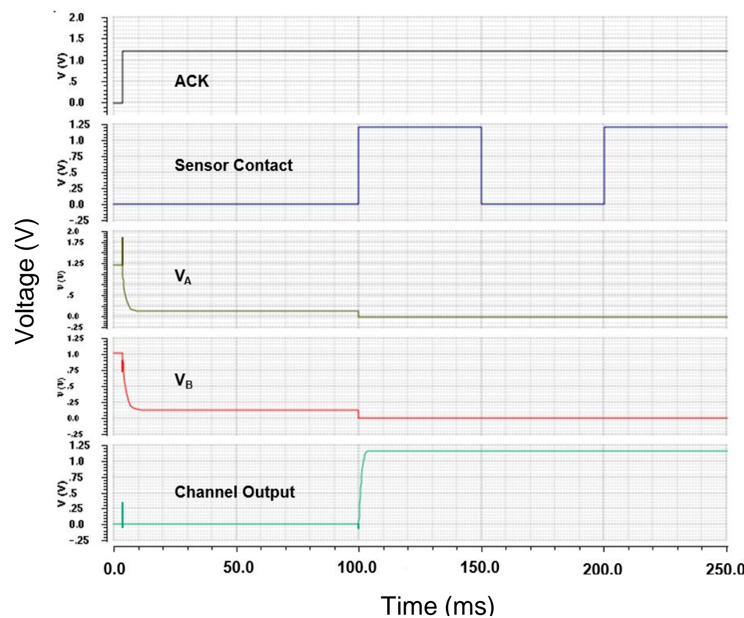


Fig. 8.39. Cadence simulated circuit response to pulsed sensor contacting.

Figure 8.38 (b) shows the timing diagram of the signal detection block. We show timing diagram of the two signal detection blocks for two sensors having different resonant frequencies. When both sensors are shorted, the output will go high and be latched until the ACK signal goes low. Figure 8.39 shows the Cadence simulation results of channel output in response to pulsed

sensor contacting. The circuit is designed to operate from a 1.2 V power supply, and power dissipation of each circuit block is less than 0.165 nW from transient current flow when no event happens, and 0.140 nW when proof-mass contacts the electrodes.

8.6 References

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Chapter 9 CONCLUSION

9.1 Accomplishments

This thesis work led to a number of technological contributions to the MEMS community including development of a novel 3D biomimetic high aspect-ratio hair-like microstructure, a new CMOS-compatible 3D MEMS microfabrication technology, the design and optimization low-noise high sensitivity lower-power silicon MEMS accelerometer and wide dynamic range MEMS accelerometer arrays. The significant accomplishments of this thesis are summarized as follows:

1) Design and analytical modeling of the 3D biomimetic high aspect-ratio hair-like microstructure as the basic sensing element for high density MEMS multi-transducer platform.

- Vertical spring /cantilever was introduced for this first time.
- Reduced device footprint enabled dense transducer array formation. The 3D hair structure with increased aspect-ratio and height achieves competitive/superior performance compared with traditional planar devices.

2) Developed and characterized an advanced Bosch deep-reactive-ion-etching (DRIE) process for realizing ultra-deep (1 mm) ultra-high aspect-ratio (UHAR) silicon structures with straight sidewalls across a wide range of feature sizes, and apply this well-characterized Bosch DRIE process to the microfabrication 3D high aspect-ratio hair structure.

- The challenges and shortcomings in Bosch DRIE was overcome by continuously ramping critical DRIE parameters throughout the process, including the 380-kHz bias power during etch step, the etch/passivation step duration, and the chamber pressure. These parameters were adjusted along with the total etch duration for a target etch depth for certain feature sizes.
- DRIE mask materials and stack thickness were studied, experimented and selected based the targeted feature sizes and etch depth.
- Aspect-ratio (AR) greater than 40 was achieved for 1 mm through-trench etch. $AR \approx 80$ was achieved for 500 μm through-trench etch, and $AR > 20$ was achieved for 500 μm through-hole etch, with straight sidewalls across a wide range of feature sizes from 2 to 100 μm.

3) Developed a two-gap double-sided silicon microfabrication process taking advantage of the ultra-deep UHAR Bosch DRIE. The process allows the 3D hair structure design to be optimized for applications in MEMS inertial sensor fabrication.

- DRIE from both sides of 500 μm and 1 mm thick silicon substrates were well characterized to suit the desired dimensions for the 3D hair structure.

4) Develop a CMOS-compatible wafer-level microfabrication technology is developed for integration of MEMS transducer device wafer built with arrays of 3D hair sensors and CMOS circuit/interconnect wafers in order to realize multi-transducer microsystems.

- The associated ultra-deep ultra-high aspect-ratio Bosch DRIE, silicon-gold eutectic bonding, and patterning were integrated into one process, and it is characterized for better process control and yield.
- Identified the major challenges in the 3D integration technology of the dense hair sensor

arrays with circuit substrates in terms of transducer integration density and post-CMOS compatibility (metallization and bonding).

5) Design, fabricate and test high performance capacitive hair accelerometer based on the 3D hair structure.

- Effective high aspect-ratio capacitive transduction was formed between the side of the tall proof-mass and stationary electrodes, which greatly extended the capacitive transduction area, the contact gap opening height being 2 μm and gap height being greater than 200 μm.
- The device was designed to achieve low mechanical noise floor at <1 μg/√Hz limited by squeeze film air damping, and high capacitive sensitivity >1 pF/g per millimeter-squared footprint.

6) Design, fabricate and test threshold hair accelerometer based on the 3D hair structure that achieves high threshold resolution and low power consumption within a small footprint. Effective contact-mode detection is formed at the top of the proof-mass and stationary electrodes.

- High acceleration threshold resolution was realized by small-area (gap being less than 50 μm in height compared to >250 μm in the capacitive devices) contact-mode detection with reduced air damping.
- In addition to varying the hair structure's physical dimensions, the threshold gap was designated as a strong design parameter to tune the threshold g-levels.

7) Demonstrate the use of MEMS sensors arrays to extend full-scale range and introduce frequency selectivity. We build arrays of both capacitive hair accelerometers and threshold hair accelerometers consisted of devices with tailored structural dimensions in order to cover wide

performance specifications in terms of full-scale acceleration levels and frequency spectrum.

9.2 Suggestions for Future Work

There are several areas we are interested in pursuing with our hair sensor and sensor array in the future.

A. Further process development and optimization on the 3D hair structure design

To further reduce the thermal mechanical noise, technology needs to be developed to improve the performance of the single hair sensor structure. For example, instead of pure silicon proof-mass, extra mass can be patterned (electroplated, printed, wire-bonded, etc.) on top of the hair structure to increase the mass density per unit footprint. The vertical spring that has a minimum width at 15-20 μm may also be further reduced to <10 μm by sacrificial layers while preserving descent spring anchors area for reliable bonding.

B. Alternative transduction gaps for higher sensitivity

In the current work, capacitive transduction and threshold detection located along the proof-mass and stationary electrodes sidewalls with minimum 1-2 μm gaps are implemented. Smaller initial sensing gap can be defined by sacrificial layers at different locations: for example, sensing gaps of 10s-100s nanometers may be located between the top surface of the proof-mass and electrodes that extend from the stationary electrodes; they may also be located between the bottom surface of the proof-mass and electrodes patterned on the circuit substrates.

C. Build high density MEMS transducer arrays

The size of sensor arrays can be extended to more than few 10s as shown in Figure 9.1. In addition to modulating the structural dimensions of the hair structure to extend the full-scale signal detection range and frequency spectrum, identical design can be duplicated to add sensor system redundancy and increase robustness. Large number of sensors with local signal processing will

further reduce noise floor and increase sensitivity proposed by the following methods.

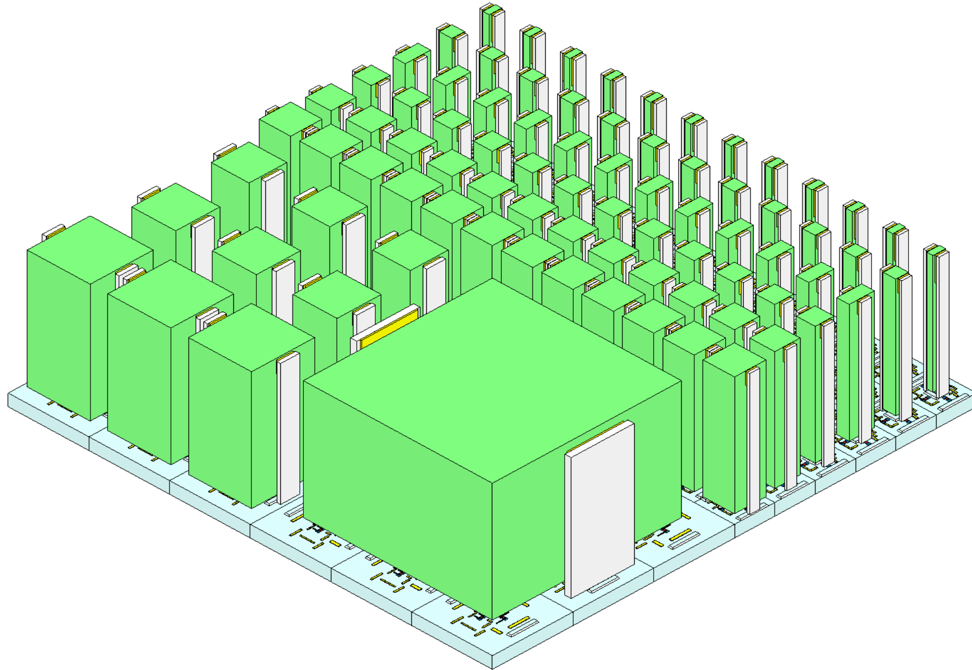

Fig. 9.1. High density MEMS transducer arrays based on the 3D biomimetic hair structures. In addition to modulated structural dimensions to extend the full-scale signal detection range and frequency spectrum, system redundancy and increase robustness are enabled by duplicating identical designs. Large number of sensors with local signal processing will further reduce noise floor and increase sensitivity by compensating for CMOS/MEMS process variations.

1) Reduce thermal mechanical thermal noise/circuit noise by arrays

Researchers have developed analytical apparatus for optimally combining measurements from N sensors into a single estimate that theoretically proves to be significantly improving the performance over that of individual element. Algorithm such as Kalman filtering is used to minimize the variance of errors [1-2]. For example, the mechanical noise $a_n = \sqrt{\frac{4kT\omega_0}{mQ}}$ (g/√Hz) inherent to the mass-spring-damper system will be reduced by √N in this fashion.

The cancellation of noise may also be done by inclusion of a reference cell. This reference sensor along with the circuit will sense the temperature variation and other electrical

and mechanical Brownian noise as all the other sensors while being immune to external vibration and motion of interest.

2) Compensate for process variation and shift of resonant frequencies by arrays

Deviations from the designed sensor specifications are partially contributed by the normally-distributed MEMS/CMOS process variations. By implementing large arrays of identical sensors, they can be compensated by post-processing the array outputs and choosing the sensor output that deviates the least from the designed features. For example, the resonant frequency of the hair structure will be different than designed value due to process variations thus we may use an array of N devices designed to offset from the nominal target frequency by few Hz to few 10s of Hz to account for the process variations.

9.3 References

[1] D. S. Bayard, S. R. Ploen, "High accuracy inertial sensors from inexpensive components," US 6,882,964, 2005.

[2] X. Liang et al., "A novel Kalman filter for combining outputs of MEMS gyroscope array," in Measurement 45, no. 4, May 2012.