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DIFFUSION EFFECTS IN SHORT-CHANNEL GaAs MESFETs

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Abstract—Diffusion effects in short-channel GaAs MESFETs are studied using a two-dimensional electron temperature simulation. A structure that consists of two n^+–n contacts on a thin channel region was used as a test vehicle for the study. This structure was found to have a higher cutoff frequency than conventionally doped devices with the same gate length due to decreased gate capacitance and a selective modulation of the device transconductance. These results suggest that the performance of short-channel microwave MESFETs may be influenced strongly by electron diffusion.

1. INTRODUCTION

It is now possible to fabricate semiconductor structures whose dimensions are comparable to Debye lengths and mean free paths of charge carriers. Present-day electron-beam lithography and photoresist technology is capable of producing line widths of the order of 250 Å[1] and GaAs MESFETs with gate lengths of 0.1 μm have been reported recently[2]. Devices with small dimensions and very short channels may have many potential advantages including high-frequency, high-speed operation and low power consumption[3].

The extrinsic Debye length represents the characteristic length over which the small unbalanced charge in a semiconductor decays:

$$L_D \simeq \sqrt{\frac{\epsilon kT}{q^2 n}}, \tag{1}$$

where ϵ = the permittivity, k = the Boltzmann constant, T = the electron temperature, $q = 1.6 \times 10^{-19}$ C and n = the carrier concentration. For 1×10^{17} cm^{-3} doped GaAs at 300 K, the Debye length is approximately 140 Å. As channel lengths become equal to a few Debye lengths, diffusion from highly doped contacts into the more lightly doped channel of short MESFETs becomes important. Previous studies of "ballistic" short-channel devices indicated that diffusion of carriers from contact regions into lower-doped channels may be a dominant factor in determining device operation under steady-state conditions[4,5]. In this study, these diffusion effects are evaluated using a two-dimensional computer simulation. The simulation consists of simultaneous solutions of Poisson's equation, the current continuity equation, and a simplified form of the energy conservation moment of the Boltzmann transport equation. In Section 2 the device structure is introduced and an explanation of its proposed operation is given. In Section 3 a brief outline of the electron temperature model used to simulate the diffusion effects and in Section 4, the results for a range of different structures are presented. The results are summarized in Section 5.

2. THE GaAs DEVICE STRUCTURE

The structure to be studied consists of two n^+–n junctions self-aligned to a narrow channel region under the gate. This transistor structure is an extension of typical present transistor structures with ion implanted self-aligned source and drain contacts. A "conventional" transistor and the present structure both have an $n^+ nn^+$ configuration. The difference is that present structure has a channel distance between the more heavily doped contacts that is only a few Debye lengths long. The structure with parallel source and drain contacts on the ends of the device is shown in Fig. 1. If the channel region is only a few Debye lengths long, then diffusion of carriers from the contacts into the channel causes the actual carrier concentration in the channel to be higher than the doping in that area. The ratio of transconductance to gate capacitance represents the cutoff frequency, a common figure of merit for transistor operation. Both the gate capacitance and the transconductance of the short channel device depend on the electron distribution within the structure. The diffusion of the electrons into the channel from the two contact regions increases the channel electron density above the doping level and should increase the current and the transconductance. The purpose of this paper is to study these diffusion effects for a range of transistor structures with varying low doped region positions and lengths under the gate contact to see if they can be used to improve the high-frequency device operation.

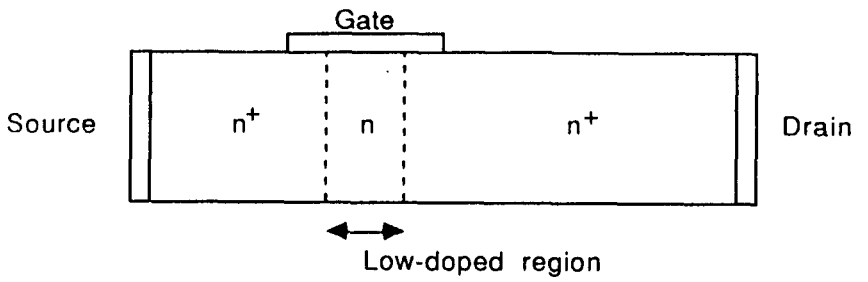


Fig. 1. The short channel field-effect transistor structure.

3. THE MODEL

A full two-dimensional electron temperature model, similar to that of Curtice and Yun[6], was used to simulate the short-channel FET structure. The model is a 2-D, time-dependent, finite-difference simulation formulated on a 2-D staggered mesh system using conservative upwind differencing techniques. The solution consists of solving Poisson's equation:

$$\nabla \cdot \bar{E} = -\frac{q}{\epsilon}(n - N), \tag{2}$$

the current continuity equation:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot \bar{J}, \tag{3}$$

and an energy equation formulated by McCumber and Chynoweth[7]:

$$\frac{\partial w}{\partial t} = -\bar{v} \cdot \nabla w - \frac{3}{2}k\frac{T - T_0}{r} - q\bar{v} \cdot \bar{E}, \tag{4}$$

where $\bar{E}$ = the electric field, n = the carrier concentration, N = the doping concentration, t = time, w = the average total kinetic energy, T = the electron temperature, T_0 = the lattice temperature and r = the energy relaxation time.

The current density is given by:

$$\bar{J} = -qn\bar{v}, \tag{5}$$

where the electron velocity is:

$$\bar{v} = -\mu\bar{E} - \frac{D}{n}\nabla n. \tag{6}$$

In formulating eqn (4), McCumber and Chynoweth assumed that the electron temperature in both conduction band valleys of GaAs was the same. To account for the upper valley electrons, all electrons with energy exceeding 0.36 eV were assumed to belong to the upper valley and the drift contribution to the change in the average total kinetic energy is assumed to be negligible compared to the thermal term:

$$\delta w = \tfrac{3}{2}k\delta T + \epsilon_v \delta F \tag{7}$$

where ϵ_v = the valley separation (energy) and F = the upper valley fraction.

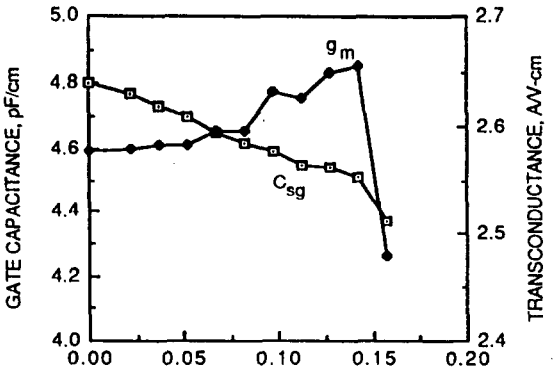
Equations (2)–(4) are solved simultaneously. The solution of eqn (4) is coupled to eqn (3) through the mobility $\mu(T)$ and diffusion coefficient $D(T)$.

This temperature treatment of carrier transport gives a better description of velocity overshoot and valley transfer than drift and diffusion based models. The mobility and diffusion coefficients in eqn (6) depend on the electron temperature given by eqn (4). A finite time or distance is required to heat electrons. This allows velocity overshoot to occur. The velocities in the channel under the gate for this model are higher than the peak velocity predicted by the static velocity vs field curve. The temperature model also moderates the effect of valley transfer. The valley transfer depends on the electron temperature and not on the local electric field. For the short gate structures under consideration, the electron temperature under the gate determined by eqn (4) does not increase enough to allow valley transfer to occur. A detailed description of a 1-D version of this model and a discussion of the calculation of μ and D is given by Sandborn *et al.*[8]. Curtice[9,10] showed that accurate device results for short gate structures can be obtained using this type of simulation approach.

4. RESULTS

In this section the simulation results for FET structures with variable low-doped channel region widths, dopings and positions relative to the gate are presented and discussed. All of the simulation results in this section are from the 2-D temperature model discussed in Section 3. The main result of this section is that electrons from the contact regions are diffusing into the channel region under the gate. This increase in the channel electron density modifies the field and velocity distribution under the gate and allows the conductance and the transconductance to approach a more heavily doped structure. The gate capacitance also depends on the charge distribution and diffusion under the gate. The net result is a modified capacitance and transconductance vs gate bias and a slightly better cutoff frequency. The remaining portion of this section will describe these results in more detail.

The device used has a length of 1.455 μm, an epitaxial layer thickness of 0.12 μm, contact



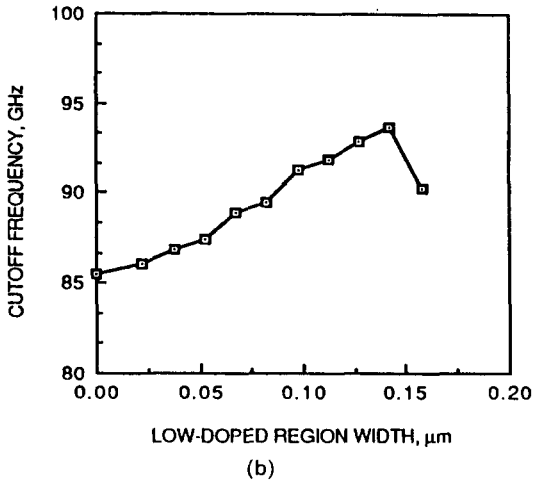


Fig. 2. (a) Gate capacitance (▣) and transconductance (◆) characteristics for a GaAs short channel FET. $V_{ds} = 1.0$ V, $V_g = -0.55$ V, $N_{contact} = 1.5 \times 10^{17}\,cm^{-3}$, $N_{low\text{-}doped\ region} = 1.1 \times 10^{17}\,cm^{-3}$, $V_{bi} = 0.6$ V, device width = 0.12 μm, device length = 1.455 μm and gate length = 0.25 μm. (b) Cutoff frequency for a GaAs short channel structure. All device information is given in (a).

doping of $1.5 \times 10^{17}\,cm^{-3}$, a gate length of 0.25 μm and a built-in voltage on the gate of −0.6 V. A bias point was selected from I–V characersitics in which a uniformly doped conventional device ($N = 1.5 \times 10^{17}\,cm^{-3}$) was in the current saturation region. The bias point selected for the calculation of cutoff frequency was $V_{ds} = 1.0$ V and $V_g = -0.55$ V. Figure 2 shows the characteristics as the width of the low-doped region is varied. The solution gives the 2-D charge distribution in the structure as a function of the bias conditions. The charge on the gate Schottky barrier metal contact can be found using Gauss' law and the gate capacitance can be found by finding the change in the gate contact charge for a small change in the gate source voltage. Figure 2(a) gives gate capacitance and transconductance characteristics and Fig. 2(b) shows the resulting cutoff frequency as the low-doped region width is varied.

For this device, the right edge of the low-doped region is fixed at the right edge of the gate contact and the left edge of the low-doped region is varied. The doping of the low-doped region was set so the pinchoff voltage of a conventional device with a doping equal to the low-doped region would approximately equal $|V_g + V_{bi}|$. The value used was $N_{low\ doped\ region} = 1.1 \times 10^{17}\,cm^{-3}$. Figure 2(a) indicates that the gate capacitance drops as the low-doped region width is increased. This is to be expected since the charge associated with the gate depletion layer is reduced as the width of the lower doped channel region increases. If the gate were longer, reducing the channel doping would also reduce the channel electron density. However, for the short channel structure, the channel electron density also depends on diffusion from the contacts. From Fig. 2(a) it can be seen that the transconductance rises to a peak value at a low-doped region width of 0.1425 μm before dropping. The transconductance curve can be explained with the help of Fig. 3. This figure shows the transconductance vs gate voltage relation for a conventional MESFET doped at $1.5 \times 10^{17}\,cm^{-3}$. As $|V_g|$ is increased, the volume of the channel under the gate and the total number of electrons in the channel of the MESFET decreases. For low $|V_g|$, the electron velocity increases compensating for the decrease in carrier concentration as V_g is varied. This effect reduces changes in drain current with gate bias and keeps the transconductance low. As $|V_g|$ is further increased, the electron velocity can no longer increase fast enough to compensate for the loss of charge in the channel and the drain current begins to decrease quickly causing the transconductance to increase. As the device approaches pinchoff (large $|V_g|$), the small current begins to flatten causing the transconductance to decrease. This type of transconductance variation with gate bias has also been shown by Buot and Frey [11]. For devices with longer gates, the peak in the transconductance relation is not present, presumably due to the decrease in electric

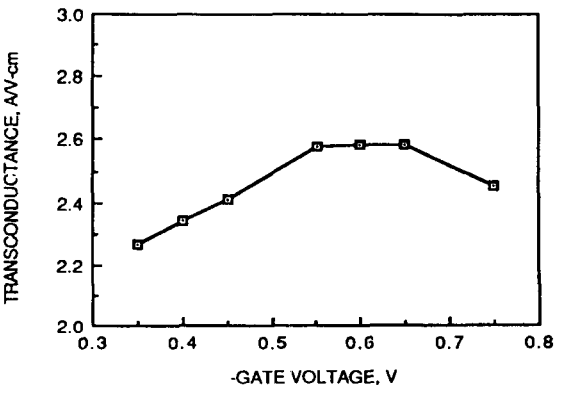


Fig. 3. Transconductance vs gate bias for a conventional FET. $V_{ds} = 1.0$ V, $n = 1.5 \times 10^{17}\,cm^{-3}$, all other device information is given in Fig. 2(a).

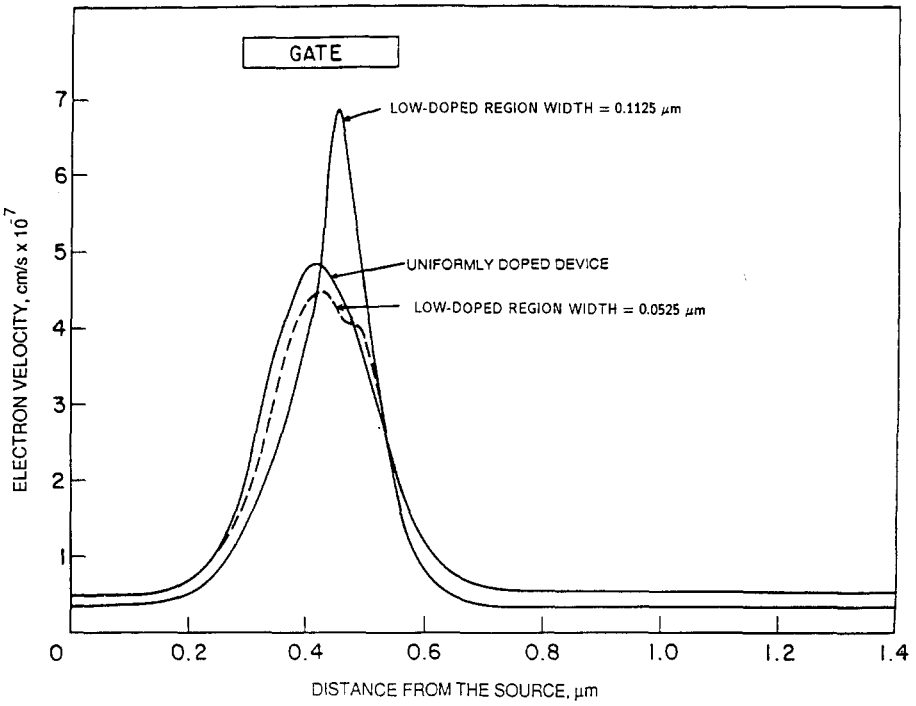


Fig. 4. Electron velocity in the channel of present structure. $V_g = -0.05$ V all other device information is given in Fig. 2(a).

field gradients that account for velocity overshoot that accompanies increased gate lengths†

The mechanism leading to the peaked transconductance relation in the short channel n^+nn^+ structure is the same as in the uniform structure except the width of the low-doped region, instead of the gate voltage, is used to modulate the change in the carrier concentration. This can be checked by observing the electron velocity in the channel for different low-doped region widths. From Fig. 4 it is seen that the electron velocity increases as the low-doped region is widened. The effect of inserting the low-doped

†Buot and Frey [11] give transconductance results for a 0.6-μm gate MESFET in which transconductance decreases monotonically with $|V_g|$.

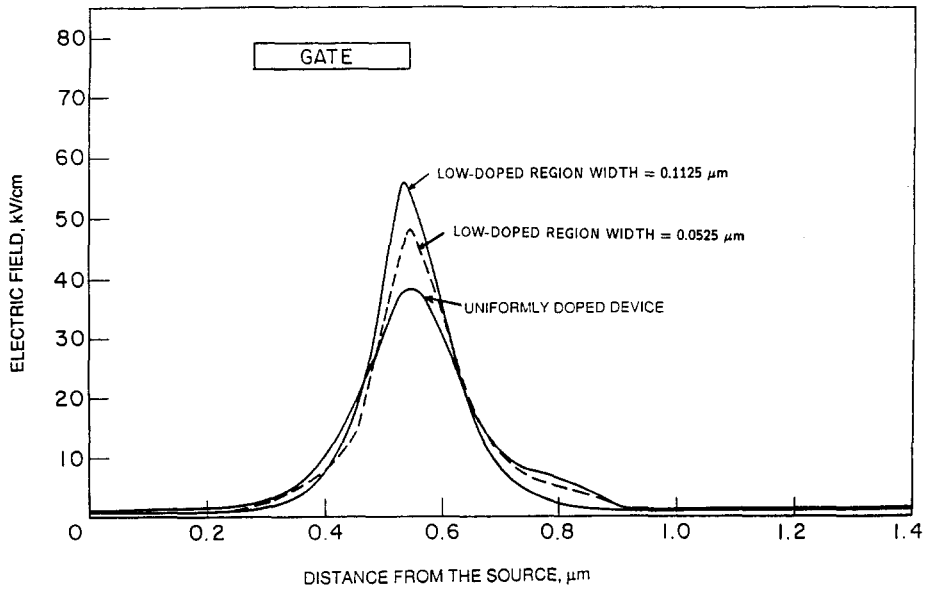


Fig. 5. Electric field in the channel of present structure. $V_g = -0.5$ V, all other device information is given in Fig. 2(a).

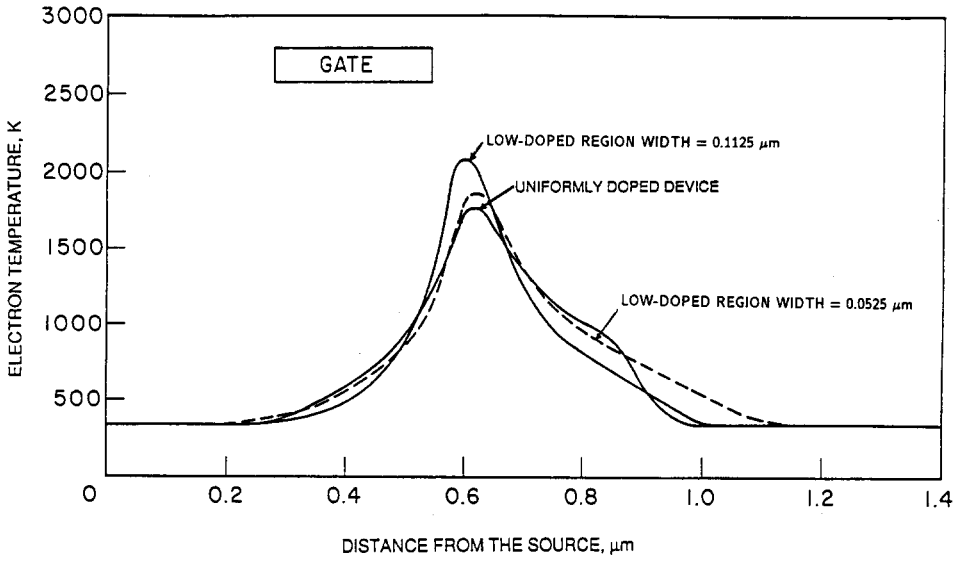


Fig. 6. Electron temperature in the channel of present structure. $V_g = -0.5$ V, all other device information is given in Fig. 2(a).

region compresses the distance over which the drain–source voltage is dropped and pushes up the electric field under the gate edge closest to the drain (Fig. 5). The electron temperature and carrier concentration in the channel are shown in Figs 6 and 7. The net effect of the decrease in gate capacitance and the increase in transconductance is to increase the cutoff frequency of the short-channel structure over a conventionally doped device with the same gate length.

A design parameter in the design of the short-channel structure is the placement of the low-doped region with respect to the gate contact. Three different structures were considered. These are shown in Fig. 8. All the devices have the same geometry, doping and bias levels as the device described in Fig. 2.

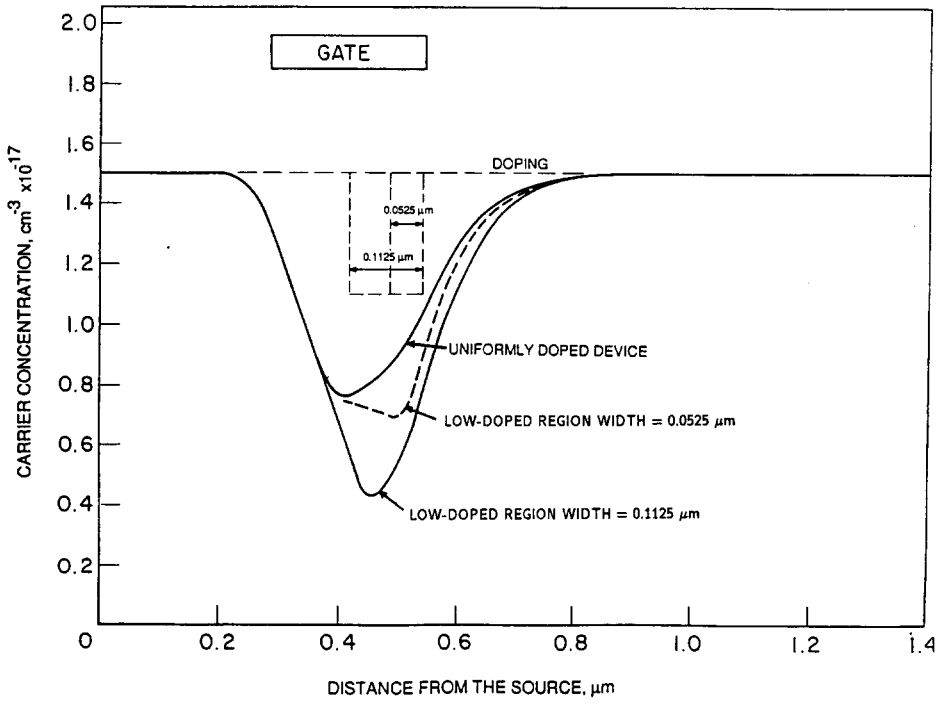


Fig. 7. Carrier concentration in the channel of present structure. $V_g = 0.5$ V, all other device information is given in Fig. 2(a).

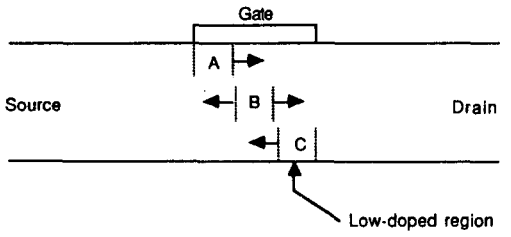


Fig. 8. The positioning of the low-doped channel region in the structures.

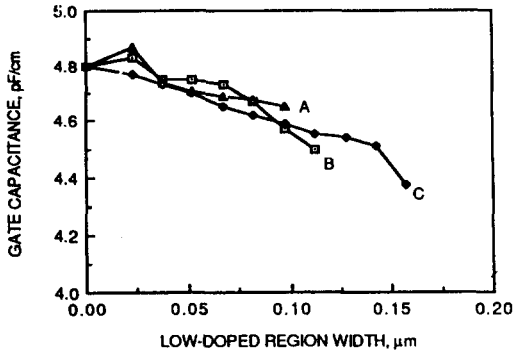


Fig. 9. Gate capacitance comparison with different low-doped region positions relative to the gate. △ = Device A, ▣ = device B and ◆ = device C. Devices A, B and C are defined in Fig. 9. All device information is given in Fig. 2(a).

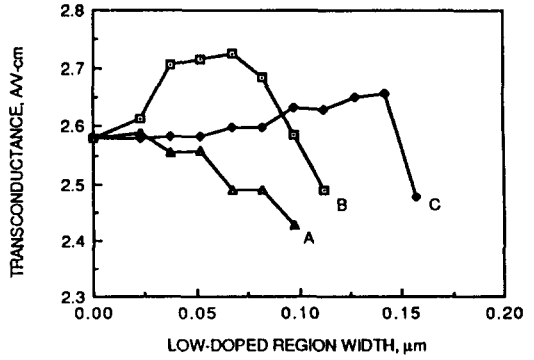


Fig. 10. Transconductance comparison with different low-doped region positions relative to the gate. △ = Device A, ▣ = device B and ◆ = device C. All device information is given in Fig. 2(a).

Figure 9 shows the gate capacitance comparison of the devices. The gate capacitance for the three structures is approximately the same. Figure 10 shows that the variation of transconductance with low-doped region width in the three devices is quite different. The change in transconductance can be explained in the following way: the device transconductance is assumed to depend on the width of the conducting channel at its narrowest, most heavily depleted point[12]. The position of the low-doped region relative to this point is important since the width of the depletion region is inversely proportional to

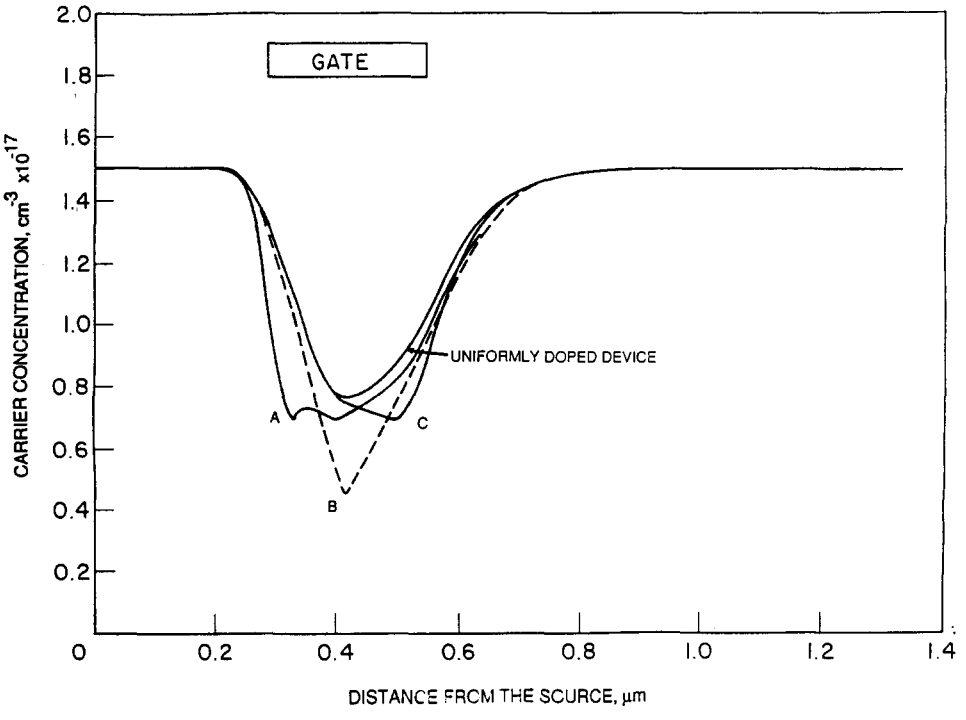


Fig. 11. Comparison of carrier concentrations in different structures. $V_g = -0.5$ V and the low-doped region width = 0.0525 μm. All other device information is given in Fig. 2(a).

$\sqrt{N}$ where N is the doping in the depleted region. From Fig. 11 it is seen that the minimum carrier concentration in the channel of the uniformly doped conventional device is approximately at the center of the gate. This figure shows that the insertion of a low-doped region at the maximum depletion point (device B) causes the minimum carrier concentration in the channel to deplete further. The insertion of a thin low-doped region away from the maximum depletion point in the channel has little or no effect on the carrier concentration at the maximum depletion point. Therefore, devices A and C have little effect on the transconductance for small low-doped region widths. As a result of this process, the low-doped region width at which the transconductance peaks is a function of the position of the low-doped region relative to the gate. Figure 12 shows the cutoff frequency curve whose shape follows that of the transconductance closely. These results show that better performance is obtained with low-doped regions not centered on the gate, since the gate capacitance is lower when the transconductance peaks.

The low-doped region doping has also been varied. Figure 13 shows the characteristics of identical structures with different dopings. As the doping of the low-doped region is decreased, the gate capacitance decreases more rapidly with increasing low-doped region width. The transconductance was found to peak for shorter low-doped region widths due to greater depletion in the channel. The lower doped structure is only usable for very short low-doped regions since the device pinches off much more readily.

5. DISCUSSION AND CONCLUSIONS

The short-channel n^+nn^+ field-effect transistor was found to have a higher cutoff frequency than a conventional MESFET with the same gate length. The structure has a higher cutoff frequency due to a decreased gate capacitance coupled with an increased transconductance. The gate capacitance was found to decrease as the width of the low-doped channel region was increased, regardless of the position of the low-doped region relative to the gate. The transconductance was found to increase initially as the width of the low-doped region was increased due to enhanced velocity overshoot in the channel of the

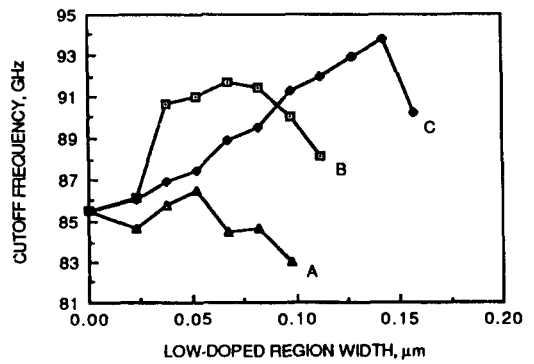


Fig. 12. Cutoff frequency with different low-doped region positions relative to the gate. △ = Device A, ▣ = device B and ◆ = device C. All device information is given in Fig. 2(a).

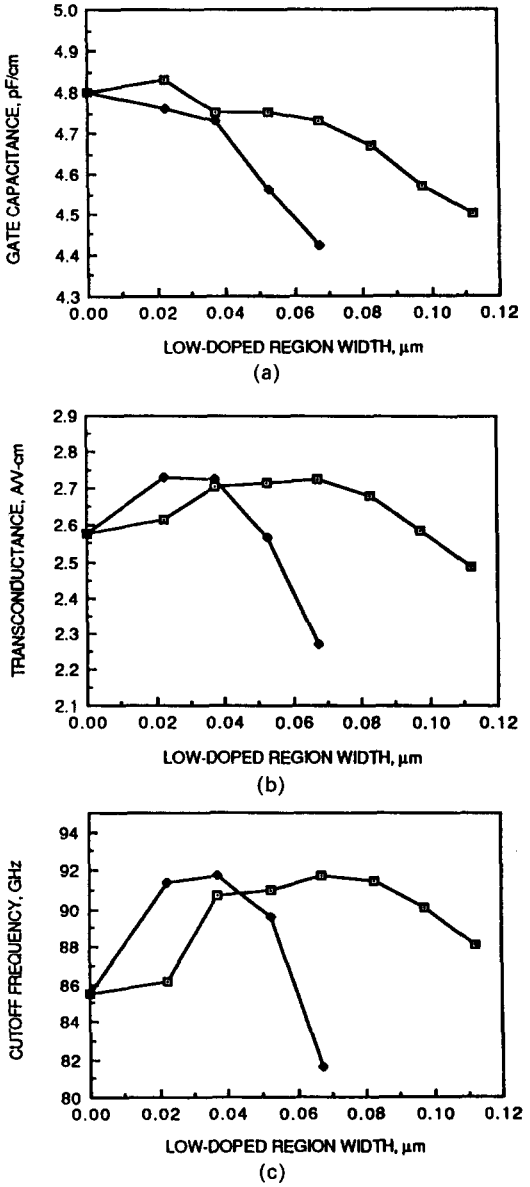


Fig. 13. (a) Gate capacitance comparison with different dopings. Device B (Fig. 9), ▣ = $N_{\text{low-doped region}} = 1.1 \times 10^{17}\,\text{cm}^{-3}$ and ◆ = $N_{\text{low-doped region}} = 8 \times 10^{16}\,\text{cm}^{-3}$. All device information is given in Fig. 2(a). (b) Transconductance comparison with different dopings. Device B (Fig. 9), ▣ = $N_{\text{low-doped region}} = 8 \times 10^{16}\,\text{cm}^{-3}$. All device information is given in Fig. 2(a). (c) Cutoff frequency comparison with different dopings. Device B (Fig. 9), ▣ = $N_{\text{low-doped region}} = 1.1 \times 10^{17}\,\text{cm}^{-3}$ and ◆ = $n_{\text{low-doped region}} = 8 \times 10^{16}\,\text{cm}^{-3}$. All device information is given in Fig. 2(a).

MESFET. The effect of inserting the low-doped region compressed the distance over which the drain–source voltage was dropped. As the width of the low-doped region became large and the device approached pinchoff, the transconductance began to decrease. The low-doped region width at which the transconductance peaks was found to depend on the position of the low-doped region relative to the maximum depletion point in the channel. Structures with low-doped regions fixed on the gate edge closest to the drain yielded the highest cutoff frequencies. Decreasing the doping of the low-doped region caused the transconductance to peak at thinner low-doped regions since the device approaches pinchoff more quickly.

Today's submicron MESFET structures with heavily doped contacts and lighter channel dopings are quickly approaching the n^+nn^+ structures. The results presented in this paper indicate that the performance of short-channel microwave MESFETs is strongly influenced by electron-diffusion effects. While practical and operational limitations may make realization of this device difficult to attain at this time, the study should aid in the understanding of submicron structures and advances in fabrication technology may make such devices quite realistic.

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