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# A new low-temperature high-aspect-ratio MEMS process using plasma activated wafer bonding

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## Abstract

This paper presents the development and characterization of a new high-aspect-ratio MEMS process. The silicon-on-silicon (SOS) process utilizes dielectric barrier discharge surface activated low-temperature wafer bonding and deep reactive ion etching to achieve a high aspect ratio (feature width reduction-to-depth ratio of 1:31), while allowing for the fabrication of devices with a very high anchor-to-anchor thermal impedance ( $>0.19 \times 10^6 \text{ K W}^{-1}$ ). The SOS process technology is based on bonding two silicon wafers with an intermediate silicon dioxide layer at 400 °C. This SOS process requires three masks and provided numerous advantages in fabricating several MEMS devices, as compared with silicon-on-glass (SOG) and silicon-on-insulator (SOI) technology, including better dimensional and etch profile control of narrow and slender MEMS structures. Additionally, by patterning the intermediate SiO<sub>2</sub> insulation layer before bonding, footing is reduced without any extra processing, as compared to both SOG and SOI. All SOS process steps are CMOS compatible.

(Some figures in this article are in colour only in the electronic version)

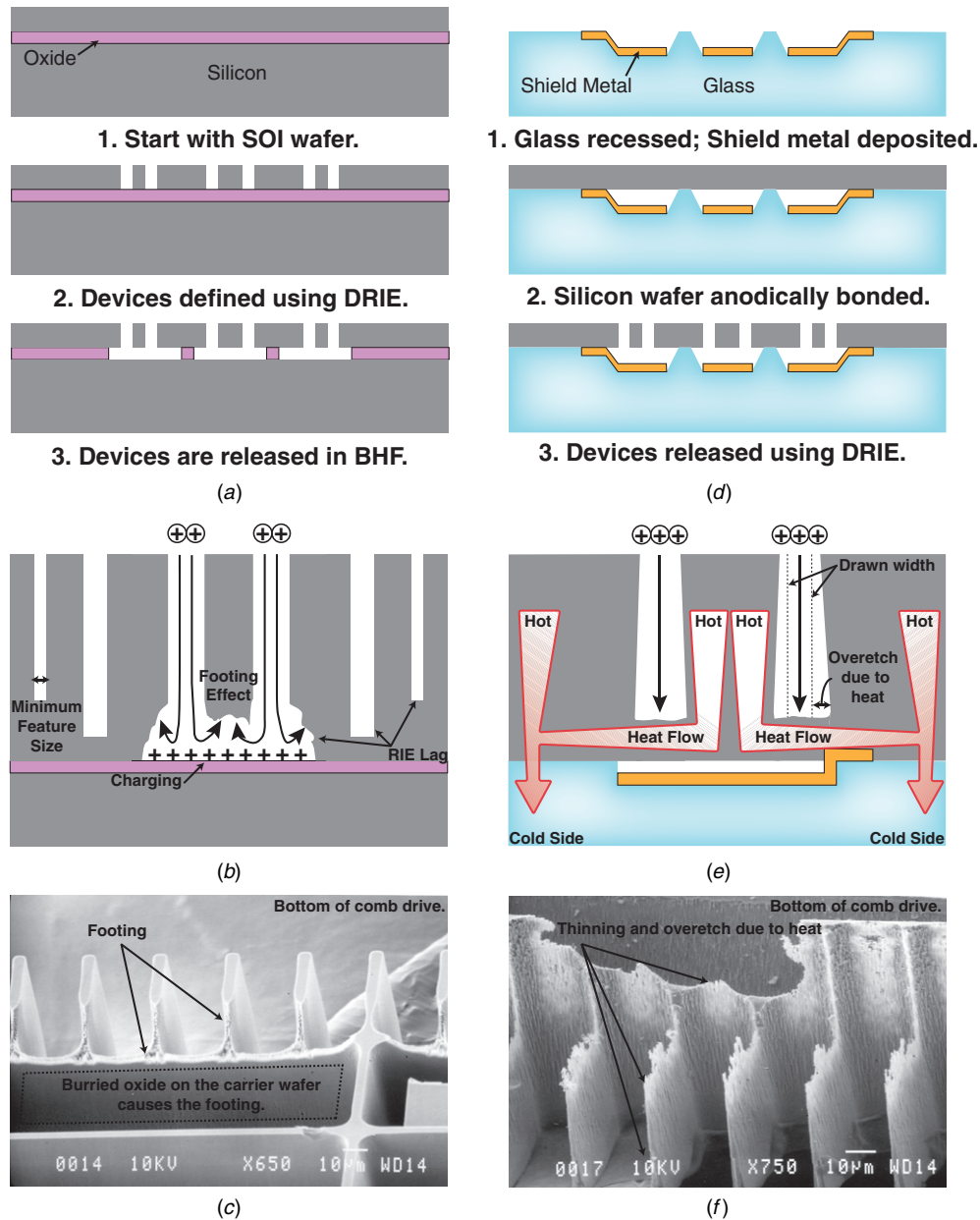
## 1. Introduction

One of the most significant discoveries in the MEMS field was the advent of the deep reactive ion etching (DRIE) process [1]. Its utility has been clearly demonstrated by MEMS researchers and industry worldwide. Based on DRIE, many high-aspect-ratio single-crystal silicon structures have been demonstrated. Although the utility of these high-aspect-ratio silicon devices is wide, nowhere is their impact as powerful as in inertial sensing and actuation. Due to the large surface area and small gaps, large in-plane sensitivity can be achieved, while allowing for designs mitigating cross-axis noise. Additionally, because the structural material is bulk crystalline silicon, mechanical stresses are eliminated when compared with deposited materials. Lastly, a large proof-mass can be formed in order to reduce noise in precision sensors.

The main fabrication paradigm employed in these devices is to anisotropically etch a single-crystal silicon film, which is structurally supported by a carrier layer, and often electrically isolated by an intermediate dielectric film. This fabrication

paradigm is embodied in the silicon-on-insulator (SOI) process [2], arguably one of the most popular process technologies worldwide. In SOI, pre-fabricated substrates consisting of a silicon film, separated from a silicon substrate by an intermediate oxide layer, are etched using DRIE. The SOI process is shown in figure 1(a). The MEMS devices are subsequently released using an isotropic etch of the buried oxide layer. In this easy way, a multitude of sensors and actuators have been created by both academia and industry.

However, SOI comes with a variety of problems that must be overcome in cases where critical dimension control and precision operation are essential. The main problem stems from RIE lag [3], sometimes referred to as microloading, which is the interdependence of the etch rate and the aspect ratio as shown in figure 1(b), where narrow features etch slower than wider ones. Due to microloading, which results in wider features being etched faster than narrower ones, and because DRIE is typically not uniform throughout the diameter of the wafer (it can vary by 1–15%), as the etch reaches the dielectric in some places, charge starts to build



**Figure 1.** (a) SOI process flow. (b) Illustration of how RIE lag necessitates overetching, which leads to footing in SOI. (c) SEM of the bottom of silicon electrodes that have been overetched due to footing. (d) SOG process flow. (e) Illustration of the thermal transport problems in SOG leading to overetching. (f) SEM of the bottom of silicon electrodes that have been overetched due to overheating.

up on the dielectric. This leads to ‘footing’ or ‘notching’ [4–8]. The built-up charge on the buried dielectric deflects the incoming ions, and instead of etching down, they begin to undercut the silicon structures laterally. Because of the high-density plasma used in DRIE systems, this undercut is not negligible and can cause severe problems and unexpected results. Thin structures or devices with small anchors can be completely undercut as wide trenches are overetched while the narrower areas finish etching. Many methods have been devised to manage the footing effect. An attempt was made [9] to eliminate footing by increasing the sidewall passivation. While the footing effect became negligible in narrow trenches, it created a ‘grass’ effect on the bottom surface in the wide trenches. The authors concluded that the only robust solution

was to design the mask layout such that all areas to be etched have a uniform width, and also to design large anchors that could survive footing, but this places severe constraints on device design. In a subsequent work, a study was performed to see if platen power and etch pressure could be tuned in order to eliminate footing [10]. The authors observed that increasing platen power and process pressure exacerbated the footing effect, and that the impact of process pressure was higher than that of platen power. They concluded that it is better to select low process pressure and a higher platen power when the layout feature sizes varied greatly; however, footing could not be eliminated. A different strategy of mitigating the footing effect is to place guard structures to protect the main device from overetching. These guard devices are designed in

one of two ways: (1) so that they are sacrificial and will be consumed or at the very least released completely during the etching [11], or (2) they have negligible influence on the device and remain attached after etching [12]. The etch trench width between the guard structure and the device is made uniform throughout the wafer such that the overetch time that the actual device experiences due to microloading is minimized. While placing guard structures did improve etch uniformity, it places a large burden on layout and device design and geometry. The standard SOI process is altered in [13], such that the wafer is etched from the back initially, and the oxide layer underneath the devices is removed before the top-side DRIE. Lastly, new DRIE etchers incorporate low-frequency power supplies that apply pulses to the platen in order to mitigate charging and reduce footing [14].

A close relative of SOI is the silicon-on-glass (SOG) process [15] shown in figure 1(d), where a Pyrex glass wafer is recessed using isotropic etching, a silicon device wafer is anodically bonded to it, and MEMS devices are formed using DRIE from the silicon wafer. The advantage SOG has over SOI is that a method exists to remove the footing effect. By placing a metal layer on the glass surface which is connected to the silicon wafer, charge accumulation does not occur because charge is evacuated to the silicon substrate [16]. Nonetheless, SOG has a serious problem in that it complicates thermal transport during etching. Etch temperature is critical in high-density plasma etching such as DRIE. Typical ICP chambers use pressurized helium to cool the wafer from the back while it is being etched in order to keep a constant etch temperature. However, these tools are designed for silicon, which is 100 times more thermally conductive than glass. As a result, suspended structures, which have a large thermal impedance from anchor to anchor, are overetched and in many cases completely disappear during DRIE. The problem is compounded by the fact that glass is not strong enough to survive the pressure from the helium. So normally a backing silicon wafer is used, attached using photoresist, or thermally conductive grease, both of which add more insulating material.

This paper describes the development and characterization of a new process for high-aspect-ratio MEMS devices based on low-temperature plasma activated fusion bonding [17, 18]. This silicon-on-silicon (SOS) process combines elements of both SOI and SOG while eliminating footing and thermal problems during etching. Unlike the SOI technology, no wet processing is needed after release, and the thermal mismatch between glass and silicon, present in the SOG process, is eliminated. This is very important in some types of precision sensors where the temperature coefficient of expansion (TCE) mismatch adds a significant thermal component to their sensitivity. Also, the carrier wafer can undergo various microfabrication steps before bonding. Although, a process consisting of fusion bonding and DRIE has previously been reported [19], the low-temperature bond allows this process the added flexibility of having buried feedthroughs, using a variety of materials including some metals, and because all process steps are CMOS compatible, full integration can be achieved.

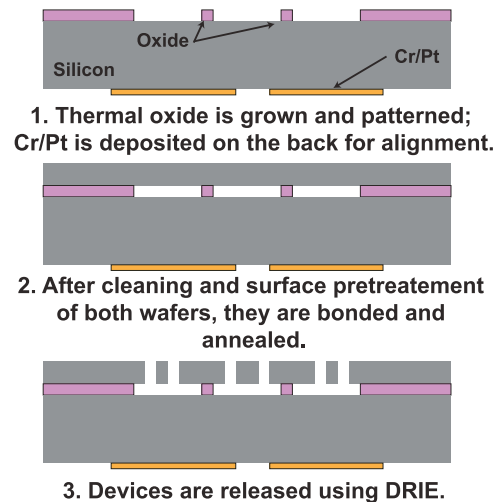


Figure 2. SOS process flow.

## 2. Process details

The SOS process essentially consists of making a custom SOI wafer, where the oxide is patterned before being buried under the second silicon device layer. This way the dielectric layer is removed from places where it will cause charging and overetch during DRIE. At the same time, since the carrier wafer is silicon, thermally related etching problems are minimized. As shown in figure 2, the process begins by oxidizing a silicon wafer. The oxide is patterned, and a layer is deposited and patterned on the backside of the wafer for future alignment purposes. A second silicon wafer is then directly bonded on top of the oxide. The two wafers are bonded using a low-temperature plasma activated fusion bond. This prevents the bonding temperature from exceeding 400 °C, and allows for post-CMOS MEMS integration. Finally, the MEMS devices are released using DRIE.

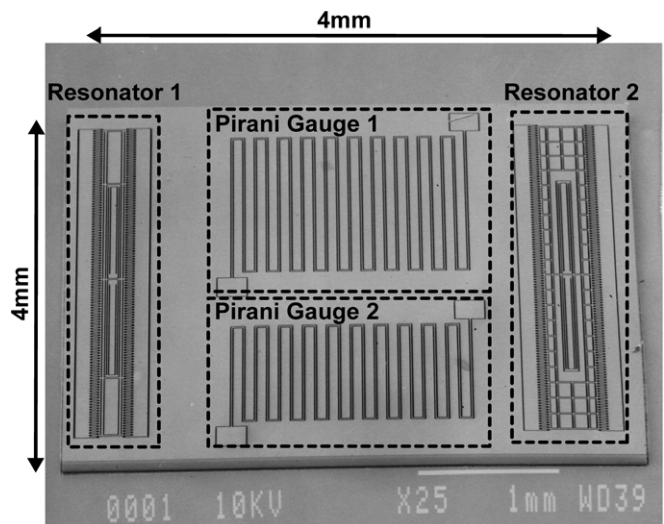
For these experiments,  $\langle 100 \rangle$  oriented p-type Czochralski grown silicon wafers with a resistivity of 1–20  $\Omega$  cm and a diameter of 100 mm were used. The carrier wafers were either single- or double-side polished. The type of wafer was not shown to have any significant bearing on the process, although the double-sided polished wafers had a wafer curvature several micrometers less than the single-side polished ones. In general, single-sided wafers were used in bonding experiments, and double-sided wafers were needed when backside alignment was required. For the device wafer, 0.005  $\Omega$  cm boron-doped silicon was used. These wafers were thinned down to a thickness of 100  $\mu$ m in order to form the required device mass.

The carrier wafer is first cleaned using the RCA-1 ( $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ , 1:1:5, 80 °C) solution to remove organics, followed by the RCA-2 ( $\text{HCL}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ , 1:1:6, 80 °C) solution in order to remove any traces of ionic contamination, and rinsed in deionized water (DIW). A 1  $\mu$ m thermal wet oxide is then grown at 1100 °C to serve as insulation and as a bonding layer. Optionally, the wafer can then be polished using chemical mechanical polishing in order to bring the surface to a roughness of <4 Årms.

Lithography is performed and the wafers are etched using buffered hydrofluoric acid (BHF) to define the bonding islands. Care is taken during design and layout to either add lateral access holes that ventilate the cavities to the outside or to not make large sealed areas. This is necessary when dealing with a thin device wafer because pressure buildup during the bonding anneal can have adverse effects and even cause cracking in the thin wafer during subsequent processing. Alignment patterns are placed on the back of the wafer. A thin layer of Cr/Pt 250/250 Å is evaporated and patterned using lift-off. Although the material and thickness for the alignment pattern are not important, care has to be taken such that this material does not influence the rest of the process in two ways: (1) the amount of materials (i.e. thickness and surface area) should not induce significant wafer bowing, and (2) the material should be able to sustain the bonding temperature without causing deleterious effects. At this point a thin 100 μm p<sup>++</sup> silicon wafer, which has previously been cleaned using a 20 min Piranha clean (H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub> 1:1), is dipped in BHF and rinsed in DI water. The carrier wafer is megasonically cleaned and dried in a SÜSS MicroTec CL200 cleaner. Both wafers are then pretreated using dielectric barrier discharge (DBD) atmospheric pressure N<sub>2</sub> plasma in a SÜSS MicroTec nanoPREP 200 system. The plasma is created with a 400 W ac bias and scanned across the wafers at a gap of 300 μm, while 50 slpm N<sub>2</sub> flows between the electrodes. The plasma activation is necessary to decrease the bond temperature of standard fusion bonding. By exposing the wafer to plasma, it is 'activated' or rendered highly hydrophilic by inducing bond defects and adding hydroxyl O–H groups [20] to the surface. The more hydroxyl groups, the higher the surface tension of the wafer, leading to improved reactivity. The improved reactivity in turn leads to increased bond kinetics: so a high strength bond can be achieved with less time and/or a lower temperature anneal. Water molecules bind to the hydroxyl sites and when the wafers are brought together, hydrogen bonding can be realized across the two mating surfaces. This is a particularly strong form of van der Waals attraction. The water molecules bridge the gaps between the two mating surfaces and create a force attracting them to each other. When the silanol groups on either surface get close enough they can polymerize to form strong stable siloxane (Si–O–Si) bonds via the reaction Si–OH + HO–Si → Si–O–Si + H<sub>2</sub>O. As the two wafers are annealed, water molecules either diffuse out along the bonded interface or oxidize silicon according to 2H<sub>2</sub>O + Si → SiO<sub>2</sub> + 2H<sub>2</sub>. A more detailed characterization of the DBD plasma activation is offered later in the paper.

Following plasma treatment the carrier wafer is again megasonically cleaned. The two wafers are brought into contact by hand and pinch bonded in the middle. After this the wafer pair is placed in a SÜSS MicroTec SB6e substrate bonder and annealed at 400 °C for 4 h while a pressure of 200–400 kPa is applied. The bonding temperature is ramped at a rate of 200 °C h<sup>-1</sup> in order to allow for water molecules to have time to diffuse out of the bond interface without causing voids.

The MEMS devices are released by performing lithography and then DRIE using a high-density inductively



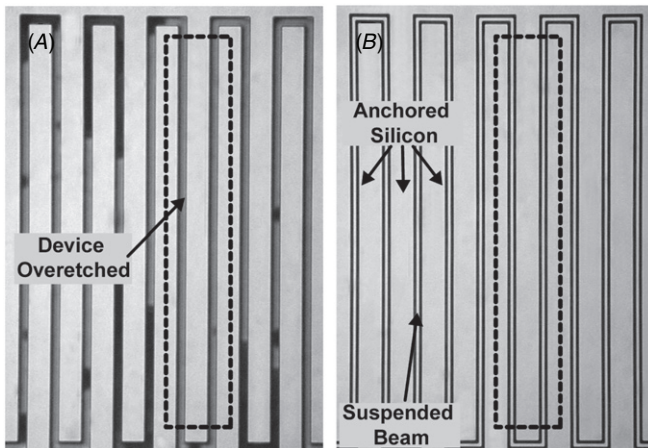
**Figure 3.** SEM of several devices fabricated using the SOS process, including two different comb-drive resonators and two Pirani gauges.

coupled plasma system from Surface Technology Systems (STS). The applied platen electrode power is 100 W for the etch cycle, and the coil power is set to 800 W during both etching and passivation. The SF<sub>6</sub> gas flow is set to 130 sccm during etching and the C<sub>4</sub>F<sub>8</sub> flow is set to 85 sccm during passivation. Etch and passivation cycles are repeated at intervals of 12 and 6 s, respectively. The base pressure is set to 0.093 Pa. The automatic pressure control valve is varied during etching, starting at 64% of base pressure and reduced by 0.4% min<sup>-1</sup> in order to increase the mean free path and preserve the anisotropic etching as the silicon is recessed.

### 3. Results

The SOS process was designed in order to address the issues that prevented a number of devices from being successfully fabricated using the SOG technology. A scanning electron micrograph (SEM) of a die fabricated using SOS is shown in figure 3. It has four devices: two Pirani gauge pressure sensors and two resonant pressure sensors. What these devices have in common is that they present a large thermal impedance from anchor to anchor, which made it impossible to manufacture using SOG. Repeated attempts to modify the SOG process parameters and to reduce the heat buildup during DRIE failed. Included in these attempts are drastic measures such as etching in very short intervals, a few minutes at a time, and allowing the wafer to cool in between. However, even these attempts resulted in a yield of zero. The reason is that despite the constant need for the wafer temperature to remain stable during etching in order to keep a straight and uniform etch profile, the most critical part is when the device is almost released. At this point, the thermal impedance increases dramatically, as does the wafer temperature. Combined with RIE lag, the result is that in a very short duration of time the situation goes from one of having poorly etched but usable devices to a completely overetched wafer. A close-up photograph of one of the Pirani gauge sensors is shown in figure 4. The Pirani

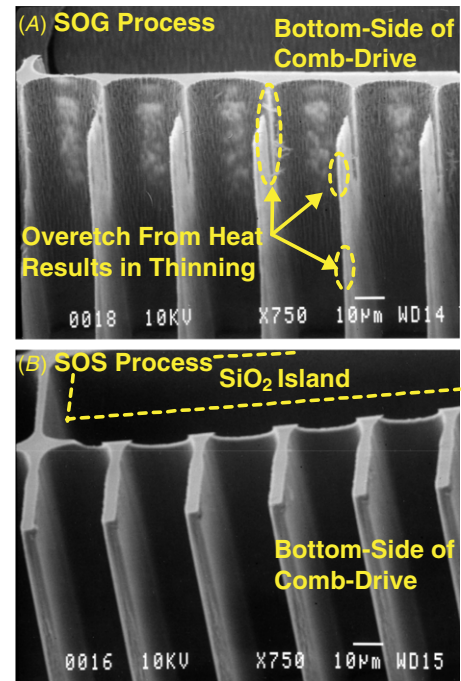




**Figure 4.** Close-up photograph of two Pirani gauges of identical design; however, the one shown in photograph A was fabricated using the SOG process and the one shown in photograph B is made using SOS. The Pirani gauge is essentially a long meandering beam suspended above the silicon substrate and anchored at its two ends. It can be seen that the devices fabricated using SOS survive the processing, whereas the devices made using the SOG process are overetched due to heat buildup during DRIE. The dark spots in A constitute areas where the underlying shield metal has been burned due to the intense heat.

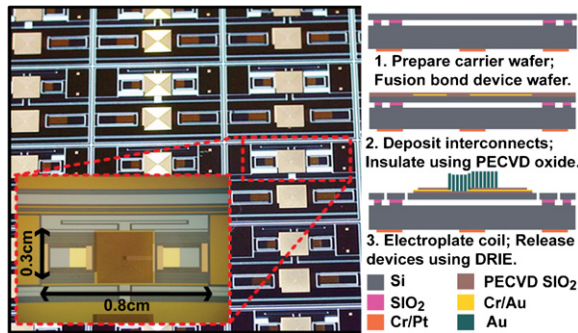
gauge is essentially a long 30 mm beam, which is 10  $\mu\text{m}$  wide and 100  $\mu\text{m}$  thick. The etch gap between the beam and the rest of the wafer is 5  $\mu\text{m}$  on both sides. It has an anchor-to-anchor thermal impedance of  $>0.19 \times 10^6 \text{ K W}^{-1}$ . One can see in the photograph in figure 4(a), that the attempted fabrication of this long meandering beam using the SOG process failed to such an extent that the entire device was overetched and is completely gone. In contrast, the same exact Pirani gauge fabricated using the SOS process can be seen in figure 4(b), released and suspended as designed.

Fabrication of the resonant pressure sensors is even more challenging than the simple beam because they can fail in two ways. These resonators have long and thin supports, with minimal gap between the supports and the rest of the substrate, in order to increase the squeezed-film damping, and to increase their sensitivity at low pressures. All of the heat from the etching has to be transported through these supports when the devices are almost released. In addition to this challenge, now there are closely packed comb-fingers where the plasma density is very high, and during etching a great deal of heat is produced in this area. This heat is dissipated easily through the opposing fingers, which are anchored to the substrate. However, when the devices are almost released, this is no longer sufficient. The result of poor heat dissipation during SOG processing is shown in figure 5(a). Adhesive tape was used to pull the resonators off the substrate and expose the bottom for inspection. An SEM of the resultant fingers shows that they are severely overetched. Additionally, their profile is thinned along the thickness. These non-idealities cause unexpected results during operation and severely limit the device sensitivity. At the same time, an SEM of the same resonator fabricated using SOS shows a dramatically improved etch profile in figure 5(b). Some small signs of footing are seen in the SEM due to a nearby oxide island.



**Figure 5.** SEM of the bottom of two sets of comb-fingers of identical design, where A was fabricated using the SOG process and the one shown in B is made using SOS. The device made using SOG is severely overetched, while the SOS device shows a better etch profile with mild footing.

One of the great advantages of the SOS process is that it does not place difficult restrictions on the geometry of the layout. For example, to make devices using the SOG process one has to limit the thermal impedance of the various paths through which the structures can dissipate heat during etching. Similarly, SOI technology places restrictions on the etch trench width in order to limit DRIE lag: namely that all of the etch widths need to be the same. To demonstrate the flexibility of the SOS process, an example is shown in figure 6, where the SOS process was extended and used to manufacture a number of inertial micro power generators. The challenges associated with fabricating the devices shown in figure 6 stem from two main points: (1) the size of the suspended mass and (2) the aspect ratio needed. The proof mass of the vibration scavenger has to remain as large as possible. However, a large mass can heat up because of the large area that is being exposed to the plasma during etching, and because of its large thermal capacitance ( $5.94 \times 10^{-3} \text{ J K}^{-1}$  in this case), it can be challenging to cool down. At the same time, the low stiffness spring supports that hold the mass suspended present a large thermal impedance. Some of the designed devices have a mass of 9.13 mg (several orders of magnitude larger than typical MEMS devices), and silicon spring suspensions with designed stiffness of  $4.75 \text{ N m}^{-1}$ . Lastly, while the devices have to have a large motion range, tens of microns, the electrode gap associated with a number of interdigitated comb-fingers has to remain as small as possible. This means that multiple geometries with varying etch widths have to be accommodated. While allowing for all of this design versatility, the SOS process achieves a very high-aspect-ratio etch profile. A feature width reduction-to-depth



**Figure 6.** Energy harvesting devices fabricated by utilizing an extended version of the SOS process shown to the right. The SOS process is ideal in this case because of the many different etch gaps, thin and long supports, and large proof masses that are needed.

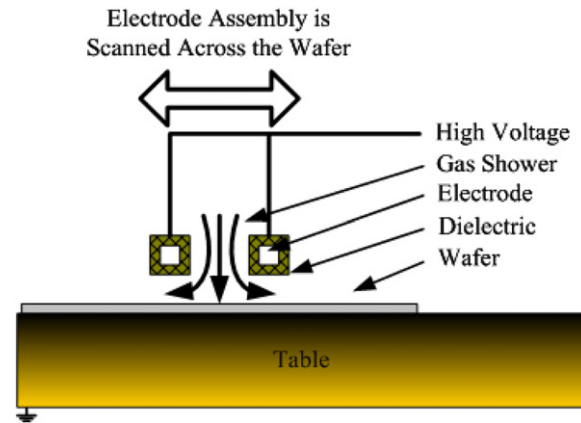
ratio of 1:31 has been achieved in fabricating the geometry shown in figure 6. Feature width reduction refers to the change in the width of the silicon comb-fingers between the top and the bottom, along the thickness of the device. The fabricated devices in figure 6 highlight the fact that the SOS process can be used to make complex structures with pre- and post-bonding processing. In this case, the final device release is performed much later, after first integrating a micromachined two-layer planar coil. It is made by insulating interconnects while sandwiching them between two PECVD  $\text{SiO}_2$  layers, and electroplating a gold coil on top. Finally, the devices are released using DRIE.

#### 4. Characterization of the low-temperature fusion bond

There are two critical process steps in the SOS sequence: the fusion bond and the final plasma etch. However, the process is primarily designed to be insensitive to the complications that arise during DRIE. For this reason, no optimization is carried out with respect to the DRIE etch recipe. By using the same recipe a fair comparison can be made between the different process technologies. This leaves the low-temperature fusion bond as the key step in the SOS process. It allows the process to remain CMOS compatible while abiding with a maximum temperature and associated thermal budget requirements. A good bond is also critical for providing device structural integrity, lowering the thermal impedance of the interface and facilitating heat removal during etching, withstanding further processing steps after the bond, keeping the process geometrically insensitive, and surviving pressure variations between trapped cavities and the wafer exterior. This section is devoted to discussing the details associated with successful completion of the SOS process.

##### 4.1. Plasma activation

It has previously been reported that strong hydrophilic bonding between silicon dioxide and silicon can be achieved at low annealing temperatures ( $< 400^\circ\text{C}$ ) by exposing the wafers to the low-pressure plasma of various gases  $\text{O}_2$ , Ar,  $\text{N}_2$ , and others, prior to bonding [20–23]. This process has been



**Figure 7.** Dielectric barrier discharge creates a uniform plasma discharge due to a high-frequency ac voltage applied between two electrodes. The discharge is scanned across the wafer surface. This process does not damage the surface of sensitive substrates, and when configured in the indirect mode can additionally be applied to electronic devices.

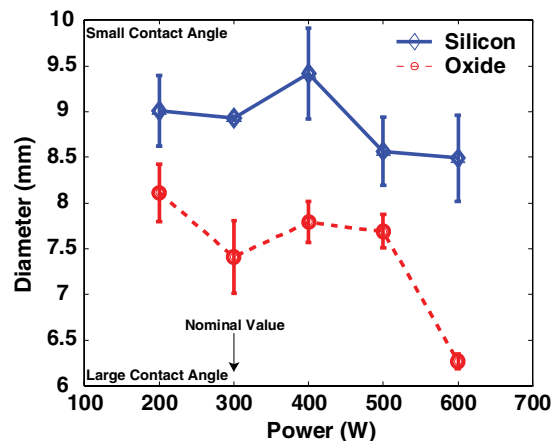
studied and modeled by a number of authors, characterizing the influence of various parameters on the strength and quality of the resultant bond [24–32]. Alternatively, surfaces have been activated by ion bombardment or wet chemical means [20].

Another form of plasma activation, called dielectric barrier discharge [33, 34], is used in this work. Two electrodes, covered by a dielectric, are placed very close to the wafer surface and an ac voltage is applied while surrounding them by a continuous gas flow. This leads to the creation of localized atmospheric pressure plasma micro-discharges with a filament radius of 0.1 mm. Figure 7 is a diagram detailing the electrode assembly and wafer activation process. This whole electrode assembly is scanned across the wafer surface, exposing it to the plasma discharges. In the typical case (direct mode), the ac voltage is referenced with respect to the table upon which the wafer is resting; it can also be applied only between the two electrodes (indirect mode). In this indirect mode, electronic components on the wafer are protected from the electric field. Alternatively, only one of the wafers can be activated, so that the sensitive circuit wafer is protected from the high voltage. The main difference between atmospheric pressure and low-pressure plasma activation is that the latter is dominated by the formation of ions and their interaction with the wafer surface, while the atmospheric pressure discharge does not depend on the action of ions but rather UV radiation and a high concentration of electrons. From the perspective of process integration, this leads to several advantages including the reduced bombardment of the wafer surface by energetic species, and sensitive substrates can be protected from excess heating because the DBD discharge is short.

A significant amount of literature is available pertaining to low-pressure plasma activation and subsequent direct wafer bonding of  $\text{Si-SiO}_2$  and  $\text{SiO}_2\text{-SiO}_2$ : examining the bonding mechanisms [20–22, 25, 31, 32], void formation [29], and surface energy [21, 24–26, 35] as a function of plasma duration and intensity, gas species, bonding time and temperature, and storage time. However, because ambient pressure

plasma activation has only recently been suggested for use in semiconductor fabrication, very little data exists, and so we next characterize this method.

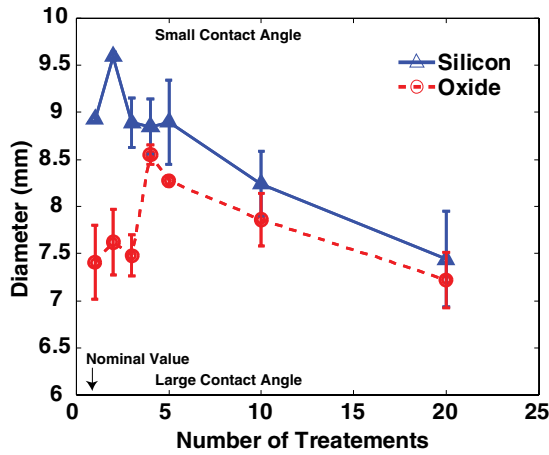
To study the effect that the wide array of DBD process parameters has on the surface quality of the treated wafer, a quasi-contact angle measurement method is used. The contact angle of DIW can be used to measure the surface tension of the silicon or oxide surface. The lower the contact angle, the higher the surface tension and the more hydrophilic the wafer becomes, which is necessary to achieve a high quality bond after annealing at a relatively low temperature. Although the contact angle of water on Si and SiO<sub>2</sub> is highly dependent on the surface preparation, typical values for Si are in the range of >45° and for SiO<sub>2</sub> around 22°. For bonding purposes, the wafer is considered hydrophilic below 25° [22], and to get a high quality bond it would be preferable to get a contact angle below 10°. Because a goniometer was not available to measure the contact angle, another method was used. A droplet of water was placed on the surface of the wafer and a Nikon MM-40 microscope was used to measure the diameter of the droplet after spreading on the wafer surface. The volume of the droplet is controlled precisely using a pipette, and each time 1 μL of DIW was placed on the surface. This way the diameter of the droplet was only influenced by the contact angle and not the amount of water. The larger the diameter of the droplet, the lower the contact angle of the water, and thus the more hydrophilic the surface had become. Two types of samples were used. A number of (100) oriented p-type 10–20 Ω cm silicon wafers were split into two batches. The wafers had undergone RCA1 and RCA2 cleans. Wet thermal oxide was grown on half of them to a thickness of 1 μm. The wafers were then diced into pieces, and cleaned once again in acetone and isopropanol. The Si pieces were dipped in hydrofluoric acid to remove the native oxide, rinsed in DIW, and kept in the bath until just before activation and measurement. The Süss NP12 tool was configured with the following nominal configuration: power was set to 300 W, N<sub>2</sub> gas flow at 50 slpm, the electrode assembly moved at 50 mm s<sup>-1</sup>, the electrode–wafer gap was set to 0.5 mm, and one scan was performed. While each parameter was studied separately, the remaining settings were left at their nominal configuration. The gas flow rate was left at the maximum value through the experiments, because it was believed that a high gas flow would best be able to maximize the N<sub>2</sub> concentrations around the wafer and the electrodes, and minimize the availability of other incident gas species in the atmosphere. After each exposure, a water droplet was immediately applied to the sample, and its diameter was quickly measured to minimize the effect of evaporation. The effect of each parameter was measured three separate times on each type of substrate. After direct exposure using the default configuration, the diameter of the droplet increased over 250% for silicon and 150% for oxide. Results in figures 8–11 summarize the effect of varying the plasma power, scan speed, number of scans, and gap between the electrodes and the wafer. Plasma exposure may affect the silicon in different ways, including the promotion of different chemical reactions, charge injection into the oxide or semiconductor, and of course structural changes may be induced. Although no



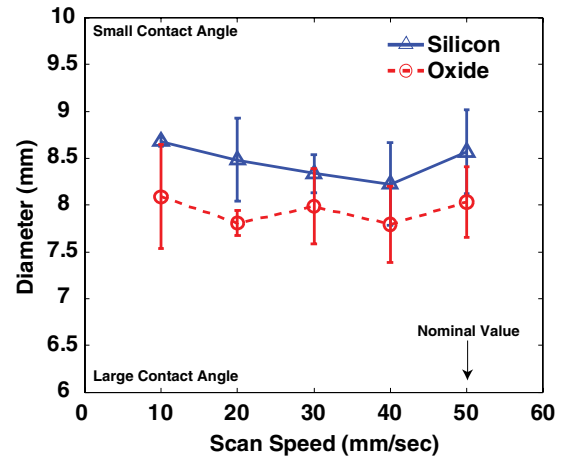
**Figure 8.** The diameter of a water bubble on the surface of silicon and oxide as the plasma power is varied. An optimal point is reached at 400 W for both materials. Underexposure and overexposure both lead to decreased surface energy.

exact explanation of the influence of plasma activation on the bonding properties has been proposed to date, the prevailing theory suggests that an important role is played by the surface treatment in helping rapidly remove water and other gaseous species away from the interface [21, 24, 25]. Regardless of the specific effects of the plasma treatment on the wafer surface and its influence on the bonding mechanism, when the wide body of literature on low-pressure plasma is taken as a whole, it is obvious that an optimal point is evident for the intensity of the plasma activation, intensity in this case being a complex function of plasma power, bias voltage, gas flow and time. While pre-treating the surface has the effect of promoting higher surface energy after bonding, too much exposure to plasma has been shown to have the opposite effect. Although a specific set of reasons for this have not been elucidated, one proven effect is the increased surface roughness due to the prolonged ion bombardment [26, 35]. Wafer pre-treatment using DBD displays similar trends where the diameter of the bubble decreased as the power (figure 8) and the number of treatments (figure 9) were increased. Further, as the electrode gap (figure 10) was increased, and consequently the plasma exposure lessened, the diameter of the bubble decreased. Scan speed (figure 11) did not provide a clear trend. It is theorized that either the selected range of speeds was insignificantly small or since the remaining parameters were set to their default value, the plasma exposure was weak and it was not altered significantly by varying the speed. Figure 9 showing the number of treatments is the most telling. As the number of treatments is increased, an optimal point is reached, and the surface tension begins to decrease after that. An optimal value of plasma exposure is also observed when silicon is exposed to O<sub>2</sub> low-pressure plasma [26]. It was found that the contact angle of water decreased for exposures between 1 and 15 min, and increased for longer exposure. The decrease in the contact angle is attributed to the significant change in surface bond states due to plasma exposure. However, the reason for the subsequent increase in the contact angle is not well understood. In low-pressure plasma two possible reasons are the increase in surface roughness, and for plasma times longer

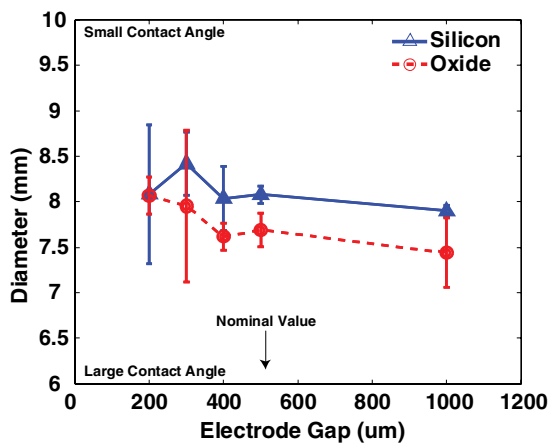




**Figure 9.** The diameter of a water bubble while the number of treatments is varied. An optimal point can once again be found. It is more difficult to make silicon dioxide hydrophilic.



**Figure 11.** How quickly the electrodes move across the surface can again lead to an optimal plasma treatment. It also confirms the trend that oxide needs a higher exposure than silicon.



**Figure 10.** Analysis of the distance between the wafer surface and the electrodes. This plot confirms that oxide needs a higher plasma exposure, showing that as the gap increases the surface energy decreases. The same trend is true for silicon.

than 15 min the wafer temperature was shown to increase to over 270 °C [26]. The reason for the decreased surface tension when using DBD plasma activation is likely quite different. The wafer temperature is not changed because of the short duration of the plasma discharges. Also, it has been reported that the wafer roughness is not modified by DBD plasma [34] after prolonged exposures, a result which is consistent with the observations made during this study as will be discussed in the next section.

It has further been observed that silicon dioxide is more difficult to treat, resulting in the need for a slower scan speed, smaller gap, or more treatments. In figures 8–11, the diameter of the water droplet remained smaller when compared to activated silicon. It has previously been demonstrated that the final bond surface energy is a strong function of the interfacial SiO<sub>2</sub> thickness: the thicker the oxide, the more difficult it is to achieve a high quality bond, and in fact a reduced surface energy of 45% was observed for an increase from 0.1 to 0.9 nm in oxide thickness [27].

While each parameter was studied separately, further studies were performed to deduce what combination yielded the best results. Although it is tempting to draw the conclusion that using the optimal values of each parameter will yield the best plasma treatment, this would be incorrect. Figures 8–11 show the influence of each parameter while the rest are held to a nominal value. Using all of the optimized values together could lead to overexposing the wafers to plasma. As before, p-type silicon wafers as well as wafers with a 1 μm wet thermal oxide were activated, bonded and annealed. The bond and anneal conditions were kept constant, while the activation was varied. Afterward, a razorblade was inserted and used to pry apart the wafers. Bond uniformity was examined qualitatively. When the wafers were pried apart, the SiO<sub>2</sub> would tear through its thickness or completely transfer from the oxidized wafer to the silicon wafer in places where the wafers were bonded well. The best uniformity and bond strength were attained when the wafers are treated at 400 W with 50 slpm N<sub>2</sub>, applied 300 μm above the wafer surface while the electrodes are scanned at 20 mm s<sup>-1</sup>.

#### 4.2. Surface quality

Since surface roughness plays a key role in fusion bonding, measurements of both Si and SiO<sub>2</sub> wafers were performed using atomic force microscopy (AFM) in order to study the effects of plasma activation. AFM measurements were performed in the ‘tapping mode’ with a silicon tip using a Veeco NanoMan system. A typical surface roughness for RCA cleaned silicon is 1 Årms [25], and wafers undergoing hydrophilic bonding should not have a mean roughness higher than 4 Årms [20]. Silicon and oxide wafers with an 0.8 μm wet thermal oxide are measured before undergoing plasma activation, immediately following exposure to one scan of DBD N<sub>2</sub> plasma, and then following an additional 20 scans. The plasma is applied using the optimal conditions reported in the previous section. The results of this study are presented in table 1. A smoothing of the surface of both silicon and oxide can be seen. The reduction in surface roughness after

**Table 1.** Effects of plasma activation on the surface roughness of Si and SiO<sub>2</sub>.

	Si wafer (Årms)	SiO <sub>2</sub> wafer (Årms)
Preactivation	4.2	3.4
1 scan DBD N <sub>2</sub> plasma	0.7	2.7
20 scan DBD N <sub>2</sub> plasma	0.8	1.8

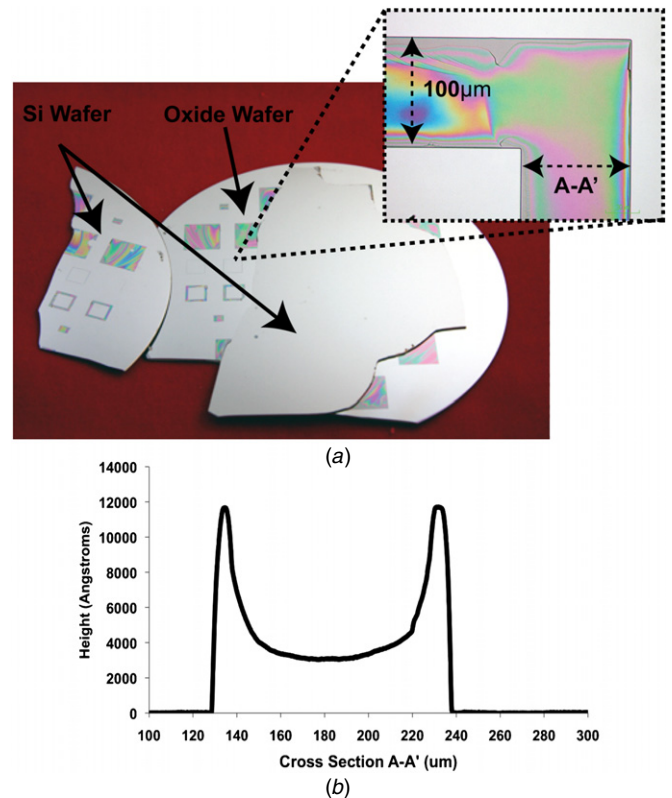
plasma exposure has been reported before [24, 25, 33–35] and is likely due to the removal of hydrocarbon contamination from the surface immediately after exposure. However, the use of large power as in [21] has been shown to increase the wafer roughness. Nonetheless, the ionic bombardment of the wafer surface in atmospheric pressure plasma can be neglected, and no negative effect with respect to surface roughness is expected. That being said, this reduction in surface roughness should not be misunderstood as being a benefit in all cases. As previously demonstrated, prolonged exposure to plasma has other effects which impact the bond quality, including reduction in the surface tension of the wafer.

#### 4.3. Bonding conditions

Similar qualitative studies to the ones used to understand the optimal plasma activation conditions were used to deduce the optimal anneal process. Pure silicon and oxidized wafers were activated using the previously determined optimized plasma treatment recipe, and the conditions such as anneal time and applied pressure were explored. The wafers were again pried or broken apart using a razorblade and studied to find the optimum conditions for high bond strength. The maximum temperature (400 °C) that would allow this process to remain CMOS compatible was used. An anneal time of 4 h was found to be sufficiently long to produce a strong bond such that the wafers would not break apart in the interface, but rather somewhere in the bulk silicon or the Si–SiO<sub>2</sub> interface of the oxidized wafer. This still relatively higher bonding temperature can likely be reduced without deterioration in bond strength if a thinner oxide is used.

#### 4.4. Oxide bond pad feature size

An important aspect of the SOS process is the bonding of patterned oxide substrates. In order to characterize what types of features can be successfully bonded, oxide wafers are patterned to form bonding areas of varying sizes and assorted separations from each other. These wafers were then bonded to plain silicon wafers. A razorblade was used to separate one such bonded wafer pair and the result can be seen in figure 12. The plain silicon wafer is on top. After breaking apart using a razorblade, the oxide is torn through its thickness and part of it is transferred to the silicon wafer. This is confirmed using a surface profilometer and the resultant measurement is shown in the figure inset. The oxide is originally 1.2 μm thick, and after separation one can see that part of the bond ring is torn out and missing from the middle. Features as small as 100 μm were able to bond reliably across the wafer. Additionally, 10 × 10 μm features bonded with sufficient strength to cause oxide

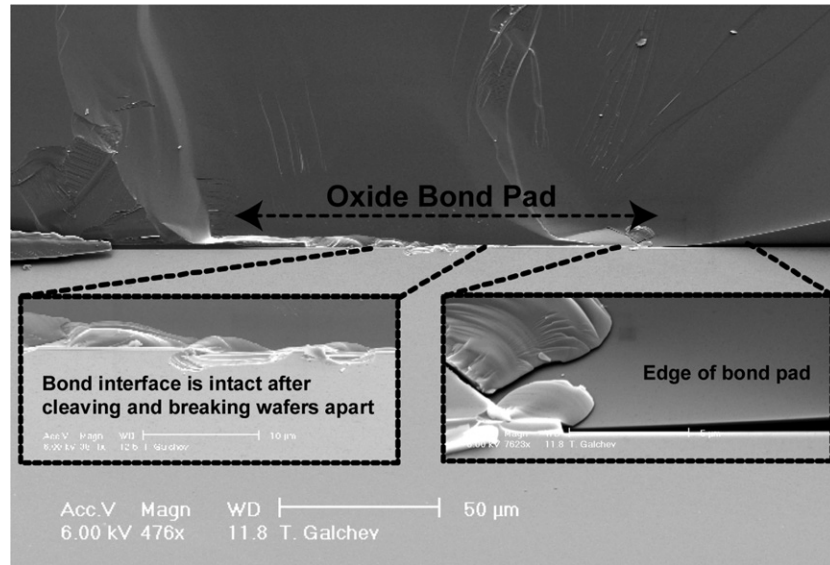


**Figure 12.** (a) Photograph of a patterned 1.2 μm SiO<sub>2</sub> wafer bonded to a plain silicon wafer. The silicon wafer, which is on top, has been pried open using a razorblade and flipped over to reveal that the SiO<sub>2</sub> has torn through its thickness and transferred to the silicon wafer. On the top right a close-up of one of the 100 μm wide bond rings is shown. (b) A surface profile of that bond ring (cross section AA') shows how a significant part of the oxide from the middle is gone.

tearing; however, they were not found to bond with a high yield across the wafer. Nonetheless, 100 μm bond rings and bond pads were able to bond reliably during the plasma activated fusion bond, and they are small enough that they offer the SOS process sufficient layout and geometric flexibility.

#### 4.5. Bond strength

Figure 13 is a SEM showing the bond interface of a patterned oxide wafer bonded to silicon. The two wafers are cleaved and a razorblade is used to break off the top silicon wafer to expose the area where the two are bonded. The SEM clearly shows a very strong bond because the interface remains intact after trying to break off the top wafer, and any breaking occurs in the bulk silicon. In order to evaluate the strength of the fusion bond, an oxidized wafer is activated and annealed under the aforementioned optimal conditions. This wafer is then diced into 5 × 5 mm pieces. Since the shear failure mode typically occurs at a lower stress than when the force is applied normal to the bond interface, the shear strength of the bonded pieces is evaluated. A custom-built [36] shear strength measurement setup is used. The maximum shear stress that could be applied is 50 MPa. At the maximum shear stress, no separation of the two pieces is observed. This strength is more than sufficient



**Figure 13.** SEM of a bond interface between a Si and a patterned SiO<sub>2</sub> wafer. The two wafers are bonded under optimal activation and anneal conditions. The wafer pair was cleaved and further broken apart to give access to the bond interface for inspection. The images reveal that the bond interface remains intact and that any breaking occurs in either the top or bottom silicon.

for many different MEMS sensors, actuators and packaging applications.

#### 4.6. Single-wafer DBD activation

While carrying out experiments to determine the optimal plasma activation and anneal conditions, it was also evaluated if the bond can be achieved by activating only one of the wafers. A number of bonding experiments have been performed when only the silicon was activated. No tangible effect on bond quality and strength was found by performing the razorblade tests as before. Although the shear strength of these bonded wafers was not explicitly measured, the qualitative razorblade test shows that the strength of the interface is as good as the intermolecular bonds of the grown oxide and the bulk silicon. This result implies that in the future it would suffice to simply activate the silicon wafer while the oxide carrier, which might feature sensitive circuitry, would be spared the high plasma activation voltage.

## 5. Conclusion

This paper presented the development and characterization of a new CMOS compatible process for creating high-aspect-ratio MEMS devices based on low-temperature plasma activated fusion bonding. The SOS process technology is based on bonding two silicon wafers with a patterned intermediate silicon dioxide layer at 400 °C, after which DRIE is used for device definition and release. The SOS process provided several advantages over similar technologies, including better etch profile and dimensional control without further processing steps. The two critical process steps are the DRIE final device release, and the low-temperature fusion bond of the carrier and device wafers. Having the ability to pattern the intermediate dielectric before DRIE desensitizes the entire process to the

final reactive ion etch processing and associated challenges. In order to achieve this patterned interface while keeping the process CMOS compatible, a low-temperature plasma activated fusion bond is developed. The plasma treatment relies on a new DBD atmospheric plasma discharge. The bonding process is characterized in detail. A uniform bond can be formed by applying N<sub>2</sub> plasma to both wafers at 400 W while scanning the electrodes 300 µm above the wafer surface at 20 mm s<sup>-1</sup>. The two wafers are subsequently annealed at 400 °C for 4 h. This recipe leads to a very strong bond (>50 MPa shear yield strength). A strong and uniform fusion bond provides good structural integrity for the devices, as well as low thermal impedance at the anchor, and is critical for SOS processing and using the technology to make precision devices.

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