Charge Pump Power Conversion Circuits for Low Power, Low Voltage and Non-Periodic Vibration Harvester Outputs

by

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Abstract

The primary goal of this research is to develop circuits capable of cold start, boosting, rectifying and storing the harvested energy of mechanical vibration harvesters that have outputs that are low power, low voltage and non-periodic. The techniques developed to overcome the diode drops inherent in rectification are critical contribution of this research. New techniques for high efficiency low voltage functioning and sub-threshold start-up are introduced. Additionally, the circuits work with the up-conversion based harvester "The Parametric Frequency Increased Generator (PFIG)", which is designed to harvest vibrations found on bridges or under bridge-like conditions tested in a lab setting. The goal of energy harvesting from bridges or other parts of the nation's infrastructure is to power bridge health monitoring sensors that could be placed throughout the bridge in difficult to reach locations where battery replacement would be expensive or dangerous.

This research investigated the feasibility, from the circuit side, of harvesting the low power, low voltage and non-periodic outputs of harvesters, which are actuated by vibrations from cars passing on a major suspension bridge or similar vibrations from other parts of the nation's infrastructure (i.e. buildings). On a suspension bridge vibrations are non-periodic and range in frequency between approximately 2 Hz and 30 Hz and have accelerations that are regularly in the range of 10 mg and 100 mg. Typically, the PFIG up-converts these low bridge vibration frequencies (2 – 30 Hz) to near 110 Hz. This happens even if the PFIG is actuated over a wide range of frequencies. Higher PFIG voltages are seen if the PFIG is actuated with a higher bridge acceleration or frequency.

The contributions of this research are: 1) The development of innovative IC harvesting circuits for electromagnetic vibration harvesters capable of enabling active diode charge pumps to record high boosting**,** high power harvesting efficiency, low power functioning, and record low input voltage functioning in a boosting circuit; 2) The use of sub-threshold functioning to enable a boosting low voltage active diode cold start-up on an IC-based energy harvesting circuit utilizing the unique start-up properties of charge pumps; 3) The use and study of discrete passive circuit solutions for vibration harvesters with record low voltage and low power outputs; and 4) The testing of these circuits under bridge-like conditions or on a real suspension bridge. While there is a specific real world motivation for the development of these circuits, continued investigation into these circuits will advance the state-of-the-art in the design and understanding of vibration harvester circuits such as the charge pump, sub-threshold design in start-up circuits, the use of discrete circuits in energy harvesting, and the testing of a harvesting system in a harsh real world environment. The innovations and learning from this research will be applicable to many other areas of energy harvesting circuit research where an AC input or clock is harvested.

In this abstract, work is presented on discrete circuit solutions developed to boost, rectify and store the power generated from the PFIG, with actual bridge results from short-term tests and long-term tests including a year-long test of a harvesting system on a suspension bridge in California. Also, the results and novel architecture of fabricated IC-based charge pump systems with multiple innovations relating to a lowest voltage stage driven active diode charge pump are presented. These active diode charge pumps use the unique start-up behavior inherent to a charge pump with large capacitors that is both harvested and is clocked by its input to aid deep sub-threshold active diode start-up. These fabricated IC systems allow for ~×6 or ~×16 boosting down to an ideal sinusoidal signal of ~110 mV under regular operation and can cold start-up with

a minimum ideal sinusoidal input of 220 mV. Both the minimum input voltage necessary for start-up and regular functioning operation represent records for an energy harvester circuit capable of boosting from a vibration harvester in the literature. The maximum power conversion efficiency of the circuit is near ~68% with sinusoidal operation, which is comparable to other state-of-the-art boosting circuits. Also, the IC is capable of start-up with PFIG based signals occurring at actuations of 4.5 Hz with an input peak of 415 mV (versus 220 mV with an ideal sine-wave) and has an estimated efficiency with a PFIG-like signal of near 50%.

This thesis analyzes the discrete and IC-based charge pump harvester. It also demonstrates their unique functioning with low voltage and low power inputs, including the challenges and opportunities of using discrete components (passive charge pumps and transformers) to achieve ultra-high boosting or using active diode sub-threshold functioning to enable sub-threshold active diode start-up. Finally, potential improvements to these systems and future work building on the concepts in these systems are discussed.

Chapter I

Introduction and Literature Review

There are multiple energy sources that can be utilized on a bridge, including solar, thermal, radio frequency (RF), and mechanical energy. Each of these methods has benefits and drawbacks. Solar energy is presently being used to power Structural Health Monitoring (SHM) nodes on bridges, including the previously mentioned New Carquinez Bridge [1]. Solar panels produce sufficient power on sunny days for regular sensor data collection and transmission, but power is limited or non-existent during the night, cloudy periods, or when excessive dust accumulates on the solar panels. For SHM nodes at interior points or under the bridge deck, wiring must be routed from the solar panels on the bridge surface to the sensor locations, adding significantly to the system complexity and cost. Thermal harvesting from the temperature difference between the bridge surface and the outside air has been investigated and shows promise [2]; however, the available temperature difference varies and can be very small, making reliable harvesting a challenge. RF harvesting also has been investigated [3]; however, little RF power is typically available in the environment due to the rapid attenuation away from distant transmitters. Solutions using dedicated RF transmitters in close proximity to or on the bridge can supply considerably more power to the RF harvesters [2]; however, their installation may not always be feasible. While each of these harvesting methods has certain advantages, none of them alone supplies the continuous energy needed to power wireless sensors throughout the bridge. This motivates the need to investigate other sources of harvestable energy.

Vibration energy harvesting may be an effective way to power wireless SHM sensors by harvesting power during periods of high traffic and storing that power for later use. A resonant vibration harvester for powering a bridge SHM sensor [4] has been demonstrated, where the resonant frequency of the harvester was tuned to a modal frequency of the bridge at the specific sensor location to obtain optimal performance for one week. Studies show that bridge resonant frequencies can vary significantly from bridge to bridge or between positions on the bridge [2], so it may be difficult to broadly apply resonant harvesters. The non-resonant PFIG, introduced in the Abstract, is capable of working on a bridge with a range of frequencies without tuning; however, it produces a low-power, low voltage, decay sine-wave outputs that are actuated non-periodically

A harvester and interface circuit that harvests the vibrations on a large suspension bridge to supply bridge health monitoring sensors is an example of a system with a harvester that produces a low power, low voltage and non-periodic output signal that will often need to start from a capacitor at near 0 V (for example after a quiet night with little traffic) [1, 5]. The basic circuit solution to interface with the bridge vibration harvester is the classic passive half-wave charge pump [6]. Other better and more complex circuit solutions are possible and will advance the state-of-the-art, but they have not been investigated in the literature. Better circuit solutions will also allow complete testing of a vibration harvesting system on a bridge, including a long-term test, because enough power can be generated to make a meaningful assessment of the efficacy of the system. A long-term test on an actual bridge could not have been completed without an improvement over the initial passive charge pump vibrational harvester circuit [6].

From the purely circuit side, transformers matched to the high output impedance (300 Ω - 1500 kΩ) and low frequency signals (100 – 110 Hz), which output from a harvester based on the low acceleration actuations present on a bridge, have been used only by this author as part of an overall system [7]. Other energy harvesting literature only analyzes transformers matched to harvesters with an output impedance of (3 - 4 Ω) at low frequency outputs [8-10]. These transformer-based circuits matched to high output impedance warrant more investigation. However, the most interesting and potentially beneficial area of circuit research investigates the opportunities and obstacles of transitioning the classic Cockcroft-Walton charge pump [11] into an active diode IC based system. Little work has been done with active diode IC's and this classic charge pump architecture other than purely discrete active diode charge pumps [12, 13] that rely on passive diodes for start-up. The classic charge pump's start-up is unique because during the start-up the stages of the charge pump are charged at different rates. This concept is described in section 1.3. In an IC-based system, advancement in the state-of-the-art can be made in the circuit's sub-threshold functioning during start-up using the unique characteristics of this charge pump. Additionally, advancements can be made in the start-up operation and regular operation relating to high power conversion efficiency, low power operation, and mitigation of the effect of the loading on the charge pump's start-up.

1.1 Expected Thesis Contributions

There are four main contributions in this thesis. First, there is the development of innovative IC harvesting circuits for electromagnetic vibration harvesters capable of enabling active diode charge pumps to record high boosting (10x – 16x), while maintaining high power harvesting efficiency (>50 %) , low power functioning (<1 μW) and record low input voltage functioning in a boosting circuit (<150 mV). Second, sub-threshold functioning will be used to

enable record cold-start-up on IC energy harvesting circuits that boosts based on ultra-low voltage inputs (<250 mV voltage for start-up). This start-up would enable boosting out of sub-threshold and into regular operation without the use of passive diodes while relying on the unique characteristics of charge pump operation for sub-threshold active functioning. Third, there is the development, use and study of discrete passive circuit solutions that are capable of boosting, rectifying, and storing the harvested PFIG outputs or harvesters with record low voltage (<60 mV), high output impedance (~300 Ω) and low power outputs (<5μW) . These circuit limitations will be explained including the Schottky diodes turn-on voltage, voltage mismatch, the transformers ability to match to the harvester's output impedance, and transformer efficiency. Finally, these circuits have been tested and will continue to be tested under bridge-like conditions or on a real suspension bridge. This includes the installation and testing of short-term and long-term systems on a suspension bridge with the PFIG and electronics. This long-term test lasted over 1 year. The following thesis discusses these contributions and relevant background emphasizing their value and their advancement to the state-of-the-art.

1.2 Up-conversion Based Harvesters

Low frequency vibrations have been shown to be efficiently harvested by compact mechanical harvesters using the concept of up-conversion [14] introduced at the University of Michigan in a micro-vibration harvester. The original idea behind mechanical up-conversion is that low frequency vibrations can be up-converted to higher frequency vibrations, so there is better energy conversion efficiency when harvesting these lower frequencies. To accomplish this, a mechanical cantilever resonates when actuated by low frequency vibrations and a magnet and coil on the cantilever generates current, voltage and power. The voltage output of this coil takes the form of decaying sinusoids that occur based on low frequency vibration actuations [14].

This up-conversion idea can be generalized to a larger mechanical harvester that is more suitable for scavenging bridge vibrations. Previously, the Parametric Frequency Increased Generator (PFIG) has been introduced at the University of Michigan. Multiple versions of the PFIG have been published, including a bench-top version [15] and smaller self-contained piezoelectric and electromagnetic versions [16, 17]. In the last publication a PFIG for bridge SHM was introduced (PFIG-B1) [6]. It consists of a large inertial mass that snaps back and forth between two "Frequency Increased Generators (FIGs)". Each FIG consists of a latching magnet glued to a spring on top of which is another power generation magnet. The latching magnetic of an individual FIG attaches and detaches from the inertial mass as bridge vibrations occur. The power generation magnets are surrounded by coils that have output impedance ranging between 300 Ω [7] to 1.5 kΩ [6]. When the large inertial mass detaches from a FIG, the power generation spring vibrates at an up-converted frequency generating current and power in the coil surrounding the power generation magnet. Figure 1 shows the architecture of the PFIG and describes its functioning. The entire volume of the PFIG-B1 is minimized to be about the size of a "D" cell battery (<68 cm^3).

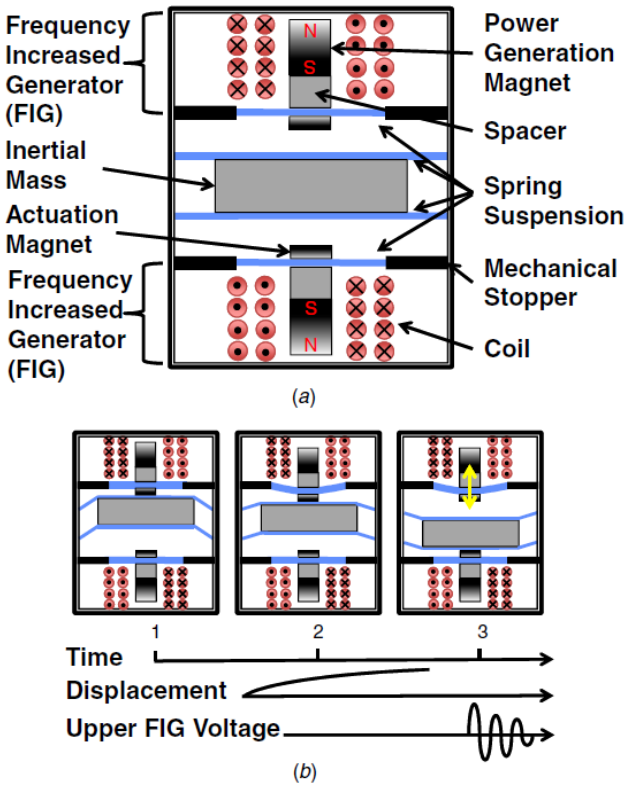

Figure 1. The diagram of the PFIG is shown in (a), while the functioning of the PFIG is shown in (b) where the inertial mass snaps back and forth between FIGs when actuated by a bridge vibration [6].

The PFIG was tested on the New Carquinez (NC bridge) suspension bridge in California. The PFIG was attached to the bridge by first attaching it to a plastic plate that was then magnetized to the bottom of a suspension bridge as seen in Figure 2. The parameters of this first bridge based harvester presented a considerable challenge to the interface circuitry. These parameters included an output impedance of 1.5 kΩ and matched output voltages that regularly reached a peak of 200 to 300 mV based on bridge accelerations measured on the NC Bridge. Average power recorded on the NC bridge, with the PFIG alone, ranged between 0.47 µW and 0.75 µW. Better results were seen in the lab under steady conditions, including 2.3 µW at 2 Hz and 0.54 m s^{-2} actuation and 57 µW at 10 Hz and 0.54 m s^{-2} [6]. There are two versions of the PFIG capable of bridge harvesting. The first version of the PFIG capable of bridge harvesting

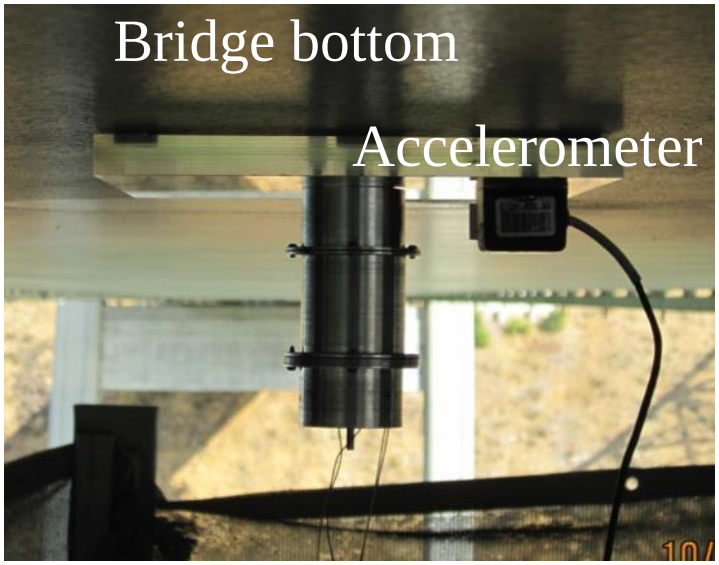

Figure 2. The PFIG is attached to a plastic plate which is magnetically attached to the bottom of the NC bridge. An accelerometer is included to measure the vibrations which actuate the PFIG.

was just described [6]. From now on this first version will be referred to as PFIG-B1 and the second version, described in Chapter 2, will be described as PFIG-B2.

1.3 The Classic Passive Cockcroft-Walton Multiplier as Harvesting Circuit

1.3.1 Start-up Functioning in a Cockcroft-Walton Multiplier

The start-up of the Cockcroft-Walton charge pump is unique in circuit design. For instance, an input signal clocks the charge pump while being harvested and boosted by this charge pump at the same time. The charge pump works by cascading a series of voltage doublers and using the diodes as switches to enable charge to flow from the capacitors nearest to the input to the capacitors farthest from the input raising the voltage at the output of the charge pump. The conventional way that the charge pump is drawn in the left diagram of Figure 3 is not intuitive in that it doesn't clearly show how the diodes (switches) enable the cascaded voltage doublers. If the diodes (switches) all have same orientation and are lined up in the center of the charge pump, it is clear to see how the different paths are formed by periodically switching alternate diodes. These alternating paths are shown with solid and dashed ovals. From these diagrams in Figure 3 it is clear that the initial stages of the charge pump (the stages closer to the supply) naturally

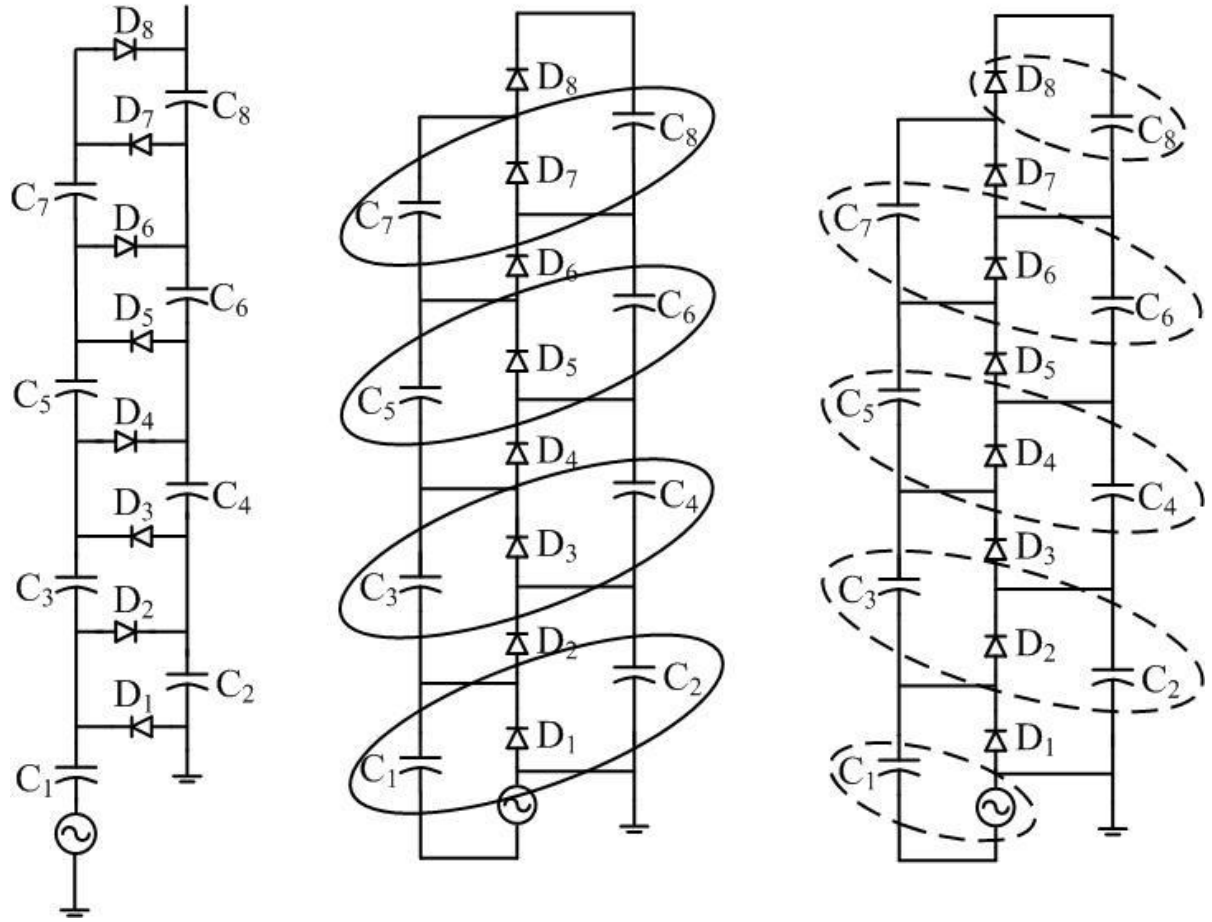

Figure 3. The left diagram shows the standard way the charge pump is drawn, while the middle and right diagrams show the switches (diodes) oriented the same in the center of the charge pump. The current paths for the charge part are now visible for a negative signal (center diagram) and positive signal (right diagram).

charge first. This process can be described as follows. First, capacitor C_1 charges as the diodes D1 and D2 act like switches. D1 is on and D2 is off with a positive sine-wave input to allow C1 to charge from the input. Next, diode D1 is off and D2 is on. This allows for the capacitor C1 to no longer charge from the input and the charge on C1 to be split between capacitor C1 and C2. After the next switch, the charge in C2, which is approximately half of what was originally on the capacitor C1, is connected to C3 and the charge is split once again between C2 and C3. The charge pump start-up is illustrated in Figure 4. It shows how the charge initially flows in a charge pump. In the initial charging the first stages of the charge pump will charge more quickly first until the charge pump can move into a more steady stage operation.

The two graphs in Figure 4 show LTspice simulations of an ideal four stage Cockcroft-Walton half-wave rectifier charged over 1 second. In this simulation, the capacitors are all 100 μF, the diodes are ideal, and are driven by a sine-wave modeling a harvester with a 300 Ω input impedance. On the bottom of Figure 4, a graph shows the total combined voltage at each stage as the charge pump charges. The bottom graph demonstrates that it takes until 0.2 V and 0.3 V for the top stages starts to separate from the rest of the stages; however, by the end of 1 second all of the stage's voltages have separated and the top stage is nearly charged to 0.7 V. The top graph in Figure 4 shows the separate voltage across each stage in the charge pump. Initially, no charge is built up on the last stage, farthest from the input to the charge pump, while significant charge is built on the first stage closest to the charge pump. It takes nearly 0.1 seconds until the charge pump's last stage starts to charge as seen on the top of Figure 4. In the time that it takes for the charge pump to reach 20 mV, the output of the charge can reach up to ~0.25 V. This uneven charging in a charge pump is an inherent quality of the charge pumps.

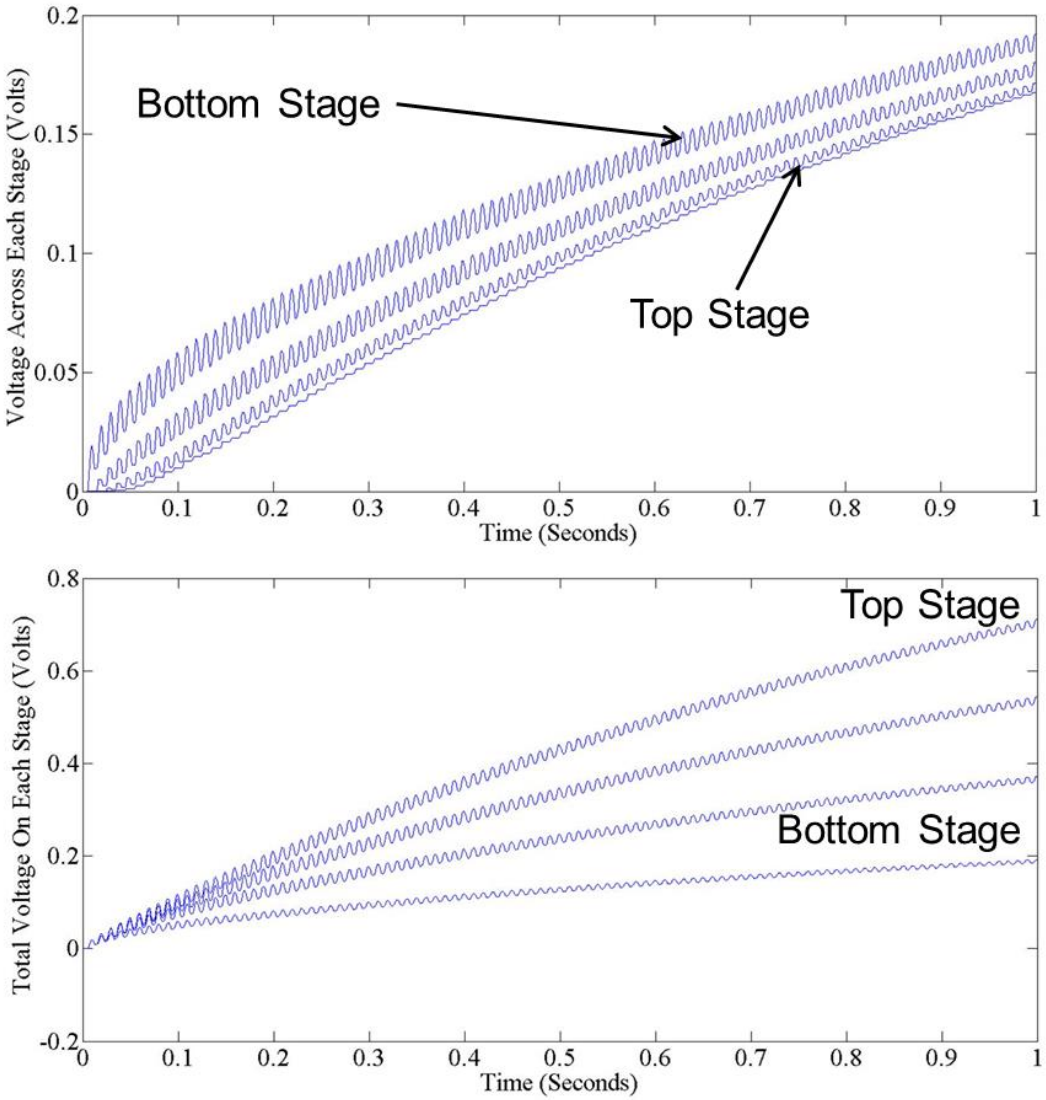

Figure 4. A Cockcroft-Walton start-up is shown with ideal diodes simulated in LTspice. The bottom graph shows the voltage on all the stage of the charge pump while the top graph shows the voltage across the stages on the charge pump.

The fact that a charge pump that is both harvested and is clocked by its input unevenly charges its stages can be used to enable low voltage start-up in far more advanced circuits. In other words, the charge pump behavior during start-up is always changing. Initially, the stage farthest away from the input to the charge does not charge. Midway through start-up, the voltages farthest away from the input in the charge pump begins to charge pump while the stages closest to the charge pump input are well charged. Finally, as demonstrated in Figure 4, as the

charge becomes more fully charged, the charge across the stages becomes more nearly equal. However, for this author's initial design as described in Figure 5 in the next section, all that mattered was that a charge pump could passively start-up and boost an input voltage. The intricacies of the charge pump functioning and start-up will be analyzed later and used to enable an IC-based active diode start-up.

1.3.2 The Cockcroft-Walton Multiplier as a Harvesting Circuit

The classic Cockcroft-Walton multiplier [11] with passive diodes was the first solution this author used to boost, rectify, and store harvested power from a system containing the PFIG-B1 [6]. A schematic of the discrete passive circuit used is shown in Figure 5. Each stage acts as a

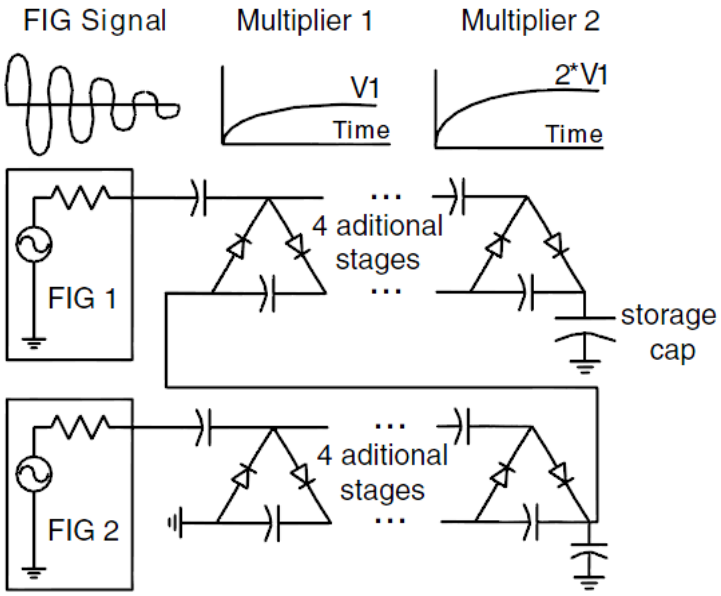

Figure 5. Shows the original circuit used with the PFIG. Both outputs of the PFIG are fed into 6 stage Cockcroft-Walton multipliers. The multipliers are cascaded [6].

voltage doubler. This particular configuration cascades the multiplied outputs of both FIGs of the PFIG to increase the maximum boosted voltage from the circuit. The voltage multiplication from the original circuit is given in the equation below:

$$V_{out\_original} = 2 \times V_{out-CW} = 4 \times n \times V_{Peak} = 24 \times V_{peak}, \quad (1)$$

where n is the number of stages per multiplier, V_{peak} is the unmatched input peak voltage, and $V_{out\text{-}CW}$ is the output of a single Cockcroft-Walton charge pump. The factor of four comes from boosting the two serially cascaded Cockcroft-Walton multipliers. Six stages were chosen based on simulation, so that a PFIG output with a peak near 375 mV at 2 Hz would reach 2.4 V in approximately 60 seconds [6]. Simulated efficiency for this solution at an output of 2.4 V was given as 13% [6]. While this solution was functional in a lab setting, to harvest actual bridge based outputs, the low power of the non-periodic PFIG vibrations on the bridge along with the low efficiency of the circuit [6] meant that the initial circuit was unable to consistently work on the bridge. This motivated the author to develop other circuit solutions better able to overcome the diode drops.

The PFIGs circuit interface inability to start-up and function at high efficiency is a main motivator behind this author's research. As just mentioned, the diode drops of the charge pump limit the start-up and regular function. As indicated by the contributions of this thesis, either transformers or active diode functioning can be used to overcome the diode drops. Transformers can be matched to an improved PFIG with an input impedance far lower than 1.5 kΩ used in PFIG-B1 such as 300 Ω used in the PFIG-B2. While this matched transformer performance is still not ideal because the input impedance from the harvester is still very high, the study of the system using this transformer is valuable and gives useful preliminary data from a complete system functioning on a bridge. To use active diode function during start-up requires deep sub-threshold functioning, which presents major problems in the works presented in literature [18-20] so far and will be discussed in Section 1.4.1. Specifically, at such low voltages (0.2 – 0.3 V) on the supply and low power input from the PFIG (5 – 10 μW), sub-threshold functioning in an active diode system will cause considerable problems. Further, very limited opportunity is

available for active circuit manipulation or logic functioning to correct for the sub-threshold functioning issues that arise during functioning. As previously mentioned in the second expected thesis contribution (Section 1.1), part of the focus of this thesis is to utilize the uneven charging and changes in the behavior of a charge pump that inherently occur in start-up to aid active functioning. A specific IC circuit architecture can be built to make use of this uneven charging in the different charge pump stages to enable active diode start-up in deep sub-threshold.

1.4 Literature Review of Energy Harvesting Circuits

1.4.1 Sub-threshold Functioning in Energy Harvesting

A major goal of this research is to enable sub-threshold active diode start-up in a Cockcroft-Walton multiplier for vibration harvesting circuits. Before going into a total overview of energy harvesting literature, it is useful to look at that few energy harvesting IC-based works that are designed to function in deep sub-threshold with vibration harvesters. These are rectifier circuits rather than LC boost or charge pump circuits. While the rectifier circuits are limited by not being able to boost, the lessons learned from these sub-threshold rectifiers for vibration harvesting are useful, as a boosting sub-threshold based active diode charge pump is designed that both is clocked by and harvests its input.

Relevant work in sub-threshold circuit functioning and start-up in energy harvesting interface circuits using IC technology [18-20] shows that active deep sub-threshold behavior is possible with increasing challenges as lower and lower voltages supply the circuits. Because of these challenges, there has not been a system that can both start-up and function in deep sub-threshold while at the same time producing high efficiency operation at a low input voltage low power input signal once the system has started. The basic problem is that in deep sub-threshold

only minimal functioning is possible even at the low frequencies (i.e. ~130 Hz) produced by the PFIG. The exponential equation representing sub-threshold operation is given below [21]:

$$I_D = I_0 \left(\frac{W}{L}\right) \times e^{\frac{qV_{gs}}{nkT}} \quad (2)$$

From this equation, multiple reasons are seen to make sub-threshold operation far more difficult. First, the change in the current through an amplifier or comparator will create far less of a change in V_{gs} compared to when the device is functioning in saturation. Saturation is described using a square law below.

$$I_D = I_0 \left(\frac{W}{L}\right) \times \left(V_{gs} - V_{th}\right)^2 \quad (3)$$

This means that for low sub-threshold current, both a larger change in the current and a faster change in the current are needed for functional sub-threshold operation. Simply put, far more margin is needed for the system to function in deep sub-threshold operation. Secondly, from this author's experience it has been seen that models over process for deep sub-threshold often do not accurately reflect hardware results. Finally, mismatch in the system due to layout or processing variations can change current in a differential amplifier more readily because of the exponential relation to V_{gs}. This mismatch will potentially mean that sub-threshold operation is more likely to fail or have a large variation in functioning because of mismatch in differential comparator structures used in the system.

Energy harvesting systems have been built that either work on the cusp of sub-threshold and saturation operation or deep in sub-threshold operation; however, additional circuit techniques, structures or system modifications are needed to enable these circuits to work. Additionally, no work has been done showing sub-threshold start-up ability in a circuit or system that can both boost and harvest a low power low voltage input while operating in deep sub-threshold operation.

There are several examples of sub-threshold operation allowing for start-up in literature, and understanding the techniques and limitations in these systems is critical. A negative voltage converter and half wave rectifier allow for an input signal with a peak of 380 mV to start-up and a regular input signal of 500 mV to function at high efficiency [20]. These voltages mean that this system works at the border of sub-threshold functioning in this technology (0.35µm). This is shown in Figure 6. The diode-based negative voltage converter is limited to functioning with an input voltage in between 340 - 380 mV. Similar to other works that use this same architecture [20, 22], initial active functioning is enabled as the positive voltage from the negative voltage converter overcomes the V_{th} of the PMOS portion of the active diode, even when the active diode is not functioning. As the minimum functioning of 380 mV is so close to the threshold of the system, an additional PMOS diode is installed labeled "MPBD" compared to other higher voltage applications of the same architecture. This helper diode "MPBD" effectively lowers the V_{th} that the input voltage from the negative voltage converter must overcome to function. Once this active system is enabled in active operation, it functions with high efficiency near 500 mV. This means that the comparator in the system functions adequately in moderate sub-threshold operation where this supply of (500 mV) must at least allow proper function for two devices (a PMOS and a NMOS) in a comparator switching the active diode.

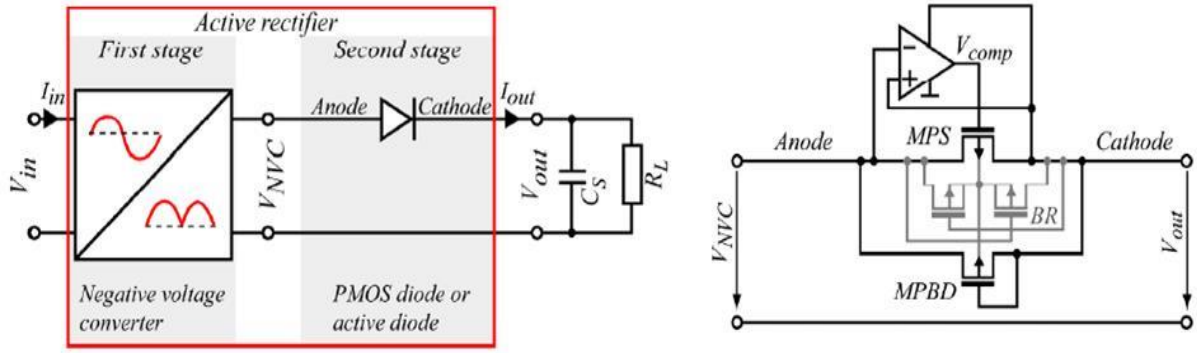

Figure 6. On the left, the top level is shown with a negative voltage converter followed by a half wave rectifier. On the right, the active diode rectifier is shown with a helper diode (MPBD) [20].

Other sub-threshold harvesting circuits are built that are capable of functioning at as low as a 200 mV supply [18, 19]; however, external diode based structures are needed for start-up and in one case an additional input is needed to supply the source power through an external Schottky diode charge pump [19]. In either case no efficiency results are given at low input voltages (100 – 200 mV) that, at maximum, are supplied by ~200 mV, which has been harvested and stored on integrated capacitors. This is likely because of very low efficiencies and difficulties operating in deep in sub-threshold (i.e. the inability of the low sub-threshold current to quickly switch the comparators). In the case of a fully integrated solution seen in Figure 7 reported active functioning with approximately ~200 - 250 mV across the comparators with a 100 mV input voltage, an integrated passive diode structure labeled "AC/DC Doubler with Passive Diodes" is necessary to enable even basic start-up. Again, no efficiencies are reported at these deep sub-threshold voltages. In this case, the conference paper [18] lists the entire system as an "integrated solution" meaning that the capacitors storing charge are "on-chip", so they are likely in the ~1 pf range. For a harvester producing several µW of average power, sub-threshold functioning alone through diodes (without active diode functioning) may be enough to charge ~1 pf capacitor. While this structure start-ups with as low as a ~140 mV peak input, it is unclear if large capacitors (in the ~µF range) can be charged with this system. Conversely, it is unclear if the active diode functioning would even be necessary to charge the ~1 pf integrated capacitor in this system, so that it is unclear how well the active diode rectifier is working with peak inputs between 100 and 200 mV.

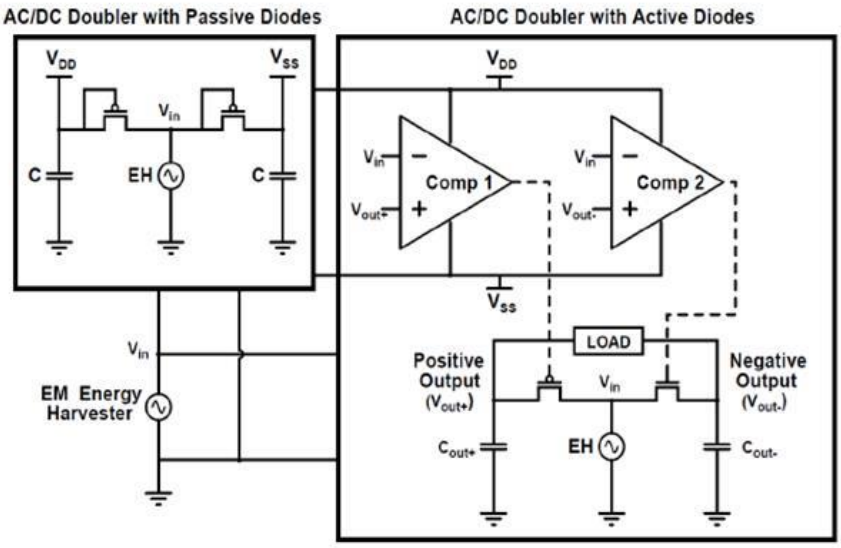

Figure 7. Shows a doubler active diode circuit where start-up is enabled by passive doubler structure. All functioning is necessary in deep sub-threshold [18].

Another major weakness of this architecture is its inability to boost. This is not a charge pump, so the only way that boosting is possible is by using an additional LC boost circuit. To effectively boost a DC voltage, a clock signal with adjustable duty cycle in the range of ~10 MHz must be generated. This is generally not possible in deep sub-threshold, so a properly biased clocking system capable of duty cycle adjustment is needed to generate this signal clocking if the signal in the range of ~10 Mhz. This system combining this active diode doubler with an LC boost circuit was previously built using discrete components before publication of this doubler as a sub-threshold circuit. To understand the limitations of the sub-threshold doubler alone, the previously published work using this doubler structure[23] is reviewed in this Introduction. The doubler diode structure used in this sub-threshold rectifier [18] was nearly identical to the previously mentioned structure used to provide a DC voltage that could be boosted with a LC boost circuit [23]. This system is shown in Figure 8. In this diagram the same rectifier structure is used; however, instead of the comparators in the active diode voltage structure being supplied by the output of the doubling active rectifier, they are supplied by the

output of the LC boost circuit that also powers the clock, with adjustable duty cycle. This circuit is unable to start-up without a high voltage near 1.25V. This start-up is enabled even without active functioning by the passive diodes in both the doubler structure and the LC boost circuit. This very high peak to peak input voltage is needed to enable a high DC output voltage on the output of the LC boost circuit that then can enable functioning in saturation of the clock with adjustable duty cycle that powers the LC boost circuit. Demonstrating these difficulties with

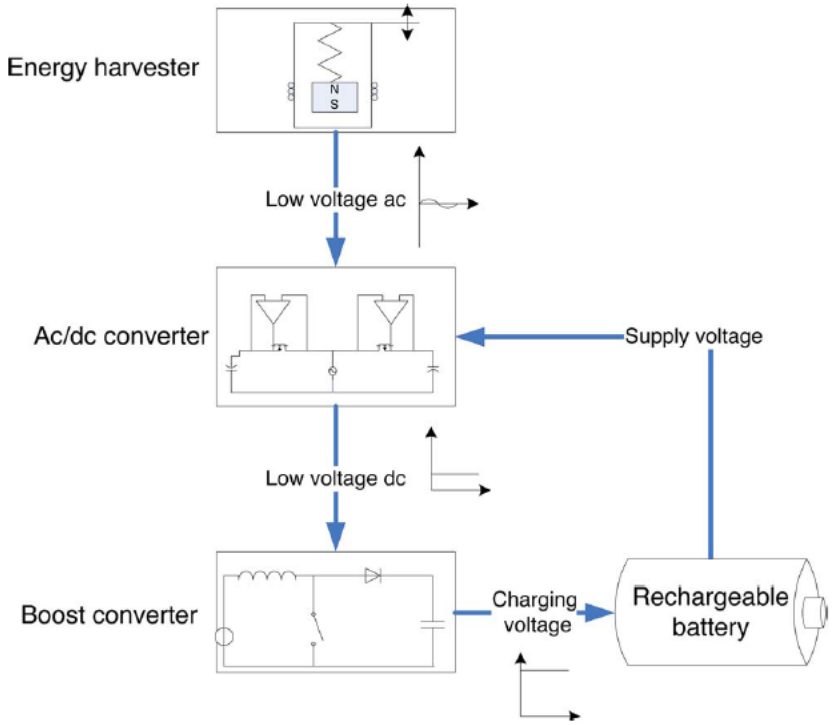

Figure 8. Shows a voltage doubler combined with a LC boost circuit built from discrete components [23].

start-up and boosting of this structure shows the limitations of LC boost circuit enabling start-up in deep sub-threshold functioning and the limitations of using just this doubling structure alone as a sub-threshold harvesting circuit [18].

To summarize sub-threshold literature, sub-threshold harvesting is possible yet limited. Only marginally functional vibration harvesting circuit interfaces have been reported that actively function in deep sub-threshold. There have been no reported works capable of boosting

using active sub-threshold operation from a vibration harvester output. Additionally, high efficiency operation charging to useful large capacitors has not been reported in sub-threshold operation with a vibration harvester input. As discussed previously in section 1.4.1 high margin is needed to enable sub-threshold functioning. Therefore, it is not surprising that only limited sub-threshold operation is possible for sub-threshold based active diode vibration harvesting circuits. A significant contribution presented in this thesis is the use of this limited sub-threshold functioning to allow for start-up in a harvesting system that can both enable an active boosting start-up with low voltage low power input voltages and high efficiency operation once the system has started.

1.4.2 Overview of Vibration Energy Harvesting Circuit Literature

Numerous energy harvester circuit solutions have been published, which are capable of bucking, rectifying, and boosting an AC input signal (Figure 9). Bucking circuits are possible with either a transformer or a clocked inductor based circuit. Boosting circuits can be built using

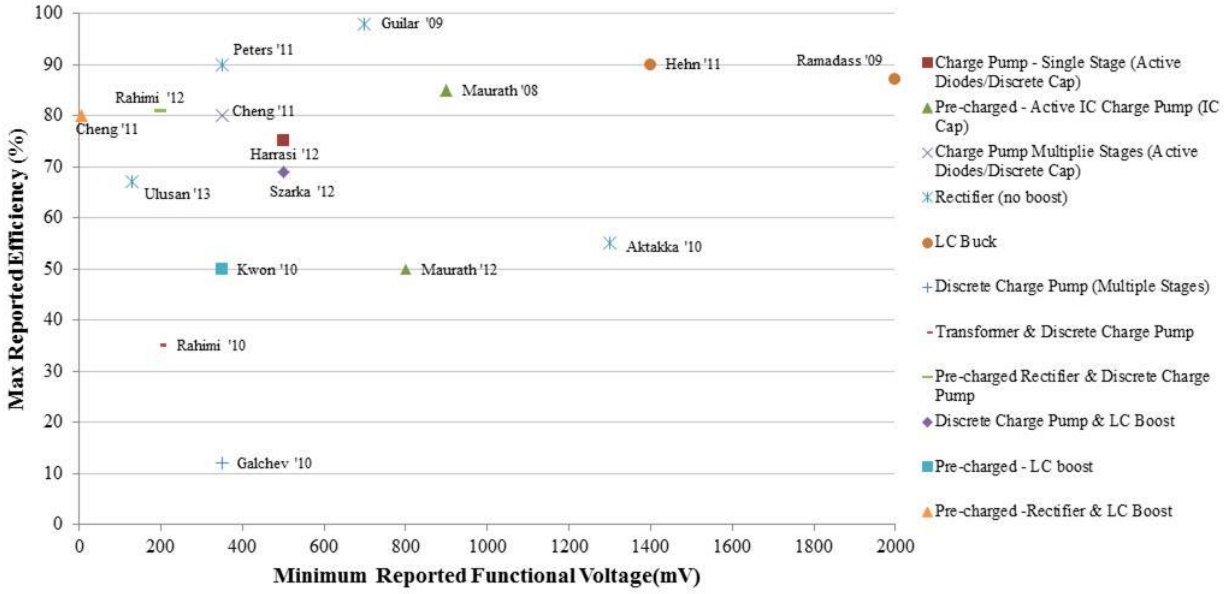

Figure 9. Shows the numerous circuits used to interface with vibration harvesters including the circuits that can boost, buck and rectify.

a transformer, clocked inductor based circuits, or charge pumps. A key requirement of circuits built for vibration harvesters on bridges is that they can cold-start and boost. Because of this requirement, this thesis focuses on boosting circuits capable of start-up as described in the Abstract and Introduction. Relevant vibration energy harvesting literature's (either journals or

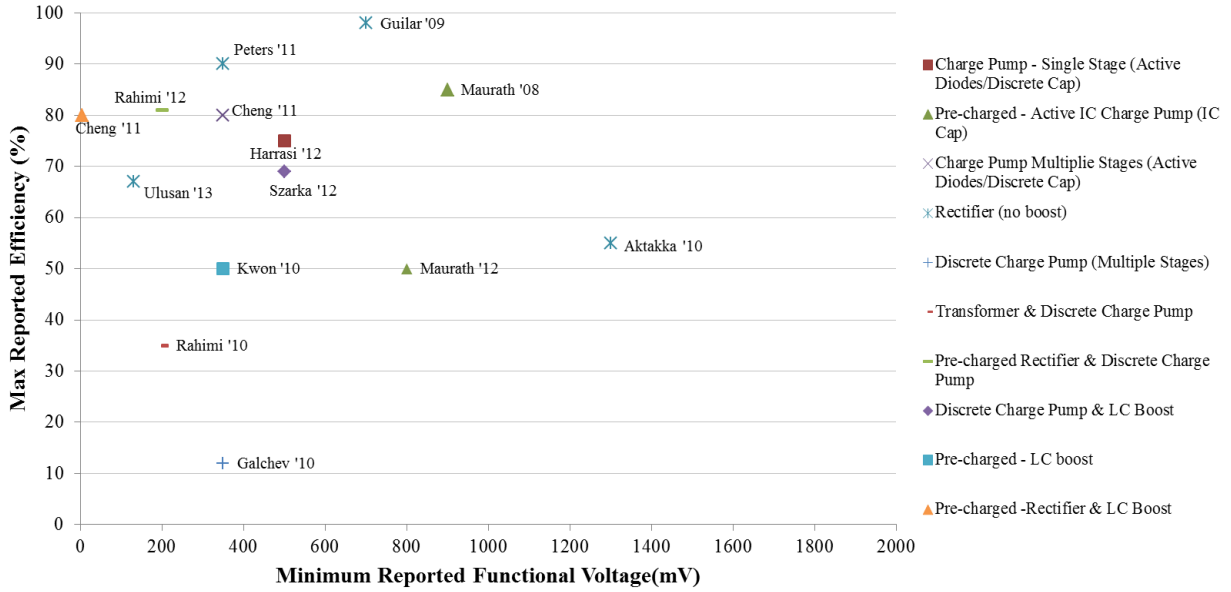

Figure 10. Shows the numerous circuits used to interface with vibration harvesters that can boost and rectify.

conference papers) minimum functional input voltages vs. their maximum power conversion efficiency are summarized in Figure 9. Figures 10 and 12-14 show similar graphs with Journal or Conference papers either removed or further clarified after explanation. The goal of this literature review process as presented in Figures 9-10 and 12-14 is to determine where the state of the art can be advanced in vibration energy harvesting circuits.

To simplify Figure 9, the functioning of circuits that only buck are identified and described, so that the next chart (Figure 10) will only focus on those circuits that are more relevant to the author's research. This focus on boosting and rectifying circuits will demonstrate where it is possible to advance the state-of-the-art and meet the system requirements (i.e. a

boosting system is needed capable of sub-threshold functioning). High quality LC bucking circuits have been designed, which can start-up with passive diodes in their system. They exhibit high efficiencies and overcome specific challenges pertinent to LC bucking circuits [24, 25], but a circuit that boosts is needed for this application. LC converters circuits are ideal for bucking through start-up. To maintain proper bucking, the duty cycle of switching in the LC bucking circuit must be controlled. A high enough input voltage through a rectifier can easily be used to start-up through a diode rectifier and achieve a high enough voltage far out of sub-threshold so that a high frequency signal with a correct duty cycle can be achieved. Start-up is generally not a challenge in bucking circuits, and therefore not a focus of this research. Rectifier circuits, charge pump circuits, and even LC boost circuits that start-up are relevant to this research.

Figure 10 displays these remaining circuits excluding two bucking IC-based configurations (Hehn ’11 and Ramadass ’09). However, many published boosting circuits and rectification circuits are unable to start-up. The ability to start-up is a major requirement of this system. To further focus on where advancement in the state-of-the-art can be made, boosting and rectifying circuits that are unable to start-up are identified and discussed. Figure 12 only displays those circuits able to start-up and boost or rectify (as compared to those circuit that can and cannot start-up as presented in Figure 10).

Purely inductor based circuits can be used, but they require a pre-charged battery [26, 27] (Kwon ‘10) not available on the bridge after long periods without PFIG actuation. Charge pumps completely fabricated in CMOS technology (including capacitors in ~pf range) have been built. These use higher frequency clocks to control boosting operation; however, they also require a pre-charged battery [28, 29] (Maurath ’08 and ’12). An active rectifier using a passive charge pump supply for start-up has been implemented (also described in Section 1.4.1) [19] (Rahimi

‘12), but it requires two separate harvester inputs for start-up. Remaining works are included in Figure 12 to further focus on works that can boost, rectify and start-up.

Transformers can also be used for boosting and they allow start-up; that is, they can boost a signal to overcome diode drops of a rectifier. As mentioned in the Introduction, energy harvester work based on transformers has been published [8-10]; however, these transformers match to a harvester’s output impedance that is far less than the PFIG’s. For example, the PFIG output impedance is 300 Ω to 1.5 kΩ, but current literature shows transformers matching to impedances in the 3 Ω to 4 Ω range [8-10]. Figure 11 shows an example of how a transformer is used in boosting circuit capable of harvesting [10]. The output of a 1:15 step-up transformer is both sent through a charge pump and harvested through an active rectifier (powered by the high voltage charge pump output). It gives an efficiency of 35%. Additionally, a conference paper [9] reports an IC rectifier circuit that follows a transformer for an up-converted signal. It reports 65% maximum power conversion efficiency. This work is not included in the list of energy harvester literature (Figures 9-10 & 12-14), because it does not mention the input signal voltage (without the transformer), and it is difficult to understand how efficiency and steady results were reached with the information in the conference paper, and there was no journal paper covering similar work. Investigation into circuits using transformers matched to higher impedances, like the output of the PFIG (300 Ω), would be of value and are not addressed in literature.

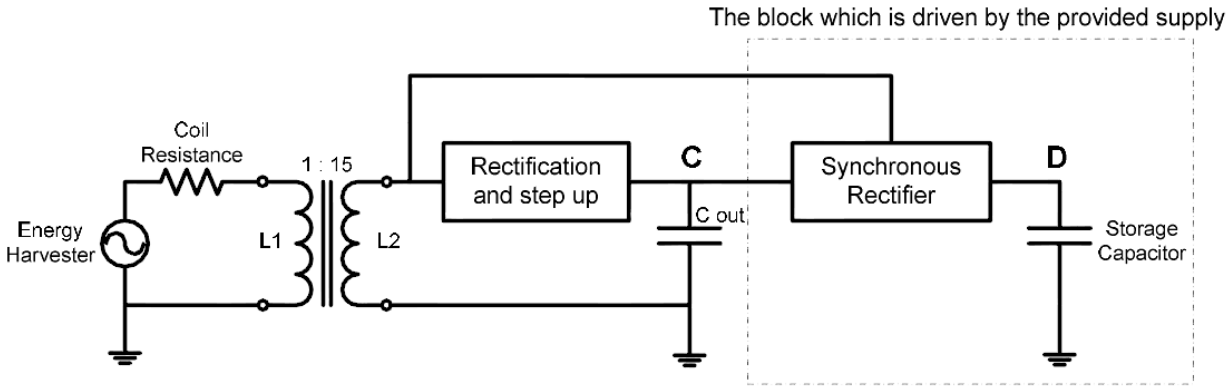

Figure 11. Shows a transformer, charger pump (rectification and step up) and rectifier used in a harvesting circuit [10].

While transformers present one solution to interface with vibration energy harvesters worthy of further investigation, circuits that are required to store, boost, and/or rectify the harvested energy from a vibration energy harvester all face similar challenges (cold-start and enabling high power conversion efficiency). The main issue is how to overcome the passive diode drops required in any type of harvesting system. These diode drops limit the minimum voltage that will enable start-up and they decrease efficiency for all boosting/rectifying circuits (LC boost, rectifier, or charge pump). Figure 12 shows the remaining works that either boost or rectify and can start-up without a transformer to focus on how the diode drops of system are overcome with various non-transformer based circuit techniques.

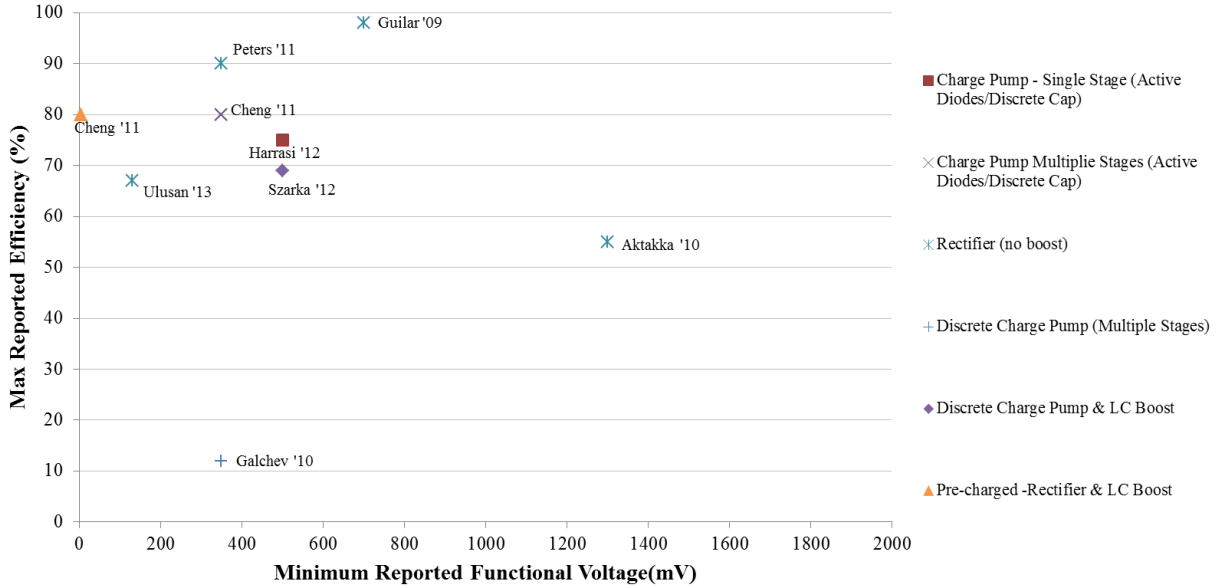

Figure 12. Shows the numerous circuits used to interface with vibration harvesters that can boost, rectify and cold-start.

Occasionally, there are significant differences in the reported start-up and the minimum reported functioning once started for a specific circuit. In the case of a discrete active diode charge pump (Cheng ’11) [12], the minimum reported start-up voltage is 500 mV while the minimum reported functioning is 350 mV. The difference between initial start-up and regular function is the fact that passive diodes are used for start-up, so the diode drop cannot be ignored lowering the maximum boosting capability of the system, while active functioning will enable much higher boosting functioning because the diode drop is limited. In an extreme example (also described in section 1.4.1), minimum functioning is listed as 5 mV, but minimum start-up is 1.25 V[23] (also Cheng ‘11). At 5 mV the system only works with an external battery. Additionally, work has been described that is only capable of charging integrated capacitors in the ~pf (Ulusan ’13) (also described in section 1.4.1) [18]. While this work gives interesting results because it shows minimum sub-threshold functioning, reported efficiency charging a capacitor with useful storage (10 µF) is not available. To see a more useful diagram that reports either minimum start-up or a minimum voltage where efficiency is reported vs. efficiency these

three works are either moved to their minimum start-up value or lowest value where efficiency is reported. This new diagram is shown in Figure 13.

Figure 13 still includes rectifiers. Innovations in rectifier circuits continue to be made. There are many examples, and some of them investigate sub-threshold functioning as previously described in Section 1.4.1. A high frequency rectifier can operate with multiple inputs at different resonance frequencies [30]. A "negative voltage converter" has been built from passive

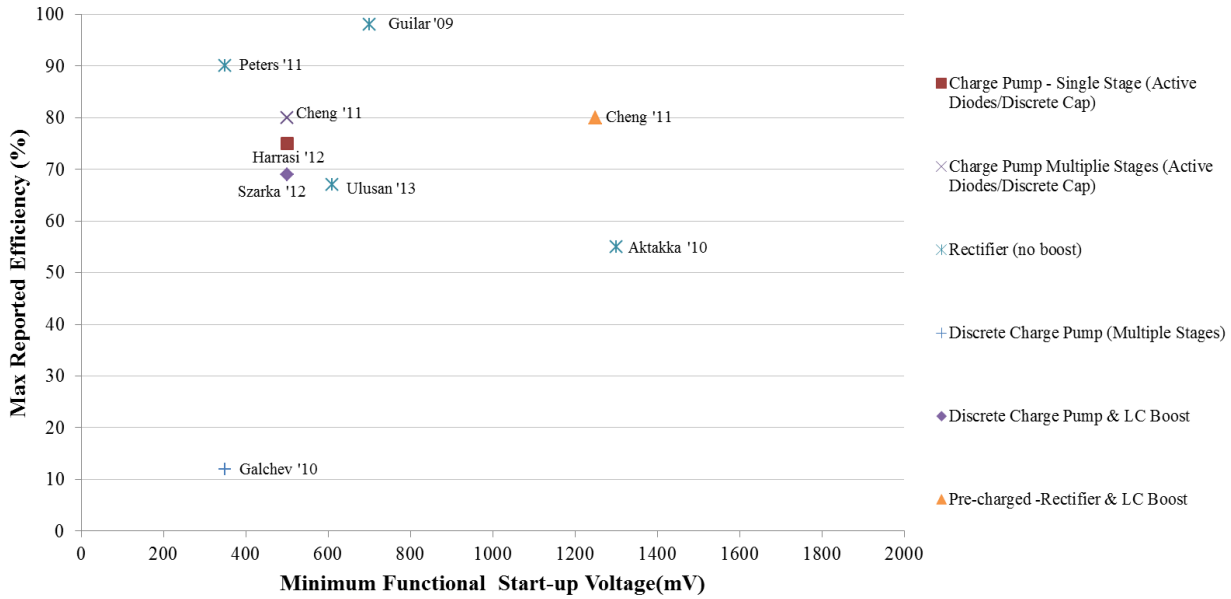

Figure 13. Shows the numerous circuits used to interface with vibration harvesters that can boost, rectify and cold-start. Three works Cheng '11 (LC boost), Cheng '11 (charge pump), and Ulusan '13 positions are adjusted.

diodes, which converts the negative portion of an input AC signal positive so only a half-wave rectifier is necessary [20, 22, 31]. One of these works is described in Section 1.4.1 and operates in sub-threshold [20]. Also mentioned in Section 1.4.1, there has been one conference paper showing ultra-low voltage rectifiers that use both a connected passive diode start-up circuit and active diode rectifier circuit [18], using a nearly identical rectifier circuit architecture previously used [23]. This conference paper claimed operation at ~150 mV; however, no efficiency results are given at low input voltages, nor are the values of the capacitor being charged given. These

circuits do not address the challenges of boosting operation including start-up, the use of appropriate storage element (capacitors or inductors), or the transition into regular boosting functioning from start-up functioning.

A figure without rectifiers is shown in Figure 14. It shows the general trade-offs and concerns when designing a boosting system that must cold start. A passive charge pump alone will be limited by the diode drops and minimum start-up may only be as low as 300 mV when using passive Schottky diodes (Galchev ’10). The problem with passive Schottky diodes at low input voltages is that the efficiency of the system is very poor as most the power is lost in the diode drops. If a charge pump is not used and an LC boost rectifier is used, virtually no boosting charge pump start-up is possible (Cheng ’11). Solutions that can both start-up at a reasonable input voltage and still produce a high efficiency use a passive charge pump combined with either

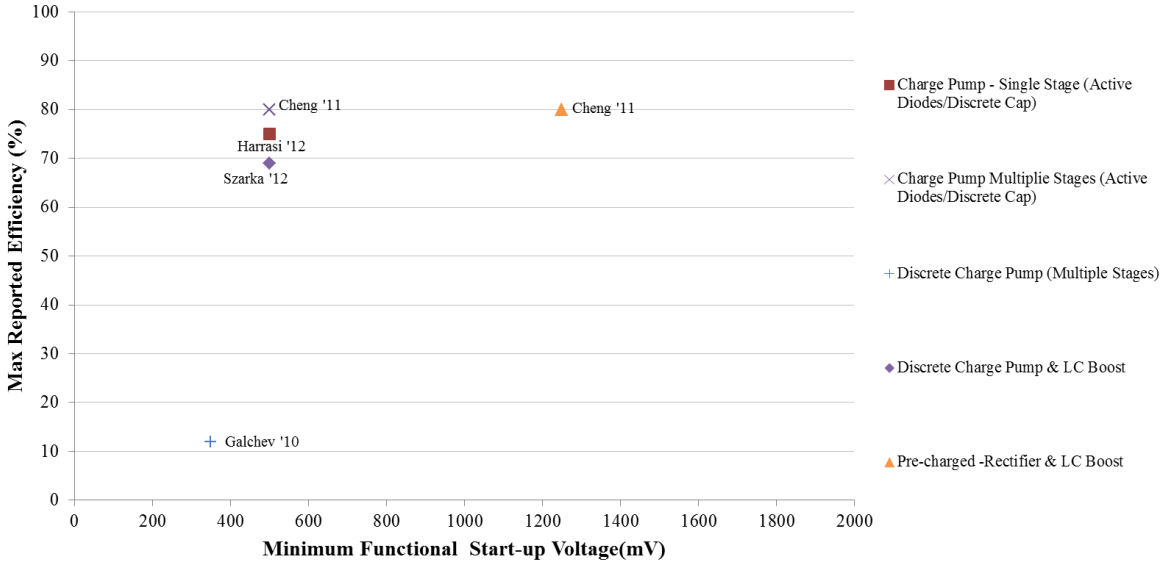

Figure 14. Shows the few circuits used to interface with vibration harvesters that can boost and cold-start while boosting.

an active charge pump (Cheng ’11 and Harrasi ’12) or active LC boost circuit Szarka ‘12. Basically, in the three cases with high efficiency and a reasonable minimum start-up a passive

charge pump for start-up is used followed by an active system for regular functioning. These passive charge pumps are still limited by the turn-on voltage of the diode chosen diodes. A more in-depth look at these remaining works will further focus a major contribution of this thesis.

The author's previously cited work, made up of discrete passive Schottky diodes, produced an efficiency of 12% at an input voltage of 375 mV [6]. A multiple stage and a single stage discrete active diode charge pump have been built, and their operation is similar [12, 13]. Figure 15 shows the multiple stage active diode charge pump [12]. Each device is discrete, and the bulk connections from the individual transistors are used to create passive diodes that are used in start-up [12]. These bulk connections would not be available in some CMOS

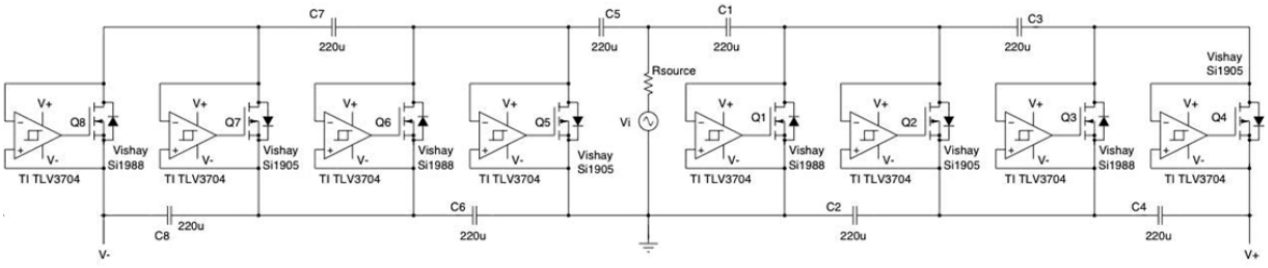

Figure 3. Complete schematic of the voltage multiplier based on active diodes.

Figure 15. Shows a multiple stage discrete active diode charge pump where the bulk connections from the individual transistors are used to create passive diodes seen besides the transistors in [12].

technologies including 180 nm that is used to design the work in this thesis. The discrete comparators only begin operation at near 2.1 V emphasizing this circuit's need for the passive diodes [12]. Both discrete charge pumps use approximately ~6 µW of power [12, 13]. This also makes them unsuitable for harvesting the outputs of a bridge based energy harvester. On the positive side, this work can exhibit high efficiencies (> 80%) with a high power input signal from a vibration harvester.

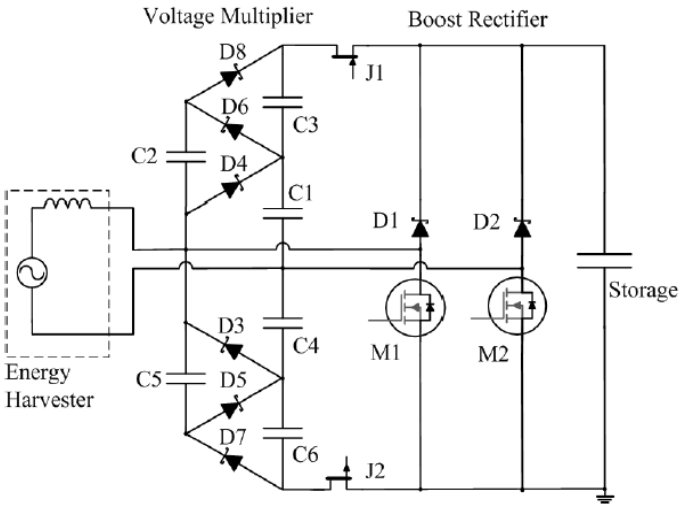

Figure 16. Shows a start-up circuit for circuit interfaced with a vibration energy harvester. A passive diode based full-wave charge pump is used until a LC boosting circuit takes over. The inductance of the harvester coil is used as the "L" in the LC circuit [32].

Figure 16 also shows a work that uses both a discrete passive charge pump and an active LC boosting circuit [32]. This is a significant work for higher power and higher voltage applications, because it uses a maximum power tracking to control the LC boosting to create optimal power conversion efficiency. Its drawbacks are its higher power consumption (~21 μW) and the minimum voltage for operation of (500 mV); however, its start-up architecture has considerable value even though it still relies on passive diodes [32]. Its maximum efficiency is relatively high at 68% for very high power signals in the ~mW range. This LC based harvester circuit is shown in Figure 16. In this figure, a full-wave passive diode circuit starts up the circuit until a LC boosting circuit can take over. The "L" in the LC circuit comes from the inductance of the harvester. This is possible if the resistance of the coil is much smaller than the inductance (this is not the case with the PFIG with output impedances between 300 Ω and 1.5 kΩ).

A main focus of this thesis is on alternative methods to overcome the diode drops that limit function in a charge pump by using sub-threshold active diode functioning for start-up while maintaining reasonably high efficiency for regular functioning using the same active diodes. The use of sub-threshold active diodes boosting in a charge pump has the potential to improve minimum functional start-up on Figure 14 far lower while maintaining comparable or greater efficiency. These two major works [12, 32] demonstrate the present limits of the state-of-the-art and motivate multiple solutions that will be investigated, including transformers matched to a much higher vibration harvester output impedance (lower power vibrational harvester), the use of sub-threshold functioning immediately in the start-up of a charge pump to enable record low voltage turn-on for a boosting circuit, and the use of a unique full-wave active diode architectures to enable high power efficiency operation with low power and low voltage vibrational harvester outputs.

1.4.3 Other Types of Start-up in Thermal Harvesting

There have been numerous studies and publications into thermal harvesting start-up techniques and challenges with low voltage thermal harvesters. Very similar techniques and challenges exist in the start-up of thermal harvesting circuits and vibration harvesting circuits even though thermal harvesters supply a DC supply and vibration harvesters supply an AC input signal. For example, similar to vibration harvester circuits, bulky transformers can be used to allow start-up at ultra-low DC input voltages; charge pumps are pushed at the edge of sub-threshold functioning; and additional start-up architectures are built to manage start-up functioning. These works are important to review so that there can be understanding of the relevant parts of the thermal harvesting circuit literature relating to vibration harvesting circuits.

As before, transformers can and have been used for over a decade to enable low voltage start-up from thermal harvester's DC voltage using a technique shown in Figure 17 [33]. This technique can enable start-up as low as a DC voltage of 20 mV [34]. The 1:45:65 transformer in the "starter circuit" on the bottom left hand corner enables start-up. In this circuit the JFET T1 is chosen to always be on creating negative feedback in the 1:45 portion of the transformer starting an oscillation that is then amplified in the 45:65 portion of the transformer and stored in capacitor C2 after being rectified by the diode D1. Just as transformers are used in vibration harvester circuits to enable start-up, they are also a main tool used to enable start-up in thermal harvester circuits. Transformers are bulky and expensive, motivating other start-up solutions that are used in thermal harvesting and also relevant to vibration harvesting circuits.

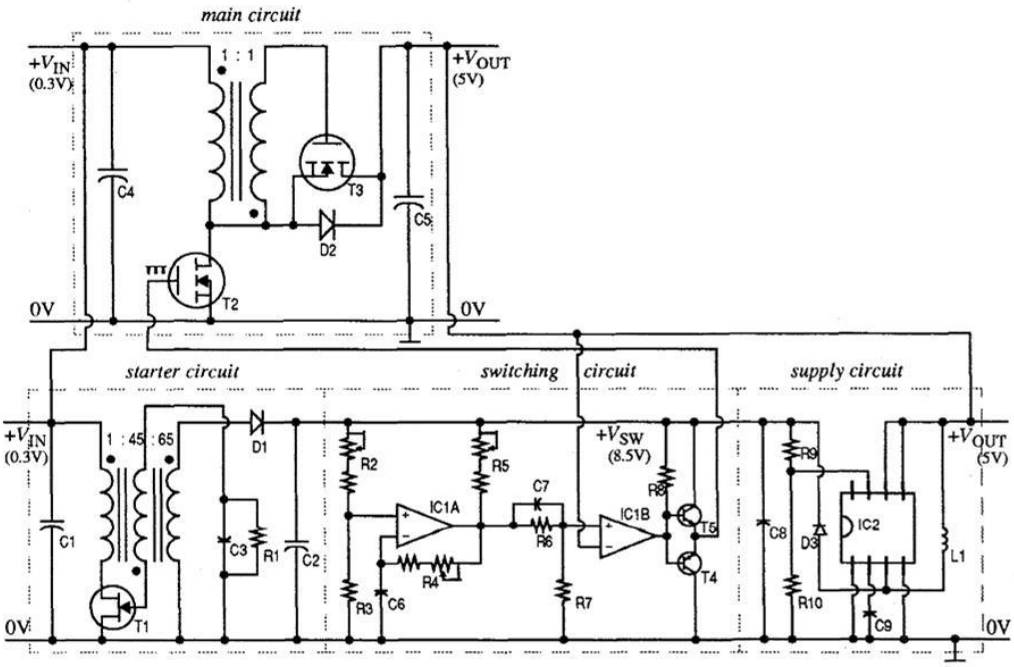

Fig.4. Circuit diagram of the complete circuit. In parentheses the voltages during regular operation are given. The values of the devices are given as follows: Starter circuit: R1=1MΩ, C1=1mF, C2=470μF, C3=1nF, D1=1N4148, T1=J105; main circuit: C4=2.2mF, C5=1mF, D2=1N4001, T2=T3=SMP 60N06-18; switching circuit: R2=350kΩ, R3=1MΩ, R4=1.8kΩ, R5=32kΩ, R6=270kΩ, R7=1MΩ, R8=2.2kΩ, C6=10nF, C7=1nF, T4=BC313, T5=BC182, IC1=TLC372CP; supply circuit: R9=1MΩ, R10=182kΩ, C8=100μF, C9=47pF, L1=1.7mH, D3=1N4148, IC2=MAX630.

Figure 17. The starter circuit in the left bottom corner shows the main way transformers can be used in thermal harvesting start-up [33].

In an effort to find alternative solutions to thermal energy harvester start-up, research has been done using an externally actuated switch for start-up in a thermal harvesting circuit, and start-up as low as 35 mV has been demonstrated. The switch is part of an LC circuit seen in Figure 18 [34]. . This is also worth mentioning, because it shows an alternative use of a motion

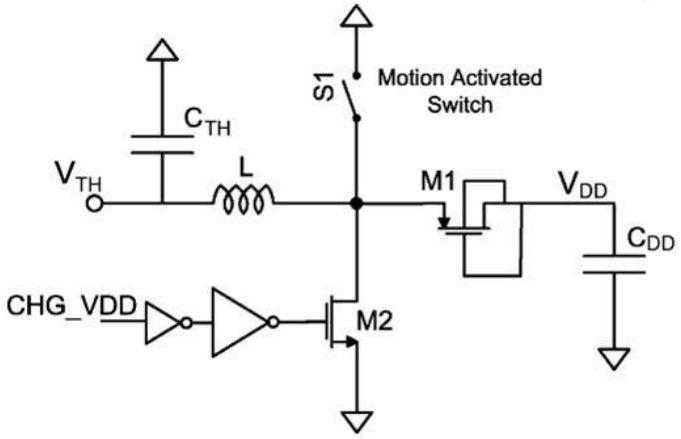

Figure 18. Shows a start-up circuit using a motion activated switch in LC configuration [34].

based switching source for use in harvesting start-up. Such a switch could be considered as part of the PFIG or multi-mode system functioning if necessary in a future design. The switch generates a signal that is boosted and is stored in the capacitor C_{DD} (Figure 19) through the diode M1 (Figure 18). Figure 19 further shows the start-up functioning and start-up circuitry. This

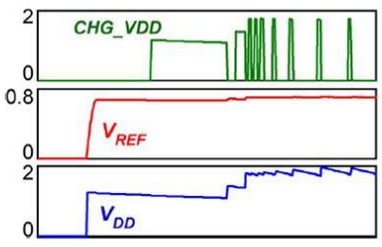

Fig. 4. Simulated waveforms showing the functioning of the startup block.

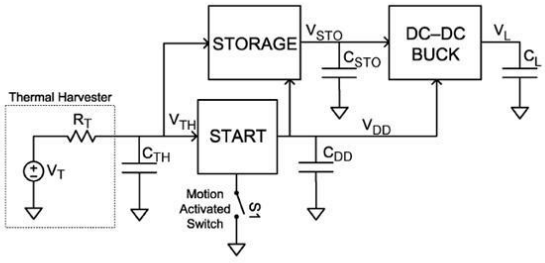

Fig. 5. Architecture of the thermoelectric energy harvesting system.

Figure 19. Shows the start-up functioning (left) and start-up architecture of system (right) where start-up is enabled with a motion activated switch [34].

functioning immediately charges the V_{DD} in figure 19. This then allows a storage block, V_{REF}, and CHG_VDD signal of the DC-DC bucking circuit to begin to function. Once the start-up is enabled, this system switches to entirely different part of the circuit for regular functioning. This scheme shows the challenge of start-up and the additional design that is needed to appropriately enable start-up in LC boost circuits that do not use a charge pump in order to maintain high efficiency operation.

Start-up can also be enabled by a charge pump system. As mentioned before with LC boost circuits in vibration harvester circuits, the LC boost circuit must enable a clocking signal in the range of ~10 MHz with accurate duty cycle control. This well controlled high frequency signal is not possible in deep sub-threshold functioning (also discussed in an example in Section 1.4.1). As with vibration harvester charge pump circuits, thermal harvesting charge pump circuits can be used and can actually allow for limited functioning in deep sub-threshold. An example of this is shown in Figure 20. In this case a 0.18 V DC signal and a 0.18 V clock are supplied to a

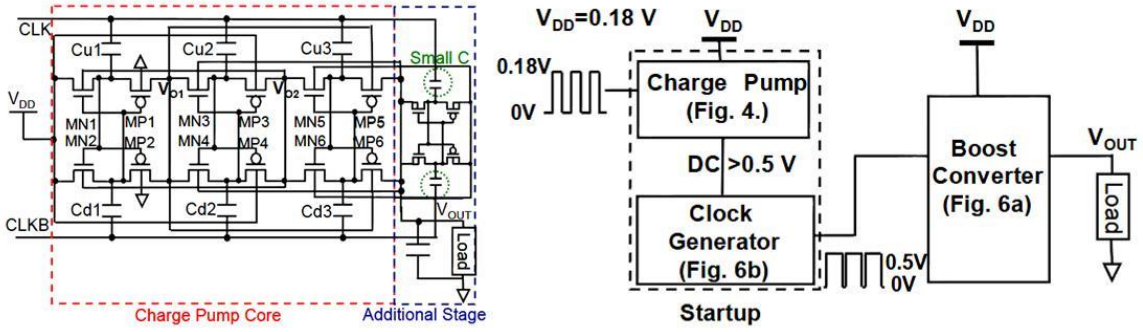

Figure 20. Show thermal harvesting start-up using an integrated charge pump followed by and LC Boost converter. A 0.18 V DC voltage and clock are needed for start-up [35].

fully integrated charge pump (with integrated capacitors in the ~pf range). The output of the charge pump is then sent to a separate higher voltage clock generator to enable a high frequency signal with a controlled duty cycle to enable a boost converter which also boosts the signal from

the output of the first charge pump (> 0.5 V). An integrated charge pump is used that makes use of every available technique to enable adequate functioning in sub-threshold operation. A 65 nm CMOS technology is used with both a deep PWELL and NWELL allowing for the bulk connections to be connected where they optimize the charge pump functioning. Instead of connecting an NMOS to gnd and PMOS to supply, the V_{th} of the devices can be reduced by connecting the bulks to the nearest stage. Additionally, instead of just single NMOS or PMOS diode, CMOS active diodes are used comprising of both and NMOS and PMOS devices to increase boosting efficiency. CMOS 65 nm technology has V_{th} less than 400 mV, and this is less than the Vth in 180 nm which can be over 450 mV. It is difficult to directly compare start-up performance between technologies and between a clocked charge pump boosting a DC signal and an AC signal that alone is boosted by a charge pump. The low input voltage of 0.18 V requires sub-threshold functioning in the charge pump; however, the charge pump is only charging ~pf capacitors and then the system converts the charge pump output to high voltage DC output voltage. No efficiency results are reported here, and the output current is near 6 mA. In terms of input power this means that this circuit's input is potentially ~1000 greater in power compared to what is regularly produced by the PFIG. This further casts doubt on whether a LC boost circuit or charge pump with capacitors in the ~pf range are suitable for very low power harvesting solutions.

Vibration harvesting circuits and thermal harvesting show similar challenges, solutions and opportunities to advance the state-of-the-art. Similar to vibration harvesting, transformers can be used for ultra-low voltage start-up. Switches can be used to enable start-up in an LC configuration; however, this requires both a DC signal and must be aggressively actuated using human body motion. Sub-threshold functioning can be used in a charge pump; however, both an

external DC signal and DC clock are necessary, and the charge pump system described [35] can only operate at very high input power (in the ~mW range). It is difficult to think of an instance where both a low voltage and very higher power thermal harvester are suitable for any application and somehow supply both a DC voltage and well defined clocks in the ~kHz range to trigger a charge pump. These continued challenges in start-up of both thermal harvesting and vibration harvesting motivate solutions that can work with both low power and low voltage harvesters. Solutions using charge pumps and sub-threshold design described in the contributions of this thesis may be easily used in thermal harvesting.

1.5 Efficiency in Energy Harvesting Circuits

The Figure of Merit used to measure the power conversion of any type of harvester circuit is efficiency. This is the same figure of merit for a rectifier, boosting or bucking circuit. There is significant controversy in how efficiency is reported, and likely some journals and conference papers have reported it incorrectly, leading this author to question the results in some publications. Below is how efficiency, η, should **NOT** be reported.

$$\eta \neq \frac{\text{Output Power}}{\text{Input Power}} \tag{4}$$

The inherent problem with this definition of efficiency is that input impedance of interface circuit can change depending on the voltage level of the storage capacitor. If this definition is used, one could have the extreme situation where there is higher efficiency through an interface circuit, but lower power produced at the output of the circuit. A more widely, and in the author's opinion, more correct definition of efficiency is using the "Maximum Input power" instead of "Input Power" as seen below.

$$\eta = \frac{\text{Output Power}}{\text{Maximum Input Power}} \tag{5}$$

In the case of an electromagnetic vibration harvester, a load attached to the energy harvester, which is the same as the energy harvester's matched load, will give the optimal input power. Therefore, efficiency, η, is used to measure the performance of the circuit. Circuit efficiency is calculated in this case by comparing the average harvestable power that can be delivered to a matched resistive load (ideal case) to the power delivered by the power management circuit (1).

$$\eta = \frac{\frac{1}{t_2-t_1}\int_{t_1}^{t_2} P_{out-matched\ load}}{\frac{1}{t_2-t_1}\int_{t_1}^{t_2} P_{out-CW}} \tag{6}$$

For a sine-wave, the input power from a harvester can be given below. V_{peak} of a sine-wave is defined by the voltage between the peak of the sine-wave and the center of the sine-wave. For a PFIG input the same definition is used on the largest peak of the decaying sine-wave. In this thesis "rms" voltages are <u>not</u> used.

$$Input\ Power = \frac{V_{peak}^2}{8\times \text{Input Impedance}} \tag{7}$$

Average output power can be measured in steady-state by loading the output with a resistor to obtain current and voltage. In this case output power is simply given below.

$$Output\ Power = \frac{V^2}{\text{R}} \tag{8}$$

Alternately, average start-up output power can be obtained by measuring the energy in the storage capacitor divided by the storage period. This is given below and has been very useful in the long-term tests.

$$Output\ Power = \frac{\frac{1}{2}CV^2}{Period} \tag{9}$$

These definitions will be used to calculate efficiency in the following chapters.

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Chapter II

A Transformer-Based Harvesting Solution and Long Term On-Site Bridge Test

2.1 Bridge Testing Motivation

Performing tests on an actual suspension bridge with the PFIG is critical to this research to give an accurate understanding of average power available on the bridge, the range of instantaneous power, and the frequency of lulls (periods of non-actuation). According to the US Department of Transportation, more than 10% of the nation's bridges are structurally deficient [1]. Wireless sensor technology is a superior solution for monitoring this deteriorating infrastructure as it eliminates the need for expensive wiring and permits easy relocation of sensors nodes. As these Structural Health Monitoring sensors (SHM) must operate continuously for many years without human intervention, battery replacement is a significant concern since the sensors are typically located in hard-to-reach and dangerous locations. Various bridge locations can give different power results and the behavior of the PFIG. Therefore the charge pump's reaction can be different and will affect the ability to recharge a capacitor or battery between locations. The New Carquinez Bridge (or NC Bridge) near Vallejo, California (also known as the Alfred Zampa Memorial Bridge) (Figure 21), where a present long-term study is ongoing, is an example of a large suspension bridge over water with heavy traffic containing many such inaccessible locations. To allow for the study of these locations, an improved harvester and electronics was necessary. The original electronics used with the PFIG-B1

consisting of two cascaded Schottky diode Cockcroft-Walton charge pumps and PFIG were not suitable for bridge operation on the NC bridge. A transformer-based solution allows a complete harvesting system (power management electronics and harvester) to be installed on the New Carquinez suspension bridge in California for the first time. The power management circuit is added to rectify and boost the low AC output of the harvester and convert it into a usable DC voltage that, at minimum, is 0.7 V.

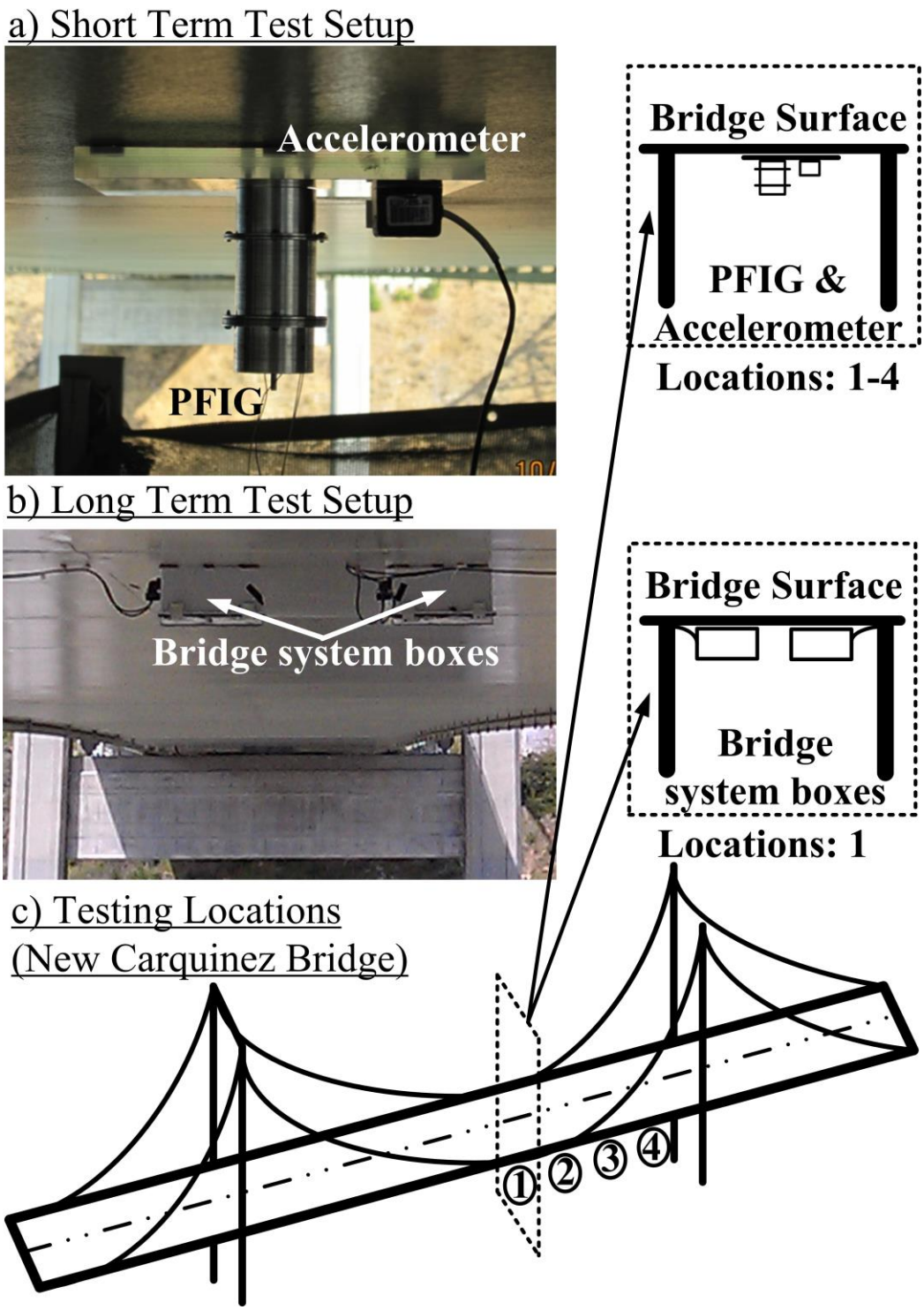

Figure 21. a) Short-term test setup with the PFIG and accelerometer. The PFIG is attached to a plastic plate attached magnetically to the bottom of the bridge. b) Long-term test setup is shown with system boxes attached magnetically to the bottom of the bridge. c) Approximate positions of installation locations the New Carquinez Bridge. Locations 1-4 were used for short term tests, while the location 1 was used for long term tests [2].

Improvement in the PFIG was necessary before a transformer-based system could be built. For a transformer matched to 1.5 kΩ output impedance at 100 – 200 Hz, there is only a very limited chance of finding an efficient reasonably sized transformer that could be matched to this output impedance and low frequency; however, if a lower output impedance like 300 Ω is implemented in the PFIG, there are transformer solutions readily available commercially. The PFIG's reduction in output impedance to 300 Ω also resulted improved performance and robustness. For example, during short-term on-bridge testing, the system is able to charge a 10 μF capacitor to 2 V DC, and the average harvester output power ranges from 1.6 to 5.0 μW, depending on the location on the bridge, a 10× improvement over previous results. The technical viability and in situ characterization of the PFIG-B1 (the first bridge based PFIG) was completed during a temporary installation on the New Carquinez Bridge (Figure 21a). The measured average output power was 0.5-0.75 μW over several minutes, when bridge accelerations ranged from 0.1- 0.5 $m \cdot s^{-2}$ at frequencies of 2-30 Hz [3].

Because of the improvements in both the PFIG and use of the transformer in the system electronics, a long-term test of the harvesting system has been initiated, during which the performance of the system is monitored remotely using a wireless sensor network. The system improvements have enabled continuous operation in the harsh bridge environment for 13 months starting April 30, 2012 (ongoing) and constitute a major milestone in the development of miniaturized motion harvesters. This long-term test and system configuration allows for advancement in the state-of-the-art in the understanding of the range of non-periodic PFIG responses on a bridge as well as the response of a charge pump circuit to the PFIG's non-periodic actuation.

In addition to the electromechanical behavior of the harvester, power management and rectification is essential at the system design level. Essential elements in vibration harvesting typically involve AC to DC conversion, voltage boosting, and regulation. In the case of the PFIG-B1 harvester a number of challenges existed that made these power management tasks complicated. First the electrical outputs of the PFIG resemble decaying sinusoidal waveforms due to the nature of the up-conversion process. Second, the PFIG-B1 harvester has a high output impedance (1.5 kΩ). Lastly, the harvester produced a non-optimized low output voltage [3]. A preliminary attempt at power management was made by using two cascaded six-stage passive Schottky diode charge pumps to simultaneously rectify and boost the PFIG output signal [3]. However, this circuit exhibited a very low efficiency (13% with a decaying sine wave input of peak 375 mV), and ceased to work below 200 mV. The main problem was the low output voltage relative to the turn-on voltage of the Schottky diodes [3].

A simple method to overcome very low voltage inputs, one that is particularly suited toward electromagnetic harvesters, is to utilize transformers. They offer a passive way to overcome diode turn-on voltages, and high efficiencies (65%) have been demonstrated in transformer based systems [4-6]. A necessity for these high efficiencies is that the output impedance of the harvester must be small (3 - 4 Ω), otherwise the size of the matched transformer would be impractical. Provided that the output impedance of the harvester is reduced, combining a passive charge pump with an input transformer can provide a simple and passive way of rectifying and boosting the output voltage of the PFIG.

This chapter discusses the improved performance of the harvesting system electronics with the improved harvester PFIG-B2, including the adjustment of its technical characteristics with system level considerations in mind. With the new PFIG (PFIG-B2), a power management

circuit consisting of input transformers and two cascaded passive charge pumps are used to rectify and boost the output voltage of the harvester and store energy on a capacitor. These enhancements allowed a complete system to be installed on a suspension bridge where it has operated for 13 months (on going), and its performance has been remotely monitored and recorded since April 30, 2012 [2]. This complete system has given valuable data showing the performance of the PFIG with a charge pump and range of the PFIG power produced on the a major suspension bridge for over 1 year. Additionally, it showed the power that could be generated using a transformer based system and the PFIG-B2 with a 300 Ω output impedance.

2.2 New PFIG Characteristics

The 2nd PFIG built for bridge harvesting had reduced output impedance from 1.5 kΩ to 300 Ω, and this enabled a matched transformer solution for the PFIG. Frequency vs. power plots for various versions of the PFIG are shown in Figure 22. They are actuated at the minimum acceleration level needed for operation, which was designed to be different in each case in order to explore the limits of the harvester. The different acceleration levels in Figure 22 should be considered when comparing the three plots. This plot shows both the PFIG-B1 and two versions of the PFIG-B2. Both versions of the PFIG-B2 produce far more power than the PFIG-B1. The versions of the PFIG-B2 are with and without a double magnet structure to increase the power generated from the PFIG [2]. The PFIG-B2 on the NC bridge is capable of between 1.6 µW and 5 µW of average power generated clear improvement from the PFIG-B1 which can only produce between 0.47 µW and 0.75 µW of power.

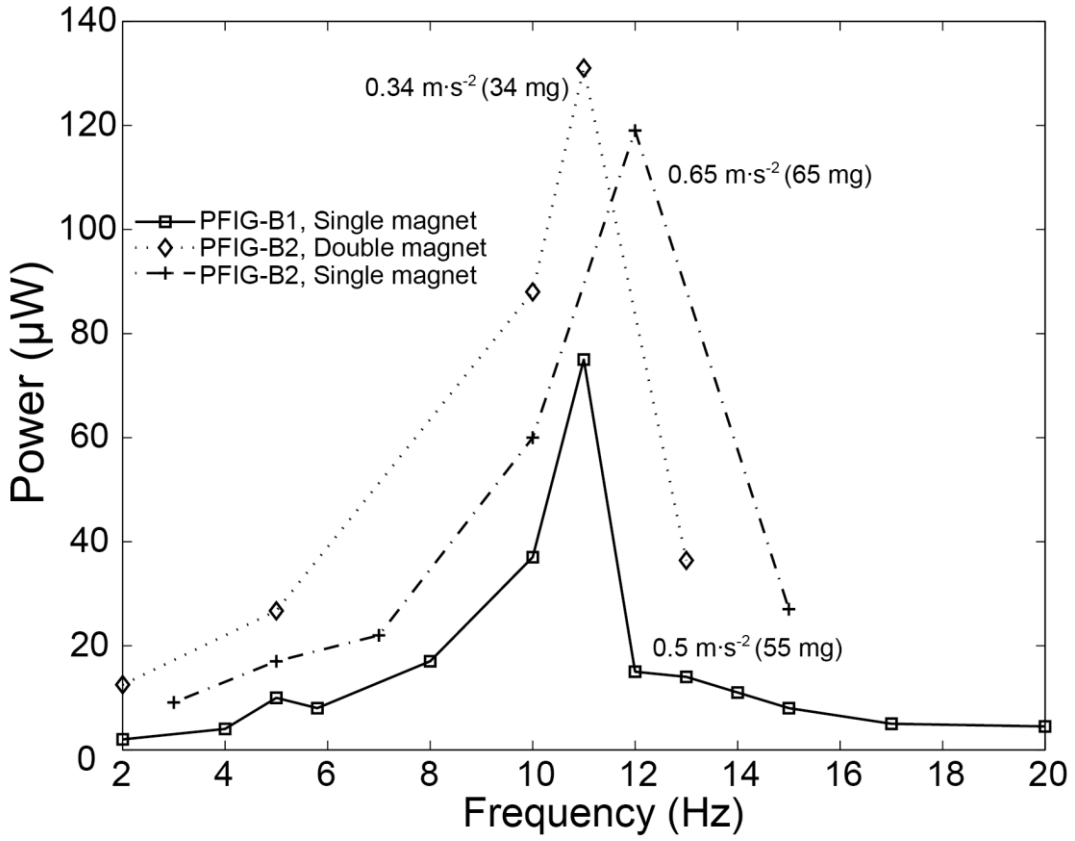

Figure 22. The graph of frequency vs. power is shown for multiple versions of the PFIG. The enhanced PFIG-B2 with and without a double magnet structure show significantly improved power output as compared with the previous PFIG-B1.

These plots in Figure 22 also show the challenges of harvesting from the PFIG including the range of power seen with different accelerations. For example, there will be periods of very little power actuated, even though there are vibrations from vehicles passing overhead present on a bridge. This is because the range of frequencies does not efficiently actuate the PFIG near its resonance (near 10 Hz) which is set by the Tungsten Carbide inertial mass and inertial mass springs. For example, at 2 Hz far less power will be produced by the PFIG compared to at 10 Hz. The reduction of the output impedance of the PFIG was actually able to improve the power generated by the PFIG for multiple versions of the PFIG-B2 [2] meaning the PFIG-B2 was more suitable for the power electronics both in the reduction in output impedance and the increased power.

2.3 Passive power management electronics for the PFIG-B2

The PFIG-B1 used a cascade of two six-stage discrete charge pumps to boost and rectify the harvester output signal [3]. Schottky diodes (BAT54WS) were used in the charge pump. However, the diode drop losses significantly reduced both the efficiency and boosting ability of the previous circuit making it unsuitable for bridge operation. Therefore, any new interface has several requirements. First, the circuit must easily start-up based on the smallest expected harvester output. Next, the circuit should optimize power transfer to a load or storage capacitor at these very low harvester outputs. Finally, it should enable long-term installation of the bridge harvesting system (BHS), so that the limits of the system (PFIG and circuit) can be studied and characterized. To accomplish these goals and enable the rate at which the BHS storage capacitor voltage rises to serve as the basis for estimating power during the bridge installation, the circuit needed to start-up, and its output voltage needed to rapidly rise to a usable voltage from even the lowest PFIG output voltage signal (~60 mV). State-of-the-art ICs can regularly operate at 1.2–1.8 V, and there are even sub-threshold microcontrollers that can operate below 0.7 V. Because of this, the PFIG should be able to efficiently charge a storage capacitor to at least 0.7 V.

The addition of the transformers between the harvester and the charge pump immediately mitigates the effect of the diode turn-on voltage losses and even reduces the number of required multiplier stages while still significantly improving the circuit's boosting ability. If a transformer is used in a boosting circuit interface, there will always be a trade-off between what harvester output impedance is best for matching with the transformer and what output impedance gives the best performance from the harvester. A transformer with a high turns ratio (i.e. 1:100 resulting in 1:10 boosting) will be less efficient than a transformer with a lower turns ratio. The additional turns add DC resistance that reduces power, and each additional turn will add more DC

resistance than the previous turn. Also, with higher turns-ratio, the transformer is larger, adding additional inductive coupling losses. Additionally, the higher a harvester's output impedance, the higher the transformer's input impedance must be to achieve maximum power transfer. However, the large transformer input impedance will also increase the size of the transformer and therefore its dc resistance and inductive losses.

Previously, for the circuit used with the PFIG-B1, without the addition of transformers and not taking into account the characteristic decay in the PFIG output waveform, the theoretically available maximum voltage of the cascaded charge pumps is $V_{out_{CCW}}$, where V_{CW} is the maximum output of a single Cockcroft-Walton Multiplier:

$$V_{out_{CCW}} = 2 \times V_{CW} = 4 \times n \times V_{Peak} \tag{10}$$

Here *n* is the number of stages per multiplier, and V_{Peak} is the unmatched input peak voltage. The factor of four comes from boosting the two serially cascaded Cockcroft-Walton multipliers. For the two six-stage cascaded multipliers the max boosting is:

$$V_{out_{CCW}} = 24 \times V_{Peak} \tag{11}$$

While this is significant boosting, the Schottky diode turn-on $V_{diode-drop}$ needs to be accounted for, resulting in the following:

$$V_{out_{CCW}} = 24 \times \left(V_{Peak} - V_{diode-drop}\right) \tag{12}$$

If the Schottky drop is near 180 mV, and the typical PFIG output maximum peak is 200 mV, most of the signal is wasted. This results in an output of 480 mV by using (4). Because the PFIG output decays, only the first few peaks will be useful and the rest of the output signal will be lost due to the diode drops. Ideally, the circuit would make use of as many of the decaying peaks as possible and be capable of operating from the low ~60 mV peaks.

The new circuit presented and used with the PFIG-B2 (characteristics described in

Table 1) makes use of a transformer with a 1:10 multiplication factor to boost the low and decaying PFIG outputs. When the transformers are matched to the FIG output impedance, to obtain maximum power transfer, the voltage is reduced by a factor of two in essence resulting in a 5× gain in voltage. This gives the ideal maximum voltage for a circuit containing a Cockcroft-Walton Multiplier preceded by a 1:10 matched transformer as $V_{out_{TCCW}}$:

$$V_{out_{TCCW}} = 2 \times V_{CW} = 4 \times n \times \left(5 \times V_{Peak} - V_{diode-drop}\right) \quad (13)$$

Assuming n = 3 stages, a 180 mV diode turn-on voltage, and V_{Peak} of 60 mV, the boosted DC output is 1.44 V, which will yield ~0.72 V when optimally loaded. Therefore, the target requirements can be met with only 3 stages. The inter-stage capacitors were chosen to be 10 μF

Table 1. Summary of (PFIG-B2 and circuit) performance and characteristics

Performance Summary PFIG-B2	
Minimum Acceleration	0.34 m/s^2
Internal Volume	43 cm^3
Total Volume	68 cm^3
Avg. Power (0.34 m/s^2, 2 Hz)	12.5 μW
Avg. Power on New Carquinez Bridge	1.6 μW – 5.02 μW
Altered Mechanical Parameters From previous PFIG [3]	
Coil Turns, N	1200
Coil Resistance	275 kΩ
Spring Constant, k_i (Both springs combined)	535 N/m
Circuit Characteristics	
Boosting Methods	CW Charge Pump & Transformer
Transformer	Picoelectronics T-22940
Transformer Volume	5.09 cm^3
Diode	BAT54WS Surface Mount Schottky Diode
Capacitors	10μF (Tantalum Surface Mount)
Maximum Circuit Efficiency	27%

(see Table 1) based on the need to quickly charge capacitance while maintaining a reasonable efficiency.

The schematic of the interface circuit is shown in Figure 23. The two transformers used in the system are Picoelectronics T-22490. Even at 200 - 300 Ω, the output impedance of each FIG still imposes stringent transformer characteristics. To maximize power transfer the transformer input impedance should match the impedance of the FIGs [7]. As discussed earlier, a transformer with a ratio of 1:10 was chosen. Higher ratios are possible; however, every additional turn added in a transformer increases its DC resistance. Producing a desired ratio and matched input impedance is a challenge. As part of the passive circuit design process, the efficiency of the matched T-22490 was measured to be ~63% with a 100 Hz signal and an input power of 6.4 μW. This ~63% alone is a significant drop in power efficiency. Figure 9 (see section 1.4) shows harvesting solutions whose entire circuit efficiency is better than ~63%. Picoelectronics transformers [8] are rated at 1 mW and have a frequency range of 20 Hz - 25 kHz; however, at low frequency there seems to be significant reduction in the inductive coupling. Laboratory measurements show that maximum efficiency occurs near 500 Hz, which is much

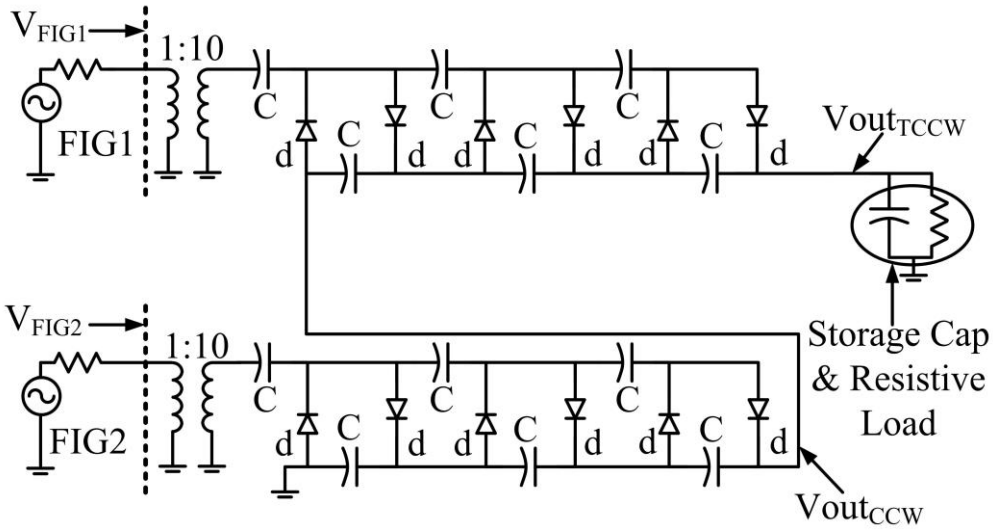

Figure 23. The circuit schematic shows two transformers that increase the harvester outputs and feed them into two cascaded 3-stage Cockcroft-Walton Multipliers. The storage capacitor and load are indicated along with other important nodes [2].

higher than the frequency output of the FIGs (~130 Hz). The PFIG's 200 - 300 Ω impedance and the 1:10 multiplication factor result in a relatively large transformer. The diameter of the T-22490 is ~1.8 cm and the height ~2 cm resulting in a total volume of 5.09 cm^3, larger than the volume of each individual FIG. A photo of the realized circuit is shown in Figure 24.

The maximum circuit efficiency is measured using a 130 Hz sine-wave from a function generator with 300 Ω series resistances. The efficiency is 27%. Efficiencies up to 65% have been reported by others regarding other up-conversion works containing transformers [4, 6]; however, these works have source impedances of 3 - 4 Ω, hinting that further optimization is needed

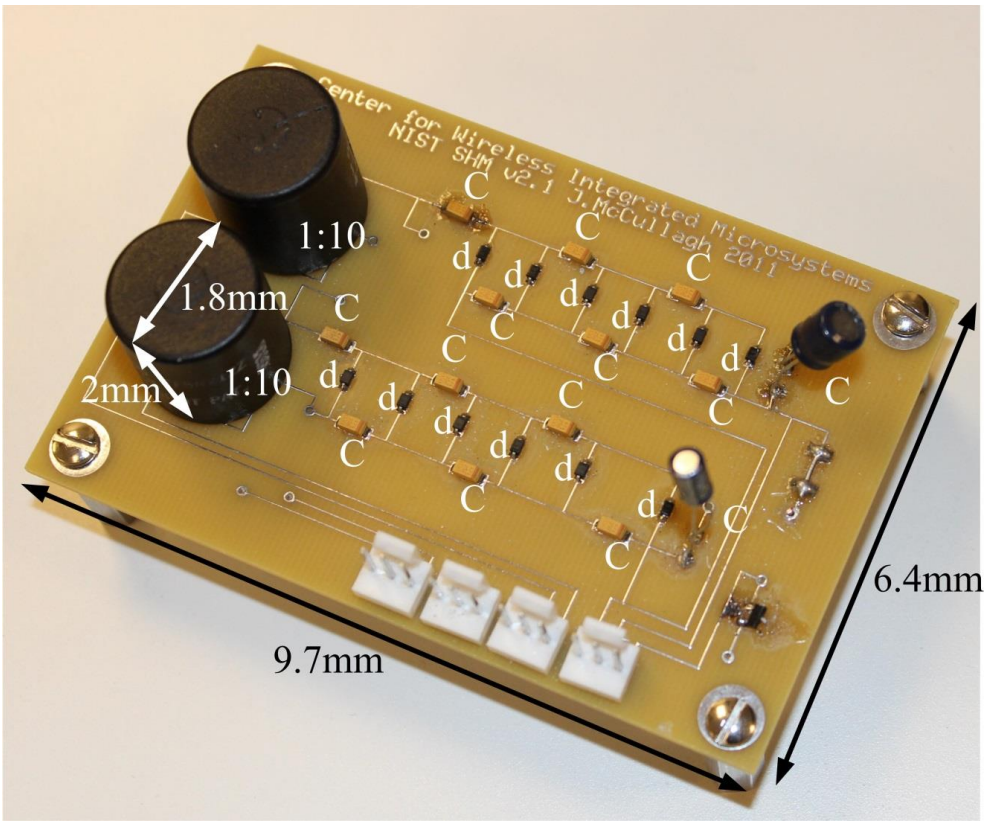

Figure 24. The picture of the circuit used with two transformers and two cascaded Cockcroft-Walton multipliers. Capacitors, diodes and transformers are labeled C, d, and 1:10 respectively.

within the PFIG in the future. Additionally, this author had difficulty fully understanding how efficiency was calculated in the conference paper reporting 65% efficiency [6]. It is possible

various incorrect definitions of efficiency may have been used in this and other works, so it may be difficult to get accurate performance comparisons between some systems presented in literature.

Because the efficiency of a rectifier changes as it charges a capacitor, the output is held constant at 1.2 V by varying the impedance (resistors at the output), while the input voltage is varied. The results are shown in Figure 25. Here the two charge pumps are cascaded and show a maximum efficiency of 27%. A half-wave multiplier only harvests the positive part of the input waveform reducing efficiency. Other efficiency losses are due to the transformers, diode drops, and loading between the cascaded charge pumps. Figure 26 shows the efficiency of a single multiplier (including transformer). The maximum efficiency is 38%, which is higher than that obtained using cascading. Connecting the charge pumps together generates a higher output voltage, but charge coming from the bottom charge pump must again be boosted through the top pump where it will face losses from another set of diode drops and leakage, thereby further reducing the circuit's overall efficiency.

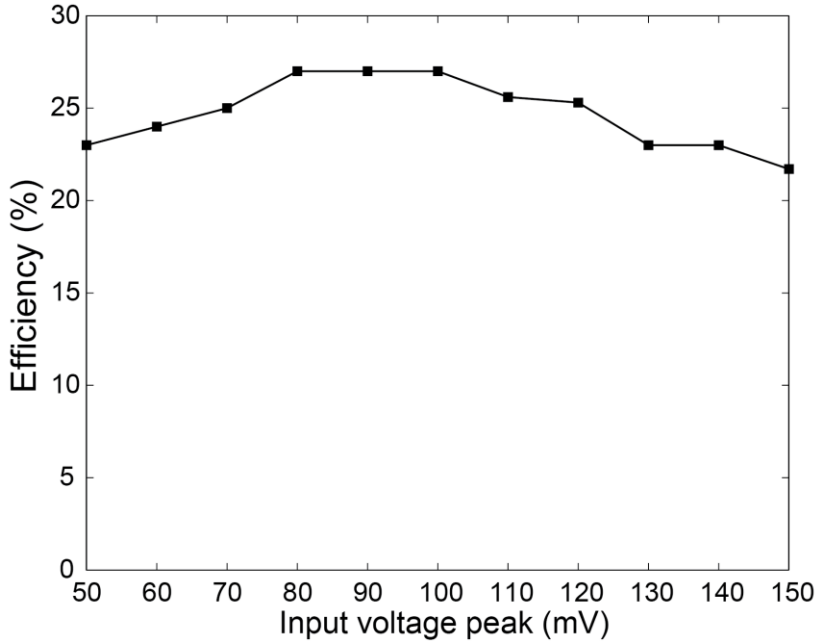

Figure 25. Efficiency of the power management circuit using sinusoidal inputs at 130 Hz in place of FIGs (same output impedance). The output is held constant at 1.2 V by adjusting the output load. Both inputs are changed together to yield a maximum efficiency of 27%.

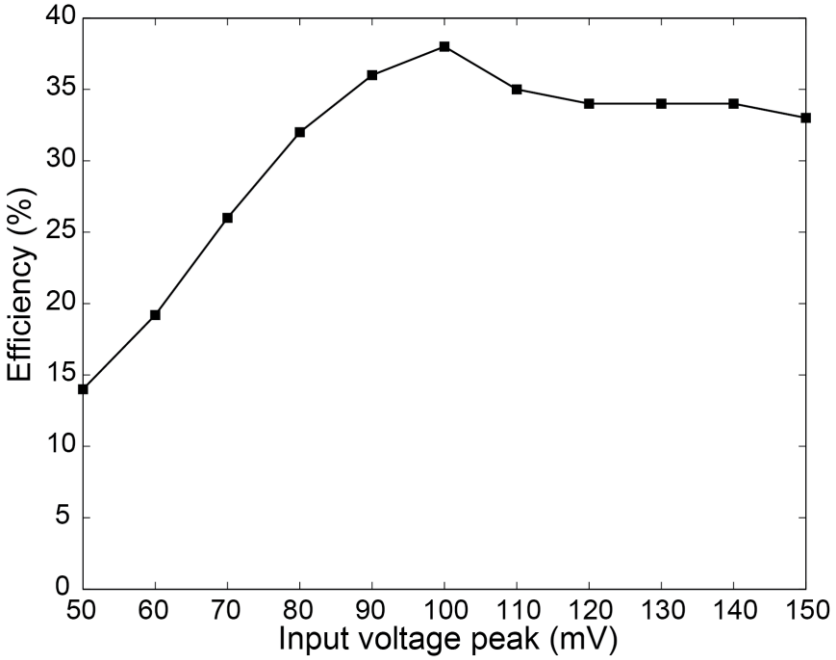

Figure 26. Efficiency of a single Cockcroft-Walton 3-stage multiplier and transformer with a sinusoidal input at 130 Hz in place of FIGs (same output impedance). The output is held constant at 1.2 V by adjusting the output load. The input is changed to yield a max efficiency of 38%.

To determine efficiency in a more realistic way, two function generators are used to approximate the PFIG outputs using two time-offset decaying sinusoids at 10 Hz. A very low input current op-amp (LMC6484, National Semiconductor) buffer is used to monitor the storage capacitor voltage. Holding the output constant at 1 V, by varying the output load, the efficiency was measured to be 14.4%. The measured efficiency of the circuit, charging a 10 µF capacitor from 0 to 0.7 V, is 5.5%. This efficiency is much lower than when the output is held constant. The reason for this is that the capacitors in the charge pump stages must be charged before optimal efficiency can occur at the output.

Table 2 compares the BHS system to other efforts aimed at harvesting low-frequency non-resonant signals. The ability of the BHS system to generate energy in extremely challenging

Table 2. Comparison of non-resonant low-frequency electromagnetic harvester systems

	This Work	**[3]**	**[4, 5]**	**[4, 6]**	**[9]**
Harvester Type	PFIG	PFIG	Up-Conversion	Up-Conversion	Two Coils/ Free Magnet
Minimum Acceleration	0.34 m/s^2	0.54 m/s^2	--	--	0.64 m/s^2
Operation Frequency	2 Hz	2 Hz	10 Hz	10 Hz	6 Hz
Output impedance	275 Ω	1.5 kΩ	3-4 Ω	3-4 Ω	27.5 Ω/55 Ω
Circuit Boosting Method	Charge pump /Transformer	Charge pump	Charge pump /Transformer	Transformer	Charge pump supplies active rectifier
Max Circuit Efficiency	27% (14.4% with decaying inputs)	12%	35%	65%	80% at 5 m/s^2, 6 Hz (Only one coil harvested out of two)

conditions (combination of very low accelerations and frequency) is unrivalled. While this version of power management circuit efficiency still needs to be improved, the challenges in this

application are more stringent than those previously faced by other works [4-6, 9]. Clearly, further improving the harvester electromechanical transducers to produce higher voltage signals with a lower output impedance would greatly benefit the system efficiency. At the same time, active rectification without the use of transformers could be used to enhance the interface electronics because there such a significant decrease in efficiency with the use of transformers. However, this basic charge pump circuit did allow for extensive evaluation of the PFIG and harvesting interface electronics on the NC Bridge.

2.4 Long-term and Short-term testing results and the range of PFIG bridge outputs

The PFIG and harvesting interface were tested on the New Carquinez Suspension bridge in California. There were multiple goals in this implementation. First, understanding of the longevity of both the PFIG and circuit system could be gained in this long term test in a harsh real world environment. Second, an understanding of the range power produced by the PFIG outputs on the bridge could be achieved. Finally, the circuit's response to the non-periodic outputs of the PFIG can be better understood.

2.4.1 On-site short term bridge tests

Two BHS units (containing the PFIG-B2 and passive electronics) were temporarily installed on the NCB for short-term tests. On-site testing allows for more detailed performance measurements to be made. An example of such an installation can be seen in Figure 21a, where the harvester and an accelerometer are magnetically attached under the bridge. Initially, the harvester is tested using a matched load, and the signal is recorded with LabView. Sample waveforms are shown in Figure 27a, where the average power produced is 3.24 μW. Small mismatches in the equilibrium positions of the two FIGs result in the asymmetric actuation.

Table 3 shows the average power generated on the bridge at different locations. Two different versions of the PFIG-B2 were tested (with and without the double magnet structure). The best result in Table 3 is from location 2 where $P_{average}$ = 5.02 µW was generated over a time period of 125 seconds, and represents a 10× improvement over previously reported on-site testing results using the PFIG-B1 [3]. The double and single magnet structure gave similar results in the on-site bridge tests, while in the lab, the double magnet structure performed better. There are two possible reasons for this. First, vibrations on the bridge can vary significantly from minute to minute, and the two PFIG designs were not tested at the same time. Second, the short-term tests were performed before design changes allowed for the harvester to be shipped fully assembled. This means that the harvester was assembled and adjusted on the bridge, resulting in only a rough optimization (much less accurate than a laboratory setting).

Table 3. Short-term results for double and single magnet PFIG designs at different bridge locations.

Location (Figure 21)	**Average Power, PFIG (Double Magnet)**	**Average Power, PFIG (Single Magnet)**
1	4.4 µW	3.24 µW
2	3.13 µW	5.02 µW
3	3.73 µW	--
4	1.6 µW	--

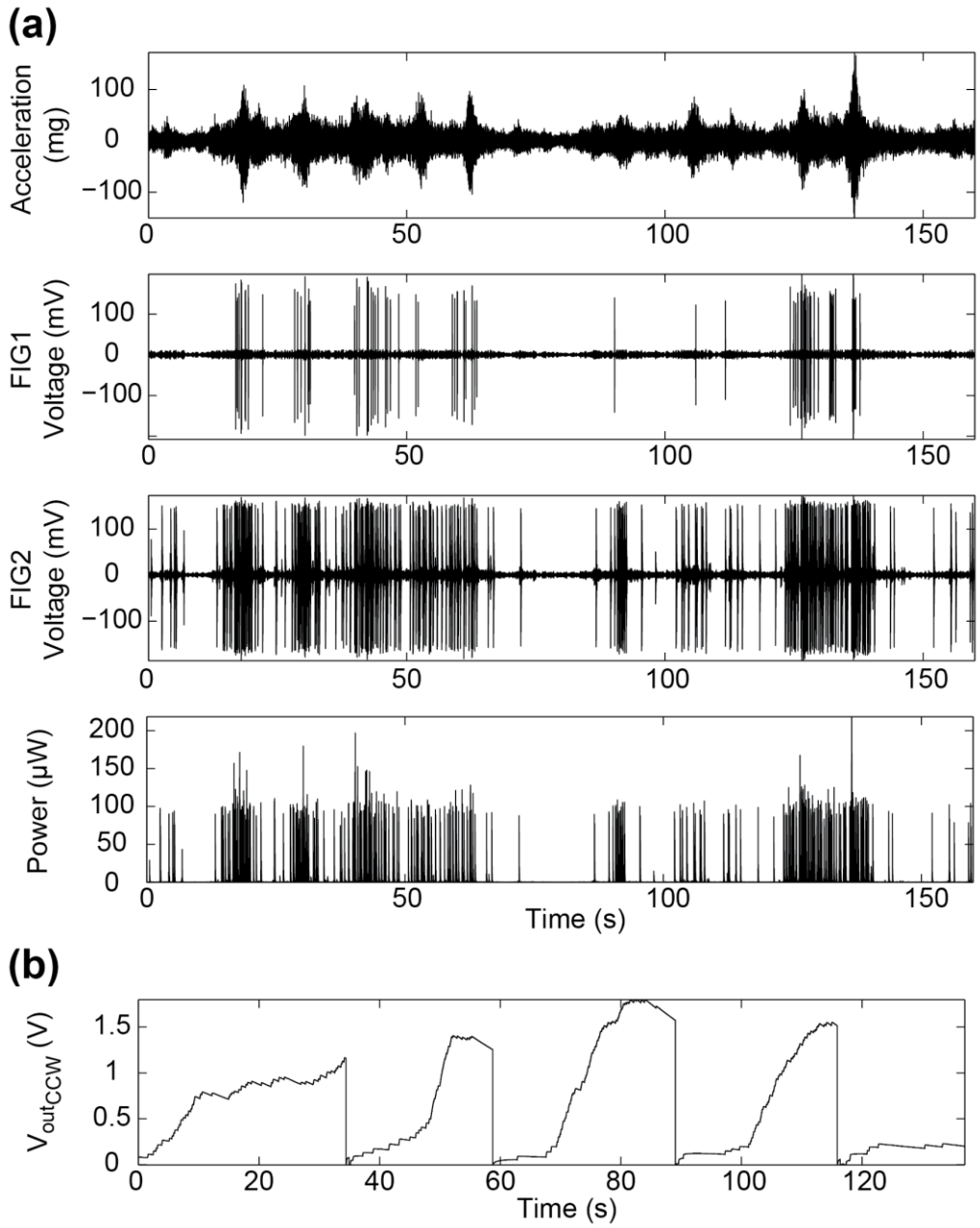

Figure 27. (a) Short-term testing data showing acceleration, FIG1 and FIG2 outputs, and total instantaneous output power taken on the NCB; and (b) separately measured voltage on the storage capacitor taken at a different time than (a) [2].

In a second set of experiments (Figure 27b), the full BHS system (PFIG-B2 and circuit) was tested, and a 10 μF storage capacitor's voltage was repeatedly charged by the PFIG outputs and then manually discharged. The DC output could reach as high as 2 V within a reasonable time period (48 seconds); however, as seen in Figure 27b, the higher the voltage, the slower the

capacitor charges. At high output voltages, the lower voltage peaks of the decaying waveform are not harvested, while the highest peaks are harvested at a reduced efficiency. As the output voltage further increases, the peaks are no longer able to add any charge and so a maximum achievable voltage is reached. Additionally, there are parasitic leakage paths that limit the voltage, especially when the vibrations are sparse. The storage capacitor was continually discharged so an understanding of the rate at which the storage capacitor charges could be gained and used to optimize the system for the long-term installation discussed in the next section.

2.4.2 Long-term bridge test implementation

The goal was to install and monitor the BHS over a long period of time and to monitor the FIG outputs and the storage capacitor voltage, so that the BHS performance can be quantitatively assessed. For this goal a special-purpose *Narada* [4] wireless sensor node, already deployed on the NCB, is used. The *Narada* node samples the key BHS metrics once per hour for 90 seconds at a sampling rate of 100 Hz. The results are wirelessly transmitted to a base station and are then available through remote access [10]. To facilitate the long-term evaluation of the BHS, the *Narada* node automatically discharges the storage capacitor when it reaches 0.7 V. This allows for the average power to be estimated by the number of discharges in the 90-second sampling period. Solar cells on top of the bridge are wired and power the *Narada* node allowing it to perform the described functions. The BHS is not used to power the *Narada* wireless sensor node. Figures 28a and 28b show the long-term test system. The PFIG, harvesting circuit, buffer and level shift circuits, transmission antenna, *Narada* node, and rechargeable batteries (powered by solar panels on top of the bridge) are contained inside a commercially available water-tight box. The batteries are used to power the *Narada* system, the buffers, and the level-shift circuits, which interface the BHS to the *Narada* node. The dimensions of the box are 30.5 x 20.3 x

13.2 cm. On April 30, 2012, two of these water tight boxes were installed under the bridge deck at location 1 (Figure 21b).

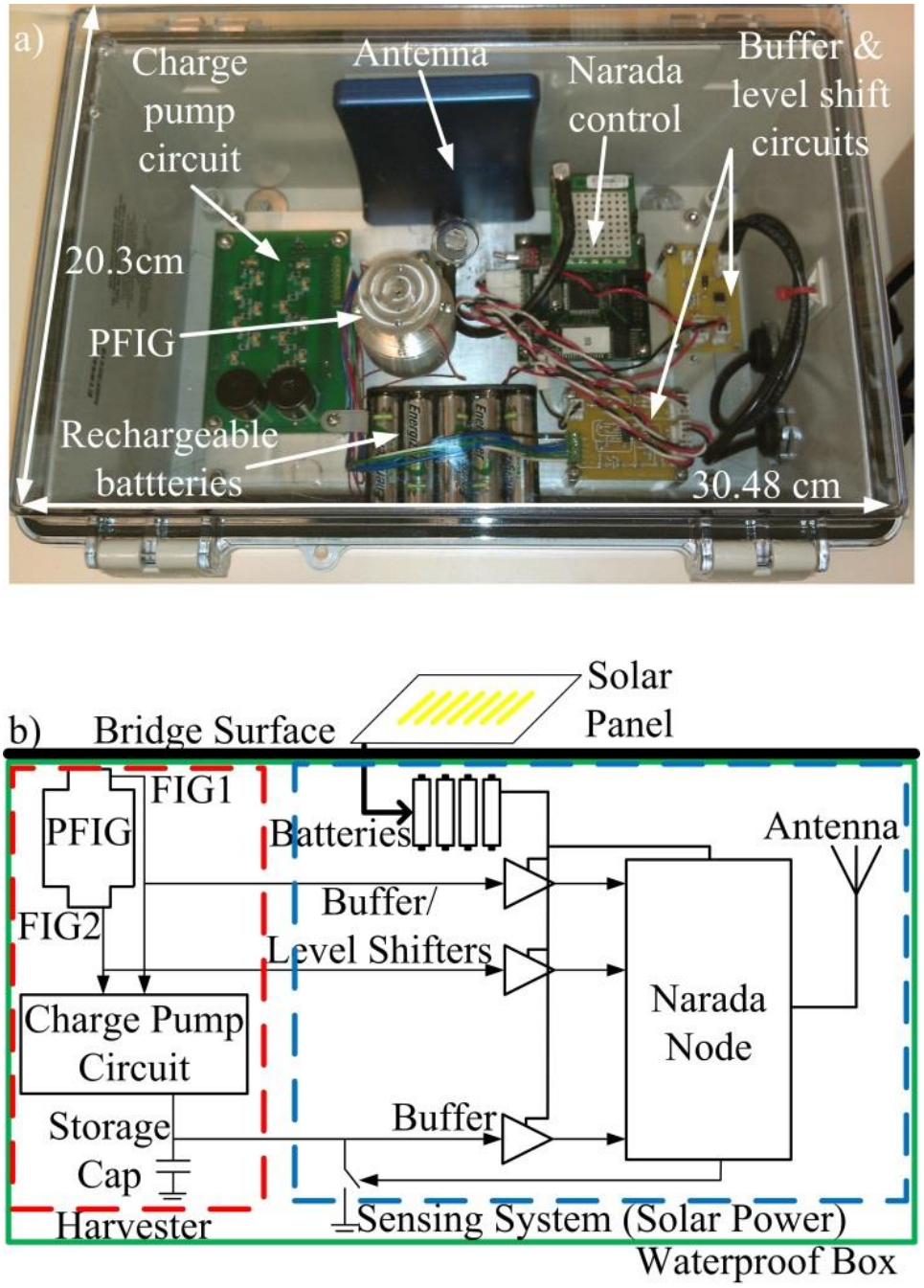

Figure 28. The PFIG, passive harvesting circuit, *Narada* control, *Narada* antenna, buffer and level shift circuits used in the long-term test on the New Carquinez Bridge. a) The water tight box and b) a schematic of the long-term test system [2].

2.4.3 Long Term Results

A sample of recorded data is shown in Figure 29. The voltage on the storage capacitor rises faster and is discharged more frequently when the FIGs actuate more often and at higher amplitudes. The FIG outputs are under-sampled at 100 Hz (sample rate chosen to minimize *Narada* power consumption). Nonetheless, the basic functionality of the system can be discerned from the plots. The circuit in Figure 23 is used and while this circuit suffered from significant efficiency problems, it was well suited for a long-term test because it could quickly charge up the storage capacitor to between 0.7 V and 1 V.

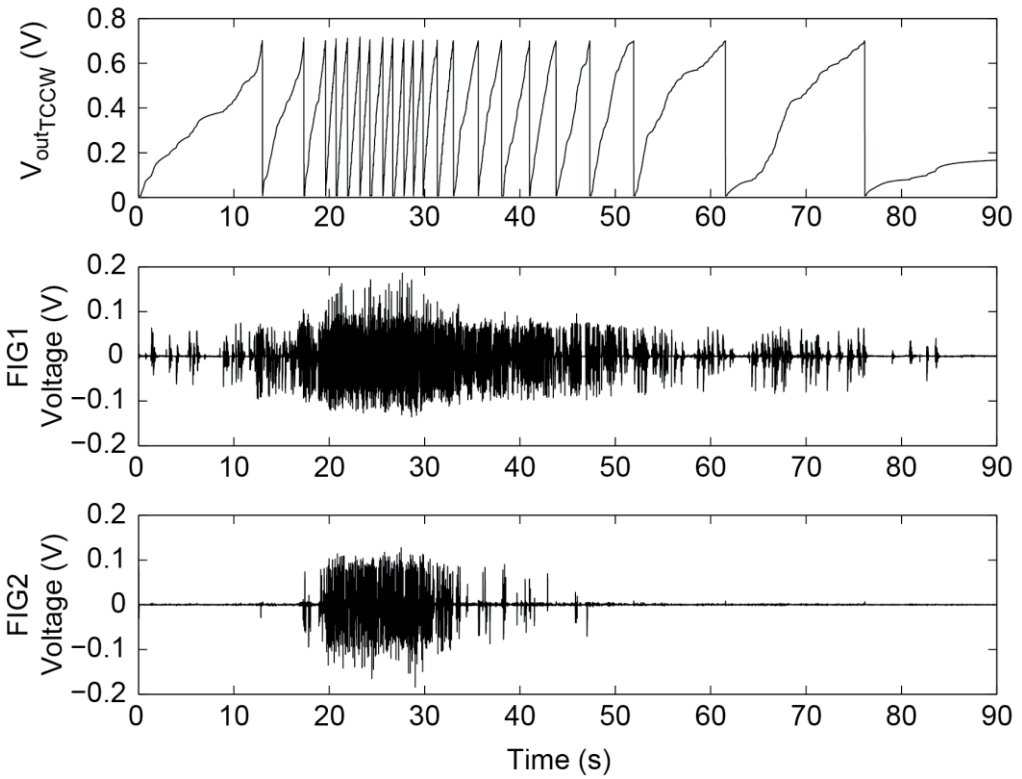

Figure 29. Data recorded on May 29, 2012 by the *Narada* wireless node [2].

Figure 30 summarizes one week of data. Harvested power is greater during daytime and weekdays. Each discharge occurring at 0.7 V on the 10 µF capacitor, recorded during a 90

second period, corresponds to 27 nW of power delivered to a load. Once again, it should be noted that data recordings are only made once per hour and the number of discharges shown in Figure 30 is only during the several 90 second measurement windows. Lab measurements described earlier estimated the efficiency of the PFIG and circuit during start-up to be 5.5%. Therefore, each capacitor discharge corresponds to an unprocessed PFIG output power of ~0.5 µW, and the results in Figure 30 indicate a nearly identical amount of power harvested during daytime (2-12 discharges or 1.0-6.0 µW) as was measured during the short-term tests of the PFIG (Table 1). Figure 31 further verifies these power levels. It shows a histogram of the number of discharges in a 90 second period from May 1st to June 18th in 2012. Figure 31 shows the histogram peak centers around 1 and 2 discharges, with 0 to 11 discharges being common. The mean and median of the data in Figure 31 is 3.29 discharges and 3 discharges. As each discharge represents approximately 0.5 µW produced by the PFIG, it can be concluded that for an optimally functioning PFIG, average power in the range of 1.5 µW to 2 µW is common, going up to 3 µW during daytime.

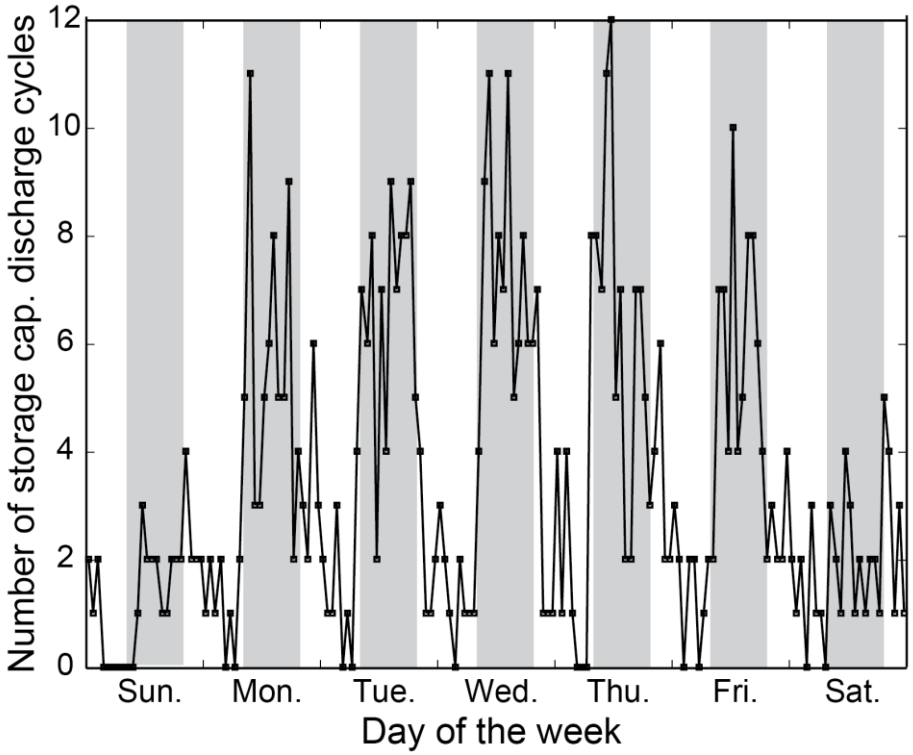

Figure 30. Circuit discharges for one week starting May 13, 2012. Each circuit discharges represents approximately 0.5 µW in unprocessed PFIG output power. The shaded areas represent 8am to 8pm [2].

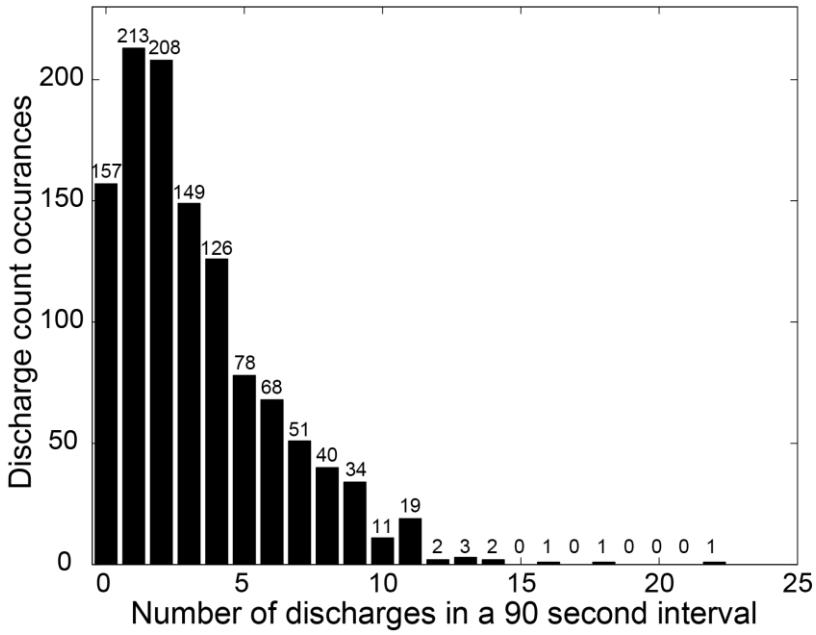

Figure 31. A histogram of the discharge counts per 90 second period. Data from May 1st – June 18th is shown. The median value is 3 while the mean value is 3.29. The specific discharge count occurance frequency is shown above the histogram bar.

The BHS has operated continuously on the NCB for 13 months starting April 30, 2012 (Figure 32), and the experiment is still ongoing as of the writing of this thesis (January 2014). Starting in late May 2013, the wireless data collection system began to have outages. In many of these cases, measurements from the BHS were still received a few times a day. The root cause of this is the solar harvesting used to power the Narada. The raw output of both FIGs and storage capacitor are regularly checked to verify the Narada is transmitting successfully and the raw discharge count can be believed. Likely, either there is not enough light, debris and dust collected on the solar cells, or the rechargeable batteries that store the energy for the Narada have degraded. This highlights a potential weakness of solar energy harvesting in unmanned systems. During future retrieval of the harvester from the bridge, measurements will be made to verify if it is still functional. In the long-term test (Figure 32), the same weekly pattern seen in Figure 30

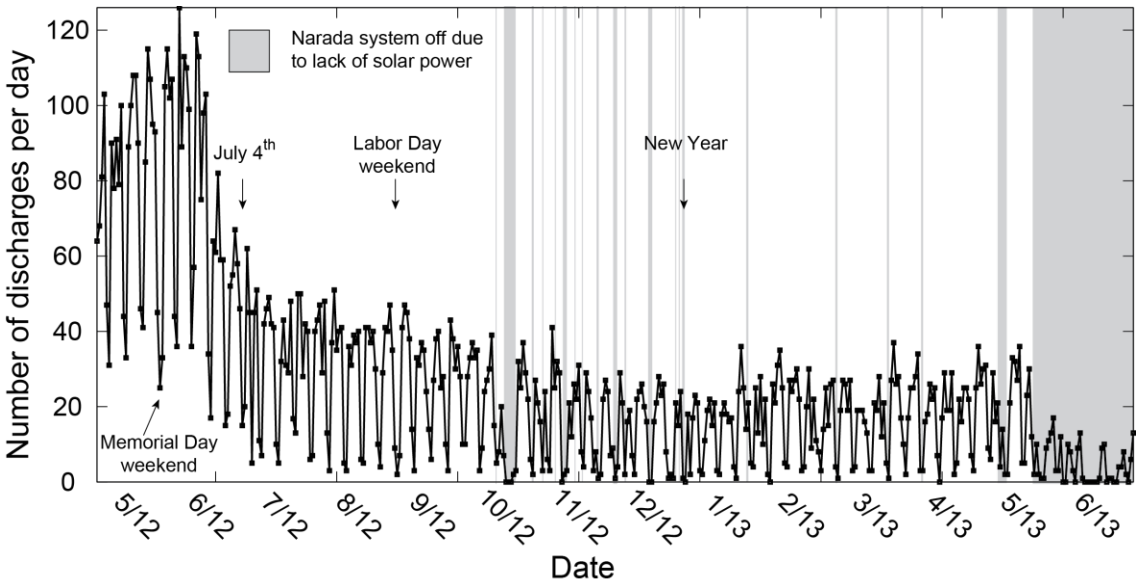

Figure 32. Entire transmitted data set since installation on April 30, 2012. Each point represents the total number of discharges per day over 24 ninety-second recording periods. Grey areas represent periods where the *Narada* system was not functional due to solar panels not collecting power (i.e. June 2013).

continues to be observed, as well as sharp drops in harvested power on U.S. national holidays. Over the first six weeks the power output remained relatively consistent. The highest power was recorded the morning following Memorial Day on May 29th, 2012 and is estimated to be 10.9 μW (22 discharges over 90 seconds, Figure 29). The data clearly demonstrates that the power harvested correlates directly to traffic and thus could be a sensed variable itself. The PFIG exhibited a reduction in power at the end of June, producing approximately half as much energy. The most probable mechanism for such a decrease will be discussed next.

2.4.4 Long-term performance discussion

The results in Figure 32 show a significant reduction in performance after around six weeks in mid-June. While the exact cause is not known because the experiment is still ongoing, the reduction in energy by half immediately raises the question whether both FIGs are working. For the ease of assembly the individual FIGs are held in place only by the friction of set screws along the side of the FIG casing as well as one on the bottom. This makes this assembly method susceptible to slipping. Additionally, since a wide range of frequencies and amplitudes are exhibited on the bridge, the response of the inertial mass-spring system can be unpredictable. It can be driven into resonance at its natural frequency around 10-12 Hz, and at high amplitudes it can begin to strike the top of the FIG casing, which also serves as a safety barrier to protect the internal mechanism. Experimental results in both the laboratory and during the short-term tests have shown that striking the end-stops can drive the inertial mass system into a non-linear regime that can even amplify the amplitude of the motion. In the laboratory, it was verified that repeated contact between the inertial mass and the FIG surface produces enough force to alter the FIG positions. The changed spacing and alignment of the components then leads to an increase

in the minimum acceleration needed for proper operation and the reduction in power seen in Figure 32.

Before the long-term bridge test, all set-screws were well tightened and Silca Gel Packets were included in the water-tight box. However, temperature changes, the high humidity, and other environmental factors may have been enough to weaken the set-screw grip and allow ~10-40 micrometers in slippage, which would be enough to disturb the optimal operation of the BHS. The set-screws were included to allow for different experiments to be carried out in the lab by varying the FIG positions, prior to PFIG-B2 installation on the bridge. In the future the set-screws will be removed and other methods will be used to fix the FIG positions within the harvester mechanism. In the broad area of vibration harvesters and frequency up-converting harvesters such as the PFIG, analysis has been done on what environmental conditions can potentially cause harvester failure where functioning stops [11]. Usually this analysis focuses on damage that can be caused by a single shock to the system that can physically break the system. This long-term study shows that the damage can be gradual, and the harvester may still be functional even after damage has occurred.

2.5 Conclusion

This chapter discusses the development and long-term testing of a bridge harvesting system (BHS), including improvements in the vibration harvester and its power management circuitry with the goal of providing power for structural health monitoring. The short-term and long-term testing of the BHS on the New Carquinez suspension bridge shows a 10× improvement in unprocessed harvested power (PFIG-B2) [2] compared to a previous version (PFIG-B1) [3]. A new power management circuit is presented, which can “cold-start” without any pre-charged voltage and can boost the very low-voltage and decaying PFIG signal. By using

a transformer followed by a charge pump, a 10 µF capacitor can charge up to 2 V on the bridge. The average unprocessed PFIG power is between 1 µW and 6 µW, while the maximum observed power is estimated to be 10.9 µW. The output of the PFIG was estimated from the start-up efficiency mentioned earlier. This long-term test then could be used to specify the requirements for an active diode circuit which will be discussed in section 2.3, and these results show that there will be enough power during the day to regularly power an active diode IC.

The long-term study showed a decrease in harvested power after approximately six weeks. A likely cause of this reduced power is slippage of the FIG position, which has been repeated in the lab and can be eliminated in future harvester designs. The circuit efficiency of 14.4% allows for a 10 µF capacitor to quickly charge to a high voltage based on the low voltage PFIG inputs allowing for the circuit's use in the long-term test. This circuit provides a proof-of-concept design with efficiency that can readily be improved by using active circuits designed in a low-power IC technology and by eliminating the transformers. The most unique result is that the BHS system has been continuously functional and monitored for more than one year since April 30th, 2012 (on going) on the New Carquinez Bridge in California. Energy harvesting applications derive their value from the ability to operate for many years and decades, and this is the first long-term study of a mechanical harvester and system.

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Chapter III

16x Active Diode Charge Pump Circuit Design and Innovations

3.1 Design Description

An IC-based architecture (Figure 33) was taped out in June 2013 with the goal of eliminating the transformers, producing low voltage low power start-up, and achieving high harvesting efficiency once the system was started. The goal of this structure was to enable active diode functioning very early on in the start-up of the system while in deep sub-threshold. This IC-based design (Figure 33) improves upon the discrete design by eliminating the inherent diode

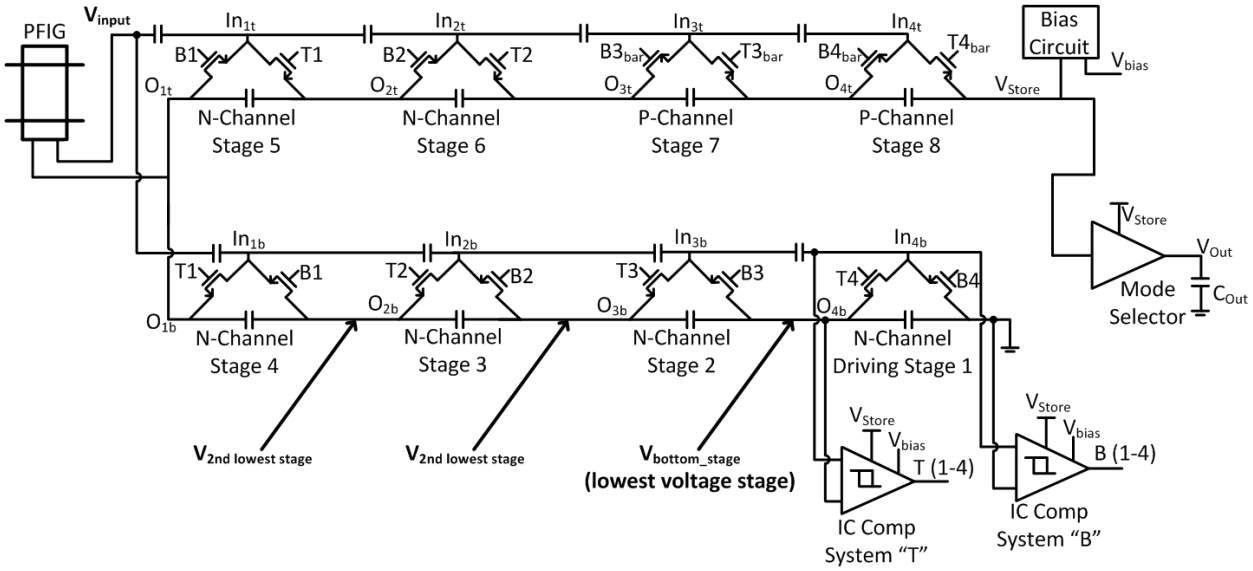

Figure 33. An eight stage full wave Cockcroft-Walton active diode charge pump with the driving comparators on the lowest voltage stage next to ground are shown. Four stages go in the negative and positive direction.

drops in both sub-threshold and regular functioning by using active functioning. These active diodes improve upon the discrete design by adding additional boosting ability. Also, an adjustable mode selector is included so that voltage at which the capacitive load charges can be

optimized. Finally, the use of the lowest voltage stage driving all comparators increases the ability of the IC-based system to start-up in deep sub-threshold functioning and operate in regular functioning with ultra-low power inputs. The lowest voltage stage comparators work in deep sub-threshold functioning based on the Cockcroft-Walton multipliers characteristics that charge the stages farthest from the input last.

In this design, start-up can be achieved at an input voltage below the V_{th} (and passive diode turn-on voltage) in the given technology (CMOS 180 nm with a V_{th} ~0.42 V). The use of an IC also allows flexibility in choosing the PFIG output impedance. No longer would the output impedance need to be reduced to meet the transformer's matching limitations as in Chapter 2. A charge pump, rather than an inductive based boosting circuit, is still necessary for this circuit to enable cold-start. While inductor based circuits can boost the output of a vibration harvester, they either require a pre-charged battery [1] or a charge pump circuit, which is used for start-up and then allows a LC boost circuit to turn on for regular functioning [2].

Current state-of-the-art discrete active diode charge pumps show minimum cold start near 500 mV and regular functioning near 350 mV [3]. They require passive diodes formed from the free bulk connections (not available in some integrated CMOS technologies) for cold start because the discrete comparators do not operate until they reach near 2 V. In fact, all of the circuits that can start-up are limited by their passive diode turn-on voltages. Solutions that can overcome this minimum passive diode-based turn-on would have considerable value to all types of energy harvesting circuits. Along with the passive diode limitation, these discrete active diode solutions consume near 6.4 µW of average power (greater than the power regularly produced by a PFIG on a bridge) [3]. In this discrete configuration large capacitors (47 µF or higher) give optimal power conversion efficiency [3]. Higher capacitances (not possible in an IC), will

continue to be necessary in this classic charge pump architecture when, and an IC with external pads can connect to these large capacitors. The use of IC technology to implement an active diode charge pump that advances the state-of-the-art in the areas of sub-threshold start-up without reliance on passive diodes, low voltage functioning, low power functioning, and high power conversion efficiency functioning is a major contribution of this thesis.

This deep sub-threshold active diode functioning will enable dramatically improved start-up ability for low power low voltage inputs that are well below the V_{th} of the CMOS technology. Once the system was started and stabilized, operation for optimized efficiency was enabled. All of these characteristics were made possible using the characteristics of a full wave Cockcroft-Walton charge pump multiplier that were described in Chapter 1.3. This full wave multiplier for this IC-based system consists of 8 stages. Four stages (stages 5 -8) harvest the positive part of the signal on top of the charge pump, while four stages (stages 1-4) harvest the negative part of the input signal on the bottom part of the charge pump in Figure 33. Each stage doubles the voltage, and with 8 stages, the maximum theoretical voltage is ~×16 the peak input voltage. This

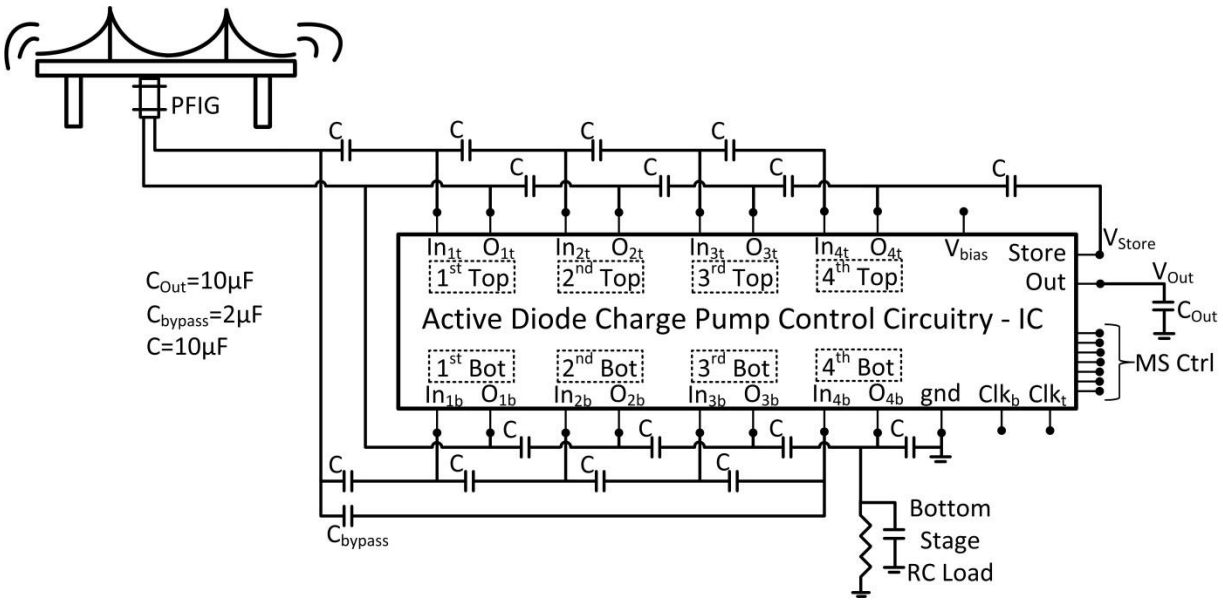

Figure 34. The off-chip and on-chip components of the system are specified.

architecture included a Schmitt trigger like circuit called a “mode selector” [4] to avoid loading during start-up. Also, two comparators drive the active diodes of the entire system through inverters on the lowest voltage stage using a common gate comparator. This lowest voltage driven architecture facilitates efficient low voltage functioning out of sub-threshold and start-up in deep sub-threshold.

Figure 34 shows this architecture with on-chip and off-chip components of this system. Additionally, simulation of this circuit requires a low value bypass capacitor used to aid in the simulated start-up of the circuit to make sure that the signal initially reaches comparators to allow them to more easily work. In hardware, the bypass capacitor was never needed for optimal functioning, and the insertion of the bypass capacitor would decrease efficiency in actual hardware. All of the system comparators are driven by the decision on the lowest voltage stage to allow for high margin in sub-threshold operation. “Margin” in this situation can be thought of as an extra difference in the inputs into the comparator above what would normally be expected to switch the comparator. For example, if the comparator normally switches when and the inputs differ by 10 mV in regular functioning, a difference of 50-100 mV may be needed in in deep sub-threshold. The lowest voltage stage takes a significant amount of time to begin charging, even though the signal reaches the lowest voltage stage to allow functioning. This process will be explained in depth later in this chapter. To aid in evaluation and fix potential issues, the biasing lines are brought out to the pads. This could potentially be very helpful if the bias were to oscillate. For example, in a previous IC design, the bias oscillated, and it was able to be fixed with a large resistor (5 MΩ). This created a filter stopping the oscillation. Also, the clocks from the top and bottom comparators are buffered and brought out to the pads to enable understanding of their functioning.

This design uses a mode selector circuit that lets current pass when a specific and programmable voltage is reached. It is similar to the mode selector used in RF harvesting designs to allow the charge pump to connect to the final output at a given voltage [4]. This mode selector is adjustable to allow its output to turn on at various voltages. Seven control lines for this mode selector device are indicated in Figure 34. This allows charging into V_{out} at various voltages. The mode selector (Figure 35) contains large resistors that take up a significant amount of space in the actual circuit, making the circuit area larger. These large resistors are actually larger than the size of the active diodes and control circuitry. As seen in Figure 36, the circuit still occupies a small portion of the total chip area (this IC is 1.0 mm x 1.2 mm). The mode selector consists of a simple amplifier with two inputs controlled by diodes and large (5 MΩ) resistors. Depending on the characteristics of the diodes on the input stages, the mode selector turns on at different voltages indicated in the table in Figure 35. The diode characteristics can be changed by connecting the MS pins. The simulated values at which the mode selector turned on were very similar to what was seen in hardware. The bottom of Figure 35 shows the behavior during start-

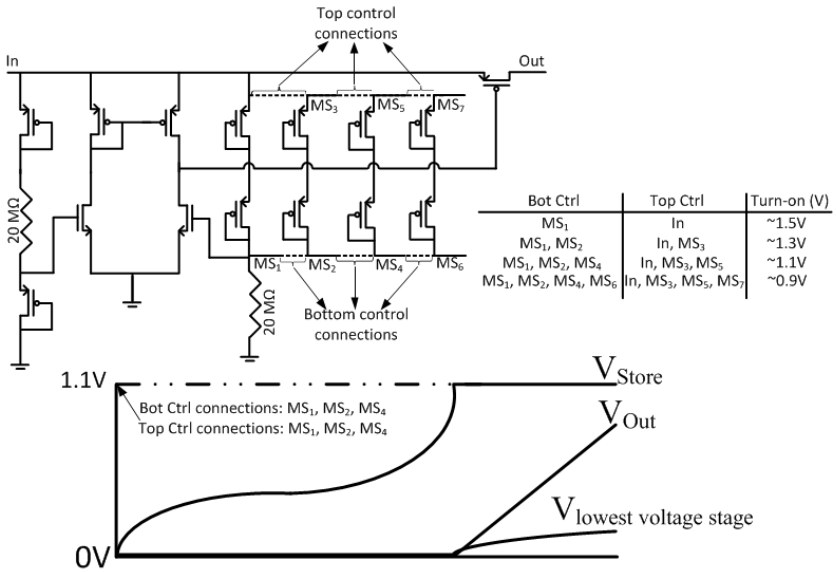

Figure 35. The adjustable mode selector is shown similar to other circuits previously used in RF harvesting [5]. A table shows how the connections can adjust the turn on voltage functioning that is ideally drawn below the figure.

up. The voltage on the lowest voltage stage starts to rise more significantly once the charge pump starts to charge the capacitive load. Analysis of the effect of changing the turn on voltage on system performance will be described later in this chapter (Section 3.3).

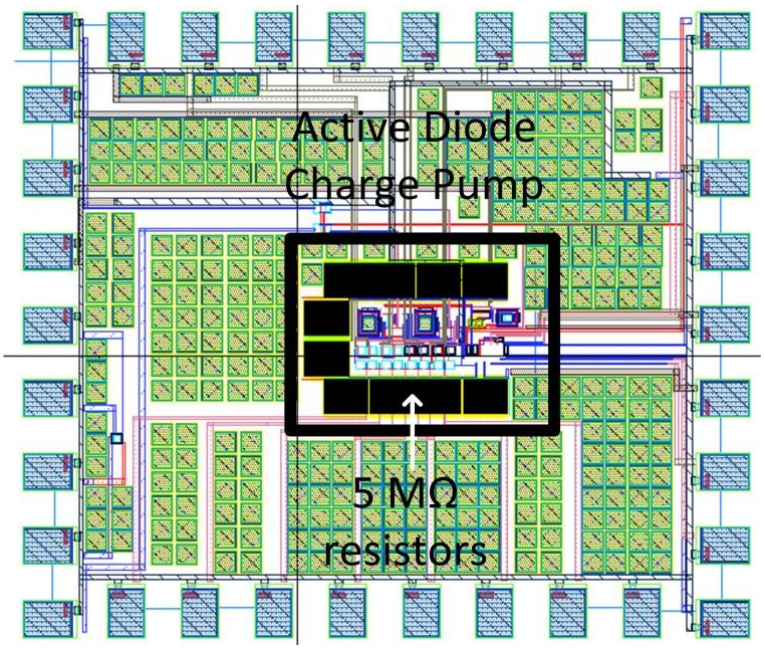

Figure 36. The layout of the chip fabricated in 180 nm technology is shown. A rectangle surrounds the active diode charge pump area in the layout, and the 5 MΩ resistors are indicated.

A differential common gate comparator is used on the lowest voltages stage of the full-wave charge pump (Figure 33), and this first comparison drives the rest of the stages through buffers. This comparator and inverter/buffer chain are shown in Figure 37. This comparator and inverter structure is ideal for this architecture, and only the comparators on the lowest voltage stage need to function well for the system to be operational with low voltage input in deep sub-threshold operation. Inverters will always be more likely to operate at some level in deep sub-threshold because they inherently operate with significant margin. Rather than trying to discern between voltages of similar values like a comparator is trying to do, inverters must either recognize a “high” or “ground” input, and recognizing these signals is far easier in deep sub-threshold for an inverter versus a comparator.

The proper comparator choice also aides in harvesting low voltage inputs while working in the sub-threshold regime. First, the common gate comparator has inputs on its sources rather than the gates. This way the comparator needs to only recognize the difference between two low voltages at the sources of its inputs rather than at gates. Needing to have the inputs on the device's gates forces the use of sub-threshold functioning in all circumstances. This sub-

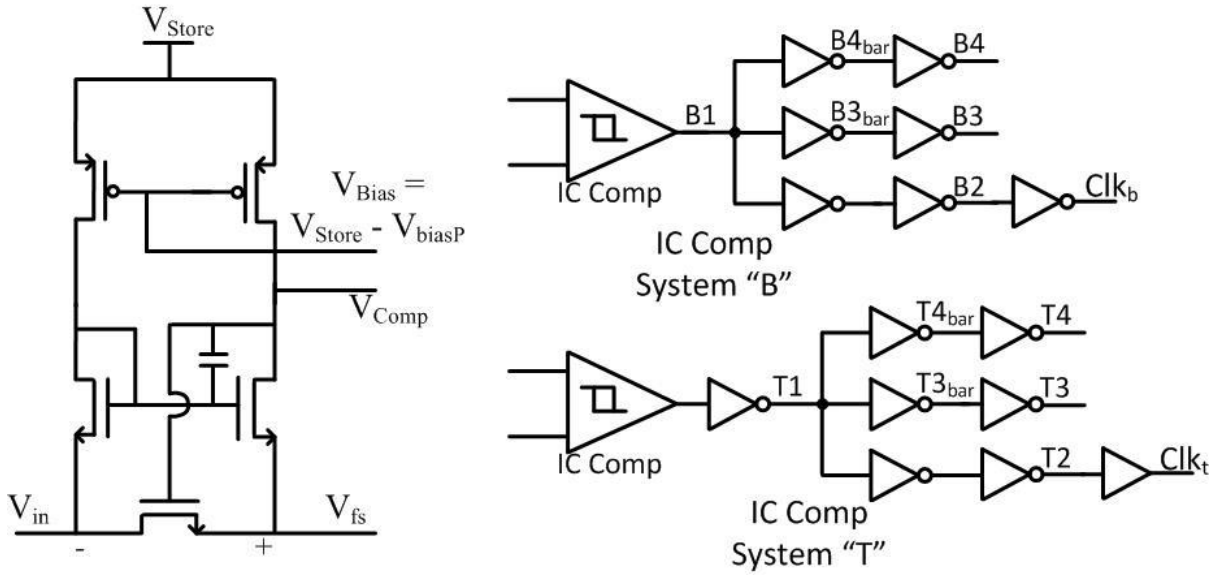

Figure 37. A differential common gate comparator regularly used in energy harvesting literature [6, 7] is shown. The (+) input is the output of the first stage of the charge pump.

threshold functioning is necessary because the low input voltages would need to overcome the V_{th} of the inputs when driving the gates of devices. Using the sources of the devices that are biased near ground means that the comparator is less likely to need to work in deep sub-threshold functioning. As long as V_{store} is high enough to keep the comparator out of sub-threshold functioning, the use of this comparator will mean that sub-threshold functioning is never necessary. If the comparator's V_{store} is too low for regular operation, the bias voltage into the comparator will also be low, and the system must work in sub-threshold, this comparator still works as long as the first stage voltage of the charge pump also stays low. The input offset

voltage into the comparator ranges between 0 and 200 mV allowing for optimal functioning. The Cockcroft-Walton charge pump behaves in such a way as the lowest voltage stage charges last as described in Chapter 1.3. Similar comparator designs have been used in other energy harvesting applications [6, 7]; however, these applications do not make use of the comparator's ability to function with low input voltages in and out of sub-threshold design. Finally, the bias generator [6] is used to allow the bias voltage to turn on when V_{store} is at least at V_{th}. Once on, the bias generator maintains a voltage that is one V_{th} away from V_{store}. Figure 38 shows the bias circuit which can produce two voltages. The higher voltage "VbiasP" is used in this design.

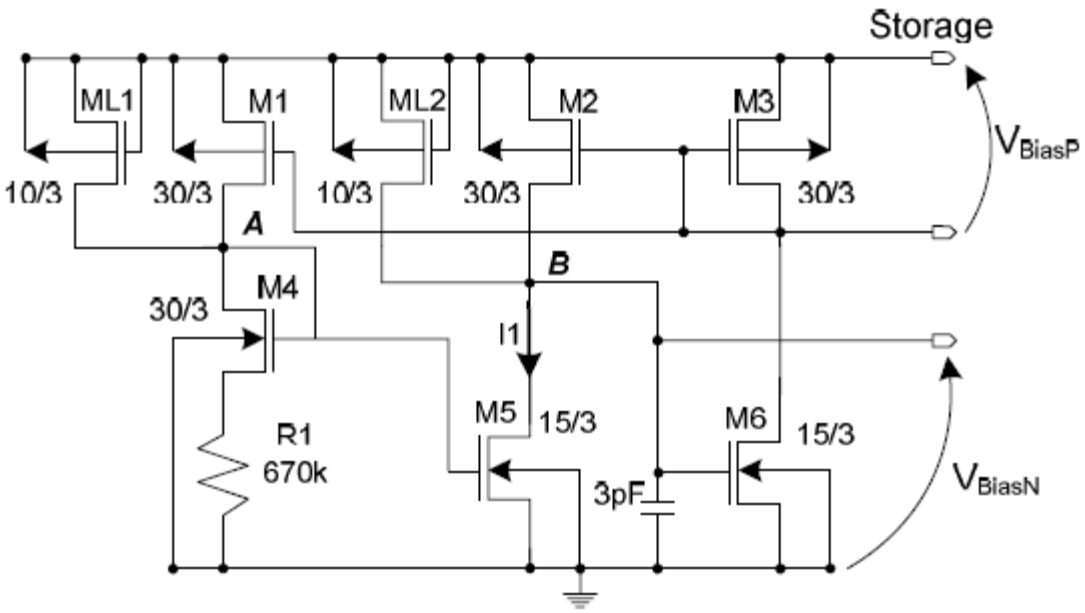

Figure 38. A bias generation circuit used in this system is shown [6].

3.2 Simulation Results of the 16x Charge Pump Design

Solid simulation results were observed with this new ×16 charge pump design. Power conversion efficiency and minimum start-up results are seen in the Tables 4 to 6. The circuit is able to operate at high efficiencies that would have been impossible with lower boosting (for example, a 150mV input producing 70% efficiency at an output of 1.2 V would not be possible

with only ×6 boosting). Data was taken for a range of sine-wave inputs and a PFIG like input. Also, a 335 mV minimum start-up is shown. This is a significant improvement over simulated IC results for a ×6 boosting system that will be discussed in Chapter 4 (version 1). This ×6 IC-based boosting system was only able to start-up with an input at ~700 mV in simulation. The present system was able to start-up down to 335mV with 100 µF capacitors following the mode selector. The simulated start-up is seen from Cadence in Figure 39 where both the output storage capacitor (10 µF), and the V_{store} output are shown with a 340 mV input. It is seen that V_{store} stays low for 2 seconds. In these 2 seconds the bias of the circuit is not on; however, the comparator is still functioning. Once the bias circuit begins to function, the circuit rapidly charges. This deep sub-threshold functioning, discussed later in this Chapter, was further verified in hardware.

Table 4: This shows simulated sine-wave efficiency at different voltage levels with a 300 Ω input impedance

AC Input Peak Voltage (mV)	Input Power (µW)	DC Output (V)	Efficiency (%)
150	9.38	1.2	70
200	16.67	1.2	72
250	26.04	1.2	74
300	37.50	1.2	67
400	66.67	1.2	60

Table 5: This shows simulated efficiency with a PFIG like input with a 300 Ω input impedance

AC Input Peak Voltage (mV) (extraction)	Input Power (µW)	DC Output (V)	Efficiency (%)
Decaying Sinusoid (450 top peak & 100mV lowest peak)	12.00	1.2	56

Table 6: This shows minimum start-up performance of corners and compared to the first IC's simulation

Minimum Start-up (mV)	IC Conditions
335	typ
370	ff
350	ss
700	Chapter 4 (version 1)

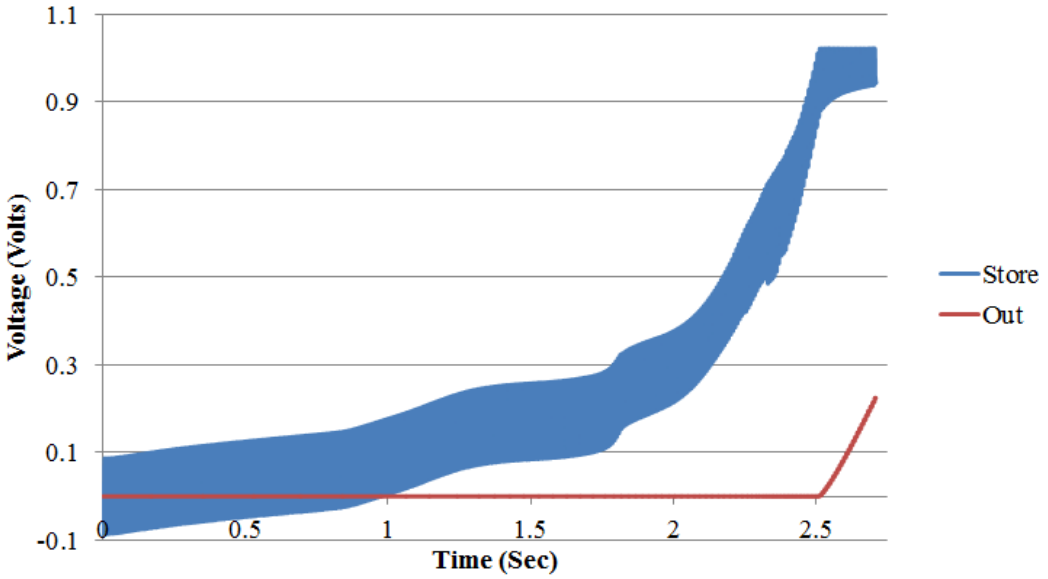

Figure 39. Cadence simulation results showing cold start-up in the ×16 IC are shown. V_{Store} is shown in blue and the V_{Out} is shown in red. At ~1.0V the load capacitor on V_{Out} begins to charge.

3.3 Start-up Hardware Analysis

Start-up in this system begins when the system is off, and ideally every node is charged to zero volts. Initially, the input voltage from the harvester is boosted in the charge pump system via passive diode sub-threshold rectification using the NMOS and PMOS devices. All systems capable of start-up must use some type of passive rectification for start-up because a system cannot use active diode rectification with a 0 V power supply. In the case of this system, passive rectification is only needed until the system supply (V_{store}) reaches ~150 – 200 mV and active rectification can begin. During initial start-up, the gates of the all active diodes are floating between 0 and V_{store}. This means that the two top PMOS stages and the bottom four NMOS stages will initially act to some degree as sub-threshold passive rectifiers allowing for initial start-up. The top PMOS diodes allow for some conduction as the harvester input nears the value of the gate voltage floating between 0 and V_{store}. For example, during the very initial start-up, the gate of PMOS is near 0 V, and the source is near 100 – 200 mV. In this case, either side of the

PMOS can act as the source, so the input acts as the source due to the symmetric nature of the devices in CMOS technology. While this is not enough to overcome the V_{th} of the system, enough current still flows (versus when the input on the PMOS source is negative) to allow for some charging and start-up to near 100-200 mV on the supply V_{store}.

Similarly, the bottom NMOS diodes allow for conduction of the negative portion of the harvester's input when it is far below the gates (0 and V_{store}) on the bottom NMOS devices. For example, during initial start-up, if the negative input at the source of the bottom NMOS devices is between -100 and -200 mV and the gate is positive (between 0 and V_{store}), the NMOS devices conduct far more when the input is negative than when the input from the harvester is positive. This means the negative portion of the input is able to charge the voltage on the bottom portion (the portion that is entirely NMOS) of the charge pump raising the overall voltage V_{store} on the top of the charge pump.

The first two NMOS stages on the top charge pump were chosen as NMOS to optimize efficiency once the circuit was started, but if a future design needs to be optimized for minimum start-up; all devices on the top positive charge pump may need to be PMOS. At first these two NMOS stages of the top multiplier are unable to help start-up and may even prevent start-up; however, as the system quickly begins to turn-on, the deep sub-threshold functioning allows these two NMOS devices to quickly begin to function. This initial start-up is not the main limiting factor for start-up of this system. Initial start-up and active sub-threshold functioning can begin as low as 100 mV; however, sub-threshold active diode start-up failure (the active diodes no longer function) is likely to be when V_{store} is near 300-400 mV. This will be described later in this chapter. Figure 40 shows this initial start-up without clocking. With a 350 mV input, Figure 40 shows that V_{store} quickly rises, and it takes until V_{store} reaches 200 – 300 mV before the clocks

begin to function. Once the clocks begin to function, V_{store} rises another ~200 mV to near 500 mV before the voltages on the lowest voltage stages begins to rise.

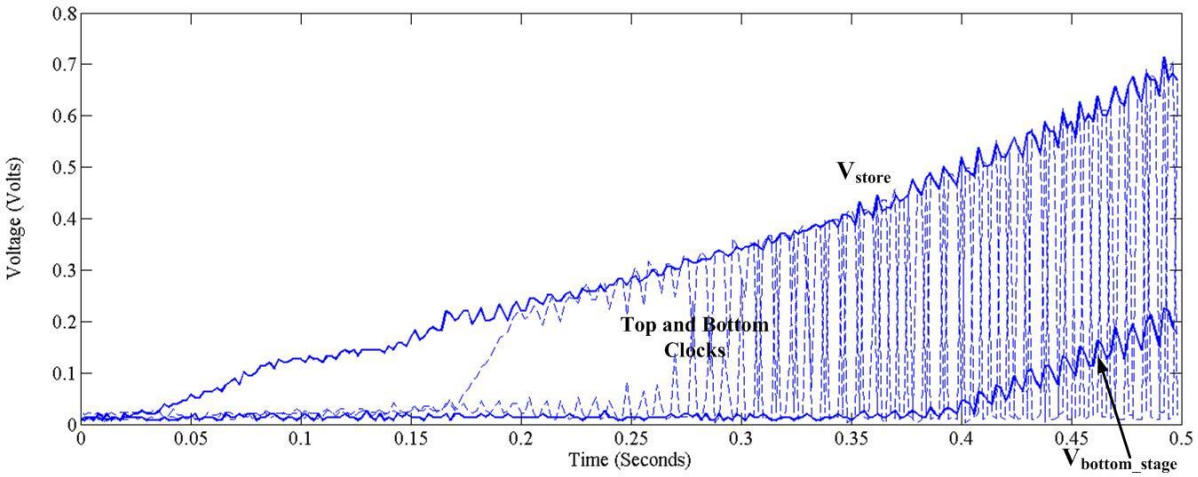

Figure 40. Measured results with an input sine-wave show V_{store}, the two clocks and the lowest voltage stage. Initially the clocks do not work, and the rectification is due the passive nature of the devices used as diodes. The voltage on the lowest voltage stage rises after the system has worked for 0.4 sec.

A separate system start-up is shown in Figure 41 with a 250 mV peak input (a lower voltage than Figure 40). Figure 41 shows the very initial start-up in stages 7, 6, 5, and 4 and shows this very initial start-up as V_{store} rises to 0.14 V over 1.6 seconds. In this portion of the start-up, the clocks controlling the active diodes are not working, so the voltage rises due to the passive nature of the devices in the top and bottom charge pumps. Even though the clocks controlling the active diodes are not working, the voltage on the active diodes is positive between V_{store} and ground. This means that the PMOS stages on the top stage will act as sub-threshold active diodes as just described in the last paragraph. In other words, more charge will flow in the PMOS when the input is positive because the input signal is at a higher voltage than the gates than if the input is negative. Similarly, on the negative charge pump on the bottom of the system, charge flows when the input is farthest away from positive voltage on the gate versus when the input is positive. Analyzing and describing the NMOS and PMOS stages on the top charge pump of the system during start-up will illustrate this concept.

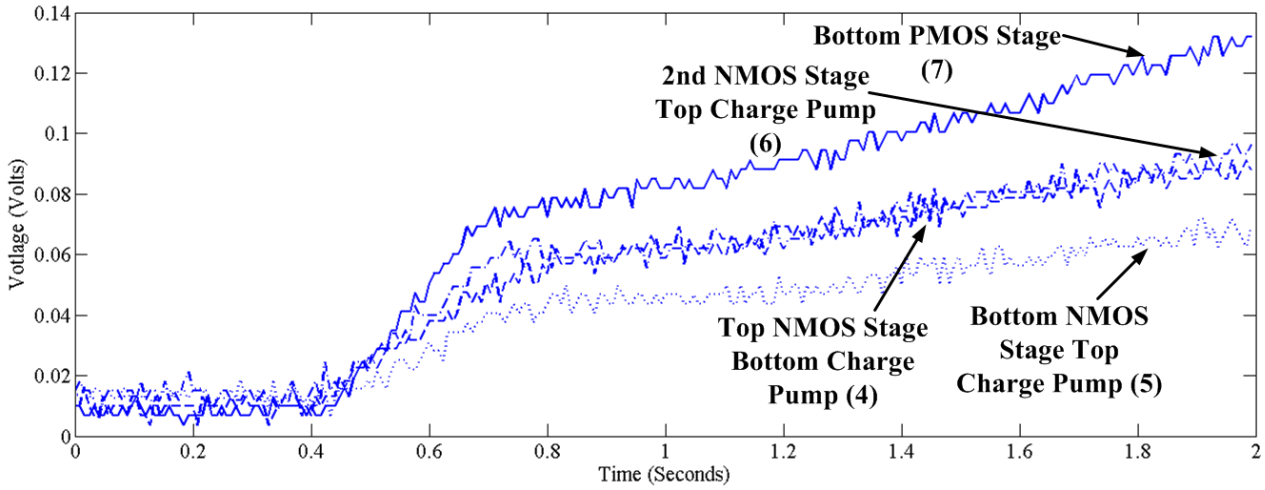

Figure 41. Measured results with an input sine-wave show the start-up voltages on stages 7 (Bottom PMOS Stage), 6 (2nd NMOS Stage Top Charge Pump), 4 (Top NMOS Stage Bottom Charge Pump), and 5 (Bottom NMOS Stage Top Charge Pump). Stage 7 shows a PMOS based stage that effectively charges well above stage 6. Stages 6 and 5 (NMOS based stages on the top charge pump) barely rise above stage 4 (NMOS based stages on the lowest charge pump).

Because there are NMOS stages on the top positive charge pump and the clocks are not functioning, there will be limitations in charging these stages as expected. The two NMOS stages on the bottom of the top charge pump do not function well during the initial start-up. Figure 41 shows this problematical functioning in the NMOS stages. In this figure, the voltage on stage 7 (Bottom PMOS Stage), the 2nd PMOS stage rises as expected. Also, the voltage on stage 4 (Bottom NMOS Stage Top Charge Pump) rises as expected. Figure 41 shows that the voltages on the two NMOS stages on the top charge pump (5 (2nd NMOS Stage Top Charge Pump), and 6 (Top NMOS Stage Bottom Charge Pump)) rise no higher than the NMOS stage 4. Likely, the NMOS stages do not decrease because of leakage from the top stages. Further improvement in start-up should occur using all PMOS stages on the top charge pump. Two NMOS stages were chosen to maximize efficiency once the system was started.

Once the charge pump becomes active, all stages begin to charge. A Cockcroft-Walton charge pump that both harvests and is clocked by its own input does not charge all stages at once. Instead, it works as series of cascaded voltage doublers as described in the Introduction

(Chapter 1.3). In this situation, the first stage charges, and this allows current to flow into the next stage and so forth. If all stages have similarly functioning diodes, it means that the stage closest to the input charges first, while the stage farthest away from the input charges last. As expected, this pattern holds true for the initial active diode sub-threshold start-up on the bottom negative charge pump. The lowest voltage stage charges last. Figure 42 shows V_{store}, and the output of the bottom 3 stages. Stages 3 (3rd lowest NMOS stages), 2 (2nd lowest NMOS stage), and 1 (lowest voltage stage) are shown. Stages 3 and 2 initially charge soon after V_{store} rises. The output of stage 1 (lowest voltage stage) stays low for nearly 0.7 seconds as voltage builds on the stages before the voltage on the lowest voltage stage begins to finally rise. As this begins, the voltage on the stages closest to the lowest voltage stage dip slightly. This is also observed in simulation. This dip occurs when the clocks begin to minimally function and charge in the 3rd and 2nd lowest voltage stage flows to the lowest voltage stage. In this start-up, it is shown that the comparator decision is based off of the lowest voltage stage that stays close to ground the entire time enabling high margin for sub-threshold functioning.

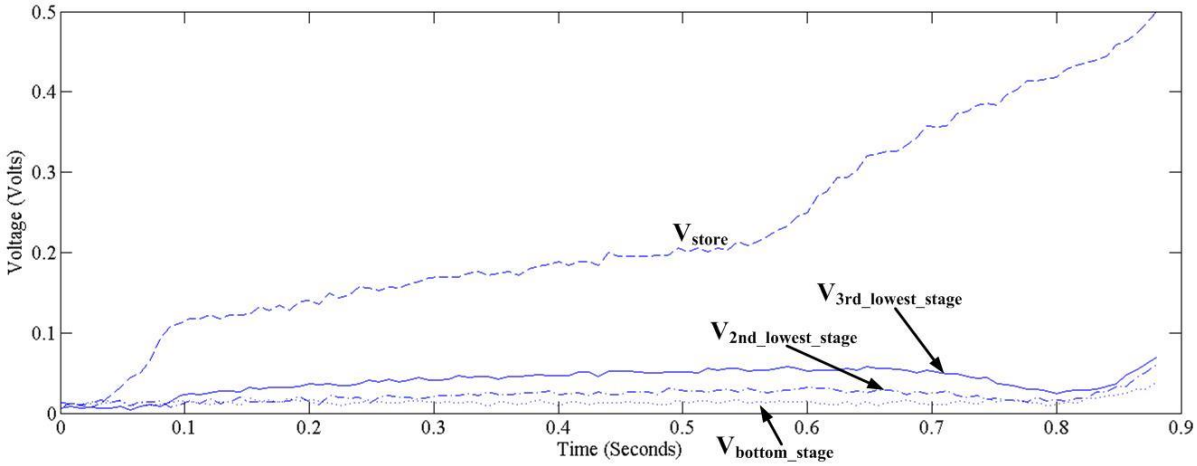

Figure 42. Measured results with an input sine-wave show V_{store}, and the voltage output on the bottom three lowest voltage stages on Figure 33. It is seen that the very lowest voltage stage charges last and stays near ground for a considerable period of time.

As described in the Introduction, initially, active sub-threshold functioning is barely effective. As described in Chapter 1.4.1, this is because of issues in sub-threshold mismatch and the slow speed of sub-threshold functioning. Specifically, the clocks do not switch close to where an ideal diode should turn on with the input; however some of the stage's voltages begin to rise due to the limited active diode functioning. As the voltage of the system starts to rise out of sub-threshold, the clocks become more accurate. The higher voltage on V_{Store} which is supplies the active diodes allows for faster turn-on of these active diodes because the comparators and inverters driving the active diodes are farther out of sub-threshold. Eventually, the voltage on the lowest voltage stage begins to rise, but for optimal start-up this will not occur until the system is out of sub-threshold. The low voltage on the inputs into the comparators on the lowest voltage stage allow high margin for initial start-up. Figure 43 shows V_{store}, the lowest voltage stage and input into the lowest voltage stage harvesting a sine-wave input from a harvester with a 350 mV peak value.

As seen in Figure 43, initially, for the first 1.3 seconds very little of the input signal is

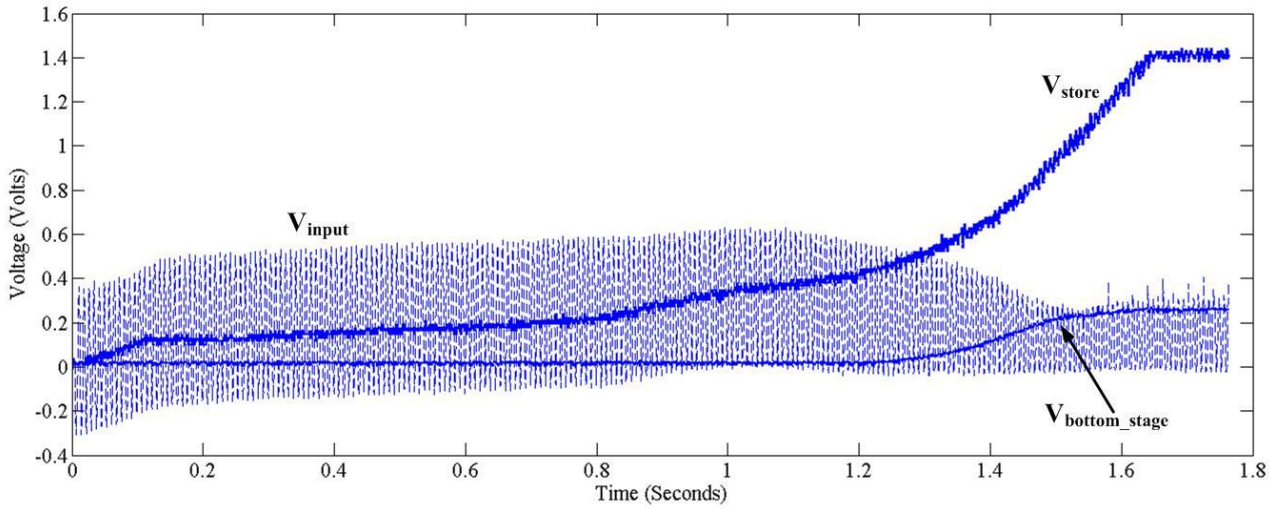

Figure 43. Measured results with an input sine-wave show V_{store}, the voltage on the lowest voltage stage and the input into the lowest voltage stage. Only once voltage on the lowest voltage stage rises, does the input at the lowest voltage stage lower, responding to the rising voltage on the lowest voltage stage.

harvested, so the input into the lowest voltage stage stays close to the original unloaded value. The nature of the charge pump allows the input signal to be transferred through the capacitors into the lowest voltage stage. As the clocks begin to function and V_{store} begins to rise, the input into the lowest voltage stage starts to decrease as more of the input signal is harvested. Essentially, as the charge pump's voltage starts to rise, the input impedance of the interface circuit decreases, and, correspondingly, the input signal also decreases. To understand this better, the harvester and interface circuit can be thought of as acting like a voltage divider as shown in Figure 44, where the input voltage seen by the harvester is given below.

$$V_{Peak-IC} = V_{Peak} \times \frac{R_{Effective-IC}}{R_{Effective-IC}+R_{Harvester}} \quad (14)$$

Initially, $R_{Effective-IC}$ is high as the charge pump begins to charge. As the charge pump continues to charge, $R_{Effective-IC}$ continues to drop. This, in turn, lowers the $V_{Peak-IC}$ into the interface circuit. Any harvester interface circuit will load its harvester. This loading is unavoidable. During sub-threshold operation this architecture limits this loading because the active diodes are not fully functional. This in turn limits the interface circuit loading during initial start-up. The output of the charge pump rises until the system is out of sub-threshold, and the DC voltage on the lowest voltage stage begins to rise. At this point, far more of the input into the lowest voltage stage is

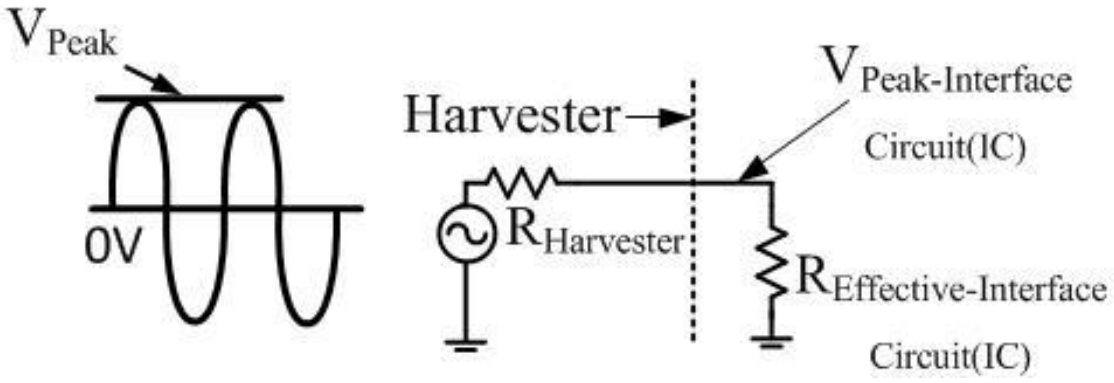

Figure 44. This shows harvester and interface circuit as a voltage divider to help better understand circuit characteristics.

harvested, and input on the lowest stage peak is the same value as the lowest voltage stage. Also, the input impedance of the harvesting interface circuit is lowered until the voltages are across the stages on the charge pump are similar.

Figure 45 shows the full start-up with V_{store}, V_{bias}, V_{store}, and the lowest voltage stage (labeled Vstage1). In this particular figure, a PFIG input with a 450 mV peak is harvested. As described earlier, V_{store} initially rises because the NMOS and PMOS devices act as diodes. After the comparators begin to work, the diodes become active near V_{store}=0.2 V. When V_{store} reaches 0.4 V, V_{bias} begins to rise. V_{bias} maintains a voltage one V_{th} below V_{store}. Also, at $V_{store}\approx$ 0.4 V the voltage on the lowest voltage stage begins to rise. When V_{store} reaches 1.5 V, the voltage on the large 100 µF capacitor at V_{out} begins to rise as the Mode Selector is enabled. The mode selector

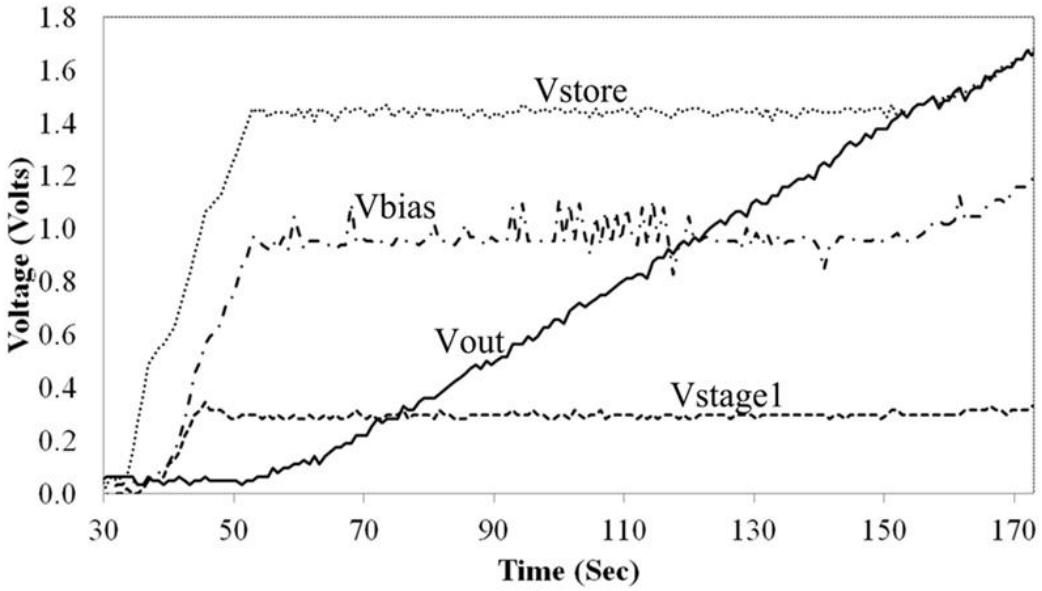

Figure 45. Measured results with an input PFIG show the start-up of the system with the lowest voltage stage (Vstage1), V_{bias}, V_{store}, and V_{out}. V_{bias} begins to rise once V_{store} is over ~400 mV. This figure shows that the large storage capacitor on V_{out} charges once V_{store} reaches 1.5 V.

[5] is necessary to prevent loading into a large storage capacitor or ultra-capacitor. A single capacitor is far more difficult to charge to a large voltage compared to a series of capacitors staked in series. This is seen in Figure 45 where the time it takes to charge a single capacitor

(V_{out}) to 1.5 V is several times longer than charging a series of 100 µF capacitors (V_{store}). This is because the stacked capacitors add in parallel when stacked in series reducing the overall capacitance the charge pump needs to charge to reach 1.5 V compared to a single large output capacitor.

It is important that the charge pump is loaded as little as possible during start-up to take full advantage of the reduction in capacitance due to the capacitors stacked in series (adding in parallel to reduce the total capacitance) in the negative and positive direction in the charge pump. Even the slightest loading on the output of the charge pump considerably increases the charge time. The goal is to charge the main charge pump quickly, so that the output (V_{store} which supplies the active system) charges as quickly as possible compared to the voltage increase on the lowest voltage stage.

With the mode selector preventing the significant loading on V_{store} from a large capacitor, V_{store} rises far more quickly than without the large capacitor directly attached. Without the mode selector the voltage on the lowest voltage stage rises before enough margin can be enabled to allow for sub-threshold functioning. In other words, V_{store} does not rise fast enough before the voltage on the lowest voltage stage begins to rise to bring the system out of sub-threshold where no additional margin is needed for functioning. Figure 46 shows a description of this behavior with a large 100 µF capacitor at V_{store}. Initially V_{store} rises; however, the voltage on the lowest voltage stage begins to immediately rise to about 50 mV after about 30 seconds. Even though this is a small change in voltage on the lowest voltage stage, it is enough to limit the margin in the active diodes. At this time, V_{store} starts to rise far more slowly compared to the initial start-up from 15 to 20 seconds and the voltage on the lowest voltage stage decreases slightly. At ~60 seconds, the voltage on the lowest voltage has decreased enough, so that V_{store} rises quickly

again. Just like at ~30 seconds, the voltage on the lowest voltage stage then increases. Finally, this prevents the system from charging, V_{store} levels off, and the system can no longer increase in voltage. It is important to note that it is difficult to compare this start-up time with the charge pump circuit seen on the bridge because this charges 100 µF capacitors, while the bridge based harvester is charging 10 µF.

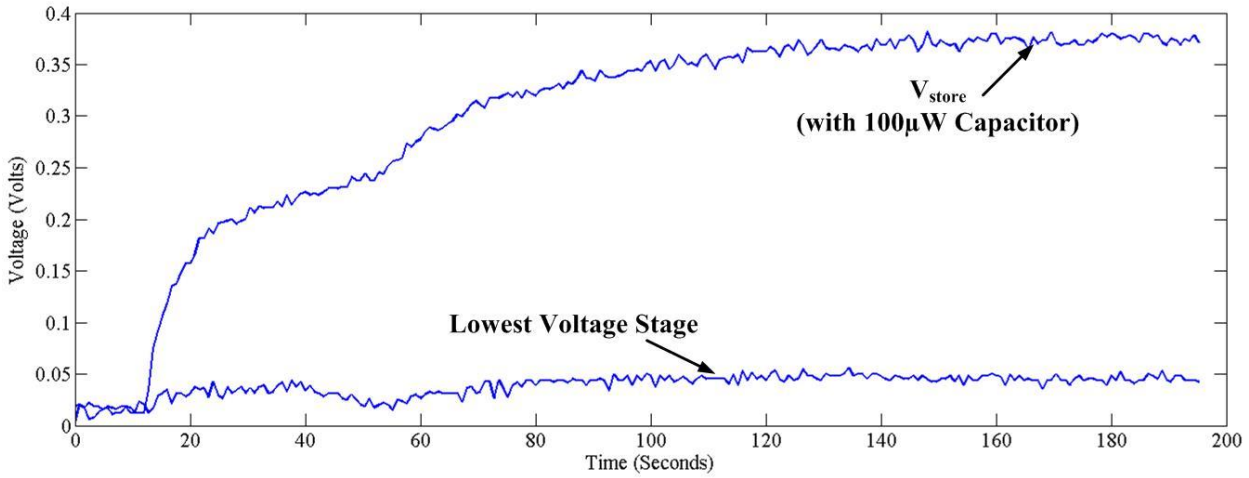

Figure 46. Measured results with an input sine-wave show the lowest voltage stage and V_{store} during a failed start-up.

The mode selector prevents loading from either a capacitor or resistor, so that the only loading on the system when charging is the low ~10-50 nA current needed to supply the mode selector at these low sub-threshold voltages. As described earlier in Section 1.3, the mode selector is adjustable to be able to allow the turn-on in a range of 0.8 - 1.5 V. This ability to change the turn-on level is of significant interest to understand sub-threshold functioning. For example, if the mode selector turns-on around 0.8 V, the system still remains in sub-threshold. However, if the system turns-on near 1.5 V, it is far out of sub-threshold. Figure 47 shows the problems that occur if the mode selector turns on near 0.8 V. The voltage at the output on the large capacitor V_{out} rises to approximately 0.26 V, and at this point the voltage on the lowest voltage stage has risen to nearly 0.1 V. This decreases the margin in the lowest voltage

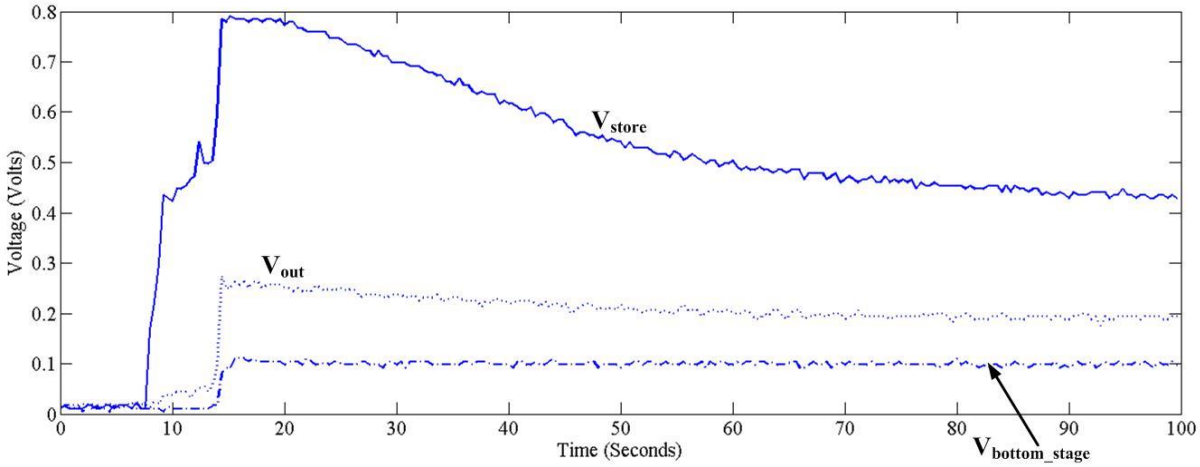

Figure 47. Measured results with an input sine-wave show start-up failure when the mode selector turns on at approximately 0.8 V. V_{store} rises to 0.8 V and the voltage on the lowest voltage stage (labeled "bottom stage") rises to ~0.1 V; however, at 0.8 V V_{out} rises as V_{store} remains constant. V_{store} stops charging as the voltage on the lowest voltage stage goes too high too quickly.

stage, and the system fails to function. When the failure happens, V_{store} decreases as the voltage supply is used to supply clocks that are barely working but whose operation consumes power.

Figure 48 shows the zoomed-in view of a start-up failure when the mode selector turns on at 0.8 V. This figure shows the behavior of the system just as V_{store} peaks near 0.8 V and the system begins to fail when the active diodes no longer function. In this close up the V_{out} only rises for about 1/20 of a second until V_{out} and V_{store} slowly begin to fall once the voltage on the lowest voltage stage begins to rise. At this zoomed-in portion of the start-up, the voltage on the lowest voltage stage also begins to rise, but this leads to less margin for the comparators driving the active diode clocks because V_{store} remains at 0.8 V and then slightly decreases. As the voltage on the lowest voltage stage rises, the comparators on the lowest voltage stage are given less margin to function and produce clocking outputs unsuitable to drive the active diodes. At the transition, V_{out} stops charging near about 260 mV. As this continues the clocks switching the active diodes become narrower and narrower and therefore less and less effective. At this point the harvested power is less than the power that the circuit consumes, so V_{store} begins to decrease. V_{store} then starts to decrease far more rapidly at this point as the voltage at the lowest voltage

stage rises and the system goes deeper and deeper into sub-threshold. This further puts pressure on the comparators at the lowest voltage stage that have less and less margin to function. Before V_{store} reaches 0.8 V, the active diode switching signal is wide enough for the active diode to turn on and allow a significant portion of the harvester's input signal to be harvested. However, once the voltage on the lowest voltage stage begins to rise, less margin is seen on the lowest voltage stage and the active diode pulses are far narrower. This means that very little power is harvested.

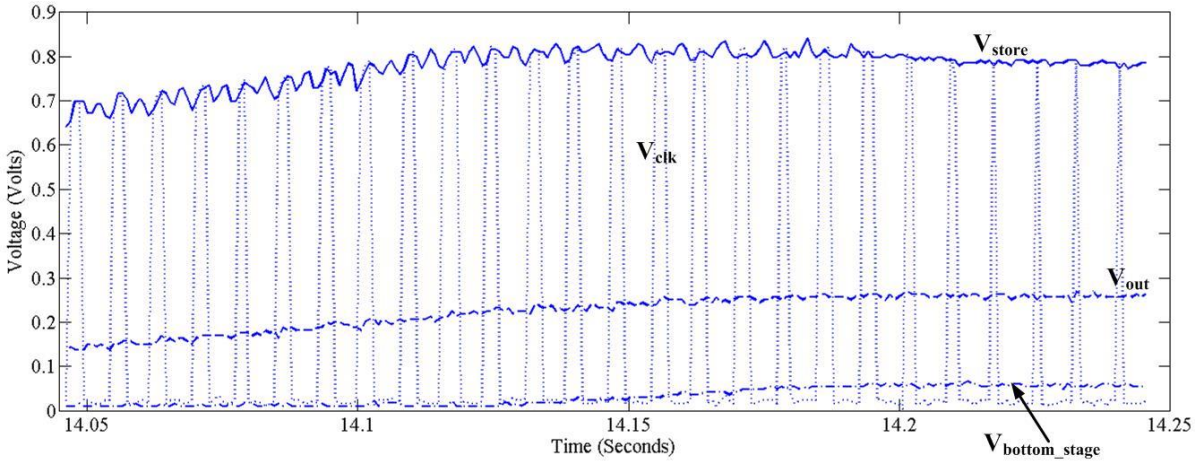

Figure 48. Measured results with an input sine-wave show that the clock pulses become much smaller once V_{store} reaches 0.8 V because the voltage on the lowest voltage stage (labeled "bottom stage") rises while V_{store} stays constant as it begins to charge V_{out}. This leads to a failure in the charging of V_{store}.

This analysis demonstrates that the weakest point during start-up is not the very initial start-up that can begin at ~110 mV rather; it is between 350 mV to 800 mV on V_{store}. The comparator is able to initially start-up around ~250 mV (the initial start-up is due to passive functioning). Near 350 mV to 800 mV the comparator can fail to function. As demonstrated in the figures 46 to 48 in this chapter, this is the point where the voltage on the lowest voltage stage begins to rise, limiting the margin for the comparators to function in sub-threshold. Figures 49 and 50 demonstrate how close the system is to active diode failure near 350 – 400 mV. Figure 49 shows the results of a failed start-up of the charge pump. Here, V_{store} is near 0.35 V and the

voltage on the lowest voltage stage is 50 mV. At this point, the clocks driving the active diodes barely function. They resemble more triangle waves that do not reach as high as V_{store}. These clocks are unable to drive the active diodes causing the voltage supply to decrease. This means that the power harvested is less than the power used by the active functioning of the circuit. In this situation, as V_{store} decreases, the clock functioning driving the active diode charge pump looks less and less like a clock and more low voltage triangle wave. Figure 50 shows a situation with a very similar voltage on V_{store} and the lowest voltage stage. V_{store} is slightly higher compared to Figure 49 (0.38 V vs. 0.35 V) and the lowest voltage stage is slightly lower compared to the situation in Figure 49 (0.035 vs. 0.045V). While not very much of a difference, these differences are enough to generate significantly improved signals clocking the active

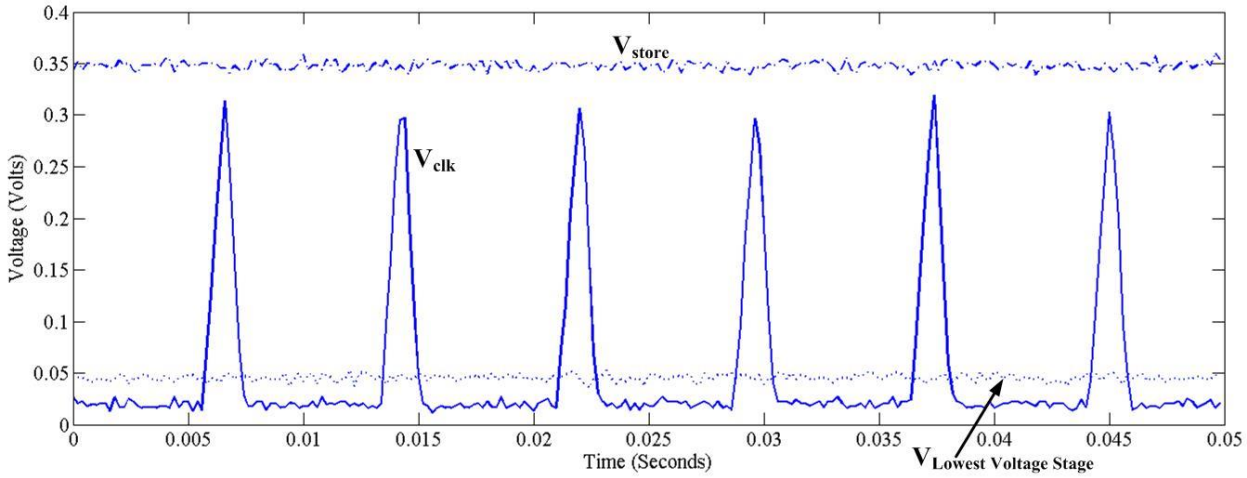

Figure 49. Measured results with an input sine-wave show the lowest voltage stage and V_{store} during a failed start-up that is zoomed in on a period where the clocking shows failed active diode sub-threshold operation.

diodes that look more like square waves because enough margin is available at the lowest voltage stage and the voltage on V_{store} is high enough. These two pictures were generated by putting in different input voltage into the system for start-up (for example, 200 versus 350 mV peak start-up). In the case of 200 mV, V_{store} just does not rise fast enough before the voltage on the lowest voltage begins to rise.

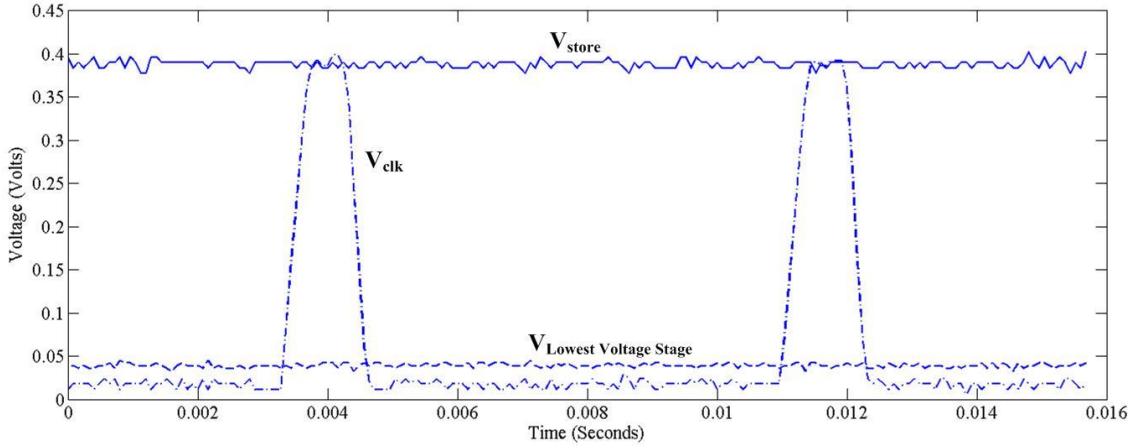

Figure 50. Measured results with an input sine-wave show the lowest voltage stage and V_{store} during a successful start-up that is zoomed in on a period, where the clocking shows successful sub-threshold operation.

Improvement in this mid-charging level between 350 mV to 800 mV could occur in several ways. First, PMOS devices could be used on the entire top positive charge pump to optimize passive diode operation. Part of the voltage increase is due to the diodes again acting like passive diodes during start-up, as described earlier in the section and chapter, so it will always be wise to optimize this passive functioning, even though it is not the main source of charging once the system is active. Second, sub-threshold biasing techniques to supply a bias that turns on before V_{th} could be used. Figure 45 shows that the bias voltage does not rise until the V_{store} reaches near 0.4 V. A bias voltage that could rise before V_{th} could potentially enable better sub-threshold functioning on the lowest voltage stage comparators. Third, keeping the lowest voltage stage low for a longer time by adding additional stages or using other methods might be a viable way to improve sub-threshold functioning by enabling high margin sub-threshold operation for longer time during start-up.

3.4 Steady State Hardware Analysis

Ideally, the voltage across all eight stages would be evenly distributed; however, this does not necessarily happen in steady stage operation. This is because the instance at which the

lowest voltage stage switches is close to ideal, but it is not necessarily the perfectly ideal time that the rest of the stages should switch. The switching is optimized for the lowest voltage stage, so as the system reaches steady-state, voltage tends to build up on this lowest voltage stage.

In steady state, the lowest voltage stage architecture does not optimize efficiency unless the system harvests very low power and the reduction in comparators of the system reduces enough active power. At higher harvester input power, driving all stages by the decision on the lowest voltage stage does not optimize the system though. This optimization will not occur because the system efficiency will always be best if charge is evenly distributed across the stages, and driving from the lowest voltage stage will not evenly distribute the charge across stages. One option is to put a single comparator on every active diode [3]. Other options are possible and these options will be explained and evaluated in the following paragraphs.

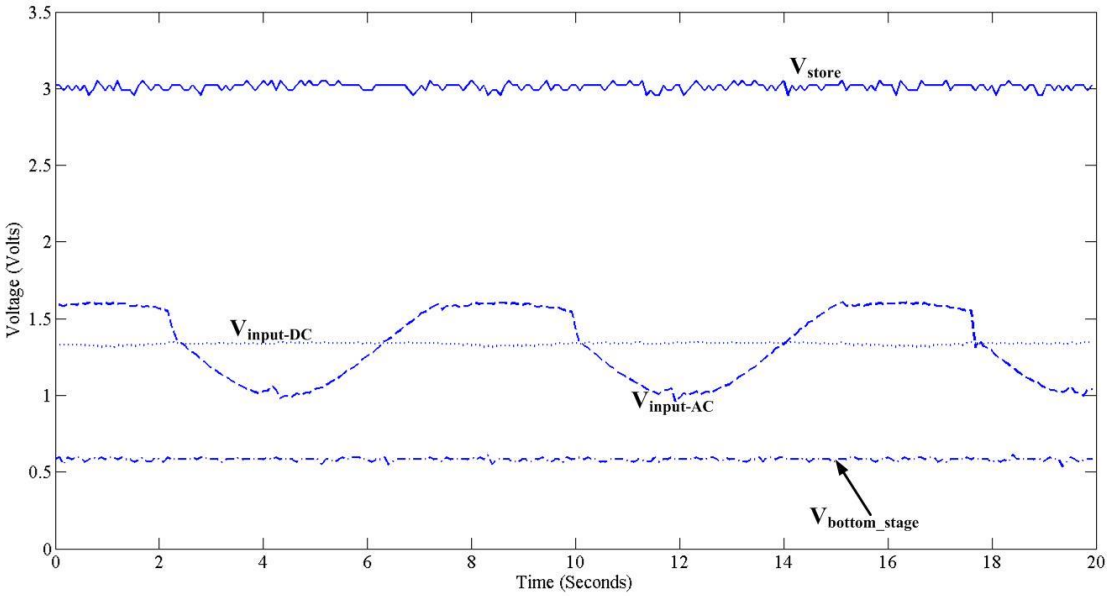

Figure 51. Measured results with an input sine-wave show the output (V_{store}=V_{out}), V_{stage}, and the bottom and top of the input. The input is 350 mV and the output is unloaded.

To initially illustrate uneven charging in the system, Figure 51 shows a steady state operation with the input near a 350 mV peak voltage. This steady state operation gives an

example of a situation where the charge distribution is not optimized across the stages. Shown in Figure 51, the lowest voltage stage, V_{store}, the top ($V_{input-AC}$) and bottom ($V_{input-AC}$) of the input into the charge pump. On the top and bottom of the input into the charge pump, the side of the harvester input that is referenced to ground through capacitors is nearly a DC value labeled "$V_{input-DC}$", while the other side of the charge pump represents an AC input that is loaded by the charge pump interface circuit labeled "$V_{input-AC}$". In Figure 51 the output is unloaded at ~3 V and the output of the lowest voltage stage is at ~0.6 V. In this example, the voltages are not optimized. The voltage on the lowest voltage stage should be multiplied by ×8 (since 8 stages), so the output should be near 4.8V. Also, the input voltage is not even raised to half of 3 V. $V_{input-DC}$ is near 1.3 V. Ideally, the input voltage should be between ground and the V_{store} (near ~1.5 V).

It is shown that to better optimization of the charge pump occurs by slightly lowering the voltage on the lowest voltage stage with a resistor. In the specific case of Figure 52, a 5 kΩ

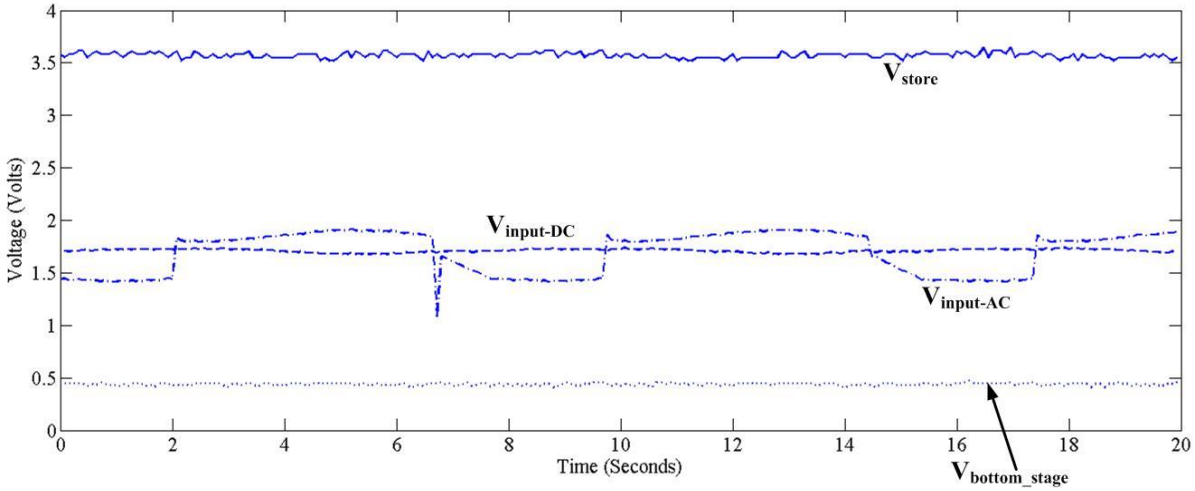

Figure 52. Measured results with an input sine-wave show the output (V_{store}=V_{out}), V_{stage}, and the bottom and top of the input. The input is 350 mV. The lowest voltage stage is loaded with a 5 kΩ resistor, so that the system is better optimized resulting in V_{store} rising to ~3.6 V from 3 V.

resistor was used. Some power is lost with this loading resistor; however, improved optimization occurs and far outweighs the loss of power through the resistor on the lowest voltage stage.

Figure 52 again shows the voltage on the lowest voltage stage, the voltage at the top and bottom of the input, and the output on V_{store}. In this case the voltage on the lowest voltage stage is 450 mV and the output voltage on is V_{store} ~3.6 V, which is approximately ×8 the lowest voltage stage value of 450 mV. Also, the top and bottom voltage of the input are centered near ~1.75V, which is approximately half of V_{store}. The system continues to remain optimized if the output of the charge pump is loaded. In Figure 53, the output of the charge pump is reduced by loading to the value of 2.8 V. As expected the voltage on the lowest voltage stage reduces to ~0.35 V, which is approximately one eighth of V_{store}. This is expected for an optimized system. Also, the input voltage is centered on ~1.5 V, which is closer to half of 2.8 V.

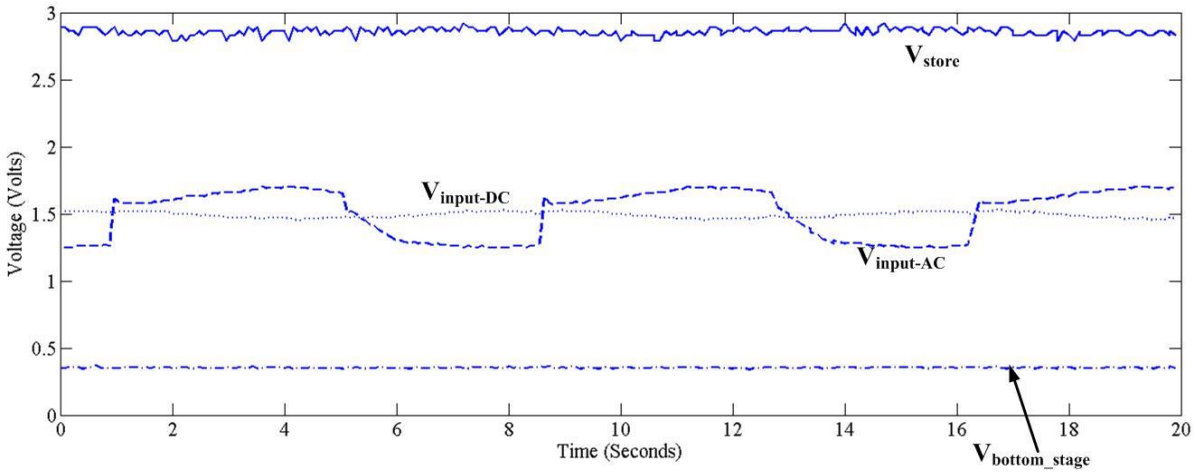

Figure 53. Measured results with an input sine-wave show the output (V_{store}=V_{out}), V_{stage1}, and the bottom and top of the input. The input is 350 mV. The lowest voltage stage is loaded with a 5 kΩ resistor and loaded at V_{store}. The voltage on the lowest voltage stage lowers to 0.325 V and the V_{store} is lowered to 2.8 V.

The AC signals, as shown in Figure 53, into the interface circuit look like square wave or a sine-wave with top "chopped". This behavior is expected and can be explained by again thinking of the interface between the harvester and the charge pump as a voltage divider like is seen Figure 54. When the active diodes are off, the interface circuit has a high input impedance, whereas when the active diodes are on, the interface circuit has a lower input impedance. This describes how the input signal seen by the interface signals changes or appears to be "chopped"

at a certain point in its functioning. This concept is further elaborated on in Figure 54 below. The point at which the voltage flattens out is the point at which the active diodes turn on, lowering the impedance seen by the harvester.

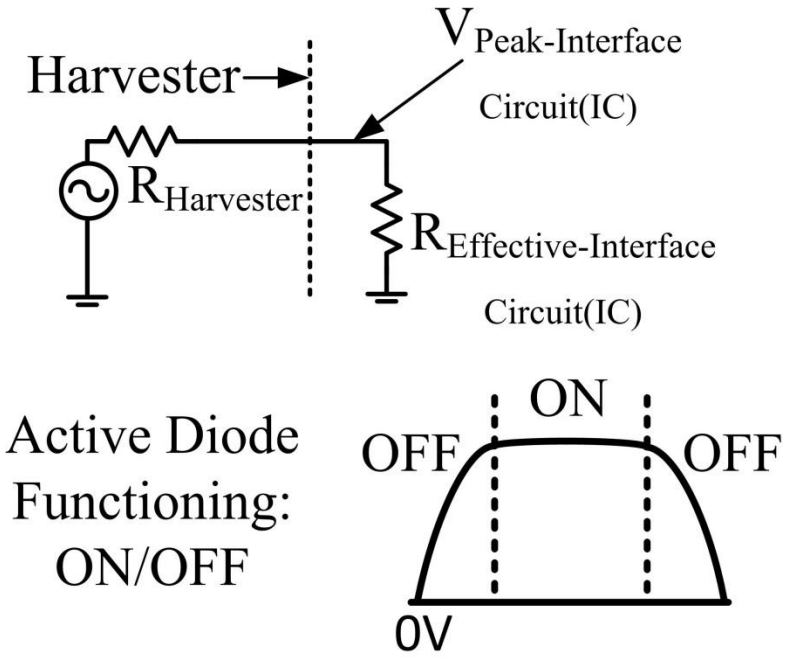

Figure 54. This shows the harvester and interface circuit as a voltage divider to help better understand circuit characteristics.

3.5 The IC with a PFIG input

The IC's functioning with a PFIG input is very similar to the functioning with an input sine-wave. As described in Chapter 2, a PFIG input into a harvester produces less efficient harvesting because the lower peaks of the harvester are not harvested as efficiently. An example of the PFIG signal used here is shown in Figure 55 below. In this picture the PFIG input is unloaded and the maximum peak has a value of 450 mV. The PFIG decays until the other FIG in the PFIG takes over abruptly ending the first FIG output signal.

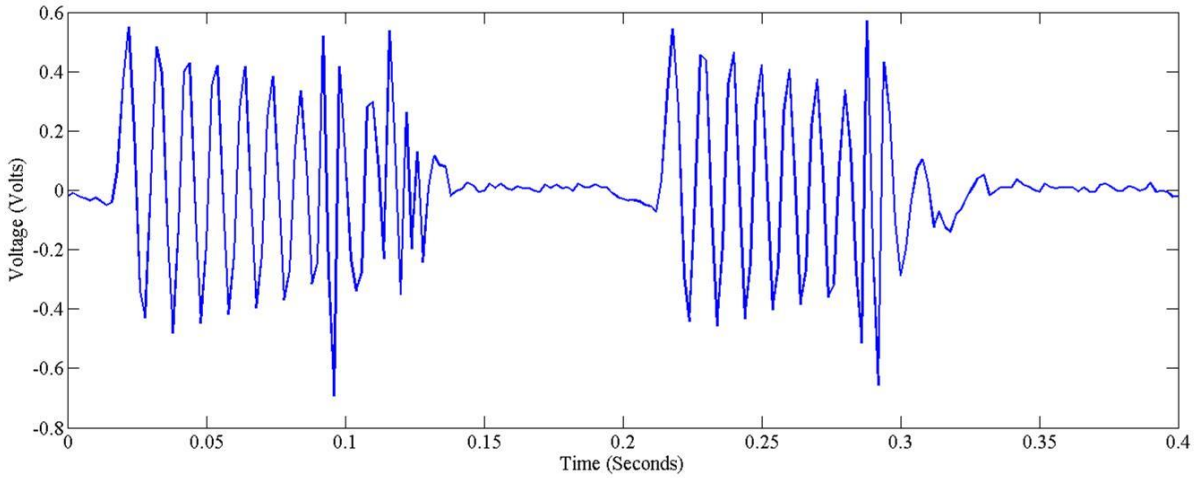

Figure 55. This shows the measured PFIG input used for these examples.

The PFIG based start-up is shown in Figure 56. Similar to the start-up with a sine-wave, the lowest voltage stays low while V_{store} rises. Both the input (V_{input}) and the input into the lowest voltage stage ($V_{input\_lowest\ voltage\ stage}$) tend to look like each other following the general shape and amplitude of the PFIG input. This makes sense as the input into the charge pump is really just the same signal transferred to the different stages of the charge pump with varying offsets

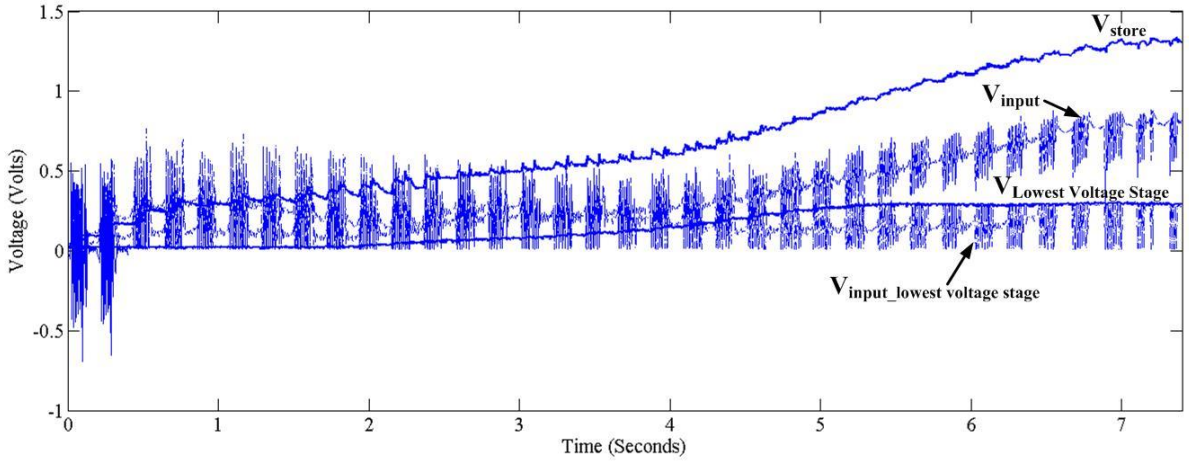

Figure 56. The measured PFIG input, AC input into the lowest voltage stage, the voltage on the lowest voltage stage and V_{store} are shown for a successful PFIG start-up. During the first 3 – 4 seconds, the voltage on V_{input} and $V_{input\_lowest\_voltage\_stage}$ are nearly the same.

corresponding to different voltages on the different stages of the charge pump. As the charging progresses V_{input} and $V_{input\_lowest\ voltage\ stage}$ move apart as the charge becomes distributed across the stages in the charge pump. Eventually, V_{input} moves to nearly the center between V_{store} and

ground similar to when a sine-wave is charging the system. Figure 57 shows a close up of the system stabilizing where V_{input} and $V_{input\_lowest\ voltage\ stage}$ move apart.

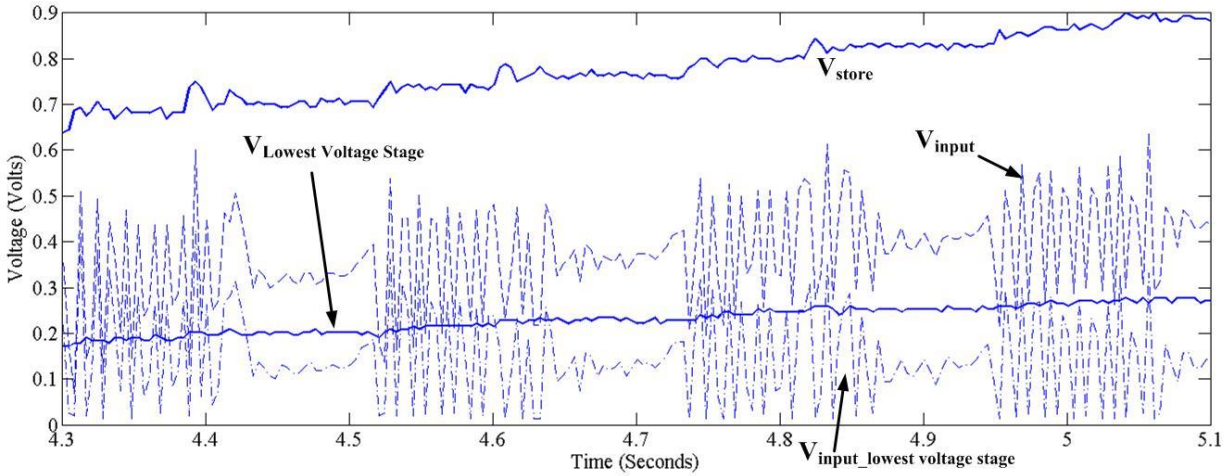

Figure 57. Measured results with an input PFIG show a zoomed in portion of the start-up showing the PFIG input, AC input into the lowest voltage stage, the voltage on the lowest voltage stage and V_{store} for a successful PFIG start-up.

Because of the decaying nature of the PFIG (Figure 55), the charge pump circuit system will respond differently to each peak in the decaying sine-wave. This is also seen in Figure 56. As the V_{store} and the voltage on the lowest voltage stage stabilize, many of the lower voltage peaks on the input (V_{input}) and the input transferred into the lowest voltage stage ($V_{input\_lowest\ voltage\ stage}$) do not occur. These lower voltage peaks are not harvestable by the circuit as it becomes more fully charged. For these lower voltages of the PFIG, the charged system basically acts as a very low valued impedance. Again, using the voltage divider analogy, this means that as the system being driven by the PFIG stabilizes the input impedance of the harvester system decreases to a level where some peaks of the PFIG are not harvested if they are not high enough.

This trend continues as the system reaches steady state. Figure 58 shows the V_{store}, the voltage on the lowest voltage stage, the input into the lowest voltage stage, and the input. It is seen here that basically only 1 or 2 peaks are harvested and appear on the input into the lowest voltage stage. With this input of the PFIG, the voltage on the lowest voltage stage rises to

0.35 V; however, V_{store} is only ~1.6 V. Since V_{store} should be ×8 the lowest voltage stage, this system is not optimized. Even at this low input of 0.35 V, only 1 or 2 peaks from the PFIG that are over 0.4 V are harvested in this system as they overcome the voltage on the lowest voltage stage. The rest of the peaks are not visible because the interface circuit acts as a very small resistance for the peaks that are not observed.

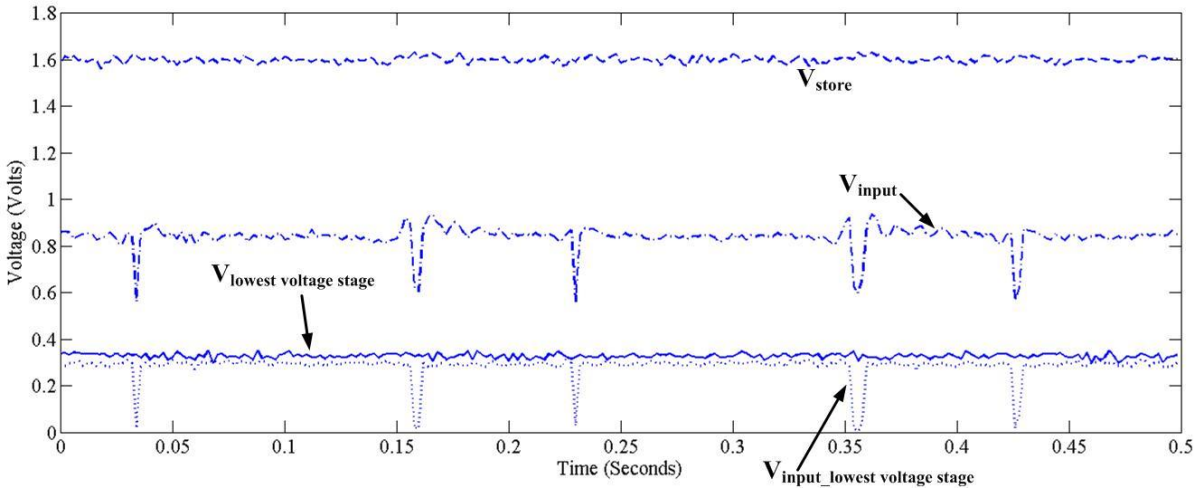

Figure 58. Measured results with an input PFIG show the PFIG input, AC input into the lowest voltage stage, the voltage on the lowest voltage stage and V_{store} for steady state operation. Only the highest peak from the PFIG is harvested by the system.

If the output of the system is loaded as in Figure 59, V_{store} decreases as expected and most of the PFIG peaks appear because they are harvested in the system with a reduced supply voltage V_{store}. In terms of the voltage divider analogy, a system with a reduced V_{store} and voltage on the lowest voltage stage will cause the input impedance of the interface circuit to be higher for more of the PFIG's peaks. With V_{store} pushed down, this also decreases the voltage on the lowest voltage stage. In this case 0.29 V is on the lowest voltage stage while V_{store} is 1.35 V, so this continues to not be optimized because the V_{store} should be ×8 the voltage on the lowest stage if the voltages are correctly multiplied through the system. As mentioned before in Figures 52 and 53, improvement can be done by loading the lowest voltage stage to slightly lower voltage so

more peaks are harvested. Figure 60 shows the results when the lowest voltage stage is loaded. The voltage in this figure is actually improved to 1.4 V with a lowest voltage stage of 0.25 V. Loading the lowest voltage stage does not always help with the PFIG. Hypothetically, if the loading on the lowest voltage stage is too low, it will reduce the overall efficiency of the system as more power is drained.

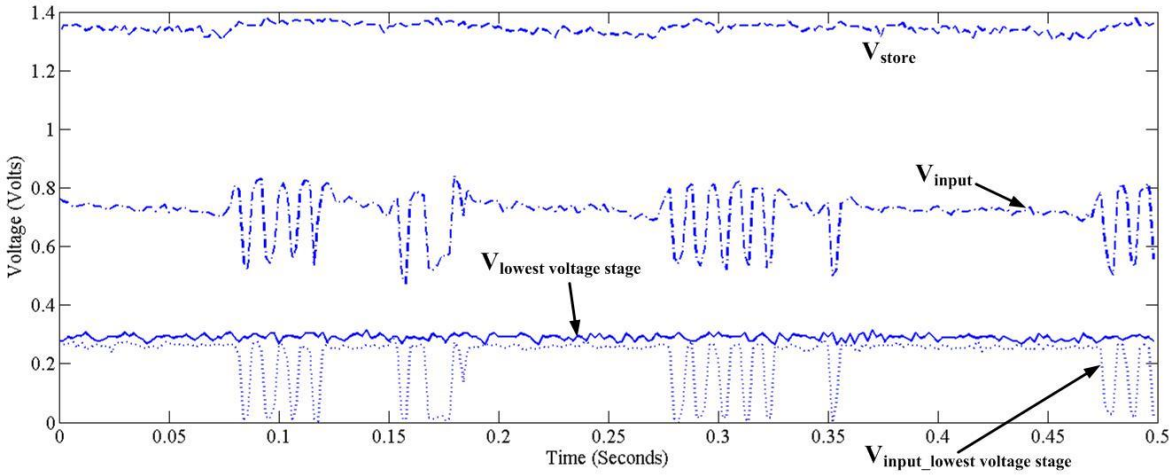

Figure 59. Measured results with an input PFIG show the PFIG input, AC input into the lowest voltage stage, the voltage on the lowest voltage stage, and V_{store} for steady state operation. The system is loaded so many of the PFIG peaks are harvested.

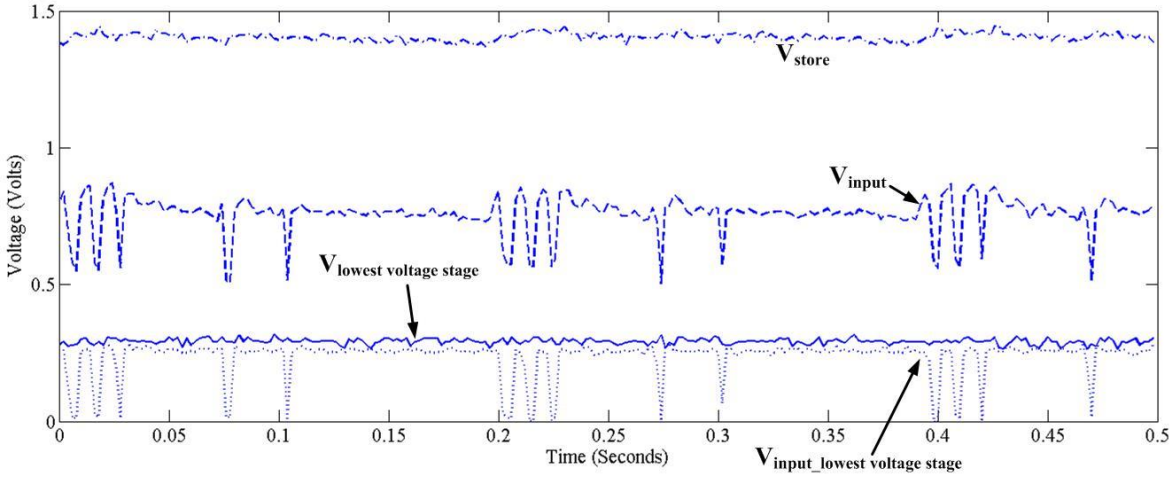

Figure 60. Measured results with an input PFIG show the PFIG input, AC input into the lowest voltage stage, the voltage on the lowest voltage stage, and V_{store} for steady state operation. The system is loaded so many of the PFIG peaks are harvested. The lowest voltage stage is also loaded. The main difference between this Figure and Figure 59 is the higher V_{store}.

While the interface circuit behaves similarly with a sine-wave input or a PFIG input, there is always the following question: what are the additional challenges associated with the start-up and functioning of this circuit when driven by the PFIG. Aside from the problems associated with the different peaks of the PFIG that have different peak voltages behaving differently when harvested by the circuit, the system must also function when the PFIG does not actuate over periods of time. For example, the bridge vibrations may actuate at very low frequencies causing the PFIG's decaying sinusoid to completely decay out, or the PFIG may not actuate at all for several seconds because there are no vehicles coming over the bridge.

Figure 57, for instance, shows the middle of start-up with a PFIG. The major issue observed is that V_{store} and other voltages slightly decrease during the periods with no PFIG actuation because power is consumed in the circuit and no power is harvested. Due to these periods without harvestable inputs, that a system charging with the PFIG will charge slower than if the input into the system is constant because power will still be consumed when the system is not harvesting PFIG inputs. In severe cases when the PFIG input is random as seen on a bridge or the PFIG is actuated at a very low frequency (i.e. 1Hz), a system that would start-up with a sine-wave may not be able to start-up with a PFIG when both cases have similar maximum peak voltages.

3.6 Results Summary and Comparison of the 16x Charge Pump Design

The 2nd IC arrived for evaluation at the end of August 2013. Initial evaluation was successful showing functioning with the PFIG similar to what was predicted in simulation. Start-up with PFIG input with a 450 mV peak sinusoid occurring at 5 Hz is shown in Figure 45. The signals shown in this figure (45) are before and after the mode selector "V_{Store}" and "V_{Out}" respectively. Also, the voltage on the lowest voltage stage is shown along with the bias signal

V_{biasP}. All data was taken through low current input buffers consuming <10nA of current. Table 7 includes the data for this 16x charge pump, demonstrating its ability to start-up while boosting with low input voltages, low power functioning, power consumption, and circuit efficiency. Table 7 shows a list of power harvester circuits and comparisons between this ×16 boosting harvester and other works.

Table 7. Shows the comparison of this ×16 charge pump versus other major works from literature. Peak voltages are reported as defined in Section 1.5. Values are assumed to be for a sine-wave unless indicated with a "PFIG".

Works capable of boosting from a harvester	**×6 Charge Pump Chapter 3 IC 2012***	**×16 Charge Pump Chapter 4 IC 2013***	**[8] McCullagh Chapter 2**	**[9] Kwon**	**[10] Arnold**	**[3] Arnold**	**[2] Szarka**	**[11] Rahimi**
Technology	180 nm & Discrete	180 nm & Discrete	Passive Discrete	2µm BiCMOS & Discrete	Active Discrete	Active Discrete	Active Discrete	Active Discrete
Max Boosting	×6	×16	×60	~×4	×12	×8	×14	×15 due to 1:15 transformer
Boosting Method	Charge Pump	Charge Pump	Transformer Charge/ Pump	Inductor	Rectifier /Inductor	Charge Pump	Inductor/ Charge Pump	Transformer Charge/ Pump/ Rectifier
Circuit Power Consumption	~0.6 µW	~0.6 µW	0 µW	estimate ~0.25 µW	Not given	6.4 µW	~21µW	Estimate ~1 µW
Min Start-up Voltage	280 mV	220 mV 415 PFIG	60 mV	Pre-charge required	1.25 V or Pre-charge for 5 mV	500mV	~500mV	200 mV
Min Functional Voltage	138 mV	110 mV	60 mV	350 mV	~5mV	350 mV	~500mV	200 mV
Max Circuit Efficiency	69% SW	66% 50% PFIG	27%	49.9%	84%	82%	76%	35%

*Journal papers in preparation by McCullagh

With the use of active diodes being driven by the lowest voltage stage and the use of a mode selector to prevent loading during start-up, the system cold-starts with a minimum decaying sinusoid PFIG output with peak values of 415 mV occurring at 4.5 Hz with average power of ~9 µW. For a similar decaying sinusoid with a peak of ~450 mV at 3 Hz with 7.6 µW PFIG output power, the circuit efficiency is ~50%. With an ideal sine-wave, the system is able to cold-start with an input with a peak of 220 mV at 110 Hz and power of ~30 µW. Under these

conditions the circuit efficiency is 66% for a DC output of 1.7 V. The circuit remains functioning for decaying sinusoids at frequencies as low at 1 Hz. This ultra-low power operation is possible due to the use of two comparators. The IC chip is fabricated in 180 nm CMOS on a 1.2 mm^2 die.

3.7 Model to Hardware Discrepancies

There are significant model to hardware discrepancies in the start-up for this design covered in Chapter 3. The main issue is that hardware's minimum start-up was over 100 mV lower than simulated start-up that gave a minimum result of 335 mV. Hardware based start-up worked with peak inputs as low as 220 mV. Also, the group of different ICs tested in hardware produced a wide range of minimum peak start-up voltages with a sine-wave. Some devices minimum start-up was near 330 mV, which is very close to what is predicted by simulations; however, as just mentioned, some devices were able to start-up with an input signal as low as 220 mV, while some devices needed an input signal greater than 400 mV for start-up. Extreme care was taken before testing the system's start-up to make sure all nodes were at ground, and there was no charge left over in the capacitors. To accomplish this, every input point on the IC was discharged to ground, the voltages were checked on the circuit to make sure they remained at ground, and if any voltages were still not at ground, all points on the circuit were discharged to ground once more.

Another major concern encountered in simulation is that decreasing the output impedance of the harvester, which will increase the power generated by the harvester in simulation, has

virtually no effect on the minimum start-up. These points towards a sub-threshold modeling problem in the sense that more input power should have a greater likelihood of active functioning and a greater ability to start-up at lower voltages. Also, hardware results point to better start-up performance with a higher power harvester input.

3.7.1 Start-up measurement methods

To test this circuit, a sine-wave was needed that was not referenced to ground. The output of a regular single ended function generator will always be referenced to ground. The voltage of the harvester input signal needs to rise, as is required by the nature of the interface circuit. Multiple ways exist to provide such a signal. The first and most obvious way is to test with a harvester, and this, of course, is done with the PFIG. However, often the circuit needs to be tested under more ideal circumstances in order to be compared to other energy harvesting circuits in literature. Also, an ideal input sine-wave will allow additional learning that a PFIG input, for example, might not allow. The effect of an ideal sine-wave input versus a PFIG input that will not regularly actuate is a specific example of what should be studied with an ideal sine-wave. Two ways exist to test with a differential input other than using an actual harvester. A differential sine-wave generator can be used, but these are expensive and were not available to the author. The method used by the author is a transformer attached to a function generator. As long as the input impedance is properly measured to obtain accurate input power into the interface, this is a viable method. There is a small possibility that charge might be trapped in the transformer; however, results have been repeated for specific devices. For instance, one IC as part of an IC based system will start-up at 220 mV regularly, while another IC will regularly start-up at 330 mV.

3.7.2 Simulated Mismatch and Process

Investigations were needed to further understand and quantify the model-to-hardware differences. Monte Carlo simulations can be run in the Cadence schematic to assess how mismatch between devices in a design affect the design's performance. For example, devices are designed to have specific parameters, but they may not because of edge effects, material imperfections, etc. Start-up was run in Monte Carlo to test how mismatch variation affected start-up. The results are shown in Figure 61 over 10 runs at 330 mV. It is seen that only one of the 10 cases started with an input at 330 mV, while start-up is always possible with an input at 335 mV. With inputs any lower than 330 mV, start-up is never possible in any type of simulation. This would seem to eliminate simulated mismatch as a possible reason for the extreme variation in measured performance. Process was also run including fastfast, slowslow, and typical process corners, and no improvement in minimum start-up was observed in simulation.

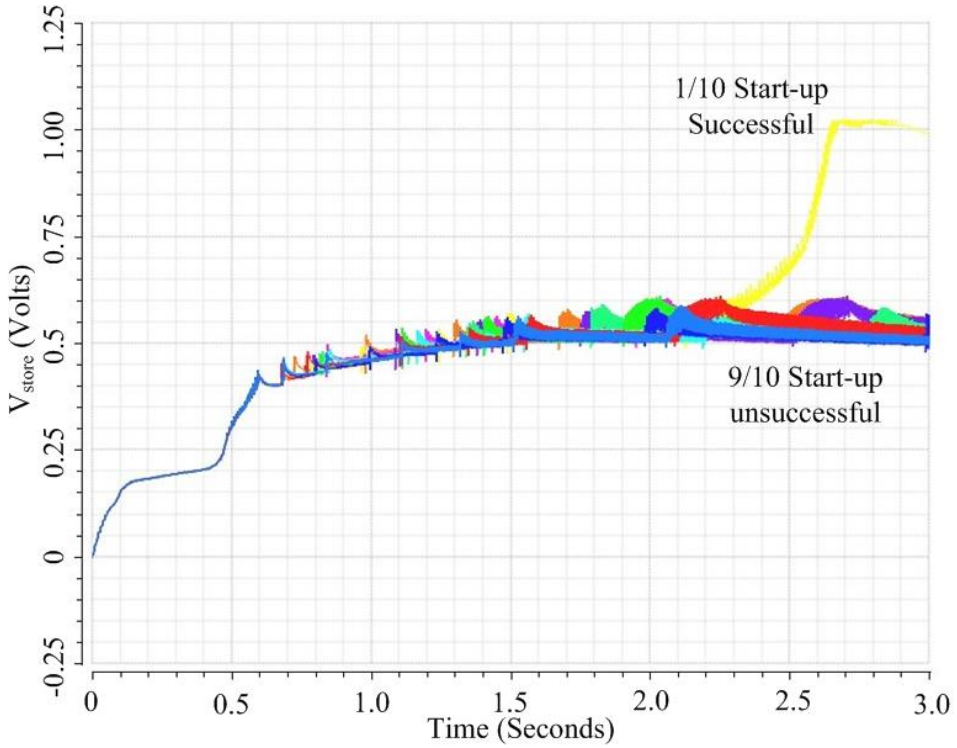

Figure 61. Simulated start-up for Monte Carlo mismatch was done with a peak sine-wave input at 330 mV. Only one case out of ten can start-up.

3.7.3 The Effect of ESD Diodes on Start-up

Limited electrostatic discharge protection (ESD) was added to the circuit (Figure 62) to

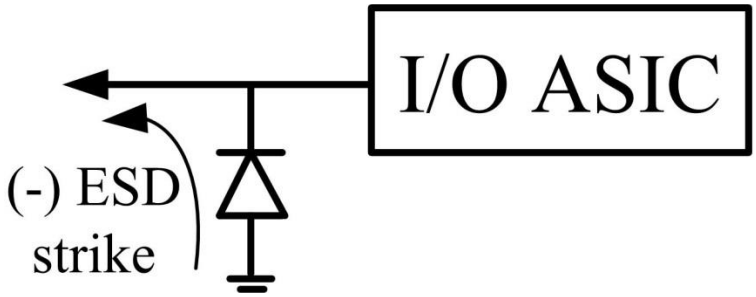

Figure 62. An ESD diode to ground is shown similar to what was used in this design is shown.

minimize the effect of a possible ESD event. This consisted of a diode connected to the input

pads. These ESD diodes actually improve the performance of this circuit, because a small amount of the input signal actually goes through ground up through the diode to the various nodes of the design. Figure 63 shows the difference (from schematic) between performance with and without the ESD diodes. With ESD diodes minimum start-up is 335 mV; however, without ESD diodes minimum start-up is 350 mV. Figure 63 shows simulated results with and without the ESD diodes at an input voltage of 335 mV. This figure shows that ESD diodes are needed to obtain start-up in simulation at 335 mV (without ESD diodes, start-up is only possible at 350 mV). Extracted start-up was run with the ESD diodes, and no difference was seen compared to simulated start-up that was simply run in schematic (with ESD diodes attached). This would indicate that ESD diodes can improve the performance of the system, but it again does not fully explain the model to hardware discrepancies. As just mentioned, some sub-threshold leakage through the ground path and ESD diodes of the system improves performance. Similar passive diode based improvements might be obtained by adding additional passive diodes to increase the sub-threshold current along the charge pump architecture itself instead of relying solely on the passive diode nature of the devices in the system. This idea has been used before in active diode sub-threshold designs [12].

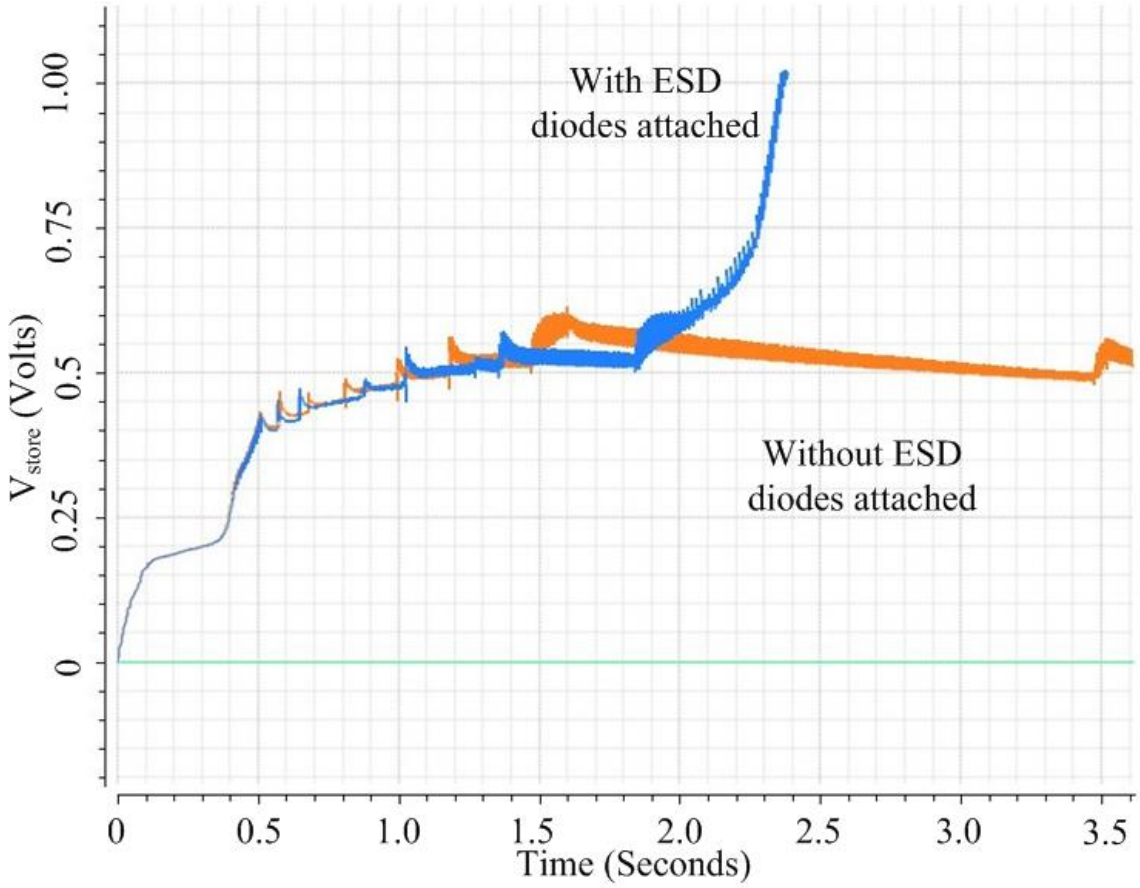

Figure 63. The difference between simulated start-up with and without ESD diodes with a peak input of 335 mV is shown. The system starts-up with the ESD diodes at this low input voltage but does not start-up without the ESD diodes.

Because simulation cannot resolve the low voltage discrepancies between model and hardware, it points to significant problems in the basic models of the system in deep sub-threshold. This is further emphasized by the fact that simulated minimum start-up does not change with dramatically reduced or increased power. In extreme cases (such as milliWatt or Watt inputs), simulated start-up is the same for an input signal with microwatts of power versus high milliWatts of power. Likely, the simulated deep sub-threshold functioning of the devices is not modeled correctly or the effect of some type of mismatch property is not modeled effectively in deep sub-threshold. Because the average start-up between devices is reasonably close to what was predicted by simulation, a process or mismatch variation likely is not modeled fully for deep sub-threshold. To further narrow down possible causes of the modeling discrepancies, additional

measurements were taken over temperature as well measurements taken while externally controlling the circuit's bias voltage. The goal of these measurements was to show extreme sensitivity to a characteristic (i.e. temperature or bias voltage) of the circuit.

This chapter describes a ×16 IC-based charge pump structure capable of sub-threshold active diode start-up and high efficiency operation with a harvester input. The PFIG harvester was used with this circuit design producing 50% efficiency with a low power signal (<10 µW). Additionally, a PFIG signal down to 415 mV was able to start-up the system. An ideal sine-wave generated by a transformer was able to show start-up down to 220 mV. The system uses a method relying on the comparator decision on the lowest voltage stage of the charge pump. The lowest voltage stage charges last due to the characteristics of a Cockcroft-Walton charge pump. Because the lowest voltage stage charges last, this enables additional margin in the sub-threshold active diode start-up. Other architectures and circuit mechanisms are possible where a comparator decision on the lowest voltage stage drives the decision on all stages of the charge pump to enable sub-threshold start-up. The next chapter describes such a mechanism where the choices of devices used in the full-wave active charge pump allow the lowest voltage stage to stay low.

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Chapter IV

A ×6 Boosting Active Diode Charge Pump IC-Based System and Related Comparator and Charge Pump Loading Methodologies

Other circuit methods are possible to allow an active diode charge pump to operate in deep sub-threshold using an architecture where all stages in the charge pump are driven by a comparator on one stage. As in Chapter 3, the goal is that this stage with a comparator is charged last, so that additional margin is available in deep sub-threshold functioning for the comparator operation. Chapter 3 shows an IC-based ×16 full-wave charge pump design that relies on the lowest voltage stage to give additional margin to aid in deep sub-threshold active diode start-up. In Chapter 3, the lowest voltage stage is charged last because it is farthest away from the harvester input into the charge pump. This chapter describes another lowest voltage stage driven active diode charge pump that is a ×6 boosting design; however, the method to hold the lowest voltage stage low is different in this design versus the design in chapter 3. The choice of the active diode device (either NMOS or PMOS) allows the lowest voltage to stay low and gives the comparator on the lowest voltage stage additional margin. This different ×6 IC-based full-wave charge pump design is explained in depth in the chapter.

4.1 IC-Based×6 Charge Pump Circuit

4.1.1 Motivation for a ×6 Charge Pump Circuit Design

The goals of these 180 nm CMOS IC-based systems are to achieve a cold-start and function with high power conversion efficiency in regular operation without the need for transformers. Chapter 3 described a system that uses "lowest voltage stage comparators" to enable active functioning for start-up in deep sub-threshold in a ×16 full wave active diode charge pump. This chapter (4) provides a similar design relying on the lowest voltage functioning using a ×6 full wave active diode charge pump. In Chapter 4 the method for maintaining a low voltage on the lowest voltage stage is different than in Chapter 3, and this difference related to the specific devices chosen in the charge pump stages is analyzed.

Both the ×16 and ×6 designs in Chapters 3 and 4 use an IC-based system where the lowest voltage stages charges last, so that high margin on the lowest voltage stage can be used to drive the rest of the stages through inverters based off of the lowest voltage stage's comparison in deep sub-threshold. Also, in both designs, as the system reaches steady state, the lowest voltage stage finally charges and this optimizes the system for higher efficiency operation. In Chapter 3, a ×16 full wave rectifier design with two Cockcroft-Walton multipliers going in the positive and negative direction are used, and the lowest voltage stage is the last stage on the negative charge pump. In this chapter (4) a full-wave charge pump is used; however, it only charges in the positive direction using a string of six rectifiers where each stage only multiplies the voltage by ×1. This means that the maximum theoretical voltage boosting in this IC-based design is ×6 rather than ×16. While this is a decrease in performance, it is the method for holding the lowest voltage stage low during initial start-up and is different than the circuit described in Chapter 3. In Chapter 3, the lowest voltage stage charges last because it is farthest away from the

input, so the system in Chapter 3 uses the inherent properties of a Cockcroft-Walton charge pump to keep the lowest voltage stage low for as long as possible to enable high margin for active deep sub-threshold start-up. In this chapter (4), the charge pump only charges in the positive direction, so the voltage in the charge pump should have built up on the lowest voltage stage first. It doesn't because of the type of devices used on the lower voltages stages (NMOS devices are used) versus the devices used on the higher voltage stages (PMOS devices are used) of this design.

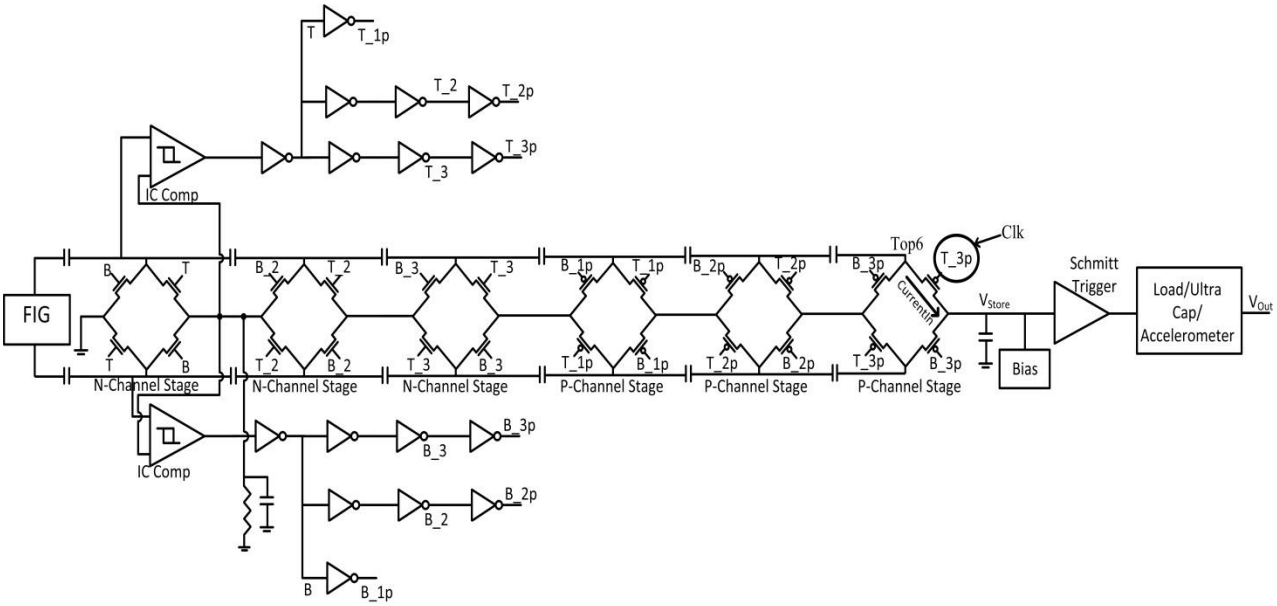

Figure 64. This shows the initial IC based harvester system containing 6 stages (3 NMOS and 3 PMOS), two comparators driving all stages, a bias circuit and a Schmitt trigger.

4.1.2 Charge Pump Circuit Design

The ×6 full-wave architecture is shown in Figure 64. This IC-based harvester system contains 6 stages (3 NMOS and 3 PMOS) and is capable of ×6 boosting. PMOS stages are used on the top stages because the system is supplied by the output of the charge pump. For example, if NMOS devices were used on the top stages, they would not be able to turn-on since the gate would be no higher than the source. A bias circuit is attached to the charge pump output and is

used for the comparators. The bias voltage turns on once the circuit achieves a specific voltage near the threshold level (V_{th} ~ 0.42 V) of a NMOS or PMOS device in this technology (180 nm). A Schmitt trigger is attached at the output of the charge pump. The goal of both discrete or IC based Schmitt triggers is to allow charge into a storage capacitor once the charge pump's output exceeds a specific turn-on voltage. This active diode charge pump was taped out in 180 nm CMOS. The die size was about 1mm x 1mm; however, the actual size of the circuits is about 300 × 150 µm. The die with the specific active diode structure highlighted is seen in Figure 65.

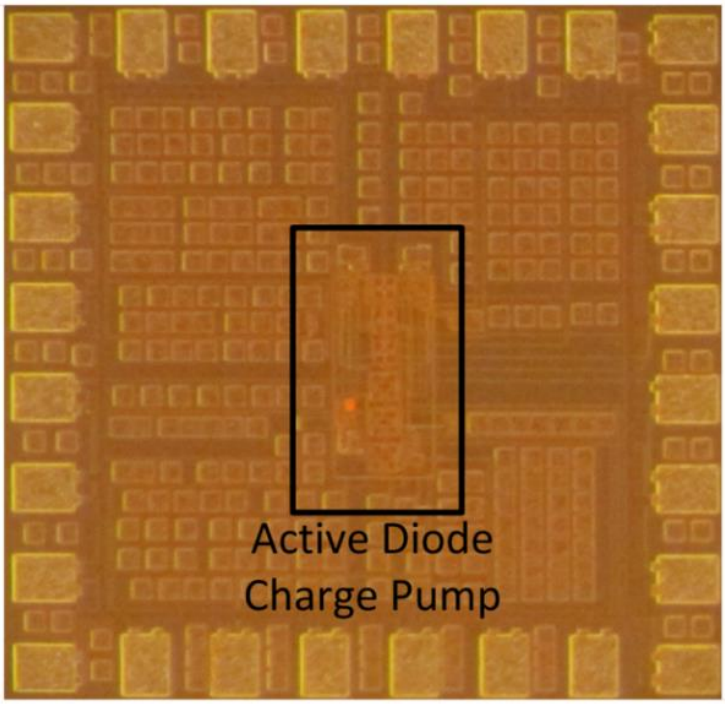

Figure 65. This shows the initial charge pump design fabricated in 180nm CMOS technology. The active diode portion is surrounded by a rectangle.

As in the ×16 IC-based charge pump design, a differential common gate comparator is used on the first stage of the charge pump (Figure 66), and this first comparison drives the rest of the stages through buffers. This comparator is ideal because it can make low input amplitude comparisons without the need for sub-threshold operation as long as V_{store} is high enough to keep

the comparator out of sub-threshold functioning. If the comparator's V_{store} is too low for regular operation and the bias voltage into the comparator is also low, this comparator still works in sub-threshold as long as the first stage voltage of the charge pump also stays close to ground. Similar comparator designs have been used in other energy harvesting applications [1, 2]; however, these applications do not make use of the comparator's ability to function with low input voltages in and out of sub-threshold design. The Schmitt trigger was either made from an IC based design that turned on near 0.4 V (Figure 79) and was not adjustable or a discrete Schmitt trigger that could be designed to have a turn-on near 1.0 V (Figure 78). This Schmitt trigger (or Mode Selector from Chapter 3) is a critical component of this system. Preventing loading on the charge pump is essential for an optimal start-up. The various designs used for this Schmitt trigger will be discussed later in this chapter in Section 4.3.

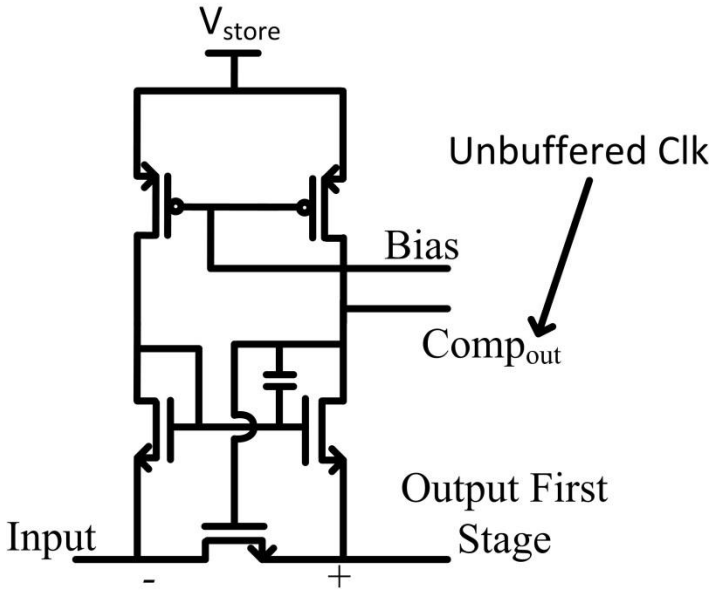

Figure 66. This shows a differential common gate comparator regularly used in energy harvesting literature [1, 2]. The (+) input is the output of the first stage of the charge pump.

4.1.3 Innovations in this charge pump design

There are multiple areas of innovation in this active diode charge pump that advance the state-of-the-art. 1) Unlike most other energy harvesting charge pump designs or rectifier designs [2-5], charging occurs without a capacitive or resistive load. Charging without loading improves start-up by improving the biasing of the lowest voltage stage comparators allowing their inputs to stay low (discussed later in Section 4.2). Unlike in Chapter 3 where the input of the lowest voltage stage stays low due to the inherent nature of the Cockcroft-Walton charging, the lowest voltage stage stays low here because of the choice of NMOS devices in the lowest voltage stage rather than PMOS devices. 2) A classic differential common gate comparator is used in a novel fashion to enable low voltage functioning in and out of sub-threshold in a multiple stage charge pump architecture. This comparator allows low voltage comparisons and operation making the need for passive diodes unnecessary for most of the charge pump's start-up. 3) A lowest voltage stage driven charge pump structure is used to further aid start-up and create an ultra-low power design capable of actively working with the low power outputs of the PFIG on the New Carquinez Bridge. Driving from the lowest voltage stage means that all active diode decisions are made based on the output of the charge pump's lowest voltage stage and then transferred to all other stages and diodes through buffers. This architecture has advantages. First, the lowest voltage stage comparators use the full range of available voltage. Second, the voltage on the lowest voltage stage can be controlled, so that the all actives diodes operate even during the initial charging, a period in which the charge pump stage's voltages rise unevenly, limiting the appropriate biasing if there were a comparator for each stage. Fewer comparators mean less power required, and only the first stage comparator needs to be functional for all other stages to work.

4.2 Start-up for the 6x Active Diode Design

4.2.1 Simulated Start-up for the 6x Active Diode Design

As expected, simulation results produced high power conversion efficiencies in regular operation once the charge pump IC-based system had started. These were measured by changing the resistive load on the output of the charge pump until the output was constant. The output power was then divided by the maximum harvestable power (with the harvester outputs matched) from the harvester. With a sine-wave, efficiencies between 60% and 70% were regularly reached in simulation. In simulation the charge pump consumed 0.5 µW. These results are verified in more detail in the next section. The unique start-up of this circuit is a significant contribution, and its simulation will be discussed in this next section in detail.

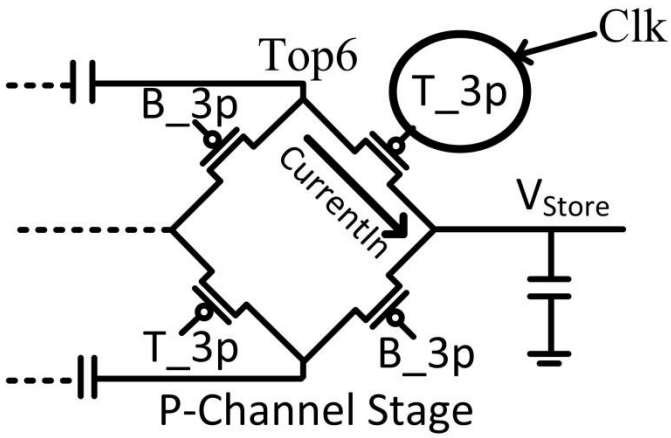

Figure 67. A close-up of the last stage of the charge pump is shown. Sub-threshold current flows through the PMOS on the top right corner during initial start-up.

As mentioned in Section 4.1, this circuit's start-up relies on deep sub-threshold functioning rather than passive diodes during start-up (Figures 67 to 71). This means that almost immediately, parts of the circuit allow for the charge pump to actively function. Figure 67 shows a close up of the last stage of the charge pump. Figure 67 will be closely analyzed in simulation to understand the initial start-up.

Figure 68 shows the beginning of the start-up process simulated in Cadence with an input of 700 mV. Initially, the input into the last stage of the charge pump goes to 0.6 V (Top 6). Even though the PMOS is not technically on, enough sub-threshold current flows through the PMOS on the last stage of the charge pump to start charging the parasitic capacitance and line of stacked

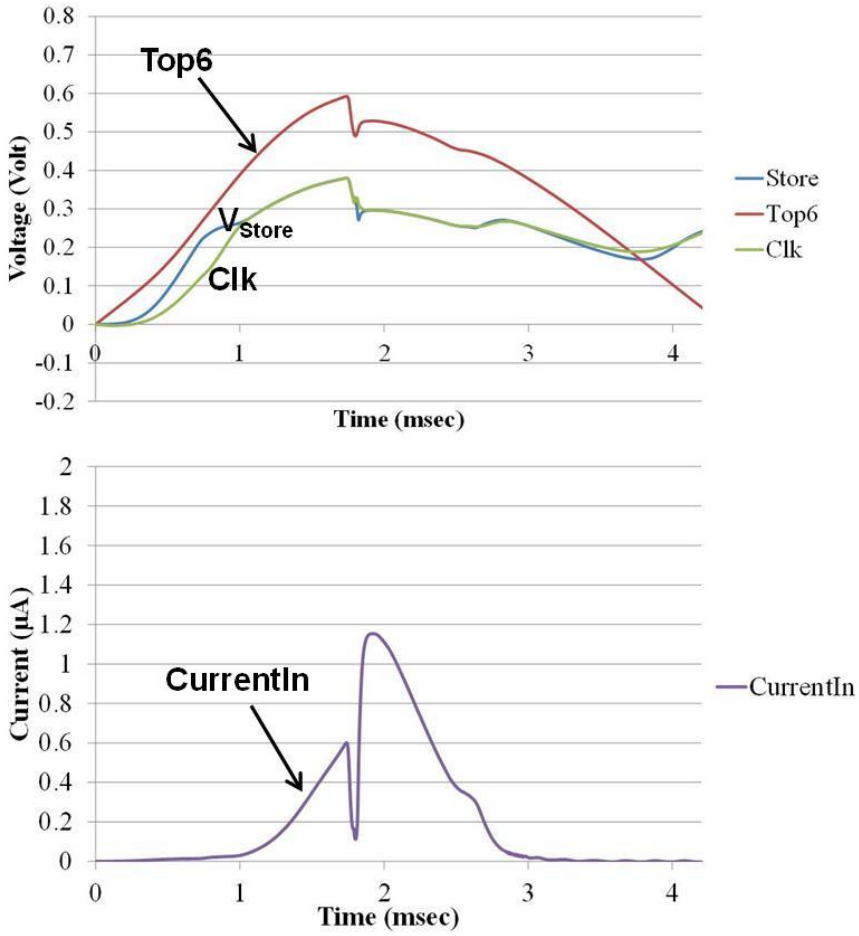

Figure 68. The first 4.2 mille-seconds of simulated start-up is shown. The top figure shows the input into the last PMOS when the system is off (Top6), the clock on this PMOS (Clk), and the output of this PMOS (Store). The bottom figure shows the current through the PMOS.

capacitors which add in series at the output of the charge pump (the signal labeled "Store"). The clock output soon follows the signal "Store." Eventually, this results in a peak of 1 µA flowing through the PMOS permanently storing charge on the capacitor chain of the charge pump. In the PMOS stages, far more charge flows when the signal is positive compared to when the signal is

negative. This can be deduced from Figure 68. The “Clk” will always be at a voltage between V_{store} and ground. Therefore, when the input at “Top6” is positive, the input into the “source” of the devices is more likely to be close to or above the gate voltage ‘Clk’ compared to when the input at the source is negative. This means far more current will flow when the input at the “source” is positive compared to when that input is negative in the PMOS devices. This will allow voltage and charge to build up on V_{store} and the later PMOS stages. With a slightly higher output voltage built up on the charge pump in the process just described, the next input peak results in a functional clock, which goes low as seen in Figure 69 near 10 ms, resulting in a peak current near 10 μA.

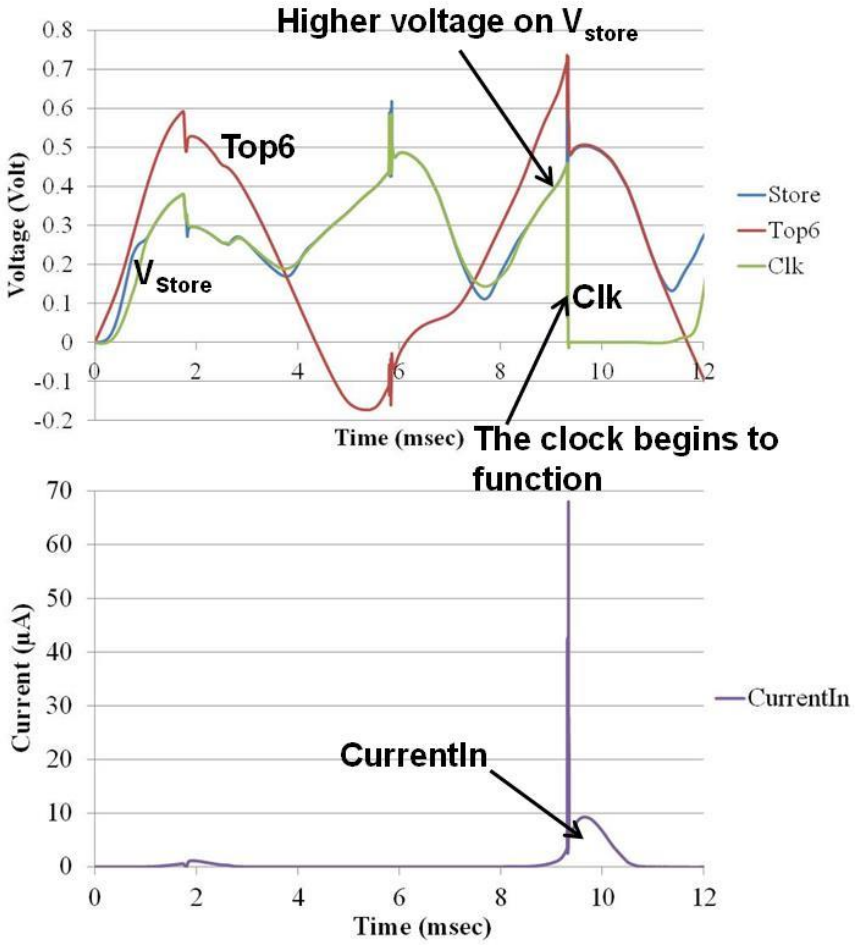

Figure 69. As before, the top figure shows the input into the last PMOS when the system is off (Top6), the clock on this PMOS (Clk), and the output of this PMOS (Store). The bottom figure shows the current through the PMOS. The first 12 seconds of simulated start-up is shown.

Since the PMOS devices are able to charge during start-up, it would be expected that the NMOS devices would not passively charge. This is true, and it is the method by which this system keeps the lowest voltage stage (an NMOS stage) low during initial start-up. This process is seen in Figure 70. This simulation results show that the top 3 PMOS stages charge first, while the bottom NMOS stage remains low during initial start-up. When the clock controlling the active diodes turns on, the voltage on the bottom NMOS stage begins to rise. It can also be seen in this picture that the top PMOS stages charge unevenly. In this simulated picture, the top PMOS stage "V_{Store}" charges more slowly than the lower PMOS stages 4 and 5. If there were a

comparator for every stage, this would mean that there would be a different level of margin for the comparators to work on each stage in deep sub-threshold. These varying margin levels in the different stages would be challenging if a comparator were used on each stage of the charge pump in deep sub-threshold start-up.

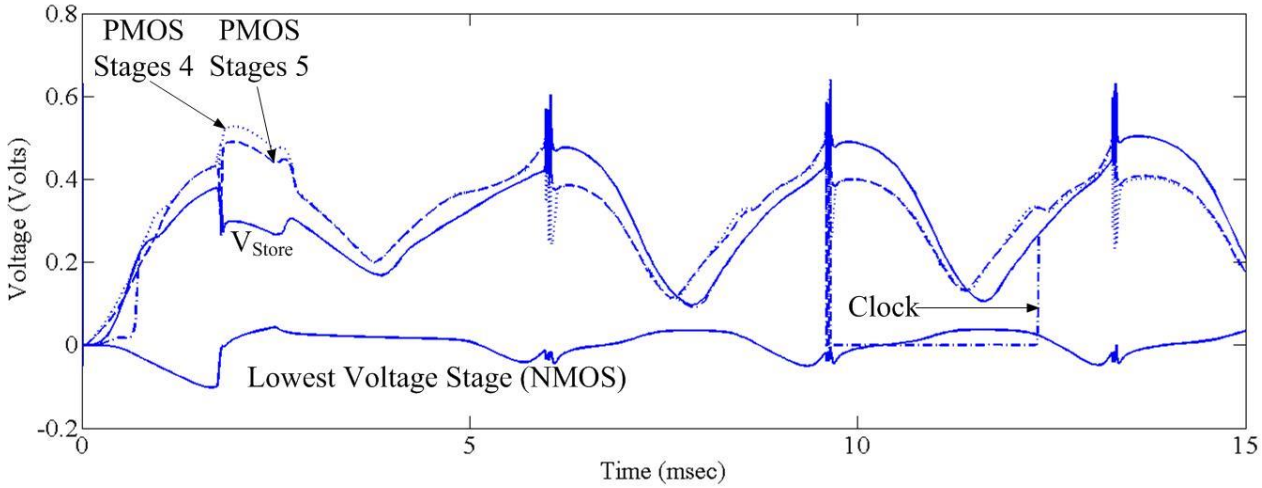

Figure 70. The first 15 mille-seconds of simulated start-up is shown. The top three PMOS stages, lowest voltage NMOS stage, and clock are shown in Cadence simulation.

Finally, Figure 71 shows the charging of this circuit over 0.5 seconds in Cadence. Near ~0.4V to ~0.5 V, the Schmitt trigger circuit turns on, and this enables the output's 10 µF storage capacitor to begin to charge. By initially enabling the charge pump to function without loading, the first stage of the charge pump is able to stay at a lower voltage. With the loading of a large capacitor on the output of the charge pump, it charges far more slowly because the charge pump is both charging the stacked capacitors (they add in parallel) and the large capacitor at the output. If there is a large capacitor at the output, the voltage on the lowest voltage stage will rise more quickly compared to the output at V_{Store}. This will limit start-up margin in deep sub-threshold just like with the circuit described in Chapter 3. If the voltage on the lowest voltage stage rises and V_{Store} remains basically constant the lowest voltage stage comparators will have less margin

to operate with in deep sub-threshold and will more likely fail to function leading to the need for an unloaded start-up.

Understanding the issue of "margin" explains the characteristics and potential problems seen in Figure 71. Figure 71 shows a simulation with the minimum turn on possible in this IC-based circuit simulation (near 700 mV). The voltage on the lowest voltage stage in Figure 71 begins to rise when the Schmitt trigger turns on and V_{Out} and V_{Store} are rising at nearly the same voltage after that. At voltages below this, the voltage on the lowest voltage stage rises enough, so that comparators will not function in simulation. For the comparators to optimally function, a comparison should be made between the input voltage and near 0 V at the output of the first

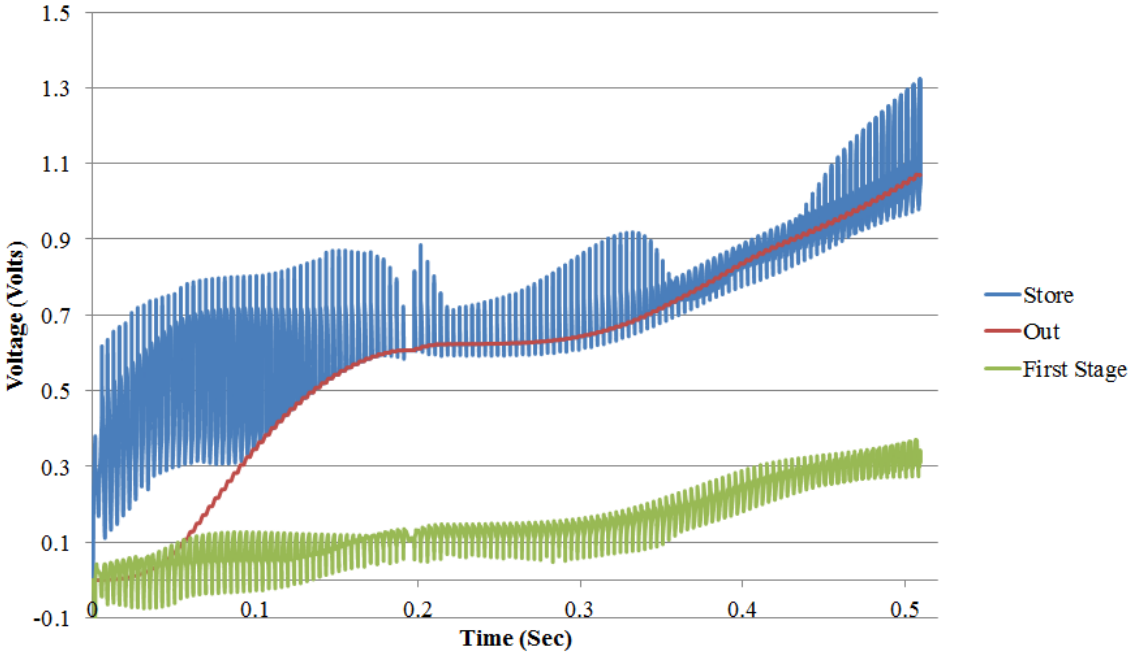

Figure 71. Cadence plots of the circuit start-up are shown. The voltage on the storage capacitor output (after the Schmitt trigger), charge pump output, and the voltage on the first stage of the charge pump are shown.

stage of the charge pump. This comparison to near 0 V avoids sub-threshold modeling and differential matching problems by giving the comparators more "margin" to operate with until the "V_{Store}" voltage is higher bringing the circuit out of sub-threshold. Once the charging of the large output capacitor begins to charge around 0.2 seconds, the voltage on the first stage begins

to rise as the circuit charges itself into regular operation. Without the Schmitt trigger, a charge pump's first stage voltage would rise first, even before later stages, meaning that some type of Schmitt trigger is necessary. Along with the necessity of the Schmitt trigger, best functioning occurs if the inverters are connected to the first stage comparator and all stages are driven based on the first stage comparison. This alleviates biasing issues because the voltages on the charge pump stages initially rise unevenly across the stages by making sure maximum margin is available by relying on the lowest voltage stage.

These biasing issues would be present if every active diode had its own comparator similar to previous published work [3, 4] and likely explain why the minimum start-up in these works is only at 500 mV. Minimum start-up in the charge pumps discussed in Chapter 3 and this chapter (4) are below 300 mV. Lab results will be discussed in the next section (Section 4.2.1) and will show minimum cold start working down to 280 mV; however, simulation shows minimum start-up near 690 mV. This significant difference is explained more in the model to hardware Section 4.5. At 280 mV the start-up occurs with the comparators functioning without the bias circuit operating, and both the input and the output of the charge pump (the output of the charge pump supplies the power for the system) are operating below the threshold of the technology near $V_{th} \sim 0.42$ V.

4.2.2 Measured Start-up for the 6x Active Diode Design

Many start-up characteristics and problems seen in simulation are also observable in hardware. Figure 72 shows the initial start-up observed in hardware with a 540 mV input. The top two PMOS stages are shown (specifically the outputs at V_{Store} and the 5^{th} PMOS stage). Also shown is the clock output driving the top diodes and the lowest voltage stage. Just as before in simulation (Figure 70), the PMOS stages charge first due to sub-threshold leakage and the lowest voltage stays low until the clock begins to function. As the clock voltage is low, the lowest voltage stage finally begins to slowly charge. This diagram shows that one input peak is higher than the other during the initial charging. For example, in Figure 72 the first peak reaches up to

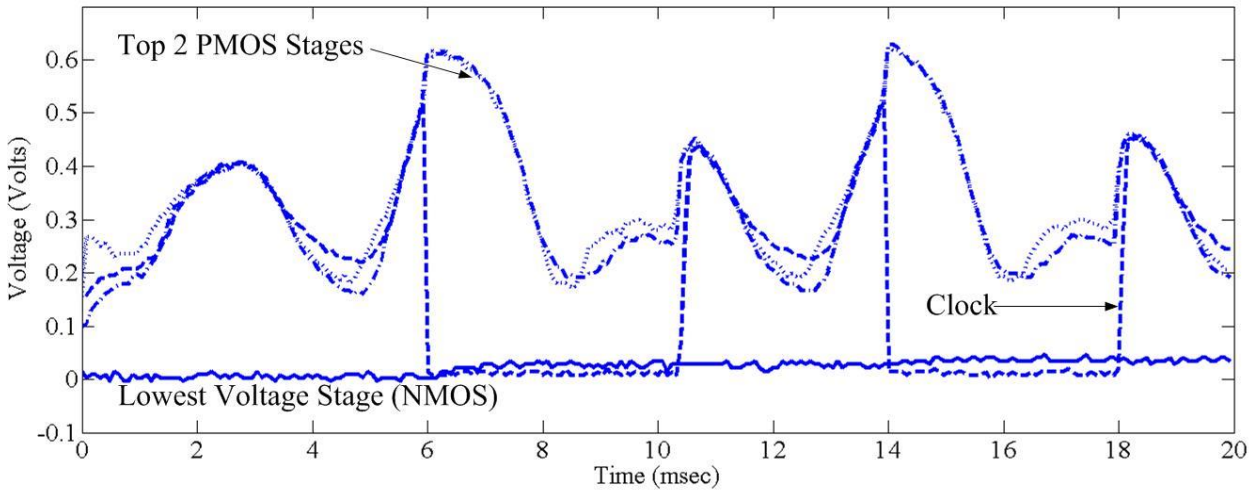

Figure 72. The first 20 mille-seconds of start-up are shown from hardware. The top two PMOS stages, lowest voltage NMOS stage, and clock are shown.

0.4 V while the second peak is above 0.6 V. This is likely because the input harvester into the system is floating with neither side being connected to ground. At the initial start-up, the harvester may not be centered at exactly ground like in simulation, resulting in the non-uniform peaks on the PMOS stages when initially charging.

Figure 73 shows the start-up of the PFIG over several seconds with an input sine-wave of 700 mV. The clock nearly immediately functions once the input is on and the "Store" signal also immediately starts to rise. There are likely one or two cycles where the clock is not functioning as seen in Figures 70 or 72; however, these cycles are not going to be observed when looking at the start-up over several seconds. Once "Store" is high enough (~near 0.4 V), the 10 µF capacitor at the outputs starts to charge. There is a long lull of several seconds before the output voltage of the charge pump rises above 1 V. This is similar to problematical functioning of the circuit described in Chapter 3.3. The interface circuit initially acts as a high input resistor, so the loaded input of the signal is near to the maximum of 700 mV, but as the charge pump is loaded the interface circuit's resistance decreases resulting in a lowered input into the harvester circuit.

Hardware results show that the general trends of start-up that are observed in simulation are observed in hardware. The structure using 3 NMOS stages followed by 3 PMOS stages allows for a lowest voltage stage high margin start-up because the voltage at the lowest voltage stage initially stays near ground. This behavior is seen in both hardware and simulation results.

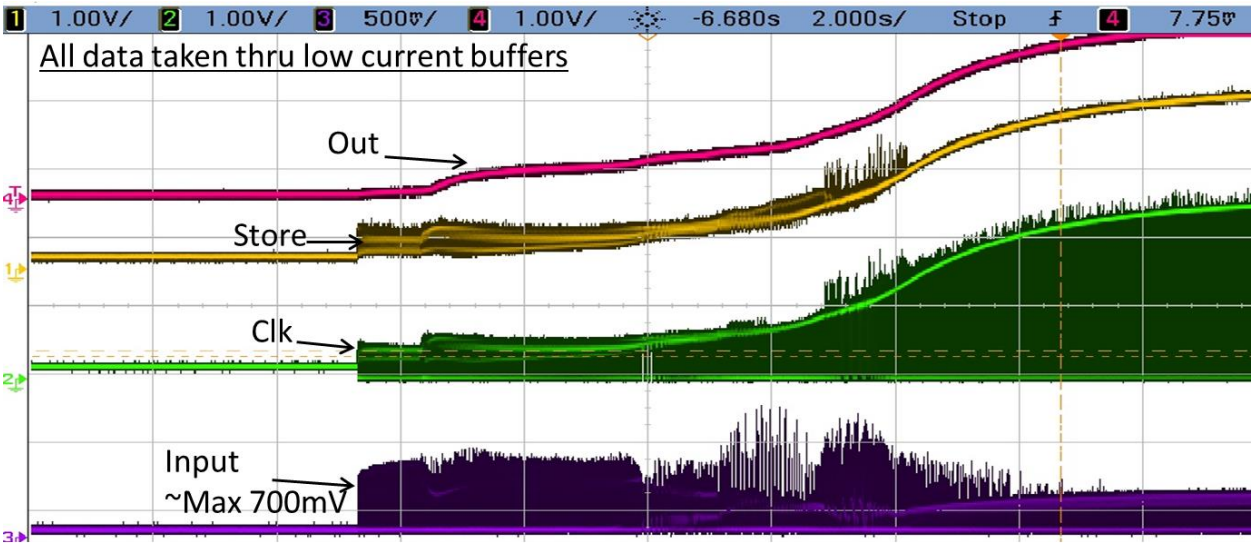

Figure 73. This shows oscilloscope outputs with the Input, Clk, "Store" signal and "Out" signal.

There is a significant mismatch between minimum start-up in both simulation and hardware. Without a load, minimum hardware's start-up is as low as 280 mV using a sine-wave generated by a transformer. In simulation minimum start-up is ~690 mV. This discrepancy of 410 mV is larger than what was seen with the IC-based system in Chapter 3, where hardware was only approximately ~100 mV better than what was predicted by simulation. This model to hardware discrepancy will be further analyzed Section 4.4 of this chapter.

4.3 Loading Methodologies

As discussed in both Chapters 3 and 4, the effect of the loading on the charge pump functioning reduces the charge pump's ability to start-up using designs that drive the active diodes of all stages with the comparator decision on the lowest voltage stage. To be able to power a bridge health monitoring sensor, the charge pump should be loaded with either a capacitor or resistor; however, for both IC-based designs in Chapter 3 and 4 the voltage on the lowest voltage stage will start to rise more quickly versus the harvester output if the system is unloaded. This will mean loss of margin for deep sub-threshold functioning. To avoid this type of loading problem, a low power circuit must be used to prevent current flow into a load until a high voltage can be achieved on the unloaded charge pump.

The circuit in Figure 35 solves the problem of how to design a circuit that consumes low power in the ~nA range and also does not let substantial current flow (even in start-up) until a specific adjustable voltage. There were multiple challenges in this design of this circuit, and the author tested and reviewed many designs before arriving at Figure 35. Because of the importance of this circuit, this section focuses on the literature and understanding of this low power circuit that does not allow substantial current flow until a specific voltage is reached. Every conceivable

problem was observed when trying to design this circuit with the various designs. Examples of circuit failure mechanisms include the following: (1) the turn on voltage would be near impossible to correctly set; (2) current would flow to the load for ultra-low voltages < 0.3 V no matter what was designed; (3) too much power would be used (>1 μW); or (4) too much power was for low voltages ~.7 V to 1V.

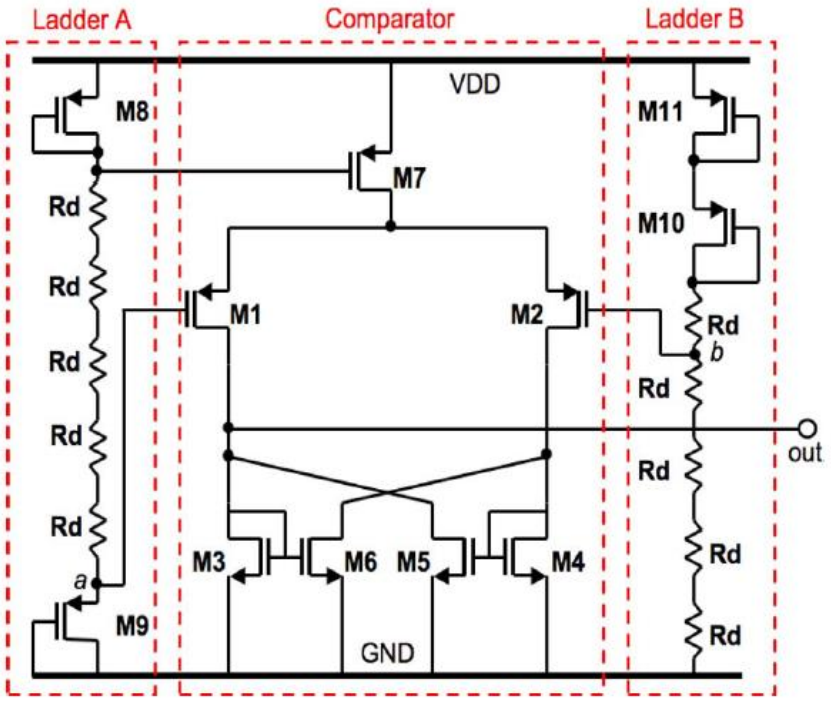

Figure 74. A previously designed mode selector circuit consists of a comparator and two input lines are shown. When the inputs into the comparator cross, the voltage from the supply is sent to the comparator's output [6].

After an extensive literature review this author concluded that using a comparator with two input lines called a mode selector seen in Figure 74 [6] is the most effective strategy for this switch. One input contains a diode at the bottom while the other line uses a resistive ladder. The behavior in the line with the diode is non-linear while the resistive line is linear. The point of crossing enables current to flow from the "VDD" of the system to the output. This same method has been used in other energy harvester rectifying circuits as seen in Figure 75 [2]. This "switch" in this rectifying harvester circuit uses a group of comparators to provide the initial start-up

decision to allow current to flow into a load. The initial turn-on is controlled by two inputs into comparators. One input is from a linear resistor ladder while another input is from a bias reference circuit (Figure 38). Figure 38 is referenced to be the same as is used in Figure 75. In this system (Figure 75) one output (the bias circuit output) is non-linear and controlled by a diode attached to ground just like in Figure 74, while the other output is linear based on resistor ladder just like in Figure 74. As in Figure 74, the output comparators of Figure 75 allow for initial turn-on when the linear and non-linear inputs lines cross into comparators. There are two drawbacks of these circuits. First, these utilize high power. While the specific current used in the mode selector (Figure 74) or comparator, bias circuitry and resistive line (Figure 75) are not specifically given. The system containing the mode selector consumes near 5 μW, while the rectifying circuit consumes up to 2 μW. Second, these designs do not provide a method to control the exact time when the system turns on into a load.

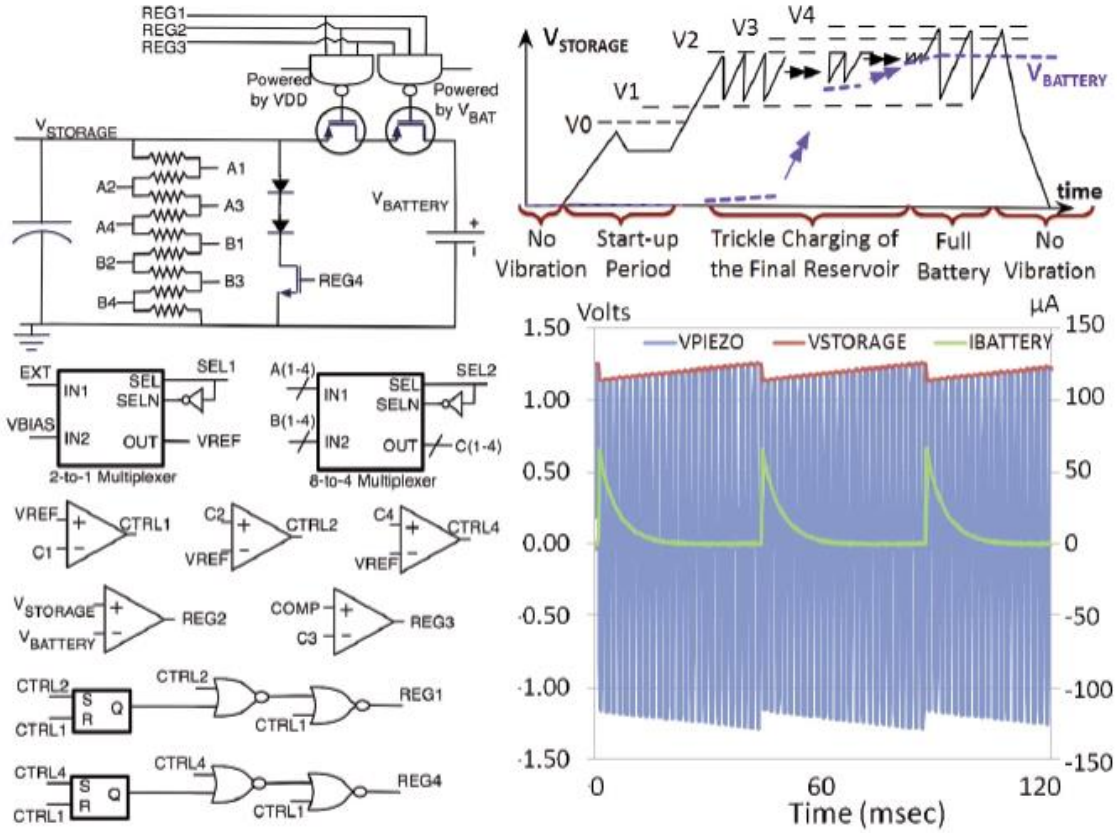

Figure 75. This shows a rectifier circuit with cold start-up that allows start-up that turns on at a specific voltage using a method similar to Figure 74. This turn "switch" was part of a piezoelectric rectifying circuit [2].

The redesigned mode selector in Figure 35 provided an effective solution that is both adjustable and consumes low power (~100 – 150 nA); however, the author designed several circuits before deciding on a low power design similar to Figure 74. Multiple discrete solutions were designed. The first discrete solution by this author used the LTC 1540 comparator [7]. Figure 76 shows the discrete hysteresis switch used with an initial charge pump design. It is similar to the Figure 74 in that one input line is linear while the other input line contains some type of diode. This design using the LTC 1540 comparator [7] even worked well in LTspice simulations; however, in lab evaluations significant issues were encountered with the comparator's start-up behavior. While the comparator regularly consumes near 1 µW of power at near 2 V, the power consumption during start-up was near 2 – 3 µW near 0.8 V. This

dramatically reduced start-up ability. Also, during low voltage start-up, the comparator had the

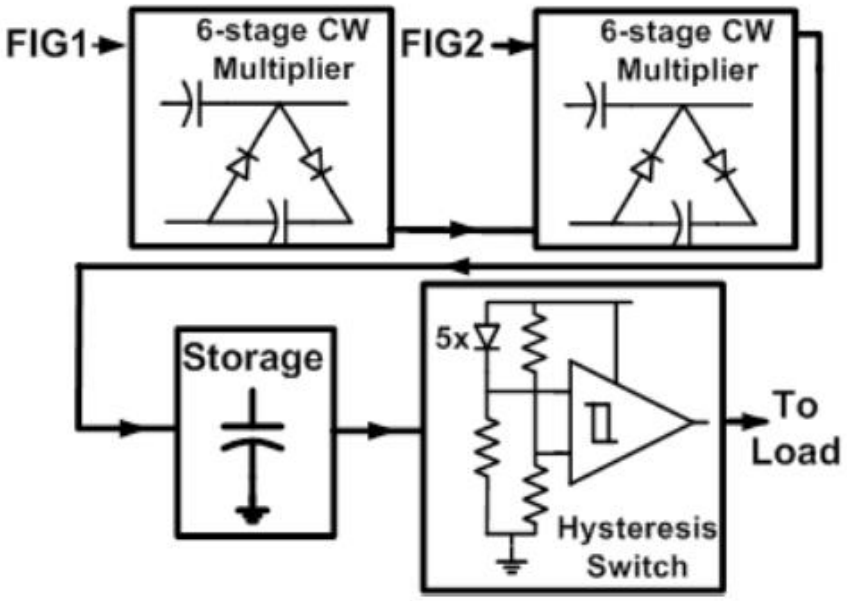

Figure 76.The author's previously published work showing two cascaded six stage multipliers followed by a discrete hysteresis switch using a LTC 1540 comparator is shown [7].

tendency to inexplicably turn-on at low voltages under 0.4 V. This also dramatically reduced start-up ability. The turn-on voltage with hysteresis was eventually achieved that resulted in the comparators ability to discharge near 2 – 2.5 V (but not appropriately start-up). The storage signal is seen in Figure 77. In this figure, the hysteresis switch discharge near 2.5 V and stops discharging near 2 V. While this discharge pattern looks good, significant manipulation was needed to obtain these characteristics, and the comparator switch would not maintain the same characteristics when its design was transferred from a bread board to a PCB board because the resistors in the hysteresis switch needed to be so finely set. These various problems emphasized the limitations of discrete comparators.

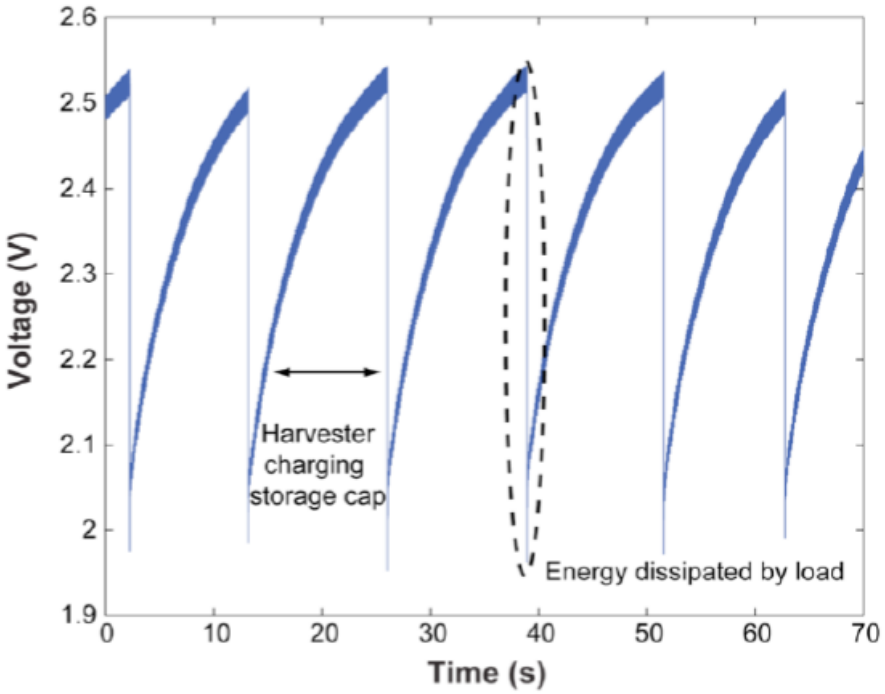

Figure 77. The measured storage characteristics with the hysteresis switch are shown. The switch discharges near 2.5 V and stops discharging near 2 V.

Other discrete methods were attempted to create a switch with and without hysteresis. Figure 78 shows another effort at a discrete switch. There is no hysteresis in this specific switch. It works because V_{Store} both supplies the drain and the gate on $NMOS_1$. In the ideal case when $NMOS_1$ switches on, the input into the first inverter goes negative and a positive output from this inverter turns $NMOS_2$ on. The output of $NMOS_2$ then goes through a buffer so the voltage delivered to the load is at the same voltage level as V_{Store}. Again, this switch worked in simulation and consumed about 200 – 300nW; however, significant problems were also observed in hardware. Many devices were used in the place of $NMOS_1$ and $NMOS_2$, and eventually the Advance Linear Devices ALD110904 with a V_{th} of 420 mV was used for $NMOS_1$ and the Advanced Linear Devices ALD110914 with a V_{th} of 1.42 V was used for $PMOS_2$. The inverters used were Fairchild NC7SP04. The inherent problem with most of the discrete NMOS devices is that they are not suitable for deep sub-threshold currents in the ~100 nA range and do not always function remotely close to expectations. This means that it is very difficult to have an adjustable

turn-on voltage while maintaining low current operation in this switch. In the ideal case, the V_{th} of $NMOS_1$ controls when the switch turns on; however, this was not accurate in deep sub-threshold. After much trial and error, turn on was achieved near approximately 1 V turn on.

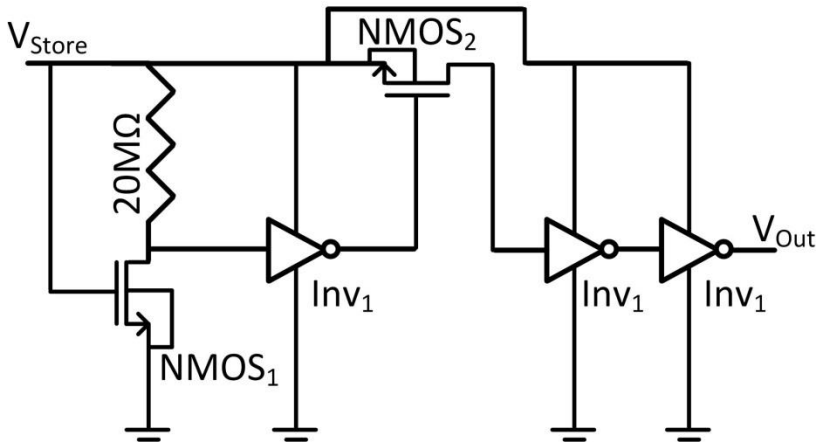

Figure 78. A discrete switch consisting of two PMOS devices and multiple inverters is shown. This switch turns on when V_{Store} reaches approximately ~1 V.

While the IC design that was finally settled on consumed between 100 – 200 nW of power in Figure 35, another IC design of a switch with much lower power consumption was attempted with minimal success. One such attempt is shown in Figure 79. This IC design makes use of the level of a charging capacitor to create a low power switching circuit. If this design were working correctly, the capacitor's voltage would rise. The diodes on top of the charging capacitor are used to offset the voltage from supply. When the voltage on the capacitor is high enough it would activate the inverters in the system to turn on the PMOS sending current to the output load. The additional diode that switches into the system would have been used to add hysteresis. This switch worked in simulation and only consumed near 30 nW. It even worked in hardware with a very steadily rising input; however, with a charge pump input being driven by either sine-wave or PFIG output and quickly rising and constantly changing, this switch does not respond quickly enough to be effective. This means that with the changing of the sine-wave or

PFIG input, the switch is constantly turning on and off, meaning it is doing more harm than good. The switch in Figure 79 was used in the simulations in this IC-based system. By attaching a very minimal capacitance, the inverters can basically immediately send a low voltage to the PMOS connecting to the large output capacitance in the system turning it on. Since only a small capacitor is used to charge, the switch is not turning off and on. With this setting using a small capacitance to charge, the "In" signal must be at least one V_{th} ~0.42 V for the overall switch to activate and allow current to flow through the PMOS switch to "Out".

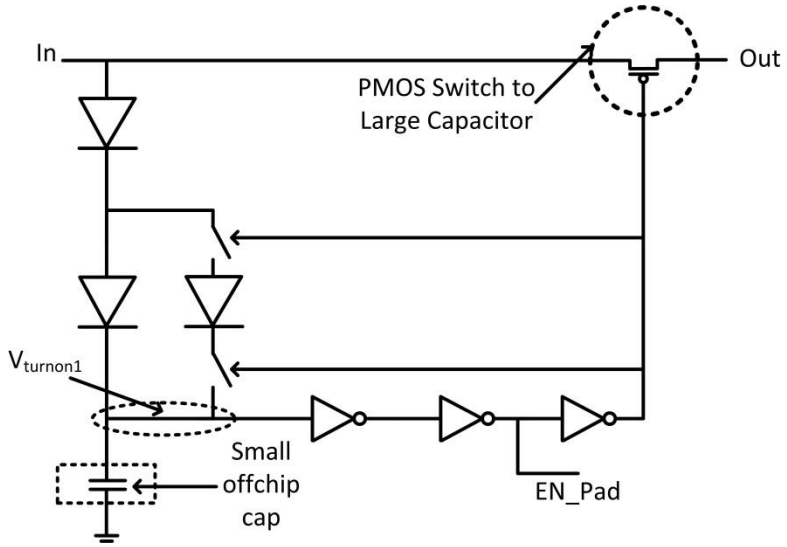

Figure 79. This shows an IC-based switch using an off-chip capacitor. Hysteresis is added by additional switching in an additional diode.

Because of these minimally functioning designs of this switch, it was concluded that for a low power solution capable of adjustability, not only is an IC design necessary, but to maintain proper control over the turn-on voltage a comparator structure is needed similar to either Figure 74 or Figure 35. A structure similar to Figure 78 might be tried in an IC; however there will still be limitations in the voltage thresholds of available devices to enable adjustability. This author concluded that a comparator structure similar to what was used in Figure 35 was the most effective strategy.

4.4 Lab Results for 6x Active Diode Charge Pump

Power conversion efficiency results for this IC, shown in Figure 80, are compared to the results of one three-stage discrete charge pump similar to what would be used in Chapter 2. The voltage is held constant by adjusting the load at the output of both the discrete and active diode IC based charge pump. Adjusting the load at the output of an energy harvester circuit is a common technique for measuring efficiency. Efficiency is the power measured at the output divided by the maximum power produced by a perfectly matched harvester as defined in Section 1.5. Results were taken with a sine-wave generated by two transformers with output impedances of 1.2 kΩ and 300 Ω. In both cases the IC based charge pump produced high efficiencies (up to 69%), which is significantly higher than the discrete passive diode charge pump. There is

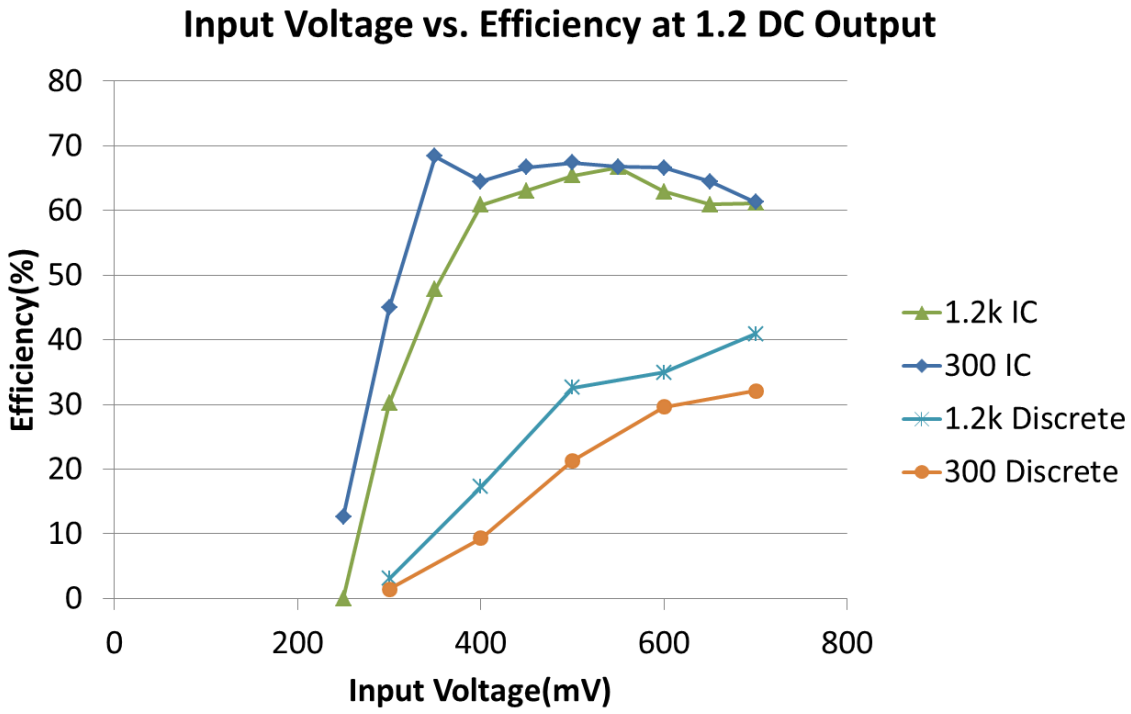

Figure 80. This shows the power conversion efficiency measured results for the first fabricated IC and one discrete charge pump (not cascaded) over range of input voltages with a sine-wave generated by transformers with output impedances of 1.2 kΩ and 300 Ω.

increased efficiency in the IC-based charge pump because the diode's turn-on voltages are dramatically decreased by the active diode architecture. As expected, the circuit consumed between 0.5 µW and 0.6 µW tested at ~1.1 V.

Start-up also occurred with the PFIG, but a higher voltage was necessary because the PFIG signals produced so much less power than a sine-wave. For example, for a PFIG actuated at 6 Hz, start-up was possible with a PFIG output with peak near 700mV, while start-up was possible at higher frequency PFIG actuations with a lower voltage maximum peak. Without loading at the output, start-up was possible down to a 280 mV sine-wave, and with a 10 µF capacitor on the output (after the Schmitt trigger) start-up was possible with a 380mV input sine-wave. As in simulation, the ×6 charge pump was able to start-up without loading in hardware; however, measured hardware start-up was much better than simulated start-up. Simulated start-up occurred at a minimum of 690 mV with this design. These differences are discussed in the next chapter.

4.5 Model to Hardware Correlation in Sub-threshold Start-up

Figure 81 shows the comparison between the minimum start-up of the simulation results and the lab results for the initial IC tested in the lab. In simulation and lab tests, better results were seen with the same voltage at lower output impedances. The smaller the output impedance, the more power generated from the vibration harvester at the same voltage, and more power is likely to enable active start-up. As described previously in Section 4.2.1, the loading on the charge pump affects the biasing of the first stage comparator, negating the beneficial effects of the lowest voltage stage driven active diode charge pump. This results in higher minimum start-up with a capacitive loading. The Schmitt trigger for these specific hardware results turns on near

~0.4 V as just described in Section 4.3, which still causes loading problems. The IC in Chapter 3, uses a better Schmitt trigger (mode selector), which has a higher turn-on. This enables lower voltage start-up because the capacitive loading will occur at a higher voltage. The key feature of Figure 81 is the significant difference between the simulation and measured results. Without loading, hardware results show start-up possible at ~280 mV, which is less than half of the simulated minimum start-up (~near 690 mV). Initial simulation work leads to the conclusion that deep sub-threshold conduction is not modeled correctly (i.e. what current flows when the V_{gs} of a device is significantly below threshold).

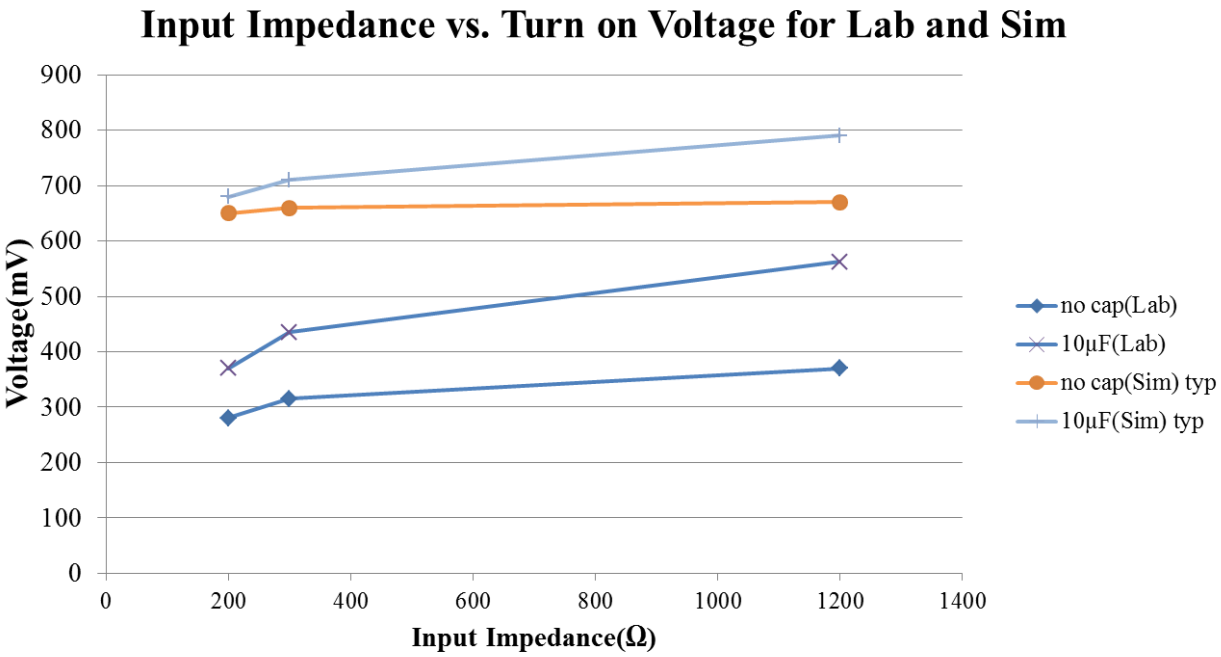

Figure 81. This shows the minimum voltage where start-up is possible for varying harvester input impedances and varying capacitive loads on the charge pump output. A very significant difference is seen between lab and simulated minimum start-up which shows that lab results are twice as good as simulated results for the "2012" IC.

Also, the measured long-term transient behavior during start-up is significantly different than simulation results. As described previously, Figure 73 shows start-up measured in the lab. In this figure, the charge pump experiences a relatively long lull lasting several seconds, before quickly charging up to higher voltage levels. This behavior is not seen in simulation. Either the circuit quickly starts up in simulation with a minor lull of a fraction of a second as seen in Figure 71, or the circuit does not start-up at all in simulation. These start-up differences between both simulation and hardware continue to point to an incorrect modeling in the sub-threshold characteristics of the devices.

4.6 Applying Learning from the ×6 Charge Pump to an Improved ×16 Charge Pump

This chapter presents a method where the voltage on the lowest voltage stage remains low during the passive part of the start-up. The choice of the device on the lowest voltage stage causes the lowest voltage stage to stay low. In the case of ×6 charge pump, the NMOS devices on the lowest voltage stage prevent passive charging. This allows the lowest voltage stage to stay near 0 V during passive start-up, which allows for high margin comparator operation once the sub-threshold active start-up in the charge pump begins. Once active functioning is enabled, all voltages on active diode stages begin to rise. This idea discussed in this chapter can be used to enable a more robust start-up in the ×16 charge pump discussed in the last chapter. Figure 82 shows possible changes in the ×16 IC-based charge pump using the ideas discussed in this chapter. First and most importantly, the lowest voltage stage on the bottom of the negative charge pump would be changed to PMOS. This would prevent passive charging during initial start-up and enable lowest voltage active functioning at high margin once active diode rectification begins. Additionally, the two NMOS stages of the on the top charge pump would be changed to PMOS to further aid in passive start-up. In the present start-up of the ×16 charge

pump analyzed in Chapter 3, these two NMOS stages do not add to the passive start-up of the system.

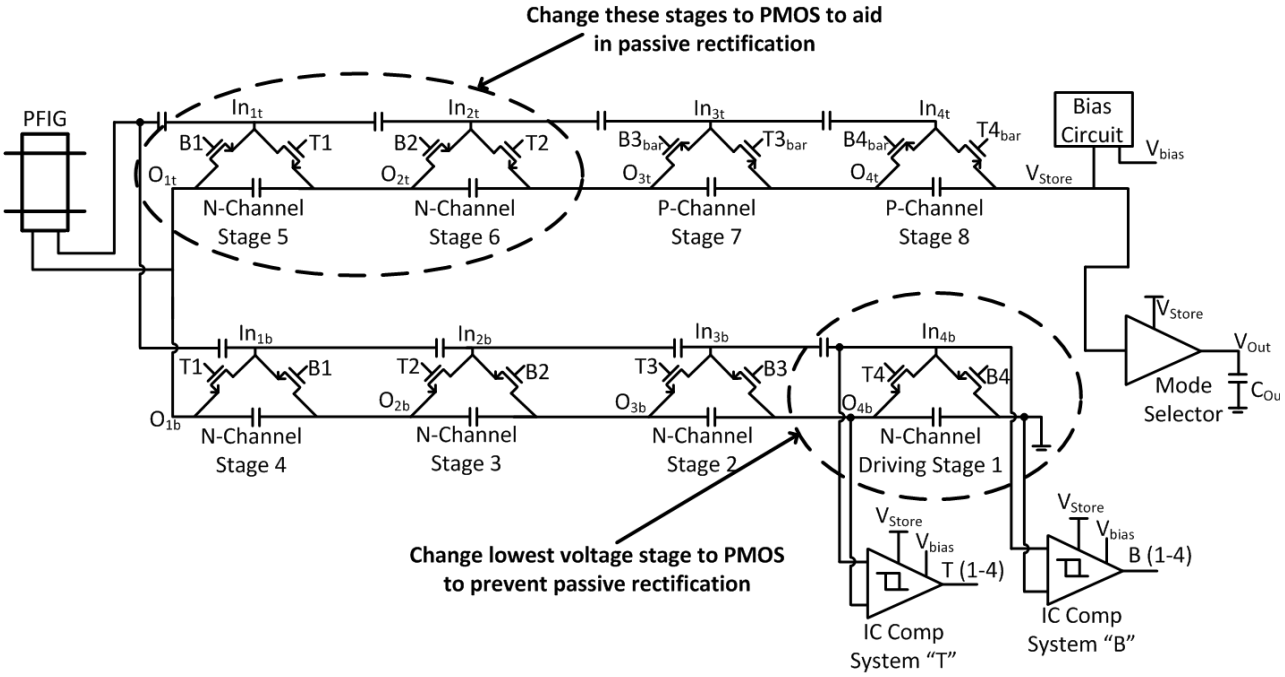

Figure 82. Shows possible improvements to the ×16 IC-based charge pump based on the ideas in this Chapter 4. The lowest voltage stage would be changed to PMOS (from NMOS) and the bottom two NMOS stages of the top positive charge pump would be changed to PMOS.

4.7 IC-based ×6 Charge Pump Circuit Conclusions

This ×6 charge pump circuit provides a solution to start-up, boost, and rectify the ultra-low power inputs from a vibration harvester that is either a sine-wave or a PFIG like decaying sine-wave input. The system is capable of active sub-threshold diode start-up using techniques that drive the charge pump system from the lowest voltage stage. The use of only NMOS devices on the lowest voltage stage causes the lowest voltage stage to remain low compared to the PMOS stages. Since the lowest voltage stages remain low, high margin sub-threshold functioning is possible on the lowest voltage stage, and the comparator decisions can be transferred to the rest

of the stages through inverters. This system demonstrates a different method of sub-threshold start-up using the lowest voltage stage functioning compared to the ×16 design discussed Chapter 3. Table 8 shows the ×6 IC-based charge pump compared to other works and designs by this author and other authors. Other than transformer-based solutions and this author's ×16 design, this design shows minimum cold-start and minimum regular functioning that exhibits record low active functioning. Minimum cold-start is at 280 mV and minimum functioning is at 138 mV. Efficiencies as high as 69% were measured using a sine-wave input.

Table 8. Shows the comparison of this ×6 charge pump versus other major works from literature. Peak voltages are reported as defined in Section 1.5. Values are assumed to be for a sine-wave unless indicated with a "PFIG".

Works capable of boosting from a harvester	**×6 Charge Pump Chapter 3 IC 2012***	**×16 Charge Pump Chapter 4 IC 2013***	**[8] McCullagh Chapter 2**	**[9] Kwon**	**[5] Arnold**	**[4] Arnold**	**[10] Szarka**	**[11] Rahimi**
Technology	180 nm & Discrete	180 nm & Discrete	Passive Discrete	2µm BiCMOS & Discrete	Active Discrete	Active Discrete	Active Discrete	Active Discrete
Max Boosting	×6	×16	×60	~×4	×12	×8	×14	×15 due to 1:15 transformer
Boosting Method	Charge Pump	Charge Pump	Transformer Charge/ Pump	Inductor	Rectifier /Inductor	Charge Pump	Inductor/ Charge Pump	Transformer Charge/ Pump/ Rectifier
Circuit Power Consumption	~0.6 µW	~0.6 µW	0 µW	estimate ~0.25 µW	Not given	6.4 µW	~21µW	Estimate ~1 µW
Min Start-up Voltage	280 mV	220 mV 415 PFIG	60 mV	Pre-charge required	1.25 V or Pre-charge for 5 mV	500mV	~500mV	200 mV
Min Functional Voltage	138 mV	110 mV	60 mV	350 mV	~5mV	350 mV	~500mV	200 mV
Max Circuit Efficiency	69% SW	66% 50% PFIG	27%	49.9%	84%	82%	76%	35%

*Journal papers in preparation by McCullagh

4.8 Comparator Improvement Analysis

In both Chapters 3 and 4, the IC-based system used the same common gate differential to single ended comparator. This comparator is the weak point of this design. In many cases, passive functioning will enable the output voltage to rise to 0.2 – 0.3 V. At this voltage the comparators begin to function. The weakest point for failure is between the voltages of 0.35 to 0.8 V. The failure here is when the comparator stops functioning and the output of the charge pump (V_{store} for both IC-based systems) stalls. This section gives continued analysis of this comparator failure and possible solutions to improve it in future designs. It begins with a section showing that a bias voltage the rises earlier than designed leads to improvement in the comparator functioning. Temperature variation of the ×16 design is then investigated. The third section shows the specific simulated failure that occurs near 0.35 to 0.8 V. Finally the model to hardware discrepancy is further discussed.

4.8.1 Forcing the Bias on Earlier in the Start-up Process

Figures 83 – 88 show the effect a higher V_{bias} has on improving start-up. During start-up with an input that would regularly fail (270 mV for this particular IC), each time V_{store} stalls and V_{bias} is external raised, V_{store} immediately rises again due to the comparator becoming functional. In these cases where V_{bias} is externally raised, the clocks immediately begin to function allowing for V_{store} to continue rising. Figure 83 shows a start-up with a 270 mV sine-wave input into an IC that can successfully start-up with a 300 mV input. When the V_{store} levels off, V_{bias} is externally raised through the connection on the pad of the IC. Once V_{bias} is raised, V_{store} rises for about 1 second before leveling off again when the active diodes no longer again function. Figure 84

shows the V_{store}, V_{bias}, and the clocks of the system. The point of this Figure 84 is to show that where the clocks begin to function. Similar to other diagrams, the clocks controlling the active diodes begin to function once V_{store} reaches 0.2 – 0.3 V

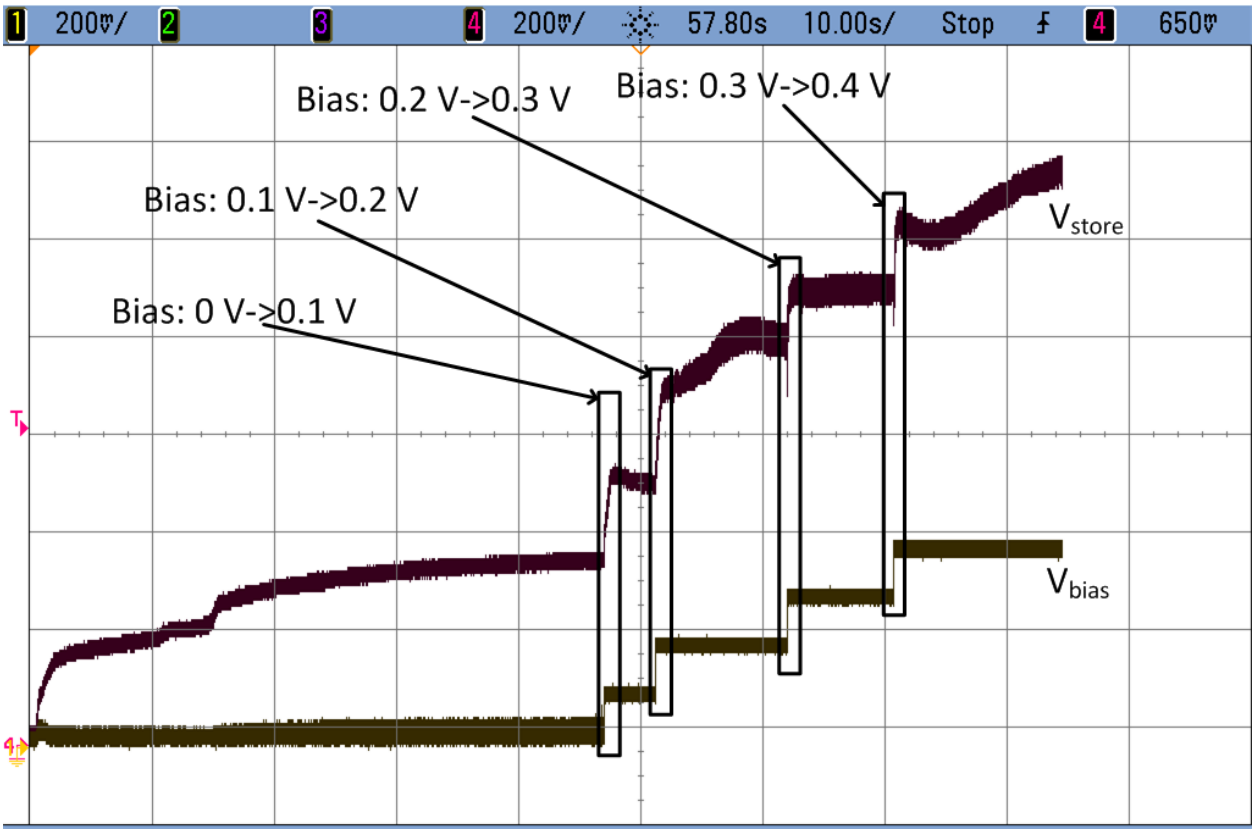

Figure 83. This shows measured V_{store} on top and Vbias on the bottom. Every time V_{bias} is externally raised, V_{store} quickly rises for about 1 second before leveling off again.

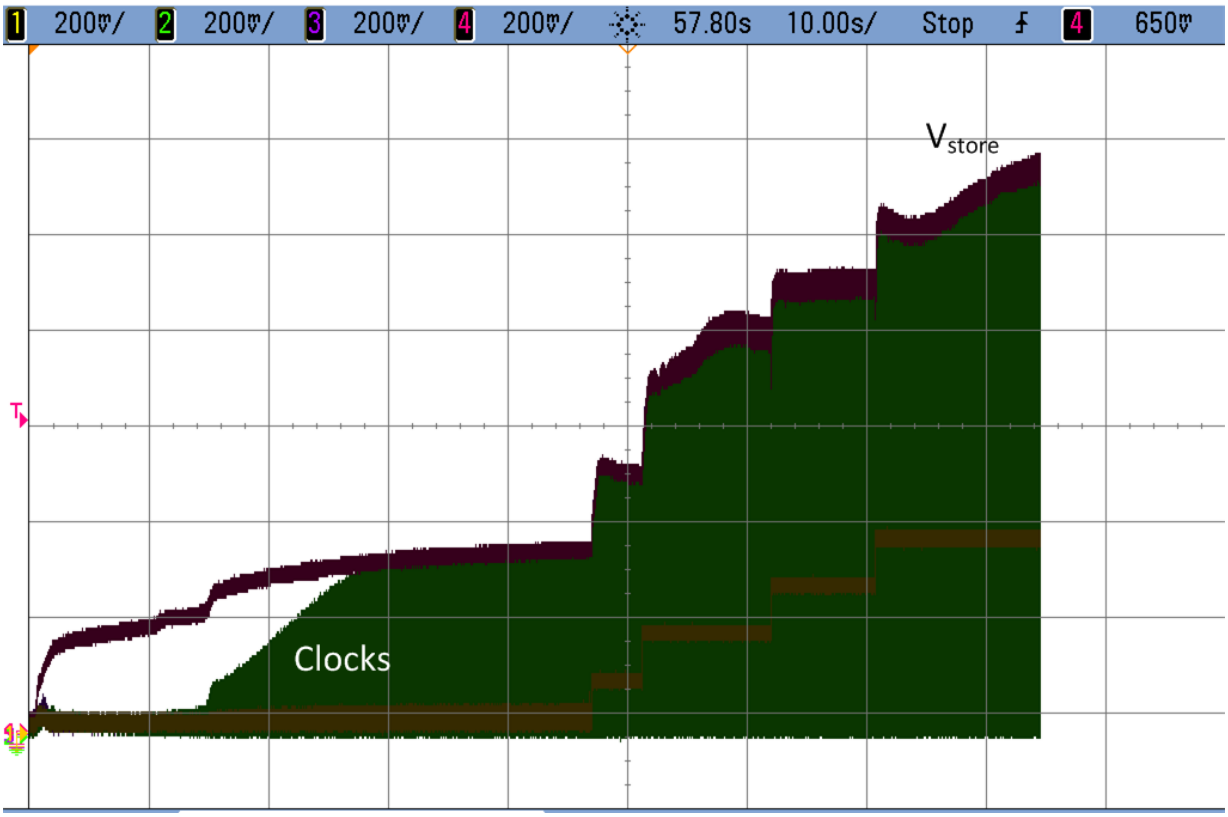

Figure 84. This shows measured V_{store} and the active diode clocks as V_{bias} is externally raised. As expected the clocks turn on near 0.2 – 0.3 V.

Figures 85 – 88 show the close ups of the clocks as the bias is externally changed from 0 to 0.1 V, 0.1 to 0.2 V, 0.2 to 0.3 V, and 0.3 to 0.4 V respectively. In every case both active diode clocks work far better immediately after the bias voltage into the circuit is externally increased. These diagrams show that a bias voltage that could actively function and turn on well below the V_{th} of the system would dramatically improve the comparator functioning in the active diode sub-threshold region of this circuit's operation.

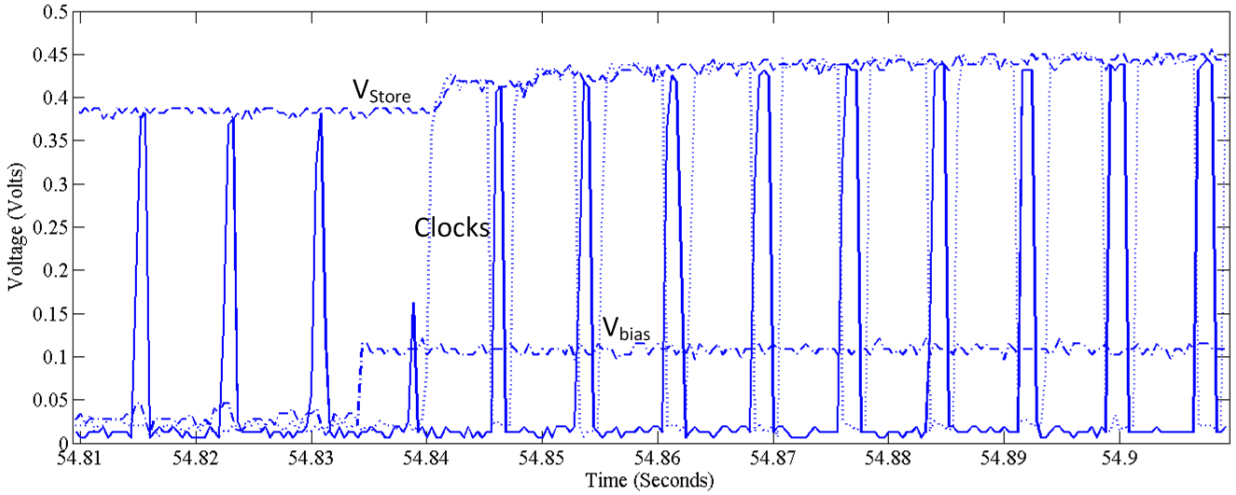

Figure 85. A measured close up of V_{store}, active diode clocks and V_{bias} as the V_{bias} is external changed from 0 to 0.1 V is shown.

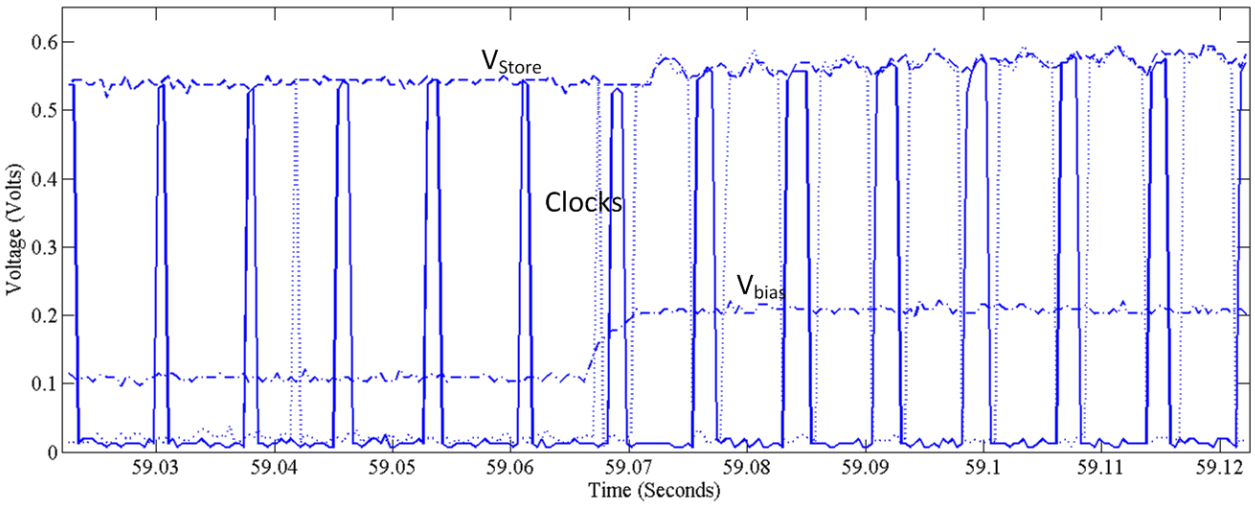

Figure 86. A measured close up of V_{store}, active diode clocks and V_{bias} as the V_{bias} is external changed from 0.1 to 0.2 V is shown.

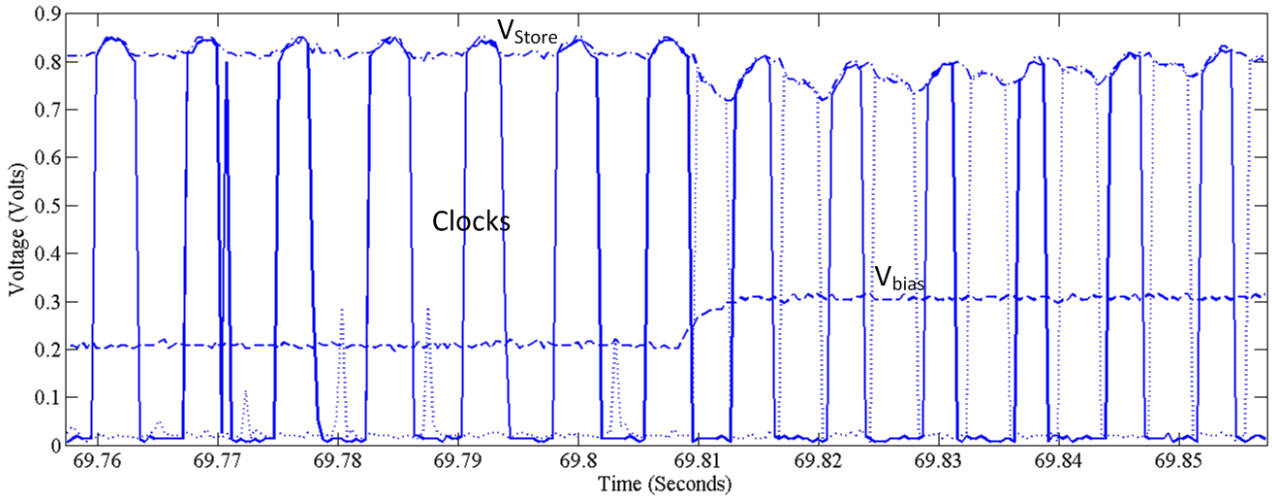

Figure 87. A measured close up of V_{store}, active diode clocks and V_{bias} as the V_{bias} is external changed from 0.2 to 0.3 V is shown.

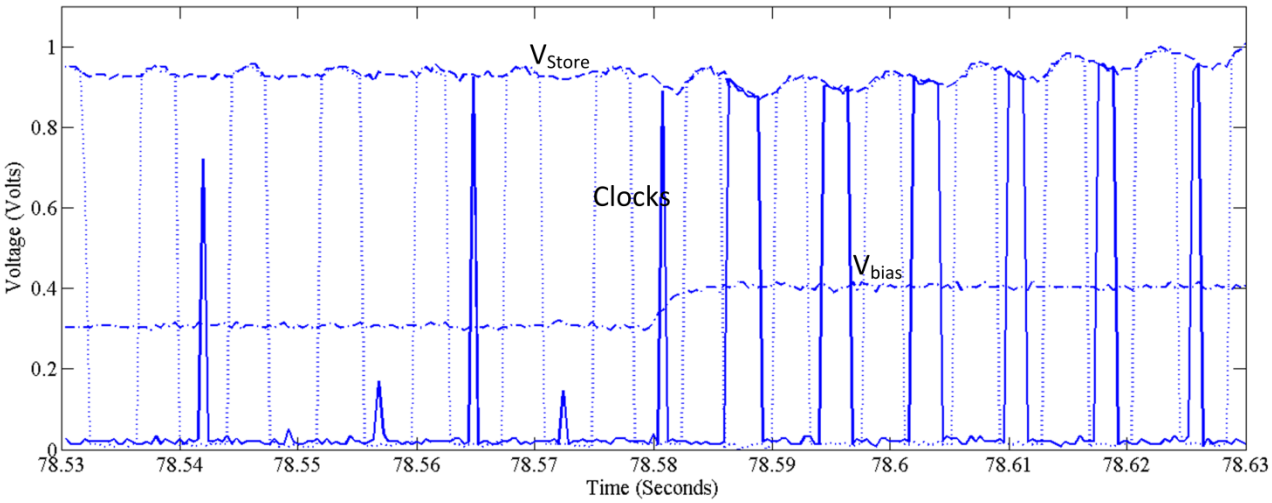

Figure 88. A measured close up of V_{store}, active diode clocks and V_{bias} as the V_{bias} is external changed from 0.3 to 0.4 V is shown.

4.8.2 Comparator Functioning Over Temperature

To better understand what characteristics this design is sensitive to, temperature data on start-up on the ×16 design was taken between 0 – 100 °F for a specific IC that regularly started at 300 mV. Little variation (20 mV) was seen in minimum start-up over temperature. At 0 °F start-

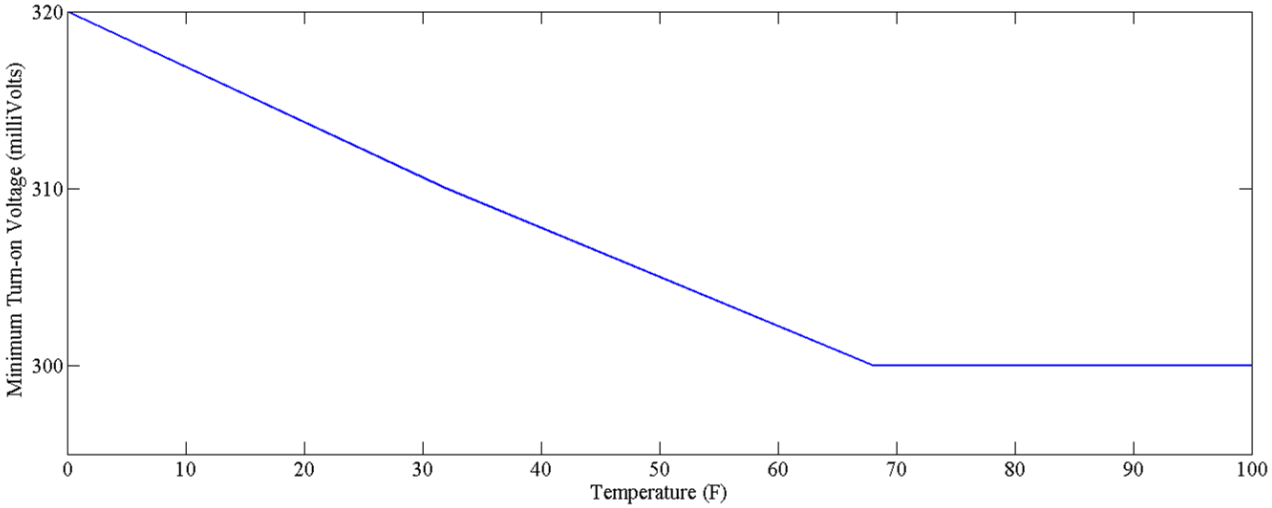

Figure 89. Measured data taken in a temperature chamber shows minimum start-up on an IC that regularly starts at 300 mV taken from 0 to 100 °F. A 20 mV variation is seen over temperature.

up was 320 mV. Similar results were seen in simulation. These results verify that the temperature's effect on start-up is not a major concern. In fact the minimum start-up over temperature is robust with a slightly higher minimum start-up measured at low temperatures. From this data, it is concluded that the comparators remain functional over temperature, and an extreme sensitivity to temperature does not explain the model to hardware discrepancy.

4.8.3 Simulated Comparator Failure

The section explains what specifically happens when the differential to single ended common gate comparator stops functioning during start-up. In the examples from the Chapter 3, this usually happened between 0.35 and 0.8 V as indicated in Figures 46 – 49. Figure 90 shows

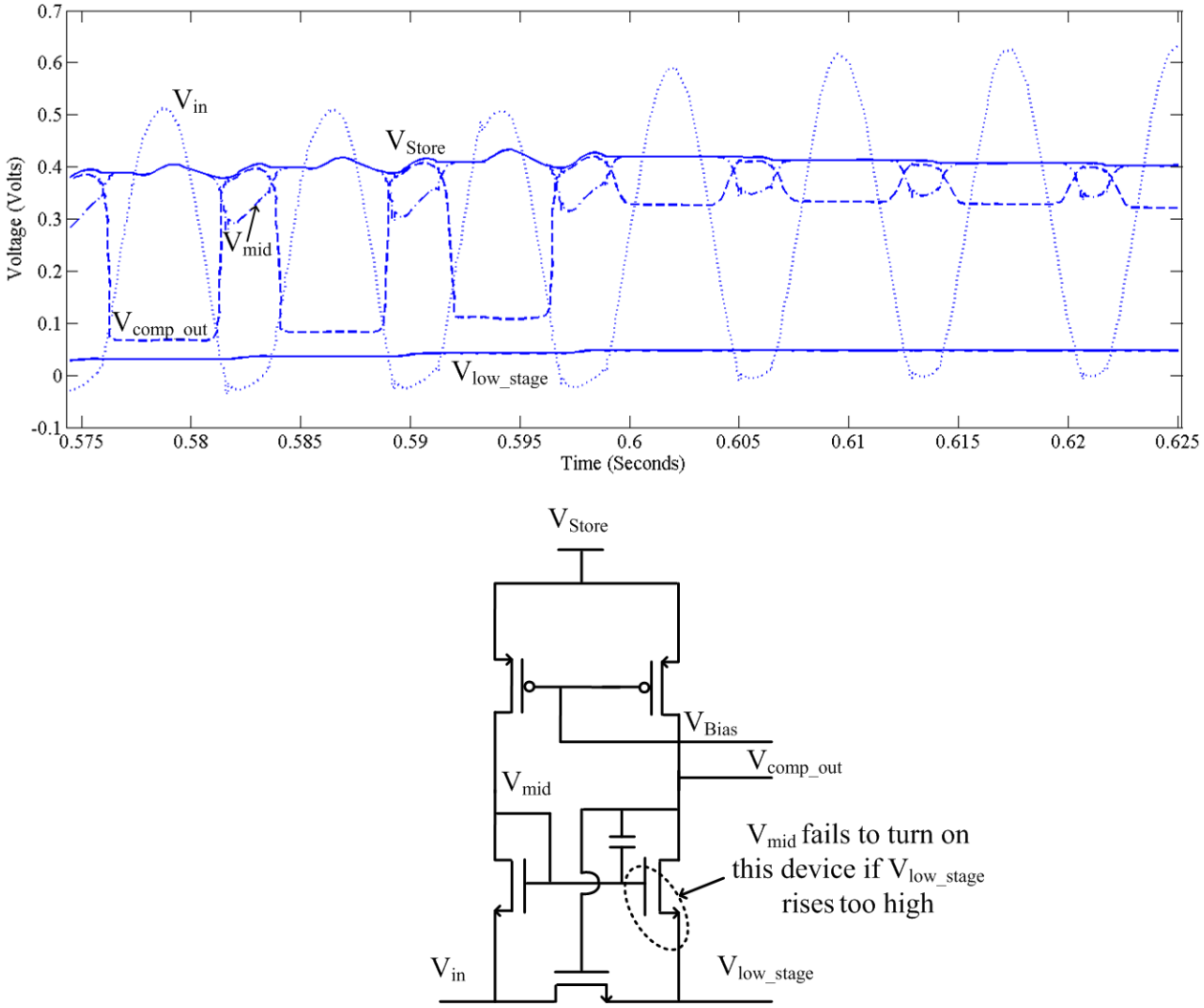

Figure 90. This shows a simulated close up of the compactor failure that occurs between 0.595 and 0.6 seconds. V_{store}, V_{mid}, V_{comp_out}, V_{low_stage} (the lowest voltage stage), and V_{in} are defined on the comparator and shown in the simulation.

the simulated comparator failure during start-up that occurs near 0.4 V. Also, for reference the comparator is included in Figure 90. V_{store}, V_{mid}, V_{comp_out}, V_{low_stage} (the lowest voltage stage), and V_{in} are defined in both the simulation and comparator. This plot shows that up until near

0.595 seconds V_{store} rises based off of the harvested input V_{in}. Around this time the lowest voltage stage V_{low_stage} rises to between 30 – 40 mV. At this point V_{comp_out} stops switching low meaning that the comparator has stopped functioning. It is interesting to note that that this failure occurs at a similar voltage as is seen in hardware from Figures 49 and 50 when the lowest voltage stage is between 30 and 40 mV. This failure where the comparator no longer functions occurs because the voltage V_{mid} that creates a V_{gs} across the device circled in Figure 90 can no longer overcome the sub-threshold turn-on requirements when V_{low_stage} rises over 30 – 40 mV.

4.8.4 Section Summary and Model to Hardware Discrepancy Discussion

This chapter shows where the comparator failure comes from as the input voltage into the comparator is unable to pull down the output of the comparator. For future designs, the first section has demonstrated that a bias that turns on earlier will certainly aid in the ability of the input into the comparator to pull down the comparators output and create a functional comparator at lower input voltages. A better biased comparator will allow the PMOS devices in Figure 90 to have a resistance that is better able to pull down the comparator output. This is easily demonstrated by externally biasing the comparator. Interestingly, the comparator functioning in the lab is very close to what is predicted in simulation. With a V_{store} near ~0.4, the comparator failure occurs when the lowest voltage stage rises to between 30 to 40 mV in both simulation and hardware. To explain the large minimum start-up differences observed between the simulated and measured results, it is likely that the passive functioning of the devices is modeled incorrectly. Specifically, it is possible that this passive functioning is modeled incorrectly while the comparator functioning is generally modeled correctly. The comparators function in a region that could be considered a “mid sub-threshold” region of operation where the devices are functioning 100 to 250 mV below the threshold of a device, while much of the

passive turn-on of the initial system or when the comparator stalls is in a region that could be considered a “deep sub-threshold” region where the devices are allowing current flow in a region 250 to 350 mV below the threshold of the devices.

Bibliography Chapter 4

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Chapter V

Conclusion

The need to power wireless structural health monitoring sensors motivated the author to investigate harvesting sources other than solar energy. Specifically, thermal, Radio Frequency (RF), and vibration harvesting sources have been investigated. Interface circuits showing the viability of vibration harvesting has been the overriding focus of this thesis. The vibrations on a major suspension bridge due to vehicles passing overhead, such as the New Carquinez Bridge in California, are considerably lower (i.e. in the 50 mg acceleration range) than what was produced to actuate other reported vibration energy harvesters. Additionally, the vibrations on a bridge are non-periodic as vehicles pass over the bridge in random traffic patterns. These non-periodic low acceleration bridge conditions motivated the design of the Parametric Frequency Increased Generator (PFIG) at the University of Michigan by Professor Khalil Najafi, Dr. Haluk Kulah, and Dr. Tzeno Galchev [1, 2]. The PFIG responded to the low voltage non-periodic vibrations on the New Carquinez Bridge; however, the PFIG produced a low voltage and low power decaying sinusoid. This output from the PFIG was extremely challenging for an interface circuit that needed to boost, rectify, and store energy at a high power conversion efficiency. Initial charge pump circuit interface attempts showed considerable challenges boosting the input signal at high efficiency and low input voltage. Not only was minimal power harvested, but initial interface circuit designs did not allow for long-term evaluation about the PFIG in an actual bridge environment.

After the initial discrete circuit attempts without transformers, harvesting interface circuits designs used a transformer-based system that investigated the limits of low voltage harvesting. Optimal efficiency with a sine-wave near 27% was observed with inputs as low as 60 mV; however, the transformer used in this new interface circuit had very limited efficiency near 66%. This limited transformer efficiency motivated alternative solutions that did not use a transformer. On the positive side, it also allowed long-term testing of the PFIG and interface circuit on the New Carquinez Bridge within the constraints of the Narada system, which did not have the power to constantly monitor the PFIG outputs. This long-test allowed understanding of the PFIG performance over 1 year and identified areas of improvement within the PFIG.

Motivated by the limited results of initial circuits designed by the author, IC-based circuits were designed with the goal of eliminating the use of the transformers in the system. Two designs were built using a ×16 and ×6 IC-based active diode charge pump. These designs were capable of a sub-threshold boosting start-up that transitions into high efficiency operation once the systems are charged. Both designs used techniques that drove the active diodes in all the stages of the charge pump by a comparator decision on the lowest voltage stage. In both cases (the ×16 and ×6 boosting charge pump designs), sub-threshold functioning was enabled using techniques to hold the lowest voltage stage near ground for as long as possible during start-up. Holding the lowest voltage stage near ground for as long as possible gave the comparators on the lowest voltage optimal margin to allow sub-threshold functioning during active deep sub-threshold start-up. The ×16 and ×6 designs use different full wave charge pump architectures that are both theoretically capable of 100% efficiency. In the ×16 and ×6 charge pump designs different techniques are used to hold the lowest voltage stage near ground for initial start-up. Both designs enable active boosting start-up with inputs <300 mV. In both designs efficiency

with an input sine-wave is over 60%, and in the ×16 circuit design efficiency can be as high as 50% with a PFIG input. Both designs use less than 0.7 µW of active power with PFIG inputs that would typically be seen on a bridge.

These circuit designs used for power management of the ultra-low power low voltage inputs from the PFIG advance the state of the art in vibration harvester interface circuits. They investigate the limits of ultra-low power low voltage designs with PFIG inputs that might be seen on a bridge and also ideal sine-wave inputs. This research demonstrates that vibration harvesting on a major suspension bridge is a viable method to power wireless bridge health monitoring sensors. It motivates further research and study into both vibration harvesters and interface circuits capable of being used on a major suspension bridge.

5.1 Thesis Contributions

Literature related to energy harvesting IC interface circuits and long-term tests of energy harvesting systems were evaluated. This is summarized in the first two thesis contributions.

1) The literature on circuits and systems capable of interfacing with vibration harvesters has been analyzed and reviewed to understand where the state-of-the art can be advanced.
2) Based on the literature survey, areas that had not been investigated were identified that are important to the development of the field. These include active boosting solutions that can cold-start using deep sub-threshold active functioning and a system's long-term performance for more than one week.

Once the literature was analyzed, a discrete transformer-based circuit was designed investigating the limits of ultra-low voltage harvesting summarized in contribution 3.

3) The limits of boosting low power and ultra-low voltage (~60 mV) harvester outputs was investigated with a passive discrete transformer-based circuit.

This transformer-based circuit that also used a discrete charge pump was able to significantly boost the ultra-low voltage PFIG outputs on the New Carquinez Bridge. This enabled short-term and long-term bridge system tests on the New Carquinez Bridge in California investigating reliability of this vibration harvesting system summarized in the following contributions.

4) This discrete transformer-based circuit was tested on the New Carquinez Bridge for short-term and long-term testing yielding valuable information on the nature of a charge pump's response to the PFIG actuated by bridge vibrations.

5) This discrete circuit enabled study of the long-term PFIG performance under bridge-like conditions showing mechanical performance issues after about six weeks of testing.

The electronics of the system enabled understanding of the long-term PFIG performance and identified a long-term failure. Analysis of the PFIG failure identified on the New Carquinez Bridge resulted in a contribution to this thesis, namely the long-term bridge data was used to narrow down the cause of the mechanical failure.

6) The long-term PFIG failure was related to the mechanism used to set the FIG position. Basically, the FIG positions slipped during operation. Fatigue lab testing showed that fatigue in the inertial mass springs is not possible in such a limited time frame leading to the final conclusion that the FIG positioning method was responsible for the decrease in power.

The transformers and discrete diodes in the transformer-based system experienced significant power losses that reduced efficiency. The transformer-based power efficiency losses motivated deep sub-threshold active diode charge pumps that eliminated the need for low power efficiency

transformers. Several contributions relating to the IC-based charge pump systems are discussed below.

7) An IC-based active diode system capable of ×6 boosting ability was designed and tested in hardware. It can produce 60% efficiency with a sine-wave, start-up with both the PFIG and sine-wave down to 280 mV, and function as low 110 mV. Advances in the state-of-the-art were identified relating to driving the active diodes from the lowest voltage stage. These advances include the system's cold start-up that uses sub-threshold functioning rather than relying on passive diodes. Also, the circuit is able to transition to regular high power conversion efficiency functioning once charged.

8) Another IC was taped out in June 2013 capable of ×16 boosting that improved sub-threshold start-up performance and low voltage operation with continued high power conversion efficiency. This design also drives the active diodes of all the stages from the lowest voltage stage; however, different circuit characteristics allow for a different mechanism to maintain optimal sub-threshold start-up performance compared to the ×6 design. It can produce 60% efficiency with a sine-wave, 50% efficiency with a PFIG input, start-up with both the PFIG down to 415 mV peak and sine-wave down to 220 mV peak, and function as low 110 mV.

9) Both the ×6 and ×16 charge pump designs showed significant differences between simulated modeled results and actual hardware results. Extensive simulations were run in Monte Carlo and in extraction, but the same minimum input voltage start-up hardware results were still not observed in these simulations. The model to hardware correlation problems point to the actual model problems used in this 180 nm CMOS design. Specifically, the model's behavior during deep sub-threshold functioning is likely incorrect. For example

minimum start-up in the ×16 design is 220 mV while simulation predicts a minimum of 335 mV. Section 4.8 shows that the "mid sub-threshold" functioning of the comparator is likely modeled correctly. This result points to the passive functioning of the charge pump devices as being incorrectly modeled. The passive functioning of the devices uses deep sub-threshold operation that is between 250 to 350 mV below the device thresholds.

10) Both ICs were tested with the PFIG at frequencies and amplitudes similar to what would be produced by the PFIG under bridge-like conditions.

To summarize the contributions from this work using the figures of merit of efficiency and minimum start-up voltage the chart, similar to Figure 14, is shown with the three works from this thesis included. This is seen in Figure 91 where the three works show lower voltage minimum start-up than the reported works from literature and comparable efficiency results.

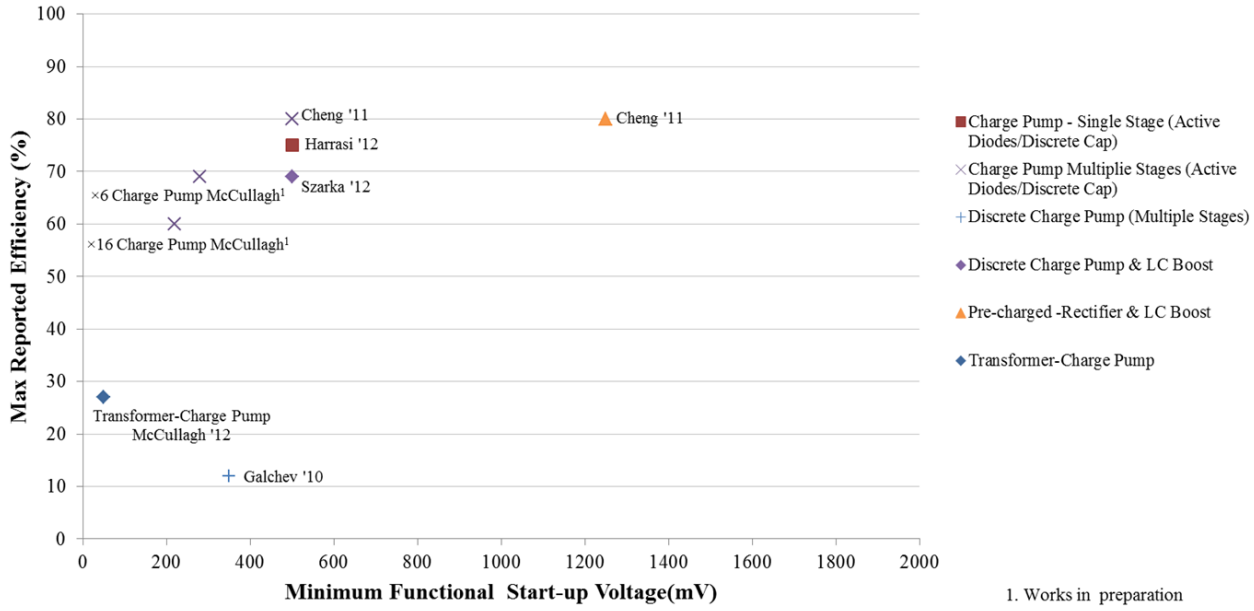

Figure 91. Building on Figure 14 this chart includes the two IC-based works and the two discrete works from this thesis. The works included here can both boost and cold-start.

5.2 Recommendations for Future Work

As discussed throughout Chapters 3 and 4, there could be continued improvement in the active diode IC-based charge pump circuits. Both Chapters 3 and 4 discussed methods to maintain high margin for sub-threshold operation in the lowest voltage stage of a charge pump. Chapter 3 discussed a lowest voltage stage driven charge pump that uses the inherent properties of a Cockcroft-Walton charge pump to allow for high margin sub-threshold start-up based on the comparator decision of the lowest voltage stage. Chapter 4 used the placement of the different types of devices, either NMOS or PMOS, to maintain a low voltage on the lowest voltage stage of a 6 stage charge pump to maintain high margin sub-threshold operation during start-up. These ideas presented in Chapters 3 and 4 could be combined to optimize a charge pump for minimum input voltage start-up operation in deep sub-threshold. The end of Chapter 4 explains this in detail.

During initial start-up, the NMOS and PMOS devices of both IC-based systems act as passive diodes allowing for limited sub-threshold current flow for start-up; however, the gates of these devices are "floating" during start-up between V_{store} and gnd. These floating gates do not optimize passive start-up. A solution that either keeps the gates close to gnd during start-up or adds helper diodes around the charge pump structure for start-up similar to Figure 6 [3] would improve this passive start-up and optimize the system in spite of "floating gates". Additionally, improvements in the bias circuitry could improve sub-threshold operation of the comparator. The bias circuit turns on when the supply "V_{Store}" in both designs is at least at one "Vth" of the given technology. Sub-threshold biasing techniques could be used to turn the bias on earlier, so that the comparator using the bias is better able to make a correct decision in deep sub-threshold.

Modeling of this technology was a constant problem during the design of both ICs. In both active diode designs, hardware results gave a minimum voltage start-up that was considerably lower than anything observed in simulation. In Chapter 4, a wide range of minimum start-up results (220 to 400 mV) were observed in hardware that were not observed in simulation. Monte Carlo and process variation simulations only predicted about a 5 mV variation in start-up. Improved modeling that accurately predicts operation and variation in deep sub-threshold could potentially improve future designs. The end of Chapter 4 discusses how modeling is incorrectly observed in deep sub-threshold where devices are operating 250 – 350 mV below the sub-threshold of the devices, while "mid sub-threshold functioning" that is 100 to 250 mV below the threshold of the devices (i.e. used for the comparator operation) tends to be modeled correctly.

The architectures in these active diode IC-based systems should be able to be used for other vibration harvesting sources including piezoelectric sources that need a boosting start-up. The main concern would be that there was enough power to provide the active diode start-up. If piezoelectric harvesters are used, care must be taken to optimize the system for the capacitive element in the piezoelectric harvesters. Some IC-based systems have gone to considerable lengths to optimize for the capacitive element and optimize efficiency [4, 5]. Similar methods may be needed to maximize start-up using this active diode architecture with piezoelectric harvesters. If the source frequency is higher, the general architectures could still be used; however, the comparators would need to be optimized for higher frequencies.

These lowest voltage stage techniques in Chapters 3 and 4 could be used on thermal harvesting start-up. Without transformers or an external switch, minimum reported thermal harvesting cold start-up is greater than 300 mV as discussed and referenced in detail in Section

1.5 (a system the can start-up with just a DC input rather than a DC input and high speed clock). Sub-threshold techniques similar to what was described in Chapters 3 and 4 using external capacitors, an IC, and a very slow generated clock (likely generated by a sub-threshold ring oscillator) could potentially create considerably lower voltage thermal harvesting start-ups than what has been reported in literature.

Finally, the long-term bridge test demonstrated problems in the performance of the PFIG. As discussed in Chapter 2, after about 6 weeks of testing, the performance of the PFIG decreased. This decrease is very likely due to a performance issue related to part of the mechanism which sets the FIG placement in the PFIG. An improved mechanical PFIG design that can better adjust the placement of the FIGs in the PFIG and would be able to tolerate a PFIG resonance condition would have the potential to last far longer in a long-term bridge-based test. In the future, an improved PFIG or PFIG like design should be retested in another long-term test on a suspension bridge to reevaluate its long-term performance.

Bibliography Chapter 5

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