LOW-TEMPERATURE ELECTRODEPOSITION OF CRYSTALLINE SEMICONDUCTOR MATERIALS

by

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DEDICATION

To my parents and my wife,

whose support and encouragement made this thesis possible.

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TABLE OF CONTENTS

DEDICATION ... ii

ACKNOWLEDGEMENTS ... iii

LIST OF FIGURES ... viii

LIST OF TABLES ... xviii

ABSTRACT ... xix

CHAPTER 1. Introduction ... 1

A. Background ... 1

i. Group IV Semiconductors and Their Applications ... 1

ii. Production Methods of Group IV Semiconductors ... 1

iii. Electrodeposition Features and Advantages ... 3

iv. Electrodeposition of semiconductors ... 4

v. Mechanisms for Crystallization ... 6

B. Approaches and Hypotheses ... 7

C. Content Description ... 11

D. References ... 14

CHAPTER 2. Electrodeposition of Crystalline Ge on Liquid Ga and its Alloys by ec-LLS Method ... 19

A. Introduction ... 19

B. Methods ... 20

C. Results ... 21

D. Discussions ... 31

E. Conclusions 33

F. References 33

CHAPTER 3. Template-Free Preparation of Crystalline Ge Nanowire Film Electrodes via an ec-LLS Process in Water at Ambient Pressure and Temperature for Energy Storage 35

A. Introduction 35

B. Methods 38

C. Results 39

D. Discussions 66

E. Conclusions 67

F. References 68

CHAPTER 4. Room-Temperature Epitaxial Electrodeposition of Single-Crystalline Germanium Nanowires 70

A. Introduction 70

B. Methods 71

C. Results 73

D. Discussions 89

E. Conclusions 91

F. References 91

CHAPTER 5. Direct Electrodeposition of Crystalline Silicon at Low Temperatures by ec-LLS 94

A. Introduction 94

B. Methods 95

C. Results 97

D. Discussions 127

E. Conclusions 128

F. References 129

CHAPTER 6. Surface Enhanced-Raman Spectroscopy for Studying Cd-VI Electrodeposition and Surface Chemistry 131

A. Introduction 131

B. Methods 132

C. Results 134

D. Discussions 144

E. Conclusions 146

F. References 146

CHAPTER 7. Conclusions and Future Work 149

A. Conclusions 149

B. Future Work 150

i. Improving Purity of the ec-LLS Deposit 150

ii. r-GO Functionalization of Au Electrode for in-situ TEM Study for ec-LLS Processes 152

iii. Studying Semiconductor Surface Chemistry by in-situ SERS and DFT Simulation 156

C. References 161

LIST OF FIGURES

Figure 1.1. Annual production of a) Si and b) Ge materials worldwide for the past decade. Data adapted from 2014 Mineral Commodity Summaries, U.S. Geological Survey. 2

Figure 1.2. Schematic depiction of the electrochemical liquid-liquid-solid growth mechanism. 8

Figure 1.3. Depiction of the waveform used in a) cyclic voltammetry and b) chronoamperometry. 10

Figure 2.1. iR-corrected current-potential response of liquid a) Ga, b) GaSn and c) GaIn electrodes in 0.1 M KNO_3, 0.01 M $Na_2B_4O_7$ aqueous solution (black) with and (red) without 0.05 M GeO_2 at 40 ^oC. The scan rate is 20 mV s^{-1} 22

Figure 2.2. Chronoamperometric response obtained from two repeated depositions of a liquid Ga electrode in 0.01 M $Na_2B_4O_7$(aq) and 0.05 M GeO_2(aq) at constant potential of -1.6 V vs. Ag/AgCl for 2 h. Inset: optical images of black deposit on the Ga electrodes before being removed from the electrochemical cell. 24

Figure 2.3. Chronopotentiometric response of a liquid Ga electrode in 0.01 M $Na_2B_4O_7$(aq) and 0.05 M GeO_2(aq) at constant current of a) 1 mA, and b) 2 mA for 2 h. Inset: optical images of the black deposit on the Ga electrodes after being removed from the electrochemical cell. 25

Figure 2.4. Optical image of Ge deposit obtained after a 10 h electrodeposition on a) liquid Ga electrode, and b) a solid Ga electrode. 27

Figure 2.5. Background-subtracted X-ray diffractogram of Ge deposit obtained on (red) liquid and (black) solid electrode of a) pure Ga, b) GaSn eutectic and c) GaIn eutectic. 28

Figure 2.6. Scanning electron micrographs of as-deposited Ge on liquid Ga at a) ×25000 and b) ×1000 magnification. ec-LLS condition: -1.6 V vs. Ag/AgCl for 2 h in 0.01 M $Na_2B_4O_7$(aq) and 0.05 M GeO_2(aq). Scale bare: 2 μm and 50 μm. 29

Figure 2.7. a) Scanning electron micrographs of as-deposited Ge highlighting a nanowire-free region. b) - e), Electron backscatter patterns of the labeled spots in a)..... 30

Figure 3.1. Schematic depiction of the electrodeposition setup for the Ge nanowire growth from an aqueous solution at ambient condition. 37

Figure 3.2. Current-potential responses for n-Si electrodes immersed in 0.01 M $Na_2B_4O_7$. Responses are shown for (dashed line) bare n-Si electrodes in electrolyte + 0.05 M GeO_2, (solid red line) n-Si electrodes decorated with In nanoparticles in electrolyte without 0.05 M GeO_2, and (solid black line) n-Si electrodes decorated with In nanoparticles in electrolyte with 0.05 M GeO_2. Scan rate = 0.025 V s^{-1} 41

Figure 3.3. Scanning electron micrographs of a) In-coated n-Si and b) bare n-Si substrate after ec-LLS growth of Ge nanowires from 0.01 M $Na_2B_4O_7$(aq) and 0.05 M GeO_2(aq), at -2.0 V vs. Ag/AgCl for 10 min. Scale bare: 500 nm. 42

Figure 3.4. a) Chronocoulometric response for an n-Si electrode coated with In nanoparticles biased at -2.0V vs. Ag/AgCl for 10 min while immersed in 0.01 M $Na_2B_4O_7$(aq) and 0.05 M GeO_2(aq) after subtraction of the background faradaic charge for H^+ reduction. b) Raw (uncorrected) chronoamperometric responses for (black line) a bare n-Si electrode and (red line) an n-Si electrode coated with In nanoparticles in 0.01 M $Na_2B_4O_7$ and 0.05 M GeO_2 biased at -2.0 V vs. Ag/AgCl for 10 min. c) Corrected current transient with current normalized to the peak current density and time normalized to the time corresponding to the peak current density. Models for (blue line) instantaneous and (black line) progressive nucleation models are also shown.. 43

Figure 3.5. Measured X-ray diffraction pattern collected after Ge electrodeposition at -2.0 V vs. Ag/AgCl for 1 h.. 45

Figure 3.6. a) Low magnification transmission electron micrograph of an individual Ge nanowire electrodeposited at -2.0 V vs. Ag/AgCl for 10 min. Scale bar: 50 nm. b), c) High resolution transmission electron micrographs of the same Ge nanowire as in a). Scale bar: 10nm, 5 nm.. Inset: selected area electron diffraction pattern taken over the area shown in b)... 46

Figure 3.7. Top-down view scanning electron micrographs of n-Si electrodes decorated with different densities of In nanoparticles a)-d) before and e)-h) after Ge electrodeposition at -2.0 V vs. Ag/AgCl for 10 min... 48

Figure 3.8. a) Comparison of the observed density of Ge nanowires as a function of the observed density of In nanoparticles on n-Si electrodes. Dashed line corresponds to 1 Ge nanowire per 1 In nanoparticle. b) Observed size distribution of In nanoparticles at several different In nanoparticle densities, as indicated in a). c) Size distribution of Ge nanowires electrodeposited from In nanoparticles at the four different densities of In nanoparticles shown in b). Bin sizes in b) and c) are 5 nm. 49

Figure 3.9. Scanning electron micrograph of Ge nanowires electrodeposited with an n-Si electrode with large In nanoparticles. Scale bar: 200 nm.. 51

Figure 3.10. Plan-view scanning electron micrographs of Ge nanowires electrodeposited at -2.0 V vs. Ag/AgCl for a) 1 min, b) 10 min, c) 1 hr, and d) 12 hr. e)-g) Corresponding cross-sectional scanning electron micrographs showing the film thickness.................... 52

Figure 3.11. Scanning electron micrographs showing the In-coated Si substrate a) before and b) after being biased in 0.01 M $Na_2B_4O_7$ buffer at -2.0 V for 10 min. c) Histogram showing the diameter distribution of the nanoparticles shown in a) and b). 53

Figure 3.12. a) Secondary electron scanning electron micrograph of an individual Ge nanowire electrodeposited at -2.0 V vs. Ag/AgCl for 10 min. b), c) Energy dispersive spectroscopic elemental mapping of same area in a) with the detector channel for b) the *L* line for Ge or c) the *M* line for In. Images were collected with the sample tilted at 45°. Scale bars: 500 nm. Arrows highlight features of interest as discussed in the text. 55

Figure 3.13. a) Optical image showing a Cu electrode support before and after Ge nanowire film electrodeposition. b) Optical image of a Swagelok battery test cell used for the capacity measurement. 57

Figure 3.14. a) First, second, third, and twenty-sixth charge-discharge curves for a Li^+ anode recorded at 1C rate using an as-prepared Ge nanowire film electrodeposited onto a Cu support from 0.01 M $Na_2B_4O_7$(aq) and 0.05 M GeO_2(aq). b) Galvanostatic Li^+ (black squares) charge and (red circles) discharge cycling at 1C rate using an as-prepared Ge nanowire film electrodeposited onto a Cu support from 0.01 M $Na_2B_4O_7$(aq) and 0.05 M GeO_2(aq). (blue triangles) The coulombic efficiencies for each charge-discharge cycle are indicated on the right y-axis.. 58

Figure 3.15. a) Scanning electron micrographs of Ge nanowires electrodeposited on In-coated Cu electrodes. In catalysts were electrodeposited at -2.0 V for 30 sec from 0.1 M $InBr_3$, 0.1 M KNO_3 and Ge nanowires were subsequently electrodeposited at -2.0 V for 1 hr from 0.05 M GeO_2, 0.01 M $Na_2B_4O_7$. b) Scanning electron micrograph showing the same electrode after charge-discharge cycling at 1 C rate for 20 cycles. 59

Figure 3.16. Li^+ charge and discharge capacities at 1C rate as a function of repetitive cycling for 1) bare Cu substrate, 2) In-coated Cu substrate and 3) Ge nanowires film on In-coated Cu substrate... 60

Figure 3.17. Twentieth charge-discharge curves for (top) an as-prepared Ge nanowire film electrodeposited onto a Cu electrode, (middle) a bare Cu electrode, and (bottom) a Cu electrode coated with In nanoparticles. 64

Figure 3.18. Li^+ charge and discharge capacities at 5C rate as a function of repetitive cycling for three separately prepared Ge nanowire film electrodes. Ge nanowires were

electrodeposited at -2.0 V for 1 hr from 0.05 M GeO_2, 0.01 M $Na_2B_4O_7$ for all three electrodes. 65

Figure 4.1. a) Optical image depicting the benchtop experimental setup used for wafer-scale ec-LLS of Ge nanowire films. Insets: Schematic depiction of ec-LLS process. b) Cyclic voltammetric response of an n-Ge(111) electrode (R = 24.8 – 30 Ω·cm) decorated with (blue) and without (black) Ga(l) nanodroplets in 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$. The current-potential behavior for the same Ga(l) decorated n-Ge(111) electrode in the absence of dissolved GeO_2 is shown in red. c) Optical image of a 2-inch wafer coated with Ge nanowires after 300 s ec-LLS nanowire deposition over the bottom half of the wafer. d) Scanning electron micrograph collected from Ge nanowires grown for 30 s from a Ge(111) substrate. Scale bar: 1 μm. ec-LLS conditions: E_{app} = -1.6 V vs. Ag/AgCl, T = 40 ± 2°C, 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$.. 75

Figure 4.2. Cross-sectional scanning electron micrograph of a Ge(111) substrate decorated with discrete liquid Ga nanodroplets a) before and b) after a 30 s ec-LLS process. Scale bar: 500 nm. c) 40 ^{o} tilted scanning electron micrograph of the same substrate c) before and d) after a 30 s ec-LLS process. Scale bar: 1 μm. e) Size distribution of the Ga nanodroplet electrodes and resultant Ge nanowire base widths obtained after a 30 s ec-LLS experiment. f) Cross-sectional high resolution transmission electron micrograph of an as-prepared single Ge nanowire on a wafer substrate produced after a 30 s ec-LLS. Scale bar: 100 nm. g) Energy dispersive X-ray spectroscopic elemental map of the structure in (f). ec-LLS conditions: E_{app} = -1.6 V vs. Ag/AgCl, T = 40 ± 2°C, 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$. 77

Figure 4.3. a) Chronoamperometric response for an n-Ge(111) electrode coated with Ga(l) nanodroplets in 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$ biased at -1.6 V vs. Ag/AgCl for 300 s. Inset highlights the first 10 s of the current profile. b) Same current-transient data with current density normalized to the peak current density and time normalized to the time with maximal current (triangle). Models for progressive (blue line) and instantaneous (black line) nucleation models are also shown. c) Cross-sectional scanning electron micrograph of Ge nanowires grown for 30 s at -1.6 V vs. Ag/AgCl. Scale bar: 500 nm. d) Corresponding histogram of Ge nanowire heights (N = 196) after 30 s extracted from SEM images... 78

Figure 4.4. Scanning electron micrographs showing Ge nanowire orientations grown from various electrode substrates. a) Cross-sectional view and b) top-down (plan) view of Ge nanowire films prepared through a 30 s ec-LLS experiment on an n^+-Ge(111) electrode substrate. Scale bar: 500 nm. Insets: possible orientation for nanowire growth along any <111> direction from a (111) substrate. c) A high resolution transmission electron micrograph cross-sectional view of the interface between the base of a Ge nanowire prepared by ec-LLS and the n^+-Ge (111) substrate viewed along the [110] zone

axis. Scale bar: 5 nm. Inset: selected area electron diffraction pattern collected over the nanowire/substrate interface. d) Cross-sectional view and e) plan view of Ge nanowire films prepared through a 30 s ec-LLS experiment on a degenerately doped n^+-Ge(100) electrode substrate. Scale bar: 500 nm. Insets: possible orientation for nanowire growth along any <111> direction from a (100) substrate. f) Cross-sectional view and g) plan view of Ge nanowire films prepared through a 30 s ec-LLS experiment on a degenerately doped n^+-Si(100) electrode substrate. Scale bar: 200 nm. Insets: possible orientation for nanowire growth along any <111> direction from a (100) substrate. ec-LLS conditions: E_{app} = -1.6 V vs. Ag/AgCl, T = 40 ± 2 °C, 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$.............. 80

Figure 4.5. a) Cross-sectional scanning electron micrograph of Ge nanowires grown from n-Ge(111) electrode biased at -1.6 V in a solution of 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$ for 60 s. Scale bar: 500 nm. b) Corresponding height histogram of Ge nanowires grown from Ge(111) substrates prior to the first kink (N = 102). 82

Figure 4.6. a) Transmission electron micrograph of a Ge nanowire prepared with a 300 s ec-LLS experiment. Scale bar: 100 nm (b-f) High resolution transmission electron micrographs for the corresponding boxed regions in (a). Scale bar: 2 nm. Insets: selected area electron diffraction patterns of the corresponding region. g) Schematic depiction of the crystal growth process of the nanowire, highlighting the formation of stacking faults and kinking of the nanowire. ec-LLS conditions: E_{app} = -1.6 V vs. Ag/AgCl, T = 40 ± 2 °C, 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$. 84

Figure 4.7. a) Plan-view scanning electron micrograph of a Ge nanowire film prepared with a 300 s ec-LLS experiment. Scale bar: 2 μm. b) Distribution of the Ge nanowire orientations from plan view images (as in (a)) after the first kink. Insets: Schematic of the expected orientations for nanowire growth along the <111> family. ec-LLS conditions: E_{app} = -1.6 V vs. Ag/AgCl, T = 40 ± 2 °C, 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$.............. 85

Figure 4.8. (a) Plan-view scanning electron micrograph of Ge nanowires grown on n-Ge(111) coated with Ga(l) nanodroplets biased at -1.6 V for 300 s during vigorous solution convection. Scale bar: 1μm. b) Corresponding histogram of nanowire growth orientations normalized to 0 ^{O} (N = 116). c) Plan-view scanning electron micrograph of Ge nanowires electrodeposited galvanostatically at 5 μA for 1 hr from 0.001 M GeO_2 and 0.01 M $Na_2B_4O_7$, 0.1 M KNO_3 on n-Ge(111) coated with Ga(l) nanodroplets. Scale bar: 1 μm. d) Corresponding histogram of nanowire growth orientations normalized to 0 ^{O} (N = 191). (e) Plan-view scanning electron micrograph of Ge nanowires grown on n-Ge(111) coated with electrodeposited Ga(l) nanodroplets biased at -1.6 V for 300 s. Scale bar: 1 μm. (f) Corresponding histogram of nanowire growth orientations normalized to 0 ^{O} (N = 235). 86

Figure 4.9. a) Schematic depiction of the conductive atomic force microscopic (c-AFM) measurement performed on (*1*) intact Ge nanowires after 30 s growth, (*2*) laterally fractured Ge nanowires and (*3*) oxide-free Ge substrate. b) Current-voltage response in c-AFM measurement for *1-3* near zero voltage region. Current-voltage responses measured by conductive atomic force microscopy across (c) an intact, as-grown, Ge nanowire on an n^+-Ge substrate, (d) a fractured Ge nanowire and (e) the oxide free n^+-Ge substrate. ec-LLS conditions: E_{app} = -1.6 V vs. Ag/AgCl, T = 40 ± 2 °C, 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$. 88

Figure 5.1. Schematic depiction of the ec-LLS process for electrodepositing crystalline Si from dissolved $SiCl_4$ in propylene carbonate on liquid Ga electrode........ 98

Figure 5.2. Cyclic voltammetric response of a Ga(l) electrode in propylene carbonate containing 0.2 M TBAC and various concentrations of $SiCl_4$ (0 mM, 50 mM, 100 mM to 500 mM) at room temperature under N_2 (g) both a) before and b) after correction for iR drop in solution. Scan rate = 0.025 V s^{-1}. Nyquist plot of impedance response of a Ga(l) electrode in propylene carbonate containing 0.2 M TBAC at open circuit potential (-0.96 V vs. Pt QRE) at room temperature for c) full frequency range, d) high frequency range. 101

Figure 5.3. Cyclic voltammetric response of a Ga(l) electrode in propylene carbonate containing 0.2 M TBAC (red) with and (black) without 0.5 M of $SiCl_4$ at 100 °C and 2.76 MPa, under Ar (g) both a) before and b) after correction for iR drop in solution. Scan rate = 0.025 V s^{-1}........ 102

Figure 5.4. a) Optical photograph of a clean Ga(l) working electrode. b) Optical photograph of the same electrode after galvanostatic electrodeposition of Si in propylene carbonate containing 0.2 M TBAC and 0.5 M $SiCl_4$ at 20 mA cm^{-2} for 2 h at 100 °C. c) Optical photograph of a Ga(l) electrode exposed to 0.5 M $SiCl_4$ and 0.2 M TBAC in propylene carbonate at 100 °C and 2.76 MPa at open circuit potential for 2 h. Images c) and d) were obtained after physical removal from the cell........ 103

Figure 5.5. a) Optical photograph of the as-deposited Si powder immediately after purification. b) Optical image of the same Si powder after being stored in lab ambient for 30 days. 105

Figure 5.6.a) X-ray diffractograms of as-deposited Si powder before and after being etched with 5 % w/w HF solution for 30 s, along with the diffraction background from the glass slide support. The latter was used for background correction. b) Background-corrected X-ray diffractogram of the etched Si powder. c) Raw X-ray diffractogram of the same etched Si powder measured using a 50 μm point-focus X-ray source. The Si sample was galvanostatically deposited in a propylene carbonate solution of 0.2 M

tetrabutylammonium chloride (TBAC) and 0.5 M of $SiCl_4$ with current density of 20 mA cm^{-2} for 2 h at 100 ^oC and 2.76 MPa pressure. 106

Figure 5.7. Scanning electron micrographs of electrodeposited Si at a) 20 000× and b) 80 000× times magnification. c) High-resolution transmission electron micrograph of electrodeposited Si at 800 000× magnification. Inset: selected area electron diffraction pattern obtained with the electron beam parallel to the [011] zone axis. Crystalline Si was electrodeposited in a propylene carbonate solution containing 0.2 M TBAC and 0.5 M $SiCl_4$ at 20 mA cm^{-2} for 2 h at 100 °C and 2.76 MPa pressure. As-deposited Si was etched in 5% HF solution for 30 s prior to electron microscopy analysis. 107

Figure 5.8. a) Energy dispersive energy spectrum of a Si sample taken in the scanning electron microscope at 15 kV. b) and c) Energy dispersive energy spectra of two different crystallites from a same sample taken in the transmission electron microscope at 300 kV. Crystalline Si was electrodeposited in a propylene carbonate solution containing 0.2 M TBAC and 0.5 M $SiCl_4$ at 20 mA cm^{-2} for 2 h at 100 °C and 2.76 MPa pressure. As-deposited Si was etched in 5% HF solution for 30 s prior to electron microscopy analysis. 109

Figure 5.9. a) A plot of the collected electrodeposited mass as a function of electrodeposition time. Each point represents a separate electrodeposition experiment. b) Representative chronopotentiometric response of the Ga(l) electrode during a 2 h galvanostatic electrodeposition at 20 mA cm^{-2} current density at 100 ^oC and 2.76 MPa pressure in a propylene carbonate solution containing 0.2 M TBAC and 0.5 M $SiCl_4$. . 110

Figure 5.10. a) Optical micrograph of the white/transparent film obtained at the Ga(l) electrode surface after a 2 h electrodeposition at 20 mA cm^{-2} current density at 100 ^oC and 2.76 MPa pressure. b) Energy dispersive energy spectrum of the isolated film taken in the scanning electron microscope at 15 kV. 111

Figure 5.11. Optical image showing the deposit from a dual working electrode experiment.. 113

Figure 5.12. Optical micrographs of Si deposits obtained after 1 h electrodeposition at -2.5 V vs. Pt QRE at 100 ^oC and 2.76 MPa pressure in a propylene carbonate solution containing 0.2 M TBAC and a) 500 mM, b) 50 mM and c) 5 mM $SiCl_4$. Optical micrographs of Si deposits obtained after 1 h electrodeposition at 100 ^oC and 2.76 MPa pressure in a propylene carbonate solution containing 0.2 M TBAC and 50 mM $SiCl_4$ at d) -1.5 V, e) -2.0 V, f) -2.5 V), and g) -3.0 V vs. Pt QRE 114

Figure 5.13. a) X-ray diffractograms of etched Si powder deposited in a propylene carbonate solution of 0.2 M TBAC and 0.5 M of $SiCl_4$ with current density of 20 mA cm^{-2} for 2 h at 100 ^oC and ambient pressure. b) X-ray diffractograms of etched Si powder

deposited in a propylene carbonate solution of 0.2 M TBAC and 0.5 M of $SiCl_4$ with current density of 20 mA cm^{-2} for 2 h at 80 ^oC and 2.76 MPa pressure. c) Optical photograph of the room temperature deposit after being heated to 100 °C for 2 h inside the cell under Ar(g). 116

Figure 5.14. Scanning electron micrographs of Si electrodeposited at -2.5 V vs. Pt QRE in a propylene carbonate solution of 0.2 M TBAC and 50 mM of $SiCl_4$ at a) 120 ^oC, b) 140 ^oC, 160 ^oC, and 2.76 MPa pressure for 1 h. For c), the Ga(l) electrode was biased at initial open circuit potential value during temperature ramp to minimize Ga surface oxidation. Scale bar: 2μm. 118

Figure 5.15. a) Raman spectra of as-deposited Si obtained on the Ga(l) electrode after electrodeposition at -2.5 V vs. Pt QRE in a propylene carbonate solution of 0.2 M TBAC and 50 mM of $SiCl_4$ at temperatures from 100 ^oC to 200 ^oC, and at 2.76 MPa pressure for 1 h. b) High wavenumber region of the Raman spectrum for an as-electrodeposited Si sample prepared by galvanostatic electrodeposition in a propylene carbonate solution of 0.2 M TBAC and 0.5 M of $SiCl_4$ at 20 mA cm^{-2} for 2 hr at 100 oC and 2.76 MPa pressure. 119

Figure 5.16. a) X-ray diffractograms and b) Raman spectra of Si deposit annealed at various temperatures up to 300 ^oC for 30 min at each temperature point. The starting Si sample was prepared by galvanostatic deposition with current density of 20 mA cm^{-2} for 2 hr in propylene carbonate containing 0.2 M TBAC and 0.5 M of $SiCl_4$ h at 100 ^oC and 2.76 MPa pressure.. 120

Figure 5.17. Scanning electron micrographs of Si deposit a) before annealing, after being annealed at b) 150 ^oC, c) 200 ^oC, d) 250 ^oC, and e) 300 ^oC for 30 min at each temperature point. Scale bar: 500 nm. The starting Si sample was prepared by galvanostatic deposition with current density of 20 mA cm^{-2} for 2 hr in propylene carbonate containing 0.2 M TBAC and 0.5 M of $SiCl_4$ at 100 ^oC and 2.76 MPa pressure.............................. 122

Figure 5.18. High angle annular dark field images of Si deposit a) before annealing, after being annealed *in situ* at b) 200 ^oC, c) 300 ^oC, for 5 min at each temperature point and d) after cooling down to room temperature. The starting Si sample was prepared by potentiostatic deposition at -2.5 V vs. Pt QRE for 1 hr in propylene carbonate containing 0.2 M TBAC and 0.5 M of $SiCl_4$ at 100 ^oC and 2.76 MPa pressure.............................. 123

Figure 5.19. High angle annular dark field images of Si deposit a) before annealing, after being annealed *in situ* at b) 235 ^oC, c) 240 ^oC, and d) 245 ^oC for 5 min at each temperature point. High angle annular dark field images of Si deposit after being annealed *in situ* at 240 ^oC for e) 5 min, f) 6 min, g) 7 min and 8) min. Scale bar: 200nm. The starting Si sample was prepared by potentiostatic deposition at -2.5 V vs. Pt QRE for

1 hr in propylene carbonate containing 0.2 M TBAC and 0.5 M of $SiCl_4$ at 100 ^oC and 2.76 MPa pressure.. 125

Figure 5.20. a) High angle annular dark field image, b) Si K line map and c) Ga L line map of Si deposit without thermal annealing. Scale bare: 100 nm. d) High angle annular dark field image, e) Si K line map and f) Ga L line map of Si deposit after being annealed at 300 ^oC for 30 min. Scale bar: 500 nm. The starting Si sample was prepared by galvanostatic deposition with current density of 20 mA cm^{-2} for 2 hr in propylene carbonate containing 0.2 M TBAC and 0.5 M of $SiCl_4$ at 100 ^oC and 2.76 MPa pressure. 126

Figure 6.1. *Ex-situ* SERS spectra of multilayer CdSe dry films with increasing thickness acquired under a) 785 nm and b) 647 nm laser excitation with 1.1 mW power. Se monolayer was electrodeposited at -0.85 V for 3 min in 5 mM SeO_2, 10 mM $Na_2B_4O_7$, 100 mM Na_2SO_4. Cd monolayer was electrodeposited at -0.7 V for 3 min in 1 mM $CdSO_4$, 100 mM Na_2SO_4. Each spectrum was acquired for 10 sec and the spectra where normalized and offset for clarity.. 135

Figure 6.2. *In-situ* SERS spectra of Cd electrodeposition on Se monolayer at Au nanoparticle electrode acquired under a) 785 nm and b) 647 nm laser excitation with 1.1 mW power. Se monolayer was first electrodeposited *ex situ* at -0.85 V for 3 min in 5 mM SeO_2, 10 mM $Na_2B_4O_7$, 100 mM Na_2SO_4. The spectra were taken after the electrode was biased at the designated potential for 1 min. Each spectrum was acquired for 10 sec and the spectra where normalized and offset for clarity... 136

Figure 6.3. *In-situ* SERS spectra of Cd electrodeposition on Se monolayer at Au nanoparticle electrode acquired under a) 785 nm and b) 647 nm laser excitation with 1.1 mW power. Se monolayer was first electrodeposited *ex situ* at -0.85 V for 3 min in 5 mM SeO_2, 10 mM $Na_2B_4O_7$, 100 mM Na_2SO_4. The spectra were taken after the electrode was biased at the designated potential for 1 min. Each spectrum was acquired for 10 sec and the spectra where normalized and offset for clarity... 138

Figure 6.4. a) and b) Time-dependent SERS spectra of Se monolayer in 10 mM $CdSO_4$, 100 mM Na_2SO_4 at open circuit potential taken at two different spot on same electrode. Spectra were acquired under 4.3 mW, 633 nm excitation with 2 sec exposure. Time-dependent SERS spectra of Se monolayer in 10 mM $CdSO_4$, 100 mM Na_2SO_4 at c) open circuit potential, d) -0.7 V. Spectra were acquired under 4.0 mW, 785 nm excitation with 10 sec and 1 sec laser exposure, respectively. 139

Figure 6.5. Time-dependent SERS spectra of Te monolayer in 1 mM $CdSO_4$, 100 mM Na_2SO_4 at -0.5 V. Spectra were acquired a) under 4.0 mW, 785 nm excitation with 10 sec exposure, b) 4.3 mW, 633 nm excitation with 10 sec exposure. Te monolayer was

first electrodeposited *ex situ* at -0.4 V for 3 min in 0.5 mM TeO_2, 10 mM $Na_2B_4O_7$, 100 mM Na_2SO_4. 141

Figure 6.6. Time-dependent SERS spectra of Cd monolayer biased at -0.35V in 0.5 mM TeO_2, 10 mM $Na_2B_4O_7$, 100 mM Na_2SO_4 under a) 4.3 mW, b) 30.4 mW laser illumination, c) 4.3 mW illumination after the sample was illuminated with 30.4 mW power laser for 2 min, d) 4.3 mW illumination at a new location on the same electrode. All spectra were taken under 785 nm laser excitation. Cd monolayer was first electrodeposited *ex situ* at -0.7 V for 3 min in 1 mM $CdSO_4$, 100 mM Na_2SO_4. 142

Figure 6.7. a) SERS spectra of benzenethiol adsorbed on bare Au, CdTe, CdSe and CdS monolayer. b) Surface vibration region of the SERS spectra of adsorbed benzenethiol on bare Au and CdTe monolayer. c) Molecular vibration region of the SERS spectra of adsorbed benzenethiol on bare Au, CdTe, CdSe and CdS monolayer. The spectra were collected at 785 nm laser excitation, 1.1 mW power with 10 sec exposure. Spectra were offset for clarity.. 143

Figure 7.1. Scanning electron micrograph of Au electrode a) before and b) after Ga electrodeposition. Energy dispersive X-ray spectroscopy of the Au electrode c) before and d) after Ga electrodeposition. 154

Figure 7.2. Scanning electron micrograph of the Au electrode surface after sequential electrodeposition of a) r-GO thin film, b) Ga nanodroplet and c) Ge nanowire............ 155

Figure 7.3. Potential dependence of the Raman vibrational modes of adsorbed benzenethiol at CdTe surface highlighting a) the surface vibration region and b) the molecular vibration region. c) Qualitative depiction of the ligand-to-metal charge transfer magnitude (red arrow) under different external biases. 159

Figure 7.4. Schematic depiction of the Cd-VI-benzenethiol cluster model used for DFT calculation (Cd = blue, VI = orange). b) Computed static dipole moment and dynamic dipole moment for Cl, Li, 4-methoxybenzenethiol (MOBT) and 4-trifluoromethyl benzenethiol (TFMBT) on Au clusters. 160

LIST OF TABLES

Table 3.1. Reported Discharge Capacity for Ge Li^+ Insertion Anodes[a] 61

Table 3.2. Measured Li^+ charge and discharge capacity for Ge nanowires film electrodes[a] 62

Table 5.1. Solubility of Si in Ga as a function of temperature... 99

ABSTRACT

Crystalline group IV semiconductor materials, silicon (Si) and germanium (Ge) are essential building blocks in energy conversion, storage and optoelectronic devices. The state-of-art material synthetic methods fail to offer a non-energy-intensive solution for producing crystalline group IV semiconductor materials using easy-to-access apparatuses under ambient conditions. The primary aim of this thesis is to develop a cost-effective synthetic method, namely electrochemical liquid-liquid-solid (ec-LLS) growth, for preparing these materials at low temperatures using simple instruments and chemicals. The key innovation of the ec-LLS approach is the utilization of liquid metal electrodes in an electrodeposition process, during which the liquid metal serves simultaneously as a conductive substrate for current flow and as a solvent phase for semiconductor crystallization. The unique combination of electrodeposition and liquid-phase crystallization in this strategy opens new possibility for low temperature preparation of crystalline group IV semiconductors.

This thesis will test a few key hypotheses regarding the fundamental and practical aspects of ec-LLS. Chapter 2 focuses on the Ge electrodeposition on liquid pool electrodes with various compositions to demonstrate the versatility of the ec-LLS approach. The significant role of liquid metal electrodes in the crystal formation process will be highlighted by the X-ray diffraction data. Chapter 3 expands the application of ec-LLS strategy to the controlled electrodeposition of Ge nanowires using nano-sized growth catalyst. As-deposited Ge nanowires will also be tested as Li^+ battery anodes without further processing. Chapter 4 details the direct epitaxial growth of single-crystalline Ge nanowires at room temperature by the ec-LLS approach. Discrete Ga nanoparticles will be used as the seeding catalyst for the Ge nanowire growth on a single crystal Ge wafer. Electron microscopy evidence supporting the notion of epitaxial growth will be presented. Chapter 5 demonstrates the application of ec-LLS strategy for electrodeposition of crystalline Si at temperature as low as 80 ^{o}C from an organic

electrolyte. $SiCl_4$ precursor in propylene carbonate will be electrochemically reduced onto liquid Ga pool electrode to form high-coverage elemental Si. In summary, the collected results from this thesis will endorse ec-LLS as a non-energy-intensive synthetic method for producing crystalline group IV semiconductor materials.

CHAPTER 1

Introduction

A. Background

i. Group IV Semiconductors and Their Applications

Since the discoveries of semiconducting effects in 1830s[1,2], semiconductor materials have served as integral components in numerous fields of modern day technology, including energy conversion[3,4], information technology[5], lighting and display[6,7]. In the year 2012, the annual sales from semiconductor industry reached $299.9 billion worldwide.[5] Among various types of semiconductor materials, group IV semiconductors, namely Si and Ge, are of particular practical interest due to their essential roles in solar energy conversion[3,4,8], electronics[5,9] and sensor[10,11] industry. As in 2008, crystalline Si photovoltaic cells hold a dominating 90 % percent share of the world total photovoltaic cell production.[12] Recent development in semiconductor nanomaterials has unveiled further potentials of nanostructured Si and Ge in next generation solar energy conversion[13,14], energy storage[15,16] and microelectronic[17-19] devices. For example, due to improved light absorption[20,21], charge extraction[22,23] and defect tolerance[24] properties, Si nanowires have been of intense research interest for enhancing current device performance for current photovoltaics[13,14,24,25]. In the field of microelectronics, novel architecture for nanostructured Si[17,19] and Ge[26] are being investigated, driven by the continuous miniaturization of logic and memory components. Si[16,27,28] and Ge[29,30] nanomaterials are also considered to be viable candidates as anode materials in Li ion battery for energy storage purpose.

ii. Production Methods of Group IV Semiconductors

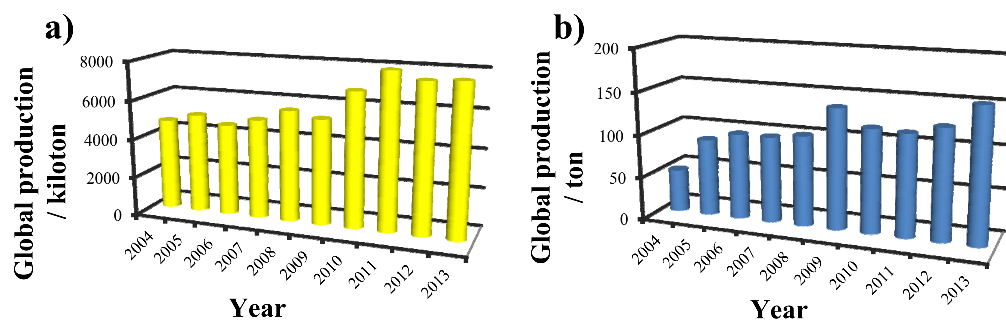

Figure 1.1. Annual production of a) Si and b) Ge materials worldwide for the past decade. Data adapted from 2014 Mineral Commodity Summaries, U.S. Geological Survey.

The apparent practical importance of group IV semiconductors gives rise to massive production demand for crystalline Si and Ge. According to recent statistics from U.S. Geological Survey, the global production of Si and Ge materials reached 7700 kt and 155 t, respectively in 2013 (Figure 1.1). However, the conventional protocol for producing crystalline group IV semiconductors at such grand scales heavily relies on energy-intensive processes. Taking bulk Si wafer as an example, the production process comprises of a series of energy-demanding steps, including hydrothermal reduction of quartz (50 kWh/kg), reduction of trichlorosilane to polycrystalline-Si (200 kWh/kg), and Czochralski growth of monocrystalline-Si ingot (100 kWh/kg).[31] The related cost of these processing steps contributes up to 50 % of the total cost of Si solar cell.[24] In the case of nanostructured Si and Ge, typical preparation methods include vapor-based techniques such as chemical vapor deposition[17], molecular beam epitaxy[32], laser ablation[33] and solution-based synthetic techniques[34]. Although these methods represent the state-of-art strategies for producing crystalline semiconductor nanomaterials, they bear a few undesirable properties as material preparation methods, such as high processing temperatures, nontrivial setup (i.e. vacuum/heating systems, high-power sources, etc.) and complex reagents. The need to reduce energetic and financial cost, to minimize instrumental complexity has motivated the search for alternative synthetic strategies for semiconductor materials.

iii. Electrodeposition Features and Advantages

Electrochemical deposition is a versatile material synthetic method that offers a cost-effective solution for preparing semiconductor material.[35,36] Initially developed in early 19th century for the purpose of metal plating[37], the field of electrodeposition has witnessed expansion far beyond its original scope. A wide variety of materials can now be prepared by electrodeposition with great flexibility, the list of which includes but is not limited to metals[38,39], ceramics[40,41], semiconductors[36,42] and even polymers[43,44]. The popularity of electrodeposition stems from its unique combination of several advantages desired for material synthesis. 1) Low operational temperature. With a few exceptions using high temperature molten salts[45,46], electrodeposition is typically carried out at room temperature or moderately elevated temperatures below the boiling point or

decomposition temperature of the solvent. The preparation temperature is thus a few hundred degrees lower comparing to average temperature used for conventional vapor phase synthetic methods. Such low temperature synthetic strategy is beneficial for reducing energy consumption and environmental footprint. 2) Simple setup. Electrodeposition can be implemented with only benchtop apparatuses; in principle, beakers, electrodes, precursor-containing electrolytes and battery sources. Carried out at low temperature and ambient pressure conditions, electrodeposition does not rely on high temperature furnaces or vacuum systems, effectively minimizing the instrumental complexity and maintenance cost. 3) Scalability. Using convenient and inexpensive setup, electrodeposition has been adopted for large scale material production in industry. For example, beginning in 1990s, Cu electrodeposition for multilevel interconnections has been accepted for mainstream Si chip processing[47]. 4) Flexibility. During an electrodeposition process, the kinetics and thermodynamics of nucleation and crystal growth are directly determined by the applied current and electrochemical potential[38]. As a result, product composition, quantity and morphology can all be controlled with high accuracy by varying the electrochemical parameters in the experiment[38,40]. These advantages are particularly beneficial for the preparation of semiconductor materials, since various semiconductor properties such as band-gap, dopant type and doping density can be effectively tuned[48]. 5) Easy precursor preparation. Most Electrodeposition is a one-step process directly utilizing common soluble ions or oxides as precursors. This avoids additional processes either for preparing target materials in rf-sputtering and pulse laser deposition[40] or for synthesizing molecular precursors in metalorganic chemical vapor deposition[49], thus greatly improving the overall throughput of this method.

iv. Electrodeposition of semiconductors

For semiconductor preparation, electrochemical deposition has been successfully applied to the most common categories of semiconductor materials including metal oxides (ZnO[50,51], Cu_2O[51,52]), II-VI semiconductors (CdTe[53,54], CdS[55], ZnTe[56,57], Zones[58]), III-V semiconductors (GaAs[59,60], InAs[61], InSb[62]). Typically, the electrodeposition is carried out in one pot for binary semiconductor using an electrochemical bath containing both precursor ions simultaneously. The stoichiometry of the product is controlled by pH

value, precursor concentrations as well as the applied electrochemical conditions.[53,55-58,60,62] The same technique can also be applied for more complex semiconductor such as $CuInSe_2$[63] and $Cu(Ga,In)Se_2$[64]. Alternatively, single crystalline semiconductor materials can be electrodeposited in a layer-by-layer fashion via an electrochemical atomic layer epitaxy (ec-ALE) approach. The process takes advantage of the self-limiting growth character of underpotential deposition, leading to accurate control of deposit thickness down to atomic level.[42] Besides conventional semiconductor materials, ec-ALE also allows the formation of unique semiconductor superlattice structure such as InAs/InSb[65], PbSe/PbTe[66]. Finally, transition metal oxides (TiO_2[67,68], ZnO[69,70], WO_3[71]) can also be prepared by electrophoretic deposition, where suspended metal oxide particles are driven to the electrode substrates by large electric field between two electrodes.[72]

Electrodeposition has also undergone intense scrutiny by numerous research groups as a viable route for preparing crystalline Group IV semiconductor materials, such as Si and Ge.[36] Since the early attempt in 1860s by Ullik[36] of electrodepositing elemental Si using molten salt mixture (K_2SiF_6/KF) at 600 ^oC to 900 ^oC, various approaches have then been proposed for Si electrodeposition, including the use of silicon halides in organic solvents[73-78] or ionic liquids[79-82] at low temperatures, and silicon oxide[46,83] or fluorosilicate[45,84,85] in high temperature molten salts. Taking the low temperature approach, Agrawal and Austin[73] reported formation of hydrogenated Si deposits via potentiostatic deposition from propylene carbonate solution containing 1.0 M $SiHCl_3$ at temperatures between 35 ^oC to 145 ^oC. Nicholson[77] demonstrated elemental Si deposition from $SiCl_4$ and $SiBr_4$ in various solvents including acetonitrile, tetrahydrofuran, propylene carbonate, dimethyl sulfide and 1-methyl naphthalene. Borisenko and Endres[86] reported electrodeposition of Si from 0.1 M $SiCl_4$ in the room temperature ionic liquid, 1-butyl-1-methylpyrrolidinium bis(trifluoromethylsulfonyl)imide. Despite various reports for successful deposition of elemental Si, the as-prepared Si from low-temperature electrodeposition is always amorphous.[73-80] Excessively high (>700 °C) temperatures are required for an electrodeposition process to yield crystalline Si.[83-85] In the case of Ge, room temperature electrodeposition can yield elemental Ge from germanium halides precursor dissolved in either organic solvent[87] or ionic liquids[81,82,88]. Similarly, the Ge material obtained in these reports is all amorphous as deposited[81,82,87,88]. Crystalline Ge

can be obtained at room temperature from dissolve GeO_2 in aqueous electrolytes by an ec-ALE approach[89,90], but the deposition process was revealed to be self-limiting up to a few monolayers by scanning tunneling microscopy[89] and surface-enhanced Raman spectroscopy[90]. Unabated electrodeposition of crystalline Ge has so far been only achieved using high temperature molten salts containing GeO_2 as the precursor[91].

v. Mechanisms for Crystallization

In order to device a low temperature strategy for depositing crystalline Si and Ge electrochemically, the fundamental mechanisms for crystal growth should first be discussed. Two major crystal growth pathways have been proposed. The first is an irreversible deposition process with high surface or bulk mobilities in the solid phase, and the other is a reversible deposition process from the solution, liquid or vapor phase.[92] The first mechanism typically requires high temperature conditions in order to achieve high mobility of the Si or Ge atom in solid state, thus not compatible with the thesis goal for developing low energy synthetic method for crystalline Si and Ge. The second route has been widely adopted for synthesizing ionic compounds, as their precursors can be readily solvated in the solution phase to satisfy the reversible deposition condition for the crystal growth.[92] The growth of crystalline covalent semiconductor materials, such as Si and Ge based on the same mechanism requires the use of a proper substrate phase in which the precursors can be dissolved and allowed to equilibrate to form the solid crystal phase. This approach has been established and developed in a group of separate but related semiconductor growth techniques, namely, vapor-liquid-solid (VLS)[17,93,94] growth, solution-liquid-solid (SLS)[34,92] growth and supercritical fluid-liquid-solid (SFLS)[95] growth.

In 1964, Wagner and Ellis[93] reported the first example of crystalline semiconductor synthesis via the VLS mechanism by showing the growth of crystalline Si whiskers from a vapor phase precursor in the presence of Au seeding catalysts. The growth followed a well-studied mechanism starting with the melting of metal catalyst particles in the presence of a vapor phase precursor. The precursor is decomposed at the surface of the catalyst and forms liquid droplets of the metal/semiconductor alloy. The continuous dissolution of the precursor into the alloy eventually leads to a supersatuation

condition, after which crystalline semiconductor materials are precipitated from the alloy as the final product. The VLS method is capable of yielding highly crystalline nanomaterials with large quantity in a controllable manner, soon rendering itself an ideal choice of fabrication method for crystalline semiconductors.[17,96] At the meantime, analogous methods have been explored and developed to supply the precursors from lower temperature solution phase or supercritical fluid, and are known as SLS and SFLS growth methods. Despite the variation in experimental details such as the use of different catalyst metals or the adoption of different physical forms of the precursors, the essence of these methods remains the same, i.e. the use of a liquid phase medium that solvates the precursor material, leading to reversible equilibration that is necessary for the formation of a crystalline product.

B. Approaches and Hypotheses

The use of liquid phase metal catalyst in the VLS, SLS and SFLS studies have suggested a potential route to achieve crystalline growth by electrodeposition for covalent semiconductor materials like Si and Ge. Our group has thus proposed the use of a liquid metal electrode to replace the conventional solid electrode materials like Au, Pt or graphite for the application of electrodeposition[97]. In this case, the liquid electrode serves two purposes simultaneously. First, the liquid metal serves as a conductive substrate where current flows through as in any conventional electrochemical experiment. At the meantime, the liquid metal can also function as the crystallization phase where the reduced form of the precursor can be solvated and crystallizes. This approach presents a unique combination of electrochemical deposition and VLS-like crystal growth. As shown in Figure 1.2, the oxidized form of the precursor is first dissolved in a solution liquid phase and is electrochemically reduced to the elemental form. The elemental form of the precursor is then dissolved into the liquid metal phase. Further feeding in the reduced precursors into the liquid metal phase by the electrochemical deposition allows the supersatuation condition to be reached. As a result, a solid phase deposit is precipitated out from the liquid metal as the final product. This method is dubbed electrochemical liquid liquid solid method.

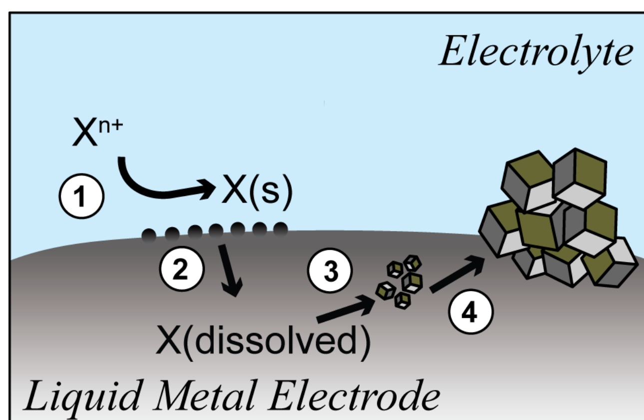

Figure 1.2. Schematic depiction of the electrochemical liquid-liquid-solid growth mechanism.

Comparing with conventional VLS and SLS methods, the ec-LLS has a few distinct advantages. 1) Low operation temperature. According to the proposed mechanism, the precursor for ec-LLS is first electrochemically reduced as is in a conventional electrodeposition setup. This allows the precursor decomposition step to be completely driven by electrochemistry at low temperature, sharply contrasting the VLS and SLS methods where the precursor decomposition is either driven thermally or chemically by reducing agents at high temperatures[17,34]. 2) Simple setup. The setup for ec-LLS does not differ significantly from that of a conventional electrodeposition. A standard three electrode configuration can be adopted without additional accessories. 3) Electrochemically controlled. A key advantage for ec-LLS method is that the crystal growth kinetics and thermodynamics can be controlled directly from electrochemical parameters. 4) Non-exotic precursor. The precursors used for the ec-LLS are simple molecular precursors including oxides or halides with no need for additional synthesis for complex precursors such as those used in solution liquid solid growth or metalorganic chemical vapor deposition.

The primary strategy for conducting the electrochemical investigation and the ec-LLS growth utilizes a conventional three-electrode setup featuring a liquid metal as the working electrode, Pt mesh as the counter electrode and AgCl-coated Ag rod in saturated KCl solution as the reference electrode. The working-counter electrode pair constitutes one circuit branch where current passes for the redox reactions associated with ec-LLS. The working-reference electrode pair represents a second circuit branch where no current flows. In this way, the reference electrode provides a stable sensing point for applying a potential to the working electrode to move its Fermi level.

In a three electrode cell, different excitation waveforms can be used to either differentiate redox processes or facilitate bulk redox reactions. In this thesis, two electrochemical techniques that employ different excitation waveforms are used to study the ec-LLS process. The first technique is cyclic voltammetry that measures the current responses during a linear scan of the applied potential. (Figure 1.3a) This technique reveals all the electrochemical processes within potential range of interest. The second technique is chronoamperometry where a constant applied bias is applied to trigger redox processes. (Figure 1.3b)

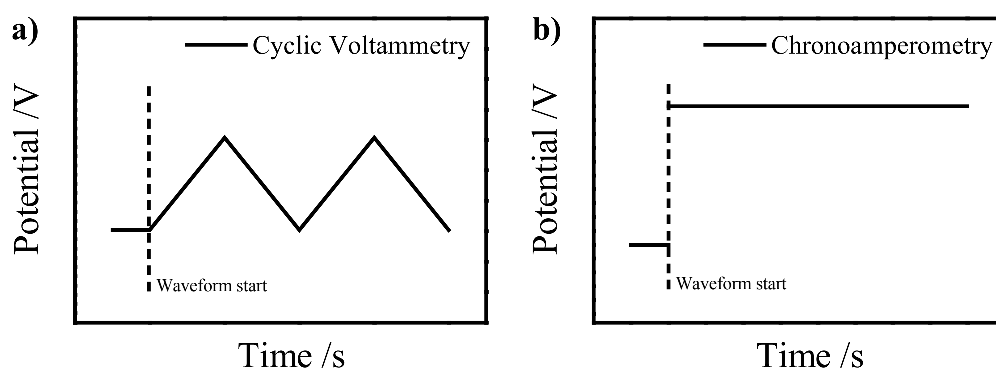

Figure 1.3. Depiction of the waveform used in a) cyclic voltammetry and b) chronoamperometry.

The practicality of the ec-LLS method has been demonstrated by our group in a report by Carim[97] showing the electrodeposition of large quantity of Ge onto liquid Hg electrode under ambient conditions from aqueous solution of GeO_2 without any physical or chemical templating agents. The formation of the Ge crystals followed the processes of electroreduction, dissolution into a liquid Hg electrode, saturation of the liquid alloy, and solid precipitation. The deposits were confirmed to be crystalline Ge by both X-ray diffraction and transmission electron microscopy. Further analysis of the X-ray diffraction data revealed effective control of the deposit crystallinity, i.e. average crystallite size by varying the electrochemical potential. A variety of material morphologies were obtained as deposited based on scanning electron microscopy, including dense films of oriented nanostructured filaments with large aspect ratios (>103). This report serves as the first demonstration of ec-LLS as a non-energy-intensive method for preparing crystalline semiconductor materials.

The primary scope of this thesis is to establish detailed understanding of ec-LLS as a synthetic method for preparing crystalline semiconductor materials. A number of key hypotheses will be tested regarding both the fundamental and practical aspects of ec-LLS. 1) The universality of the ec-LLS approach will be explored by performing crystal growth for Ge using various liquid pool electrodes besides liquid Hg. 2) Controlled ec-LLS growth of Ge nanowires will be carried out using nano-sized In seeding particles for the application of Li ion battery. 3) The possibility of room temperature epitaxial growth for Ge nanowire will be tested using liquid Ga nanodroplets. 4) Application of ec-LLS as a low temperature method for producing crystalline Si nanomaterials will be demonstrated.

C. Content Description

Chapter 2 explores the room temperature ec-LLS process for preparing crystalline Ge on liquid metal electrodes other than liquid Hg. Three different electrode materials were selected as the cathode material for the electrodeposition, pure Ga, Sn/Ga eutectic and In/Ga eutectic. Cyclic voltammetric response of these electrodes immersed in aqueous GeO_2 solution showed faradaic process associated with GeO_2 reduction. Poising the liquid metal electrodes at potential more negative than the reduction potential for

GeO_2 caused a conformal black film to form over the electrode surface. X-ray diffraction confirmed the black deposit to be crystalline Ge from all three liquid electrodes. Optically similar black deposits were also obtained on the solid form of the Ga metal/alloy electrodes at lower temperatures, but they did not yield any crystalline pattern in X-ray diffraction, effectively supporting the notion that liquid metal plays a key role in crystallizing the deposits. Scanning electron microscopy revealed a mixed morphology of faceted crystals and nanowires for the deposits, and detailed analysis of the faceted crystals by electron backscatter diffraction revealed the crystal facets were made of single crystal domains. The data collectively endorse ec-LLS as a versatile method for preparing crystalline semiconductor materials at room temperature.

Chapter 3 demonstrates the direct electrodeposition of crystalline Ge nanowires from an aqueous solution of dissolved GeO_2 using discrete 'flux' nanoparticles. Room temperature electrodeposition of Ge at conductive Si substrates decorated with small (<100 nm), discrete indium (In) nanoparticles resulted in crystalline Ge nanowire films with definable nanowire diameters and nanowire densities without the need for a physical or chemical template. As shown by X-ray diffraction and electron diffraction, the Ge nanowires exhibited strong polycrystalline character as-deposited, with approximate crystallite dimensions of 20 nm and a mixed orientation of the crystallites along the length of the nanowire. Energy dispersive spectroscopic elemental mapping of individual Ge nanowires showed that the In nanoparticles remained at the base of each nanowire, indicating the nanowire formation was governed by a root-growth mechanism. Furthermore, as-deposited Ge nanowire films prepared on Cu supports were used without further processing as Li^+ battery anodes. Cycling studies performed at 1C indicated the native Ge nanowire films supported stable discharge capacities at the level of 973 mA h g^{-1}, higher than analogous Ge nanowire film electrodes prepared through an energy-intensive vapor-liquid-solid nanowire growth process. The cumulative data show that ec-LLS is a viable method for directly preparing a functional, high-activity nanomaterials-based device component. The developed method is a step towards the realization of simple processes that make fully functional energy-conversion/storage technologies based on crystalline inorganic semiconductors entirely through benchtop, aqueous chemistry and electrochemistry without time- or energy-intensive process steps.

Chapter 4 details the possibility of achieving room temperature epitaxial nanowire growth via ec-LLS. Single crystalline Ge nanowires were obtained on a Ga-decorated Ge single crystal wafer by direct electrodeposition at room temperature from an aqueous solution containing GeO_2. Scanning electron micrograph showed uniformly vertical aligned Ge nanowires on a Ga-decorated Ge (111) wafer after electrodeposition. Varying the crystal orientation of the underlying Ge substrate caused an alteration of the growth orientation of the electrodeposited Ge nanowires, consistent with an epitaxial growth. The interfacial details between the Ge substrate and the as-deposited Ge nanowires were studied with atomic resolution by cross-sectional high-resolution transmission electron microscopy and selected area electron diffraction. Lattice continuity across the substrate-nanowire interface was concluded from both techniques, confirming the epitaxial nature of the growth. Crystallinity and defect formation were probed by transmission electron microscopy, followed by the proposal of a detailed growth pathway. At the same time, evidence of analogous heteroepitaxial growth of Ge nanowire on Ga-coated Si wafer was also observed. In addition, current-voltage responses measured in conductive atomic force microscopy across many individual nanowires yielded reproducible resistance values. The presented data cumulatively show epitaxial growth of covalent group IV nanowires is possible from the reduction of a dissolved oxide under purely benchtop conditions. As a result, uniformly aligned single crystalline nanowires with electrical integrity with the substrate can be obtained by room temperature electrodeposition.

Chapter 5 demonstrates the application of ec-LLS strategy for electrodeposition of crystalline Si at temperature as low as 80 ^{o}C from an organic electrolyte. Dissolved $SiCl_4$ in propylene carbonate was electrochemically reduced onto liquid gallium pool electrode to form high-coverage elemental Si. X-ray diffraction and electron diffraction data separately indicated that the as-deposited (i.e., with no annealing) materials were crystalline with the expected patterns for a diamond cubic crystal structure. Scanning electron microscopies further revealed the as-deposited materials to be faceted nanocrystals with diameters in excess of 500 nm. The influence of various experimental parameters such as temperature, precursor concentration, deposition time and applied electrochemical potential on the deposition product was discussed. Additional *in-situ* and *ex-situ* annealing experiments with Raman spectroscopy, X-ray diffraction, scanning

electron microscopy and scanning transmission electron microscopy revealed possible phase transition of the as-deposited Si crystallites upon annealing. The cumulative data support two primary contentions. First, a liquid-metal electrode can serve simultaneously as both a source of electrons for the heterogeneous reduction of dissolved Si precursor in the electrolyte (i.e., a conventional electrode) and a separate phase (i.e., a solvent) that promotes Si crystal growth. Second, ec-LLS is a process that can be exploited for direct production of crystalline Si at much lower temperatures than ever reported previously. The further prospect of ec-LLS as an electrochemical and non-energy-intensive route for preparing crystalline Si is discussed.

Chapter 6 summarizes other efforts and directions regarding semiconductor material preparation and characterization that do not fall under the primary scope of the ec-LLS growth. This chapter highlights data that described an overlayer surface-enhanced Raman spectroscopy (SERS) strategy for studying crystal quality of thin film semiconductors and the interfacial bonding between the semiconductor surfaces and foreign adsorbates. The study was motivated by the significant influence of material crystallinity as well as interfacial chemistry on semiconductor performance in energy conversion, sensing and microelectronics. In this work, Raman data detailing phonon evolution of Cd-based II-VI semiconductor at Au nanoparticle substrate during electrodeposition were presented to first demonstrate SERS as a facile approach for evaluating the integrity and crystallinity of semiconductor thin films in real time. The selection of suitable laser conditions (e.g. excitation wavelength, power density) for *in-situ* SERS measurement that resulted in minimal laser perturbation to data acquisitions was discussed. The semiconductor thin films on SERS-active Au substrate was then served as an overlayer SERS platform for studying the vibronic processes at the semiconductor surfaces. Preliminary data on the surface functionalization of the Cd-based semiconductor thin films were presented to show that the adsorption of benzenethiol onto CdS, CdSe and CdTe can be detected in aqueous solution at ambient conditions.

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CHAPTER 2

Electrodeposition of Crystalline Ge on Liquid Ga and its Alloys by ec-LLS Method

A. Introduction

This chapter explores the room temperature Ge electrodeposition from aqueous GeO_2 solution by ec-LLS on three different metal or metal alloys, Ga, GaSn eutectic and GaIn eutectic. Specifically, the electrochemical behavior of these three types of electrodes towards GeO_2 reduction was studied by cyclic voltammetry. The electrodeposition was carried out both potentiostatically and galvanostatically to obtain uniform black deposit at the electrode surface. The average crystallinity of these deposits obtained from all three types of electrodes at both solid and liquid state was evaluated by X-ray diffraction. Crystallinity for individual crystallites was also investigated in detail using an electron backscatter diffraction setup in the scanning electron microscope. The accumulative data indicate crystalline Ge materials can be obtained on liquid Ga, GaSn eutectic and GaIn eutectic at room temperature from an aqueous electrolyte by the ec-LLS method.

Group IV semiconductor materials are key functional components in solar energy conversion[1-4], energy storage[5-8] and optoelectronic applications[9-11]. Comparing with conventional material synthetic technologies[2,12-16], electrodeposition offers a unique combination of several advantageous properties, including low operation temperatures[17,18], simple instrument setup[19] and demonstrated scalability[20]. However, electrodeposition for preparing covalent group IV semiconductor materials have so far found limited practical applications due to the lack of crystallinity in the as-deposited materials[21-26]. As recently demonstrated in our group[27], a novel electrochemical liquid-liquid-solid growth method was developed for producing large quantity of crystalline Ge materials from an aqueous precursor electrolyte at room temperature. The key innovation

in the ec-LLS process was the use of liquid metal, Hg, as the working electrode. Unlike conventional solid electrodes, liquid Hg electrode forms liquid alloy with reduced Ge materials and facilitates the crystallization process. The as-deposited Ge materials were found to be crystalline by both X-ray diffraction and electron diffraction.

This chapter advances our understanding of the ec-LLS method in the following aspects. 1) The ec-LLS method will be applied to Ge deposition on three different metal and metal alloys so the universality of the ec-LLS mechanism can be tested. Replacing Hg with other liquid metals/alloys is also of other practical advantages due to the volatility and toxicity[28,29] of Hg. 2) The role of the liquid metal electrode in the ec-LLS process can be further studied by characterizing the deposits obtained on solid and liquid electrodes with identical chemical composition. The metal and metal alloys selected for this study all have melting points near room temperature (30 ^{o}C, 23 ^{o}C, 25 ^{o}C for Ga, GaSn eutectic and GaIn eutectic, respectively). As a result, both the solid and liquid state of the electrodes can be easily accessed in the laboratory environment.

B. Methods

Methanol (Certified ACS, Fisher), acetone (Certified ACS, Fisher), GeO_2 (99.999%, Acros Organics), $Na_2B_4O_7 \cdot 10H_2O$ (Analytical Reagent Grade, Mallinckrodt), KNO_3 (99+%, Acros Organics), HCl (GR ACS, EMD) were used as received. Materials used for electrode fabrication included In(*s*) (99.9+%, Aldrich) and Ga(*l*) (99.99%, Aldrich). Water with a resistivity > 18.2 MΩ cm^{-1} (Barnsted Nanopure) was used throughout.

The GaSn eutectic electrode was made by mixing 0.89 mass fraction of Ga and 0.11 mass fraction of Sn. The alloy was heated at 60 ^{o}C for 15 min in a muffle oven under ambient atmosphere to allow complete dissolution of solid Sn into Ga. Similarly, the GaIn eutectic electrode was made by mixing 0.75 mass fraction of Ga and 0.25 mass fraction of In. Prior to the mixing, the In metal was briefly etched with 1 M HCl solution to remove the native oxide.

All Ge electrodeposition was performed with a CH Instruments 760C potentiostat or an Eco Chemie Autolab PGSTAT302N potentiostat in a custom-built double-compartment glass cell. A three-electrode configuration with a Pt mesh counter electrode

and a Ag/AgCl (sat. KCl) reference electrode was employed. During the electrodeposition experiment, the Pt mesh counter electrode was positioned in the separate cell compartment to avoid the evolving O_2 from reaching the working electrode area. The electrical contact to the liquid metal working electrode was made from the bottom using a W rod sealed within a glass plug. The cell was immersed in the propylene glycol/water temperature bath to achieve the desired experimental temperatures. All reported electrochemical potentials were measured with respect to *E*(Ag/AgCl)(sat. KCl). The cyclic voltammetry was carried out in 0.1 M KNO_3, 0.05 M GeO_2(aq) and 0.01 M $Na_2B_4O_7$(aq) at 20 mV s^{-1} scan rate. Ge electrodeposition was performed at constant potential or constant current in 0.05 M GeO_2(aq) and 0.01 M $Na_2B_4O_7$(aq). After electrodeposition, the liquid metal working electrode was frozen by liquid N_2 to allow easy sample transfer and analysis.

Powder X-ray diffraction patterns were collected with a Bruker D8 Advance diffractometer equipped with a Cu Kα source, 0.6 mm incident beam slit and a Lynx Eye detector. The peak refinement and crystallite size analysis were performed in Crystal TOPAS (VERSION 4.1). Scanning electron microscopy (SEM) was conducted with a FEI Nova Nanolab Dual beam FIB-SEM with an in-lens secondary electron detector and a Philips XL30 FEG SEM with an Everhart-Thornley detector, both operated at 15 kV. Electron backscatter diffraction (EBSD) measurement was carried out in the Philips XL30 FEG SEM at 70 ^{o}C tilting angle.

C. Results

The electrochemical reduction of aqueous GeO_2 at Ga, GaSn as well as GaIn was first investigated by cyclic voltammetry. Figure 2.1 shows the iR-corrected current-potential response of liquid Ga, GaSn and GaIn electrodes in 0.1 M KNO_3, 0.01 M $Na_2B_4O_7$ solution with and without 0.05 M GeO_2 at 40 ^{o}C. In contrast to the slow current increase with the absence of dissolved GeO_2, the cathodic current rose sharply around -1.3 to -1.4 V vs. Ag/AgCl for all three types of working electrodes when 0.05 M GeO_2 was present in the solution. A net cathodic current observed only in the presence of dissolved GeO_2 indicated the cathodic features at potentials more negative than -1.3 V vs.

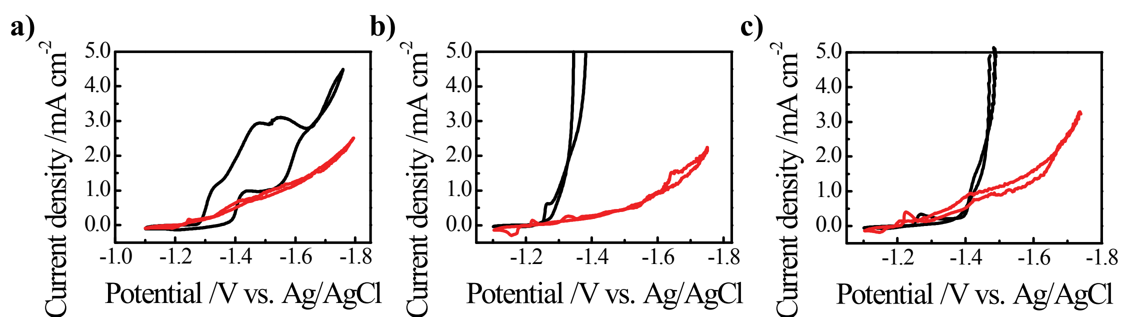

Figure 2.1. iR-corrected current-potential response of liquid a) Ga, b) GaSn and c) GaIn electrodes in 0.1 M KNO_3, 0.01 M $Na_2B_4O_7$ aqueous solution (black) with and (red) without 0.05 M GeO_2 at 40 ^oC. The scan rate is 20 mV s^{-1}

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Ag/AgCl were associated with the electrochemical reduction of GeO_2. Further analysis of the electrochemical data revealed little influence of the electrode composition on the H^+ reduction kinetics. The potential needed to achieve 2 mA cm^{-2} in the electrolyte buffer without dissolved GeO_2 was -1.75 V, -1.74 V, and -1.66 V vs. Ag/AgCl for Ga, SnGa and InGa, respectively. On the other hand, the GeO_2 reduction features were not identical at Ga, GaSn and GaIn electrodes. On both GaSn and GaIn electrodes, the lack of resolved reduction peaks within the current window suggested the reduction process was kinetically limited under current density of 5.0 mA cm^{-2}. Conversely, the cathodic current obtained on pure Ga electrodes showed several reduction peaks indicating that current-limiting factors other than the reduction kinetics was in effect.

Electrodeposition of Ge was then carried out on Ga(l) electrodes by applying a constant potential or a constant current. Figure 2.2 shows the chronoamperometric responses for two identical potential-step electrodeposition using Ga(l) electrodes in aqueous solutions containing 0.01 M $Na_2B_4O_7$ and 0.05 M GeO_2 at -1.6 V vs. Ag/AgCl for 2 h. The two potential-step experiments yielded unique yet reproducible current responses. In both cases, the cathodic current increased steadily from 0.68 mA cm^{-2} at the beginning, before reaching maximum value around 4000 s and declining till the end of the experiments. After the 2 h electrodeposition, black deposits with complete surface coverage were obtained on both electrodes, as shown in the insets of Figure 2.2. The electrodeposition was also performed galvanostatically on Ga(l) in the same electrolyte. Figure 2.3a shows the chronopotentiometric response of a Ga(l) electrode in the aqueous solution containing 0.01 M $Na_2B_4O_7$ and 0.05 M GeO_2 solution when a current of 1 mA (0.59 mA cm^{-2}) was applied. Starting at -1.30 V, the current reached steady state at -1.32 V after 800 s and maintained the same value throughout most of the experiment except towards the very end when the potential started to shift towards to more negative value. Figure 2.3b shows the chronopotentiometric response the Ga(l) electrode when the experiment was repeated using higher current at 2 mA (1.18 mA cm^{-2}). The potential started at -1.39 V vs. Ag/AgCl but only maintained at the steady state for 1500 s before drifting to more negative values. The potential was able to find another plateau at -1.86 V after 4000 s. The intense fluctuation of the recorded in this region suggests the Faradaic

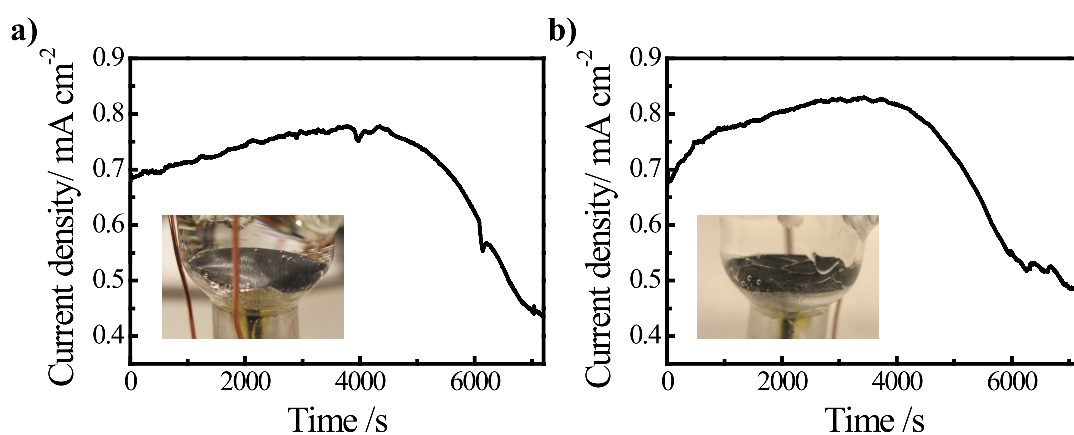

Figure 2.2. Chronoamperometric response obtained from two repeated depositions of a liquid Ga electrode in 0.01 M $Na_2B_4O_7$(aq) and 0.05 M GeO_2(aq) at constant potential of -1.6 V vs. Ag/AgCl for 2 h. Inset: optical images of black deposit on the Ga electrodes before being removed from the electrochemical cell.

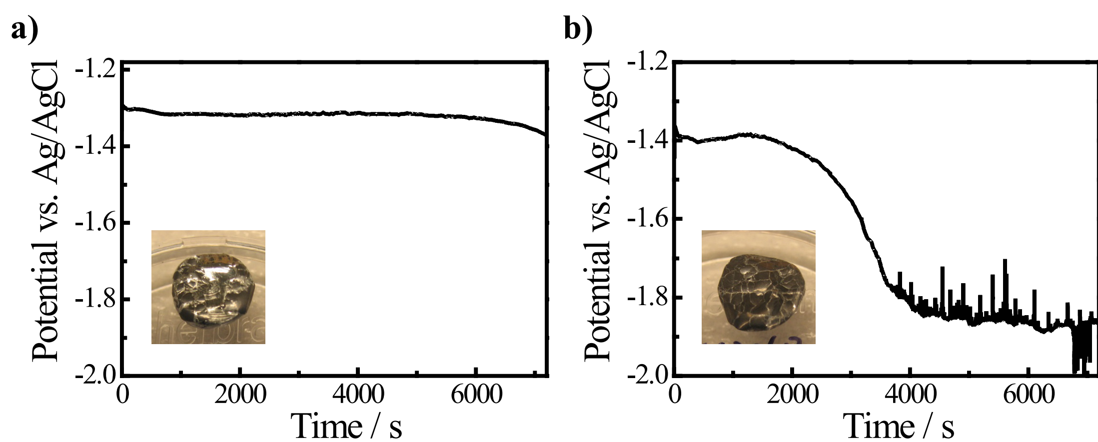

Figure 2.3. Chronopotentiometric response of a liquid Ga electrode in 0.01 M $Na_2B_4O_7$(aq) and 0.05 M GeO_2(aq) at constant current of a) 1 mA, and b) 2 mA for 2 h. Inset: optical images of the black deposit on the Ga electrodes after being removed from the electrochemical cell.

process at this potential became dominated by H_2 evolution. For the final products, experiments at both current setting produced black deposit with complete surface coverage (Figure 2.3 inset), similar to those obtained by potentiostatic deposition.

Figure 2.4 shows the side-by-side optical images of Ge deposits obtained by electrodeposition on a Ga liquid electrode at 40 ^{o}C and a Ga solid electrode at 25 ^{o}C. The deposits in these two samples both showed black hue and metallic reflection, bearing no discernable difference in appearance. Further analysis with X-ray diffraction however revealed drastic difference in the crystalline content within the samples. Figure 2.5a shows the background-subtracted X-ray diffractograms for both deposits obtained at liquid Ga and solid Ga electrode surfaces. For the deposit obtained at Ga(l) electrode, a set of diffraction peaks consistent with the diamond cubic structure of crystalline Ge was observed. The lattice constant was determined to be 5.65 Å, in good agreement with the expected value of 5.66 Å. Attempt was made to estimate the average crystallite size based on the diffraction peak broadening, but due to the dominating instrumental broadening for narrow diffraction peaks, only a lower bound of 100 nm could be determined for the average size based on the Scherrer equation. On the contrary, deposits obtained at the solid Ga electrode only yielded plain diffractogram with no discernable peaks associated with any crystalline content. As shown in Figures 2.5b, 2.5c, such contrast in the measured crystalline content between liquid electrode deposits and solid electrode deposits is also observed in the cases of GaSn and GaIn electrode.

Figure 2.6a shows a representative scanning electron micrograph of Ge deposits obtained by potentiostatic deposition on a liquid Ga electrode at -1.6 V vs. Ag/AgCl. The growth of nanowire structure was observed at the electrode surface. These nanowires were of large size distribution with no apparent ordering in the growth orientation. Multiple kinks were observed for individual nanowires along the growth direction, but the sidewall of the nanowire appeared to be smooth throughout the length of the nanowire. Underneath the nanowires, there formed a layer of faceted crystal aggregates. These crystals also showed large size distribution, with the largest crystal size up to 2-3 μm. The nanowires appeared to form along the boundaries where two adjacent crystals meet. Such morphology appeared to be a dominating motif over the entire surface, as shown by the low magnification scanning electron micrograph in Figure 2.6b.

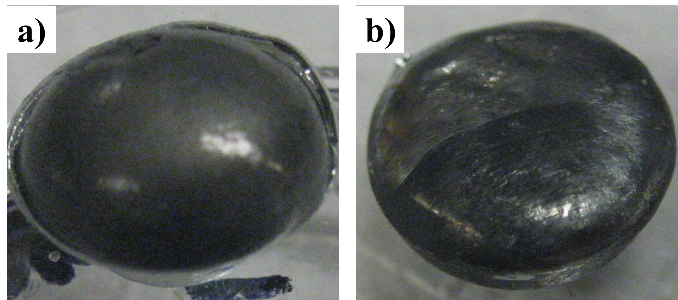

Figure 2.4. Optical image of Ge deposit obtained after a 10 h electrodeposition on a) liquid Ga electrode, and b) a solid Ga electrode.

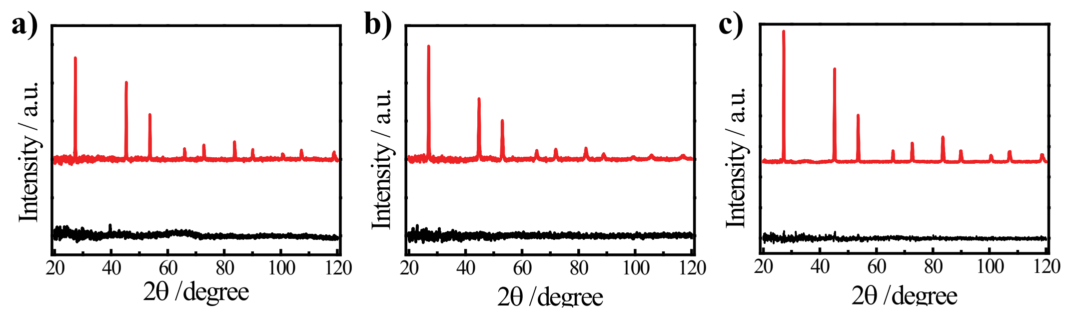

Figure 2.5. Background-subtracted X-ray diffractogram of Ge deposit obtained on (red) liquid and (black) solid electrode of a) pure Ga, b) GaSn eutectic and c) GaIn eutectic.

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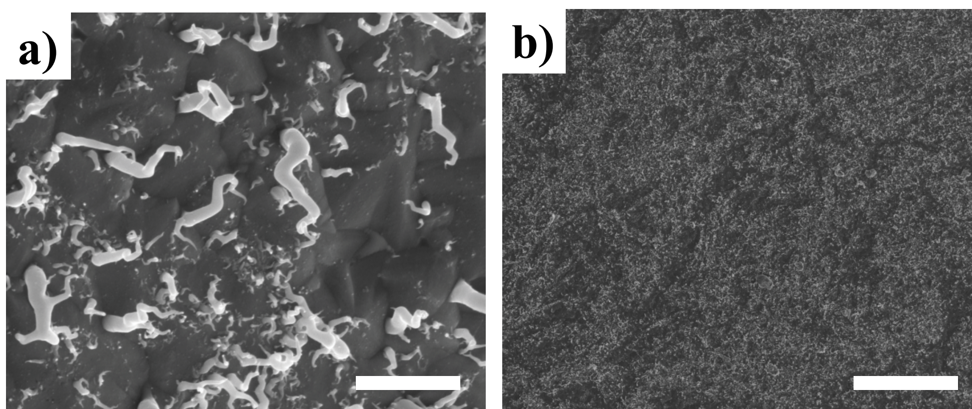

Figure 2.6. Scanning electron micrographs of as-deposited Ge on liquid Ga at a) ×25000 and b) ×1000 magnification. ec-LLS condition: -1.6 V vs. Ag/AgCl for 2 h in 0.01 M $Na_2B_4O_7$(aq) and 0.05 M GeO_2(aq). Scale bare: 2 μm and 50 μm.

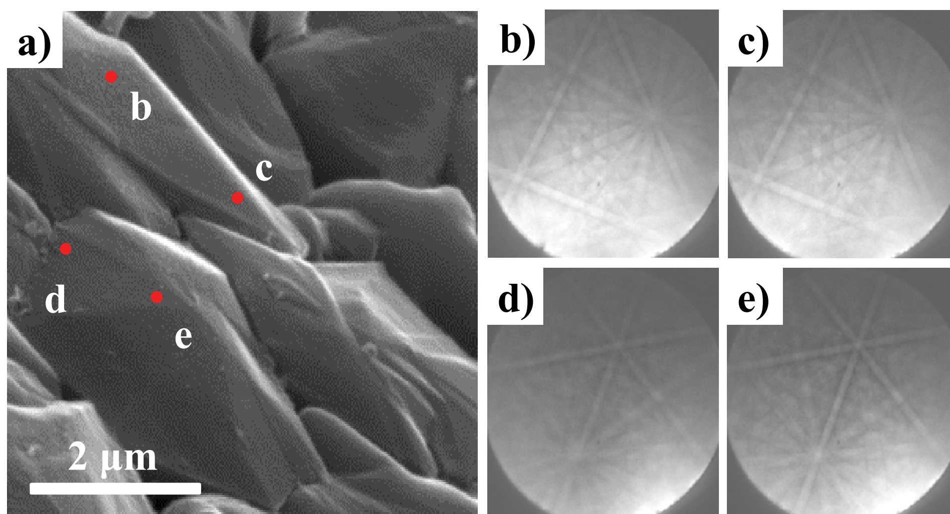

Figure 2.7. a) Scanning electron micrographs of as-deposited Ge highlighting a nanowire-free region. b) - e), Electron backscatter patterns of the labeled spots in a)

The crystallinity of the deposit was further studied using electron backscatter diffraction in the scanning electron microscope setup. Figure 2.7a shows a scanning electron micrograph highlighting a sample region with exposed crystal facets. The absence of overlayer nanowires on the large crystal facet allows the probing of crystal orientation using the EBSD technique. Figures 2.7b, 2.7c present the Kikuchi pattern obtained at the labeled locations on the first crystal facets. The observed pattern is consistent with a diamond cubic crystal structure. The two patterns measured at the opposite edge of the facet were identical, indicating the entire facet belongs to one single crystalline domain with the same crystal orientation. Figure 2.7d, 2.7e show the Kikuchi pattern obtained at the label locations on the second crystal facets. The same Kikuchi pattern was observed with altered orientation. Similar to the first facet, the two patterns measured at the opposite edge of this facet were also identical, suggesting the crystal is single crystalline.

D. Discussions

The data collectively indicate crystalline Ge can be electrodeposited at room temperature on liquid Ga, GaSn eutectic and GaIn eutectic. This suggests the ec-LLS mechanism is applicable to the electrodeposition on various kinds of liquid metal electrodes, and is not unique to the previously reported liquid Hg electrode.[27] The crystallography data demonstrate that ec-LLS method is a viable synthetic strategy for producing crystalline Ge materials.

The primary finding in this chapter is that using a liquid metal as the electrode substrate is critical for successful formation of crystalline Ge materials. The X-fay diffraction detects no crystalline content within the sample, if the deposit is obtained from solid Ga, GaSn eutectic or GaIn eutectic. This is consistent with the early reports[22,26,30] that electrodeposited Ge is only amorphous as deposited at low temperatures. The similarity in the optical appearance between the deposits obtained on liquid Ga and solid Ga suggested the electroreduction process of the GeO_2 precursor is not significantly sensitive to the state of the Ga electrode. However, the contrast in the crystallinity of the resultant deposits measured by the X-ray diffraction suggests the electrochemically reduced Ge interacts differently with a solid metal electrode vs. a liquid metal electrode.

When the covalent Ge is reduced onto the solid electrode interface, it relies on surface or bulk migration to achieve crystal formation.[15] This pathway is kinetically unfavorable due to the large crystallization barrier at room temperature.[31] Using a liquid metal electrode instead introduces another crystallization pathway where the now liquid-metal-solvated Ge atoms are allowed to undergo reversible equilibration that facilitates the crystal formation.[15]

Ge obtained on the liquid Ga (and its alloy) electrodes differs from the previously-reported Ge at liquid Hg electrodes in three major aspects. First, the average crystallite size of the Ge crystal is much larger in this report than 5 nm in the case of Hg liquid electrode. Although only a lower bound value of 100 nm can be directly obtained from the X-ray diffraction data, the SEM and EBSD measurements suggests surface is covered with faceted crystals with domain size on the order of a few μm. Second, the Ge materials obtained on the liquid Ga electrodes showed unique morphologies that were not previously observed in the liquid Hg case. The mixed morphologies of large crystal facets and smaller nanowires suggest two different types of crystal growth took place. The large faceted crystal is characteristic of an isotropic growth process, expected from a non-templated crystal growth in a homogeneous solution. The template-free growth of the nanowires from the liquid metal on the hand is somewhat peculiar. Close scrutiny of the scanning electron micrographs suggests the growth of the nanowire is concentrated at the grain boundaries of the large Ge crystals. Small pool of Ga droplets may be isolated during the merging of large crystals and serve as the nucleation center for the anisotropic nanowire growth. The observation of nanowire formation on the liquid Ga pool electrode hints the possibility of controlled Ge nanowire growth by the ec-LLS method. Such possibility will be tested in detail in the following chapters with In nanoparticles and Ga nanoparticles, respectively. Third, unlike the unabated growth of Ge on liquid Hg electrode, the electrochemical data suggest the growth process on the Ga electrodes is not unlimited and shows signs of decay after 1-2 h. In the potentiostatic deposition, the current started to diminish after about 6000 s, and in the galvanostatic deposition, the required potential to maintain the demanded current began to drift to more negative values during the course of the 2 h experiments. In both cases, the change in the current or potential traces was relatively abrupt, unlikely to be caused by the gradual decrease in

the precursor concentration. The optical images and scanning electron micrographs both indicate high coverage film formation after a typical 2 h deposition. The decay in the observed electrochemical reduction may thus be caused by the blockage of the active liquid Ga metal sites.

E. Conclusions

This chapter discussed the electrodeposition of crystalline Ge materials on three different liquid metal or metal alloys, pure Ga, GaSn eutectic and GaIn eutectic. X-ray diffraction confirms the black deposit obtained from the electrodeposition process to be crystalline Ge using all three liquid electrodes. Optically black deposits were also obtained on the solid form of the Ga metal/alloy electrodes at lower temperatures, but they did not yield any crystalline pattern in X-ray diffraction, effectively supporting the notion that liquid metal plays a key role in crystallizing the deposits. Scanning electron microscopy revealed a mixed morphology of faceted crystals and nanowires for the deposits, and detailed analysis of the faceted crystals by electron backscatter diffraction revealed the crystal facets were made of single crystal domains. The data collectively endorse ec-LLS as a versatile method for preparing crystalline semiconductor materials at room temperature.

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CHAPTER 3

Template-Free Preparation of Crystalline Ge Nanowire Film Electrodes via an ec-LLS Process in Water at Ambient Pressure and Temperature for Energy Storage

A. Introduction

This chapter discusses the possibility of direct electrodeposition of crystalline Ge nanowires from an aqueous solution of dissolved GeO_2 using discrete 'flux' nanoparticles. Room temperature electrodeposition of Ge at conductive Si substrates decorated with small (<100 nm), discrete indium (In) nanoparticles resulted in crystalline Ge nanowire films with definable nanowire diameters and nanowire densities without the need for a physical or chemical template. As shown by X-ray diffraction and electron diffraction, the Ge nanowires exhibited strong polycrystalline character as deposited, with approximate crystallite dimensions of 20 nm and a mixed orientation of the crystallites along the length of the nanowire. Energy dispersive spectroscopic elemental mapping of individual Ge nanowires showed that the In nanoparticles remained at the base of each nanowire, indicating the nanowire formation is governed by a root-growth mechanism. Furthermore, as-deposited Ge nanowire films prepared on Cu supports were used without further processing as Li^+ battery anodes. Cycling studies performed at 1C indicated the native Ge nanowire films supported stable discharge capacities at the level of 973 mA h g^{-1}, higher than analogous Ge nanowire film electrodes prepared through an energy-intensive vapor-liquid-solid nanowire growth process. The cumulative data show that ec-LLS is a viable method for directly preparing a functional, high-activity nanomaterials-based *device* component. The work presented here is a step towards the realization of simple processes that make fully functional energy-conversion/storage technologies based on crystalline inorganic semiconductors entirely through benchtop, aqueous chemistry and electrochemistry without time- or energy-intensive process steps.

Scalable, non-energy intensive, and environmentally benign methods for producing crystalline, nanostructured semiconductor materials are paramount to advance next generation energy conversion/storage technologies.[1,2] To this end, assembly strategies that do not rely on existing semiconductor industry fabrication practices[2] but instead yield fully functional nanomaterials-based *devices* in a single preparative step need to be demonstrated.[3] As shown in the previous chapter, the ec-LLS process can be utilized to electrodeposit Ge crystals and nanowires on bulk liquid Ga electrodes from aqueous solutions at room temperature. The absence of annealing steps and the use of low-toxicity GeO_2 precursor are desirable aspects for facile and direct production of crystalline Ge. However, in the original embodiment of ec-LLS, mixed morphologies of crystalline Ge materials were obtained from a macroscale (radius = 10^{-2} m) liquid 'flux' electrode with limited control of the feature sizes. Hence, this chapter will further discuss ec-LLS approach as a simple, controlled fabrication method for electrodepositing Ge nanowires on nano-sized 'flux' droplets. To avoid potential coalescence between closely-spaced liquid metal (e.g. Hg) droplets[4], less mobile 'flux' materials like indium (In) nanoparticles are used in this study. Although bulk In has a moderately low melting point (ca. 156 °C), the surface melting point of In is near 100 °C,[5] and the melting point of small In nanoparticles is below 100 °C,[6,7] In is not typically considered a liquid metal at room temperature. However, separate studies have shown that In nanoparticles specifically in intimate contact with Ge have an unusually low melting point, with In-Ge nanoparticles apparently showing liquid properties at room temperature.[8] This large melting point depression has been rationalized to arise from large heteroepitaxial stress between two dissimilar materials.[8,9] In nanoparticles prepared on a conductive support that is otherwise inactive towards Ge electrodeposition may thus be a stable and ideal platform for ec-LLS preparation of individual Ge nanowire film electrodes (Figure 3.1a). The discussion in this chapter will focus on testing the hypothesis that electrodeposited In nanoparticles can facilitate a simple benchtop, room-temperature preparation of crystalline Ge nanowire film electrodes from an aqueous solution containing dissolved $GeO_2(aq)$ via the ec-LLS scheme. The data cumulatively describe the effectiveness, simplicity, and general features of the ec-LLS process for making functional,

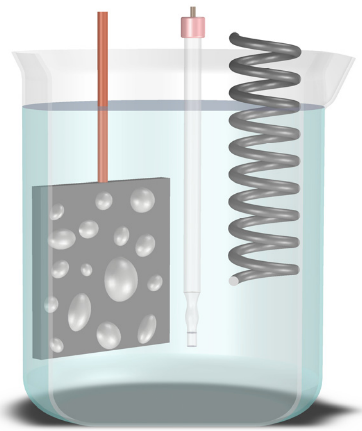

Figure 3.1. Schematic depiction of the electrodeposition setup for the Ge nanowire growth from an aqueous solution at ambient condition.

nanostructured, and crystalline Ge nanowire electrode materials. As a proof-of-concept demonstration of ec-LLS as a potentially scalable, non-energy intensive method for making energy technologies, as-electrodeposited Ge nanowire film electrodes are investigated as anodes in Li^+ battery applications.

B. Methods

Methanol (Certified ACS, Fisher), acetone (Certified ACS, Fisher), $InBr_3$ (99.99%, Alfa Aesar), Li foil (Strem Chemicals), GeO_2 (99.999%, Acros Organics), HF (49%, Transene Inc.), H_2O_2(30%, Fisher), H_2SO_4(doubly distilled, Sigma-Aldrich), $Na_2B_4O_7 \cdot 10H_2O$ (Analytical Reagent Grade, Mallinckrodt), $LiPF_6$ (99.99%, Aldrich), ethylene carbonate (Aldrich), and diethyl carbonate (Aldrich) were used as received. Materials used for electrode fabrication included Si (P-doped n-type, 1-10 ohm cm, 0.5±0.025 mm thick), Cu foil (99.9%, McMaster-Carr), In(*s*) (99.9+%, Aldrich) and Ga(*l*) (99.99%, Aldrich). Water with a resistivity > 18.2 MΩ cm^{-1} (Barnsted Nanopure) was used throughout.

Powder X-ray diffraction patterns were collected with a Bruker D8 Advance diffractometer equipped with a Cu Kα source, 0.6 mm incident beam slit and a Lynx Eye detector. The peak refinement and crystallite size analysis were performed in Crystal TOPAS (VERSION 4.1). Transmission electron microscopy (TEM) was performed with a JEOL 3011 TEM equipped with a LaB_6 source operated at 300 kV. Samples for TEM analysis were prepared by removing as-deposited Ge nanowires from the electrode supports through sonication in methanol for 30 sec. The suspension was then drop cast onto copper grids coated with ultra-thin carbon films on holey carbon (Ted Pella). Scanning electron microscopy (SEM) was conducted to characterize the quality of as-prepared Ge nanowire films with a FEI Nova Nanolab Dual beam FIB-SEM operated at 5 kV with an in-lens secondary electron detector. Energy dispersive spectroscopy (EDS) was performed at 10 kV with an EDAX UTW detector. Particle density and size distributions were analyzed based on the SEM images over an area of 5.66 μm^2 using ImageJ (Version 1.45s) software.

All In and Ge electrodepositions were performed with a CH Instruments 760C potentiostat and either a custom-made Teflon cell with a 0.0252 cm^2 window (for

electrodeposition on Si) or a single-compartment glass cell (for electrodeposition on Cu foil). In either case, a three-electrode configuration with a Pt wire counter electrode and a Ag/AgCl (sat. KCl) reference electrode was employed. All reported electrochemical potentials are with respect to *E*(Ag/AgCl)(sat. KCl). Prior to use, Si sections were cut, sonicated in acetone for 15 min, etched in 1:3 (v/v) 30% H_2O_2:98% H_2SO_4 for 30 min at 50 ^oC, and etched in 5% HF for 1 min to remove surface oxides. Immediately following the last etch step, each Si section had an In-Ga eutectic film applied to the back and then was transferred onto a stainless steel support. In nanoparticles were electrodeposited at a constant potential for 1 s in 0.1 M $InBr_3$(aq) and 0.1 M KNO_3(aq). The In nanoparticle conditions (*I-IV*) described in Figures 3.3 and 3.4 of the main text were effected by pulsed electrodeposition at -1.0 V, -1.2 V, -1.4 V, and -1.6 V vs. Ag/AgCl, respectively. Ge nanowires were subsequently electrodeposited at a constant applied potential in 0.05 M GeO_2(aq) and 0.01 M $Na_2B_4O_7$(aq).

Capacity measurements for Li^+ charge and discharge cycles were performed with a CH Instruments 760C potentiostat in a 2 electrode configuration with a potential window from +2.00 V to +0.05 V vs. *E*(Li^+/Li). Prior to cell assembly, the mass of the electrodeposited Ge nanowires was determined with a Sartorius ME36S microbalance (readability 0.001 mg). All battery cells were assembled in a Vacuum Atmospheres OmniLab glove box under Ar(*g*). For each electrode, a Cu substrate containing ca. 100 μg Ge nanowires was loaded in a home-made PTFE union cell with a 2 cm inner diameter. Li foil was used as the counter/reference electrode, separated from the working electrode by a piece of filter paper (Whatman, grade 2). The electrolyte was 1 M $LiPF_6$ in 2:1 (v/v) ethylene carbonate and diethyl carbonate. Both solvents were dried over P_2O_5 prior to use. For cycling experiments described in Section S8, electrodes were initially cycled at 1C rate for one charge-discharge prior to repetitive cycling at 5C rate.

C. Results

Figure 3.2 summarizes the current-potential responses of GeO_2 electrochemical reduction on bare n-Si wafer and n-Si wafer coated with In nanoparticles. When a bare n-Si wafer was used as the working electrode in 10mM $Na_2B_4O_7$ and 0.05 M GeO_2, the only apparent feature observed during the cathodic scan was the reversible current

associated with H^+ reduction at potential more negative than -1.4 V vs. Ag/AgCl. No evidence of Ge electroreduction was observed in this electrolyte, in accord with past reports of Ge electrodeposition.[10,11] These electrodes also yielded similar current-potential responses as n-Si electrodes coated with In nanoparticles immersed in aqueous electrolyte without dissolved GeO_2, indicating that the presence of In nanoparticles did not substantially enhance the observable activity for H_2 evolution at negative applied potentials, in agreement with the known poor electrocatalytic activity of In for H^+ reduction.[12] The small reductive peak at -1.2 V vs. Ag/AgCl prior to the H_2 evolution is caused by the reduction of native In_2O_3 at the In nanoparticle surface. For an aqueous electrolyte containing 50 mM GeO_2, n-Si electrodes coated with In nanoparticles showed uniformly higher current densities at potentials more negative than -1.4 V vs. Ag/AgCl, in accord with the notion that the reduction of dissolved GeO_2 occurred exclusively at the In nanoparticles. Ge nanowire growth was then carried out potentiostatically at -2.0 V vs. Ag/AgCl. The growth selectivity on In nanoparticles was also verified by scanning electron micrographs shown in Figure 3.3. A 10 min Ge reduction at -2.0 V vs. Ag/AgCl at In-coated n-Si substrate, as shown in Figure 3.3a, revealed nanowire morphology with high coverage. On the contrary, Ge reduction at identical conditions did no yield any discernable deposits on bare n-Si substrates (Figure 3.3b).

Chronocoulometric experiments showed that the Ge electrodeposition process was unabated over the course of at least 5 min (Figure 3.4a). The In-coated n-Si electrodes visibly darkened during the course of electrodeposition, eventually becoming dull black (see below). Figure 3.4b illustrates the current transients from a chronoamperometric experiment at -2.0 V vs. Ag/AgCl of a n-Si electrode coated with In nanoparticles in an aqueous electrolyte with and without dissolved 0.05 M GeO_2 precursor. With the presence of dissolved GeO_2, the measured current response consistently showed a peaked profile mirroring the shape typically observed in data for chronoamperometric electrodepositions.[13] Figure 3.4c shows the normalized current transient of Ge electrodeposition after the contribution from H^+ reduction was subtracted. The normalization was carried out with respect to the maximum current i_{max} as well as to the time at which the maximum current was obtained t_{max}. Plotted along with the

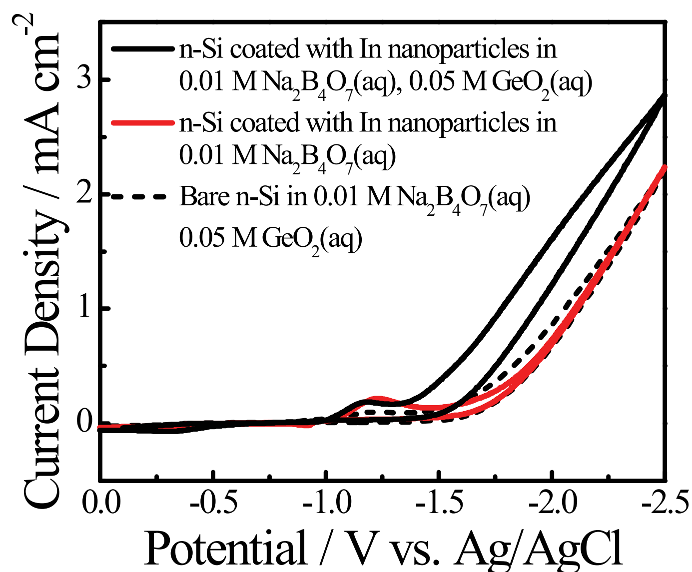

Figure 3.2. Current-potential responses for n-Si electrodes immersed in 0.01 M $Na_2B_4O_7$. Responses are shown for (dashed line) bare n-Si electrodes in electrolyte + 0.05 M GeO_2, (solid red line) n-Si electrodes decorated with In nanoparticles in electrolyte without 0.05 M GeO_2, and (solid black line) n-Si electrodes decorated with In nanoparticles in electrolyte with 0.05 M GeO_2. Scan rate = 0.025 V s^{-1}

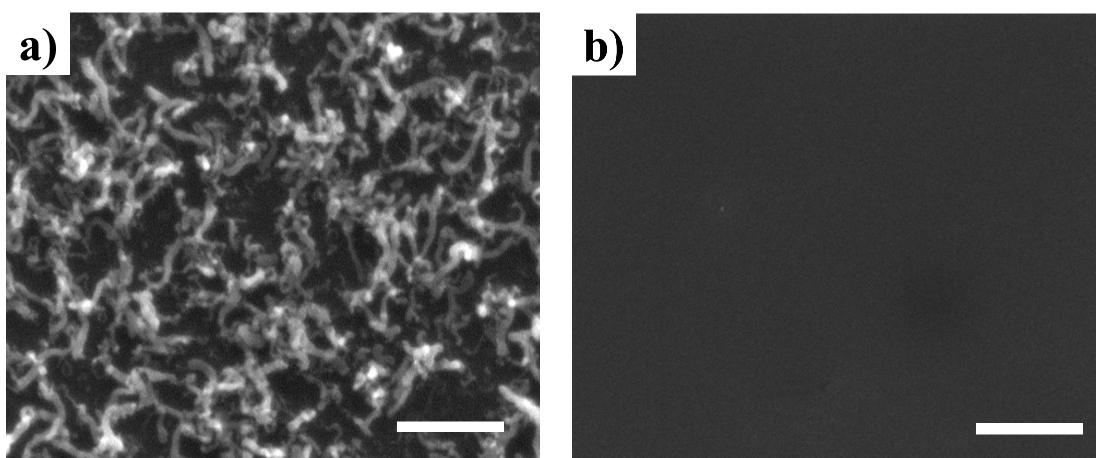

Figure 3.3. Scanning electron micrographs of a) In-coated n-Si and b) bare n-Si substrate after ec-LLS growth of Ge nanowires from 0.01 M $Na_2B_4O_7$(aq) and 0.05 M GeO_2(aq), at -2.0 V vs. Ag/AgCl for 10 min. Scale bare: 500 nm.

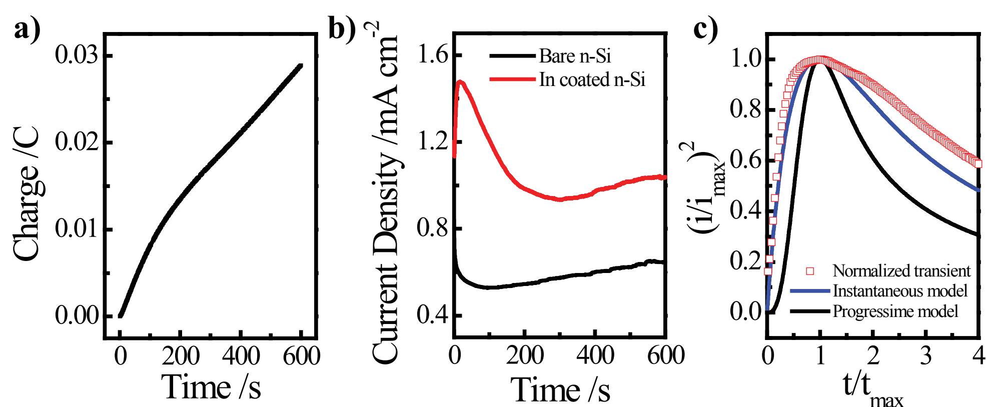

Figure 3.4. a) Chronocoulometric response for an n-Si electrode coated with In nanoparticles biased at -2.0V vs. Ag/AgCl for 10 min while immersed in 0.01 M $Na_2B_4O_7$(aq) and 0.05 M GeO_2(aq) after subtraction of the background faradaic charge for H^+ reduction. b) Raw (uncorrected) chronoamperometric responses for (black line) a bare n-Si electrode and (red line) an n-Si electrode coated with In nanoparticles in 0.01 M $Na_2B_4O_7$ and 0.05 M GeO_2 biased at -2.0 V vs. Ag/AgCl for 10 min. c) Corrected current transient with current normalized to the peak current density and time normalized to the time corresponding to the peak current density. Models for (blue line) instantaneous and (black line) progressive nucleation models are also shown.

experimental transient are the expected transient responses from the two prevailing models (instantaneous nucleation and progressive nucleation) for electrodeposition processes.[13,14] As shown in the figure, the collected transient data at the beginning stage of the experiment agreed well with the instantaneous nucleation model, suggesting Ge electrodeposition occurred immediately at a finite number of In nanoparticles (i.e. the electrodeposition of each Ge nanowire in the film began instantly and uniformly rather than a progressive initiation of additional Ge nanowires throughout the potential step experiment).

Figures 3.5 and 3.6 collect data describing the crystallinity of the as-prepared Ge nanowires. Following Ge electrodeposition at -2.0 V vs. Ag/AgCl for 60 min, electrodes were removed from solution, thoroughly rinsed and dried under N_2(g). Figure 3.5 shows the observed X-ray diffraction pattern for the as-prepared Ge nanowire thin film, showing characteristic diamond cubic lattice structure of crystalline Ge. Fitting the broadened line shape yielded polycrystalline domains of ca. 20 nm, and the pattern of reflections corresponded to a lattice constant of 5.67 Å, in good agreement with the expected lattice constant of 5.66 Å for bulk crystalline Ge. Additional reflections in the X-ray diffractogram were determined to be caused by residual metallic In on the substrate. To further study the crystallinity of the as-deposited Ge nanowires, separate transmission electron microscopy was performed on isolated Ge nanowires without the interference from the underlying Si substrate. Figure 3.6a shows a low magnification transmission electron micrograph of a typical Ge nanowire after a 10 min ec-LLS process. The irregular variation in the contrast throughout the body of the nanowire suggested the as-prepared Ge nanowire was not single crystalline. High resolution transmission electron micrograph (Figure 3.6b) revealed the Ge nanowire was composed of polycrystalline domains of different orientations with respect to the nanowire long axis, the domain sizes of which were in accord with those noted from the X-ray diffraction. The observation of polycrystallinity was also supported by the disordered diffraction spot pattern in the selected area electron diffraction shown in the figure inset. These features were consistent with previous observations of Ge nanowires prepared via ec-LLS at macroscale liquid 'flux' electrodes.[15] High resolution transmission electron micrograph (Figure 3.6c)

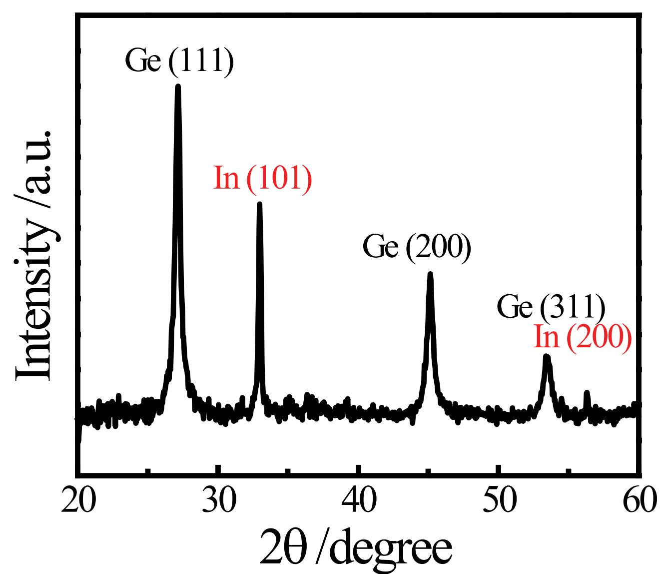

Figure 3.5. Measured X-ray diffraction pattern collected after Ge electrodeposition at -2.0 V vs. Ag/AgCl for 1 h.

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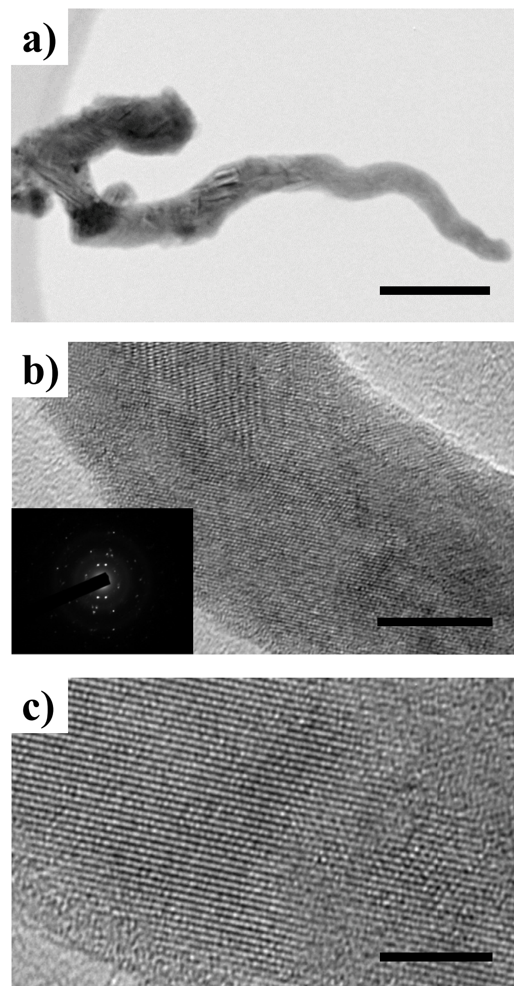

Figure 3.6. a) Low magnification transmission electron micrograph of an individual Ge nanowire electrodeposited at -2.0 V vs. Ag/AgCl for 10 min. Scale bar: 50 nm. b), c) High resolution transmission electron micrographs of the same Ge nanowire as in a). Scale bar: 10nm, 5 nm.. Inset: selected area electron diffraction pattern taken over the area shown in b).

focusing on a single crystal domain shows orderly lattice fringes with the distance between the (111) planes, d_{111}, being estimated as 3.29 Å, in reasonable accord with the known d_{111} value of 3.26 Å for diamond cubic Ge.

Figures 3.7 and 3.8 describe how the Ge nanowire films were influenced by the features of the initial In nanoparticles. As shown in the plan-view scanning electron micrographs in Figures 3.7a-d, experiments were performed on n-Si electrodes with varied loadings of In nanoparticles controlled through the parameters used for In electrodeposition. The densities and sizes of In nanoparticles were controlled solely through the applied potential used to electrodeposit In from solution. By increasing the electrodeposition potential from -1.0 V to -1.6 V vs. Ag/AgCl for a 1 sec pulse deposition process in 0.1 M $InBr_3$ and 0.1 M KNO_3 solution, the average size of In nanoparticles tended to decrease as the density of In nanoparticles increased. After thorough rinse, each of these n-Si platforms loaded with In nanoparticles was then subject to the same Ge electrodeposition step at -2.0 V vs. Ag/AgCl lasting 10 min in 0.01 M $Na_2B_4O_7$ and 0.05 M GeO_2. The resultant Ge nanowires from each platform were shown in the scanning electron micrograph in Figure 3.7e-h. Three points are visually apparent from the micrographs in Figure 3.7. First, the density of Ge nanowires tracked the density of In nanoparticles, i.e. higher densities of Ge nanowires were obtained with n-Si substrates decorated with higher densities of In nanoparticles. Second, the diameters of the electrodeposited Ge nanowires tracked the diameters of the In nanoparticles, i.e. thicker Ge nanowires were observed with larger In nanoparticles. Third, each Ge nanowire appeared to emanate from a single and distinct location on the electrode surface. The correlations between In nanoparticle and Ge nanowire size/density are shown more quantitatively in Figure 3.8. Figure 3.8a is a plot of the Ge nanowire density as a function of the In nanoparticle density, spanning a range of 19.3 to 207.5 objects μm^{-2}. The dashed line indicates the expected correlation if every In nanoparticle yields a single Ge nanowire. The cumulative data from four separate trials indicated that the correlation was closer to one Ge nanowire obtained from every two In nanoparticles, i.e. not every In nanoparticle facilitated the electrodeposition of a Ge nanowire under the employed conditions. Figure 3.8b illustrates that the electrodeposition protocol used to prepare the

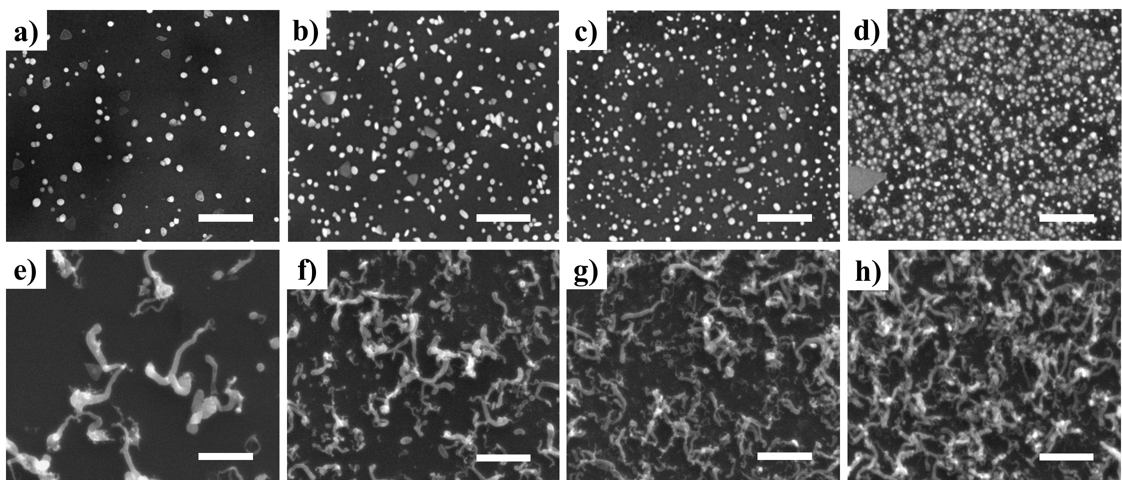

Figure 3.7. Top-down view scanning electron micrographs of n-Si electrodes decorated with different densities of In nanoparticles a)-d) before and e)-h) after Ge electrodeposition at -2.0 V vs. Ag/AgCl for 10 min.

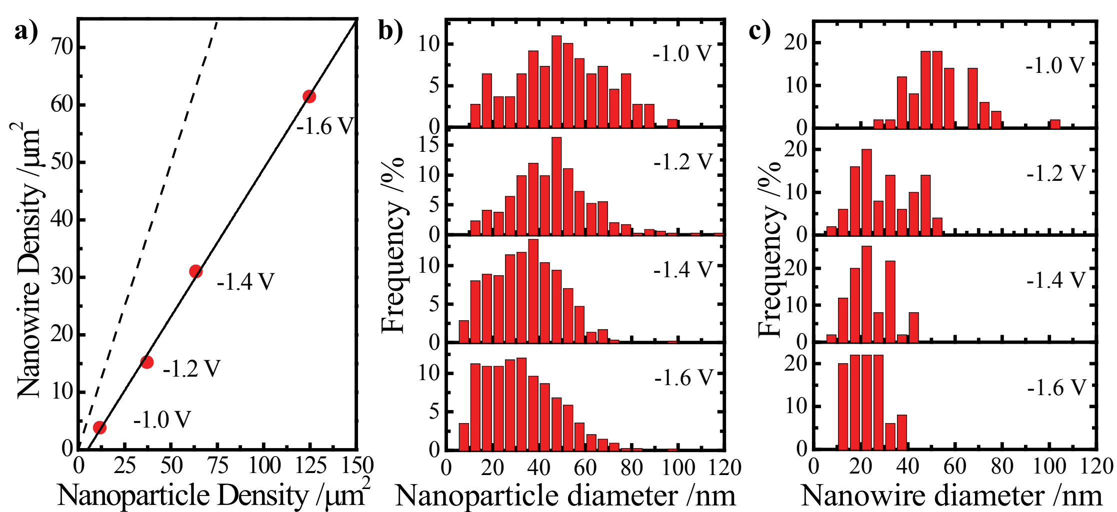

Figure 3.8. a) Comparison of the observed density of Ge nanowires as a function of the observed density of In nanoparticles on n-Si electrodes. Dashed line corresponds to 1 Ge nanowire per 1 In nanoparticle. b) Observed size distribution of In nanoparticles at several different In nanoparticle densities, as indicated in a). c) Size distribution of Ge nanowires electrodeposited from In nanoparticles at the four different densities of In nanoparticles shown in b). Bin sizes in b) and c) are 5 nm.

In nanoparticle films on n-Si yielded broad distributions with respect to nominal particle diameter. The asymmetries in the distributions partially reflect the insensitivity of the scanning electron microscopic analysis towards ultra-small (<5 nm) In nanoparticles. Nevertheless, Figure 3.8c demonstrates that the observed size (width) distributions of the Ge nanowires closely followed the distributions in Figure 3.8b. Separately, Figure 3.8c also shows that the variation in diameter, as described by the distribution width, was slightly narrower for the electrodeposited Ge nanowires as compared to the parent In nanoparticles, particularly at higher densities. In these experiments, In nanoparticle sizes were kept below 100 nm and the majority of In nanoparticles were below 60 nm. Separate experiments were performed to electrodeposit Ge nanowires on In nanoparticles with diameters > 100 nm. The large In nanoparticles were electrodeposited onto n-Si at -1.6 V vs. Ag/AgCl for 1 s from a solution containing 0.1 M KNO_3 and low concentration of $InBr_3$ at 0.01 M. Figure 3.9 shows the scanning electron micrograph of the as-prepared Ge nanowires after electrodeposition at -2.0 V vs. Ag/AgCl for 10 min in a solution of 0.01 M $Na_2B_4O_7$ and 0.05 M GeO_2 on these In nanoparticles. In contrast to In nanoparticles smaller than 100 nm, the large nanoparticle seeds favored the growth of multiple Ge nanowires from a single nanoparticle.

Figure 3.10 highlights the time-dependent growth of Ge nanowires up to 12 hr. The n-Si substrates were first coated with In nanoparticles by electrodeposition at -1.6 V for 1 sec from 0.1 M $InBr_3$ and 0.1 M KNO_3. Ge nanowires were then deposited by ec-LLS at various durations from 1 min to 12 hr. The plan-view scanning electron micrographs in Figures 3.10a-d show increasing coverage of Ge nanowires as the electrodeposition time increases. After 1 min deposition (Figure 3.10a), nanowires with lengths longer than 500 nm could be observed on the n-Si substrate along with unseeded In nanoparticles seen across the sample surface, indicating uneven growth rates of Ge nanowires at different In nanoparticles. The percentage of unseeded In nanoparticles appeared to decrease as the Ge deposition time increases. According the cross-sectional scanning electron micrographs in Figures 3.10e-h, the thickness of overall Ge nanowire thin film did not increase significantly after the initial 10 min deposition, suggesting the growth of an individual nanowire can achieve terminal length within 10 min. Multiple

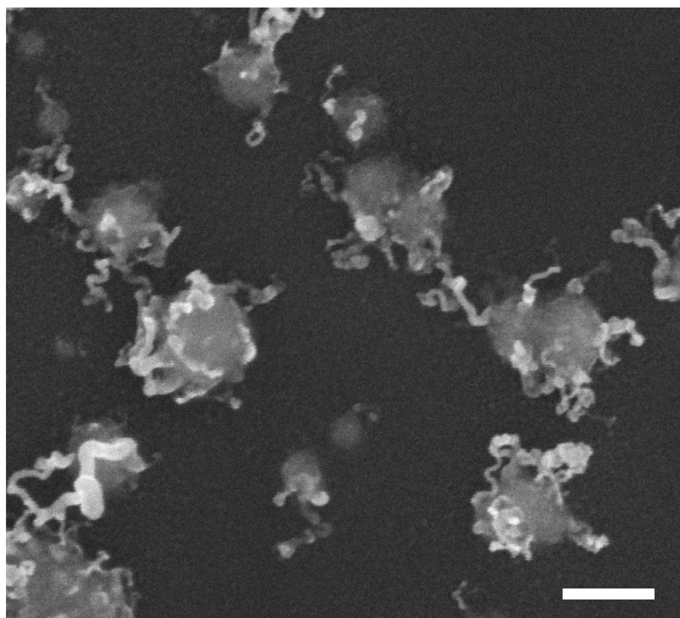

Figure 3.9. Scanning electron micrograph of Ge nanowires electrodeposited with an n-Si electrode with large In nanoparticles. Scale bar: 200 nm.

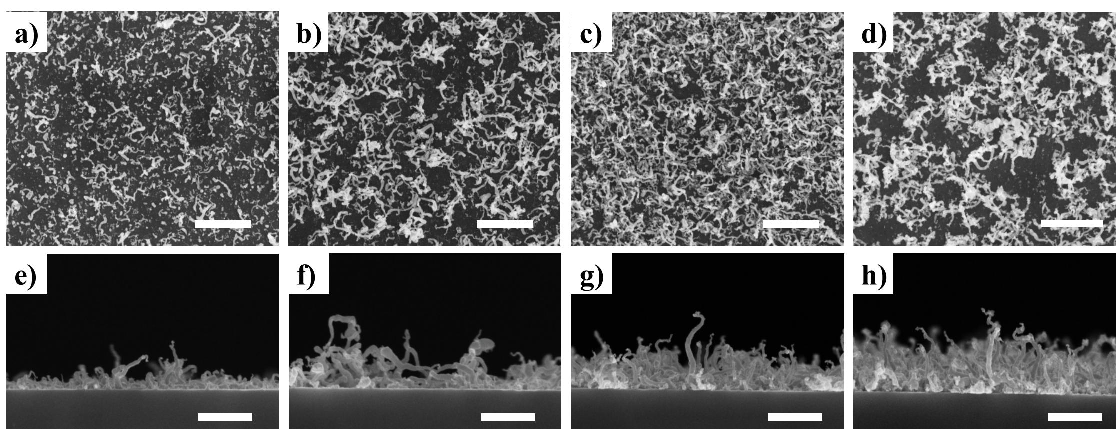

Figure 3.10. Plan-view scanning electron micrographs of Ge nanowires electrodeposited at -2.0 V vs. Ag/AgCl for a) 1 min, b) 10 min, c) 1 hr, and d) 12 hr. e)-g) Corresponding cross-sectional scanning electron micrographs showing the film thickness.

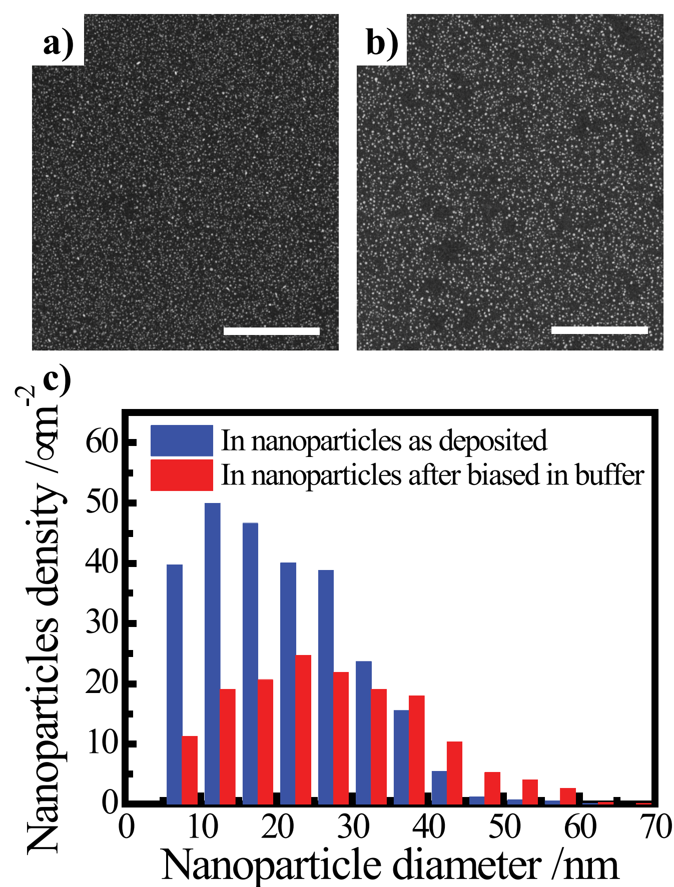

Figure 3.11. Scanning electron micrographs showing the In-coated Si substrate a) before and b) after being biased in 0.01 M $Na_2B_4O_7$ buffer at -2.0 V for 10 min. c) Histogram showing the diameter distribution of the nanoparticles shown in a) and b).

void patches observed in the plan-view micrograph after 12 hr deposition in Figure 3.10d raises the possibility of In seed/Ge nanowire loss due to H_2 evolution during prolonged ec-LLS process, as the applied -2.0 V potential was negative enough to cause H^+ reduction. The notion of surface perturbation by H_2 evolution was further demonstrated in Figure 3.11. Figures 3.11a, 3.11b show scanning electron micrographs of In-coated n-Si substrate before and after the substrate was biased in a 10 mM $Na_2B_4O_7$ buffer at -2.0 V for 10 min. Random empty regions free of In nanoparticle were observed on the substrate after the cathodic process, providing direct evidence of In nanoparticle loss as a result of H_2 evolution. Further statistical analysis (Figure 3.11c) revealed that In nanoparticles with sizes smaller than 25 nm were preferentially removed.

Additional measurements were performed to elucidate the location of the In nanoparticle following electrodeposition of a Ge nanowire. Figure 3.12 presents a set of micrographs highlighting the secondary electron image of a single electrodeposited Ge nanowire and energy dispersive spectroscopic (EDS) maps of Ge and In, respectively. EDS Ge mapping (Figure 3.12b) showed the nanowire was composed of Ge with no detectable In throughout the length. Similarly, In mapping (Figure 3.12c) showed localized concentrations of In only at the base of the Ge nanowire and not at the tip, as described in Figure 3.1b. A second nanowire located at the top left corner and a second In nanoparticle at the top right corner of Figure 3.12a were also observed (denoted with arrows in Figures 3.12b and 3.12c, respectively). The presence of a metallic nanoparticle at the base of each Ge nanowire suggested that every Ge nanowire was electrically addressable and accordingly electrochemically active. To test this hypothesis, the activity of as-prepared Ge nanowire film electrodes as Li^+ battery anodes was explored. For Li^+ battery applications, Ge is an attractive anode material since it has a larger theoretical charge-discharge capacity than graphite (1624 mA h g^{-1} for $Li_{4.4}Ge$ vs. 372 mA h g^{-1} for LiC_6) and supports faster Li^+ diffusivity than Si, facilitating Li^+ batteries with faster charge-discharge times.[16-21] A critical disadvantage with Ge as an electrode in Li^+ batteries is the large volumetric expansion upon Li^+ insertion which effectively pulverizes the material and limits the total lifetime of the electrode. In this capacity, the as-prepared Ge nanowires prepared here should show both high and long-lasting Li^+

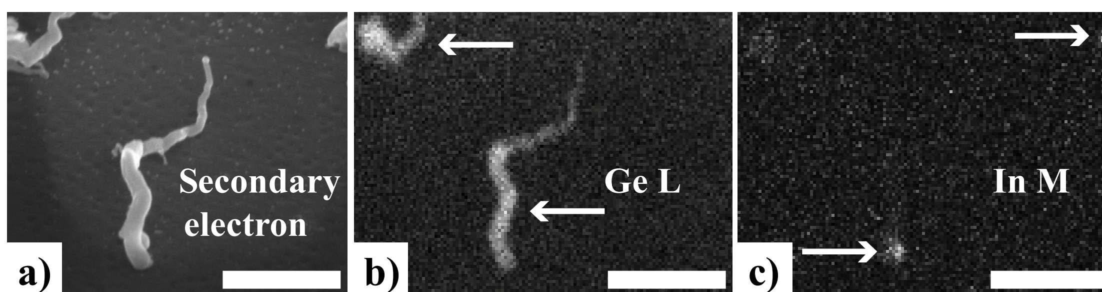

Figure 3.12. a) Secondary electron scanning electron micrograph of an individual Ge nanowire electrodeposited at -2.0 V vs. Ag/AgCl for 10 min. b), c) Energy dispersive spectroscopic elemental mapping of same area in a) with the detector channel for b) the *L* line for Ge or c) the *M* line for In. Images were collected with the sample tilted at 45°. Scale bars: 500 nm. Arrows highlight features of interest as discussed in the text.

charge-discharge capacities specifically due to their nanostructured, high aspect ratio electrode form factor. Since Si can also alloy with Li, a copper (Cu) foil was used as the electrode support for Ge nanowire electrodeposition for films that were interrogated as potential Li^+ battery electrodes.

Figure 3.13a shows the appearance of a ca. 0.5 cm^2 Cu support before and after the Ge ec-LLS preparation step on Cu, highlighting the dark color of an as-prepared, dense Ge nanowire film. These Ge nanowire film electrodes were dried, massed, and then immediately tested as Li^+ battery electrodes in a Swagelok cell (Figure 3.13b) without any further processing and/or application of binding agents or conductive carbon additives. The capacity and stability for Li^+ insertion-deinsertion of as-prepared Ge nanowires films were assessed in a two electrode configuration with 1 M $LiPF_6$ in 2:1 (v/v) ethylene carbonate/diethyl carbonate. Figure 3.14a shows the as-recorded 1st, 2nd, 3rd, and 26th charge-discharge curves for an electrodeposited Ge nanowire film electrode recorded at 1C rate. The general profile of these chronopotentiograms mirrors previous reports of crystalline Ge charge-discharge curves at this C-rate.[16-20,22] Similarly, the notable drop off in charging capacity after the first cycle is in accord with the known irreversible film formation at the solid-electrolyte interface of Ge Li^+ battery electrodes.[17,18] Control experiments performed with just the Cu foil and the Cu foil coated with In nanoparticles showed markedly different electrochemical behavior and much lower capacities for storing Li^+ The magnitude of the measured discharge capacity supports the notion that all of the Ge nanowires are electrochemically active. Figure 3.14b summarizes the as-recorded cycling data for an entire 26 cycle sequence. Following the second charge-discharge cycle, every subsequent cycle occurred with greater than 91 % coulombic efficiency. The discharge capacity slowly decreased over the course of the entire cycling period, dropping by less than 25% from the first to the twentieth discharge. A decrease in capacity over repeated cycles is common in Li^+ battery electrodes composed of Group IV elements that alloy with Li due to pulverization from extreme volumetric expansion. Scanning electron microscopy (Figure 3.15) conducted for the Ge nanowires before and after the battery cycling experiments revealed the Ge nanowires maintained the nanowire morphology after the battery test but experienced

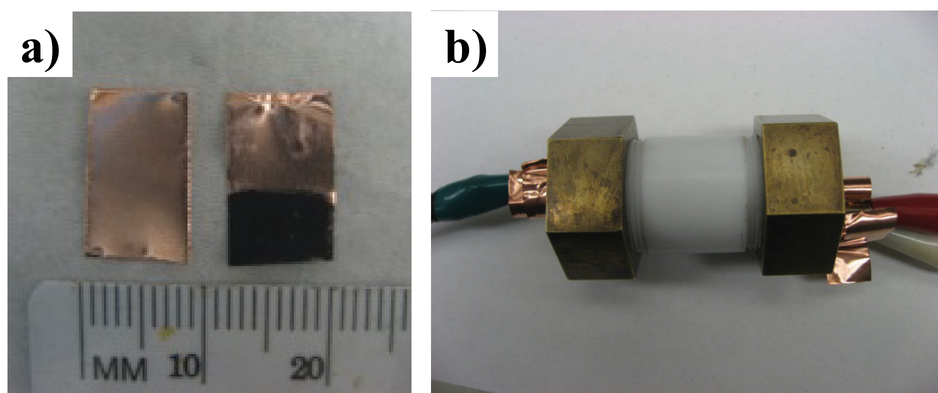

Figure 3.13. a) Optical image showing a Cu electrode support before and after Ge nanowire film electrodeposition. b) Optical image of a Swagelok battery test cell used for the capacity measurement.

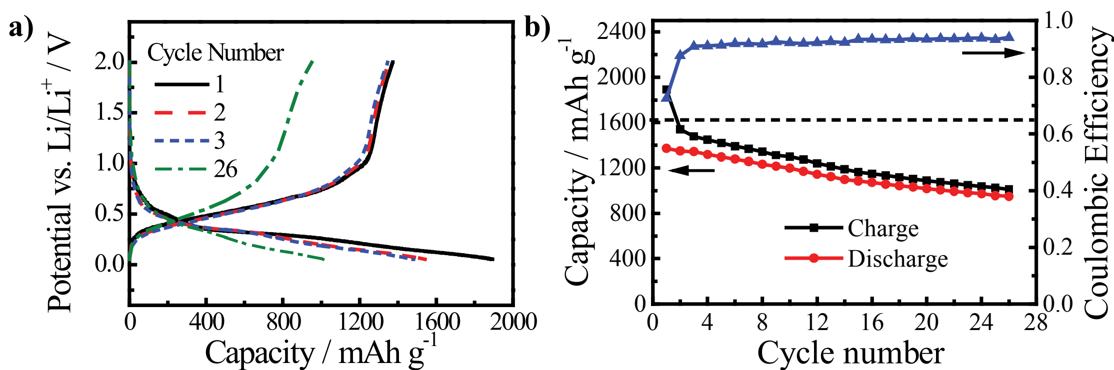

Figure 3.14. a) First, second, third, and twenty-sixth charge-discharge curves for a Li^+ anode recorded at 1C rate using an as-prepared Ge nanowire film electrodeposited onto a Cu support from 0.01 M $Na_2B_4O_7$(aq) and 0.05 M GeO_2(aq). b) Galvanostatic Li^+ (black squares) charge and (red circles) discharge cycling at 1C rate using an as-prepared Ge nanowire film electrodeposited onto a Cu support from 0.01 M $Na_2B_4O_7$(aq) and 0.05 M GeO_2(aq). (blue triangles) The coulombic efficiencies for each charge-discharge cycle are indicated on the right y-axis.

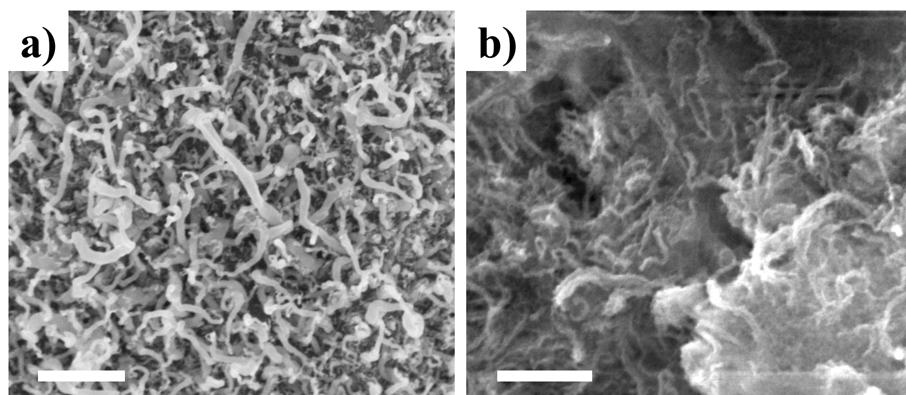

Figure 3.15. a) Scanning electron micrographs of Ge nanowires electrodeposited on In-coated Cu electrodes. In catalysts were electrodeposited at -2.0 V for 30 sec from 0.1 M $InBr_3$, 0.1 M KNO_3 and Ge nanowires were subsequently electrodeposited at -2.0 V for 1 hr from 0.05 M GeO_2, 0.01 M $Na_2B_4O_7$. b) Scanning electron micrograph showing the same electrode after charge-discharge cycling at 1 C rate for 20 cycles.

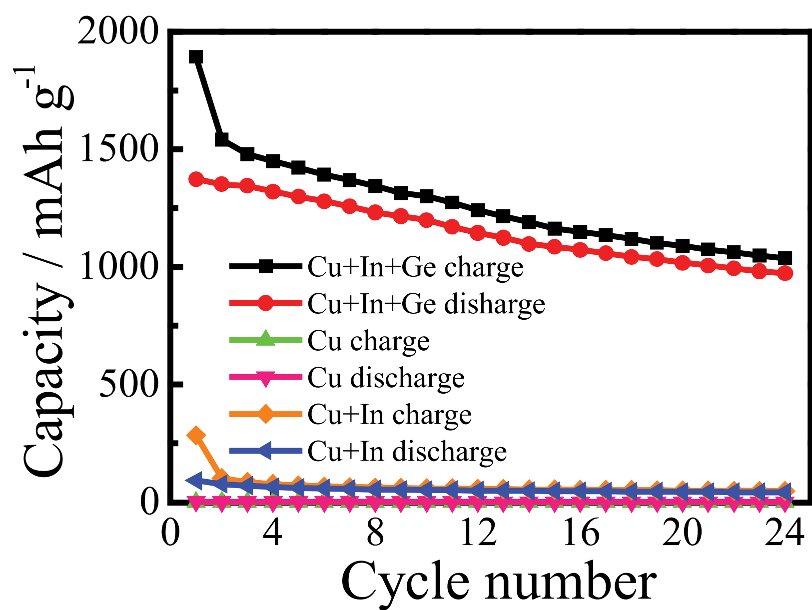

Figure 3.16. Li^+ charge and discharge capacities at 1C rate as a function of repetitive cycling for 1) bare Cu substrate, 2) In-coated Cu substrate and 3) Ge nanowires film on In-coated Cu substrate.

Table 3.1. Reported Discharge Capacity for Ge Li^+ Insertion Anodes[a]

Morphology	*Capacacity /mA h g^{-1}*	*Notes*	*Reference*
bulk	<< 100	obtained at C/4 after 7 cycles	17
thin film	600	evaporated under vacuum	17
nanostructured thin film	1000	obtained at C/0.9, ion beam modified for nanostructuring	22
nanoparticles	1460	prepared from $GeCl_4$ in dimethoxyethane, dried at 200 °C, butyl-capped	18
nanotubes	765	prepared at 700 °C with Sb, coated with amorphous carbon	23
nanoporous film	1415	prepared from $GeCl_4$, annealed at 800 °C, coated with amorphous carbon	21
nanowires	597	prepared from GeH_4 via VLS at 520 °C, annealed at 320 °C	19
nanowires	970	electrodeposited from GeO_2(aq) at room temp, no annealing	*this work*

a. reported at 1C after 20 cycles unless noted otherwise

Table 3.2. Measured Li^+ charge and discharge capacity for Ge nanowires film electrodes[a]

Sample	*Charge capacacity /mAh g^{-1}*	*Discharge capacacity /mAh g^{-1}*	*Coulombic efficiency*
I	733	713	0.973
II	936	902	0.964
III	804	782	0.973
average		800 ± 95[b]	

a. obtained at 5C at 20th cycle for Ge samples deposited at -2.0 V for 1hr

b. average ± 1σ

considerable roughening at the surface, supporting the notion of pulverization under cycling stress. However, the capacity decay shown here is much less pronounced than for a planar crystalline Ge film (no effective Li^+ capacity after only seven cycles),[17] indicating the form factor of the as-electrodeposited Ge nanowires natively imparts stability against pulverization.

The corrected charge and discharge capacity for the electrodeposited Ge nanowire film electrodes shown here have been adjusted for Li^+ capacity contributions from other components in the sample, i.e. contributions from the underlying Cu substrate and In seed. The correction was carried out by measuring Li^+ charge-discharge capacity of Cu substrates and In-coated Cu substrates in 1 M $LiPF_6$ 2:1 (v/v) ethylene carbonate and diethyl carbonate solution at identical charging current density used for Ge nanowire electrodes. Figure 3.16 summarizes representative capacity cycling responses for Ge nanowire film electrodes (electrodeposited at -2.0 V vs. Ag/AgCl for 10 min in 0.01 M $Na_2B_4O_7$(aq) and 0.05 M GeO_2(aq)), Cu electrodes coated with In nanoparticles (electrodeposited at -2.0 V vs. Ag/AgCl for 30 sec in 0.1 M $InBr_3$(aq) and 0.1 M KNO_3(aq)), and bare Cu electrodes. Figure 3.17 shows representative potential-capacity curves for the 20th cycle for Ge nanowire film electrodes, Cu electrodes coated with In nanoparticles, and bare Cu electrodes. Bare Cu electrodes exhibited no meaningful Li^+ capacities while Cu electrodes coated with In nanoparticles supported discharge capacities of 50 mA h g^{-1}, i.e. less than 5% of the measured capacity of the Ge nanowire film electrodes.

To gauge the overall performance quality of these Ge nanowire film electrodes prepared via ec-LLS, Table 1 summarizes the reported capacity benchmarks for related Ge materials as Li^+ battery anodes at 1C and includes the results of this work. As evident from Table 1, the discharge capacity at 1C for the Ge nanowires prepared here via ec-LLS compare favorably with other Ge nanomaterials, approximately 160% larger than the previous reported capacity of Ge nanowire film electrodes prepared through high temperature VLS.[16] Only two reports have shown Ge nanomaterials with markedly larger discharge capacities after 20 cycles, achieved by adding a carbon coating for stability.[18,20] A comparison of those data[18,20] and the responses shown here show that the discharge

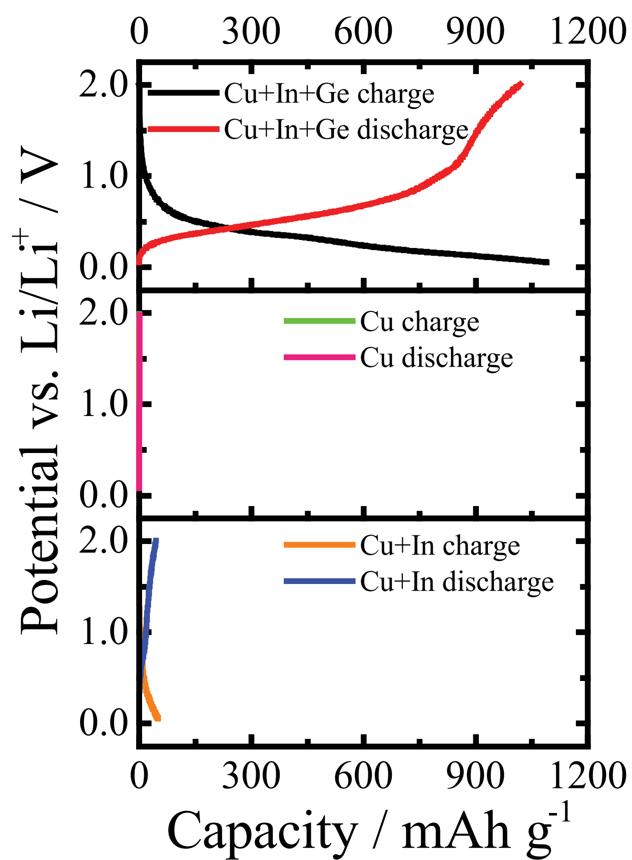

Figure 3.17. Twentieth charge-discharge curves for (top) an as-prepared Ge nanowire film electrodeposited onto a Cu electrode, (middle) a bare Cu electrode, and (bottom) a Cu electrode coated with In nanoparticles.

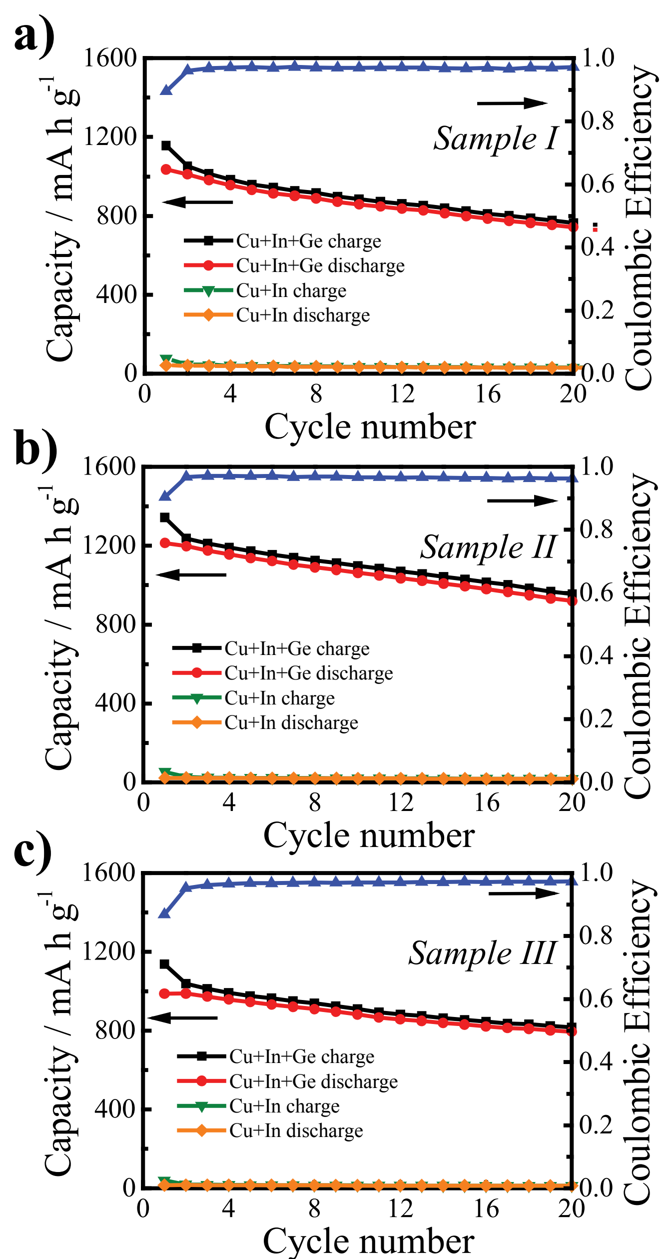

Figure 3.18. Li^+ charge and discharge capacities at 5C rate as a function of repetitive cycling for three separately prepared Ge nanowire film electrodes. Ge nanowires were electrodeposited at -2.0 V for 1 hr from 0.05 M GeO_2, 0.01 M $Na_2B_4O_7$ for all three electrodes.

capacities at the initial cycles are nominally equivalent. The polycrystalline nature of these Ge nanowires, particularly the randomized orientation of the crystallites along the nanowire long axis which presents lattice planes favorable for Li^+ insertion, is the likely source for the high capacities exhibited by the as-prepared Ge nanowire film electrodes. Although no additional measures were taken to stabilize and/or augment the native Li^+ capacities measured here, separate coating strategies[18,20] could in principle be applied to the materials presented here to impart added stability. Moreover, the Ge nanowire film electrodes investigated here were not rigorously optimized in terms of nanowire diameter, density, or length. Further refinements in these parameters ought to lead to improved performance characteristics. A final point to consider about the activity of these Ge nanowire film electrodes is the reproducibility of this method of preparation. Table 2 and Figure 3.18 summarize the cycling data recorded at a faster charge-discharge rate (5C) for several separately electrodeposited Ge nanowire film electrodes. Using the unrefined conditions used here, capacity values varied by less than 12 % between different electrodeposited Ge nanowire film electrodes.

D. Discussions

The cumulative data indicate that ec-LLS is a viable and simple bottom-up strategy for directly producing functional Ge nanowire electrodes for energy conversion devices. These results highlight several advantages that ec-LLS has over both VLS and SLS strategies as well as alternative physical-template-based electrochemical nanowire syntheses[23,24] for this purpose. Both VLS and SLS routes for Ge nanowire growth require high (>300 °C) temperatures.[25,26] Physical-template-based electrochemical strategies similarly require a high temperature annealing step to effect an amorphous to crystalline transition.[23,24] The data here illustrate that nanowires are crystalline when prepared through the ec-LLS route and require no subsequent annealing. Both VLS and SLS methods as well as physical-template-based electrochemical methods require high energy density, partially reduced chemical precursors such as GeH_4,[27] $GeCl_4$,[28] GeI_2[25] or diphenylgermane[29]. As embodied here, the ec-LLS process for Ge nanowires used a fully oxidized precursor (GeO_2) as the feedstock. For the purposes of making electrodes, VLS requires growing nanowires on a substrate that can withstand high temperatures while

SLS requires separate processing steps for collecting and attaching nanowires to a current collector.[30,31] As shown here, the ec-LLS process yielded crystalline Ge nanowires directly on a variety of conductive substrates. VLS, SLS, and traditional electrochemical synthetic strategies do not tolerate the presence of water.[10,23,24] For Ge nanowires, the results show ec-LLS can be readily performed in an aqueous electrolyte that does not have to be either caustic or highly acidic. Template-based electrochemical methods require a hard, physical mold to define particular nanostructured morphologies. No physical or chemical templates were needed to control nanowire diameters or densities through the ec-LLS method.

Several additional factors regarding ec-LLS must be developed to further expand its utility. A quantitative description of how the interplay between the relative rates of mass transport in solution, electroreduction, dissolution, crystal nucleation, and precipitation impact the crystallinity, morphology, and conductivity of the electrodeposited semiconductor material is needed to prepare crystalline materials with precisely tunable morphological and electronic properties. For example, for applications such as solar energy conversion, the tolerances for concerted shape and doping properties in semiconductor nanowire electrodes are low[32,33] and more stringent than for battery applications. Accordingly, a better understanding of the ec-LLS process will enable a wider breadth of potential applications. Similarly, demonstration of controlled ec-LLS preparations of additional semiconductor material types is needed. In this regard, identification of the entire possible set of liquid metal 'flux' electrode materials would be advantageous, as different liquid metal electrode types may enable the electrosynthesis of new semiconductor materials. Work dedicated to these points is ongoing in our lab and will be reported separately.

E. Conclusions

The cumulative data show that the ec-LLS process for crystalline Ge previously observed at liquid Hg electrodes also occurs at small, discrete In nanoparticles supported on either n-type silicon (Si) or copper (Cu) electrode substrates. The presented results indicate that the size and density of the crystalline Ge nanowires are readily tunable through control of the parent In nanoparticles and that each electrodeposited Ge nanowire

is in direct electrical contact with the underlying electrode support through the In nanoparticle at the base of each nanowire. The activity of the as-prepared Ge nanowire film electrodes was competitive with existing, alternative protocols for producing nanostructured Ge battery anodes, with the important caveats that the method developed here was simpler, less energy-intensive, and was performed entirely under benchtop conditions. Overall, the salient feature of this work is the demonstration of ec-LLS as a method to prepare directly a functional, high-activity nanomaterials-based *device* component. The dataset shown here is a step towards the realization of simple processes that make fully functional energy-conversion technologies entirely through benchtop chemistry and electrochemistry.

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CHAPTER 4

Room-Temperature Epitaxial Electrodeposition of Single-Crystalline Germanium Nanowires

A. Introduction

This chapter details the direct epitaxial growth of single-crystalline germanium (Ge) nanowires at room temperature by an aqueous electrodeposition process. The nanowire morphology is studied by plan-view and cross-sectional scanning electron microscopy. The crystal details of the as-deposited nanowires including crystallinity, growth orientation and crystal defects are investigated. Current-voltage responses measured across many individual nanowires yielded reproducible resistance values. The presented data cumulatively show epitaxial growth of covalent group IV nanowires is possible from the reduction of a dissolved oxide under purely benchtop conditions.

The ability to synthesize structurally and electrically integrated group IV semiconductor nanowire arrays directly onto device platforms is desirable for continued minimization of transistor footprints.[1-6] However, the stringent purity and thermal constraints associated with complementary metal oxide semiconductor (CMOS) technologies are incompatible with the temperatures, growth catalysts, and environments currently used to synthesize covalent inorganic semiconductor nanowires.[7-10] In comparison, electrodeposition is an alternative synthetic method for nanowires that bypasses these constraints. Still, although heavily used for metallization in the semiconductor industry,[11,12] electrodeposition is not presently used for covalent semiconductor nanowires because exotic solvents are necessary[13] and the resultant material is amorphous,[14] requiring high temperature refining.

So far, major evolution in the capacity of benchtop electrochemistry has been demonstrated in preparing crystalline covalent semiconductor nanomaterials at room temperature (Figure 4.1a). The key distinguishing feature of an ec-LLS process is the use

of a liquid metal both as an electron source for the heterogeneous electrochemical reduction of dissolved species (i.e. as a conventional electrode) and as a separate phase for crystal growth (i.e. as a melt solvent). An oxidized semiconductor precursor is initially electrochemically reduced and then dissolves into, or reacts with, the liquid metal electrode. As the liquid metal reaches saturation and then supersaturation conditions, concomitant precipitation of crystalline material follows.[15-18] To date, only polycrystalline materials have been prepared by ec-LLS without any discernible control over the crystal growth orientation.[15-18]

This chapter advances three separate hypotheses regarding the development of ec-LLS as a nanomaterials synthetic strategy: (*1*) liquid Ga nanodroplets represent a platform for high yield Ge nanowire ec-LLS at room temperature; (*2*) *single-crystalline* Ge nanowires can be prepared from an aqueous solution at room temperature with liquid metal nanodroplets; and (*3*) *epitaxial* crystal growth for a covalent semiconductor is possible electrochemically with liquid metal nanodroplets at room temperature.

B. Methods

Materials and Chemicals Methanol (ACS grade, BDH), acetone (ACS grade, BDH), GeO_2 (99.999%, Acros Organics), $Na_2B_4O_7\cdot 10H_2O$ (Analytical Reagent Grade, Mallinckrodt), hydrofluoric acid (49%, Transene Inc.), KNO_3 (99+%, Acros Organics), In(*s*) (99.9+%, Aldrich) and Ga(*l*) (99.99%, Aldrich) were used as received. Wafers used as growth substrates included Ge (MTI, <111> Sb-doped n-type, 24.8 – 30.0 ohm cm, 0.5 mm thick), Ge (MTI, <100> Sb-doped n-type, 0.2 – 0.23 ohm cm, 0.5 mm thick), Si (Crysteco, <100> As-doped n-type, < 0.007 ohm cm, 0.625 ± 0.020 mm thick). Water with a resistivity > 18.2 MΩ cm (Barnsted Nanopure) was used throughout.

Electrodeposition and Electrochemical Measurements A CHI760C workstation was used for electrochemical experiments. All electrochemical data were acquired under open atmosphere in either a custom-made PTFE cell with 0.101 cm^2 exposed area (small scale) or in 400 mL glass beaker (wafer-scale). A standard three-electrode configuration with a Pt mesh counter electrode and a Ag/AgCl (sat. KCl) reference electrode was employed. All reported electrochemical potentials are with respect to E(Ag/AgCl)(sat. KCl). Electrical contact to either Ge or Si wafer substrates was established by applying a

thin layer of InGa eutectic on the back of the wafer and pressing the substrate against a thin stainless steel electrode support. Electrodeposition of Ge nanowires was conducted in a temperature-controlled recirculating bath (Polystat) held at 40 °C. Gallium nanodroplets were electrodeposited on Ge(111) or Si(100) substrates from a solution containing 0.1 M $Ga(NO_3)_3$ and 0.1 M KNO_3 at a potentiostatic bias of -1.6 V for 5 s. Samples were rinsed in DI H_2O for 30 s and dried under $N_2(g)$.

Scanning and Transmission Electron Microscopy TEM samples for dispersed nanowires were prepared by first removing the nanowires from the growth substrate using a razor blade. The razor blade was then sonicated in a glass vial containing 1 mL of methanol for 30 min to fully disperse the nanowires in the solvent. 100 μL of the nanowire suspension was drop-cast on a 400 mesh copper TEM grid coated with an ultra-thin carbon film (Ted Pella). Cross-sectional TEM samples were prepared by mechanical polishing as described here.[19] Briefly, a 1.5 x 2.5 mm rectangular section was cut from a Ge wafer containing the as-grown wires and glued face-to-face between two clean Si pieces of equivalent dimension. Samples were mounted on a tripod polisher (Precision TEM) and mechanically polished to a thickness of 10 μm. They were transferred onto a slotted Ni TEM grid (Ted Pella) and thinned to electron transparency using cryo-Ar^+ ion milling (-160 °C) at 4.5 keV for 3.5 h. High resolution transmission electron microscopy (HRTEM) were conducted with a JEOL 2010F analytical microscope equipped with a zirconiated tungsten (100) thermal field emission source at 200 keV acceleration voltage as well as a JEOL 3011 high resolution electron microscope equipped with a LaB_6 source operated at 300 keV. All HRTEM images were recorded along the $[1\bar{1}0]$ zone axis of the Ge crystal. Scanning transmission electron microscopy (STEM) was conducted using the JEOL 2010F analytical microscope with 1.0 nm probe size and 8 cm camera length. Energy dispersive X-ray maps were generated using 500 μs dwell time per pixel each frame at 512x400 resolution using an EDAX r-TEM Detector. Scanning electron microscopy was performed with an FEI NOVA Nanolab Dualbeam Workstation with a Schottky field emitter operated at 15 keV beam voltage and 0.14 nA beam current coupled with a through-the-lens detector (TLD). Cross-sectional images were collected with the vertically-mounted substrate tilted 4° towards the substrate surface plane.

Molecular Beam Epitaxy Gallium (Ga) droplets were prepared on Ge(111) wafers by molecular beam epitaxy. Prior to growth, the substrate was cleaned chemically by dipping in HCl(36 %)/H_2O 1:4 solution for 30 s to remove native GeO_2. Substrates were introduced into the load-lock of the GEN II MBE chamber within 10 min of etching. The load-lock was baked at 150 °C for 8 hours prior to substrate transfer into the MBE growth chamber. Substrates were heated at 800 °C for 30 min in the growth chamber, at which point a streaky RHEED pattern was observed revealing a smooth Ge surface free of GeO_2. The substrate temperature was reduced to 550 °C for growth and Ga droplets were deposited at a constant Ga beam equivalent pressure of 3.7 x 10^{-7} torr for 10 s, corresponding to 7.5 ML of Ga.

Conducting Probe Atomic Force Microscopy (AFM). Conducting probe AFM measurements were made with a Veeco Dimension 3100 AFM equipped with the extended TUNA module. Ohmic contacts were made to the Ge substrates by abrasion with a diamond scribe, 60 s etch in 5 % HF(aq) and the application of indium-gallium eutectic. Mikromasch NSC15 cantilevers were used for tapping mode images. Platinum wire probes (25Pt300B, Rocky Mountain Nano) were used as top-contacts for CP-AFM experiments. Cantilever displacements of 5 nm were used, resulting in probe-sample forces of ca. 100 nN. Nanowires of interest were centered in scan areas of decreasing size until two successive scans showed acceptably small piezo creep, allowing current-voltage curves to be obtained on the top of the nanowire. During these measurements, the probe is held at virtual ground and the sample bias is ramped. Subsequently, a much larger force (ca. 1 μN) was applied and the probe was allowed to scan until the nanowire was broken off and pushed out of the image area. The same procedure was then followed to obtain current-voltage curves on the nanowire “stump”. Before measuring the I-V response for the bare Ge substrate, additional bias cycling from -10 to 10 V was applied until steady I-V curves were recorded in order to locally vaporize the oxide.

C. Results

Ge nanowire films were prepared through ec-LLS with only a digital potentiostat and a standard setup of three-electrode cell shown in Figure 4.1a. The current-potential characteristics (Figure 4.1b) for Ge electrodeposition were first measured using an n-

Ge(111) electrode (R = 24.8 - 30 Ω·cm) decorated with Ga(l) nanodroplets immersed in a 0.01 M $Na_2B_4O_7$ solution with 0.05 M GeO_2. The increase in current density at potentials more negative than -1.3 V vs. Ag/AgCl corresponds to GeO_2(aq) reduction on discrete Ga(l) droplets through Reaction 1

$$HGeO_3^-(aq) + 4e^- + 2H_2O(l) \rightarrow Ge(s) + 5OH^-(aq) \qquad (1)$$

Such cathodic feature was not observed with the absence of dissolved GeO_2 in the electrolyte. Further comparison between the voltammetric response for a bare Ge(111) substrate and that of a substrate decorated with Ga(l) nanodroplets indicates the electroreduction of GeO_2 only occurred selectively in the presence of liquid Ga. Electrodeposition of Ge nanowire was then carried out potentiostatically in the same cell setup at -1.6 V vs. Ag/AgCl. Figure 4.1c illustrates the uniformity of the Ge electrodeposition film across the immersed portion of a 2-inch wafer substrate. The entire wetted fraction of the wafer developed a dull, grey film that visibly changed over the course of the ec-LLS process. Microscopically, free standing Ge nanowires with uniform density were observed, and no non-nucleated Ga(l) nanodroplets could be found over the entire field of view in the cross-sectional scanning electron micrograph after Ge nanowire deposition for 30 s on Ge(111) (Figure 4.1d). Analysis of the substrates before and after electrodeposition using cross-sectional (Figures 4.2a, 4.2b) and tilted scanning electron microscopy (Figure 2c, d) indicated the density of initial Ga nanodroplets and the density of as-prepared Ge nanowires were equivalent (3.1 ± 0.1 and 3.3 ± 0.1 μm^{-2}), i.e. every Ga nanodroplet seeded the electrochemical growth of a single Ge nanowire. The histogram of measured Ga nanodroplet diameters and Ge nanowire base widths in Figure 4.2e describes the correlation between nanodroplet and nanowire size. The resultant Ge nanowires were slightly smaller (96.6 ± 8.6 nm, N = 203) than the Ga nanodroplets (108.7 ± 10.3 nm, N = 171), but the relative standard deviations were comparable (8.9 and 9.4%, respectively). The resemblance in the size distribution profile of the initial Ga nanoparticles and the resultant Ge nanowires is indicative of the controllability of nanowire diameter by the seeding Ga nanoparticles. The location of the seeding Ga particles was revealed by high resolution transmission electron micrographs (HRTEM)

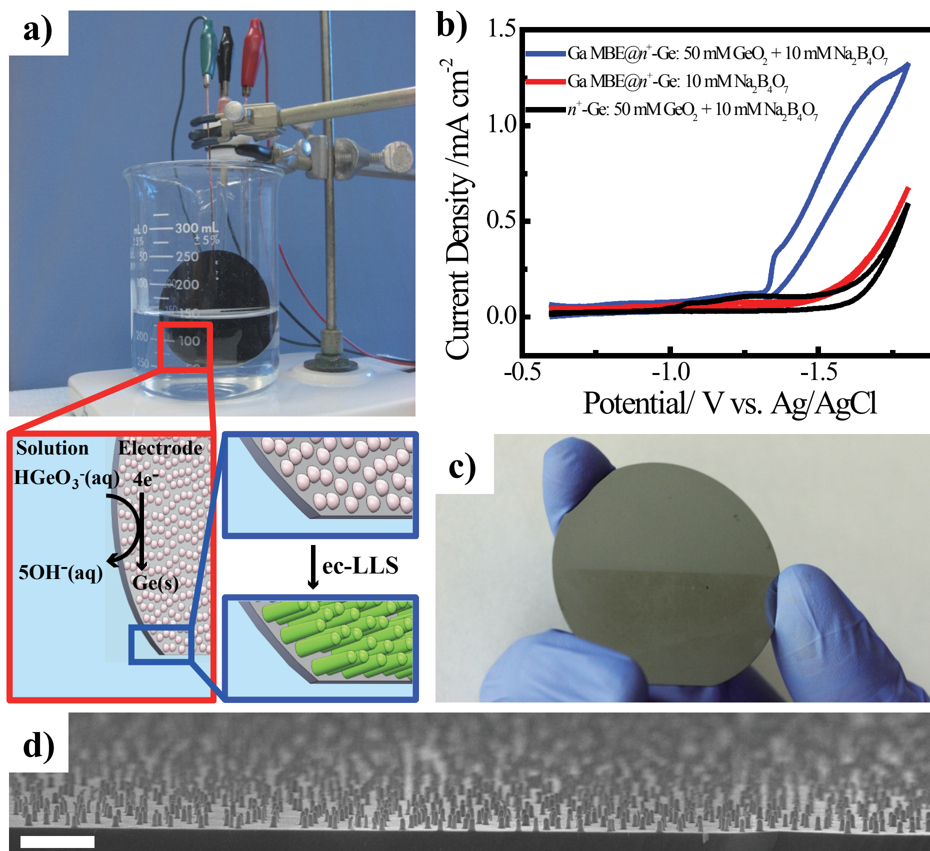

Figure 4.1. a) Optical image depicting the benchtop experimental setup used for wafer-scale ec-LLS of Ge nanowire films. Insets: Schematic depiction of ec-LLS process. b) Cyclic voltammetric response of an n-Ge(111) electrode (R = 24.8 – 30 Ω·cm) decorated with (blue) and without (black) Ga(l) nanodroplets in 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$. The current-potential behavior for the same Ga(l) decorated n-Ge(111) electrode in the absence of dissolved GeO_2 is shown in red. c) Optical image of a 2-inch wafer coated with Ge nanowires after 300 s ec-LLS nanowire deposition over the bottom half of the wafer. d) Scanning electron micrograph collected from Ge nanowires grown for 30 s from a Ge(111) substrate. Scale bar: 1 μm. ec-LLS conditions: E_{app} = -1.6 V vs. Ag/AgCl, T = 40 ± 2°C, 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$.

and X-ray energy dispersive spectroscopic (XEDS) mapping of individual Ge nanowires after a short (*t* = 30 s) ec-LLS experiment (Figures 4.2f and 4.2g). Ga enrichment was consistently observed in the elemental mapping at the tip of the growing nanowire, coincided with a visible cap in the transmission electron micrograph. Ge comprised the majority of nanowire body and no increased concentration of Ga was observed at the base of the nanowires, similar to the metal catalyst position observed in vapor-liquid-solid nanowire growth[20] but in contrast to our prior ec-LLS observations.[15,17]

The electrochemically-driven nanowire growth allows the growth kinetics to be monitored in real time based on amperometric response of the Ge(111) substrate coated with Ga nanodroplets. Analysis of the current-time transient recorded during an ec-LLS experiment at -1.6 V vs. Ag/AgCl suggested synchronized and instantaneous nucleation of Ge nanowires,[21] i.e. the growth of every Ge nanowire initiated simultaneously without a measurable induction time. The raw chronoamperometric response for a Ge(111) wafer coated with Ga(l) nanodroplets biased at -1.6 V vs. Ag/AgCl in a solution of 0.05 M GeO_2(aq) and 0.01 M $Na_2B_4O_7$(aq) is shown in Figure 4.3a. The magnitude of cathodic current decreased over time and flatlined after 150 s, indicating the majority of the nanowire growth occurred within the initial 150 s. The acute increase in current density at ~1.8 s highlighted in the Figure 4.3a inset is consistent with transient response during electrochemical deposition. To compare the experimental chronoamperometric response with common electrochemical nucleation model, current transient was normalized to the maximum current i_{max} as well as to the time at which the maximum current was obtained t_{max}. The normalized current transient along with two simulated transients based on instantaneous nucleation model and progressive nucleation model are shown in Figure 4.3b. The close agreement with the instantaneous nucleation model supports the notion that all nanowires are nucleated simultaneously. Figures 4.3c and 4.3d show the cross-sectional scanning electron micrograph of Ge nanowires grown for 30 s and the corresponding height histogram. The narrow height distribution of 125 ± 9 nm (N = 196) for Ge nanowires prepared by the ec-LLS process separately supported the notion that wire growth initiates at the same time and proceeds at a nominally identical rate over the growth duration.

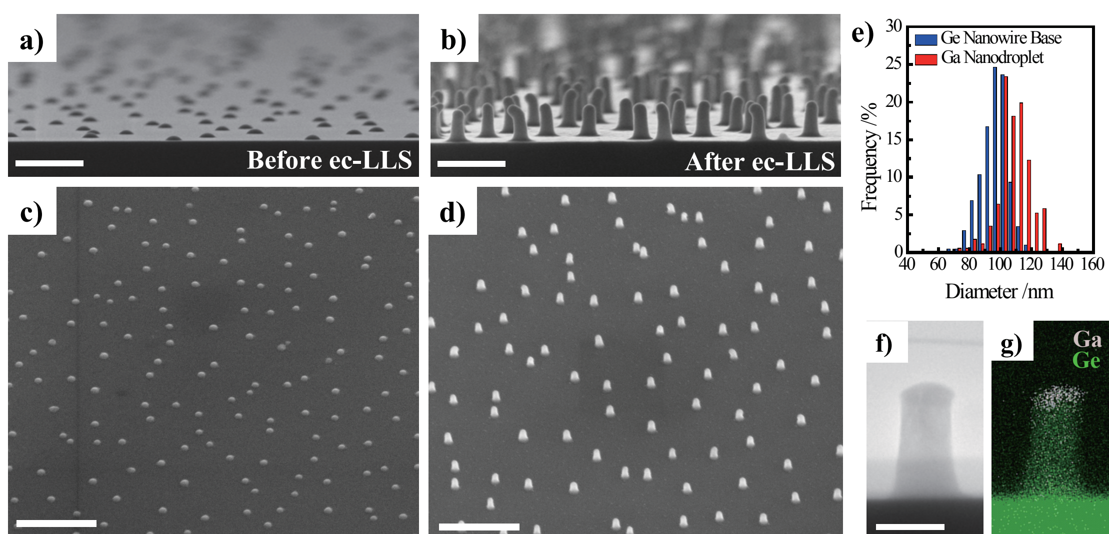

Figure 4.2. Cross-sectional scanning electron micrograph of a Ge(111) substrate decorated with discrete liquid Ga nanodroplets a) before and b) after a 30 s ec-LLS process. Scale bar: 500 nm. c) 40 ^{o} tilted scanning electron micrograph of the same substrate c) before and d) after a 30 s ec-LLS process. Scale bar: 1 μm. e) Size distribution of the Ga nanodroplet electrodes and resultant Ge nanowire base widths obtained after a 30 s ec-LLS experiment. f) Cross-sectional high resolution transmission electron micrograph of an as-prepared single Ge nanowire on a wafer substrate produced after a 30 s ec-LLS. Scale bar: 100 nm. g) Energy dispersive X-ray spectroscopic elemental map of the structure in (f). ec-LLS conditions: E_{app} = -1.6 V vs. Ag/AgCl, T = 40 ± 2°C, 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$.

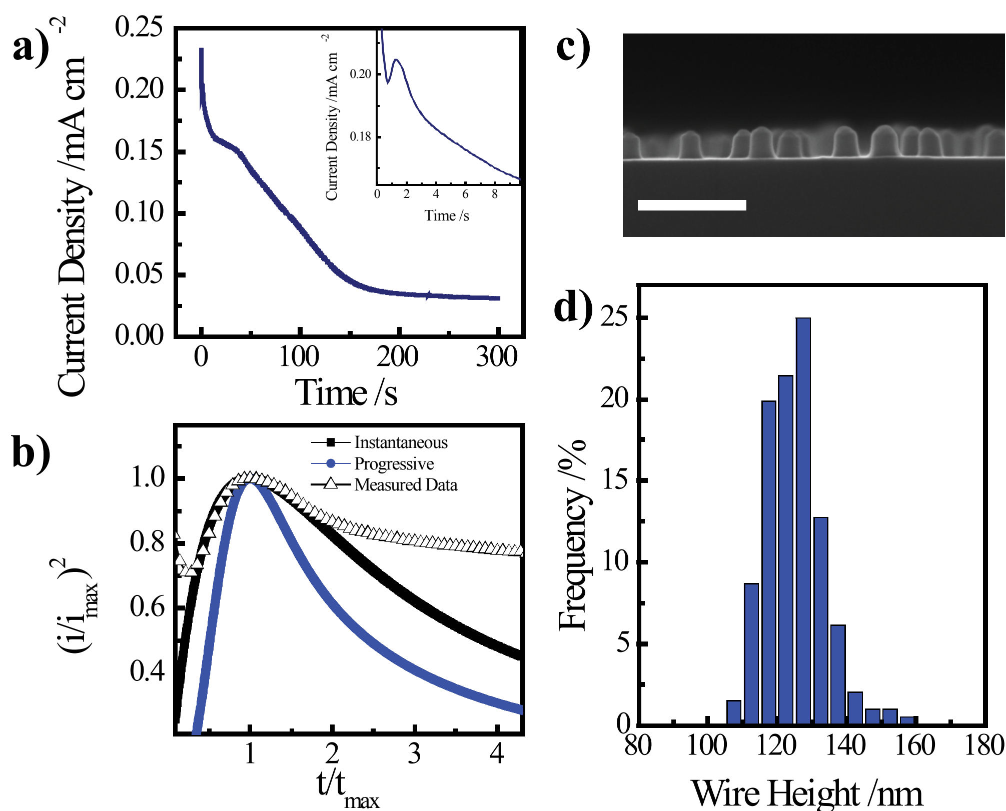

Figure 4.3. a) Chronoamperometric response for an n-Ge(111) electrode coated with Ga(l) nanodroplets in 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$ biased at -1.6 V vs. Ag/AgCl for 300 s. Inset highlights the first 10 s of the current profile. b) Same current-transient data with current density normalized to the peak current density and time normalized to the time with maximal current (triangle). Models for progressive (blue line) and instantaneous (black line) nucleation models are also shown. c) Cross-sectional scanning electron micrograph of Ge nanowires grown for 30 s at -1.6 V vs. Ag/AgCl. Scale bar: 500 nm. d) Corresponding histogram of Ge nanowire heights (N = 196) after 30 s extracted from SEM images.

Electron microscopy was performed to assess the crystallinity of individual nanowires and to identify any evidence of preferred growth orientation. Representative cross-sectional and plan-view scanning electron micrographs (SEM) collected after a short (t = 30 s) ec-LLS experiment on a Ge(111) wafer substrate are shown in Figures 4.4a and 4.4b, respectively. Short ec-LLS experiments were specifically analyzed to avoid mechanical perturbation of nanowire orientation from capillary forces during drying.[22] As shown in the cross-sectional scanning electron micrograph, every Ge nanowire across the entire field of view was oriented normal to the substrate plane, i.e. collinear with the [111] direction of the wafer substrate. In the plan-view micrograph, the projection of all extruded nanowires was confined within the circular base with no off-axis growth observed. The regularity in the initial vertical nanowire orientation observed in Figures 4.4a and 4.4b supports the notion of an epitaxial crystal growth process along [111] growth direction on a [111] substrate.[23] To further test the possibility of epitaxy, cross-sectional transmission electron micrographs were collected of the interface between the as-grown Ge nanowire and the Ge(111) substrate. Figure 4.4c depicts the atomically resolved interface between the Ge nanowire and the substrate. As shown in the highlighted region, the substrate/nanowire boundary revealed no evident discontinuities in the crystal lattice. Atomic arrangement on both sides of the interface showed identical pattern matching that of the diamond cubic Ge crystal structure viewed along the [110] zone axis. Two Lattice spacings of 3.31 and 2.86 Å were measured, respectively, consistent with the d_{111} and d_{200} spacings of a single Ge crystal.[24] Further evidence of epitaxial growth was provided by the selected area electron diffraction (SAED) pattern in the inset of Figure 4.4c. The electron diffraction pattern, acquired over the interfacial region between the Ge nanowire and substrate revealed a single set of diffraction spots of Ge lattice viewed along the [110] zone axis. Separately, XEDS mapping showed no detectable concentration of Ga at the substrate/nanowire interface. Moiré fringes, additional diffractions spots, or diffuse rings in the collected diffraction patterns suggestive of GeGa alloys were not observed. Collectively, these data argue that crystalline Ge nanowires were epitaxially deposited on Ge(111) substrates via ec-LLS. Evidence supporting homoepitaxial and heteroepitaxial Ge nanowire growth on other

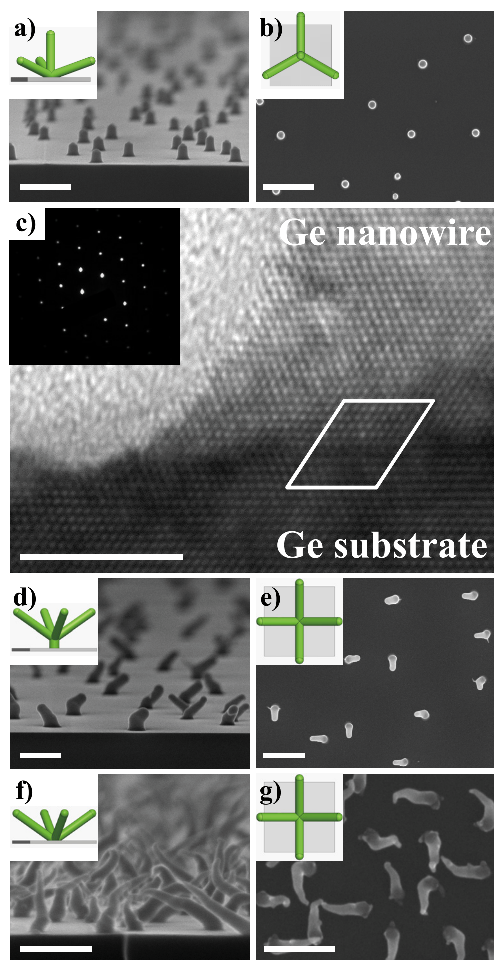

Figure 4.4. Scanning electron micrographs showing Ge nanowire orientations grown from various electrode substrates. a) Cross-sectional view and b) top-down (plan) view of Ge nanowire films prepared through a 30 s ec-LLS experiment on an n^+-Ge(111) electrode substrate. Scale bar: 500 nm. Insets: possible orientation for nanowire growth along any <111> direction from a (111) substrate. c) A high resolution transmission electron micrograph cross-sectional view of the interface between the base of a Ge nanowire prepared by ec-LLS and the n^+-Ge (111) substrate viewed along the [110] zone axis. Scale bar: 5 nm. Inset: selected area electron diffraction pattern collected over the nanowire/substrate interface. d) Cross-sectional view and e) plan view of Ge nanowire films prepared through a 30 s ec-LLS experiment on a degenerately doped n^+-Ge(100) electrode substrate. Scale bar: 500 nm. Insets: possible orientation for nanowire growth along any <111> direction from a (100) substrate. f) Cross-sectional view and g) plan view of Ge nanowire films prepared through a 30 s ec-LLS experiment on a degenerately doped n^+-Si(100) electrode substrate. Scale bar: 200 nm. Insets: possible orientation for nanowire growth along any <111> direction from a (100) substrate. ec-LLS conditions: E_{app} = -1.6 V vs. Ag/AgCl, T = 40 ± 2 °C, 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$.

substrate orientations was also collected (Figures 4.4d and 4.4e). In Figure 4.4d, electrodeposition of Ge on Ga-coated Ge(100) substrate resulted in collinear nanowire growth in the lowest portion directly above the surface plane, which suggests initial epitaxial growth along <100> direction. Above this height, the Ge nanowires showed a change in orientation with respect to the surface plane. As seen in Figure 4.4e, the nanowire growth continued at four distinct angles with 90° in-plane angle separation. This orientation is consistent with continued crystal growth along the <111> direction off a (100) crystal base, as depicted in the schematic (inset). Heteroepitaxy on lattice mismatched substrates is also shown (Figures 4.4f and 4.4g). In Figure 4.4f, Ge nanowire electrodeposition on Si(100) substrates resulted in wires oriented 36 ± 3° from the surface plane. The plan view image in Figure 4.4g additionally reveals nanowires oriented along four separate 90° relative in-plane angles. This observation is in accord with epitaxial crystal orientation along the four possible <111> directions on a (100) substrates. In combination, the data implicate the capacity to perform homoepitaxy and heteroepitaxy through ec-LLS.

Additional analyses were performed to determine whether the electrodeposited Ge nanowires remained single-crystalline throughout the course of longer ec-LLS experiments. Cross-sectional scanning electron microscopy indicated that nanowires prepared by a 60-sec ec-LLS process on Ge(111) wafers uniformly showed an initial vertical growth followed by at least one kink and concomitant change in crystal growth direction (Figure 4.5a). Statistical analysis of 102 randomly chosen nanowires revealed an average vertical height of 185.7 ± 25.8 nm (Figure 4.5b) prior to the first kink. Figure 4.6a shows a transmission electron micrograph of a representative Ge nanowire prepared by ec-LLS for 300 s (the coating apparent in the micrograph is due to *in-situ* carbon deposition inside the microscope during image acquisition). Two separate changes in the nanowire growth direction were apparent, dividing the nanowire into three formal segments. High resolution transmission electron microscopy (Figure 4.6b-6f) taken locally at the selected regions of the nanowire in Figure 4.6a however revealed identical atomic arrangement as well as crystal orientation among these three segments, suggesting the nanowire is comprised of one single continuous crystalline domain. Similarly, the

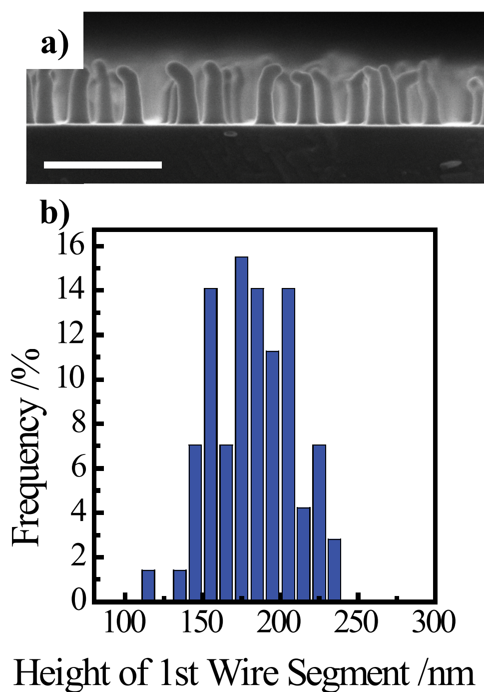

Figure 4.5. a) Cross-sectional scanning electron micrograph of Ge nanowires grown from n-Ge(111) electrode biased at -1.6 V in a solution of 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$ for 60 s. Scale bar: 500 nm. b) Corresponding height histogram of Ge nanowires grown from Ge(111) substrates prior to the first kink (N = 102).

SAED patterns collected from each nanowire segment (insets in Figures 4.6b-4.6d) were superimposable on each other, i.e. there was no alteration in crystal orientation of the nanowire across a kink. The lattice continuity across the two nanowire kink segments was explicitly shown in Figures 4.6e and 4.6f. Also revealed in Figures 4.6e and 4.6f were the stacking faults propagating within the (111) lattice planes immediately before each kink, angled at 70° with respect to the initial growth front. The new growth direction is collinear with the stacking fault direction, suggesting the kinks are directed by stacking fault formation. Figure 4.6g summarizes one possible crystal growth sequence that incorporates experimentally observed stacking faults and single crystal formation. At the initial stage (t < 30 s), epitaxial growth in a layer-by-layer fashion proceeds vertically along the [111] direction. As crystal growth continues, stacking faults form within the $(11\bar{1})$ lattice plane because of low stacking fault formation energy (13 meV/bond),[25] shifting the crystal growth direction by 70° from $[11\bar{1}]$. Similar stacking faults formed within the new segment, and guided further change of the crystal growth into a new <111> direction, resulting in a kinked but still single crystalline nanowire.

To ascertain whether the model in Figure 4.6g applies across an entire film, plan view scanning electron micrographs were collected to statistically identify the growth directions of the nanowires following the first kink. Upon analyzing 294 nanowires over the field of view, six discrete angles at in-plane angle intervals of 60° for the nanowire growth direction changes were observed (Figures 4.7a and 4.7b). These data were consistent with the premise that growth of the first kinked segment of the nanowire continued along one of the three <111> or the three mirrored <111> directions (introduced by in-plane inversion of a crystal growth front within the first growth segment).[26] Since stacking faults and twinning in single-crystalline semiconductor nanowires can arise from depletion of precursor at a metal catalyst in high temperature nanowire growth,[27] attempts were made to change the twinning density in this ec-LLS process through introduction of solution convection and reduction in GeO_2 concentration. Figures 4.8a, 4.8b show a plan-view scanning electron micrograph of Ge nanowires grown for 300 s on Ge(111) in a stirred solution and the orientation histogram of the first nanowire kink of each nanowire. Six preferred growth orientations separated by 60 deg

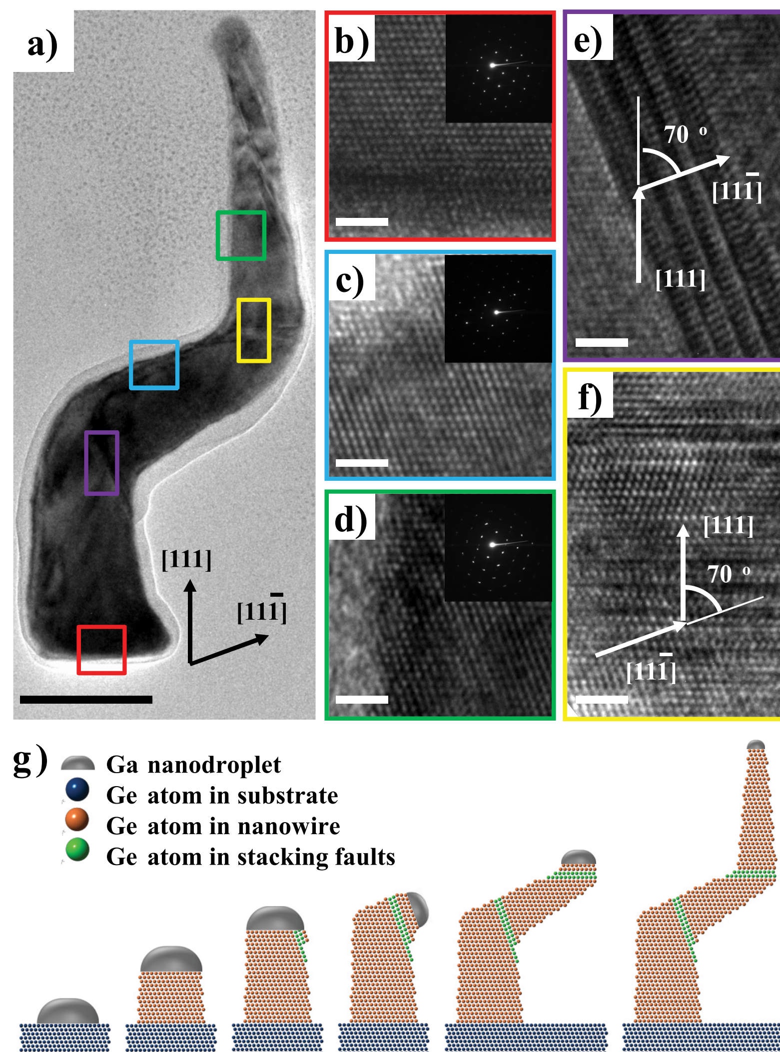

Figure 4.6. a) Transmission electron micrograph of a Ge nanowire prepared with a 300 s ec-LLS experiment. Scale bar: 100 nm (b-f) High resolution transmission electron micrographs for the corresponding boxed regions in (a). Scale bar: 2 nm. Insets: selected area electron diffraction patterns of the corresponding region. g) Schematic depiction of the crystal growth process of the nanowire, highlighting the formation of stacking faults and kinking of the nanowire. ec-LLS conditions: E_{app} = -1.6 V vs. Ag/AgCl, T = 40 ± 2 °C, 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$.

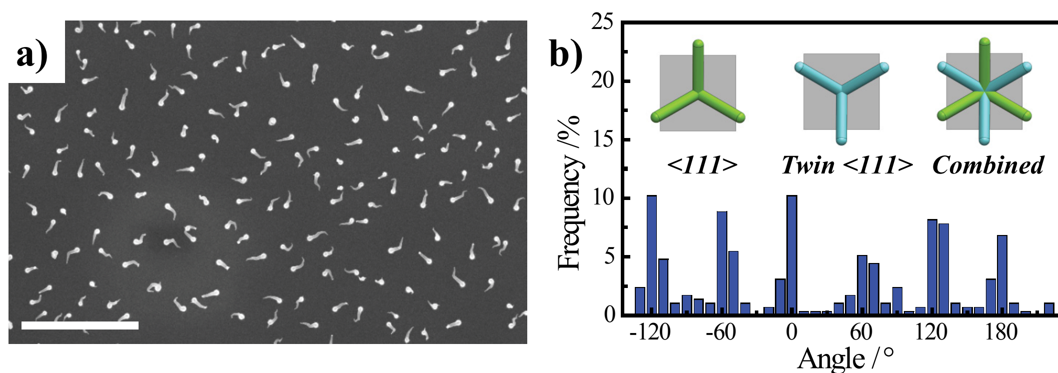

Figure 4.7. a) Plan-view scanning electron micrograph of a Ge nanowire film prepared with a 300 s ec-LLS experiment. Scale bar: 2 μm. b) Distribution of the Ge nanowire orientations from plan view images (as in (a)) after the first kink. Insets: Schematic of the expected orientations for nanowire growth along the <111> family. ec-LLS conditions: E_{app} = -1.6 V vs. Ag/AgCl, T = 40 ± 2 °C, 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$.

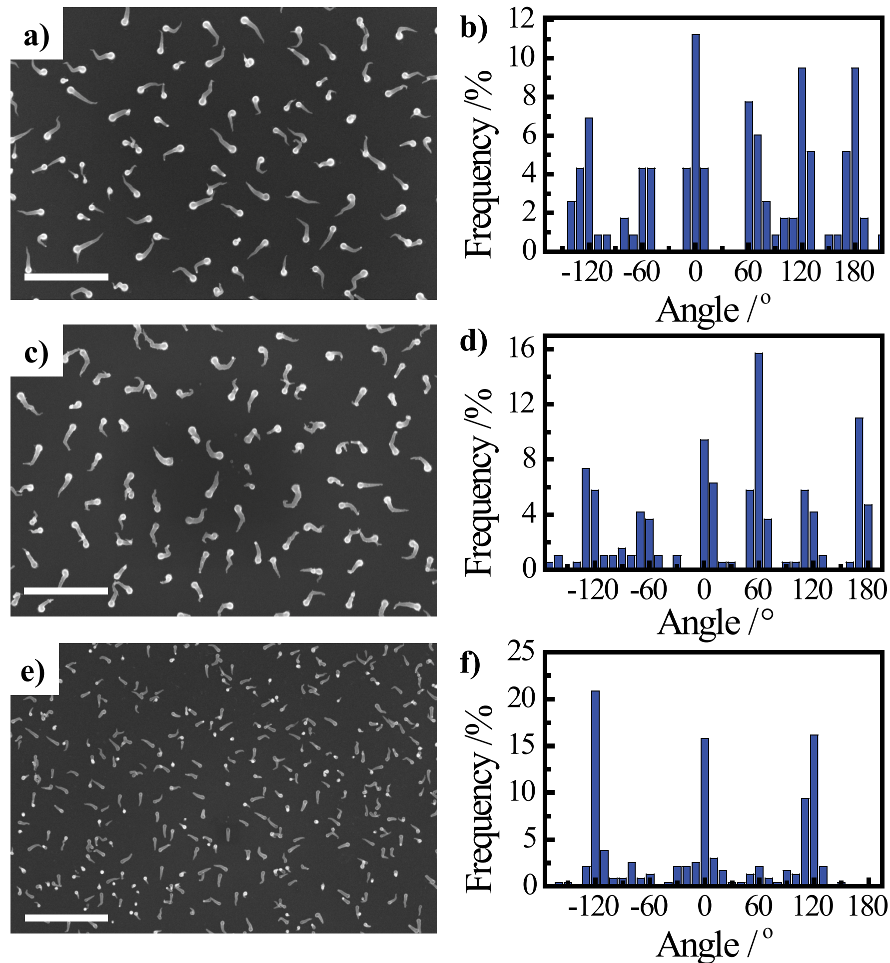

Figure 4.8. (a) Plan-view scanning electron micrograph of Ge nanowires grown on n-Ge(111) coated with Ga(l) nanodroplets biased at -1.6 V for 300 s during vigorous solution convection. Scale bar: 1μm. b) Corresponding histogram of nanowire growth orientations normalized to 0 ^{O} (N = 116). c) Plan-view scanning electron micrograph of Ge nanowires electrodeposited galvanostatically at 5 μA for 1 hr from 0.001 M GeO_2 and 0.01 M $Na_2B_4O_7$, 0.1 M KNO_3 on n-Ge(111) coated with Ga(l) nanodroplets. Scale bar: 1 μm. d) Corresponding histogram of nanowire growth orientations normalized to 0 ^{O} (N = 191). (e) Plan-view scanning electron micrograph of Ge nanowires grown on n-Ge(111) coated with electrodeposited Ga(l) nanodroplets biased at -1.6 V for 300 s. Scale bar: 1 μm. (f) Corresponding histogram of nanowire growth orientations normalized to 0 ^{O} (N = 235).

in-plane angles were recorded, nominally identical to nanowires produced in quiescent solutions with 0.05 M GeO_2(aq). Similar results were obtained for Ge nanowires grown on Ge(111) from 0.001 M GeO_2(aq) solutions under 5 μA galvanostatic condition for 1 hr (Figures 4.8c, 4.8d). Neither method of changing the local concentration of dissolved GeO_2 significantly impacted the occurrence of kinks in the electrodeposited nanowires, indicating precursor concentration was not the defining factor in kink formation. In the case of using freshly-electrodeposited Ga nanoparticles as growth seeds, a 300-sec ec-LLS process at -1.6 V vs. Ag/AgCl yielded Ga nanowires with first kinks at only three angles separated by 120° (Figure 4.8e 4.8f), suggesting nanowire epitaxy occurred with no in-plane inversion of the initial crystal growth front. However, no evidence supporting epitaxial growth was observed if electrodeposited Ga(*l*) nanodroplets were allowed to age in lab ambient for weeks prior to Ge nanowire electrodeposition.

To understand the relative resistance at the electrical contact between the epitaxial Ge nanowire and the underlying Ge(111) substrate, current-voltage responses through individual nanowires were measured using conductive atomic force microscopy. As shown in the schematic, a Pt-Ir AFM probe was used to contact individual Ge nanowires (Figure 4.9a). Following measurement of the electrical response, individual nanowires were laterally fractured 20 - 30 nm from the base and the electrical characteristics were re-measured. Figure 4.9b shows representative current-voltage profile for an individual Ge nanowire, a Ge nanowire laterally fractured at the base, and the oxide-free n-Ge substrate. At large applied bias, the current through Pt/Ge nanowire/n-Ge wafer had rectifying character in accord with metal/n-Ge contacts[28] (Figure 4.9c-e). The quasi-linear region of the current-voltage characteristic near zero bias was used to estimate relative resistance values through the Ge nanowire/n-Ge substrate junction, the fractured Ge nanowire/substrate junction, and the Pt/n-Ge substrate interface. Average resistance values extracted from full length nanowires and fractured nanowires were ostensibly identical within the error of the measurement (Figure 4.9b), indicating the overall Ohmic contribution through the nanowire was negligible. The contact resistance at the Pt/n-Ge substrate junction contributed 27 % to the cumulative measured resistance, with the remaining resistance mostly from the contact resistance at the Ge nanowire/n-Ge

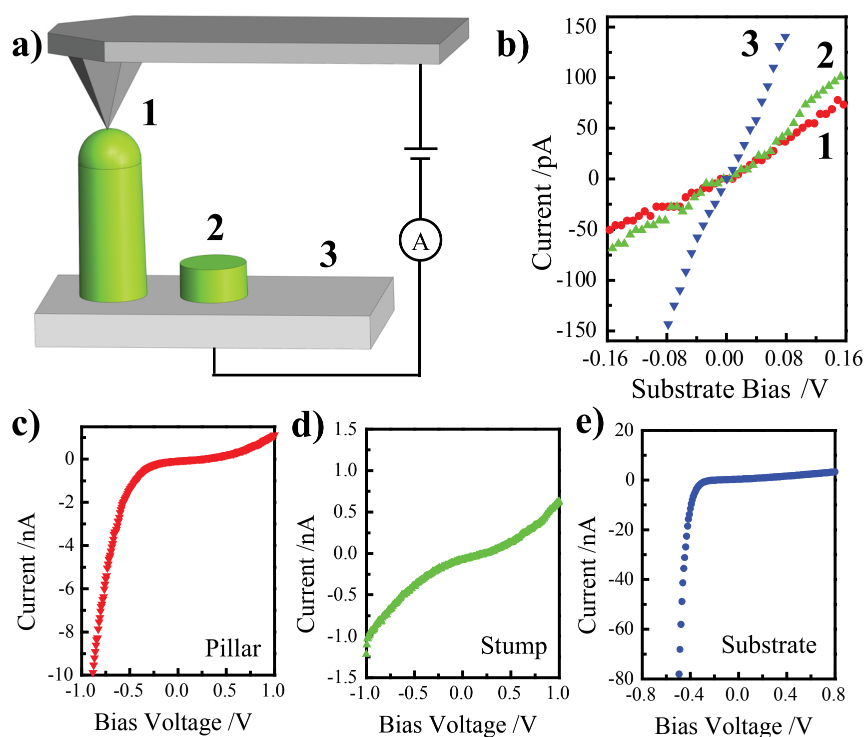

Figure 4.9. a) Schematic depiction of the conductive atomic force microscopic (c-AFM) measurement performed on (*1*) intact Ge nanowires after 30 s growth, (*2*) laterally fractured Ge nanowires and (*3*) oxide-free Ge substrate. b) Current-voltage response in c-AFM measurement for *1-3* near zero voltage region. Current-voltage responses measured by conductive atomic force microscopy across (c) an intact, as-grown, Ge nanowire on an n^+-Ge substrate, (d) a fractured Ge nanowire and (e) the oxide free n^+-Ge substrate. ec-LLS conditions: E_{app} = -1.6 V vs. Ag/AgCl, T = 40 ± 2 °C, 0.05 M GeO_2 and 0.01 M $Na_2B_4O_7$.

substrate junction rather than through the nanowire itself (Figure 4.5b). Previous work by our group has shown that conductivity values measured across polycrystalline Ge nanowires obtained with Hg(l) were consistent with Hg incorporation at dopant-levels consistent with the solubility of the liquid metal in Ge at ambient temperature.[15] As Ga is a p-type dopant in Ge, the substrate/nanowire contact resistance measured here is nominally consistent with a p-n homojunction formed between the n-type Ge substrate and a p-type nanowire. However, further measurements are needed to explore this point comprehensively. The electrical measurements shown here did reveal uniformity in the apparent resistance values, with a relative standard deviation of 17 % *(N* = 20).

D. Discussions

The presented data illustrate that semiconductor electrodeposition via ec-LLS with liquid metal nanodroplets possesses three unique synthetic features. First, no other known synthetic strategies combine the possibility of epitaxial and single-crystalline growth with ambient process conditions, aqueous solutions, and simple equipment. The formation of Ge/Ga eutectic at temperature as low as 29 ^{o}C enables the crystallization of Ge at temperature about 200 ^{o}C lower than the required temperature for the commonly used Au catalyst. The electrochemical reduction of aqueous Ge precursors at the catalytic Ga surface eliminates the need for high processing temperature that is typically necessary for precursor decomposition in VLS growth. The adoption of aqueous solution and bench-top electrochemical setup minimizes the use of furnace, vacuum, and additional plumbing, and thus greatly reduces the instrumental complexity as well as the associated cost. Second, the electrochemical process described here uses only an oxidized precursor and requires no exotic solvents or elevated temperatures/pressures, in contrast to the highly processed and partially-to-completely reduced chemical precursors in molecular beam epitaxy (MBE), chemical vapor deposition, and solution-liquid-solid crystal growth.[29,30] Furthermore, the ec-LLS process also stands apart from other electrochemical-based efforts to make crystalline semiconductor materials. For a covalent semiconductor like Ge, electrodeposition on a solid electrode at room temperature consistently yields amorphous films with entrapped solvent since the factors that promote bulk crystal growth are not accessible. Specifically, movement of Ge adatoms to a crystal

growth front on a Ge surface is much greater than k_BT at room temperature,[31] solvation and re-precipitation of reduced Ge by the aqueous electrolyte is not feasible, and templating substrate effects like those in electrochemical atomic layer epitaxy[32] do not readily translate into thick films.[33] Instead, solvation by the liquid metal of elemental Ge lowers the energy for crystal nucleation and growth within the liquid metal. In this way, the identity of the liquid metal nanodroplets matters critically.

In this work, both complex (i.e. MBE) and simple (i.e. pulsed electrodeposition) protocols were used to prepare Ga nanodroplets without changes in the primary findings, i.e. epitaxial and single-crystalline nanowire electrodeposition. This indicates the critical steps of the ec-LLS process, i.e. electroreduction of the precursor, dissolution of the reduced species, nuclei formation and crystal growth are not sensitive to the different techniques leading to the growth catalyst formation. Such insensitivity allows the complete substitution of the complex fabrication techniques with electrodeposition for Ge nanowire epitaxy. Furthermore, the electrodeposited Ga nanodroplets favor the ec-LLS process by reducing the total amount of twinning defects. The observed discrepancy in growth orientation between Ge nanowires grown from MBE-prepared Ga droplets and electrodeposited Ga droplets suggest that the liquid metal/substrate interface plays important roles in crystallographic twin formation. Assuming that the conditions at the three phase contact line (i.e. interface between liquid electrolyte, liquid metal, and crystalline Ge) affect crystal growth, the wetting properties of the liquid metal nanodroplet, the capacity of the liquid metal to act as a dissolving and recrystallizing solvent for the semiconductor, and the electrostatics of the double layer at the electrode/electrolyte interface could be factors in crystallographic defect formation in ec-LLS.

With respect to nanofabrication, ec-LLS with liquid metal nanodroplets offers practical advantages. A single electrochemical step for the concerted synthesis and growth of nanowires is naturally compatible with the equipment already used for electroplating in microelectronics. For example, electrochemical plating of copper contacts at the wafer scale is presently performed with electrolyte baths (e.g. oxidized copper salts in water) and low process temperatures (e.g. 25 °C) consistent with the ec-LLS process reported here.[34] Furthermore, with individually addressable liquid metal

nanodroplets, the possibility exists to fabricate nanowire-based circuits locally on a large device platform. While development of the ec-LLS process is still in the early stages, the work reported here, in conjunction with recent breakthroughs for the ec-LLS preparation of covalent semiconductors like Si[18] and GaAs[16], suggest that ec-LLS with liquid metal nanodroplets could serve as a new method for conductive nanowire device construction and integration.

E. Conclusions

This chapter presents data supporting the notion of epitaxial nanowire growth at room temperature via ec-LLS. Single crystalline Ge nanowires were obtained on a Ga-decorated Ge single crystal wafer by direct electrodeposition from an aqueous solution containing GeO_2. Scanning electron micrograph showed uniformly vertical aligned Ge nanowires on a Ga-decorated Ge (111) wafer after electrodeposition. Varying the crystal orientation of the underlying Ge substrate caused an alteration of the growth orientation of the electrodeposited Ge nanowires, consistent with an epitaxial growth. The interfacial details between the Ge substrate and the as-deposited Ge nanowires were studied with atomic resolution by cross-sectional high-resolution transmission electron microscopy and selected area electron diffraction. Lattice continuity across the substrate-nanowire interface was concluded from both techniques, confirming the epitaxial nature of the growth. Crystallinity and defect formation were probed by transmission electron microscopy, followed by the proposal of a detailed growth pathway. At the same time, evidence of analogous heteroepitaxial growth of Ge nanowire on Ga-coated Si wafer was also observed. In addition, current-voltage responses measured in conductive atomic force microscopy across many individual nanowires yielded reproducible resistance values. The presented data cumulatively show epitaxial growth of covalent group IV nanowires is possible from the reduction of a dissolved oxide under purely benchtop conditions. As a result, uniformly aligned single crystalline nanowires with electrical integrity with the substrate can be obtained by room temperature electrodeposition.

F. References

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CHAPTER 5

Direct Electrodeposition of Crystalline Silicon at Low Temperatures by ec-LLS

A. Introduction

This chapter demonstrates the application of ec-LLS strategy for electrodeposition of crystalline Si at temperature as low as 80 °C from an organic electrolyte. Dissolved $SiCl_4$ in propylene carbonate was electrochemically reduced onto liquid gallium pool electrode to form high-coverage elemental Si. X-ray diffraction and electron diffraction data separately indicated that the as-deposited (i.e., with no annealing) materials were crystalline with the expected patterns for a diamond cubic crystal structure. Scanning electron microscopies further revealed the as-deposited materials to be faceted nanocrystals with diameters in excess of 500 nm. The composition of the product was evaluated by elemental analyses, and the possible impurities were identified.

Presently, the major industrial method for the production of crystalline Si, the key semiconductor in many optoelectronic technologies[1-3], involves a series of energy-intensive, highly polluting carbothermal reduction reactions that produce undesirable byproducts, including CO_2.[4] Electrodeposition has long been identified as a potential alternative route for the preparation of Si since electrodepositions can be inherently simple, clean, and comparatively non-energy-intensive.[5,6] However, resource-intensive carbothermal reactions are generally still preferred over electrodeposition for Si production for two principal reasons. First, as-prepared Si from low-temperature electrodepositions is often impure with components from the electrolyte at >10–1 atom %[7,8] and is always amorphous,[7-16] requiring additional thermal annealing and purification. Second, excessively high (>700 °C) temperatures are required for an electrodeposition process to yield crystalline Si.[17-20] The incompatibility of low temperatures and a pure, crystalline product have thus severely limited the appeal of Si

electrodeposition. Accordingly, a new Si electrodeposition method that overcomes this longstanding challenge would be highly desirable and could have substantial technological impact. In previous chapters, ec-LLS has been shown as a versatile tactic for direct electrodeposition of crystalline Ge at room temperature under various experimental settings from using liquid pool electrodes to nano-sized liquid droplets. A key advancement for ec-LLS as a synthetic strategy would be to determine whether a liquid-metal electrode could facilitate the direct preparation of crystalline Si. Accordingly, this chapter highlights data demonstrating the use of a liquid-metal electrode as a platform for direct electrodeposition of crystalline Si from a dissolved precursor under relatively benign conditions.

B. Methods

Materials and Chemicals Methanol (ACS grade, BDH), acetone (ACS grade, BDH), HF (49%, Transene Inc.), propylene carbonate(PC, 99.5%, Acros Organics), $SiCl_4$ (99.99+%, Strem Chemicals), Ga(*l*) (99.999%, Alfa Aesar) were used as received. Tetrabutylammonium chloride (TBAC, 95%, Alfa Aesar) was dried first under vacuum for 2 days at room temperature and transferred into a N_2-purged glove box with O_2 and H_2O levels at 1.5 and 0.1 ppm, respectively. TBAC was further dried for 2 days after dissolution in PC with molecular sieves (4A, 8-12 mesh, Sigma-Aldrich).

Electrodeposition of Si All electrodepositions were performed with an Eco Chemie Autolab PGSTAT302N potentiostat in a custom-built two compartment glass cell separated by a porous frit placed inside a stainless steel vessel. The vessel was pressured via a gas inlet connected to a purged gas manifold that included pressurized Ar(g) (99.998%, Detroit Metro Welding). The vessel temperature was set by heat wrap and monitored with a thermocouple positioned just above the solution level inside the vessel. All electrodepositions were performed with a three-electrode configuration, using a 200 μL Ga(*l*) pool as the working electrode (ca. 0.616 cm^2 active area), a Pt sheet as the counter electrode, and a cleaned Pt wire as the quasi-reference electrode, respectively. The electrical contact to the Ga(*l*) electrode was made through a piece of Pt wire enclosed in the PTFE heat-shrink tubing. The cell and vessel were transferred into a N_2 glove box, loaded with 14 mL of electrolyte (0.5 M $SiCl_4$, 0.2 M TBAC in PC), then sealed, and

finally transferred back to the lab ambient where both electrical connections and pressurized gas connections were subsequently made. Electrodepositions were performed under galvanostatic control, with J = 20 mA cm^{-2} and sufficient backpressure to overcome the volatility of $SiCl_4$ at T = 200 °C (2.76 MPa backpressure). After each electrodeposition, the chamber was cooled down and vented slowly over the course of 1 hr. The collected film from the working electrode was suspended and washed with acetone 3 times, dried under flowing $N_2(g)$, etched with 5% w/w HF solution for 30 s, and washed with methanol. The mass of the electrodeposited Si after purification was measured with a Sartorius ME36S microbalance (readability 0.001 mg).

Material Characterization Powder X-ray diffractograms were collected with a Bruker D8 Advance diffractometer equipped with a Cu Kα source (λ = 1.5406 Å), an adjustable incident beam slit and a Lynx Eye detector. *Ex-situ* diffractograms were obtained with a 0.6 mm beam slit at a sampling rate of 20 data points per degree 2θ at 4 s point^{-1}. The *in-situ* annealing X-ray diffraction experiments were carried out on a custom-built ceramics heating stage. The sample was annealed at ambient atmosphere for 30 min at each temperature point prior to the data acquisition. The diffractograms were taken with a 2.0 mm beam slit at a sampling rate of 20 data points per degree 2θ at 1 s point^{-1}. Spot-focus powder X-ray diffraction was collected using a Bruker D8 Discover equipped with a general area detector diffraction system (GADDS). The spot size of the Cu Kα Radiation X-ray was selected to be 50 mm. The diffractogram was first collected using a 2-D HighStar detector for 1 hr exposure and then integrated over the 2-D space to obtain the conventional 1-D diffractogram.

Raman spectra were obtained using a Renishaw Raman Microscope Spectrometer equipped with a Nikon LU Plan 20x objective (NA = 0.4) and edge filters to reject the 785 nm excitation line. A 785 nm diode laser was used as the incident excitation at a total radiant power of 1.12 mW over a 20 μm^2 incident spot. The *ex-situ* annealing sample for Raman analysis was prepared by annealing the Si samples under ambient atmosphere in a muffle furnace for 30 min at each temperature point.

High-resolution transmission electron microscopy (HRTEM) and selected area electron diffraction (SAED) were performed with a JEOL 3011 TEM equipped with a LaB_6 source operated at 300 kV. Samples for TEM were prepared by first dispersing the

collected powder in methanol through sonication for 30 s. Then approximately 10 μL of the suspension was drop cast onto 400 mesh copper TEM grids coated with an ultra-thin carbon film (Ted Pella). Energy dispersive spectra were taken with an electron beam at 300 kV and an EDAX r-TEM detector. Scanning transmission electron microscopy (STEM) was conducted using the JEOL 2010F analytical microscope equipped with a Zirconiated Tungsten (100) thermal field emission source operated at 200 kV. The *in-situ* annealing experiments were carried out with a Gatan double-tilt heating holder. Scanning electron micrographs (SEM) were taken at 15 kV with a FEI/Philips XL30 FEG SEM, equipped with an Everhart-Thornley secondary electron detector. Energy dispersive spectra were taken at 20 kV with an EDAX UTW detector.

C. Results

Figure 5.1 illustrates the proposed mechanism for direct electrodeposition of Si by the ec-LLS method. As has been demonstrated for Ge[21,22] and GaAs[23], the initial stage would involve electroreduction of an oxidized precursor ($SiCl_4$) to the fully reduced state (Si) at the electrode–electrolyte interface. Electroreduction of $SiCl_4$ at solid electrodes has been investigated on various substrates previously[7,8,11,15] and found to produce purely amorphous Si. In the ec-LLS scheme, the initially reduced Si could be partitioned into the liquid gallium [Ga(l)] phase. The solubility of Si in Ga between room temperature and 200 °C was tabulated in table 5.1, as determined by extrapolations of published metallurgical data for the Ga-Si system,[24] ranges from 10^{-8} to 10^{-6} atom %. Although low, the solubility of Si in Ga at 100 °C is comparable to the solubility in another ec-LLS system (Ge in Hg at room temperature)[25] demonstrated previously.[21] The dissolved Si in Ga(l) could then reach saturation and supersaturation conditions if $SiCl_4$ is continuously reduced at the electrode–electrolyte interface. When a critical supersaturation condition is reached, phase separation of Si(s) from Ga(l) followed by crystal growth would occur.

To determine whether any observable for the electroreduction of $SiCl_4$ at Ga(l) electrodes would support the scheme in Figure 5.1, a three-electrode configuration was used to electrodeposit Si onto a Ga(l) electrode at several different temperatures up to 200 °C. The cell was pressurized to 2.76×10^6 Pa (400 psi) to offset the volatility of

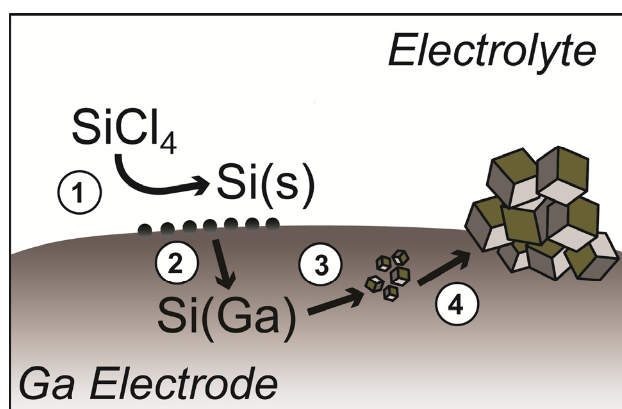

Figure 5.1. Schematic depiction of the ec-LLS process for electrodepositing crystalline Si from dissolved $SiCl_4$ in propylene carbonate on liquid Ga electrode

Table 5.1. Solubility of Si in Ga as a function of temperature

Temperature /°C	*Solubility of Si in Ga / log (atomic percent)*
20	-7.37126
40	-6.65081
60	-6.01686
80	-5.45472
100	-4.95284
120	-4.50201
140	-4.09484
160	-3.72527
180	-3.38832
200	-3.07985

$SiCl_4$ at elevated temperatures.[26] A fritted two compartment cell was used to prevent any anodic products from diffusing back to the cathode where the active $SiCl_4$ reduction occurs. Figure 5.2 shows the cyclic voltammetric responses for $SiCl_4$ reduction at Ga(l) electrodes in propylene carbonate containing 0.2 M TBAC at room temperature. Before correction for iR drop in the liquid electrolyte, the voltammogram appeared to be highly resistive, and all responses at the collected current densities were significantly distorted. Figure 5.2b shows the true current-potential responses for the working electrodes after iR correction based on impedance. At low concentration of $SiCl_4$, the voltammetric response showed a clear diffusion-limited wave at -2.0 V vs. Pt QRE that was well separated from the onset of cathodic solvent decomposition. A small pre-wave was also observable on the very first cathodic sweep that was associated with the reduction of trace proton in the solution. These features are generally consistent with the previous reports of $SiCl_4$ reduction[8,12,14,27]. With increasing concentration of $SiCl_4$, the cathodic feature at -2.0 V increased in magnitude, further confirming that the reduction peak was resulted from the reduction of dissolved $SiCl_4$. The impedance data used for the solution iR correction was shown in Figure 5.2c. The high frequency intercept (Figure 5.2d) of the Nyquist plot indicated a solution resistance of approximately 200 Ω at room temperature. Under the same conditions at 100 °C the measured solution resistance dropped to slightly less than 100 Ω. Figure 5.3 shows representative voltammograms both before and after iR correction for a Ga(l) working electrode scanned to negative potentials in propylene carbonate containing 0.2 M tetrabutylammonium chloride (TBACl) with or without 0.5 M $SiCl_4$ at 100 °C. A diffusion-limited voltammetric wave was no longer observable below 20 mA cm^{-2}.

Figures 5.4a, b highlight the optical appearance of a Ga(l) pool electrode before and after a galvanostatic experiment at 20 mA cm^{-2} at 100 °C for 2 h. The fresh Ga droplet showed a shiny metallic reflection before Si deposition (Figure 5.4a), indicating low oxide content at the surface. A dull black film was developed over the entire Ga surface after the 2 h deposition process as shown in Figure 5.4b. The mass of the black film on the Ga(l) electrode following the galvanostatic deposition was sensitive to the length of the experiment, with a smaller apparent mass collected after shorter

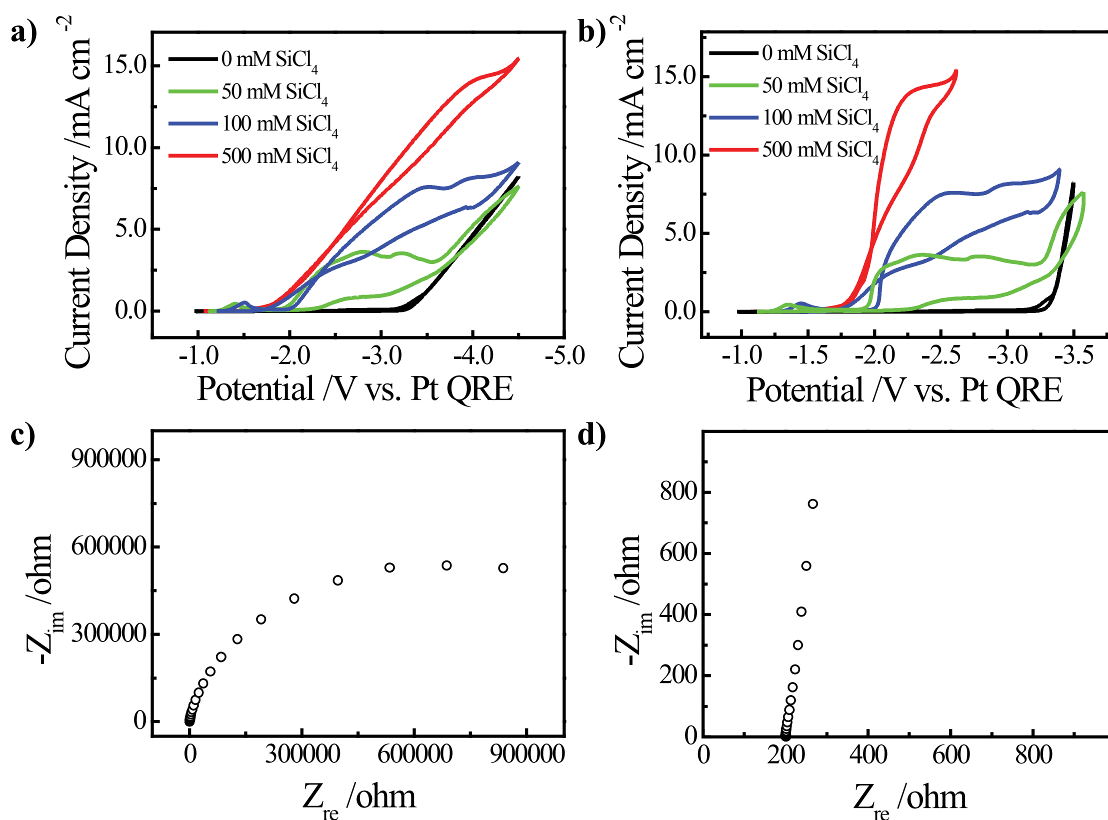

Figure 5.2. Cyclic voltammetric response of a Ga(l) electrode in propylene carbonate containing 0.2 M TBAC and various concentrations of $SiCl_4$ (0 mM, 50 mM, 100 mM to 500 mM) at room temperature under N_2 (g) both a) before and b) after correction for iR drop in solution. Scan rate = 0.025 V s^{-1}. Nyquist plot of impedance response of a Ga(l) electrode in propylene carbonate containing 0.2 M TBAC at open circuit potential (-0.96 V vs. Pt QRE) at room temperature for c) full frequency range, d) high frequency range.

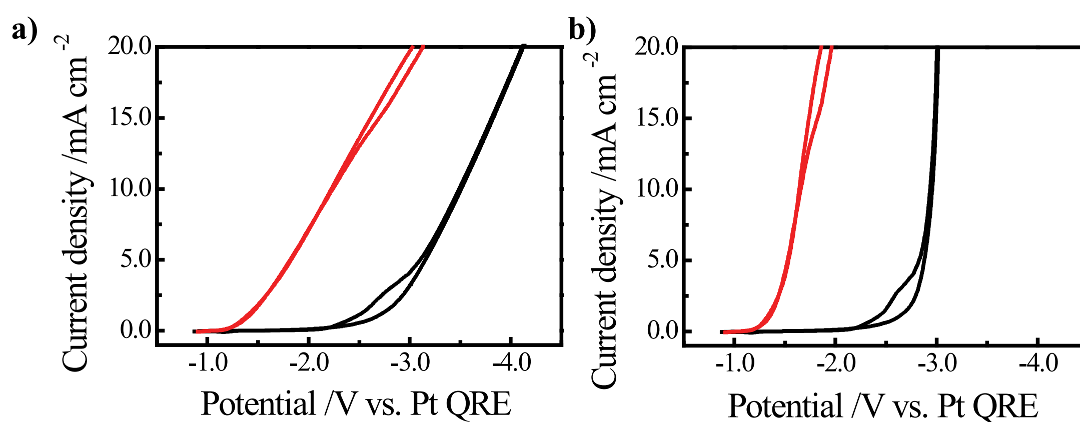

Figure 5.3. Cyclic voltammetric response of a Ga(l) electrode in propylene carbonate containing 0.2 M TBAC (red) with and (black) without 0.5 M of $SiCl_4$ at 100 ^oC and 2.76 MPa, under Ar (g) both a) before and b) after correction for iR drop in solution. Scan rate = 0.025 V s^{-1}.

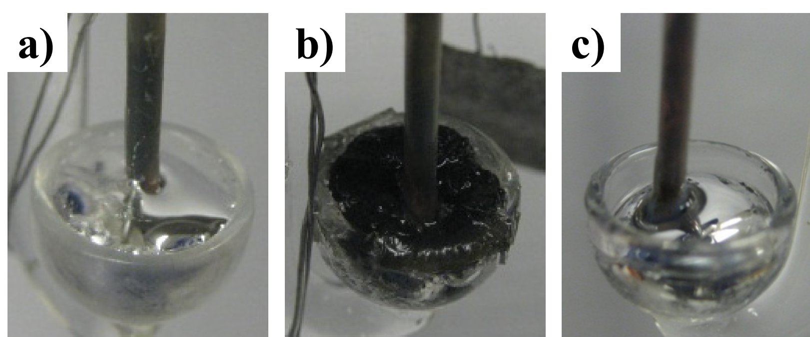

Figure 5.4. a) Optical photograph of a clean Ga(l) working electrode. b) Optical photograph of the same electrode after galvanostatic electrodeposition of Si in propylene carbonate containing 0.2 M TBAC and 0.5 M $SiCl_4$ at 20 mA cm^{-2} for 2 h at 100 °C. c) Optical photograph of a Ga(l) electrode exposed to 0.5 M $SiCl_4$ and 0.2 M TBAC in propylene carbonate at 100 ^oC and 2.76 MPa at open circuit potential for 2 h. Images c) and d) were obtained after physical removal from the cell.

experiments. A control experiment was carried out by exposing the Ga(l) electrode to 0.5 M $SiCl_4$ and 0.2 M TBAC in propylene carbonate at 100 ^oC and 2.76 MPa at open circuit potential for 2 hr. As shown in Figure 5.4c, no Si deposit was observed in the absence of an applied electrochemical potential, suggesting that a purely chemical substitution reaction between Ga(l) and $SiCl_4$ did not occur at the experimental conditions applied in this study. The as-prepared film was physically removed from the surface of the Ga(l) pool electrode, dried, and collected as a powder. After washing/etching of the collected mass to remove solvent, physisorbed electrolyte salt, and native oxide, the black powder was stored dry under ambient conditions. A comparison of electrodeposited Si powder immediately after wash and after storage in air for 30 days is shown in Figure 5.5. The hue and texture of the collected electrodeposit did not appear to change over time in air, in contrast to the common discoloration observed for porous, amorphous Si in air.[8,13,16]

Figure 5.6a presents representative powder X-ray diffractograms of the black film as-deposited and after being etched by 5 % HF solution along with a diffractogram of the underlying glass substrate used during X-ray diffraction measurement. No qualitative difference was observed in the diffractogram caused by the etching process, indicating the crystallinity of deposit was preserved in the HF etching process. Figure 5.6b shows the X-ray diffraction data after correction for the scattering contribution from the underlying support. Analysis of the corrected diffractogram revealed that the sharp diffraction patterns were in accord with the diamond cubic crystal structure expected for crystalline Si. Using either Rietveld refinement or Scherrer line width analysis, the crystalline domain size inferred from the X-ray diffraction data was large (>100 nm). The X-ray diffraction measurement was also repeated using a point-focus X-ray source with small probe volume (spot size = 50 μm) to maximize the signal contribution from solid deposit over underlying glass support and air scattering as observed in Figures 5.6a. Comparable results were obtained showing crystalline Si diffraction pattern with reduced scattering feature below 30 degree.

Figures 5.7a, 5.7b show the representative scanning electron microscopy images that detail the morphology of the as-electrodeposited Si powder. Uniformly sized grains were consistently observed with total widths of 500 nm. A fraction of the observed

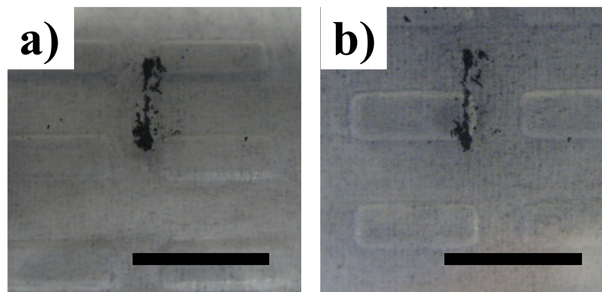

Figure 5.5. a) Optical photograph of the as-deposited Si powder immediately after purification. b) Optical image of the same Si powder after being stored in lab ambient for 30 days.

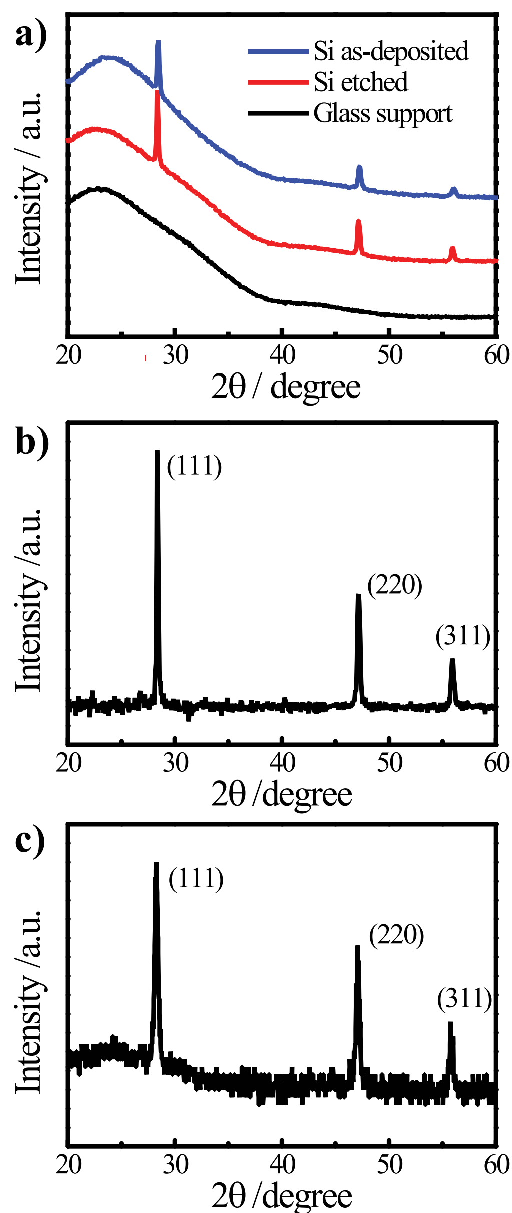

Figure 5.6.a) X-ray diffractograms of as-deposited Si powder before and after being etched with 5 % w/w HF solution for 30 s, along with the diffraction background from the glass slide support. The latter was used for background correction. b) Background-corrected X-ray diffractogram of the etched Si powder. c) Raw X-ray diffractogram of the same etched Si powder measured using a 50 µm point-focus X-ray source. The Si sample was galvanostatically deposited in a propylene carbonate solution of 0.2 M tetrabutylammonium chloride (TBAC) and 0.5 M of $SiCl_4$ with current density of 20 mA cm^{-2} for 2 h at 100 ^oC and 2.76 MPa pressure.

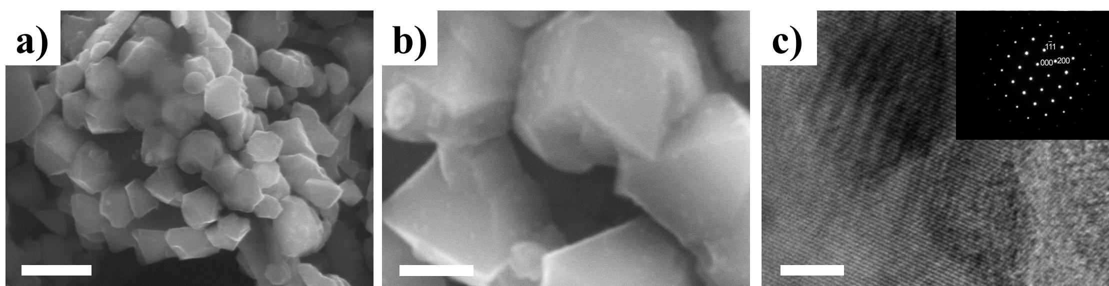

Figure 5.7. Scanning electron micrographs of electrodeposited Si at a) 20 000× and b) 80 000× times magnification. c) High-resolution transmission electron micrograph of electrodeposited Si at 800 000× magnification. Inset: selected area electron diffraction pattern obtained with the electron beam parallel to the [011] zone axis. Crystalline Si was electrodeposited in a propylene carbonate solution containing 0.2 M TBAC and 0.5 M $SiCl_4$ at 20 mA cm^{-2} for 2 h at 100 °C and 2.76 MPa pressure. As-deposited Si was etched in 5% HF solution for 30 s prior to electron microscopy analysis.

particles appeared fused together along an edge. However, the majority of particles were unfused but aggregated in large clusters. Nearly every observed grain showed sharp facets, consistent with the premise that each grain constituted a single crystal. Electron backscatter diffraction experiments were attempted in order to determine whether each grain in an aggregate was in fact a uniform single crystal, but the grain sizes were too small for conclusive evidence to be obtained. Instead, transmission electron microscopy (TEM) was performed on individual Si grains. Figure 5.7c shows a representative high-resolution TEM image. Lattice fringes commensurate with the d_{111} spacing for crystalline Si were observed. A representative selected-area electron diffraction (SAED) pattern obtained along the [011] zone axis is shown in the inset of Figure 5.7c. The observed diffraction pattern is consistent with a diamond cubic lattice and $d_{111} = 3.1$ Å, as expected for a single crystal of Si. Every particle observed by this method exhibited similar diffraction characteristics. Figure 5.8a presents an energy-dispersive X-ray (EDX) spectrum acquired using the scanning electron microscope for the sample. As the Si K line being the dominating feature in the spectrum, Ga L line at 9.2 keV was also detected. Difficulty in rigorously excluding Ga upon removal of the film from the electrode limited accurate ensemble assessment of the residual Ga content. A small amount of Cl due to residual electrolyte was also detected slightly above the baseline in the sample. Additional Cu signal detected was caused by the Cu tape support used for the measurement. Further attempts were made to measure the elemental composition of dispersed crystals using energy-dispersive X-ray spectroscopy in a transmission electron microscope. As shown in Figures 5.8b, c, mixed results were obtained when different portion of the crystal was probed. When a few spots within the crystal appear to be free of Ga impurity (Figure 5.8b), Ga can be detected by EDX in other location of the crystal (Figure 5.8c). As a result, possibility of Ga incorporation in the Si crystal cannot be ruled out.

Figures 5.9, 5.10 present the data elucidating the cessation of the ec-LLS process of Si at Ga(l) electrode. The deposition process was carried out galvanostatically at 20 mA cm^{-2} current density at 100 ^{o}C and 2.76 MPa pressure. The obtained deposit mass was plotted as a function of deposition time in Figure 5.9a. The quantity of the product

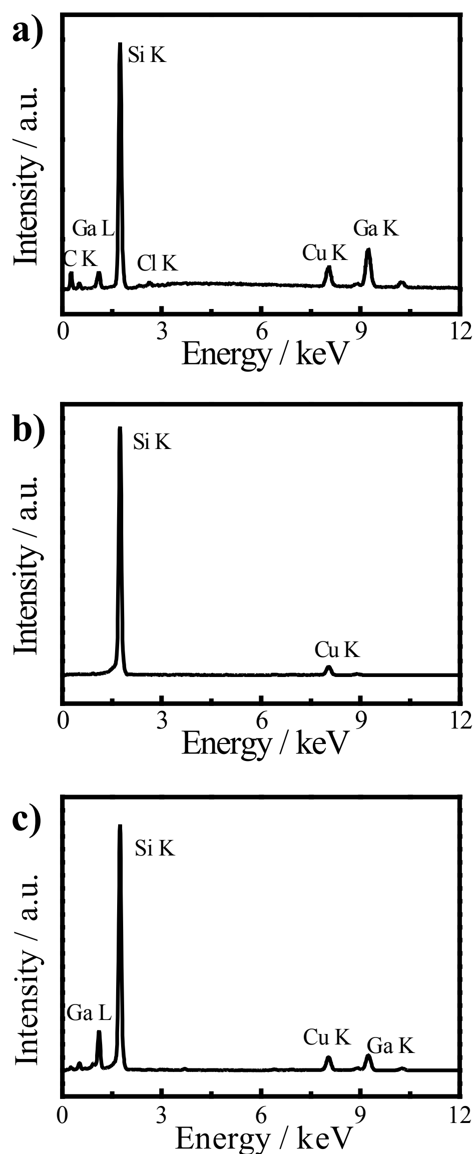

Figure 5.8. a) Energy dispersive energy spectrum of a Si sample taken in the scanning electron microscope at 15 kV. b) and c) Energy dispersive energy spectra of two different crystallites from a same sample taken in the transmission electron microscope at 300 kV. Crystalline Si was electrodeposited in a propylene carbonate solution containing 0.2 M TBAC and 0.5 M $SiCl_4$ at 20 mA cm^{-2} for 2 h at 100 °C and 2.76 MPa pressure. As-deposited Si was etched in 5% HF solution for 30 s prior to electron microscopy analysis.

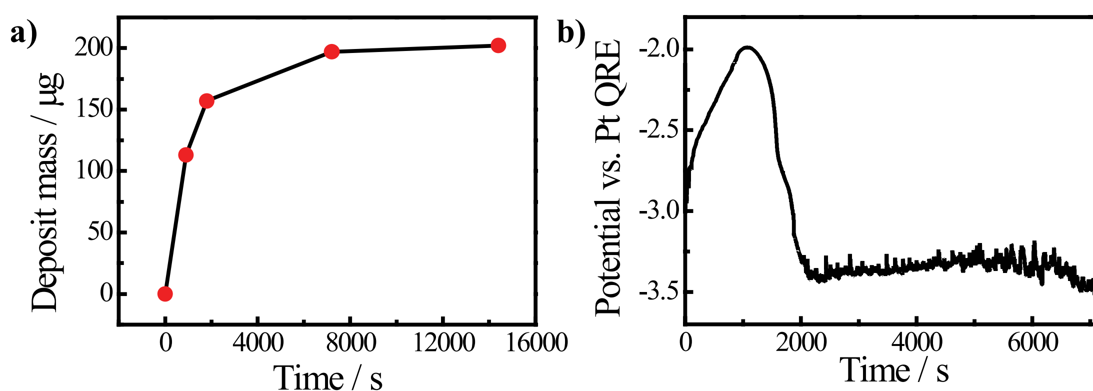

Figure 5.9. a) A plot of the collected electrodeposited mass as a function of electrodeposition time. Each point represents a separate electrodeposition experiment. b) Representative chronopotentiometric response of the Ga(l) electrode during a 2 h galvanostatic electrodeposition at 20 mA cm^{-2} current density at 100 °C and 2.76 MPa pressure in a propylene carbonate solution containing 0.2 M TBAC and 0.5 M $SiCl_4$.

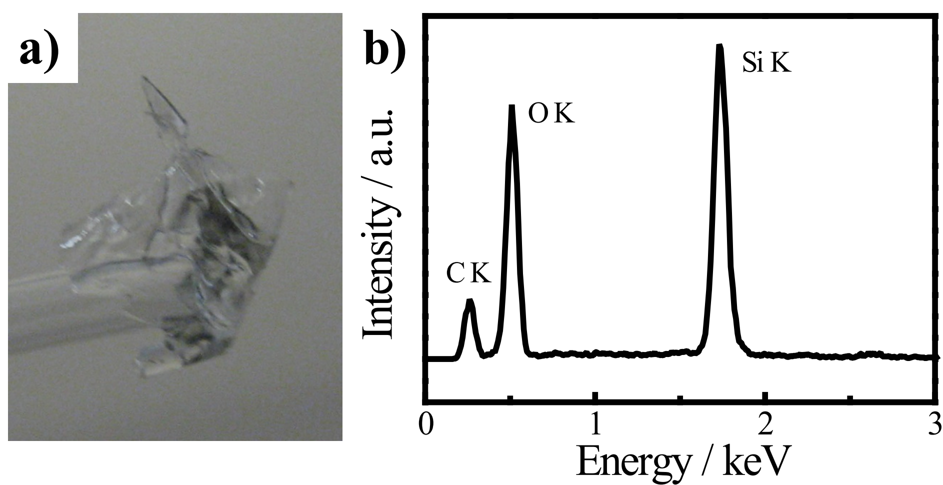

Figure 5.10. a) Optical micrograph of the white/transparent film obtained at the Ga(l) electrode surface after a 2 h electrodeposition at 20 mA cm^{-2} current density at 100 ^{o}C and 2.76 MPa pressure. b) Energy dispersive energy spectrum of the isolated film taken in the scanning electron microscope at 15 kV.

first rose steadily till ca. 1800 s before the deposit mass started to level. A representative chronopotentiometric response (Figure 5.9b) of the Ga(l) electrode over the 2 hr experiment under identical condition revealed that the potential required to supply the demanded current became more negative after 1100 s and reached the solvent decomposition potential at ca. 2000 s, coinciding with the critical time at which the deposit mass stopped to accumulate. Further analyses were carried out to understand the primary causes of the cessation. One possible cessation mechanism was the through the development of a glass layer from $SiCl_4$ interaction with the electrolysis decomposition products of the solvent at long times. As shown in Figure 5.10a, white/transparent precipitates were noted at the Ga(l) electrode surface upon disassembly of the cell after long electrodeposition. Precipitate formation only occurred after electrolysis, i.e. a cell charged with materials and heated but no applied potential was indefinitely stable against precipitate. The white precipitate was determined to be SiO_2 in nature by energy dispersive X-ray spectroscopy as shown in Figure 5.10b. The formation of the SiO_2 layer over time along with the initial Si deposit could serve as a physical insulating blockage that prevents $SiCl_4$ from further being reduced on the Ga(l) electrode. Further control experiments were conducted to determine whether there exist extrinsic factors that also contribute to the deposition cessation, e.g. loss of $SiCl_4$, electrolyte fouling over time. In brief, electrodeposition of Si on two separate Ga(l) electrodes was performed in a single vessel as shown in Figure 5.11a. The experiments involved performing a typical electrodeposition with the first working electrode (WE1) to the point of cessation and then switching over immediately to the second working electrode (WE2) to perform a new electrodeposition. If Si electrodeposition proceeded as 'normal' on WE2, then the implication would be the Si ec-LLS is intrinsically limited. If Si electrodeposition on WE2 was inhibited, then instability of the electrolyte occurred throughout the solution. Figure 11b shows the results of these control experiments, with no visible deposit on WE2, arguing the cessation was also triggered by extrinsic aspect of this system.

To demonstrate the versatility of the Si ec-LLS, the electrodeposition processes were repeated under various applied potential and precursor concentration conditions. Figures 5.12a-c show the optical images of Si product deposited potentiostatically at -2.5

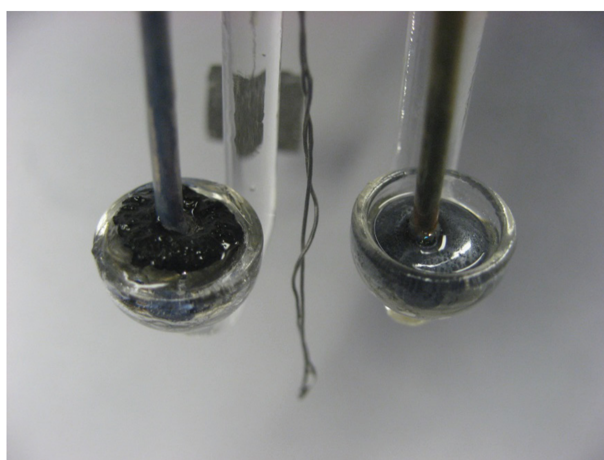

Figure 5.11. Optical image showing the deposit from a dual working electrode experiment.

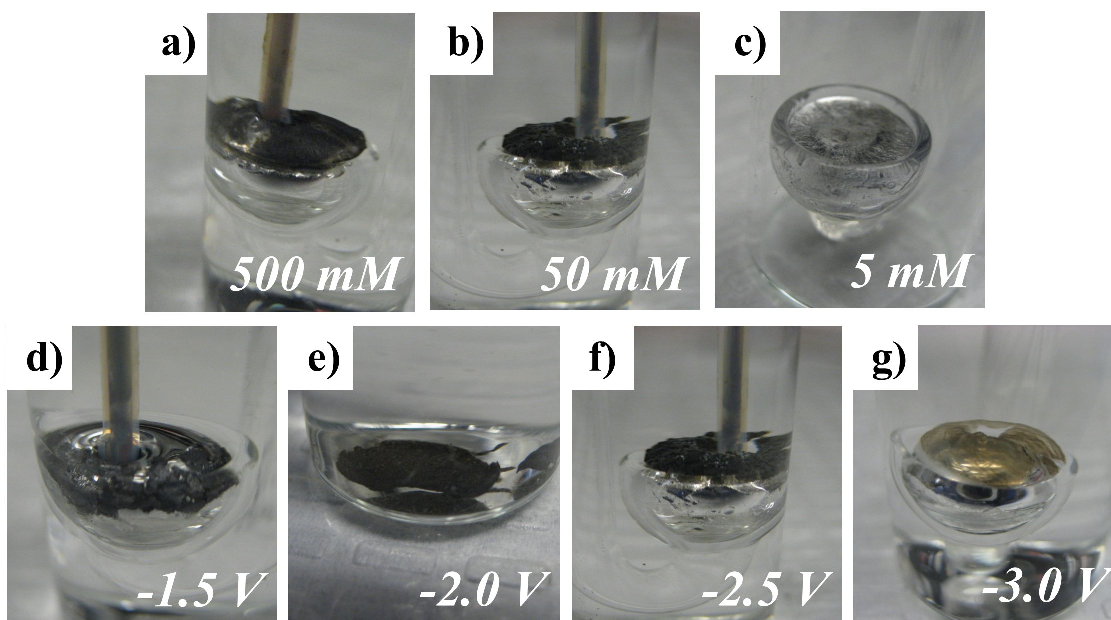

Figure 5.12. Optical micrographs of Si deposits obtained after 1 h electrodeposition at -2.5 V vs. Pt QRE at 100 ^{o}C and 2.76 MPa pressure in a propylene carbonate solution containing 0.2 M TBAC and a) 500 mM, b) 50 mM and c) 5 mM $SiCl_4$. Optical micrographs of Si deposits obtained after 1 h electrodeposition at 100 ^{o}C and 2.76 MPa pressure in a propylene carbonate solution containing 0.2 M TBAC and 50 mM $SiCl_4$ at d) -1.5 V, e) -2.0 V, f) -2.5 V), and g) -3.0 V vs. Pt QRE

V for 1 h from 500 mM, 50 mM and 5 mM $SiCl_4$ solution at 100 ^oC. Full coverage of the Si deposit could be achieved when the precursor concentration was reduced to as low as 50 mM. Decreasing the $SiCl_4$ concentration further by other order of magnitude to 5 mM resulted in no apparent deposit on the Ga(l) electrode surface after 1 h deposition, marking the lower bound for the minimal precursor needed for successful Si electrodeposition. Figures 5.12d-g show the optical images of Si deposits prepared potentiostatically at -1.5 V, -2.0 V, -2.5 V, and -3.0 V from 50 mM $SiCl_4$ solution at 100 ^oC. After 1 h deposition, full Si coverage was achieved in a potential window at least 0.5 V wide from -2.0 V to -2.5 V. When the lower over-potential was applied, only a small amount of the black dull deposit was observed at the corners of the Ga(l) electrode at -1.5 V, implying a slow growth kinetics. Applying large over-potential at -3.0 V on the contrary, yielded only transparent/brown film, reminiscent of the SiO_2 layer formed during long galvanostatic growth.

Additional key experimental parameters such as temperature and pressure were studied further to understand their influence on the deposit crystallinity and morphology. Figure 5.13a presents the X-ray diffractogram of the Si deposit obtained by electrodeposition at 100 °C yet at low (ambient) pressure, showing comparable crystalline diffraction pattern analogous to that obtained at high pressure, 2.76 MPa. The insensitivity of deposit crystallinity to the pressure variation indicates that high pressure was not responsible for the observed crystalline character of the Si deposit from the ec-LLS process. Electrodeposition carried out at slightly reduced temperature at 80 °C still yielded a crystalline deposit evidenced by the X-ray diffractogram (Figure 5.13b). Analogous electrodeposition performed at ambient temperature, 25 °C gave rise to similar dark films initially, followed by rapid discoloration over the course of a few hours. No X-ray patterns characteristic to crystalline Si was acquired on these samples. Finally, experiments in which films were electrodeposited at room temperature and then heated to 100 °C for 2 h inside the cell also produced pale, white material (Figure 5.13c). The absence of any signatures indicative of crystalline Si in these last control experiments argue for a concerted ec-LLS process in the main experiments that is not equivalent to separate electrodeposition and annealing.

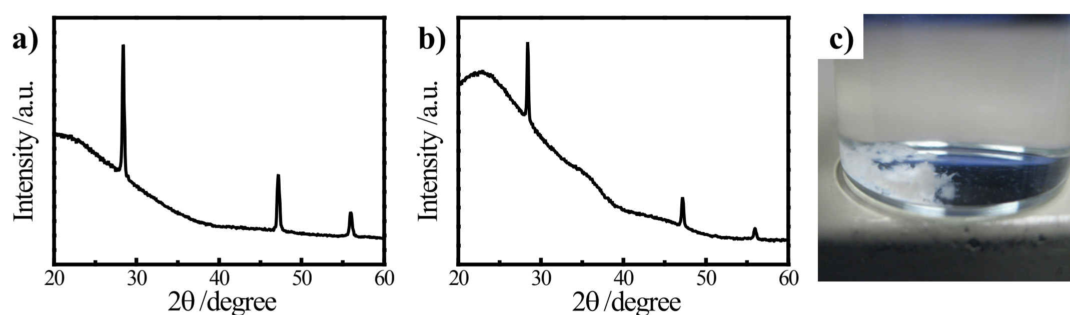

Figure 5.13. a) X-ray diffractograms of etched Si powder deposited in a propylene carbonate solution of 0.2 M TBAC and 0.5 M of $SiCl_4$ with current density of 20 mA cm^{-2} for 2 h at 100 ^oC and ambient pressure. b) X-ray diffractograms of etched Si powder deposited in a propylene carbonate solution of 0.2 M TBAC and 0.5 M of $SiCl_4$ with current density of 20 mA cm^{-2} for 2 h at 80 ^oC and 2.76 MPa pressure. c) Optical photograph of the room temperature deposit after being heated to 100 °C for 2 h inside the cell under Ar(g).

Figure 5.14 highlights the temperature-dependent morphology change at deposition temperature higher than 100 ^{o}C. The electrodeposition was carried out potentiostatically at -2.5 V vs. Pt QRE at 120, 140 and 160 ^{o}C, respectively in the propylene carbonate solution containing 0.05 M $SiCl_4$ and 0.2 M TBAC. For Si deposits obtained at 120 and 140 ^{o}C, the scanning electron micrographs (Figure 5.14a, 5.14b) show that the morphology was dominated by faceted nano-crystals, indicating the crystalline nature of the product. Further increase in the growth temperature to 160 ^{o}C resulted in the emergence of a high-aspect-ratio morphology that was not previously observed at lower temperature conditions (Figure 5.14c). Electrodepositions at temperatures higher than 160 ^{o}C were greeted with low production yield, prohibiting proper sample isolation for morphological studies. The results collectively indicate that growth temperature can be a key factor influencing the deposit morphology.

The Si deposit prepared by the ec-LLS methods was studied by Raman spectroscopy to provide further information regarding the crystallinity. Figure 5.15a shows the Raman spectra of the Si materials electrodeposit at various temperatures between 100 - 200 ^{o}C under otherwise identical conditions. Despite previous evidence supporting crystallinity based on X-ray diffraction and electron microscopy, Raman spectroscopy did not reveal a crystalline phonon mode of Si, a sharp spectral peak 520 cm^{-1} in samples prepared at temperatures between 100 - 160 ^{o}C. Conversely, only a broad feature centered around 480 cm^{-1} was observed, characteristic of amorphous Si. For Si sample prepared at 200 ^{o}C, features associated with both crystalline and amorphous Si were observed. Raman measurements were also performed to determine whether the material obtained through electrodeposition also contained a substantial amount of amorphous carbon from the decomposition of solvent at the interface with the Ga(l) electrode. A representative spectrum obtained for the as-prepared (i.e., no etching or washing steps) electrodeposited Si mass (Figure 5.15b) shows no detectable Raman signatures for either amorphous or diamond-like carbonaceous species.

Inconsistency in the crystallinity measured by Raman spectroscopy and other diffraction methods prompted further interrogation of the temperature effect on crystallinity. Various in-situ and ex-situ annealing experiments were conducted in order

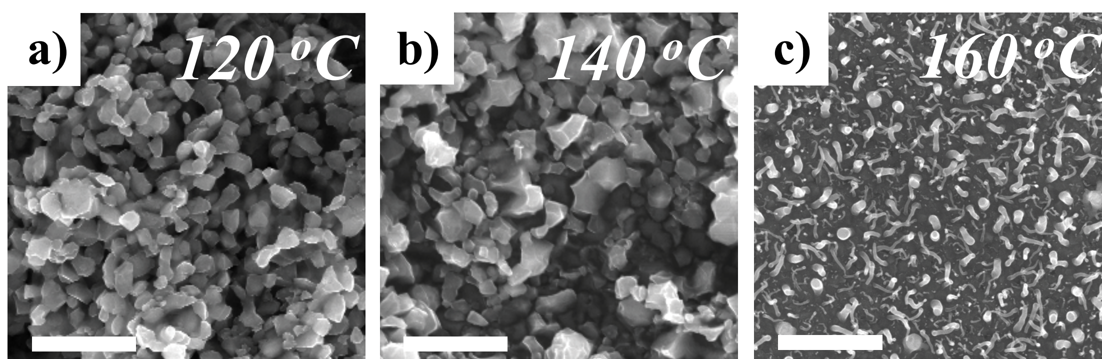

Figure 5.14. Scanning electron micrographs of Si electrodeposited at -2.5 V vs. Pt QRE in a propylene carbonate solution of 0.2 M TBAC and 50 mM of $SiCl_4$ at a) 120 ^{o}C, b) 140 ^{o}C, 160 ^{o}C, and 2.76 MPa pressure for 1 h. For c), the Ga(l) electrode was biased at initial open circuit potential value during temperature ramp to minimize Ga surface oxidation. Scale bar: 2μm.

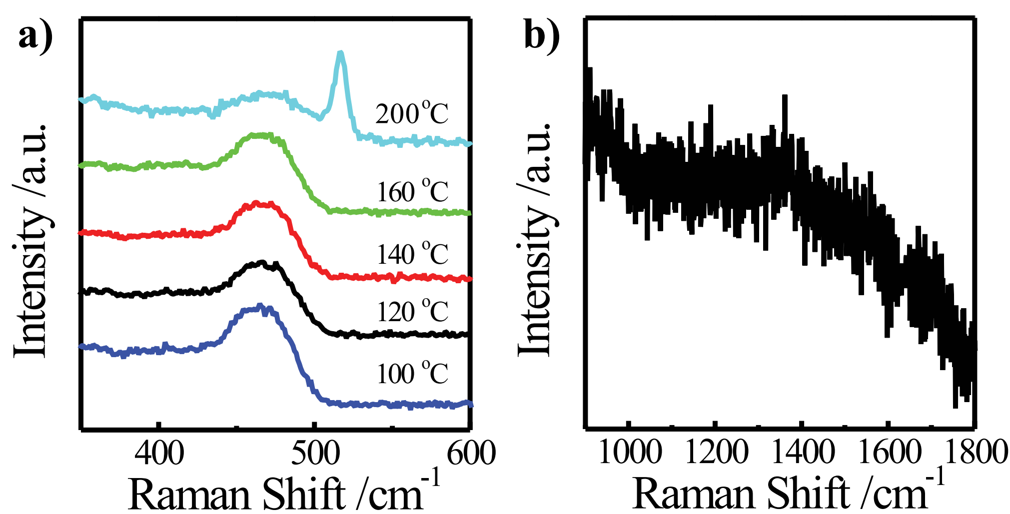

Figure 5.15. a) Raman spectra of as-deposited Si obtained on the Ga(l) electrode after electrodeposition at -2.5 V vs. Pt QRE in a propylene carbonate solution of 0.2 M TBAC and 50 mM of $SiCl_4$ at temperatures from 100 °C to 200 °C, and at 2.76 MPa pressure for 1 h. b) High wavenumber region of the Raman spectrum for an as-electrodeposited Si sample prepared by galvanostatic electrodeposition in a propylene carbonate solution of 0.2 M TBAC and 0.5 M of $SiCl_4$ at 20 mA cm^{-2} for 2 hr at 100 oC and 2.76 MPa pressure.

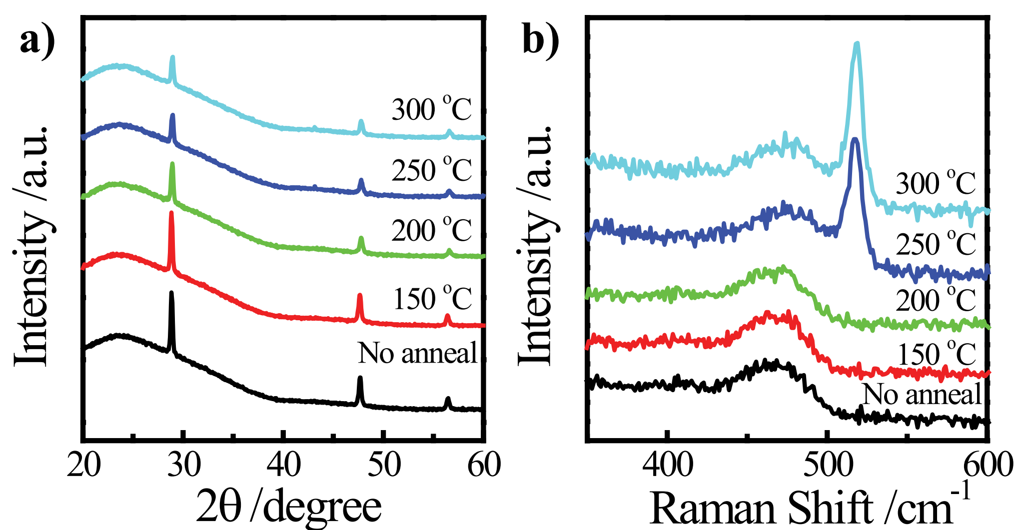

Figure 5.16. a) X-ray diffractograms and b) Raman spectra of Si deposit annealed at various temperatures up to 300 °C for 30 min at each temperature point. The starting Si sample was prepared by galvanostatic deposition with current density of 20 mA cm^{-2} for 2 hr in propylene carbonate containing 0.2 M TBAC and 0.5 M of $SiCl_4$ h at 100 °C and 2.76 MPa pressure.

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to shine light on the root cause of the discrepancy between the Raman and diffraction data. Figure 5.16a shows a series of in situ annealing X-ray diffractograms taken for Si deposit prepared initially at 100 ^{o}C by the above-described ec-LLS process. The sample was annealed in situ at the target temperature for 30 min under ambient condition prior to the data collection. No additional diffraction features were observed besides the initial crystalline Si pattern within the annealing temperature range up to 300 ^{o}C, and the diffraction pattern of Si was preserved during the entire process. The slight decrease in the diffraction intensity at high temperatures was likely due to the thermal drifting of the sample out of the probe volume. Figure 5.16b presents data summarizing a similar experiment carried out for Raman spectroscopy. Si initially deposited at 100 ^{o}C by the ec-LLS process was annealed ex situ in a muffle furnace under ambient conditions at target temperatures for 30 min. Samples after lower temperature annealing or no annealing at all showed no crystalline signature in the Raman spectroscopy. However, contrary to the temperature insensitivity of the X-ray diffraction patterns, Si sample after being annealed for at temperatures above 250 ^{o}C showed the evolution of crystalline Si phonon mode above the baseline. This set of experiments revealed a critical temperature around the 250 ^{o}C that altered the structural nature of the deposit.

Figure 5.17 presents the scanning electron micrographs of the annealed Si samples used in Figure 5.16b. As shown in Figures 5.17a-c, the morphology of the Si deposits maintained a similar faceted motif below the critical temperature. As the annealing temperature was increased above 250 ^{o}C, the surface morphology of the deposit was drastically different from that seen at low temperatures. As shown in Figures 5.17d, e, the previously discrete crystallites were fused to form continuous agglomerates. More importantly, small droplets appeared to have been 'secreted' from the Si crystal and could be found over the entire surface of the deposit. The spherical nature of the emerging particles raised the possibility of the emerging particles being liquid Ga droplets as a result of heat-induced phase separation. More direct evidence supporting the notion of thermal phase separation was captured in real time by the in situ heating scanning transmission electron microscopy. Figure 5.18a shows the high angle annular dark field (HAADF) image of the Si deposit annealed in situ. Before any annealing, the

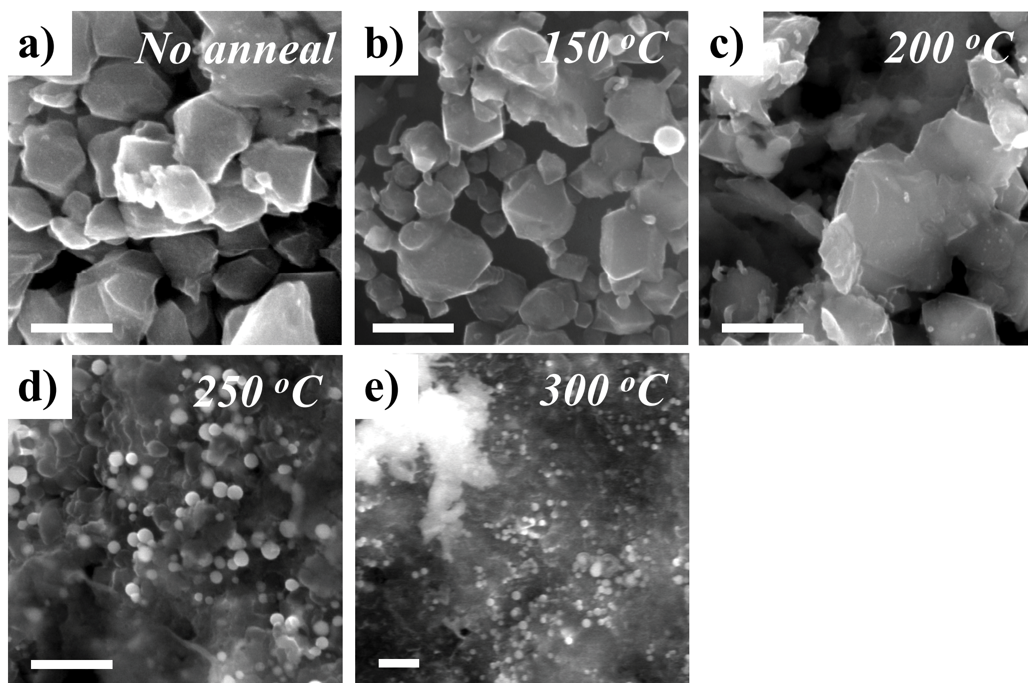

Figure 5.17. Scanning electron micrographs of Si deposit a) before annealing, after being annealed at b) 150 ^{o}C, c) 200 ^{o}C, d) 250 ^{o}C, and e) 300 ^{o}C for 30 min at each temperature point. Scale bar: 500 nm. The starting Si sample was prepared by galvanostatic deposition with current density of 20 mA cm^{-2} for 2 hr in propylene carbonate containing 0.2 M TBAC and 0.5 M of $SiCl_4$ at 100 ^{o}C and 2.76 MPa pressure.

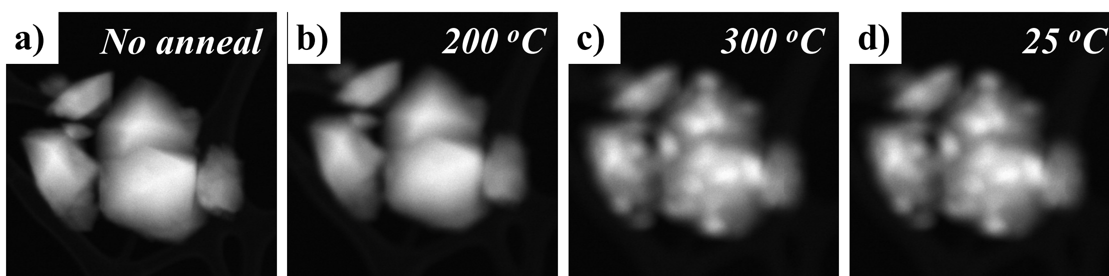

Figure 5.18. High angle annular dark field images of Si deposit a) before annealing, after being annealed *in situ* at b) 200 ^{o}C, c) 300 ^{o}C, for 5 min at each temperature point and d) after cooling down to room temperature. The starting Si sample was prepared by potentiostatic deposition at -2.5 V vs. Pt QRE for 1 hr in propylene carbonate containing 0.2 M TBAC and 0.5 M of $SiCl_4$ at 100 ^{o}C and 2.76 MPa pressure.

faceted nature of the crystal was the key feature of the deposit, consistent with the faceted morphology generally observed for ec-LLS Si crystal by scanning electron microscopy. Upon annealing, no significant morphological change was observed up to 200 ^{o}C (Figure 5.18b). The loss of image focus was caused by the thermal drift of the sample stage. Raising the annealing temperature to 300 ^{o}C (Figure 5.18c) resulted immediate deformation of the initial crystals along with the formation of multiple small particles over the entire sample. These emerging particles closely mirrored those droplets previously observed under scanning electron microscope for Si samples annealed above 250 ^{o}C. Image taken after the sample was allowed to cool down to room temperature (Figure 5.18d) was nominally identical to the high temperature image, indicating the irreversible nature of the morphological change. A repeated annealing experiment with 5 ^{o}C temperature increment revealed the same structural change for another freshly prepared sample and pinpointed the critical transition temperature to be 240 ^{o}C (Figures 5.19a-d). Time-dependent images (Figures 5.19e-h) taken continuously at 240 ^{o}C recorded real-time migration of the newly form droplets. The droplets appeared to form within the crystallite at the beginning but gradually migrated outwards to the crystal surface over the course of the experiment. Finally, compositional identification of the emerging particles was carried out *ex situ* based on a combination of HAADF images and EDS elemental maps. Figure 5.20a shows a HAADF image of a Si crystallite deposited at 100 ^{o}C before annealing. The signal appeared to be uniform across the crystallite, i.e. no abrupt change in contrast was evident, indicative of uniform elemental distribution within the sample. Elemental mapping (Figures 5.20b, 5.20c) of the same crystal also revealed even distribution of Si and Ga throughout. Absence of higher Ga signal counts (brighter in contrast) at the edge of the crystal argues against the notion that Ga is concentrated near the surface. Figure 5.20d shows a HAADF image of a different crystallite from the same sample after 30 min ex situ annealing at 300 ^{o}C, above the previously determined critical transition temperature of 240 ^{o}C. Regions with brighter contrast were observed within the crystallite, suggesting the presence of concentrated elements with larger atomic weight, consistent with the previous results from the in situ annealing experiment. These regions were then confirmed to be Ga rich based on the results of EDS elemental

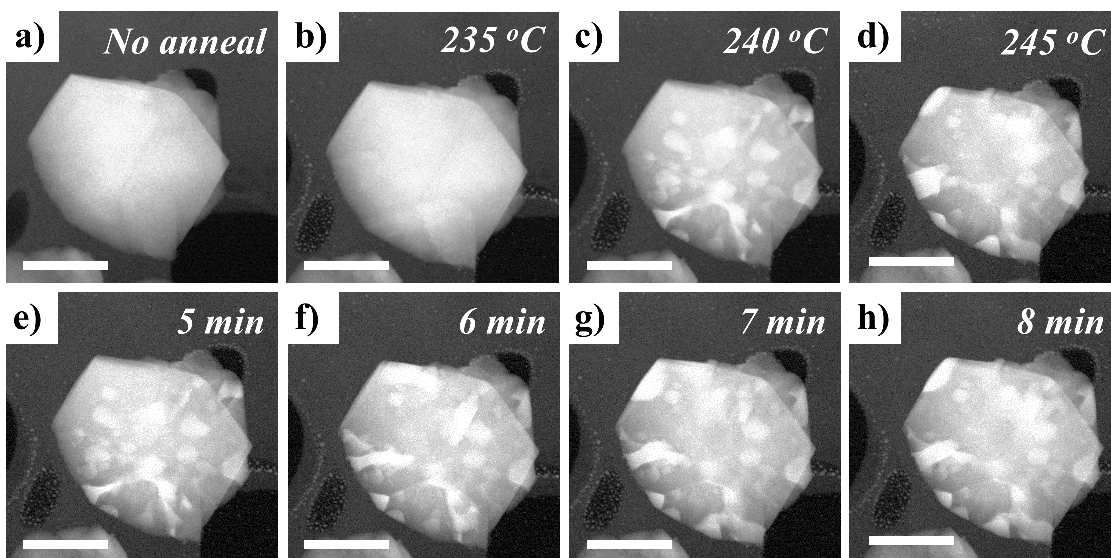

Figure 5.19. High angle annular dark field images of Si deposit a) before annealing, after being annealed *in situ* at b) 235 ^{o}C, c) 240 ^{o}C, and d) 245 ^{o}C for 5 min at each temperature point. High angle annular dark field images of Si deposit after being annealed *in situ* at 240 ^{o}C for e) 5 min, f) 6 min, g) 7 min and 8) min. Scale bar: 200nm. The starting Si sample was prepared by potentiostatic deposition at -2.5 V vs. Pt QRE for 1 hr in propylene carbonate containing 0.2 M TBAC and 0.5 M of $SiCl_4$ at 100 ^{o}C and 2.76 MPa pressure.

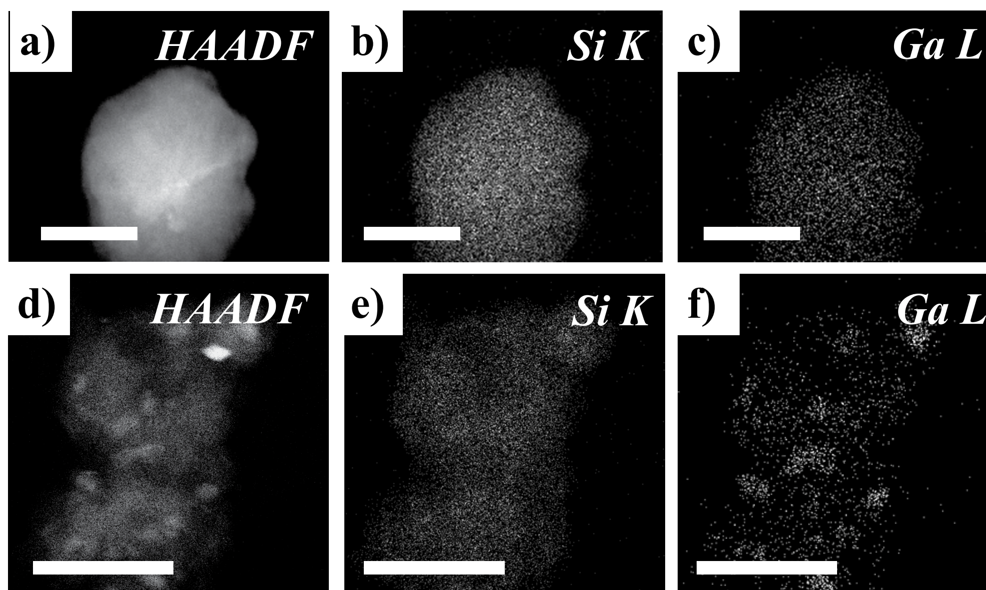

Figure 5.20. a) High angle annular dark field image, b) Si K line map and c) Ga L line map of Si deposit without thermal annealing. Scale bare: 100 nm. d) High angle annular dark field image, e) Si K line map and f) Ga L line map of Si deposit after being annealed at 300 ^{o}C for 30 min. Scale bar: 500 nm. The starting Si sample was prepared by galvanostatic deposition with current density of 20 mA cm^{-2} for 2 hr in propylene carbonate containing 0.2 M TBAC and 0.5 M of $SiCl_4$ at 100 ^{o}C and 2.76 MPa pressure.

mapping (Figure 5.20f). The thermal-induced shift in the elemental distribution strongly indicates a phase separation process takes place at temperatures above 240 ^{o}C.

D. Discussions

Collectively, the data presented here represent the first successful demonstration of an unassisted (i.e., no sonication[28], no additional chemical reductant/template[29]) electrochemical process that produces crystalline Si in a single step under mild conditions. The lowest temperature demonstrated here (80 °C) significantly bests both the previous reported record for direct electrodeposition of crystalline Si (745 °C in a fluoride melt electrolyte)[20] and more recent reports on the electrodeposition of Si through $CaSiO_3$ (850 °C in molten $CaCl_2$).[30] The electrodeposition temperatures shown here are also below the known temperature thresholds for metal-induced amorphous-to-crystalline Si transitions.[27]

In this work, the dissolved reducible species ($SiCl_4$), the electrolyte (TBACl), and the solvent (propylene carbonate) all are electrochemical components that have previously been explored separately and collectively in studies that universally yielded only amorphous Si.[8-10,31] Thus, the key innovation shown here is the specific use of Ga(l) as a liquid-metal electrode, consistent with ec-LLS at low temperatures. As described previously,[21-23] the ability of a liquid metal to act as a separate phase for recrystallization is a powerful and underutilized concept in electrochemistry. The present results are strong evidence in support of the contention that the ec-LLS approach can be exploited for the preparation of crystalline Si. Demonstration of successful Si deposition from large potential window (500 mV) using precursor with various concentrations (50 mM, 500 mM) also indicates the ec-LLS is a robust technique for Si production.

The time-dependent deposition does suggest a decrease in Faradaic efficiency over long time deposition. According to the obtained Si mass after deposition of various durations, the faradaic efficiencies of the electrodeposition were 14.0% for 15 min, 9.7% for 30 min, 3.1% for 2 hr and 1.6% for 4 hr electrodeposition. The leveling of the product quantity after ca. 1800 s suggested a sharp decrease in the growth kinetics and that the majority of the deposit was obtained within the first 30 min of the experiment. The time for the mass plateau coincided with the time at which the solvent decomposition potential

is reached, suggesting an increasing barrier for supporting the cathodic current needed for the Si reduction at prolonged deposition time. Operating at the potentials negative enough for solvent decomposition beyond the critical time point of ca. 1800 s also indicates the Faradaic efficiency for long time deposition becomes dominated by the solvent decomposition, consistent with the observed decrease in the Faradaic efficiency of Si deposition. The cessation is likely to be caused by multiple factors, based on the control experiments. First of all, the coverage of Si was complete for a 2 hr electrodeposition, suggesting the absence of available Ga sites for Si reduction at long durations. The blockage of active electrode area can also be contributed by the observed SiO_2 film. At the meantime, using fresh Ga electrode in a 2 hr old electrolyte failed to yield high coverage Si. This is indicative of possible extrinsic causes for the abated deposition, such as solvent fouling or precursor loss over the course of the deposition.

Further work is needed to advance the Si ec-LLS strategy as a practical and scalable wet-chemical process for the preparation of crystalline Si. The electrochemical reduction of $SiCl_4$ is not optimal at scale since $SiCl_4$ is readily hydrolyzed by water and is itself a high-energy-content, highly refined chemical. The reactivity of SiCl4 toward trace water in the solvent is detrimental in the presented system since an insulating film that limits the progression of Si electrodeposition can develop. Furthermore, $SiCl_4$ is prepared from Si rather than SiO_2, so this particular ec-LLS process parallels the Siemens process more than carbothermal reduction.[4] Nevertheless, further studies of Si ec-LLS with $SiCl_4$ in propylene carbonate should still be useful for understanding how the interplay of steps 2–4 in the Si ec-LLS process (Figure 5.1a) affects the resultant crystallinity/morphology. The results of such investigations should prove informative and general for the maturation of a viable ec-LLS process for crystalline Si that does use raw feedstock like silica. The electrochemical reduction of fully oxidized (low-energy-content) Si precursors in step 1 in Figure 5.1a also requires a more detailed and microscopic understanding of electrodepositions at liquid-metal electrodes. Such work is ongoing in our laboratory.

E. Conclusions

In this chapter, the data collectively demonstrated the application of ec-LLS strategy for electrodeposition of crystalline Si at low temperature from an organic

electrolyte. High coverage of crystalline Si was obtained using liquid Ga as the working electrode. The crystallinity of the as-deposited Si was verified by X-ray diffraction and electron diffraction data. Additional in situ and ex situ annealing experiments with Raman spectroscopy, X-ray diffraction, scanning electron microscopy and scanning transmission electron microscopy revealed possible phase transition of the as-deposited Si crystallites upon annealing. The cumulative data support two primary contentions. First, a liquid-metal electrode can serve simultaneously as both a source of electrons for the heterogeneous reduction of dissolved Si precursor in the electrolyte (i.e., a conventional electrode) and a separate phase (i.e., a solvent) that promotes Si crystal growth. Second, ec-LLS is a process that can be exploited for direct production of crystalline Si at much lower temperatures than ever reported previously. The further prospect of ec-LLS as an electrochemical and non-energy-intensive route for preparing crystalline Si is discussed.

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CHAPTER 6

Surface Enhanced-Raman Spectroscopy for Studying Cd-VI Electrodeposition and Surface Chemistry

A. Introduction

This chapter describes a surface-enhanced Raman spectroscopy (SERS) strategy for *in-situ* study of semiconductor electrodeposition and interfacial chemistry. Data will be shown to highlight both *ex-situ* and *in-situ* SERS spectra of Cd-VI semiconductors on Au nanoparticles substrates prepared by electrochemical atomic-layer-epitaxy (ec-ALE). The selection of suitable laser conditions (e.g. excitation wavelength, power density) for *in-situ* SERS measurement that result in minimal laser perturbation to data acquisitions will be discussed. The semiconductor thin films on SERS-active Au substrate will be served as an overlayer SERS platform for studying the vibronic processes at the semiconductor surfaces. Preliminary data on the surface functionalization of the Cd-based semiconductor thin films will be presented to demonstrate the surface sensitivity of the overlayer-SERS strategy

Electrodeposition is considered to be a facile method for preparing crystalline semiconductor materials[1,2]. Typically performed at room temperature and under ambient environment, electrodeposition provides a low cost and energy efficient solution for preparing a wide variety of semiconductors, the list of which includes but is not limited to II-IV (ZnSe[3], ZnTe[4,5], CdTe[6]), III-V (GaAs[7], InSb[8]), and tertiary ($CuInSe_2$[9]) compounds. Among various electrodeposition strategies, electrochemical atomic layer epitaxy (ec-ALE)[10] allows the formation of crystalline semiconductor materials[11-15] in a layer-by-layer fashion, introducing unique features to the semiconductor electrodeposition process, such as accurate thickness control[16,17] and superlattice manipulation[11,14,18]. The deposition process of ec-ALE is studied by various surface investigation techniques such as Low-

energy electron diffraction, Auger spectroscopy and X-ray photon spectroscopy.[19,20] These techniques suffer from limited throughput due to sophisticated sample preparation and/or sample loading. The *ex-situ* nature of these surface techniques also hinders the utilization of these methods for studying the ec-ALE crystal growth in real time during the electrodeposition.

Raman spectroscopy has been used to the perform real time investigation of electrodeposition processes due to its compatibility with ambient pressure and aqueous system.[21-23] The formation of the target semiconductor phases as well as the undesirable impurity phases can be identified by the detection of the corresponding vibrational modes in Raman spectra. Information regarding the semiconductor crystallinity can be readily obtained based on the spectral peak position, width as well as the overtone intensity.[24,25] Nevertheless, the conventional Raman spectroscopy usually experiences low signal intensity when investigating thin film semiconductor materials, which prevents the acquisition of the structural information at the early growth stage. The low signal intensity of the conventional Raman spectroscopy can be overcome by implementing surface-enhanced Raman spectroscopy (SERS) using nanostructured Au support as the signal enhancing substrate. The surface plasmon generated from the Au nanoparticle upon laser irradiation provides routine signal boost of 10^5,[26] allowing monolayer detection of the semiconductor phonon modes.[24,25]

Data will be shown to illustrate SERS as a high throughput analytical method capable of obtaining real time crystallographic information for the ec-ALE process. Layer-by-layer electrodeposition of Cd-VI semiconductors will be used as model systems for the discussion. The primary goal in this chapter is to establish the criteria of laser excitation conditions suitable for *in-situ* SERS study of semiconductor electrodeposition. Additional data will be shown to demonstrate the ec-ALE grown thin film semiconductors as SERS-active substrate for study the interfacial chemistry at the semiconductor surfaces.

B. Methods

Materials and Chemicals Methanol (Certified ACS, Fisher), acetone (Certified ACS, Fisher), isopropanol (Certified ACS, Fisher), $H_2N(CH_2)_3Si(OC_2H_5)_3$ (99%,

Aldrich), $HAuCl_4 \cdot H_2O$ (99.9%, Strem Chemicals), $Na_3C_6H_5O_7$ (98%, Acros Organics), NH_4OH (50 wt. % in H_2O, Aldrich), $CdSO_4$, TeO_2 , SeO_2 $(NH_4)S$ NaOH ,Na_2SO_4 (99+%, Aldrich), and $Na_2B_4O_7 \cdot 10H_2O$ (Analytical Reagent Grade, Mallinckrodt), Ag epoxy (CG Electronics), epoxy (1C Hysol, Loctite), H_2O with a resistivity > 18.2 MΩ cm^{-1} (Barnsted Nanopure) was used throughout. Glass coated with a indium-doped tin oxide (ITO, $R_s < 12\ \Omega\ cm^{-1}$) were used as support substrates.

Au Nanoparticle Electrode Fabrication The preparation of SERS-Active Au Nanoparticle Electrode was described elsewhere.[27] In brief, the ITO glass was used as the electrode substrate with an active surface area of ca. 0.20 cm^2. The surface of the ITO electrode was functionalized with silane-based linkers by immersing the electrode into a 10% v/v solution of $H_2N(CH_2)_3Si(OC_2H_5)_3$ in isopropanol for 48 hrs. The Turkevich method was used to prepare suspensions of Au nanoparticles through the reduction of aqueous $HAuCl_4$ by $Na_3C_6H_5O_7$ under reflux (size verified by UV-Vis absorption, λ_{max} = 518 nm). After functionalization, the ITO electrode was immersed in an aqueous colloidal Au suspension for 12 hrs, followed by through rinse with H_2O. This step was repeated two more times to obtain Au nanoparticle films that exhibited a detectable, albeit weak SERS enhancement. To increase the SERS activity of the Au nanoparticle films, the effective size of the adhered nanoparticles was increased through additional electroless plating of Au. The ITO substrate functionalized with Au nanoparticles was immersed in 10 mL of 0.01 wt. % $HAuCl_4$. 4 mL of 0.4 mM NH_4OH was added over a course of 20 minutes with stir during which the Au nanoparticle films turned from light blue to golden. The electrodes were then rinsed with H_2O, and stored at ambient before use.

Electrodeposition of Cd Chalcogenides. All electrodeposition was carried out using a CH Instruments 760C potentiostat. A single glass compartment, three-electrode cell was employed consisting of a Pt wire and a Ag/AgCl (sat. KCl) electrode as the counter and reference electrodes respectively while a Au nanoparticle electrode served as the working electrode. Cd ML was deposited in 1 mM $CdSO_4$, 100 mM Na_2SO_4 at -0.70 V vs. Ag/AgCl. The chalcogenide UPD was carried out at various potential in 1 mM $(NH_4)_2S$, 10 mM NaOH, 100 mM Na_2SO_4 for S, 5 mM SeO_2, 10 mM $Na_2B_4O_7$, 100 mM Na_2SO_4 for Se and 0.5 mM TeO_2, 10 mM $Na_2B_4O_7$, 100 mM Na_2SO_4 for Te. $N_2(g)$ was

bubbled through all solutions for 20 min prior to the start of the deposition and an N_2 atmosphere was maintained above the solution layer in the cell during depositions.

Surface-enhanced Raman Analysis Raman spectra under 633 nm and 647 nm laser excitation were collected using a Renishaw inVia Raman spectrometer equipped with a Leica microscope, an Olympus SLMPlan 20x objective (numerical aperture = 0.35), a RenCam CCD detector, a 1800 lines/mm grating, a 632.8 nm HeNe laser (Renishaw RL633), and a 647 nm ArKr Laser. Raman Spectra under 785 nm laser excitation were collected using a Renishaw Ramascopoe spectrometer equipped with a Leica microscope, a Nikon 20X objective, a 1200 lines/ grating, and a 785 nm solid state laser(Innovative Photonic Solutions). *Ex-situ* Raman spectra were acquired at ambient immediately after the deposition. *In-situ* Raman spectra were acquired in a custom built glass cell with a quartz window containing 5 mL of electrolyte, Ag/AgCl (sat. KCl) reference, and Pt coil counter electrodes.

C. Results

The influence of laser excitation wavelength on the semiconductor materials were studied both *ex situ* using dry films of CdSe after electrodeposition as well as *in situ* under the electrochemical bias during the electrodeposition process. Figure 6.1 shows the *ex-situ* SERS spectra of CdSe thin films prepared by ec-ALE obtained under the excitations of two different laser wavelengths, 647 nm and 785 nm. The initial electrodeposition of the first monolayer of Se was confirmed by the Se feature at ca. 250 cm^{-1} observed in both Figure 6.1a and 6.1b.[28] The transition from the elemental Se layer to CdSe monolayer was reflected by the disappearance of the original Raman feature at 250 cm^{-1} and the appearance of a new Raman feature close to 208 cm^{-1}, consistent with the longitudinal optical (LO) phonon mode of CdSe semiconductor. The red shift of the phonon mode away from the peak value of bulk CdSe semiconductor at 211 cm^{-1} [29] is consistent with the quantum confined nature of the as-prepared CdSe[30]. The complete disappearance of Se mode in Raman indicates that the deposition yields conformal thin film of CdSe, instead of separate domains of elemental Se and Cd. Continuing the atomic layer deposition process produces CdSe thin films with increasing total thickness,

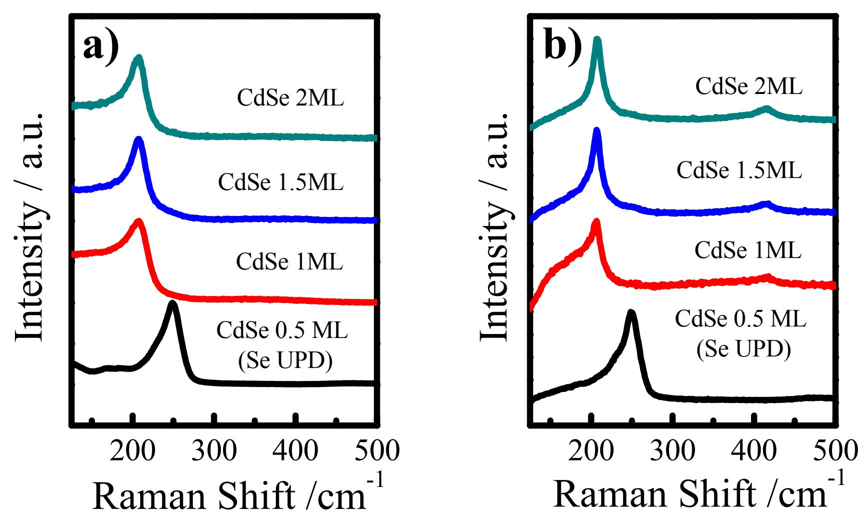

Figure 6.1. *Ex-situ* SERS spectra of multilayer CdSe dry films with increasing thickness acquired under a) 785 nm and b) 647 nm laser excitation with 1.1 mW power. Se monolayer was electrodeposited at -0.85 V for 3 min in 5 mM SeO_2, 10 mM $Na_2B_4O_7$, 100 mM Na_2SO_4. Cd monolayer was electrodeposited at -0.7 V for 3 min in 1 mM $CdSO_4$, 100 mM Na_2SO_4. Each spectrum was acquired for 10 sec and the spectra where normalized and offset for clarity.

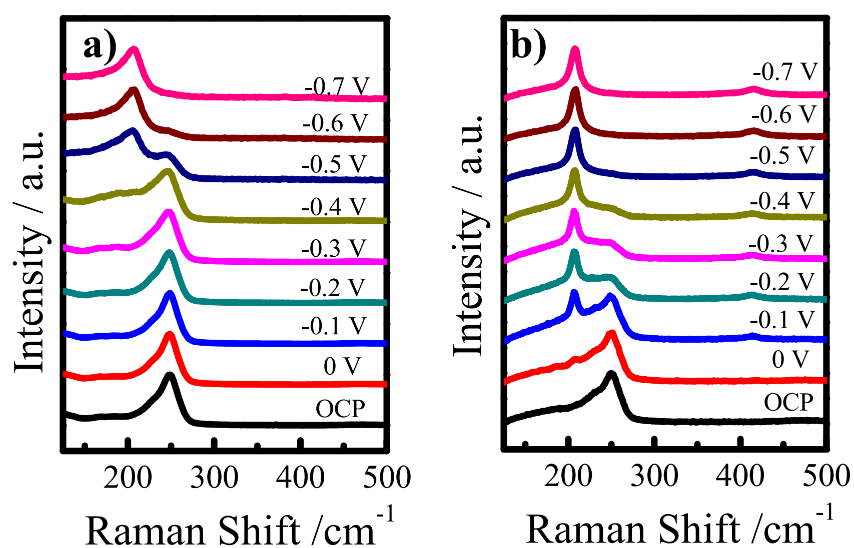

Figure 6.2. *In-situ* SERS spectra of Cd electrodeposition on Se monolayer at Au nanoparticle electrode acquired under a) 785 nm and b) 647 nm laser excitation with 1.1 mW power. Se monolayer was first electrodeposited *ex situ* at -0.85 V for 3 min in 5 mM SeO_2, 10 mM $Na_2B_4O_7$, 100 mM Na_2SO_4. The spectra were taken after the electrode was biased at the designated potential for 1 min. Each spectrum was acquired for 10 sec and the spectra where normalized and offset for clarity.

indicated by the decreasing width of the phonon mode as well as the slight blue shift of the phonon peak towards the bulk value. The difference of the spectra taken at 647 nm and 785 nm was highlighted in the absence of the phonon overtone mode at 415 cm^{-1} under the 785 nm illumination, suggesting a lack of resonance effect under longer wavelength excitation.[31]

The same electrodeposition process was then monitored *in situ* by SERS under 647 nm and 785 nm illumination conditions. Figure 6.2a shows the SERS spectra acquired under 785 nm laser excitation for an as-deposited Se monolayer immersed in a Cd precursor solution at various electrochemical potentials. At open circuit potential with no external bias, the initial Se monolayer was stable and showed a prominent feature at 250 cm^{-1}. The real-time transition from Se monolayer to CdSe monolayer was captured by the *in-situ* spectral change at -0.5 V highlighting the appearance of the CdSe phonon mode at 206 cm^{-1} as well as the diminishing of Se feature at 250 cm^{-1}. Further biasing the electrode at -0.7 V caused a slight blue shift of the peak center to 207 cm^{-1} and the complete disappearance of the Se feature. Figure 6.2b shows the *in-situ* SERS spectra of the same Cd deposition process measured with 647 nm laser excitation. Although similar spectral evolution was observed, the data showed major discrepancy in the critical potential at which the Se to CdSe transition occurs. The potential indicating the first CdSe appearance was 500 mV more positive at 647 nm than that at 785 nm. At 0 V, a small peak at 207 $cm^{-1}$was already resolved from the background indicating the formation of CdSe domain. The CdSe LO phonon was well-resolved at -0.1 V, so was the 1st order overtone at 414 cm^{-1}. The complete conversion from Se monolayer to CdSe monolayer was accomplished at -0.5 V, 200 mV more positive when the 785 nm excitation was used.

To further pursue the nature of the observed discrepancy in the transition potential, time-dependent SERS spectra were taken for the Se to CdSe transition at 633 nm laser illumination. Figure 6.3a shows the time-dependent SERS spectra of Se monolayer in 10 mM $CdSO_4$ and 100 mM Na_2SO_4 electrolyte under 633 nm laser excitation at open circuit potential. Before data acquisition, the laser shutter was kept close to avoid any laser illumination on the sample. The presence of Se monolayer was verified by the Se Raman signature observed at ca. 250 cm^{-1} in the first scan immediately after the shutter was open.

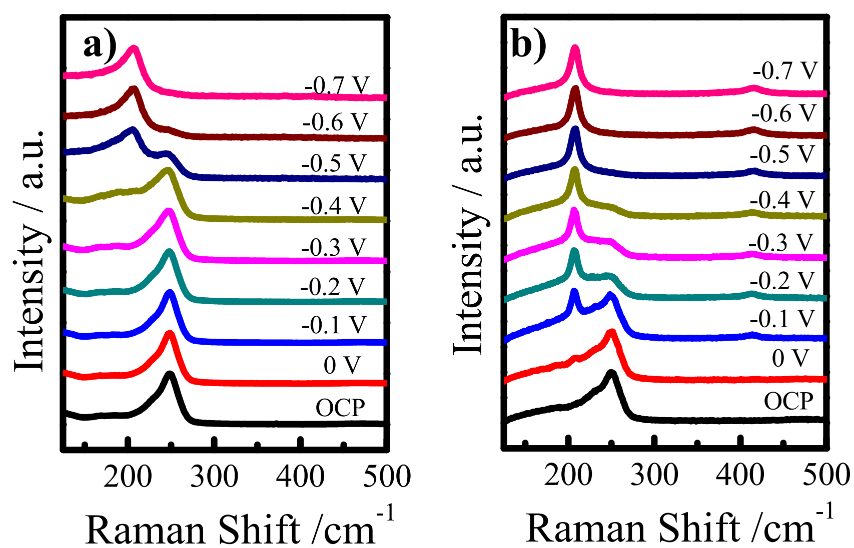

Figure 6.3. *In-situ* SERS spectra of Cd electrodeposition on Se monolayer at Au nanoparticle electrode acquired under a) 785 nm and b) 647 nm laser excitation with 1.1 mW power. Se monolayer was first electrodeposited *ex situ* at -0.85 V for 3 min in 5 mM SeO_2, 10 mM $Na_2B_4O_7$, 100 mM Na_2SO_4. The spectra were taken after the electrode was biased at the designated potential for 1 min. Each spectrum was acquired for 10 sec and the spectra where normalized and offset for clarity.

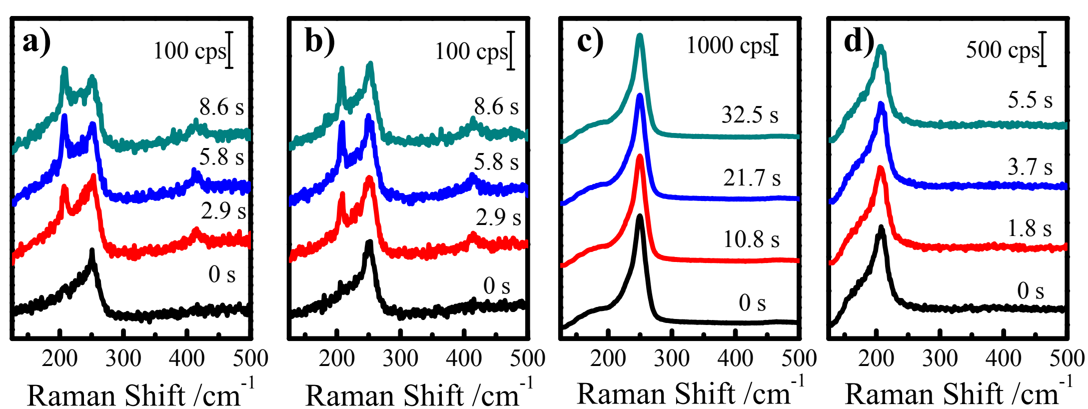

Figure 6.4. a) and b) Time-dependent SERS spectra of Se monolayer in 10 mM $CdSO_4$, 100 mM Na_2SO_4 at open circuit potential taken at two different spot on same electrode. Spectra were acquired under 4.3 mW, 633 nm excitation with 2 sec exposure. Time-dependent SERS spectra of Se monolayer in 10 mM $CdSO_4$, 100 mM Na_2SO_4 at c) open circuit potential, d) -0.7 V. Spectra were acquired under 4.0 mW, 785 nm excitation with 10 sec and 1 sec laser exposure, respectively.

In the subsequent scans after the initial 2.9 sec, the CdSe LO phonon with increasing intensity became observable at 209 cm^{-1}, indicating the formation of crystalline CdSe domain on the electrode surface. In the absence of an applied bias, such crystal transition was driven completely by the photoelectrochemistry induced by the laser. Figure 6.3b showed one repetition of the laser-induced CdSe formation at another fresh location on the same electrode. The first spectrum acquired immediately after the shutter was open showed only Se feature indicating that the CdSe observed after 2.9 sec in Figure 6.3a was a result of local laser illumination and should not be interpreted as the representative spectral feature over the entire electrode surface. Figure 6.3c shows the same deposition process with 785 nm laser excitation. Contrary to the previous SERS spectra taken at shorter wavelength, no CdSe phonon was within the time scale of the measurement when the Se-covered Au nanoparticle electrode was left at the open circuit potential. After poising the electrode at the -0.7 V (Figure 6.3d), CdSe LO phonon was clearly observed without detectable Raman signature at ca. 250 cm^{-1}. Similar wavelength dependence was also observed in the case of CdTe deposition. Figure 6.4 shows the real time spectral evolution when Te monolayer was biased at -0.5 V in the Cd precursor solution. Under 785 nm illumination, no major spectral change was observed over the course of the experiment. On the contrary, under 633 nm illumination, a sharp peak corresponding to the CdTe LO mode was resolved from the baseline.

Figure 6.5 demonstrates the influence of laser intensity on the *in-situ* SERS measurement. Figure 6.5a shows a series of time-dependent SERS spectra with 4.3 mW 785 nm laser excitation of a Cd monolayer immersed in an aqueous solution containing 0.5 mM TeO_2 biased at -0.35 V. No apparent spectral change was observed. Subsequently, the laser power was increased to 30.4 mW, and another set of time-dependent SERS spectra (Figure 6.5b) was taken at the identical sample spot. The fundamental phonon mode of CdTe was immediately observed after 4 sec irradiation, so was the 1st vibrational overtone. Figure 6.5c shows the SERS spectra at the sample spot after the power was reduced back to 4.3 mW. The phonon mode associated with crystalline CdTe could still be observed and appeared to be time-invariant, indicating the spectral transition observed under high incident laser flux is not reversible. The SERS

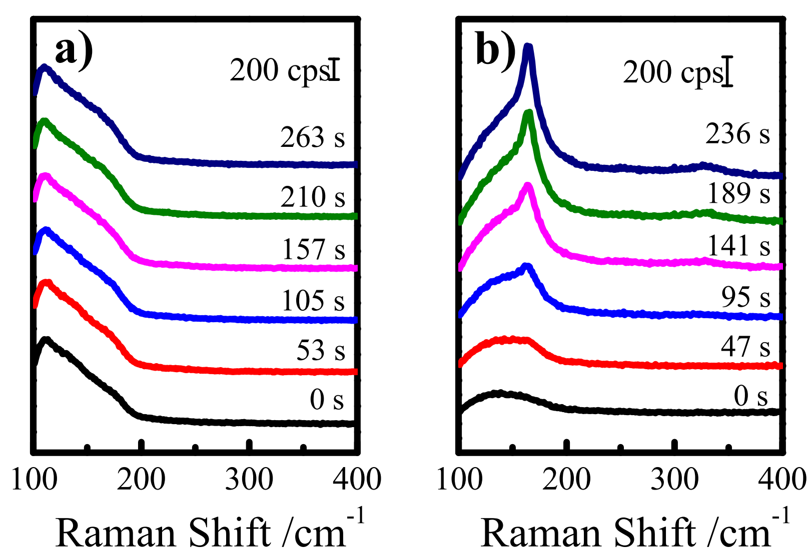

Figure 6.5. Time-dependent SERS spectra of Te monolayer in 1 mM $CdSO_4$, 100 mM Na_2SO_4 at -0.5 V. Spectra were acquired a) under 4.0 mW, 785 nm excitation with 10 sec exposure, b) 4.3 mW, 633 nm excitation with 10 sec exposure. Te monolayer was first electrodeposited *ex situ* at -0.4 V for 3 min in 0.5 mM TeO_2, 10 mM $Na_2B_4O_7$, 100 mM Na_2SO_4.

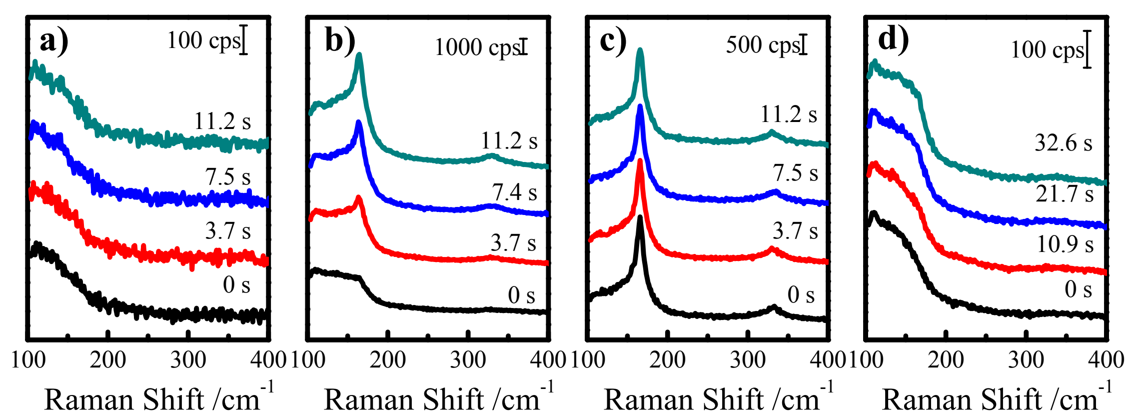

Figure 6.6. Time-dependent SERS spectra of Cd monolayer biased at -0.35V in 0.5 mM TeO_2, 10 mM $Na_2B_4O_7$, 100 mM Na_2SO_4 under a) 4.3 mW, b) 30.4 mW laser illumination, c) 4.3 mW illumination after the sample was illuminated with 30.4 mW power laser for 2 min, d) 4.3 mW illumination at a new location on the same electrode. All spectra were taken under 785 nm laser excitation. Cd monolayer was first electrodeposited *ex situ* at -0.7 V for 3 min in 1 mM $CdSO_4$, 100 mM Na_2SO_4.

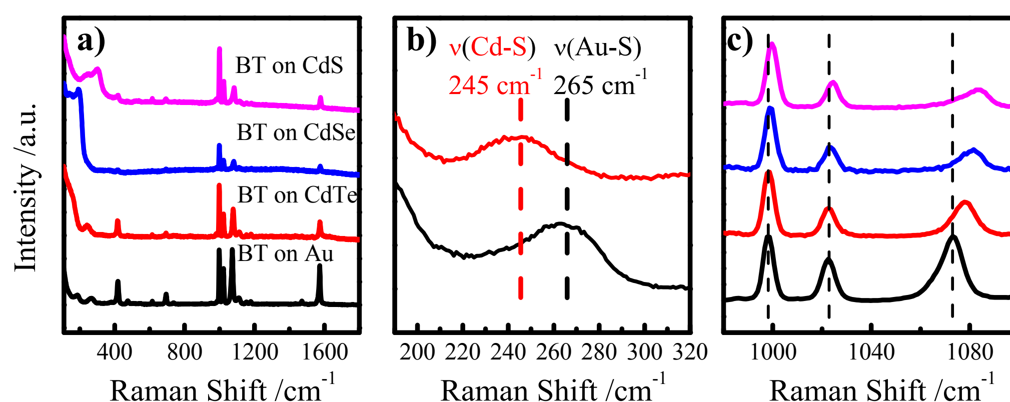

Figure 6.7. a) SERS spectra of benzenethiol adsorbed on bare Au, CdTe, CdSe and CdS monolayer. b) Surface vibration region of the SERS spectra of adsorbed benzenethiol on bare Au and CdTe monolayer. c) Molecular vibration region of the SERS spectra of adsorbed benzenethiol on bare Au, CdTe, CdSe and CdS monolayer. The spectra were collected at 785 nm laser excitation, 1.1 mW power with 10 sec exposure. Spectra were offset for clarity.

spectra were acquired again at 4.3 mW laser illumination at a new location within the same sample (Figure 6.5d), and no Raman features related to crystalline CdTe was observed.

Figure 6.6 demonstrates the application of the electrodeposited Cd chalcogenide monolayer on Au nanoparticle surface as a SERS-active platform for studying the interfacial bonding of organic ligands at the semiconductor surfaces. *Ex-situ* SERS spectra were acquired for benzenethiol-treated CdS, CdSe and CdTe monolayer thin films on Au nanoparticle electrode support (Figure 6.6a). SERS spectrum of bare Au nanoparticle electrode treated with benzenethiol was also obtained as the reference. Figure 6.6b highlights the low wavenumber spectral feature of benzenethiol at CdTe and Au surface assignable to the surface stretching mode between the interfacial metal atom and the binding sulfur atom from the benzenethiol. A 20 cm^{-1} shift in the vibration mode was noted for the benzenethiol bonded to CdTe compared to that bonded to bare Au. The detection of such surface vibration mode at CdTe interface provides direct spectroscopic evidence for chemical bond formation between benzenethiol and Cd atom at CdTe interface. Surface vibration mode was not resolved for benzenethiol on CdSe or CdS due to the interference from the semiconductor phonon signature.

D. Discussions

The data have collectively demonstrated that SERS can be used to study real-time ec-ALE processes of Cd-VI semiconductor materials as well as the interfacial chemistry at the semiconductor surfaces. The critical prerequisites for accurate reflection of the electrodeposition process rely on the choice of proper laser excitation condition such as wavelength and intensity. Using laser with high intensity causes undesirable increase of the local temperature at the sample spot under investigation.[32-34] Such annealing effect has been widely observed for crystallization of amorphous semiconductor materials.[35-37] In addition to the thermal annealing effect, the *in-situ* investigation of electrodeposition process can be subjected to undesirable laser-induced photoelectrochemical effect[38,39]. Such effect was highlighted in the discrepancy in the transition electrochemical potential of Se monolayer to CdSe monolayer during the Cd electrodeposition under 647 nm and 785 nm laser excitation at comparable illumination intensity. Under the illumination of

647 nm laser, the electrodeposition potential of Cd was shifted ca. 500 mV more positive, which indicates that reduction of Cd was greatly facilitated by the incident laser. The local formation of CdSe under 633 nm laser illumination without applied electrochemical potential suggests that the reduction of Cd can even be driven solely by laser illumination. The effectiveness of the photoelectrochemical reduction processes appears to be influenced by the choice of incident laser wavelength. By using a low energy photon at sub-bandgap 785 nm, such undesired processes can be minimized and the actual electrochemical potential for monolayer CdSe formation can be obtained *in situ*. Due to the potential misinterpretation of the SERS data due to laser-induced spectral features, it is essential to use minimal incident laser power and sub bandgap laser excitation when conducting SERS experiments.

With properly chosen laser excitation conditions, SERS can serve as a powerful *in-situ* technique to study the electrodeposition process, especially at the initial stage. The high surface sensitivity granted by the Au nanoparticle electrodes allows real-time measurement of structural transition from Se, Te monolayers to CdSe and CdTe bilayer during the electrodeposition process. As a result, the electrochemical potential that yields pure phase Cd-VI can be determined *in situ* based on the complete disappearance of the pure phase chalcogenide monolayer signal. The electrochemical parameters for electrodeposition at initial stage can be conveniently determined in such real time manner with no requirement for ultrahigh-vacuum-based techniques. The crystallinity of the deposit with increasing layer thickness can be further evaluated by the peak width and position of the phonon mode. Blue shift of the peak position as well as decrease in the line width is observed for CdSe of increasing layer thickness, indicating improved crystallinity.

The semiconductor thin films prepared by ec-ALE on the Au nanoparticle electrodes can be used as a SERS-active platform for studying the interfacial chemistry at the semiconductor surfaces. The plasmonic enhancement from textured Au has been demonstrated to propagate through thin overlayers of metals[40-42] or dielectric materials[43] to enable SERS measurements at the overlayer interfaces. The same principle is applied in the chapter behind the overlayer SERS measurement at the semiconductor thin film surfaces. Using this overlayer SERS strategy, the adsorption of benzenethiol monolayer

at CdTe interfaces was confirmed by the observation of the Cd-S surface vibration mode in the low wavenumber region. A 20 cm^{-1} downshift of the surface vibration frequency of Cd-S comparing with that of Au-S implies a weaker metal-sulfur bond of Cd-S than that of Au-S according to the simple harmonic oscillator approximation. More quantitative details regarding the bonding energetics require more comprehensive modeling using density functional theory[44,45]. The molecular vibration region of benzenethiol at Au and Cd-VI surface appears to be mostly identical except for the known 'surface sensitive mode at 1080 cm^{-1}. As a coupled mode of phenyl ring deformation and C-S stretching, its SERS peak position and intensity changes at CdS, CdSe and CdTe. This indicates that the thiol bonding at the Cd chalcogenide surface is not only sensitive to the type of immediate bonding atom, but is also influenced by the type of underlying chalcogenide atom. Such sensitivity of the vibration mode to the bonding environment suggests that bonding energetics of benzenethiol on CdS, CdSe and CdTe are not identical even the adsorption is all established through the Cd-S bond.

E. Conclusions

The collective data have demonstrated that SERS can be used as a convenient, high throughput method to study ec-ALE processes at ambient condition *in situ*. In order to obtain accurate structural information from the SERS spectra, low laser intensity as well as the long wavelength laser excitation is desired. With properly-selected laser excitation conditions, the crystallinity of the Cd-VI monolayers prepared by ec-ALE can be studied and described by the phonon lineshape, peak position and width both *ex situ* and *in situ*. Such prepared monolayer semiconductor thin films were used as the SERS platform to study the chemical bonding between benzenethiol on CdS, CdSe and CdTe surfaces. These data highlighted the capacity of SERS for studying the electrodeposition process for semiconductor thin films as well as the overlayer SERS strategy for studying interfacial chemistry of adsorbate bonding.

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CHAPTER 7

Conclusions and Future Work

A. Conclusions

This thesis established the ec-LLS process as a versatile material synthetic strategy for preparing crystalline group IV semiconductor materials under benign conditions. Both the fundamental and practical perspectives of ec-LLS were investigated to establish experimental guideline for preparing crystalline Ge and Si materials with desired size and morphology. The potential applications of the ec-LLS method as a fabrication method for function device components were also discussed. The key findings were summarized as follows.

First, the liquid metal electrode plays an essential role in an ec-LLS process, as both a conductive substrate as well as a crystallization solvent. Consequently, the composition of the liquid metal has significant influence on the product crystallinity and morphology. The comparison between the Ge materials obtained on liquid Ga electrode and those obtained on liquid Hg electrode highlights the solubility of the product in the liquid metal electrode as the most deterministic factor during crystal formation. Ge with crystalline domain at a micrometer scale can be readily obtained on liquid Ga electrodes due to the small degree of supersatuation during nucleation as a result of large Ge solubility in Ga. The composition of the metal also plays a key role in epitaxial growth of Ge nanowire on the nano-sized metal catalyst, as shown in Chapter III and Chapter IV. Under identical electrodeposition conditions, epitaxial growth of Ge nanowires was only achieved on Ga nanodroplets but not on In nanoparticles. The large solubility and mobility of Ge in Ga allows a heterogeneous nucleation process to occur at the crystalline substrate surface, leading to the epitaxial crystal growth. Electrodeposition of Ge on In nanoparticles on the contrary is dominated by a homogeneous nucleation process within the In nanoparticles due to limited solubility and mobility of Ge in In.

Besides, the ec-LLS process can be applied to liquid pool electrodes as well as nano-sized metal seeds on a conductive support. The size and morphology of the deposits can thus be manipulated by proper control of the beginning state of the liquid metal electrodes. Faceted crystals can be obtained by using liquid metal pool electrodes that facilitate an isotropic growth pattern, as demonstrated by the Ge (Chapter II) and Si (Chapter V) deposition on Ga pool electrode. Conversely, using nano-sized growth seeds on conductive supports will favor an anisotropic growth process, and typically yield nanowire morphology. Such growth pattern was shown in the case of Ge nanowire growth on In nanoparticles (Chapter III) and Ga nanodroplets (Chapter IV). The nanowire growth seeded by discrete metal also allows facile diameter control of the nanowire by managing the initial size of the metal seeds. Strong correlation between nanowire widths and nanoparticle diameters were observed the Ge nanowire growth on both In and Ga.

In the end, the ec-LLS process has also been demonstrated as a direct fabrication tool for preparing functional device components. As shown in Chapter III, Ge nanowires prepared by the ec-LLS method maintains electrical contact to the underlying substrate through the In nanoparticles. The as-deposited nanowire thin films exhibited high charge capacity as Li^+ battery anode materials, comparable to those prepared by conventional high temperature methods. In Chapter V, electrically-integrated Ge nanowires were prepared by room temperature ec-LLS epitaxy, and the rectifying effect was demonstrated by the conductive atomic force microscopy.

B. Future Work

i. Improving Purity of the ec-LLS Deposit

Highlighting the exploratory work for understanding the ec-LLS growth method, the thesis has placed the emphasis on showcasing the utility and scope of this newly-established synthetic approach, yet numerous questions regarding the fundamental aspects of ec-LLS still remain unanswered. These questions, if properly answered will provide further knowledge that is essential for evaluating the potential of ec-LLS as an alternative material preparation method. One of the key questions remains unanswered is the observed discrepancy in the crystallinity of the ec-LLS deposit measured by

diffraction-based techniques and by Raman spectroscopy. Such discrepancy hints additional complication in the crystal composition of the as-deposited material by ec-LLS. Preliminary annealing results discussed in Chapter V suggest the presence of incorporated Ga within the Si lattice in a meta-stable manner. The detection of Ga element in the Si lattice using energy dispersive X-ray spectroscopy indicates a minimal of 0.1 % Ga incorporation at room temperature, a value significantly higher than the equilibrium concentration allowed by the phase diagram. Such deviation from the equilibrium condition indicates the crystal growth in ec-LLS is primarily driven by a kinetic process. Future investigation should device a combined strategy using both experimental and computational techniques to establish a theoretic base for the formation of such meta-stable structure. Density functional theory (DFT) will be leveraged to calculate the energetics of the meta-stable structure under question in order to evaluate the accessibility of such structure during crystal formation. The DFT simulation is also capable of computing the energetic barrier for the phase transition from the meta-stable state to the pure-phase structure and predicting the thermal energy required to trigger the transition. The calculated transition temperature should be compared to the experimental value of 240 ^{o}C determined in the annealing experiment for the Ga-incorporated Si crystals. On the other hand, experimental quantification of Ga incorporation is critical for providing accurate initial conditions for the structural modeling, thus needs to be the focus of the experimental effort. Quantitative electron energy loss spectroscopy and atom probe tomography are both viable techniques to provide compositional information at microscopic scale. In addition, these techniques can reveal spatial distribution of the incorporated elements within the nanowires and nanocrystals so that the time-dependence of the incorporation process during the crystal formation can be probed. Collectively, these efforts will help shine light on the cause for Ga incorporation during the ec-LLS process.

Separately, systematic study will be performed to bring insight to how various experimental factors influence the incorporation of growth catalyst into the product lattice, paving paths for obtaining high purity crystals as well as achieving controlled doping in the semiconductor materials prepared by the ec-LLS methods. The study will focus on the effect of both environmental conditions, such as temperature and pressure as

well as experimental parameters including applied waveform, precursor concentration and pH value of the deposition electrolyte. Experimental temperatures play essential roles in determining the thermodynamics of the crystal formation as it may shift the energetics for the meta-stable phase formation. Increasing reaction temperature also favors the formation of thermodynamically stable product, i.e. the pure phase group IV crystals by limiting the kinetically-controlled pathways. The crystal growth kinetics can also be modulated to control the level of catalyst incorporation by tuning the electrochemical driving force during the electrodeposition. By slowing down the electrochemical reduction of the initial precursor onto the liquid metal surface, the crystal growth will be allowed to occur near equilibrium condition, favoring the formation of stable-phase product. Experimentally, such goal can be achieved either galvanostatically using small cathodic current or potentiostatically using low over-potential. Applying pulsed waveforms may yield similar effect as the pulses allow extra time for the atoms to reach equilibrated configuration during crystal growth. Other strategies to favor the thermodynamic pathway include lowering the concentration of the precursors in the solution or introducing binding ligands to slow down the electrochemical reduction kinetics.

ii. r-GO Functionalization of Au Electrode for in-situ TEM Study for ec-LLS Processes

In this thesis, the primary investigation tools for understanding various material properties of the ec-LLS product were limited to conventional analytical techniques such as X-ray diffraction, scanning electron microscopy and transmission electron microscopy, and were typically applied after the material preparation was complete. Even though such analyses were critical in supporting the key findings in this thesis, these post-synthesis techniques were not capable of providing structural and compositional insight during the electrodeposition and crystal growth process in real time. Such ability to observe and monitor the growth process *in situ* can generate rich information regarding the crystal nucleation and growth kinetics as well as kinking and defect formation. Among various *in-situ* techniques, *in-situ* transmission electron microscopy has attracted much attention in the field of nanomaterial synthesis[1-3] and electrodeposition[4,5], due to its ability to provide high spatial and temporal resolution during the material preparation process.

Successful implementation of the *in-situ* TEM technique for studying the ec-LLS process relies on specially designed electrochemical cells equipped with electron-transparent SiN membrane that can withstand the high vacuum environment in the TEM column. Due to complications in the fabrication process, degenerately-doped Si or Ge substrate cannot be directly integrated into the *in-situ* cell as the working electrode. As a result, an ultrathin Au membrane was used instead in the available cell design.

In order to perform the *in-situ* TEM experiment on the ec-LLS growth of Ge nanowires, the Ge nanowire growth needs to first be reproduced on Au working electrodes. The existing protocol for preparing Ge nanowires by ec-LLS on single crystal Ge substrate utilizes electrodeposited Ga nanodroplets as the liquid-phase seeding material. The challenge for replicating such protocol on Au electrode stems from the difficulty in re-creating the Ga nanostructure on the Au electrode surface. Figures 7.1a and 7.1b show the plan-view scanning electron micrographs of the Au electrode surface before and after the electrodeposition of elemental Ga. The Ga electrodeposition was carried out by cycling the Au electrode in an aqueous solution containing 100 mM $Ga(NO_3)_3$ and 100 mM KNO_3 between 0.4 V and -1.8 V at 25 mV/s for 2 cycles. No apparent morphological change associated with Ga deposition was observed. At the same time, elemental analysis (Figures 7.1c and 7.1d) did confirm the presence of Ga element after the electrodeposition. The lack of distinguishable Ga morphology suggests the electrodeposited Ga formed a thin film covering the Au electrode surface. The Ga thin film in direct contact with the Au electrode appears to be no longer active for the subsequent ec-LLS process, as the attempt to deposit Ge nanowire on the Ga thin film failed to yield any detectable Ge deposit.

To preserve the nanodroplet morphology of the electrodeposited Ga as well as its ability to seed the ec-LLS growth on the Au electrode support, surface modification was carried out to create ultrathin reduced grapheme oxide (r-GO) interlayer that chemically isolates the electrodeposited Ga from the underlying Au substrate while maintaining electrical conductivity. Figure 7.2 summarizes the preliminary results of the effect of r-GO functionalization on the Ga electrodeposition and the Ge nanowire ec-LLS growth.

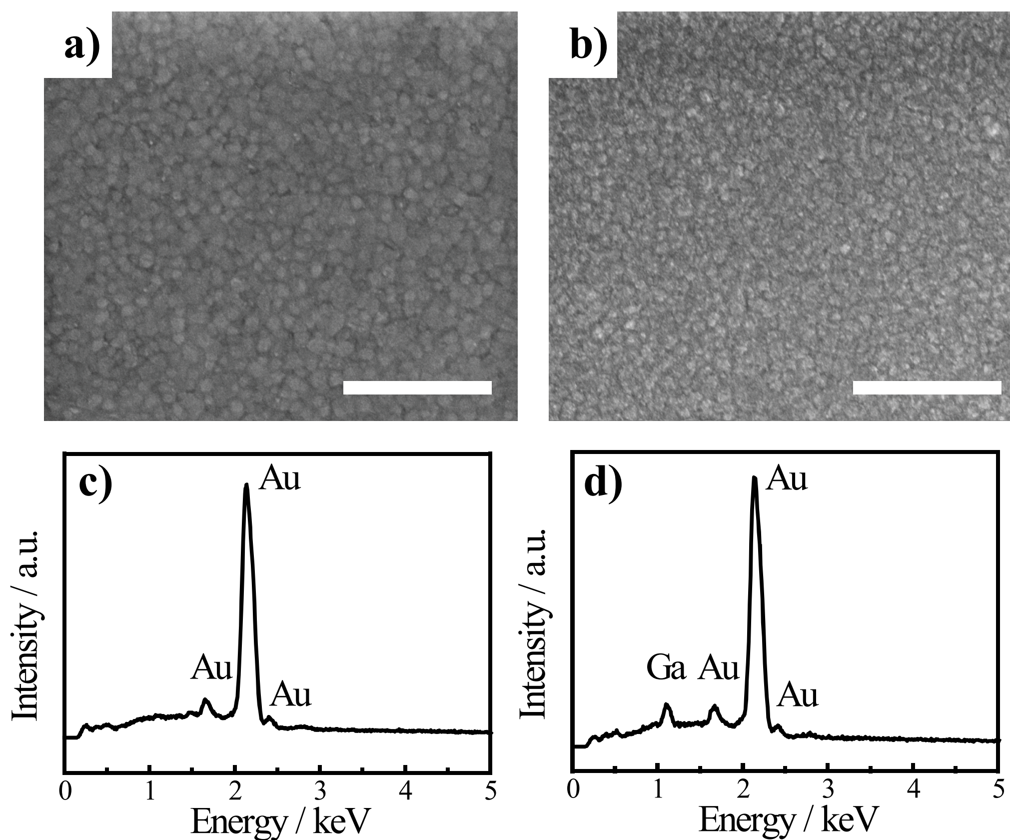

Figure 7.1. Scanning electron micrograph of Au electrode a) before and b) after Ga electrodeposition. Energy dispersive X-ray spectroscopy of the Au electrode c) before and d) after Ga electrodeposition.

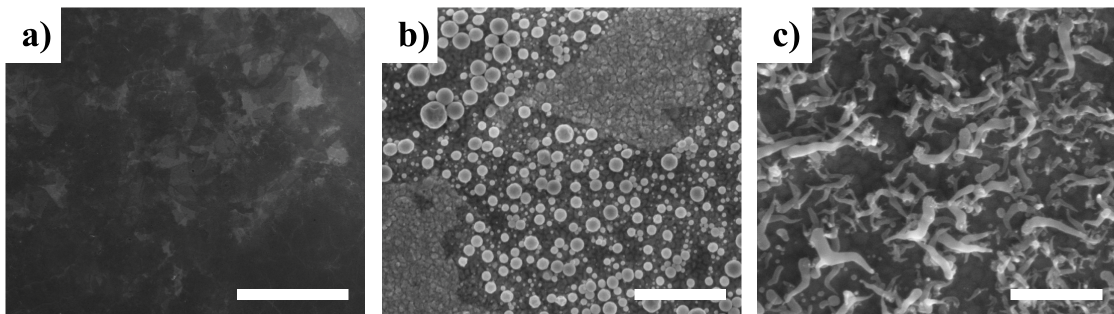

Figure 7.2. Scanning electron micrograph of the Au electrode surface after sequential electrodeposition of a) r-GO thin film, b) Ga nanodroplet and c) Ge nanowire.

Figure 7.2a shows the Au electrode surface after r-Go modification viewed under scanning electron microscope. The surface modification was achieved by electrochemically cycling the Au electrode in a graphene oxide suspension between -0.1 V and -1.4 V at 25 mV/s for 2 cycles. The area covered by r-GO on the electrode could be seen as the overlapping dark sheets under the electron microscope. The electrodeposition of Ga was then carried out using identical protocol as was used for the bare Au substrates in Figure 7.1b. Figure 7.2b presents the scanning electron micrograph after Ga electrodeposition showing the discrete nanodroplet morphology on the surface. The selective formation of these Ga nanodroplets only on the dark r-GO region supports the notion that r-GO functionalization allows the preservation of the Ga nanostructure on the Au electrode. Ge electrodeposition was subsequently performed on these Ga nanodroplets by potentiostatic deposition at -1.6 V for 30 min from a solution containing 50 mM GeO_2 and 10 mM $Na_2B_4O_7$. The scanning electron micrograph (Figure 7.2c) confirms the formation of nanowire morphology on the Au surface, indicating the introduction of the r-GO interlayer also preserves the catalytic activity of Ga droplet towards ec-LLS growth. Collectively, these preliminary results summarize the challenges and effort to replicate the Ge ec-LLS process on Au working electrode for *in-situ* TEM study. Further optimization is needed to improve the coverage of the r-GO thin film on the Au electrode by adjusting the precursor suspension concentration and the electroreduction parameters. Other methods to achieve surface modification such as direct graphene transfer should also be investigated.

iii. Studying Semiconductor Surface Chemistry by in-situ SERS and DFT Simulation

Chapter 6 focused on the fabrication of SERS-active substrates using ec-ALE method that can be used for studying the interfacial chemistry at the semiconductor surface. Detection of the monolayer thiol molecules adsorbed on Cd-VI thin films by SERS provides a unique opportunity for future investigation of the bonding character of thiol molecules at these surfaces. The main tactic for the investigation will leverage the electric field dependence of the spectral feature, known as the Stark effect. The magnitude and direction of the spectral feature shift under the influence of the external electric field reveals information such as bonding energetics and covalent/ionic character.

Experimentally, the Stark effect can be captured by measuring the spectral shift in vibrational spectroscopy under various electrochemical biases. Such strategy can be readily adopted in an *in-situ* electrochemical SERS setting, owing to the high compatibility of Raman spectroscopy with aqueous electrochemistry. The Raman-transparency of the water guarantees minimal spectral interference from the aqueous electrolyte during the Stark effect measurement.

An example for the Stark effect of chemisorbates on semiconductor thin films is shown in Figure 7.3. Figures 7.3a and 7.3b highlight the spectral shift of the surface vibration mode and the molecular vibration mode of adsorbed benzenethiol at CdTe surface under different electrochemical biases in an aqueous solution containing 10 mM $Na_2B_4O_7$ and 100 mM Na_2SO_4. At more positive potential, the 245 cm^{-1} feature assignable to the metal-sulfur surface stretching is blue-shifted, while the high wavenumber molecular vibration mode is red-shifted. The strengthening of the surface bonding as well as the weakening of the molecular vibration mode suggests an attraction of the electron density towards the electrode interface at positive electrochemical bias. Such attraction is characteristic of a ligand-to-metal charge transfer process across the interface. As depicted in the schematic in Figure 7.3c, the ligand-to-metal charge transfer process is facilitated at more positive bias, resulting in an enhancement in the surface bonding strength. The opposite will be expected if the surface interaction is primarily contributed by the metal-to-ligand back-bonding.

Further comprehensive depiction of the surface bonding character requires additional input from computational perspective using density functional theory. Two primary parameters, the static dipole moment and the dynamic dipole moment can be obtained from DFT simulation, and are critical for understanding the interaction between the organic adsorbate and semiconductor surface. The static dipole moment μ_s is the negative derivative of the bonding energy with respect to the electrical field strength, which describes the extent and direction of the charge separation of the surface bond at equilibrium bond distance. The dynamic dipole moment μ_d is the derivative of the static dipole moment with respect to the bonding distance, and dictates how the charge separation changes as the adsorbate approaches or leaves the semiconductor surface. The positive/negative signs of these two quantities divide all adsorbates into four categories,

anionic, cationic, covalent with ligand-to-metal charge transfer and covalent with metal-to-ligand charge transfer. Preliminary simulation was carried out for various adsorbates on Au clusters to determine their bonding character.

Figure 7.4a shows the cluster model used in the DFT simulation. A two-layer cluster was used to represent the Au metal or Cd-VI semiconductor surface. All DFT calculations were employed using the Amsterdam Density Functional package (ADF 2010.02c). A triple-ζ polarized (TZP) Slater-type basis set was applied for all atoms while the inner cores of the atoms were frozen to the following orbitals: C 1s, N 1s, O 1s, Na 1s, Au 4d, Cd 3d, S 2p, Se 3d, Te 4d. The Kohn-Sham one-electron equations were separately solved using the Becke-Perdew (BP86) function of the generalized gradient approximation (GGA) and Vosko-Wilk-Nusair form of the local density approximation (LDA). Scalar relativistic effects were considered within the zeroth-order regular approximation (ZORA). The (111) surface of the Cd-VI was modeled using a two-layer Cd_7X_6 (X=S, Se, Te) cluster with C_{3v} symmetry. The bond distances within each cluster were fixed at the experimental value of their corresponding bulk zincblende crystal. Monoatomic adsorbates (S, N, Na) were attached to the central atop Cd to maintain the C_{3v} symmetry of the complex, and the molecular adsorbates (trifluoromethylbenzenethiol, 4-methoxybenzenethiol) were attached the central atop Cd with the C_s symmetry enforced. Binding energies of the cluster-adsorbate bond were determined by subtracting the total energy and isolated adsorbate and cluster from that of the cluster-adsorbate complex. For field-dependent study, variable homogenous electric fields were applied along the Cd-adsorbate bond. Prior to the calculation of the bonding energy, both the isolated adsorbates and the adsorbate-cluster complexes were allowed to relax in the applied electric field to reach the optimal geometries.

The computed values of μ_s and μ_d for various adsorbate-surface pairs are summarized in Figures 7.4b and 7.4c. Monoatomic adsorbate Cl and Li were chosen as standard examples for anionic and cationic adsorbates, respectively. For cationic adsorbate like Li, the adsorbate holds partial positive charge at equilibrium bond distance, giving rise to the positive μ_s value in the simulation. As the cationic adsorbate moves away from the surface, it becomes completely ionized, gaining a full positive charge. The

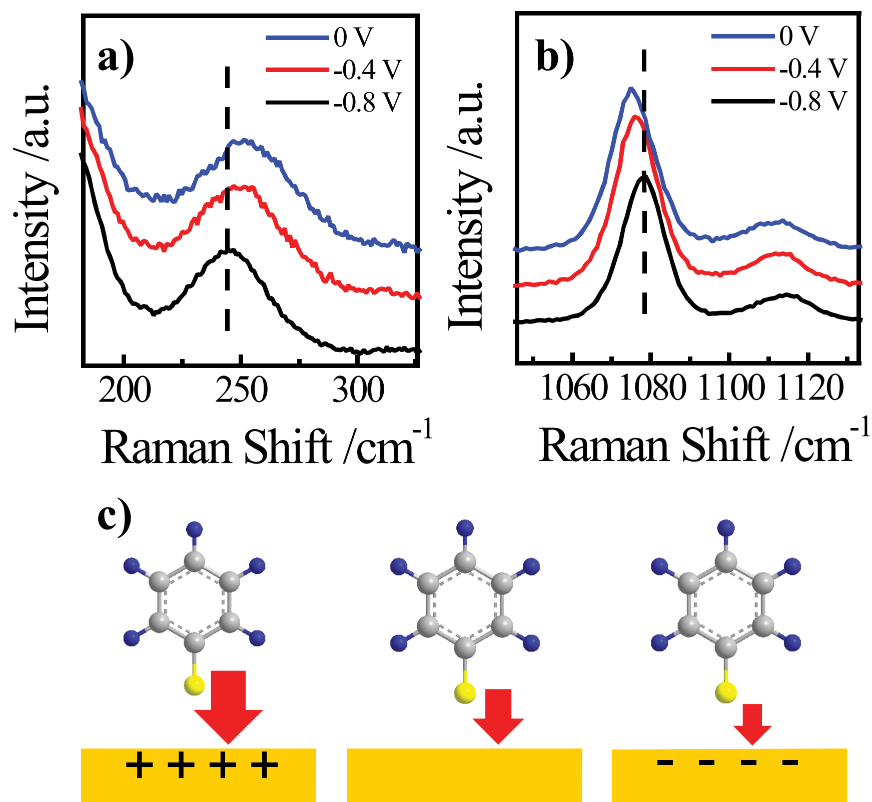

Figure 7.3. Potential dependence of the Raman vibrational modes of adsorbed benzenethiol at CdTe surface highlighting a) the surface vibration region and b) the molecular vibration region. c) Qualitative depiction of the ligand-to-metal charge transfer magnitude (red arrow) under different external biases.

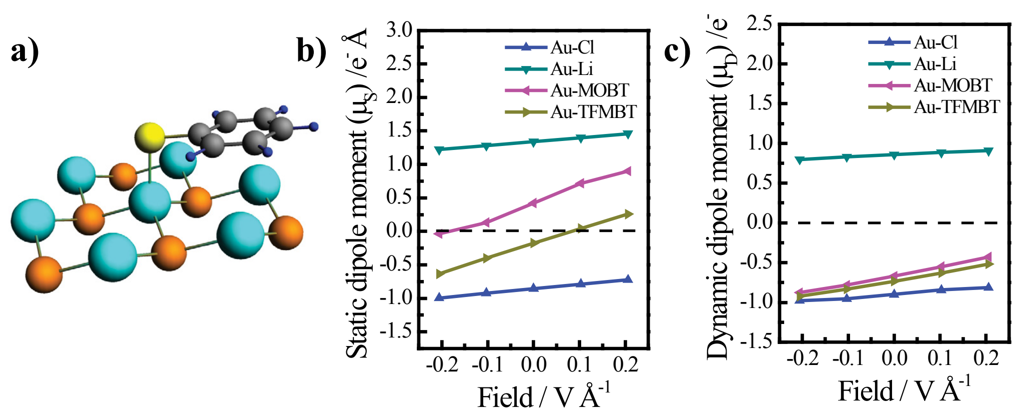

Figure 7.4. Schematic depiction of the Cd-VI-benzenethiol cluster model used for DFT calculation (Cd = blue, VI = orange). b) Computed static dipole moment and dynamic dipole moment for Cl, Li, 4-methoxybenzenethiol (MOBT) and 4-trifluoromethyl benzenethiol (TFMBT) on Au clusters.

increasing magnitude of charge separation at increasing bond distances results in the positive value of the dynamic dipole moment μ_d. The opposite behavior was observed in the case of anionic adsorbates like Cl, where both μ_s and μ_d values were negative. The same modeling principles were applied to more complex thiol derivatives, and their corresponding μ_s and μ_d values were calculated. As shown in Figures 7.4b and 7.4c, the 4-trifluoromethylbenzenethiol was clearly anionic in nature caused by the strong electron-withdrawing trifluoromethyl group in the molecular structure. Replacing the trifluoromethyl group with the electron-donating methoxy group completely altered the bonding behavior of the thiol. The surface bond now yielded a positive static dipole, indicating the adsorbate was partially positively charged. A negative dynamic dipole moment suggests a decrease in the degree of this positive dipole as the adsorbate moved away from the surface. Such behavior bears the signature of a ligand-to-metal charge transfer process in which the electron density is drawn towards the surface at bonding distance, yet retracts back to the adsorbate at increasing bonding distances due to the lack of effective orbital overlapping.

In summary, the preliminary results provide a glimpse of the application of *in-situ* SERS and DFT simulation for studying the interfacial interaction at the semiconductor surfaces. Future investigation should focus on the systematic study of the Stark effect on CdS, CdSe and CdTe surfaces with various thiol ligands in order to understand how the composition of the semiconductor as well as the nature of the substitution group on the thiol adsorbates affect the bonding character. Meanwhile, the modeling effort needs to transition from pure energetic computation to the simulation of actual Raman spectra for the aforementioned adsorbate-semiconductor pairs so as to understand the influence of applied electric field on the Raman vibrational modes. With this combined strategy of *in-situ* SERS and DFT simulation, a comprehensive picture of the interfacial interaction between the adsorbate and semiconductor can be obtained.

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