MICROELECTROMECHANICAL SYSTEMS FOR WIRELESS RADIO FRONT-ENDS AND INTEGRATED FREQUENCY REFERENCES

by

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To my family

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LIST OF ABBREVIATIONS

ADC	Analog-to-digital converter
ALN	Aluminum nitride
BAW	Bulk acoustic wave
BVD model	Butterworth van-Dyke model
BW	Bandwidth
C	Capacitance (capacitor)
CMOS	Complementary metal-oxide-semiconductor
Cr	Chromium
Cu	Copper
DC	Direct current
DRIE	Deep reactive-ion etching
DSP	Digital signal processor
EM	Electromagnetic
FBAR	Film bulk acoustic resonator
IF	Intermediate frequency
IPD	Integrated passive device
L	Inductance (inductor)
LBAR	Length extensional mode bulk acoustic resonator
MCXO	Micro-computer controlled crystal oscillator
MEMS	Microelectromechanical systems

MIM	Metal-insulator-metal
Mo	Molybdenum
NET	Noise equivalent temperature
OCXO	Ovenized quartz crystal oscillator
Op-amp	Operational amplifier
PFD	Phase frequency detector
PLL	Phase-locked loop
OTA	Operational transconductance amplifier
PVT	Process-voltage-temperature
Q	Quality factor
R	Resistance (resistor)
RF	Radio frequency
RTD	Resistive temperature detector
SAW	Surface acoustic wave
SEM	Scanning electron microscope
Si	Silicon
SiO_2	Silicon dioxide
TCE	Temperature coefficient of elasticity
TCF	Temperature coefficient of frequency
TED	Thermoelastic damping
UWB	Ultra-wide band
XeF_2	Xenon difluoride
XO	Quartz-crystal oscillator

ABSTRACT

Microelectromechanical Systems for Wireless Radio Front-Ends and Integrated Frequency References

by

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Chair: Mina Rais-Zadeh

Microelectromechanical systems (MEMS) have great potential in realizing chip-scale integrated devices for energy-efficient analog spectrum processing. This thesis presents the development of a new class of MEMS resonators and filters integrated with CMOS readout circuits for RF front-ends and integrated timing applications. Circuit-level innovations coupled with new device designs allowed for realizing integrated systems with improved performance compared to standalone devices reported in the literature.

The thesis is comprised of two major parts. The first part of the thesis is focused on developing integrated MEMS timing devices. Fused silica is explored as a new structural material for fabricating high-Q vibrating micromechanical resonators. A piezoelectric-on-silica MEMS resonator is demonstrated with a high Q of more than 20,000 and good electromechanical coupling. A low phase noise CMOS reference oscillator is implemented using the MEMS resonator as a mechanical frequency reference.

Temperature-stable operation of the MEMS oscillator is realized by ovenizing the platform using an integrated heater. In an alternative scheme, the intrinsic temperature sensitivity of MEMS resonators is utilized for temperature sensing, and active compensation for MEMS oscillators is realized by oven-control using a phase-locked loop (PLL). CMOS circuits are implemented for realizing the PLL-based low-power oven-control system. The active compensation technique realizes a MEMS oscillator with an overall frequency drift within +/- 4 ppm across -40 to 70 ℃, without the need for calibration. The CMOS PLL circuits for oven-control is demonstrated with near-zero phase noise invasion on the MEMS oscillators. The properties of PLL-based compensation for realizing ultra-stable MEMS frequency references are studied.

In the second part of the thesis, RF MEMS devices, including tunable capacitors, high-Q inductors, and ohmic switches, are fabricated using a surface micromachined integrated passive device (IPD) process. Using this process, an integrated ultra-wideband (UWB) filter has been demonstrated, showing low loss and a small form factor. To further address the issue of narrow in-band interferences in UWB communication, a tunable MEMS bandstop filter is integrated with the bandpass filter with more than an octave frequency tuning range. The bandstop filter can be optionally switched off by employing MEMS ohmic switches co-integrated on the same chip.

CHAPTER 1.

Introduction

1.1 Background

MEMS and microsystems with sensing, computing, and wireless communication capabilities have numerous applications and are ubiquitous in modern life. The need for low power, low cost, and small form-factor has stimulated large efforts in developing devices and circuits for these microsystems and user-end terminals. Advances in semiconductor technology will continue to offer more computation and storage capabilities with reduced power consumption. Moreover, having sensing and wireless connectivity features is more critical in emerging technologies such as the internet of things (IoTs). Such a technology direction is also described as the "More-than-Moore" trend according to the International Technology Roadmap for Semiconductors (ITRS) [1] (Figure 1.1). Besides the need for cramming more transistors into an integrated circuit chip for enhancing computing power (following Moore's Law), functional diversification demands new types of devices to be integrated, including RF/analog components, sensors/actuators, energy/power devices, *etc*.

The demand for more functionality already has significant impact on the hardware implementations of compact-size user-end terminals. A large number of sensors and

wireless devices are included in smart phones (Figure 1.2), imparting such small devices with numerous capabilities.

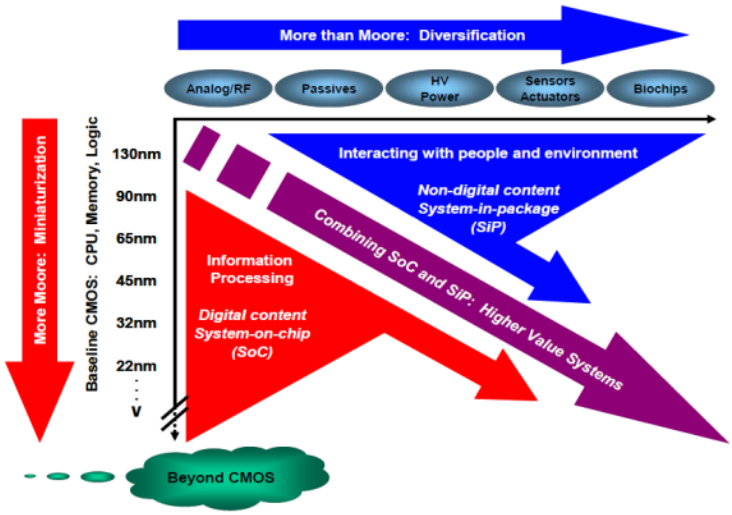


Figure 1.1. The future technology trend, indicating the need for functional diversification in the so called "More than Moore" era [1].

Figure 1.2. Diversified functions integrated in a typical user-end terminal, including wireless communications and sensors.

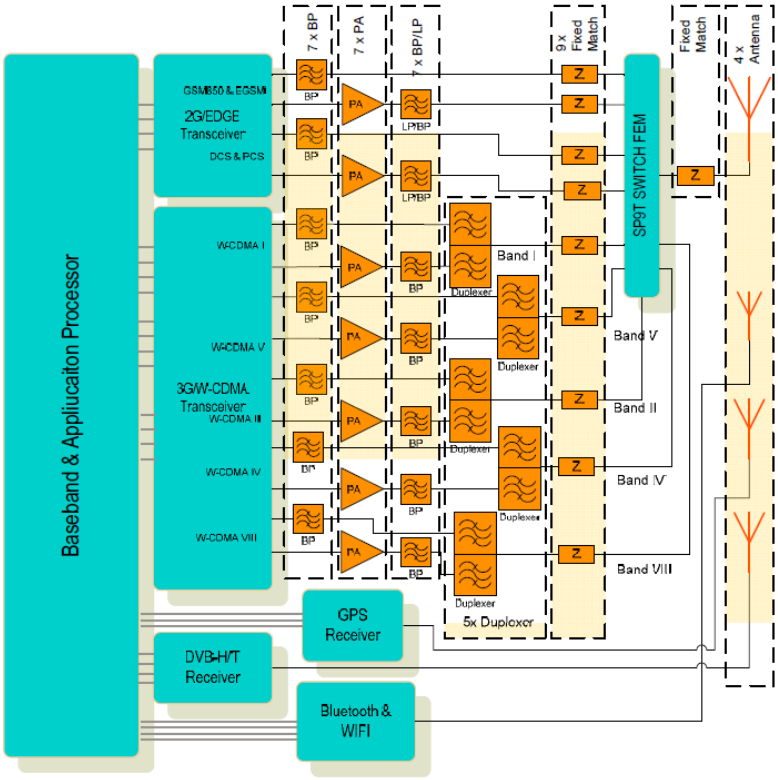


Figure 1.3. A universal transceiver used in cell phones (highlighted in the dash box is the use of off-chip components in a large number) [2].

Digging into wireless technology for example, the proliferation of wireless communication standards in the past few years has urged cellular transceivers to have increased hardware complexity in order to support different communication bands covering 800 MHz to 2,400 MHz (Figure 1.3). The design complexity cannot be solely solved by integrating more transistors on a silicon chip. A universal wireless transceiver requires more than 10 different filters or duplexers and several quartz crystal frequency references, which are still implemented using off-chip components. The passive components in a multiband cell phone occupy 65–80% of the circuit board area, with an RF loss of 3–6 dB between the silicon chip and the antenna(s) [3]. There is also a

growing interest in developing adaptive hardware for accommodating emerging standards having constrained area, power, and re-development time. The number of individual off-chip components used for various functionalities is expected to further increase.

The research community and industry have focused on resolving these challenges with innovative solutions. So far, the efforts in circuit-level innovations have achieved great progress by leveraging advanced signal processing and data conversion capabilities of the CMOS technology. Also, migrating off-chip passives, such as RF inductors, onto a CMOS die has been quite instrumental in realizing modern RF transceivers with a system-on-chip solution. However, there exist concerns regarding the size of passive devices, which consume a large area on the expensive CMOS die, as well as the limited performance on-chip RF passives offers. The performance of CMOS on-chip passive devices, including inductors and varactors, still falls short for realizing the majority of much needed functions such as filtering, timing, and low-loss power combining networks. The performance of such devices is mostly limited by the fundamental device physics using the current device technology. For example, the noise performance of an electrical oscillator is highly dependent on the Q of a reference resonator. Given a specific oscillator power budget, close-to-carrier phase noise is inversely proportional to Q^2 [4]. Therefore, the performance of the resonator sets a hard limit on the achievable figure-of-merit for an oscillator, and the achievable Q of the on-chip LC tank circuits are limited by their intrinsic material properties. In another example that concerns a wireless receiver implementation, the front-end filtering affects the architecture choice and the linearity requirement of the subsequent stages [5]. As a result, the availability of passive

filters may dictate the power consumption of the receiver circuits. Some emerging wireless systems are designed using digital signal processing to eliminate the use of passive components. Examples include a software defined radio (SDR) that relies on baseband digital signal processing to realize re-configurability [6]. However, such a SDR requires high-bit rate analog-to-digital converters (ADCs) along with a high-performance digital signal processor (DSP), which consumes excessive power. Instead, a large part of analog signal conditioning or spectrum processing can be done efficiently using high-performance passive devices, leading to drastic reduction in power consumption. It is obvious that passive devices, if come as discrete components, are hurdles to overcome in further miniaturization of analog/RF sub-systems. However, they are still widely adopted as essential components in modern systems because of the low performance of their on-chip alternatives. In seeking better solutions, the main focus of this dissertation is exploring the use of MEMS technology for analog spectrum processing, including filtering for the wireless spectrum as well as using MEMS as frequency references.

1.2 MEMS for Analog Spectrum Processing

1.2.1 Integrated MEMS as Replacement for Low-Performance Passive Devices

To eliminate the use of conventional bulky passive devices, a feasible technology direction is to develop miniature replacement devices that can be integrated on a chip. Such an idea has been successfully realized in the example of integrated passive device (IPD) technology [7], which resolves the difficulties of fabricating high-performance RF passive devices on a CMOS chip. IPD allows a complex analog/RF system to be implemented in the form of multi-chip modules or system-in-package (SiP) [8], where

passive devices, including high-Q RF inductors (Q > 60 at GHz frequencies), high-density thin-film capacitors, and high-precision resistors, are integrated on a carrier substrate (or an interposer). The adoption of IPD significantly reduces the footprint of a RF sub-system compared to the case where conventional discrete components are used.

Mechanical resonators, as another major type of passives, are widely used as frequency references and mechanical filters. The concept of IPD can be expanded if MEMS technology is adopted to integrate micro-mechanical resonators on the same interposer chip. MEMS resonators rely on mechanical vibration of micro-structures and exhibit much higher Qs than electromagnetic (EM) resonators at the same frequency range. The high-Q and precise frequency provided by MEMS resonators make them potential replacements for off-chip quartz crystals. Various types of MEMS resonators and oscillators have been developed as integrated frequency references in the past [9], and several MEMS oscillators have demonstrated good performance as to satisfy demanding wireless specifications [10]-[11]. The excellent electromechanical energy coupling demonstrated in some miniature MEMS resonators also proves potential in realizing integrated IF/RF filters [12]-[14] to replace off-chip surface acoustic wave (SAW) filters for spectrum processing.

A big challenge in implementing high-Q MEMS resonators is to ensure they have a stable frequency over environmental changes. For a MEMS resonator, the product of resonance frequency and quality factor (f×Q) is typically adopted as a figure-of-merit (FOM). State-of-the-art MEMS resonators are demonstrated with a high f×Q (f×Q > 10^{12}-10^{13}) [9]. If these resonators are used for precision frequency generation or narrowband

RF channel filtering, the intrinsic frequency drift of the resonators has detrimental effects due a narrow fractional bandwidth tied to a high device f×Q. Various factors that cause frequency instability can be found in a typical MEMS-based oscillator, as sketched in Figure 1.4. Sources of frequency drift can be categorized into deterministic drift and random noise effects.

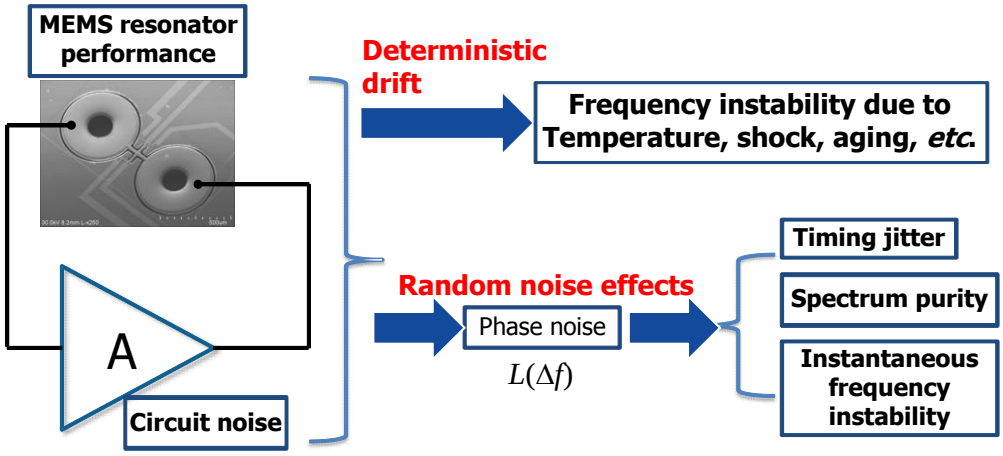


Figure 1.4. Sources of frequency instability in a MEMS reference oscillator.

Deterministic drift in an electrical oscillator is due to the sensitivity of device characteristics to working conditions. Temperature-induced frequency drift is typically a dominant frequency error in MEMS resonators and oscillators. As a common structural material for fabricating MEMS resonators, silicon shows a large linear temperature coefficient of frequency (TCF) of approximately -30 ppm/K when in mechanical resonance. The TCF of a resonator directly determines the temperature stability of a MEMS oscillator, and a prohibitively large frequency drift can occur over a typical working temperature range of -40 °C to 85 °C. Other environmental effects, such as

acceleration/shock, humidity, and radiation, also cause undesirable frequency drift. Further, the environmental effects are combined with the intrinsic material properties of a MEMS resonator to cause device aging. The environmental effects and device aging are relatively slow varying processes. These slow variations affect the mid-term and long-term frequency stability, which is a critical concern in implementing MEMS-based time keeping devices. Frequency stability of a MEMS oscillator is also affected by electrical conditions. Frequency drift of a MEMS oscillator can also be induced by changes in the supply voltage (supply pulling), oscillator loading conditions (loading pulling), *etc.* All the deterministic drift mechanisms cannot be avoided, but they can be characterized and mitigated by incorporating proper device, packaging, and circuit designs.

Another type of frequency drift comes from noise in the devices and circuits (Figure 1.4). The noise-induced frequency drift needs to be treated using statistical methods, and the frequency drift involves both slow varying processes (1/f noise) and fast variations. First, noise-induced instability affects the purity of an oscillator output spectrum. The spectrum purity can be represented as phase noise power density relative to the carrier power, *i.e.*, phase noise (L(Δf) in dBc/Hz). For an electrical oscillator, which is referenced to a high-*Q* resonator, a simplified expression for the phase noise is [4]

$$L(\Delta f) = 10\log\left\{\frac{k_b TF}{P_{sig}}\left[\frac{1}{4Q_L^{\,2}}\left(\frac{f_0}{\Delta f}\right)^2 + 1\right]\right\}, \tag{1.1}$$

where F, k_b, T, P_{sig}, Q_L, and Δf are noise factor, Boltzman's constant, temperature (in Kelvin), signal power, loaded *Q* of the resonator, and offset frequency from carrier,

respectively. For a wireless system, the noise performance of a reference oscillator highly affects the phase noise of a frequency synthesizer. Typically, a wireless system specifies the maximum allowed phase noise at some critical offset frequencies from the RF carrier frequency. In other applications, noise-induced instability is also viewed as timing jitter (or phase jitter) in the clock output signal from an oscillator. Timing jitter is a measure of uncertainty of clock transitions, and it directly affects the performance of sampling data systems or high-speed serial links. The statistical variance of timing jitter can be obtained by integrating the phase noise over the bandwidth of interest. Phase noise can be also studied in the frequency domain. L(Δf) in Equation (1.1) can be multiplied by the Fourier frequency (f^2) to get the frequency noise spectrum density. Then, the statistical variance of frequency instability can be obtained by integrating frequency noise spectrum density over the bandwidth of interest. It is worth noting from Equation (1.1) that the phase noise performance of a reference oscillator is highly dependent on the *Q* of the resonator. Therefore, the use of a high-*Q* resonator in an electrical oscillator design is extremely beneficial for reducing noise-induced frequency instabilities.

MEMS resonators offer *Q*s that are orders of magnitude higher than their EM counterparts. In addition, the working frequencies of MEMS resonators span from kHz range to GHz range, with physical sizes that are in the order or few 10's of micrometer [9]. Therefore, there are several applications MEMS resonators can be used for, the most immediate being low phase noise timing devices and frequency synthesizers.

Although micro-mechanical resonators exhibit high *Q*s, these devices cannot be tuned in a large frequency range to enable multi-band/multi-standard operation. In order to

enable frequency tuning functions, miniature MEMS actuators can be integrated. These MEMS actuators are commonly referred to as RF MEMS devices [3]. Tunable RF MEMS, including MEMS capacitors and ohmic switches, can be used along with other IPDs to realize tunable filters, reconfigurable antennas, phase shifters, and adaptive matching networks. MEMS tunable filters have been demonstrated, showing wide frequency coverage, low loss, and excellent linearity [3], [15]. These filters are potential replacements for a large number of conventional fixed-frequency filters, which is instrumental in realizing ultra-compact and re-configurable RF transceivers. A further progress is to combine the benefits of tunable RF MEMS and high-Q micromechanical resonators by fabricating these devices on the same chip, simultaneously, using micromachining processes [16].

1.2.2 New Architectures Enabled by MEMS Resonators

The unique properties of MEMS resonators have been further exploited to enable new designs, which are beyond the scope of conventional circuit implementations. As bulk acoustic wave (BAW) MEMS resonators can be designed in GHz frequencies, a BAW MEMS resonator with good frequency stability can be incorporated in a frequency reference to directly generate a stable RF carrier frequency without the need for frequency up-conversion. This eliminates the need for a PLL as a RF frequency synthesizer. A wireless synthesizer composed of a MEMS-based digital controlled oscillator (DCO) achieves much faster startup time than a conventional PLL (Figure 1.5). Such a property is highly desirable in implementing ultra-low power wake-up radios. Also, due to a high f×Q inherent in MEMS, excellent phase noise performance can be

obtained with a low-power oscillator design. Reported works have demonstrated MEMS-based low-power radio transceivers with frequency-shift keying (FSK) modulation [17] and on-off keying (OOK) modulation [18]. Some other innovative implementations include the use of a super-regenerative MEMS oscillator to directly sample at RF for a low-power receiver implementation [18].

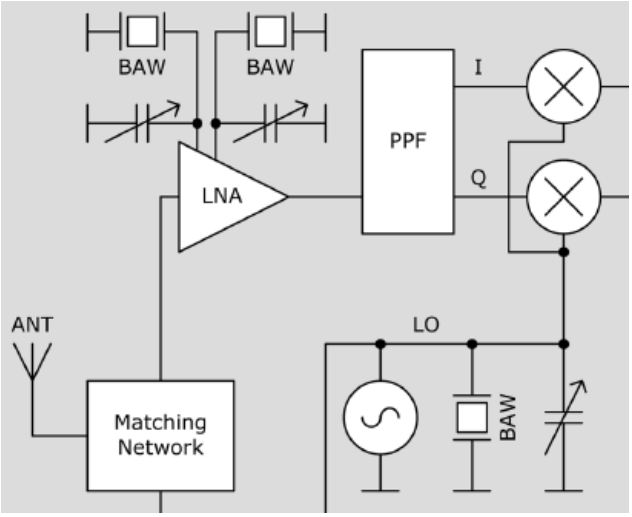


Figure 1.5. A PLL-less frequency synthesizer using a MEMS-based digital-controlled oscillator for wake-up radios [17].

1.3 Research Objectives

Targeting frequency references and RF filtering applications, the objective of this thesis is to develop MEMS devices and MEMS-enabled circuits based on devices integrated in a heterogeneous scheme. First, using an aluminum nitride (AlN) thin-film process, piezoelectric-on-substrate MEMS resonators are developed. High-aspect-ratio deep reactive-ion etching (DRIE) is used to fabricate micromechanical resonators which utilize the high quality substrate material. Both fused silica and high resistivity silicon

exhibit excellent mechanical properties and low acoustic loss. Combining such materials with low intrinsic energy dissipation and the piezoelectric property of AlN for electromechanical transduction, high-performance piezoelectric-on-substrate MEMS resonators are developed as integrated frequency reference devices. Design of low phase noise reference oscillators is also studied based on the fabricated MEMS resonators. In order to improve the frequency stability of MEMS oscillators, TCF-compensation techniques are investigated. The MEMS resonators in this thesis are integrated in thermally-isolated platforms to improve immunity to external temperature variations. The MEMS platforms are co-fabricated with the MEMS devices, allowing deep fusion of multiple devices with temperature-stable operation. Material aspects and device designs are studied to realize both passive TCF-compensation on MEMS resonators and micro-structures with high thermal isolation. The MEMS platforms with good thermal isolation property enable low power ovenization as an effective active compensation method. Ovenized MEMS is realized by temperature *servo*-control using temperature sensors and built-in heaters on the MEMS platforms.

Considering electrical properties of the substrate materials used for fabricating MEMS resonators, fused silica (*i.e.*, high purity amorphous silicon dioxide) is also an ideal carrier substrate for RF applications due to its excellent electrical insulation property and low loss tangent (< 0.0001 at 1 GHz). High-resistivity silicon, as a common type of RF IPD substrate material, also exhibits acceptable RF loss in many applications. Using the same substrate as a carrier substrate (or an interposer), passive components, including high precision resistors, high-*Q* inductors, metal-insulator-metal (MIM)

capacitor, and other microwave components, can be fabricated using standard thin-film metallization and dielectric processes. Further, the adoption of surface micromachining process introduces a sacrificial layer that allows the formation of suspended mechanical actuators for building RF MEMS tunable capacitors and switches on-chip. The RF MEMS devices are used to implement low-loss tunable filters.

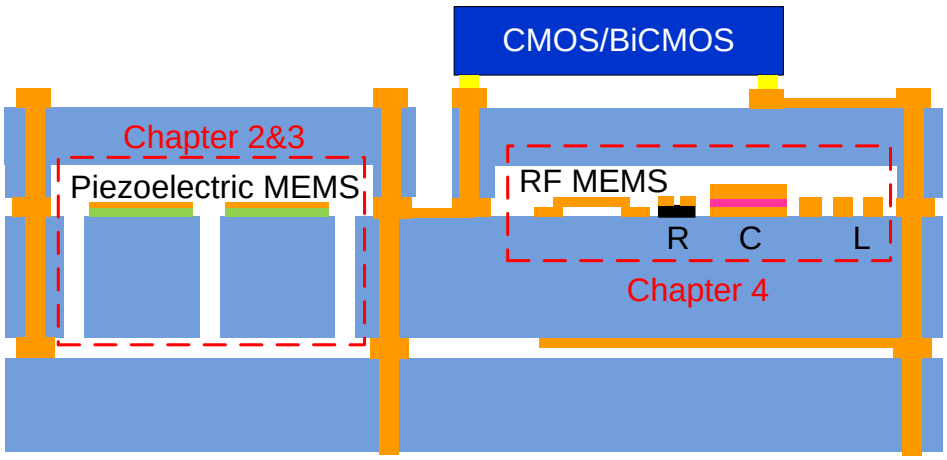


Figure 1.6. The concept of multi-device platform for integrating high-performance passives, MEMS, and ICs in a chip-scale.

The general view of the proposed heterogeneous platform is sketched in Figure 1.6. The work in this thesis covers the development a new class of piezoelectric MEMS resonators and tunable RF MEMS devices in the platform. The process compatibility between the resonators and the tunable RF MEMS devices potentially enables co-integration of them in the same heterogeneous platform for enhancing system functionalities. For delivering a packaged multi-device fusion platform, wafer-bonding can be further adopted for hermetic sealing of MEMS devices in the platform, and high-

aspect-ratio substrate micromachining also allows the formation of through-substrate-vias (TSVs) to realize low-loss vertical interconnects. Finally, active CMOS circuit chips can be integrated by die stacking with the MEMS platform. The push towards co-integration of various types of emerging MEMS devices, as proposed in this work, has clear benefits. If MEMS devices are developed as stand-alone components, the devices only serve as replacement components and in these cases still require further packaging and assembly before they can be integrated with other components, which in large part loose attractive features of integrated MEMS. From a system design perspective, it is highly desirable if various types of emerging MEMS devices are accessible to designers as chip-scale integrated components. As discussed in Section 1.22, innovations in new circuit techniques, system architectures, and applications entail the use of different types of devices in a concurrent fashion or even in small to medium-scale integrated solutions. Therefore, a unified fabrication, integration, and packaging technology to integrate various types of devices are extremely beneficial.

1.4 Organization of the Dissertation

In Chapter 1, the benefits of integrating MEMS devices for realizing new analog functionalities have been presented. The objective of research is introduced. In Chapter 2, fused silica is investigated for realizing high-performance micromechanical resonators. Using fused silica MEMS, a CMOS reference oscillator is developed. The silica MEMS resonator is further integrated in an ovenized platform for temperature-stable operation. In Chapter 3, a new temperature sensing and active compensation scheme is presented by

utilizing the intrinsic temperature sensitivity of frequency of MEMS on a miniature thermal-isolation platform. The temperature *servo*-control system for ovenized MEMS is realized using a custom-designed CMOS PLL circuit. In Chapter 4, a micromachining technology for fabricating high-performance RF passives and tunable RF MEMS devices on-chip is introduced. Low-loss and miniaturized tunable/switchable RF filters are implemented based on the RF MEMS devices. In Chapter 6, the presented research work is summarized and future research directions are discussed.

CHAPTER 2.

Fused Silica MEMS Frequency References

Due to the fact that acoustic waves in solids have much smaller wavelength than electromagnetic waves traveling in common media, mechanical resonators can be made much smaller compared to electromagnetic resonators at similar standing-wave frequencies. MEMS technology enables fabrication of micromechanical resonators with very low energy dissipation. Compared to conventional electrical resonators such as LC tanks or distributed electromagnetic resonators, vibrating MEMS resonators exhibit much higher *Q*s (Q > 1,000 - 10,000). Also, the working frequency of MEMS resonators can be defined precisely by micromachined structures on a chip, and resonators with multiple working frequencies can be integrated. In this chapter, fused silica is investigated for realizing micromechanical resonators. The silica MEMS resonator implementation is targeted for high Q and excellent electromechanical energy coupling, enabling the potential use of the devices in low noise timing references. The temperature-induced frequency drift in fused silica MEMS is also addressed using low-power ovenization, which utilizes the low thermal conductivity of fused silica material. The ovenization is applied to a device-fusion platform, where multiple fused silica sensors and resonators can be integrated. Such a platform could be used for implementing an all-silica chip-scale timing and inertial measurement unit (TIMU) [19].

2.1 Fused Silica MEMS Resonator

Over the past decade, MEMS resonators are developed as promising replacements for bulky quartz crystal frequency references. So far, most research has been focused on developing silicon MEMS resonators [10], [11], [20], [21] or thin-film AlN resonators [12], [22]. In this work, material properties and design aspects of fused silica MEMS are investigated for realizing high-performance integrated MEMS frequency references. In terms of material properties, fused silica has low intrinsic phonon-phonon dissipation. A high $f \times Q$ product has been predicted for quartz [23], which has very similar material constants to fused silica (except for the fact that quartz is piezoelectric). Due to very low thermal conductivity and small linear thermal expansion coefficient, mechanical resonators made using pure fused silica have low thermoelastic damping (TED) [24]. Fused silica mechanical resonators with Qs exceeding 1 million have been demonstrated as early as 1970s [24]. In addition, the excellent thermal isolation property of fused silica makes it ideal as both the device and the packaging material, enabling all-silica packaged MEMS that can be ovenized at low power. Towards the goal of realizing a silica-based chip-scale timing and inertial measurement unit (TIMU), high-performance silica MEMS resonators [25], a silica packaging process, and multi-layer vertically stacked fused silica microsystems [19] have been demonstrated.

On the flip side, one of the limitations of silica MEMS is the relatively immature micromachining technique of fused silica material. Dry etching of fused silica is more challenging as compared to conventional silicon MEMS. In this work, an advanced silica DRIE technique [26], [27] is utilized to implement high-performance MEMS resonators.

To overcome weak signal transduction between the mechanical and electrical domain inherent in capacitively actuated resonators, a piezoelectric thin-film layer on top of bulk fused silica is used to obtain strong electromechanical coupling. The energy loss in a resonator with composite piezoelectric-on-silica materials is studied, revealing the upper bound on the achievable resonator *Q*. Resonator design techniques are investigated with reduced anchor loss given the limitations in defining small feature sizes and high-aspect-ratio (ratio of height over width) micro-structures in fused silica. The fused silica MEMS resonator demonstrated in this work exhibit a high *Q*, low motional impedance, and good power handling capability, making it a good candidate for a miniature frequency reference.

2.1.1 Piezoelectric-on-Substrate Resonator Fabrication Process

Micromachining of glass-type materials, including Pyrex glass, fused silica, and quartz, conventionally has relied on wet etching [28], [29] or serial machining processes [30]-[32]. These machining techniques have limited resolution or low through-put, making wide adoption of glass-MEMS devices difficult. In this work, we utilize DRIE of fused silica [26] to fabricate high-performance micromechanical resonators in batch mode. The silica DRIE process allows machining of high-aspect-ratio mechanical structures. Therefore, a large choice of vibration modes can be adopted in the resonator design. Also, a piezoelectric thin-film layer is added on top of bulk fused silica to enable strong electro-mechanical energy coupling. The fabrication process flow of the piezoelectric-on-silica resonator is sketched in Figure 2.1. The process starts with a 4" Corning 7980 high-purity fused silica wafer. A 1000 Å thick Molybdenum (Mo) layer is

deposited and patterned as the bottom electrode. Then, a 1 μm thick AlN layer is sputtered as the piezoelectric material. The top electrode is formed by evaporation of a Chrome/Gold (Cr/Au: 100Å/1000Å) layer. The fused silica wafer is subsequently flipped and attached to a carrier for wafer thinning. Afterwards, backside DRIE is applied to form high-aspect ratio trenches and define the resonator device geometry. The devices are detached from the carrier by dissolving the temporary bond in solvent in a final release step. A scanning electron microscope (SEM) image of a fabricated fused silica MEMS resonator is shown in Figure 2.2. In this work, 60 μm-thick fused silica is used for the device layer.

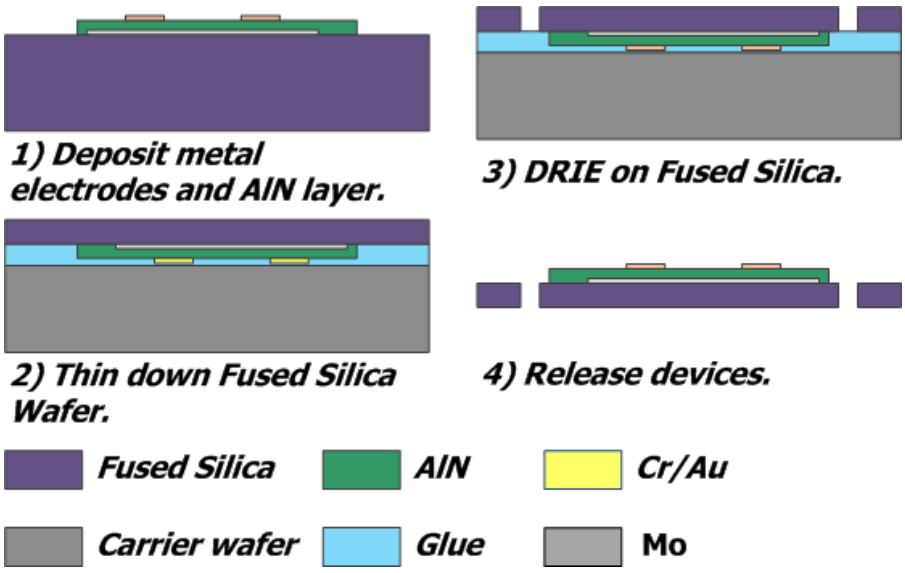


Figure 2.1. Fabrication process flow of the fused-silica resonators.

Using fused silica DRIE process, limitations in trench aspect-ratio still impose design constraints. With the chosen device layer thickness, the minimum DRIE trench width is 20 μm, indicating an achievable aspect-ratio of about 4:1 in the DRIE trenches. The

smallest structure width is 15 μm. A cross-section image of a fused silica structure after DRIE is shown in Figure 2.3. It can be observed that the DRIE trenches have slight trapezoid shape and trench widening by 1 to 2 μm. The DRIE trench also exhibits significant sidewall roughness.

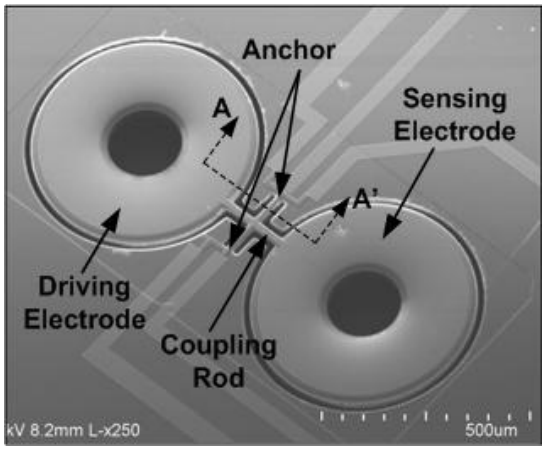


Figure 2.2. A SEM image of a fabricated fused silica MEMS resonator.

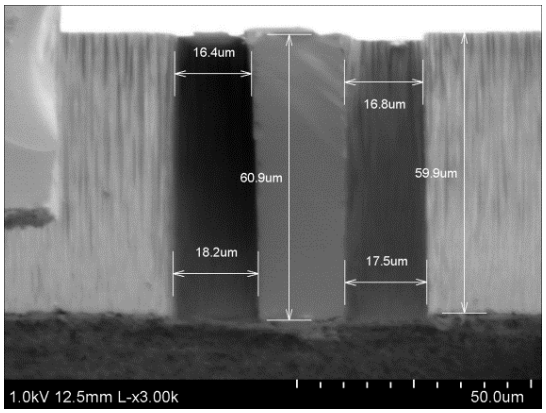


Figure 2.3. A cross-section view of the fused silica DRIE trench profile.

2.1.2 Piezoelectric-on-silica Resonators Design

In high-*Q* MEMS resonator designs, placing supporting tethers in nodal points [33], [34] or using soft tethers [35] prove effective in reducing anchor loss. However, a large

minimum feature width (15 μm) in the fused silica DRIE process makes low-loss anchor design challenging. The non-ideal sidewall profile, along with other structural imperfections, such as thickness non-uniformity induced from backside thinning, also introduce difficulties in designing low-loss micro-resonators using fused silica material, especially for vibration modes which are highly dependent on thickness. Surface roughness is also known to cause energy dissipation in vibrating mechanical devices [36]. Although fused silica is known to have low intrinsic loss, various limitations and imperfections in its micromachining process with the current technology introduce challenges in implementing a high-performance resonator.

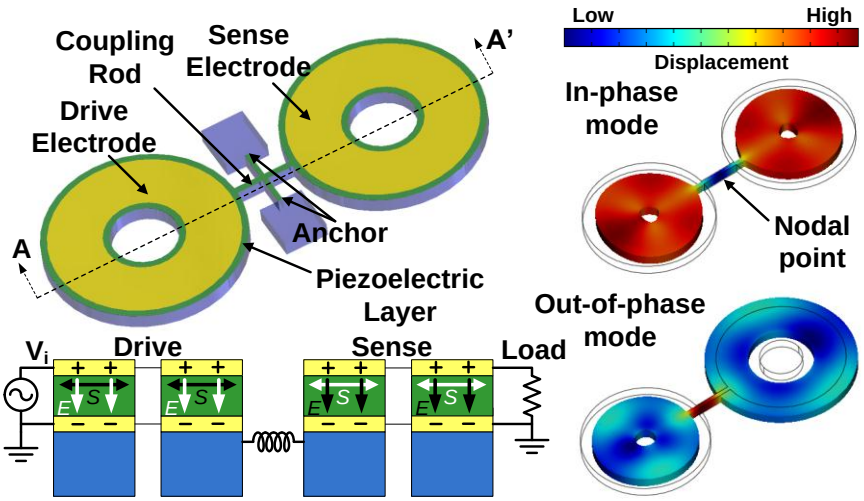


Figure 2.4. 3-D model of the piezoelectric-on-silica MEMS resonator design; diagram of piezoelectric actuation; and mode shapes of the in-phase and out-of-plane coupled radial extensional modes.

For a practical design, it is beneficial to pick a vibration mode that is relatively tolerant to fabrication imperfections. Among various vibration modes, BAW resonators have high energy density [37]. Such property helps improve the ratio of energy storage to

energy loss [35], thereby, achieving high quality factors given various loss mechanisms. If an in-plane BAW resonance mode is used, the resonance frequency can be defined using lithographic patterns, and it is relatively insensitive to thickness variation of the device. Successful examples of BAW resonator designs include in-plane extensional mode resonators [11], [21], showing high $f \times Q$ products. As for piezoelectric-on-substrate MEMS resonators, in-plane extensional modes exhibit excellent electromechanical coupling, as a strong strain density on the resonator surface facilitates piezoelectric transduction with a thin-film piezoelectric capping layer [39]. In this work, a fused silica resonator is designed by utilizing in-plane radial extensional vibration of a ring structure, having the merits of BAW resonators. As sketched in Figure 2.4, the resonator is comprised of two vibrating rings that are connected through a center coupling beam. The coupling beam is attached to the edge of the ring, which is a high velocity point in radial extensional vibration. This configuration creates a strong acoustic energy coupling between the two vibrating rings. Such strong coupling splits the resonance frequencies of the in-phase and out-of-phase modes apart. Two long anchor beams are attached to the center of the coupling beam. For the in-phase mode, the center of the coupling beam is a *pseudo*-nodal point. Such a structure mitigates loss of energy into the anchors or the substrate. For the out-of-phase mode, the coupling beam is moving, and the anchor beams have flexure motion. Long and flexible anchor beams ensure that the energy lost in the anchor is significantly less than the energy stored in extensional vibration of the rings, thereby still achieving high anchor Q. Even though the minimum feature size imposed by fused silica DRIE is as large as 15 μm for the chosen device thickness, the supporting

tether design avoids direct anchor attachment to the vibrating rings to reduce the anchor loss. The two-ring vibrating structure also doubles total energy storage compared to a single vibrating ring design.

The natural frequency of the radial extensional ring resonator operated in the 1st order mode can be calculated using [40]

$$f_0 \approx \frac{1}{2\pi\sqrt{R_{in}R_{out}}}\sqrt{\frac{E_{silica}}{\rho_{silica}}}, \tag{2.1}$$

where R_{in} and R_{out} are the inner and outer radii of the ring, respectively; E_{silica} is the Young's modulus, and ρ_{silica} is the mass density of fused silica. With a larger R_{out}/R_{in}, significant circumferential stresses add to the stiffness and the natural frequency shifts higher [40]. The mechanical coupling in the two-ring design also changes the effective Young's modulus (E_{eff}) and effective mass (ρ_{eff}) of the in-phase and out-of-phase modes, resulting in two different resonance frequencies. The physical dimensions used for the resonator design with ~5 MHz natural frequency are denoted in Figure 2.5, with a cross-section view showing the thickness of each material in the stack.

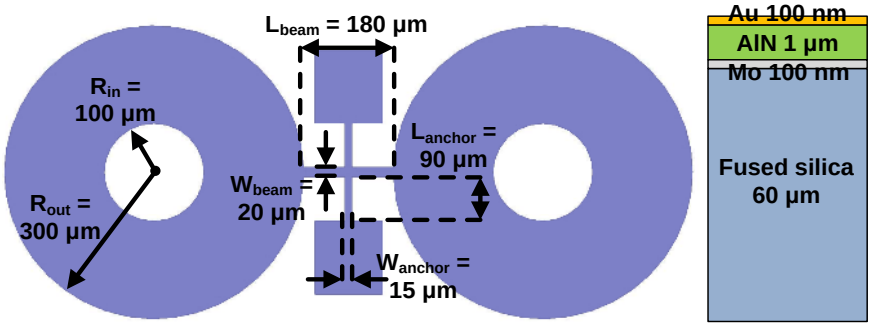


Figure 2.5. Dimensions and material stacks used in the silica resonator design.

The principle of piezoelectric transduction is depicted in Figure 2.4, the drive and sense electrodes are placed on the top surfaces of the rings. When an AC signal is applied across the piezoelectric layer on the drive electrode, mechanical strain (S) is induced through cross-axis piezoelectric coupling coefficient (d_{31}). Near the mechanical resonance frequency, radial extensional vibration can be effectively excited. The strain in the sense ring induces charge on the piezoelectric layer through reverse piezoelectric effect, and the charge is picked up by the sense electrode. In normal operation, the bottom electrode is connected to ground for establishing a vertical electrical field with drive and sense electrodes (Figure 2.4). The rings in radial extensional vibration experience a large in-plane volumetric change. Therefore, the top surfaces of two vibrating rings show large strain density, which facilitates piezoelectric transduction through d_{31} of an AlN thin-film deposited on top of silica.

Intrinsic sources of energy dissipation also limit the maximum achievable Q of fused silica resonators. TED and phonon-phonon loss have been studied in several types of BAW resonators [41]. It was found that although the ring resonator has large volumetric change in the radial extensional mode, the volumetric strain is uniform across the resonator body and to the first order, the gradient of strain energy density across the thickness and radial directions is near zero [41]. Therefore, the temperature gradient is insignificant across the resonator body, and a single-material ring resonator in radial extensional vibration is expected to have low TED loss. Further, low thermal conductivity of fused silica material results in small TED. Using COMSOL FEM simulation to study TED [42], the energy loss due to heat flow on the resonator body

during vibration is calculated. A pure fused silica resonator in radial extensional mode is designed with an extremely high Q_{TED} of 9.41×10^{10}. However, with an AlN material stack on top of silica, the simulated Q_{TED} drops to ~6×10^{5} (Figure 2.6). The temperature profile of a piezoelectric-on-silica resonator in radial external vibration is obtained from simulation and plotted in Figure 2.6. For the designed ring geometry, there exists an obvious temperature gradient along the radial direction. More importantly, the mismatch of material properties between fused silica and AlN induces a large temperature gradient between the silica and AlN layers (Figure 2.6), implying addition thermal modes near the interface that cause energy loss. The materials constants used for TED simulation are summarized in Table 2.1. The large mismatch of material constants between fused silica and AlN creates stress jump at the interface, which in turn results in considerable interface loss [43]. Design techniques such as patterning the piezoelectric layer [44] or using an alternative piezoelectric material along with fused silica need to be further investigated to further reduce interface losses.

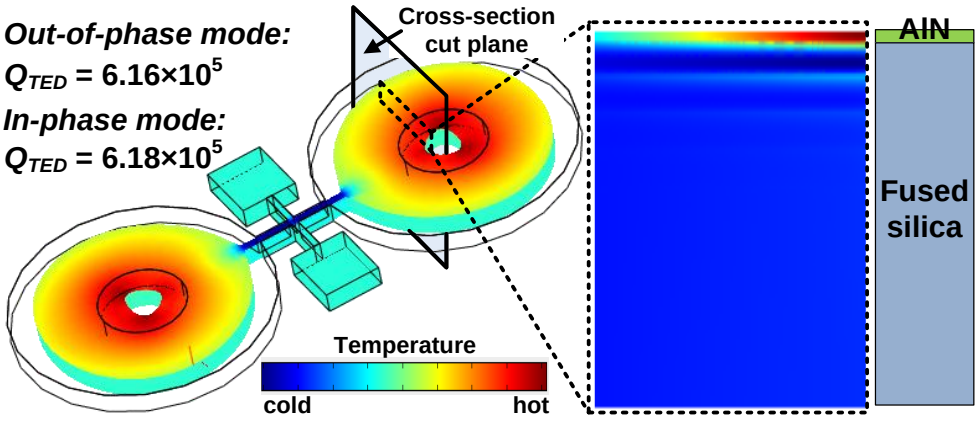


Figure 2.6. Simulated temperature distribution of the radial extensional mode with cross-section view showing temperature gradient between AlN and fused silica device layer.

Table 2.1. Material constants used for TED simulations.

	Fused Silica	AlN
Young's Modulus (GPa)	72.7	309
Poisson's Ratio	0.16	0.287
Mass density (kg m^{-3})	2201	3260
Thermal expansion coefficient (K^{-1})	0.57×10^{-6}	4.2×10^{-6}
Thermal conductivity (W m^{-1} K^{-1})	1.3	60
Specific heat capacity (J kg^{-1} K^{-1})	703	600

The anchor loss of the piezoelectric-on-silica resonator is also studied using COMSOL FEM by employing perfect matched layer (PML) boundary condition. Thanks to the structural design that mitigates anchor loss, the simulated Q due to anchor loss (Q_{anchor}) reaches 5.6×10^5 and 1.2×10^6 for the out-of-phase and the in-phase couple modes, respectively. For the fabricated resonator, additional loss mechanisms are more difficult to model, including the surface loss, the loss due to asymmetrical structures, and non-ideal sidewall profiles. These additional losses are still believed to limit the performance of the fabricated resonators, as will be presented in the next section.

2.1.3 Resonator Results and Characterization

2.1.3.1 Resonator Frequency Response

The *S*-parameter response of a fabricated piezoelectric-on-silica resonator is measured using an Agilent E5061b vector network analyzer (VNA) in a vacuum chamber with pressure levels below 1 mTorr. The radial extensional vibration modes are captured in the *S*-parameter response. As shown in Figure 2.7, twin peaks are observed near 4.9 MHz, which is in accordance with a mechanically coupled two-resonator system. The

resonance peak at 4.88 MHz corresponds to an out-of-phase vibration, while the peak at higher frequency (4.98 MHz) is due to an in-phase vibration. The piezoelectric layer (AlN) provides a strong electromechanical coupling for the designed vibration modes, and a low insertion loss (IL) is obtained. The unloaded *Q*s of two extensional vibration modes and their motional impedances are further extracted in Figure 2.7.

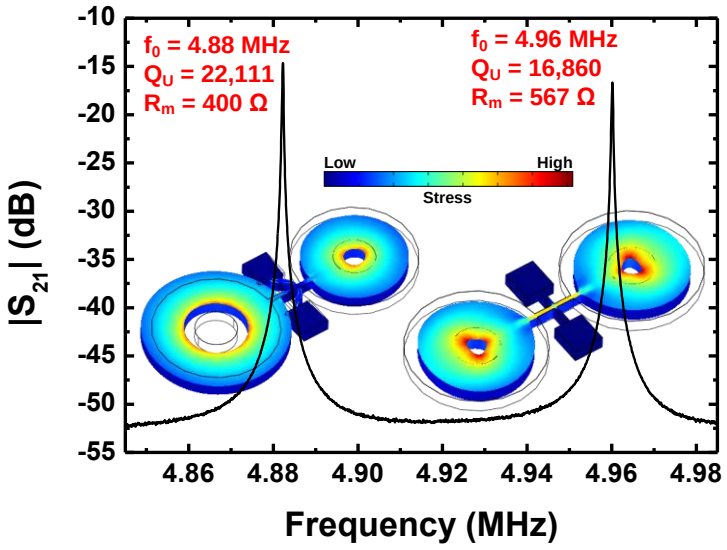


Figure 2.7. S-parameter responses of the in-phase and out-of-phase coupled radial extensional modes near 4.9 MHz (with mode shapes, *Q*, and motional impedance).

The fabricated fused silica resonator also shows other distinctive peaks. A coupled in-plane shear mode is captured in Figure 2.8. This mode has a measured 3-dB *Q* of 46,203 at 2.9 MHz. However, the insertion loss of the shear mode is significantly higher. The shear mode is more difficult to be effectively transduced with cross-axis piezoelectric coupling coefficient (d_{31}) of AlN layer as compared to the radial extensional mode. Another high-frequency second-order radial-extensional mode is captured at 16.4 MHz with a measured 3-dB *Q* of ~ 3,325, as shown in Figure 2.9.

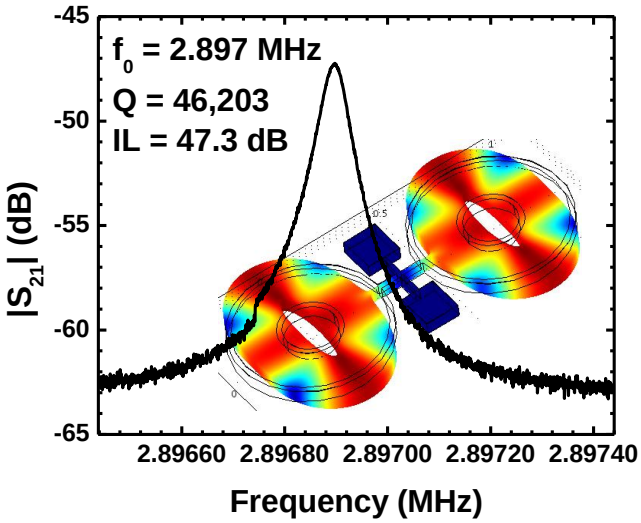


Figure 2.8. S-parameter response of the in-plane shear mode at 2.9 MHz.

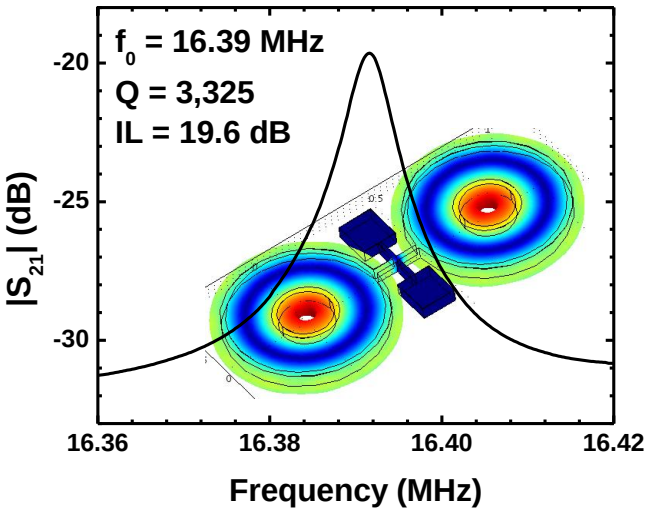


Figure 2.9. S-parameter response of the in-plane second-order radial-extensional mode at 16.4 MHz.

If the Q of a MEMS resonator is extracted directly from 3 dB fractional bandwidth of the measured transmission responses, $|S_{21}|$, the Q value incorporates loading effects from the VNA 50 Ω port impedances as well as the loss from electrical parasitics. The

unloaded Q (Q_U), *i.e.* Q of the mechanical vibration mode, can be further extracted after de-embedding the loading effects. As sketched in Figure 2.10, the device under measurement can be expressed by a two-port Y-parameter matrix, [$\mathbf{Y_{DUT}}$]. The [$\mathbf{Y_{DUT}}$] incorporates a network [$\mathbf{Y_{res}}$], which accounts for the response of mechanical vibration near resonance using a simplified Butterworth-Van Dyke (BVD) model, and a network [$\mathbf{Y_{par}}$] which accounts for electrical parasitics. The effect of electrical parasitic network appears as a feedthrough floor in the $|S_{21}|$ response, as shown in Figure 2.10. The parameters in [$\mathbf{Y_{par}}$] can be obtained by fitting the measured wideband S-parameter response of the device to the parasitic circuit model in Figure 2.10. The fitted parasitic model removes sharp mechanical resonance peaks, and [$\mathbf{Y_{par}}$] only incorporates admittances Y_f, Y_{sub1}, and Y_{sub2}. Y_f accounts for the electrical feedthrough effect, including a feedthrough capacitance (C_f) and conductance (G_f). The feedthrough components can be extracted from Y_{12} element in the [$\mathbf{Y_{par}}$] matrix

$$Y_f(\omega) = -Y_{12}(\omega) = G_f + j\omega C_f \tag{2.2}$$

Y_{sub1} and Y_{sub2} in Figure 2.10 model the substrate effects, including the substrate parasitic capacitance (C_{sub1}, C_{sub2}) and parasitic conductance (G_{sub1}, G_{sub2}). They also can be extracted from elements in the [$\mathbf{Y_{par}}$] matrix

$$Y_{sub1}(\omega) = G_{sub1} + j\omega C_{sub1} = Y_{11}(\omega) + Y_{12}(\omega) \tag{2.3}$$

$$Y_{sub1}(\omega) = G_{sub2} + j\omega C_{sub2} = Y_{22}(\omega) + Y_{12}(\omega) \tag{2.4}$$

Then, the response of the pure mechanical vibration, [$\mathbf{Y_{res}}$], can be obtained by subtracting the parasitic network, [$\mathbf{Y_{par}}$], from the measured device response, [$\mathbf{Y_{DUT}}$],

$$[\mathbf{Y_{DUT}}] = [\mathbf{Y_{DUT}}] - [\mathbf{Y_{par}}], \tag{2.5}$$

and the *S*-parameter of the mechanical vibration, [$\mathbf{S_{mech}}$], can be obtained from [$\mathbf{Y_{mech}}$] in Equation (2.5). Such de-embedding procedures derive the true response of mechanical vibration, [$\mathbf{S_{mech}}$], and it is applicable to general MEMS resonators. Applying this de-embedding process is especially important for resonators where electrical feedthrough can significantly affect the measured resonator responses (*e.g.*, resonators designed at high frequencies or with low motional impedances). Referring to a certain mechanical resonance, the motional impedance (R_m) can be extracted as

$$R_m = 2Z_0|S_{110}|/(1-|S_{110}|), \tag{2.6}$$

where S_{110} is the element from the [$\mathbf{S_{mech}}$] matrix at the mechanical resonance frequency. The coupling coefficient (k) is the ratio of the power dissipated in the external loads to that dissipated in the mechanical vibration, and k can be extracted by

$$k = (1-|S_{110}|)/|S_{110}|. \tag{2.7}$$

Using k, the unloaded Q (Q_U) can be calculated from the 3-dB Q of $|S_{21}|$ in the [$\mathbf{S_{mech}}$] matrix (Q_L),

$$Q_U = (1+k)Q_L. \tag{2.8}$$

Here, the Q_U is the true quality factor of the mechanical vibration with all the electrical loss subtracted. For a resonator with a small motional impedance (R_m) (comparable to 50 Ω), the Q obtained from 3 dB bandwidth of $|S_{21}|$ underestimates the true Q of the mechanical vibration. The Q_U extraction results for the silica resonator are summarized in Table 2.2. The f×Q product demonstrated in this work is the highest among reported micromachined fused silica/quartz resonators. We believe the Q values obtained from the fabricated silica resonator are still limited by loss mechanisms which originate from interface losses, and can be further improved by optimizing the silica process/ stack material.

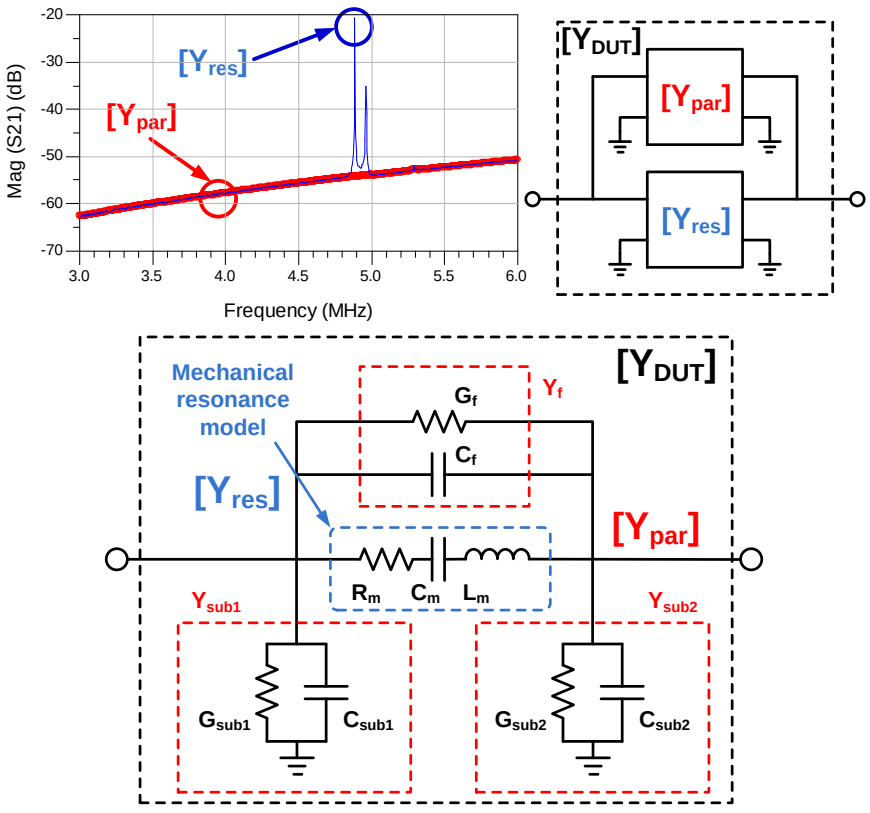


Figure 2.10. Y-parameter representation and equivalent circuit model of the resonator and electrical parasitics.

Table 2.2. Extracted motional impedance (R_m), unloaded Q (Q_U), and f×Q_U product of the silica resonator.

Mode	R_m	Q_U	f×Q_U
2.9 MHz	24.1 KΩ	46,394	1.35×10^{11}
4.88 MHz (out-of-phase mode)	400 Ω	22,111	1.08×10^{11}
4.96 MHz (in-phase mode)	567 Ω	16,860	0.84×10^{11}
16.4 MHz	1.33 KΩ	3,574	0.59×10^{11}

2.1.3.2 Nonlinearity and Power Handling

When making low phase noise oscillators, nonlinearity and power handling of the resonator is another important metric. The phase noise of an electrical oscillator is inversely proportional to the signal power [4], which is limited by the power handling capability of a MEMS resonator. Generally speaking, power handling of piezoelectric resonators is better than capacitive resonators as the nonlinearity due to capacitive transduction is not a limiting factor. To characterize the nonlinearity and power handling, the frequency responses of the silica MEMS resonator are measured by changing the source power levels, and the results for the out-of-phase coupled mode are plotted in Figure 2.11. The measured $|S_{21}|$ responses show that the frequency blue shifts at higher source power levels, indicating "spring stiffening" effect. Such "spring stiffening" is expected to be caused by the nonlinear Young's Modulus of the fused silica/AlN material and the clamped-clamped nature of the support tethers under large vibration displacement. Obvious spring stiffening is observed when a source power of +2 dBm is applied.

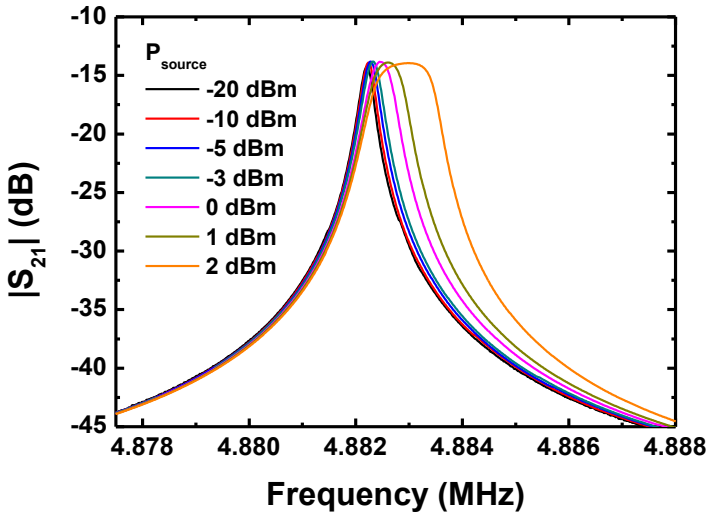


Figure 2.11. S-parameter responses of the out-of-phase resonance mode with various source power levels.

When comparing power handling of MEMS resonators, it is necessary to extract the true driving power that sustains the mechanical vibration given a source power value. The de-embedded *S*-parameter of a resonator reflects the electrical response of mechanical vibration transduced piezoelectrically. Referring to Figure 2.12, the equivalent circuit for an *S*-parameter measurement includes a resonator device, a power source with source impedance of R_0 (50 Ω), and a 50 Ω load termination from the VNA. The VNA source power setting (P_{source}) is the power delivered to the device only if the device presents a matched input impedance (*i.e.*, a 50 Ω input). With a device under test, a portion of the source power is reflected back to the source terminal (P_{ref}), another portion is transmitted through the device and delivered to the load (P_{load}), and the rest of the power is dissipated in the vibration (P_{drive}). The resonator driving power (P_{drive}) can be calculated using

$$P_{drive} = P_{source} - P_{ref} - P_{load} = P_{source}\left(1 - |S_{11}|^2 - |S_{21}|^2\right) \tag{2.9}$$

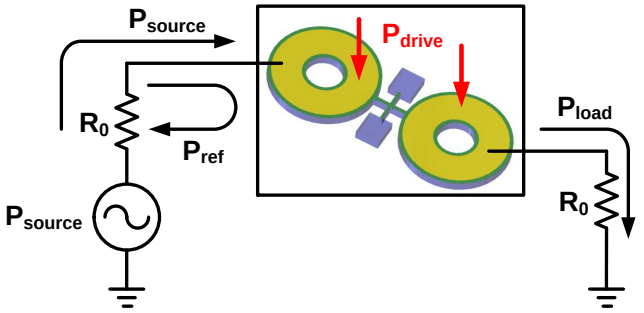


Figure 2.12. Equivalent circuit representing the source and load configurations in an *S*-parameter measurement on a resonator.

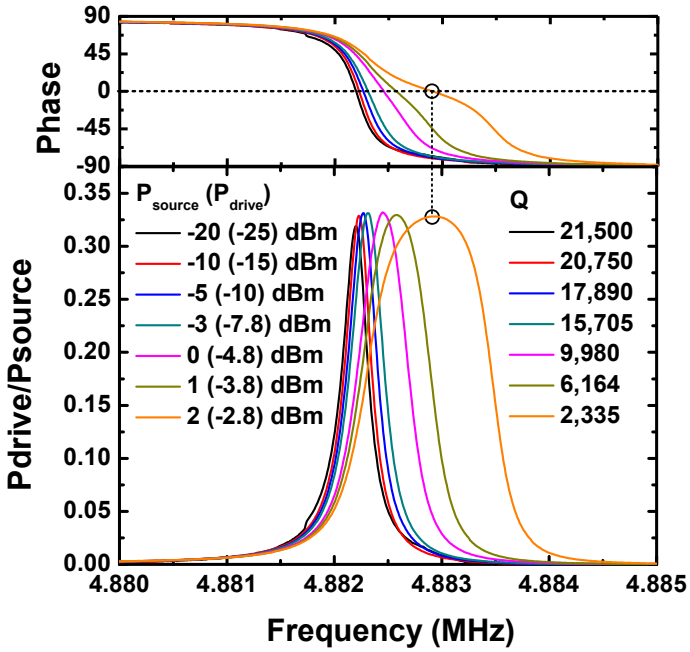


Figure 2.13. The ratio of dissipated power to source power (P_{diss}/P_{source}) for the out-of-phase mode versus source power and the extracted resonator driving power (P_{drive}).

The ratio of P_{drive} to P_{source} is plotted for the out-of-phase mode near the resonance peak at various source power levels in Figure 2.13. It can be observed that there is maximum power dissipation at the resonance frequency, which coincides with the zero phase crossings in the phase responses. Intuitively, at the mechanical resonance frequency, the

resonator can store maximum strain energy in vibration. The extracted driving power (P_{drive}) at resonance frequency is also given in Figure 2.13 with reference to source power. Also, it can be observed in Figure 2.13 that due to the nonlinear property of the resonator, the effective phase slope near mechanical resonance is less steep at a higher driving power. The steepness of phase slope is an indication of rejection of frequency variations due to phase fluctuations. In fact, a quality factor definition for resonators can be expressed as by derivative of phase (θ) with respect to frequency (f) in Figure 2.13,

$$Q|_{\varphi=0^\circ} = \frac{f_0}{2}\frac{d\theta}{df}|_{f=f_0}. \tag{2.10}$$

Although driving the resonator at higher power improves signal-noise-ratio (SNR) when making an oscillator, the nonlinear property causes degradation of the effective Q at a high driving power level. Using (2.10), the unloaded Qs of the fused silica resonator at 0° phase-crossings are also extracted in Figure 2.13 at various source power levels. In an MEMS oscillator design, a resonator in the oscillator loop normally works at inductive region instead of the 0° phase crossing frequency. Other circuit elements also affect the effective Q of the resonator in the oscillator loop. An oscillator implementation based on the fused silica resonator will be discussed in the later section of this chapter.

2.1.3.3 Resonator Temperature Stability

The TCF of the silica resonator is characterized across -40˚C to +85˚C. The resonance frequency is measured in a temperature-controlled probe station with less than mTorr

vacuum level, and the measurement results are plotted in Figure 2.14. The TCF values for three vibration modes are fitted nicely using a linear model. The extracted first-order TCF values range from +76 to +90 ppm/°C. The higher TCF value in silica resonators compared to silicon resonators is mainly due to the intrinsic material property of fused silica, *i.e.* higher temperature coefficient of elasticity (TCE). In order to make a temperature-stable frequency reference, the TCF of silica resonators can be reduced using passive material compensation [45]. However, the high TCE of fused silica material makes it very difficult to realize complete TCF compensation by using a material with opposite TCE, such as silicon. On the other hand, extremely low thermal conductivity of fused silica (1.3 $K \cdot m^{-1} \cdot K^{-1}$) makes it ideal for realizing thermal isolation structures. Therefore, ovenized fused silica MEMS can be implemented with low power consumption for temperature-stable operation. Fused silica MEMS in an ovenized device-layer will be introduced later in this chapter.

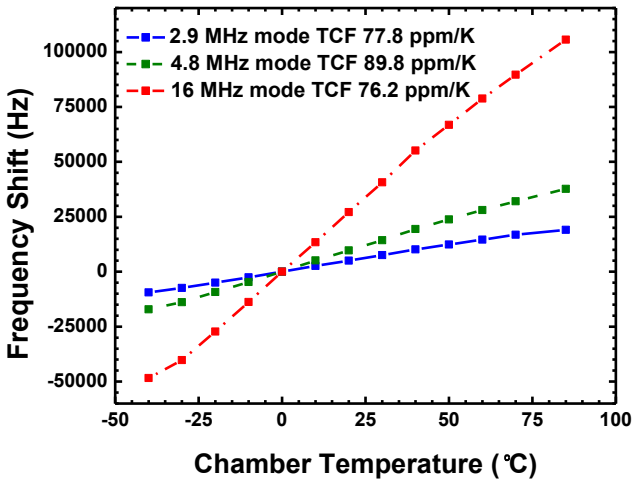


Figure 2.14. Resonator frequency shift versus temperature and extracted TCF for three vibration modes (4.8 MHz mode refers to the out-of-phase radial extensional mode).

2.2 Fused Silica MEMS Oscillator

2.2.1 MEMS Oscillator Design and Implementation

Using the piezoelectric-on-silica MEMS resonator as a mechanical frequency reference, a Pierce MEMS oscillator is implemented using 180 nm CMOS technology (Figure 2.15). The CMOS circuit is interfaced to the fused silica resonator at the board level. In the fused silica resonator design, both the out-of-phase and in-phase coupled-radial vibration modes exhibit high Q and low motional impedance, as re-plotted in the measured frequency responses in Figure 2.16. In a Pierce oscillator, the MEMS resonator works in the inductive region, and two capacitors (C_{p1} and C_{p2}) together with the MEMS resonator, provide 180 °phase shift. The phase condition in the oscillator loop provides a natural mode-selection that excites the out-of-phase vibration mode which has 0°-phase crossing at the resonance frequency (Figure 2.16). Capacitors C_{pl} and C_{p2} can be configured to tune the oscillator frequency, and they also absorb chip and package parasitic capacitances.

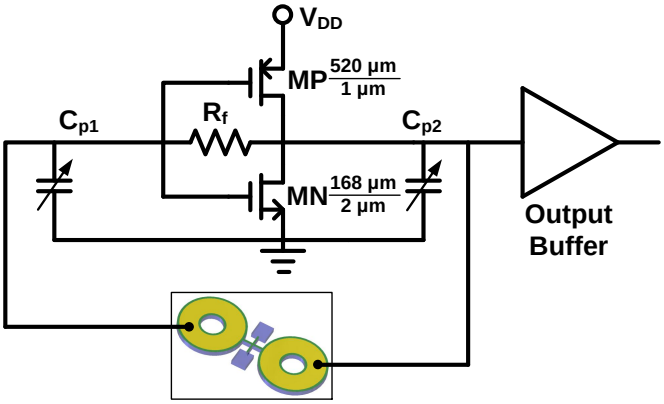


Figure 2.15. Circuit schematic of the Pierce MEMS oscillator.

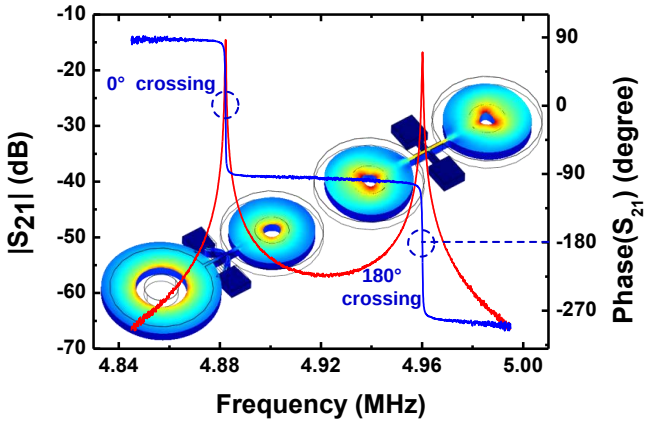


Figure 2.16. The measured frequency responses of the silica resonator near radial vibration modes (showing phase responses of both out-of-phase and in-phase modes).

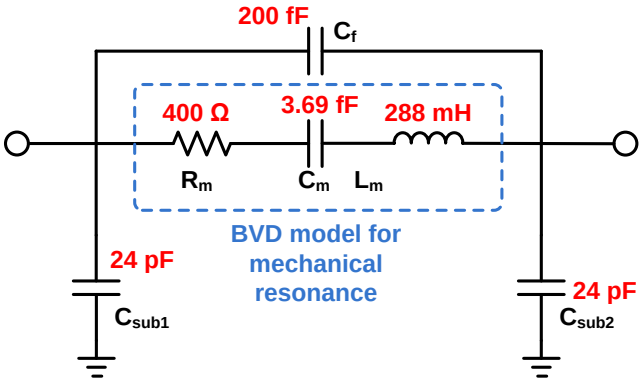


Figure 2.17. An extracted equivalent circuit model for the out-of-phase mode of the fused silica resonator in a ceramic package.

Using the equivalent circuit model for the MEMS resonator extracted from measurement (Figure 2.17), the CMOS oscillator circuit can be optimized. The design considerations of the MEMS oscillator can be obtained from the analysis using the small signal model in Figure 2.18. In Figure 2.18(a), the MEMS resonator is represented by the BVD model (R_m, L_m, C_m), along with parasitic capacitances, including feedthrough

capacitance (C_F) and substrate parasitic capacitances (C_{sub1}, C_{sub2}). To meet the phase condition for oscillation, the MEMS resonator needs to provide an inductive impedance to cancel out the capacitive elements. Hence, the BVD model of the resonator is transformed to a parallel combination of L_P and R_P in Figure 2.18(b). The Q_U of the MEMS resonator can be related to the BVD model elements by

$$Q_U = \omega_0 \cdot L_m / R_m, \tag{2.11}$$

where ω_0 is the mechanical resonance frequency,

$$\omega_0 = \sqrt{1/(L_m \cdot C_m)}. \tag{2.12}$$

For a MEMS resonator having a high Q_U, the value of L_P in Figure 2.18(b) can be calculated as

$$L_P(\omega) \approx L_m\left(1-\frac{{\omega_0}^2}{\omega^2}\right) = \frac{R_m Q_U}{\omega_0}\left(1-\frac{{\omega_0}^2}{\omega^2}\right). \tag{2.13}$$

The oscillation frequency (ω_{OSC}) is determined by parallel resonance of L_P with the total parallel capacitance (C_P). C_P includes parasitic capacitances C_{sub1}, C_{sub2}, C_F, and additional capacitances, C_{p1} and C_{p2}, added to define the oscillator output frequency. If in a simplified analysis the drain output resistance (r_{oN}//r_{oP}) of the NMOS/PMOS pair is very large, C_P can be calculated as

$$C_P = C_{sub1} // C_{sub2} + C_F + C_{P1} // C_{P2}. \tag{2.14}$$

Then, the oscillation frequency be derived as

$$\omega_{OSC} = \sqrt{\omega_0{}^2 + \frac{\omega_0}{R_m \cdot Q_U \cdot C_P}} \approx \omega_0 \left(1 + \frac{C_m}{2C_P}\right). \tag{2.15}$$

It is worth noting that by using large C_{P1} and C_{P2}, the minimum oscillation frequency can be set close to

$$\omega_{OSC}\big|_{\min} = \omega_0, \tag{2.16}$$

whereas the maximum oscillation frequency is bounded by the parasitic capacitances from the MEMS resonator and the CMOS circuit,

$$\omega_{OSC}\,|_{\max} \approx \omega_0 \left(1 + \frac{C_m}{2\left(C_{sub1} \,//\, C_{sub2} + C_F\right)}\right). \tag{2.17}$$

If two resonators have same Q_U and ω_0, the one with a larger R_m has a narrower range of frequency that an oscillation can be designed. The value of R_P in Figure 2.18(b) can be calculated as

$$R_P(\omega) \approx \left\{ Q_U{}^2 \cdot \left(\frac{C_m}{C_P}\right)^2 + 1 \right\} \cdot R_m. \tag{2.18}$$

It can be found in (2.18) that a high Q_U results in Q-amplification that generates a high R_P value. The negative resistance, $-1/(g_{mN}+g_{mP})$ from the NMOS/PMOS pair in Figure 2.18 is the equivalent impedance looking into the input and output terminals of the CMOS inverter amplifier. The negative resistance cancels out resistive elements, which is

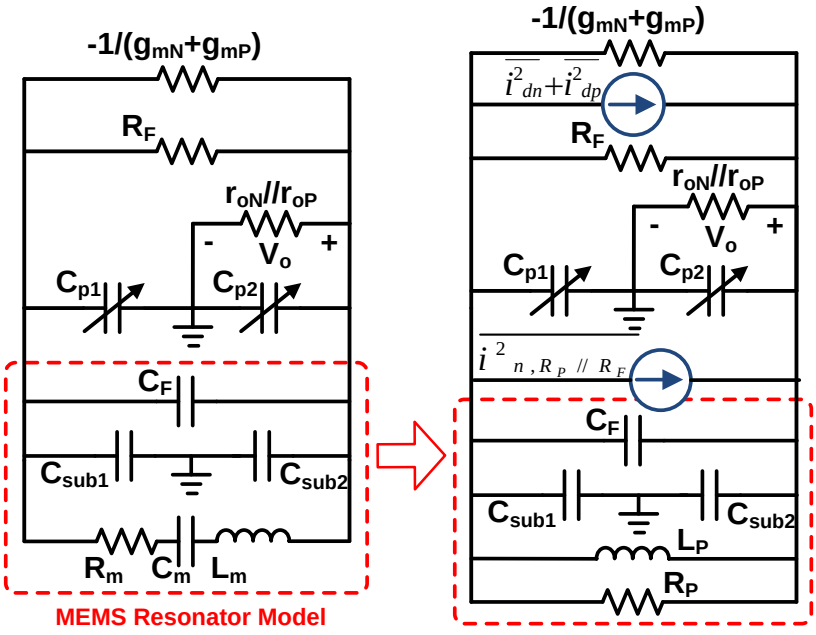


Figure 2.18. (a) Small signal circuit model of the Pierce MEMS oscillator; (b) Modified equivalent circuit model of the MEMS oscillator with noise sources.

indicative of using active MOSFETs to compensate energy loss. With a high R_P value, less transconductance gain (g_{mN}+g_{mP}) is needed to sustain the oscillation. However, if too large of a C_P value is used to pull the oscillator frequency close to ω_0 (from Equation (2.15)), the value of R_P is significantly reduced according to Equation (2.18), and a larger transconductance gain is needed. In the fused silica MEMS oscillator, a low R_m value and a high Q_U ensures that a single-stage CMOS inverter amplifier can provide sufficient gain for sustaining stable oscillation in a large C_P range.

The circuit model in Figure 2.18 also includes dominant noise sources in the oscillator circuit. The drain current noise in NMOS and PMOS include both thermal noise and Flicker (1/f) noise,

$$\overline{i^2_{dn}} + \overline{i^2_{dp}} = 4kT\gamma\left(g_{mn} + g_{mp}\right) + g_{mp}{}^2 \frac{K_P}{W_P L_P C_{ox}} \frac{1}{f} + g_{mn}{}^2 \frac{K_N}{W_N L_N C_{ox}} \frac{1}{f}. \quad (2.19)$$

It can be found that over-designing the transistors for too large of a transconductance gain (g_{mn} and g_{mp}) results in excessive noise injection. The resistor, R_F, in the oscillator circuit is for self-biasing the inverter amplifier, which has a large value (~1 MΩ). It is also beneficial to make (R_P//R_F) large to reduce their thermal noise contribution:

$$\overline{i^2_{n,R_F // R_P}} = 4kT/\left(R_F // R_P\right). \quad (2.20)$$

The Q_L of the MEMS resonator in the oscillator circuit is affected by the resistive elements in Figure 2.18 that loads the parallel tank, including R_P, R_F, and r_{oN}//r_{oP}. These resistive elements are preferably to be maximized. It is worth to note that noise analysis on the oscillator needs to treat the oscillator as a time variant system. Also, the CMOS inverter amplifier works in a nonlinear class-AB operation where the output voltage of the MEMS oscillator swings almost rail-to-rail at the drain of the MOSFETs. Therefore, the transconductance (g_{mn}+g_{mp}), the drain output resistance (r_{oN}//r_{oP}), and noise sources needs to be treated as large signal equivalent elements to more accurately predict the oscillator performance. The MEMS resonator also exhibits nonlinear property at large driving amplitude, and such nonlinearity needs to be captured with a more complicated circuit model for the MEMS resonator [46]. Here, the analysis using small signal equivalent model is used mainly to give insights for optimizing the MEMS oscillator design.

Although Leeson's model [4] is derived by treating an oscillator as a linear time

invariant (LTI) system, it is very straightforward in highlighting factors that determine phase noise of an electrical oscillator. The single side band (SSB) phase noise of an oscillator at offset frequency (Δf) from the carrier frequency (f_0) can be expressed as

$$L(\Delta f) = 10\log\left\{\frac{i_n^{\,2}}{2i_{drive}^{\,2}}\left(1+\frac{f_C}{\Delta f}\right)\left(1+\left(\frac{1}{2\Delta f Q_L}\right)^2\right)\right\}, \tag{2.21}$$

where i_n^2 is a noise current power that includes all the noise sources in Figure 2.18; i_{drive}^2 is the driving amplitude on the MEMS resonator; f_C is a corner frequency determined by Flicker noise. In designing a low phase noise MEMS oscillator, a high resonator Q_U helps obtaining a high Q_L, which shapes the close-in-carrier phase noise. If a MEMS resonator exhibits good power handling, sufficient driving power (i_{drive}^2) can be applied to the resonator to improve phase noise. Also, low motional impedance ensures that a sufficient driving current can be obtained when a low voltage swing is applied on the resonator. This property is preferable for making low phase noise oscillators using deep sub-micron CMOS with limited supply voltage. For improving Flicker noise performance of the oscillator, the MOSFETs are sized with large gate areas according to (2.19). Also, a linear time-variant (LTV) model of electrical oscillators [47] indicates that Flicker noise can be reduced by designing the oscillator with symmetrical rising and falling edges in the output waveform. Therefore, the NMOS and PMOS in Figure 2.15 are sized with near equal transconductance.

For the MEMS oscillator design in this work, the supply voltage (V_{DD}) of the circuit can be adjusted to control the circuit gain and the driving power on the MEMS resonator.

A stable oscillation is obtained at a low supply voltage (V_{DD}) of 1 V and low bias current of ~120 μA. The phase noise performance is measured using an Agilent E5500 system. With C_{P1} and C_{P2} of 40 pF, the MEMS oscillator shows a phase noise of -138 dBc/Hz at 1 kHz offset，-154 dBc/Hz at 10 Hz offset, and -155 dBc/Hz at far-from-carrier (Figure 2.19). The Flicker noise corner frequency (f_C) is observed near 2 kHz. The power supply is provided to the oscillator using an Agilent E3612A DC source. The phase noise plot shows spurs induced from the Agilent E3612A power supply due to poor supply noise rejection property of the CMOS inverter amplifier. The output waveform of the oscillator is shown in the inset of Figure 2.19. Being a first demonstration of an electrical oscillator using fused silica MEMS, the measured phase noise performance is comparable to that of the reported silicon-based MEMS oscillators (Table 2.3).

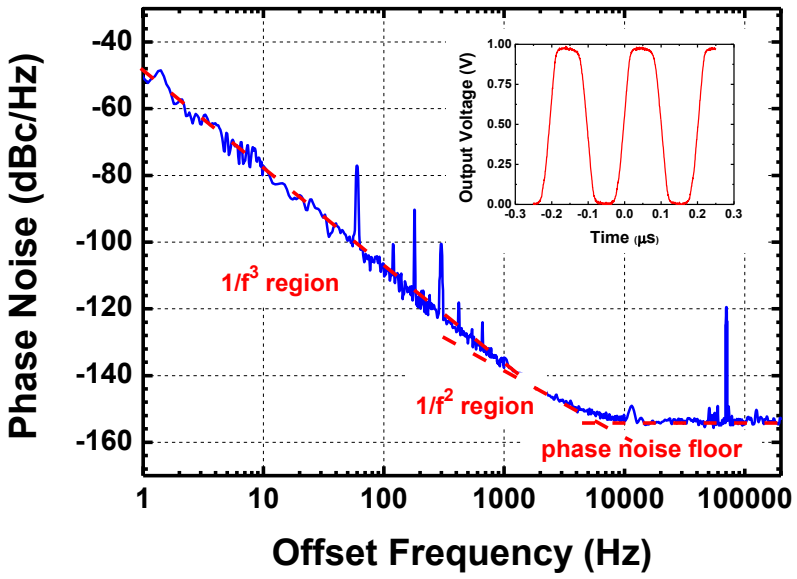


Figure 2.19. Measured phase noise of the silica MEMS oscillator at a low supply voltage of 1 V (with oscillator output waveform shown in the inset).

Table 2.3. Performance comparison of the silica MEMS oscillator with reported silicon MEMS oscillators.

Oscillator	Resonator	Phase Noise (dBc/Hz)	Normalized to 10 MHz
60 MHz [48]	Silicon	-123 @ 1 KHz; -136 floor	-139 @ 1 KHz; -152 floor
145MHz [49]	Silicon	-111 @ 1 KHz; -133 floor	-134 @ 1 KHz; -156 floor
496 MHz [50]	AlN-on-Si	-92 @ 1 KHz; -147 floor	-126 @ 1 KHz; -181 floor
6 MHz [51]	Silicon	-112 @ 1 KHz; -135 floor	-108 @ 1 KHz; -131 floor
This work 4.9 MHz	**AlN-on-silica**	**-138 @ 1 kHz; -155 floor**	**-132 @ 1 KHz; -148 floor**

2.2.2 Oscillator Vibration Stability

If a timing reference is designed for use in a navigation system such as a timing and inertia measurement unit (TIMU), the existence of external vibration or shock is significant. Vibration causes shifts in the center frequency of the resonator and degradation on the oscillator phase noise. In this work, the use of piezoelectric transduction eliminates the impact of vibration on electrical stiffness, which can dominate the frequency drift in capacitive MEMS resonators [52]. Instead, the frequency shift of the silica MEMS resonator is mainly due to the mechanical stress induced from vibration. Quartz crystal oscillators can experience similar effects, with a typical frequency shift of 10^{-12}/g for precision SC-cut quartz to more than 10^{-7}/g for low-cost AT-cut quartz. As the silica micro-resonator has very small mass compared to a quartz resonator, the effect of vibration is expected to be less significant. Using COMSOL FEM software, the vibration sensitivity of the silica resonator has been simulated to be $\Delta f/f_0 < 10^{-12}$/g in all directions (Figure 2.20).

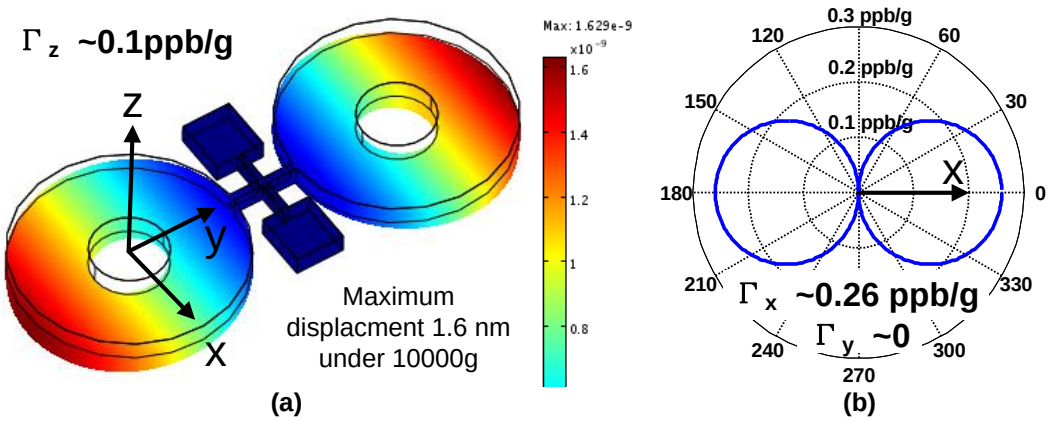


Figure 2.20. (a) Simulated bending due to 10000 g acceleration in z-direction and vibration sensitivity (Γ_z); (b) Simulated in-plane vibration sensitivity.

The vibration sensitivity is difficult to measure by directly capturing the small shift of resonance peak in the *S*-parameter response by a network analyzer. Instead, as vibration modulates the oscillator output signal and hence excites sideband peaks in the oscillator output spectrum; the vibration sensitivity of the oscillator can be extracted from the power of the sideband peaks [53]. The vibration-induced frequency shift Δf_{vib} for a resonator is expressed as

$$\Delta f_{vib} / f_0 = \boldsymbol{\Gamma} \cdot \mathbf{a}, \tag{2.22}$$

where f_0 is the resonance frequency, $\mathbf{a}$ is the vector acceleration, and $\boldsymbol{\Gamma}$ is the vector vibration sensitivity. With an external vibration at frequency f_v, the power of the sideband peak excited by vibration can be expressed as

$$L(f_v) = 20\log\left[(\boldsymbol{\Gamma} \cdot \mathbf{a})\frac{f_0}{2f_v}\right]. \tag{2.23}$$

To measure the vibration sensitivity, the silica MEMS oscillator is mounted in a custom-made vacuum chamber. The vacuum chamber is firmly mounted on a vibration stage, while the MEMS oscillator is running. An Agilent E5500 phase noise measurement tool is used to capture the sideband peaks due to external vibration. A sideband peak excited by vibration appears as a spur in the phase noise measurement tool, which is captured as the output power of the spurs (in dBm) instead of phase noise power density (dBc/Hz). The sensitivity can be directly extracted from the peak power using Equation (2.23). A sinusoidal vibration at 100 Hz is applied in the range of 1 g to 4 g in the direction orthogonal to the resonator device (z-direction in Figure 2.20). As shown in Figure 2.21, spurs are generated at the offset frequency of 100 Hz from the carrier in the phase noise measurement results. Using (4.13), the vibration sensitivity (Γ_z) is extracted to be less than 4 ppb/g (Figure 2.22). This result is comparable with some SC-cut quartz-based oscillators. However, we believe that the vibration sensitivity is still dominated by the electrical components in the measurement setup as observed in [52], including bondwires, cable connections, *etc*. The silica resonator itself is expected to have significantly smaller vibration sensitivity.

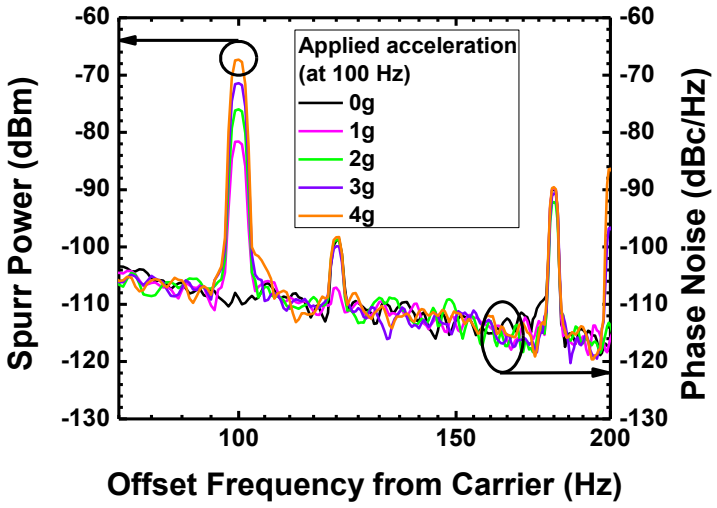


Figure 2.21. Phase noise measurement results of the silica MEMS oscillator, showing spurs in responses of sinusoidal vibration in the range of 1-4g at 100 Hz.

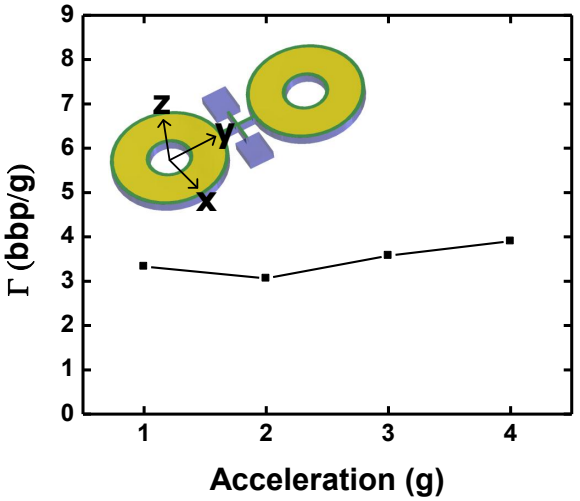


Figure 2.22. Extracted z-axis acceleration sensitivity of the silica MEMS oscillator.

2.2.3 Oscillator Frequency Tuning Techniques

When implementing a precision frequency reference, frequency tuning techniques are employed to compensate for initial frequency error or frequency drift. While the fused

silica MEMS resonator is demonstrated with low phase noise in this work, a large TCF of +89 ppm/K in the fused silica resonator demands frequency compensation techniques. The large frequency drift over working temperature (typically -40 °C to 85 °C) exceeds the tuning range of normal electrical frequency tuning techniques. However, utilizing the extremely low thermal conductivity of fused silica material, the large drift of frequency over working temperature is drastically reduced by low power ovenization. The fused silica MEMS resonator in an ovenized device-layer will be presented in the later section. Apart from ovenization, frequency tuning techniques that can cover medium to high resolution are also investigated for compensating other sources of drift, such as acceleration/shock, supply or load pulling effects, *etc*.

2.2.3.1 Capacitive Frequency Tuning

Conventional capacitive tuning method can be employed to tune the MEMS oscillator frequency. Capacitors C_{P1} and C_{P2} in the Pierce oscillator (in Figure 2.15) can be made in the form of varactors or switched-capacitor banks to pull the MEMS oscillator frequency. To characterize the tuning characteristic, two Zetex 835A varactors are connected in parallel with fixed capacitors to form C_{P1} and C_{P2}. Figure 2.23 plots the frequency shift of the silica oscillator when both C_{P1} and C_{P2} are changed by changing the DC bias voltage of the varactors. A change of 33 pF in both C_{P1} and C_{P2} causes 2 KHz (*i.e.*, 408 ppm) of frequency shift in the oscillator output signal. The extracted pulling sensitivity is 1.4–3.7 ppm/pF. To achieve more accurate capacitive tuning and lower noise, varactors can be replaced by digital switched capacitor banks.

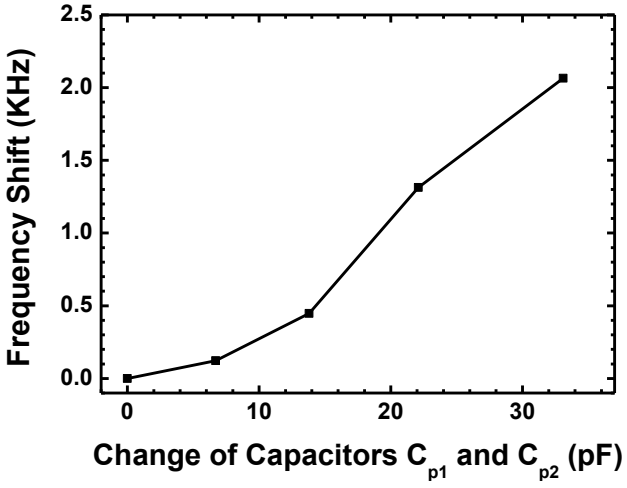


Figure 2.23. Measured oscillator output frequency shift as both capacitors C_{p1}, C_{p2} are changed.

There exists a tuning range limit by using the capacitive frequency tuning method. From the analysis in Equations (2.16) and (2.17), the output frequency tuning range of a MEMS oscillator is limited by

$$\frac{\Delta\omega_{OSC}}{\omega_0} < \frac{C_m}{2\left(C_{sub1} // C_{sub2} + C_F\right)}. \tag{2.24}$$

Equation (2.24) above indicates the effect of parasitic capacitance (C_{sub1}, C_{sub2}, and C_F) on the achievable frequency tuning range. The parasitic capacitance of the MEMS resonator is unavoidable. In fact, the ratio of the motional capacitance (C_m) to the total parasitic capacitance ($C_{sub1}//C_{sub2}+C_F$) in a MEMS resonator (Eq. (2.25)), is related to a fundamental physical property, *i.e.* "electromechanical coupling coefficient (k_t^2)".

$$r = \frac{\left(C_{sub1} // C_{sub2} + C_F\right)}{C_m}. \tag{2.25}$$

k_t^2 is a parameter that describes the conversion between electrical and mechanical energy intrinsic to the piezoelectric device. The value k_t^2 is related to r by [54]

$$k_t^2 = \frac{\pi^2}{8}\left(\frac{1}{r}\right)\left(1-\frac{1}{r}\right). \tag{2.26}$$

From the resonator circuit model in Figure 2.17, the fused silica resonator in a ceramic package achieves a k_t^2 value of 0.04% (r of 3306). This k_t^2 number sets the maximum frequency tuning range to ~150 ppm for the MEMS oscillator. The parasitic capacitance from the package and the CMOS circuit further reduces the tuning range. The maximum achievable value of k_t^2 for MEMS resonators using the cross-axis piezoelectric coupling (d_{31}) of sputtered AlN thin-film has been reported around 1-2% [55], which is limited by the intrinsic piezoelectric property of the AlN material.

The frequency tuning characteristic in a MEMS oscillator can deviate from the above analysis that uses a linear resonator model. With a higher driving amplitude on the MEMS resonator, a larger frequency shift can be induced by amplitude change ("A-F" effect), as shown the power handling characterization in Section 2.1.3.2. The "A-F" effect also explains the higher measured frequency tuning range in Figure 2.23 than the estimated maximum tuning range using a linear resonator model. However, nonlinearity in the MEMS resonator potentially injects additional phase noise from amplitude noise through "AM-PM conversion". To obtain a near-constant phase noise performance with a large change in C_{P1} and C_{P2} to pull the oscillator frequency, a common practice is to use an automatic amplitude limiting circuit to adaptively adjust the gain of the oscillator [56].

2.2.3.2 Piezoelectric Frequency Tuning

In this work, we also propose a new high-resolution frequency tuning technique by utilizing the physical property of piezoelectric-on-substrate MEMS resonators. Very tight frequency accuracy is commonly required in making precision clocks for navigation-grade time keeping and wireless frequency synthesizers. For example, Global Standard for Mobile Communications (GSM) and Wideband Code Division Multiple Access (WCDMA) standards require that the average frequency deviation of the transmitted carrier frequencies from handsets must be better than 0.1 ppm with respect to the receiving carrier frequencies in base stations [57], [58]. Such stringent frequency accuracy requirement is usually achieved through an automatic frequency control (AFC) loop, which synchronizes a handset to a base station through digital tuning. We have shown the vibration sensitivity of the silica MEMS oscillator is better than 4 ppb/g, which also requires frequency pulling resolution at sub-ppm or ppb level to compensate for frequency drift induced by vibration. However, an ultra-small frequency step requires a very small unit capacitance change when capacitive tuning is employed. The unit capacitance can be overwhelmed by parasitic capacitance, which limits the tuning resolution for capacitive tuning method [59]. As a remedy, a Σ-Δ modulator has been proposed to achieve a finer resolution [60] given a smallest unit capacitance step, but at the cost increased circuit complexity.

As a new method, piezoelectric-tuning is proposed for high-resolution frequency tuning for piezoelectric-MEMS oscillators. Different from normal operation that grounds the bottom electrode, the resonator bottom electrode can be connected to a DC bias

(Figure 2.24). If the sputtered AlN thin-film has c-axis point down toward the bottom electrode, applying a positive DC voltage on the bottom surface causes the AlN layer to compress [61]. Therefore, the Young's modulus of the AlN film increases due to compressive strain. The effective Young's modulus of AlN-on-silica composite material can be expressed as

$$E_{composite} = \frac{E_{silica} + E_{AlN} \cdot (t_{AlN} / t_{silica})}{1 + (t_{AlN} / t_{silica})}, \tag{2.27}$$

where E_{silica} and E_{AlN} are the Young's modulus of fused silica and AlN, respectively; t_{silica} and t_{AlN} are thickness of fused silica and AlN, respectively. With a large thickness ratio of t_{silica}/t_{AlN} (i.e., 60 μm/1 μm), the composite Young's modulus ($E_{composite}$) changes in a very small amount due to stiffening of the AlN layer. Therefore, the natural frequency of the AlN-on-silica resonator experiences a slight up-shift with a positive DC bias applied on the bottom electrode. We utilize this small frequency shift to DC voltage to achieve high-resolution frequency tuning for the MEMS oscillator, that we call "piezoelectric tuning".

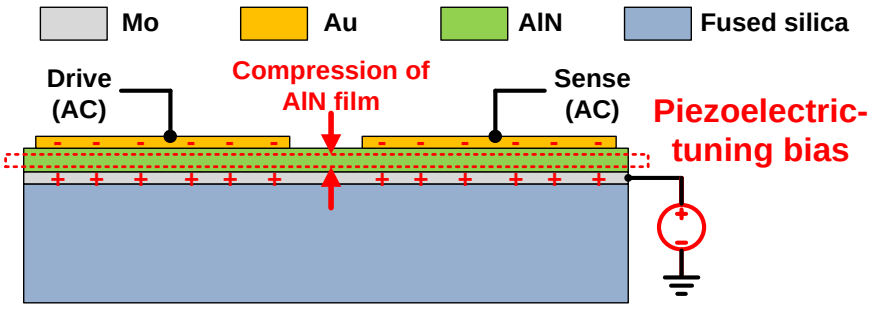


Figure 2.24. Cross-section view of the piezoelectric-on-silica resonator, showing the principle of piezoelectric-tuning: applying a DC bias voltage on the resonator bottom electrode causes compression of the AlN film.

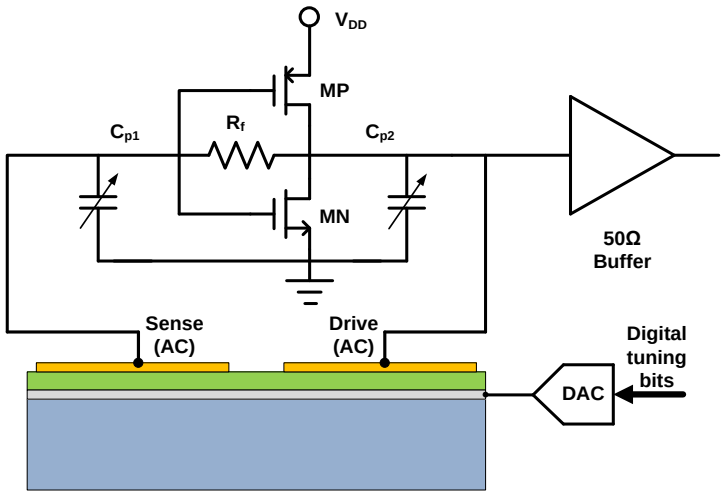


Figure 2.25. Circuit schematic of the silica MEMS oscillator with piezoelectric-tuning. A DAC is used to generated digital-controlled tuning bias voltage on the bottom electrode of the AlN-on-silica MEMS resonator.

To realize piezoelectric tuning, the silica MEMS resonator is still connected in the oscillator loop, and the bottom electrode is connected to the output of an 8-bit digital-to-analog converter (AD7801) for generating a digital-controlled tuning bias (Figure 2.25). In order to extract the tuning sensitivity, the input control bits are programmed to generate various output bias voltages, while the output frequency of the MEMS oscillator is monitored through a frequency counter (Agilent 53181A). Figure 2.26 plots frequency shift of the oscillator (in ppm) with respect to piezoelectric tuning bias voltage. Multiple measurements are taken to ensure consistency and repeatability of the tuning technique. It can be found that the tuning curve shows excellent linearity with a tuning coefficient of 0.3 ppm/V. Therefore, using a low resolution DAC and low reference voltage (typical in deep sub-micron CMOS), an oscillator frequency tuning step of less than 0.1 ppm or down to ppb can be easily achieved.

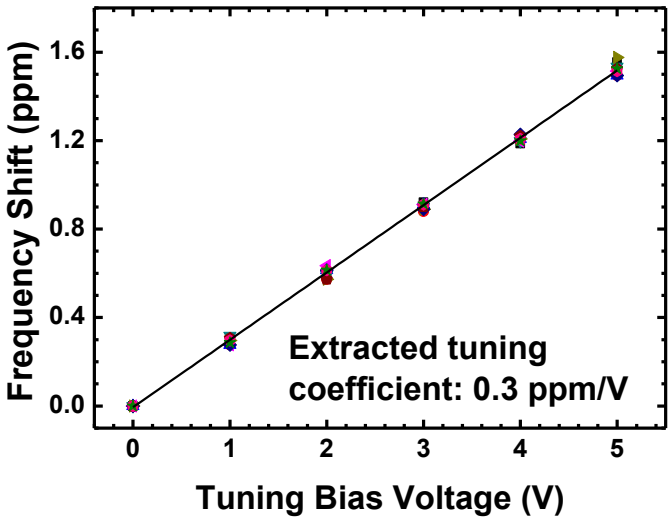


Figure 2.26. Measured MEMS oscillator frequency shift versus piezoelectric tuning bias voltage. Different symbols are from different measurement runs.

The phase noise performance of the oscillator with piezoelectric-tuning is also measured. Figure 2.27 shows the phase noise performance of the MEMS oscillator when a DAC is connected to resonator bottom electrode. The phase noise with "piezoelectric tuning" is shown when the output from the DAC is at 5 V. It can be observed that there is negligible degradation on the phase noise performance when the piezoelectric tuning technique is used. In this oscillator implementation, a linear voltage regulator (ADP1706) is used to provide the power supply for the CMOS inverter amplifier. Due to the supply noise rejection provided by the linear regulator, spurs in the phase noise spectrum are significantly attenuated. For the use of MEMS oscillators in mix-signal environments, where nearby switching circuits are functioning, such power supply interference rejection property is critical. However, it can be observed that the phase noise performance is degraded from 1 kHz to 100 kHz offset frequencies when a linear voltage regulator is

employed. The added phase mainly comes from the noise of the voltage regulator. This emphasizes the importance of using low-noise voltage or current reference.

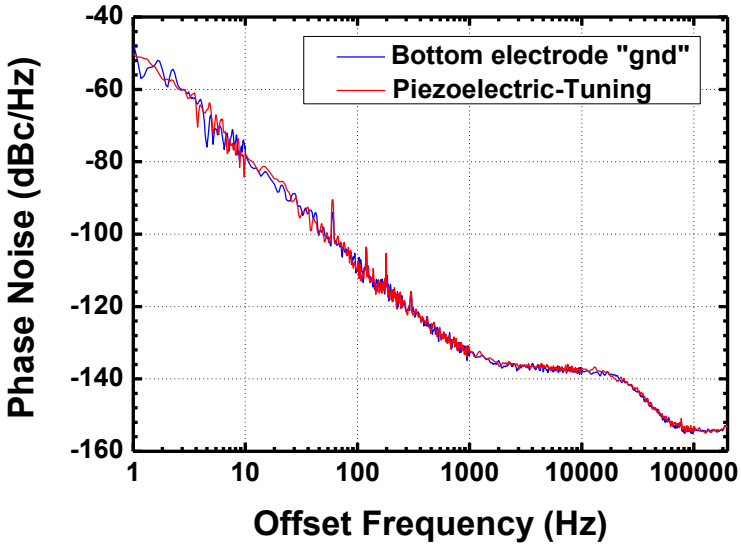


Figure 2.27. Measured phase noise of the MEMS oscillator with piezoelectric-tuning and compared to the MEMS oscillator in normal operation.

2.2.4 MEMS Resonators in an Ovenized Platform

2.2.4.1 Ovenized Fused Silica Device Layer

According to the characterization results in the previous section, fused silica MEMS resonators exhibit a high TCF of ~+89 ppm/K, owing to the high TCE of silica. For fused silica MEMS oscillators, the overall temperature-induced frequency drift over a typical work temperature range (-40 to 80 °C) is larger than the frequency pulling range of any electrical compensation technique.

Here, ovenization is sought as an effective temperature compensation method and applied to a large fused silica platform (or so called device-layer) having multiple

devices. Ovenization is known to offer excellent thermal stability. Ovenized quartz crystal oscillators (OCXOs) are known to deliver best stability among crystal timing references. Moreover, ovenized MEMS resonators have been demonstrated with power consumption as low as tens of milli-Watts [62], [63]. However, most reported approaches are specific to a single resonator and are not directly applicable to a multi-device fusion platform. In this section, an ovenized fused silica platform is developed that can stabilize multiple MEMS devices over a wide external temperature range. This way, the temperature stability of all devices is drastically improved, irrespective of their specific device design. Such an approach is more generic as compared to the previous works [62], [63] that use specific thermal isolation methods for regulating the TCF-induced drift of individual micro-devices. A scanning electron microscope (SEM) image of the fabricated fused silica platform is shown in Figure 2.28. The fabrication of the device-layer follows the same steps used in fabricating a silica resonator, as introduced in Section 2.1.1. The platform has a large active area of 3 mm × 3 mm. As a proof-of-concept of the device fusion capability, four resonators are included in this prototype design. A resistive temperature detector (RTD) is co-fabricated on the device-layer using a 1000 Å-thick platinum (Pt) layer. The RTD has a nominal resistance of 7 kΩ. A Pt resistive heater ring is placed on the edge of the active area and is used to heat the platform to a fixed oven-set temperature to counter external temperature changes.

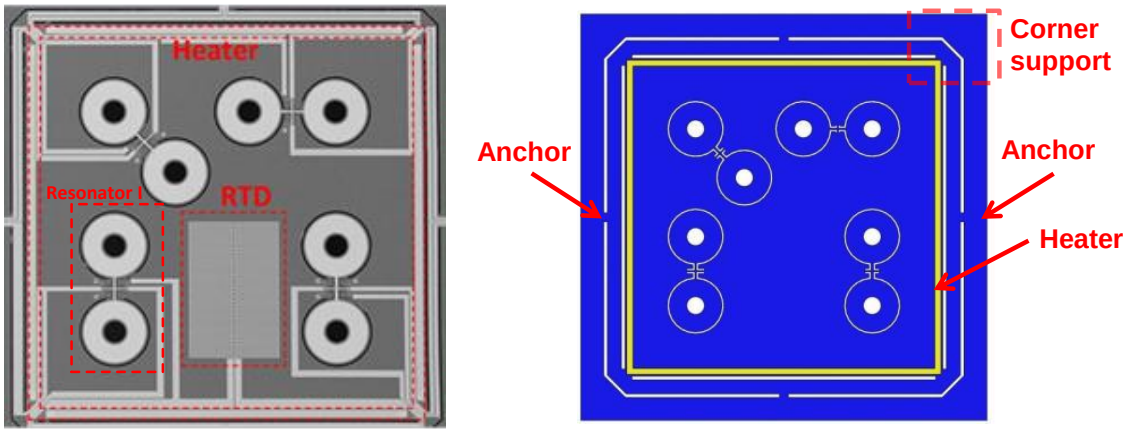


Figure 2.28. (Left) SEM image of a fused silica device-fusion platform with multiple devices in the active area, thermal isolation legs, an integrated thermistor, and a heater; (Right) Sketch of the platform design with highlight on key parts.

2.2.4.2 Thermal Analysis on the Ovenized Fused Silica Device-Layer

In order to reduce the power consumption of ovenization, it is critical to thermally isolate the active area from the external environment. Thermal isolation of the fused silica platform is characterized by the effective thermal resistance (R_{th}) from the platform to the external environment. Here, the effective thermal resistance is the temperature difference between the platform (T_{pl}) and external temperature (T_{ext}) that creates a heat flow (Q_{heat}) in steady-state,

$$R_{th} = \left(T_{pl} - T_{ext}\right) / Q_{heat}. \tag{2.28}$$

With a large thermal resistance, heat loss from the MEMS platform to the external environment is minimal when the platform is heated to an oven set temperature. Therefore, low-power ovenized MEMS require maximizing the thermal resistance between the device and the external thermal boundary.

There are three heat transfer mechanisms: conduction transfer through solids, convection transfer through gas, and radiation heat transfer. The heat loss from these mechanisms adds up, and the total thermal resistance is determined by thermal resistances from conduction ($R_{th,cond}$), convection ($R_{th,conv}$), and radiation ($R_{th,rad}$),

$$R_{th} = \left(\frac{1}{R_{th,cond}} + \frac{1}{R_{th,conv}} + \frac{1}{R_{th,rad}} \right)^{-1} . \tag{2.29}$$

The general equation that describes conduction heat transfer can be expressed as

$$\vec{q}_{cond} = -k \cdot \nabla T . \tag{2.30}$$

where heat flux, $\vec{q}$ (in W/m^2), is the heat flow per unit area due to a temperature gradient (∇T) in a solid material; k (in W m^{-1}K^{-1}) is the thermal conductivity of material. In practical designs, the conduction transfer equation can be simplified as a 1-D problem, and the temperature gradient can be simplified as the end-to-end temperature difference (ΔT) across distance (L) in a thermal isolation structure. Then, the heat flux is the heat flow through a cross-section area (A),

$$Q_{cond} / A = -k \cdot \Delta T / L . \tag{2.31}$$

The thermal resistance due to conduction heat transfer can be expressed as

$$R_{th,cond} = \frac{L}{k \cdot A} . \tag{2.32}$$

In order to maximize the $R_{th,cond}$ of a thermal isolation structure, increasing the L to A ratio is critical. Also, the choice of material with low thermal conductivity is highly desirable. Fused silica (*i.e.* very pure quality amorphous SiO_2) has very low thermal conductivity (1.3 $W\,m^{-1}K^{-1}$). The low thermal conductivity allows for designing relatively wide (width=100 μm) and thick (thickness = 60 μm) isolation legs (Figure 2.29). Such a design improves the platform mechanical robustness by avoiding long and meandered supporting legs usually seen in thermally isolated silicon MEMS [62]. Also, the wide legs allow for wiring of multiple low-resistance electrical routings to external pads using a thin-film metal layer, which favors integration of multiple devices on the platform.

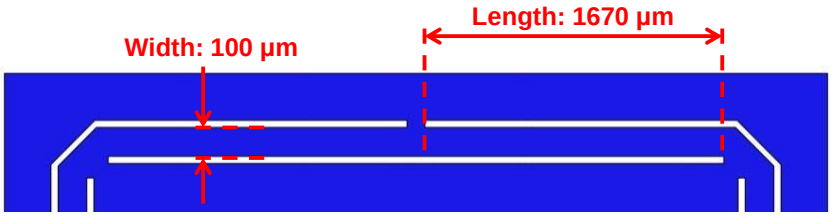


Figure 2.29. Dimension of the thermal isolation legs in the fused silica device-layer.

Convection transfer is the transfer of heat between the surfaces of a device to the surrounding gas environment. In order to minimize convection transfer, it is desirable to operate the device in a low-pressure environment (<1 Pa). This is normally realized by encapsulating the MEMS devices using a hermetic vacuum package [62]. In such a low pressure condition (< 10 mTorr) offered by a MEMS package, heat transfer occurs mainly through the collision of gas molecules on the surfaces of the device, whereas

intermolecular collision is insignificant. With a temperature difference between the MEMS platform (T_{pl}) and the ambient gas (T_{ext}), the convection heat flux from the MEMS device to ambient can be expressed as

$$q_{conv} = h_{conv} \cdot \left(T_{pl} - T_{ext}\right), \tag{2.33}$$

where h (in W·m^{-2}·K^{-1}) is the heat transfer coefficient. The convective heat transfer coefficient (h) is affected by several ambient conditions, including pressure, type of gas, air flow velocity, *etc*. The accurate number of h_{conv} is normally obtained from experimental data and extensive characterization. Here, a simplified physical model can be used to estimate h_{conv} [64].

$$h_{conv} = \alpha_s \Lambda_0 P \cdot \left(\frac{273.2}{T_{ext}}\right), \tag{2.34}$$

where α_s is the accommodation coefficient, P is the gas pressure, and Λ_0 is the free molecular conductivity at 0 ℃. If a MEMS device is in vacuum environment with N_2 gas in the ambient, Λ_0=16.63×10^{-2} (W·m^{-2}·K^{-1}·mTorr^{-1}) can be adopted for estimating convection heat transfer [64]. In addition, it is worth mentioning that the whole surface area of the MEMS platform is exposed to ambient gas, subject to convection heat loss. Therefore, the total heat flow is proportional to the total surface area (A_S) of the MEMS platform,

$$Q_{conv} = q_{conv} \cdot A_S . \tag{2.35}$$

The thermal resistance due to convection heat transfer can be written as

$$R_{th,conv} = \frac{1}{h_{conv} \cdot A_S}. \tag{2.36}$$

Radiation heat transfer is also caused by the temperature difference between the device and ambient environment. The heat flux due to radiation can be expressed as

$$q_{rad} = \varepsilon \cdot \sigma \cdot \left({T_{pl}}^4 - {T_{ext}}^4 \right). \tag{2.37}$$

where ε denotes an emissivity factor (the emissivity of fused silica is ~0.9), and σ is the Stefan-Boltzmann radiation constant (σ =5.56×10^{-8} W m^{-2} K^{-4}). Radiation heat transfer becomes more significant if the MEMS device-layer is heated to high temperature, creating a large temperature difference between the platform (T_{pl}) and the ambient (T_{ext}). Also, heat flux (q_{rad}) through the total device surface area (A_S) creates a radiation heat flow,

$$Q_{rad} = q_{rad} \cdot A_S. \tag{2.38}$$

The thermal resistance due to radiation can be expressed as

$$R_{th,rad} = \frac{1}{\varepsilon \cdot \sigma \cdot (T_{pl} + T_{ext})({T_{pl}}^2 - {T_{ext}}^2) \cdot A_S}. \tag{2.39}$$

Accounting for the above heat transfer mechanisms, the thermal isolation property of the fused silica device-layer in Figure 2.28 can be quantitatively analyzed by incorporating the geometry and material information, which is summarized in Table 2.4.

If the whole active area is heated to maintain an oven temperature of 90 °C, the thermal resistances versus ambient temperature for conduction ($R_{th,cond}$), convection ($R_{th,conv}$), and radiation ($R_{th,rad}$) are compared in Figure 2.30. The total thermal resistance is in the range of 10-18 K/mW. The analysis here has two assumptions: (1) Conduction transfer is only through the eight thermal isolation legs of the platform (Figure 2.28). The assumption is reasonable as the thermal resistance of the isolation legs dominates for the design. (2) The surface area used for calculating convection and radiation transfer treats the whole active region as a fused silica box with the geometry given in Table 2.4. Using the above analysis, the heat flows due to conduction (Q_{cond}), convection (Q_{conv}), and radiation (Q_{rad}) are also plotted in Figure 2.31. The total heat flow indicates the power consumption needed to overcome the heat loss for ovenizing the fused silica platform at a set temperature of 90 °C. It is noteworthy that convection and radiation heat loss needs to be considered for the fused silica device-layer due to a large surface area, which are not significant in small individual MEMS resonators [62], [63].

Table 2.4. Geometries and material properties of the fused silica device-layer.

Thermal isolation legs (length ×width ×thickness)	$1670 \times 100 \times 60\ \mu m^3$
Active region (edge ×edge ×thickness)	$3060 \times 3060 \times 60\ \mu m^3$
Thermal conductivity of fused silica, k ($W\ m^{-1}K^{-1}$)	1.3
Free molecular conductivity at 0 °C, Λ_0 ($W\ m^{-2}\ K^{-1}\ mTorr^{-1}$)	16.63×10^{-2}
Ambient Pressure, P (mTorr)	5
Accommodation coefficient, α_s	0.5
Emissivity of fused silica	0.9

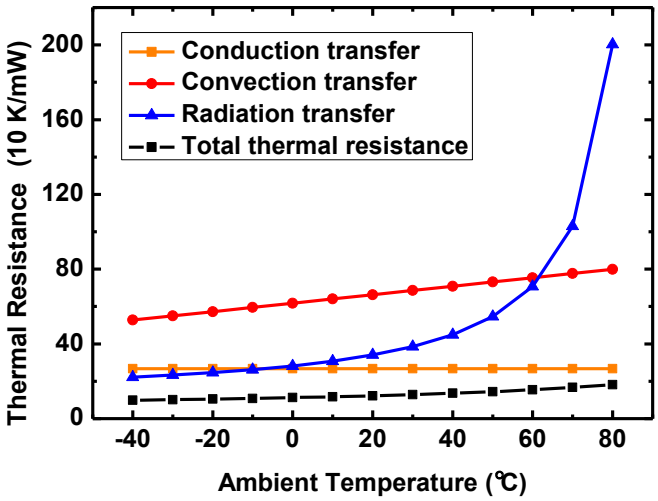


Figure 2.30. Thermal resistance due to conduction, convection, and radiation heat transfer for the fused silica device-layer (with an oven-set temperature of 90 °C).

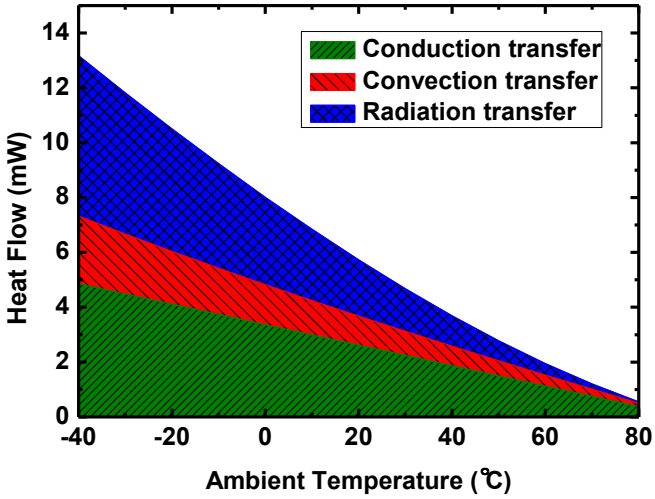


Figure 2.31. Heat flow due to conduction, convection, and radiation heat transfer across ambient temperature range of -40 to 80 ℃ (with an oven-set temperature of 90 °C).

Another adverse effect is the temperature non-uniformity across different devices and the RTD on the platform. Convection and radiation induces heat loss internal to the whole structure, and such heat loss cannot be avoided by using thermal isolation legs. The heat loss from convection and radiation creates temperature gradient within the active area. As the high-*Q* MEMS resonator in this work employs long and narrow supporting tethers to reduce anchor loss (Figure 2.32), the large thermal resistance of these tethers makes it harder to balance the temperature between the resonator body and the rest of the platform. A more realistic study should also consider the working condition of a MEMS resonator. When a MEMS resonator is operated in a reference oscillator or as a resonant sensor, it is beneficial to apply high driving power to the resonator to improve the phase noise. Figure 2.33 plots the simulated temperature distribution within the platform using COMSOL FEM when a heater power of 4.3 mW is applied to the Pt heater to heat up the platform when ambient temperature is 233 K. As shown in Figure 2.33, one of the fused silica resonators on the platform is operated in an oscillator and is sustaining a driving power of 400 μW. The body of the vibrating resonator is heated up when connected in an oscillator circuit, and a higher temperature on the resonator is observed. The vibrating resonator has a high power density of 16×10^6 W/m^2. Such self-heating effect is more pronounced in miniature MEMS resonators than in conventional devices with macroscopic scales. On the other hand, the other resonators left static show lower temperature than the outer boundary (Figure 2.33). As can be observed in Figure 2.33, the resonators on the platform experience large temperature

offsets compared to the region where the on-chip RTD is placed. Therefore, it is very difficult for the RTD to accurately sense the real temperature of all devices.

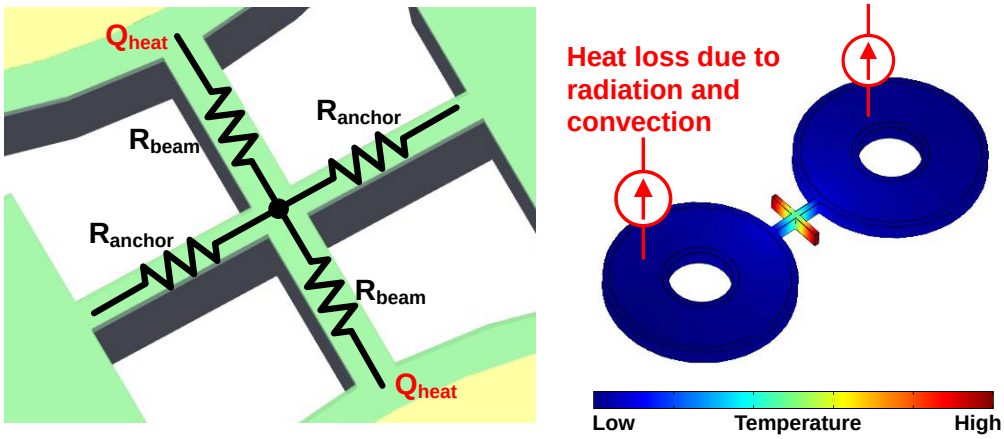


Figure 2.32. Left: Long and narrow anchors of the resonator introduce large thermal resistance; Right: Heat flow on the resonator body creates temperature difference between the resonator body to external boundary.

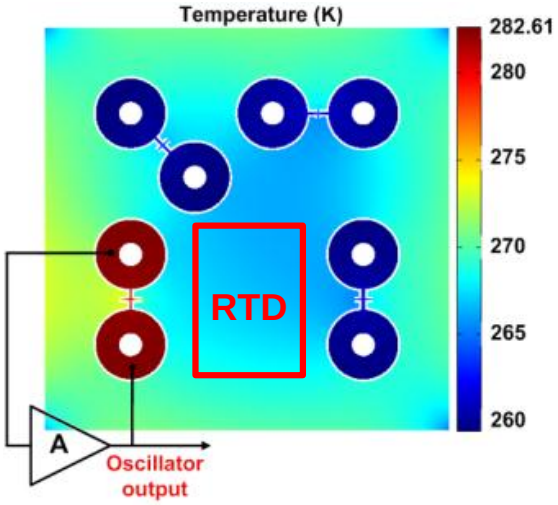


Figure 2.33. Temperature distribution of the active area with a heater power of 4.3 mW and a resonator driving power of 400 μW (in an oscillator loop) at an external temperature of 233 K.

2.2.4.3 Temperature Controller for Ovenized MEMS

For active temperature compensation, a *servo*-control system is implemented to monitor the RTD response and generate a feedback heater control signal. The performance of a conventional analog servo-control system is studied. As shown in the circuit schematic in Figure 2.34, the RTD is connected in a Wheatstone bridge configuration along with three other low-temperature coefficient of resistance (TCR) and precision resistors. The RTD and other resistors have a nominal resistance of approximately 7 kΩ. The Wheatstone bridge is biased with a stable voltage reference (V_B) of 1.2 V and interfaced to an instrumentation amplifier (IA) for pre-amplification. The IA (AD8553) provides a very low input offset voltage of 20 μV and a high voltage gain of 10,000. Having an RTD with measured TCR of 0.26%, the low IA input offset voltage translates to a temperature sensing error of 13 mK. The signal generated from the IA is filtered to reduce the noise bandwidth and increase the signal to noise ratio. The heater driver is implemented using an analog square-root generator based on BJT translinear circuits [65], as shown in Figure 2.35. The square-root generator linearizes the transfer function from the input control voltage to the output heater power. Figure 2.36 plots the normalized power gain versus input voltage of the square-root generator extracted from measurement. Compared to an earlier work that employed a linear amplifier to generate a heater current proportional to the sensor signal [66], the heater driver design in this work ensures a near constant thermal loop gain across a wide input range. Therefore, a sufficient thermal loop gain can be ensured even at low heater power levels. Using the square-root driver, the oven temperature can be set close to the

maximum working temperature without degrading the control performance, thus minimizing the power consumption of ovenization.

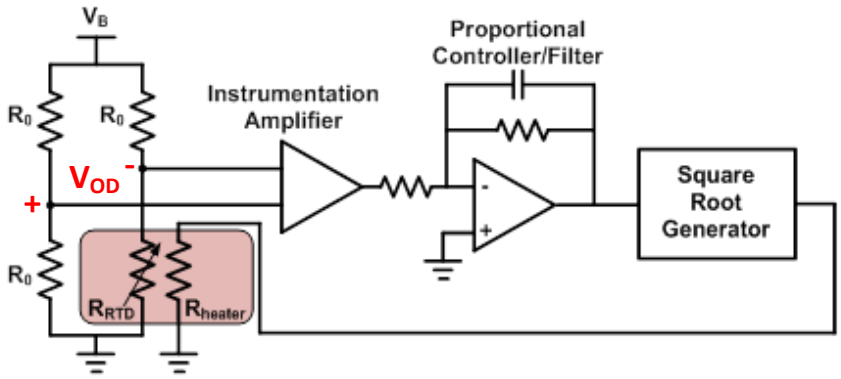


Figure 2.34. Circuit schematic of the resistive temperature detector (RTD) interface and analog oven-control system.

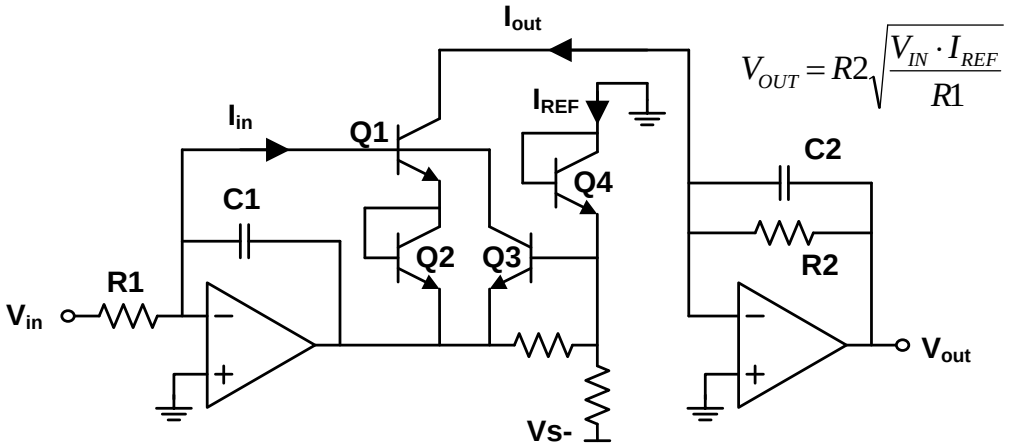


Figure 2.35. Circuit schematic of the square-root generator as the heater driver.

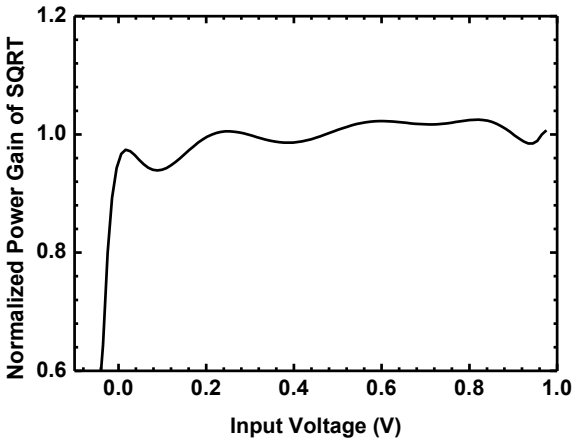


Figure 2.36. Normalized power gain vs. input voltage of the square-root generator.

The temperature stability of a resonator on the platform (Resonator I in Figure 2.28) is measured over external temperature changes. During temperature measurements, the fused silica die is mounted in a package (Figure 2.37) and placed in a vacuum chamber with pressure of less than 10 mTorr. The chamber temperature can be set to any value between 7 K and 400 K with +/-0.1 K accuracy. While the analog temperature controller is used to provide a *servo*-control, the frequency drift of the resonator is monitored using a network analyzer, and the results are plotted over a chamber temperature of -40 ℃ to +75 ℃ in Figure 2.38. Using oven-control with a thermal loop gain of ~1900, the effective TCF of the fused silica resonator has been reduced to +10 ppm/K, as compared to +89 ppm/K for an uncompensated silica resonator. Although the active compensation has reduced the uncompensated TCF of a fused silica resonator by almost an order of magnitude, a significantly smaller drift is expected due to a large thermal loop gain of the servo-control system design. Yet, there is an overall frequencies drift of 1163 ppm over -40 ℃ to +75 ℃. This is mainly due to the temperature gradient within the active area as

analyzed in the previous section. Since the temperature sensor (RTD) is not sensing the true resonator temperature, further increase in the thermal loop gain is ineffective in improving the temperature control accuracy (comparing the results with loop gain of ~5,000 against loop gain of 1,900 in Figure 2.38).

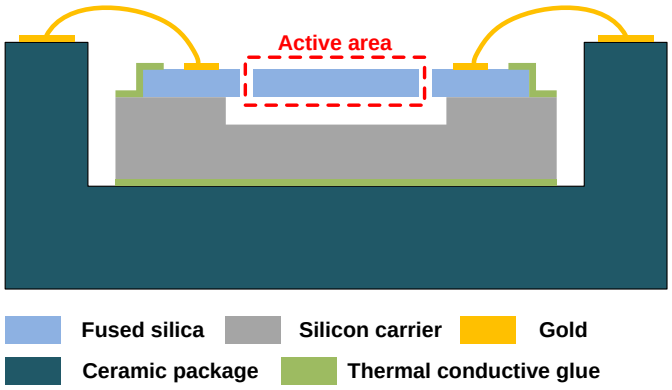


Figure 2.37. Cross-sectional view showing the fused silica die mounted in a ceramic package for temperature stability measurement.

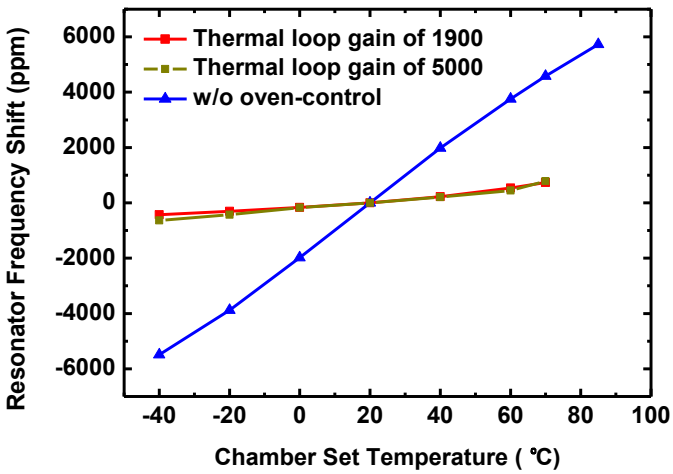


Figure 2.38. Measured effective TCF of the ovenized silica resonator compared to that of an uncompensated fused silica resonator. As shown, increasing the thermal loop gain does not improve the effective TCF due to the offset between the actual temperature of the resonator and the temperature sensed by the RTD.

The RTD-based temperature compensation method mainly suffers from offset errors due to a non-uniform temperature distribution in the active area. The offset error can be compensated using digital calibration in the temperature controller design; as plotted in Figure 2.39, after the RTD response is pre-amplified and filtered, the output voltage is digitized for further processing. A digital calibration table is used to store the offset errors across the RTD output range. After the data is converted back to the analog domain to generate a heater control signal, the offset errors are effectively removed in the *servo*-control system. The square root function from control voltage to heater driver voltage can also be performed in a digital calibration look-up table to simplify the analog implementation. In characterizing the properties of the control system, the MEMS resonator is connected in a continuously running oscillator loop so that the self-heating effect is also considered. This reflects the real working condition of an integrated MEMS clock in the fused silica device-fusion platform.

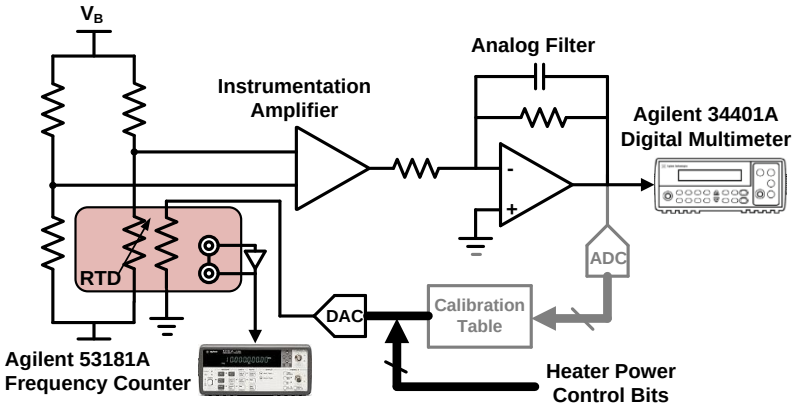


Figure 2.39. Circuit schematic of the RTD interface and oven-control system with digital calibration to reduce sensor offset.

During measurements, the temperature control system is operated by setting the control bits (instead of using closed-loop operation) to control the heater power for stable oscillator output. Meanwhile, the output frequency of the MEMS oscillator is monitored using a frequency counter. The output voltage from the RTD is also monitored using a digital multimeter (Figure 2.39). From the sensor output voltage measurement, the resistance change of the RTD is back calculated. This time, the oven-set temperature for the silica platform is ~ 70 ℃.

During measurements, the heater power is controlled digitally to stabilize the output frequency of the MEMS oscillator. The frequency drift of the oscillator is plotted in Figure 2.40 over the chamber set temperature of -40 ℃ to +65 ℃. The overall frequency drift of the oscillator has been reduced to 11 ppm. The output voltage from the RTD front-end is also recorded, and the extracted RTD resistance change is plotted in Figure 2.40. It can be seen that the RTD resistance increases at lower chamber temperature. This indicates the RTD is experiencing a temperature increase at lower external temperature, if the system tries to stabilize the oscillator frequency. Therefore, an upper shift of the heater control voltage needs to be performed in the digital calibration table for stabilizing the oscillator frequency, as plotted in Figure 2.41. The difference in the heater control voltage shown in Figure 2.41 is what needs to be calibrated and stored in the look-up table during the initial calibration process. The power consumption of the heater is plotted in Figure 2.42.

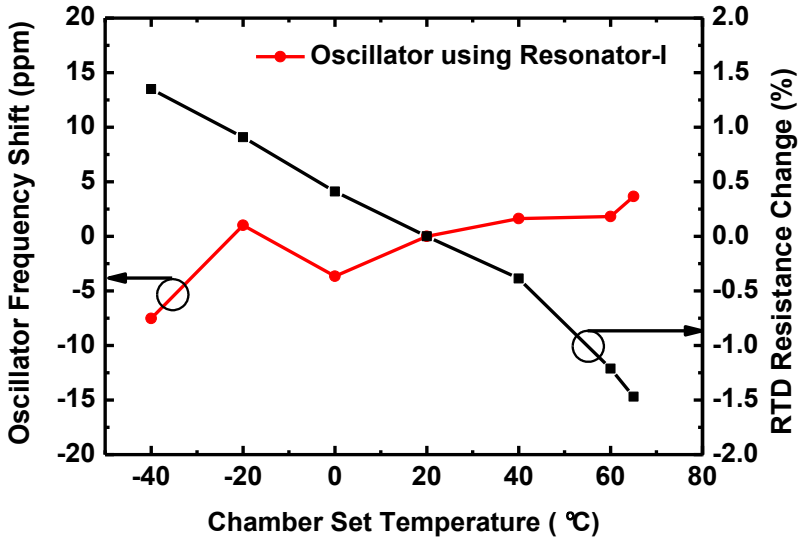


Figure 2.40. Frequency drift of the MEMS oscillator using Resonator I on the platform with controlled heater power to maintain a stable oscillator frequency (RTD resistance change is plotted).

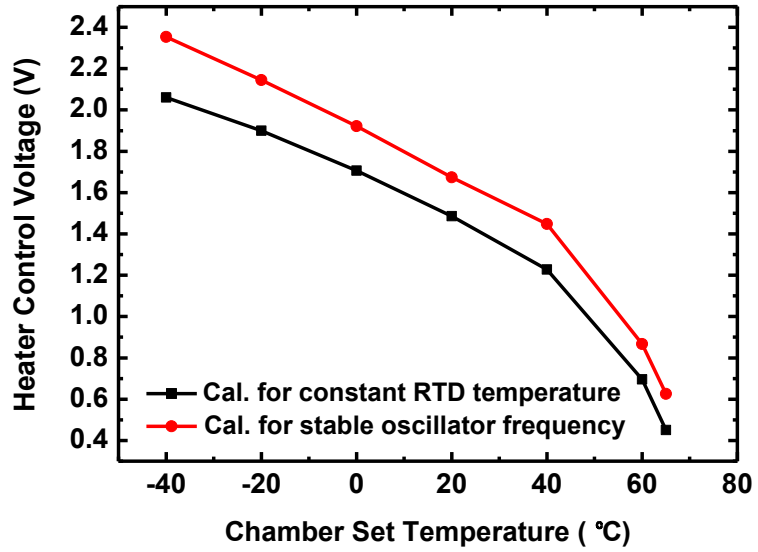


Figure 2.41. Heater control voltage calibrated for constant RTD temperature and stable oscillator frequency over chamber temperature range.

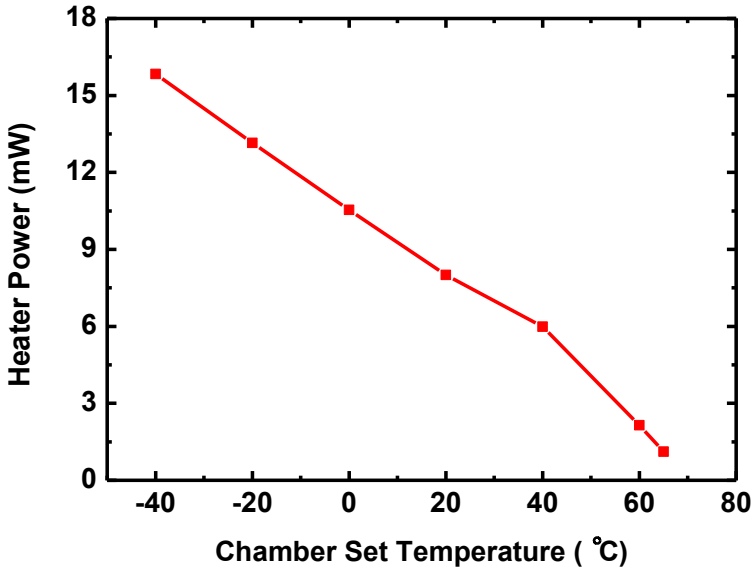


Figure 2.42. Extracted power consumption of the heater vs. chamber set temperature to stabilize the MEMS oscillator.

2.2.4.4 Challenges in Realizing Ultra-stable Integrated Timing

The resistive sensor interface is implemented using a Wheatstone bridge in Figure 2.34. The small-signal gain (sensitivity) of the Wheatstone bridge is a differential voltage output (V_{OD}) over the resistance change in the RTD (ΔR_{RTD}),

$$G_{bridge} = \frac{V_{OD}}{\Delta R_{RTD}} = \frac{V_B}{4R_0}. \tag{2.40}$$

In the temperature controller of this work, off-chip resistors with high precision and low TCR are used. However, if the temperature controller is designed using integrated circuits, CMOS on-chip resistors have much larger component variation and TCR. The process-voltage-temperature (PVT) variations in R_0 causes additional offset errors in temperature sensing, and the offset errors can drift over operating conditions. The bias

voltage (V_B) comes from an on-chip bias generator, and the circuit is also susceptible to PVT variations. Although a CMOS instrumentation amplifier can be designed with very low offset voltage (<10 μV) using auto-zeroing techniques, the offset effects coming from the Wheatstone bridge (in front of the amplifier stage) cannot be mitigated by a high-gain instrumentation amplifier.

Although digital calibration can be performed to remove the offset errors in temperature sensing, a fixed-point calibration is only effective if the offset is repeatable over changes in working conditions. However, ovenization on a fused silica device-fusion platform only ensures the MEMS devices are in a well-controlled and repeatable thermal condition. If the circuits are not ovenized with MEMS in a same miniature vacuum package, changes in external temperature conditions and thermal transient processes will induce unpredictable temperature gradients between the MEMS devices and the circuits. As the resistive temperature sensor and the analog interface are susceptible to PVT-induced errors, the achievable accuracy in temperature control will be ultimately limited by the unrepeatable offset errors.

2.3 Summary

In this chapter, an AlN thin-film process and DRIE of fused silica are combined to fabricate piezoelectric-on-silica MEMS resonators. Limitations in the fused silica fabrication process are discussed. Design techniques for realizing high-Q fused silica MEMS resonators are investigated given the fabrication limitations. A piezoelectric-on-silica MEMS resonator is demonstrated, showing a high Q at low megahertz regime and excellent motional resistance, making it a good candidate as a miniature frequency

reference. Further, a low phase noise MEMS oscillator is implemented based on the silica MEMS resonator. To our best knowledge, this is the first demonstration of a CMOS oscillator directly interfaced to a fused silica MEMS resonator. The low vibration sensitivity from the measured MEMS oscillator proves the potential of using the silica MEMS frequency reference in dynamic platforms. The frequency tuning techniques of the MEMS oscillator are also investigated for compensating initial frequency errors or frequency drifts over working environment. A piezoelectric tuning technique is proposed for realizing ultra-high resolution frequency tuning using a simple circuit. To overcome the high TCF of silica resonators, temperature-stable operation is realized using ovenized-MEMS technique. Targeting device-fusion capability, a thermal isolation platform is implemented for integrating multiple devices on a single-layer device-fusion platform. The high thermal isolation property of the fused silica platform enables low-power ovenization. Temperature sensing and closed-loop *servo*-control is further demonstrated by using an on-chip RTD. The thermal properties of a large MEMS platform are analyzed. The analysis reveals non-ideal effects using an on-chip RTD for temperature sensing. Calibration techniques to improve the performance of a conventional analog proportional controller are discussed. The results obtained in this chapter are the first steps towards implementing an integrated timing module using a silica-based MEMS resonator.

CHAPTER 3.

Two-Oscillator Temperature Sensing and Active Compensation Using a Phase-Locked Loop

In Chapter 2, the frequency drift of a silica MEMS oscillator is significantly reduced using a closed-loop oven-control system to stabilize the device temperature. It has also been discussed that an on-chip resistive temperature detector exhibits an offset error when it is used to sense the resonator temperature.

In this chapter, a passive TCF-compensation technique applied to a MEMS resonator is combined with active compensation to further improve the frequency stability of the oscillator. As a proof-of-concept, silicon MEMS resonators and oscillators are developed. Due to the intrinsic TCE of silicon, the linear TCF of an uncompensated silicon MEMS resonator is approximately -30 ppm/K [67], which dominates the frequency drift of a silicon MEMS oscillator with temperature. By using an oxide-refill process, the TCF of a silicon MEMS resonator can be significantly reduced and the large 1^{st}-order TCF can be cancelled [45]. With passive TCF compensation, silicon MEMS resonators have been shown with an overall frequency drift within 200 ppm over -40 ℃ to 80 ℃ [45], [67], [68]. Still, using this technique, the 2^{nd}-order TCF term of silicon is remained uncompensated, resulting in non-negligible frequency drift with temperature. In this

work, an active compensation method is exploited to further reduce the frequency drift of a MEMS oscillator over a wide working temperature range. The proposed active compensation method utilizes the intrinsic frequency drift of two MEMS oscillators for temperature sensing, and an ovenized MEMS platform is realized by *servo*-control using a CMOS PLL circuit. Even though silicon is used as the main structural material, excellent thermal isolation is obtained by employing oxide islands formed in the thermal isolation legs. The improved thermal isolation ensures low power consumption for ovenization.

3.1 Two-Oscillator Sensing and Oven-control using a Phase-Lock Technique

The working principle of the two-oscillator temperature sensing technique can be seen in Figure 3.1. Two MEMS resonators are fabricated on a single platform thermally isolated from the chip boundary (thermal-isolation platform). If properly designed, the temperature of the two resonators is nearly equal. One of the resonators is made of silicon and is not temperature compensated. The oscillator built using this uncompensated silicon MEMS resonator shows a TCF of ~-30 ppm/K. The other resonator is a silicon-silicon dioxide composite. The oscillator using this MEMS resonator with passive TCF-compensation exhibits a smaller frequency drift. As sketched in Figure 3.1, the two MEMS oscillators have different frequency drift characteristics as the temperature of the thermal-isolation platform changes. By comparing the output frequencies of these two MEMS oscillators, the temperature of the platform (*i.e.*, the temperature of the resonators) can be extracted. Such a temperature sensing method is based on frequency detection instead of resistance detection method (using an RTD). Active compensation on

the oscillator drift can be realized by open loop operation, for example, using a frequency-to-digital converter [69] to generate tuning bits to pull the MEMS oscillator frequency against temperature variations. Such a technique has also been successfully adopted in quartz crystal references, such as dual-mode micro-computer controlled crystal oscillators (MCXOs) [70]. Another way of active compensation uses closed-loop operation [66], [71]. In order to build a closed-loop system for active compensation, the error signal for feedback control can be extracted from the frequency difference between the two MEMS oscillators. Using negative feedback, the system autonomously locks into the oven-set temperature, where the two oscillators have the same frequency output (Figure 3.1). With such a *servo*-control loop, the frequency outputs of the two oscillators are stabilized at the oven-set point regardless of external temperature variations. In this work, the closed-loop compensation method is adopted for realizing ovenized MEMS oscillators. The ovenization technique stabilizes the frequency of the MEMS oscillators. In the meantime, the temperature of the thermal-isolation platform is stabilized and thus the platform can further include other devices (such as gyroscopes and accelerometers) requiring temperature-stable operation.

As can be seen in Figure 3.1, the proposed oven-control system is in fact implemented by phase-locking two MEMS oscillators (through a phase detector) instead of locking the frequencies. So, the control system is a PLL working in both electrical and thermal domains. With this implementation, nice features of a PLL are fully exploited. The first benefit comes from the fact that frequency is the first derivative of phase ($f=\mathrm{d}\varphi/\mathrm{d}t$). Non-ideal circuit behaviors, such as offset in amplifiers, circuit delay, finite

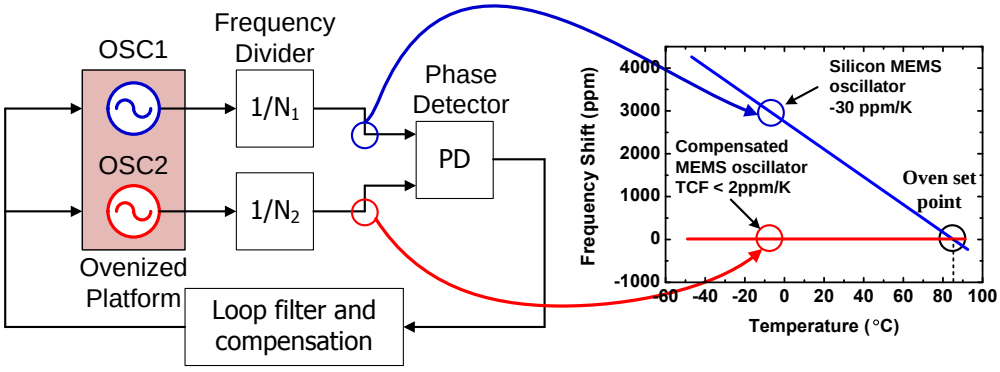


Figure 3.1. Principle of using two oscillators for temperature sensing and oven-control: two MEMS oscillators show different temperature coefficient of frequency (TCFs); the temperature of the resonators and the thermal platform is designed to be locked to the oven set point where two oscillators have identical frequency.

rise/fall time in digital logics, and temperature-induced variations, only induce a static phase offset between the two oscillators. However, a static phase offset does not result in frequency error if the PLL is locked. By contrast, temperature sensing using an RTD is prone to sensing error if the front-end amplifier or the bias generator has an offset. The second benefit comes from the fact that high-*Q* resonators are naturally suitable for implementing high-resolution sensors. A high-*Q* resonator provides a reliable frequency reference for a resonant sensor, and the oscillator frequency is insensitive to undesirable circuit variations, *e.g.* drift of gain, resistance, capacitance, and voltage reference over process-voltage-temperature (PVT) variations. On the other hand, the intrinsic frequency drift in the resonator due to variations in the measurand can be easily detected from the oscillator frequency output. Using MEMS technology, a resonant sensor can be designed with miniature size, and the resonator can be integrated with other MEMS devices for sensor fusion or with ICs in a heterogeneous platform. If a PLL-based compensation

method is used, the stability of the system relies more on the intrinsic properties of the MEMS resonators on a thermal-isolation platform instead of the precision of circuits. It is expected that with a proper design of MEMS devices, MEMS oscillators using PLL-based ovenization can achieve high temperature stability without any need for system-level calibration.

3.2 Fabrication Process for MEMS Resonators and Thermal Isolation Platforms

For passive or material-based TCF compensation, the use of a material with an opposite TCE has been proved effective. It has been observed in Chapter 2 as well as other reported works [45], [67], [68] that a MEMS resonator fabricated using silicon dioxide (*i.e.* fused silica) has a large linear positive TCF, opposite to the negative TCF in silicon resonators. In order to realize a TCF-compensated resonator, a silicon MEMS resonator can include silicon dioxide trenches or islands to make a device with composite material. Efficient temperature compensation on silicon resonators can be achieved by utilizing oxide-refilled trenches in areas of high strain energy density [45], which minimizes oxide material deposition and Q degradation.

As for thermal properties, silicon dioxide has very low thermal conductivity (1.3 W $m^{-1}K^{-1}$). The oxide islands used for passive TCF-compensation can also be utilized for thermal isolation. Including oxide structures in the isolation legs overcomes the difficulty in designing high thermal resistivity legs using only silicon material, which has a much higher thermal conductivity (131 W $m^{-1}K^{-1}$).

The fabrication process flow is sketched in Figure 3.2. The fabrication starts with a 4-inch silicon-on-insulator (SOI) wafer with a 20-μm-thick high-resistivity (> 1000 Ω·cm)

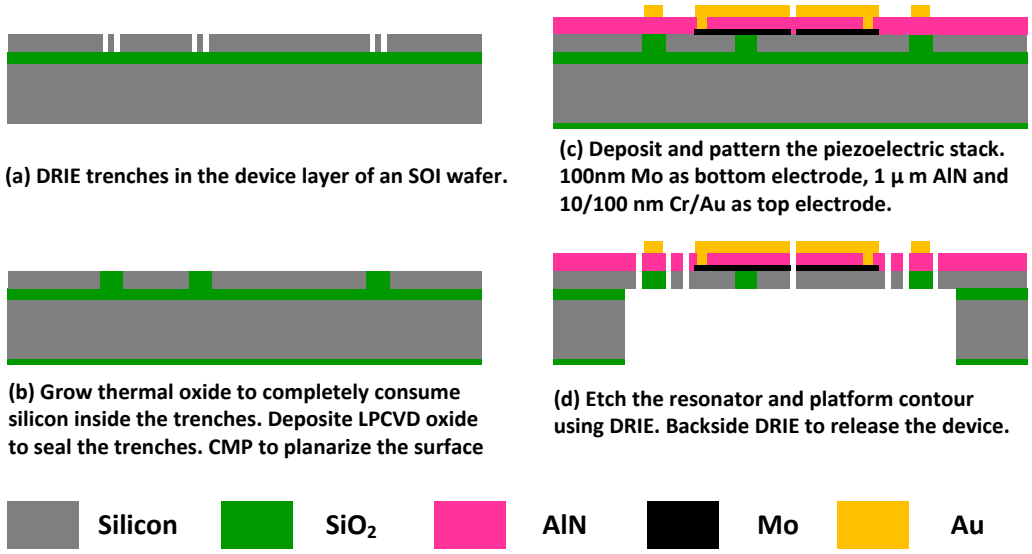


Figure 3.2. Process flow for fabricating AlN-on-silicon resonators with passive TCF compensation and thermal isolation structures using a SOI wafer.

silicon device layer. The process steps are described as follows: (a) High-aspect-ratio trenches are etched using DRIE. These trenches are subsequently refilled by growing 2.5 µm of thermal silicon dioxide at 1200 °C. In order to ensure that the silicon material within the thermal isolation structures are completely transformed to silicon dioxide, the DIRE trenches are etched down to the buried oxide layer used as an etch-stop. (b) The wafer surface is planarized using an oxide chemical–mechanical polishing (CMP) process to ensure a smooth and flat finish. A smooth surface is essential for the reactive sputtering of high-quality AlN with low stress and vertical c-axis orientation. (c) After CMP, 100-nm-thick Mo is deposited and patterned as the bottom electrode. A 0.5-µm-thick low-stress AlN piezoelectric thin-film layer is subsequently deposited using reactive sputtering. A Cr/Au (10 nm/100 nm) layer is evaporated and lift-off patterned as the top metal. (d) Geometries of the MEMS devices and thermal platforms are defined by plasma

etching the AlN thin-film layer and subsequently DRIE of the silicon device layer. Finally, the device is released by backside DRIE of the silicon handle layer and dry etching of the buried oxide layer. The SEM images of two fabricated silicon MEMS platforms are shown in Figure 3.3. Each platform integrates two MEMS resonators and a built-in heater. The active area of a platform which contains MEMS resonators is supported by four thermal isolation legs. A cross-sectional view of the oxide refill structures fabricated using this process is shown in Figure 3.4.

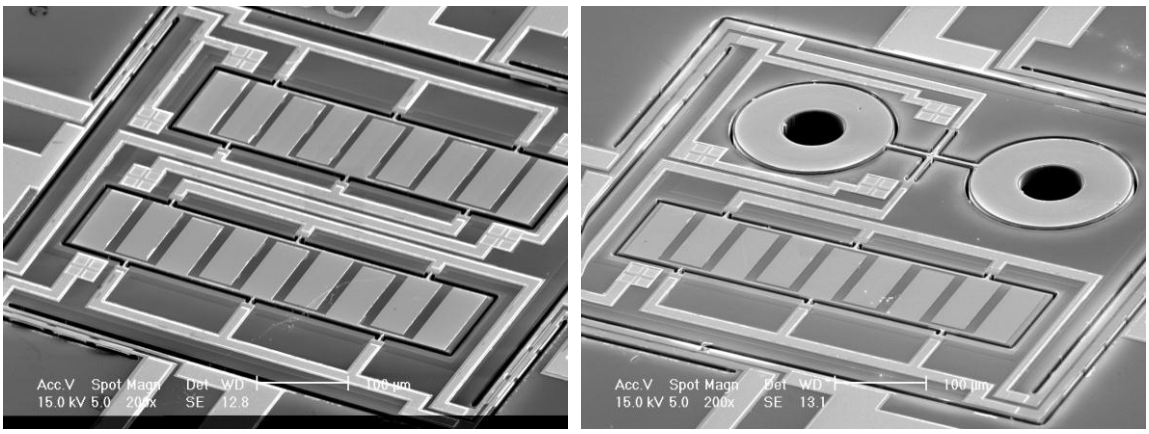


Figure 3.3. SEM images two silicon MEMS platforms fabricated using the process.

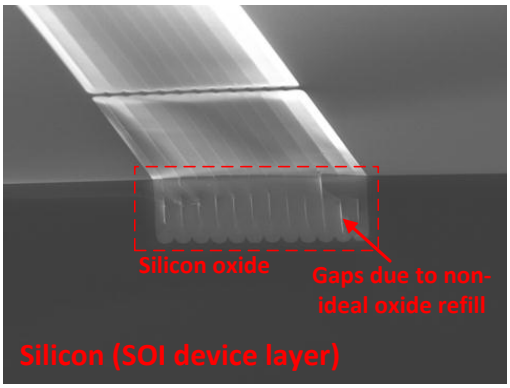


Figure 3.4. Cross-section SEM of an oxide island formed using the process.

3.3 MEMS Resonator Design

3.3.1 80 MHz Length Extensional Mode Resonators

The PLL-based active compensation scheme requires two MEMS resonators with different TCFs for building oscillators. Both an uncompensated and a TCF-compensated resonator are fabricated on the platform using the developed MEMS process. In order to implement MEMS oscillators with low phase noise, the MEMS resonator designs are targeted for high Q, low motional impedance, and good power handling capability. For an uncompensated AlN-on-Si resonator, a high-order length extensional mode is used. As shown in Figure 3.5, a 9th-order length extensional mode bulk acoustic resonator (LBAR) is designed. Due to the use of a high-order extensional vibration, multiple regions on the resonator body can store high strain energy during vibration, leading to high total strain energy during vibration. The supporting tethers are placed on the nodal points of the vibrating device, which minimizes anchor loss of the resonator. Six tethers are used to provide a robust anchor. The electrode configuration for single-ended input/output operation of the LBAR is sketched in Figure 3.5. There are in total nine electrodes patterned on the top metal layer, and the electrodes cover the high stress regions for picking up the electric signal through transverse piezoelectric coupling (d_{31}) of AlN.

The measured frequency response of the LBAR near the 80 MHz 9th-order extensional mode is shown in Figure 3.6. Using multiple electrodes to improve signal pick up, the resonator exhibits a low insertion loss of 8.6 dB. The extracted motional impedance is 94 Ω. The measurement Q_U of this vibration mode is 9,885.

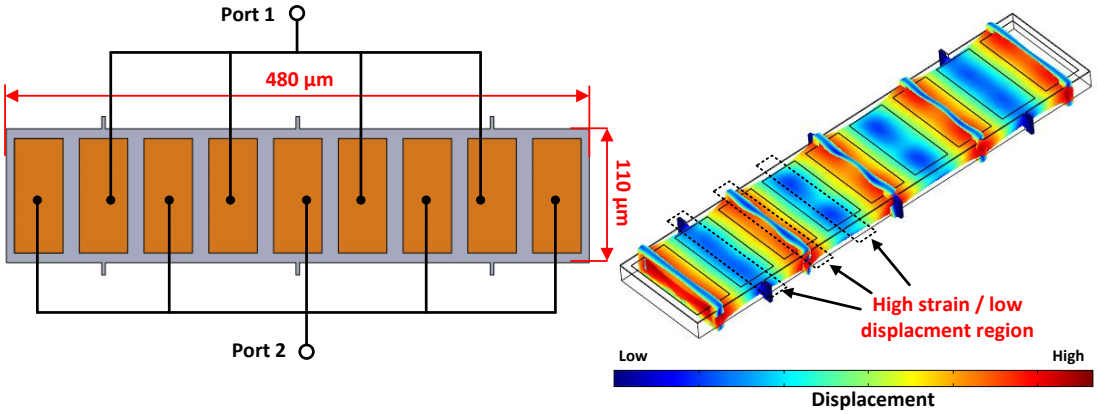


Figure 3.5. Left: Geometry of an 80 MHz 9th-order LBAR; Right: mode shape of the resonator.

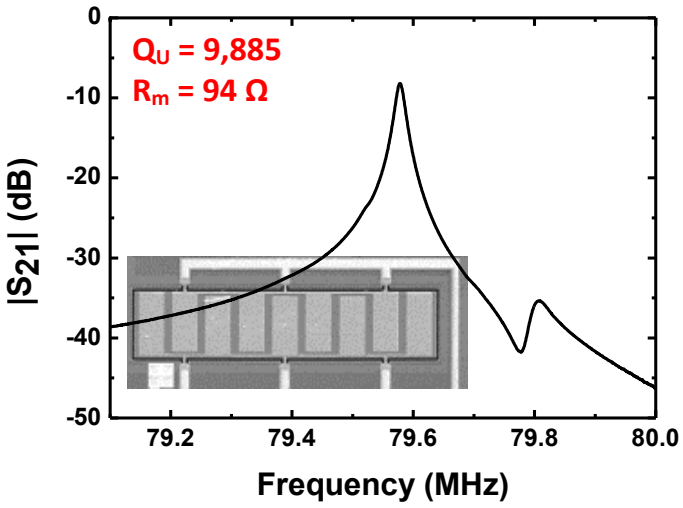


Figure 3.6. Measured response of a 9th-order LBAR without TCF compensation (inset shows the SEM image of the fabricated resonator).

The strain profile of an LBAR can be further exploited for passive TCF compensation. For the 9th-order length extensional mode resonator, high strain regions on the resonator body can be identified in Figure 3.7. By placing oxide islands in the high

strain regions, the resonator TCF can be reduces. Also, as the high strain regions are concentrated in specific regions (Figure 3.7), only narrow oxide-refill trenches are needed to fully compensate the negative TCF of silicon. The oxide trench dimensions used for TCF-compensation are denoted in Figure 3.7. The volume of the oxide trenches occupies only 10 % of the total resonator volume.

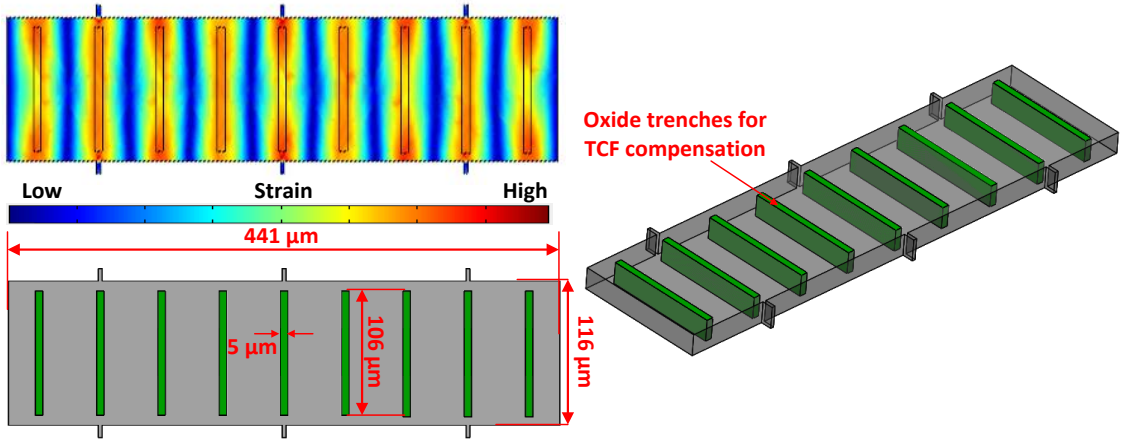


Figure 3.7. Geometry sketch, strain profile of the 9th-order length-extensional mode, and the oxide trenches used for TCF compensation (shown in green).

The measured response of the TCF-compensated LBAR is shown in Figure 3.8. A 9th-order extensional mode is captured near 78.55 MHz. The TCF-compensated resonator exhibits a high Q_U of 11,601 and a low motional impedance of 58 Ω. The measured TCF of the device is shown in Figure 3.9. With the oxide-refill geometries used in the design, the compensated LBAR shows a positive TCF of +4 ppm/K when the resonator is operated near a desired oven-set temperature of ~85 °C. The extracted turn-over temperature (zero-TCF point) is near 150 °C. The measured results indicate that the resonator TCF is over-compensated in the target working temperature range. The over-

compensation was expected due to the trench widening seen in the oxide trench patterns during the mask fabrication as well as the non-ideal silicon DRIE process. Further optimization on the oxide patterns and better control on the fabrication parameters are required in order to obtain a turn-over point at the desired oven-set temperature.

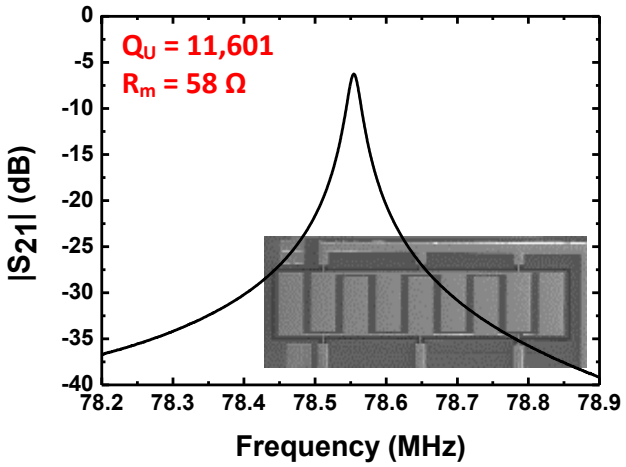


Figure 3.8. Measured response of a TCF-compensated 9th-order length extensional mode resonator (LBAR) (inset shows the SEM image of the fabricated resonator device).

The measured wideband responses of both the uncompensated and TCF-compensated LBARs are shown in Figure 3.10. It can be seen that the only strong resonance peaks captured in the $|S_{21}|$ responses are the main vibration modes near 80 MHz, and both resonators are free from strong spurious modes. If electrical oscillators are designed using the LBAR devices, no electrical filtering in the circuit is necessary to reject spurious resonances.

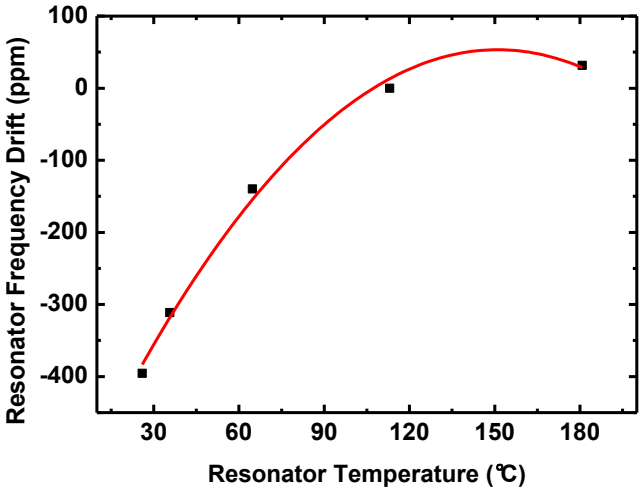


Figure 3.9. Measured frequency drift of the TCF-compensated 80 MHz LBAR versus device temperature (fitted to a 2nd-order polynomial curve).

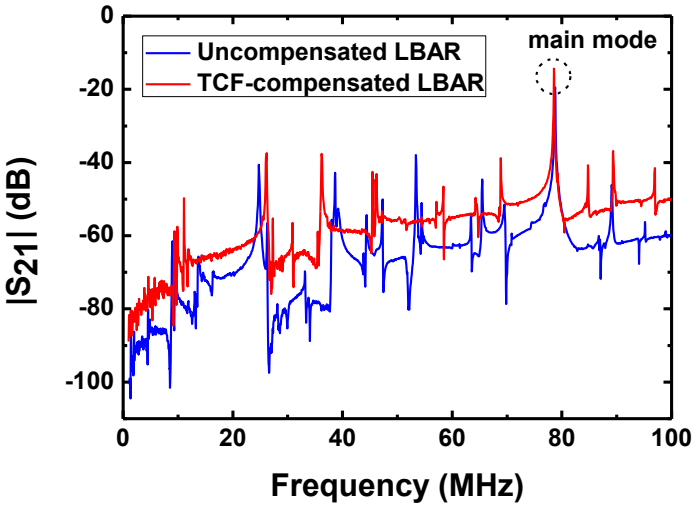


Figure 3.10. Wideband responses of the uncompensated and TCF-compensated LBARs.

3.3.2 20 MHz TCF-Compensated Radial Extensional Mode Resonators

The coupled-ring resonator design mentioned in the previous chapter can also be TCF compensated using a similar technique (Figure 3.11) [72]. Oxide islands can be placed

inside the bodies of the two vibrating rings. By changing the spacing between the oxide island and the resonator boundary, the turnover temperature can be controlled [72]. The geometry of the oxide islands used in this work is also marked in Figure 3.11. The measured response of a TCF-compensated coupled-ring resonator is plotted in Figure 3.12, showing a resonance mode near 19.2 MHz. This TCF-compensated coupled-ring resonator exhibits a Q_U of 7,354 and a motional impedance of 443 Ω. The extracted TCF of the resonator is +5 ppm/K near the desired oven-set temperature, as shown in Figure 3.13. The turn-over temperature is near 190 °C, showing over-compensation of the TCF.

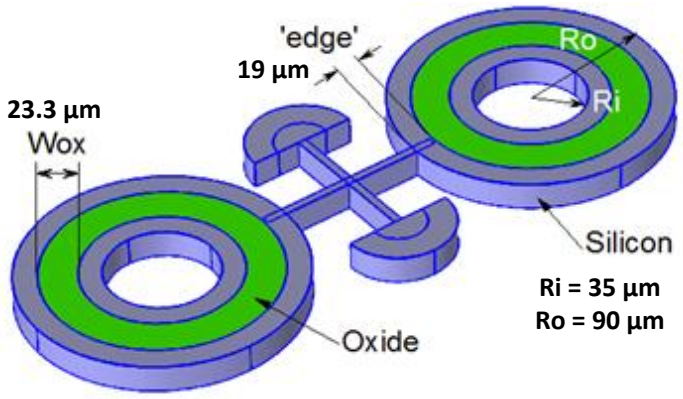


Figure 3.11. Schematic of a TCF-compensated coupled-ring resonator.

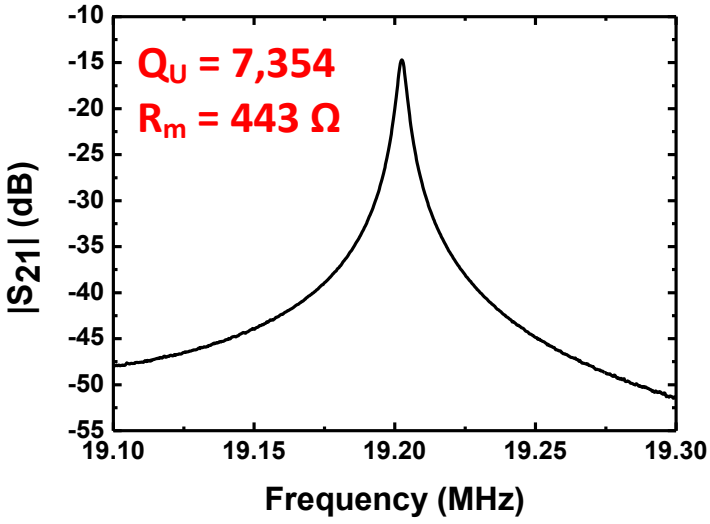


Figure 3.12. Schematic of a 19.2 MHz TCF-compensated coupled-ring resonator.

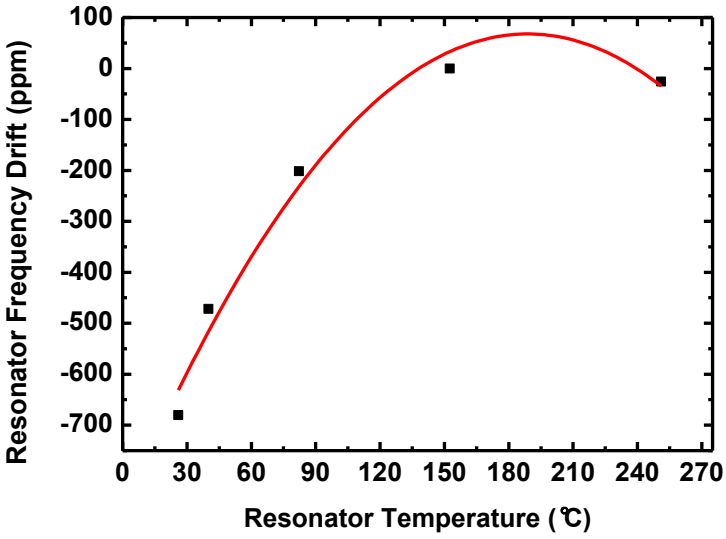


Figure 3.13. Measured frequency drift of the 19.2 MHz coupled-ring resonator versus device temperature (fitted to a 2nd-order polynomial curve).

3.4 Thermal Design for the Two-resonator Platform

3.4.1 Thermal Isolation Structure Design

As presented in Section 3.2, the fabrication process introduces a silicon etch and oxide-refill process that can selectively transform a thick layer of silicon in the SOI device layer to silicon dioxide. The oxide islands are placed in the thermal isolation legs. The top view of a silicon platform with thermal isolation legs is sketched in Figure 3.14. The regions in the supporting legs that are embedded with oxide islands are highlighted. The DRIE process on the silicon device layer is aligned to completely remove the silicon material on the sidewalls of the oxide islands. Therefore, the thermal isolation property of the supporting legs is determined by the large thermal resistance provided by the oxide structures. By employing oxide islands, the legs can be designed with sufficient stiffness to improve the robustness of the supporting structures, while good thermal isolation is still obtained. Also, the wide supporting legs allow routings of multiple low-resistance electrical connections using the top metal layer, which enables integrating multiple devices on the platform.

As thermal oxidation process is employed to fabricate the oxide islands, the residual stress after the high-temperature oxidation process is a concern. To relieve the effect of residual stress in the oxide islands, the supporting legs are designed using a crab-leg configuration (Figure 3.14). The oxide refill process can also introduce gaps or voids in the oxide islands due to non-conformal silicon dioxide growth (Figure 3.4), and the air voids can potentially cause cracks and degrade robustness. In order to improve robustness of the supporting legs, the long and narrow DRIE trenches for oxide-refill process are

designed with periodic patterns (shown in Figure 3.14). Between each adjacent column of DRIE trenches, a thin silicon strip is added to firmly link the adjacent oxide islands (Figure 3.14). Similar DRIE patterns have been used in a previous work [73] to improve robustness. Two variations of the thermal isolation legs are successfully fabricated. The dimensions of the isolation legs are sketched in Figure 3.14.

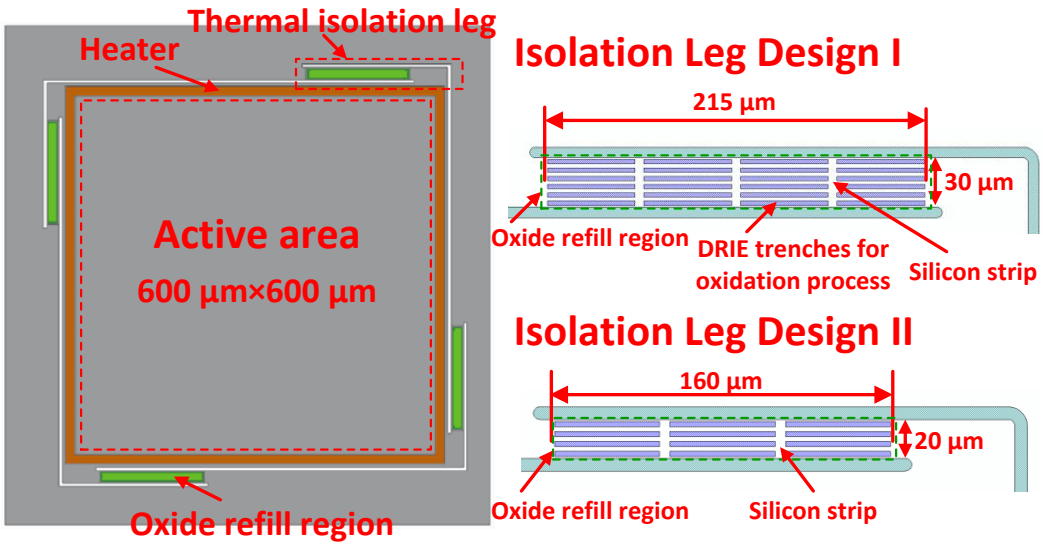


Figure 3.14. Schematic sketch showing the silicon platform with thermal isolation legs; geometries of two thermal isolation leg designs are provided, with DRIE patterns of the silicon device layer for oxidation and trench refill.

The analysis on the thermal isolation property of the silicon platform follows the procedures outlined in Section 2.2.4. The material properties used in thermal analysis are listed in Table 3.1. The geometries of the platform for analyzing the thermal properties are summarized in Table 3.2. Considering the typical working temperature of a MEMS frequency reference, it is assumed that the whole active area is heated to maintain an oven-set temperature of 90 ℃. Two assumptions are used for deriving the analytical

results: (1) Conduction transfer is only through the four thermal isolation legs of the platform (Figure 3.14). This assumption is reasonable as the thermal resistance of the isolation legs dominates in this design. (2) The surface area used for calculating convection and radiation transfer treats the whole active area as a box with the geometry given in Table 3.2. For the thermal isolation leg Design I (in Figure 3.14), the thermal resistances versus ambient temperature for conduction ($R_{th,cond}$), convection ($R_{th,conv}$), and radiation ($R_{th,rad}$) are plotted in Figure 3.15. In calculating convection heat transfer, air pressure of 5 mTorr, free molecular conductivity of 16.63×10^{-2} W m^{-2} K^{-1} mTorr^{-1} at 0 ℃, and accommodation coefficient of 1 are used to account for a MEMS chip in a hermetic packaging. In calculating radiation transfer, a radiation emissivity of 0.52 is used to account for the silicon material property. It can be observed in Figure 3.15 that the total thermal resistance (R_{th}) is dominated by the thermal resistance due to conduction transfer ($R_{th,cond}$). The total thermal resistance maintains a near constant value across ambient temperature. The heat flows due to conduction (Q_{cond}), convection (Q_{conv}), and radiation (Q_{rad}) are plotted in Figure 3.16. The total heat flow equals the power consumption needed to ovenize the silicon platform at the 90 ℃ oven-set temperature. The analysis in Figure 3.16 indicates a maximum power of less than 8 mW for ovenization. For the thermal isolation Design II in Figure 3.14, a slightly larger ratio of length over width is used in the oxide islands. As a result, Design II has slightly better thermal isolation property. If these results are compared to the analysis in Section 2.2.4 for a fused silica platform, it can be found that a device platform with a smaller surface area significantly reduces the heat loss due to convection and radiation transfer. With the

current silicon platform designs, the thermal resistance due to convection and radiation is approximately two orders magnitude higher than the thermal resistance due to conduction transfer. Therefore, there is still room to design more aggressive thermal isolation legs for further reducing the power consumption for ovenization. On the other hand, further enlarging the active area without significantly degrading the thermal resistance is possible. The prototype platform design can be further scaled to a larger size for integrating more MEMS devices.

Table 3.1. Material properties used in the thermal analysis for the silicon platforms.

	SiO_2	AlN	Si
Thermal conductivity ($W\ m^{-1}K^{-1}$)	1.3	160	131
Specific heat capacity ($J\ kg^{-1}\ K^{-1}$)	703	600	710
Mass density ($kg\ m^{-3}$)	2201	3260	2330

Table 3.2. Geometries of the silicon platforms and thermal isolation legs.

Thermal isolation legs (Design I) (L × W)	215 μm ×30 μm
Thermal isolation legs (Design II) (L × W)	160 μm ×20 μm
Material stacks of the oxide islands	AlN/SiO_2 (0.5 μm/19 μm)
Active region (edge ×edge ×thickness)	600 ×600 ×20 μm^3

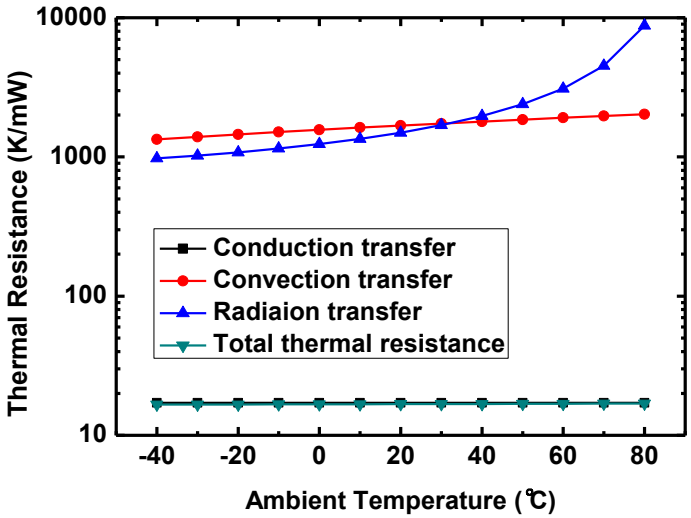


Figure 3.15. Thermal resistance due to conduction, convection, and radiation heat transfer for the silicon platform (using isolation leg Design I).

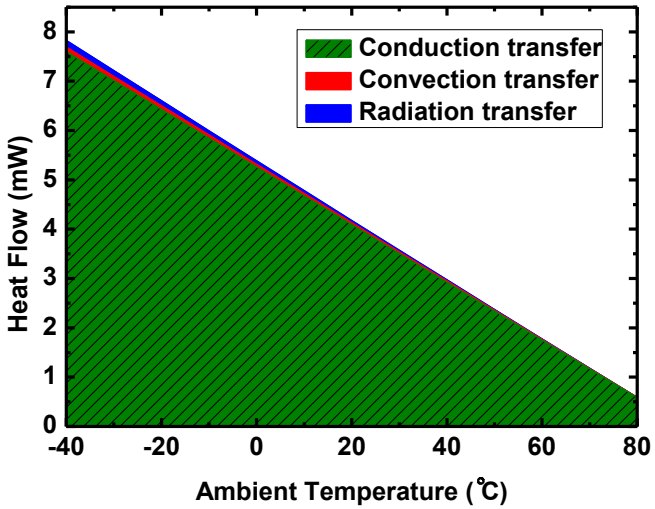


Figure 3.16. Heat flow due to conduction, convection, and radiation heat transfer across ambient temperature range of -40 to 80 ℃ (using isolation leg Design I).

The thermal resistances of the platforms are measured as following: a fabricated MEMS chip is mounted on a temperature-controlled chuck to maintain a fixed

temperature. Heating current is applied to the heater on the platform to raise the temperature of the active area, while the frequency shift of the uncompensated MEMS resonator on the platform is monitored using a network analyzer. Using the known TCF of the uncompensated silicon resonator (-30 ppm/K), the temperature of the active area can be extracted from the frequency shift of the silicon resonator. The temperature rise of the thermal platform versus the heater power for the two thermal isolation leg designs are obtained, and the measured results are plotted in Figure 3.17. The large thermal resistances extracted from the measured results prove good thermal isolation obtained, which enables low-power ovenization (< 10 mW). The small discrepancy between the measurement results and the analytical results mainly comes from the inaccuracy in material constants used in Table 3.1 and the assumptions made in the simplified analysis.

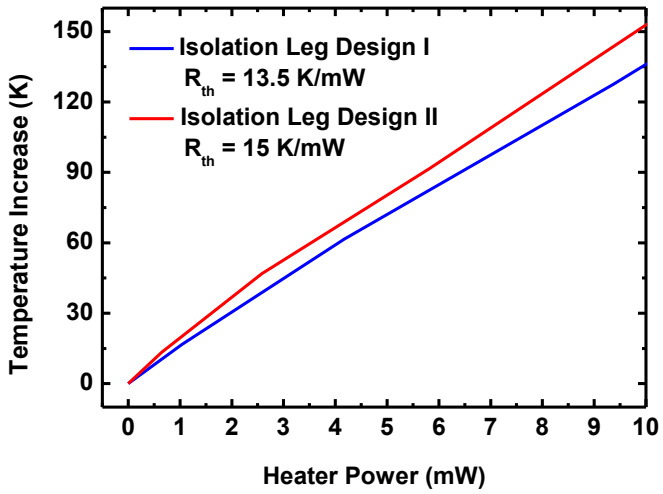


Figure 3.17. Temperature increase of the active area in the platform versus heater power extracted from measurement.

3.4.2 Equivalent Circuit for Thermal Model

The thermal analysis in the above section does not consider the properties of the MEMS resonators in the platforms. A more detailed thermal model for a two-resonator platform needs to be extracted for predicting both static and dynamic thermal performance. As heat transfer equations are analogous to circuit current-voltage equations, the thermal property can be modeled using an RC equivalent circuit as shown in Figure 3.18. In the equivalent circuit model, the thermal resistance introduced by the isolation legs of the platform is represented by a resistor, $R_{th,leg}$. The thermal resistance of the resonator tethers is represented by a resistor ($R_{th,RES1}$ and $R_{th,RES2}$ for the two resonators on the platform). Heat capacity (thermal mass) of a solid structure is modeled using a capacitor. In Figure 3.18, capacitor, C_{pl}, models the heat capacity of the large platform, and two capacitors, C_{RES1} and C_{RES1}, model the heat capacity of the MEMS resonators in the platform. The heat capacity of a device can be calculated from the material properties in Table 3.1

$$C = \rho V c_p, \tag{3.1}$$

where ρ is the mass density, and V is the volume of the device, C_p is the specific heat capacity the material.

The thermal model in Figure 3.18 uses a first-order RC network for modeling an individual structure. This model gives reasonable accuracy if: (1) the thermal resistance from the active area to the external boundary is dominated by the thermal resistance of the isolation legs; and (2) the thermal resistance that isolates a resonator from the

platform is dominated by the thermal resistance of the supporting tethers of the resonator. The first condition is satisfied as the platform is relatively small and is operated in vacuum. The second condition also gives reasonable results as the main body of both resonators is small and the conduction is the dominate heat dissipation mechanism. In Figure 3.18, heating power injected into the platform (*i.e.*, from the built-in heater for ovenization) and the resonators (*i.e.* due to self-heating of the resonators in a circuit) is modeled by current sources. Heat flows due to convection and radiation heat transfer are also included as current sources. The external temperature is modeled by a voltage source (T_{ext}) in Figure 3.18. In common situations, the detailed thermal model for the environment external to the platform (including external silicon chip, package, and board assembly, *etc*.) cannot be precisely defined. However, it is worth noting that the ovenized MEMS platform is a miniature structure with a total thermal capacity much smaller than the thermal capacity of external materials (including external silicon die, package, *etc*.). As a good approximation, the small heat flow through $R_{th,pl}$ to the external boundary cannot change the external temperature (T_{ext}).

It can be observed from Figure 3.18 that if the heat sources internal to the two resonators, including resonator self-heating (P_{drive1} and P_{drive2}), convection (Q_{conv1} and Q_{conv2}), and radiation (Q_{rad1} and Q_{rad2}) heat losses, are zero, the two resonators in the platform always maintain an equal temperature ($T_{RES1} = T_{RES2}$). As shown in the analysis in Section 3.4.1, the heat transfer due to convection and radiation is very minor for the silicon platform designs, and their effects can be neglected in the model. However, the resonators in oscillator circuits experience self-heating due to driving power applied on

the devices. If the thermal resistances of the resonators ($R_{th,RES1}$ and $R_{th,RES2}$) can be made very small, the temperature offset between T_{RES1} and T_{RES2} can still be minimized.

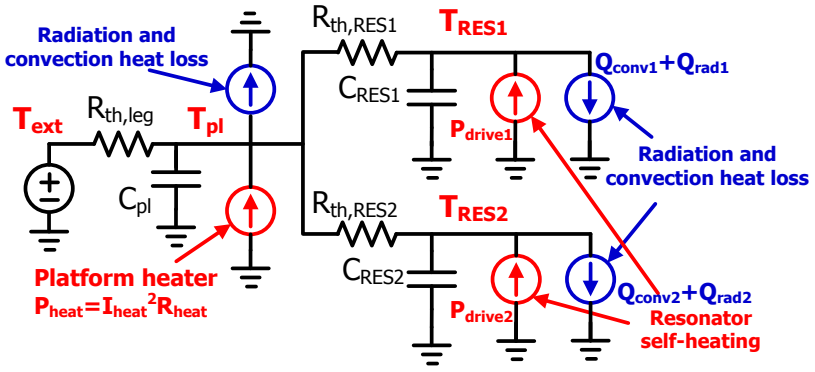


Figure 3.18. Equivalent circuit model for the thermal property of a silicon platform integrated with two MEMS resonators.

In order to analyze the linear transfer function of the PLL-based oven-control system, a simplified thermal model in Figure 3.19 is used. The non-ideal effects, such as resonator self-heating, will be discussed later. Two design variations of the silicon MEMS platforms are studied. In Platform-I, thermal isolation leg Design I (in Figure 3.14) is adopted. Two resonators are integrated on the platform, including a TCF-compensated coupled-ring resonator (RES1, Figure 3.11) and an uncompensated LBAR (RES2, Figure 3.6). In another design, Platform-II, the thermal isolation leg Design II (in Figure 3.14) is adopted. The resonators in the platform include a TCF-compensated LBAR (RES1, Figure 3.8) and an uncompensated LBAR (RES2, Figure 3.6). The elements in the thermal model for these two platform designs are extracted in Table 3.3. It can be found in Figure 3.11 that the coupled-ring resonator has a long anchor structure, which introduces a larger thermal resistance compared to the LBARs.

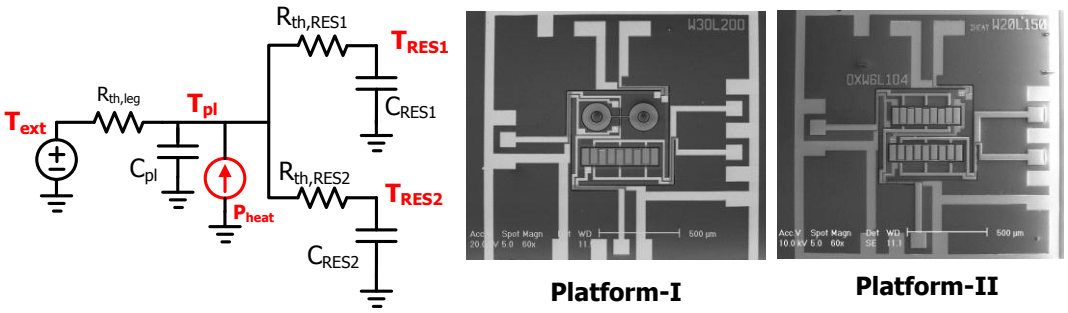


Figure 3.19. A simplified thermal model for platform design variations, including Platform-I and Platform-II.

Table 3.3. Extracted element values in the thermal equivalent circuits.

	Two-resonator Platform-I	Two-resonator Platform-II
Rth,leg (K/mW)	13.5	15
C_{pl} (J/K)	8.2×10^{-6}	8.2×10^{-6}
$R_{th,RES1}$ (K/mW)	2.7 (Ring)	0.24
C_{RES1} (J/K)	1.5×10^{-6}	1.8×10^{-6}
$R_{th,RES2}$ (K/mW)	0.24 (LBAR)	0.24
C_{RES2} (J/K)	1.73×10^{-6}	1.73×10^{-6}

3.5 PLL-based Control System Design for Ovenized MEMS

3.5.1 Control System Design

A linear model of the PLL-based oven-control system is sketched in Figure 3.20. In this model, temperature-induced frequency drift of two oscillators are modeled with coefficients, TCF_1 and TCF_2, respectively. The frequency dividers divide the frequencies of the oscillators by $1/N_1$ and $1/N_2$, respectively, so that two frequency inputs to the phase-frequency detector (PFD) are identical (f_{div0}) at the oven set-point, *i.e.*

$$f_{div0} = \frac{f_{OSC1}}{N1} = \frac{f_{OSC2}}{N2} \text{ (at the oven set-point).} \quad (3.2)$$

The PLL is a negative feedback loop that self-adjusts the frequencies of two oscillators to lock into the oven-set point. The phase-lock is achieved by heating the platform to an oven-set temperature. The PFD detects the phase difference between two divided-down frequencies from the oscillators, and the average voltage output from the PFD indicates the phase difference. As phase is the integration of frequency, the PFD acts an integrator in the control loop. Therefore, the PLL-based control loop is naturally a proportional-integral (PI) control system. The integrator from the PFD is modeled with 1/s in the Laplace domain. The loop filter performs filtering on the voltage pulses from the PFD output and extracts the average value. If the loop filter does not contain an additional integrator, the PLL is a Type-I PLL. On the other hand, if the loop filter is designed to have an additional integrator, the PLL becomes a Type-II PLL. The loop filter can also include compensation zeroes for improving stability and optimizing the performance of the control loop. The heater driver generates a heating current (I_{heat}) from the loop filter output voltage (V_{CTRL}), which is flowing into the metal heater on the silicon platform (in Figure 3.14). The Joule heating is modeled as a current controlled current source (CSCS) in the thermal domain. The heater driver is designed using a square-root generator to linearize the transfer characteristic from the control voltage (V_{CTRL}) to the heater power (P_{heat}). Using such design, the PLL can be treated as a linear control system, and the loop gain is near constant regardless of the operating point. As discussed in Section 3.4.2, the static and transient thermal properties are modeled using an RC network representing

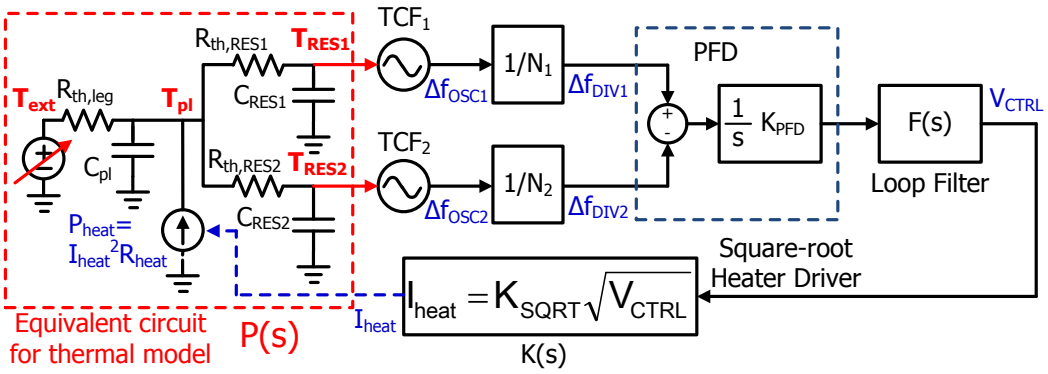


Figure 3.20. Linear model for the PLL using two MEMS oscillators for temperature sensing and oven-control.

thermal resistances and heat capacities of the devices in the platform. The platform is thermally isolated from the external boundary by a large thermal resistance ($R_{th,leg}$). As listed in Table 3.3, the thermal resistances of the resonators in the platform ($R_{th,RES1}$ and $R_{th,RES2}$) are relatively small. Also, the heat capacity of the MEMS platform (C_{pl}) is much larger than an individual MEMS resonator. Therefore, the thermal pole at lowest frequency in the PLL comes from the thermal time constant of the large platform, and it can be identified as

$$\omega_{p,pl} = 1/\left(R_{th,leg} \cdot C_{pl}\right). \tag{3.3}$$

According to Table 3.3, other thermal poles from two MEMS resonators, $\omega_{p,RES1}=1/(R_{th,RES1}\cdot C_{RES1})$ and $\omega_{p,RES2}=1/(R_{th,RES2}\cdot C_{RES2})$, are at ten times to a hundred time higher frequencies than $\omega_{p,pl}$. This also indicates that the resonator temperature can track the variations in the temperature of the silicon platform. Therefore, oven-control on the

platform can also stabilize the resonators inside. As the thermal pole, $\omega_{p,RES1}$, is not equal to $\omega_{p,RES2}$, the transfer function of the heater power (P_{heat}) to the temperature of the two resonators (T_{RES1} and T_{RES2}) experience slightly different thermal lags. In the PLL-based oven-control system design, the unity-gain bandwidth of the PLL can be designed much less than $\omega_{p,RES1}$ and $\omega_{p,RES2}$. In this case, the dynamic behaviors caused by unequal $\omega_{p,RES1}$ and $\omega_{p,RES2}$ become insignificant. A simplified thermal model in Figure 3.20 uses a same transfer function, $P(s)$, to account for the responses in T_{RES1} and T_{RES2} due to I_{heat}. The simplified linear model reveals design insights in linear analysis, as will be shown later.

The PFD typically detects two inputs at a sufficiently high frequency (> 1 kHz), which is much higher (> 10×) than the PLL unity-gain bandwidth. Therefore, sampling effect is avoided [74] and the PLL can be analyzed using as a linear system. According to Figure 3.20, the loop gain of the PLL in the Laplace domain can be expressed as

$$A_{loop}(s) = f_{div0}(\Delta TCF)\frac{1}{s}K_{PFD}F(s)K(s)P(s), \tag{3.4}$$

where ΔTCF is the difference of between TCF1 and TCF2 from two oscillators,

$$\Delta TCF = TCF1 - TCF2. \tag{3.5}$$

In Equation (3.4), the loop gain transfer function has an integrator and a thermal pole ($\omega_{p,pl}$ in $P(s)$) at very low frequency, which potentially results in small phase margin as a negative feedback loop. To ensure stability, compensation can be realized in the loop filter implementation ($F(s)$). The closed-loop gain of the PLL ($A_{cl}(s)$) can be written as

$$A_{cl}(s) = \frac{A_{loop}(s)}{1 + A_{loop}(s)}. \tag{3.6}$$

The physical meaning of the closed-loop gain can be interpreted in Figure 3.21. The response of $A_{cl}(s)$ indicates how well the feedback temperature, $T_{fb}(s)$, tracks the external temperature, $T_{ext}(s)$, to effectively cancel out the temperature variations in the ovenized platform, $T_{pl}(s)$. If in the simplified model the temperature of the resonators (T_{RES1} and T_{RES2}) is equal to the temperature of the platform (T_{pl}), the resonator temperature can be stabilized using the negative feedback.

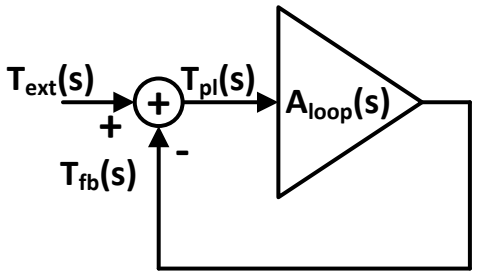


Figure 3.21. Interpretation of the control loop using a feedback system diagram.

The PLL can be designed as a Type-I PLL, and a loop filter design can set the unity-gain bandwidth of A_{loop} well below $\omega_{p,pl}$ so that sufficient phase margin (>60°) can be obtained. Such design can be obtained by setting a low gain on the loop filter to satisfy the stability condition. In this scenario, the loop filter only needs to provide lowpass filtering for voltage pulses from the PFD output, and the circuit is very simple. Another loop filter design for a Type-I PLL includes a compensation zero to cancel out the dominant thermal pole ($\omega_{p,pl}$) in the system. As a result, the unity-gain bandwidth of A_{loop}

can be extended even beyond $\omega_{p,pl}$, and a higher loop gain can be obtained. Figure 3.22 compares the loop gain (A_{loop}) of PLL designs using a simple loop filter and a loop filter with compensation zero in a Bode plot. Using Matlab/Simulink, the transient responses of the platform temperature (T_{pl}) under external temperature ramp (T_{ext}) are simulated in Figure 3.23. It can be found that using a compensation zero in the loop filter, the PLL-based oven-control system can better reject transient thermal shocks. This is due to the higher thermal loop gain and the higher bandwidth in the control loop. Therefore, adding a compensation zero can significantly improve the dynamic performance of the system. The zeros and poles added in the PLL circuit for the Type-I PLL designs are listed in Table 3.4.

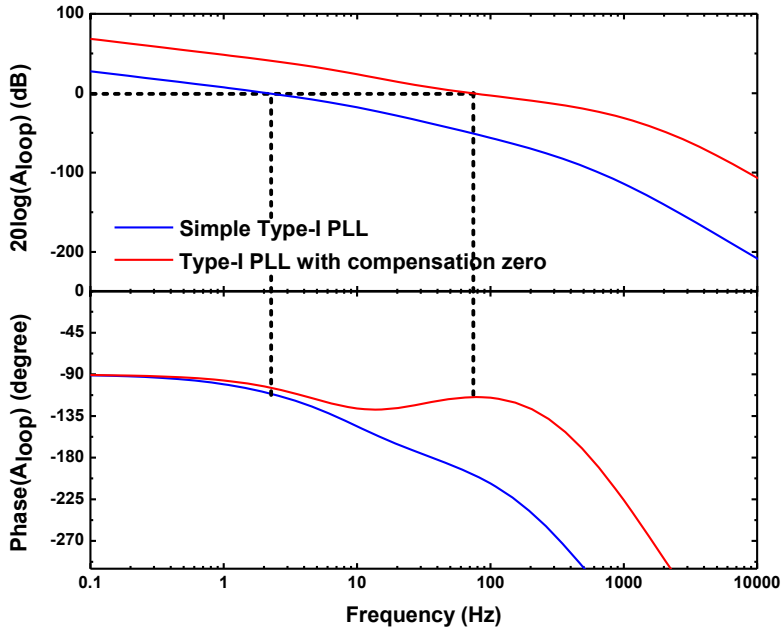


Figure 3.22. Loop gain (A_{loop}(s) of the Type-I PLL implementations on a Bode plot.

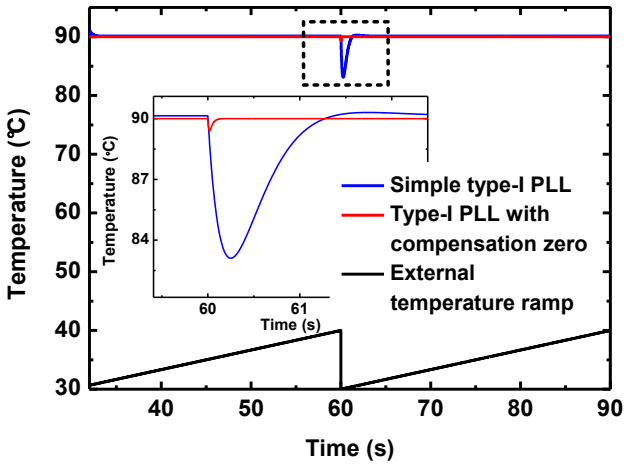


Figure 3.23. Transient responses of the Type-I PLL implementations under external temperature ramp.

Table 3.4. Compensation zeros and poles in the loop filter for the Type-I PLL.

Simple Type-I PLL		Type-I PLL with a compensation zero	
Compensation zero	N/A	Compensation zero	f_{z1} = 4 Hz
Loop filter poles	f_{p1} = 100 Hz	Loop filter poles	f_{p1} = 80 Hz f_{p2} = 200 Hz

If the PLL is designed as a Type-II PLL, there are two integrators in the control loop: one integrator from the PFD and another integrator from the loop filter. Due to the existence of two integrators, the loop gain of the control system starts with 0° phase margin from DC. In order to ensure stability, a loop filter with two compensation zeroes can be employed. The first zero is used to cancel out the low frequency thermal pole ($\omega_{p,pl}$). The second zero can be used to create a phase margin, set the loop gain, and the bandwidth of the PLL. The loop gain ($A_{loop}(s)$) of a Type-II PLL design is plotted in Figure 3.24. The zeros and poles introduced by the PLL circuit for the Type-II PLL are listed in Table 3.5. If the two-zero compensation technique is employed in the loop filter

design, the unity-gain bandwidth can be optimized so that the PLL has a high thermal loop gain at frequencies where external thermal variations exist. Thus, the control loop can be designed to effectively reject thermal transients given specific working environments. The benefit of extending the PLL bandwidth can be also seen in the closed-loop gain of the PLL plotted in Figure 3.25. Below the lowpass cut-off frequency of $A_{cl}(s)$, the feedback signal ($T_{fb}(s)$) tracks the input signal (T_{ext}) to reject thermal transients in T_{ext}. If a PLL can be optimized in such ways, the oscillator with a high TCF (*i.e.*, ~ -30 ppm/K) can also maintain good stability as long as it is in-lock with the other low-TCF oscillator under external temperature variations. In addition, the PLL design with two compensation zeros in Figure 3.24 has a flat phase response near the unity-gain frequency. The compensation scheme ensures that the system is stable against large gain variations in the circuits or thermal stages.

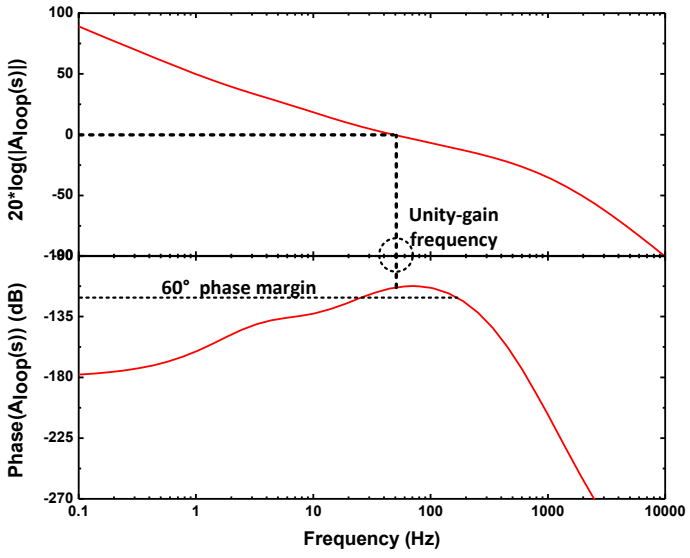


Figure 3.24. The loop gain (A_{loop}(s) of the Type-II PLL with two compensation zeros on a Bode plot.

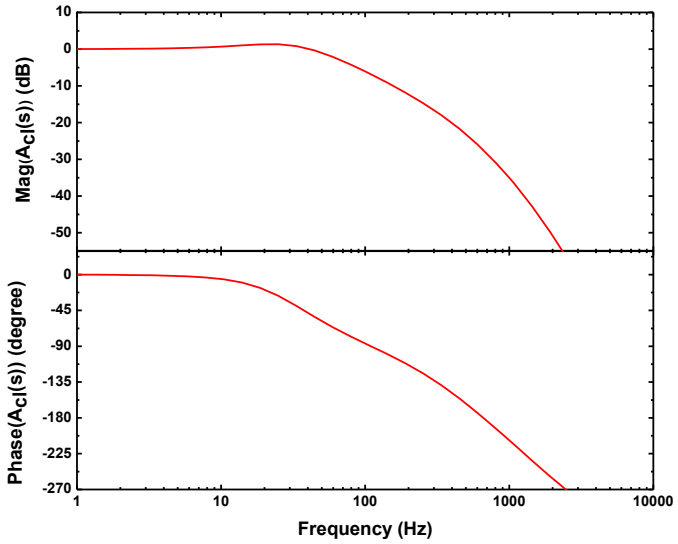


Figure 3.25. Closed-loop gain of the Type-II PLL implementation.

Table 3.5. Compensation zeros and poles in the loop filter for the Type-II PLL.

Compensation zeros	f_{z1} = 0.34 Hz, f_{z2} = 3 Hz
Loop filter poles	f_{p1} = 0, f_{p2} = 90 Hz, f_{p3} = 200 Hz

3.5.2 Noise Analysis

When the MEMS oscillators are placed in the PLL for active compensation, additional phase noise invasion from the PLL circuits into the oscillators is a critical design concern. In previous works, phase-lock loops are used for compensating frequency drift over temperature or correcting initial frequency errors in MEMS clocks [75]. Design efforts have focused on circuit techniques for minimizing degradation on the phase noise performance of MEMS oscillators [75], [76]. In this work, the PLL-based compensation loop is an electro-thermal feedback loop. Noise sources cause random

fluctuations in the heater control voltage (V_{CTRL}), and, hence, frequency fluctuations in the oscillators are induced through non-zero TCFs.

In Figure 3.26, the noise sources from all individual blocks in the PLL are identified. The noise contribution from each block can be studied by removing other noise sources and setting the external excitation (T_{ext}) to zero. In the analysis, the noise sources can be referred to the noise-equivalent temperature (NET) of the silicon MEMS platform ($\overline{T_{n,pl}^{\ 2}(f)}$), which ultimately determines the achievable temperature sensing and control resolution of the active compensation method (in the absence of deterministic errors).

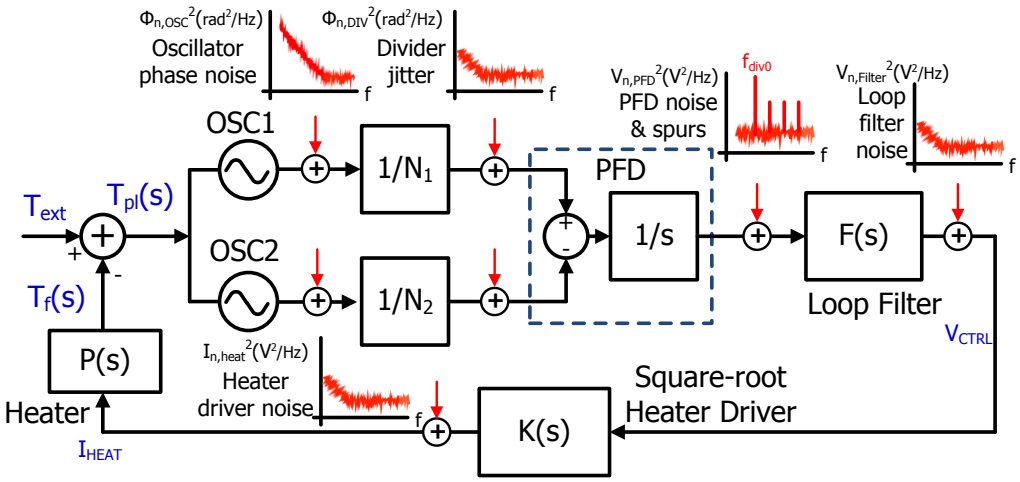


Figure 3.26. Noise sources in the PLL-based oven-control system.

First, two MEMS oscillators in the PLL (OSC1 and OSC2) have their phase noise at the oscillator output. The phase noise of an oscillator is expressed as the relative noise power to the carrier power per unit bandwidth (in dBc/Hz). For a low phase noise oscillator, the phase modulation due to noise has a small modulation index (the root-

mean-square (rms) value of random fluctuation of phase is much less than 1 radian), and the noise spectrum density of phase variation ($\overline{\varphi^2{}_{n,OSC}(f)}$ in rad^2/Hz) is equal to the single side-band phase noise of an oscillator ($L_{OSC}(\Delta f)$) [77],

$$\overline{\varphi^2{}_{n,OSC}(f)} = L_{OSC}(\Delta f) \quad (\Delta f \text{ can be treated as } f). \tag{3.7}$$

The NET (expressed as noise power density) due to the phase noise of two oscillators in the PLL can be derived as

$$\begin{aligned}\overline{T_{n,pl}{}^2(f)} = {} & \overline{\varphi^2{}_{n,OSC1}(f)} \cdot f^2 \cdot \left(\frac{1}{f_{OSC1} \cdot \Delta TCF} \right)^2 \cdot \left| A_{cl}(jf) \right|^2 \\ & + \overline{\varphi^2{}_{n,OSC2}(f)} \cdot f^2 \cdot \left(\frac{1}{f_{OSC2} \cdot \Delta TCF} \right)^2 \cdot \left| A_{cl}(jf) \right|^2 \end{aligned} . \tag{3.8}$$

It can be observed in Equation (3.8) that the transfer of the oscillator phase noise to NET is filtered by the closed-loop gain of the PLL ($A_{cl(s)}$), which is plotted in Figure 3.25 for a Type-II PLL design. When the MEMS oscillators are placed in the PLL, the phase noise of each oscillator causes random fluctuations in the platform temperature (T_{pl}) and corrupts the response of the other oscillator. If the oscillator phase noise is the only noise considered in the PLL, the total phase noise of the oscillator, OSC1, in the PLL can be derived using linear analysis,

$$L_{1tot}(\Delta f) = L_1(\Delta f) + L_2(\Delta f) \left(\frac{f_{01} \cdot TCF_1}{f_{02} \cdot \Delta TCF} \right)^2 \cdot \left| A_{cl}(jf) \right|^2 . \tag{3.9}$$

Similarly, the phase noise of another oscillator, OSC2, can be express as,

$$L_{2tot}(\Delta f) = L_2(\Delta f) + L_1(\Delta f) \cdot \left(\frac{f_{02} \cdot TCF_2}{f_{01} \cdot \Delta TCF} \right)^2 \cdot \left| A_{cl}(jf) \right|^2 . \quad (3.10)$$

In Equations (3.10) and (3.11), again the phase noise corruption on one oscillator from another in the PLL is filtered by the closed-loop gain ($A_{cl}(s)$). This property reveals the benefit of using a thermal PLL control loop compared to other electrical PLL-based compensation techniques. As the unity-gain bandwidth of the electro-thermal PLL is designed comparable to the thermal pole, $\omega_{p,pl}$ in Equation (3.3) (less than 100 Hz according to the loop design in Figure 3.24), the phase noise corruption on each MEMS oscillator is lowpass filtered with a low cut-off frequency. Therefore, only phase noise at the close-in-carrier region (offset frequency below ~100 Hz) will be degraded if the oscillators are placed in the PLL for active compensation. The close-in-carrier phase noise captures slow phase variations, and other drift mechanisms, such as thermal transients or random walk, typically dominating the frequency instability instead of the 1/f noise from circuits. Another important observation from Equations (3.9) and (3.10) is that the phase noise corruption on one oscillator from the other is scale by ΔTCF. If passive compensation can realize a MEMS oscillator with a TCF close to zero while maintaining a large ΔTCF between two oscillators in the PLL, the phase noise corruption on the near-zero TCF oscillator in the PLL will be negligible. This opens the possibility of using a sensing oscillator with poor phase noise performance (*e.g.*, an ultra-low power MEMS oscillator) in the PLL without degrading the phase noise of the oscillator what has a small TCF (*e.g.*, a high performance silicon MEMS resonator on the same platform).

The noise contribution from two frequency dividers is also modeled as phase noise (phase jitter) in Figure 3.26. The phase noise power at the outputs of the dividers can be referred to the divider inputs by multiplying the divide-ratios (N1 and N2). Then, the NET due to divider noise can be calculated similar to the oscillator NET expressions (Equations (3.8), (3.9))

$$\begin{aligned}\overline{T_{pl}^{\,2}(f)} &= \overline{\varphi^2{}_{n,DIV1}(f)} \cdot N1^2 \cdot f^2 \cdot \left(\frac{1}{f_{OSC1} \cdot \Delta TCF}\right)^2 \cdot \left|A_{cl}(jf)\right|^2 \\ &+ \overline{\varphi^2{}_{n,DIV2}(f)} \cdot N2^2 \cdot f^2 \cdot \left(\frac{1}{f_{OSC2} \cdot \Delta TCF}\right)^2 \cdot \left|A_{cl}(jf)\right|^2\end{aligned} \quad . \tag{3.11}$$

The PFD noise is modeled as a voltage noise at the output ($\overline{V_{n,PFD}^{\,2}}$) in Figure 3.26, which include 1/f noise and thermal noise from the PFD circuit. The PFD circuit normally has lower noise contribution compared to other blocks in the PLL, such as the MEMS oscillators. The PFD output is in the form of voltage pulses with a period same as the divider output signal. Digital switching in the PFD introduces spurs. The spurs will be filtered out by the PLL loop. However, it is important to minimize injection of spurs into the output spectrum of the oscillators through EM coupling or supply/ground bounce.

The noise contributions from the loop filter and the heater driver are modeled as voltage noise ($\overline{V_{n,Filter}^{\,2}}$) and current noise ($\overline{I_{n,SQRT}^{\,2}}$), respectively, in Figure 3.26. The noise from the PFD, the loop filter, and the heater driver can be readily analyzed by

referring all noises to the loop filter input, and their contributions on NET are

$$\overline{T_{n,pl}{}^2(f)} =$$
$$\overline{V^2{}_{n,PFD}} \cdot \left(\frac{jf}{f_{div0} \cdot \Delta TCF \cdot K_{PFD}} \right)^2 \cdot |A_{cl}(jf)|^2$$
$$+ \overline{V^2{}_{n,Filter}} \cdot \left(\frac{jf}{f_{div0} \cdot \Delta TCF \cdot K_{PFD} \cdot F(jf)} \right)^2 \cdot |A_{cl}(jf)|^2 \quad . \tag{3.12}$$
$$+ \overline{V^2{}_{n,SQRT}} \cdot \left| \frac{jf}{f_{div0} \cdot \Delta TCF \cdot K_{PFD} \cdot F(jf) \cdot K(jf)} \right|^2 \cdot |A_{cl}(jf)|^2$$

As seen in Equation (3.12), the noise contribution from the heater driver ($\overline{I_{n,SQRT}{}^2}$) is scaled by the gain of the loop filter, |F(jf)|. It is a natural consequence of cascading multiple gain stages. Therefore, a loop filter design with a high gain relaxes the noise performance requirement on the heater driver stage. In a Type-II PLL implementation, the loop filter can be designed with a high gain up to the PLL bandwidth. In order to minimize noise corruption on the PLL, it is more critical to design the loop filter with low 1/f noise to minimize noise invasion on the oscillators.

3.6 Non-ideal Properties

The motivation behind the two-oscillator sensing and PLL-based compensation scheme is to achieve temperature-stable operation for MEMS reference oscillators. The concept of using frequency drift of two oscillators to define a unique oven-set point in Figure 3.1 still suffers non-ideal properties. A closer analysis on the non-idealities will reveal important design considerations.

By nature, all MEMS devices and circuit components suffer temperature-induced drift. A simplified circuit for a Pierce MEMS oscillator is sketched in Figure 3.27. The MEMS resonator can be represented by the BVD model (R_m, L_m, C_m), along with parasitic capacitances, including feedthrough capacitance (C_F) and substrate parasitic capacitances (C_{sub1}, C_{sub2}). The BVD model of the resonator is transformed to a parallel combination of L_P and R_P for analysis. To meet the phase condition of an oscillator loop, the MEMS resonator provides an inductive impedance to cancel out the capacitive elements. According to the circuit analysis presented in Chapter 2, Section 2.2.1, the oscillator output frequency can be found as

$$\omega_{OSC} = \sqrt{\omega_0{}^2 + \frac{\omega_0}{R_m \cdot Q_U \cdot C_P}} \approx \omega_0 \left(1 + \frac{1}{2\omega_0 \cdot R_m \cdot Q_U \cdot C_P} \right), \tag{3.13}$$

where C_P is total parallel capacitance presented from the MEMS resonator (C_{sub1}, C_{sub2}, C_F), input and output capacitances of the amplifier circuits (C_{in} and C_{out}), as well as the capacitors added (C_{P1} and C_{P2}) to define the Pierce oscillator frequency. If we assume the input and output resistance from the amplifier (R_{in} and R_{out}) is large, the value of C_P in Equation (3.13) can be written as

$$C_P = \left(C_{sub1} + C_{in} + C_{P1} \right) // \left(C_{sub2} + C_{out} + C_{p2} \right). \tag{3.14}$$

With a finite value of R_{in} and R_{out}, the effective C_P value changes slightly from (3.14) (the effective C_P can be derived using linear circuit analysis with intensive algebra). The drift

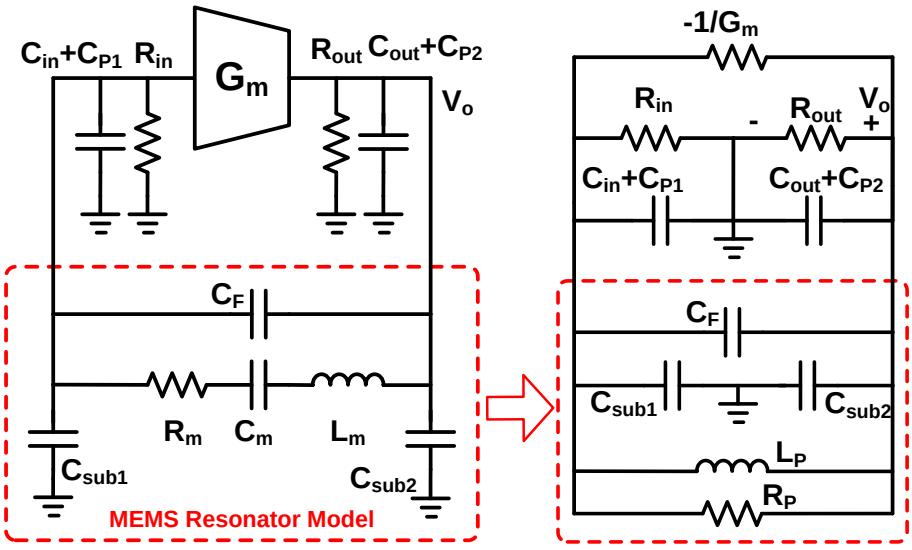


Figure 3.27. Equivalent circuit model of a Pierce oscillator using a transconductance gain stage and a MEMS resonator.

of C_P value first comes from temperature variations. Each capacitor has a temperature coefficient of capacitance (TCC) associated with it. In addition, temperature change induces variations in the circuit gain (G_m) and the motional impedance of a MEMS resonator (R_m). These variations change the effective loop gain of the oscillator, and the oscillation amplitude changes. Hence, the effective input impedance and output impedance of an amplifier varies with the oscillation amplitude due to changes in operation conditions of active transistors. Considering the typical situation that the circuits are not ovenized in the same thermal platform as the MEMS devices, the temperature distribution on the MEMS-circuit combination cannot be well controlled in a changing environment. The temperature gradient between the MEMS and the circuit varies with thermal agitations and other environmental conditions. Effectively, the TCF

curves for two MEMS oscillators become unrepeatable, as sketched in Figure 3.28(a). Fortunately, a MEMS resonator with a high Q tends to rejects these temperature-induced effects. If we look at the sensitivity of the oscillator frequency (ω_{OSC}) to C_P from Equation (3.13), we can find

$$\frac{d\omega_{OSC}}{dC_P} \approx -\frac{1}{2R_m \cdot Q_U} \cdot \frac{1}{C_P^{\,2}} \cdot \tag{3.15}$$

Therefore, a MEMS resonator with a high Q_U significantly reduces the sensitivity of oscillator frequency to component values. It is expected that the effect of TCC on the frequency stability is on the order of ppb to sub-ppm level if high-Q_U (Q_U > 10,000) MEMS resonators are employed for temperature sensing and active compensation.

Another major issue that prevents the active compensation system from achieving ultra-high stability comes from thermal properties. In the two-resonator MEMS platform, there exist a small thermal resistance between the two MEMS resonators ($R_{th,RES1}$ plus $R_{th,RES2}$ in Figure 3.19 and Table 3.3). Due to convection, radiation, and self-heating effects in the resonators, the temperature of the MEMS resonators could be slightly different when the PLL is in-lock. Such an effect can be seen in Figure 3.28(b) in an intuitive way: the MEMS oscillators can have an identical frequency output (in locked condition) while they are at different effective temperatures. As the driving power on the MEMS resonators also changes with the loop gain of the oscillator, the self-heating effect is sensitive to PVT variations, which makes it hard to completely eliminate the temperature offsets. However, the non-ideal effect can be mitigated if one of the MEMS oscillator has near zero-TCF at the oven-set temperature (or has its turn-over temperature

at the oven-set temperature). This requires precise passive TCF-compensation to control the turn-over temperature of a MEMS resonator. Another solution is using a dual-mode resonator instead of two devices so that the temperature offset can be totally eliminated. A dual-mode resonator needs to show different TCFs in two vibration modes; the PLL-based active compensation can be realized in a similar way as a two-oscillator MEMS platform.

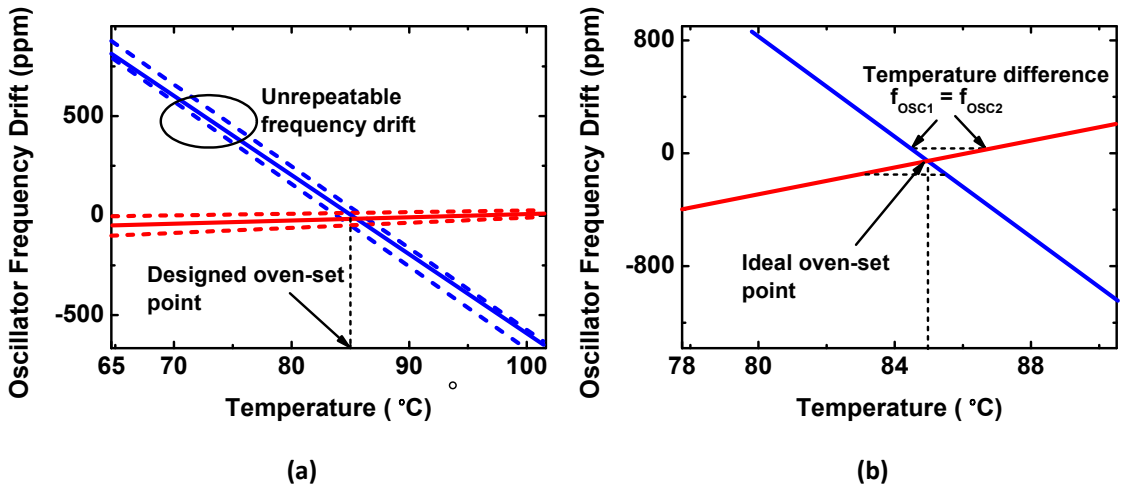


Figure 3.28. Non-ideal effects in the two-resonator temperature sensing scheme. (a) Unrepeatable TCF curves in the oscillators due to temperature gradients; (b) phase-lock at the frequency where two oscillators show different effective temperature.

3.7 CMOS Circuit Implementations

The linear analysis in the above section reveals the considerations in optimizing static and dynamic performance for a PLL-based compensation system. The noise analysis also indicates several key factors in optimizing the circuit noise performance. In this section, CMOS circuits are implemented for the PLL-based compensation system. The circuits are designed using 180 nm CMOS technology.

3.7.1 Low-Jitter Programmable Frequency Dividers

Two frequency dividers are used to generate two clock signals with closely matched frequencies from the MEMS oscillators for phase (or frequency) comparison at the PFD. It is very useful to design the frequency dividers to be programmable. If a programmable divider is used, the MEMS oscillators (using both the uncompensated and TCF-compensated MEMS resonators) do not need to not have a very tight frequency match. In this work, a truly modular programmable divider/counter is implemented by cascading multiple dual-modulus divide-by-2/3 cells [78]. The divide-by-2/3 cells can be constructed by using CMOS D-latches and NAND gates, as shown in Figure 3.29. For each cell, a program-input (P) can configure the divide-ratio by either 2 (P="0") or 3 (P="1"). When N-stages of divide-by-2/3 cells are cascaded (Figure 3.30), the total divide-ratio can be configured using P_0-P_{n-1} control bits from each cell. With an input clock at a period of (T_{in}), the period of the output clock is

$$T_{out} = \left(2^n + 2^{n-1} \cdot P_{n-1} + 2^{n-2} \cdot P_{n-2} + \cdots + 2 \cdot P_1 + P_0\right) \cdot T_{in} . \tag{3.16}$$

For the PLL-based compensation system, ten divide-by-2/3 cells are needed in a cascaded configuration to divide the 80 MHz oscillator down to 50 kHz (with a nominal divide-ratio of 1600) for phase-lock operation. If six programmable bits (P0-P6) are used, the integer division ratio can be configured in a range of 1536 to 1663 (+/- 4%), which accounts for +/- 4% in the initial frequency variation of the MEMS oscillators. Also, the divider provides a tuning resolution of 625 ppm/bit. A high enough resolution in programming the frequency division ratio can be utilized to fine tune the oven-set point.

The oven tuning resolution can be further improved by using a lower divided-down frequency for phase/frequency detection. The lowest frequency needs to be sufficiently higher than the unity gain bandwidth of the PLL loop (~10×) to avoid undesirable sampling effects.

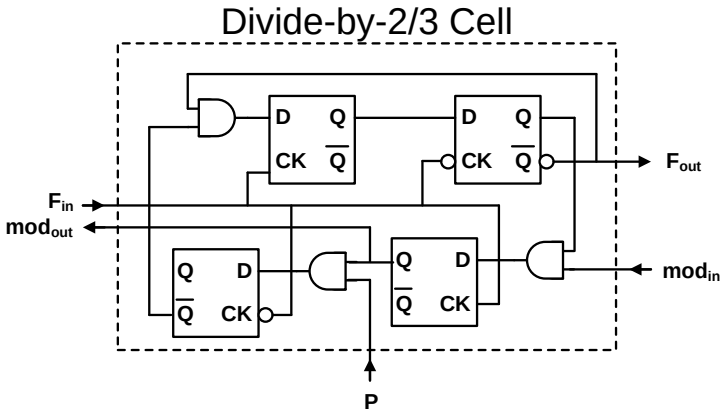


Figure 3.29. Circuit schematic of a divide-by-2/3 cell used in the programmable divider.

Compared to normal PFD circuits used in a PLL, the programmable divider has a significantly longer logic path. Each logic stage adds jitter to the clock signal due to noise from the MOSFET devices. The clock jitter (or phase noise) of each divider stage in the cascaded chain accumulates at the divider chain output [47]. Therefore, a divider with a large division ratio has degraded noise performance. As denoted in Figure 3.30, a multi-stage frequency divider design has progressively higher jitter through the divider chain. In order to reduce the clock jitter, an additional D Flip-flop is used to provide frequency gating for the final clock output. The D Flip-flop is clocked using the reference clock input. Therefore, the final signal output will be synchronized to the initial input clock. Using such a design, the accumulated jitter will be effectively bypassed [79].

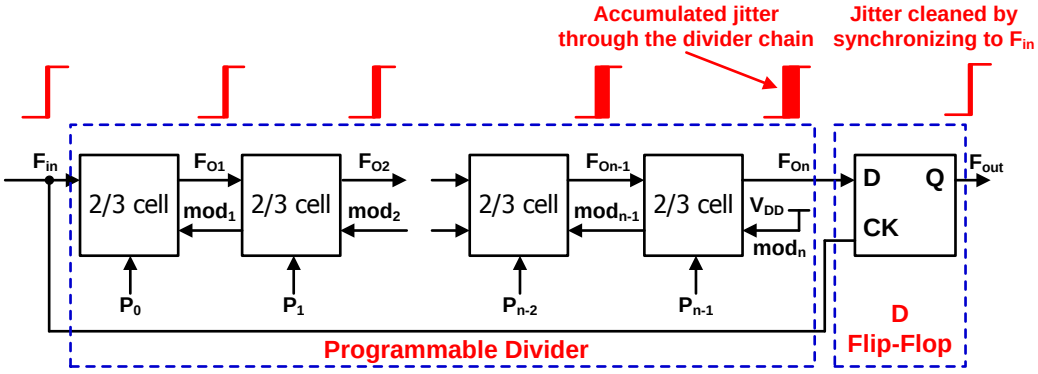


Figure 3.30. Programmable counter/divider with multiple stages.

3.7.2 Phase Frequency Detector

The PFD in the PLL is responsible for detecting the phase or frequency difference between two divider outputs, CLK1 and CLK2 (Figure 3.31). The phase or frequency difference between two clock signals (CLK1 and CLK2) are converted to voltage output signals (V_{Up} and V_{Down}) through the PFD. The voltage pulses (V_{Up} and V_{Down}) are further subtracted and averaged to generate an error signal for the feedback control loop. A simplified PFD circuit is sketched in Figure 3.31. The PFD design employs resettable D Flip-flops. The phase detection range is from -2π to $+2\pi$. Referring to the linear model in Figure 3.20, the gain of the PFD can be written as

$$K_{PFD} = V_{DD}/(2\pi). \qquad (3.17)$$

If two clock inputs have a large difference in frequency, the PFD also works as a frequency detector. The frequency detection function improves the acquisition range,

which is critical for locking two oscillators in the active compensation system. A delay element in the PFD circuit is used to avoid the "deadband" problem.

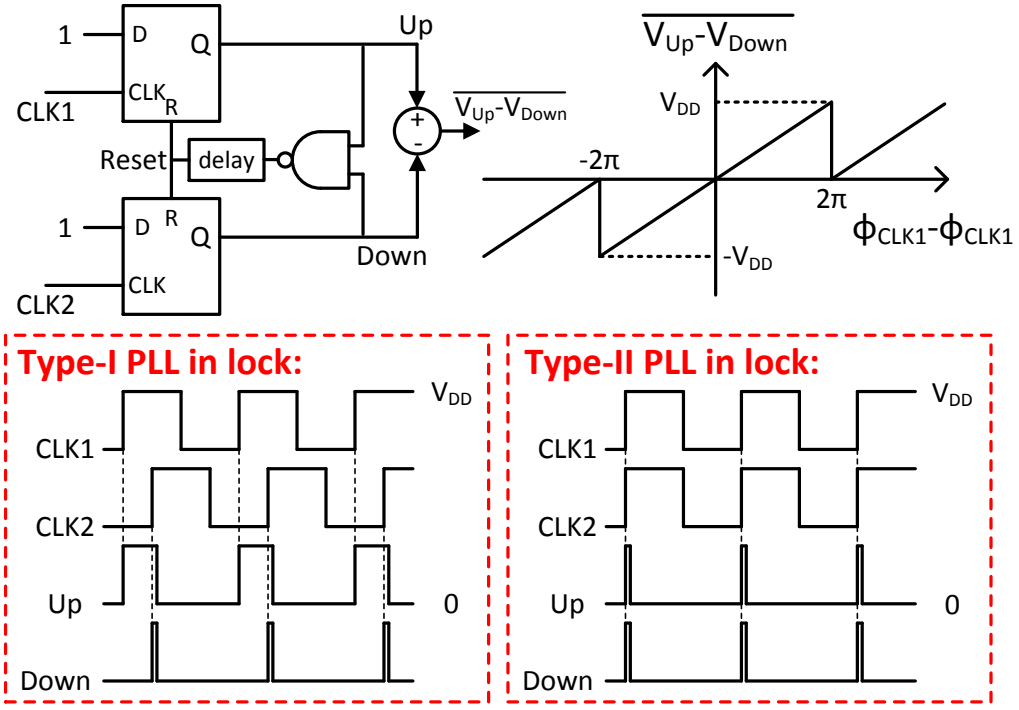


Figure 3.31. Simplified circuit of the phase-frequency detector (PFD), transfer characteristics, input/output waveforms workings in both type-I and type-II PLLs.

The typical input/output waveforms of the PFD in a Type-I and a Type-II PLL (when a PLL is in-lock) are sketched in Figure 3.31. In a Type-I PLL, CLK1 and CLK2 exhibit a static phase offset in locked condition, the output voltage pulses, (V_{Up} - V_{Down}), are averaged to generate a proportional control signal to set the heater power. In a Type-II PLL, CLK1 and CLK2 has near zero phase offset in locked condition (the output from the PFD are narrow voltage pulses with pulse width defined by the delay element to avoid "deadband"). Although the net averaged PFD output (V_{Up}-V_{Down}) is zero for a

Type-II PLL, the loop filter for a Type-II PLL has an integrator that stores the steady-state operating point of the control loop. The narrow pulses in the Type-II PLL output contain smaller energy in the voltage ripples injected into the later loop filter stage, which relaxes the ripple-filtering specification of the loop filter design compared to a Type-I PLL design.

The gate-level circuit schematic of the PFD is sketched in Figure 3.32. The PFD in this work has a relatively low clock frequency (50 kHz). The logic gates and buffers are all designed using static CMOS logic circuits. As discussed in the noise analysis, it is desirable to improve the 1/f noise performance of the circuit. The 1/f noise can be reduced by using MOSFETs with large gate areas [5]. Therefore, the static CMOS gates are sized with large (large W/L ratio) NMOS/PMOS transistors.

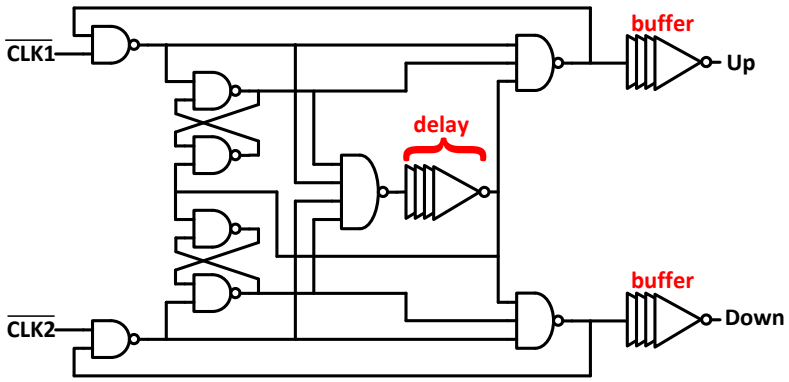


Figure 3.32. Gate-level circuit schematic of the PFD.

3.7.3 Loop Filter

As mentioned earlier, the loop filter subtracts the PFD output signals and averages the signal to generate an error voltage signal. The output from the loop filter is a feedback

control signal for adjusting the heater power in the oven-control loop. Before presenting the loop filter design in this work, a conventional charge pump/loop filter is plotted in Figure 3.33. In this implementation, the PFD output signals (Up and Down) control the charging and discharging current delivered to the passive RC filter. The passive filter contains an integrator and a lead-lag compensator. The transfer function of the charge pump/loop filter is

$$F(s) = \frac{I_{cp}}{2\pi} \cdot \frac{1}{s(C1+C2)} \cdot \frac{1+s/(R1 \cdot C2)}{1+s/[R1 \cdot (C1 // C2)]}. \tag{3.18}$$

However, there are several issues if this charge pump/loop filter is employed in the PLL-based oven-control system. First, the current sources in Figure 3.33 introduce a finite output resistance (R_{out}). The R_{out} comes from the equivalent drain-source resistance of MOSFETs. The leakage current through R_{out} transforms the integrator (1/s) in Equation (3.18) to a low-frequency pole. Moreover, the pole frequency cannot be well controlled, as R_{out} has large variations over process corners and operating regions of CMOS devices. Second, as discussed in the previous section, a two-zero compensation technique is preferred in the loop filter implementation for optimizing the dynamic thermal performance of a Type-II PLL. However, the conventional charge pump/loop filter design can only contain one compensation zero. Third, the 1/f noise from the current sources in the charge pump potentially degrades the noise performance of the oscillators in the PLL.

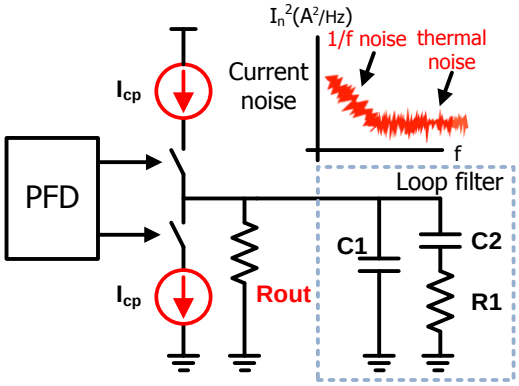


Figure 3.33. Schematic of a conventional charge pump loop filter.

In this work, a flexible and low 1/f noise loop filter design is proposed for the PLL-based oven-control system. If a CMOS op-amp is configured as a loop filter in Figure 3.34, the passive impedances Z1 and Z2 determine the transfer function of the loop filter. The analysis on the loop filter transfer function can be obtained by decomposing the input signal to a common-mode input ($V_{in,cm}$) and a differential-mode input ($V_{in,dm}$). The output of the loop filter due to $V_{in,cm}$ can be expressed as

$$V_{o,cm} = -V_{in,cm} \cdot \frac{Z2}{Z1+Z2}. \tag{3.19}$$

The output of the loop filter due to $V_{in,dm}$ can be expressed as

$$V_{o,dm} = V_{in,dm} \cdot \frac{Z1}{Z2}\left(1+\frac{Z2}{Z1+Z2}\right). \tag{3.20}$$

As the square-wave output voltage pulses from the PFD outputs (V_{Up} and V_{Down}) always satisfies

$$V_{in,dm} = \frac{1}{2} V_{in,cm}, \tag{3.21}$$

the transfer function of the op-amp loop filter can be simplified as

$$V_o = V_{in,dm} \cdot \frac{Z1}{Z2}. \tag{3.22}$$

As intended, the loop filter in Figure 3.34 detects the differential-mode input ($V_{in,dm}$), and it can be used to subtract the "Down" signal from the "Up" signal (V_{Up}-V_{Down}) from the PFD output (Figure 3.31).

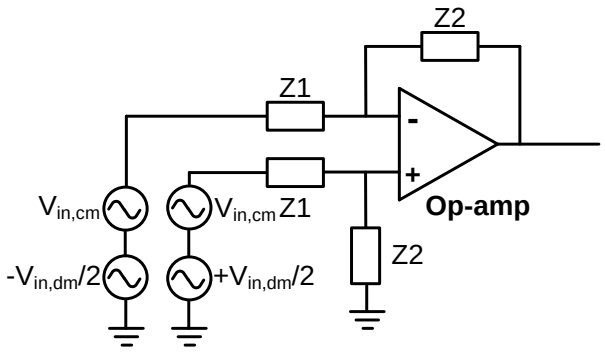


Figure 3.34. Op-amp configured as a loop filter.

Two useful loop filter configurations are discussed here. The first loop filter design can be used to construct a Type-I PLL with a compensation zero. The RC networks used for the loop filter is show in Figure 3.35. The transfer function of the loop filter can be derived as

$$F(s)=\frac{R_2}{R_{12}}\cdot\frac{1+s(R_{11}+R_{12})C_1}{(1+sR_2C_2)(1+sR_{11}C_1)}. \tag{3.23}$$

The transfer function contains one zero and two poles. The zero can be configured at the lowest frequency. Two poles can be used to provide filtering for the voltage ripples coming from the PFD.

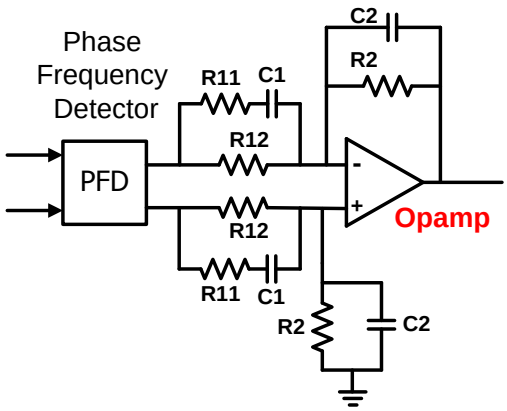


Figure 3.35. Loop filter design with one compensation zero and two poles.

The second loop filter design can be used to implement a Type-II PLL with two compensation zeros, as shown in Figure 3.36. The transfer function of the loop filter can be derived as

$$F(s)=\frac{1}{sR_1(C_1+C_2)}\cdot\frac{1+sR_2C_1}{1+sR_2(C_2\,//\,C_1)}\cdot\frac{1+s(R_1+R_3)C_3}{1+sR_3C_3}. \tag{3.24}$$

The transfer function contains one integrator, two compensation zeros, and two poles. The zeros can be configured at lowest frequencies to cancel the thermal pole and define

the PLL loop bandwidth, as discussed in Section 3.5.1. The two poles can be used to provide filtering for the voltage ripples coming from the PFD.

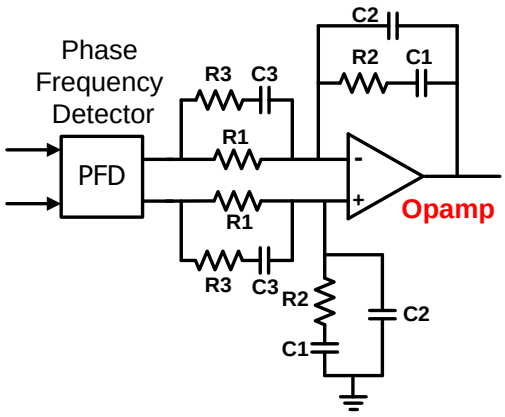


Figure 3.36. Loop filter design with one integrator, two compensation zeros, and two poles.

A low-noise CMOS op-amp design is used for the loop filter implementation. As shown in the circuit schematic of the op-amp in Figure 3.37, the op-amp uses a folded-cascode input stage and a class-AB output stage. The input stage of the op-amp consists of a PMOS pair (M1 and M2) connected in folded-cascode to extend the input common-mode range down to ground. The use of PMOS only as the input transistors reduces 1/f noise of the op-amp. The output stage consists of a NMOS/PMOS pair (M17 and M18) in common-source configuration, providing a rail-to-rail output range. The output FETs, M17 and M18, are biased using a floating voltage bias generated using M14-M16 [80], making efficient use of the supply current. To ensure stability across the whole voltage operating range, a cascode Miller compensation capacitor (C_{comp}) is used. The biasing network of the op-amp is also shown in Figure 3.37.

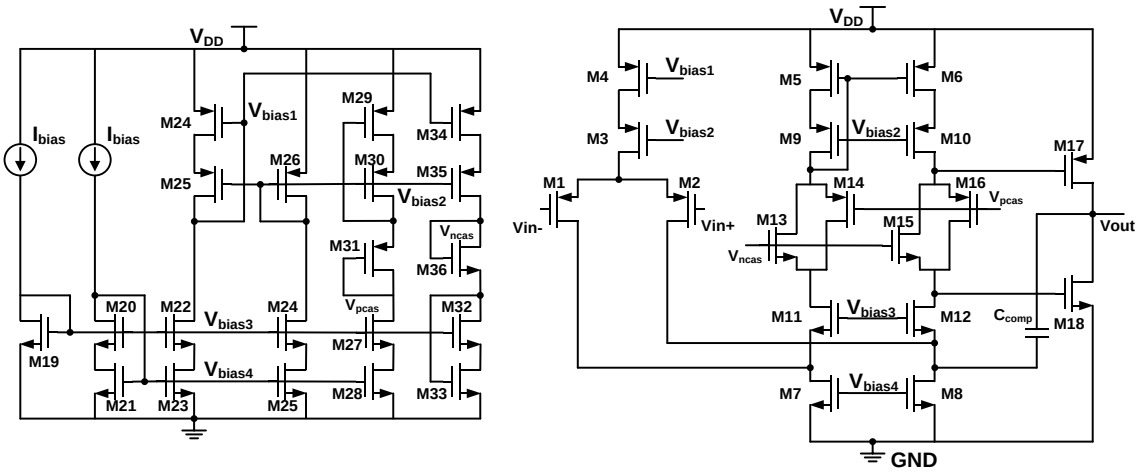


Figure 3.37. Circuit schematic of CMOS op-amp and the bias generator.

Using the CMOS op-amp, the 1/f noise corner frequency is typically still beyond the bandwidth of the PLL, indicating potential noise degradation of the PLL. By using chopper-modulation, the 1/f-noise can be effectively removed [81]. The CMOS op-amp design can be further modified to include chopper modulators, as shown in Figure 3.38. The chopper modulator up-converts the input signal to a chopper frequency. The demodulator down-converts the signal back to its original frequencies. In the meantime, the 1/f noise and DC-offset are modulated to the chopper frequency at the output, and they can be easily filtered out by the PLL loop transfer function. As the electro-thermal PLL in this work has relatively low bandwidth, picking a low chopper frequency above 1 kHz is sufficient. The voltage pulses originated from chopper modulation can be filtered by the passive RC networks used in constructing a loop filter for the PLL. As discussed in Section 3.1, the offset voltage in the chopper-stabilized op-amp is not a critical concern, because the offset does not directly induce frequency error using a phase-lock technique

for active compensation. The modulators and demodulators are implemented using CMOS switches driven with complimentary clock signals. The simulated input-referred noise voltage of the CMOS op-amp is shown in Figure 3.39, where the noise of the chopper-modulated op-amp is compared to the original design.

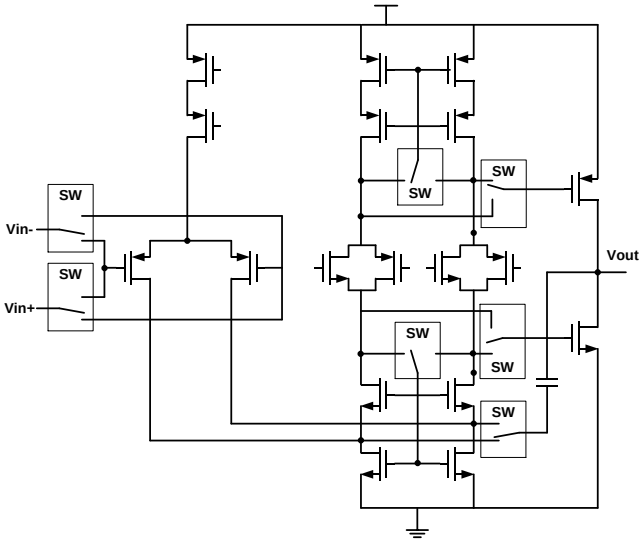


Figure 3.38. Circuit schematic of the CMOS op-amp with chopper modulation to reduce 1/f noise.

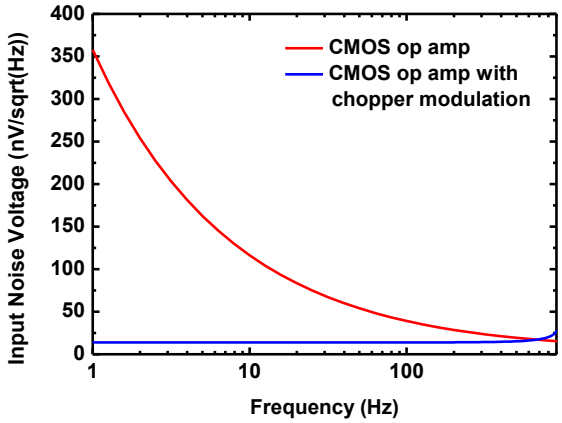


Figure 3.39. Simulated input referred noise voltage of the CMOS op-amp design and the op-amp with chopper modulation to reduce 1/f noise.

3.7.4 Square-root Heater Driver

As shown in Figure 3.20, the loop filter output is a control voltage signal (V_{CTRL}) which indicates the phase offset between two MEMS oscillators in the PLL. The control voltage is further processed to generate a current delivered to the heater (I_{heat}) on the platform to control the temperature. A voltage-to-current (V-to-I) converter is first used to generate a control current (I_{CTRL}) from the control voltage (V_{CTRL}). A V-to-I design with a large input/output voltage operation range is desirable, as it directly determines the control range of the PLL-based oven-control system. The V-to-I design in this work is based on a two-stage amplifier configuration, as shown in Figure 3.40. The differential pair as an operational transconductance amplifier (OTA) in the first stage forces the voltage, V_{REF}, to track the input voltage, V_{CTRL}. A reference resistor (R_{REF}) is employed to transform V_{REF} to I_{CTRL}. The upper swing range of V_{CTRL} is limited by the overdrive voltage of the M7, and V_{CTRL} can swing from near ground all the way close to VDD. The MOSFET, M8, is used to replicate I_{CTRL} and deliver the current to the later stage for further processing. The two-stage amplifier is compensated using a cascode Miller compensation technique, and a capacitor, C_{comp}, is used to ensure stability across the input range, *i.e.*, V_{CTRL} from 0 to V_{DD}.

Due to the nature of Joule heating, there is quadratic transfer function from the heater current to the heating power in a resistor,

$$P_{heat} = I_{heat}^{\ 2} \cdot R_{heat}. \tag{3.25}$$

If a linear heater driver is used, the gain of the heater stage is proportional to the heater current level (I_{heat}). Across a wide operating range of the heater, there is a large gain variation in Equation (3.25). The gain variation not only affects the control loop performance but also causes stability issues in PLL-based oven-control system. In order to resolve this problem, linearization on the heater gain is performed by using an analog square-root heater driver, as shown in the schematic in Figure 3.41. In the square-root circuit, PMOS devices M1-M4 construct a translinear loop [65], [82] that efficiently generates an analog square-root function. Taking the input from the V-to-I circuit (I_{CTRL}), the output current of the square-root generator (I_{SQRT}) can be expressed as

$$I_{SQRT} = \sqrt{\frac{I_{CTRL} \cdot I_{REF}}{4}} \,. \tag{3.26}$$

Then, the square-root current, I_{SQRT}, is amplified by using CMOS current mirrors to generate a heater driver current (I_{heat}) that flows into the heater resistor on the MEMS platform. The current mirrors are arrayed in 4 cells, forming a 4-bit binary-weighted programmable output driver. Control bits P0-P4 are used for heater power control,

$$P_{heat} = \frac{I_{CTRL} \cdot I_{REF}}{4} \left[P0 \cdot (N) + P1 \cdot (2N) + P3 \cdot (4N) + P4 \cdot (8N) \right]^2 \cdot R_{heat} \,. \tag{3.27}$$

Using the programmable driver, the heater power can be adjusted to accommodate ovenized MEMS platforms or other ovenized devices with different thermal properties. In order to reduce the total area of the MOSFETs that deliver a large output current (I_{heat}), the MOSFETs are sized with small gate length (L). However, the drain to source voltage

of the heater driver MOSFETs experiences a large change with the changing voltage drop on R_{heat}, and channel length modulation will induce errors in the current mirrors if short channel devices are employed. The problem is solved by designing the current mirrors using regulated-cascode technique, as shown in Figure 3.41. A near constant gain can be obtained in a large operation range. The heater current versus the input current from the V-to-I circuit (I_{CTRL}) is plotted in Figure 3.42, showing a square-root fashion.

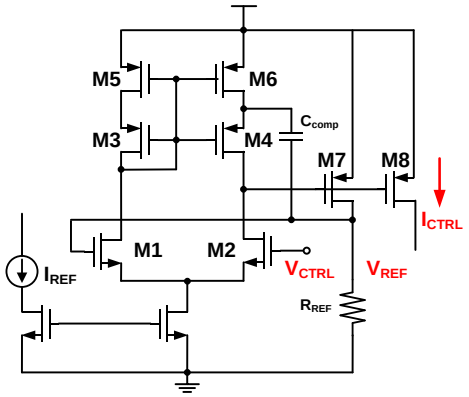


Figure 3.40. Circuit schematic of the high input range voltage-to-current (V-to-I) converter.

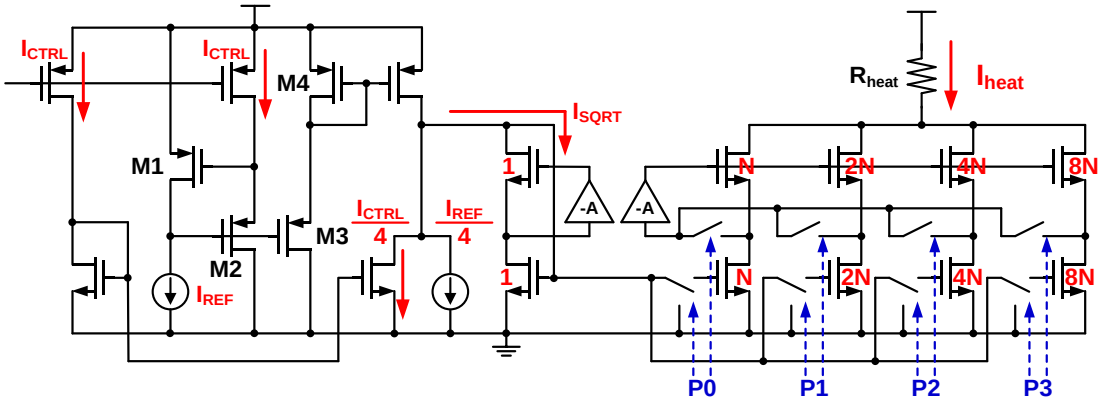


Figure 3.41. Circuit schematic of the analog square-root generator and the 4-bit binary-weighted programmable heater current driver.

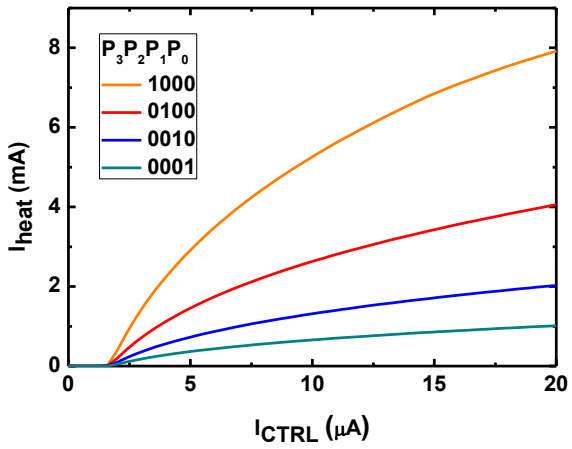


Figure 3.42. Simulated heater current versus the input current from the V-to-I circuit (I_{CTRL}) for 4 tuning states (a heater resistor of 200 Ω is assumed on the silicon platform).

In the heater driver design, it is also critical to consider the limited supply voltage in the CMOS circuit implementation. If a large heating current is used to ovenize the MEMS across a wide working temperature range, the voltage drop on the heater resistor (R_{heat}) can exceed the supply voltage limit. Fortunately, with the high thermal resistance obtained in the ovenized MEMS platforms in this work ($R_{th,leg}$ > 13 K/mW), a voltage drop of 1.6 V on a heater resistor (R_{heat}) of 250 Ω can raise the platform temperature by 130 K above the external temperature. Therefore, a nominal voltage of 1.8 V used in the 180 nm CMOS is sufficient for designing the heater driver to cover a large working temperature range. In order to further extend the control range, high voltage devices in the 180 nm CMOS technology with a nominal supply voltage of 3.3 V can be used in designing the heater driver stage.

3.8 Measurement Results of the PLL-based Oven-Control System

3.8.1 System Implementation

The CMOS PLL circuits for the oven-control system are implemented using TSMC 180 nm CMOS technology. A microscopic photograph of the CMOS chip is shown in Figure 3.43. The individual circuit blocks are marked in the chip photo. According to the extracted thermal models for the fabricated two-resonator platforms, a Type-II PLL is implemented for active compensation. The components used in the loop filter design are denoted in Figure 3.44. The design is based on a Type-II PLL implementation with two compensation zeros in loop filter design. In measuring the prototype control system, the CMOS chip and the MEMS chip are mounted separately in ceramic packages, and the packages are assembled on a PCB.

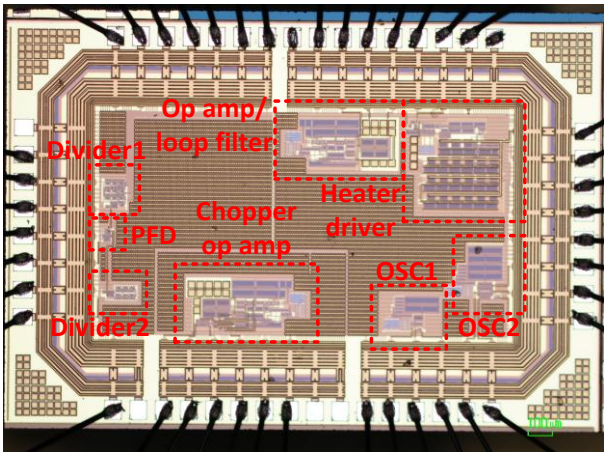


Figure 3.43. Microscopic photograph of the CMOS chip for the PLL-based control system.

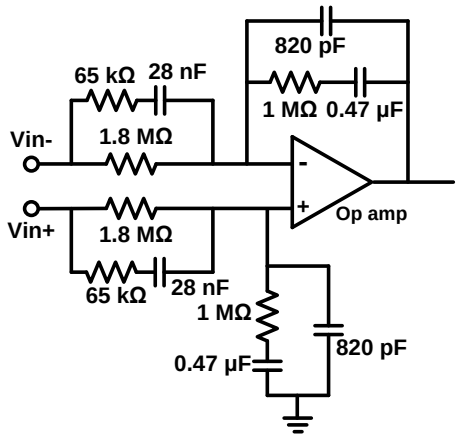


Figure 3.44. Components used to configure the loop filter.

3.8.2 Temperature Stability of the MEMS Oscillators

Using the PLL-based oven-control scheme, the frequency stability of MEMS oscillators under external temperature change is measured. During the measurements, the PCB containing both the MEMS chip and the CMOS chip is mounted in a vacuum chamber with a pressure level of less than 10 mTorr. The chamber temperature is swept from 343 K down to 233 K while the output frequency of the MEMS oscillators in the PLL is monitored using a frequency counter (Agilent 53181A). As the chamber temperature ramp is a relatively slow process, while the Type-II PLL implementation has a sufficiently large bandwidth to ensure dynamic performance, the two oscillators used for active compensation are locked during the chamber temperature ramp. As a result, the frequency counter records identical frequency outputs from the oscillators. In the measurements, Labview interface is used to continuously record the chamber temperature and the oscillator frequency. The frequency drift of the MEMS oscillators using the Platform-I design is measured and plotted in Figure 3.45(a). The overall frequency drift is

within +/-5 ppm in the chamber temperature range of -40 ℃ to 70 ℃. In another measurement, the overall frequency drift of a MEMS oscillator using Platform-II is within +/-4 ppm in the chamber temperature range of -40 ℃ to 70 ℃, and the result is plotted in Figure 3.45(b). It can be found that, with the proposed active compensation system, the effective TCF of a MEMS oscillator has been reduced to 36 ppb/K, an almost three orders of magnitude improvement compared to an uncompensated silicon MEMS oscillator (TCF of ~-30 ppm/K). The residual frequency drift seen is due to the non-ideal characteristics of the current MEMS platform design, as discussed in Section 3.6.

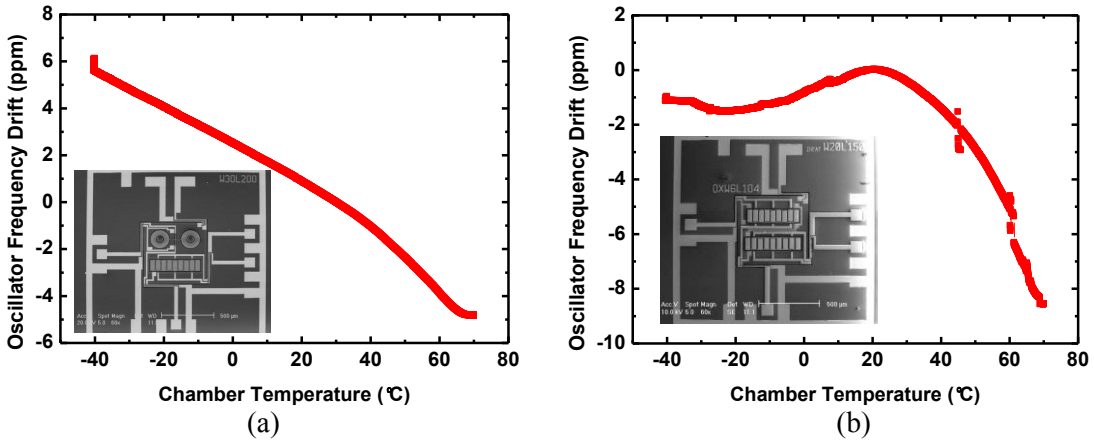
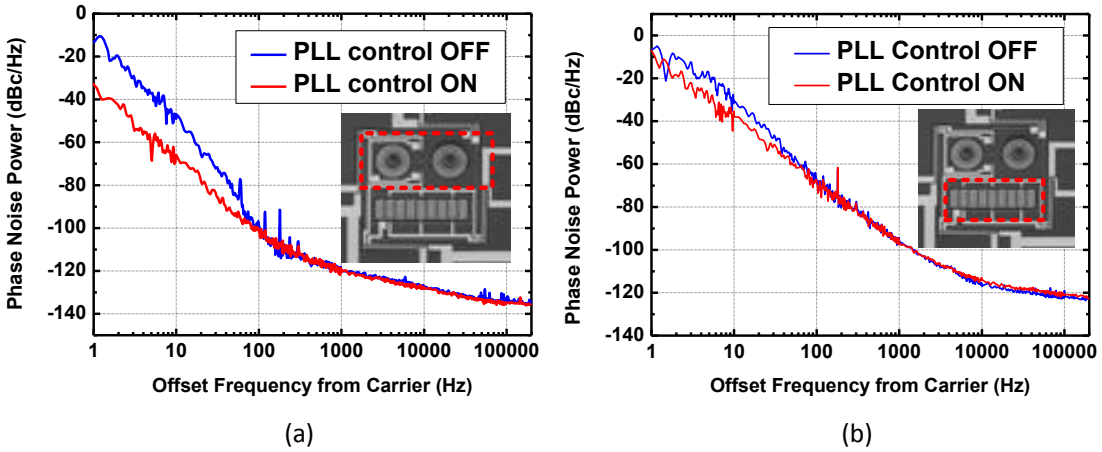


Figure 3.45. (a) Frequency drift of MEMS oscillators using two-resonator Platform I; (b) Frequency drift of MEMS oscillators using two-resonator Platform II.

3.8.3 Noise Performance

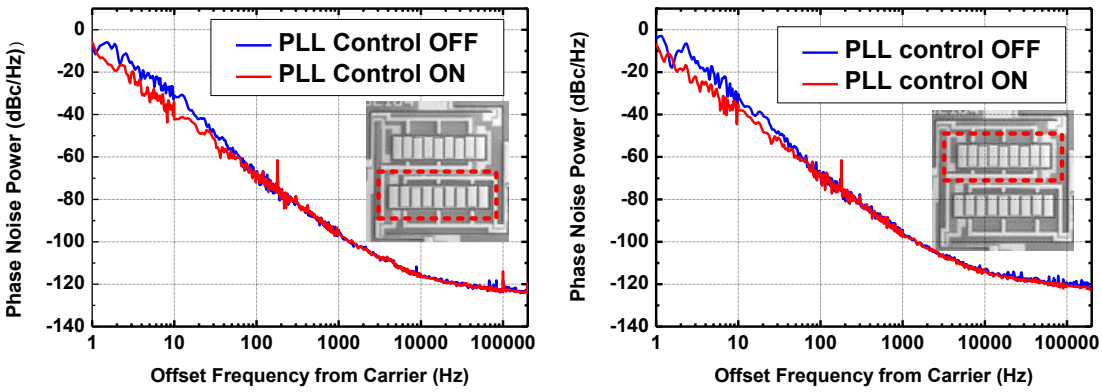
The phase noise performance of the MEMS oscillators in the PLL-based compensation system is also measured. The performance of two oscillators using Platform-I is plotted in Figure 3.46, including a 20 MHz MEMS oscillator using a TCF-compensated coupled-ring resonator and an 80 MHz MEMS oscillator using an

uncompensated LBAR. Also, Figure 3.46 compares the phase noise of the oscillators with and without PLL-based ovenization. It can be found that in the far-from-carrier region, the PLL does not degrade the phase noise of the oscillators. In the close-to-carrier region, the MEMS oscillators in the PLL even exhibits better measured noise performance. According to the noise analysis presented before, the electro-thermal PLL is expected to have a minimal noise impact with a proper control loop design and circuit implementation. In the phase noise measurement using an Agilent E5500 system, the measurement on close-in-carrier region (offset frequency in the range of 1-100 Hz from carrier) takes approximately 5-10 s to complete a frequency scan. In this measurement, slow frequency fluctuations due to the resonator temperature variations cannot be distinguished from 1/f noise in the measured phase noise plot. In fact, slow temperature variations tend to dominate the fluctuations in the close-in-carrier region. If the MEMS oscillators are placed in the PLL, the active compensation effectively regulates the temperature variations of the MEMS resonator. Therefore, we observe improvement in phase noise from the measurement results. Another design using a two-resonator Platform-II is also measured. The phase noise of an 80 MHz MEMS oscillator using an uncompensated LBAR and an 80 MHz uncompensated LBAR oscillator on Platform-II is plotted in Figure 3.47. The phase noise performance exhibits similar improvement in the close-in-carrier region if the oscillators are in the PLL. In the phase noise measurement, the loop filter of the PLL uses the CMOS op-amp design without chopper modulation. As the thermal effects dominate the close-in-carrier noise, the benefit of using chopper modulation is not obvious.



(a) (b)

Figure 3.46. (a) Measured phase noise performance of a 20 MHz MEMS oscillator (using a TCF-compensated coupled-ring resonator in Platform-I) and (b) an 80 MHz MEMS (using an uncompensated LBAR in Platform-I). The phase noise performance with PLL-based compensation is compared to the performance without PLL compensation.



(a) (b)

Figure 3.47. (a) Measured phase noise performance of a 80 MHz MEMS oscillator (using a TCF-compensated LBAR in Platform-II) and (b) an 80 MHz MEMS (using an uncompensated LBAR in Platform-II). The phase noise performance with PLL-based compensation is compared to the performance without PLL compensation.

The effect of the oscillator phase noise on the NET of the platform can be calculated using Equation (3.11). In the calculation, the measured phase noise of the oscillators in

the active compensation loop is adopted. The noise power, $\overline{T_{n,pl}^{2}(s)}$, is integrated over the bandwidth of 1 Hz to 200 kHz to obtain the variance of temperature fluctuations due to oscillator phase noise. The results indicate the resolution of temperature sensing in the two-oscillator compensation scheme. It is found that the square-root value of the temperature variance for the Platform-I design is 5.4×10^{-8} K, while the square-root value of the temperature variance for the Platform-II design is 3.2×10^{-8} K. These results indicate that the achieved temperature control accuracy is still much worse than limitations set by noise-induced fluctuations. Therefore, there is more room to design one of the sensing oscillators at a low power to trade-off phase noise performance. In this scenario, the temperature sensing accuracy will not be degraded if the thermal design can minimize the temperature offset between the resonators on the MEMS platform.

3.8.4 Power Consumption

The power consumption of the PLL-based oven-control system is compiled in Table 3.6. The majority of power consumption comes from the heating power used for ovenization, especially at low external temperature. As discussed in Section 3.4, the heating power can be further reduced by improving the thermal isolation design to obtain larger thermal resistance. The power consumption of a MEMS oscillator is determined by the noise performance requirement. As discussed in the last section, the temperature resolution in the PLL-based oven-control system is not limited by the phase noise. Therefore, it is possible to design a sensor oscillator with low power while sacrificing the noise performance, and the degradation in frequency stability is expected to be negligible.

Also, as the control system has a low bandwidth (related to the large thermal time constant), there is potential to design circuits at ultra-low power with reduced bandwidth and speed.

Table 3.6. Power Consumption of the PLL-based Oven-control System.

Functional Blocks	**Power Consumption**
Heater power	0.3 – 8 mW
20 MHz MEMS oscillator (TCF-compensated)	4 mW
80 MHz MEMS oscillator (uncompensated)	5.1 mW
80 MHz MEMS oscillator (TCF-compensated)	4.8 mW
Frequency divider and PFD	100 μW
Loop filter (with op-amp)	650 μW
V-to-I and square-root generator	360 – 680 μW

3.9 Towards "sub-ppm-level to ppb-level" Frequency Accuracy

High-end applications demand frequency references with frequency accuracy better than 1 ppm or in ppb levels. These applications include precision clocks in navigation systems, radars, and cellular base-stations, which at present mostly use bulky OCXOs or atomic time keeping devices. The deployment of ultra-stable, low-power, and miniaturized MEMS timing units enables new attractive applications, such as the chip-scale TIMU microsystem that can be used for navigation and positioning in GPS-denied environments.

As discussed in Chapter 1, the term of frequency accuracy can be decomposed into deterministic drift and random noise effects. In the two-oscillator sensing and compensation scheme, the temperature-induced deterministic drift can be further reduced by improving the MEMS devices through: (1) better process control on the passive TCF-compensation so that the turn-over temperature is placed at the oven set point; and (2)

minimizing the temperature offset between two resonators, or using two vibration modes of the same dual-mode MEMS resonator. It is expected that frequency drift can be further improved to sub-ppm level without the need for calibration. The frequency or phase variations in the output clock signal due to oscillator phase noise can be reduced by improving the Q of MEMS resonators and increasing the driving signal power on MEMS resonator.

As discussed in Section 3.6, the use of a high-Q device in an oscillator makes the frequency stability robust against circuit variations. Therefore, there exists less concern on the temperature gradient between the MEMS and the circuits compared to the use of a resistive temperature sensor in Chapter 2. This property helps obtain a more repeatable and consistent residue frequency drift with PLL-based oven-control if the MEMS devices and package are well characterized. In the two-resonator sensing scheme, calibration can be utilized to effectively remove known offset errors. Using calibration, the residue frequency drift of the MEMS oscillators with PLL-based compensation can be partially eliminated by either capacitive tuning (with ppm resolution) or piezoelectric tuning (with ppb resolution) introduced in Chapter 2. Other environmental effects on the oscillator, such as acceleration, shock, vacuum-degradation in a MEMS package, *etc*., can be mitigated by using integrated sensors to actively generate tuning signals that control the frequency pulling capacitors or piezoelectric tuning bias in a piezoelectric MEMS oscillator. A combination of closed-loop compensation and fixed point calibration is expected to push the frequency stability to ppb-level under typical working conditions.

Another critical concern for MEMS timing technology is the initial frequency accuracy of a MEMS resonator. Any MEMS device is prone to variations in the fabrication process. Due to the fact that MEMS resonators are miniature devices, conventional machining techniques used in quartz references for frequency trimming cannot be applied to MEMS. The initial frequency error in a MEMS resonator can be in the range of 100 to 1000 ppm, depending on the fabrication control and yield. The initial frequency error of a MEMS oscillator can be corrected using capacitive tuning or piezoelectric tuning. The combination of capacitive tuning and piezoelectric tuning can cover a medium to high resolution in terms of frequency trimming accuracy. However, the maximum tuning range is limited by physical properties of the MEMS resonator as discussed in Chapter 2, and the initial frequency error is typically beyond capacitive tuning range. Using low-power ovenized MEMS technology, the initial frequency of MEMS oscillators can be also configured by changing the oven set temperature. With silicon MEMS which has a TCF of -30 ppm/K, the change of oven set point within +/- 10 K can cover a frequency tuning range of +/- 300 ppm. Such a thermal frequency trimming technique can cover the typical range of initial frequency errors in MEMS resonators. Also, changing the oven set point induces minimal phase noise degradation on the MEMS oscillators, as the Q of MEMS resonator only has very slight change over a small change of working temperature. This property compares favorably to the conventional method that relies on a fractional-N PLL frequency generator [75], [76], which introduces excessive noise. The thermal frequency trimming can be easily realized by using programmable dividers in the PLL-based oven-control system (discussed in

Section 3.7) to configure the oven set point. The thermal tuning, as a coarse frequency trimming method, can be combined with capacitive and piezoelectric tuning methods, which provide fine resolution coverage.

3.10 Summary

In this chapter, the issue of frequency drift in MEMS oscillators over temperature is addressed by using an alternative temperature sensing and oven-control scheme. The analysis presented reveals the advantages of using a two-oscillator temperature sensing technique as compared to the use of conventional resistive temperature sensors. The active compensation is realized using a PLL-based oven-control system to stabilize the frequency of MEMS oscillators. Circuit techniques for implementation a flexible, low-noise, and low-power PLL for oven-control are demonstrated. The active compensation technique realizes a MEMS oscillator with an overall frequency drift within +/- 4 ppm across a working temperature range of -40 °C to 70 °C without the need for system calibration. The noise property is analyzed using a linear model for the control loop. In contrast to conventional PLL circuits used to actively compensate for the MEMS frequency drift, the PLL-based oven-control system implemented in this chapter exhibits near-zero phase noise degradation on the MEMS oscillators.

CHAPTER 4.

Integrated Ultra-Wideband Filters and Tunable Bandstop Filters

With the goal of implementing an interposer having all needed MEMS and microsystems for communication applications, in this chapter, the use of integrated RF MEMS devices to implement RF filters with wide frequency tuning capability is studied. High-performance and miniaturized RF filters are implemented using an IPD technology on a high-resistivity silicon substrate, which offers chip-scale integration capability compared to prior works that rely on conventional low-loss microwave substrates. The filter implementations are designed for ultra-wide band (UWB) radios. Integration of RF MEMS devices (including both MEMS tunable capacitors and MEMS ohmic switches) on a same chip enables the realization of tunable/switchable RF filters. A tunable bandstop filter has been demonstrated that offers more than an octave tuning range. In additional to the frequency tuning capability offered by RF MEMS capacitors, integrated MEMS ohmic switches are also exploited to add switch on/off capability to the tunable bandstop filter. Having the switchable function, the notch can be strategically switched off and the filter can be configured as an all-pass circuit in case no interference is present.

The tunable and switchable filter demonstrated in this chapter is a step toward the cognitive spectrum utilization of the wireless spectrum resources.

4.1 RF Front-end Filters for UWB Radios

UWB communication has emerged as a fast growing technology since the Federal Communications Commission (FCC) approved the unlicensed use of the frequency spectrum from 3.1 GHz to 10.6 GHz [83]. The allocated wide spectrum enables Impulse Radio-UWB (IR-UWB), which is based on transmitting and detecting pulses with short time durations. In contrast to narrow-band systems, IR-UWB is carrier-less, greatly simplifying the RF front-end by using all-digital transmitters [84], [85] and receivers that do not require power hungry RF oscillators or PLLs [86], [87]. The low-cost and energy-efficient IR-UWB scheme is a good candidate for several applications, such as wireless sensor networks and low power hand-held devices.

UWB communication stimulates both opportunities and challenges in the design and implementation of fully integrated RF front-ends [84]-[88]. Still, a major impediment to the wide adoption of UWB technology is the issue of narrow-band interferences that co-exist in the same frequency band as well as out of the UWB communication band (Figure 4.1). The FCC-regulated low UWB emission power (-41.3 dBm/MHz) necessitates interference mitigation techniques. Circuit design techniques, such as frequency selective receivers, have been explored to reject the interferences using active filters, but at the cost of increased CMOS chip area and higher power consumption [89], [90]. Alternatively, RF front-ends exploiting only sub-bands of the UWB frequency range have been used to address the interference issue [91], [92], but they tend to reduce the communication

capacity. It is known that RF pre-select filtering greatly relaxes the receiver linearity requirement and reduces the gain desensitization due to strong interferers. Also, for IR-UWB, filters used in transmitters can regulate the emission power of short duration pulses to comply with the FCC spectral mask and eliminate the use of additional pulse shaping circuits as in [93]. Therefore, low-loss, highly selective, and integrated passive UWB filters are very useful components in UWB RF front-end modules.

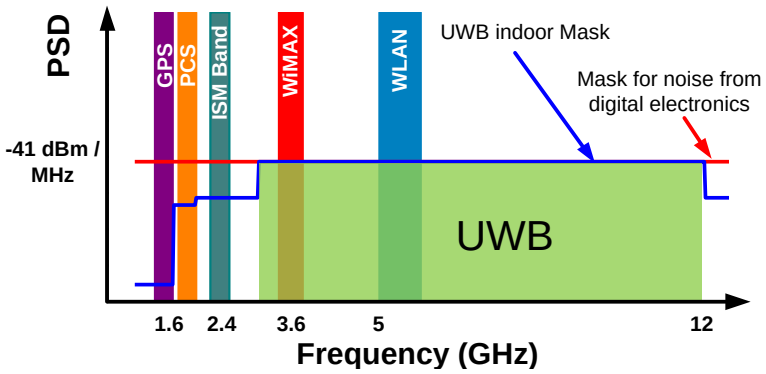
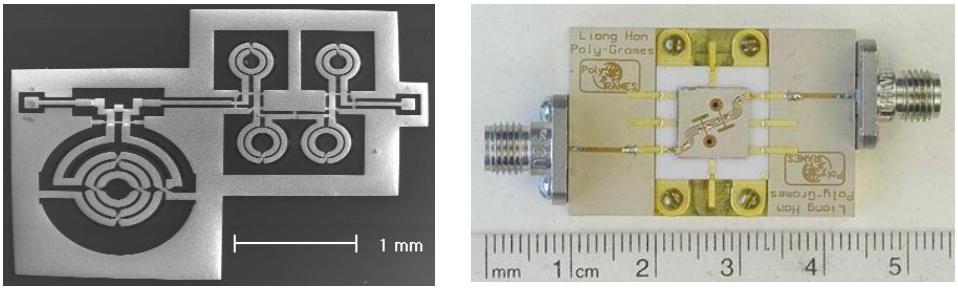


Figure 4.1. Ultra-wideband system spectrum distribution and co-existence with other wireless standards.

So far, reported works have focused on small-size UWB filter designs based on microstrip, coplanar waveguide (CPW), or quasi-lumped components on low-loss microwave substrates such as FR4, LTCC, or LCP [94]-[101]. Although size reduction has been achieved using various smart design techniques, these filters are developed mostly as stand-alone components. If these conventional filters are employed in UWB radio front-ends, the size and volume of a UWB microsystem will be still dominated by the passive microwave filter. In this work, silicon-based IPD is employed to implement low-loss and miniaturized UWB filters. The size of an IPD UWB filter in this work [102]

and a reported small-size microstrip UWB filter [95] can be compared in Figure 4.2, showing significant size reduction using the proposed technology. In addition, the proposed IPD technology has the capability of integrating other RF MEMS devices on-chip for implementing tunable filters. The tunable bandstop filters demonstrated in this work are also some of the most compact filters reported [103]-[110] that provide interference rejection of more than 20 dB (in 4.9 to 6.5 GHz frequency range) and low passband loss. Integration of a UWB filter bandpass filter with a tunable bandstop filter allows detect-and-avoid (DAA) mechanism, which can address the issue of in-band interferences in UWB communication.



(a) (b)

Figure 4.2. Comparison of filter size: (a) UWB filter design using silicon IPD in this work, and (b) conventional microwave filter design on low loss substrate [102].

4.2 Fabrication Process of the Integrated Passive Devices

Surface micromachining on a low-loss carrier substrate (including high resistivity silicon or fused silica) is used. Based on this process, RF MEMS tunable capacitors, switches, and high-*Q* inductors can be simultaneously fabricated. The fabrication process is shown in Figure 4.3. For proof-of-concept, high-resistivity silicon substrate (> 1 kΩ•cm) is adopted as the substrate material while still offering good performance. The

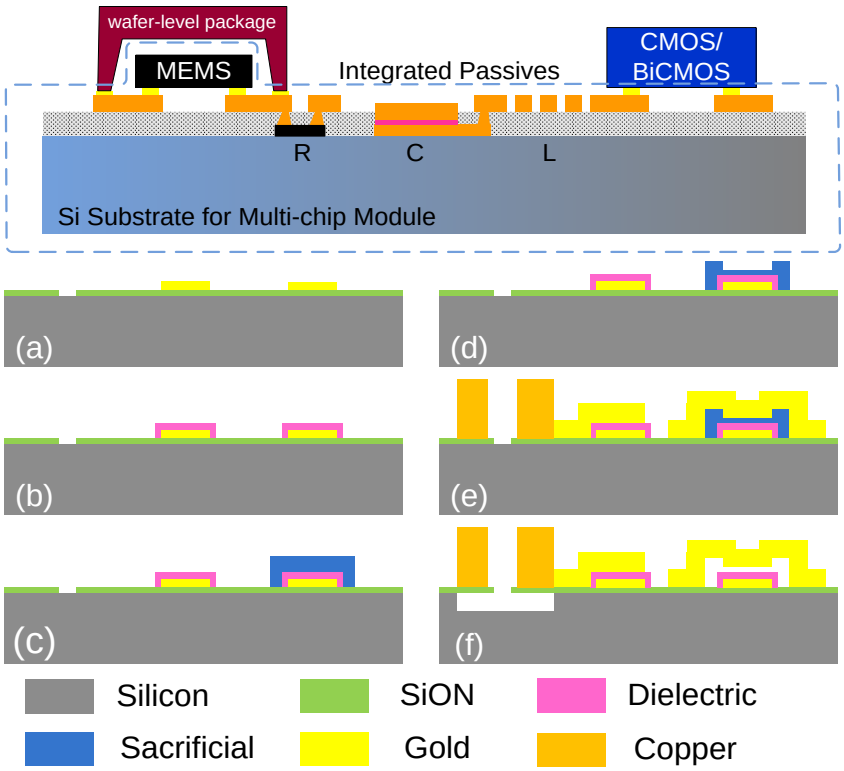


Figure 4.3. The process flow of the IPD technology on silicon substrate.

process starts with the deposition of a 2 μm-thick low- stress silicon oxynitride (SiON) dielectric layer as a surface passivation layer. The processing steps are: (a) deposition and patterning of gold as the bottom electrode; (b) deposition of a dielectric layer for MIM capacitors; (c) deposition and patterning of a PMMA sacrificial layer; (d) etching the sacrificial layer to form a step for realizing high tuning ratio MEMS tunable capacitors and ohmic-contact dimples; (e) gold electroplating for the top metal electrode of MIM capacitors; (e) thick copper electroplating to form high-Q inductive components; (f) dissolve the PMMA sacrificial layer in solvent to release the suspending membranes of RF MEMS devices. A xenon difluoride (XeF_2) gaseous etch can be further used to selectively remove the silicon substrate to reduce the substrate loss. With the selective

removal of substrate, a SiON dielectric membrane provides support for the metal structures for enhanced mechanical robustness. If fused silica substrates are used, substrate removal is not necessary due to the excellent insulation property and extremely low loss (loss tangent < 0.0001 at 1GHz) of silica. The sacrificial layer step etch in (d) allows the formation of dual gaps for high analog tuning range (> 4:1) MEMS capacitors, and contact dimples used in ohmic-contact MEMS switches. Due to the use of thin-film processes on silicon to fabricate the passive devices as well as RF MEMS devices, the tunable filters are suitable for flip-chip assembly or multi-chip module integration with CMOS ICs, which is desirable for the implementation of highly integrated RF front-end modules.

4.3 Design and Implementation of Filters

Using the proposed IPD technology, low-loss and miniaturized UWB bandpass filters are implemented. The filters are designed in co-planar configuration with proximate ground plane so that the electromagnetic field is confined on the surface of the substrate. Therefore, the performance of filters is not affected by backside metallization, variations in the substrate thickness, or the packaging layer.

To accurately predict parasitic effects of the co-planar filter configuration, filters are simulated using the HFSS full-wave electromagnetic simulation tool [111]. In all HFSS simulations, the conductivity of electroplated copper is taken as 4.9×10^7 S/m and the loss tangent and conductivity of the silicon substrate are assumed to be 0.004, and 1 kΩ·cm, respectively. In the following subsections, the design strategy of the UWB filters, tunable

bandstop filters, and UWB filter with an integrated tunable stopband will be introduced, and the simulation results of the filters will be compared with measured results.

4.3.1 Cascaded UWB Bandpass Filter

The bandpass filter implementation is based on a cascade of lowpass and highpass filter sections to define the UWB bandpass response. This filter design utilizes inductive coupling structures that are enabled by the integrating multiple passive devices on a single chip. Also, the IPD process is based on μm-precision lithography patterning, and tight control on the coupling structures is realizable. The availability of coupling structures demonstrates the benefits of having passive devices fully integrated even though discrete inductors can offer higher *Q*s.

The filter networks were synthesized from generalized Chebyshev configuration [112], providing steep rejection with a low order filter network. Figure 4.4 shows the circuit diagram of the highpass filter section. From filter synthesis and optimization, the highpass filter design can achieve a cut-off frequency of 3.1 GHz and out-of-band rejection of 30 dB below 2 GHz. The derived filter network contains a high-value inductor, L_3, in the T-junction, which can be eliminated by transforming the T-junction into a pair of mutually coupled inductors [113]. The component values for the coupled inductor pair are listed in Table 4.1. Mutual coupling (k) of 0.2 is difficult to implement using either tightly coupled interleaved structures [114] or loosely coupled proximate inductor pairs. Therefore, a custom-designed inter-winded inductor pair is used (Figure 4.4(b)). The inter-winded pair has tight coupling in the inner turns and weak coupling in the outer turns of the inductors, offering the desired mutual coupling of 0.2. The

relatively small size of these mutually coupled inductors is the main contributing factor in significant size reduction of the highpass filter.

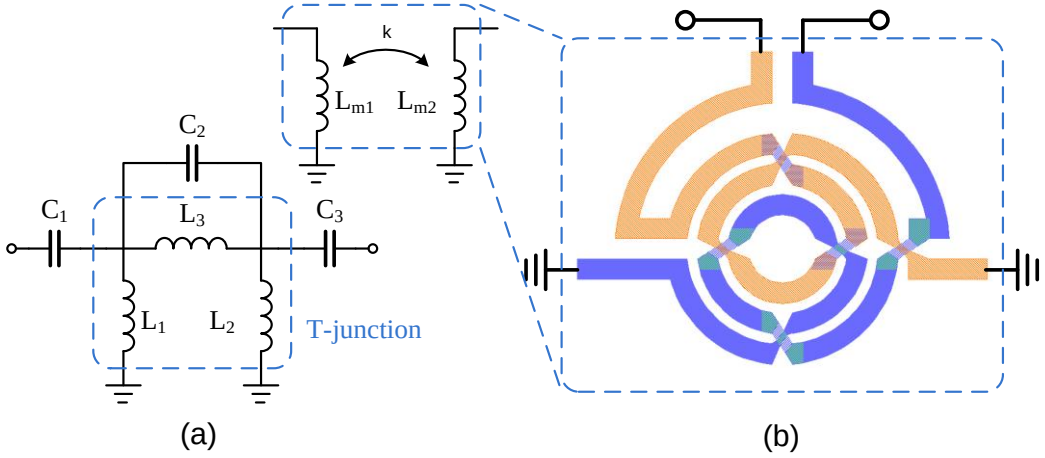


Figure 4.4. (a) Highpass filter circuit, and (b) layout of coupled inductors.

Table 4.1. Components in the Highpass Filter.

C_1 (C_3)	C_2	L_1 (L_2)	L_3	L_{m1} (L_{m2})	k
1.04 pF	0.825 pF	2.21 nH	8.83 nH	1.84 nH	0.2

The circuit diagram of the lowpass filter section of the UWB filter is shown in Figure 4.5. Inductors L_2 and L_3 are purposefully coupled by placing them in close proximity, as depicted in Figure 4.5(b). As a result, the transmission zero is moved close to the passband to improve the roll-off at the edge of the high-frequency cut-off. The component values used in the lowpass filter are listed in Table 4.2. It can be seen that the substrate parasitic capacitances in the filter can be absorbed into components C_1, C_2 and C_3 in the filter circuit, making it possible to realize a low-loss filter at frequencies up to 10 GHz with lumped components.

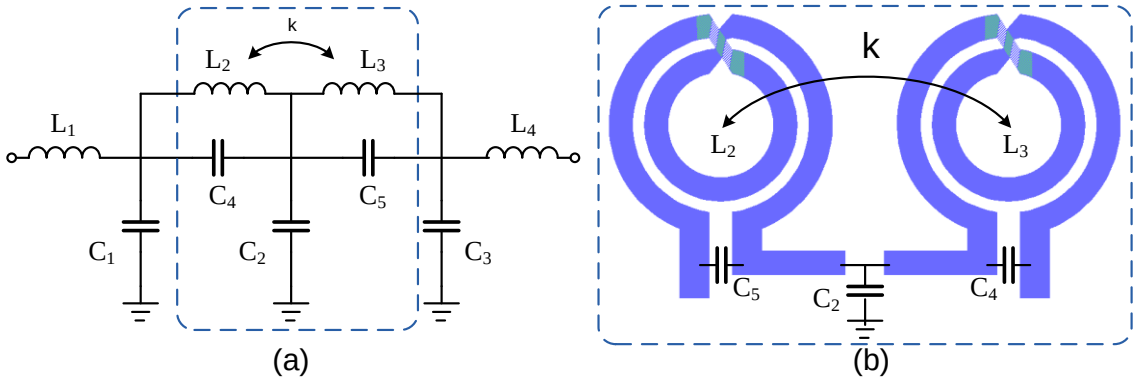


Figure 4.5. (a) Lowpass filter circuit, and (b) layout of the coupled inductor pair.

Table 4.2. Components in the Lowpass Filter.

C_1 (C_3)	C_2	C_4 (C_5)	L_1 (L_4)	L_2 (L_3)	k
0.361 pF	0.275 pF	1 pF	0.77 nH	1 nH	0.08

Using this design, the size of the UWB bandpass filter can be reduced to 2.9 mm × 2.4 mm while still maintaining a steep rejection response. The image of the fabricated cascaded filter is shown in Figure 4.6. Measured and simulated responses of a cascaded (highpass-lowpass) UWB bandpass filter on a micromachined silicon substrate are shown in Figure 4.7. The cascaded UWB filter has a bandwidth of 7.6 GHz (3-10.6 GHz) within which the return loss is better than 15 dB. The mid-band insertion loss of the filter is 1.1 dB (at 6.85 GHz). This filter exhibits an excellent out-of-band rejection of at least 30 dB at lower (< 2 GHz) and upper (> 13 GHz) sides of the passband. A spurious-free response up to 40 GHz is obtained. The group delay is less than 0.25 ns. Measured responses of the cascaded UWB bandpass on a solid silicon substrate are also plotted in Figure 4.8. The 3 dB bandwidth of the cascaded bandpass filter on a solid silicon substrate is 7.3 GHz (2.9-12 GHz). The minimum insertion loss is 1.4 dB, which is slightly higher than the filter on

a micromachined silicon substrate. The attenuation at lower (<2 GHz) and upper (> 12.5 GHz) sides of the passband is also better than 30 dB. As can be seen in the measured results, the design technique realizes low-loss UWB filters even on a solid silicon substrate, which is considered lossy for microwave filter implementations.

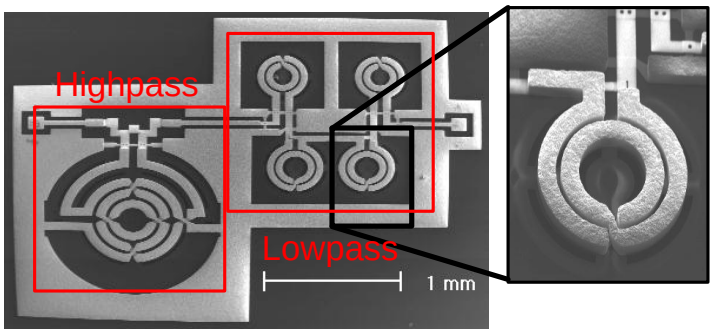


Figure 4.6. A SEM image of a cascaded bandpass filter on a micromachined substrate (size: 2.9 mm × 2.4 mm). Inset shows the inductor on a SiON membrane.

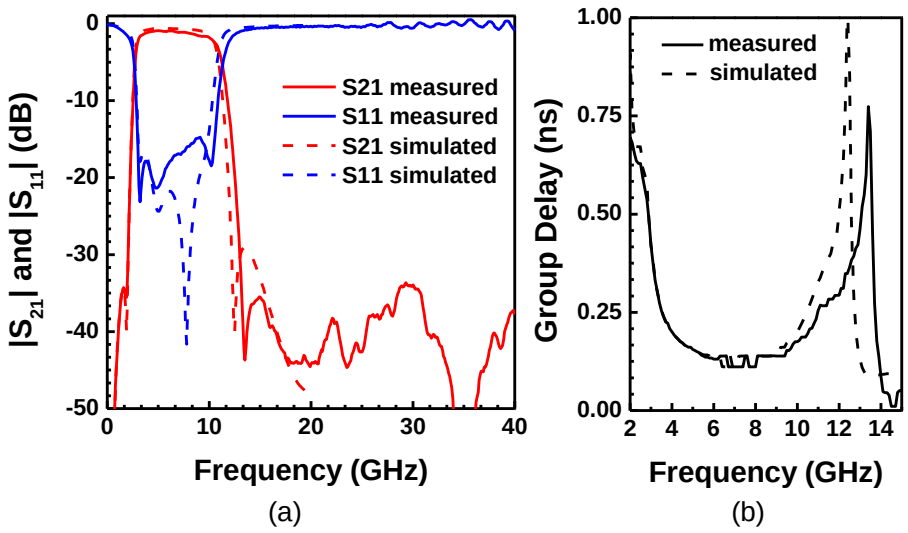


Figure 4.7. Measured response of the cascaded bandpass filter on a micromachined silicon substrate (silicon is removed beneath the inductors). (a) Insertion loss and return loss; (b) group delay.

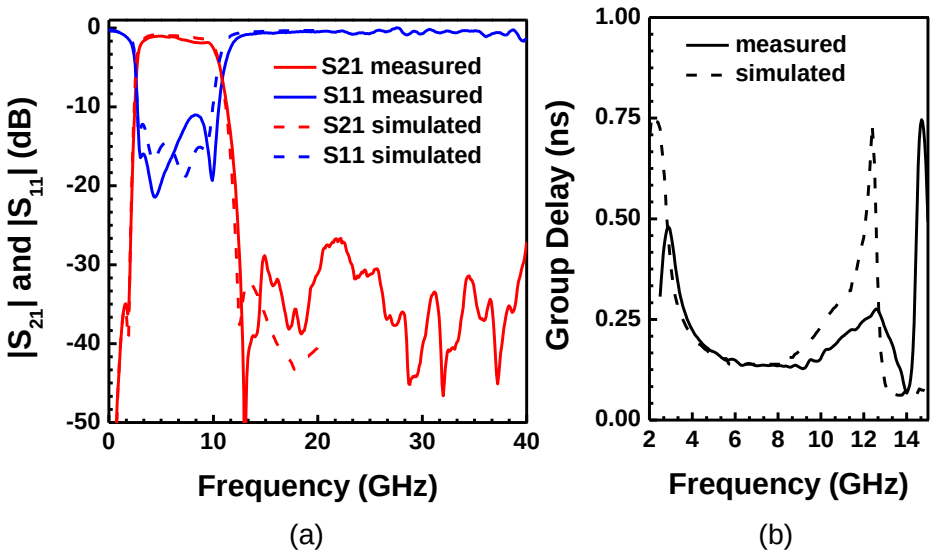


Figure 4.8. Measured response of the cascaded bandpass filter on a solid silicon substrate. (a) Insertion loss and return loss; (b) group delay.

4.3.2 RF MEMS Tunable Bandstop Filter

As shown in Figure 4.1, a UWB receiver front-end that relies on a bandpass filter may still suffer from strong in-band interferers. The center frequencies of in-band interferences may not be known in advance. Considering the IEEE 802.11a interferers, for example, narrow-band interferers can appear in a range of 4.9 GHz to 5.85 GHz. Therefore, a fixed bandstop filter cannot completely resolve the interference problem in UWB communication. It is also necessary that the bandstop filter has sufficient rejection level across the communication band of interferers. As such, tuning of a stopband filter with high rejection level is required to block un-known interferers. Reported works have been focused on the design of fixed-frequency narrow-band bandstop filters embedded with UWB bandpass filters [94], [98]-[100]. In this section, we demonstrate a tunable

bandstop filter that can be monolithically integrated with a UWB bandpass filter to mitigate the interference issue.

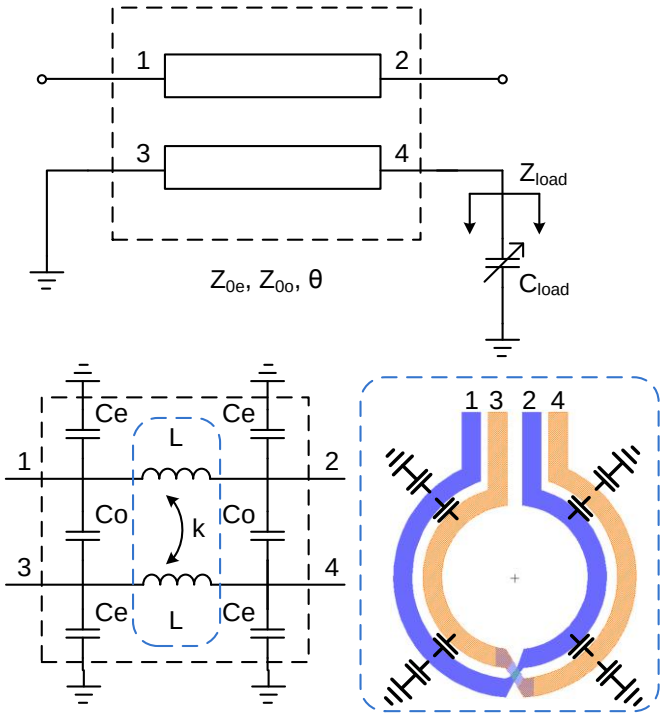


Figure 4.9. Circuit implementation of the bandstop filter.

The design of miniaturized bandstop filters in this work is based on the configuration of coupled transmission line bandstop filters [115]. As can be seen in Figure 4.9, a 1st-order bandstop filter cell is obtained by loading a pair of coupled transmission lines with a capacitor. If the even-mode and odd-mode impedances (Z_{0e} and Z_{0o}) of a coupled line are designed to match the port impedance Z_0 (Z_0 = 50 Ω), *i.e.*

$$Z_0 = \sqrt{Z_{0e} Z_{0o}}\,, \tag{4.1}$$

the four-port S-parameter matrix [S] of a pair of symmetrical coupled transmission line with electrical length θ can be written as [116]

$$[S]=\begin{pmatrix} 0 & \alpha & \beta & 0 \\ \alpha & 0 & 0 & \beta \\ \beta & 0 & 0 & \alpha \\ 0 & \beta & \alpha & 0 \end{pmatrix}, \tag{4.2}$$

where

$$\alpha = \sqrt{1-C^2}\,/\left(\sqrt{1-C^2}\cos\theta + j\sin\theta\right), \tag{4.3}$$

$$\beta = jC\tan\theta/\left(\sqrt{1-C^2} + j\tan\theta\right). \tag{4.4}$$

C is the coupling coefficient defined as

$$C=\left(Z_{0e}-Z_{0o}\right)/\left(Z_{0e}+Z_{0o}\right). \tag{4.5}$$

When Port 3 is grounded, the reflection coefficient at Port 3 is

$$\Gamma_{L3}=-1. \tag{4.6}$$

Further, when Port 4 is terminated with impedance Z_{load}, the reflection coefficient at Port 4 is

$$\Gamma_{L4}=\left(Z_{load}-Z_0\right)/\left(Z_{load}+Z_0\right). \tag{4.7}$$

With these terminations on Ports 3 and 4, the coupled line becomes a two-port network with S-parameters of

$$S_{11} = -S_{22} = -\frac{\beta^2}{1+\alpha^2\Gamma_{L4}}, \tag{4.8}$$

$$S_{21} = S_{12} = \alpha\left(1-\frac{\beta^2\Gamma_{L4}}{1+\alpha^2\Gamma_{L4}}\right). \tag{4.9}$$

When there is an ideal capacitive load (C_{load}) terminating Port 4, the two-port network is a bandstop network. By solving $|S_{21}|=0$, the stopband center frequency, ω_0 can be found.

$$\omega_0 C_{load} Z_0 \tan\theta = \sqrt{1-C^2}\,. \tag{4.10}$$

The bandwidth of the stopband can be found from (4.8), (4.9) and (4.10). For example, the -10 dB bandwidth of S_{21} can be obtained by solving $20\times\log(|S_{21}|) = -10$ dB. The -10 dB fractional bandwidth versus stopband center frequency is plotted in Figure 4.10 for various electrical lengths (θ) and coupling coefficients (C).

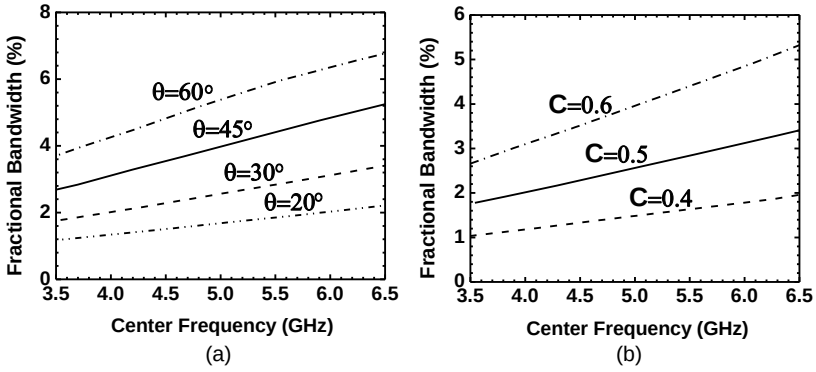


Figure 4.10. Fractional bandwidth (-10 dB) of the bandstop filter versus center frequency. (a) Different electrical lengths (θ) at 5.25 GHz, coupling coefficients (C) =0.5; (b) different C values, θ=30 ° at 5.25 GHz.

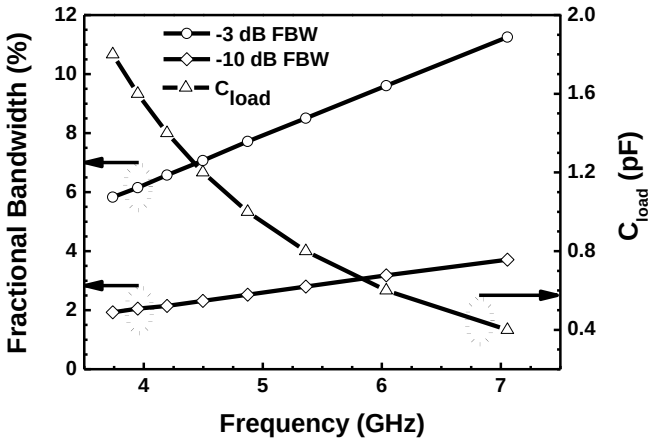


Figure 4.11. Fractional bandwidth and load capacitance (C_{load}) of the lumped notch filter versus center frequency.

To further reduce the filter size, the coupled transmission line section is transformed into a lumped LC coupler [117], as seen in Figure 4.9. Using this lumped transformation, narrow-band bandstop filters can be designed using low-value inductors, making it possible to optimize for high inductor Q-factor, small size, and improved filter shape compared to conventional bandstop lumped LC filter designs [103]-[105]. Although the lumped conversion is in principle a narrow-band approximation of the coupled transmission line configuration, the converted lumped network has low passband insertion loss up to very high frequencies. In designing the lumped coupled inductors, parasitic capacitors need to be taken into account as part of the even-mode (C_e) and odd-mode capacitances (C_o), as depicted in Figure 4.10. A lumped bandstop filter is transformed from a coupled line filter with electrical length (θ) of 31.5° at 5.25 GHz and coupling coefficient (C) of 0.51, which results in a pair of inductors with inductance of 0.93 nH and mutual coupling coefficient (k) of 0.51 (Table 4.3). If a tunable capacitor (C_{load}) with tuning range from 0.4 to 1.8 pF is used, the bandstop center frequency can be

tuned from 7 down to 3.7 GHz. The expected frequency tuning as well as the -3 dB and -10 dB fractional bandwidths across the tuning range is plotted in Figure 4.11.

Table 4.3. Component Values of the Tunable Notch Filter.

L	k	C_e	C_o
0.93 nH	0.51	98 fF	100 fF

Dual-gap MEMS tunable capacitors are employed to achieve continuous frequency tuning. As can be seen in the SEM image and cross-sectional view shown in Figure 4.12, the narrow center gap defines the tunable RF capacitor (C_{MEMS}) while the wider side-gap is used for electrostatic actuation. This configuration overcomes the pull-in effect of electrostatic actuators [118]. A fabricated dual-gap MEMS capacitor is tuned from 0.38 to 2.1 pF (5.5:1) when measured at 500 MHz (Figure 4.12). The equivalent circuit model of the RF MEMS tunable capacitor is plotted in Figure 4.12, and the equivalent component values are given in Table 4.4. The design of the MEMS capacitors involves several trade-offs among various parameters including Q, tuning voltage, linearity, power handling, and tuning speed. The most important parameter depends on the application and the capacitor design may be optimized to achieve a specific goal.

Table 4.4. Component Values in the MEMS Capacitor Model.

C_{MEMS}	L_{series}	R_{series}	C_{sub}	G_{sub}
0.38-2.1 pF	130 pH	0.36 Ω	55 fF	30 kΩ

There is no stringent requirement on the tuning speed of the bandstop filter if the existing interferences do not change frequently. Therefore, continuously tuned MEMS capacitors that offer a tuning speed on the order of 100 μs is reasonable for the filter

design. Low tuning bias voltage is preferred as it reduces the power consumption of DC converters and simplifies the implementation of the tuning bias circuit. However, a capacitor with low tuning bias suffers from insufficient power handling capability, as will be analyzed in the later section. The designed parameters of the RF MEMS tunable capacitor used in the tunable notch filter are summarized in Table 4.5.

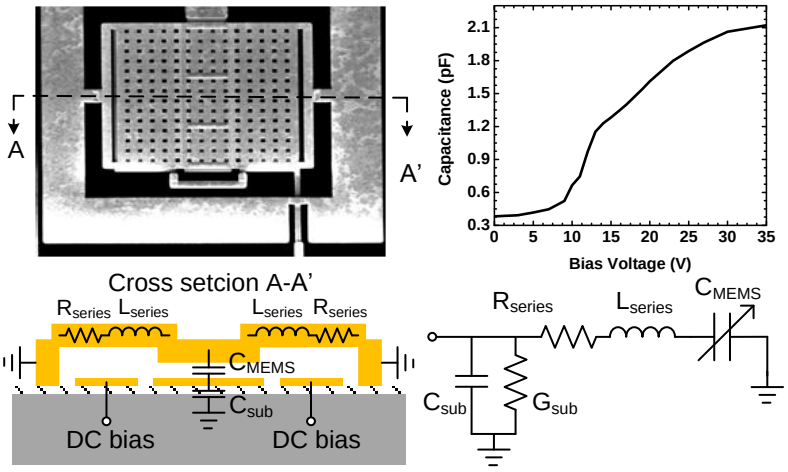


Figure 4.12. A SEM image, measured tuning results, cross-sectional view, and circuit model of a fabricated dual-gap MEMS capacitor.

Table 4.5. Parameters of Dual-gap MEMS Capacitor.

DC actuation area	$270 \times 70 \times 2\ \mu m^2$
RF capacitor area	$260 \times 70\ \mu m^2$
Initial DC actuation air gap (g_{DC0})	2 μm
Initial RF air gap (g_{RF0})	0.4 μm
Spring constant (k)	36 N/m
Mechanical Q	1
Resonance frequency (f_0)	9 kHz

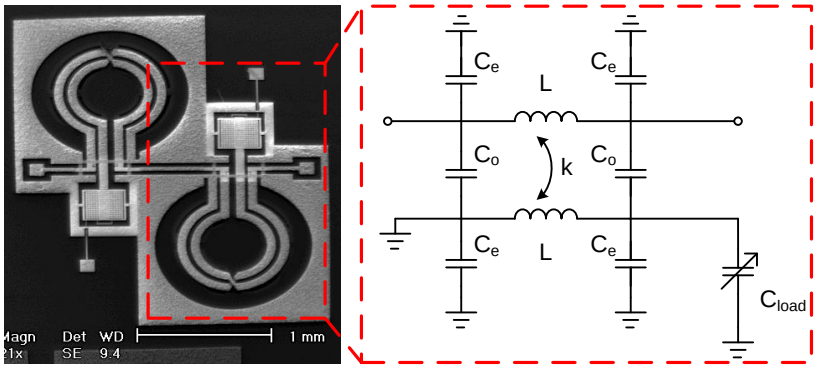


Figure 4.13. A SEM image of a fabricated two-pole tunable bandstop filter together with the circuit schematic of the tunable notch filter cell.

As can be seen in Figure 4.13, the RF MEMS tunable capacitor forms a series LC resonator in the bandstop filter. Also, the MEMS tunable capacitor has a series parasitic inductance, L_{series} (see Figure 4.13). The parasitic inductance of the MEMS capacitor is absorbed into the main inductor of the tank. Therefore, the Q of the MEMS capacitors is improved at high frequencies and the usable frequency range of the device is extended beyond the self-resonant frequency predicted by the conventional extraction method using Z-parameters: $|imag(Z_{12})|/real(Z_{12})=0$. A two-pole tunable bandstop filter is realized by cascading two 1st-order bandstop cells in Figure 4.13. The measured tuning characteristic of the two-pole bandstop filter is shown in Figure 4.14. A tuning range of 3 GHz (6.5 to 3.5 GHz) is achieved by applying a DC bias voltage up to 17 V to the MEMS capacitors. Further increasing the tuning bias voltage to 29 V achieves more than octave frequency coverage (6.5 GHz to 3.1 GHz). The tunable bandstop filter maintains low passband loss (< 1 dB) up to 13 GHz at all tuned states.

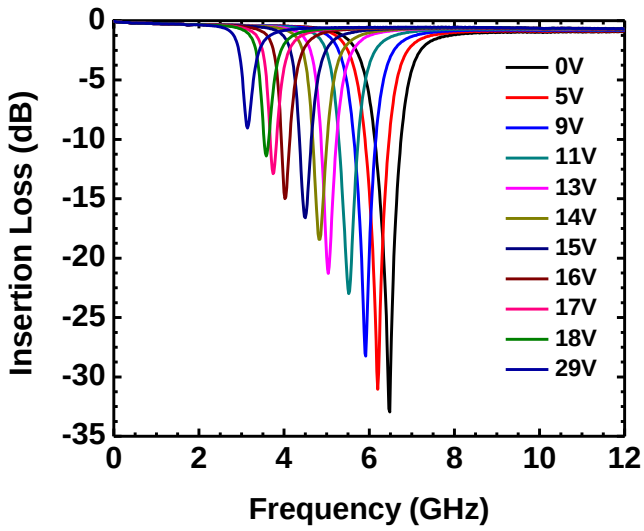


Figure 4.14. Measured tuning characteristics of a two-pole tunable bandstop filter.

The two-pole tunable bandstop filter is cascaded with a UWB bandpass filter (in Figure 4.15) to allow in-band interference rejection capability in a DAA capability in UWB communication. The measured and simulated responses of the filter at two tuning states are shown in Figure 4.16. The two states are set to reject the interferences from 802.11a, at either the IEEE 802.11a lower band (5.15–5.35 GHz) or the higher band (5.725–5.825 GHz). The measured rejection level of the tunable notch filter is better than 20 dB covering the 5–6 GHz Unlicensed National Information Infrastructure (U-NII) band. The UWB passband insertion loss is less than 2.7 dB. The size of the UWB filter integrated with the two-pole tunable notch filter is 4.8 mm × 2.9 mm (Figure 4.15).

The FCC indoor mask is overlapped on the filter responses in Figure 4.16. Although the current design does not fully satisfy the FCC mask, compliance to FCC mask can be met by slightly reducing the filter bandwidth to account for the brick wall passband transition. Table 4.6 compares the tunable filters in this work with other recently reported

works. As highlighted in the table, the UWB filters implemented in this work achieve a significant size reduction (of 10×) with a competitive performance. Also, monolithic tunable UWB filters are for the first time realized in a silicon IPD technology.

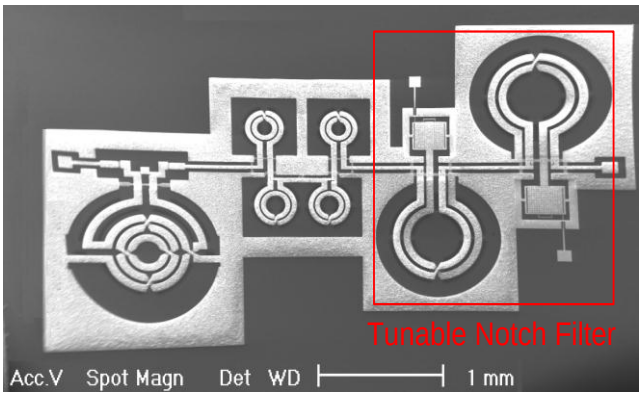


Figure 4.15. A SEM image of the fabricated UWB filter integrated with a two-pole tunable notch filter (overall size: 4.8 mm × 2.9 mm).

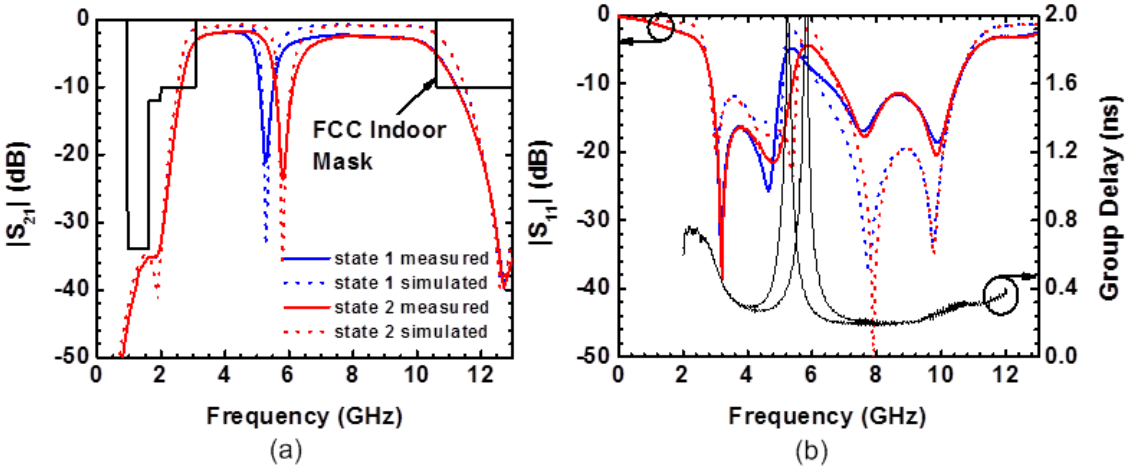


Figure 4.16. Measured and simulated responses of the UWB bandpass filter integrated with a two-pole tunable notch filter (State 1: notch center at 5.25 GHz; State 2: notch center at 5.8 GHz). (a) Insertion loss; (b) return loss and group delay.

Table 4.6. Comparison of UWB Filters with Narrow Stopband.

	[98]	[99]	[100]	[101]	This Work
Technology	Single layer PCB	Multilayer LCP	PCB (Hybrid Microstrip/CPW)	Multilayer LCP with GaAs varactors	Silicon IPD with RF MEMS
Filter Size	$22.2 \times 15.1 mm^2$	$37.6 \times 8 mm^2$	$16.2 \times 12.6 mm^2$	N/A	**$4.8 \times 2.9 mm^2$**
In-Band Insertion Loss (dB)	< 0.7 dB at center of sub-passband	0. 16 dB at 4.28 GHz; 0.54 dB at 7.08 GHz; 0.75 dB at 9.53 GHz	0.69 dB at lower 1.49 dB at middle 0.63 dB at upper	N/A	1.8 dB at lower 2.6 dB at higher
Group Delay (ns)	~ 0.5 ns at center of sub-passband	0.4 ns at 4.28 GHz; 0.14 ns at 7.08 GHz; 0.54 ns at 9.53 GHz	< 0.59 ns; < 0.36 ns variation	N/A	< 0.3 ns
Wide Stopband	No	Yes	10.3-15.1 GHz	N/A	**Up to > 40 GHz**
Notched-band and Rejection	32 dB at 6.6 GHz	26.4 dB at 6.4 GHz; 43.7 dB at 8.0 GHz	21.9 dB at 5.23 GHz; 24.0 dB at 5.81 GHz	N/A	21 dB at 5.25 GHz; 23 dB at 5.8 GHz;
Notch Tuning	fixed	fixed	fixed	Tunable: 4.5-6.5 GHz	**Tunable: 3.5-6.5 GHz**

4.3.3 Switchable Wide Tuning Range Bandstop Filters

In the previous section, a bandstop filter with a wide frequency tuning range has been demonstrated. Compared to tunable bandpass filters, bandstop filters exhibit lower passband insertion loss, minimizing the degradation of receiver noise figure, while providing high rejection level for removing interference signals. Therefore, tunable bandstop filters have the potential to replace more complicated and higher loss switched bandpass filter banks used in multi-band RF front-ends (Figure 4.17). In a cognitive spectrum utilization scheme, it is useful to switch off the bandstop filter in case no interference is present. When the filter is switched off, loss of wireless spectrum

resources introduced by the bandstop filter will be minimized and the available wireless spectrum can fully utilized. In this section, MEMS ohmic switches are exploited to add switch on/off capability to the wide tuning range bandstop filters. As shown in the circuit schematic of Figure 4.18, a MEMS ohmic switch is connected in parallel with the tunable capacitor. When the RF MEMS ohmic switch is in contact, it shorts the capacitive load port to ground. In this switched-off state, the filter becomes an all-pass network.

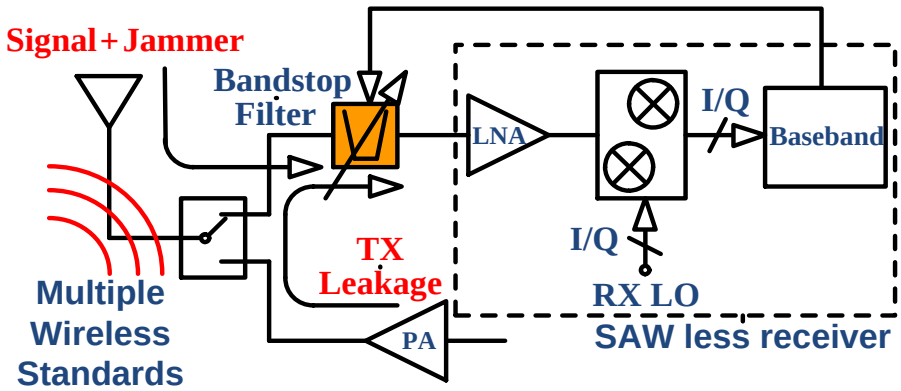


Figure 4.17. Schematic of a frequency-agile RF front-end with tunable bandstop filter.

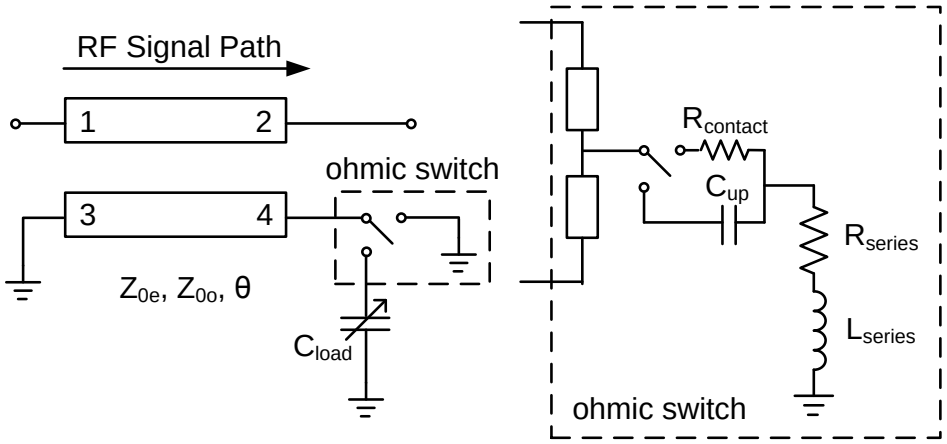


Figure 4.18. Circuit schematic of the tunable bandstop filter with switch on/off capability and the electrical model of the MEMS ohmic switch.

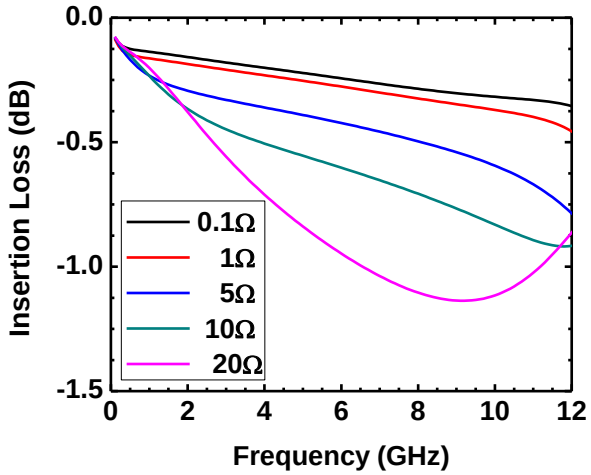


Figure 4.19. Insertion loss of the filter path when the bandstop filter is switched off using a MEMS ohmic switch.

In the proposed switchable bandstop filter design, the MEMS switch is placed in the coupled line section instead of in the main RF signal path (Figure 4.18). Therefore, the filter loss is less sensitive to the contact resistance of the ohmic switch. The pass-band insertion loss of the filter having different contact resistance ($R_{contact}$) for the switch is simulated and shown in Figure 4.19. Simulation results indicate that even with a contact resistance of 10 Ω, the insertion loss when filter is switched-off is less than 0.83 dB up to 10 GHz. Because of the low sensitivity to contact resistance, the switchable filter can also employ RF MEMS switches that use hard metals (*e.g.*, rubidium (Ru)) as the contact material to improve the life cycle reliability.

A SEM image of a fabricated switchable filter is shown in Figure 4.20. The RF MEMS ohmic switch is embedded in the capacitive load port, as can be seen in the close-up view show in Figure 4.20. The size of the switchable filter is 2.2 mm × 2.6 mm, close to the size of the tunable bandstop filter in Section 2.3.2. The measured response of the

filtering path when the bandstop filter is switched off is shown in Figure 4.21. With increasing actuation voltage on the switch, the contact resistance of the RF MEMS switch is reduced and the insertion loss of the switched-off bandstop filter is improved. The measured insertion loss is less than 0.84 dB up to 10 GHz. The higher insertion loss from the measured results is due to the higher resistance of the electroplated metal and fabrication imperfections that cause non-ideal electrical performance for the lumped coupled inductors. The measured bandstop filter responses at switch on/off states are compared in Figure 4.22.

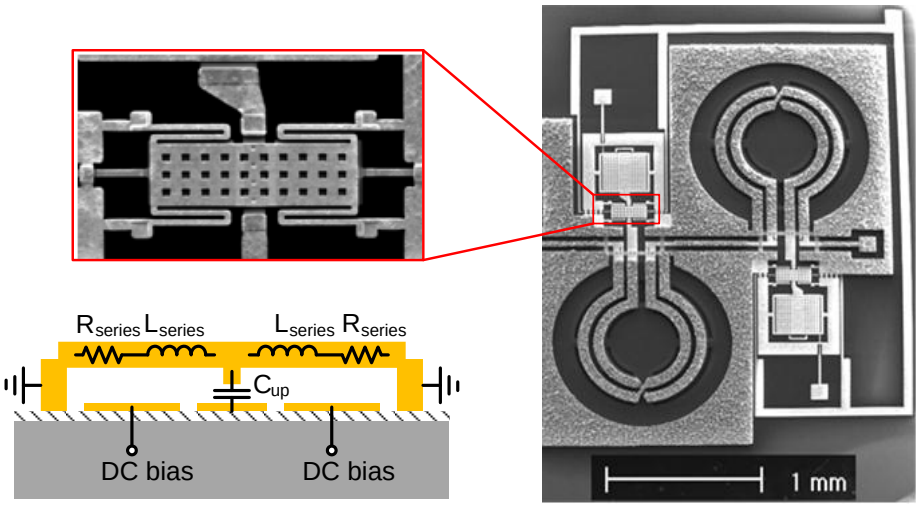


Figure 4.20. A SEM image of the fabricated tunable bandstop filter with closed-up view and circuit model of the RF MEMS ohmic switch (up-state).

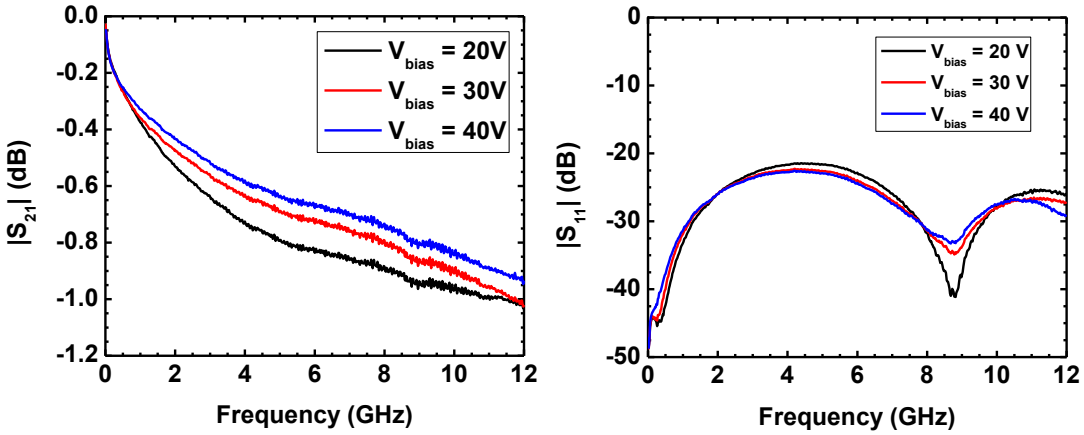


Figure 4.21. Measured responses of the switched-off bandstop filter with varied DC bias on MEMS ohmic switch; (a) Insertion loss, and (b) return loss.

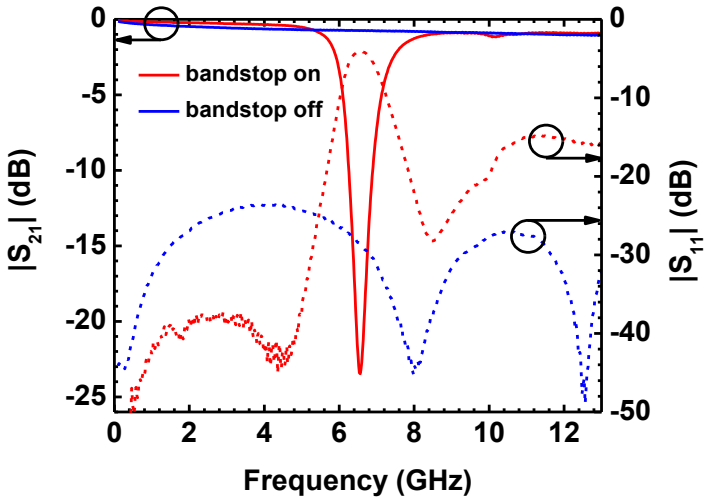


Figure 4.22. Insertion loss and return loss when the bandstop filter is switched-on and switched-off (a 30 V bias on ohmic switch).

4.3.4 Power Handling and Linearity of RF MEMS Tunable Filters

In addition to small-signal performance, power handling and linearity are also important performance metrics for tunable RF filters. The RF signal that passes through

RF MEMS devices has an effective DC bias and causes self-actuation. As a result, at higher RF powers, the tuning range of the MEMS capacitor will be limited [119]. In addition, inter-modulation signals are generated due to the nonlinearity of MEMS devices [118], [120]. It should be noted that the AC voltage swing across a MEMS capacitor in a tunable LC circuit is amplified by the Q of the LC tank. Therefore, estimation of the power handling and linearity performance is essential when designing tunable filters.

The power handling of a MEMS capacitor is limited to an RF power level that causes the membrane to pull-in [118]. The maximum RF voltage that can be applied to a dual-gap MEMS capacitor at various DC bias before pull-in is analyzed according to [118]. As shown in the inset of Figure 4.23, the dual-gap MEMS capacitor used in the tunable bandstop filter has separated RF and DC electrodes, with g_{DC0} as the initial DC actuation gap and g_{RF0} as the initial RF capacitor gap. The electrostatic actuation force (F_e) due to both the DC bias and the RF signal can be written as

$$\begin{aligned} F_e &= \frac{1}{2}\frac{\varepsilon_0}{\left(g_{DC0}-x\right)^2}{V_{DC}}^2 + \frac{1}{2}\frac{\varepsilon_0}{\left(g_{RF0}-x\right)^2}\left[V_{RF}\sin\left(\omega_{RF}t\right)\right]^2 \\ &= \frac{1}{2}\frac{\varepsilon_0}{\left(g_{DC0}-x\right)^2}{V_{DC}}^2 + \frac{1}{4}\frac{\varepsilon_0}{\left(g_{RF0}-x\right)^2}{V_{RF}}^2 \\ &\quad -\frac{1}{4}\frac{\varepsilon_0}{\left(g_{RF0}-x\right)^2}{V_{RF}}^2\cos\left(2\omega_{RF}t\right) \end{aligned} , \tag{4.11}$$

where x is the displacement of the membrane, V_{DC} is the DC bias voltage, V_{RF} and ω_{RF} are the amplitude and angular frequency of the RF signal, respectively. ε_0 is the air permittivity. The mechanical response of the MEMS capacitor due to electrostatic force (F_e) is

$$m\frac{d^2x}{d^2t}+b\frac{dx}{dt}+kx=F_e, \tag{4.12}$$

where m is the mass of the movable membrane, b is the damping coefficient, and k is the spring constant. The second term of Equation (4.11) describes the effective electrostatic force due to the RF signal which causes self-actuation. As the dual-gap MEMS capacitor has small center air gap (g_{RF0}), it is more sensitive to RF self-actuation. In a straightforward treatment, the power handling of the MEMS capacitor is limited to an RF power level that causes the membrane to pull-in [118]. The maximum RF voltage that can be applied to a dual-gap MEMS capacitor at various DC bias before pull-in can be solved by

$$F_{tot}=\frac{1}{2}\frac{\varepsilon_0}{(g_{DC0}-x)^2}V_{DC}{}^2+\frac{1}{4}\frac{\varepsilon_0}{(g_{RF0}-x)^2}V_{RF}{}^2-kx=0, \tag{4.13}$$

$$\partial F_{tot}/\partial x<0. \tag{4.14}$$

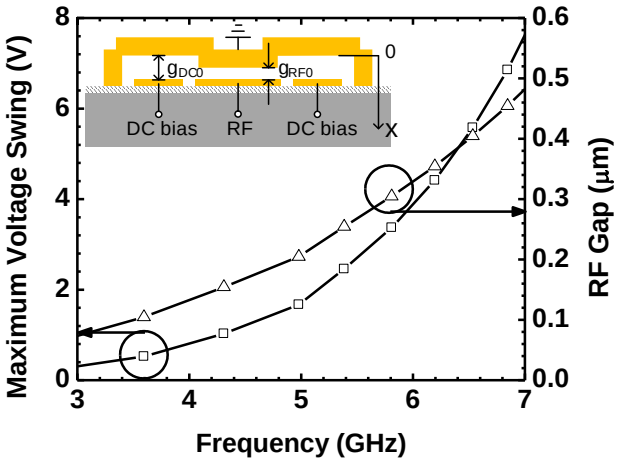


Figure 4.23. Maximum allowed RF voltage swing (peak-to-peak voltage) of the bandstop filter.

For the designed dual-gap MEMS capacitor of Figure 4.12, the maximum tolerable RF voltage swing (peak-to-peak voltage) versus center frequency of the stopband is plotted in Figure 4.23. As can be seen, the maximum allowed RF voltage swing is larger than 1.6 V if the bandstop filter is tuned to center frequencies above 5 GHz. Therefore, the tunable bandstop filter in this work is suitable for UWB receivers. Higher power handling can be achieved by increasing the stiffness of the RF MEMS capacitors at the cost of increasing DC bias for tuning.

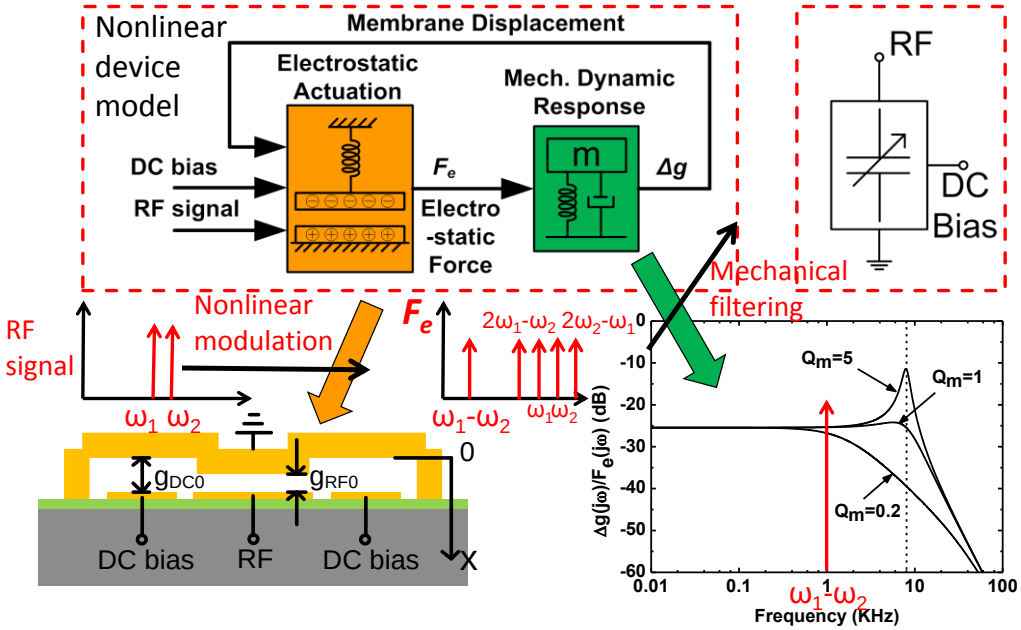


Figure 4.24. Principle of the physical-based nonlinear model for a dual-gap RF MEMS capacitor.

To study the linearity performance of the RF MEMS tunable bandstop filter, a nonlinear model is developed for the MEMS capacitor following the method reported in [121]. Modifications are made to accurately reflect the dual-gap configuration as well as

the separate DC bias and RF electrodes using the device characteristics summarized in Table 4.5. The physical-based nonlinear model for the dual-gap MEMS capacitor is explained in Figure 4.24. The nonlinearity comes from the electrode static actuation force induced by an RF signal on the MEMS capacitor. According to Equation (4.11), the transfer of the RF voltage (V_{RF}) to the electrostatic actuation force (F_e) involves a nonlinear characteristic that generates intermodulation tones. Afterwards, the transfer of F_e to the movement of air gap (Δg) experiences a lowpass filtering due to the dynamic response of the suspending membrane (*i.e.* a "spring-mass-damping" system). The membrane displacement further causes a capacitance change, which again follows a nonlinear function. The nonlinear MEMS capacitor model is included in the two-pole tunable bandstop filter to predict the linearity and the large signal behavior. The bandstop filter is tuned to 5.25 GHz, a typical tuning state to reject the interference from WLAN. Agilent ADS [122] Harmonic Balance simulation is used to predict the filter large signal behavior. In simulations, two-tone signals are applied to the bandstop filter with center frequency of 5.25 GHz, frequency offset of 1 kHz, and input power of -10 dBm (amplitude of 0.1 V across a 50 Ω termination). Because of the high resonator Q, the voltage swing at 5.25 GHz across the tunable capacitor is amplified to more than 0.5 V peak-to-peak. The displacement of the MEMS capacitor membrane under such two-tone input is plotted in Figure 4.25. As shown, the displacement fluctuation of the MEMS capacitor membrane under such high voltage swing (0.5 V) is less than 3.5 nm. This is due the fact that the membrane has a mechanical resonant frequency of less than 10 kHz (Table 4.5). The lowpass mechanical response of the MEMS device significantly

attenuates the high frequency membrane vibration. The observed membrane movement is a response to the inter-modulations that generate a signal tone at 1 kHz and excite the capacitor membrane through electrostatic force in the RF gap (as explained in Figure 4.24). When applying two-tone signals with larger frequency offsets (> 10 kHz), the frequency of the inter-modulation tone (ω_1-ω_2) is beyond the mechanical resonant frequency of the membrane and even smaller vibration is expected.

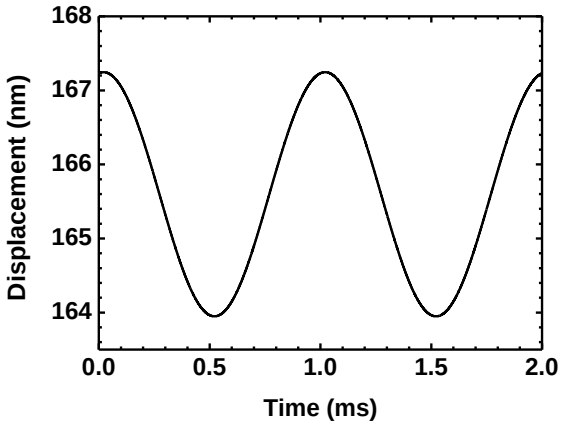


Figure 4.25. Displacement of the tunable capacitor membrane at input power of -10 dBm.

Using two-tone Harmonic Balance simulations in ADS, the output spectrum of the UWB filter integrated with tunable bandstop filter is plotted in Figure 4.26. The two-pole bandstop filter is tuned to 5.25 GHz when the two-tone inputs have a center frequency of 5.25 GHz and input power of -10 dBm. In Figure 4.26 (a) and (b), two-tone inputs with a frequency offset of 1 kHz and 10 MHz are applied, respectively. It can be observed that there is higher harmonic output power around 5.25 GHz when two-tone inputs have 1 kHz offset. However, such inter-modulation tones are still within the center of the stopband, and they do not sit in the communication band. As can be observed in Figure

4.26(b), when the frequency offset of the two-tone input (10 MHz) is far beyond the mechanical resonant frequency of the MEMS capacitor (*i.e.* 9 kHz), the inter-modulation signals are highly attenuated. Therefore, very low-power inter-modulation tones are observed in Figure 4.26(b). Another situation considers the nonlinear distortion of input signals within the passband of the bandstop filter. As shown in Figure 4.27, the coupled-line bandstop filter has the property that a very weak portion of the input signal power is coupled to the MEMS capacitor when the signal is out of the stopband. The coupling strength is determined by the coupling coefficient (C) in (2.5) in the bandstop filter design. With a two-tone input with offset frequency of 1 kHz is applied within the passband, the simulated IIP3 is +48 dBm, which is beyond the measurement range of the equipment used in the work. The analysis indicates good linearity performance of the tunable bandstop filter by using RF MEMS capacitors even with low tuning bias design.

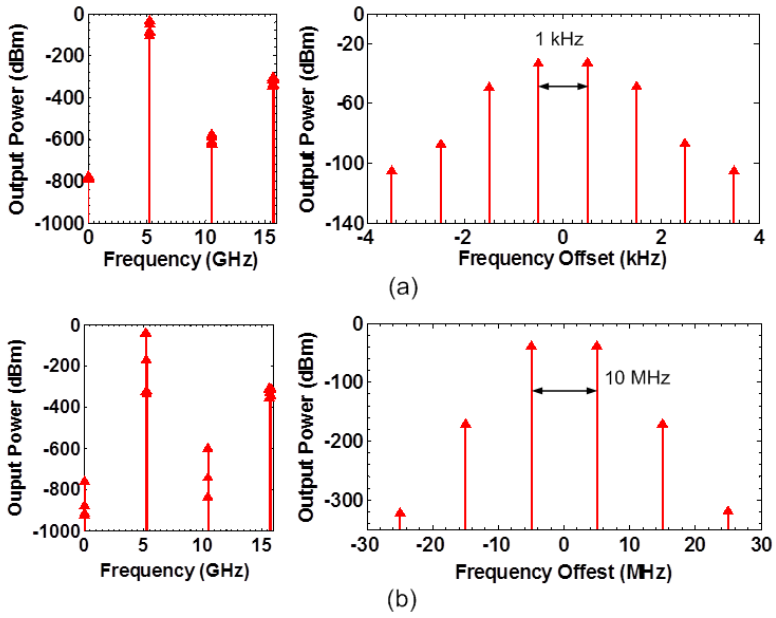


Figure 4.26. Simulated output spectrum when a two-tone input is at the center of stopband with offset frequency of (a) 1 kHz, (b) 10 MHz.

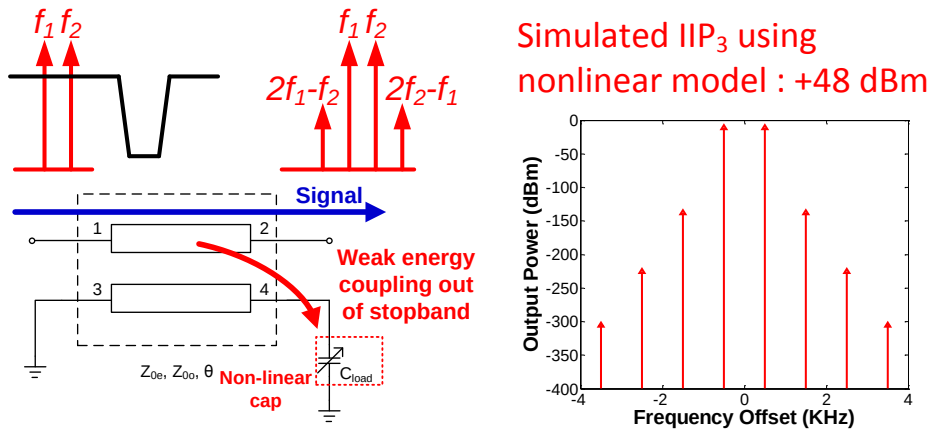


Figure 4.27. Simulated output spectrum when a two-tone input with offset frequency of 1 kHz is applied within the passband of the bandstop filter.

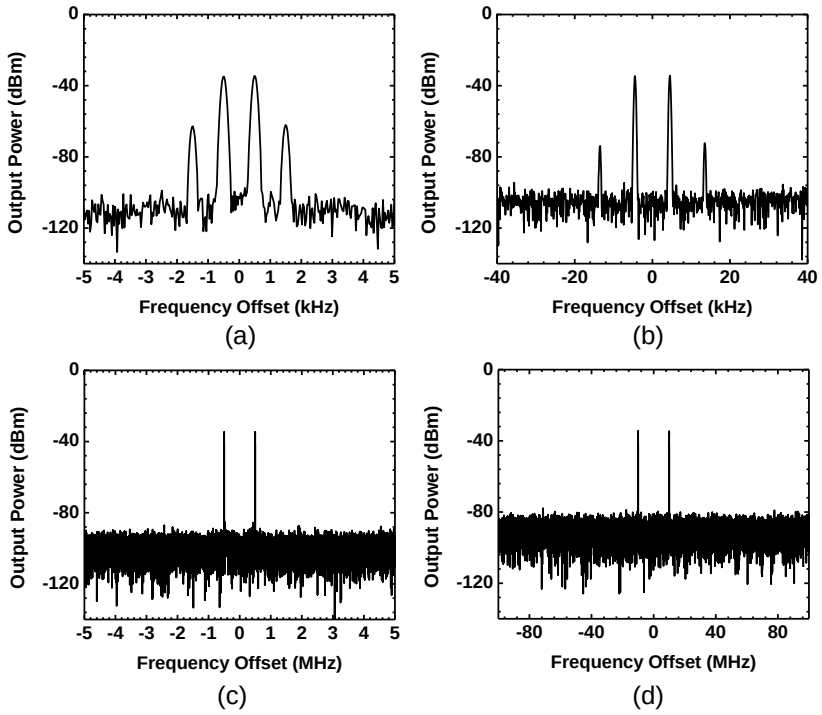


Figure 4.28. Output spectrum with input offset of (a) 1 kHz, (b) 9 kHz, (c) 1 MHz, and (d) 20 MHz.

Two-tone measurements are also carried out to verify the inter-modulation outputs generated from the tunable bandstop filter. A two-tone input is applied at the center frequency of 5.25 GHz with input power of -10 dBm when the two-pole tunable notch filter is tuned to 5.25 GHz. The measured output spectra with frequency offset of 1 kHz, 9 kHz, 1 MHz, and 20 MHz are shown in Figure 4.28(a)-(d). It can be found that inter-modulation output terms are attenuated as the input frequency offset increases, which is consistent with the simulation results using the nonlinear RF MEMS model. The extracted third–order input intercept point (IIP3) from the measurement is +10 dBm at 9 kHz frequency offset. The low mechanical *Q* of the membrane helps with avoiding linearity degradation when frequency offset is equal to the membrane natural resonance frequency. Significant linearity improvement can be obtained by using higher stiffness MEMS capacitor design or MEMS switched capacitors. Although low bias voltage MEMS capacitor design is employed in this work, it is shown that the power of inter-modulation terms generated is low enough not to cause interference across the whole passband. These nonlinear analysis results show unique benefits of RF MEMS devices used in tunable bandstop filters.

4.3.5 Temperature Stability

The temperature stability of the integrated passive filters is examined using a temperature-controlled probe station. The frequency response of the UWB bandpass filter is measured from to -30 ℃ to 70 ℃. The frequency stability of the UWB passband edges are plotted in Figure 4.29. It can be observed that the passband edges are very stable under the temperature change, and the rejection level of the filter is maintained.

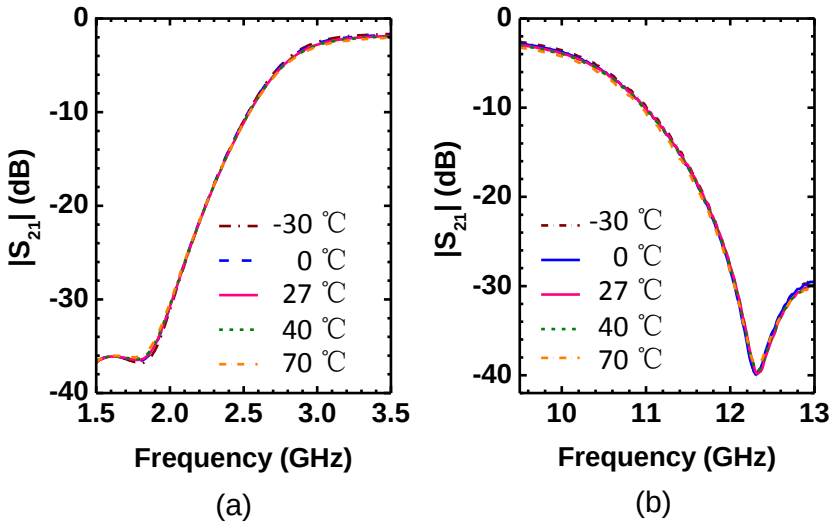


Figure 4.29. Frequency stability of the UWB bandpass filter edges. (a) Highpass edge; (b) lowpass edge.

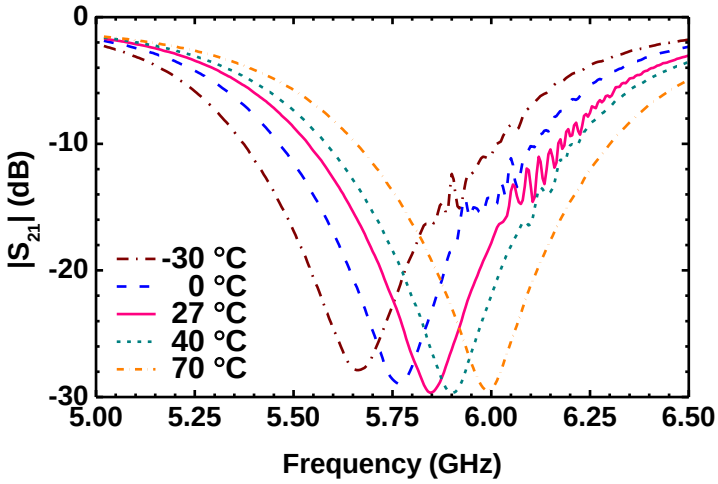


Figure 4.30. Frequency responses of the two-pole tunable notch filter at different temperatures.

A two-pole tunable bandstop filter implemented with RF MEMS capacitor is also characterized under temperature change (Figure 4.30). The bandstop filter is tuned to 5.8 GHz at room temperature. It can be seen that the measured center frequency drift is 5.6%

when temperature is changed from -30 ºC to 70 ºC. The frequency shift because of temperature change is significantly smaller than the electrostatic frequency tuning range, which is more than 60%. Therefore, frequency change due to temperature drift can be compensated by adjusting the bias on the tunable notch filter. Improvement to the temperature stability of the RF MEMS tunable notch filter can be achieved using a temperature-stable RF MEMS design [123].

4.4 Summary

In this chapter, low-loss, miniaturized, and tunable RF filters are implemented using an integrated passive device technology. The filter design exploits significant EM coupling enabled by precise lithographic patterns to significantly reduce the overall size. The UWB filters demonstrated in this chapter occupy significantly smaller die area (by a factor of ten) compared to other reported state-of-the-art UWB filters, while offering a competitive performance. Using this technology, miniaturized UWB bandpass filters as well as tunable/switchable bandstop filters are demonstrated on a silicon chip, exhibiting high performances and small size. The features of these filters make them suitable candidates for use in highly integrated and frequency-agile RF front-end modules.

CHAPTER 5.

Conclusion and Future Directions

5.1 Thesis Contributions

The research described in this thesis provides the following key contributions:

1. Investigation on fused silica as a new material for realizing high-performance micromechanical resonators and integrated MEMS timing references.
   - An aluminum nitride thin-film process is combined with fused silica DRIE technology to realize piezoelectric-on-silica MEMS resonators. A piezoelectric-on-silica resonator is demonstrated with high Q (Q > 20,000), low motional impedance (Rm ~400Ω), and good power handling capability. The achieved $f \times Q$ product of this resonator is the highest amongst reported micromachined silica/fused quartz resonators.
   - A CMOS reference oscillator is implemented using the piezoelectric-on-silica MEMS resonator. The MEMS oscillator exhibits low phase noise at a low-supply voltage. The oscillator noise performance is comparable to state-of-the-art silicon MEMS oscillators. Also, this is the first reported electrical oscillator that uses a fused silica MEMS resonator interfaced directly to a CMOS IC.
   - Temperature-stable operation of the fused silica oscillator is realized by integrating the MEMS resonator on an ovenized platform. The fused silica device-

fusion platform is designed to enable low-power ovenization. The thermal properties and temperature *servo*-control circuits for device-layer ovenization are studied. This was the first demonstration of active TCF compensation applied to oscillators using fused silica resonators.

2. Development of passive TCF-compensation method and thermal isolation structures based-on silicon MEMS. Active TCF-compensation on MEMS oscillators is realized by utilizing the intrinsic frequency drift of MEMS for temperature sensing and low power oven-control.
    - An oxide refill process is demonstrated to fabricate TCF-compensated MEMS resonators and thermal isolation platforms.
    - The PLL-based active compensation technique is demonstrated on a MEMS oscillator with an overall frequency drift within +/- 4 ppm across a working temperature range of -40 ℃ to 70 ℃ without the need for system calibration.
    - CMOS circuits for the PLL-based oven-control system are implemented, achieving near-zero phase noise invasion on the MEMS oscillators.
    - Thermal properties of the two-resonator system are analyzed, and non-ideal effects that cause residual frequency drift are discussed. Design considerations for realizing ultra-stable MEMS frequency references using PLL-based active compensation are investigated.
3. Development of a micromachining process on silicon that simultaneously integrates MEMS tunable capacitors, inductors, and MEMS ohmic switches on the same chip.

- Implementation of low-loss integrated UWB filters on silicon substrates with filter size 10× smaller than the current state-of-the-art.
- Implementation of an octave tuning range bandstop filters. The tunable bandstop filter is integrated with a UWB filter to address in-band interferences in UWB communication. The bandstop filter is further demonstrated with switchable function by utilizing MEMS ohmic switches integrated on the same chip.

5.2 Future Research Directions

The research in this thesis has contributed to the improvement in the performance of RF front-ends and integrated timing units using novel materials, devices, and circuits. Based on the results achieved in this thesis, possible directions for future research are suggested as following:

1. On the PLL-based active compensation method for MEMS oscillators, new device concepts and circuit techniques can be pursued to further improve the frequency stability. On the MEMS side, a two-oscillator temperature sensing scheme can be improved by designing better MEMS devices. The non-ideal thermal properties inherent in the two-resonator platform can be significantly mitigated by using a dual-mode MEMS resonator instead. On the circuit side, the design of low phase noise MEMS oscillators using a dual-mode MEMS resonator needs to be investigated. Instead of using conventional electrical filter (such as a LC tanks) to select and simultaneously excite different vibration modes, the mode-selection can be also realized by designing a MEMS resonator with specific input-output phase responses to aid the mode-selection (such as the coupled-ring

resonator that shows both in-phase and out-of-phase resonance modes). For the PLL circuits used in oven-control, more digital-assisted circuits can be explored instead of the all-analog design presented in this thesis. The benefit of going toward mixed-signal is to further eliminate the use of external RC components in the loop filter, hence, achieving extreme miniaturization for the final MEMS-IC microsystem. Also, calibration can be easily done using digital functions on a CMOS chip for mitigating known offset errors. Although digital-assisted active compensation introduces quantization errors, it is expected that excellent frequency stability can still be achieved with a moderate resolution required for the analog-to-digital conversion or frequency-to-digital conversion circuits. By further exploiting the mixed-signal design, PLL-based active compensation can be done without even heating a thermal platform or a MEMS device. The active compensation can be implemented using an open loop method if the temperature sensing using a MEMS resonator can achieve very good accuracy and repeatability. The system without ovenization can further reduce the power consumption. In the meantime, the thermal isolation structure provided by MEMS technology can be employed as a thermal filter to improve the dynamic stability under external thermal shock or fast transients in external temperature.

2. On the tunable RF MEMS side, more innovative MEMS-based RF circuits can be explored by employing both MEMS tunable capacitors and MEMS ohmic switches. A combination of both types of devices in a design potentially enables better re-configurability, extended frequency coverage, and better performance,

while the concerns for parasitic effects, cost, and area can be avoided by integrating all devices on the same chip using the developed micromachining process in this work. Potential areas of research include tunable filters, reconfigurable antennas, and adaptive matching networks for RF power amplifiers.

3. If various types of MEMS devices are integrated all together in a heterogeneous platform, a broader picture of research is to treat all types of MEMS devices as a standard design library for circuit or architectural-level innovations. If the features of individual MEMS devices are combined in a smart way, the technology will further enable significant improvements to conventional hardware architectures. The micromachining fabrication processes in this thesis needs to be combined enabling a complete heterogeneous platform with both piezoelectric layers and tunable structures.

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