Amorphous In-Ga-Zn-O Thin-Film Transistors for Next Generation Ultra-High Definition Active-Matrix Liquid Crystal Displays

by

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To my family, especially my parents, Yung-Fu Yu and Hsiu-Ming Liu,
for all the sacrifices they have made to provide for our family.

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ABSTRACT

Title: Amorphous In-Ga-Zn-O Thin-Film Transistors for Next Generation Ultra-High Definition Active-Matrix Liquid Crystal Displays

Chair: Professor Jerzy Kanicki

Next generation ultra-high definition (UHD) active-matrix flat-panel displays have resolutions of 3840×2160 (4K) or 7680×4320 (8K) pixels shown at 120 Hz. The UHD display is expected to bring about immersive viewing experiences and perceived realness. The amorphous In-Ga-Zn-O (a-IGZO) thin-film transistor (TFT) is a prime candidate to be the backplane technology for UHD active-matrix liquid crystal displays (AM-LCDs) because it simultaneously fulfills two critical requirements: (i) sufficiently high field-effect mobility (μ_{FE} = 10 $cm^2/V{\cdot}s$) and (ii) uniform deposition in the amorphous phase over a large area.

We have developed a robust a-IGZO density of states (DOS) model based on a combination of experimental results and information available in the literature. The impact of oxygen partial pressure during a-IGZO deposition on TFT electrical properties/instability is studied. Photoluminescence (PL) spectra are measured for a-IGZO thin films of different processing conditions to identify the most likely electron-hole recombination. For the first time, we report the PL spectra measured within the

a-IGZO TFT channel region, and differences before/after bias-temperature stress (BTS) are compared.

To evaluate the reliability of a-IGZO TFTs for UHD AM-LCD backplane, we have studied its ac BTS instability using a comprehensive set of conditions including unipolar/bipolar pulses, frequency, duty cycle, and drain biases. The TFT dynamic response, including charging characteristics and feedthrough voltage (ΔV_P), are studied within the context of 4K and 8K UHD AM-LCD and compared with hydrogenated amorphous silicon technology. We show that the a-IGZO TFT is fully capable of supporting 8K UHD at 480 Hz. In addition, it is feasible to reduce a-IGZO TFT ΔV_P by controlling for non-abrupt TFT switch-off.

CHAPTER 1

Introduction

1.1 Overview and Background

1.1.1 Current status of backplane technology for ultra-high definition active-matrix liquid crystal displays

In the first decade of the twenty-first century, the active-matrix liquid crystal display (AM-LCD) became the dominant display technology over the plasma display panel and the cathode-ray tube monitor. During the same period, video image specifications made the leap from 480i standard definition (640×480 pixels, interlaced) to 1080p full high-definition (Full HD, 1920×1080 pixels, progressive scan) recorded/shown at 60 frames per second. Despite the emergence of active-matrix organic light-emitting diode (AM-OLED) technology, the AM-LCD is expected to hold over 95% of the TV market and 70% of the mobile display market by 2017 [1].

In 1995, the NHK (Japan Broadcasting Corporation) Science & Technology Research Institute started research on the next generation digital video format, dubbed Super Hi-Vision [2]. It was defined as 3840×2160 pixels (4K) or 7680×4320 pixels (8K) displayed at a frame rate of up to 120 Hz. Studies in human visual perception have shown that the sensation of immersion ("being-there") and perceived realness (real objects and images become indistinguishable) can be achieved when field-of-view (FOV) approaches

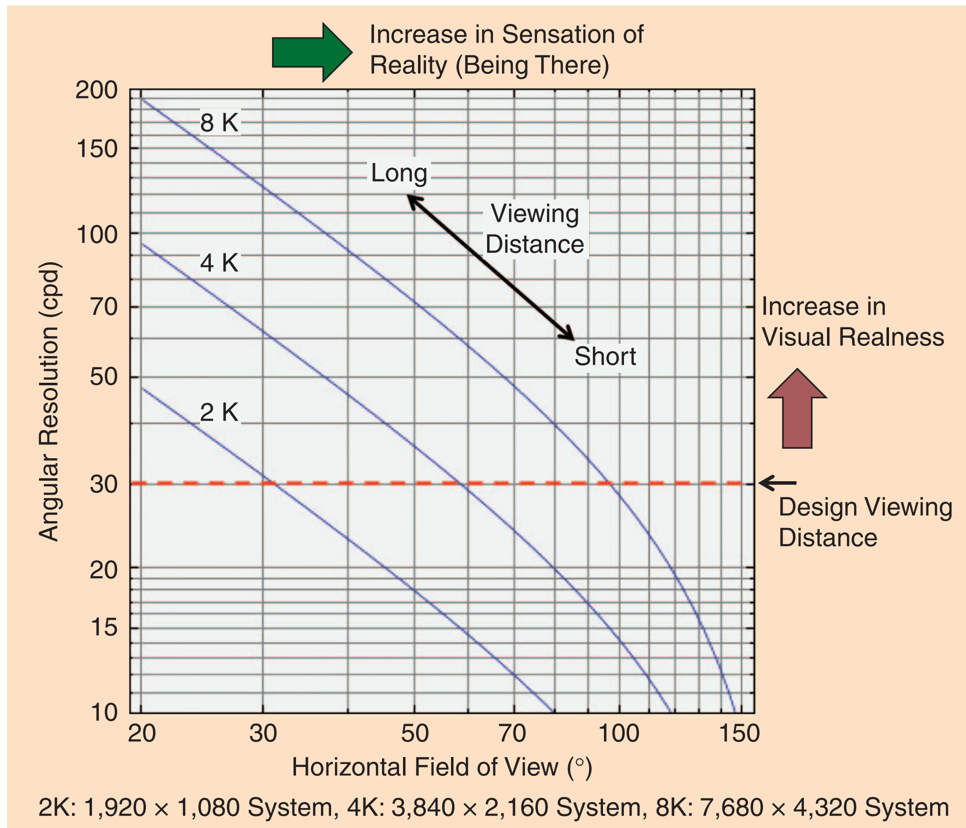


Figure 1.1 The field-of-view and the corresponding angular resolution offered by various AM-FPD resolutions when viewed at the optical distance for any given display size [6].

100° and angular resolution exceeds 30 cycles/degree (cpd) [3]–[5]. For a fixed angular resolution and viewing distance, FOV is increased for greater pixel count. According to Figure 1.1, assuming the minimal 30 cpd and a fixed optimal viewing distance for any given panel size, the FOV increases to 60° and 100° for 4K and 8K resolutions, respectively [6]. In addition, the frame rate is increased to 120 Hz to reduce the motion blur of moving images, further enhancing the viewing experience. In 2012, Super Hi-Vision, or Ultra High Definition (UHD) everywhere outside of Japan, was formally adopted by the International Telecommunications Union as Recommendation BT.2020 for next generation information displays [6], [7].

At time of writing, 4K UHD TVs are just beginning to enter the market while 8K UHD TVs are several years away from commercialization. Table 1.1 lists the

Manufacturer	Model	Size	Resolution @ Frame Rate	MSRP
Sharp	UD27U	70”	3840×2160 @ 60 Hz	$3600
Sony	X950B	65”	3840×2160 @ 60 Hz	$6000
Samsung	HU9000	65”	3840×2160 @ 60 Hz	$6000
LG	UB9800	65”	3840×2160 @ 60 Hz	$6000

Table 1.1 List of commercially available 4K UHD TVs as of April 2015.

4K TVs from the major manufacturers on the market as of April 2015, along with their size, suggested retail price, and maximum supported display specifications. The challenge with very high resolution on a large area (over 40”) display is multifaceted. Manufacturing yield decreases with higher number of pixels—a single defective pixel could potentially ruin an entire substrate. Another issue is RC line delay on the select and data bus lines, where a large number of pixels makes the margin of error for accommodating signal propagation delays on a large substrate even smaller [8]. These are all solvable with process engineering or design improvements, such as low-resistivity Cu bus lines [9] and dual-sided row drivers [10]. A more fundamental problem, and one more difficult to overcome without modifying display production lines, is the AM-LCD thin-film transistor (TFT) backplane. In active-matrix addressing, an array of TFT pixel circuits directly drives and charges the individual liquid crystal cells. This addressing method significantly reduces cross talk between neighboring pixels and enables far greater resolution compared to passive-matrix addressing. Presently, the two mainstream TFT backplane technologies are hydrogenated amorphous silicon (a-Si:H) and low-temperature poly-silicon (LTPS).

A-Si:H TFTs can be fabricated with a simple 4–5 mask process, enabling low production costs with very high throughput. Its uniform amorphous deposition over a

large area makes it suitable for large LCD TVs, currently produced on Gen 10 (2.8 m × 3 m) glass substrates. However, its low field-effect mobility (μ_{FE}) of 0.5–1 $cm^2/V \cdot s$ is only adequate for up to 1080p Full HD and insufficient for UHD TV specifications.

On the other hand, the LTPS TFT has μ_{FE} of around 100–200 $cm^2/V \cdot s$, which well exceeds the requirements for 4K and 8K UHD at 120 Hz. Electrical stability, which directly impacts display lifetime and pixel circuit complexity, is also much better for LTPS than a-Si:H TFTs. The biggest weakness of LTPS TFT technology is the non-uniformity of electrical properties due to polycrystalline grain boundaries, which are typically on the order of 0.3–3 μm depending on process conditions. The single most critical step in the fabrication of LTPS TFT is the crystallization of amorphous silicon into polysilicon. Today, this can be achieved by several different methods, each with its own advantage and disadvantages: excimer-laser annealing (ELA) [11], sequential lateral solidification (SLS) [12], metal seeding [13], or solid-phase recrystallization [14]. Despite its excellent electrical properties and stability, LTPS recrystallized from any growth method suffers from the necessary trade-off between cost and performance. This is particularly evident in the well-established ELA process: uniformity improves with more irradiations by the excimer laser at a cost of reduced productivity and throughput. In order to produce uniform LTPS TFTs with μ_{FE} = 100 $cm^2/V \cdot s$ on a Gen 4 glass substrate, two scans across the whole substrate is required due to the limited beam length, with each unit processing area irradiated 10–20 times by the laser for each scan—more irradiations corresponds to better electrical properties. Furthermore, additional non-uniformity is introduced in the area of overlap between each scan, making production of large area displays extremely challenging. Non-uniformity of electrical properties over a

Requirement	a-Si:H	LTPS	a-IGZO
Large-Area Uniformity	Good	Poor	Good
Mobility	Poor 0.5–1 $cm^2/V \cdot s$	Excellent 100-200 $cm^2/V \cdot s$	Good 10-20 $cm^2/V \cdot s$
Electrical Stability	Poor	Excellent	Better than a-Si:H
Process Complexity & Cost	Low	High	Lower than LTPS

Table 1.2 Comparison of different active-matrix flat panel display backplane technologies for ultra-high definition television.

large substrate will manifest itself as uneven patches of changes in luminance, known as *mura* (Japanese for blemish). It is evident that a new backplane technology is needed to satisfy the requirements of backplane technology for large-area UHD AM-LCDs.

Since the publication of the seminal paper by Nomura *et al*. in 2004 [15], the ternary oxide semiconductor amorphous In-Ga-Zn-O (a-IGZO) has emerged as a strong candidate to be the backplane technology for next-generation UHD AM-LCDs. The a-IGZO has μ_{FE} = 10 $cm^2/V \cdot s$, which is substantially higher than that of a-Si:H, and it can be uniformly deposited in the amorphous phase over a large substrate area. In amorphous covalent semiconductors such as a-Si:H, electrons conduct through highly directional sp^3 bonds, which are severely impacted by bonding angle variations and thus have very low μ_{FE} [16]. In an ionic semiconductor like a-IGZO, the μ_{FE} is higher than most other amorphous materials because conduction occurs through the overlapping s orbital of the metal ions—in this case the large In^{3+} ion. In addition, a-IGZO TFT has a low off-state leakage current (I_{off}), can be processed with 4–5 masks, is transparent within the visible-light spectrum, and has better electrical stability than a-Si:H TFTs [15], [17]–[19]. The

pros and cons of each backplane technology in the context of requirements for UHD AM-LCD are summarized in Table 1.2.

1.1.2 Requirements for UHD AM-LCD Backplane Technology

In evaluating TFT backplane technology for application to next generation UHD AM-LCDs, the following should be considered:

- For large-area UHD LCD TVs, the μ_{FE} should be sufficiently high to ensure that each row of liquid crystal is charged/discharged to the correct data voltage level within one gate selection time. The gate selection time is simply equal to 1/(Frame Rate × Number of Rows), which would correspond to 3.8 μs for 4K UHD at 120 Hz. Incomplete charging/discharging directly leads to grayscale errors and image retention. The charging characteristics can be roughly estimated as a RC exponential effect i.e. $V = V_{data}\,(1-\exp(-t/RC))$. After $t = 5RC$, V would have reached 99.3% of the target V_{data} and can be considered as fully charged. The effective resistance and capacitance are given by

  $$R = R_{data} + R_{on} = R_{data} + \frac{L}{WC_G\mu_{FE}(V_{GS}-V_{th})}, \quad (1\text{-}1)$$

  and

  $$C = C_{st} + C_{LC} + C_{GS} + C_{data}, \quad (1\text{-}2)$$

  where R_{data} is the data bus line resistance, R_{on} the TFT on-resistance, W and L the TFT channel width and length, C_G the TFT gate insulator capacitance, V_{GS} the applied gate pulse amplitude, C_{st} the storage capacitance, C_{LC} the liquid crystal capacitance, C_{GS} the TFT parasitic capacitance, and C_{data} the data bus line parasitic capacitance. Assuming a 50" AM-LCD with Cu bus lines, and negligible

C_{data} and C_{GS}, we can estimate that μ_{FE} should be at least 1.5 $cm^2/V \cdot s$ in order to fully charge all the pixels in a 4K UHD AM-LCD operating at 120 Hz. This value is just above the typical 1 $cm^2/V \cdot s$ achievable for a-Si:H TFTs, but can be easily fulfilled with the a-IGZO TFT.

- In order to support a very large display (> 50”) in which the gate and data bus line resistances may become significant, adoption of low resistivity metals such Al (ρ = 4 μΩ·cm) or Cu (ρ = 2.5 μΩ·cm) may become necessary. Because Cu has been shown to be relatively unstable and may diffuse during device processing [20], a compatible TFT fabrication process should be developed if not already available.
- To achieve higher pixel density for UHD AM-LCD resolution without sacrificing the aperture ratio, the TFT should be scaled down accordingly. As mentioned in the previous section, when the resolution on a 50” LCD TV increases from Full HD to 8K UHD, the size of each subpixel reduces by a factor of 16 to 144 μm × 48 μm. In the same way, the TFT W and L should both be reduced to 1/4 to maintain similar I_D–V_{GS} characteristics while keeping aperture ratio the same. In this case, to ensure proper TFT operation, the source/drain (S/D) contact resistance should be as low as possible and/or the TFT μ_{FE} needs to be sufficiently high. In a short-channel TFT, μ_{FE} becomes lower because the S/D contact resistance (R_{SD}) dominates channel on-resistance. Baek *et al.* has shown that in the high-performance coplanar homojunction a-IGZO TFT with highly-conductive S/D contact regions formed by hydrogen doping, the S/D contact resistance is negligible [21]. In such a device configuration, the a-IGZO TFT μ_{FE} = 13.1 $cm^2/V \cdot s$ did not degrade even when L = 5 μm.

- The pixel feedthrough voltage (ΔV_P), a dc voltage drop at the pixel electrode that is responsible for flicker and image retention, should be made as low as possible. While flicker may be offset with row-, line-, or dot-inversion driving methods, reducing ΔV_P to approximately 0.1 V is critical for minimizing image retention. In addition, it would be beneficial to display engineers if the magnitude of ΔV_P can be reliably predicted based on driving waveform and TFT configuration. A typical voltage divider equation

  $$\Delta V_P = (V_{GH} - V_{GL}) \frac{C_{GS}}{C_{GS}+C_{st}+C_{LC}} \quad (1\text{-}3)$$

  can be used to estimate ΔV_P to the first order, but is inadequate for in-depth analysis due to contributions from accumulated channel charge. A more robust model should be developed and evaluated for the UHD AM-LCD TFT backplane technology.

- The TFT backplane should be sufficiently reliable against pulsed (ac) bias-temperature stress (BTS) corresponding to AM-LCD addressing conditions. In a previous-generation 60-Hz Full HD (1920×1080) AM-LCD display, the select (gate) pulse for each row has pulse width of 16 μs, and the pulse amplitude is typically +13/−13 V. For such an operating condition, Chiang *et al*. showed that it would take approximately 10 years for the a-Si:H TFT threshold voltage shift (ΔV_{th}) to reach the nominal end-of-life limit for AM-LCDs [22]. In UHD AM-LCD operation, the gate driving waveform is expected to have higher frequencies (for higher refresh rates), shorter pulse widths (for larger number of rows), and higher gate bias amplitude (for faster pixel charging). These are all

stress conditions that should be addressed in the TFT backplane technology for UHD AM-LCDs.

- A robust DOS model based on experimental observations should be developed for use in numerical simulations. The model should be able to accommodate a wide variety of fabrication conditions and reflect them on the DOS parameters.
- For low-cost mass-production, the fabrication process should be simple and the mask count should be as low as possible while preserving electrical properties and reliability.

1.1.3 Current Status of Amorphous In-Ga-Zn-O TFTs for UHD AM-LCDs

Despite its obvious advantages, the a-IGZO TFT is still not yet the mainstream backplane technology for AM-LCDs. This is primarily due to the need to improve manufacturing yield and uncertainties in both device processing and achieving consistent electrical performance and stability. Although companies such as LG [23], AU Optronics [24], and Sharp [25] have demonstrated large-area 4K or 8K UHD AM-LCD prototypes with a-IGZO TFT backplanes, much work remains to be done towards their large-scale commercial production.

In amorphous semiconductors such as a-Si:H, localized states within the energy band gap arise from structural disorder (bond angles and length variations), dangling bonds, non-stoichiometry, and carrier scattering at defect sites [16], [26]. Such subgap density of states (DOS) dominates the electrical properties and stability of a-Si:H TFTs. Today it is generally accepted that the DOS can also impact a-IGZO TFT electrical performance, although the microscopic origin of DOS in a-Si:H and a-IGZO should be very different. Hsieh *et al*. extracted the density of acceptor-like states near the conduction band

minimum (E_C) in a-IGZO by fitting TFT current–voltage (I–V) data to technology computer-aided design (TCAD) simulations originally developed for a-Si:H technology [27]. Nomura *et al*. observed a large density of subgap states near the valence band maximum (E_V), possibly the origin for the lack of p-type operation, using hard X-ray photoelectron spectroscopy [28]. Below the band gap, optical absorption spectrum showed tail-like decay that can be described by the Urbach relation, although its characteristic energy slope in the literature varies with sample quality and preparation [28]–[30]. Kamiya *et al*. and Chen *et al*. performed first-principles calculations using density functional theory and found that for IGZO, oxygen vacancies form fully occupied donor levels located at 1 eV above E_V [29], [31]. Temperature-dependent TFT characteristics can also be used to extract DOS near the E_C, as shown by Chen *et al*. with the Meyer-Neldel rule [32] and Lee *et al.* with trap-limited conduction at low-temperature (77 K) [33]. For the next-generation a-IGZO-backplane active-matrix flat-panel display to be realized, a robust a-IGZO DOS model is needed for the design of devices and circuits using 2D numerical and SPICE simulations, respectively.

In order for a-IGZO TFTs to be widely adopted as the backplane technology for UHD AM-LCDs, its threshold voltage (V_{th}) stability under BTS, a critical factor for robust AM-LCDs with long lifetimes, should be evaluated in detail. Steady state (dc) positive and negative BTS, both in the dark and illuminated, have been the subject of much theoretical and experimental research effort and are well-documented [34]–[37]. Our group previously reported that the dc BTS-induced ΔV_{th} instability of the a-IGZO TFT is significantly lower than that of the a-Si:H TFT [38], in agreement with experimental data in published literature. Although there is substantial work on the dc BTS stability of a-

IGZO TFTs, the steady-state condition is not an accurate representation of AM-LCD operation, which biases the transistors in positive and negative alternating (ac) pulses. A direct comparison of ac and dc BTS on a-Si:H TFTs shows that dc BTS reliability is a poor predictor of ac BTS ΔV_{th} [22]. Thus there is strong motivation to study and verify ac BTS behavior such that the lifetime of UHD displays with a-IGZO TFT backplane technology may be properly evaluated.

Several methods have been proposed to improve TFT electrical stability, such as thermal annealing [28], [39], [40], hydrogen incorporation [41], nitrogenation [42], [43], passivation [44]–[46], among other methods [47]–[51]. However, the microscopic origin of V_{th} shift is still not yet completely understood. A hypothesis proposed in the literature suggests that oxygen-related sub-band gap states, such as oxygen vacancies, are responsible for the V_{th} instability under BTS [52], [53]. To clarify the origin of V_{th} shift from an atomic-bonding point of view, X-ray photoelectron spectroscopy studies have been reported for oxygen 1s states [40], [41], [54]–[56]. Results indicated that the higher binding energy peak of oxygen 1s states is related to smaller ΔV_{th} induced by BTS. It was assumed that higher oxygen flow during channel layer formation caused more oxygen to be incorporated into the final a-IGZO thin film, and this was found to significantly impact device BTS stability [57], [58]. However, more work is needed to ascertain the role of oxygen incorporation in a-IGZO thin film and its impact on device performance and stability.

In addition to electrical reliability, the actual dynamic operation characteristics of a-IGZO TFTs for AM-LCD pixel electrodes should be fully evaluated. Improvements to display resolution and frame rate both correspond to shorter time margin available for

each pixel to complete charging, thus placing stringent requirements on TFT dynamic response. The dynamic response of the a-Si:H TFT pixel electrode has been studied extensively in literature. The ΔV_P, which results from gate-source overlap capacitance (C_{GS}) and channel charge redistribution, is the main source of image flickering in AM-LCD operation and a key metric in TFT dynamic response [59]. Takabatake *et al.* reported a robust analytical model for ΔV_P that is very consistent with experimental values [60]. Kitazawa *et al.* investigated the impact of a-Si:H TFT device structural differences on ΔV_P [61]. Aoki conducted a comprehensive study detailing an analytical model of a-Si:H TFT dynamic operation with the liquid-crystal cell capacitance included, and the model has been verified by experimental data [62]. Lee *et al.* studied the dynamic response of a-Si:H TFT for AM-OLED pixel electrode, and reported in detail ΔV_P and charging time (t_{ch}) for various TFT structures and waveform parameters [63]. Our group has previously described preliminary results on the dynamic response of a-IGZO TFT pixel electrodes in terms of its C_{st} and TFT dimension dependences [64]. Initial data suggest that a-IGZO TFT showed very favorable dynamic characteristics when operated at a very high frequency. To date, however, comprehensive studies of a-IGZO TFT dynamic response are still lacking.

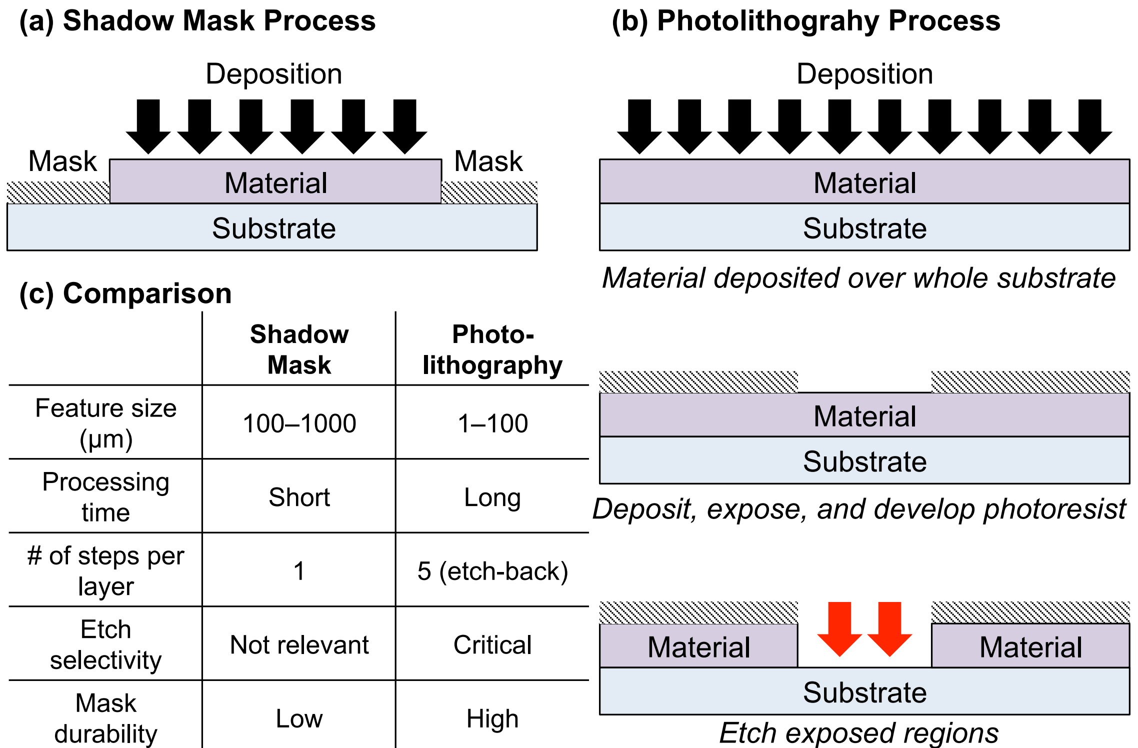
In this dissertation, our goal is to address the issues directly related to TFT electrical properties and stability under UHD dynamic operation, which include dynamic charging behavior, pixel ΔV_P, and ac BTS. A robust DOS model will also be developed to enable the development of a-IGZO TFTs suitable for dynamic operation in the active-matrix backplane of UHD AM-LCDs. Various experimental evidence will be used to support the DOS model.

1.2 Thesis Organization

This thesis begins with a detailed description in chapter 2 of a-IGZO TFT fabrication by shadow masking and by photolithography. Our proposed a-IGZO TFT DOS model is presented in chapter 3. The DOS model we have developed is derived from a combination of electrical and optical measurements and data from published literature. Oxygen-related states, such as oxygen vacancies or excess oxygen in the a-IGZO microstructure, are often discussed as the source of the subgap states in a-IGZO. Chapter 4 investigates the effect of oxygen incorporation into the a-IGZO thin film in terms of electrical properties and stability. In chapter 5, possible radiative transitions for photoluminescence (PL) in a-IGZO are proposed and discussed based on the spectra of a-IGZO thin films processed under different conditions. The PL is used as a nondestructive tool to probe the TFT channel region for changes to the subgap DOS. The PL spectra of a-IGZO TFTs before and after application of BTS are measured and discussed. Chapter 6 discusses the ac BTS of metal S/D recessed a-IGZO TFTs fabricated by photolithography on glass substrates. Both unipolar (positive or negative) and bipolar pulse waveforms with different pulse periods and duty cycles are investigated. In chapter 7, we fabricate one-transistor-one-capacitor test circuits with a-Si:H or a-IGZO TFTs and evaluate their dynamic characteristics side-by-side in the context of UHD display specifications. Lastly, chapter 8 summarizes the findings of this dissertation and future research directions are recommended.

CHAPTER 2

Fabrication of a-IGZO Thin-Film Transistors



	Shadow Mask	Photo-lithography
Feature size (μm)	100–1000	1–100
Processing time	Short	Long
# of steps per layer	1	5 (etch-back)
Etch selectivity	Not relevant	Critical
Mask durability	Low	High

Figure 2.1 A generic description of the (a) shadow mask and (b) photolithography fabrication process. A high-level comparison of the two processes are shown in (c).

2.1 Introduction

This dissertation utilizes a-IGZO TFTs fabricated by both shadow masking and photolithography at the Michigan Lurie Nanofabrication Facility and elsewhere. The main difference between shadow masking and photolithography can be seen in Figure 2.1. Fabrication by shadow masking is most suited for rapid prototyping of simple TFT

structures to investigate fundamental properties and optimize process parameters. In chapters 4 and 5, the common gate shadow mask a-IGZO TFT is used to reduce fabrication time and eliminate process variations unrelated to the a-IGZO layer. To investigate a-IGZO TFT dynamic response for real-world applications, TFTs of the back channel etch (BCE) inverted-staggered structure are fabricated by photolithography in chapter 7. For the ac bias-temperature stress studies, source/drain (S/D) recessed coplanar homojunction a-IGZO TFTs are fabricated elsewhere by our collaborators and will be discussed in chapter 6.

Within this chapter, the field-effect mobility (μ_{FE}) is extracted from a linear fit of the TFT transfer (I_D–V_{GS}) characteristics to the simplified ideal MOSFET equation

$$I_D = \frac{W}{L}\mu_{FE}C_{GI}(V_{GS} - V_{th})V_{DS} \quad (2\text{-}1)$$

in the linear region (small drain bias V_{DS}) and threshold voltage (V_{th}) from extrapolating the fitted line to the x-axis. In Equation (2-1), W and L are the TFT width and length, C_{GI} is the gate insulator capacitance per unit area, and V_{GS} is the gate bias. The subthreshold swing (SS) is derived from an average of three values around the maximum transconductance (dI_D/dV_{GS}) point of semi-log I_D–V_{GS} characteristics.

2.2 Common Gate a-IGZO TFTs by Shadow Masking

The common gate inverted-staggered a-IGZO TFT is a simple TFT structure consisting of S/D contacts and a-IGZO islands all defined by shadow masking on a SiO_2/Si substrate. A top-view image is shown in Figure 2.2. The Si substrate is heavily doped n^{++} silicon and serves as a single common gate for multiple TFTs. The individual devices can be physically separated by cleaving the substrate with a diamond cutter. The common gate a-IGZO TFT can be considered a “textbook” device in that the SiO_2 and Si

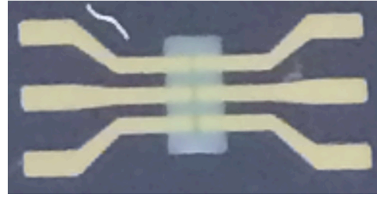


Figure 2.2 Top view photograph of the shadow mask a-IGZO TFT.

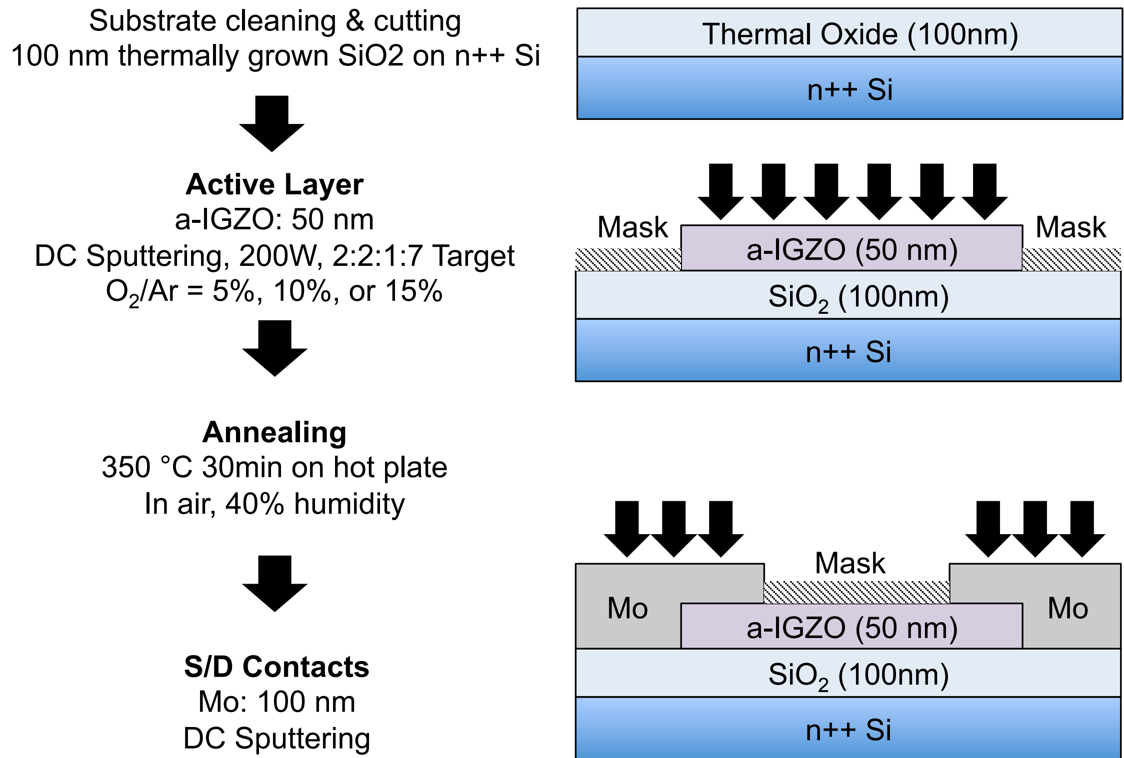


Figure 2.3 Fabrication process of the common gate inverted-staggered a-IGZO TFT by shadow mask process.

layers are very well understood and deviations are not expected. Therefore any changes to device properties and stability are directly representative of changes to the fabrication process in the channel and contact layers. It is very suitable for investigating the critical a-IGZO active layer process parameters. Its fabrication process is summarized in Figure 2.3. Depending on the thickness of the SiO_2 used (generally 100 or 200 nm), there is possibility that the gate and S/D contacts may be shorted due to physical damage to the gate oxide during the fabrication process. In the device transfer characteristics (I_D–V_{GS}), this may appear as the S/D currents tracking the gate current.

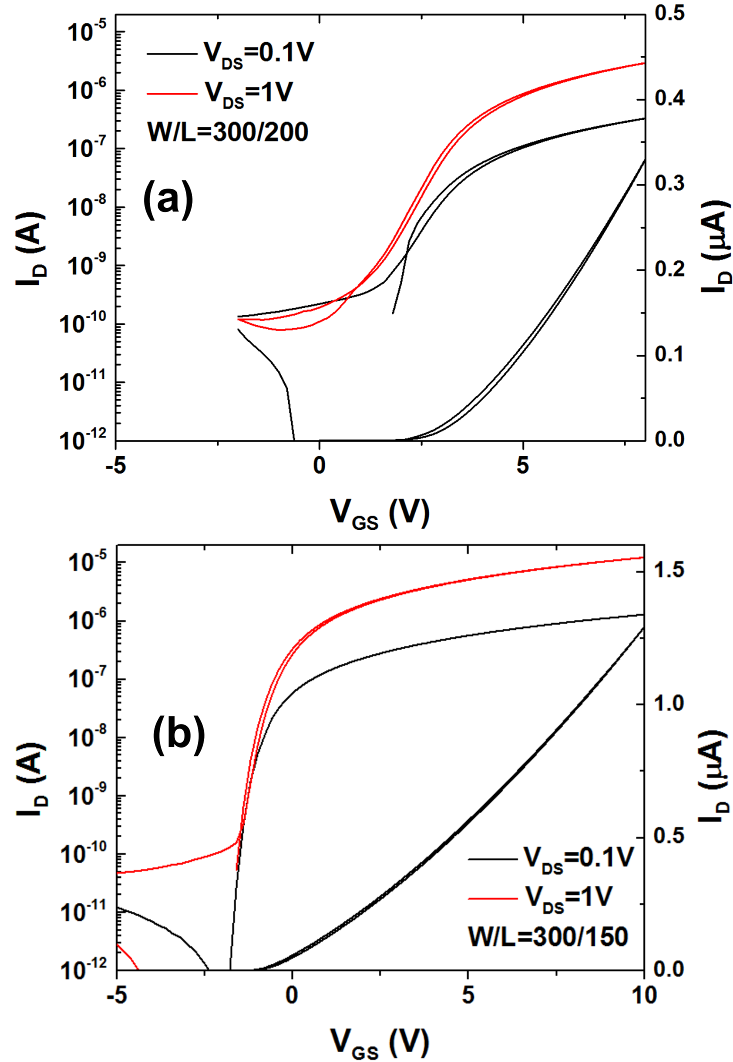


Figure 2.4 Common gate a-IGZO TFTs with (a) one post-S/D deposition annealing and (b) one pre-S/D deposition annealing.

2.2.1 Impact of Thermal Annealing

Annealing is essential for the fabrication of a-IGZO TFTs with good electrical properties [28], [65]. Without annealing, as-fabricated a-IGZO TFTs have very negative V_{th} and very high SS. We observed no significant differences between 30 and 60 minutes of annealing. We have also studied the impact of the order of annealing on a-IGZO TFT electrical properties. Within the literature, some reported annealing before S/D deposition [27], [66] while some are done after [67], [68]. In our investigations, we fabricated two

common gate a-IGZO TFTs, one annealed before S/D deposition ("pre-annealed") and the other annealed after ("post-annealed"). Their I_D–V_{GS} curves are shown in Figure 2.4. The (a) post-annealed TFT is very degraded in comparison to the (b) pre-annealed TFT. The extracted TFT electrical parameters are as follows for the pre-annealed configuration: μ_{FE} = 18.1 cm^2/V·s, V_{th} = 0.3 V, and SS = 222 mV/dec. For the post-annealed configuration, they are: μ_{FE} = 12.5 cm^2/V·s, V_{th} = 3.23 V, and SS = 410 mV/dec. In the case of the post-annealed TFT, upon visual inspection by the naked eye, the molybdenum (Mo) S/D contacts are severely oxidized, which may have greatly increased the S/D series resistance and reduced μ_{FE}. Material and chemical analysis should be conducted in the TFT channel to precisely determine the cause of the degradation. Based on these results, we have adopted pre-S/D deposition/definition thermal annealing for all our shadow mask a-IGZO TFTs throughout this dissertation.

2.2.2 Impact of Oxygen Partial Pressure

During deposition of the a-IGZO thin film by sputtering, oxygen is usually injected into the sputtering chamber with argon. The typical percentage of O_2/Ar partial pressure (p_{O_2}) ranges from 2% to 20%. Throughout this dissertation, p_{O_2} = 5% is mostly used in the fabrication of a-IGZO TFTs unless where stated. We have also fabricated a-IGZO TFTs with p_{O_2} = 10% and 15%. The I_D–V_{GS} electrical properties are shown in Figure 2.5. From the figure, we observe that V_{th} becomes more positive and field-effect mobility (μ_{FE}) is slightly reduced with higher p_{O_2}. More discussion and analysis on the impact of p_{O_2} during a-IGZO deposition on TFT electrical properties and stability will be presented in chapter 4.

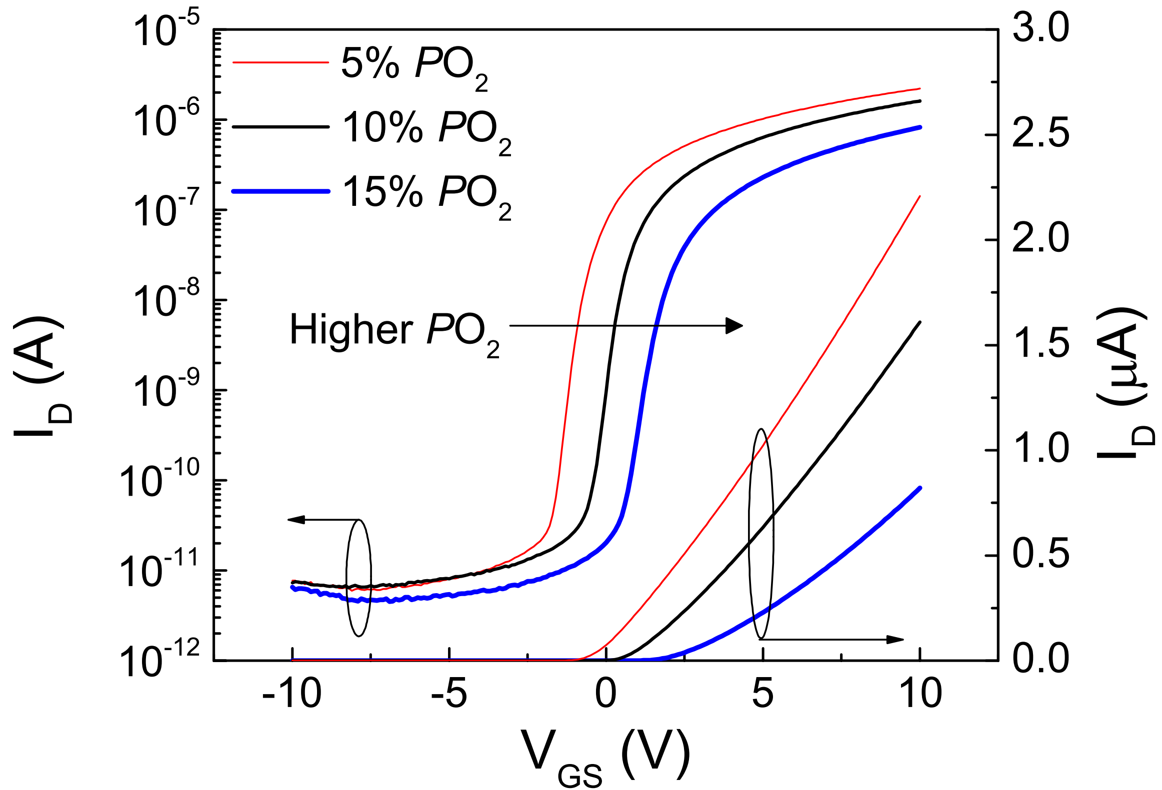


Figure 2.5 Impact of p_{O_2} during a-IGZO sputtering on the electrical properties of common gate a-IGZO TFTs fabricated by shadow mask.

2.2.3 Impact of Active-Wide vs. Contact-Wide TFT Configurations

As shown in Figure 2.2, the device configuration in which the a-IGZO island is wider than the S/D contacts is generally referred to as the "active-wide" configuration. When the gate bias is applied, the entire a-IGZO island accumulates charge carriers, and fringe field effect causes current to also flow through the vicinity of the channel region. Field-effect mobility is commonly extracted from TFT I_D–V_{GS} using Equation (2-1) while assuming that current is confined within the W/L as defined by the S/D contacts. In the case of the active-wide configuration, this will cause the μ_{FE} to appear higher than it actually is. In the "contact-wide" configuration, S/D contacts are wider than the a-IGZO island and current is confined entirely within the channel region as defined by the active

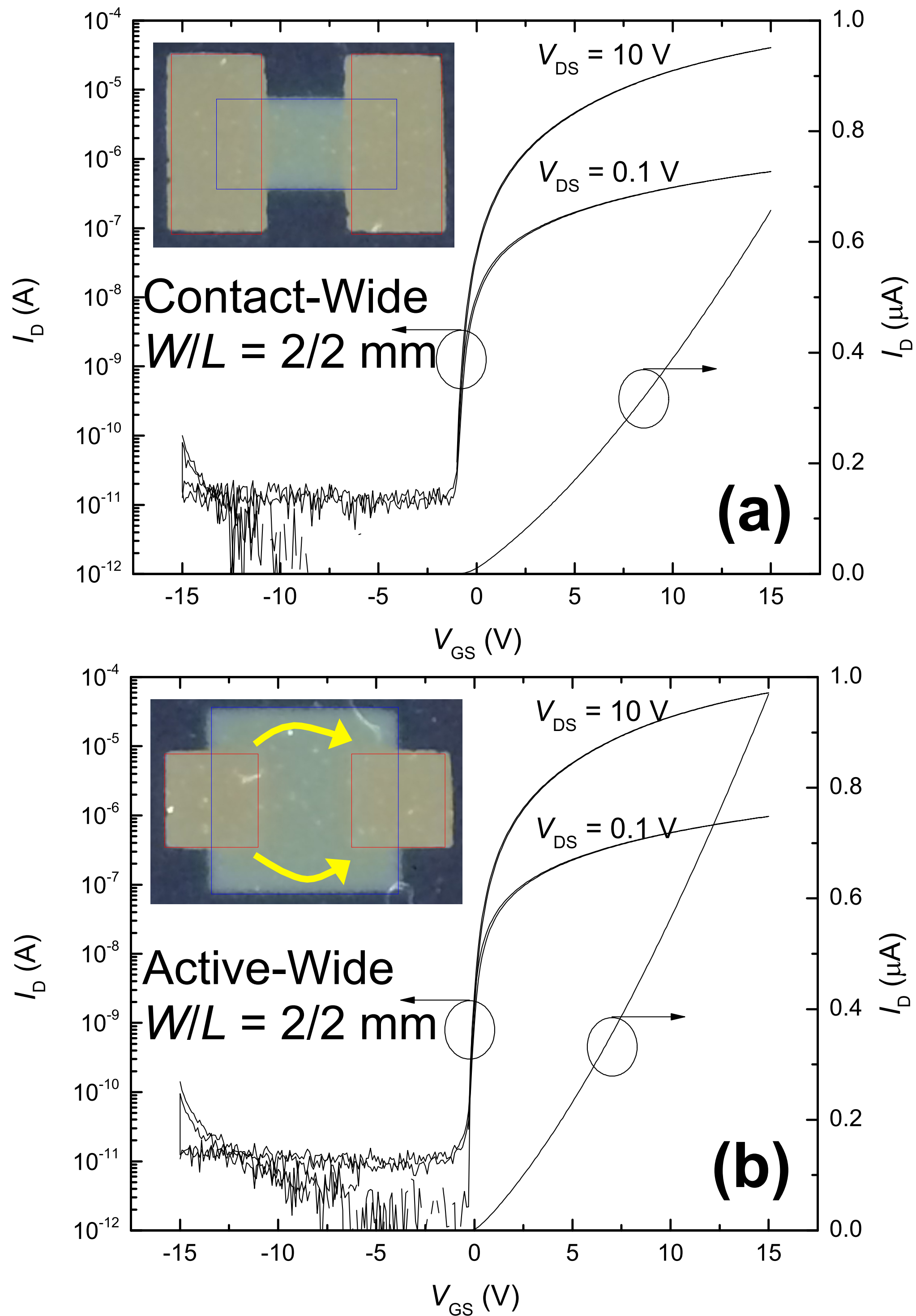


Figure 2.6 The I_D–V_{GS} at V_{DS} = 0.1 and 10 V for the common gate a-IGZO TFTs fabricated by shadow mask process with W/L = 2/2 mm in the (a) contact-wide and (b) active-wide configurations. The arrows in (b) indicate the path of the fringe field effect.

island width and the S/D contact separation. We have fabricated two TFTs of identical W/L (2/2 mm) in both the active-wide and the contact-wide configurations. The I_D–V_{GS} of (a) contact-wide and (b) active-wide a-IGZO TFTs are shown in Figure 2.6, and top-view photograph and mask design of the TFTs are shown as figure insets. It is clear to see that for devices of the same dimensions, the active-wide configuration has much higher I_D at the same bias point in the on state. Based on W/L = 2000/2000 μm, we extract the apparent μ_{FE} = 16.1 cm^2/V·s and V_{th} = 1.6 V for active-wide and μ_{FE} = 10.5 cm^2/V·s and V_{th} = 1.1 V for contact-wide configuration. The apparent μ_{FE} of the active-wide configuration is much higher, even though the two TFTs were fabricated in the same processing run on the same substrate. This indicates that using the active-wide configuration will make extraction of TFT electrical parameters difficult. Unless extra steps are taken to take into consideration of the fringe field effects, the contact-wide configuration is recommended for most cases if possible.

2.3 Defined Gate a-IGZO TFTs by Shadow Masking

In our a-IGZO TFT shadow mask set, we have also prepared masks for gate electrode and gate insulator layers. Defined gate a-IGZO TFTs may be fabricated on glass or SiO_2/Si substrates. The gate electrode material can be the same as that of the S/D electrodes, which is Mo throughout the entire dissertation. The defined gate may be used in conjunction with the metal-insulator-semiconductor (MIS) structure to explore the impact of gate insulators on a-IGZO TFT electrical properties. For the gate insulator, we have used plasma-enhanced chemical vapor deposition (PECVD) silicon oxide (a-SiO_X). It is also possible to use a PECVD silicon nitride (a-SiN_X)/a-SiO_X bilayer as gate

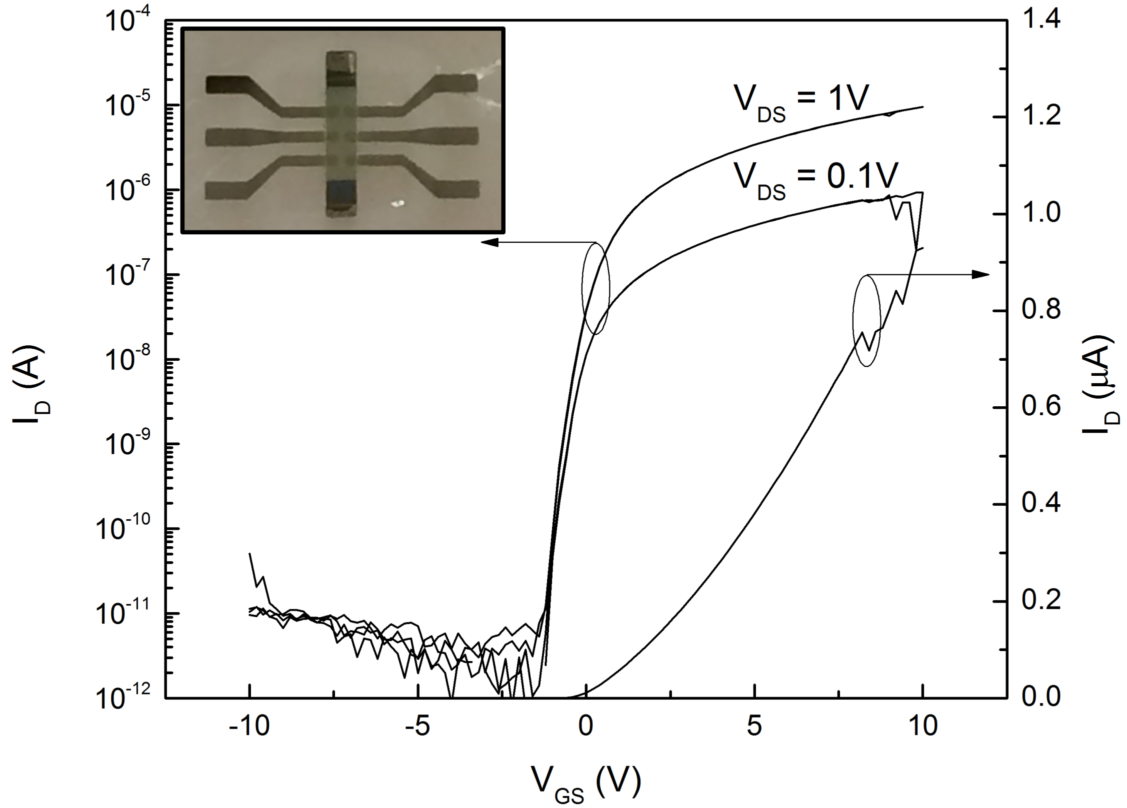


Figure 2.7 The I_D–V_{GS} at V_{DS} = 0.1 and 1 V of defined gate a-IGZO TFTs fabricated by shadow masking. The top-view photograph of the fabricated device is shown in the figure inset.

insulator, provided that the a-SiO_X layer always interfaces with a-IGZO because a-IGZO may be doped by the high hydrogen content in PECVD a-SiN_X [31], [67]–[69]. The I_D–V_{GS} and top-view photograph of the defined gate a-IGZO TFT we have fabricated are shown in Figure 2.7. The extracted electrical parameters are as follows: μ_{FE} = 13.2 $cm^2/V \cdot s$, V_{th} = 1.5 V, and SS = 261 mV/dec.

2.4 Back Channel Etch a-IGZO TFTs by Photolithography

In the active-matrix liquid crystal display (AM-LCD) industry, the TFT backplane is fabricated by photolithography. The required small feature sizes are only possible through photolithography because it is only limited by diffraction of the exposure light

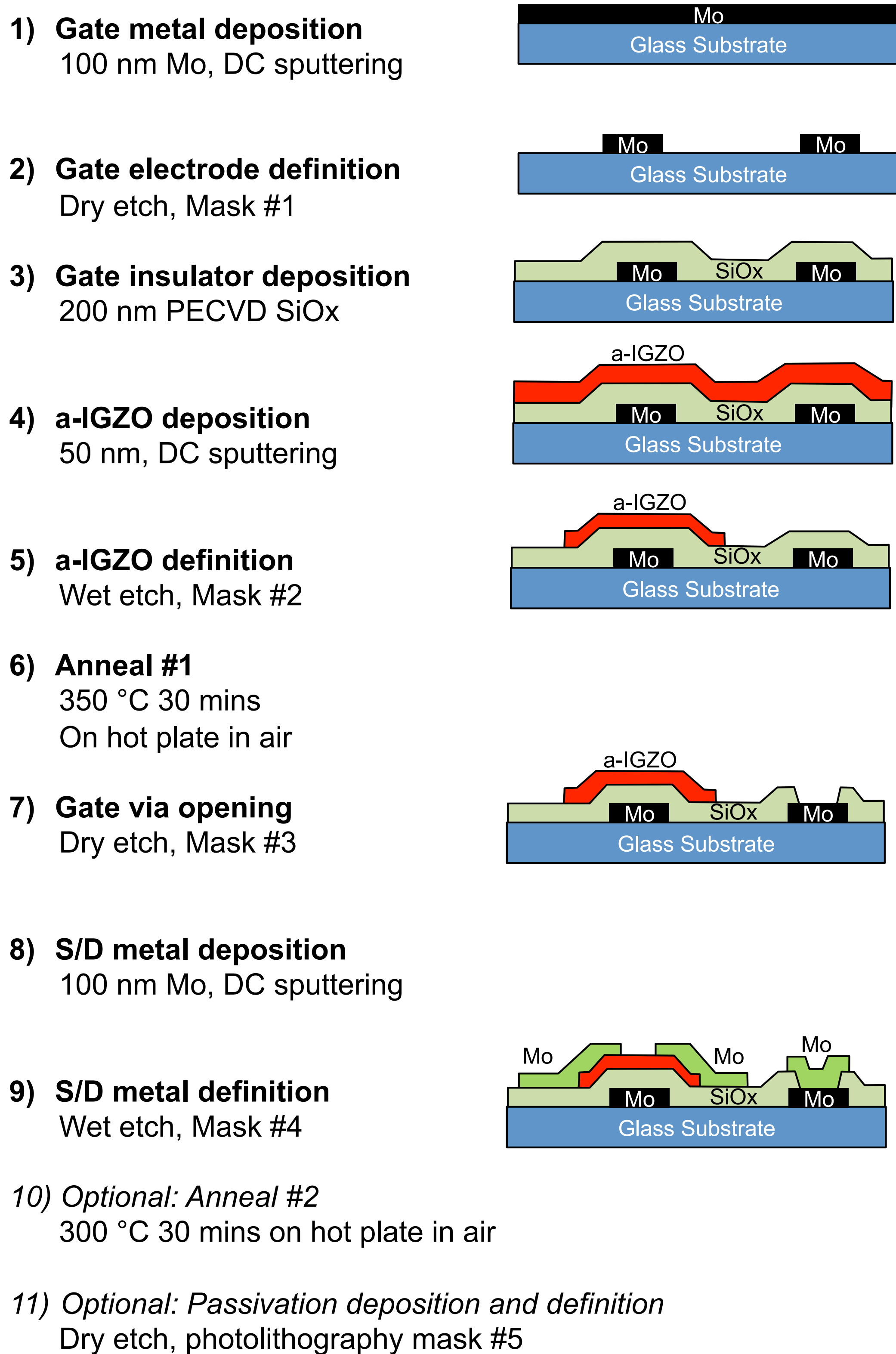


Figure 2.8 Process flow of the back channel etch a-IGZO TFTs fabricated by photolithography at the University of Michigan Lurie Nanofabrication Facility.

source. For fabricating the a-IGZO TFTs by photolithography in this study, we have adopted the BCE inverted-staggered TFT structure for its simplicity and its applicability to most existing AM-LCD production lines. The BCE structure is notable for its exposed active layer back channel during the S/D deposition and definition process. This enables reduced mask count for lower costs, higher throughput, and has been widely adopted for a-Si:H TFTs. For direct comparison of the TFT dynamic response, BCE a-Si:H and a-IGZO TFTs are fabricated and will be discussed in chapter 7. The process flow of the BCE a-IGZO TFT is shown in Figure 2.8.

2.4.1 Gate Electrode Deposition and Definition

Molybdenum was selected as the gate metal. As a refractory transition metal, it is easily processed, is stable under most processing conditions, and has decent conductivity for most applications [8]. A 100-nm-thick film of Mo is deposited as gate metal on cleaned 4" glass substrates by dc sputtering at 600 W without any RF bias on the substrate holder. The flow rate of Ar is 40 sccm in 3.78 mTorr chamber pressure. The process conditions may vary, but at time of writing it deposits Mo at 3.5 Å/s.

For patterning of each layer, photoresist (PR) is first applied by the ACS 200 automated cluster tool in the Michigan Lurie Nanofabrication Facility (LNF). It spin-coats 1.5 μm of Dow Chemical Megaposit SPR 200 positive resist and then bakes it for 90 s at 115 °C. Alignment and exposure of the first mask pattern (Mask #1: Gate) are done by the Karl Suss MA-6 alignment tool. The 405 nm UV lamp at 20 mW/cm^2 power exposes the PR for 5.5 s, which is then developed in the ACS 200 with Clariant AZ 300 metal-ion-free developer by spraying for 30 s. Finally a hard bake is applied by the ACS 200. After hard bake, the patterned PR is lightly descumed in the YES Plasma Stripper

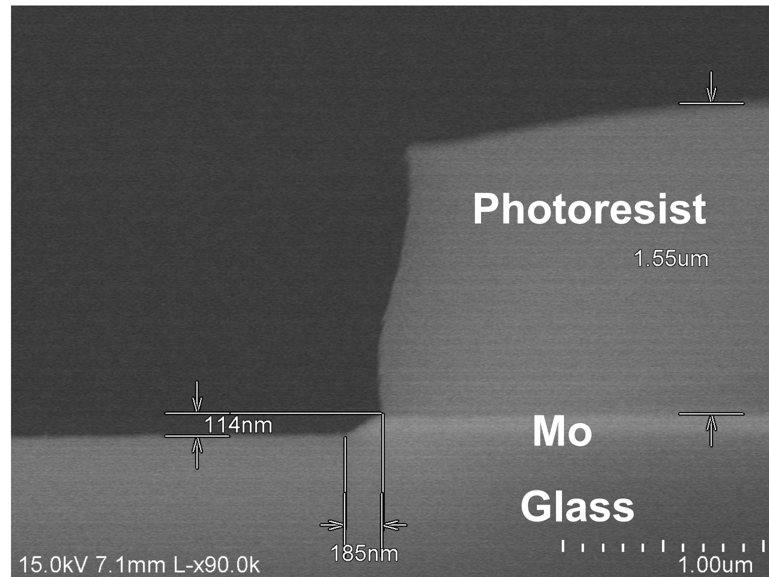


Figure 2.9 Side-view SEM image of Mo gate electrode on glass after dry etching.

with O_2 plasma for 30 s. The same photolithography procedure is used for all subsequent photolithography steps.

For gate electrode definition, dry etching in the LAM 9400 reactive ion etcher (RIE) is used with a 4”-to-6” carrier wafer. Pressure in the process chamber is 20 mTorr to prevent loss of plasma energy due to particle collision outside of deeper features. Gas chemistry used for the plasma is 30 sccm SF_6, 20 sccm O_2, and 50 sccm of He dilution. The SF_6 provides the reactive chemistry to etch Mo, while O_2 erodes the PR to encourage the formation of a tapered edge on the gate electrodes. Tapered edge is necessary for good step coverage of subsequent layers [8]. At power of 200 W + 25 W of RF power, the etch rate is 48.6 Å/s at the center of the substrate and 44.1 Å/s on the outer edge. To investigate the etch quality, Figure 2.9 shows the cross-section scanning-electron microscope (SEM) image of the etched gate electrode, and we see that a very desirable 30° tapered edge has been formed as a result of the PR erosion. After brief ashing in the YES Plasma Etcher to remove the hardened fluorocarbons generated in the dry etch process, the PR is stripped in acetone and isopropyl alcohol with ultrasonic agitation.

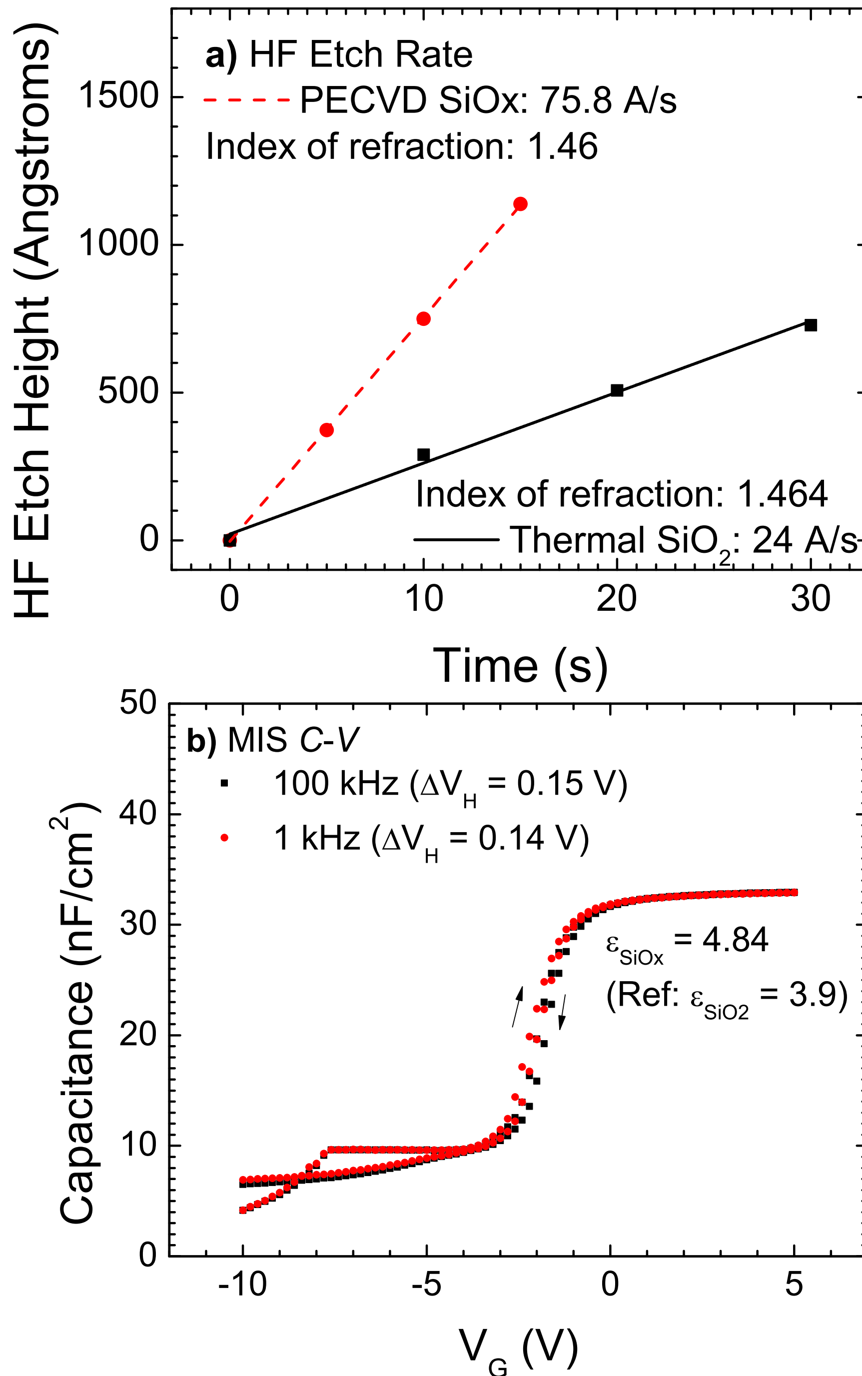


Figure 2.10 (a) The HF etch rate and refractive index of PECVD a-SiO_X used throughout this study for gate insulator purposes, compared with those of thermally grown SiO_2 on a Si substrate. (b) The *C*–*V* characteristics of the PECVD a-SiO_X MOS structure.

2.4.2 Gate Insulators and Active Layer Deposition and Definition

Gate insulator is 200 nm of a-SiO_X deposited by PECVD. In the LNF cleanroom, a high-density low-hydrogen custom recipe on the GSI PECVD tool was developed specifically for electronic applications. The gas chemistry is 5 sccm of SiH_4 (100%), 2000 sccm of N_2O, and 500 sccm of He dilution at 3 Torr chamber pressure. Power is 200W at 13.56 MHz and 20W at 400 KHz. Deposition temperature is 300 °C. The optical refractive index and HF etch rate can provide clues on the quality of the a-SiO_X in comparison to a reference thermally grown SiO_2 sample, as shown in Figure 2.10(a). The refractive index is representative of the film stoichiometry, while the HF etch rate is related to the film density. In Figure 2.10(b) the PECVD a-SiO_X MOS structure capacitance–voltage (*C*–*V*) characteristics is evaluated using a HP 4284A *LCR* meter. Although the quality of the PECVD a-SiO_X is inferior to thermally grown SiO_2, it is sufficiently robust for our purposes in photolithography a-IGZO TFTs.

After deposition of a-SiO_X gate insulator, 50 nm of a-IGZO is dc sputtered as the channel layer. The sputtering is done in a Kurt J. Lesker Lab18 sputterer with a In:Ga:Zn:O = 2:2:1:7 target purchased from Toshima Manufacturing Company. Sputtering power is 200 W, and during deposition gas mixture of O_2/Ar = 1.5/30 sccm is injected into the sputtering chamber while a turbopump maintains chamber pressure at 4 mTorr. Detailed description of the deposition conditions of the a-IGZO active layer and their impact on TFT electrical properties have been discussed in previous sections and will be continued in chapter 4. After a-IGZO sputtering, the substrate is annealed in room atmosphere (40% humidity) on a contact hot plate at 350 °C for 30 mins. The a-IGZO is then defined after PR has been deposited and patterned (Mask #2: Active) using wet

etching. The wet etchant is either 0.05 M of oxalic acid ($H_2C_2O_4$) or 0.1 M of HCl, both of which will etch a-IGZO at a reasonably low rate of ~10 Å/s for good control during the etching. No agitation is applied while the etching takes place for consistency between runs.

Photoresist is then deposited and patterned (Mask #3: Contact) for gate contact vias. The contact vias in the gate insulator are then opened using dry etching in the LAM 9400 tool. The gas chemistry is 8 sccm of SF_6, 50 sccm of C_4F_8, 50 sccm or Ar, and 50 sccm of He dilution at a pressure of 10 mTorr. After dry etching, the entire substrate should be ashed in O_2 plasma to remove hardened fluorocarbons and inhibitants resulting from the RIE etching process (primarily C_4F_8). Failure to do so will cause the metal gate pad to adhere poorly in later fabrication steps.

2.4.3 Source/Drain Electrode Definition

The S/D metal is 100 nm of Mo deposited using the identical dc sputtering recipe as the gate electrodes. After PR deposition and patterning (Mask #4: Metal), the S/D electrodes are defined. In the fabrication of hydrogenated amorphous silicon (a-Si:H) TFTs, dry etching has generally been used for the definition of S/D electrodes. However, literature has shown that a-IGZO exposed to high-energy plasma becomes very conductive [70]. To determine the impact of S/D definition processes, we fabricated one set of a-IGZO TFTs where the S/D contact electrodes are defined by dry etching and the other by wet etching.

The S/D dry etch recipe is again performed in LAM 9400 using the same SF_6 + O_2 + He recipe as the gate electrode definition described in section 2.4.1. For wet etching, 30% CMOS grade H_2O_2 (J. T. Baker) is used. Formation of a black MoO_X complex during wet

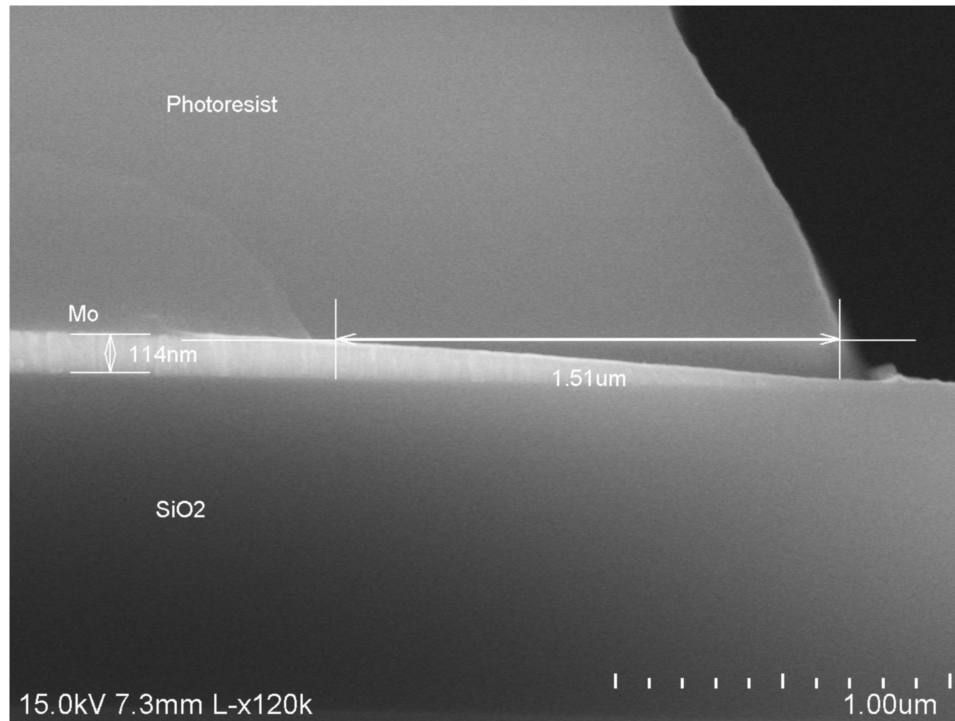


Figure 2.11 SEM cross-section of a Mo thin film on a SiO_2 dummy wafer etched by H_2O_2 + NH_4OH.

etching prompted the addition of NH_4OH to H_2O_2 (in 1:40 ratio) [71] and the use of a magnetic stirrer to promote etch uniformity. Dummy wafers are first etched in either processes to evaluate the etch selectivity against a-IGZO. By visual inspection, we have found no signs of erosion on the a-IGZO layer by wet etching or dry etching. However, a four-point probe measurement on the film surface revealed that while the as-deposited a-IGZO thin film has very high sheet resistivity outside the measurable range of the probe, dry-etched a-IGZO has low sheet resistivity of 6140 Ω/sq. The wet-etched sample remains very resistive and is also out of the range of the four-point probe. The SEM cross-section image of a wet-etched Mo film on a dummy test wafer is shown in Figure 2.11. After the S/D electrodes have been defined, the PR is then stripped and the substrate cleaned. The I_D–V_{GS} of the BCE a-IGZO TFTs we fabricated with the S/D electrodes dry-etched using the conditions mentioned above is shown in Figure 2.12. We observe that at

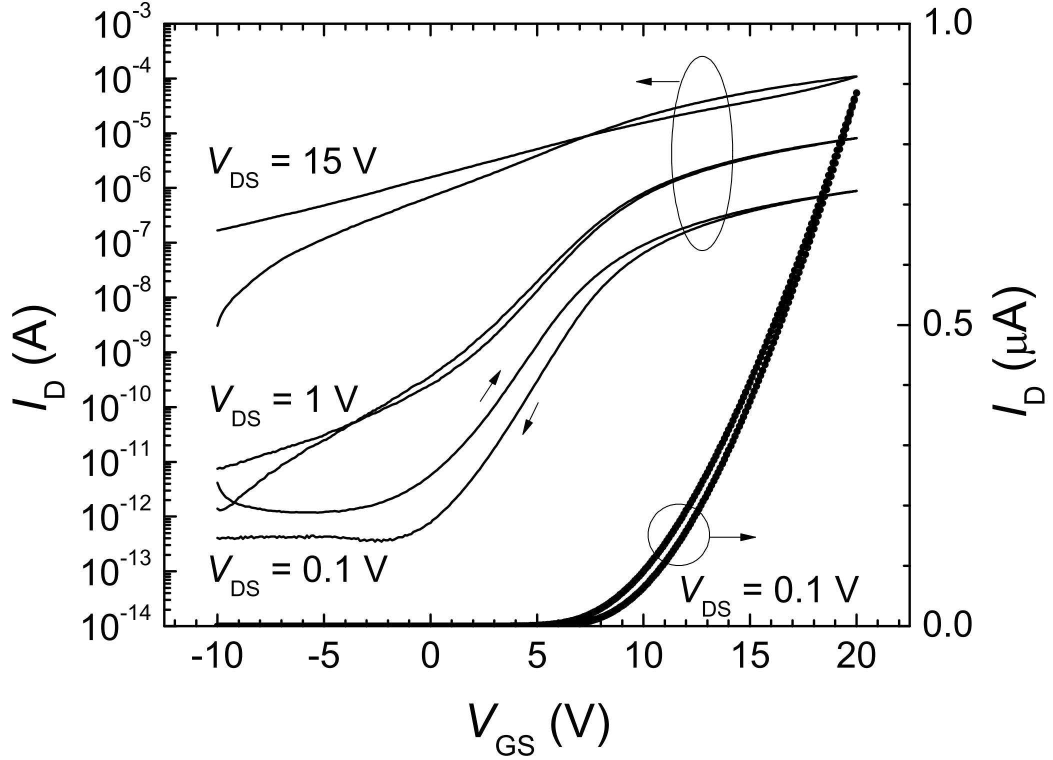


Figure 2.12 The I_D–V_{GS} of the BCE a-IGZO TFT with S/D defined by dry etching.

higher V_{DS}, because the a-IGZO TFT back channel has become very conductive during plasma exposure, the impact of a parasitic transistor is evident. Therefore, we have adopted wet etching with H_2O_2 + NH_4OH at room temperature for all S/D definition in our BCE a-IGZO TFTs.

Due to process condition variations, some samples fabricated showed very conductive behavior with only one annealing step. If deemed necessary, a second anneal of 300 °C in room atmosphere may be applied after the PR has been stripped. Figure 2.13 shows the (a) I_D–V_{GS} and (b) I_D–V_{DS} of a representative BCE a-IGZO TFT fabricated for various studies throughout this dissertation. The extracted electrical parameters are as follows: μ_{FE} = 9.8 cm^2/V·s, V_{th} = −2.0 V, SS = 700 mV/dec, and the off current is below 10^{-13} A. The output (I_D–V_{DS}) characteristics of the TFT are very good and show no sign of current crowding upon inspection in the low-V_{DS} region.

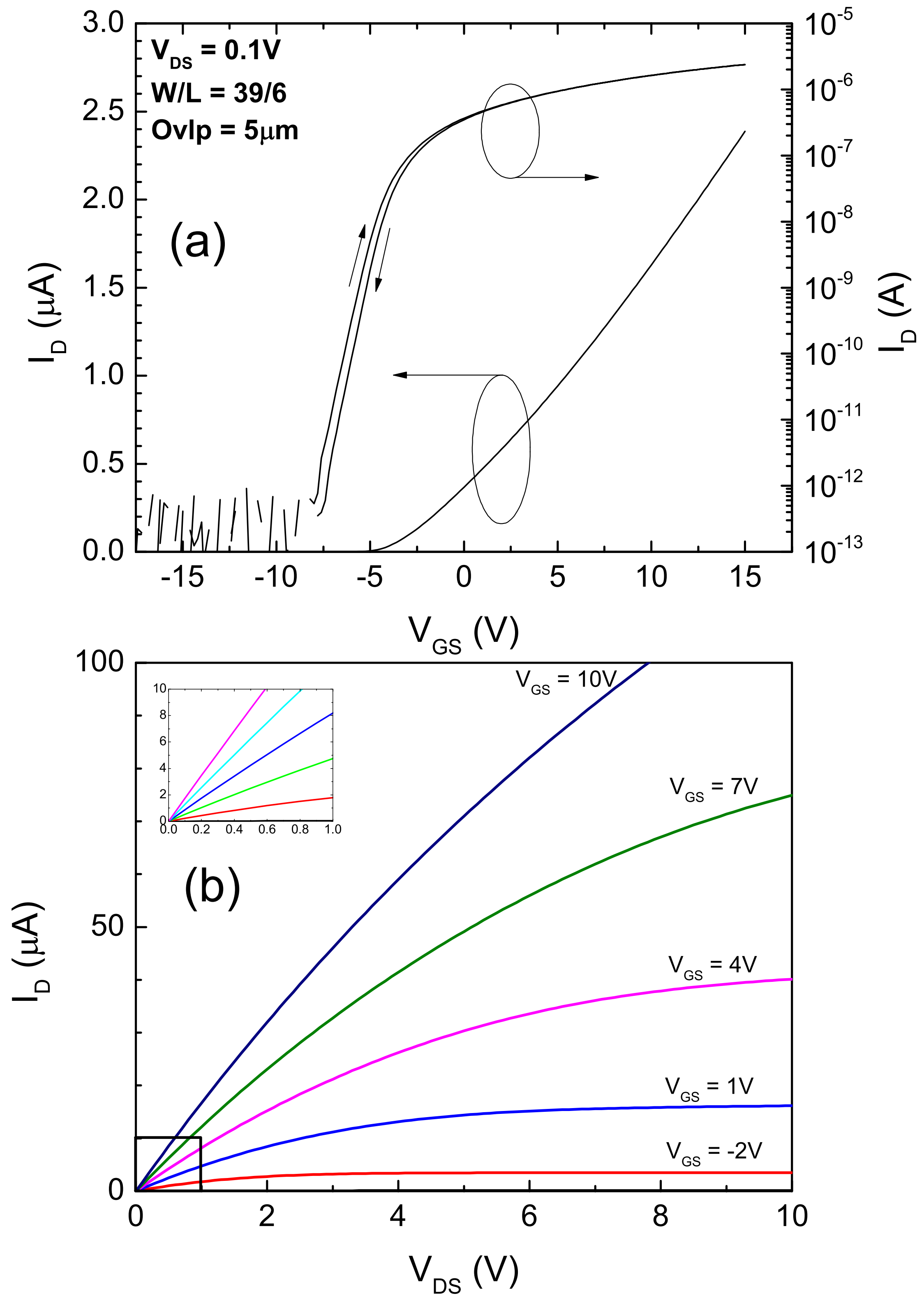


Figure 2.13 The (a) I_D–V_{GS} characteristics and (b) I_D–V_{DS} characteristics of the BCE a-IGZO TFT fabricated by photolithography for this dissertation.

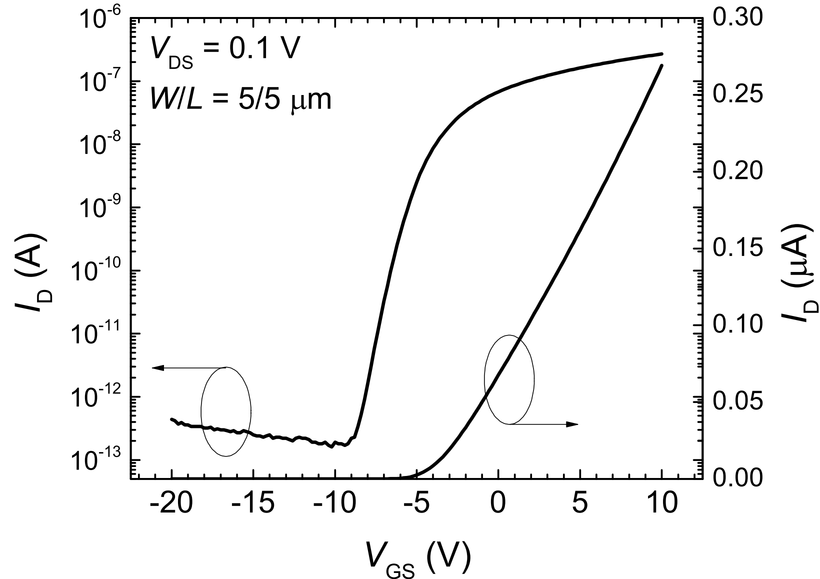


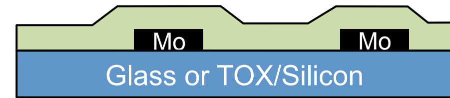
Figure 2.14 The TFT I_D–V_{GS} characteristics of the CPL a-IGZO TFT fabricated by photolithography with PECVD a-SiO_X passivation layer (300 nm).

2.5 Channel Protection Layer a-IGZO TFTs by Photolithography

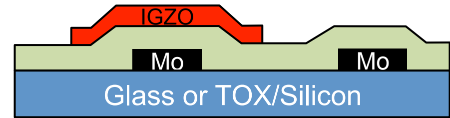
As seen in section 2.4.3, the back channel of the a-IGZO TFT heavily influences the TFT electrical properties. Damage or doping during the S/D metal deposition and/or definition may severely impact TFT operation. In order to fabricate high performance a-IGZO TFTs with photolithography, it may be desirable to add a PECVD a-SiO_X Channel Protection Layer (CPL) onto the a-IGZO active layer in the fabrication process. Dry etching is used for CPL definition, and exposure of the unprotected a-IGZO regions to high-energy plasma may facilitate the formation of highly conductive S/D contact regions. The PECVD a-SiO_X CPL should be deposited at a lower temperature than the gate insulator so as to not degrade its electrical integrity or modify the a-IGZO layer too much. The CPL a-IGZO TFT I_D–V_{GS} are shown in Figure 2.14 and the extracted parameters are μ_{FE} = 10.4 $cm^2/V{\cdot}s$, V_{th} = −3.5 V, and SS = 770 mV/dec. The a-IGZO TFTs with CPL are fabricated off-site at our collaborators' lab, and the process flow is shown in Figure 2.15.

1) Gate metal deposition/definition
Mo, 200 nm, dc sputtering
Dry etch, Mask #1

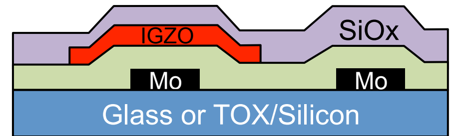
2) Gate insulator deposition
PECVD SiOx, 200 nm



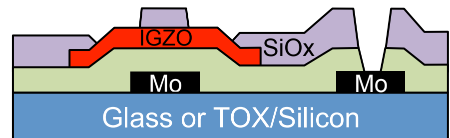
3) a-IGZO deposition/definition
50 nm, dc sputtering
Wet etch, Mask #2



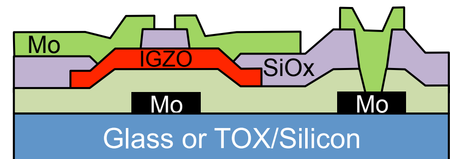
4) Channel Protection Layer (CPL) deposition
PECVD SiOx, 100 nm



5) CPL & Gate via opening
Dry etch, Mask #3 and #4

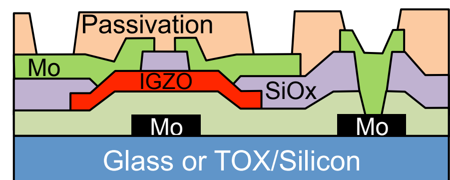


6) S/D metal deposition/definition
Mo, 200 nm, dc sputtering
Dry etch, Mask #5



7) Anneal #1

8) Passivation deposition/definition
PECVD SiOx or SiOx/SiNx bilayer
Dry etch, Mask #6



9) Anneal #2

Figure 2.15 Process flow of the Channel Protection Layer (CPL) a-IGZO TFT fabricated by photolithography.

	PECVD a-SiO_X			PECVD a-SiO_X/a-SiN_X Bilayer		
	Initial Room Air	Nitrogen Flow	Room Air (2)	Initial Room Air	Nitrogen Flow	Room Air (2)
μ_{FE} (cm^2/V·s)	10.4	10.9	10.4	9.6	9.5	9.6
V_{th} (V)	−3.5	−2.9	−3.5	3.5	3.5	3.5
SS (mV/dec)	770	309	720	285	246	275

Table 2.1 Extracted device parameters in the linear region (V_{DS} = 0.1 V) for the a-IGZO TFT with PECVD a-SiO_X or a-SiO_X/a-SiN_X bilayer as passivation.

2.5.1 Impact of Passivation Layer on a-IGZO TFTs by Photolithography

Two different types of TFT passivation are investigated: PECVD a-SiO_X (300 nm), and PECVD a-SiO_X/a-SiN_X bilayer (150 nm each). For each substrate, the TFT I_D–V_{GS} is initially measured in room air. It is then measured again after purging with N_2. In Figure 2.16(a), we observe that the TFT electrical properties significantly improved after the device has been subject to N_2 purging for 30 minutes. Once the N_2 flow has been removed for another 30 minutes, the TFT electrical properties returned to their initial states. The TFT I_D–V_{GS} curve measured in a vacuum probe (not shown) is almost identical to the curve measured in N_2. However, as shown in Figure 2.16(b), no differences are observed for the I_D–V_{GS} of the a-SiO_X/a-SiN_X bilayer-passivated device when measured in different ambient atmospheres. For both substrates, the extracted device parameters before, during, and after N_2 purging are summarized in Table 2.1. Room air is a mixture of O_2, N_2, humidity, and other negligible gaseous species. The degradation of TFT electrical properties upon air exposure suggests that the passivation is not sufficiently robust to shield the TFT back channel from O_2 and/or humidity. In terms of a-IGZO TFT with the a-SiO_X/a-SiN_X bilayer passivation, there are no sign that

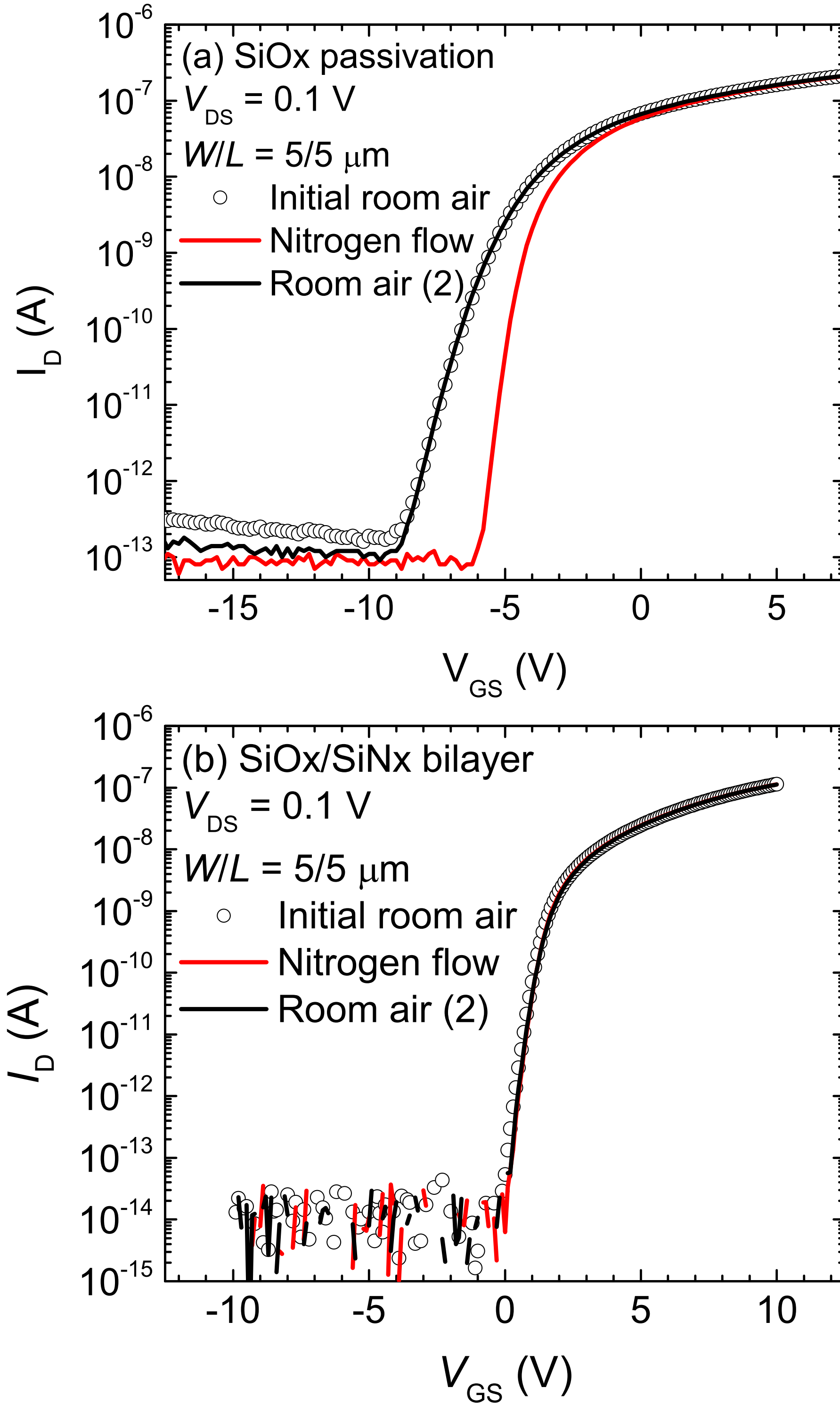


Figure 2.16 Comparison of the a-IGZO TFT I_D–V_{GS} characteristics before (open circles), during (solid red line), and after (solid black line) nitrogen purging for TFTs with (a) only PECVD a-SiO_X passivation and (b) PECVD a-SiO_X/a-SiN_X bilayer passivation.

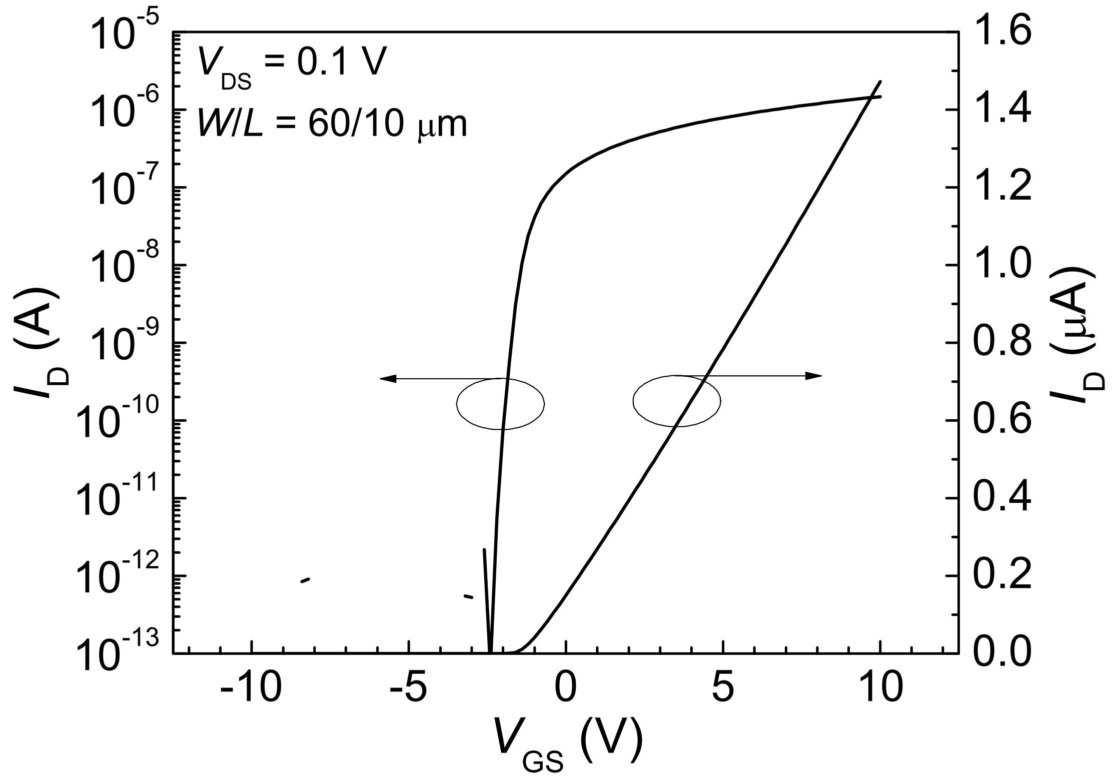


Figure 2.17 The I_D–V_{GS} at V_{DS} = 0.1 V of the S/D-recessed coplanar homojunction a-IGZO TFT fabricated by photolithography.

ambient gases affect the TFT electrical properties.

2.6 S/D-Recessed a-IGZO TFTs by Photolithography

In the dynamic operation of the TFT active-matrix backplane, the gate-source/drain overlap capacitance (C_{GS}) contributes significantly to the feedthrough voltage [61], [62], which is responsible for display flicker in AM-LCDs. A coplanar self-aligned structure, in which there is no overlap between the gate and S/D electrodes, should effectively eliminate or greatly reduce C_{GS} [67], [68]. In such a configuration, highly conductive a-IGZO homojunction regions are used as S/D contact regions and the Mo metal electrodes do not overlap at all within the TFT structure. In this configuration, the TFT is self-aligned because channel region is formed from the a-IGZO area capped by the CPL.

Regions outside CPL are converted to ohmic a-IGZO contact regions by hydrogen doping from the hydrogen-containing PECVD a-SiN_X passivation layer. It has been shown in the literature that hydrogen acts as a shallow donor level in a-IGZO [31], [69], [72], thus hydrogen doping is effective in creating S/D contact regions for the a-IGZO TFT. The typical TFT I_D–V_{GS} characteristics for this device configuration is shown in Figure 2.17 and the extracted device parameters are as follows: μ_{FE} = 10.9 cm^2/V·s, V_{th} = −1.02 V, and SS = 220 mV/dec. The process flow for the S/D-recessed coplanar homojunction a-IGZO TFT is described in Figure. 2.18. The S/D-recessed a-IGZO TFTs are fabricated off-site at our collaborators' location. These devices will be discussed and evaluated in greater detail in chapter 6.

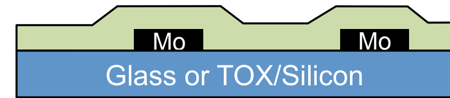
2.7 Summary of TFT Structures Fabricated

Throughout this dissertation, several different configurations of a-IGZO TFTs have been fabricated for different purposes and studies:

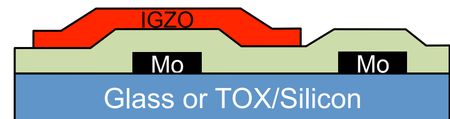
- Shadow mask a-IGZO TFTs with common gate (n^{++} Si). Used to rapidly investigate impact of processing conditions (chapter 4 and 5).
- Shadow mask a-IGZO TFTs with defined gate.
- Channel protection layer a-IGZO TFTs by photolithography.
- High-performance S/D-recessed coplanar homojunction a-IGZO TFTs by photolithography. A strong candidate for UHD AM-LCD backplane and used to investigate the dynamic operation electrical instability (chapter 6).
- Back channel etch a-IGZO TFTs by photolithography. Used to compare the dynamic response with BCE a-Si:H TFTs (chapter 7).

1) Gate metal deposition/definition
Mo, 100 nm, dc sputtering
Dry etch, Mask #1

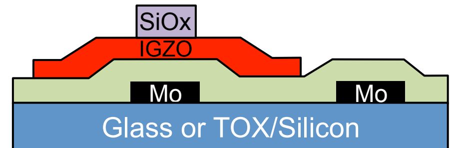
2) Gate insulator deposition
PECVD SiOx, 200 nm



3) a-IGZO deposition/definition
40 nm, dc sputtering
Wet etch, Mask #2

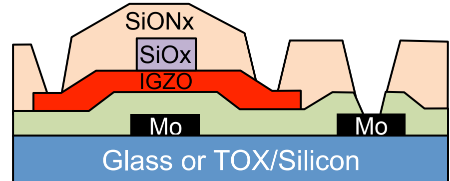


4) Channel Protection Layer (CPL) deposition/definition
PECVD SiOx, 300 nm
Dry etch, Mask #3

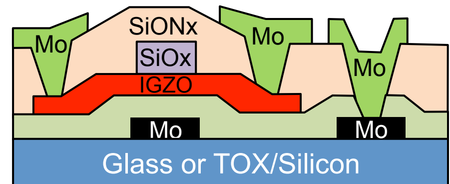


5) Rapid thermal anneal #1
290 °C, 1 hour

6) Passivation and gate via deposition/definition
PECVD SiONx, 300 nm
Dry etch, Mask #4 and #5



7) S/D metal deposition/definition
Mo, 100 nm, dc sputtering
Wet etch, Mask #6



8) Rapid thermal anneal #2
270 °C, 1 hour

Figure 2.18 Process flow of the S/D-recessed coplanar homojunction a-IGZO TFT fabricated by photolithography

CHAPTER 3

Density of States of Amorphous In-Ga-Zn-O from Electrical and Optical Characterization

3.1 Introduction

Capacitance–voltage (*C–V*) measurement can reliably probe the density of defect states in a semiconductor device and is commonly used in silicon CMOS technology. From the *C–V* measurements of an a-IGZO TFT structure, Kimura *et al*. extracted the density of states (DOS) near the conduction band minimum (E_C) [73]. In the case of TFTs with non-negligible bulk resistivity, the frequency of the ac small-signal needs to be very low (<1 Hz) so the electrons supplied from the source/drain (S/D) regions can have sufficient time to respond. Extraction of the DOS from high-frequency *C–V* measurements is demonstrated by Jeon *et al.*, who exposed a-IGZO TFTs to monochromatic sub-band gap light acting as a source of photo-excitation [74]. Considering that a-IGZO is sensitive to bias-illumination degradation, the measurement should be done without exposure to light. Lee *et al*. developed an a-IGZO TFT capacitance model that allows for the frequency-independent capacitance of localized states, and in turn the acceptor-like DOS, to be derived using the multi-frequency *C–V* response without illumination [75]. However, none of these works have addressed the need for a comprehensive a-IGZO subgap DOS model that is robust enough to

accommodate a wide variety of deposition conditions and has explicitly defined acceptor/donor assignments derived from experimental and theoretical evidence.

In this chapter, using a combination of optical methods and *C–V* measurements that are described in the literature, we develop an a-IGZO DOS model over the entire range of the band-gap. We also incorporate published data in the literature to complement and calibrate our experimental results. The photoluminescence (PL) spectrum, though commonly used in the analysis of compound (III-V, II-VI) semiconductors, is rarely reported for a-IGZO [76]–[78]. We measure the PL spectrum of a-IGZO thin film to confirm the results of our DOS extraction and, together with numerical simulations, assist the assignment of subgap states as either donor- or acceptor-like. By building our a-IGZO DOS model from multiple sources, we expect it to be robust and applicable to any laboratory research or industrial production setting.

3.2 Experimental Setup

An a-IGZO thin film with thickness of 100 nm is deposited using RF sputtering at room temperature on a clean quartz glass substrate. The sample is then annealed at 300 °C for 30 minutes in ambient air on a hot plate. The optical absorption spectrum of the a-IGZO thin film is measured with a Cary 5E UV-Vis spectrometer. The spectrometer collects the thin-film transmittance of a polarized monochromic light with wavelength varying from 300 nm (4 eV) to 1000 nm (1.24 eV). The PL spectrum of the a-IGZO film is then measured at temperatures of T = 300 K and at T = 8 K using a system consisting of a grating monochromator, a lock-in amplifier, a photodiode detector, and a closed-cycle helium cryostat. The source of the PL excitation is a He-Cd laser of wavelength λ = 325 nm with laser power of 50 W/cm^2. An in-house LabView program adjusts the

monochromator during data collection to sweep the emission wavelength from 330 nm to 700 nm at 1 nm intervals with 300 ms integration time.

For the a-IGZO TFT multi-frequency *C*–*V* measurements, bottom-gate TFTs are fabricated on glass substrates. The gate metal is sputtered, defined, and then followed by a bilayer of PECVD gate insulator. The gate insulator is a 400-nm layer of a-SiN_X (interfacing with gate metal) and 50-nm layer a-SiO_X (interfacing with the a-IGZO). The 45 nm-thick a-IGZO islands are sputtered, defined, and followed by the S/D electrodes. The fabricated devices have width (W) = 25 μm and length (L) = 10 μm. The *C*–*V* characteristics between the gate and S/D (tied together) electrodes are measured for six different a-IGZO TFTs on the same substrate by using an *LCR* meter (HP 4284A) at room temperature in the dark. The gate-to-S/D voltage ($V_{G\text{-}S/D}$) range is −20 to 20 V, and its ramp-up speed is 0.4 V/s. The amplitude (A) and frequencies (f_n) of the small-signal voltage used are A = 0.05 V and f_1=50 kHz, f_2=250 kHz, and f_3=1 MHz. With one of the six a-IGZO TFTs, we also measured the temperature-dependent *I*–*V* characteristics from 30 °C to 70 °C (10 °C intervals) and extracted the drain current activation energy [32] (E_{act}) as a function of the gate-to-source voltage (V_{GS}) under a fixed drain-to-source voltage (V_{DS} = 0.1 V).

3.3 Results and Discussion

The optical absorption spectrum (α) of the a-IGZO thin film on a quartz substrate is shown in linear and semi-logarithmic scale in Figure 3.1(a). For incident photon energies greater than 3 eV, a-IGZO shows strong absorption of at least 10^4 cm^{-1} and α increases linearly with energy. The optical band gap (E_g) of 3.37 eV can be extracted from α by extrapolating the absorption edge to its x-intercept. In the semi-logarithmic scale of

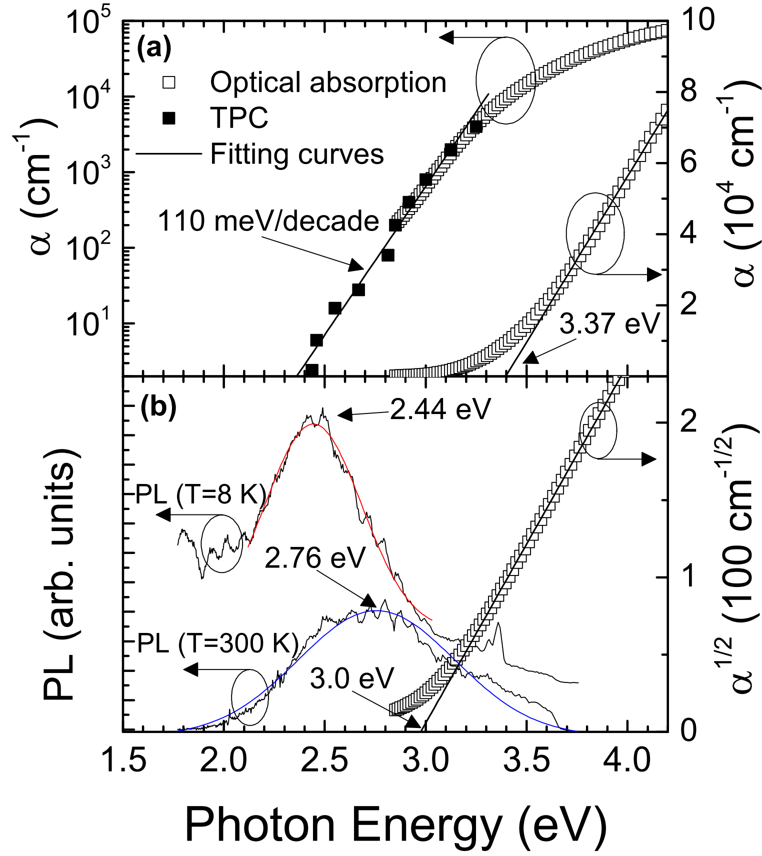


Figure 3.1 (a) The absorption spectrum of a-IGZO thin film is shown in linear and semi-logarithmic scale as empty squares (□). The transient photocapacitance (TPC) spectroscopy data from literature are reproduced in the figure as solid squares (■) [80]. The absorption edge in linear scale is used to extract the optical gap by extrapolating the *x*-intercept. (b) The PL emission at T = 8 K and T = 300 K are shown and fitted to Gaussian functions. The Tauc gap energy is extracted from the square root of optical absorption.

Figure 3.1(a), the exponential decay of α, or the Urbach edge, is visible for energies below E_g. It can be described by the equation

$$\alpha(\hbar\omega) = \alpha_0 \exp\left(\frac{E-\hbar\omega}{E_0}\right), \tag{3-1}$$

where E_0 is the characteristic energy slope of the Urbach edge and α_0 is a constant factor. The Urbach edge, which was first reported for alkali halide crystals [79], represents the band broadening due to disorder and is observed in all amorphous semiconductors [16]. In the figure, α is truncated at 2.81 eV, after which the signal intensity falls below the

detection background of the UV-Vis spectrometer. More data points are required to precisely determine the slope of the Urbach edge and extract E_0. To achieve this, the transient photocapacitance (TPC) spectroscopy data of the a-IGZO metal-insulator-semiconductor (MIS) structure is adapted from Erslev [80] and reproduced in Figure 3.1(a) as solid squares. Details regarding TPC spectroscopy can be found elsewhere [81], [82] and is summarized here. A voltage-filling pulse (zero bias) is first applied to the reverse-biased MIS junction to fill the previously depleted regions. Immediately after the voltage pulse, the capacitance transient is measured while a sub-band gap light is illuminating the sample. These two steps are then repeated without the optical excitation. The measured transient signals are each integrated over the time between the two pulses, and their difference, normalized over photon flux, is taken to be the TPC at that photon energy. Repeating this process for the photon energies of interest produces the TPC spectrum. At low optical intensities, the TPC signal is proportional to the joint DOS, similar to optical absorption but at much greater sensitivity [81]. Therefore, the signal decay in TPC spectrum is also the Urbach edge. Since we are only interested in the slope instead of actual values, the TPC data, which is in arbitrary units vs. photon energy, can be calibrated to Figure 3.1(a) by vertically aligning its data points (solid squares) with absorption (open squares) at corresponding energy values until the two curves effectively overlap over a significant range of values. We then extract the characteristic Urbach energy to be $E_0 = 110.5 \pm 2.3$ meV. Assuming parabolic band edges, the Tauc gap energy of 3.0 eV can also be extrapolated from $\sqrt{\alpha}(E)$ as shown in Figure 3.1(b). This value is consistent with our previous work [30] and other reported values in the literature [28], [29].

The PL spectrum of a-IGZO thin film at T = 8 K and T = 300 K are shown in Figure 3.1(b) for emissions between 330 nm (3.75 eV) and 700 nm (1.77 eV). At T = 8 K, we observe a broad deep-level emission at 2.44 eV followed by a weak near band-edge (NBE) emission at 3.4 eV. At room temperature, the NBE emission is almost completely obscured. We fit the deep-level emission with a Gaussian function and find that at T = 300 K the emission is centered at λ = 2.76 eV with full-width at half-maximum (FWHM) of $\Delta E_{1/2}$ = 0.91 eV. At T = 8 K, the deep-level emission is described by λ = 2.44 eV and $\Delta E_{1/2}$ = 0.57 eV. In PL spectroscopy, after an electron has been excited to the conduction band, there are four possible recombination processes: (i) band-to-band, (ii) electron trap-to-hole trap, (iii) band-to-hole trap, and (iv) electron trap-to-band. In the PL spectrum, the dominance of the deep-level emission over the NBE emission is similar to what has been reported in the literature [76], [78], meaning that the main radiative recombination process in a-IGZO cannot be band-to-band transition and must involve at least a trap level. We note that the deep-level emission peak energies are different from the one detected near 1.77 eV (700 nm) by Yamaguchi *et al*. At T = 8 K in Figure 3.1(b), there appears to be a small PL response at 1.77 eV in our a-IGZO thin film, but because it is at the edge of our detection range, we limit our discussion to the peak at 2.76 eV within the scope of this chapter. We speculate that the peaks represent two distinct transitions within the band gap, and both or only one may be observed prominently in a-IGZO depending on deposition conditions and measurement setup.

We extract the DOS near E_C using multi-frequency C–V spectroscopy [75], which is briefly described as follows. As shown in Figure 3.2 inset (i), the a-IGZO TFT under test can be modeled with an equivalent circuit consisting of gate insulator capacitance (C_{OX}),

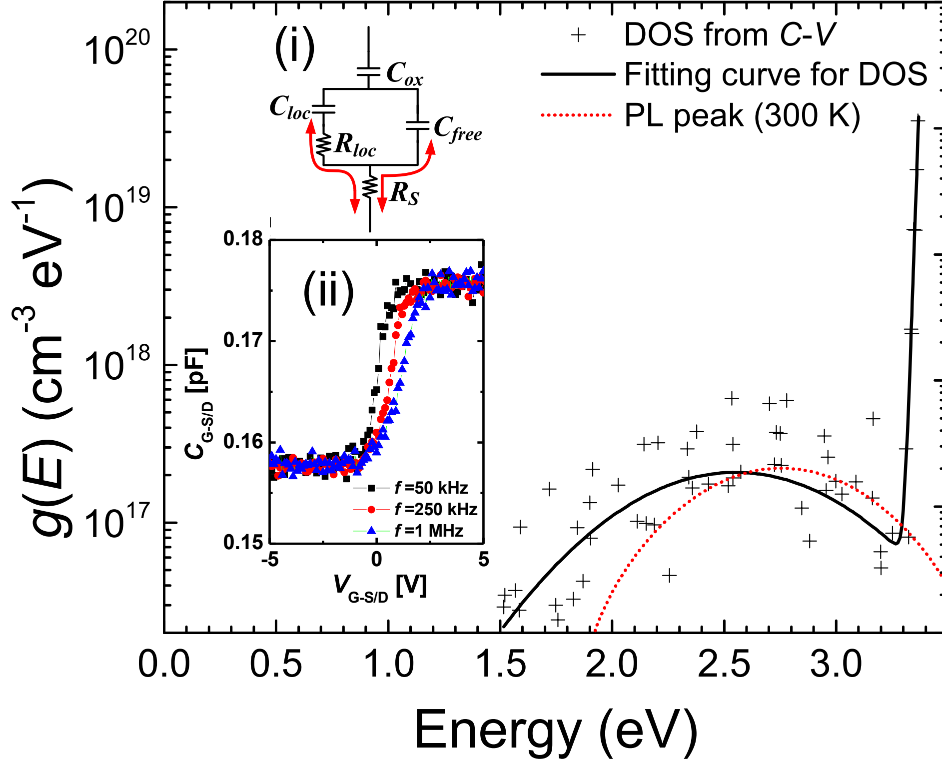


Figure 3.2 The a-IGZO DOS extracted from multi-frequency *C*–*V* measurements (crosshairs, +) and the associated fitting curve. Inset (i) shows the equivalent RC model used to extract the DOS from multi-frequency *C*–*V* measurements of a-IGZO TFTs. Inset (ii) shows the frequency-dependent *C*–*V* for one of the six a-IGZO TFTs as measured.

capacitance of V_{GS}-responsive charges captured/released by the subgap states at corresponding energy levels (C_{LOC}), equivalent resistance of the C_{LOC}-related charges (R_{LOC}), and capacitance of V_{GS}-responsive free carriers (C_{FREE}). Assuming that the *f*-dependence is entirely contained in the channel-to-S/D series resistance (R_S), the *f*-independent intrinsic *C*–*V* can be derived from the *C*–*V* at different frequencies. The *C*–*V* at f = 50 kHz, 250 kHz, and 1 MHz for a single TFT are shown in Figure 3.2 inset (ii). From the resulting *f*-independent *C*–*V* (not shown) we can extract the DOS located in the range of energies observable by electrical measurements. This is repeated for six different TFTs on the same substrate and the combined DOS are shown in Figure 3.2 as crosshairs

(some points omitted for clarity). We observe in Figure 3.2 that at energies closer to E_C, the bandtail states are an exponential distribution and can be described by the equation

$$g_{ta}(E) = N_{ta} \exp\left(\frac{E - E_C}{E_a}\right), \tag{3-2}$$

where N_{ta} is the maximum density of the conduction bandtail states and E_a is the bandtail slope. We then extract $N_{ta} = 4.2\times10^{19}$ eV^{-1}cm^{-3} and $E_a = 11 \pm 0.3$ meV by fitting the data points to Equation (3-2). The conduction bandtail slope extracted this way is comparable to the values derived from numerical simulation [83] and carrier transport [84] studies. The deep-gap states we model using a Gaussian distribution of the form

$$g_{ga}(E) = N_{ga} \exp\left[-\left(\frac{E - \lambda_a}{\sigma_a}\right)^2\right], \tag{3-3}$$

where N_{ga}, λ_a, and σ_a are the Gaussian peak value, the mean energy, and the standard deviation, respectively. We calculate the parameters $N_{ga} = 2 \times 10^{17}$ eV^{-1}cm^{-3}, $\lambda_a = 2.55\pm0.37$ eV, and $\sigma_a = 0.69$ eV by fitting the DOS near the midgap to Equation (3-3). The λ_a and the FWHM ($\Delta E_{1/2} = 0.97$ eV) of the E_C deep-gap states are very close to those of the PL deep-level emission observed in Figure 3.1(b). To verify this visually, we superimpose a Gaussian distribution centered at 2.76 eV representing the PL deep-level emission in Figure 3.2 as a dashed curve. We observe a significant overlap of the two Gaussians, which suggests that they are possibly of the same origin involving deep-gap states near the E_C.

To validate the DOS extracted from multi-frequency *C–V*, E_{act} as a function of V_{GS} is extracted from the temperature-dependent *I–V* characteristics from 30 °C to 70 °C following the methodology described in Chen *et al.* [32] The Arrehenius plot and the extracted E_{act} as a function of V_{GS} are shown in Figure 3.3(a) and Figure 3.3(b), respectively. The E_{act} in the figure is the average barrier height for an electron trapped in

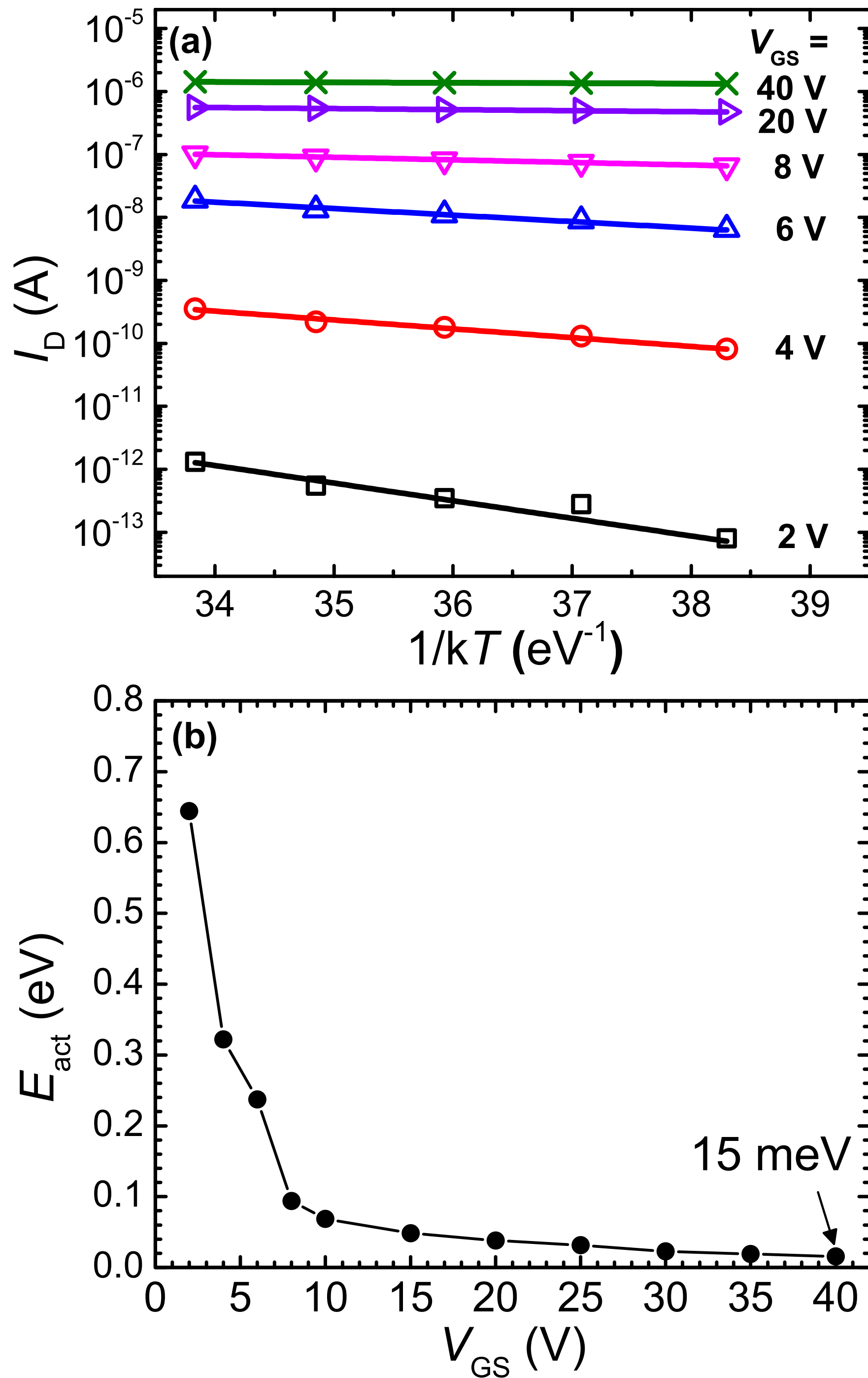


Figure 3.3 (a) The Arrhenius plot used to extract the a-IGZO activation energy E_{act} from the temperature-dependent TFT *I–V* characteristics from 30 °C to 70 °C. (b) The activation energy of a-IGZO as a function of TFT gate-source voltage. The activation energy saturates at E_{act} = 15 meV for high gate biases.

the localized states needed to jump into the conduction band. It represents the difference between the E_C and the Fermi level (E_F) at the a-IGZO/gate insulator interface ($E_C - E_F$) and any influences from the bulk. It has been shown in hydrogenated amorphous silicon (a-Si:H) TFT numerical simulations that at high V_{GS}, the deep-gap states have no influence on E_{act}, which actually approaches E_a for values less than 20 meV [85]. In the case of a sharp conduction bandtail slope, the movement of E_F in response to V_{GS} would become limited in the vicinity of a large density of tail states, i.e. when E_{act} approaches E_a. We observe in Figure 3.3 that at V_{GS} = 40 V, E_{act} saturates at 15 meV, which is very close to E_a = 11 meV. This shows that our DOS parameters extracted from multi-frequency *C*–*V* spectroscopy are reliable.

3.4 DOS Model of a-IGZO

Based on our experimental data and the extracted parameters, we construct a model for the subgap DOS of a-IGZO, which is shown in Figure 3.4. As previously mentioned, the conduction bandtail and deep-gap states are given by exponential and Gaussian distributions with parameters extracted from multi-frequency *C*–*V* measurements. We can combine Equations (3-2) and (3-3) into a single expression

$$g_a(E) = g_{ta}(E) + g_{ga}(E) = N_{ta} \exp\left(\frac{E-E_C}{E_a}\right) + N_{ga} exp\left[-\frac{(E-\lambda_a)^2}{\sigma_a^2}\right]. \quad (3\text{-}4)$$

The above equation alone provides no information about the donor/acceptor assignment of the g_{ga} states. In semiconductors, donor-like defect states are charge-neutral when occupied by electrons and positively charged when empty, whereas acceptors are charge-neutral when empty and negatively charged when occupied by electrons [86]. Most states above the Fermi level are assumed to be occupied by electrons

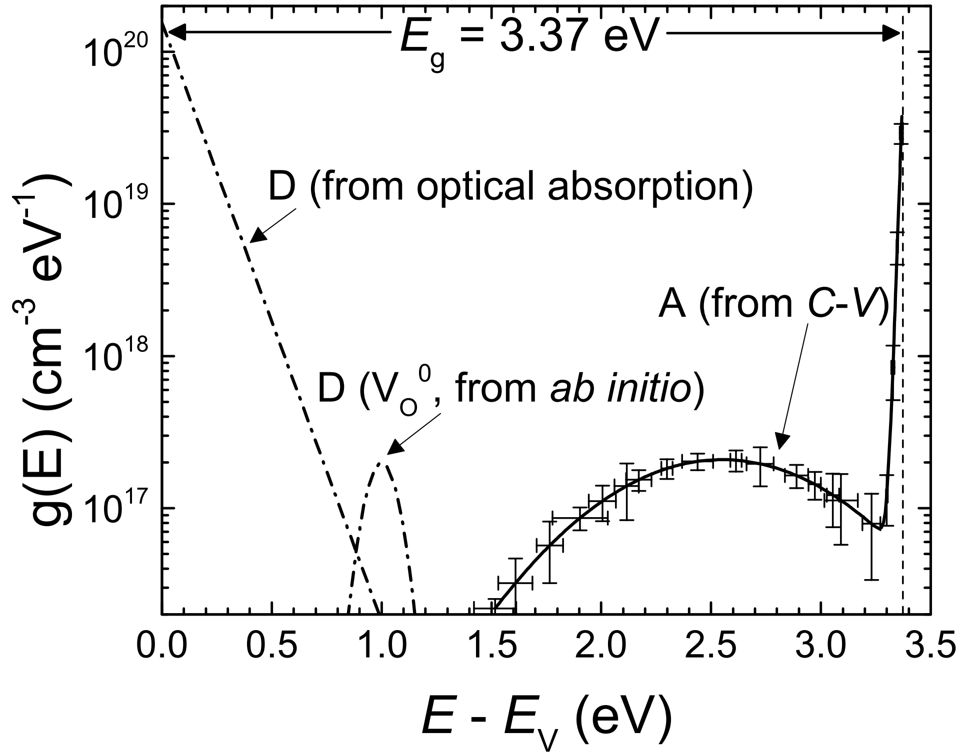


Figure 3.4 The proposed a-IGZO subgap DOS model derived from electrical and optical characterization. In this figure, D denotes donor-like states and A denotes acceptor-like states. The fully occupied deep-gap donor states (V_O^0) are adopted from first-principles calculations in the literature [31].

and those below, empty. The multi-frequency *C–V* method for extracting the DOS is responsive to both trapping and de-trapping of charge carriers at defect states and cannot differentiate between the two processes. Two-dimensional numerical simulations have shown that donor assignment has no impact on TFT threshold voltage (V_{th}), while acceptor assignment causes V_{th} to shift with peak density. The latter is consistent with experimental TFT *I–V* characteristics, therefore we designate the conduction band deep-gap states acceptor-like as shown in the figure. Although this assignment is different from what was used in previous work on a-IGZO TFT numerical simulations [83], it best describes the data collected in this study.

For the density of subgap states near the E_V, we also represent the valence bandtail states using an exponential expression

$$g_{td} = N_{td} \exp\left(\frac{E_V - E}{E_d}\right), \tag{3-5}$$

where N_{ta} is the maximum density of the valence bandtail states and E_d is the valence bandtail slope. From the results of our optical absorption experiment and the TPC spectrum in the literature, we have determined the Urbach energy to be E_0 = 110 meV. Though the Urbach edge is given by the convolution of the conduction and valence bandtail states, the characteristic energy width of the conduction bandtail states is much smaller than the Urbach energy. Therefore we expect the valence bandtail states to dominate the joint DOS of a-IGZO, similar to a-Si:H [16], which allows us to approximate the slope of the Urbach edge as the valence bandtail slope ($E_d \approx E_0$ = 110 meV). In our model, we have adopted $N_{td} = 1.5\times10^{20}$ cm^{-3}eV^{-1} from the literature [83].

From first-principles calculations based on density functional theory, it was found that oxygen vacancies form fully occupied deep donor levels (V_O^0) in both crystalline [31] and amorphous [29] IGZO located around 1.0 eV above E_V. The large molecular spacing of the oxygen vacancy is expected to trap and prevent the electrons from being released. We adopt this in our model in the form of a Gaussian distribution:

$$g_{gd} = N_{gd} \exp\left[-\frac{(E-\lambda_d)^2}{\sigma_d^2}\right], \tag{3-6}$$

where $N_{gd} = 2\times10^{17}$ eV^{-1}cm^{-3}, λ_d = 1.0 eV, and σ_d = 0.1 eV. Similar to the conduction band subgap states, the valence bandtail and deep-gap states can also be combined into a single expression

$$g_d = g_{td}(E) + g_{gd}(E) = N_{td} \exp\left(\frac{E_V - E}{E_d}\right) + N_{gd} exp\left[-\frac{(E-\lambda_d)^2}{\sigma_d^2}\right]. \tag{3-7}$$

Conduction band subgap states				
N_{ta} **(cm^{-3}eV^{-1})**	E_a **(meV)**	N_{ga} **(cm^{-3}eV^{-1})**	λ_a **(eV)**	σ_a **(eV)**
4.23×10^{19}	11 ± 0.3	2.08×10^{17}	2.55 ± 0.37	0.69
Valence band subgap states				
N_{td} **(cm^{-3}eV^{-1})**	E_d **(meV)**	N_{gd} **(cm^{-3}eV^{-1})**	λ_d **(eV)**	σ_d **(eV)**
1.55×10^{20}	110	2.0×10^{17}	1.0	0.01

Table 3.1 Parameters used in the proposed a-IGZO subgap DOS model.

The parameters of our a-IGZO DOS model are summarized in Table 3.1.

Our DOS model can be used to explain the PL emission spectrum described earlier in Figure 2.1(b). In the case of trap-to-trap transition, the recombination energy is only 1.5 eV, which is much lower than 2.76 eV and therefore cannot be responsible for the deep-level emission we have observed. The remaining two scenarios of band-to-hole trap (transition energy 2.37 eV) and electron trap-to-band (transition energy 2.55 eV) are potential candidates. In the former, the oxygen vacancy deep donor could trap a hole and then hypothetically recombine with a photo-excited electron in the conduction band. Although oxygen vacancy defects are often cited as the source of deep-level green emission in ZnO [87], Taniguchi *et al*. [77] and colleagues have shown experimentally that they may act as non-radiative recombination centers in a-IGZO. The intensity of deep-level emissions is quenched for a-IGZO deposited in low oxygen partial pressure [76] (p_{O_2}) or annealed in oxygen-deficient ambient (e.g. N_2) [77], both of which are assumed to enhance the formation of oxygen vacancies. This would eliminate all but the electron trap-to-band transition as the origin of the deep-level emission. Regarding the nature of the electron trap states, Ide *et al*. suggested that excess or weakly-bonded oxygen in the a-IGZO microstructure can exist as a broad distribution of deep-gap states

near E_C [88]. Desorption of O_2 was observed in thermal desorption spectrum measurements for a-IGZO films annealed in O_3 or O_2 ambient or deposited under high p_{O_2}. Results from our group [89] and in literature [90] also indicate that p_{O_2} has a strong impact on g_{ga}. This is consistent with our assignment based on numerical simulations that g_{ga} are acceptor-like because excess/weakly-bonded oxygen can accept/capture electron through $O^0 + e^- \rightarrow O^{1-}$ and/or $O^{1-} + e^- \rightarrow O^{2-}$. The O^{2-} ion cannot capture any electrons because of its filled outer shell. In this physical picture, the photo-excited electron falls to the band edge and then to an electron trap through scattering. It then radiatively recombines with a hole in the valence band, emitting at energy of 2.55 eV. The fact that the shape of the deep-level emission and the g_{ga} deep-gap states are very similar also supports this proposition.

It is informative to compare the DOS of a-IGZO with that of a-Si:H, which also consists of exponential tail states and Gaussian deep-gap states [16], [26]. In a-Si:H, the conduction and valence bandtail states are a result of fluctuations of the Si-Si bond angles and lengths. Structural disorder also causes the bandtail states in a-IGZO, but its conduction bandtail slope is sharper and the peak density is at least one to two orders of magnitude lower than a-Si:H because of the large overlapping s orbitals of the heavy In^{3+} cation [18]. The deep-gap states in a-Si:H are mainly attributed to dangling Si bonds and can be greatly reduced by optimized hydrogenation. The deep-gap states for a-IGZO, due to its nature as an oxide semiconductor, can be attributed to localized oxygen-deficiency or excess oxygen in the a-IGZO thin film. As mentioned in this chapter, oxygen vacancies and excess oxygen in the a-IGZO microstructure form deep donor states and deep acceptor states, respectively. Kamiya and Hosono stated that low p_{O_2} during

deposition produces films with high electron density and this is linked to oxygen vacancies, whereas the low electron density in high p_{O_2}-deposited films is attributed to excess oxygen [72]. We note that the impact of p_{O_2} on carrier density can be described using only oxygen vacancies, only excess oxygen, or both. Both descriptions are consistent with our conclusion that the transition from g_{ga} to E_V is responsible for the deep-level PL emission.

CHAPTER 4

Oxygen Flow Effects on Electrical Properties and Stability of a-IGZO Thin-Film Transistors

4.1 Introduction

To gain insight on charge injection or defect state creation in the device during bias-temperature stress (BTS) of a-IGZO TFTs, capacitance–voltage (*C*–*V*) measurements are often performed before and after stressing [91]–[93]. Lee *et al.* showed that the dispersion relation of multi-frequency *C*–*V* measurements could be used to extract the a-IGZO TFT subgap density of states (DOS) [75]. However, the relationship between device stability and the subgap DOS was rarely studied by the *C*–*V* method. Kim *et al.* used the multi-frequency *C*–*V* method to compare the positive BTS (PBTS) stability and DOS of a-IGZO TFTs with channel layers sputtered in various oxygen flow ratios [90]. They found that a higher oxygen flow ratio corresponded to a larger PBTS-induced threshold voltage shift (ΔV_{th}) and that the DOS have observable differences for different flow ratios.

For this chapter, we varied the oxygen flow rate during the sputtering of a-IGZO thin films and studied its impact on a-IGZO DOS and TFT electrical properties including stability under both PBTS and negative BTS (NBTS). From the device current–voltage (*I*–*V*) and *C*–*V* characteristics, threshold voltage (V_{th}) and mid-gap voltage (V_{mg}) were

extracted for a-IGZO TFTs before and after BTS. We extracted a-IGZO DOS from multi-frequency *C–V* measurements. The goal of this study is to correlate the TFT *C–V* and *I–V* characteristics and parameters extracted on the same device structure. Both provide different but complementary information about the properties and stability of a-IGZO TFTs and its DOS.

4.2 Experimental

4.2.1 Fabrication of a-IGZO TFTs with Various Oxygen Partial Pressures

To fabricate bottom-gate a-IGZO TFTs, n^{++}-doped silicon wafers with 100 nm of thermally grown SiO_2 were used as gate electrode and gate insulator. The a-IGZO active islands (50 nm) were deposited by dc sputtering with power of 200 W at pressure of 4 mTorr under room temperature and patterned by shadow masking. The sputtering target used has composition ratio of In:Ga:Zn:O = 2:2:1:7. While keeping the total gas flow into the sputtering chamber constant at 31.5 sccm, the oxygen/argon gas flow rate during IGZO sputtering was varied from O_2/Ar = 1.5/30 sccm, 3.2/28.3 sccm, and 4.7/26.8 sccm, which represented 5%, 10%, and 15% oxygen partial pressure (p_{O_2}), respectively. After a-IGZO deposition, thermal annealing was performed at 350 °C for 30 min in ambient air on a hot plate. Then 100 nm of molybdenum (Mo) was sputtered as the source/drain (S/D) electrodes and defined by shadow masking. The fabricated common-gate TFTs with staggered S/D electrodes were designed to have a channel width/length of 300/150 μm.

4.2.2 Measurement of a-IGZO TFT *I–V* and *C–V* Characteristics

The TFT I–V characteristics were measured using an Agilent B1500A semiconductor analyzer both before and after BTS at room temperature. During the measurement of the I–V characteristics, the gate voltage was swept from $V_g = -10$ V to +10 V while V_d = 10 V was applied to the drain terminal, while the source terminal was grounded. During BTS, the sample was first heated to stress temperature T_{st} = 70 °C by a heated chuck. The Agilent B1500 then applied the gate stress voltage for duration of $t_{st} = 10^4$ s while both the source and drain are grounded ($V_d = V_s = 0$ V). For PBTS tests, gate bias stress V_{st} = +10 V was applied to the TFT gate electrode, whereas $V_{st} = -10$ V was applied instead for NBTS. After BTS, the device was allowed to cool to room temperature and its I–V characteristics measured again. All stressing and measurements are done in ambient air in the dark. A different device on the same wafer was used for each BTS test.

The multi-frequency TFT C–V measurements were done at room temperature before and after BTS using a HP 4284A LCR meter. The dc and the small-signal ac voltages are forced through the gate electrode, while any changes to the stored charges due to the ac signal were detected through the shorted source and drain electrodes. The frequencies of the small-signal voltage oscillations are between 20 and 500 Hz. Such low frequencies are selected to allow the charging current to arrive from the source and drain regions. At higher frequencies, the subgap states cannot be filled in time, and the C–V curves become flat lines with no distinct accumulation and depletion regions. This is due to the influence of the highly resistive a-IGZO bulk region.

4.3 Results and Discussion

4.3.1 Impact of Bias-Temperature Stress on a-IGZO TFT *C–V* Characteristics

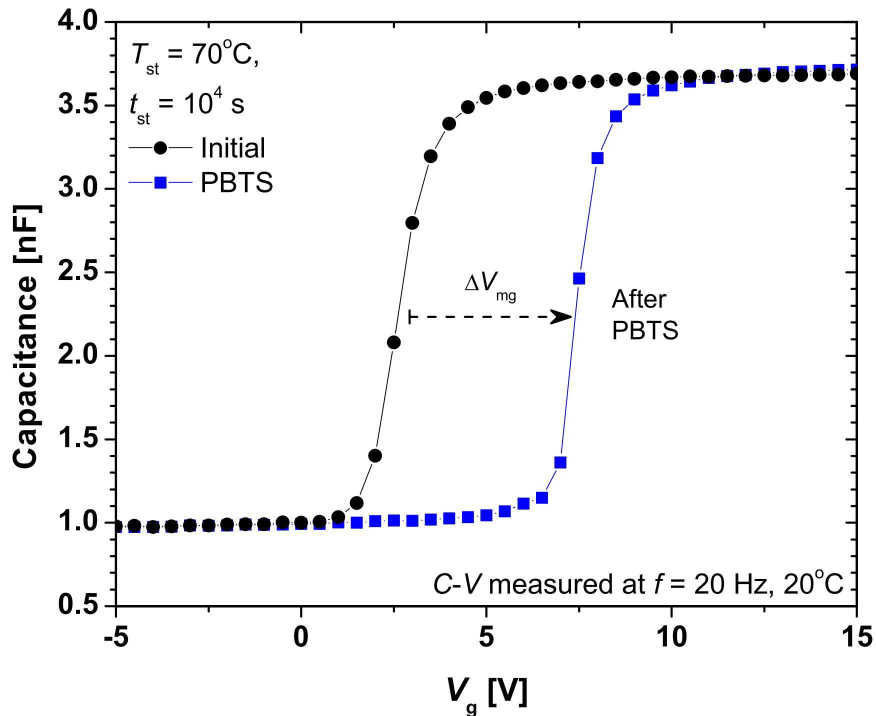


Figure 4.1 *C–V* curves before and after BTS. ΔV_{mg} is the shift of mid-gap voltage before and after BTS with 10% O_2/Ar flow ratio.

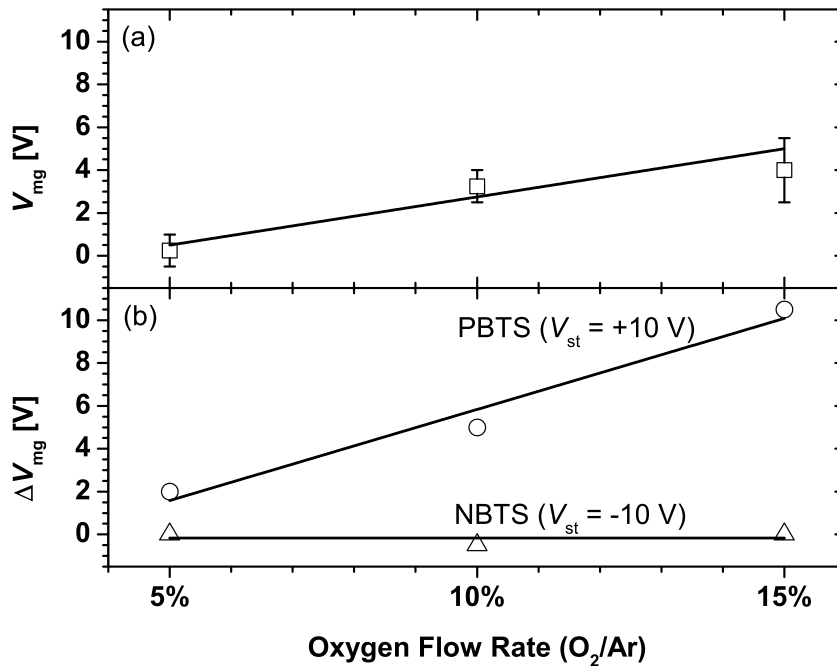


Figure 4.2 (a) The V_{mg} variation before BTS (○) and (b) the shift of V_{mg} after PBTS (■) and NBTS (●) with the oxygen flow rate.

Figure 4.1 shows the *C–V* characteristics of the a-IGZO TFT measured at $f = 20$ Hz before and after PBTS. The *C–V* curve after NBTS shows no visible changes and is omitted in the figure. Only the *C–V* of a-IGZO channel layer sputtered in 10% O_2/Ar flow ratio is shown. Similar curves were obtained for all oxygen flow ratios studied in this chapter. The V_{mg} were extracted at the maximum inclination point in the *C–V* curves. Positive V_{mg} shift (ΔV_{mg}) without any change in curve slope or shape was observed after PBTS. This is also the case for TFTs with channel layers deposited at 5 and 15% oxygen flow (not shown). From these observations, we believe that the fixed and/or trapped charges near the a-IGZO/SiO_2 interface region are most likely responsible for ΔV_{mg} [86]. In this study, the fixed charges could have originated from bonding imperfections of the non-stoichiometric composition (2:2:1:7) a-IGZO influenced by oxygen flow changes during the deposition process. We see in Figure 4.2(a) that TFTs with higher oxygen ratios have higher V_{mg}, indicating that higher oxygen flow can be responsible for larger concentration of negative oxide charges localized near or at the a-IGZO/SiO_2 interface. In Figure 4.2(b), ΔV_{mg} also increased after PBTS for TFTs with higher O_2 ratios. Based on these results we can speculate that larger oxygen flow not only has impact on initial V_{mg} but also produces larger positive shift of V_{mg} after PBTS. These effects might be due to the increase of non-stoichiometry at the a-IGZO/SiO_2 interface.

4.3.2 Impact of Bias-Temperature Stress on a-IGZO TFT *I–V* Characteristics

The TFT *I–V* characteristics for different O_2/Ar ratios before and after stressing are shown in Figure 4.3 for PBTS and Figure 4.4 for NBTS. The device parameters extracted from the *I–V* curves of unstressed TFTs are shown in Table 4.1. The device parameters were extracted from the unstressed a-IGZO TFT *I–V* shown as solid black circles in

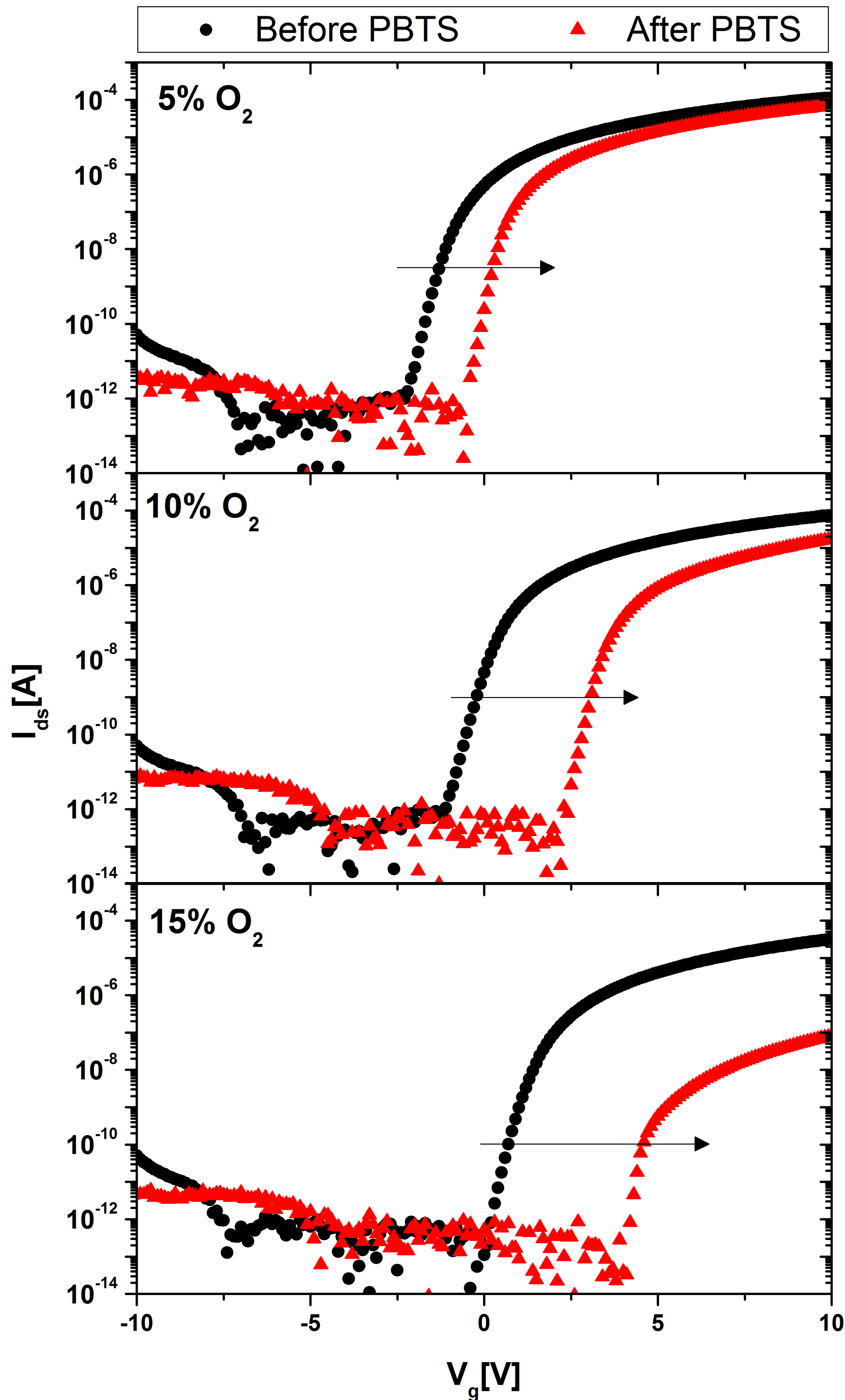


Figure 4.3 The device transfer characteristics for TFTs with different oxygen flow during sputtering. The solid circles and triangles represent before and after positive BTS (V_{st} = 10 V) for 10,000 s at 70 °C respectively.

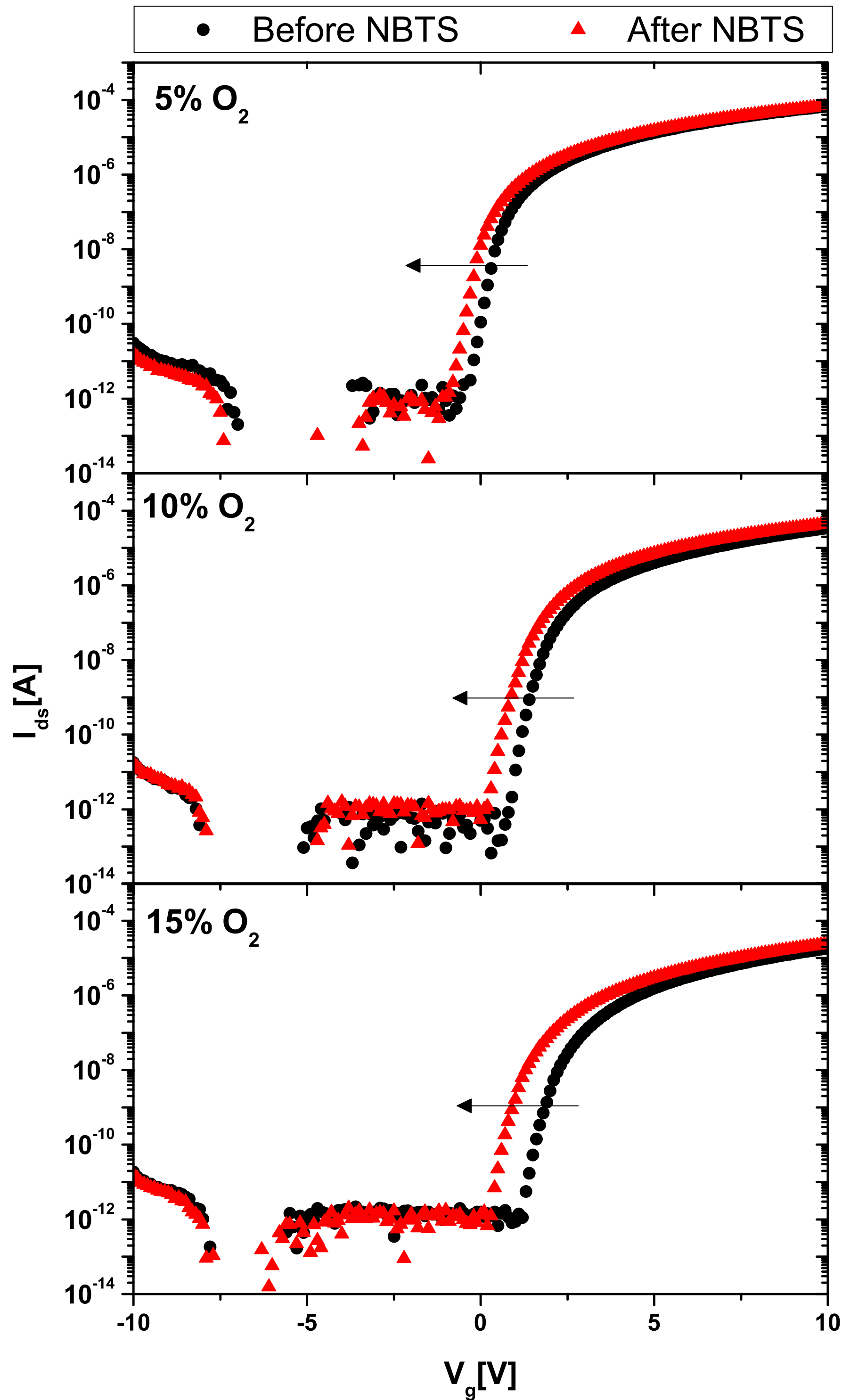


Figure 4.4 The device transfer characteristics for TFTs with different oxygen flow during sputtering. The solid circles and triangles represent before and after negative BTS (V_{st} = −10 V) for 10,000 s at 70 °C respectively.

	I_{on} (A)	I_{off} (A)	V_{th} (V)	μ_{FE} ($cm^2/V{\cdot}s$)	*SS* (V/dec)
5%	$1.14{\times}10^{-4}$	$1.21{\times}10^{-14}$	-1.55	32	0.243
10%	$7.47{\times}10^{-5}$	$2.10{\times}10^{-14}$	-0.34	27.1	0.278
15%	$3.21{\times}10^{-5}$	$1.11{\times}10^{-14}$	1.00	16.7	0.238

Table 4.1 The initial parameters of *I–V* curves with O_2/Ar flow ratios during deposition.

Figures 4.3 and 4.4. The field-effect mobility (μ_{FE}) is extracted from fitting the TFT *I–V* to the ideal MOSFET equation, and V_{th} from extrapolating the fitted curve to the *x*-axis. To examine the impact of BTS on subthreshold operation, the ΔV_{th} was calculated as the difference in the applied V_g that is required for the drain current (I_D) to reach 10^{-9} A before and after BTS. The subthreshold swing (*SS*) is calculated from the inverse average of three values near the maximum transconductance (dI_d/dV_g) point. We observe that μ_{FE} and maximum current (I_{on}) decreased with increasing O_2/Ar ratio. This suggests that increasing the oxygen flow rate reduced the carrier concentration of the samples tested. After PBTS, the ΔV_{th} were positive for all O_2/Ar ratios, while they were all negative after NBTS. For all oxygen flow ratios studied, the extracted V_{th} and ΔV_{th} after PBTS/NBTS are shown in Figures 4.5(a) and 4.5(b), respectively. Two observations can be made from Figure 4.5: 1) ΔV_{th} is smaller for lower p_{O_2} in PBTS 2) the dependence of ΔV_{th} on p_{O_2} in NBTS is insignificant. These trends are consistent with what has been reported in the literature [45], [90]. For NBTS, Chen *et al.* showed that the ΔV_{th} of unpassivated a-IGZO TFT is strongly affected by ambient gas composition during stressing: ΔV_{th} becomes very severe when moisture is present in the ambient gas [94]. This suggests that under NBTS, ΔV_{th} is associated with the adsorption/diffusion of humidity/hydrogen/hydroxyl species in the TFT back channel. Considering that all our samples are stressed under the same

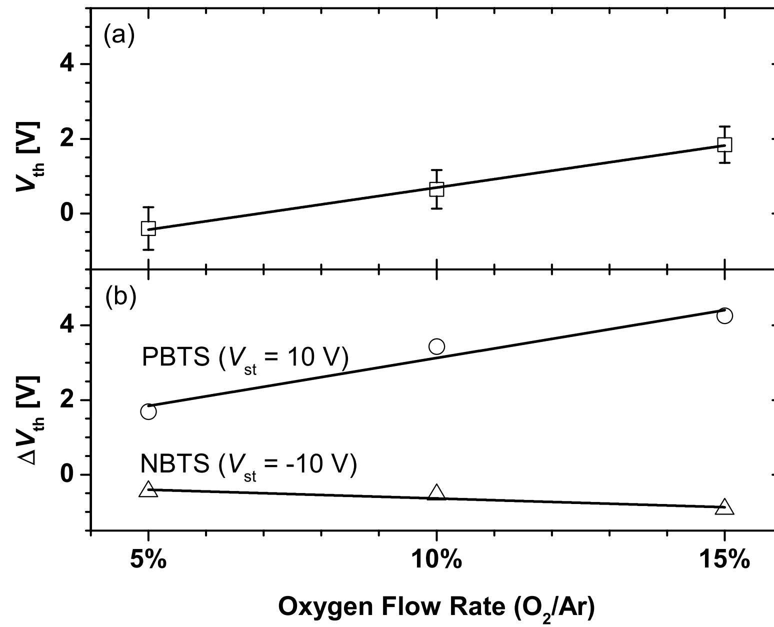


Figure 4.5 (a) Variation of V_{th} before BTS (○) and (b) after PBTS (■) and NBTS (●) with oxygen flow rate.

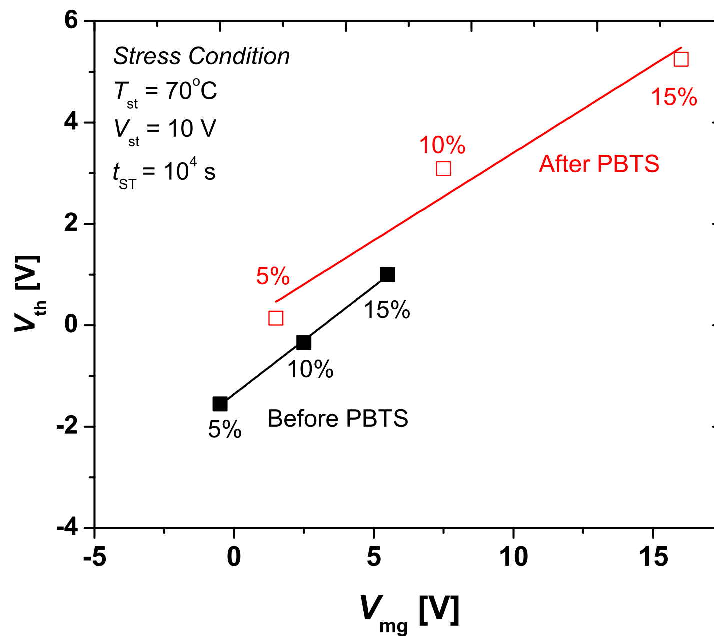


Figure 4.6 The relation between V_{th} and V_{mg} with oxygen flow rate before/after PBTS.

	a	b
Before PBTS	0.425	-1.36
After PBTS	0.345	-0.06

Table 4.2 Linear fitting curve parameters (V_{th} = aV_{mg} + b).

ambient environment, the lack of obvious trends between NBTS and p_{O_2} is within our expectations. In Figure 4.6, we show that the relationship between V_{th} and V_{mg} has a linear dependence on oxygen flow ratio. From this figure, a linear relationship can be established between TFT *I*–*V* (represented by V_{th}) and *C*–*V* (represented by V_{mg}) data, which holds even after the application of PBTS. The fit parameters for the linear relationship are shown in Table 4.2.

It should be noted that as short as 30 minutes after the stress bias was removed and device returned to room temperature, the threshold voltage began to shift back towards its initial state. While this effect is not as pronounced for devices subject to NBTS because the magnitudes of ΔV_{th} were small, the recovery was readily observable for TFTs applied with PBTS. Such recovery has been observed in the literature for unpassivated a-IGZO TFTs after PBTS [95] and NBTS [96].

4.3.3 Extraction of DOS of a-IGZO TFTs from Multi-frequency *C*–*V*

Measuring the *C*–*V* at different frequencies can allow us to extract the subgap DOS of a-IGZO [75] and investigate the influence of p_{O_2}. Knowledge of a-IGZO DOS is critical for SPICE simulations and for improving the electrical properties of a-IGZO TFTs. The experimental subgap DOS for a-IGZO TFTs of different p_{O_2} are shown in Figure 4.7 as empty symbols in each sub-figure. The experimental data were extracted from multi-frequency *C*–*V* measurements following the methodology described in [75] and then

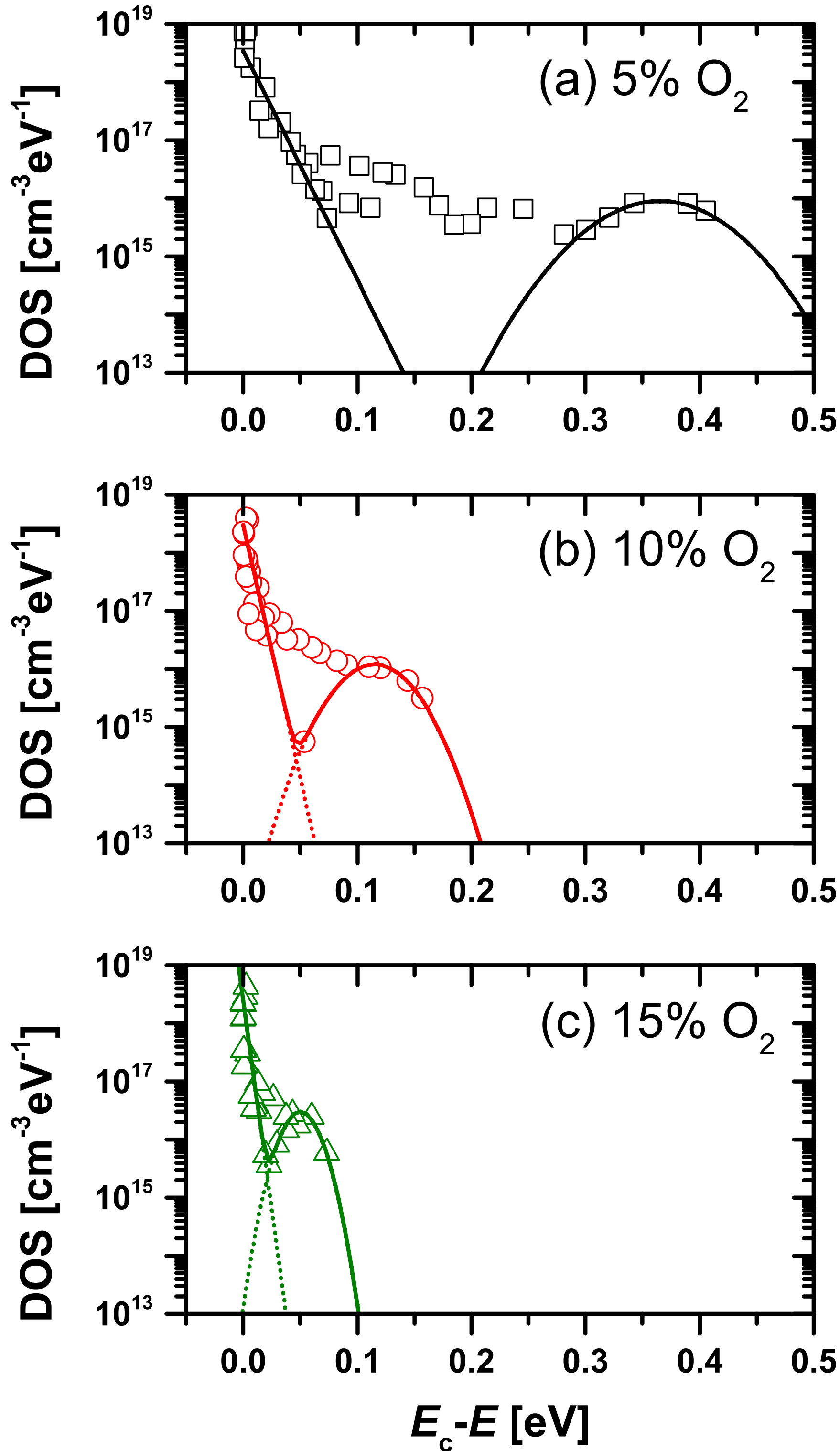


Figure 4.7 The a-IGZO DOS extracted from multi-frequency *C–V* for p_{O_2} of (a) 5%, (b) 10%, and (c) 15%. The solid lines are calculated from Equations (4-1) and (4-2), and the symbols are experimental data.

	N_{ta} (cm^{-2}eV^{-1})	E_a (meV)
5%	3.50×10^{18}	11
10%	3.00×10^{18}	5
15%	2.50×10^{18}	3

Table 4.3 Exponential subgap DOS fitting parameters for O_2/Ar flow rate.

	N_{ga} (cm^{-2}eV^{-1})	σ (meV)	λ (eV)
5%	9.00×10^{15}	0.06	0.365
10%	1.20×10^{16}	0.035	0.115
15%	3.00×10^{16}	0.018	0.05

Table 4.4 Gaussian subgap DOS fitting parameter for O_2/Ar flow rate.

fitted to the following proposed a-IGZO DOS model. The model consists of a Gaussian-like distribution and an exponential near the conduction band minimum, as given by Equations (4-1) and (4-2) [97], [98]:

$$g_{\mathrm{G}}(E) = N_{\mathrm{ga}} \exp\left[-\left(\frac{E-\lambda}{\sigma}\right)^2\right], \tag{4-1}$$

$$g_{\mathrm{exp}}(E) = N_{\mathrm{ta}} \exp\left[\frac{(E-E_C)}{E_{\mathrm{a}}}\right]. \tag{4-2}$$

In Equation (4-1), which describes the Gaussian-like states, N_{ga}, λ and σ are the peak density, the mean energy position, and the standard deviation of the distribution, respectively. For the exponential states in Equation (4-2), E_C is the conduction band edge energy, N_{ta} is the density of acceptor-like states at $E = E_C$, and E_a is the characteristic slope of the exponential states.

For all p_{O_2} studied, the DOS fits to Equations (4-1) and (4-2) are shown in Figure 4.7 as solid lines, and the extracted parameters of the subgap DOS are shown in Table 4.3

and Table 4.4. We note that there are minor but discernable differences in conduction bandtail states for the different p_{O_2} samples: higher p_{O_2} corresponded to lower N_{ta} and E_a. In a-IGZO, conduction occurs through the overlap of the large 5s orbital of the In^{3+} ion [18]. The conduction bandtail states are thus primarily a result of structural disorder, which we do not expect to be greatly affected by p_{O_2}. For the a-IGZO TFTs deposited under higher p_{O_2} in this study, it is possible that the lower Ar gas flow reduces the damage caused by the high-energy Ar plasma bombardment, which is reflected on the conduction bandtail states. We observe that as P_{O2} increases, the N_{ga} of the Gaussian-like deep-gap states increases and the mean energy position λ shifts towards E_C. Taking the TFT *I–V* characteristics into consideration, increased N_{ga} directly corresponds to reduced μ_{FE} and the shift of V_{th} towards higher positive voltage. These phenomena can be explained by assuming that the deep-gap states are acceptor-like and act as electron traps. Ide *et al*. proposed the idea that incorporation of weakly bonded oxygen, resulting from either high-temperature O_3-annealing or high p_{O_2} during a-IGZO deposition, can manifest itself as a broad distribution of deep-gap states [88]. These oxygen-related states could be either O^0 or O^{1-}, which may accept an electron to become O^{1-} or O^{2-}; O^{2-} ions could not accept an electron due to the filled outer shell. Kamiya and Hosono showed that high p_{O_2} directly leads to low electrical conductivity and TFTs not entering on state (i.e. very high V_{th}) [72], both of which are consistent with our observations. Furthermore, the designation of these deep-gap states as acceptor-like is supported by our previous results on photoluminescence (PL) of a-IGZO thin film [97] and 2D numerical simulations of a-IGZO metal-semiconductor field-effect transistors [98]. It should be noted that in chapter 3, we concluded that the PL deep-level emission peak energy corresponds to λ of

the Gaussian deep-gap states. Thus we expect the PL deep-level emission to shift towards higher energies when p_{O_2} is increased. More experimental work is required to verify this hypothesis.

With regards to PBTS for different p_{O_2}, we speculate that the larger ΔV_{th} for higher p_{O_2} is also associated with the excess oxygen weakly bonded to nearest neighbors. They can exist as non-bridging or free oxygen in the a-IGZO microstructure, and their migration can be accelerated by a combination of electrical field and temperature during PBTS. If we assume that higher p_{O_2} corresponds to greater incorporation of excess/weakly-bonded oxygen in the a-IGZO thin film, then increased accumulation of negatively charged O^{1-} or O^{2-} ions at the a-IGZO/SiO_2 interface could reasonably account for the larger ΔV_{th} in high-p_{O_2} samples. It should be noted that in Ji *et al.*, high-pressure O_2 annealing actually reduced negative-bias illumination stress (NBIS)-induced instability [99]. This was attributed to a reduction of the oxygen vacancy (V_O^0) defects, which could be photoexcited to the V_O^{2+} charged state during NBIS and cause V_{th} to shift. Taking this into consideration along with our results on PBTS, we can then conclude that there exists a continuous spectrum of oxygen incorporation in a-IGZO, depending on deposition and annealing conditions. Oxygen-deficiency and oxygen-excess, both readily discernable through conductivity and carrier density, lead to NBIS and PBTS instability, respectively. We speculate that it may be possible to optimize oxygen content for minimal PBTS and NBIS instability.

CHAPTER 5

Photoluminescence of a-IGZO Thin-Film Transistors

5.1 Introduction

Photoluminescence (PL) spectroscopy is the detection of light emission over a range of wavelengths as the result of radiative recombination between photo-excited electrons and holes [100]. In the study of semiconductor devices, PL spectroscopy has been used very extensively for identification of the impurity levels in materials such as hydrogenated amorphous silicon (a-Si:H) [101] and ZnO [102], as the photoemission energy represents the energy difference between the electron-hole recombining carriers. Few published reports in the literature have applied PL spectroscopy to the transistor channel region as a nondestructive method to rapidly evaluate the bias-operation properties of III-V high-electron mobility transistors [103], [104] and organic transistors [105]**.** To date, however, such a method has never been used to investigate the a-IGZO TFT.

The first reported study of IGZO PL by Jeong *et al*. was performed for crystalline $InGaZnO_4$ (c-IGZO) prepared from high-temperature (1250 °C) solid-state reaction [106]. After c-IGZO was annealed in an oxygen-deficient environment at 900 °C, PL emissions at 2.87 eV and deep-level emission at 1.78 eV were observed. Taniguchi *et al*. measured the low temperature (T = 77 K) PL spectra of sputtered a-IGZO thin films

annealed under different ambient conditions including air, O_2, and N_2 [77]. Together with their colleagues Yamaguchi *et al*. [76] they both observed a negative correlation between carrier concentration and intensity of the deep-level emission at 1.8 eV i.e. carrier concentration decreased when photoemission increased. In their works, oxygen vacancy defects (V_O) were treated as an intrinsic donor and a non-radiative recombination center that was passivated by atomic oxygen during annealing in oxidizing atmosphere (air or O_2). Ota *et al*. also showed that there is a negative correlation between sheet resistance of a-IGZO thin-film and the deep-level emission near 1.8 eV [107]. Tsubuku *et al*. [108] and Ishihara *et al*. [78] confirmed the observation of PL in c-axis-aligned crystalline (CAAC)-IGZO thin film with a strong deep-level emission at 1.87 eV. They attributed this to V_O but did not elaborate on the microscopic origin of this transition. They only suggested that photo-excited holes could be trapped in these V_O states and contribute to negative bias-illumination instability of TFTs. By combining the PL emission spectrum with density of states (DOS) extracted from multi-frequency capacitance–voltage measurements, Yu *et al*. developed a DOS model of a-IGZO and proposed that the deep-level transition at 2.76 eV is the result of electrons transitioning between oxygen-related acceptor-like states and the valence band maximum (E_V) [97]. Recently, Tiwari *et al*. observed in both annealed and as-deposited a-IGZO thin films a near-band edge (NBE) emission at 3.27 eV and a blue emission at 2.76 eV, the latter of which they attributed to electron transition from V_O acting as shallow donor level to valence band [109].

In this chapter, our goal is to study in detail the electron-hole transition that is responsible for the observed deep-level photoemission in a-IGZO. The PL spectra of a-IGZO thin films deposited in different oxygen flow and annealed in atmospheres of

different O_2 concentrations are measured and compared. A number of possible transitions responsible for the observed PL emissions are discussed in connection to experimental results. Finally, PL spectroscopy is then used as a nondestructive method to directly probe the a-IGZO TFT channel before/after the application of bias-temperature stress (BTS).

5.2 Experimental

5.2.1 Fabrication of a-IGZO TFTs and Thin Films for Photoluminescence Spectroscopy

The a-IGZO TFTs used in this study are fabricated on n^{++}-doped silicon substrate with 100 nm of thermally grown SiO_2. The heavily doped silicon and thermal oxide act as gate electrode and gate insulator for the TFTs. The active layer is 50-nm-thick a-IGZO deposited by dc sputtering at 200 W of power. The sputtering target has composition ratio of In:Ga:Zn:O = 2:2:1:7. During deposition of a-IGZO, a mixture of Ar and O_2 gas is injected into the sputtering chamber, with O_2 partial pressure (p_{O_2}) set at 5%. After the a-IGZO islands are deposited and defined by shadow masking, the sample is annealed in room air at 350 °C for 1 hour. The source/drain (S/D) contacts are 100 nm of Mo, also deposited by dc sputtering and defined by shadow masking. The final fabricated a-IGZO TFTs have width/length (W/L) of 3000/3000 μm. The TFTs used in this study are very large by design to facilitate the alignment between the laser and the TFT channel region. For the PL measurements, 250-nm-thick a-IGZO thin films are also deposited on the same SiO_2/Si substrates as the TFTs by dc sputtering at 200 W with p_{O_2} = 5% or 15%. After sputtering, the films are annealed in room atmosphere, O_2, N_2, or low vacuum.

The a-IGZO thin films are annealed at 350 °C for 1 hour on a hot plate in an annealing chamber. When annealing in room atmosphere, the chamber door is left open, and air at time of annealing is at 40% humidity. For annealing in O_2 or N_2 gas, the gas is fed into the chamber with the door closed and exhaust line opened while the hot plate is pre-heated to temperature. After 20 minutes, the door is then opened and the sample set onto the hot plate while the gas continues to flow, then the door is immediately closed. For low-vacuum annealing, the vacuum pump is turned on only after the sample has been set onto the pre-heated hot plate and the door has been closed. The lowest pressure achievable by the mechanical pump is ~10^{-1} Torr. Both O_2 and room air are considered to be high-O_2% atmospheres, and N_2 and low vacuum low-O_2% atmospheres. We expect low-O_2% atmospheres to be relatively deficient but not completely devoid of oxygen species in the annealing chamber.

5.2.2 Measurement of Electrical Properties and Photoluminescence Spectra

A Keysight (Agilent) B1500A semiconductor device parameter analyzer is used to measure the a-IGZO TFT transfer characteristics (I_D–V_{GS}) at room temperature before and after BTS. For BTS, the B1500A applies gate stress voltage of V_{st} = +20 V for positive BTS (PBTS) or −20 V for negative BTS (NBTS) at stress temperature of T = 80 °C while the source and drain electrodes are grounded (V_{DS} = 0 V). Different devices fabricated in the same run are used for PBTS and NBTS such that a fresh device unstressed and not irradiated by the UV laser is used for each experiment. The experiments are repeated several times and only representative data are included in this chapter.

The PL experimental setup used in this study is shown in Figure 5.1 together with a

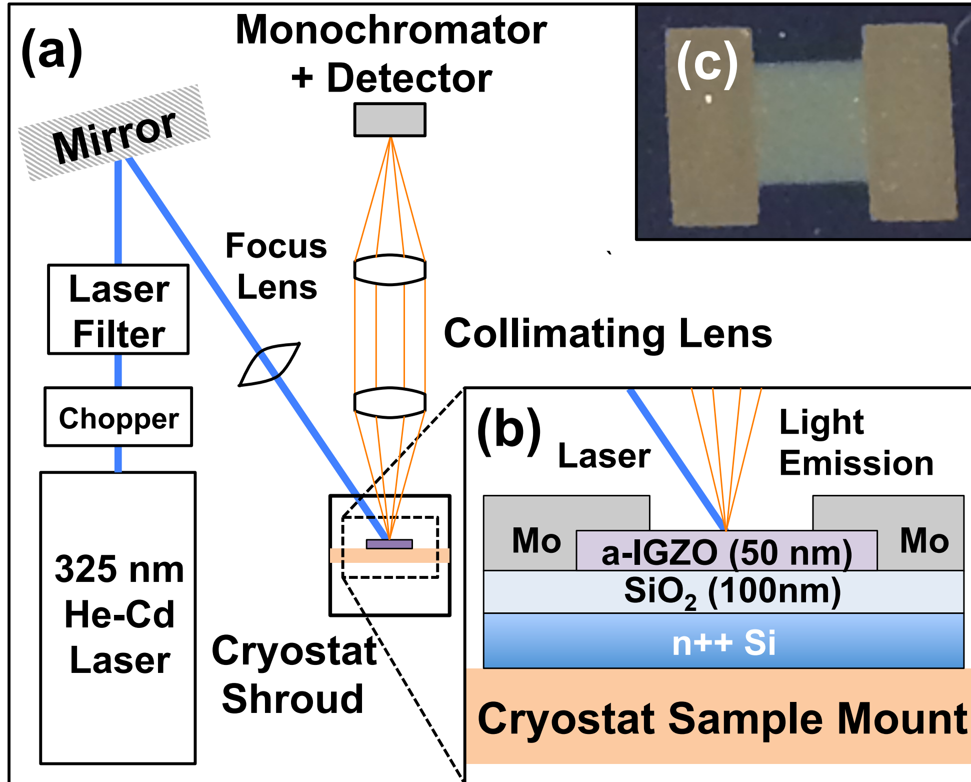


Figure 5.1 (a) The experimental setup for the photoluminescence spectroscopy performed in this study on a-IGZO thin-film transistor channel regions. (b) The top-view diagram showing the sample mounted on the cryostat sample mount and a cross section diagram of the a-IGZO TFT with the channel region irradiated. (c) A photograph of the a-IGZO TFT fabricated by shadow masking in this study.

side-view diagram of the a-IGZO TFT and a photograph of the device fabricated shown as figure insets. All PL spectra in this investigation are measured at T = 33 K using a system consisting of a grating monochromator, a lock-in amplifier, a photodiode detector, and a closed-cycle helium cryostat. The source of the PL excitation is a He-Cd laser of wavelength λ = 325 nm with laser power of 25 W/cm^2. An OD6 laser-line filter (Semrock MaxLine) is used to remove optical noise of the laser for wavelengths outside of 325 nm. The absorption of the laser may be approximated to the first order using film thickness and absorption coefficient at 325 nm from section 3.3. We estimate that 85.1% and 31.7% of the incident light is absorbed by the 50-nm a-IGZO TFT channel region and the 250-nm a-IGZO thin film, respectively. An in-house LabView program adjusts the

monochromator during data collection to sweep the emission wavelength from 350 nm to 800 nm at 2 nm intervals with 300 ms integration time. Using an arbitrary sample with very strong emission in the visible spectrum and identical thickness to the SiO_2/Si substrates, the optical elements are aligned at the beginning of experiments for maximum intensity and are not changed at all throughout the study. We measure the PL spectra of the a-IGZO thin films before any of the TFT structures. The PL spectra for all a-IGZO thin films and TFTs are measured using identical experimental setup and measurement conditions. When measuring the PL of a-IGZO TFTs, the channel region is first manually aligned to the laser at room temperature and then fixed in place with carbon tape. If the device is too small, refraction of the laser through the cryostat window and contraction of the sample/mount at low temperature may cause the laser to become misaligned. Experimentally, we find that the laser may move up to 1 mm vertically and horizontally, which necessitated the use of very large devices. Our experiments on the a-IGZO TFT channel region are performed in the following order: 1) pre-BTS PL, 2) pre-BTS I_D–V_{GS}, 3) BTS, 4) post-BTS I_D–V_{GS}, and 5) post-BTS PL.

5.3 Photoluminescence Spectra of a-IGZO Thin Films and TFTs

In this chapter, PL spectroscopy is performed on a-IGZO thin films deposited and annealed under various conditions. Figure 5.2(a) shows the PL spectra for the same a-IGZO thin film (250 nm, p_{O_2} = 5%) before and after annealing in ambient air. We observe a near-band edge (NBE) emission at 3.35 eV and a deep-level emission at 1.82 eV (full-width half-maximum FWHM = 0.39 eV). From the figure, we see that intensity of the deep-level emission greatly increased after annealing. Even at room temperature, the PL emission of the annealed a-IGZO thin film can be faintly observed by the naked

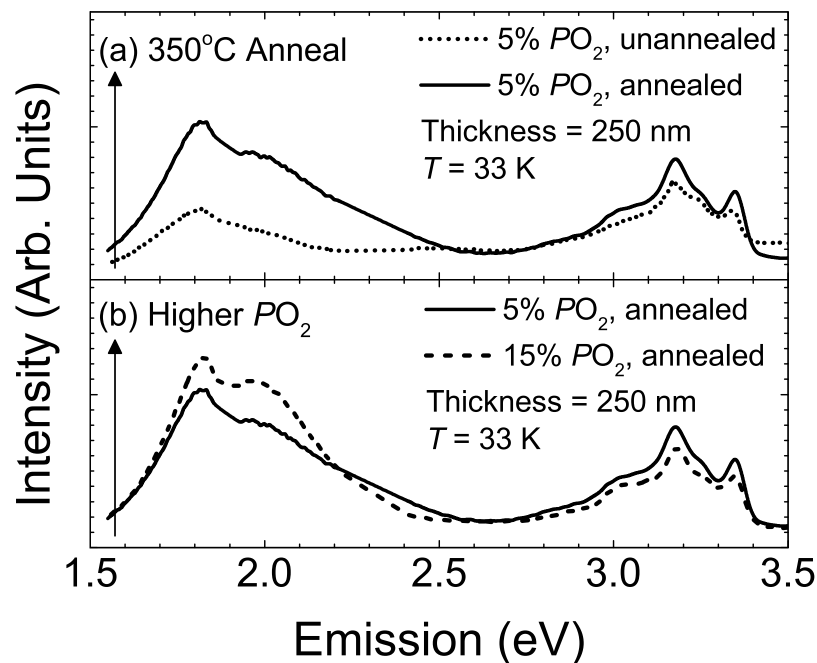


Figure 5.2 The PL emission spectrum of 250-nm a-IGZO films with (a) p_{O_2} = 5% annealed vs. unannealed and (b) p_{O_2} = 5% vs. 15%, both annealed.

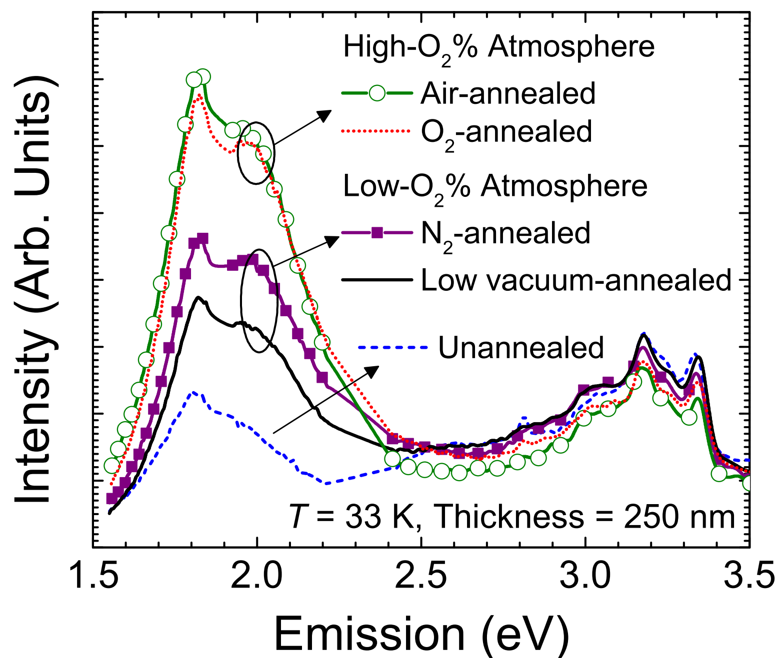


Figure 5.3 The PL emission spectrum for 250-nm a-IGZO thin film with p_{O_2} = 15% annealed in ambient air (open green circles), O_2 (red dotted line), N_2 (purple solid squares), vacuum (black solid line), or as-deposited (blue dashed line).

eye, but is not detectable at all for the as-deposited sample. In Figure 5.2(b), the PL spectra are compared for air-annealed a-IGZO thin films of p_{O_2} = 5% versus 15%, both 250-nm-thick. We note that higher p_{O_2} during a-IGZO deposition increased the intensity of the deep-level emission, although the difference is not as drastic as in Figure 5.2(a). In both sub-figures, no obvious differences are observed for the NBE emission. Figure 5.3 shows the PL spectra of a-IGZO thin films (p_{O_2} = 15%) annealed in various gas environments. For comparison, the PL spectrum for the as-deposited a-IGZO film (p_{O_2} = 15%) is also shown in the figure as a dashed blue line. It is clear that the intensity of the deep-level emission at 1.82 eV for the as-deposited sample is the lowest. After annealing in low vacuum at 350 °C for 1 hour, the deep-level emission intensity increased. The deep-level emission of the N_2-annealed film is still slightly higher than the low vacuum-annealed film. Lastly, the deep-level emissions of air-annealed and O_2-annealed a-IGZO thin films are the strongest and there are no obvious differences between the two spectra. For all five samples, the NBE emissions are all very similar. We can summarize our experimental results on PL of a-IGZO thin film as follows: 1) Deep-level emission is stronger in annealed films than as-deposited films. 2) Deep-level emission is stronger in films annealed in high-O_2% atmospheres than low-O_2%. 3) Deep-level emission is stronger in films deposited in higher p_{O_2}. All variations in the PL spectra shown in Figure 5.3 were outside of possible experimental errors. Experiments were repeated several times to exclude any possible experimental errors.

The I_D–V_{GS} of the a-IGZO TFT used in this study is shown in Figure 5.4 before and after irradiation by the laser used for PL measurements. The TFT electrical properties are very uniform for all devices tested, and one representative device is shown in Figure 5.4.

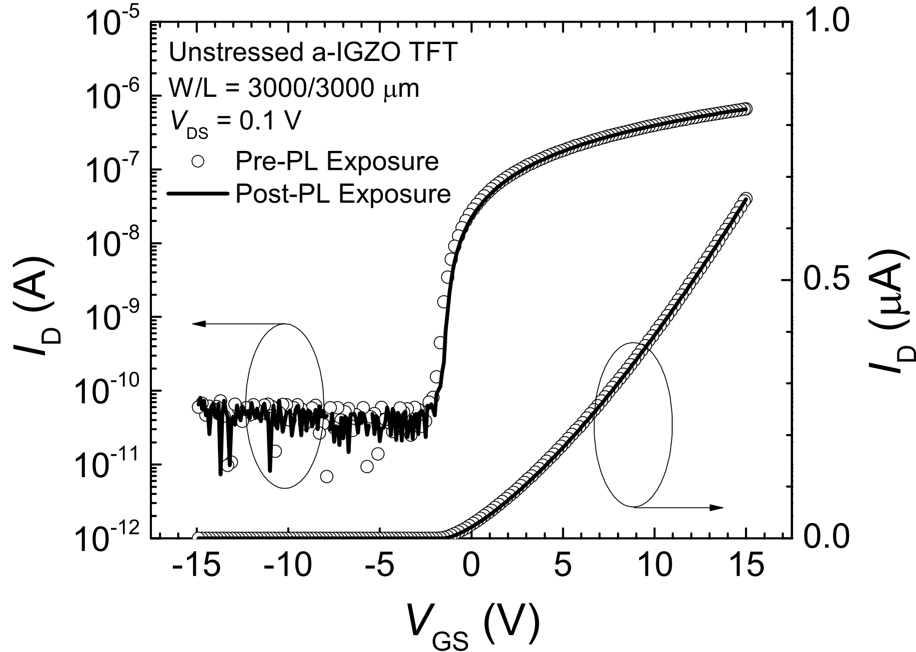


Figure 5.4 The a-IGZO TFT I_D–V_{GS} characteristics before and after exposure to the 325 nm laser. Time of exposure is between 5 and 10 minutes.

The TFT field-effect mobility (μ_{FE}) of 10.2 cm^2/V·s and threshold voltage (V_{th}) of 0.65 V are extracted from a linear fit of the I_D–V_{GS} in the TFT on-region and extrapolating that linear fit to the *x*-axis. The subthreshold swing (*SS*) is extracted to be 340 mV/dec. Exposure to the laser for less than 10 minutes during the PL measurement induced no visible impact on the TFT electrical properties. Figures 5.5(a) and (b) show the a-IGZO TFT I_D–V_{GS} before/after PBTS and NBTS, respectively. After PBTS, the V_{th} shift (ΔV_{th}) was +1.11 V and μ_{FE} decreased slightly to 9.4 cm^2/V·s. The opposite happened after NBTS: μ_{FE} increased to 10.9 cm^2/V·s and V_{th} became more negative (ΔV_{th} = −1.18 V). Any changes to *SS* after BTS are within the extraction error and no trend could be discerned. For both PBTS and NBTS, the ΔV_{th} is obtained from the difference in V_{GS} at a fixed current of I_D = 1 nA in the TFT I_D–V_{GS} before and after BTS is applied. As described in section 5.2, the TFT I_D–V_{GS} is always measured at room temperature immediately before or after BTS, thus the extracted ΔV_{th} is without any influence of the

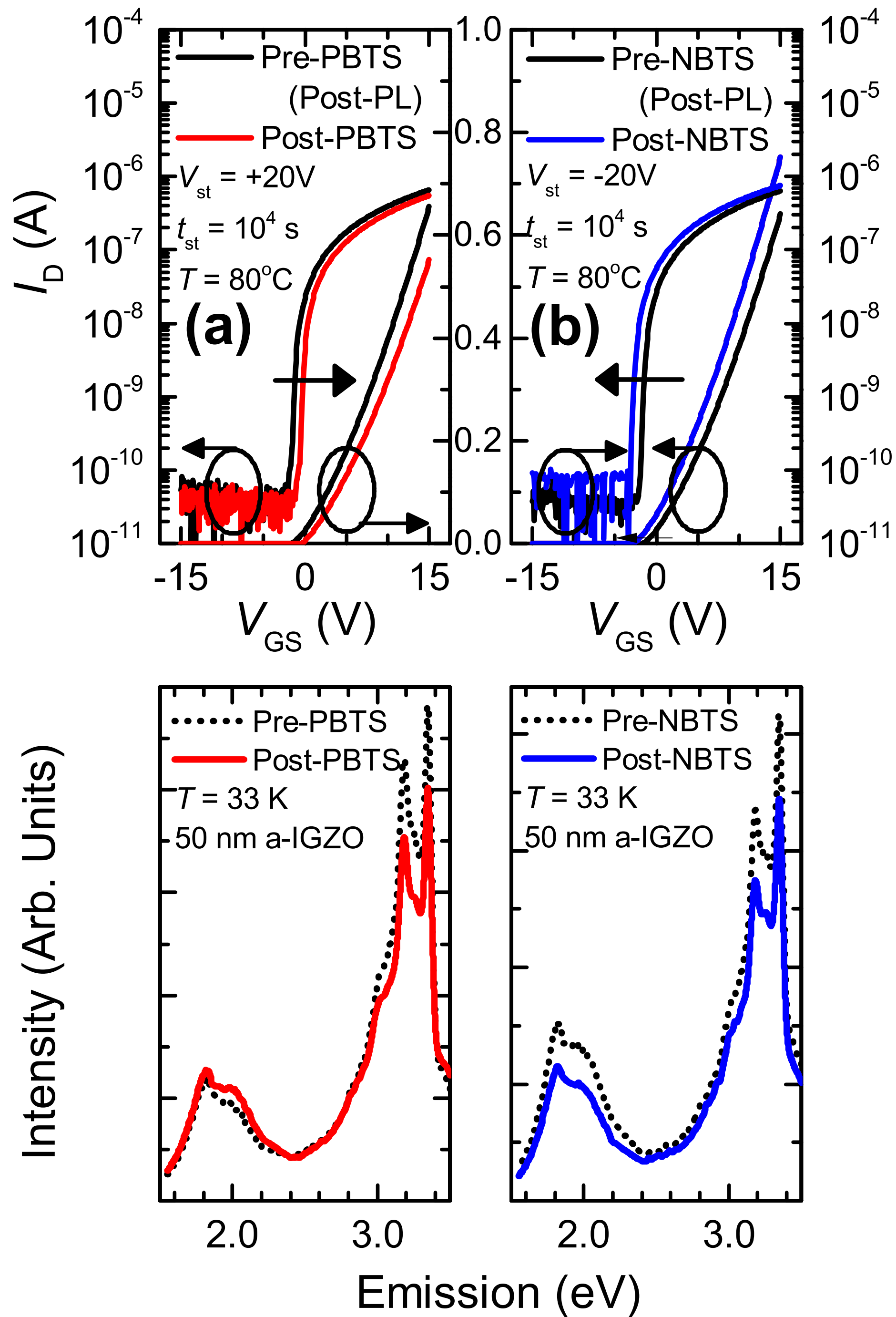


Figure 5.5 The I_D–V_{GS} of a-IGZO TFTs at V_{DS} = 0.1 V before and after (a) PBTS and (b) NBTS. The BTS applied are +20 V for PBTS and −20 V for NBTS, both at 80 °C with V_{DS} = 0 V for 10,000 s. The PL deep-level emissions are shown in (c) for PBTS and (d) for PBTS as figure insets. Directions of the arrows indicate the shift induced by the BTS.

exposure to the laser. The changes induced by PBTS and NBTS are consistent with results in the literature [37], [38], [89]. The changes to the PL spectra before and after BTS are shown in Figure 5.5(c) for PBTS and Figure 5.5(d) for NBTS. The active layer thickness of the a-IGZO TFT is 50 nm for all devices tested. We observe that the deep-level emission becomes stronger after PBTS and weaker after NBTS in comparison to the devices before BTS. These results have been reproduced several times.

5.4 Discussion of the Photoluminescence Spectra

For the purpose of analyzing our results in Figures 5.2 and 5.3, the a-IGZO DOS model we have adopted [97] is reproduced in Figure 5.6 for reference. It has very sharp acceptor-like conduction bandtail states and broad donor-like valence bandtail states. A broad Gaussian distribution of acceptor-like deep-gap states centered at 0.82±0.37 eV below E_C is assigned to weakly-bonded excess (non-stoichiometric) oxygen (O). Based on first-principle density functional theory calculations, V_O are fully-occupied deep donors located at 1.0 eV above E_V and are given in our model as a Gaussian distribution. There are four possible electron transitions that may be responsible for the observed PL emission: 1) band-to-band, 2) conduction bandtail states-to-hole trap (V_O), 3) electron trap (O)-to-valence bandtail states, 4) electron trap (O)-to-hole trap (V_O), and 5) conduction bandtail states-to-valence bandtail states. We assign the energy of the NBE emission, 3.35 eV, to the energy difference between an electron at E_C and a hole at E_V. It is similar to most published a-IGZO band gap (E_g) values in the literature [29], [30], [97], therefore we adopt E_g = 3.35 eV in this study. Since no significant differences are observed across all samples for the NBE emission, we will focus only on the deep-level PL emission located at 1.82 ± 0.39 eV. In the case of transition 2), a deep-level emission

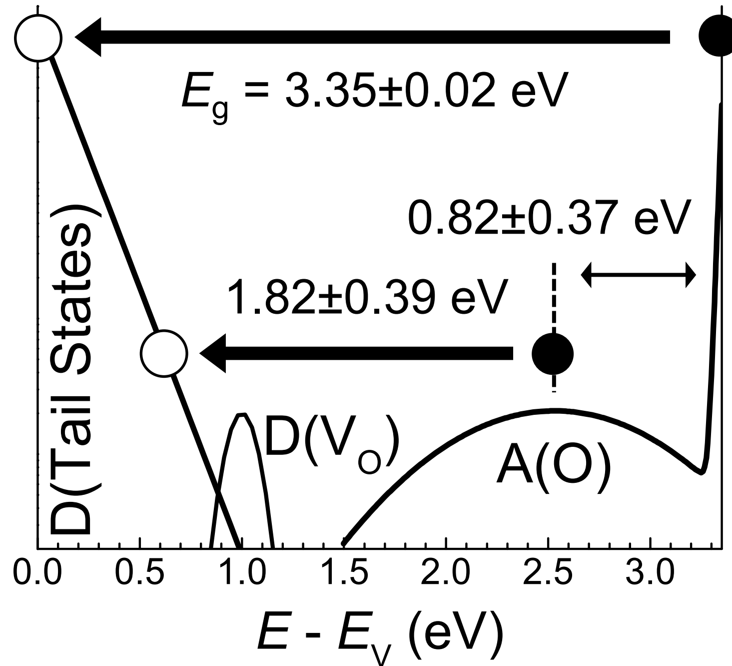


Figure 5.6 A diagram showing the a-IGZO density of states model we have adopted [97]. The thicker arrows show the two proposed radiative transitions in a-IGZO. In the figure, D indicates donor-like states and A indicates acceptor-like states.

of 1.82 eV and a very sharp conduction bandtail means that the fully-occupied deep donor V_O recombination center is located at $E_g - h\nu$ = 1.53 eV above E_V, which is too close to the midgap and does not match the energy position of 1.0 eV above E_V obtained from first-principles calculations. For transition 3), because the valence bandtail states are very broad, an electron captured by the excess-oxygen deep-gap states could radiatively recombine with a hole in the valence bandtail states, emitting photons at 1.82 eV. In the trap-to-trap transition 4), in order for there to be deep-level emission at 1.82 eV, holes captured by localized donors 1.0 eV above E_V would have to radiatively recombine with electrons captured by localized acceptors at E_g – 1.0 – 1.82 = 0.53 eV below E_C. Having excluded transition 2) as the radiative transition for the 1.82 eV photoemission, we examine transitions 3), 4), and 5) based on experimental results in various processing conditions.

After a-IGZO has been annealed in a high-O_2% atmosphere, the intensity of the deep-level emission significantly increased in comparison to the as-deposited thin film, as shown in Figure 5.3. We speculate that for the PL emission to become stronger, the concentration of the radiative excess oxygen recombination center O should increase. It is reasonable to consider that after annealing in a high-O_2% atmosphere or deposition in higher p_{O_2}, the density of atomic oxygen within a-IGZO becomes higher and that of V_O becomes lower. Using depth-dependent secondary-ion mass spectroscopy (SIMS), Nomura *et al*. reported evidence suggesting diffusion of atomic/weakly-bonded oxygen into a-IGZO after annealing in an oxidizing atmosphere at 200–400 °C [110]. For transition 3), which is from the oxygen-related acceptors to valence bandtail states, higher concentration of the O states leads to more transitions and stronger photoemission intensity. However, in 4), the transition is from O states to V_O states, so it is unlikely for the probability of this transition to become much greater if the former increases while the latter decreases. As for transition 5), the range of possible emission is between 3.35 eV (E_C-to-E_V) and 2.35 eV (E_C-to-V_O), and 1.82 eV is smaller than 2.35 eV. Thus the deep-level photoemission at 1.82 eV could only be described by transition 3) and not 2), 4), or 5). In low vacuum or N_2 gas flow, we expect that the oxygen species are not completely purged and still exist in relatively lower concentrations within the annealing chamber. The results after low-O_2% annealing are as we would expect: Because a smaller amount of oxygen is being added to the a-IGZO thin film, the intensity of the deep-level photoemission is weaker than that of the high-O_2% anneal but still stronger than as-deposited a-IGZO.

Figure 5.6 shows the PL spectrum of a-IGZO thin film (p_{O_2} = 5%, air-annealed)

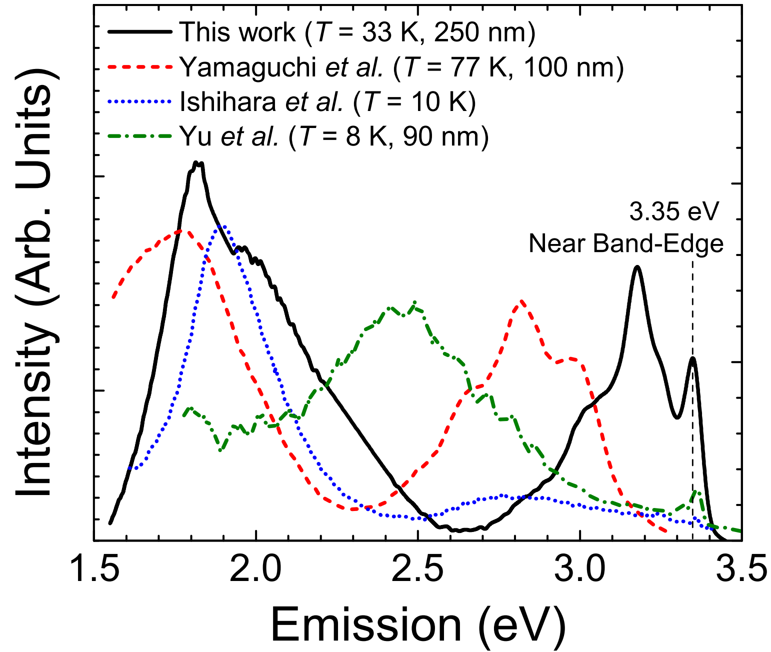


Figure 5.7 The photoluminescence emission spectrum of a-IGZO thin film measured in this study (solid black line) superimposed with data from the literature: Yamaguchi *et al*. (dashed red line) [76], Ishihara *et al*. (dotted blue line) [78], and Yu *et al*. (dash-dotted green line) [97].

measured for this work superimposed on top of a-IGZO PL data available in the literature. Our NBE emission is identical to the one reported in Yu *et al*. [97] and Tiwari *et al* [109], while an NBE emission is not observed in many published reports [78], [107], [108]. It appears that observation of the NBE emission would depend on the measurement setup and/or a-IGZO layer preparation and processing conditions. The observed strong deep-level emission at 1.82 eV is very similar to what was also observed in Yamaguchi *et al*. [76] and Ishihara *et al* [78]. Although this energy of deep-level emission appears to be different from the 2.44 eV photoemission that was observed in Yu *et al*. [97], based on our analysis above we may consider them both as originating from the excess oxygen acceptor-like states. The transition in our previous work is directly

from O to E_V, whereas the photoemission observed in the present work involves electrons recombining with holes in the valence bandtail states.

In Figure 5.5, we observe that after PBTS, more positive V_{th} is accompanied by stronger PL emission intensity at 1.82 eV and vice versa. In the above discussion, we have already established that increased deep-level photoemission is attributed to an increase of acceptor-like excess oxygen states. While V_O are deep occupied donors and have no impact on TFT operation [31], [69], weakly-bonded excess oxygen in the form of O^0/O^{1-} can trap an electron to form the negatively-charged O^{1-}/O^{2-} and cause a positive shift in V_{th}. Experimental results from high-resolution transmission electron microscopy and energy-dispersive X-ray spectroscopy showed that after PBTS, the oxygen concentration within the a-IGZO TFT channel increased in addition to compositional changes of the individual In, Ga, and Zn elements [111]. We speculate that during PBTS, the diffusion of the oxygen adsorbed at the exposed TFT back channel is influenced by electric field and stress temperature, resulting in a modified thin-film composition and higher density of excess oxygen in a-IGZO. In addition to stronger deep-level PL emission, a higher concentration of excess oxygen corresponds to more positive threshold voltage and lower μ_{FE}, which is consistent with the previously published results from our group [89]. It is possible that the exact opposite is happening after NBTS, causing lower deep-level PL emission and more negative threshold voltage.

CHAPTER 6

AC Bias-Temperature Stability of a-IGZO TFTs with Metal Source/Drain Recessed Electrodes

6.1 Introduction

For the ac bias-temperature stress (BTS) of a-IGZO TFTs, only a small number of studies have been published. Existing literature is limited in the scope of stress conditions and the BTS studies are often performed on devices with poor electrical properties and/or reliability. Fung *et al.* investigated the pulse width (*PW*) dependence of threshold voltage shift (ΔV_{th}) in a-IGZO TFTs with an inverted-staggered bottom-gate structure [112]. They reported a strong *PW* dependence for positive unipolar ac BTS, with larger ΔV_{th} for longer *PW*s up to 100 ms. Negative unipolar ac BTS exhibited very small ΔV_{th} and no obvious trend regarding *PW* was observed. Work by Ohta *et al.* showed that after 100 hours of stressing, ac BTS-induced ΔV_{th} for a-IGZO TFT is about half that of a-Si:H TFT [35]. In terms of stress conditions, the effect of different duty cycles [113] and pulse rise-times [114] have also been studied for different device structures. However, these devices showed $|\Delta V_{th}| > 5$ V after less than 10^4 s of stressing, suggesting that the observed ΔV_{th} may be the result of other fabrication deficiencies and not truly characteristic of a-IGZO. A "swing-back" of the ΔV_{th} towards its initial state (i.e., recovery) or the opposite polarity

has been observed for both positive unipolar [115] and bipolar ac BTS [116] but not negative unipolar pulses. Furthermore, existing data on the *PW* dependence of the positive unipolar ac BTS are inconsistent for different structures/processes, where some showed increased instability for dc and longer *PW*s (more dc-like) [112], [115] while others are the opposite (greater ΔV_{th} for shorter *PW*s, positive steady-state is the smallest) [114], [117]. Finally, ac BTS produces observable change in the TFT capacitance–voltage measurement after stressing [116], similar to dc BTS [34].

Our objective in this study is to fabricate highly reliable bottom-gate a-IGZO TFTs with reduced gate-to-source/drain capacitance (C_{GS}) and evaluate their electrical stability under ac BTS. In order for this work to be more applicable to ultra-high definition (UHD) active-matrix liquid crystal displays (AM-LCDs), we have fabricated the source/drain (S/D)-recessed a-IGZO TFTs by photolithography. We present a comprehensive set of data on ac electrical stability using a broad set of stress conditions: polarity, frame time (1/frequency), and duty cycle. Our devices are all very stable under ac BTS and the $|\Delta V_{th}|$ for all stress conditions are within 0.35 V or less after 10^4 s of stressing at temperature of T_{st} = 70 °C in ambient air.

6.2 Experimental

6.2.1 Fabrication of Source/Drain-Recessed a-IGZO TFTs

The fabrication process flow of the S/D-recessed a-IGZO TFTs is described in section 2.6 and will be briefly summarized in this section. The molybdenum gate electrode (100 nm) is first deposited on the glass substrate by sputtering, then patterned and defined by dry etching using CF_4/O_2 plasma. The gate insulator is a layer of amorphous silicon oxide

($a\text{-}SiO_X$) (200 nm) deposited with plasma-enhanced chemical vapor deposition (PECVD) at 340 °C. The a-IGZO active layer (40 nm) is dc-sputtered and defined (islands) using dilute hydrochloric acid. The $a\text{-}SiO_X$ channel protection layer (CPL) (300 nm) is deposited by PECVD at 285 °C and dry etched to define device geometry. After CPL definition, the substrate is treated in a rapid thermal anneal (RTA) oven at 290 °C for one hour. The amorphous silicon oxynitride ($a\text{-}SiON_X$) passivation layer (300 nm) is then deposited by PECVD at 250 °C, during which the hydrogen in the PECVD process chamber and/or the hydrogen-rich $a\text{-}SiON_X$ layer dopes the a-IGZO regions not covered by the CPL. This process greatly reduces the resistivity of a-IGZO [67], thus creating nearly self-aligned H-doped S/D contact regions. The a-IGZO area defined by the CPL width (W) and length (L) are considered the device dimensions, and in this report the TFTs studied have W/L = 60/10 μm. The S/D contact via is opened in the passivation layer by dry etching. Molybdenum S/D electrodes (100 nm) are then sputtered and wet-etched using a dilute phosphoric and nitric acid mixture. In this TFT configuration, the Mo S/D electrode edges are recessed with respect to the Mo gate electrode edges. There is a separation/underlap (UL) of about 20 μm between the CPL and the S/D via. Such device structure is expected to produce significantly lower C_{GS} in comparison to other TFT structures described in literature. After processing, the TFTs undergo one more anneal at 270 °C in ambient atmosphere for one hour. The top-view diagram, cross-section diagram, and top-view micrograph of the complete device are shown in Figure 6.1.

It should be indicated that if back exposure is used in combination with the gate electrode as mask, the top CPL can be fully self-aligned to the gate dimensions. In

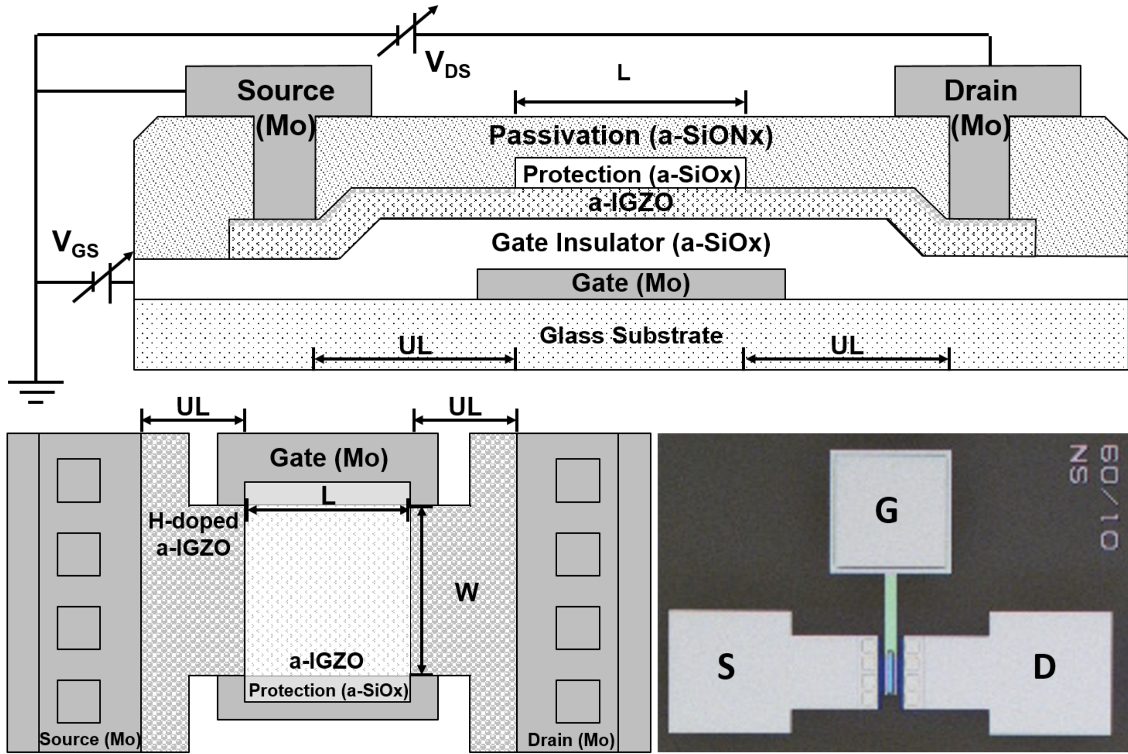


Figure 6.1 (Top) Cross-section and (Lower left) top-view diagram of the a-IGZO TFT used throughout this study. (Lower right) Top-view micrograph of the fabricated device.

addition, the CPL is used as mask for H-doping, hence creating the nearly self-aligned H-doped source/drain regions. Such a device structure is expected to have a reduced overlap between the S/D regions and gate electrode; as shown in Figure 6.1 the S/D metal electrodes do not overlap at all with the gate metal electrode (reversed TFT structure). In this TFT structure we still maintain a small overlap between H-doped a-IGZO regions and gate electrode. We expect that this overlap will not affect C_{GS}. Both these effects will be responsible for significant reduction of C_{GS} in comparison to other TFT structures used in previous BTS investigations. Therefore this BTS study is novel and significant because it can be applied to future high-resolution flat panel displays.

6.2.2 Characterization of TFT Electrical Properties and AC BTS Stability

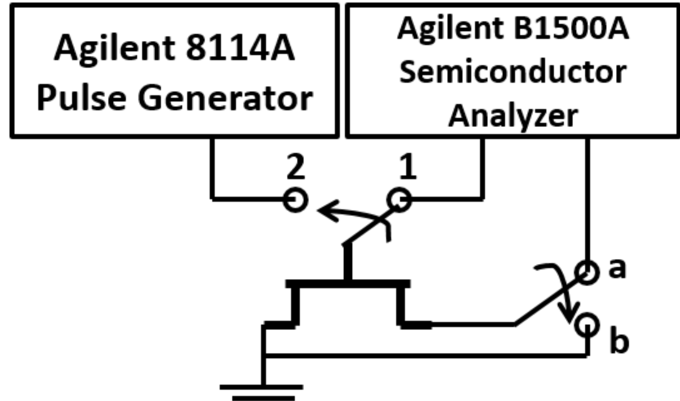


Figure 6.2 Diagram showing the experimental setup switching between stressing (switch positions 1,a) and characterization (switch positions 2,b) steps by the E5250A switching matrix.

Throughout this study, device measurement and stressing are done at T_{st} = 70 °C on a heated chuck in the dark. The illumination effect is not addressed in this study. The a-IGZO TFT transfer characteristics (I_D–V_{GS}) in the linear (V_{DS} = 0.1 V) and saturation (V_{DS} = 15 V) regions between V_{GS} = −10 V to 10 V are measured at 0.1 V steps using an Agilent B1500A semiconductor analyzer. The TFT source electrode is always grounded during device measurement.

The B1500A and a HP 8114A pulse generator are connected to a HP E5250A switching matrix. An Agilent EasyExpert software routine is responsible for switching the E5250A between the 8114A for ac stressing and the B1500A for device measurement and dc stressing, as shown in Figure 6.2. During stressing, the source and drain electrodes are tied together and grounded (V_{DS} = 0 V) to ensure a uniform distribution of the electric field across the channel. The device stressing is interrupted at pre-determined time intervals to measure the TFT transfer characteristics at T_{st} = 70 °C. This repeats until total accumulated stress time reaches 10^4 s. Total accumulated stress time is defined as the amount of time a non-zero gate bias (positive or negative) is applied to the gate. A different TFT on the same wafer is used for each stress condition.

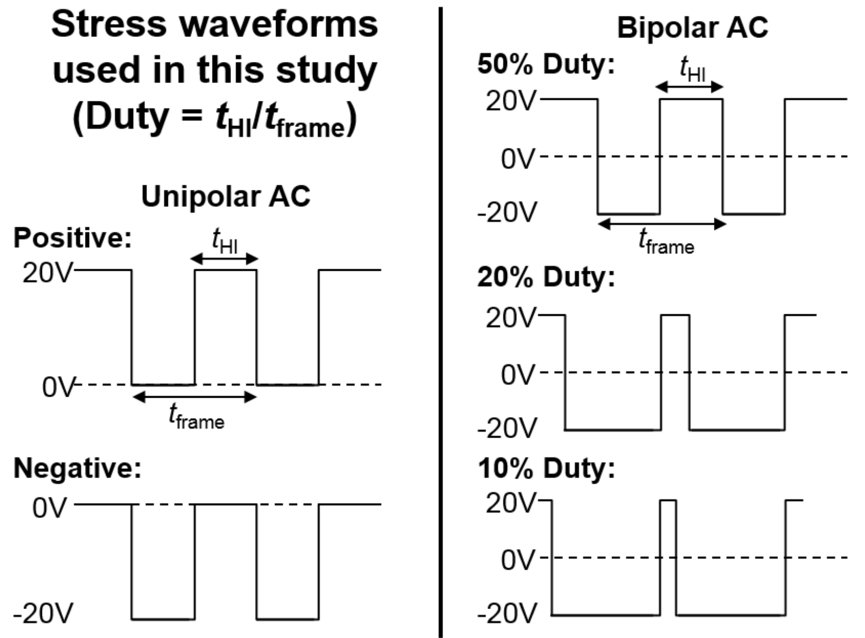


Figure 6.3 The different gate bias stress waveforms used in this study. The left half shows unipolar positive and negative pulses. The right half shows bipolar pulses of different duty cycles.

For ac gate stress, the three types of waveforms used in this study are shown in Figure 6.3: positive unipolar ($V_{G\text{-}Stress}$ = 0 to +20 V), negative unipolar (0 to −20 V), and bipolar (−20 V to +20 V). The duty cycle of a stress waveform is defined as the ratio of positive pulse width to frame time (t_{HI}/t_{frame}), and frame time is the inverse of frequency. For unipolar ac waveforms, the duty cycle is fixed at 50%, so t_{HI} is always one half the frame time. For bipolar ac waveforms, the duty cycle is varied from 10% to 50%. In the case of unipolar ac stressing, because the gate bias is 0 V for half the frame time, the stress waveform needs to be applied for twice the duration (i.e. 2×10^4 s) to achieve the same accumulated stress time (10^4 s) as dc or bipolar ac stressing.

6.3 Results and Discussion

6.3.1 Electrical Properties of Source/Drain Recessed a-IGZO TFTs

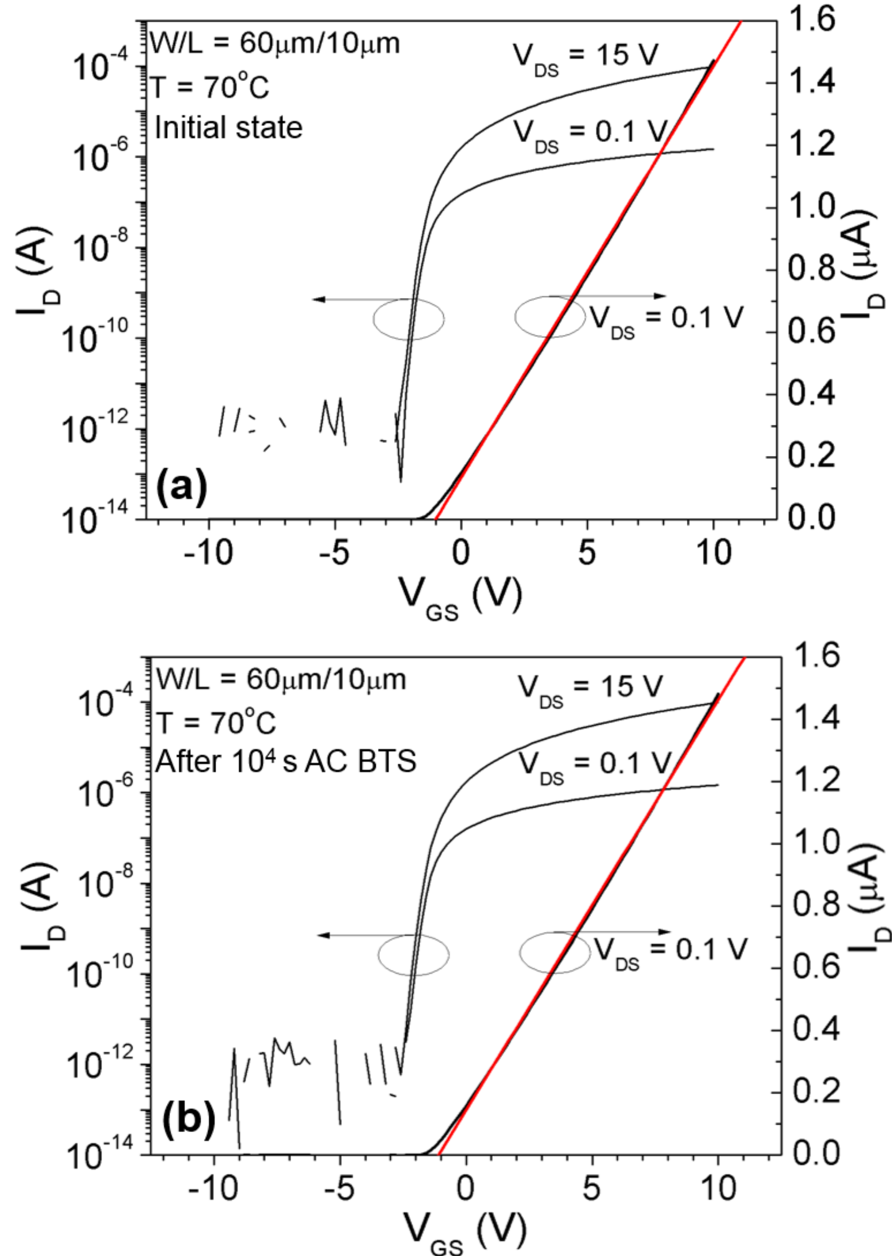


Figure 6.4 The transfer characteristics in the linear region (V_{DS} = 0.1 V) and saturation region (V_{DS} = 15 V) of (a) the a-IGZO TFT used in this study and (b) the same TFT after receiving 10^4 s of ac BTS. The red line indicates the linear fit of the device I_D at the 20% and 80% points.

μ_{EF} (cm^2/V·s)	V_{th} (V)	*SS* (mV/dec)	I_{OFF} (A)
10.9	-1.03	220	$<10^{-12}$

Table 6.1 Extracted parameters of the a-IGZO TFT in the linear region (V_{DS} = 0.1 V).

The device transfer characteristics before stress are shown in Figure 6.4(a). The TFT field-effect mobility in the linear region is extracted by fitting the linear region transfer curve in Figure 6.4(a) [26]. The threshold voltage is extracted by extrapolating the x-intercept of the fit. The TFT used in this study has the parameters μ_{FE} = 10.9 $cm^2/V\cdot s$, V_{th} = −1.03 V. We also extracted the subthreshold swing (SS) of the TFT, for which the $\partial \log I_D / \partial V_{GS}$ is taken as the average of three values nearest the maximum slope point in the subthreshold region of the transfer curve. The SS of TFT studied is calculated to be 220 mV/decade. From the device transfer characteristics we observe that I_{off} is on the order of 10^{-14} A at room temperature (not shown). The drain current is independent of the gate and drain voltage in the off-region. The off-current increases to the order of 10^{-12} A when measured at 70 °C, and it should be noted that this is a result of increased thermal noise in the measurement setup at an elevated temperature. Table 6.1 summarizes the extracted device parameters of the a-IGZO TFT at 70 °C. An example of the TFT transfer characteristics after undergoing ac BTS is shown in Figure 6.4(b) and appears almost identical to that of the unstressed device. In fact, none of the stressed TFTs show visible changes in μ_{FE}, SS, or I_{off} under any of the ac BTS stress schemes applied throughout this study, with the only noticeable degradation being ΔV_{th}.

6.3.2 Unipolar AC Bias-Temperature Stress Stability of a-IGZO TFTs

For the hydrogenated amorphous silicon (a-Si:H) TFT, it has been shown in a side-by-side comparison that a combination of positive and negative dc BTS cannot accurately predict ac BTS stability. In this study, we apply a similar methodology [22] to the a-IGZO TFT. The threshold voltage instability ΔV_{th} for a particular stress time t_{st} is defined as $\Delta V_{th}(t = t_{st}) = V_{th}(t = t_{st}) - V_{th}(t = 0)$. In Figure 6.5, ΔV_{th} over

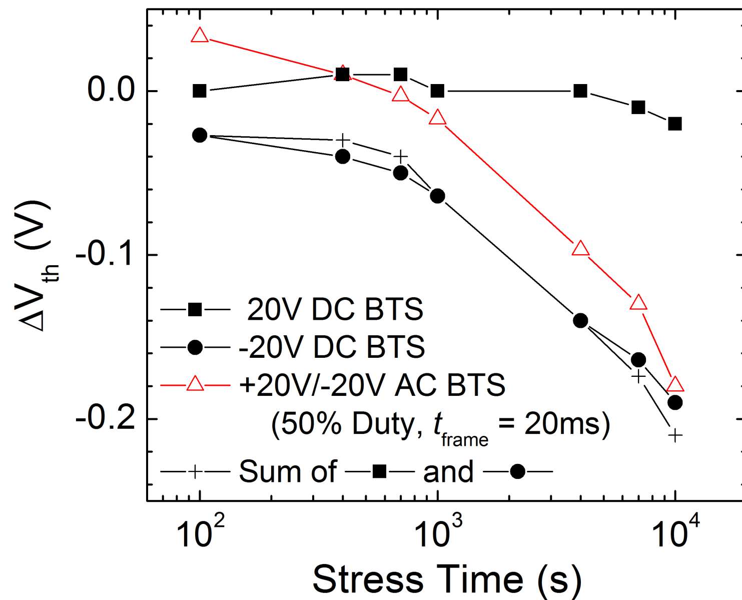


Figure 6.5 Side-by-side comparison of bipolar ac BTS (open triangles) and the sum (crosshairs) of positive (solid squares) and negative (solid circles) dc BTS. Stressing and measurements are done at T_{st} = 70 °C in ambient air in the dark.

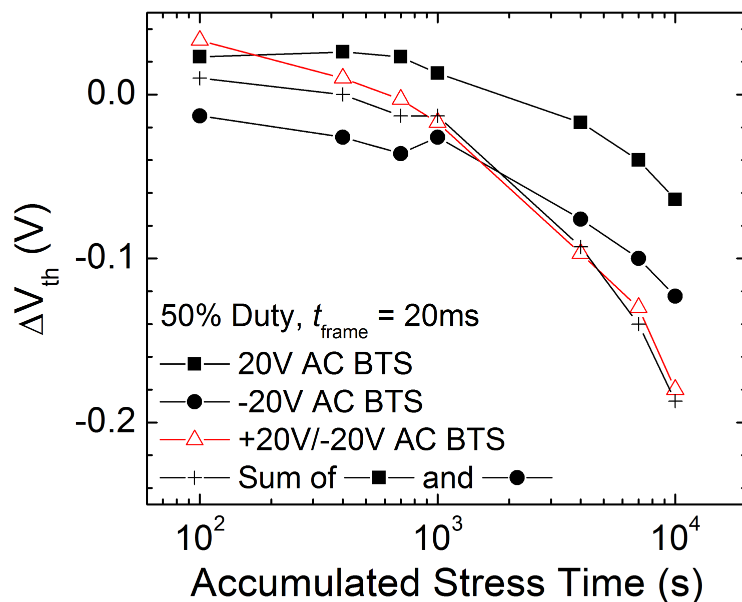


Figure 6.6 Side-by-side comparison of bipolar ac BTS (open triangles) and the sum (crosshairs) of positive (solid squares) and negative (solid circles) unipolar ac BTS. Stressing and measurements are done at T_{st} = 70 °C in ambient air in the dark.

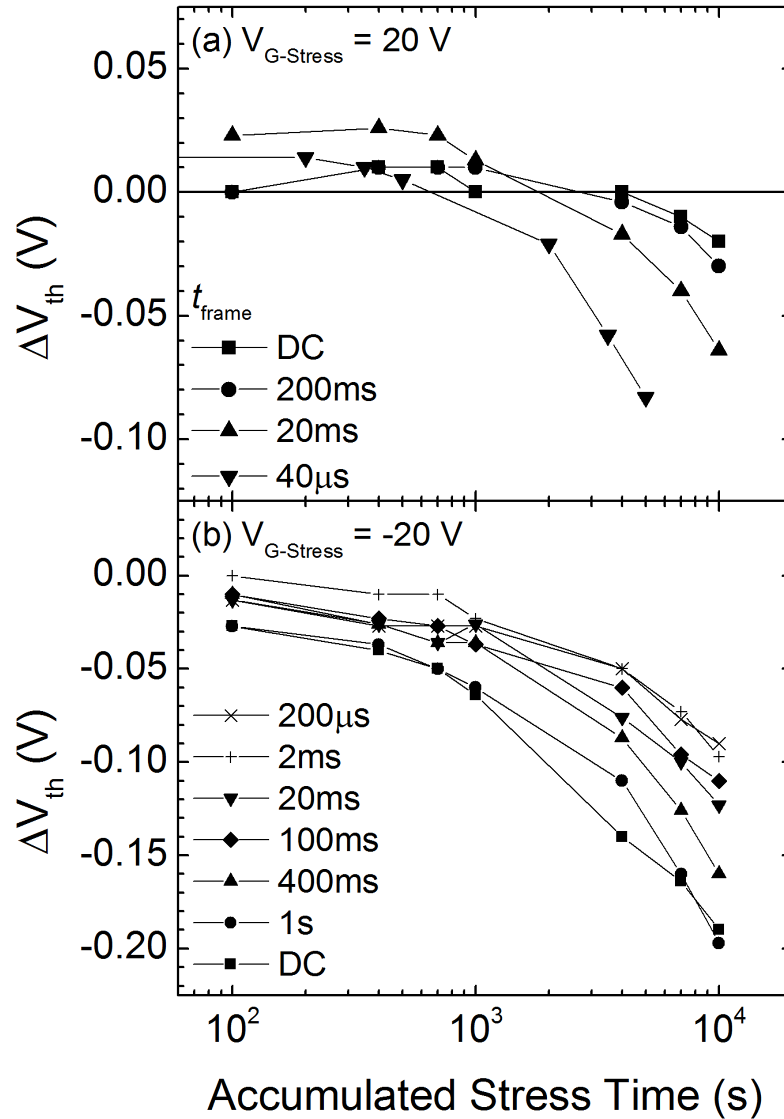


Figure 6.7 Frame-time dependence of the a-IGZO TFT threshold voltage instability under (a) positive unipolar ac BTS (b) negative unipolar ac BTS. Stressing and measurements are done at T_{st} = 70 °C in ambient air in the dark.

accumulated stress time for the positive and negative dc BTS, their sum, and bipolar ac BTS (*PW* = 10 ms) are shown superimposed in the same figure. It is clear that the sum of steady-state behavior significantly overestimates the ac BTS instability of a-IGZO TFTs. In Figure 6.6, we compare the sum of positive and negative unipolar ac BTS with bipolar ac BTS of equal frame time and stress voltage magnitude. We consider the positive and negative unipolar ac waveforms as two halves from which the bipolar waveform can be

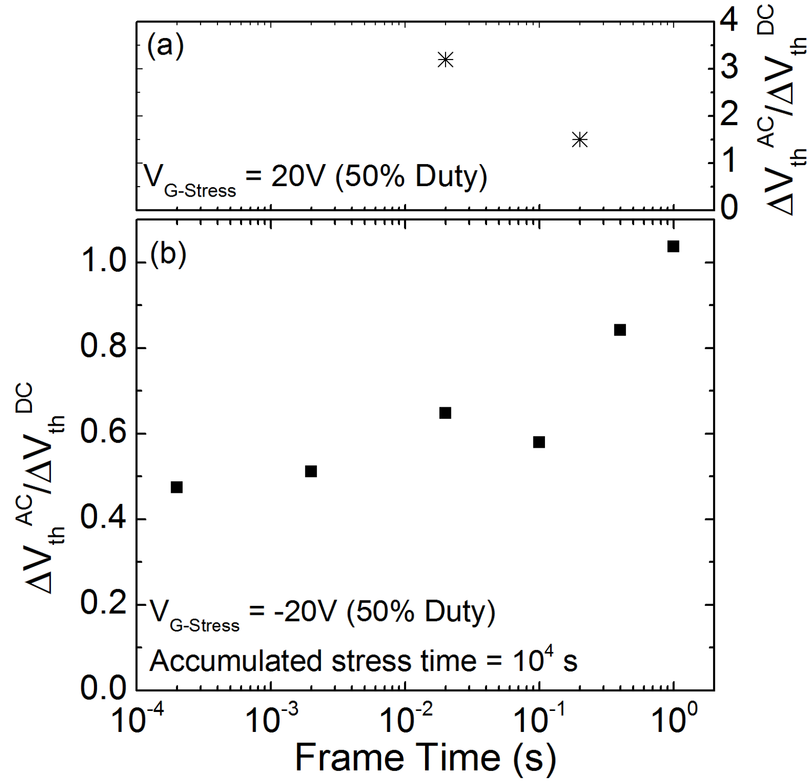


Figure 6.8 The ac BTS-induced threshold voltage shift as a function of ac stress frame times, normalized to the (a) positive or (b) negative dc BTS shift. Stressing and measurements are done at T_{st} = 70 °C in ambient air in the dark.

constructed from. This relationship is described by the equation $\Delta V_{th}^{\pm} = \Delta V_{th}^{+} + \Delta V_{th}^{-}$. In the figure, we see that the curve of the sum very closely follows that of the bipolar ac BTS instability. From this, we can conclude that in order to model or predict the lifetime of AM-LCD with a-IGZO TFT backplane technology, ac BTS evaluation is required.

In Figure 6.7, we investigate the effect of frame-time dependence for both (a) positive (+20 V) and (b) negative (−20 V) unipolar ac BTS instability as a function of accumulated stress time. For positive unipolar pulses, the ΔV_{th} of the devices are all negative and very insignificant (within −0.1 V), therefore no clear conclusions can be drawn regarding the frame-time dependence for positive unipolar ac stressing. However, upon closer examination, we find that the ΔV_{th} values actually are positive within the first

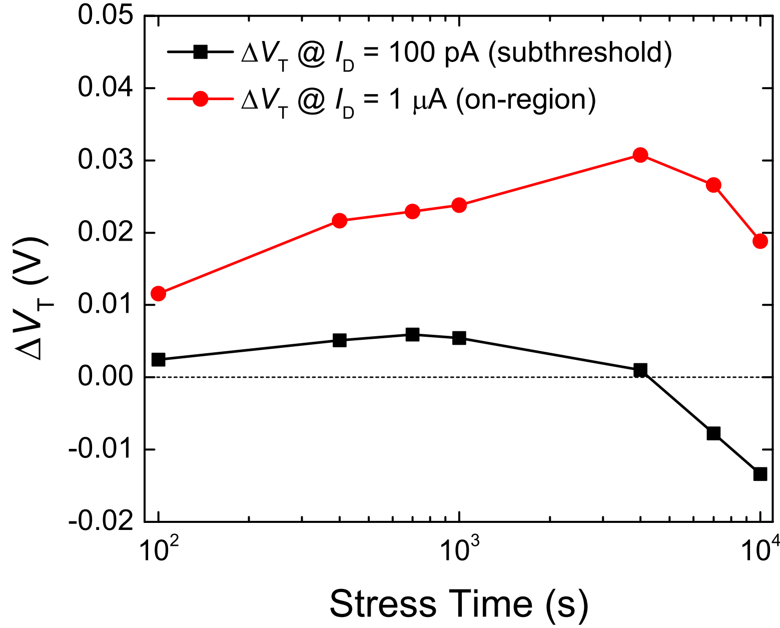


Figure 6.9 The dc BTS-induced ($V_{G\text{-Stress}}$ = +20 V) threshold voltage shift extracted by the constant current method (ΔV_T) at I_D = 100 pA for subtreshold region (solid red circles) and I_D = 1 μA for on-region (solid black squares).

1000 s of BTS, beyond which they trend negative until the end of the duration tested. For negative gate biases, the ΔV_{th} are all invariably negative and the magnitudes increase with accumulated stress time. In this case, the frame time dependence is much more obvious and larger t_{frame} cause greater ΔV_{th} instability. Regarding the strong dependence of negative unipolar ac BTS ΔV_{th} on frame time, we can consider the dc case to be the upper limit and calculate the $\Delta V_{th}^{ac}/\Delta V_{th}^{ac}$ as a function of frame time, which is shown in Figure 6.8.

In our results, the observation that V_{th} becomes more negative (ΔV_{th} < 0 V) for positive dc and positive unipolar ac BTS is very curious and deserves further discussion. This effect is contradictory to most published reports in the literature, in which ΔV_{th} > 0 V after positive gate bias stress is applied. However, in Fung *et al.*, it was observed that after application of constant positive gate bias stress, the instability in the on-region

behaves differently from that in the subthreshold region [38]. In particular, they noted that after prolonged stress of 10^4 s has been applied, positive shift is observed in the on region while the subthreshold region became more negative. Although they were unable to offer an explanation for this behavior, they suggested that a secondary time-dependent effect possibly related to a-IGZO film resistivity could work to counteract the usual a-IGZO/a-SiO_X interface trapping mechanism. In Figure 6.9, we show the positive dc ($V_{G\text{-Stress}}$ = +20 V) BTS-induced threshold voltage shifts extracted by constant current method at I_D = 100 pA (subthreshold region) and 1 μA (on region). In the constant current method, the threshold voltage shift (ΔV_T) is calculated by the difference in the V_{GS} that is required to reach a certain I_D before and after stressing. From the figure, we note that before t_{st} = 7000 s, $\Delta V_T > 0$ V in both the on- and the subthreshold regions. After 7000 and 10^4 s, ΔVT trended negative in both regions, although this appears to be stronger in the subthreshold region.

6.3.3 Bipolar AC Bias-Temperature Stress Stability of a-IGZO TFTs

One notable advantage of the a-IGZO TFT is that its superior electron mobility compared to a-Si:H TFT will enable next-generation ultra-high refresh rate displays (240–480 Hz) [118]. In Figure 6.10, we evaluate the ac BTS stability of a-IGZO TFTs with bipolar waveforms mimicking AM-FPD pixel addressing under higher frame rates. The duty cycles of the waveforms are fixed at 50%, which for bipolar pulses mean that higher frequency is equivalent to shorter frame time. From the figure, we see that for t_{st} = 1000 s (solid triangle symbols), frequencies 360 Hz and below cause almost no ΔV_{th} while it becomes slightly more noticeable at 500 Hz. After $t_{st} = 10^4$ s, this effect is magnified such that the ΔV_{th} induced by the 500 Hz waveform is almost 150% that of the ΔV_{th} induced by

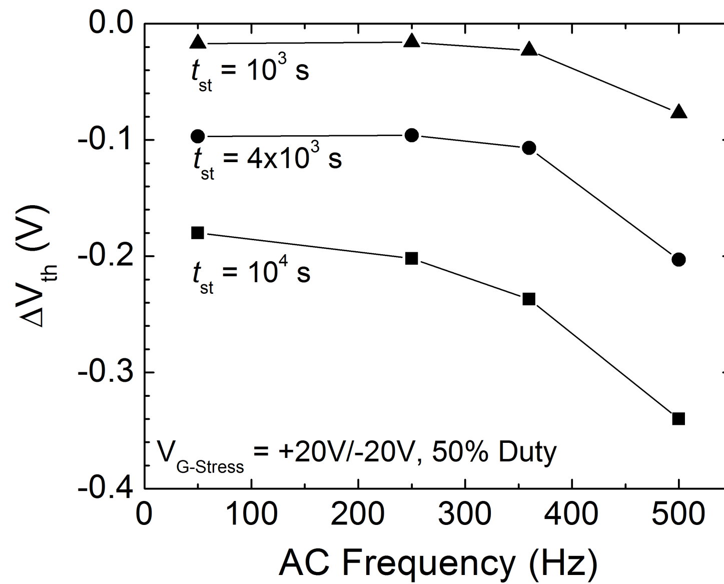


Figure 6.10 The ac BTS-induced threshold voltage shift as a function of applied bipolar stress frequency ($1/t_{frame}$). The duty cycle is kept at 50% for all frequencies. Stressing and measurements are done at T_{st} = 70 °C in ambient air in the dark.

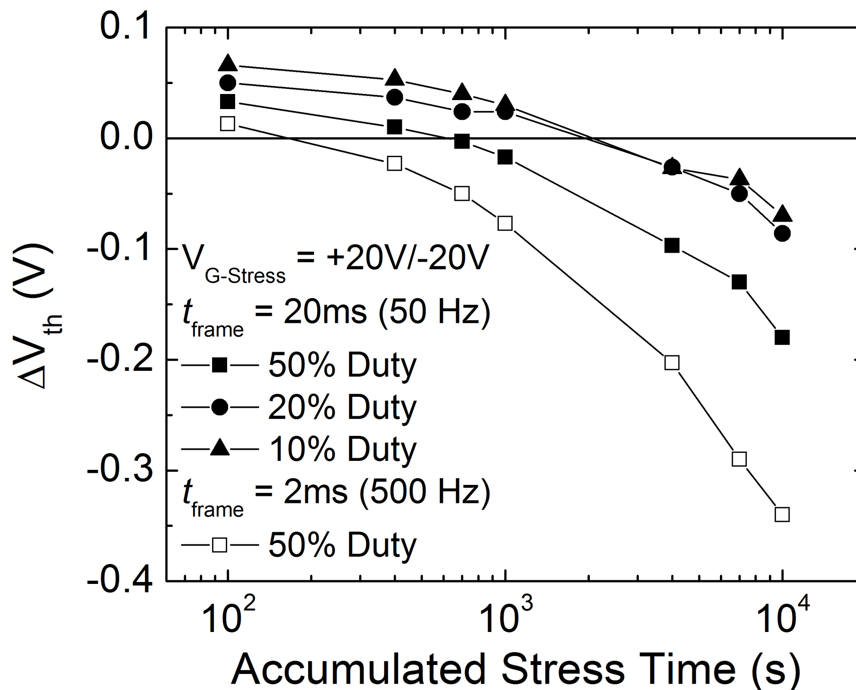


Figure 6.11 The ac BTS-induced threshold voltage shift as a function of accumulated stress time for different bipolar stress duty cycles (10, 20, and 50%) at t_{frame} = 20 ms (50 Hz). The ΔV_{th} induced by ac stress with t_{frame} = 2 ms (500 Hz) is reproduced here for reference. Stressing and measurements are done at T_{st} = 70 °C in ambient air in the dark.

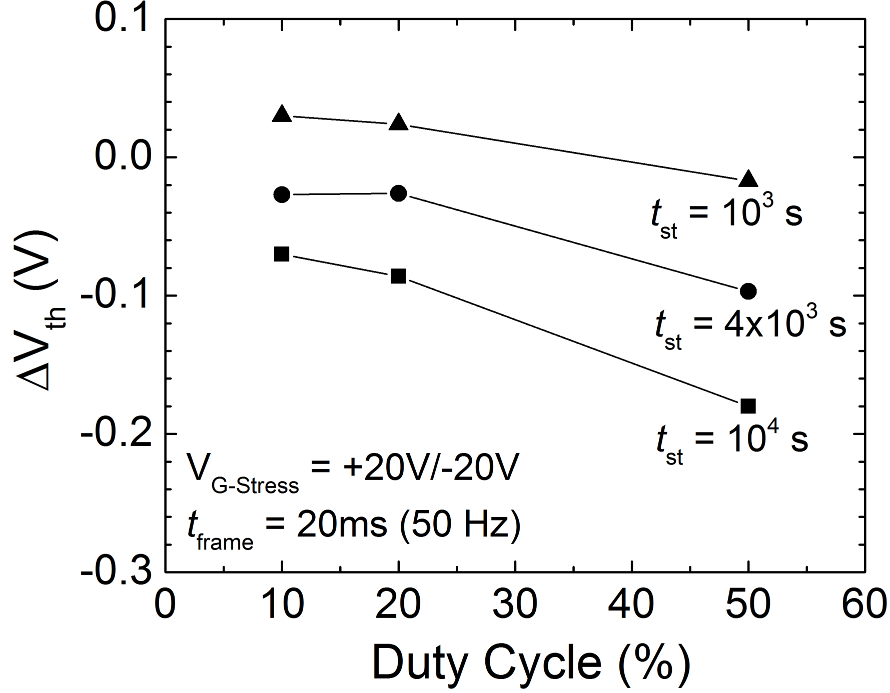


Figure 6.12 The ac BTS-induced threshold voltage shift as a function of duty cycle at t_{frame} = 20 ms (50 Hz) for different accumulated stress times. Stressing and measurements are done at T_{st} = 70 °C in ambient air in the dark.

the 360 Hz waveform. We observe higher ΔV_{th} with higher operation frequency, up to −0.35V for 500 Hz. This should be taken into consideration when using a-IGZO TFTs for ultra-high refresh rate AM-LCDs.

We then investigate for the bipolar ac BTS the effect of varying the duty cycle of the stress waveforms. Referring to Figure 6.3, we fix the frame time t_{frame} at 20 ms (50 Hz), while applying gate stress pulses with duty cycle values of 10%, 20%, and 50%. These duty cycle values would represent positive gate bias of +20 V being applied for 2 ms, 4 ms, and 10 ms within each frame, respectively, while −20 V is applied for the rest of the frame. In Figure 6.11, we see that when compared to 50% duty cycle, ΔV_{th} trends smaller for lower duty cycle values. This is better illustrated in Figure 6.12, where we plot ΔV_{th} with respect to duty cycle for three different t_{st} values. We that see for all t_{st}, ΔV_{th} is

always smaller for lower duty cycle, and this effect is even more pronounced for longer t_{st}. Considering that higher-frequency operation causes more instability in a-IGZO TFTs, adjusting the duty cycle and reducing the time portion of the positive bias segments (t_{HI}) may help reduce ΔV_{th} significantly. However, doing so may have an impact on the a-IGZO TFT pixel circuit design. In the dynamic response of an a-IGZO one-capacitor-one-transistor test circuit, it is desirable to minimize the feedthrough voltage (ΔV_P), which can be achieved by increasing the storage capacitance (C_{st}) [64] or reducing C_{GS} value. It has been shown that larger C_{st} also causes the charging time (t_{ch}) to increase, for which we are limited by the duty cycle and t_{HI} of the transistor driving the waveform. This is expected to become an important factor to consider in the design of a-IGZO TFT pixel circuits for 8K×4K and long lifetime AM-LCDs.

6.4 AC BTS Stability of a-IGZO TFTs for 4K UHD AM-LCD

Considering that the focus of this dissertation is a-IGZO TFTs as the backplane technology for UHD AM-LCDs, we are motivated to study the V_{th} instability when voltage waveforms corresponding to 4K UHD specifications are applied to the TFT gate and drain terminals. In Figure 6.13, the impact of V_{DS} data voltage is investigated with respect to stress time. In this figure, the gate voltage pulse is between −5 and +15 V at 120 Hz while constant V_{DS} is applied at 70 °C. The duty cycle of the gate pulse is 0.046%, which corresponds to the selection of 1 out of 2160 rows (1/2160 = 0.00046) in 4K UHD specifications. We observe that V_{th} becomes more negative with stress time as V_{DS} increases. This can be explained by generation of electron-hole pairs or positively charged species at the drain side by impact ionization that is accelerated by high drain-to-source lateral electrical field and elevated temperature. The existence of increasing self-

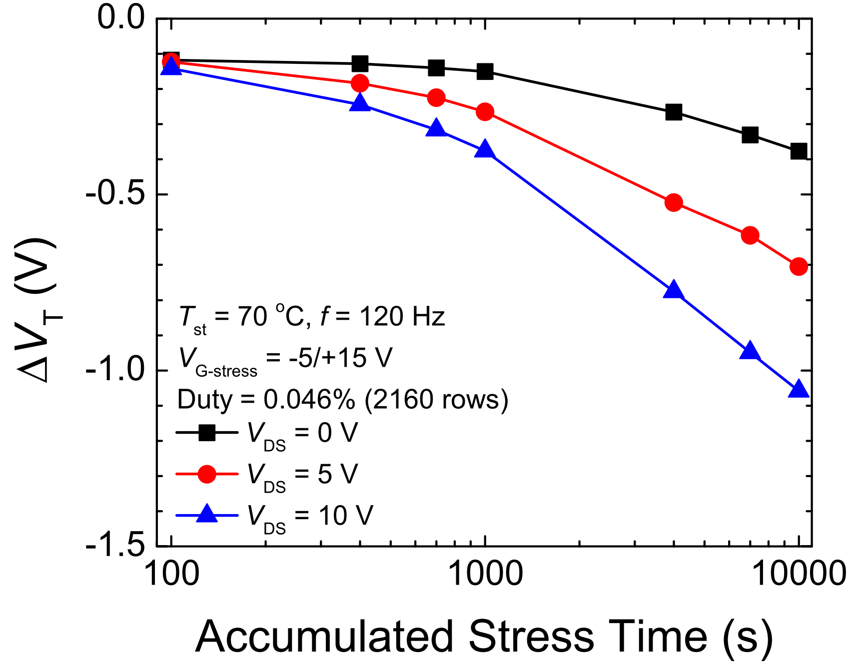


Figure 6.13 The threshold voltage shift (ΔV_T) extracted by the constant current method for a-IGZO TFT subject to various constant V_{DS} bias while voltage pulses are applied to the gate terminal. In this figure, stress temperature 70 °C and the frequency of the gate pulses is 120 Hz. Duty cycle of 0.046% represents 2160 rows of 4K UHD specification.

heating in the channel with the stress time and drain bias stress caused by the drain current have already been established by the thermal analysis [119]–[121]. Oxygen vacancies (V_o^{2+}) are possible candidates of the positively charged species [122], [123]. The generated electrons are swept into the drain electrode by the positive drain voltage, but holes are attracted and then trapped near the channel/gate dielectric interface by the pulsed gate bias, which is at −5 V for most of the frame time ($t_{LO} \approx t_{frame} = 8.33$ ms) except for a very short positive pulse of $t_{HI} = 3.9$ µs. In addition, we note that the impact on TFT *SS* is almost negligible. After stressing, the initial TFT electrical properties can be recovered by storing the devices in room temperature and atmosphere for at least one week.

Over a fixed amount of time, the number of TFT switch-on for one row can be defined as N_{on} = frequency (f) × t_{st}. By varying f while keeping t_{st} identical, we examine

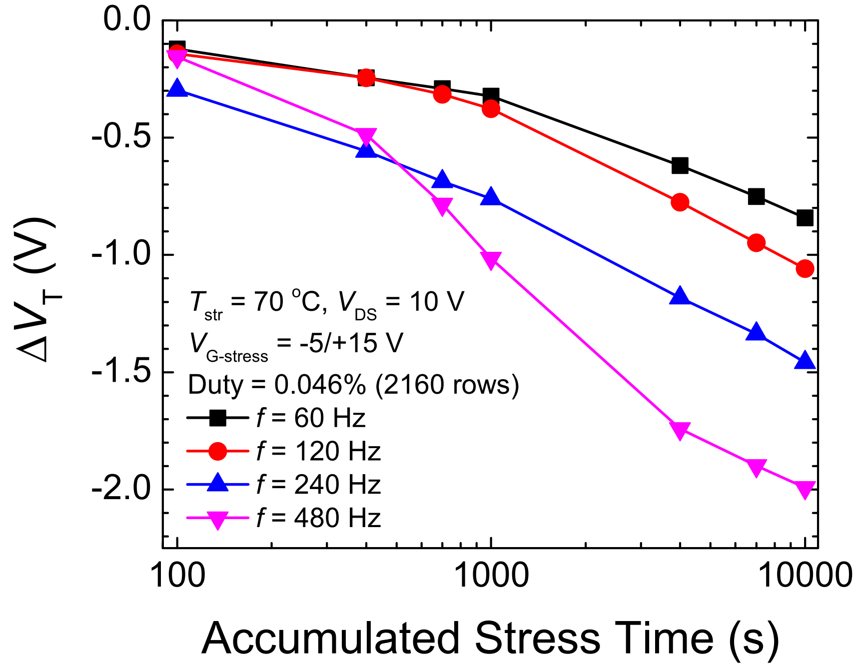


Figure 6.14 The threshold voltage shift (ΔV_T) extracted by the constant current method for a-IGZO TFT subject to constant V_{DS} = 10 V while voltage pulses are applied to the gate terminal. In this figure, stress temperature 70 °C and the frequency of the gate pulses is varied. Duty cycle of 0.046% represents the 2160 rows in 4K UHD specifications.

the influence of N_{on} on ΔV_{th} in Figure 6.14. In this figure, gate stress voltage is between −5 V and +15 V, V_{DS} = 10 V, duty cycle = 0.046%, and T = 70 °C are used for the ac BTS. Since high frame-rate operation, such as 480 Hz, has very short switch-on time (0.96 μs), it is important to verify whether V_{DS} can induce impact ionization in such a short time. If the switch-on time is extended at the same refresh rate, the influence of positive gate bias during the pulsed gate stress cannot be ignored in attracting the electrons generated by the impact ionization. As the frequency increases from 60 Hz to 480 Hz, the switch-on time per frame decreases from 7.7 μs to 0.96 μs but the number of switch-on increases from 6×10^5 to 48×10^5 over 10^4 s of stress time. We found that even a short turn-on time of 0.96 μs at 480 Hz is sufficient to generate the electron-hole pairs (or positively charged species) by impact ionization. These results are consistent with Chen *et al.*'s report [124]; in their study the switch-on time is varied from 1 μs to

100 μs and ΔV_{th} are independent of switch-on time in the investigated range. Therefore, the negative shift of threshold voltage during ac BTS should be carefully considered to realize high frame-rate driving in UHD AM-LCDs. These results clearly indicate the important role of drain bias stress in generating the electron-hole pairs needed for the hole trapping at the channel/gate dielectric interface.

CHAPTER 7

Dynamic Response of a-IGZO and a-Si:H Thin-Film Transistors for Ultra-High Definition AM-LCDs

7.1 Introduction

We evaluate and compare the dynamic response of hydrogenated amorphous silicon (a-Si:H) and a-IGZO TFTs and their potential application to pixel circuits for ultra-high definition (UHD) active-matrix liquid crystal displays (AM-LCDs). For this purpose, we have fabricated test circuits consisting of one TFT connected in series with a storage capacitor. Driving waveforms corresponding to UHD timing specifications are applied to the TFT and the resulting storage capacitance (C_{st}) charging characteristics are investigated. The test circuits are similar to an AM-LCD pixel circuit, but the liquid crystal cell is omitted for fabrication simplicity and capacitance charging is evaluated only for C_{st}. We study in detail the feedthrough voltage (ΔV_P) at C_{st} and its dependence on the gate voltage falling edge (t_{FE}) for both a-Si:H and a-IGZO TFTs. Analytical equations from the literature are adopted to calculate ΔV_P for various falling edge time (t_{FE}) and C_{st} and compared to experimental observations. In addition, we also evaluate the feasibility of overdriving the gate pulse voltage level of a-IGZO TFTs, which we expect should improve the dynamic response of a-IGZO TFTs with minimal negative impact.

7.2 Experimental

7.2.1 Fabrication of 1T1C a-Si:H TFT Test Circuits

The fabrication of back channel etch (BCE)-type bottom-gate a-Si:H TFT follows the process described in Kuo *et al*. [125] and is briefly summarized here. The a-Si:H TFT has patterned chromium gate (200 nm) followed by amorphous silicon nitride (a-SiN_X:H, 400 nm) and a-Si:H (170 nm), both deposited by plasma-enhanced chemical vapor deposition (PECVD). Near the gate insulator/semiconductor interface, deposition rates of PECVD a-Si:H and a-SiN_X:H are significantly reduced to promote higher film density and thus superior electrical properties. A 70-nm layer of phosphorous-doped n^+ a-Si:H is then deposited also by PECVD to act as source/drain (S/D) contact regions. The a-Si:H islands are then defined by dry etching using an SF_6:Cl_2:O_2:He gaseous mixture. The source/drain (S/D) electrodes are 200 nm of sputtered Mo and are wet-etched with a phosphorous-nitric-acetic acid mixture. The resulting gate-S/D metal overlap (*OVLP*) is 3 μm. During the S/D electrode definition, one set of TFTs ("S/D-recessed") is intentionally over-etched by 160 s such that the Mo S/D electrodes are recessed laterally from the channel region by 1 μm while the underlying n^+ a-Si:H layer is unmodified. Lastly, we dry-etched (HBr:Cl_2) the n^+ a-Si:H completely and 70 nm of a-Si:H in the channel region. The a-Si:H TFT dimensions are width (W)/length (L) = 57.5 μm/7.5 μm. The patterned photoresist remained on top of the Mo electrodes throughout the S/D definition steps and is removed at the end. The storage capacitor of C_{st} = 0.19 pF is fabricated at the same time as the TFT using the gate insulator layer as dielectric and is connected in series to the TFT source terminal. The a-Si:H TFT top-view micrograph and cross-section scanning electron microscope (SEM) images and diagrams illustrating the

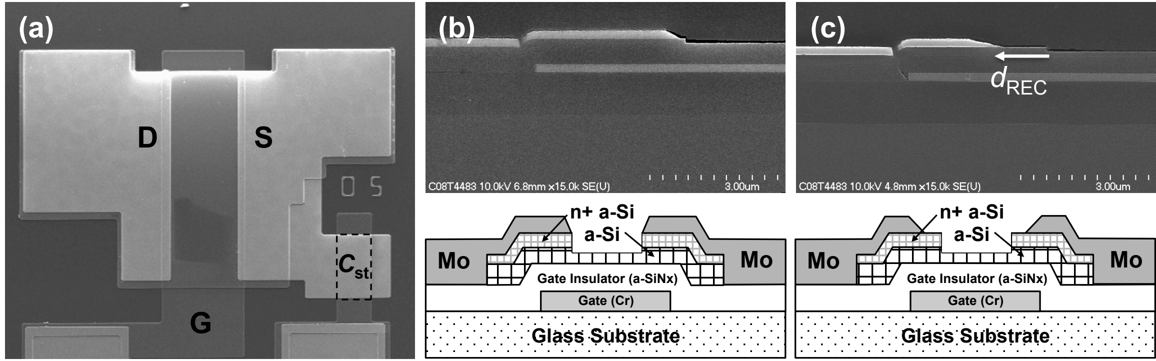


Figure 7.1 (a) Top-view micrograph and (b) SEM image and cross-section diagram of the bottom-gate a-Si:H TFT used in this study. The SEM image and cross-section diagram of the a-Si:H TFT with the S/D-recess is shown in (c), where the recess length (d_{REC}) is 1 μm.

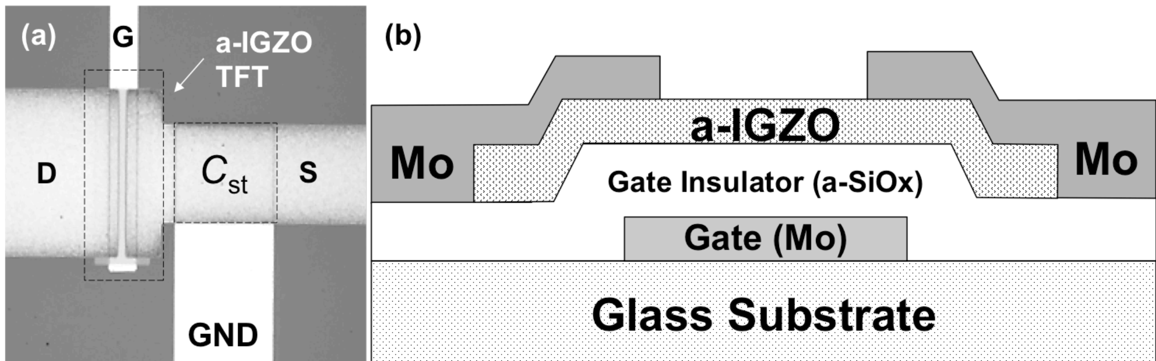


Figure 7.2 (a) Top-view micrograph and (b) cross-sectional diagrams and SEM images of the bottom-gate a-IGZO TFT used in this study.

recess are shown in Figure 7.1.

7.2.2 Fabrication of 1T1C a-IGZO TFT Test Circuits

The fabrication process of the BCE a-IGZO TFT has already been described in detail in section 2.4 and is briefly summarized here. To fabricate the a-IGZO TFT, 100 nm of Mo is first deposited on a glass substrate (Corning Eagle or Asahi PD-200) using sputtering and the gate electrodes are then defined using dry etching. The gate insulator is 200 nm of PECVD amorphous silicon oxide (a-SiO_X) deposited at 380 °C. The channel layer (50 nm) is then deposited by dc sputtering an a-IGZO target of composition ratio of In:Ga:Zn:O = 2:2:1:7. The a-IGZO active islands are defined using dilute oxalic acid

(0.05 M) and then annealed in ambient air at 300 °C for 30 minutes on a hot plate. The gate vias are then opened using dry etching and subsequently 100 nm of Mo is sputtered during metallization. The S/D electrodes are defined using wet etching with 30% H_2O_2. The dimensions of the a-IGZO TFTs fabricated are W/L = 74/3 μm and $OVLP$ = 5 μm. The a-IGZO TFTs undergo one final annealing step of 300°C for 30 minutes in ambient air. For the a-IGZO TFT, test circuits with three C_{st} are fabricated: 0.29 pF, 0.65 pF, and 1.15 pF. The C_{st} in the a-IGZO TFT test circuit is also formed from overlap of the source and common electrodes with the gate insulator as dielectric. The top-view micrograph and cross-section diagram of the a-IGZO TFT are shown in Figure 7.2.

7.2.3 Electrical Properties of a-IGZO and a-Si:H TFTs

For the TFTs fabricated, we approximate C_{GS} in the area of gate-source overlap as two parallel plate capacitors connected in series:

$$C_{GS} = W \times OVLP \times \frac{1}{\frac{1}{C_{GI}} + \frac{1}{C_{act}}}, \tag{7-1}$$

where C_{GI} is the gate insulator capacitance per unit area and C_{act} is the active layer capacitance per unit area. Both C_{GI} and C_{act} can be calculated from the layer thickness and dielectric constant. Using Equation (7-1), we calculate C_{GS} = 0.021 pF for normal a-Si:H TFTs and 0.06 pF for the a-IGZO TFTs. We expect C_{GS} to be lower than 0.021 pF for the S/D-recessed TFT, but not exactly reduced by 1/3 because the highly conductive n^+ regions are unmodified.

The device transfer characteristics (I_D–V_{GS}) at drain-source voltage V_{DS} = 0.1 V are shown in Figure 7.3(a) for normal a-Si:H TFT and Figure 7.3(b) for a-IGZO TFTs. The I_D–V_{GS} for S/D-recessed a-Si:H TFT is similar to the normal TFT and is omitted for

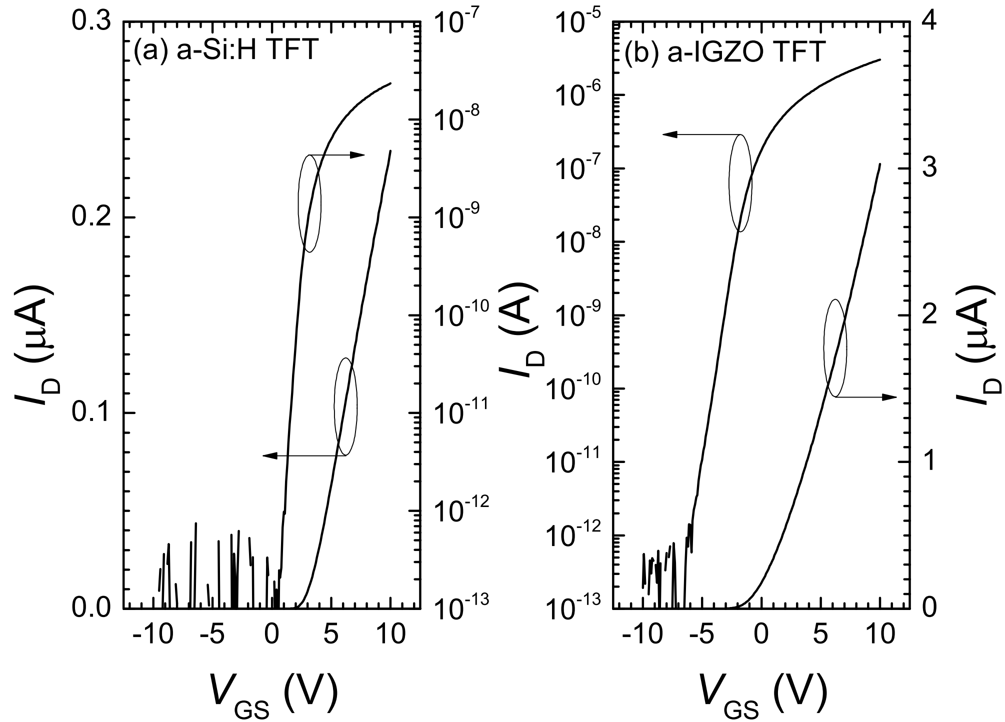


Figure 7.3 The TFT transfer characteristics (I_D–V_{GS}) of the (a) a-Si:H (normal) and (b) a-IGZO TFTs. In both subfigures, V_{DS} = 0.1 V.

	a-Si:H	**a-IGZO**
W/L (μm/μm)	57.5/7.5	74/3
Gate-S/D Overlap (μm)	3	5
Gate Insulator Thickness (nm)	400	200
Active Layer Thickness (nm)	170	50
V_{th} (V)	3.1	0.3
μ_{FE} (cm^2/V·s)	0.29	9.1
C_{st} (pF)	0.19	0.29, 0.65, 1.15

Table 7.1 Parameters of the thin-film transistors and test circuits fabricated.

clarity. The TFT device parameters are extracted from linear fits to I_D–V_{GS} and are summarized together with device dimensions in Table 7.1. We observe that the field-effect mobility of a-IGZO is much higher than a-Si:H, a well-established result in the literature [18]. In a-Si:H, conduction occurs through highly directional sp^3 orbitals, and carriers can be trapped within high-density localized states formed from bond angle fluctuations. In contrast, the conduction band minimum of a-IGZO is formed from the overlap of the large spherical s orbitals of the In^{3+} ions, which are relatively unaffected by structural disorder.

7.2.4 TFT Dynamic Response Measurement Setup

The setup for evaluating the dynamic response of a-Si:H and a-IGZO TFTs is as follows: a two-channel HP 8110A pulse generator is connected to the drain and gate electrodes of the test circuit, where the drain is the data signal and the gate is the select signal. A low-input capacitance (0.02 pF) and high-impedance (input leakage <10 fA) Picoprobe (HP18C-1-5-HV, GGB Industries) is used to measure the voltage of the storage capacitor C_{st} at the TFT source terminal. An Agilent MSO7104B oscilloscope is used to record the storage capacitor voltage measured by the Picoprobe with respect to time. Figure 7.4(a) shows the schematic for the setup used in this study. The waveforms applied to the gate and data lines are shown in Figures 7.4(b) and 7.4(c) respectively. For each frame, two gate pulses of V_{GH} = 18 V are applied to the TFT gate electrode—one for set and another for reset. The low voltage of the gate waveform is V_{GL} = −2V. The gate pulse width, indicated in Figure 7.4(b) as the charging-time margin (t_{cm}), is the time available to charge/discharge C_{st} (for set/reset) in each pixel when the row lines are selected in active matrix operation. For a simple driving scheme without any charge sharing or

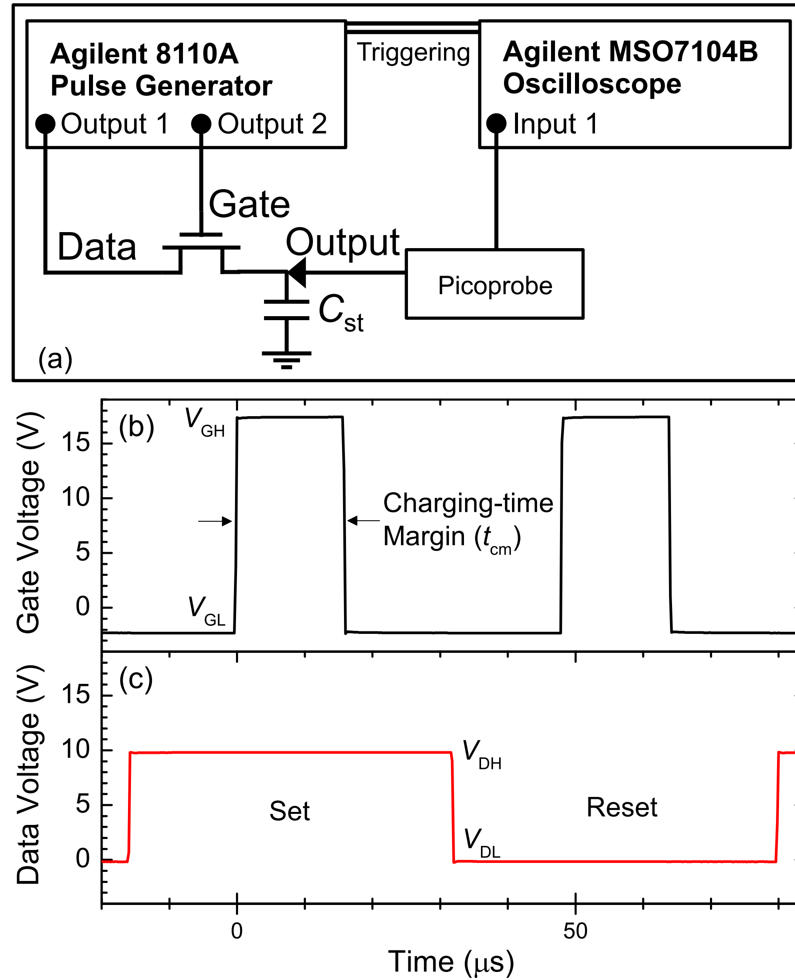


Figure 7.4 (a) The schematic for the setup used to evaluate the dynamic response of the one-TFT-one-capacitor test circuit. (b) The gate voltage applied is V_{GH} = 18 V when charging/discharging and V_{GL} = −2 V at all other times. The charging-time margin t_{cm} is the time available for the storage capacitor to completely charge/discharge. (c) The data voltage applied is V_{DH} = 10 V for set and V_{DL} = 0 V for reset. The set/reset duration is 3 × t_{cm}. The falling edge of the waveforms is 10 ns except where specified.

	Resolution		
	Full HD (1920×1080)	**4K UHD (3840×2160)**	**8K UHD (7680×4320)**
60 Hz	15.4 μs (16 μs)	7.7 μs (8 μs)	3.9 μs (4 μs)
120 Hz	7.7 μs (8 μs)	3.9 μs (4 μs)	1.9 μs (2 μs)
240 Hz	3.9 μs (4 μs)	1.9 μs (2 μs)	0.96 μs (1 μs)
480 Hz	1.9 μs (2 μs)	0.96 μs (1 μs)	0.48 μs (0.5 μs)

Table 7.2 The calculated charging-time margins calculate from various HD and UHD AM-LCD resolution and frame rate specifications.

pre-charging, t_{cm} is defined as in [126]:

$$\text{Charging-time argin } (t_{cm}) = \frac{1}{\text{Frame Rate} \times \text{Number of Row Lines}}. \quad (7\text{-}2)$$

In this study, we are most interested in the charging-time margins corresponding to the UHD display specifications in [7]. Using Equation (7-2), the t_{cm} are calculated based on these specifications and listed in Table 7.2. The values in parentheses indicate t_{cm} rounded up to the next microsecond and are the values we used for the gate and data waveforms. For each frame, a single fixed pulse of data voltage V_{DH} = 10 V is applied to the drain terminal for set, after which the data voltage is returned to its low level V_{DL} = 0 V for reset. For the data voltage waveform, each set/reset period is defined to be 3 × t_{cm}. Each gate pulse arrives exactly 1 × t_{cm} after the data voltage is applied/removed. The rising and falling edge time (t_{FE}) of the data and gate pulses are all 10 ns unless where specified. For t_{FE} values other than 10 ns, the corresponding rising edge is always 10% of that.

7.3 Results and Discussion

7.3.1 Charging Characteristics of a-Si:H and a-IGZO TFTs for UHD AM-LCDs

The output voltages (V_{out}) at the source terminal of the a-Si:H or a-IGZO TFT as a function of time after applying the gate and data waveforms are shown in Figure 7.5. In this figure, the gate and data waveforms are based on t_{cm} = 16 μs, which corresponds to Full HD 1080p resolution at 60 Hz, the current mainstream AM-LCD specification. In TFT dynamic response, one of the most important metrics is the storage capacitance charging behavior: Incomplete charging directly causes the display grayscale to deteriorate. Within this subsection, C_{st} = 1.15 pF is evaluated for the a-IGZO TFT to

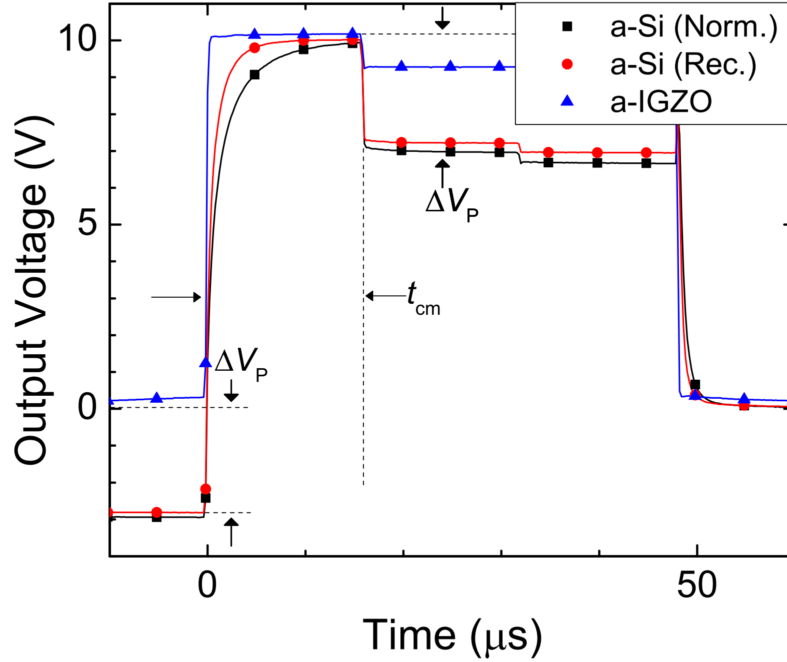


Figure 7.5 The V_{out} measured at the source terminal of the a-Si:H or a-IGZO TFTs with the data and gate waveform applied. The feedthrough voltage ΔV_P is the output voltage drop at the end of t_{cm} after the gate voltage is flipped from V_{GH} to V_{GL}. Storage capacitances are 0.19 pF for a-Si:H TFTs and 1.15 pF for a-IGZO TFT.

maximize the charging delay. In Figure 7.5, both a-Si:H TFTs are able to charge C_{st} completely to V_{DH} = 10 V within 16 μs, but the charging curvature is clearly observable at the scale of the figure. In contrast, charging by the a-IGZO TFT appears almost instantaneous. From this figure, we can approximate the charging behavior as a simple RC process and extract the exponential-fit time constant (τ) for each device structure. The values of τ are 1.35 μs, 0.76 μs, and 0.08 μs for normal a-Si:H, S/D-recessed a-Si:H, and a-IGZO TFT, respectively. In the simple RC model, the TFT drain current (I_D) supplies the charges to the capacitor:

$$C_{st}\frac{dV_{out}}{dt} = I_D. \tag{7-3}$$

We can approximate I_D using the following simplified ideal MOSFET equation, which is appropriate for small V_{DS}:

$$I_D = \mu_{FE} C_{GI} \frac{W}{L} (V_G - V_{\text{out}} - V_{th})(V_D - V_{out}). \quad (7\text{-}4)$$

We then combining Equations (7-3) and (7-4) to get

$$C_{st} \frac{dV_{out}}{dt} = \mu_{FE} C_{GI} \frac{W}{L} (V_G - V_{\text{out}} - V_{th})(V_D - V_{out}). \quad (7\text{-}5)$$

Equation (7-5) is then rearranged:

$$\frac{\mu_{FE} C_{GI} W}{C_{st} L} dt = \frac{dV_{out}}{(V_G - V_{out} - V_{th})(V_D - V_{out})}$$

$$= -\frac{1}{V_D - V_G + V_{th}} \left[\frac{1}{V_{out} + V_{th} - V_G} dV_{out} - \frac{1}{V_{out} - V_D} dV_{out} \right]$$

$$= -\frac{1}{V_D - V_G + V_{th}} \begin{bmatrix} \frac{1}{V_{out} + V_{th} - V_G} d(V_{out} + V_{th} - V_G) \\ - \frac{1}{V_{out} - V_D} d(V_{out} - V_D) \end{bmatrix}. \quad (7\text{-}6)$$

Integrating Equation (7-6) from $t = 0$ to an arbitrary $t = t_{\text{ch}}$, we obtain

$$\int_0^{t_{ch}} \frac{\mu_{FE} C_{GI} W}{C_{st} L} dt = -\frac{1}{V_D - V_G + V_{th}} \int_0^{V_{out}} \begin{bmatrix} \frac{1}{V_{out} + V_{th} - V_G} d(V_{out} + V_{th} - V_G) \\ - \frac{1}{V_{out} - V_D} d(V_{out} - V_D) \end{bmatrix} \quad (7\text{-}7)$$

$$t_{ch} \frac{\mu_{FE} C_{GI} W}{C_{st} L} = -\frac{1}{V_D - V_G + V_{th}} \left[\ln(V_{out} + V_{th} - V_G) - \ln(V_{out} - V_D) \right]_0^{V_{out}}$$

$$= \frac{1}{V_G - V_D - V_{th}} \left[\ln \frac{(V_{out} + V_{th} - V_G)}{(V_{out} - V_D)} \right]_0^{V_{out}}$$

$$= \frac{1}{(V_G - V_D - V_{th})} \ln \frac{(V_G - V_{out} - V_{th}) V_D}{(V_G - V_{th})(V_D - V_{out})}. \quad (7\text{-}8)$$

Assuming that V_{G} and V_{D} are at their maximum values V_{GH} and V_{DH}, respectively, the time required for charging C_{st} to a specific voltage V_{out} can be derived [63]:

$$t_{ch}(V_{\text{out}}) = \frac{C_{st} L}{\mu_{FE} C_{GI} W} \frac{1}{(V_{GH} - V_{DH} - V_{th})} \ln \frac{(V_{GH} - V_{out} - V_{th}) V_{DH}}{(V_{GH} - V_{th})(V_{DH} - V_{out})}. \quad (7\text{-}9)$$

With regards to Equation (7-9), τ approximately corresponds to the t_{ch} when $V_{\text{out}} = 6.3$ V (0.63 V_{DH}). We note that t_{ch} is directly proportional to C_{st} and inversely proportional to W/L, C_{GI}, and μ_{FE}. To better compare the charging time for the different TFT dimensions

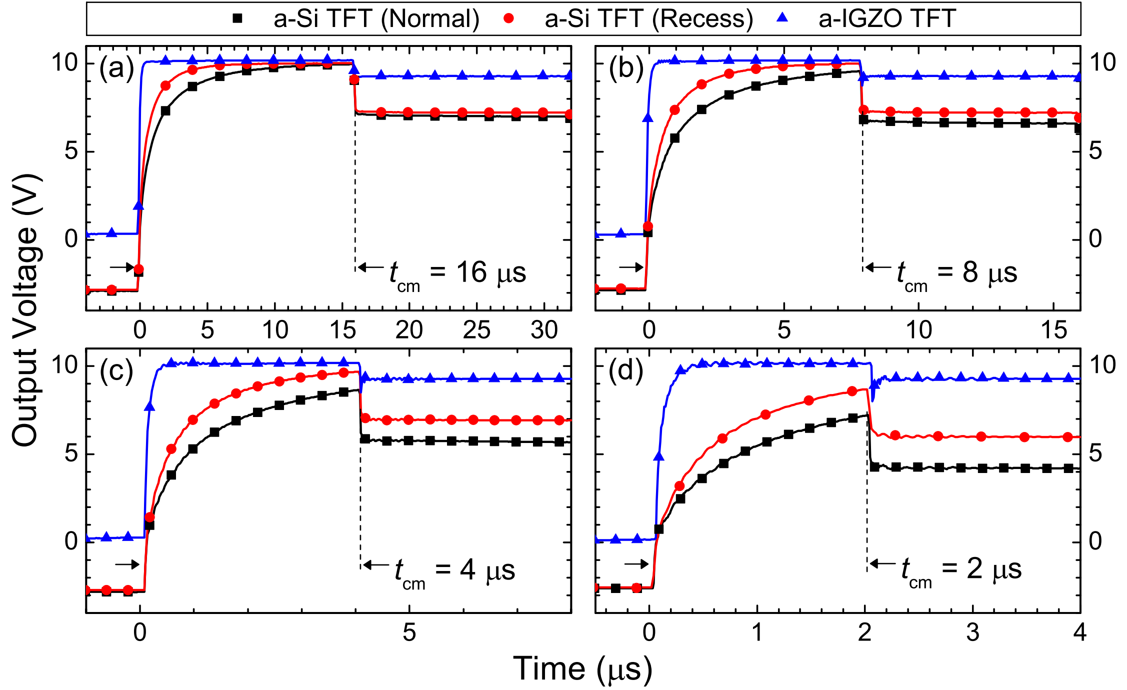


Figure 7.6 The output voltage at the source terminal of the a-Si:H and a-IGZO TFTs after applying the gate and data voltage waveforms based on (a) t_{cm} = 16 μs, (b) t_{cm} = 8 μs, (c) t_{cm} = 4 μs, (d) t_{cm} = 2 μs, corresponding to the AM-LCD specifications in Table 7.2. C_{st} is 1.15 pF for a-IGZO TFTs and 0.19 pF for a-Si:H TFTs.

and structures, we normalize τ and calculate $(\tau \times W \times C_{GI})/(C_{st} \times L)$ to be 0.828 s/cm^2, 0.466 s/cm^2, and 0.0308 s/cm^2 for the normal a-Si:H, recessed a-Si:H, and a-IGZO TFT, respectively. It becomes obvious that the charging time of the a-IGZO TFT is at least an order of magnitude lower than that of any a-Si:H TFT.

To highlight the advantage of a-IGZO TFTs over a-Si:H TFTs in terms of charging characteristics, we apply gate and data waveforms based on the charging-time margins given in Table 7.2 and show the resulting output voltages in Figures 7.6 and 7.7. In Figure 7.6(a), where t_{cm} = 16 μs, the a-Si:H TFTs are capable of fully charging C_{st} within the allotted time. As t_{cm} is reduced to 8 μs and 4 μs in Figures 7.6(b) and 7.6(c), the a-Si:H TFTs begin to struggle to charge the storage capacitor. In Figures 7.6(d), where t_{cm} = 2 μs represents the 8K×4K UHD AM-LCD at 120 Hz, the a-Si:H TFTs can only charge

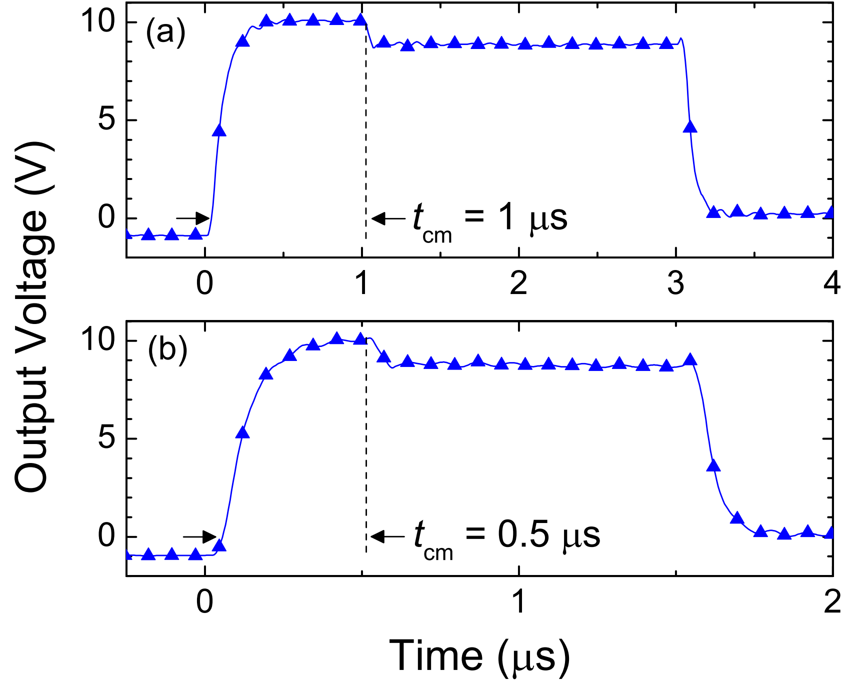


Figure 7.7 The output voltage at the source terminal of the a-IGZO TFTs after applying the gate and data voltage waveforms based on (a) t_{cm} = 1 μs and (b) t_{cm} = 0.5 μs corresponding to 8K×4K resolution at 240 and 480 Hz. For this figure, C_{st} = 1.15 pF.

C_{st} to 7.2 V (normal) and 8.7 V (S/D-recessed). In real-world AM-LCD operation, gate and data bus-line RC delay may impose additional requirements for the charging-time margin [127], meaning that further degradations are expected for a-Si:H TFTs. In comparison, the simple BCE-type bottom-gate a-IGZO TFT is able to readily charge C_{st} to V_{DH} = 10 V with ease for all four cases shown in Figure 7.6. Charging of C_{st} by the a-IGZO TFT is shown in Figure 7.7 for (a) t_{cm} = 1 μs and (b) 0.5 μs, corresponding to 8K×4K resolution at 240 and 480 Hz, and the C_{st} is fully charged to V_{DH} before the end of t_{cm}.

7.3.2 Feedthrough Voltage of a-Si:H and a-IGZO TFTs

The feedthrough voltage ΔV_P shown in Figure 7.5 is the voltage drop at C_{st} after the gate voltage V_G flips from V_{GH} to V_{GL} for both set (V_{out} charging to V_{DH} = 10 V) and reset

(V_{out} discharging to V_{DL} = 0 V). Because of the ΔV_P voltage drop, V_{out} for the a-Si:H TFTs start at negative values ($V_{out} = -\Delta V_P$) before C_{st} charging at time = 0 s. It was originally observed as clock feedthrough in CMOS switched-capacitor circuits, affecting its high-frequency accuracy [128]. In AM-LCD operation, ΔV_P at the pixel electrode primarily manifests itself as image flickering [59]. Takabatake *et al.* developed a series of equations describing ΔV_P [60], which we briefly summarize below.

There are two primary contributions to ΔV_P: channel charge redistribution when V_G is reduced from V_{GH} to $V_{th} + V_{DH}$, and capacitance feedthrough from C_{GS} to C_{st} when V_G is reduced from $V_{th} + V_{DH}$ to V_{GL}. Channel charge redistribution occurs when the TFT switches from its on to off state and the accumulated channel charge (Q_{ch}) is released towards the source and drain terminals. We can estimate Q_{ch} in the area of overlap (A) between the gate electrode and the active layer with the following equation:

$$Q_{ch} = C_{GI}A(V_{GH} - V_{th} - V_{DH}). \quad (7\text{-}10)$$

In our TFTs, we calculate the overlap area as $A = W\times(L+2OVLP)$. When $V_G = V_{th} + V_{DH}$, the TFT is turned off and half of any Q_{ch} in the channel is redistributed onto C_{st}:

$$\Delta V_{P,CR} = \alpha\frac{Q_{ch}}{C_{st}} = \alpha\frac{C_{GI}A(V_{GH}-V_{th}-V_{DH})}{C_{st}}, \quad (7\text{-}11)$$

where α is a constant factor related to the gate voltage falling edge. The capacitance feedthrough component of ΔV_P can be calculated from voltage division between two capacitors C_{st} and C_{GS}. Assuming that the initial output voltage is V_{out} and the final output voltage is V'_{out}, we can write the charge conservation equation before/after V_G flips from $V_{th}+V_{DH}$ to V_{GL} and solve for $V_{out}-V'_{out}$:

$$V_{out}C_{st} + (V_{out} - V_{th} - V_{DH})C_{GS} = V'_{out}C_{st} + (V'_{out} - V_{GL})C_{GS}$$

$$V_{out}C_{st} + V_{out}C_{GS} - V_{th}C_{GS} - V_{DH}C_{GS} = V'_{out}C_{st} + V'_{out}C_{GS} - V_{GL}C_{GS}$$

$$(V_{out} - V'_{out})C_{st} + (V_{out} - V'_{out})C_{GS} = (V_{th} + V_{DH} - V_{GL})C_{GS}$$

$$\Delta V_{P,F} = V_{out} - V'_{out} = \frac{C_{GS}}{C_{GS}+C_{st}}(V_{th} + V_{DH} - V_{GL}). \tag{7-12}$$

In Equation (7-12), capacitance feedthrough primarily depends on the ratio between C_{GS} and C_{st}. Overlap capacitance C_{GS} can be eliminated through the use of a self-aligned structure [68], [129]–[131], but is difficult to avoid in the commonly used bottom-gate staggered structure such as the TFTs in this study. The total ΔV_P is a sum of Equations (7-11) and (7-12):

$$\Delta V_P = \Delta V_{P,F} + \Delta V_{P,CR} = \frac{C_{GS}}{C_{GS}+C_{st}}(V_{th} + V_{DH} - V_{GL}) + \alpha\frac{C_{GI}A(V_{GH}-V_{th}-V_{DH})}{C_{st}}. \tag{7-13}$$

The factor α ranges from 0 to 0.5, depending on how fast the drop from V_{GH} to $V_{DH} + V_{th}$ is. For a very short t_{FE}, the TFT is turned off so abruptly that no charges can be released through the drain terminal while V_G is reduced from V_{GH} to $V_{th} + V_{DH}$. In this upper limit of $\alpha = 0.5$, t_{FE} satisfies the condition:

$$t_{FE} \ll \frac{L^2}{\mu_{FE}\cdot\Delta V_{P,CR}}. \tag{7-14}$$

The right-hand side of Equation (7-14) is the channel transit time for accumulated charges. For longer t_{FE}, α decreases until it approaches the lower limit of $\alpha = 0$. In this lower limit, t_{FE} is much slower than channel transit time of charge carriers:

$$t_{FE} \gg \frac{L^2}{\mu_{FE}\cdot\Delta V_{P,CR}}. \tag{7-15}$$

In this case, most if not all of Q_{ch} can be released through the drain terminal while V_G is reduced from V_{GH} to $V_{th} + V_{DH}$. Contribution from $\Delta V_{P,CR}$ then becomes negligible ($\alpha \approx 0$) and the total feedthrough voltage is simply

$$\Delta V_P = \Delta V_{P,F} = \frac{C_{GS}}{C_{GS}+C_{st}}(V_{th} + V_{DH} - V_{GL}). \tag{7-16}$$

We note that according Equation (7-16), in the case of slow t_{FE}, ΔV_P does not depend on

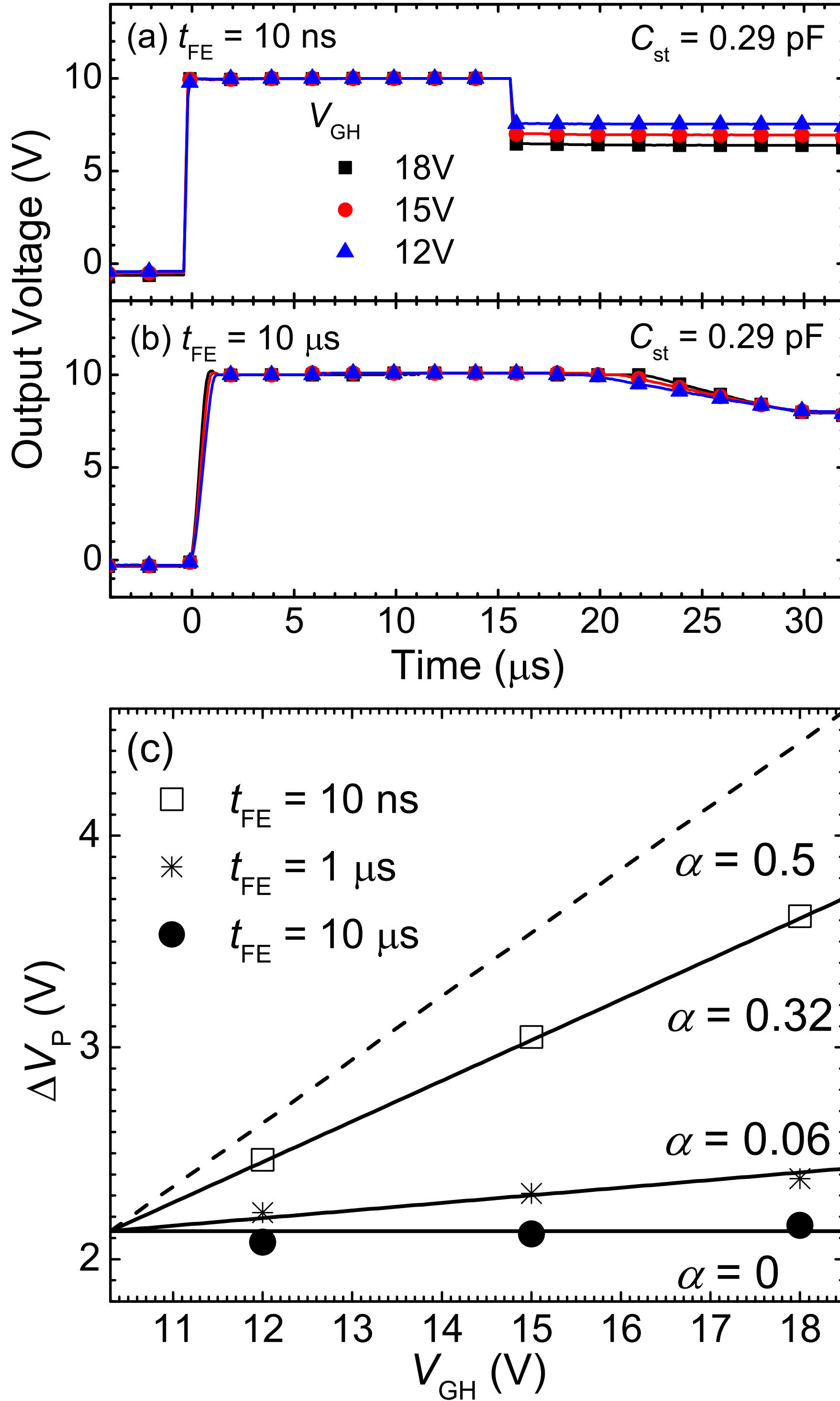


Figure 7.8 The output voltage of the a-IGZO TFT test circuit for waveforms with V_{GH} varied from 18 V to 12 V for (a) t_{FE} = 10 ns and (b) t_{FE} = 10 μs. The storage capacitance tested in this figure is 0.29 pF. In (c), the ΔV_P extracted for t_{FE} = 10 ns (empty squares), 1 μs (solid circles), and 10 μs (asterisks) are shown. The calculated ΔV_P values are also shown in the figure for α = 0 to 0.5.

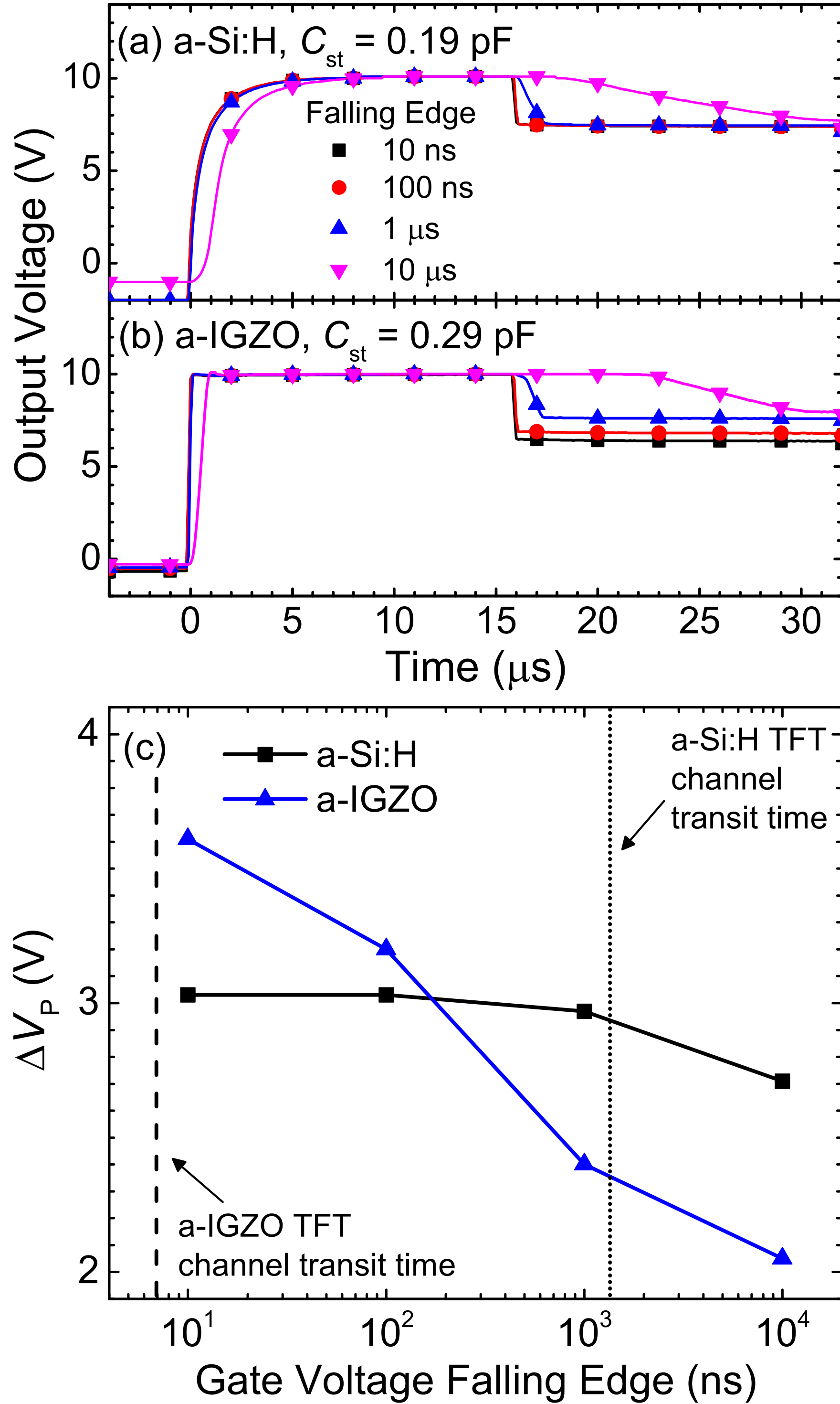


Figure 7.9 The V_{out} of the (a) a-Si:H and (b) a-IGZO TFT test circuits for waveforms with t_{FE} varied from 10 ns to 10 μs. The C_{st} evaluated in this figure is 0.19 pF and 0.29 pF for the a-IGZO and a-Si:H TFTs, respectively. The ΔV_P are extracted from (a) and (b) and shown in (c). Using Equation (7-14), channel transit times is calculated and denoted in (c) as dashed line and dotted line for the a-IGZO and a-Si:H TFTs, respectively.

V_{GH}. We can experimentally verify this by comparing the V_{GH} dependence of ΔV_P for slow and fast t_{FE}. The output voltage of the a-IGZO TFT test circuit is shown in Figure 7.8, where the falling edge of the gate pulse is (a) t_{FE} = 10 ns and (b) t_{FE} = 10 μs. In Figure 7.8(c), ΔV_P corresponding to different V_{GH} are extracted for t_{FE} = 10 μs, 1 μs, and 10 ns. We first calculate the ΔV_P for various V_{GH} using Equation (7-13) with $\alpha = 0.5$ and we find that the generated values are much larger than the experimental data for t_{FE} = 10 ns. This means that the actual fast-t_{FE} limit for a-IGZO TFTs is much smaller than 10 ns. Using Equation (7-10), we calculate the channel transit time of the a-IGZO TFT to be 7.2 ns. This is consistent with what we observe in Figure 7.8(c) in that Equation (7-14) is not satisfied because channel transit time and t_{FE} are on the same order of magnitude and thus $\alpha < 0.5$. For t_{FE} = 10 ns, we find that Equation (7-13) with $\alpha = 0.32$ models the experimental data quite well. In the same figure, ΔV_P appears to be independent of V_{GH} for t_{FE} = 10 μs and can be well described by Equation (7-16). This means that t_{FE} = 10 μs, which is three orders of magnitude larger than the channel transit time, can be considered as the slow-t_{FE} limit and Equation (7-15) is satisfied.

In Figure 7.9, we compare the impact of t_{FE} on the ΔV_P of (a) normal a-Si:H and (b) a-IGZO TFT by varying t_{FE} from 10 ns to 10 μs. The extracted ΔV_P at various t_{FE} are shown in Figure 7.9(c) for normal a-Si:H and a-IGZO TFTs. For a change of three orders of magnitude in t_{FE}, ΔV_P decreases by only 0.3 V for the a-Si:H TFT. Upon inspection, ΔV_P appears to be almost unchanged from t_{FE} = 10 ns to 1 μs. In contrast, ΔV_P decreases by 1.6 V for the a-IGZO TFT over the same range of t_{FE} values. This significant difference is primarily due the fact that the μ_{FE} of a-IGZO is more than an order of magnitude larger than that of a-Si:H, which would allow Equation (7-15) to be fulfilled at

a lower t_{FE}. We calculate the channel transit time to be 1.2 μs for a-Si:H TFTs and it is shown in Figure 7.9(c) together with that for a-IGZO TFTs. Our experimental observations are consistent with these two values in that for a-Si:H TFTs, ΔV_P remains almost constant for $t_{FE} < 1$ μs. For a-IGZO TFTs, ΔV_P is seen to be decreasing for all t_{FE} because no t_{FE} faster than 10 ns is tested in this study. An implication of Figure 7.9 is that it may be possible to reduce ΔV_P for the a-IGZO TFT by controlling for t_{FE} because of the shorter channel transit time, while the same is difficult to realize for a-Si:H TFTs.

The ΔV_P for the S/D-recessed a-Si:H TFT (not shown) is similar to the normal a-Si:H TFT curve shifted downward with the overall trend remaining the same. We have omitted some of the experimental data for the S/D-recessed a-Si:H TFT in this section because only marginal improvements to ΔV_P (<10%) were observed. This is most likely due to the fact that the n^+-doped a-Si:H S/D contact regions remain unmodified even though the metal electrodes are recessed by 1/3.

To study the impact of C_{st} on the dynamic response of a-IGZO TFT test circuits, the output voltage for circuits with three different storage capacitances are characterized and shown in Figure 7.10(a). The t_{FE} for the waveforms applied are all 10 ns. From the figure, we observe that larger C_{st} corresponds to higher charging times and lower ΔV_P, which is what we expect based on the previous analyses. The difference in terms of charging time is insignificant in this time-scale (t_{cm} = 16 μs) and only observable in the Figure 7.10(a) inset. Of particular interest is the ΔV_P, which we extract to be 3.3 V, 1.8 V, and 0.9 V for C_{st} = 0.29 pF, 0.65 pF, and 1.15 pF, respectively, and shown in Figure 7.10(b) as empty squares. The ΔV_P for the normal a-Si:H TFT (C_{st} = 0.19 pF) is extracted from Figure 7.5 to be 2.71 V and is shown in the same figure as a solid circle. From Equation (7-13), we

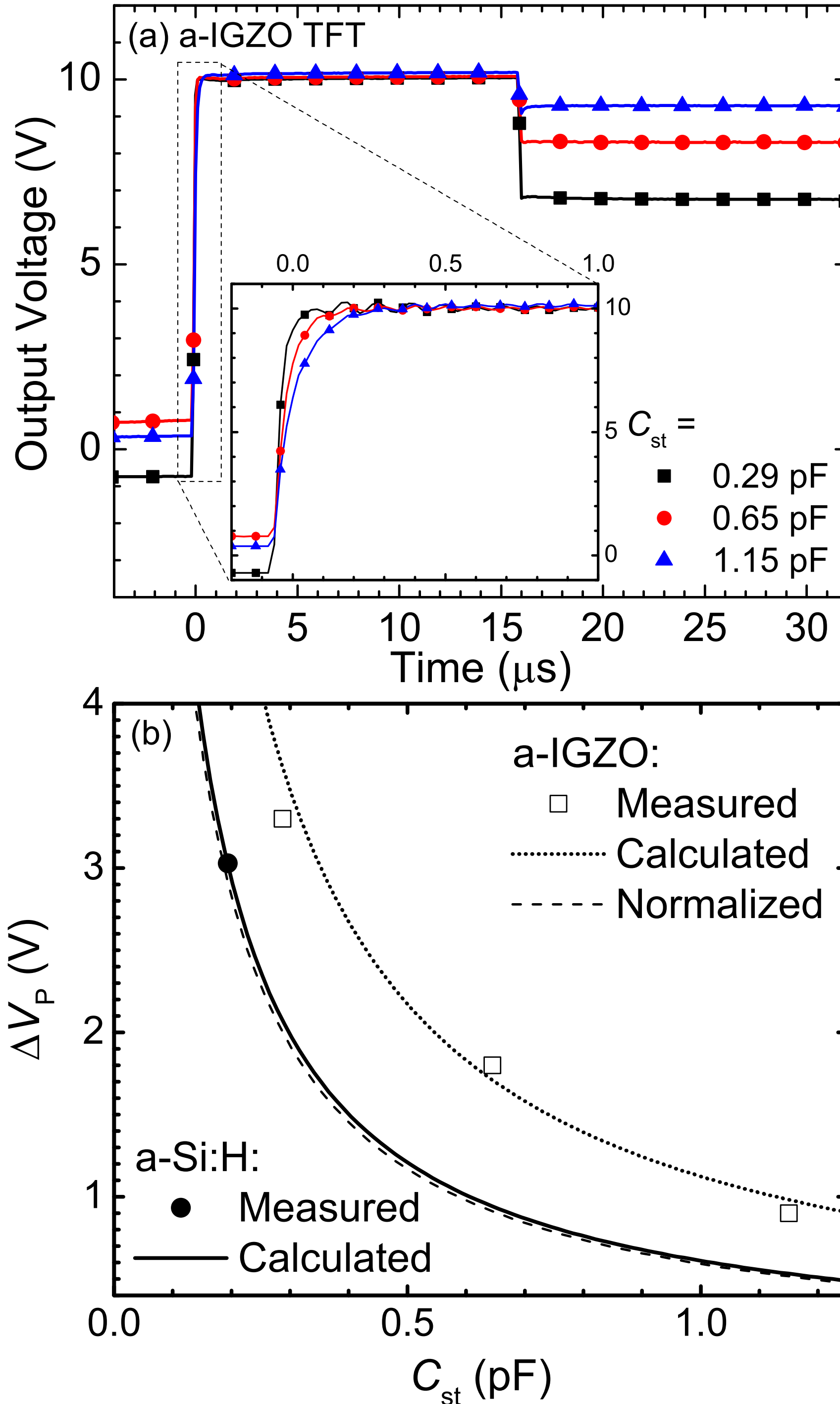


Figure 7.10 (a) The V_{out} of a-IGZO TFT test circuits with different C_{st}. The charging-time margin used for this figure is t_{cm} = 16 μs. (b) The ΔV_P for a-IGZO TFTs with different C_{st} extracted from (a) is shown as empty squares. The ΔV_P is calculated using Equation (7-13) and shown in the figure as a dotted line (α = 0.32). The normal a-Si:H TFT ΔV_P is also shown in the figure as a solid circle, with the calculated values (α = 0.5) represented as a solid line. The same calculation is performed after normalizing the a-IGZO TFT for W, L, $OVLP$, and C_{GI} and shown as a dashed line.

calculate and show the relationship between C_{st} and ΔV_P for a-Si:H (solid line) and a-IGZO TFTs (dotted line) in Figure 7.10(b). We observe that because of device structure and geometry, the a-IGZO TFT has greater ΔV_P than the a-Si:H TFT for the same C_{st}. In Figure 7.10(c), we normalize the a-IGZO TFT ΔV_P curve based on the same geometry (*W*, *L*, *OVLP*) and C_{GI} as the a-Si:H TFT and show it as a dashed line. In the normalization of the a-IGZO TFT curve, we assume a-SiO_X/a-SiN_X bilayer gate insulator having the same C_{GI} as 400-nm a-SiN_X. We can thus conclude that given identical TFT geometries and structure, the a-IGZO TFT suffers no drawbacks to ΔV_P and has vastly superior charging characteristics in comparison to the a-Si:H TFT. By implementing a larger C_{st}, the ΔV_P of a-IGZO TFTs can be further reduced. Increasing C_{st}, as shown in Figure 7.10(a), has negligible impact on the charging characteristics of the a-IGZO TFT. The limiting factor in this case would not be charging-time margin but rather the aperture ratio of the AM-LCD pixel. This also bodes well for a-IGZO TFTs as the backplane technology of large-area AM-LCDs, which have larger liquid-crystal cells and thus greater cell capacitance.

7.3.3 a-IGZO TFT Gate Overdrive Operation

Overdrive operation was initially proposed for operation of individual AM-LCD cells to improve the gray-level response when displaying high-speed motion images [132]–[134]. Because there is a time delay in the gray-level transitions of a liquid crystal cell, the image signal can be pre-processed and an additional voltage (overdrive voltage V_{OD}) can be added on top of the image signal to help the liquid crystal reach the desired transmittance faster. However, within published literature, the TFT has rarely been considered in the study of the overdrive method for AM-LCDs. In this work, we apply

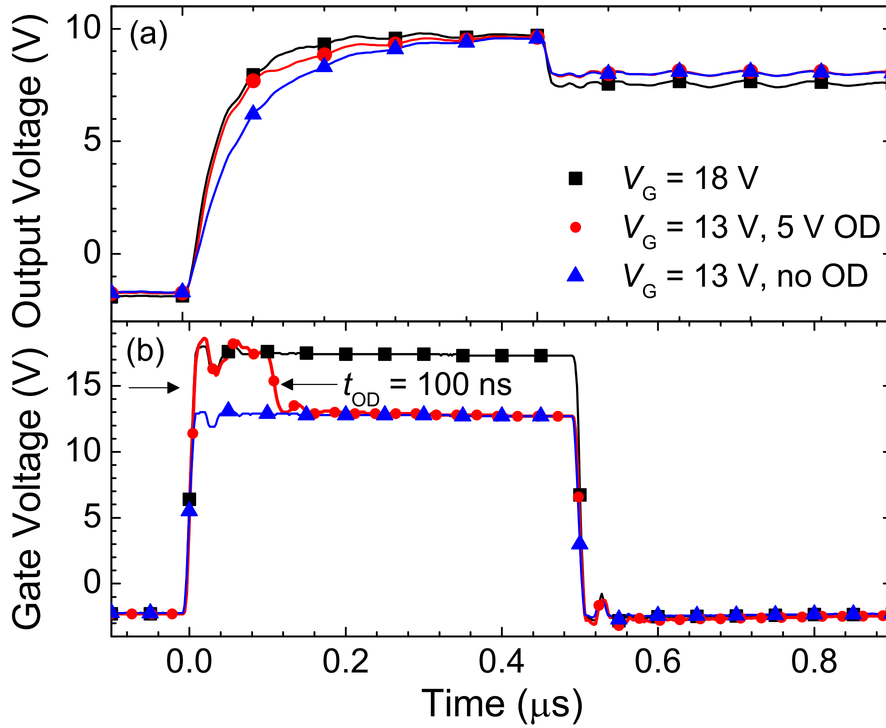


Figure 7.11 The overdrive operation of the a-IGZO TFT in the test circle is shown in (a). The waveforms for baseline, overdrive, and full overdrive are shown in (b). Overdrive operation adds t_{OD} = 100 ns of V_{OD} = 5 V on top of the baseline V_{GH} = 13 V at the beginning of t_{cm}. In full overdrive, the entire duration of t_{cm} is V_{GH} = 18 V. For this experiment, a test circuit with C_{st} = 0.65 pF was evaluated.

the voltage overdrive method to the gate signal of the a-IGZO TFT test circuit and the results are shown in Figure 7.11 for C_{st} = 0.65 pF. As shown in Figure 7.11(b), three different gate waveforms are tested: V_{GH} = 18 V (fully overdriven), V_{GH} =13 V + 5 V (overdrive time t_{OD} = 100 ns), and V_{GH} = 13 V (baseline). Alternatively, we can also consider V_{GH} = 18 V the baseline, V_{GH} = 13 V + 5 V (t_{OD} = 100 ns) partially underdriven, and V_{GH} = 13 V fully underdriven. In this scenario, by underdriving the TFT after the capacitor has been sufficiently charged, the final V_{GH} value is reduced, which according to Equation (7-13) corresponds to lower ΔV_P From Figure 7.11(a), we see that the proposed method (solid circles) is a good balance of both improved charging time compared to V_{GH} = 13 V and lower ΔV_P than V_{GH} = 18 V. In our previous work, we have

shown that reducing the duration of high gate voltage (V_{GH}) in pulsed waveforms of a-IGZO TFT dynamic operation improves the ac bias-temperature stress (BTS) stability [131]. The partially underdriven method proposed in this study is expected to help reduce ac BTS instability and still retain adequate charging characteristics.

CHAPTER 8

Conclusions and Future Work

8.1 Summary of Results and Conclusions

In this dissertation, we have developed a comprehensive and robust subgap density-of-states (DOS) model for a-IGZO based on a combination of experimental results and information available in the literature. The valence bandtail states are defined by parameters extracted from optical absorption and transient photoconductance spectroscopy. We adopt the results of first-principles calculations of a-IGZO in the literature, which states that oxygen vacancies form fully occupied deep donor states near the valence band. The conduction bandtail and deep-gap states are extracted by multi-frequency capacitance–voltage (C–V) spectroscopy. Numerical simulations indicate that the conduction band deep-gap states originate from excess oxygen acting as electron acceptors. Recombination of an electron trapped in the conduction band deep-gap state and a hole in the valence band is responsible for the deep-level emission in the photoluminescence (PL) spectrum of a-IGZO thin film. We have used this DOS model in 2D numerical simulations to obtain electrical properties of a-IGZO metal-semiconductor field-effect transistors in good agreement with experimental data, and the results are published in peer-reviewed literature [98].

In order to investigate what effect oxygen flow during a-IGZO sputtering has on TFT electrical properties and stability, we fabricated simple inverted-staggered a-IGZO TFTs on silicon substrates using mechanical masks for 5%, 10%, and 15% O_2 partial pressure (p_{O_2}). We find that the excess oxygen content can significantly impact a-IGZO TFT electrical characteristics. High p_{O_2} reduces TFT field-effect mobility (μ_{FE}) and on-current (I_{on}) and increases threshold voltage (V_{th}). When undergoing positive bias-temperature stress (PBTS) at a gate stress voltage of V_{st} = +10 V, higher p_{O_2} corresponds to larger threshold voltage shift (ΔV_{th}), while no clearly discernable trend is observed for negative bias-temperature stress (NBTS). The subgap DOS of a-IGZO are decomposed into exponential bandtail states and Gaussian-like deep-gap states, according to the DOS model we have adopted. The peak density of the Gaussian-like distributions is larger for higher p_{O_2} during deposition. Assuming that high p_{O_2} during deposition is associated with incorporation of excess/weakly-bonded oxygen in the a-IGZO thin film, then we can conclude that these deep-gap states are acceptor-like electron trap states in the form of O^0 or O^{1-} ions. The O^0/O^{1-} ions may trap an electron and become O^{1-}/O^{2-}, reducing free carriers and increasing V_{th}. During PBTS, the migration of these ion species can be accelerated by a combination of electric field and temperature, and increased accumulation at the a-IGZO/SiO_2 interface causes ΔV_{th} to become more severe.

We have thoroughly investigated the impact of annealing in high-O_2% or low-O_2% atmospheres have on the deep-level PL emission of a-IGZO thin films. We have found that the deep-level PL emission at 1.82 eV is stronger for a-IGZO annealed in high-O_2% atmospheres or deposited in higher p_{O_2}. After several possible electron-hole transitions have been discussed, it appears that radiative recombination between electrons in

acceptor-like excess oxygen (O) states and holes in valence bandtail states is most likely to be responsible for the observed deep-level PL emission. We have compared the PL intensity of this emission within the a-IGZO TFT channel before and after PBTS and NBTS. Our results show that after PBTS, V_{th} becomes more positive, μ_{FE} slightly decreases, and deep-level emission becomes stronger. We speculate that these are the results of higher concentration of excess oxygen when adsorbed oxygen diffuses into a-IGZO under the influence of electric fields and stress temperature. It is possible that the opposite is happening during NBTS.

To investigate the ac bias-temperature stress (BTS) stability of a-IGZO TFTs for ultra-high definition (UHD) active-matrix liquid crystal display (AM-LCD) applications, photolithography is used to fabricate high-performance and highly stable bottom-gate source/drain (S/D) recessed nearly self-aligned a-IGZO TFTs that have a-$SiON_X$ as passivation layer. The a-IGZO TFTs have been demonstrated to be very reliable under a wide variety of ac and dc stressing conditions at 70 °C. We find that for our TFTs, the bipolar ac BTS instability time-evolution can be well-described by a simple sum of the positive and negative unipolar ac BTS instability but not the sum of the dc BTS instabilities. The ac frame time dependence of the threshold voltage shift is thoroughly investigated. We find that negative unipolar pulses exhibit larger (more negative) ΔV_{th} shift for longer frame times. For positive unipolar pulses, the ΔV_{th} are initially positive and eventually trend towards negative for all frame time. For bipolar ac BTS, we find that instability also has a dependence on the operation frequency and that higher frequencies causes more instability. This is an important issue that should be addressed for high-refresh rate flat-panel displays. Upon changing the duty cycle of bipolar pulses from 50%

to 10%, we can suppress the ΔV_{th} for the same operation frequency. This shows that different pixel addressing schemes, in the form of duty cycle control, may be viable for improving device stability. By applying gate and data waveforms corresponding to 4K UHD AM-LCD, we observe that ΔV_{th} becomes more negative for higher frame frequencies and higher drain voltages. We speculate that electron-hole pair generation by impact ionization at the source terminal is responsible for the trapping of holes at the a-IGZO/a-SiO_X interface.

To evaluate the dynamic response of a-Si:H and a-IGZO TFTs, we have fabricated test circuits in which a TFT is connected to a storage capacitor. For the a-Si:H TFT, in addition to the normal TFT configuration, we also fabricated the S/D-recessed TFT where the S/D metal is intentionally over-etched to reduce the gate-S/D overlap. Waveforms corresponding to UHD timing specifications are tested. In our results, the S/D-recessed a-Si:H TFTs have slightly superior charging behavior and lower feedthrough voltage (ΔV_P) compared to normal a-Si:H TFTs, but both are insufficient for 8K×4K UHD AM-LCDs. Only the a-IGZO TFT is fully capable of supporting 8K×4K resolution at 480 Hz. Analytical expressions describing the ΔV_P are investigated in detail. In particular, the impact of the gate signal falling edge (t_{FE}) is thoroughly studied. We find that at the small-t_{FE} limit, channel charge redistribution and overlap capacitance feedthrough both contribute to ΔV_P. At the large-t_{FE} limit – approximately three orders of magnitude above the transit time—accumulated channel charges are almost completely released through the drain electrode and do not contribute to ΔV_P. In this case, ΔV_P becomes entirely independent of V_{GH}. The storage capacitance (C_{st}) size is shown to have a strong impact on the ΔV_P for a-IGZO TFTs but has negligible influence on its charging

behavior. After normalizing for TFT geometry and structure, ΔV_P of a-IGZO TFTs is shown to be very similar to a-Si:H TFTs. Increasing the size of C_{st} can reduce the ΔV_P, and for a-IGZO TFTs this can be done without sacrificing charging behavior.

8.2 Recommendations for Future Work

1) In light of the conclusions reached in this dissertation regarding deep-level PL emission, a-IGZO processing conditions, and TFT electrical instability, it is critical to conduct chemical and materials analysis in conjunction the PL spectroscopy evaluation of a-IGZO TFTs we have developed. Definitive microscopic observations by high-resolution tunneling electron microscopy (HRTEM), secondary ion mass spectroscopy (SIMS), and other methods should be conducted to verify our proposed model based on excess-oxygen states.
2) The evaluation of ac bias-temperature stability (BTS) and dynamic response in this dissertation is all done within the context of AM-LCDs. Considering that the active-matrix organic light-emitting diode (AM-OLED) display is expected to take on a significant role in both mobile displays and large area AM-OLED TVs, the dynamic operation instability and dynamic response should be evaluated for a-IGZO TFTs as the backplane technology of AM-OLED displays. For the ac instability, because the AM-OLED is a current-driven device, current-temperature stress should be studied with waveforms corresponding to next generation ultra-high definition AM-OLED displays. Also, the dynamic response should be evaluated for AM-OLED pixel circuits, which are much more complex than AM-LCD pixel circuits in that three or more TFTs are often used.

APPENDIX

List of Publications

Journal Papers

E. K.-H. Yu, R. Zhang, L. Bie, A. Kuo, and J. Kanicki, “Dynamic Response of a-InGaZnO and Amorphous Silicon Thin-Film Transistors for Ultra-High Definition Active-Matrix Liquid Crystal Displays,” *J. Disp. Technol.*, 2015.

Y.-S. Lee, E. K.-H. Yu, D.-H. Shim, H.-S. Kong, L. Bie, and J. Kanicki, “Oxygen flow effects on electrical properties, stability, and density of states of amorphous In–Ga–Zn–O thin-film transistors,” *Jpn. J. Appl. Phys.*, vol. 53, no. 12, p. 121101, Dec. 2014.

E. K.-H. Yu, S. Jun, D. H. Kim, and J. Kanicki, “Density of states of amorphous In-Ga-Zn-O from electrical and optical characterization,” *J. Appl. Phys.*, vol. 116, no. 15, p. 154505, Oct. 2014.

E. K.-H. Yu, K. Abe, H. Kumomi, and J. Kanicki, “AC Bias-Temperature Stability of a-InGaZnO Thin-Film Transistors With Metal Source/Drain Recessed Electrodes,” *IEEE Trans. Electron Devices*, vol. 61, no. 3, pp. 806–812, Mar. 2014.

Conference Proceedings

R. Zhang, L. Bie, T.-C. Fung, E. K.-H. Yu, C. Zhao, and J. Kanicki, “High Performance Amorphous Metal-Oxide Semiconductors Thin-Film Passive and Active Pixel Sensors,” in *IEEE International Electron Devices Meeting (IEDM)*, Washington, DC, 2013, pp. 27.3.1–27.3.4.

E. K.-H. Yu, R. Zhang, L. Bie, A. Kuo, and J. Kanicki, “Dynamic Response of a-InGaZnO Thin-Film Transistors for Ultra-High Definition Active-Matrix Liquid Crystal Displays,” in SID Vehicle Displays and Interfaces 2014, pp. 121-130 (Dearborn, MI, USA)

R. Zhang, L. Bie, E. Yu, and J. Kanicki, “Dynamic response of amorphous In-Ga-Zn-O thin-film transistors for 8K×4K flat-panel display,” in *Device Research Conference (DRC), 2013 71st Annual*, 2013, vol. Supplement, pp. 1–2.

E. K.-H. Yu, K. Abe, H. Kumomi, and J. Kanicki, “AC and DC Bias-Temperature Stability of Coplanar Homojunction a-InGaZnO Thin-Film Transistors,” *SID Symp. Dig. Tech. Pap.*, vol. 44, no. 1, pp. 174–177, Jun. 2013.

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