Techniques for Frequency Synthesizer-Based Transmitters

by

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LIST OF ABBREVIATIONS

CMOS Complementary Metal-Oxide Semiconductor

CP Charge Pump

CPU Central Processing Unit

DAC Digital-to-Analog Converter

DPLL Digital PLL

DCC Duty-Cycle Correction

EVM Error Vector Magnitude

FoM Figure of Merit

GPS Global Positioning System

I In-phase

IF Intermediate Frequency

IIR Infinite Impulse Response

IoT Internet of Things

LF Loop Filter

LP Low Pass

LO Local Oscillator

MEMS Micro-Electro-Mechanical Systems

MSK Minimum Shift Keying

MMD Multi-Modulus Divider

MDLL Multiplying Delay-Locked-Loop

OTA Operational Trans-conductance Amplifier

O-QPSK Offset-Quadrature Phase Shift Keying

PA Power Amplifier

PD Phase Detector

PDF Probability Density Function

PFD Phase-Frequency Detector

PI Proportional-Integral

PLL Phase-Locked-Loop

PSR Power Supply Rejection

PVT Process, Voltage, and Temperature

Q Quadrature-phase

RF Radio Frequency

RX Receiver

RFID Radio-Frequency IDentification

SoC System-on-Chip

TDC Time-to-Digital Converter

TX Transmitter

VCO Voltage Controlled Oscillator

XTAL Crystal

XO Crystal Oscillator

ABSTRACT

Techniques for Frequency Synthesizer-Based Transmitters

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Chair: Michael P. Flynn

Internet of Things (IoT) devices are poised to be the largest market for the semiconductor industry. At the heart of a wireless IoT module is the radio and integral to any radio is the transmitter. Transmitters with low power consumption and small area are crucial to the ubiquity of IoT devices. The fairly simple modulation schemes used in IoT systems makes frequency synthesizer-based (also known as PLL-based) transmitters an ideal candidate for these devices. Because of the reduced number of analog blocks and the simple architecture, PLL-based transmitters lend themselves nicely to the highly integrated, low voltage nanometer digital CMOS processes of today. This thesis outlines techniques that not only reduce the power consumption and area, but also significantly improve the performance of PLL-based transmitters. The main contributions of this thesis are three fold.

First, we introduce a novel frequency quadrupler with sub-picosecond jitter. The 192MHz quadrupler is ideal for generating a fast, low jitter reference for a low phase

noise PLL. The quadrupler requires far less power and area than existing methods.

Second, the CMOS current reuse VCO is modified to reduce the supply voltage and achieve good phase noise with very low power consumption. A 2.5GHz prototype achieves the best phase noise-power efficiency figure of merit for any current reuse VCO.

Third, a fully integrated 2.4GHz transmitter for ZigBee based on a digital fractional-*N* PLL is presented. The prototype achieves an MSK modulation rate of 2Mb/s, delivers -2dBm of output power, and is free of in-band fractional spurs.

CHAPTER I

Introduction

1.1 Background and Motivation

Internet of Things (IoT) is increasing the connectivity of people and things on a scale that once was unimaginable. The physical world itself is becoming a type of information system where sensors and actuators embedded in physical objects—from roadways to pacemakers—are linked through wireless networks, often using the same protocols as the internet.

Internet of things devices are poised to become the largest market for the semiconductor industry [2]. As shown pictorially in Figure 1.1, IoT devices aim to make us and our electronic devices ever more connected to the physical world around us. The applications span several industries such as smart buildings, industrial control, health care, military, and environmental monitoring. In home automation, IoT devices use light or Radio Frequency (RF) energy to power motion detectors which turn lights off if nobody is detected in a room, to dim lights depending on the light level in a room, and to sense and report temperature for air conditioning or heating [7]. In industrial control, IoT devices use vibration energy or

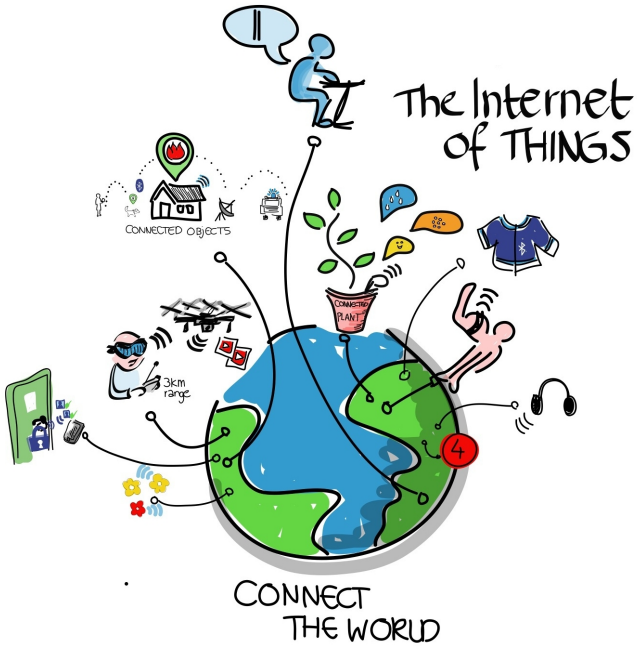

Figure 1.1: Internet of Things (IoT) [1]

thermal energy to monitor and report the condition of rotating machines. In location tracking, they use vibration energy or solar power to enable Global Positioning System (GPS) to sense and the cellular network to report the position of containers, trucks, or rail cars [8].

The diverse set of applications leads to a diverse set of requirements for the electronic devices and in particular for the integrated circuits that are at the heart of these modules. These requirements are elegantly summarized in Figure 1.2. For successful large-scale deployment of wireless IoT systems, each device must have low power consumption and a small form factor. Small form factor results in low cost which leads to mass production and the ubiquitous use of these devices. Low power consumption allows a long battery life, which is imperative in many IoT applications such as wireless sensors [9]. It is due to these requirements that nanometer Complementary Metal-Oxide Semiconductor (CMOS) technology offers the perfect platform to design IoT devices.

Sensor Property	Sub categories	Range of values
Sensing / Actuation Modality	Type	Pressure, temperature, strain, chemical, imaging, sound, etc.
	Duty Cycle	Continuous ↔ Infrequent, on-demand
	Trigger	Timer based (accuracy?); event in monitored value; external trigger (wakeup radio, battery condition, etc.)
Computational Performance		Sub-kHz ↔ 100's of MHz
Form Factor / Size		Submillimeter ↔ tens of centimeter scale
Energy Source / Life Time		Wired (permanently, intermittently); battery (primairy, secondary); energy scavenging (continuous or as available); lifetime of hrs, days, years
Communication Connectivity	Type	Wired vs. wireless (communication distance, communication standard)
	Data Rate / Packet Size	kbps ↔ Gbps; Bytes ↔ MBytes
	Communication Interval	Continuous ↔ Infrequent; triggered by monitored event or external request

Figure 1.2: Categorization of IoT design space [2]

At the heart of any wireless device is the radio that enables the communication of information. A wireless Micro-Electro-Mechanical Systems (MEMS) sensor that collects temperature readings and then must transfer this information to the base station receiver, is one example. Depending on the data rate and packet size, the radio typically consumes the majority of energy in a wireless device [10]. A wireless radio is usually partitioned into two major blocks 1) the Receiver (RX), and 2) the Transmitter (TX). Although reducing the area and power consumption for both the receiver and transmitter is important, most recent work has been focused on optimizing the receiver. However, there are several applications (such as Bluetooth Low-Energy) where power and area of the transmitter become the system bottleneck [11], [12]. For instance, Radio-Frequency IDentification (RFID) tags communicate with a host that is usually free of any power efficiency requirements. However, each RFID tag has a transmitter that needs to be very low power to achieve sufficient battery life time. The improvement in battery life is important as it facilitates a low cost perpetual

Table 1.1: RF transmitter functions and specifications

Function	**Specification**
Modulation	Accuracy
Frequency Translation	Spectral Mask
Power Amplification	Output Power Level

operation of RFID tags.

1.2 Wireless Transmitters

The transmitter is one of the key blocks in any wireless radio. In a wireless sensor node, the power consumption and area requirements of the transmitter are stringent. State of the art wireless sensor nodes typically perform some computation and signal processing on chip [13], therefore it is desirable for the radio to be integrated with the sensor's Central Processing Unit (CPU) to reduce cost. Radio frequency electromagnetic waves are chosen to enable a sufficiently long range of communication. In addition, RF transmitters lend themselves to integration due to their small size. It is for this reason that we focus on integrated RF transmitters for IoT devices.

An RF transmitter performs modulation, upconversion, and power amplification of the baseband signal before the antenna. The design of integrated RF transmitters entails several challenges at both system and circuit levels. Spectral emission mask requirements that are often specified by Federal Communications Commission (FCC), TX to RX leakage, output power level, and linearity are some of the parameters that impact the choice of transmitter architecture [14]. Typical transmitter functions and required specifications are summarized in Table 1.1.

The Modulation type exhibits trade-offs between bandwidth and power. The require-

ments of the wireless communication system impacts the selection of modulation type. Communication requirements can be talk time, maximum range, channel capacity, *etc.* There are two modulation types in an RF transmitter today 1) constant envelope (or nonlinear), and 2) variable envelope (or linear). A modulated signal $x(t) = A\cos(\omega_c t + \phi(t))$ is considered constant envelope if the envelope (amplitude), A, is constant. In linear modulation schemes, A is a function of time and therefore contains information. Constant envelope modulation is usually the adopted modulation type in IoT systems (such as ZigBee [15] and Bluetooth LE [16]) due to its simplicity. Such waveforms contain information only in the zero crossings and can therefore be processed by a nonlinear Power Amplifier (PA) with higher power efficiency[1].

1.3 RF Transmitter Architectures

Three RF transmitter architectures are common in modern nanometer CMOS integrated circuits [17]: 1) Direct conversion, 2) Dual conversion, and 3) Phase-Locked-Loop (PLL) based. In this section, we study all 3 architectures and justify the selection of a PLL based TX for this work.

A generic direct conversion TX is shown in Figure 1.3. Information, in the form of In-phase (I) and Quadrature-phase (Q) binary bits, is converted to the analog domain using a Digital-to-Analog Converter (DAC). The DAC output gets amplified and conditioned by a low pass or band pass filter in the baseband circuits[2]. The low frequency analog baseband signal is upconverted to RF frequency using a mixer that is driven by I and Q Local

[1] Power amplifiers with a constant envelope input are free of any voltage linearity requirements. Therefore, a highly nonlinear PA, such as a class D PA, can be used without the loss of information.

[2] Baseband circuits typically include trans-impedance amplifiers, filters, and programmable gain amplifiers.

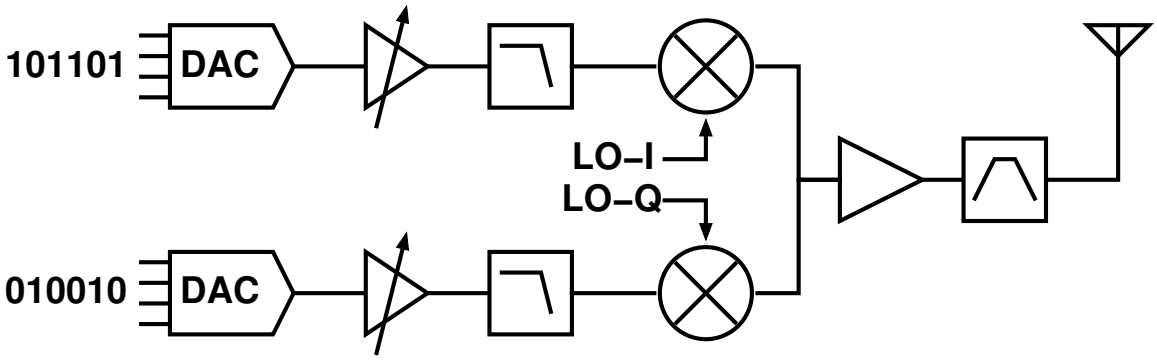

Figure 1.3: A direct conversion transmitter

Oscillator (LO) signals. The mixer output goes through a PA to to drive a 50Ω antenna. The PA output is sometimes band pass filtered before transmission. The final band pass filter is used to reduce the out of band emissions.

A direct conversion transmitter is the most common architecture used today. This transmitter is versatile since it can support any modulation type. It is fairly low power and lends itself to integration due to its relatively simple design. However, it suffers from two main problems: One is the Voltage Controlled Oscillator (VCO) pulling by the PA modulated spectrum. Since the PA and VCO operate at the same frequency, the PA spectrum can corrupt the VCO spectrum which degrades the transmitter Error Vector Magnitude (EVM). A second issue is that although this TX is rather simple, it still requires two DACs, two amplifiers, two filters, and two analog mixers. In addition, a PLL and a divide by 2 circuit is needed to generate the I and Q LO signals. Since the power and area requirements for a sensor network TX are stringent, a simpler TX that is more amenable to integration in nanometer CMOS is desired.

In order to eliminate the pulling issue in a direct conversion transmitter, the baseband signal is upconverted in two or more stages. One popular architecture is the dual conversion

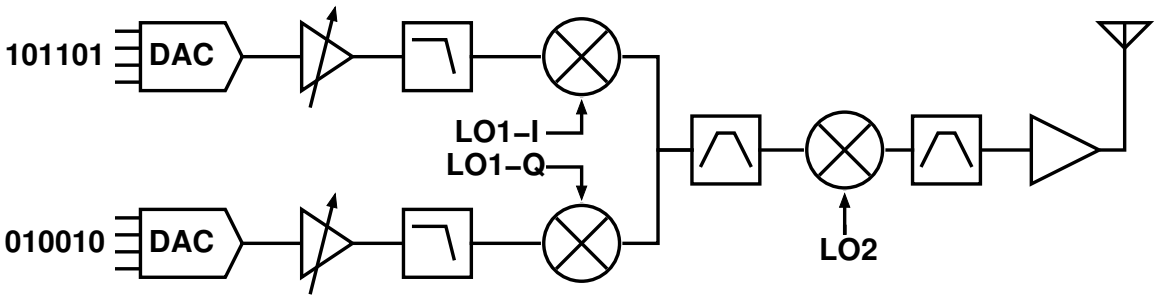

Figure 1.4: A dual conversion (two step) transmitter

(or two-step) transmitter shown in Figure 1.4. After the DAC and baseband circuits, the signal is first upconverted by LO1 to an Intermediate Frequency (IF) and then upconverted to RF by LO2. This two-step transmission eliminates VCO polling as the LO1 and LO2 frequencies are now different (often by a large amount). However, the main difficultly is the band pass filter between first and second upconversion. This band pass filter needs to attenuate unwanted side-bands by a large amount, *e.g.,* 50-60dB [14]. Furthermore, the addition of new blocks such as an IF mixer results in a large power consumption and bulky area, making this transmitter architecture unsuitable for IoT and sensor applications.

The third architecture is the PLL based transmitter shown in Figure 1.5. A $\Delta\Sigma$ Fractional-*N* (Frac-*N*) PLL performs modulation, frequency translation, and upconversion, all in one block. Information, in the form of binary bits, is applied to a digital $\Delta\Sigma$ modulator ($\Delta\Sigma$M) which in turn modulates the output frequency of the PLL through a Multi-Modulus Divider (MMD). The Phase-Frequency Detector (PFD), Charge Pump (CP), and Loop Filter (LF) compare and condition the reference and divider phase difference. When the loop is closed and the PLL is locked, the VCO outputs an RF frequency dictated by the digital information. Therefore, frequency and phase modulation can simply be performed with a PLL based transmitter by altering the $\Delta\Sigma$M divide value.

Table 1.2: Comparison of transmitter architectures

TX Type	Power	Area	Complexity	Major Concerns
Direct conversion	Low	Medium	Low	Frequency pulling
Dual conversion	High	High	High	Complex filtering needed
PLL based	Low	Low	Medium	PLL design can be complex

Because the PLL now performs the entire transmitter functions all in one block, several trade-offs arise that often complicate the design of PLL-based transmitters. For instance, a small PLL bandwidth is typically desired to achieve low integrated phase noise. However, low PLL bandwidth reduces the maximum modulation rate which limits the communication data rate. Therefore, circuit and system techniques are typically used to break this trade-off. One popular approach is to use a fast reference to reduce he $\Delta\Sigma$M quantization noise (which allows increasing the PLL bandwith without a phase noise penalty). However, reference multipliers can be complex, power hungry, and bulky. Therefore, new techniques to generate a fast reference can dramatically improve the performance, lower the power consumption, and reduce the area of PLL-based transmitters.

PLL based transmitters lend themselves nicely to the constant envelope modulation schemes that are widely used in IoT systems. It is important to note that several analog blocks such as DACs, mixers, and bandpass filters are eliminated. In addition to improving the area, the elimination of the analog circuits results in a simpler transmitter which leads to a low power consumption. It is for these reasons that a PLL based transmitter is the architecture of choice in this work.

Table 1.2 compares the three common transmitter architectures in terms of power, area, and design requirements.

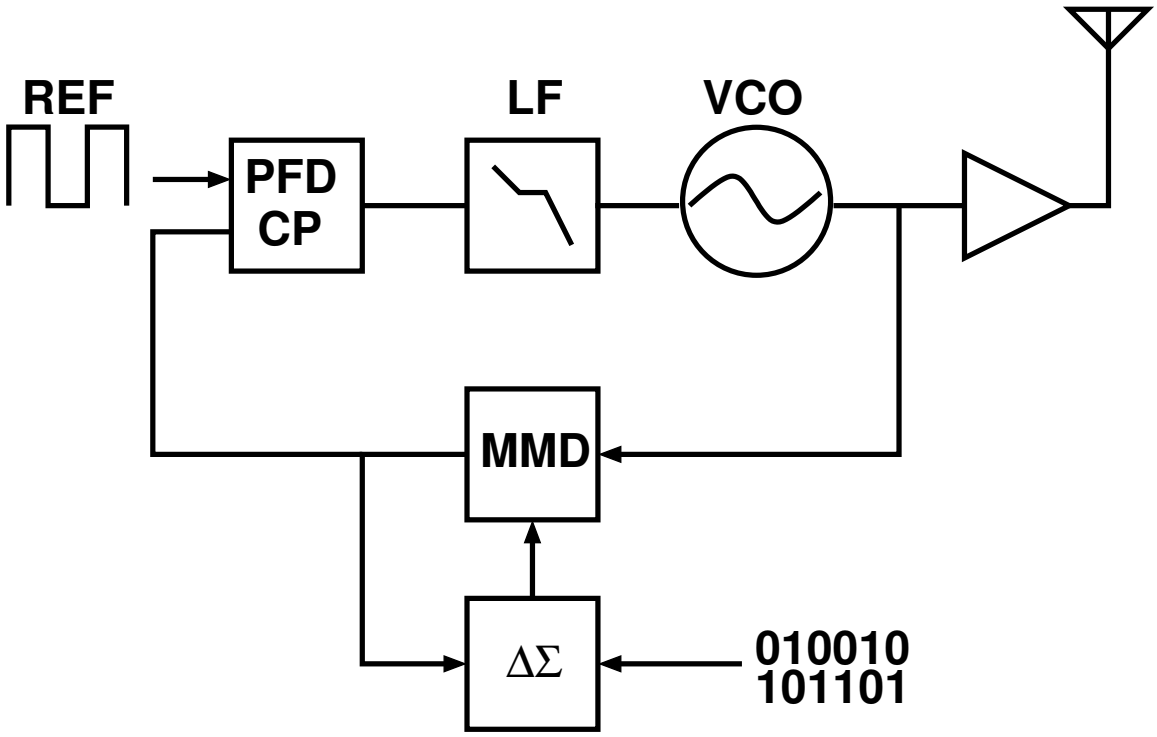

Figure 1.5: A generic PLL-based transmitter

1.4 PLL Based Transmitters

A PLL based transmitter is an ideal candidate for wireless IoT and sensor network devices as the simplicity of this architecture results in small area and low power consumption. Within the PLL based transmitter design space, there are two options available 1) An analog PLL, and 2) A Digital PLL (DPLL)[3].

Figure 1.6 shows a generic fractional-*N* analog PLL [18]. The PFD acts as the summing node in the feedback loop where it compares the phase of the reference and the divider and generates an error signal that is proportional to the phase difference. The charge pump

[3]There are several acronyms and names used for a digital PLL such as All Digital PLL (ADPLL), digital-dominant PLL, and digitally-assisted PLL. In the author's opinion, digital PLL is a misnomer since both the input and output, as well as several building blocks of an "ADPLL" are still analog. What we mean by a digital PLL is that the Proportional-Integral (PI) controller in the PLL is in the digital domain, *i.e.,* the charge pump and loop filter are replaced by digital equivalents. We will refer to this type of PLL as a DPLL throughout the thesis.

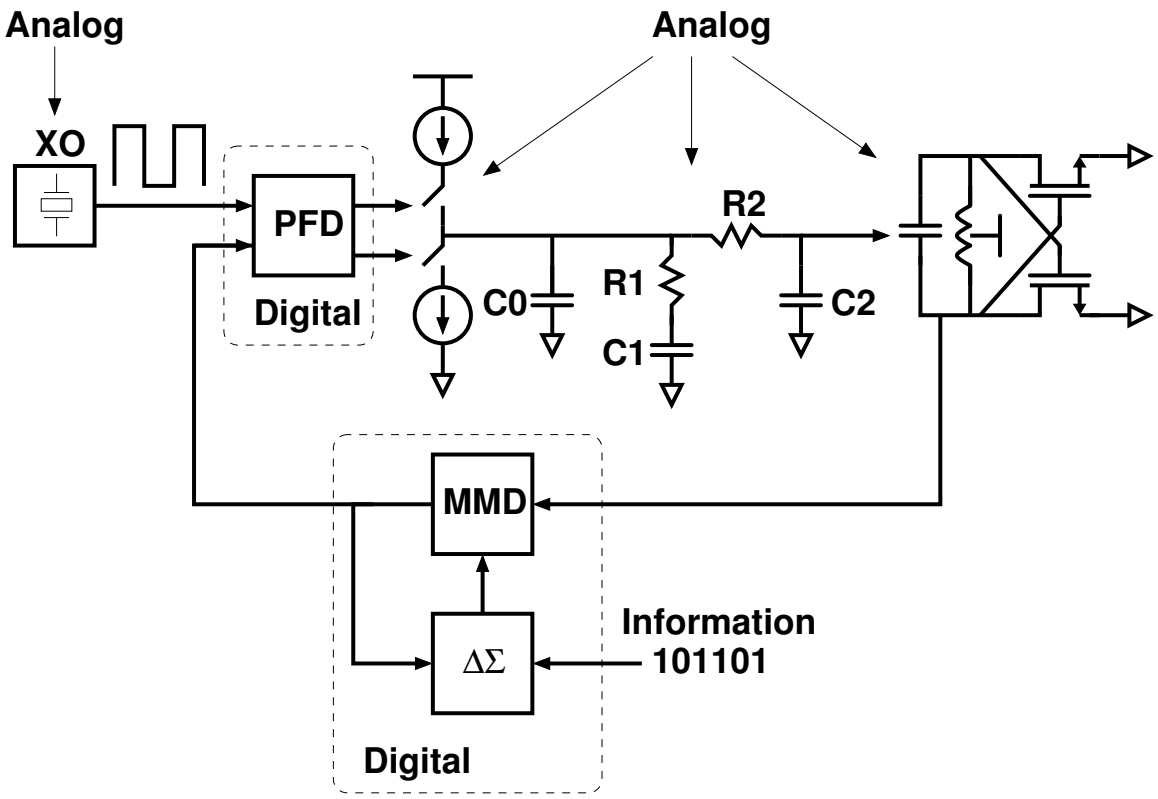

Figure 1.6: A common type-II analog PLL that is popular in PLL based transmitters

(proportional controller) gains up the PFD output and converts the error signal to the current domain. The loop filter, comprised of passive components C_0 (integrator capacitor), R_1 C_1 (which form the first pole-zero pair), and R_2 C_2 (which form the second pole, usually to attenuate the VCO control voltage ripple), converts the charge pump current to voltage. The loop filter also stabilizes the feedback loop (loop filter is essentially a lead lag compensator). The loop filter output is applied to a VCO (via a varactor) to generate the RF phase/frequency modulated signal. Typically, an *LC* VCO which has low phase noise is used to meet EVM requirements. A fractional divider, formed by a digital $\Delta\Sigma$ modulator and a multi modulus divider, is placed in the feedback loop. By dynamically changing the division ratio, a fractional divider is used to achieve both phase and frequency modulation. This is because the PLL output phase/frequency and the reference phase/frequency are related by the division

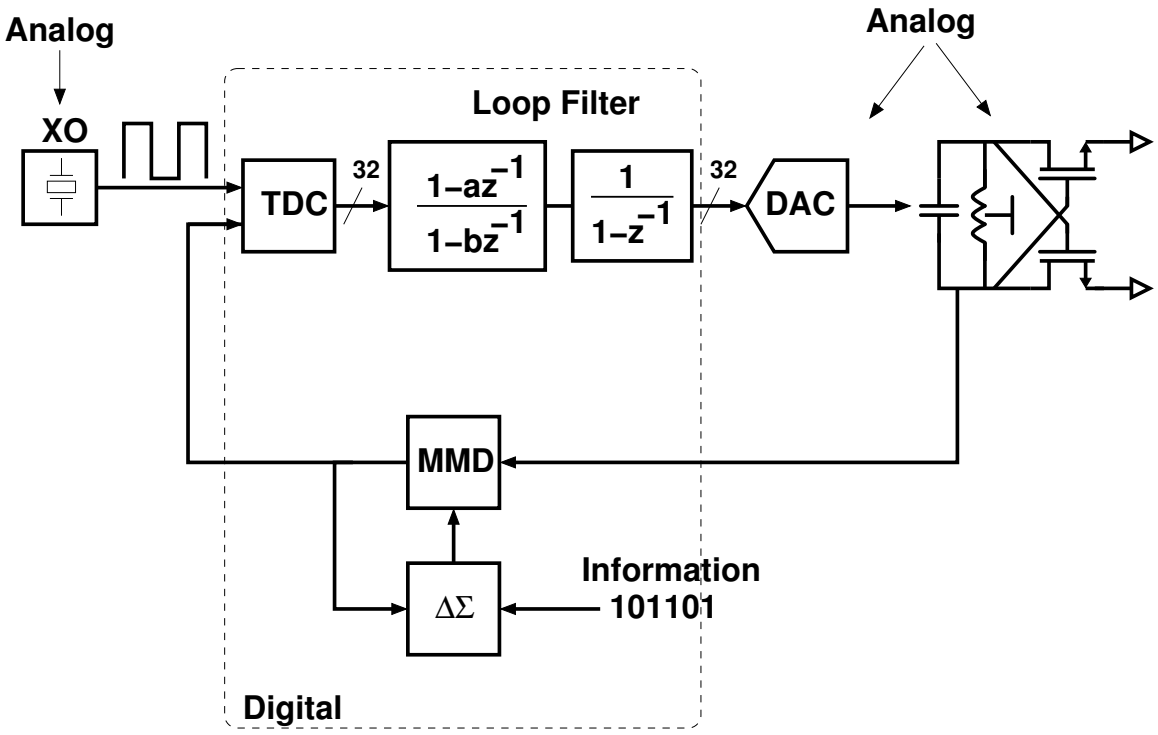

Figure 1.7: A digital PLL that is common in RF transmitters

ratio, N (*i.e.,* $F_{PLL}(t) = N(t) \times F_{REF}$ and $\phi_{PLL}(t) = N(t) \times \phi_{REF}$).

1.4.1 Digital PLL Based Transmitters

A schematic of a typical digital PLL is shown in Figure 1.7. Since their introduction in 2003 [19], DPLLs have received ample attention in industry and academia. This is primarily because the more digital nature of a DPLL makes it an attractive architecture for use in a nanometer CMOS System-on-Chip (SoC). Analog building blocks such as charge pumps and loop filters pose design and verification challenges in modern technologies. This will add significant implementation cost in a high volume digital dominant environment of IoT devices.

A Time-to-Digital Converter (TDC) replaces the PFD in a DPLL. A TDC outputs a digital word (instead of an analog error signal) that is proportional to the phase difference

between the reference and divider. This digital word can readily be applied to a digital loop filter, which in this example is a simple single pole single zero Infinite Impulse Response (IIR) filter cascaded by an accumulator (equivalent of integrator in an analog PLL). The output of the digital loop filter needs to be applied to the VCO varactor. Typically, a DAC converts the loop filter output to an analog voltage that sets the varactor capacitance.

A DPLL architecture is chosen for the transmitter in this work for the following reasons: the charge pump used in an analog PLL suffers from output resistance variation with respect to Process, Voltage, and Temperature (PVT). Mismatch in up and down currents (which results in spurs and added phase noise) is also another impediment to using a charge pump. Both these effects are further pronounced in today's nanometer CMOS nodes since the supply voltage is as low as 1V. Improving the mismatch and output resistance of a charge pump results in large area and increased power consumption. This makes the charge pump an undesirable block in sensor network transmitters. The loop filter in an analog PLL is comprised of several passive components that can have large values (*e.g.,* 30-100kΩ for R_1, and 100pF for C_1). Therefore, using an analog passive loop filter results in a large area. In addition to a large area, the leakage current through the capacitors cause spurs thereby degrading the TX fidelity.

In contrast, DPLLs use a compact digital loop filter which is insensitive to leakage. Also, unlike analog PLLs, the power consumption and area of a digital loop filter improves with scaling. Another advantage is that adopting a DPLL makes possible the use of digital signal processing algorithms to improve the transmitter functions and features. However, using a digital PLL is not without challenges. Based on the DPLL architecture chosen, implementation of a linear high resolution TDC can be difficult and results in large area and

increased power consumption [20]. This will in turn degrade the already aggressive area and power budget of an IoT system. In addition, the quantization noise and added spurs of DPLLs usually result in an inferior phase noise compared to analog PLLs. Nevertheless, DPLLs are suitable candidates for IoT systems as the simple modulation schemes used in IoT standards result in a fairly relaxed EVM requirement.

It is important to note that even in a DPLL, there are still three analog blocks: a DAC, a Crystal Oscillator (XO) reference, and a VCO. A DAC is typically a simple circuit which can be designed to have low power consumption and small area. Therefore, it can be used in a low power, compact IoT system without much overhead.

The VCO is often a bulky block that consumes several milliWatts of power. In addition, most VCOs need a high supply voltage for safe startup which limits their use in a low voltage IoT environment. Therefore, a low voltage, low current VCO architecture is desirable for a wireless sensor network device.

It is imperative to note that an often neglected part of any PLL based transmitter (analog or digital) is the power and area dedicated to the reference path (clock generation) which includes the crystal oscillator and a reference multiplier (Figure 1.8). A crystal oscillator is an electronic oscillator circuit that uses the mechanical resonance of a vibrating crystal of piezoelectric material to create an electrical signal with a very precise frequency. In most modern SoCs, the XO active circuits (such as start up, tuning capacitors, and loss compensation) are placed on chip. On chip XO circuits typically operate from a large supply (*e.g.,* 1.8V). This is to isolate the supply voltage of sensitive RF circuits (which typically run from a 1.1V supply) from the large XO spurs that would otherwise exist if the supply was shared. Integrated XO circuits are bulky and consume milliWatts of power [21].

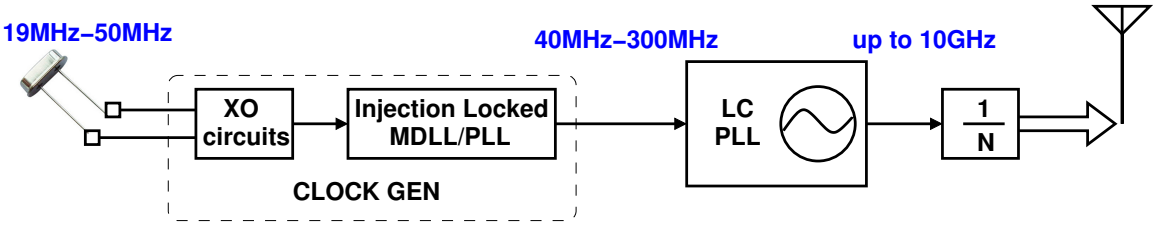

Figure 1.8: A modern high performance PLL based transmitter

Table 1.3: Comparison of analog and digital PLLs

Analog PLL	**Digital PLL**
Large area	Compact
No benefit from scaling	Improves with scaling
Excellent phase noise	Moderate phase noise
Charge pump problems	Free of charge pump
Bulky and leakage prone loop filter	Digital loop filter
Little benefit from DSP	DSP used to improve performance/features

Furthermore, the design of PVT insensitive injection locked reference multipliers is complex which results in a large power and area penalty [22]. Therefore, reducing the supply voltage and power consumption of the crystal oscillator, as well as improving the performance of the XO and reference generation circuits has an immense impact on the overall power and area of a PLL based transmitter.

In summary, the difficultly of implementing traditional analog circuits, and the many opportunities, such as compact filters and digitally assisted analog circuits, presented by DPLLs in low supply nanometer CMOS processes makes DPLL the architecture of choice in this work. Table 1.3 outlines the typical tradeoffs between analog and digital PLLs.

1.5 Thesis Contributions

New techniques proposed in this thesis dramatically reduce the power consumption, shrink the area, and also improve the performance of PLL based transmitters.

The main contributions of this work are three fold:

A 192MHz Differential XO Based Frequency Quadrupler with Sub-Picosecond Jitter in 28nm CMOS

A low jitter 192MHz crystal reference quadrupler leverages a new active inductor based 48MHz differential XO, two skewed inverters, a new duty cycle correction circuit, and a frequency doubler. The 192MHz quadrupler can serve as a fast, low jitter reference for a low phase noise PLL and requires far less power and area than reference multiplying PLL or MDLL circuits. The measured RMS jitter is 168fs for the XO, and 184fs for 96MHz output (192MHz divide by 2). The entire circuit, including the XO, draws 5.5mA from a 1V supply and occupies 0.045mm^2. To our best knowledge, this is the first reference frequency quadrupler with sub-picosecond jitter.

A Low Voltage Sub 300μW 2.5GHz Current Reuse VCO

The two transistor CMOS current reuse VCO is modified with the addition of an AC coupling capacitor to reduce the supply voltage and achieve good phase noise with very low power consumption. A 2.17GHz to 2.9GHz prototype VCO operates with a supply voltage as low as 0.6V. At 2.53GHz, with a 0.7V supply and a 185μW power consumption, the measured phase noise at 3MHz offset is -122.6dBc/Hz and varies by only 2.2dB over a temperature range from -30 to 120°C. For a 0.85V supply, phase noise is improved to -126.1dBc/Hz with a 280μW power consumption which corresponds to a Figure of Merit (FoM) of 190.2dB. This is the lowest reported power

consumption and supply voltage for any current reuse VCO[4]. Fabricated in 65nm CMOS, the prototype occupies 0.13mm^2 [23].

A 2.4GHz 2Mb/s Digital PLL-based Transmitter for 802.15.4 in 130nm CMOS

A fully integrated 2.4GHz transmitter for 802.15.4 based on a digital ΣΔ fractional-*N* PLL is presented. A self calibrated two point modulation scheme enables modulation rates much larger than the loop bandwidth. An oversampled 1-bit quantizer is used as a phase detector, reducing spurs and nonlinearity associated with some TDC based digital PLLs. The prototype achieves an MSK modulation rate of 2Mb/s, delivers -2dBm of output power, and is free of in band fractional spurs. The transmitter, implemented in 130nm CMOS, consumes 17mW from a 1.2V supply and occupies an active area of 0.6mm^2 [24].

[4] As of the date of publication in [23].

CHAPTER II

A 192MHz Differential XO Based Frequency Quadrupler with Sub-Picosecond Jitter in 28nm CMOS

2.1 Introduction

High performance frequency synthesizers often use a multiple of the Crystal Oscillator (XO) frequency as a reference input to meet stringent phase noise requirements [25], [26], [22]. A high reference frequency reduces the fractional-*N* modulator quantization noise. Because high frequency crystal oscillators are expensive, it is preferable to more than double the XO frequency. However, the use of multiple frequency doublers in series is best avoided due to high jitter. For example, when two frequency doublers are used in series, both the rising and falling edges are corrupted by long delays and therefore have high jitter.

In LO frequency synthesizers with GHz range outputs, an injection locked integer-*N* PLL or Multiplying Delay-Locked-Loop (MDLL) reference multiplier is cascaded with an *LC* fractional-*N* PLL to achieve low phase noise [22]. Nevertheless, the power consumption and area of these reference multipliers is high because of the complexity needed for PVT insensitive reference injection, to achieve low jitter and spurs [22], [27]. Although the

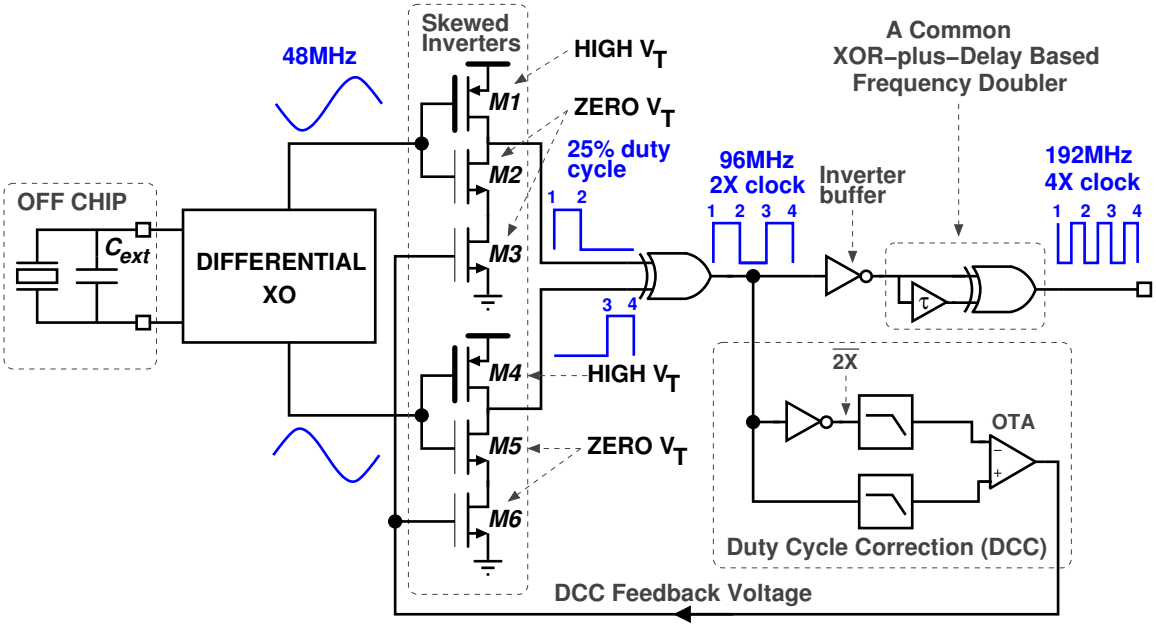

Figure 2.1: Differential XO based Frequency Quadrupler (F4Xer)

injection locked fractional-*N* MDLL in [28] has a 1.5GHz output, the use of a ring VCO means that the far offset phase noise is much worse than when a reference multiplier is cascaded with an *LC* PLL.

We introduce a new low power, compact differential XO that achieves a measured RMS jitter of 168fs. We also propose a new method to multiply the XO frequency by four with less than half the power consumption and less than a quarter of the area of conventional methods. This 192MHz quadrupler circuit achieves low edge jitter making it an ideal fast reference for low noise synthesizers.

2.2 Frequency Quadrupler Operation

Figure 2.1 shows the new differential XO based Frequency Quadrupler (F4Xer). A new active inductor based XO generates a 48MHz differential sinusoid. This work uses the differential XO outputs in a unique way to double the frequency. The differential XO outputs

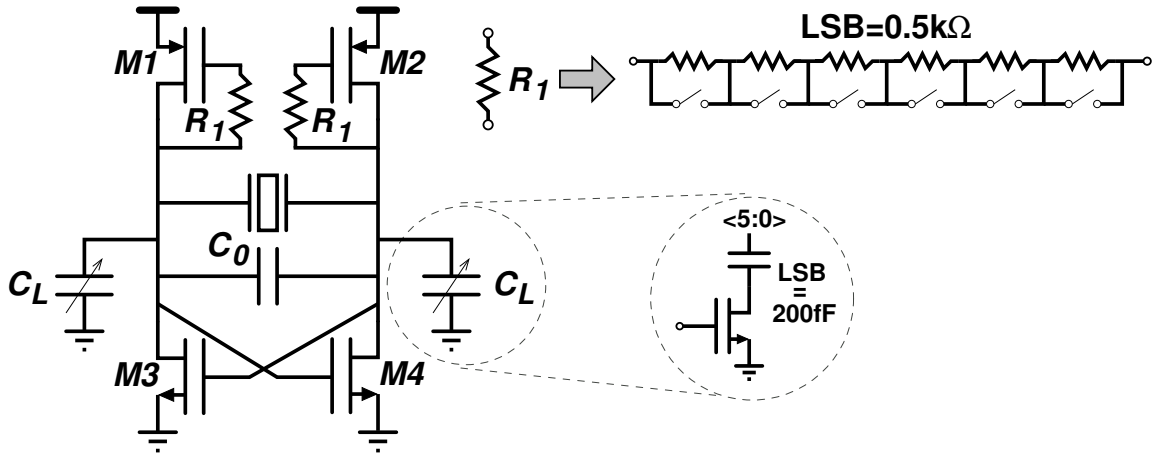

Figure 2.2: Active inductor based differential XO schematic

are fed to two skewed inverters, with thresholds adjusted by Duty-Cycle Correction (DCC) feedback, to produce two 25% duty cycle 48MHz square waves (*i.e.,* at the XO frequency). The two 25% duty cycle clocks are XORed to form a 50% duty cycle, 96MHz, 2X clock (*i.e.,* double the XO frequency). Both the rising and falling edges of the 2X clock have low jitter since they are directly generated from the XO outputs. It is important to note that this is unlike a standard frequency doubler where one edge per cycle is corrupted by a long delay. After an inverter buffer, a conventional XOR-plus-delay based frequency doubler generates a 192MHz, 4X clock. As seen in Figure 2.1, the 4X clock has one low jitter edge per cycle (directly from XO). Therefore, the 192MHz, 4X clock can serve as a clean reference in any edge-triggered system such as a PFD or PD based PLL or DLL.

2.3 Differential Crystal Oscillator

Figure 2.2 shows the new differential XO circuit. Compared to single-ended XOs, differential XOs have several advantages such as reduced spurs and better Power Supply Rejection (PSR) [29]. A differential cross-coupled oscillator circuit cannot be used because

when a crystal replaces the *LC* tank, the circuit latches up due to the lack of a low impedance DC path. The differential XO in [29] solves this latch-up problem by AC coupling the cross-coupled transistors. However, this method is susceptible to noise injection since a separate DC voltage biases the cross coupled pair in the XO core. Furthermore, it requires a large die area to reduce the noise of this on-chip DC bias voltage.

Instead, we introduce a low power, compact active inductor to provide a low impedance DC path and prevent latch up. Two single ended active inductors are formed by placing a resistor, R_1, between the gate and drain of diode-connected transistors, M1 and M2. Cross-coupled transistors, M3 and M4, provide negative resistance to sustain XO oscillation. C_L, a programmable 6-bit binary capacitor bank with an LSB of 200fF, is placed on both sides of the XO for fine tuning. C_0 is a 10pF off chip capacitor for XO coarse tuning. Resistor R_1, used in the active inductor, is a programmable 6 bit binary weighted resistor with an LSB of 0.5kΩ.

2.4 Duty Cycle Correction Operation

Two offset 25% duty cycle clocks at the XO frequency are XORed to form the 50% duty cycle 2X clock. The duty cycle of this 96MHz, 2X clock must be 50% as both its rising and falling edges are used to generate the clean edges of the 192MHz, 4X clock (Fig. 2.1). The new DCC circuit ensures the generation of the 25% duty cycle 1X clocks so that when these are combined, the duty cycle of the 96MHz, 2X clock is 50%. The DCC feedback loop forces the average (*i.e.,* DC component) of the 96MHz, 2X clock and its inverse, $\overline{2X}$ (formed by an extra inverter) to be the same to achieve a 50% duty cycle. Two RC Low Pass (LP)

filters extract the DC of 2X and $\overline{2X}$ clocks. The DCC uses a folded cascode Operational Trans-conductance Amplifier (OTA) as an error amplifier to generate a feedback voltage based on DC values of 2X and $\overline{2X}$. This feedback voltage sets the switching thresholds of the skewed inverters so that the duty cycle of both 1X clocks is 25%. The switching threshold is set by applying the DCC feedback voltage to the gates of zero V_T NMOS transistors, M3 and M6, at the bottom of the skewed inverters. The RC LP filters set the dominant pole of the DCC loop in the kHz range for easy stability.

This differential method of duty cycle correction, based on comparing DC values, does not require a precise bias voltage and is insensitive to PVT. The switching threshold of each skewed inverter is set below $V_{DD}/2$ by using high V_T PMOS transistors, M1 and M4, and zero V_T NMOS transistors, M2 and M5 (Fig. 2.1). The skewed inverters are sized large to reduce noise. The large size, in addition to a symmetric layout, yields good matching. The input stage of OTA is sized large to reduce the DC offset which manifests itself as a static duty cycle error. The DCC operation is unaffected by the extra inverter delay in the $\overline{2X}$ path since the DC value of $\overline{2X}$ remains unchanged.

2.5 XO Design Considerations

Figure 2.3 shows the small signal model for the differential XO. The crystal is modelled as a series RLC network with motion inductance L_x, motion capacitance C_{x1}, and equivalent series resistance R_x, in shunt with parasitic capacitance C_{x2}. $C_L/2$ is the equivalent series combination of on-chip fine tune capacitors. The impedance of the cross coupled pair, Z_{CC}, is $-2/g_{m_{3,4}}$ at low frequency. The active inductor small signal impedance, Z_{active_L}, has a

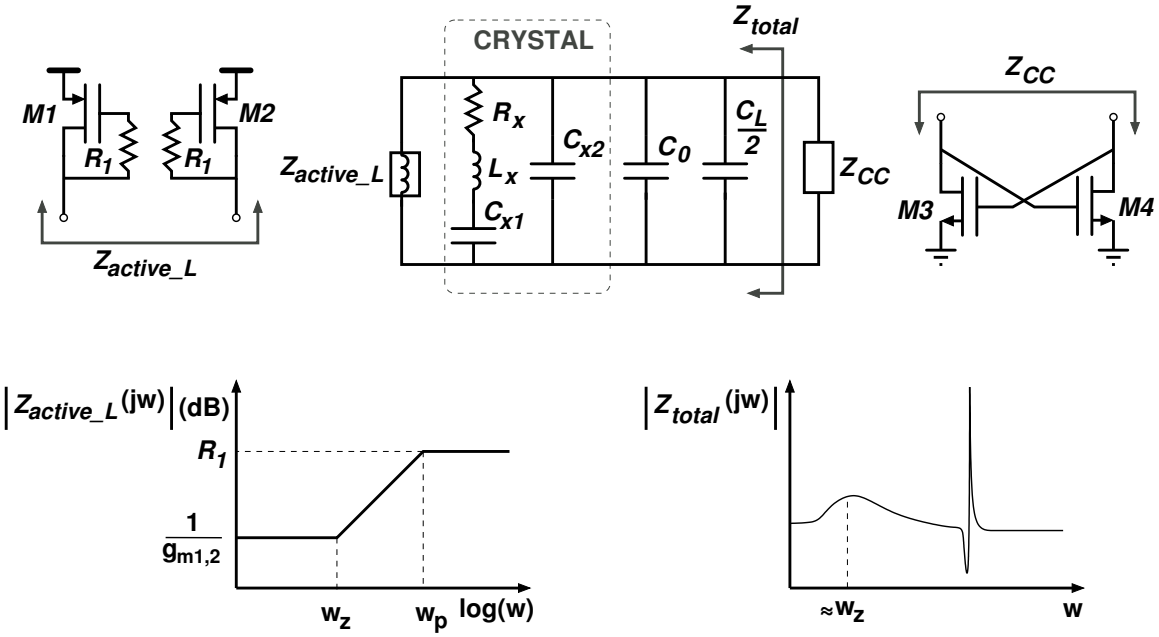

Figure 2.3: Differential XO small signal model, magnitude of active inductor impedance (Z_{active_L}), and combined impedance (Z_{total})

zero at $\omega_z = 1/R_1 C_{gs_{1,2}}$ and a pole at $\omega_p = g_{m_{1,2}}/C_{gs_{1,2}}$. Z_{total} is the combined impedance of crystal and active inductor.

As shown in the magnitude plot of Z_{active_L} vs frequency in Figure 2.3, the low frequency impedance of the active inductor is $1/g_{m_{1,2}}$ and the high frequency impedance is R_1. M1 and M2 are sized large to achieve low impedance at DC to avoid latch up (*i.e.,* DC loop gain less than 1). The active inductor impedance increases with frequency, and this affects the total impedance as shown in the plot of Z_{total} in Figure 2.3. The R_1 value of the active inductor is judiciously chosen to 1) avoid crystal loading at oscillation frequency and 2) set ω_z to prevent oscillation at any frequency other than crystal's high Q, parallel resonance frequency (*i.e.,* avoids large loop gain at any frequency other than crystal's oscillation frequency).

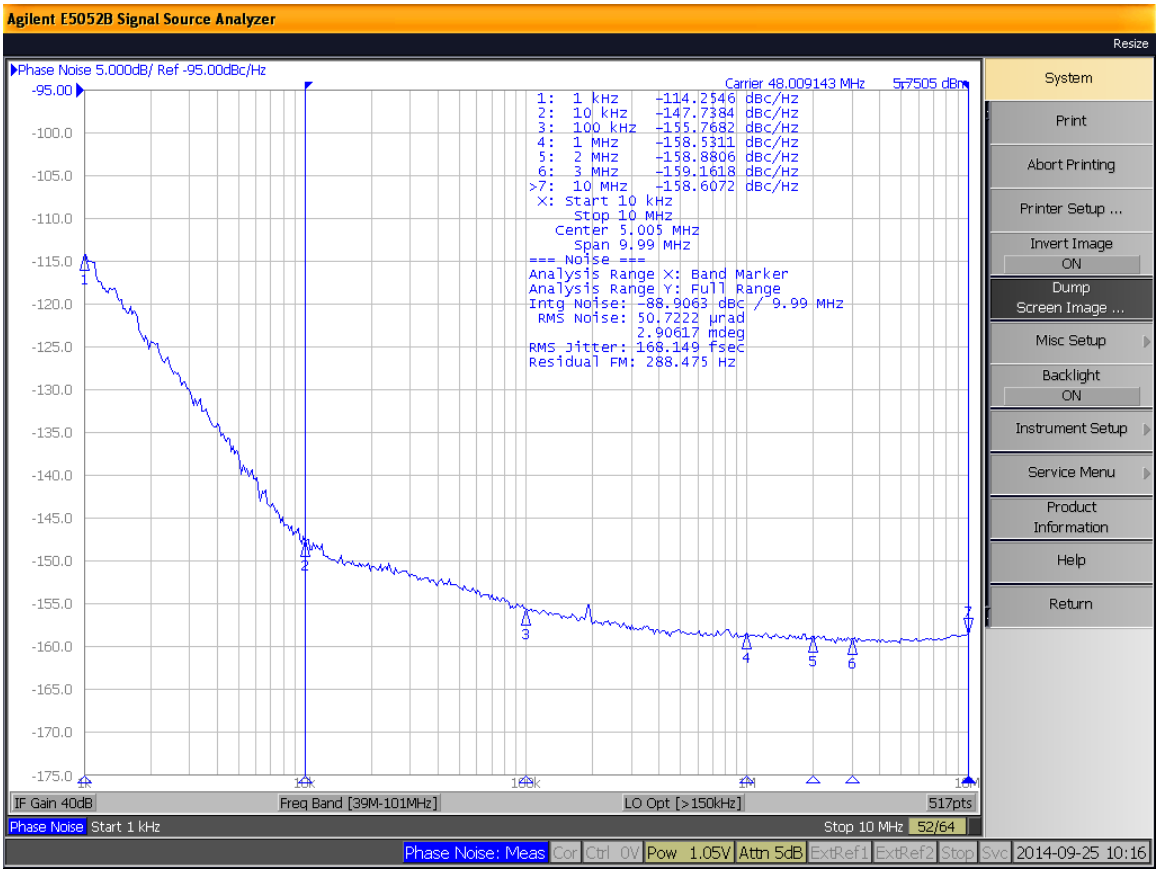

Figure 2.4: Measured phase noise of the new active inductor based 48MHz differential XO using 5052B signal source analyzer

2.6 Measurement Results

Figure 2.4 shows the measured phase noise of the 48MHz differential XO signal using an Agilent 5052B signal analyzer. The RMS jitter, measured over an integration bandwidth from 10kHz to 10MHz, is only 168.1fs. The measured phase noise is -147.7dBc/Hz, -155.8dBc/Hz, and -158.5dBc/Hz at 10kHz, 100kHz, and 1MHz offsets, respectively. Figure 2.5 shows the measured phase noise of 96MHz clock (the input to final doubler). The measured RMS jitter is 183.6fs. The phase noise of the 192MHz, 4X clock cannot be directly measured using a signal source analyzer because one edge per cycle is noisy due to

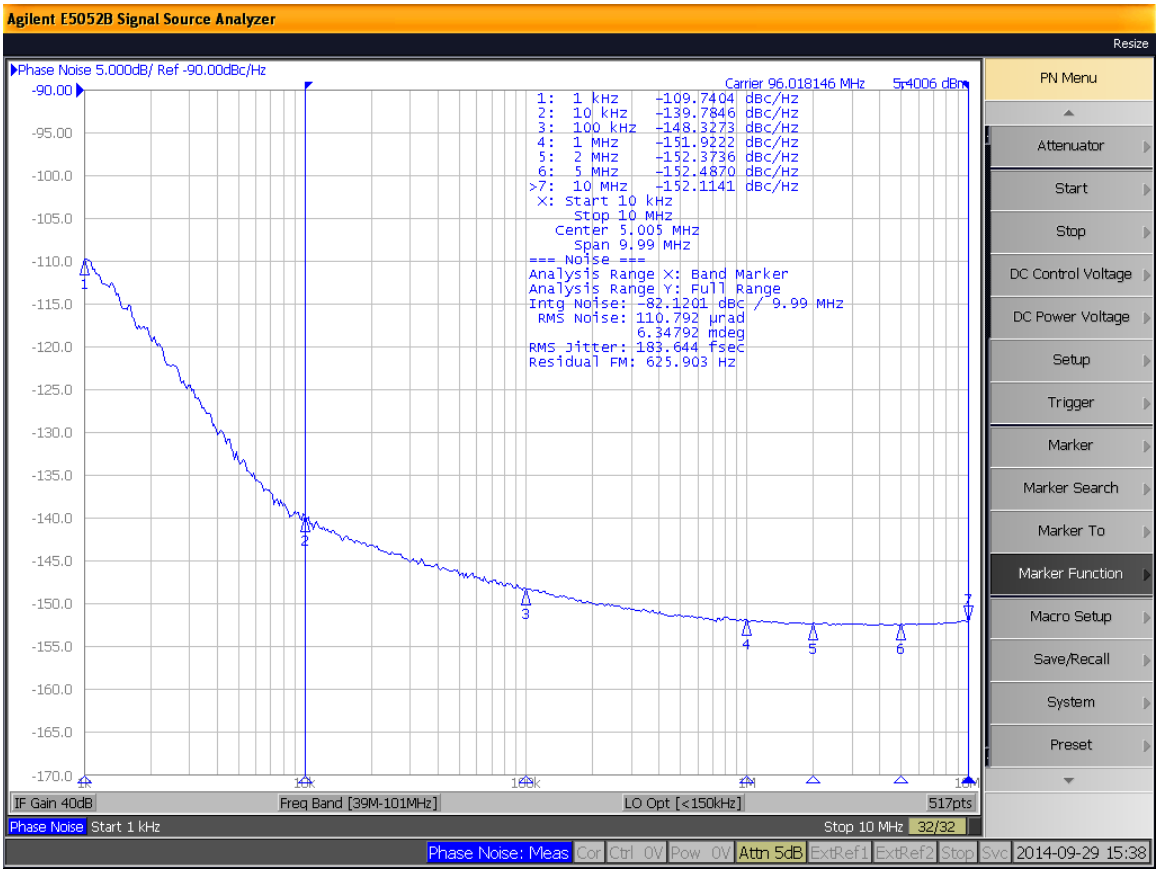

Figure 2.5: Measured phase noise of 96MHz clock (double of XO and input to final doubler) using 5052B signal source analyzer

the delay in final doubler [22] (most clock inputs are edge- triggered and require one low jitter edge). The last stage XOR-plus-delay based frequency doubler adds little phase noise [17] since the low jitter edges of the 192MHz, 4X clock are merely buffered versions of the rail-to-rail 96MHz, 2X clock edges which have low measured phase noise. Figure 2.6 shows a scope capture of the differential waveforms at the XO I/O pins, measured with an active probe. Figure 2.7 shows a scope capture of the 96MHz, 2X clock with a measured duty cycle of 50% with DCC enabled. Figure 2.8 captures the 192MHz, 4X clock that is generated from the 96MHz, 50% duty cycle 2X clock. The rising and falling edges of 2X clock are used to generate a 192MHz, 4X clock with clean falling edges. Figure 2.9 compares the

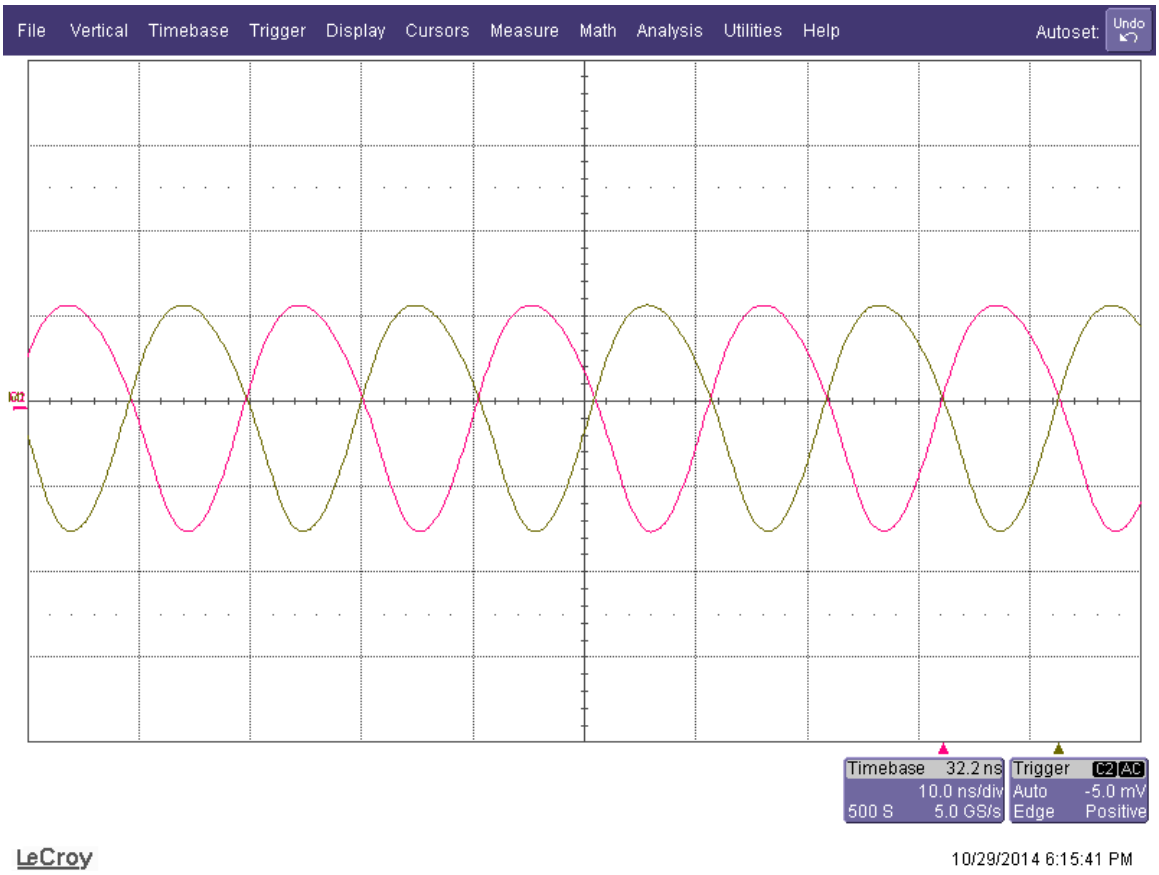

Figure 2.6: Measured 48MHz differential XO waveform probed at XO I/O pins

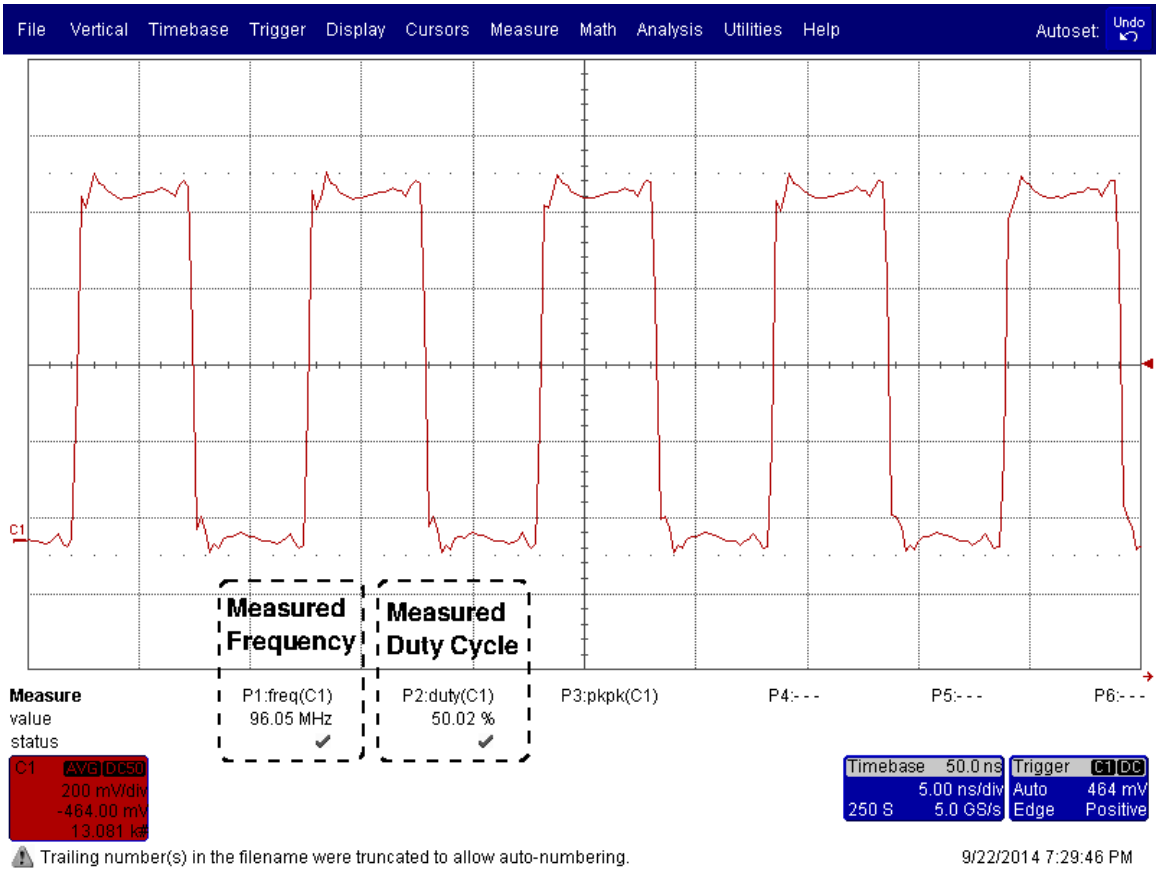

Figure 2.7: Measured 96MHz, 50% duty cycle 2X clock with DCC enabled

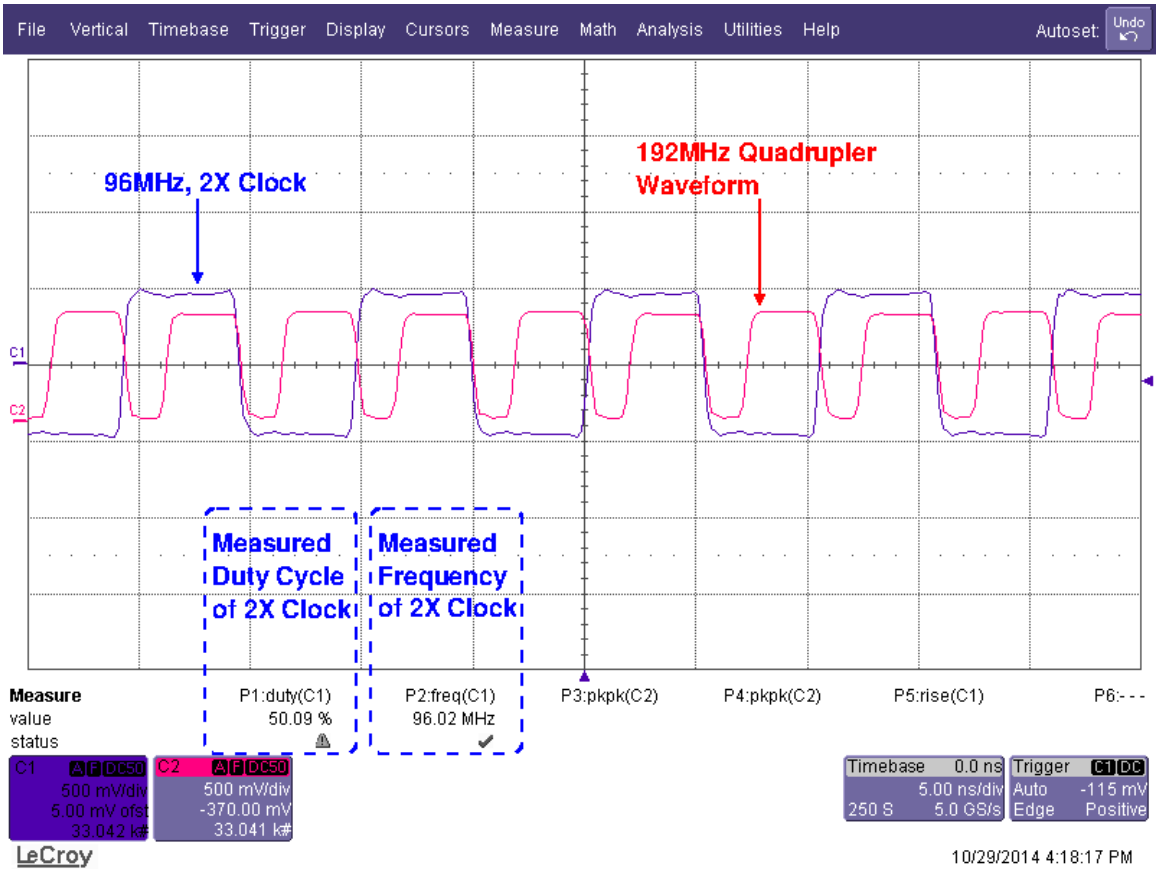

Figure 2.8: Measured 192MHz quadrupler waveform (red) generated from the 50% duty cycle 96MHz, 2X clock (blue)

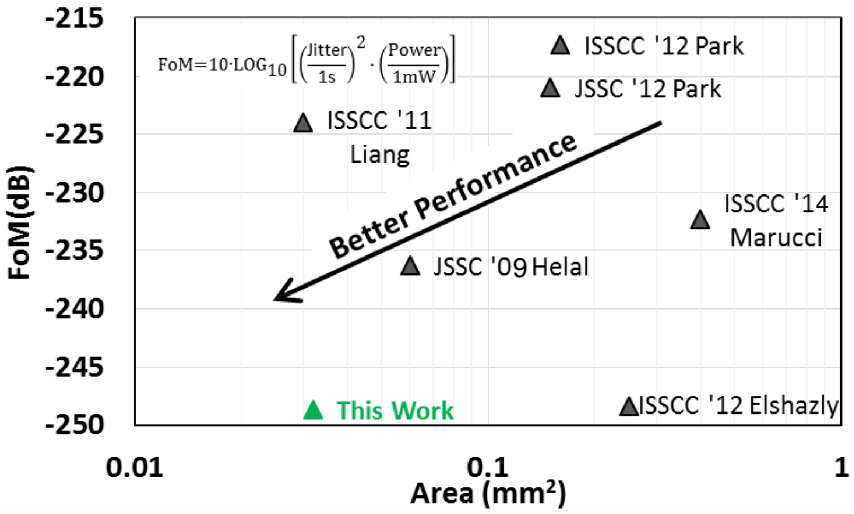

Figure 2.9: Frequency quadrupler FoM vs active area comparison [3], [4], [5]

F4Xer FoM vs area. Figure 2.10 shows the die photo. The entire circuit, including the XO, occupies an active area of 0.045mm^2. Table 2.1 summarizes the performance of differential XO and compares with recent work. Table 2.2 outlines the F4Xer measured results.

2.7 Analysis

In this section, the theoretical analysis and detailed design considerations for the new differential crystal oscillator are outlined. The differential crystal oscillator of Figure 2.2 is re-drawn[1] as shown in Figure 2.11.

As shown in Fig. 2.12, the crystal is modeled as a series *RLC* equivalent circuit (referred to as the motional arm) where R_1, L_1, and C_1 are the motional resistance, inductance, and capacitance, respectively; in parallel with a static capacitance, C_0. The motional resistance, R_1, represents the loss in the crystal. The static capacitance, C_0, is the measured capacitance associated with the crystal, its electrodes, and the stray capacitance internal to the crystal

[1]Component names are changed to make the theoretical analysis easier to follow.

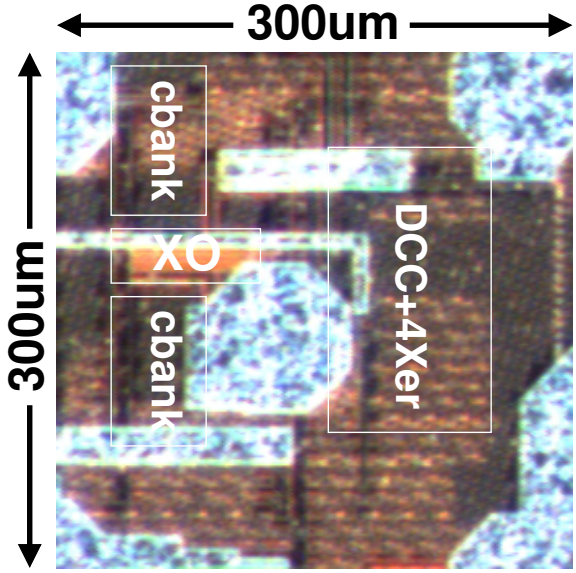

Figure 2.10: Die photo including 50Ω o/p buffers, ESD, and bypass caps. The XO and F4Xer total active area is 0.045mm^2

Table 2.1: Differential XO summary and comparison

Parameter	**This Work**	JSSC'12 [29]	RFIC'10 [21]
Differential?	**Yes**	Yes	No
CMOS tech.	**28nm**	65nm	65nm
Power (mW)	**1.5**	2.16	7
Supply voltage (V)	**1**	1.8	1.4
Active area (mm^2)	**0.0133**	0.15†	0.09
Crystal freq. (MHz)	**48**	26	38.4
Phase noise (dBc/Hz) @ 10kHz	**-147.7**	-146.4*	-144*
Phase noise (dBc/Hz) @ 100kHz	**-155.8**	-150.7*	–
Phase noise (dBc/Hz) @ 1MHz	**-158.5**	-151.3*	–
RMS jitter (fS) 10kHz-10MHz BW	**168**	420‡	–
Tuning range (ppm)	±35	±45	280
Avg. tuning step (ppm)	**1**	0.005	0.002

*Referred to 48MHz for fair comparison

†Includes coarse tuning capacitors

‡10kHz to 5MHz integration bandwidth

Table 2.2: Frequency quadrupler results summary

Technology	28nm CMOS	
Total power (mW)	5.5	
Supply voltage (V)	1	
Current (mA)	Total XO F4Xer	5.5 1.5 4
Active area (mm^2)	Total XO F4Xer	0.045 0.013 0.032
Phase noise (dBc/Hz)†	10kHz 100kHz 1MHz	-139.8 -148.3 -151.9
RMS jitter†(fS)	183.6	
96MHz 2X clock duty cycle(%)	50	

†Measured @ 96MHz (quadrupler divide by 2)

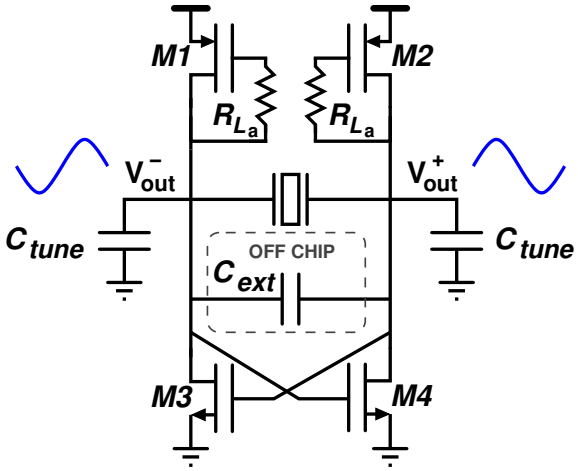

Figure 2.11: Differential crystal oscillator schematic

enclosure. The equivalent circuit model is specified in a datasheet by the crystal manufacturer. If we define $Z_0 = 1/j\omega C_0$, and $Z_1 = R_1 + jwL_1 + 1/j\omega C_1$, then the impedance of crystal is obtained as

$$Z_{xtal} = \frac{Z_1 Z_0}{Z_1 + Z_0}. \tag{2.1}$$

Even though the crystal equivalent circuit results in both a series resonance and a parallel resonance, the crystal is typically used in the parallel resonance region with the resonance frequency given by:

$$\omega_{r_p} \approx \frac{1}{\sqrt{L_1 C_1}} \left(1 + \frac{C_1}{2\,(C_0 + C_L)}\right). \tag{2.2}$$

Capacitor C_L, specified by the manufacturer, is the total capacitance that is to be presented to the crystal for oscillation in the parallel-resonance mode[2]. At frequencies much below resonance, the crystal impedance is capacitive with impedance, $Z_{xtal}(\omega \ll \omega_{r_p}) \approx 1/j\omega C_0$. The crystal, however, becomes inductive in a certain frequency range called the parallel-resonance region. The parallel-resonance region is where frequency is between $1/\sqrt{L_1 C_1}$ (also known as the series resonance frequency, ω_{r_s}) and ω_{r_p}. In this region, the crystal is modeled by an inductor, L_e, in series with a resistor, R_e. This region is important since most on-chip crystal oscillators are designed to oscillate in the parallel-resonance mode. The equivalent series impedance in parallel region is be used later in the differential crystal oscillator loop gain analysis. An equivalent circuit model for the crystal in different operation regions is shown in Figure 2.12.

The overall small signal model of the XO is shown in Figure 2.13. The impedance of

[2]It is important to note that C_L is different from the physical external capacitor, C_{ext}, placed across the crystal. Rather, C_L, is C_{ext} plus the sum of capacitances (including, for example, the crystal buffer input capacitance) across the crystal.

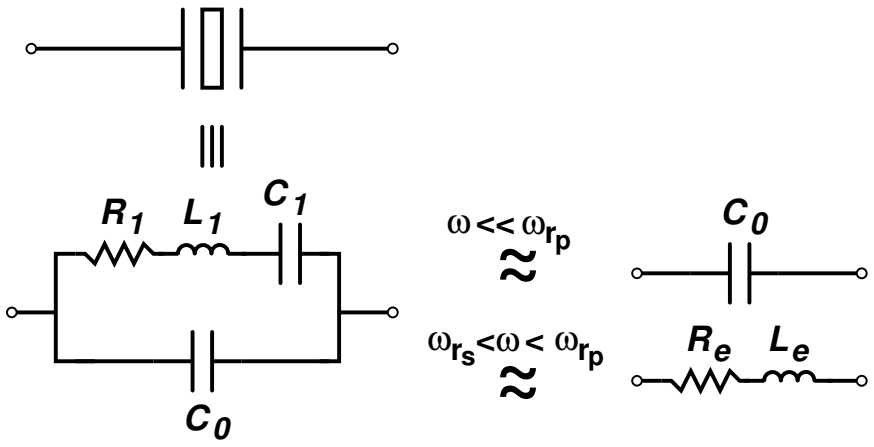

Figure 2.12: Equivalent circuit model for a crystal together with circuit model for different operation regions

the active inductor in Figure 2.13 is obtained as

$$Z_{L_a}(\omega) = \frac{2}{g_{m_p}} \frac{1 + j\omega/\omega_z}{1 + j\omega/\omega_p}, \tag{2.3}$$

where $\omega_z = -1/R_{L_a} C_{gg_p}$, and $\omega_p = -g_{m_p}/C_{gg_p}$. The pole frequency, ω_p, is equivalent to PMOS transit frequency, ω_{T_p}.

The impedance of cross-coupled pair in Figure 2.13 is given by

$$Z_{cc}(\omega) = \frac{-2}{g_{m_n}} \frac{1}{1 - j\omega/\omega_p}, \tag{2.4}$$

where $\omega_p = g_{m_n}/C_{gg_n}$. The pole frequency, ω_p, is equivalent to NMOS transit frequency, ω_{T_n}.

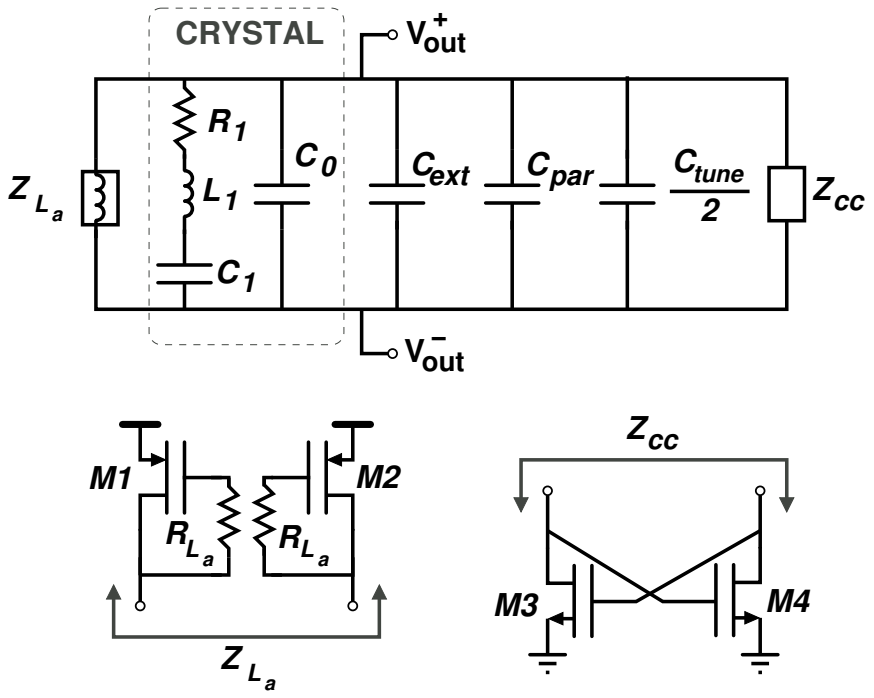

Figure 2.13: Small signal model of the differential crystal oscillator

2.7.1 Crystal Oscillator Small Signal Analysis for $\omega \ll \omega_{r_p}$

We first begin by looking at the total admittance, Y_t, at frequencies much below the resonance (*i.e.,* $\omega \ll \omega_{r_p}$). This analysis is later used to outline a set of design considerations to avoid parasitic oscillation (*i.e.,* oscillation at any frequency other than the desired frequency).

Using the crystal equivalent circuit for $\omega \ll \omega_{r_p}$ (Figure 2.12), the XO small signal model is re-drawn as shown in Figure 2.14. Using this small signal model, $\mathrm{Im}\{Y_t\}$, is obtained as

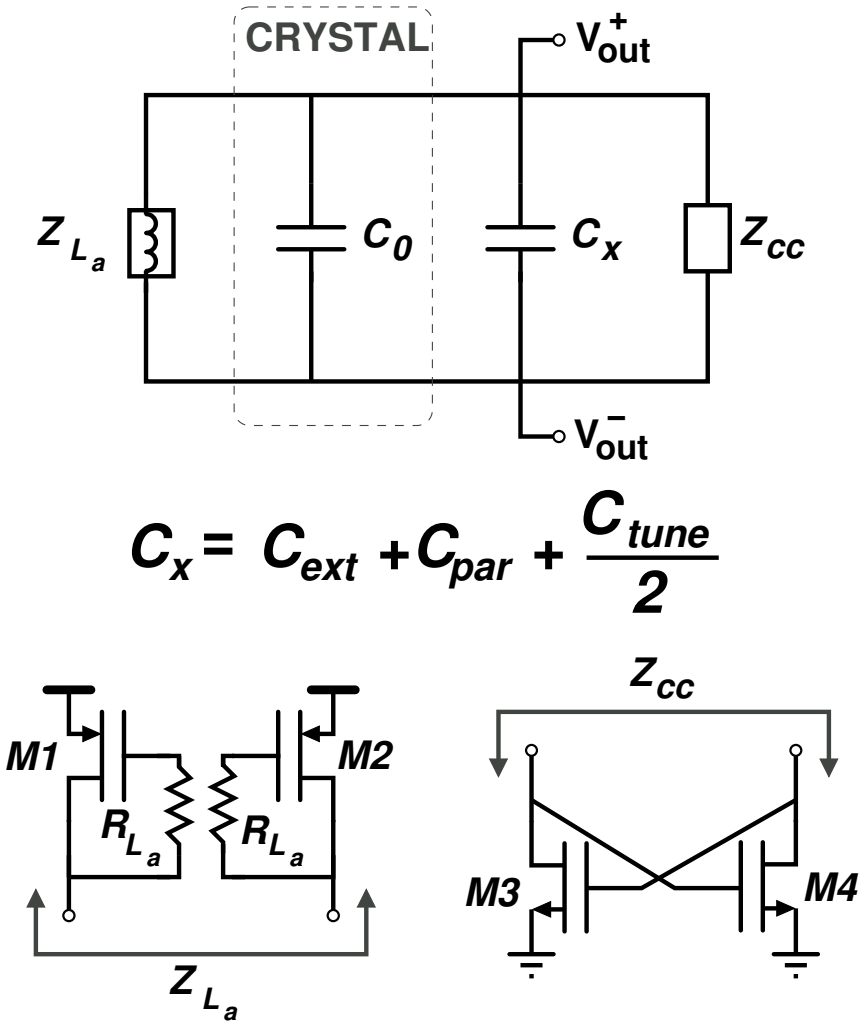

Figure 2.14: Small signal model of differential crystal oscillator for $\omega \ll \omega_{r_p}$

$$\begin{aligned}\mathrm{Im}\{Y_t\}(\omega)|_{\omega\ll\omega_{r_p}} = \frac{\omega}{2\omega_{T_n}\omega_{T_p}\left(\omega^2+\omega_z^2\right)}\Big[&\omega^2\left(g_{m_n}\omega_{T_p}+2\omega_{T_p}\omega_{T_n}(C_0+C_x)\right)\\&+g_{m_p}\omega_{T_n}\omega_z^2+g_{m_n}\omega_{T_p}\omega_z^2\\&-g_{m_p}\omega_{T_p}\omega_{T_n}\omega_z\\&+2\omega_{T_p}\omega_{T_n}\omega_z^2(C_0+C_x)\Big],\end{aligned} \tag{2.5}$$

and $\mathrm{Re}\{Y_t\}$ is obtained as

$$\begin{aligned}\mathrm{Re}\{Y_t\}(\omega)|_{\omega\ll\omega_{r_p}} = \frac{\omega^2}{2\omega_{T_p}\left(\omega^2+\omega_z^2\right)}\Big[&(g_{m_p}\omega_z-g_{m_n}\omega_{T_p})\\&+g_{m_p}\omega_{T_p}\omega_z^2-g_{m_n}\omega_{T_p}\omega_z^2\Big].\end{aligned} \tag{2.6}$$

It is important to note that the denominators in Equation 2.5 and Equation 2.6 are always positive. Therefore, they are omitted from the analysis as they have no effect on the sign of $\mathrm{Re}\{Y_t\}$ and $\mathrm{Im}\{Y_t\}$. We define

$$C_x \triangleq C_{ext}+C_{par}+\frac{C_{tune}}{2}, \tag{2.7}$$

where C_{ext} is the external capacitor placed across the Crystal (XTAL), and C_{par} is the equivalent parasitic capacitor across the crystal I/O pins, *e.g.,* including the XO buffer input capacitance[3]. $C_{tune}/2$ is the series combination of on-chip tuning capacitors.

[3]It is important to note that active inductor and cross-coupled pair capacitances are already accounted for in Equation 2.3 and Equation 2.4, respectively.

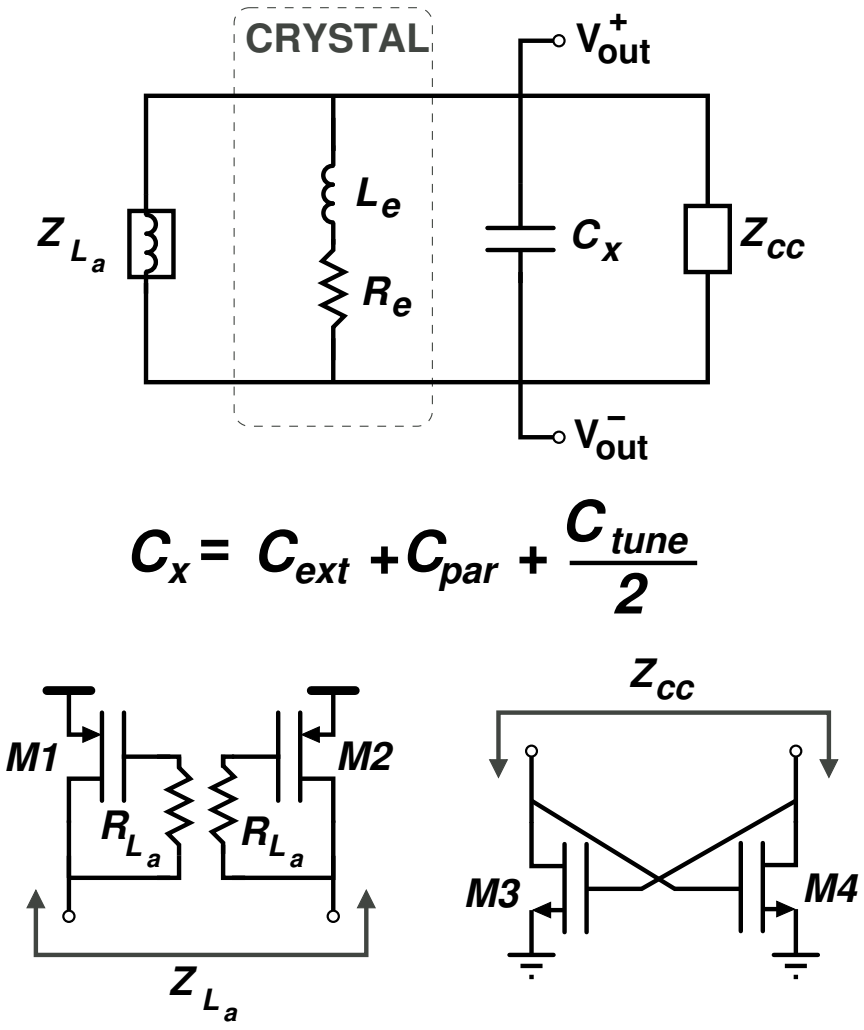

Figure 2.15: Small signal model of differential crystal oscillator for parallel resonance region

2.7.2 Crystal Oscillator Small Signal Analysis for $\omega_{r_s} < \omega < \omega_{r_p}$

The equivalent small signal model for $\omega_{r_s} < \omega < \omega_{r_p}$ (*i.e.,* parallel-resonance mode) is shown in Figure 2.15. First, we obtain the real part of the crystal oscillator total impedance,

Y_t, for $\omega_{r_s} < \omega < \omega_{r_p}$. This is defined as

$$\begin{aligned} \mathrm{Re}\{Y_t\}(\omega)|_{\omega_{r_s}<\omega<\omega_{r_p}} = & \\ & \mathrm{Re}\{Y_{xtal}\}|_{\omega_{r_s}<\omega<\omega_{r_p}} \\ & + \mathrm{Re}\{Y_{cc} + Y_{L_a}\} \end{aligned} \tag{2.8}$$

Using Figure 2.12, Y_{xtal} in parallel resonance mode is given by

$$Y_{xtal}(\omega)|_{\omega_{r_s}<\omega<\omega_{r_p}} = \frac{1}{R_e + j\omega L_e} \tag{2.9}$$

In order to obtain $\mathrm{Re}\{Y_{xtal}\}$, a series-to-parallel transformation is needed to obtain the equivalent parallel resistance, R_p[4]. The equivalent parallel resistance, R_p, is given by

$$\begin{aligned} R_p &= Q^2 R_e \\ &= \frac{\omega^2 L_e^2}{R_e}. \end{aligned} \tag{2.10}$$

Using the fact that $L_e = 1/(\omega^2 C_L)$ at resonance,

$$R_p = \frac{1}{\omega^2 R_e C_L^2}. \tag{2.11}$$

Since R_e is related to R_1 by

$$R_e = R_1 \left(1 + \frac{C_0}{C_L}\right)^2, \tag{2.12}$$

[4]This is because $\mathrm{Re}\{Y_{xtal}\}$ is $1/R_p$.

we obtain

$$R_p = \frac{1}{\omega^2 R_1 \left(C_0 + C_L\right)^2}. \tag{2.13}$$

Therefore, we obtain the first term in Equation 2.8, *i.e.,* $\mathrm{Re}\{Y_{xtal}\}$ as $1/R_p$ given by

$$\mathrm{Re}\{Y_t\}(\omega)|_{\omega_{r_s}<\omega<\omega_{r_p}} = \omega^2 R_1 \left(C_0 + C_L\right)^2. \tag{2.14}$$

Secondly, we obtain the remaining two terms in Equation 2.8, *i.e.,*

$$\mathrm{Re}\{Y_{cc} + Y_{L_a}\}(\omega) = \frac{1}{2\omega_{T_p}\left(\omega^2 + \omega_z^2\right)} \times \left[\left(g_{m_p}\omega_z - g_{m_n}\omega_{T_p}\right)\omega^2 + g_{m_p}\omega_{T_p}\omega_z^2 - g_{m_n}\omega_{T_p}\omega_z^2\right]. \tag{2.15}$$

Now that the real part of the total admittance is obtained, we look at the imaginary part of Y_t which, using Figure 2.15, is

$$\mathrm{Im}\{Y_t\}|_{\omega_{r_s}<\omega<\omega_{r_p}} = \mathrm{Im}\{Y_{xtal}\}|_{\omega_{r_s}<\omega<\omega_{r_p}} + \mathrm{Im}\{Y_{cc} + Y_{L_a} + Y_{C_x}\}. \tag{2.16}$$

The imaginary part of crystal admittance is simply given by

$$\mathrm{Im}\{Y_{xtal}\}|_{\omega_{r_s}<\omega<\omega_{r_p}} = (L_e)^{-1}. \tag{2.17}$$

However, since the crystal manufacturers already specify an equivalent parallel capacitance

that ensures a parallel-mode resonance (*i.e.,* C_L), the crystal equivalent inductance, L_e, has little significance in our analysis.

Similar to the approach for $\mathrm{Re}\{Y_t\}$, we obtain the imaginary part the cross-coupled pair and active inductor admittance. Using the small signal model of Figure 2.15, we obtain

$$\mathrm{Im}\{Y_{cc}+Y_{L_a}+Y_{C_x}\}(\omega) = \tag{2.18}$$

$$\frac{g_{m_p}\omega}{2\omega_{T_p}\left(1+\frac{\omega^2}{\omega_z^2}\right)} + \frac{g_{m_n}\omega}{2\omega_{T_n}} - \frac{g_{m_p}\omega}{2\omega_z\left(\frac{\omega^2}{\omega_z^2}+1\right)} + \omega C_x. \tag{2.19}$$

Before we provide a set of design considerations, two conditions need to be satisfied: 1) $\mathrm{Im}\{Y_{cc}+Y_{L_a}+Y_{C_x}\}$ should yield a capacitive admittance equal to the admittance of C_L at resonance to result in oscillation, and 2) the chosen design parameters must lead to a positive value for C_{ext} since this is a physical capacitor placed across the crystal. That is, $\mathrm{Im}\{Y_{cc}+Y_{L_a}+Y_{C_x}-Y_{C_{ext}}\} < Y_{C_L}$. Using Equation 2.18, Equation 2.7, and simplifying, we get

$$\frac{g_{m_p}}{2}\frac{\frac{1}{\omega_{T_p}}-\frac{1}{\omega_z}}{1+\frac{\omega^2}{\omega_z^2}} + \frac{g_{m_n}}{2\omega_{T_n}} + (C_x - C_{ext}) - C_L < 0. \tag{2.20}$$

Expanding the terms, we obtain

$$\frac{1}{2\omega_{T_n}\left(\omega^2+\omega_z^2\right)}\times$$

$$\begin{aligned}
&-\omega_z^2\left[-g_{m_p}\omega_{T_n}-g_{m_n}\omega_{T_p}\right.\\
&\left.+2\omega_{T_n}\omega_{T_p}\left(C_L-\left(C_x-C_{ext}\right)\right)\right]\\
&-\omega_z\left(g_{m_p}\omega_{T_n}\omega_{T_p}\right)\\
&+g_{m_n}\omega^2\omega_{T_p}-2\omega^2\omega_{T_p}\omega_{T_n}\left(C_L-\left(C_x-C_{ext}\right)\right)<0. \quad (2.21)
\end{aligned}$$

The inequality in Equation 2.21 is a second order polynomial of ω_z. In order to satisfy the inequality, we ensure that there are no real solutions that can violate the inequality. We let

$$a=-g_{m_p}\omega_{T_n}-g_{m_n}\omega_{T_p}+2\omega_{T_n}\omega_{T_p}\left(C_L-\left(C_x-C_{ext}\right)\right), \quad (2.22)$$

$$b=g_{m_p}\omega_{T_n}\omega_{T_p}, \quad (2.23)$$

and

$$c=-g_{m_n}\omega^2\omega_{T_p}+2\omega^2\omega_{T_p}\omega_{T_n}\left(C_L-\left(C_x-C_{ext}\right)\right); \quad (2.24)$$

and ensure that $a>0$, and $b^2-4ac<0$, to satisfy Equation 2.21. This derivation is presented below:

Using Equation 2.22, for $a>0$, we have

$$2\left(C_L-\left(C_x-C_{ext}\right)\right)>\frac{g_{m_p}}{\omega_{T_p}}+\frac{g_{m_n}}{\omega_{T_n}} \quad (2.25)$$

Since $g_{m_p}/\omega_{T_p} = C_{gg_p}$, and $g_{m_n}/\omega_{T_n} = C_{gg_n}$, we obtain

$$2\left(C_L - (C_x - C_{ext})\right) > C_{gg_p} + C_{gg_n} \tag{2.26}$$

This condition is easily satisfied since C_L is large (*e.g.,* 20pF).

Using Equation 2.23, and Equation 2.24, we want $b^2 - 4ac < 0$, that is

$$\begin{aligned} b^2 - 4ac = & \\ & g_{m_p}^2 \omega_{T_n}^2 \omega_{T_p}^2 \\ & - 4\left[-g_{m_p}\omega_{T_n} - g_{m_n}\omega_{T_p}\right. \\ & \left. + 2\omega_{T_p}\omega_{T_n}\left(C_L - (C_x - C_{ext})\right)\right] \\ & \left[-g_{m_n}\omega^2\omega_{T_p}\right. \\ & \left. + 2\omega^2\omega_{T_n}\omega_{T_p}\left(C_L - (C_x - C_{ext})\right)\right] < 0. \end{aligned} \tag{2.27}$$

Multiplying out the terms in Equation 2.27,

$$\begin{aligned} g_{m_p}^2 \omega_{T_n}^2 \omega_{T_p}^2 - 4g_{m_p}g_{m_n}\omega^2\omega_{T_n}\omega_{T_p} - 4g_{m_n}^2\omega^2\omega_{T_p}^2 & \\ + 8g_{m_n}\omega^2\omega_{T_p}^2\omega_{T_n}\left(C_L - (C_x - C_{ext})\right) & \\ + 8g_{m_p}\omega^2\omega_{T_n}^2\omega_{T_p}\left(C_L - (C_x - C_{ext})\right) & \\ + 8g_{m_n}\omega^2\omega_{T_p}^2\omega_{T_n}\left(C_L - (C_x - C_{ext})\right) & \\ - 16\omega^2\omega_{T_n}^2\omega_{T_p}^2\left(C_L - (C_x - C_{ext})\right)^2 < 0. & \end{aligned} \tag{2.28}$$

After cancellations, we obtain

$$g_{m_p}^2 + \left(16\omega^2 C_{gg_n} + 8\omega^2 C_{gg_p}\right)\left(C_L - (C_x - C_{ext})\right) < 16\omega^2 \left(C_L - (C_x - C_{ext})\right)^2 + 4\omega^2 C_{gg_n} C_{gg_p} + 4\omega^2 C_{gg_n}^2. \quad (2.29)$$

2.7.3 Low Frequency Design Considerations

At low frequencies, (*i.e.,* $\omega \ll \omega_{r_s}$) we must choose the design parameters to avoid a parasitic oscillation. With an incorrect set of design parameters, the active inductor in parallel with C_0 can form an *LC* tank. The combination of this *LC* tank and the negative resistance of the cross-coupled pair can result in an undesired oscillation.

A sufficient condition to avoid a parasitic oscillation is to choose the design parameters such that $\mathrm{Im}\{Y_t\} \neq 0$ for $\omega \ll \omega_{r_s}$. Nevertheless, even if $\mathrm{Im}\{Y_t\}$ is equal to 0 at a certain frequency, parasitic oscillation is still avoided if we ensure that $\mathrm{Re}\{Y_t\} > 0$ for that frequency (*i.e.,* avoid parasitic oscillation by depriving the circuit of the necessary loop gain).

If we let $\mathrm{Im}\{Y_t\}$ in Equation 2.5 equal to zero, three solutions for ω are obtained. Firstly, at $\omega = 0$ (*i.e.,* DC), $\mathrm{Im}\{Y_t\}$ becomes zero. Therefore, $\mathrm{Re}\{Y_t\}$ must be made positive (*i.e.,* resistive to avoid loop gain) to prevent latch-up. Using Equation 2.6 and simplifying,

$$@\ \omega = 0, \quad \mathrm{Re}\{Y_t\} > 0 \Rightarrow \boxed{g_{m_p} > g_{m_n}} \quad (2.30)$$

This makes intuitive sense as the positive resistance of the active inductor should dominate over the negative resistance of the cross-coupled pair to result in a low loop gain at DC to

prevent latch-up.

Secondly, we consider the ω^2 coefficient in Equation 2.5. We select the design parameters such that there is no real frequency which can result in $\mathrm{Im}\{Y_t\}$ equal to zero. Therefore, it is ensured that,

$$\omega^2 = \frac{\omega_z}{\omega_{T_p}} \frac{-1}{g_{m_n} + 2\omega_{T_n}(C_0 + C_x)} \left[g_{m_p}\omega_{T_n}\omega_z - g_{m_p}\omega_{T_p}\omega_{T_n} + g_{m_n}\omega_{T_p}\omega_z + 2\omega_{T_p}\omega_{T_n}\omega_z(C_0 + C_x) \right], \tag{2.31}$$

is always negative to prevent parasitic oscillation. This yields the following inequality:

$$g_{m_p}\omega_{T_n}\omega_z - g_{m_p}\omega_{T_p}\omega_{T_n} + g_{m_n}\omega_{T_p}\omega_z + 2\omega_{T_p}\omega_{T_n}\omega_z(C_0 + C_x) > 0. \tag{2.32}$$

Rearranging, we obtain

$$g_{m_p}\omega_{T_n}\omega_z + 2\omega_{T_p}\omega_{T_n}\omega_z(C_0 + C_x) > g_{m_p}\omega_{T_p}\omega_{T_n} - g_{m_n}\omega_{T_p}\omega_z \tag{2.33}$$

Assuming $g_{m_p}\omega_{T_n} \gg g_{m_n}\omega_z$, and some factoring, we obtain

$$\boxed{\omega_z > \frac{g_{m_p}}{C_{gg_p} + 2(C_0 + C_x)}}. \tag{2.34}$$

It is interesting to note that Equation 2.34 depends on the active inductor parameters. Therefore, we need to choose the active inductor PMOS transistor size and the active inductor resistance, R_{L_a}, judiciously to avoid a parasitic oscillation.

2.7.4 Parallel Resonance Mode Design Considerations

In the parallel-resonance mode, we need to ensure that $\mathrm{Re}\{Y_t\} \ll 0$ for oscillation start-up. In order to simplify Equation 2.15, we assume that the active inductor zero frequency, ω_z, is much smaller than the PMOS transit frequency, ω_{T_p} (*i.e.,* , $\omega_z \ll \omega_{T_p}$). At resonance (*i.e.,* $\omega = \omega_{xo}$), we obtain

$$\mathrm{Re}\{Y_{cc} + Y_{L_a}\}(\omega = \omega_{xo}) \approx \frac{-g_{m_n}}{2} \cdot \frac{\omega_{xo}^2}{\omega_z^2 + \omega_{xo}^2}. \tag{2.35}$$

If we choose the design parameters such that $\omega_{xo} \gg \omega_z$, we obtain

$$\mathrm{Re}\{Y_{cc} + Y_{L_a}\}(\omega = \omega_{xo}) \approx \frac{-g_{m_n}}{2}. \tag{2.36}$$

It is important to note that it is indeed desirable to set $\omega_{xo} \gg \omega_z$. This is to avoid loading the crystal with the active inductor circuit at resonance. Essentially, $\omega_{xo} \gg \omega_z$, means that the active inductor impedance is large at resonance. Using Equation 2.14 and Equation 2.36, we obtain a start-up condition ($\mathrm{Re}\{Y_t\} \ll 0$) at resonance which is

$$\frac{-g_{m_n}}{2} + \omega_{xo}^2 R_1 (C_0 + C_L)^2 \ll 0, \tag{2.37}$$

which results in

$$\boxed{g_{m_n} \cdot \frac{1}{2\omega_{xo}^2 R_1 (C_0 + C_L)^2} \gg 1}, \tag{2.38}$$

which is, in an essence, $G_m R_P \gg 1$.

Since Y_{xtal} is inductive in this region, we need to choose the design parameters (such as

g_{m_n}, g_{m_p}, and R_{L_a}) such that the combined admittance presented to the crystal is positive (*i.e.,* capacitive) in the parallel resonance regime. The admittance should precisely be equal to the admittance of C_L to result in oscillation at the desired frequency. Using Equation 2.29, we make the following assumptions to formulate a set of design equations to satisfy Equation 2.21. We assume that

$$4\left(C_L-(C_x-C_{ext})\right)^2 \gg C_{gg_n}C_{gg_p}+C_{gg_n}^2. \tag{2.39}$$

This is a reasonable assumption, since C_L is often much larger than the NMOS and PMOS gate capacitances. Using this assumption, Equation 2.29 simplifies to

$$\frac{g_{m_p}^2}{\omega^2\left(C_L-(C_x-C_{ext})\right)}+16C_{gg_n}+8C_{gg_p}<16\left(C_L-(C_x-C_{ext})\right). \tag{2.40}$$

In order to make (2.40) more tractable, we make the following design choice. If we ensure that,

$$8\left(\frac{\omega_{xo}}{\omega_{T_p}}\right)^2 \gg \frac{C_{gg_p}}{C_L-(C_x-C_{ext})}, \tag{2.41}$$

a simple design condition is achieved. That is

$$\boxed{C_L-(C_x-C_{ext})>C_{gg_p}+C_{gg_n}}, \tag{2.42}$$

yields a positive external capacitor for parallel region oscillation.

2.7.5 Duty Cycle Correction Analysis

The new duty cycle correction scheme used in the frequency quadrupler is shown in Figure 2.16. The new DCC circuit ensures the generation of the 25% duty cycle 1X clocks so that when these are combined, the duty cycle of the 96MHz, 2X clock is 50%. A non-50% duty cycle 2X clock will result in unwanted spurs in the 4X clock. If the duty cycle of the input to an XOR plus delay-based frequency doubler in non-50%, the output of the frequency doubler will have large unwanted spurs. And, if the quadrupler is used as a PLL reference, these spurs can then degrade, often severely, the synthesizer integrated phase noise. Therefore, the duty cycle of the 2X clock must be tightly controlled.

We will now outline the small signal analysis of the DCC. In order to obtain the loop gain, the DCC loop is broken at the error amplifier output. The transfer function from the break point all the way to the return point is then calculated. This transfer function is indeed the loop gain.

We need to know how the DCC control voltage, v_c, affects the 2X clock duty cycle. This derivation requires a few steps. First, it is required to obtain a relationship between the skewed inverter switching point, t_{sw}[5], and the DCC control voltage, v_c[6], *i.e.,* $\frac{\delta t_{sw}}{\delta v_c}$. This relationship is written as

$$\frac{\delta t_{sw}}{\delta v_c} = \frac{\delta t_{sw}}{\delta v_{in}} \times \frac{\delta v_{in}}{\delta v_c}. \tag{2.43}$$

[5]Defined as the time when the skewed inverter output is equal to $V_{DD}/2$.

[6]Since the inputs to the skewed inverters are differential and the 25% duty cycle clocks are a dual of one another, it is sufficient to analyze the behavior of one skewed inverter and apply the results throughout the analysis.

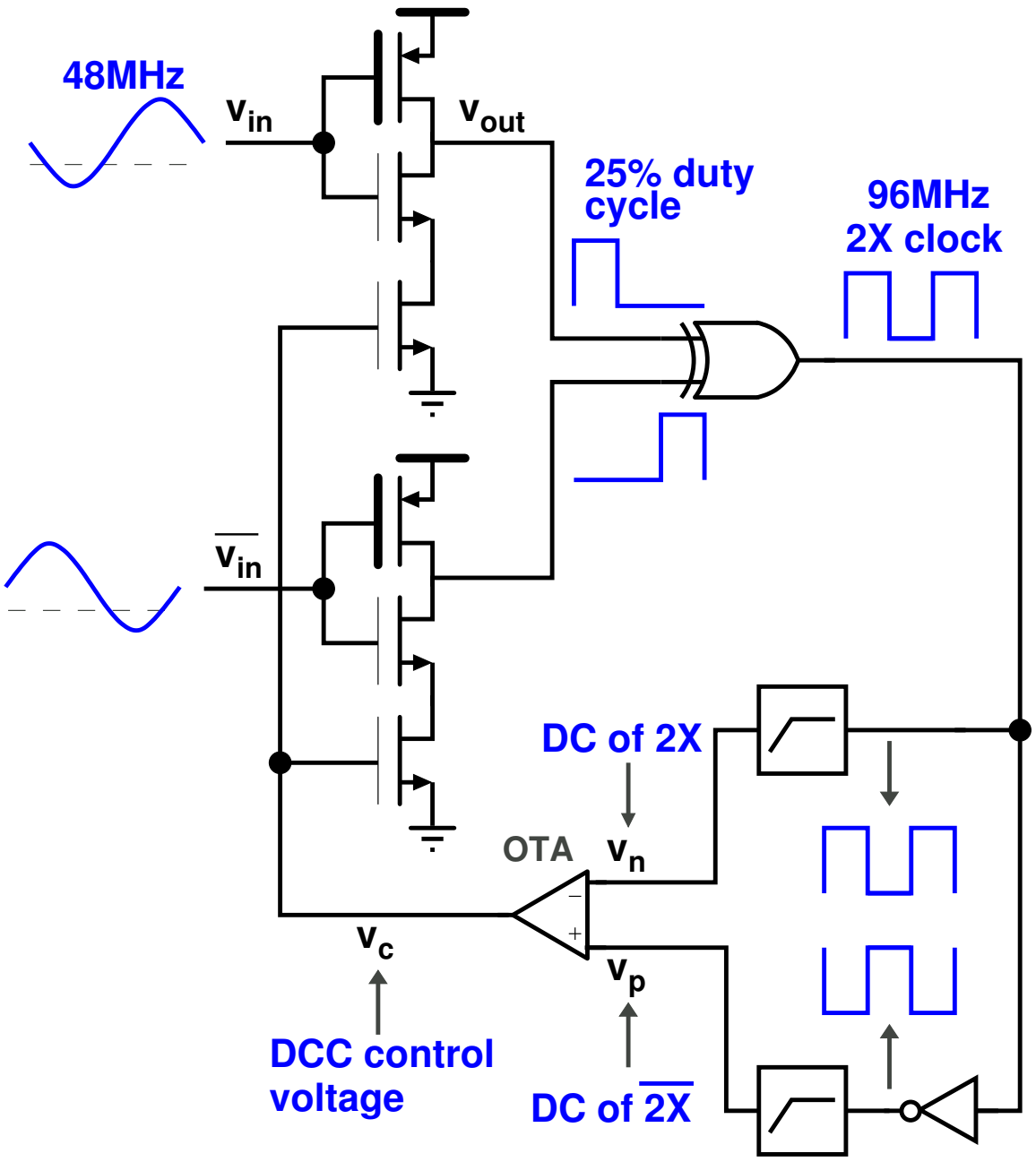

Figure 2.16: The duty cycle correction scheme used in the frequency quadrupler

The changes in the 1X, 25% duty cycle clock, $\delta_{DC_{1X}}$, can then be readily obtained as

$$\frac{\delta_{DC_{1X}}}{\delta v_c} = -2\frac{\delta t_{sw}}{\delta v_c} \times \frac{1}{T_{xo}}, \tag{2.44}$$

where T_{xo} is the XO period. The factor of 2 multiplier accounts for the fact that since both the rising and falling edges move with respect to changes in v_c, the resulting change in 1X duty cycle is doubled. The negative sign is due to the inverter operation.

We assume a sinusoidal waveform for the XO given by $v_{XO}(t) = A_{XO}\sin(\omega_{XO}t)$, where A_{XO} is the XO amplitude, and ω_{XO} is the XO frequency. Using the XO sinusoidal waveform equation,

$$\frac{\delta v_{XO}}{\delta t} = A\omega_{XO}\cos(\omega_{XO}t). \tag{2.45}$$

For $t = t_{sw}$, $v_{XO} = v_{in}$, and using Equation 2.45 we obtain

$$\frac{\delta t_{sw}}{\delta v_{in}} = \frac{1}{A\omega_{XO}\cos(\omega_{XO}t_{sw})}. \tag{2.46}$$

We now obtain the second term in Equation 2.43, *i.e.,* $\frac{\delta v_{in}}{\delta v_c}$. $\frac{\delta v_{in}}{\delta v_c}$ is obtained in two steps: First, the skewed inverter small signal output current change with respect to changes in DCC control voltage, v_c, is obtained. Second, the skewed inverter small signal output current change with respect to input voltage, v_{in}, is obtained. That is,

$$\frac{\delta v_{in}}{\delta v_c} = \frac{\left.\frac{\delta I_d}{\delta v_c}\right|_{v_{in}=0}}{\left.\frac{\delta I_d}{\delta v_{in}}\right|_{v_c=0}}, \tag{2.47}$$

where

$$\left.\frac{\delta I_d}{\delta v_c}\right|_{v_{in}=0} = g_{m_c}\frac{g_{m_n}}{g_{m_n}+\frac{1}{r_{oc}}}, \tag{2.48}$$

and

$$\left.\frac{\delta I_d}{\delta v_{in}}\right|_{v_c=0} = g_{m_p}+\frac{g_{m_n}}{1+g_{m_n}r_{o_c}}. \tag{2.49}$$

Parameters g_{m_p}, g_{m_n}, g_{m_c}, and r_{o_c} are the trans-conductance of skewed inverter PMOS, trans-conductance of skewed inverter NMOS, trans-conductance of skewed inverter bottom current control NMOS, and output resistance of skewed inverter bottom current control NMOS transistors, respectively. Therefore,

$$\frac{\delta v_{in}}{\delta v_c} = \frac{g_{m_c}\frac{g_{m_n}}{g_{m_n}+\frac{1}{r_{oc}}}}{g_{m_p}+\frac{g_{m_n}}{1+g_{m_n}r_{o_c}}}. \tag{2.50}$$

Using Equations 2.43, 2.44, 2.46, and 2.50. For a 25% duty cycle switching point (*i.e.,* $t_{sw} = T_{XO}/8$),

$$\frac{\delta_{DC_{1X}}}{\delta v_c} = \frac{-\sqrt{2}}{A\pi}\frac{g_{m_c}\frac{g_{m_n}}{g_{m_n}+\frac{1}{r_{oc}}}}{g_{m_p}+\frac{g_{m_n}}{1+g_{m_n}r_{o_c}}}. \tag{2.51}$$

Equation 2.51 establishes the relationship between the duty cycle of 1X clock (DC_{1X}) and the DCC control voltage, v_c.

Since the pair of 25% duty cycle 1X clocks are XORed to form a 50% duty cycle clock at twice the frequency (*i.e.,* the 2X clock), we need another factor of 2 multiplier to obtain the changes in the duty cycle of 2X clock. Therefore,

$$\frac{\delta_{DC_{2X}}}{\delta v_c} = 2\frac{\delta_{DC_{1X}}}{\delta v_c}. \tag{2.52}$$

Now that we have established the relationship between the duty cycle of 2X clock (DC_{2X}) and the DCC control voltage, v_c, we continue the loop gain transfer function calculation from the output of the XOR gate. Using Figure 2.16, the average (DC) of the 2X clock, v_p, is obtained as

$$v_p(\omega) = DC_{2X} \cdot \frac{V_{DD}}{1 + j\omega RC}, \tag{2.53}$$

where RC is the time constant of the averaging low pass filter. Similarly, the average (DC) of the $\overline{2X}$ clock, v_n, is obtained as

$$v_n(\omega) = -DC_{2X} \cdot \frac{V_{DD}}{1 + j\omega RC}. \tag{2.54}$$

The OTA output voltage, $V_{out_{OTA}}$, is then obtained as

$$V_{out_{ota}}(\omega) = 2 \cdot DC_{2X} \cdot \frac{V_{DD}}{1 + j\omega RC} \cdot A_{OTA}, \tag{2.55}$$

where A_{OTA} is the voltage gain of the OTA[7].

Using equations 2.51, 2.52, and 2.55, we obtain the DCC loop gain as

$$\boxed{LG_{DCC}(\omega)\frac{-4\sqrt{2}}{A_{XO}\pi} \cdot \frac{g_{m_c}\frac{g_{m_n}}{g_{m_n}+\frac{1}{r_{o_c}}}}{g_{m_p}+\frac{g_{m_n}}{1+g_{m_n}r_{o_c}}} \frac{V_{DD}}{1 + j\omega RC} \cdot A_{OTA}.} \tag{2.56}$$

[7]Since the dominant pole of the DCC feedback loop is set by the averaging low pass filters in the kHz range, (*i.e.,* much lower than the OTA bandwidth) we ignore the frequency response of the OTA for loop gain analysis.

CHAPTER III

A Low Voltage Sub 300μW 2.5GHz Current Reuse VCO

3.1 Introduction

Low supply voltages due to process scaling are an impediment to reducing the VCO power consumption, because they limit the choice of VCO topologies to those that do not have a high DC to RF conversion efficiency. VCO topologies such as CMOS current reuse and cross coupled CMOS have excellent DC to RF efficiencies, often a factor of two better than NMOS or PMOS only VCOs [30]. However, the standard implementation of such VCOs, where a PMOS transistor is stacked on top of an NMOS transistor, requires a supply voltage larger than the sum of the threshold voltages of the two transistors, $V_{th_n} + V_{th_p}$. In order to have reliable operation over PVT, the minimum supply voltage is more than this sum and can be as high as 1.1V in a 65nm digital CMOS process. In addition, VCOs are highly sensitive to supply noise, pushing, and pulling, and therefore a regulated voltage is always required. This further lowers the available internal voltage supply for VCOs and makes the use of CMOS VCOs operating from a low supply even more difficult.

In recent years, researchers have reported a number of VCOs using AC coupling capaci-

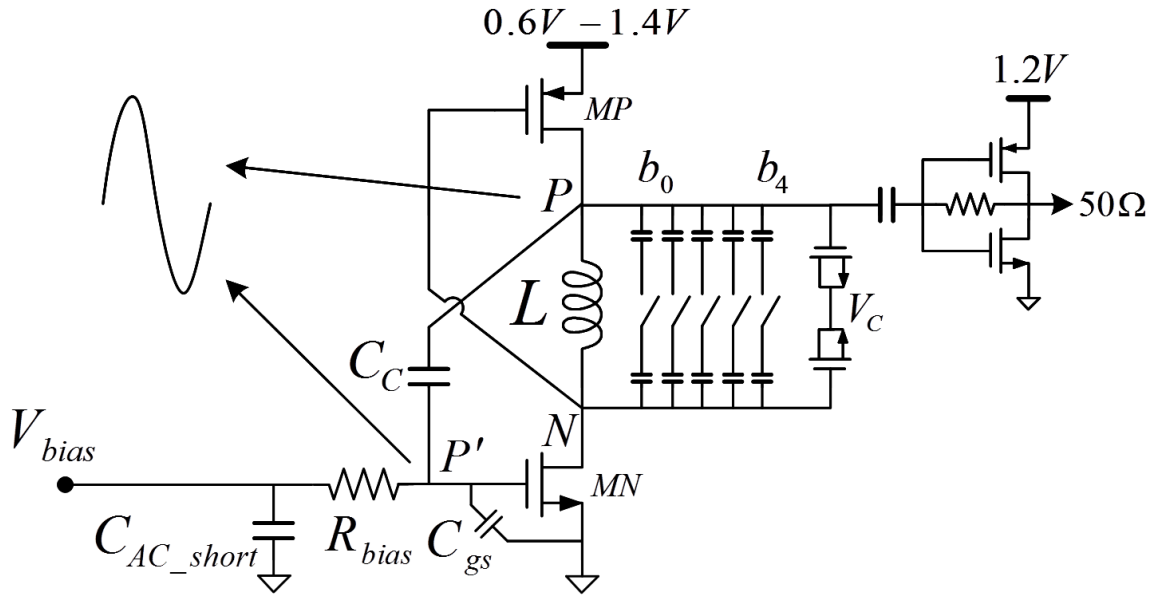

Figure 3.1: The proposed AC coupled current reuse VCO

tors to achieve better phase noise and higher FoM by operating the transistors in class C regime. However, low start up gain restricts the VCO topology to NMOS or PMOS only for low voltage operation [31], or else the penalty of a high supply voltage if the more efficient CMOS topology is used [32].

This work offers a simple technique to enable CMOS current reuse VCOs to operate at very low supply voltages by adding an AC coupling capacitor to achieve good phase noise at low power consumption. Introduced in [33], a 1.25V two-transistor current reuse VCO uses a PMOS and an NMOS transistor to provide negative resistance to sustain oscillation in an LC tank. Figure 3.1 shows the proposed current reuse VCO which operates with a supply voltage as low as 0.6V, which is much lower than the sum of NMOS and PMOS threshold voltages. In steady state, the operation of the VCO can be divided into two parts during each cycle: in the first half cycle, both MN and MP are on, injecting energy into the *LC* tank; and in the second half cycle, both transistors are off, and energy is dissipated through the loss of

the tank.

In the modified current reuse VCO, the voltage at node P is AC coupled to gate of MN (node P') through capacitor C_C. A separate DC bias is applied to the gate of MN through resistor R_{bias} to independently set its gm to ensure start up at lower supply voltages. This enables both MN and MP to operate in saturation even at supply voltages as low as 0.6V and still provide the needed start up gain. This in turn reduces the power consumption while enabling low phase noise operation.

3.2 Design Methodology

The focus of this design is to minimize power consumption while meeting the phase noise requirement for a desired application at a very low voltage supply. A large inductance is desired to achieve a very low power VCO. However, the inductance cannot be arbitrarily increased as VCO phase noise is limited by kT/C and Q, where C is the total tank capacitance, and Q the quality factor of the VCO tank. For a fixed oscillation frequency and constant Q, as inductance is increased, total tank capacitance C is reduced, therefore increasing kT/C and degrading the phase noise. The tank quality factor of the VCO shown in Figure 3.2 is given by $Q_{tank} = R_p\sqrt{\frac{C}{L}}$, where it is dominated by the inductance L and its equivalent parallel resistance R_p. The power consumption of an LC VCO is directly proportional to R_p.

In a conventional current reuse VCO [33], meeting the startup condition over PVT for a supply voltage lower than 1V is difficult. An AC coupling capacitor, C_C, enables the VCO to work at much lower supply voltages because g_{m_n} can be independently adjusted to meet

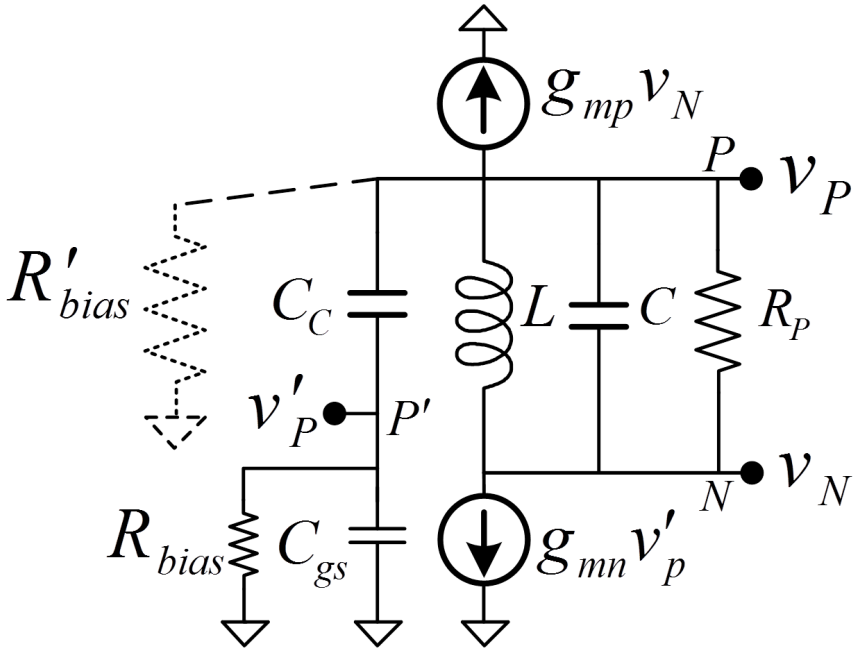

Figure 3.2: Small signal model of the proposed AC coupled VCO

the startup condition in Equation 3.1 by increasing the bias voltage V_{bias}. In order to operate the VCO at the lowest voltage supply, the start up gain needs to be maximized by choosing large values for C_C and R_{bias}. This is explained by looking at the impedance Z_P at node P at resonance using the small signal model in Figure 3.2. Impedance Z_P should be negative to ensure start up so that

$$Z_P = \left(\frac{1}{R'_{bias}} + |\alpha| g_{m_n} + g_{m_p} - |\alpha| g_{m_n} g_{m_p} R_P \right)^{-1} < 0, \tag{3.1}$$

where g_{m_n} and g_{m_p} are the trans-conductances of MN and MP, R'_{bias} the equivalent resistance seen at node P due to R_{bias}, and $\alpha = v'_p/v_p$ is the voltage divider ratio between nodes P and P'. It is important to choose the optimum values for C_C and R_{bias} to have sufficient start up gain. In an ideal case v'_p/v_p must be close to one. As suggested by Figure 3.2, C_C should be bigger than C_{gs} (capacitance at node P') by a large factor so to maximize

the transfer function

$$\frac{v_p'}{v_p} = |\alpha| = \left(1+\beta+\frac{1}{sR_{bias}C_C}\right)^{-1}, \tag{3.2}$$

where $\beta = C_{gs}/C_C$. Using Equation 3.2, a lower bound for bias resistance R_{bias} is derived as

$$R_{bias} \geq \frac{1}{\omega C_C}\left(\frac{|\alpha|}{\sqrt{1-|\alpha|^2(1+\beta)^2}}\right). \tag{3.3}$$

In addition, R_{bias} should be large to avoid degrading the tank quality factor by reducing the impedance at node P. Using Figure 3.2, R'_{bias} at resonance is given by

$$R'_{bias} = \left(\frac{1+Q^2}{Q^2}\beta^2 + 2\beta + 1\right) R_{bias}, \tag{3.4}$$

where $Q = R_{bias}C_{gs}\omega$ is the quality factor of parallel combination of C_{gs} and R_{bias}. For $\beta \ll 1$ ($C_{gs} \ll C_C$), we can assume that $R'_{bias} \approx R_{bias}$. To avoid degrading the tank Q by more than 10%, R'_{bias} should be approximately 10 times larger than R_P. This is a conservative approximation because it only considers the inductor parallel resistance R_p and not the loading effect of MN, MP, and the capacitor bank. Therefore, $R_{bias} \approx 10 \cdot R_p$ is more than enough to avoid significant Q degradation.

3.3 Practical Design Considerations

The prototype VCO, implemented in 65nm CMOS, uses a compact 5 turn 8nH inductor with a quality factor of 11. This results in an equivalent parallel tank resistance $R_P \approx 1.4k\Omega$.

Considerably higher Q values can be obtained at the cost of larger inductor area, which will further improve the phase noise and lower the power consumption.

Transistors MN (4.8μm/80nm) and MP (18μm/80nm) are sized so to meet the startup condition in Equation 3.1 for a voltage supply as low as 0.6V. Flicker noise upconversion is reduced by avoiding the use of minimum length transistors. Using longer transistors also improves the VCO loaded Q and reduces the noise contribution of MN and MP by reducing their effective g_{ds} [30]. An AC coupling capacitor C_C=250fF ($\beta \approx 0.02$) is used, which is large enough to result in a voltage divide ratio $|\alpha| \approx 0.96$ from Equation 3.2. From Equation 3.3, a resistor bias value $R_{bias} \geq 1.4k\Omega$ is sufficient for start up; and according to Equation 3.4, $R_{bias} \approx 10 \cdot R_P = 14k\Omega$ for minimum Q degradation of the tank. The analysis to optimize the start up gain and minimize the tank Q degradation, leads to R_{bias} values ranging from 1.4kΩ to 14kΩ. However, the thermal noise of R_{bias} is also important. Considering sufficient start up gain, minimal Q degradation, and the thermal noise contribution of R_{bias}, an optimum value of 5kΩ is chosen.

3.4 Implementation and Measurement

The prototype VCO (Figure 3.3) is implemented in a 1P9M 65nm digital CMOS process and occupies a core area of 0.13mm^2. The inductor is formed with thick metal 9 and tuning is achieved with a 5 bit bank of MIM capacitors. The varactor is formed with an N type MOS capacitor biased at 0.55V for all measurements. The simulated VCO gain is approximately 45MHz/V. The device is packaged in a 40 pin 6×6 QFN package. Phase noise is measured using an Agilent E5052B source analyzer, and current is sensed with a Keithley 2400 source

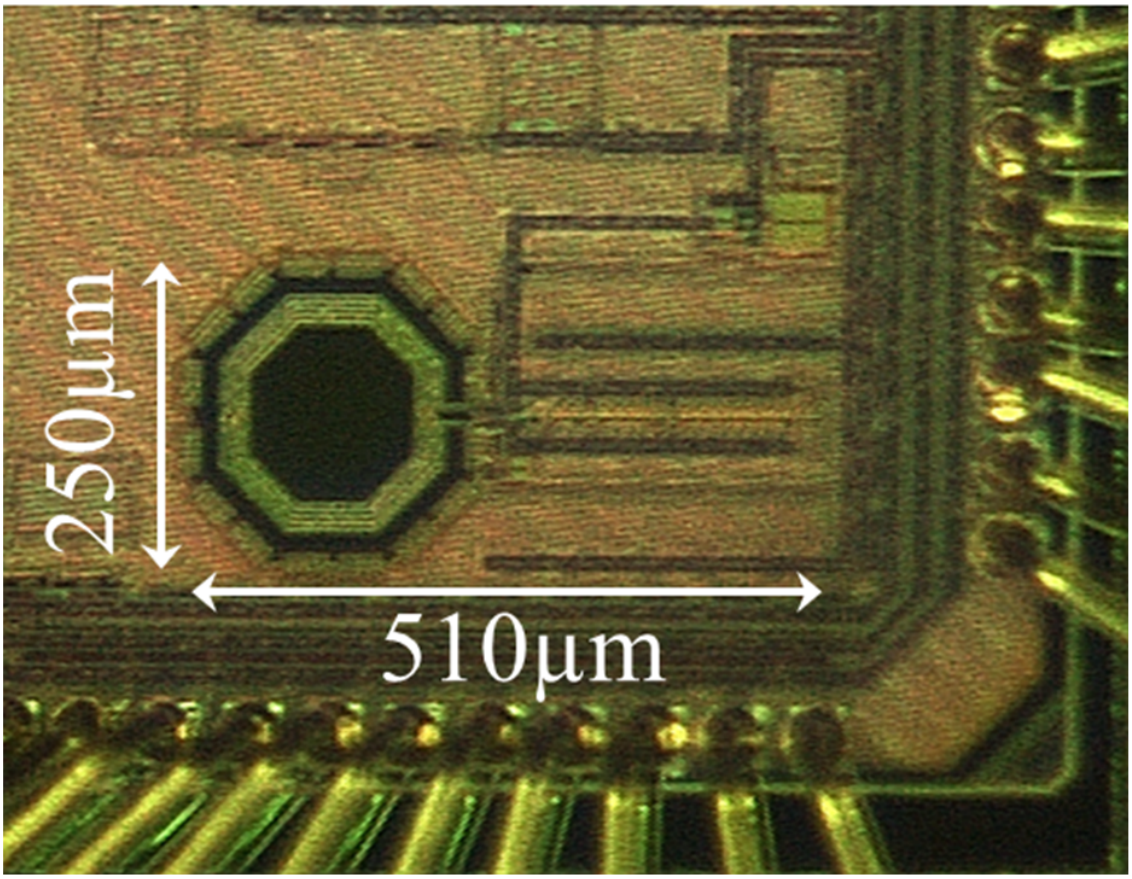

Figure 3.3: Chip photo of AC coupled VCO

meter.

The measured tuning range is 2.17GHz to 2.9GHz and the VCO operates with supply voltage as low as 0.6V. Figure 3.4 shows the measured phase noise and power consumption at 2.53GHz for different supply voltages. With a 0.7V supply, the measured VCO phase noise at a 3MHz offset is -122.6dBc/Hz with a power consumption of 185μW. For a 0.85V supply, phase noise is improved to -126.1dBc/Hz with a 288μW power consumption. For applications requiring better performance, a phase noise of -130.1dBc/Hz is achieved by increasing the supply to 1.3V with a 0.9mW power consumption.

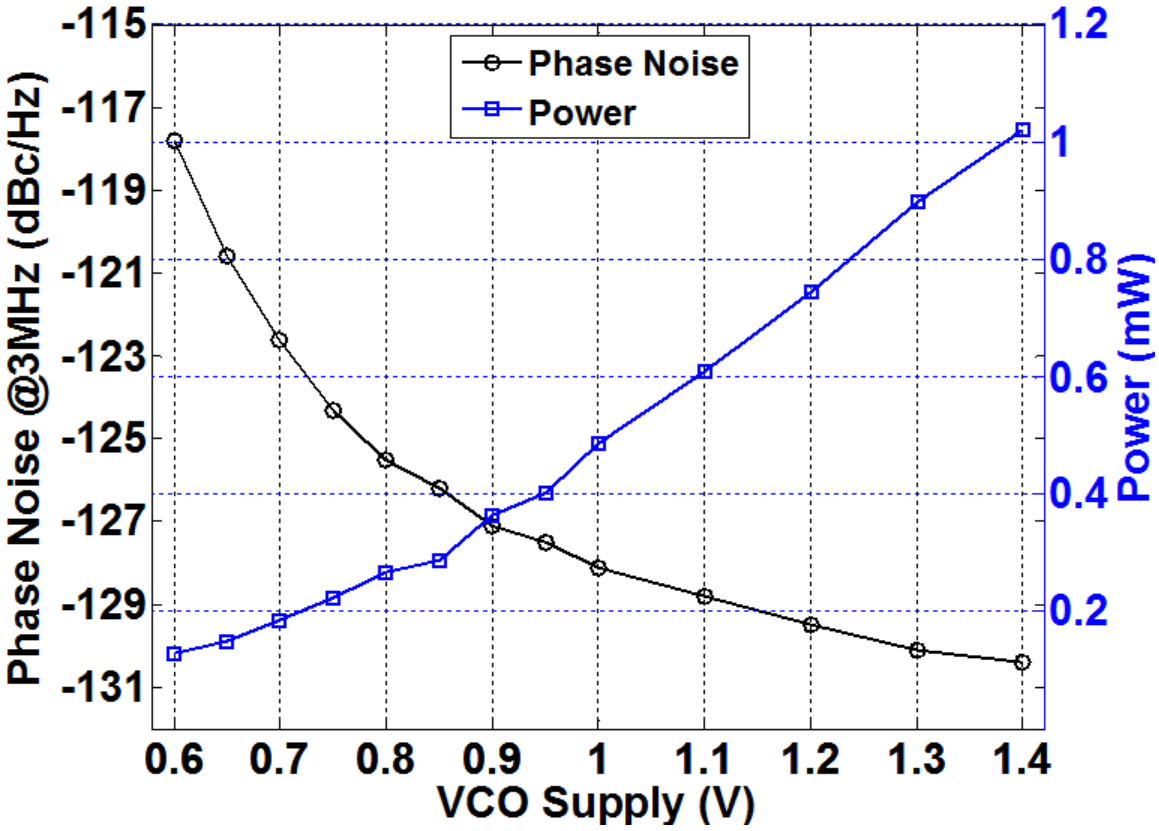

Figure 3.4: Measured VCO phase noise and power consumption at 2.53GHz for different supply voltages

The oscillator Figure of Merit (FoM) and FoMT defined as

$$\text{FoM} = 20\log\left(\frac{f_0}{\Delta f}\right) - 10\log(P) - \mathscr{L}\{\Delta f\} \tag{3.5}$$

and

$$\text{FoMT} = \text{FoM} + 20\log\left(\frac{F_T}{10}\right) \tag{3.6}$$

where

$$F_T = 2\frac{F_{max} - F_{min}}{F_{max} + F_{min}} \tag{3.7}$$

are used to characterize the VCO at a frequency f_0, where $\mathscr{L}\{\Delta f\}$ is the phase noise at Δf offset, and P, the power consumption in mW. Figure 3.5 shows the FoM associated with phase noise measurements in Figure 3.4. The VCO FoM is 188.5dB for supply voltage of 0.7V. At 0.85V, FoM is 190.2dB with phase noise of -126.1dBc/Hz at 3MHz consuming 280μW. This is the highest FoM reported for a current reuse VCO with power consumption below 300μW[1].

An instrument screen shot of phase noise measurement for the peak FoM is shown in Figure 3.6.

Figure 3.7 shows the measured phase noise at 2.53GHz with a 0.7V supply at -30, 25 and 120°C. At 3MHz offset, worst phase noise is -120dBc/Hz at 120°C with FoM of 185dB. Phase noise variation across temperature is 2.2dB.

Figure 3.8 shows the variation in phase noise for different V_{bias} values (MN gate bias) along with the corresponding power consumption. The best phase noise power tradeoff is

[1] As of the date of publication in [23].

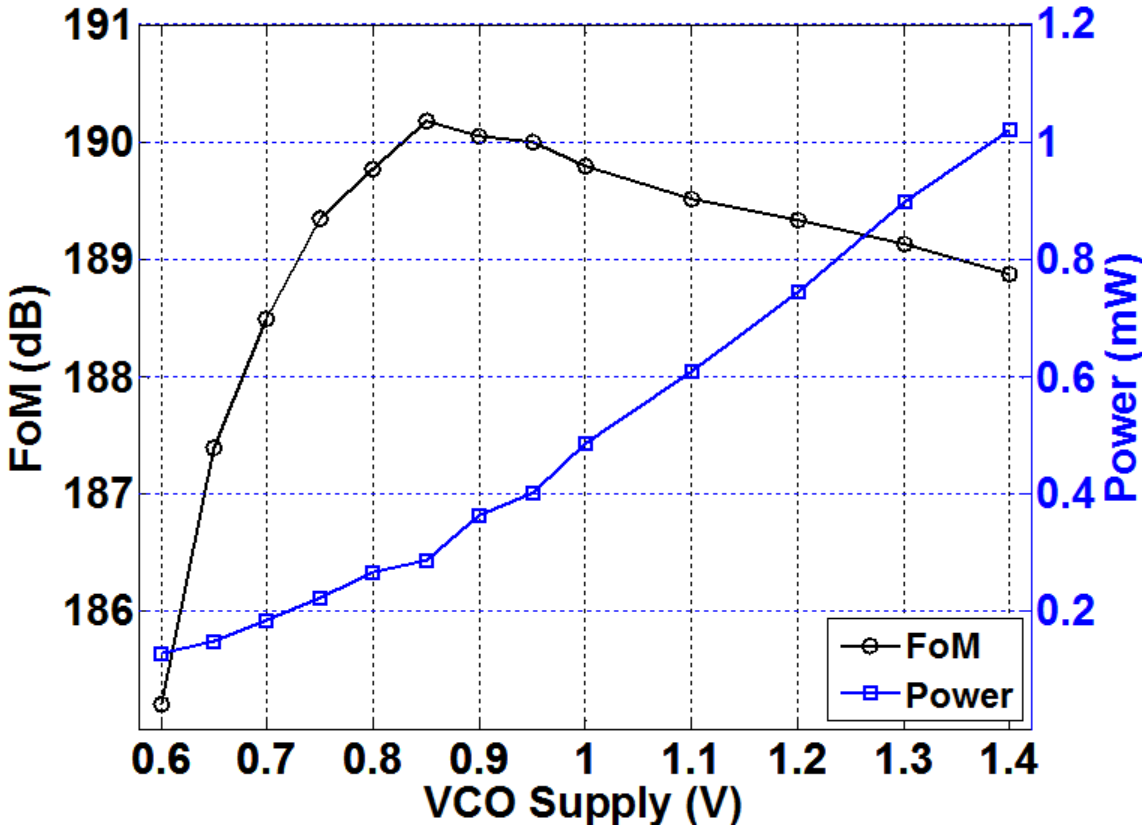

Figure 3.5: Measured VCO FoM at 2.53GHz and power consumption for different supply voltages

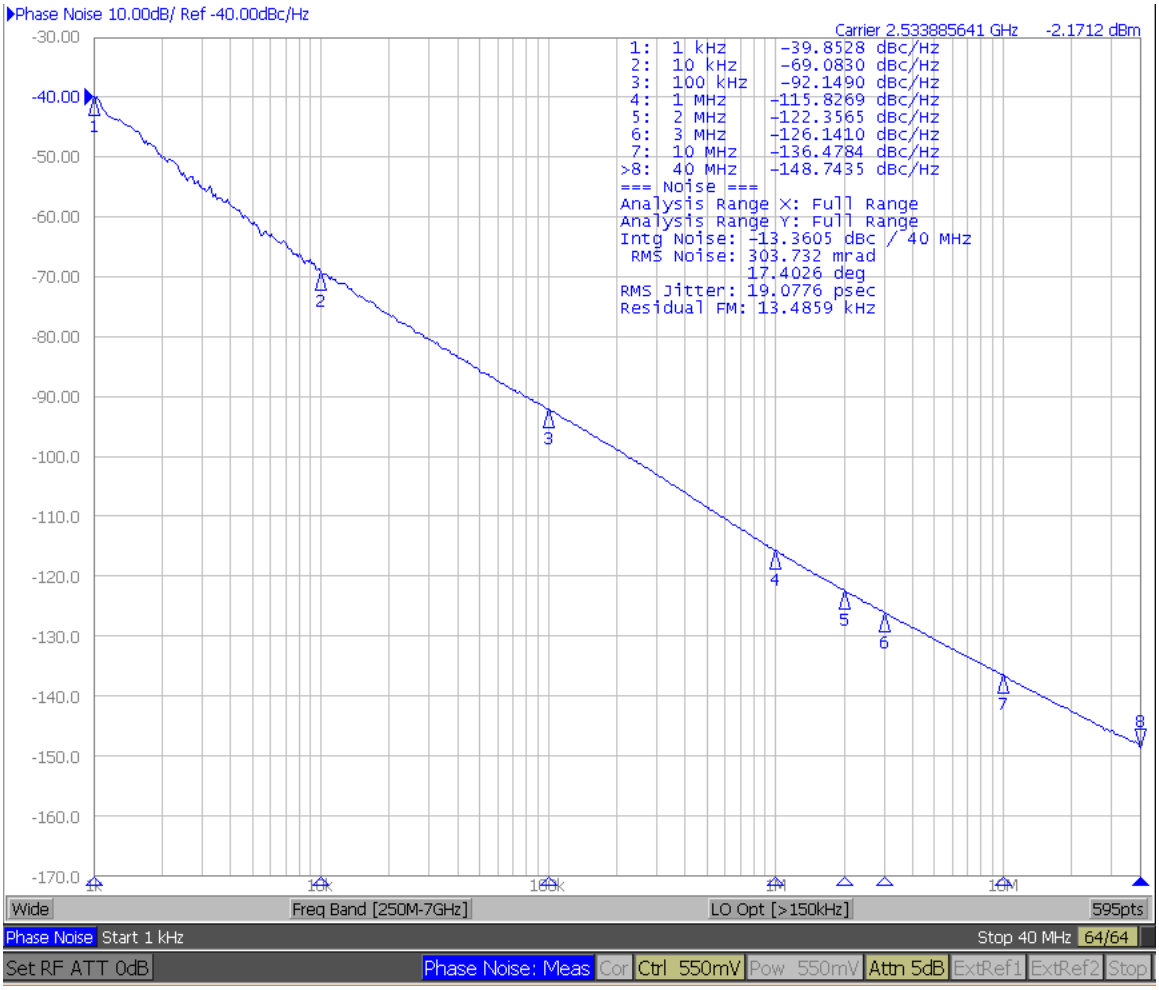

Figure 3.6: Instrument screen shot of phase noise measurement with a 0.85V supply

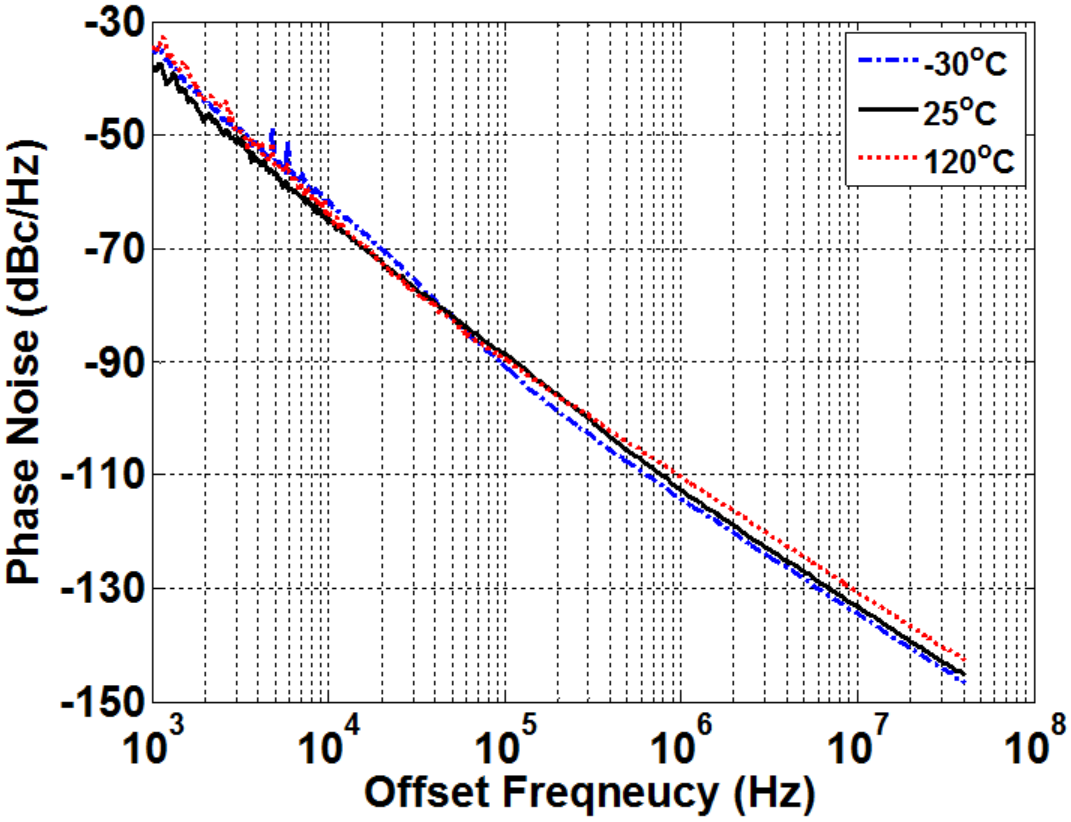

Figure 3.7: Measured phase noise at 2.53GHz over temperature

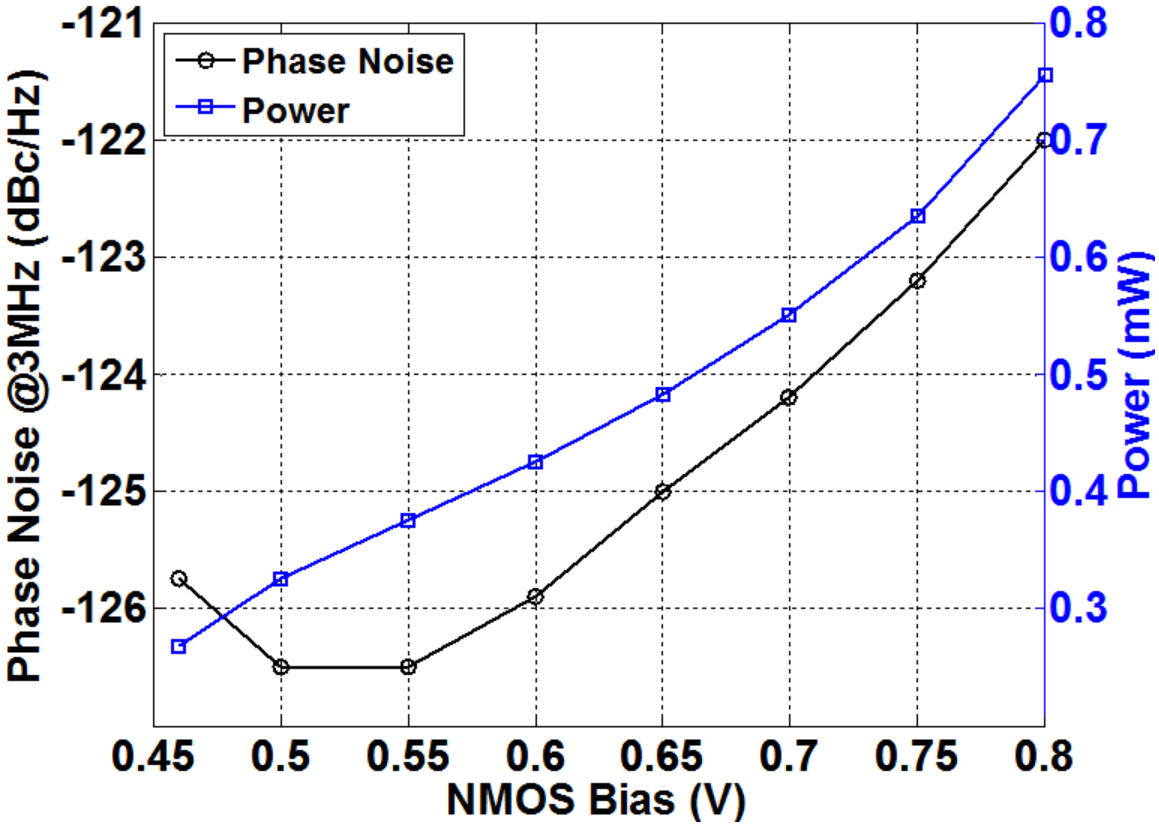

Figure 3.8: Measured phase noise at 2.53GHz versus NMOS gate bias voltage with a 0.85V supply

obtained with V_{bias} set to 0.5V. Increasing V_{bias} beyond a certain point degrades the phase noise while increasing the power consumption as MN enters the triode region.

Table 3.1 summarizes the performance of the prototype VCO with comparison to some recent low power counterparts. At 0.85V, the proposed AC coupled current reuse VCO achieves a phase noise of -126.1dBc/Hz at 3MHz offset for an oscillation frequency 2.53GHz and consumes 280μW. This corresponds to a FoM of 190.2dB which is comparable to the state of the art. Considering the 2.17GHz to 2.9GHz (29%) tuning range, the Figure of Merit with Tuning (FoMT) is 199.4dB, which is the highest, reported for any current reuse VCO[2].

[2] As of the date of publication in [23].

Table 3.1: VCO performance comparison

Parameter	**This Work**	CICC '11 [34]	CICC '11 [35]	ISSCC '12 [32]	LMWC '11 [31]	LMWC '09 [36]	ISSCC '05 [33]
Freq. (GHz)	**2.53**	1.6	5.6	3.92 (7.84/2)	3.1	3	1.97
F_T (%)	**29**	26	4	33	20	21	-
PN (dBc/Hz) at 3MHz	**-126.1**	-130	-132.3	-132.5	-121	-131	-125
$V_{DD}(V)$	**0.85**	1	0.6	1.5	1	1.5	1.25
Power (mW)	**0.28**	2.6	4.2	6	0.56	1.7	1
FoM (dB)	**190.2**	180.4	191.5	185.6	183.9	188.7	181.3
FoMT (dB)	**199.4**	188.7	183.5	195.9	189.8	195.2	-
Area (mm^2)	**0.13**	-	0.48	0.49	0.77 (w/ pads)	0.3 (w/ pads)	-
Tech.	**65nm**	65nm	0.13μm	55nm	0.18μm	0.18μm	0.18μm
Topology	**CMOS AC coupled current reuse**	NMOS QVCO	NMOS QVCO w/ cap coupling	N/PMOS combined for constant FoM	PMOS Class C w/ startup cct	CMOS Current reuse	CMOS Current reuse

CHAPTER IV

A 2.4GHz 2Mb/s Digital PLL-based Transmitter for 802.15.4 in 130nm CMOS

4.1 Background

The IEEE 802.15.4 standard specifies a 2.4GHz PHY that uses Offset-Quadrature Phase Shift Keying (O-QPSK) modulation with half sine pulse shaping [15]. This modulation is equivalent to Minimum Shift Keying (MSK) and MSK transmitters are typically implemented using cartesian or fractional-*N* PLL based modulators. Cartesian transmitters use in phase and quadrature paths requiring DACs, low pass filters, and RF mixers. These tend to be power hungry and the use of analog components makes this approach unsuitable for nanometer CMOS processes.

Although many 2.4GHz band transmitter/PLL designs are reported, most have some limitations. [37] and [38] are based on analog fractional-*N* PLLs and use components such as charge pumps and analog low pass filters, making them less suitable for nanometer CMOS. Although [39] employs a digital fractional-*N* PLL, it suffers from fractional spurs due to nonlinearity and finite resolution of the time-to-digital converter (TDC). Furthermore,

TDC based digital PLLs require extensive calibration of delay elements to reduce spurs.

The digital PLL in this work is based on the design reported in [6, Ferriss, Flynn]. However, there are several important improvements distinguishing the ZigBee TX presented here:

- A low power compact 0dBm PA is designed to drive a 50Ω antenna discussed in Section 4.5. This is more than 20dB improvement compared to [6, Ferriss, Flynn]
- The VCO used in [6, Ferriss, Flynn] is unable to meet the ZigBee center frequency and tuning range. Therefore, the VCO in this work is re designed to have better phase noise, accurate center frequency, and ZigBee compliant tuning range. This is mainly due to new *LC* tank outlined in Section 4.6
- The current draw of the DAC is reduced by 66% to improve the TX efficiency
- The frequency modulation rate in this work is 2Mb/s, twice what is reported in [6, Ferriss, Flynn]

In this work, a digitally dominant ΣΔ fractional-*N* PLL based transmitter achieves an MSK modulation rate of 2Mb/s. A compact power amplifier that does not require an output matching network delivers -2dBm of output power to a 50Ω load. The prototype transmitter is largely comprised of synthesized digital logic and the only analog components are a VCO, two DACs, and a multiplexer. An oversampled one bit phase quantizer is used instead of a TDC as a phase detector. Because the phase detector is formed with a single flip-flop, it does not require calibration of delay elements and is more linear therefore reducing spurs associated with the use of multi bit TDCs. Furthermore, a high reference frequency places

the fractional spurs out of band. A self calibrated two point PLL modulation scheme allows modulation rates that far exceed the loop bandwidth.

4.2 Transmitter Architecture

Figure 4.1 shows a block diagram of the prototype transmitter. The transmitter is comprised of a mostly digital fractional-*N* PLL modulator and a two stage power amplifier. A digital Phase Detector (PD) compares the reference clock and the divided down VCO output. A digital integrator averages the PD output. This averaged output sets the VCO varactor voltage. The output of the integrator is converted to the analog domain by a resistor string ΣΔ DAC. As explained later, two control paths, incorporating two DACs and a digital sampler, enable a self calibrated two point modulation scheme. A two stage PA delivers an output power of up to -2dBm to a 50Ω load. A programmable divider is controllable from 8 to 15. A second order ΔΣ modulator controls the divider.

4.3 Phase Detector Overview

Figure 4.2 shows a block diagram of the phase detector first presented in [40]. A single flip-flop oversamples the phase difference, $\Delta\phi$, between the reference and the divided down VCO. The quantized phase information is also fed back to the input of the ΣΔ divider to keep the phase difference between the reference and divider output small. The operation of this feedback loop is similar to that of a delta modulator (Figure 4.2) which consists of a feedback loop with a quantizer in forward path, and an integrator in the feedback path. Integration in the feedback path is achieved by feeding quantized phase information back to

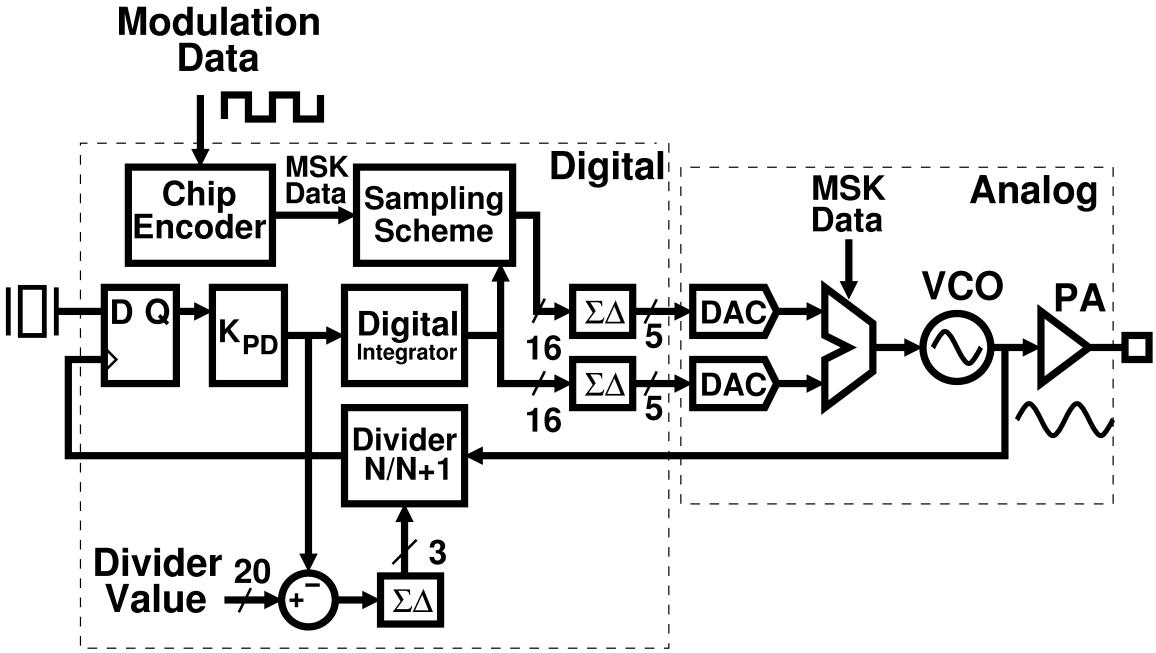

Figure 4.1: The prototype 802.15.4 transmitter

the frequency control of the divider. The delta modulator helps keep $\Delta\phi$ smaller than one quantization step. The quantization noise from the fractional-N $\Sigma\Delta$ modulator of the divider acts as dither for the oversampled phase quantizer. The integrated output (digital) of the phase detector is a digital word equal to the phase difference between reference clock and divided down VCO.

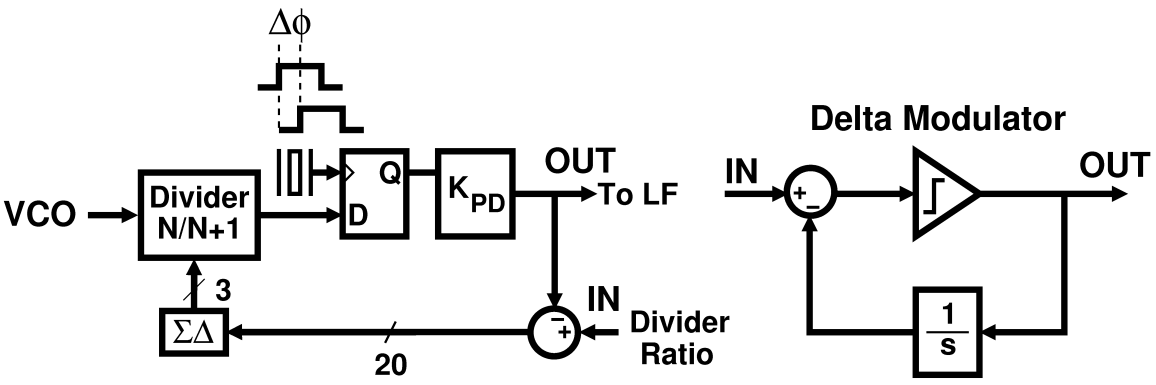

Figure 4.2: The digital phase detector and equivalent model which is a delta modulator [6]

4.4 Frequency Switching Scheme

MSK modulation is a form of FSK with frequency deviation of $1/(2 \times T_C)$. For 802.15.4, the bit period T_C is 1/(2MHz) giving a frequency deviation of 500kHz relative to the channel frequency. A two point self calibrated frequency switching modulation scheme enables modulation rates much higher than the PLL bandwidth. A block diagram of the frequency-switching scheme is shown in Figure 4.3 [6]. VCO control is split into two paths, one path for each frequency f^+ and f^-. During each bit period the loop attempts to settle to either f^+ or f^-. At the end of each bit period, the digital value of the VCO control is sampled. The difference, delta, between the control word for f^+ and f^-, is calculated and updated. This difference, delta, is added to the VCO control for frequency f^+ to give an initial VCO control value for frequency f^-. As the modulation continues to switch between f^+ and f^- , the estimate of delta converges to the correct VCO input difference for the required frequencies f^+ and f^-. When delta converges, then to a first order, the frequency switching rate is no longer dependent on the settling time of the PLL because the correct input to the VCO is readily applied for each frequency change. An example of settling behavior is shown in Figure 4.3, where after some data transitions, accurate VCO control inputs for the two frequencies are determined.

Figure 4.4 shows a more detailed block diagram of the modulation scheme. A digital IIR filter averages the difference between f^+ and f^+ and two control paths for the VCO are formed with $\Sigma\Delta$ resistor string DACs. An analog multiplexer switches between the two VCO control voltages generated by the DACs at each data transition.

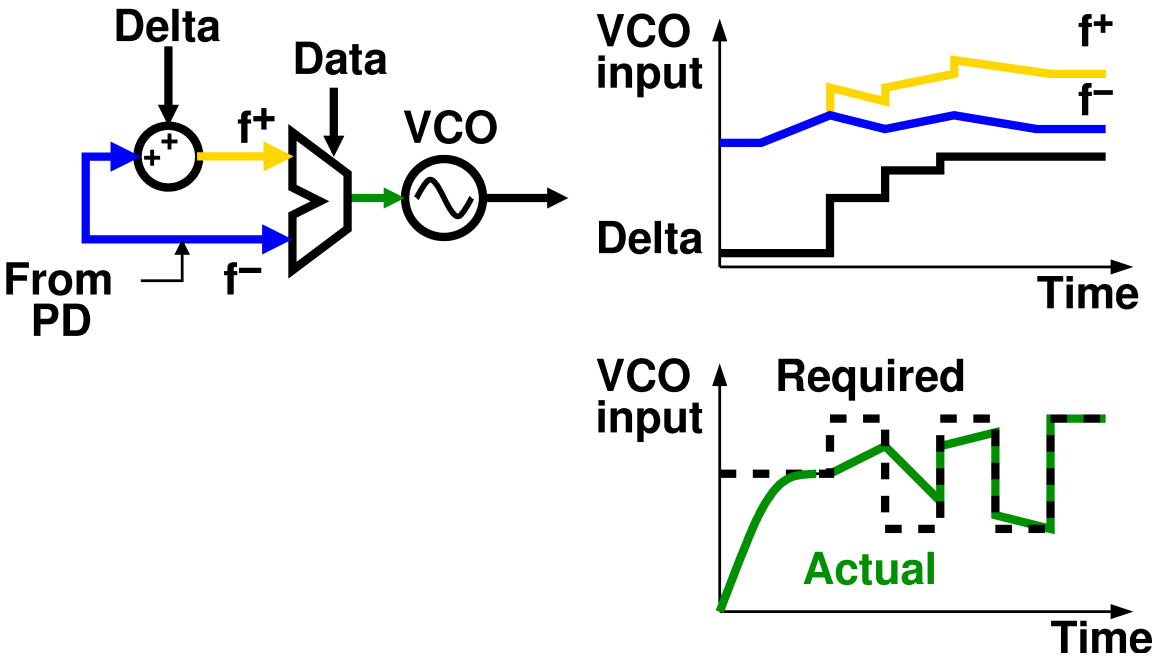

Figure 4.3: The two point frequency modulation scheme operation and an example settling behavior [6]

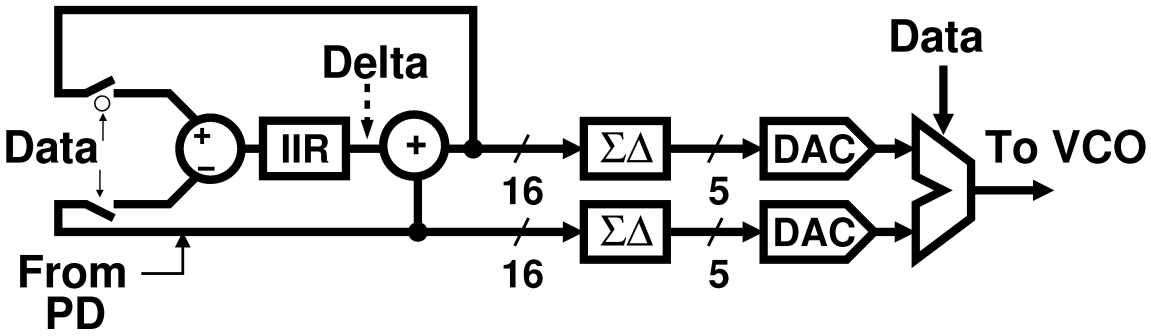

Figure 4.4: Implementation details for the two point modulation scheme [6]

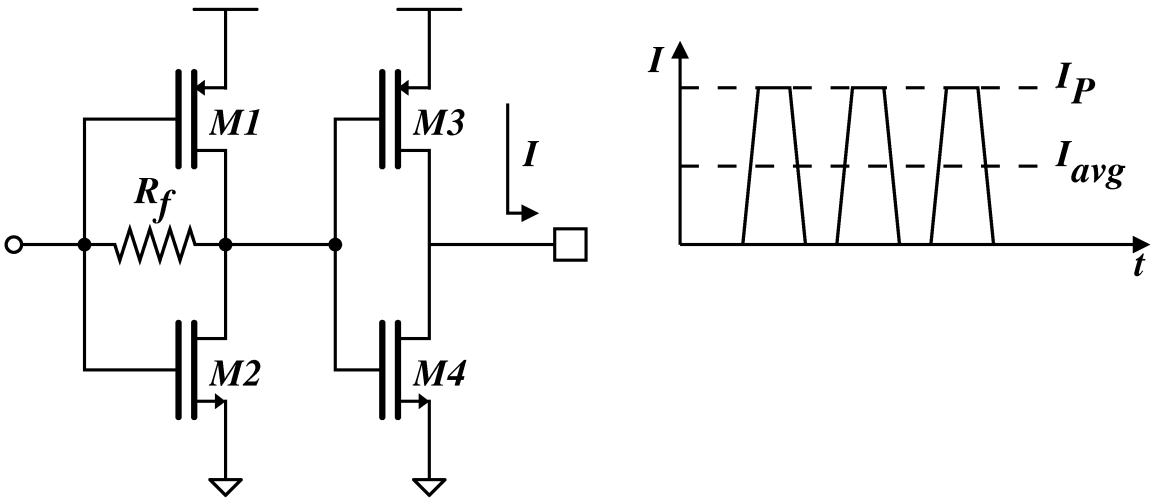

Figure 4.5: The two stage resistor feedback inverter based power amplifier

4.5 Power Amplifier

Figure 4.5 depicts the power amplifier used in this work. The PA is comprised of two stages. The first stage is an inverter amplifier with resistive feedback. Because of the feedback resistor R_f, the first stage of the PA is self biased. Linearity is improved as the bias point of the first stage is set at the middle of the analog (high gain) swing range. The input resistance of the first stage is approximated by $R_{in} \approx 1/(gm_1 + gm_2)$, and the first stage is sized to have a large input resistance to avoid loading the VCO. The second stage is sized to deliver 0dBm to a 50Ω load.

There are no internal/external matching circuits or inductors used in this PA yielding a compact area. The PA efficiency is defined as the output power divided by average DC power given by Equation 4.1 where I_{avg} is estimated to be half of I_p, the peak current delivered to the load. The PA is designed to have a 0dBm output power with simulated efficiency of 17%.

$$\text{PA Efficiency} = \frac{P_{out}}{P_{DC}} \approx \frac{I_p^2 \cdot R_L}{V_{DD} \cdot I_{avg}} \tag{4.1}$$

4.6 Voltage Controlled Oscillator

The voltage controlled oscillator used in this transmitter is shown in Figure 4.6. An NMOS, voltage biased *LC* topology is chosen due to its simplicity and good phase noise. A 6nH inductor with center tap provides the DC bias and an NMOS cross coupled pair compensates the tank loss during oscillation. The varactors are formed by NMOS devices in an n-well. The source and drain of the varactor is shorted together and VCO control voltage, V_{ctrl}, is applied to the gate. Coarse tuning is achieved by a 5 bit binary weighted bank of differential MiM capacitors with a series NMOS switch.

An example of a coarse tuning capacitor circuit used in this work is shown in Figure 4.6 [41]. V_{sw} is set to V_{DD} when the switch is OFF and to GND when the switch is ON. This method results in the largest achievable voltage difference (within the oxide breakdown limits) across the NMOS switch during both the ON and OFF states. The large overdrive during ON stage improves the Quality factor (Q) of the tank by reducing the NMOS switch ON resistance. The large overdrive during the OFF state avoids leakage based noise injection. Under steady state oscillation where a coarse tuning capacitor is OFF, leakage current is greatly reduced since both V_{GS} and V_{GD} of the NMOS switch are biased around a negative voltage ($-V_{DD}$). This results in a significantly improved phase noise compared to [6, Ferriss, Flynn].

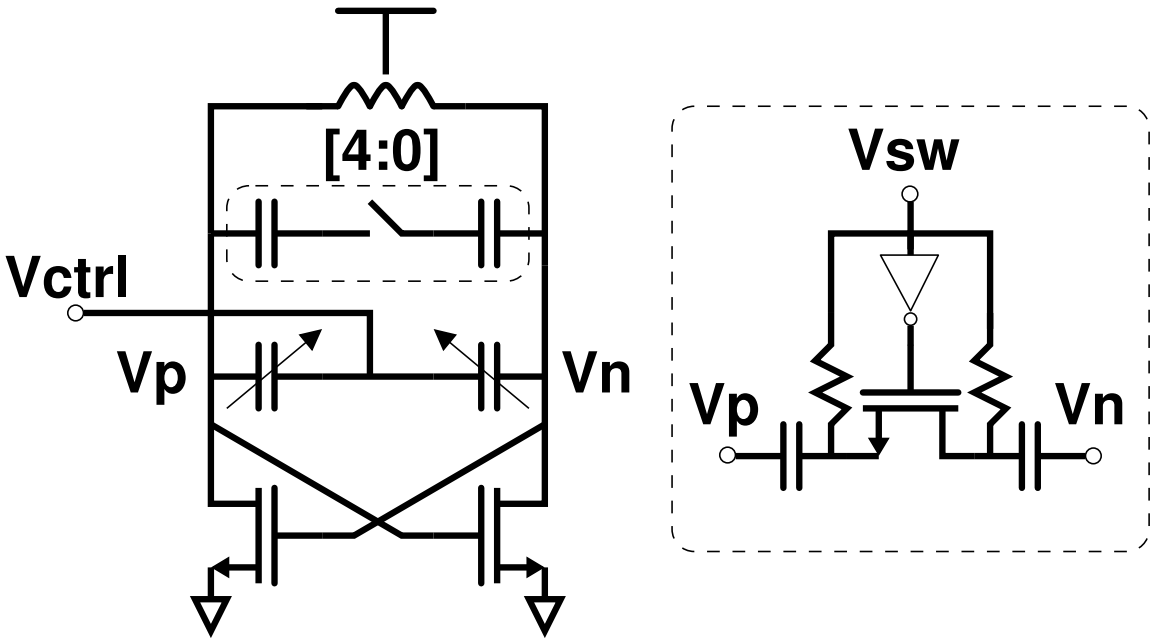

Figure 4.6: The VCO used in the transmitter

4.7 ΣΔ Digital to Analog Converter

A first order ΣΔ DAC is used to apply the digital loop filter output word to the analog VCO used in the DPLL. An alternative approach is to directly modulate a number of small capacitors in the *LC* tank. However, this method is complex and results in a large power consumption [42]. This is mainly due to the difficulty of reducing the capacitor switching noise (*i.e.,* the effective quantization noise of the capacitor DAC) at the VCO output. Methods such as dynamic element matching and use of a high frequency (*e.g.,* 400MHz), high order ΣΔ modulator are needed to reduce this noise. Therefore, we use a simple ΣΔ DAC at the digital filter output to set the VCO varactor voltage [40].

A block diagram of the ΔΣ DAC is shown in Figure 4.7. The 32 bit digital loop filter output word is converted to a 5 bit word using a first order digital ΔΣ modulator. The ΔΣ modulator clock is 200MHz which is the same as the PLL reference frequency. A first

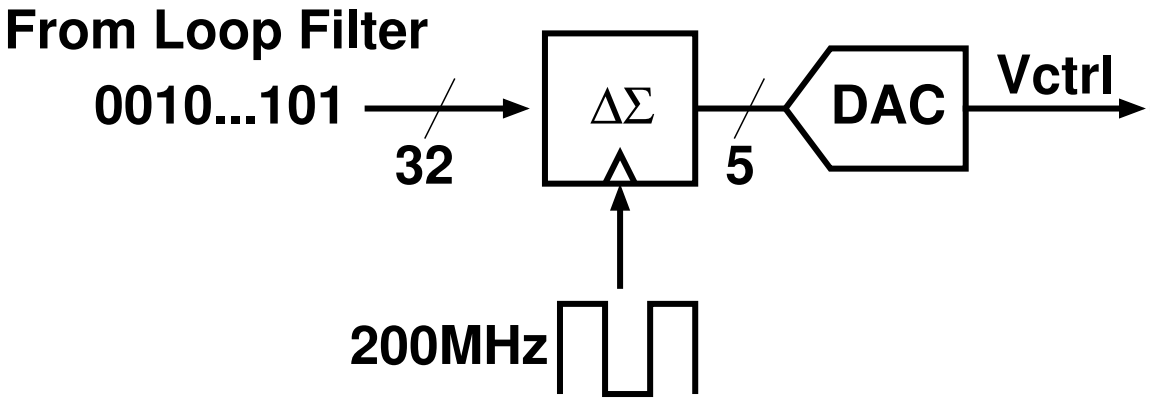

Figure 4.7: The ΔΣ DAC block diagram

order ΔΣM is intentionally chosen as the output increments by only one value at each clock edge for a DC input.[1] When the PLL is settled and locked, the digital loop filter outputs a constant DC (or very close to DC) value. Therefore, only one DAC code changes most of the time. This greatly simplifies the resistor string DAC design as it eliminates the need for high linearity which could otherwise increase the power consumption and area. A reference frequency of 200MHz is chosen to sufficiently shape the the ΔΣM quantization noise to higher frequencies. It is important to note that the DAC clock frequency is not limited to the PLL reference frequency. This is because the DAC can be clocked from the VCO and divider path which can run at a much higher rate than the overall PLL reference. In this work, PLL reference of 200MHz, together with some RC low pass filters resulted in sufficient reduction of the ΔΣ DAC noise at the PLL output.

4.8 PLL Small Signal Frequency Domain Model

In this section, we derive the frequency domain small signal model for the DPLL. First, the frequency domain models for various sub blocks used in the DPLL are outlined. Then,

[1] This is in contrast to a higher order ΔΣM that has a wider output range for a DC input [43]

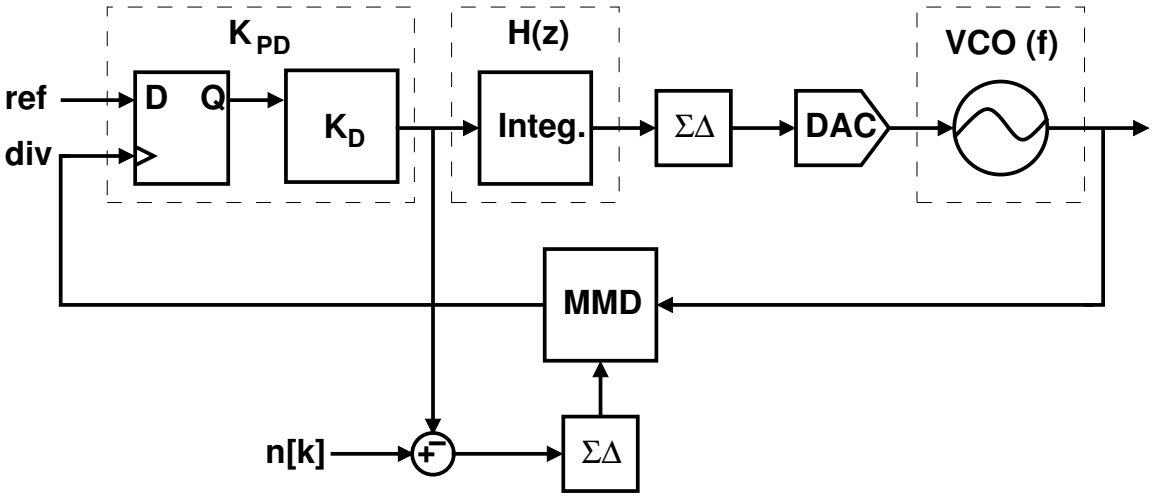

Figure 4.8: Simplified PLL block diagram

the overall frequency domain small signal model for the PLL is presented. It is important to note that because of the feed forward path from phase detector output to the ΔΣM input, the transfer function of the flip flop phase detector based DPLL is different than a generic PLL. The methodology for small signal modeling and noise calculation is adopted from Perrott's classic work [44].

The simplified DPLL block diagram (two point modulation removed) is shown in Figure 4.8. For small signal analysis, the low pass filter at DAC output (which is there to suppress the DAC quantization noise) is ignored since its corner frequency is well outside the PLL bandwidth and therefore has little effect on the loop. In our small signal analysis, the phase detector gain is K_{PD}, the digital integrator transfer function is $H(z)$, and the VCO transfer function is $VCO(f)$.

4.8.1 Phase Detector Model

Perhaps the most interesting transfer function derivation belongs to the phase detector, so we begin there. The phase detector used in this DPLL is a single D-type flip flop where a

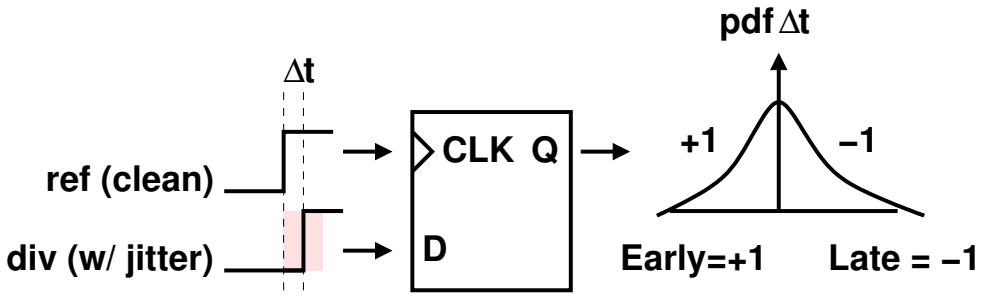

Figure 4.9: Phase detector operation

clean reference is applied to the clock input, and the PLL divider output is applied to the D input. Therefore, VCO edges (at the divider output), which have jitter, are sampled by the clean reference edges as shown in Figure 4.9. For a large phase difference (time difference) $\Delta\phi$ (Δt) between ref and div, the flip flip will act as a limiter where the output, Q, is stuck at +1 if div is early, and -1 if div is late. This behavior is large signal and therefore useless in deriving a small signal model for the DPLL. In a phase locked synthesizer, $\Delta\phi$ is small. And, because div edges have jitter, Q is no longer stuck at +1 or -1. Rather, it will toggle between +1 and -1 with a distribution that depends on the jitter of div edges (Figure. 4.9).

To derive the small signal phase detector gain, K_{PD}, we must look at the statistical behavior of the flip flop output, Q. We define the average of the phase detector output as $\mu \triangleq < Q >$. This parameter is useful in PLL small signal calculations. We need a statistical method to calculate μ. If we assume a certain Probability Density Function (PDF) for divider jitter[2] as shown in Figure 4.9, the probability that div is early, $Pr(\text{early})$, and the probability that div is late, $Pr(\text{late})$, is the area under +1 and -1, respectively. We obtain

$$\mu = (+1)Pr(\text{late}) + (-1)Pr(\text{early}). \tag{4.2}$$

[2]The PDF will be calculate later

As a quick check, in the case where div is early half the time, and late the other half, μ becomes zero since $Pr(\text{early}) = Pr(\text{late}) = 0.5$. A different μ is obtained when $\Delta\phi$ is changed by a small amount. Therefore, the phase detector small signal gain is defined as

$$K_{PD} = \frac{\delta\mu}{\delta\phi}. \tag{4.3}$$

Phase detector gain, K_{PD}, calculation is outlined below for the case where the div edges have a Gaussian distribution.[3]. Starting with $Pr(\text{late})$ calculation, first, an expression for average output μ is obtained. Then, K_{PD} is obtained using the expression for μ.

$$Pr(\text{late}) = \frac{1}{\sigma\sqrt{2\pi}} \int_0^\infty e^{\frac{(-x+\phi)^2}{2\sigma^2}} dx, \tag{4.4}$$

where σ is the standard deviation of div jitter, and ϕ the phase difference at phase detector input. A change of variables yields

$$Pr(\text{late}) = \frac{1}{\sqrt{2\pi}} \int_{\frac{\phi}{\sigma}}^\infty e^{\frac{-y^2}{2}} dy. \tag{4.5}$$

Using the Q function,

$$Pr(\text{late}) = Q\left(\frac{\phi}{\sigma}\right) \approx \frac{1}{2} - \frac{\phi}{\sigma\sqrt{2\pi}}. \tag{4.6}$$

Using the relationship $\mu = 2 \times Pr(\text{late}) - 1$, letting $\sigma = \sigma_{\Delta t}$ (where $\Delta t = \Delta\phi \frac{T_{ref}}{2\pi}$), and taking the derivative,

$$K_{PD} = \frac{1}{\sigma_{\Delta t}\sqrt{2\pi}}. \tag{4.7}$$

[3]This is a reasonable assumption for frac-N $\Delta\Sigma$ PLLs as shown in [45]

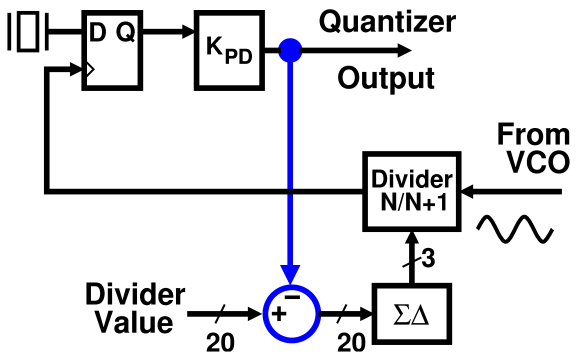

Figure 4.10: Phase detector feedforward path

This expression is similar to the result reported by Da Dalt in [46].

Since the derived the phase detector small signal gain depends on standard deviation of phase detector input, $\sigma_{\Delta t}$ (*i.e.,* standard deviation of $[t_{ref} - t_{div}]$), we need to obtain $\sigma_{\Delta t}$ to calculate K_{PD}.

In a Bang Bang (BB) integer-N PLL that uses a similar phase detector, the calculation of $\sigma_{\Delta t}$ is rather straightforward. As outlined in [47], $\sigma_{\Delta t}$ is directly related to the VCO jitter (phase noise). Therefore, $\sigma_{\Delta t}$ (and consequently K_{PD}) is readily obtained from stand-alone VCO phase noise simulations. However, we are unable to use this method to obtain $\sigma_{\Delta t}$ for the DPLL in this work because the ΔΣM in the feedback divider affects $\sigma_{\Delta t}$. The time difference at the input of the phase detector due to the ΔΣM is given by

$$T_{VCO} \sum_{k=0}^{n-1} e_{\Delta\Sigma}[k], \tag{4.8}$$

where T_{VCO} and $e_{\Delta\Sigma}[k]$ are VCO period and ΔΣM quantization noise, respectively. It is important to note that because of the fractional divider, this variation is now larger than that of an integer-N PLL. Therefore, the PD gain (which is is function of the variance of this

variation) is different compared to the integer-N PLL. The variance is given by

$$\sigma^2_{\Delta t,\Delta\Sigma} = \frac{T^2_{VCO}}{6}, \tag{4.9}$$

and

$$\sigma^2_{\Delta t,\Delta\Sigma} = \frac{T^2_{VCO}}{2}, \tag{4.10}$$

for a ΔΣM order of 2 or 3, respectively [48]. The ΔΣM used in DPLL is second order. In addition to the deterministic jitter of ΔΣM, the VCO jitter also contributes to the overall Δt at the phase detector input. An approximate relationship for contribution of VCO jitter (σ_{VCO}), based on loop parameters is derived in [47] given by

$$\sigma_{\Delta t,VCO} \approx \sqrt{\frac{\pi}{8}\frac{\sigma^2_{VCO}}{\beta K_T}}, \tag{4.11}$$

where σ^2_{VCO}, β, and K_T are variance of open loop VCO jitter, loop filter proportional gain, and VCO time domain gain, respectively. VCO time domain gain, K_T can be obtained from the more common VCO frequency domain gain, K_v, as follows:

$$F_{VCO} = F_0 + K_v * V_{in}, \tag{4.12}$$

where F_{VCO}, V_{in}, and F_0 are the VCO frequency, the varactor voltage, and the VCO frequency with $V_{in} = 0$V, respectively. K_T, defined as $\frac{\delta T_{VCO}}{\delta V_{in}}$ is calculated below: Using Equation 4.12,

$$T_{VCO} = \frac{1}{F_0 + K_v V_{in}}. \tag{4.13}$$

Factoring out F_0, we obtain

$$T_{VCO} = \frac{1}{F_0}\frac{1}{1+V_{in}\frac{K_v}{F_0}}, \tag{4.14}$$

assuming $V_{in}\frac{K_v}{F_0} \ll 1$,

$$T_{VCO} \approx \frac{1}{F_0}\left(1+V_{in}\frac{K_v}{F_0}\right). \tag{4.15}$$

Therefore, K_T is obtained by taking the derivative wrt to V_{in}, that is

$$K_T \approx \frac{K_v}{F_0^2}. \tag{4.16}$$

The standard deviation of jitter at phase detector input is the sum of the two contributions given by

$$\sigma_{\Delta t} = \sigma_{\Delta t,VCO} + \sigma_{\Delta t,\Delta\Sigma}. \tag{4.17}$$

4.8.2 Digital Integrator, DAC, VCO, and Divider Models

The digital accumulator transfer function is given by

$$H(z) = K_I\frac{z^{-1}}{1-z^{-1}} \approx \frac{K_I}{j2\pi fT}, \tag{4.18}$$

where K_I is the integrator gain.

The ΣΔM transfer function is unity. The DT to CT conversion of the DAC is approximated as $1/T$.

The VCO is modeled as

$$VCO(f) = \frac{K_v}{jf}, \tag{4.19}$$

where K_v is the VCO gain often in units of MHz/V.

The integer part of the divider is simply modeled as

$$DIV(f) = \frac{1}{N}, \tag{4.20}$$

where N is the divider value. The fractional part of the divider, however, is a discrete time signal because of the $\Delta\Sigma$ modulator and is therefore modeled as

$$\frac{\phi_n[k]}{n[k]} = 2\pi \frac{z^{-1}}{1-z^{-1}}, \tag{4.21}$$

where $n[k]$ is the deviation in divider value and $\phi_n[k]$ is the output of the divider after a discrete time accumulator. The discrete time accumulator in the transfer function is because the divider output is a phase signal, whereas $n[k]$ causes an incremental change in frequency of divider output. Therefore, an integration from frequency to phase is needed.

In DPLL, we often go between Continuous Time (CT) and Discrete Time (DT) blocks. By using a pseudo-continuous approximation, the frequency domain transfer function are given by

$$CT \longrightarrow DT = \frac{1}{T}, \tag{4.22}$$

and

$$DT \longrightarrow CT = T. \tag{4.23}$$

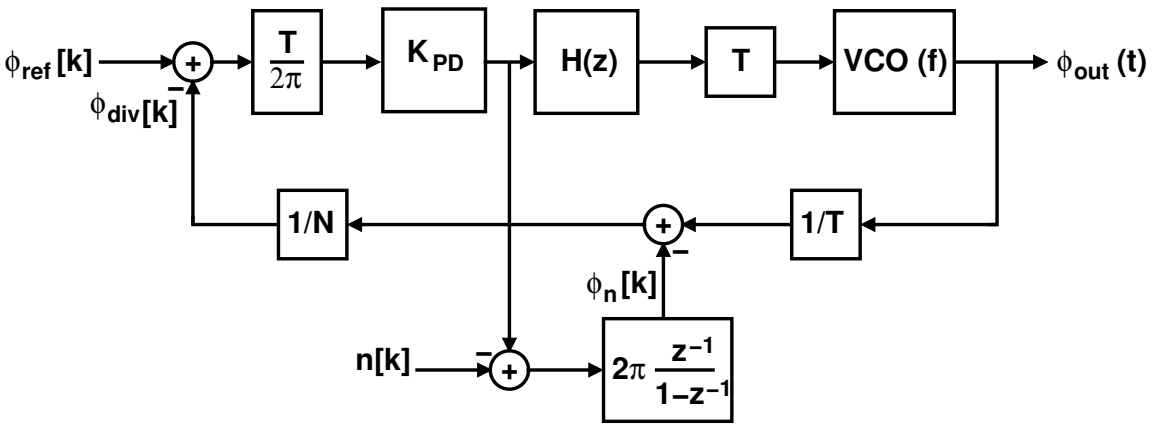

Figure 4.11: Frequency domain model of PLL

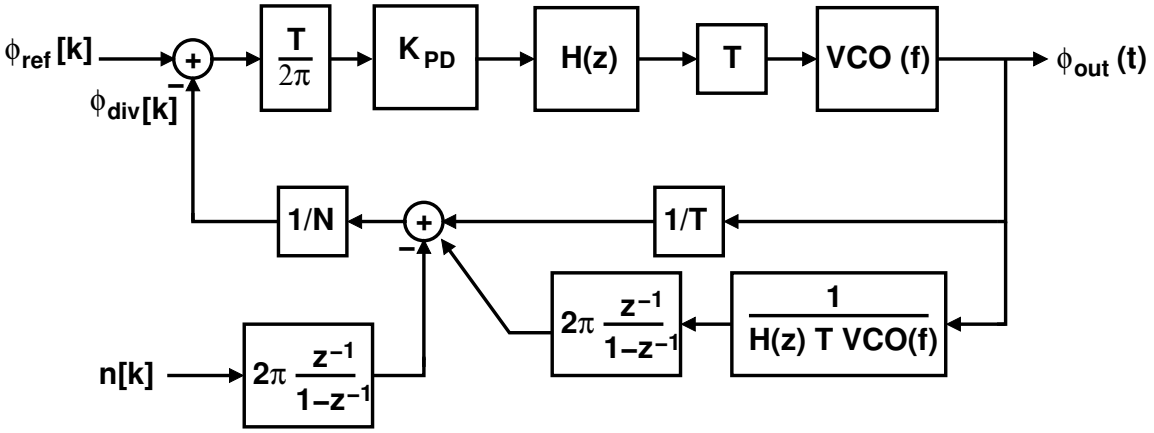

Figure 4.12: Frequency domain model of PLL, re-drawn for straightforward transfer function and noise calculations

4.8.3 PLL Transfer Function

A block diagram of the overall PLL frequency domain model is shown in Figure 4.11. The addition is $\frac{T}{2\pi}$ before K_{PD} is to convert from phase to time since the earlier K_{PD} derivation is in terms on input time difference, Δt. The frequency domain model is re-drawn using signal flow rules as shown in Figure 4.12. This not only helpful in intuitive understanding of the effect of the feed forward path in overall transfer function, it will also allow for easier signal and noise transfer function calculations. First, we derive the PLL overall transfer

function, $\frac{\phi_{out}}{\phi_{ref}}$. To obtain the transfer function from PLL input to output, we first ignore the fractional divider (*i.e.,* let $n[k] = 0$). It is helpful to obtain the loop gain, $LG(f)$ right away as it is used in all signal and noise transfer function calculations that follow. Using the frequency domain model depicted in Figure 4.12, loop gain is obtained

$$LG(f) = \frac{T}{2\pi} K_{PD} H(z)\, T\, VCO(f) \left(1/T + \frac{1}{H(z)\, T\, VCO(f)} 2\pi \frac{z^{-1}}{1-z^{-1}} \right) DIV(f) \quad (4.24)$$

Expanding using Equations 4.7, 4.18, 4.19, and 4.20,

$$LG(f) = \frac{T}{2\pi} K_{PD} \frac{K_I}{j2\pi fT} T \frac{K_v}{jf} \left(1/T + \frac{1}{K_I \frac{z^{-1}}{1-z^{-1}} T \frac{K_v}{jf}} 2\pi \frac{z^{-1}}{1-z^{-1}} \right) \frac{1}{N}, \quad (4.25)$$

which simplifies to

$$LG(f) = \frac{1}{2\pi} K_{PD} \frac{K_I}{j2\pi f} \frac{K_v}{jf} \left(1 + \frac{1}{K_I} \frac{j2\pi f}{K_v} \right) \frac{1}{N}. \quad (4.26)$$

In order to obtain the poles and zeros, it is helpful to convert Equation 4.26 to S-domain, *i.e.,*

$$LG(s) = K_{PD} \frac{K_I K_v}{s^2} \left(1 + \frac{s}{K_I K_v} \right) \frac{1}{N}. \quad (4.27)$$

The loop gain, $LG(s)$, has two poles at ω_{p1}, ω_{p2} equal to zero, and one zero at $\omega_z = -K_I K_v$. Therefore, appropriate selection of K_I and K_v results in a stable transfer function when feedback loop is closed. It is also important to not that it is the feedforward path that results in a zero in the loop gain transfer function. Without the feedforward path, loop gain will have two integrators and no zeros, and is therefore always unstable.

Using Equation 4.27, PLL transfer function is readily obtained as

$$\frac{\phi_{out}}{\phi_{ref}}(s) = \frac{N}{1+\frac{s}{K_I K_v}} \frac{LG(s)}{1+LG(s)}, \tag{4.28}$$

with a DC gain equal to division ratio, N.

4.9 PLL Phase Noise Analysis

In this section, we will use the PLL small signal frequency domain model to calculate the overall PLL noise. First, we derive the output referred transfer function for major noise sources. Then, we compute the noise contribution at the PLL output due to each noise source. Finally, we add all the output referred noise power spectral densities to obtain the total PLL output phase noise. The noise sources considered are

1. Reference noise, ϕ_r
2. DAC $\Delta\Sigma$ quantization noise, ϕ_{DAC}
3. VCO phase noise, ϕ_{vco}
4. $\Delta\Sigma$ divider quantization noise, ϕ_{div}

The noise insertion points are shown in Figure 4.13

Furthermore, since both discrete time and continuous time signals are present, the following equations need to be applied properly for power spectral density calculations [49].

Case 1) CT input $x(t)$ fed to CT filter $H(f)$ to produce a CT output $y(t)$:

$$S_y(f) = |H(f)|^2 S_x(f). \tag{4.29}$$

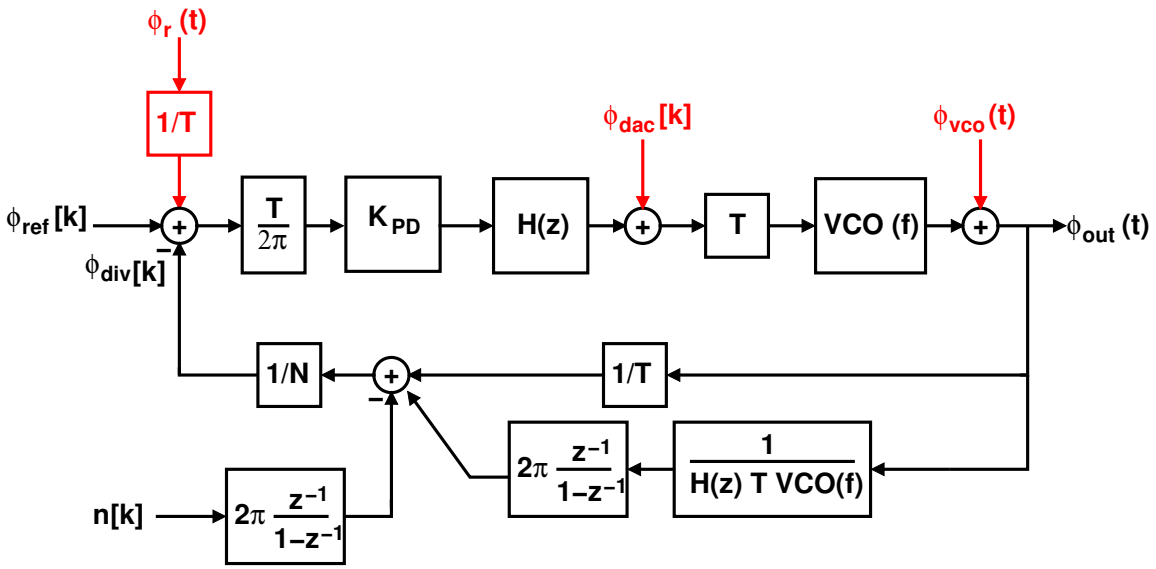

Figure 4.13: Frequency domain model of PLL with various noise insertion points

Case 2) DT input $x(k)$ fed to CT filter $H(f)$ to produce a CT output $y(t)$:

$$S_y(f) = \frac{1}{T}|H(f)|^2 S_x(e^{2\pi fT}). \tag{4.30}$$

4.9.1 Noise Transfer Function for PLL Blocks

The noise transfer function from reference to output of the PLL is obtained as

$$\frac{\phi_{out}}{\phi_r}(f) = \frac{N}{1+\frac{j2\pi f}{K_I K_v}} \frac{LG(f)}{1+LG(f)}. \tag{4.31}$$

The noise transfer function from DAC quantization noise to PLL output is given by

$$\frac{\phi_{out}}{\phi_{dac}}(f) = \frac{N}{\frac{T}{2\pi}.K_{PD}.\frac{K_I}{j2\pi fT}\left(1/T+\frac{j2\pi f}{TK_I K_v}\right)} \frac{LG(f)}{1+LG(f)}. \tag{4.32}$$

It is noted that due to DT to CT signal flow, Equation 4.30 is used later on for the PSD

calculation.

The noise transfer function from VCO output to PLL output is given by

$$\frac{\phi_{out}}{\phi_{vco}}(f) = \frac{1}{LG(f)} \frac{LG(f)}{1+LG(f)}. \tag{4.33}$$

The ΔΣM quantization noise transfer function to PLL output is calculated

$$\frac{\phi_{out}}{\phi_{div}}(f) = 2\pi \frac{e^{-j2\pi fT}}{1-e^{-j2\pi fT}} \frac{T}{\left(1+\frac{j2\pi f}{K_I K_v}\right)} \frac{LG(f)}{1+LG(f)}. \tag{4.34}$$

4.9.2 PLL Output Noise Calculation

Now that all the relevant noise transfer functions are obtained, we can calculate the power spectral density of noise at PLL output because of each noise source.

A PLL reference with noise density, $S_r(f)$, contributes to the PLL output noise given by

$$S_{out,r} = \left| \frac{\phi_{out}}{\phi_r}(f) \right|^2 S_r(f). \tag{4.35}$$

PLL reference, commonly in the form of a crystal oscillator in the MHz range, comes with a well defined noise density $S_r(f)$.

A ΣΔ DAC with white quantization noise density, $S_{dac}(f) = \frac{1}{12}$, and a first order noise shaping transfer function, $NTF = 1 - z^{-1}$, contributes to the PLL output noise given by

$$S_{out,dac} = \frac{1}{T} \left| \frac{\phi_{out}}{\phi_{dac}}(f) \right|^2 \left| 1 - e^{-2\pi fT} \right|^2 S_{dac}(f). \tag{4.36}$$

Similar to the DAC, a ΣΔ divider with white quantization noise density, $S_{div}(f) = \frac{1}{12}$,

and a second order noise shaping transfer function, $NTF = \left(1 - z^{-1}\right)^2$, contributes to the PLL output noise given by

$$S_{out,div} = \frac{1}{T} \left| \frac{\phi_{out}}{\phi_{div}}(f) \right|^2 \left| \left(1 - e^{-2\pi f T}\right)^2 \right|^2 S_{div}(f). \tag{4.37}$$

To obtain the VCO noise contribution, SpctreRF transistor level simulation are performed on a phase noise optimized VCO to obtain the noise density $S_{vco}(f)$. Once $S_{vco}(f)$ is available, the VCO noise contribution at PLL output is:

$$S_{out,vco} = \left| \frac{\phi_{out}}{\phi_{vco}}(f) \right|^2 S_{vco}(f). \tag{4.38}$$

Since the considered noise sources are uncorrelated, the overall noise density of PLL can be obtained by summing the individual noise contributions:

$$S_{out} = S_{out,r} + S_{out,dac} + S_{out,div} + S_{out,vco}. \tag{4.39}$$

4.10 Implementation Details and Test Setup

The prototype transmitter (Figure 4.14) is implemented in 130nm mixed-mode CMOS and occupies an active area of 0.6mm^2, and a total area of 2mm^2 including pads. The device is packaged in a 32 pin QFN package. The $\Sigma\Delta$ modulators, the low pass filters, the modulation scheme and chip encoder are implemented as synthesized logic and occupy 0.07mm^2, which is a small fraction of the overall area.

A reference clock of 200MHz is used, with a nominal output frequency of 2.405GHz,

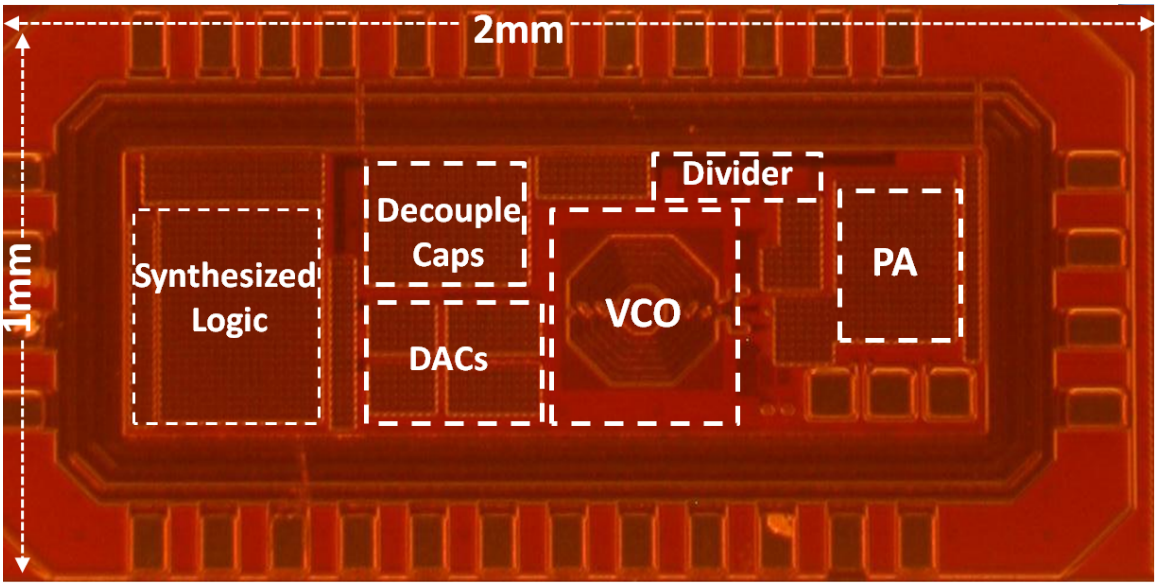

Figure 4.14: The DPLL based transmitter die photo

which corresponds to a division ratio of 12.025. The phase detector gain K_{PD} is set to 0.01, and the loop filter gain is set to 0.03, resulting in a loop bandwidth of 145kHz. The simulated VCO gain is 25MHz/V. The VCO gain is kept small in order to prevent the DAC quantization noise from corrupting the output phase noise. A high reference clock is required, so that the phase quantizer adequately oversamples the phase information. In order to convert from the digital to analog domain, a first order modulator controls a 5-bit resistor-string DAC. The programmable divider used is similar to [50]. The division ratio is controllable from 8 to 15 using 2/3 divider cells.

IEEE 802.15.4 packets are generated in an FPGA. The modulation chip sequence is then sent to the prototype device for transmission. An on-chip encoder converts the O-QPSK chip codes to MSK equivalents. The output of the transmitter is demodulated using a TI CC2420 evaluation board [51] for verification. Output spectrum is measured with an Agilent E4405B spectrum analyzer.

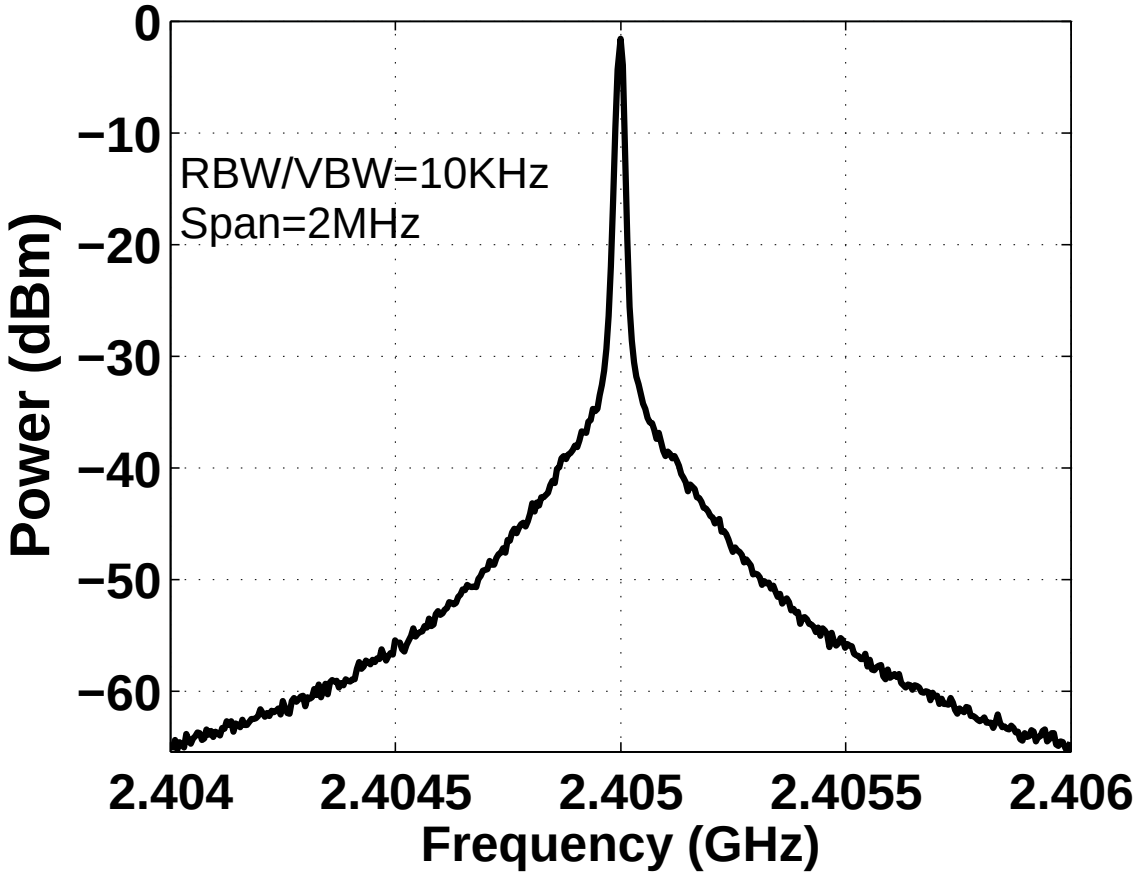

Figure 4.15: Measured transmitter spectrum without modulation

4.11 Measurement Results

Figure 4.15 shows the measured output spectrum of the PLL without modulation. The measured output power at 2.405GHz is -2dBm.

Figure 4.16 shows the MSK spectrum when a 2Mb/s PRBS modulation data is applied to the PLL through the FPGA. The IEEE 802.15.4 mask requirements are fulfilled. Multiple packets are successfully demodulated using the CC2420 evaluation board. Although the PLL loop bandwidth is only 145KHz, the self-calibrated two point modulation scheme enables modulation at rate of 2Mb/s.

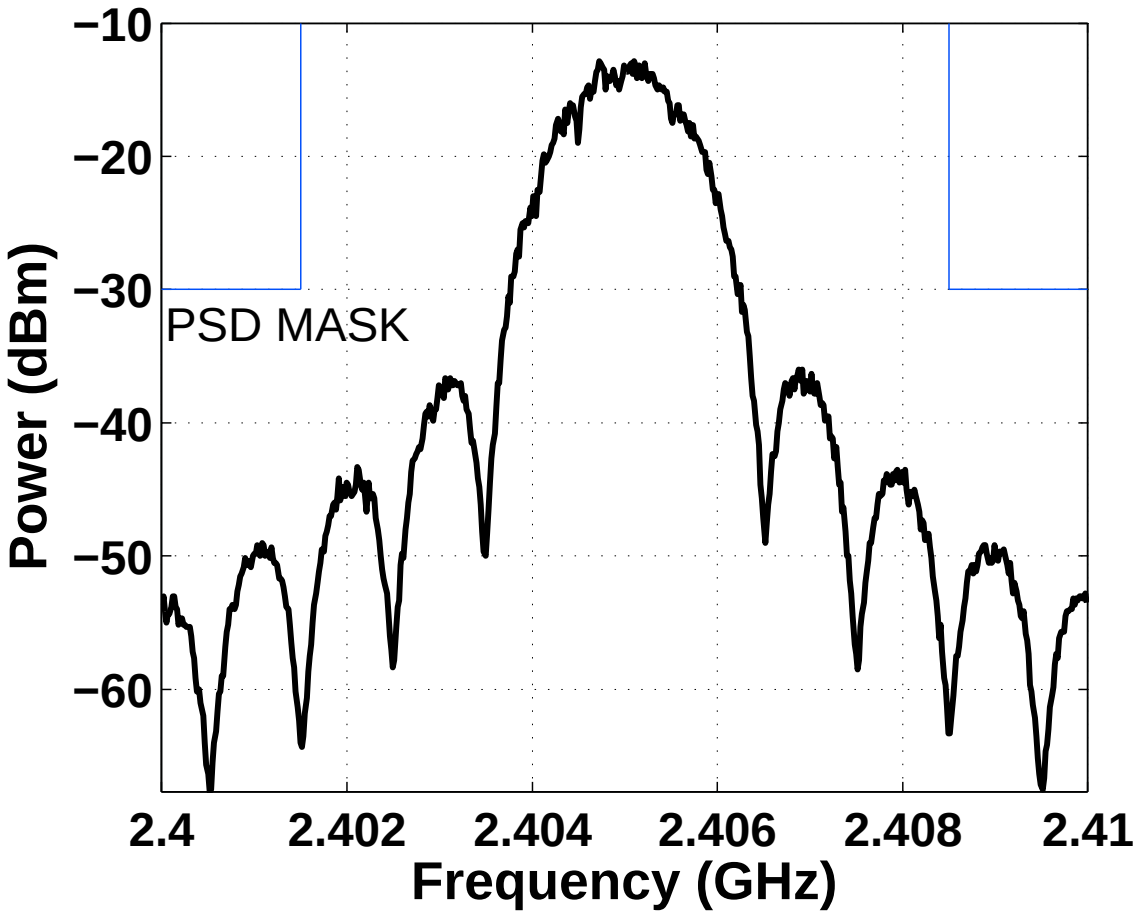

Figure 4.16: Measured PLL spectrum w/ 2Mb/s MSK modulation

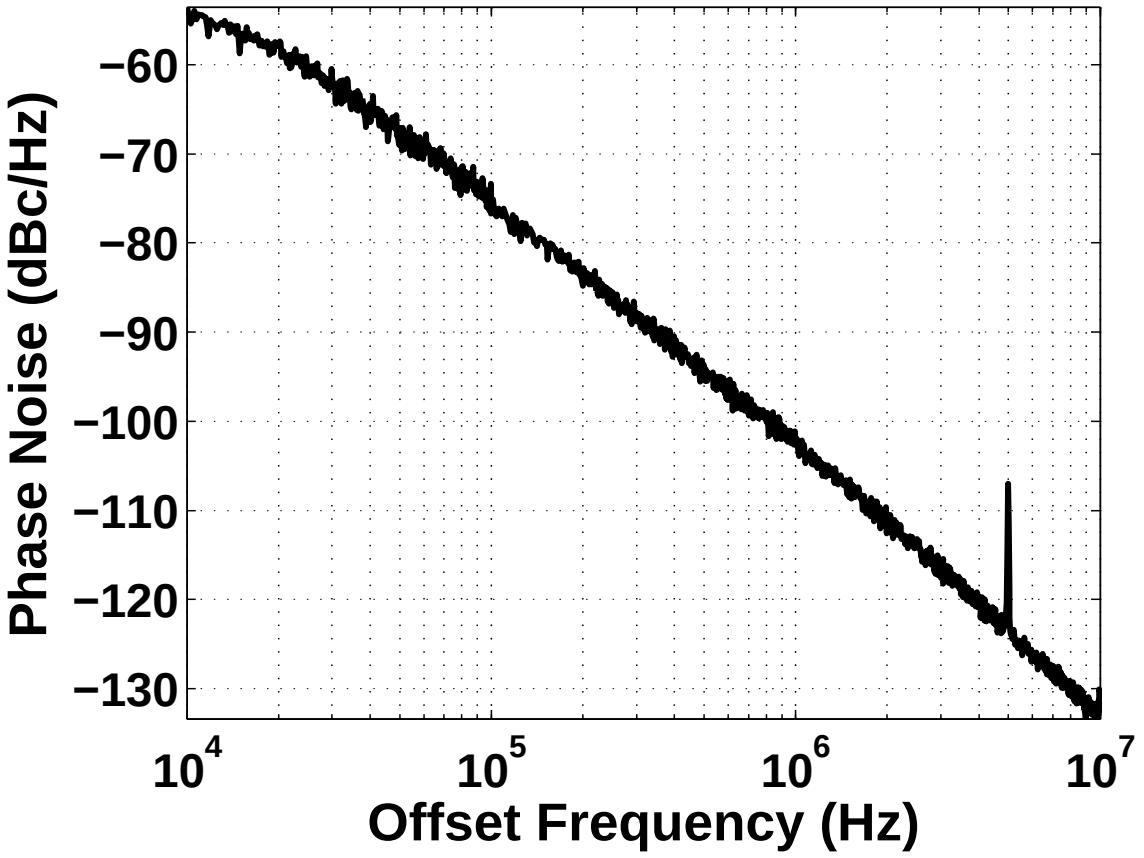

Figure 4.17: Measured PLL phase noise at 2.405GHz

Figure 4.17 shows the measured phase noise of the PLL. The phase noise at 3.5MHz offset is -120dBc/Hz which meets the 802.15.4 requirement. The PLL is free of in-band fractional spurs. The closest measured fractional spur is -60.2dBc at 5MHz offset as shown in Figure 4.18.

Figure 4.19 shows the trellis diagram of the PLL for 2Mb/s MSK modulation.

The synthesized logic draws 4mA. For a -2dBm output power, the PA consumes 4.5mA. A current consumption of 5.7mA is attributed to the divider, the VCO, and the DACs. The total power consumption of the transmitter is measured to be 17mW with 12.5mW attributed to the PLL. The chip operates with an analog and digital supplies of 1.2V.

The performance of the transmitter is summarized and compared to some recent papers

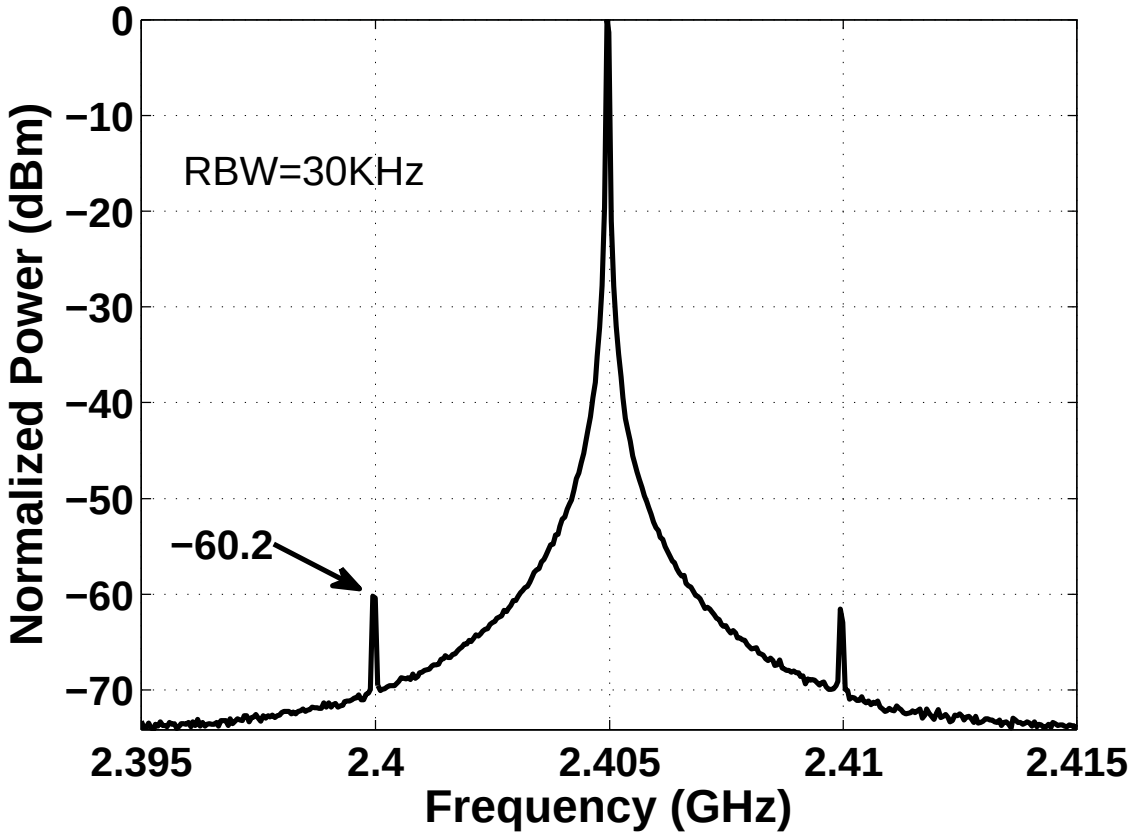

Figure 4.18: Measured PLL spur at 2.405GHz

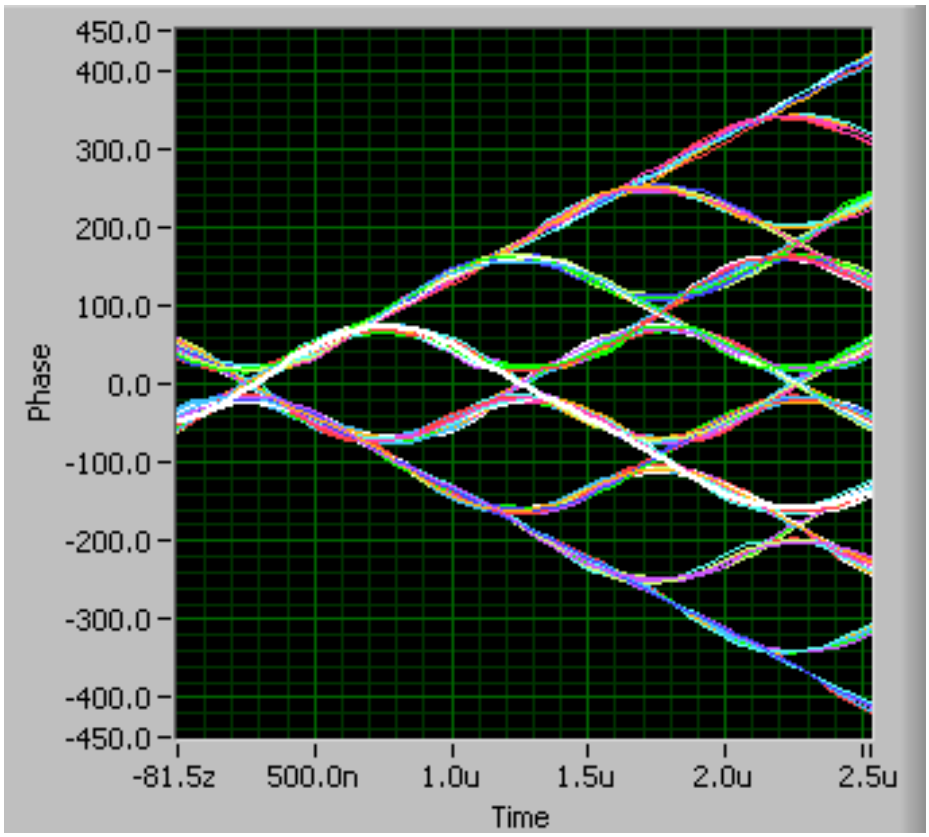

Figure 4.19: Measured trellis diagram for 2Mb/s MSK modulation

Table 4.1: Transmitter performance and comparison with prior art

Parameter	**This Work**	ISSCC '09 [37]	CICC '09 [38]	JSSC '10 [39]	JSSC '08 [6]
Tech.	**130nm**	180nm	150nm	65nm	130nm
V_{DD}	**1.2V**	1.8V	1.55V	1.2V	1.4V
PA Power (dBm)	**-2**	4	N/A	N/A	-22
Modulation	**2Mb/s MSK**	2Mb/s GMSK	2Mb/s MSK	2Mb/s FSK	1Mb/s FSK
Frequency (GHz)	**2.4-2.5**	2.48 center	2.405-2.480	2.29-2.92	2.24 max.
Power (mW) PLL/PA	**12.5/4.5**	13.32/16.39	8.525	12	14
Phase noise (dBc/Hz) 3MHz offset	**-120**	-126	-116	-132	-122
Core Area mm^2	**0.6**	1.1	0.88	0.27	0.7

in Table 4.1.

CHAPTER V

Conclusion

This thesis proposes circuit and system techniques that not only improve power consumption and reduce the form factor, but also significantly improve the performance of PLL based transmitters. The main contributions of this work are three fold.

In Chaper II, we present a new low power, low jitter, compact 192MHz reference frequency quadrupler that leverages a new low phase noise, active inductor based 48MHz differential XO. This 192MHz clock is an excellent clean reference for a low phase noise PLL. The prototype needs significantly less power and area compared to conventional methods.

In Chapter III, a versatile, compact, low voltage, low power 2.5GHz VCO with low phase noise is presented [23]. A conventional CMOS current reuse VCO is modified with the introduction of an AC coupling capacitor to reduce the supply voltage and achieve comparable phase noise at a much lower power consumption. The 2.17GHz to 2.9GHz VCO is capable of operating with a supply voltage as low as 0.6V. With a 0.7V supply and a 185μW power consumption, the phase noise at a 3MHz offset is -122.6dBc/Hz, which is suitable for applications such as ZigBee. Increasing the supply voltage to 1.3V results in a

phase noise of -130.1dBc/Hz with a 0.9mW power consumption. This phase noise meets the requirements for applications such as Bluetooth, GPS, and even some lower data rate WLAN applications. At 0.85V, the VCO phase noise is -126.1dBc/Hz with a 190.2dB FoM, the highest reported for power levels as low as 280μW. This is the lowest reported power consumption and supply voltage for any current reuse VCO[1]. Implemented in 65nm CMOS, the VCO occupies a core area of 0.13mm^2.

Chapter IV presents a fully integrated 2.4GHz transmitter in 130nm CMOS that meets the requirements of 802.15.4 standard [24]. The $\Delta\Sigma$ fractional-*N* PLL is largely comprised of synthesized digital logic and the amount of analog circuitry is minimized. The transmitter achieves a 2Mb/s MSK modulation, and delivers -2dBm to a 50Ω load using a compact two-stage PA that requires no output matching. The prototype is implemented in 0.13μm CMOS and occupies an active area of 0.6mm^2. The transmitter consumes 17mW from a 1.2V supply.

5.1 Ideas for Future Work

There are several avenues to further pursue the techniques presented in this thesis. A few ideas are outlined here.

A complete frequency synthesizer can be built around the frequency quadrupler work presented in Chapter II. This will further highlight the performance improvements as well as power and area saving in the overall PLL due to this fast, low phase noise reference. A high performance PLL, leveraging the frequency quadrupler circuit, can be realized as shown in Figure 5.1. The reference quadrupler generates a 160MHz low phase noise

[1] As of the date of publication in [23].

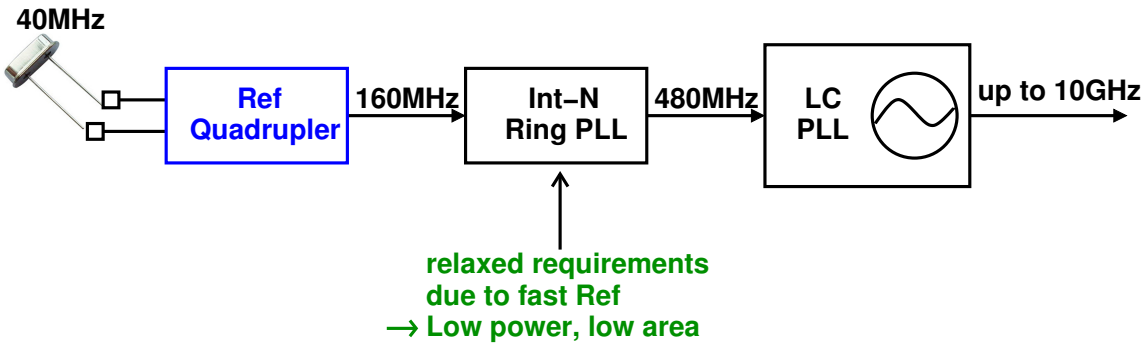

Figure 5.1: An ultra high performance PLL leveraging the reference quadrupler

reference from a standard 40MHz crystal (*e.g.,* for a Wi-Fi application). For most low phase noise PLLs, the 160MHz reference is adequate for reducing the fractional modulator noise. Nevertheless, for ultra high performance applications (such as MU-MIMO IEEE 802.11ac) it might be desirable to more than quadruple the reference. The frequency quadrupler can then be cascaded by an integer-*N* ring PLL. It is important to note that unlike the existing methods, the requirements for this integer-*N* PLL are now quite relaxed. This is because the already quadrupled 160MHz reference allows a wide loop bandwidth for the integer-*N* PLL, therefore significantly reducing the power and area requirements for the ring VCO. In addition, reference injection is no longer needed (although it can still be used if desired) since a high loop bandwidth will significantly reduce the integer-*N* ring PLL phase noise.

Another proposal, building on the new active inductor based differential XO presented in Chapter II, is to use the AC coupling technique introduced in the current reuse VCO of Chapter III to further reduce the supply voltage and power consumption of the differential XO. The schematic for such crystal oscillator is envisioned in Figure 5.2. The minimum supply voltage needed for this circuit is now reduced to $V_{dsat_n} + V_{dsat_p} + V_{T_p}$. This is lower than the differential XO presented in Chapter II, where minimum supply is $V_{dsat_n} + V_{T_n} +$

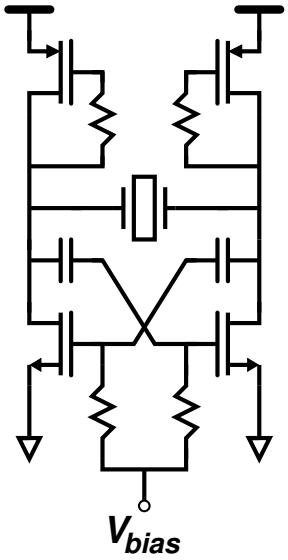

Figure 5.2: Low voltage AC coupled active inductor based crystal oscillator

$V_{dsat_p} + V_{T_p}$. This XO circuit can now operate with a sub 1V supply and is therefore suitable for ultra low voltage applications. However, the addition of an AC coupled path and reducing the supply needs rigorous analysis; and careful design choices must be made to ensure sufficient start up and loop gain.

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