Vertical Integration of Germanium Nanowires on Silicon Substrates for Nanoelectronics

by

Lin Chen

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical Engineering)
in the University of Michigan

2016

Doctoral Committee:

Associate Professor Wei Lu, Chair

Professor Cagliyan Kurdak

Assistant Professor Becky L. Peterson

Associate Professor Zhaohui Zhong

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Acknowledgements

First I would like to express my deepest appreciation and gratitude to my advisor, Prof. Wei Lu, for his patient guidance and mentorship from the day I applied for the PhD program, until the completion of this degree. This work would not have been possible without his unfailing inspiration and immense knowledge.

I would also like to thank my committee members, Prof. Cagliyan Kurdak, Prof. Peterson and Prof. Zhong, for their insightful comments and encouragement, which motivated me to improve this work from various perspectives.

I am also grateful to many current and former group members, including Jiantao Zhou, Chao Du, Ugo Otuonye, Wen Ma, Fuxi Cai, Dr. Wayne Fung, Dr. Siddharth Gaba, Dr. Patrick Sheridan, Dr. Yuchao Yang and Dr. Taeho Moon. In particular, I would like to thank Dr. Wayne Fung, who has been an excellent mentor and collaborator during my first two years in the program.

In addition, I would like to acknowledge the technical support of the Lurie Nanofabrication Facility (LNF) and the Electron Microbeam Analysis Laboratory (EMAL), especially the following staff members for their continuous assistance: Matt Oonk, Dennis Schweiger, Greg Allion, Shawn Wright, David Sebastian, Terre Briggs, Dr. Sandrine Martin, Dr. Nadine Wang, Dr. Vishva Ray and Dr. Kai Sun.

Last but not the least, my sincere thanks goes to my family and my friends, for their unconditional love and support throughout this PhD program and my life.

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Abstract

Vertical Integration of Germanium Nanowires on Silicon Substrates for Nanoelectronics

by

Lin Chen

Chair: Prof. Wei Lu

Rapid development of semiconductor industry in recent years has been primarily driven by continuous scaling. As the size of the transistors approaches tens of nanometers, we are faced with challenges due to technological and economic reasons. To this end, unconventional semiconductor materials and novel device structures have attracted a lot of interests as promising candidates to replace the Si-channel MOSFET and help extend Moore's law. In this dissertation, we focus on chemically-synthesized germanium nanowires, and investigate their potential as electronic devices, especially when vertically integrated on a Si substrate. The contributions of the work are as follows:

First, the Vapor-Liquid-Solid method for growing Ge nanowires on (111) Si substrates is explored. In addition to the growth of vertical, taper-free, intrinsic Ge nanowires, strategies for doping the nanowires, forming a radial heterojunction and controlling growth sites are also discussed.

Second, the Ge/Si heterojunction obtained via nanowire growth is examined by transmission electron microscopy. We confirm the epitaxial nature of the heterojunction despite the 4% lattice mismatch and determine the transition width to be 10-15 nm.

Vertical heterodiodes with independently-tuned doping profile in both Ge and Si are demonstrated. Different devices are obtained, including: (1) a rectifying diode with $>10^6$ on/off ratio and ideality factor of 1.16; (2) a tunnel diode with room temperature negative differential resistance, peak current density of 4.57 kA/cm^2 and reversed-bias tunnel current of 3.2 μA/μm; (3) a non-ohmic contact due to large valence band offset between Ge and Si. All observed behaviors are very well supported by theoretical analysis of the devices.

In addition, a vertical junctionless transistor with Ge/Si core/shell nanowire channel and surrounding gate is demonstrated. High performance p-type transistor behavior with on state current density of 750 μA/μm and mobility of 282 cm^2/V·s is achieved. Moreover, an analytical model is developed to quantitatively explain the measured data and excellent agreement is obtained.

Finally, progress towards the realization of a nanowire tunnel transistor is reported. A physical model for nanowire tunnel transistors is proposed. Preliminary experimental results verified that the device concept works although further optimization is still required to boost its performance.

Chapter 1

Overview

Following the invention of the first transistor, the semiconductor industry has experienced tremendous growth over the past few decades. Although merely an observation when it was first proposed, Moore’s law has been considered a roadmap and guided scientists and engineers working diligently to meet the rapid progress towards manufacturing integrated circuits with higher density and performance at a lower cost. Initially, this goal can be achieved through simply scaling the device dimensions. However, as the device size evolved from sub-micrometer and moved into nanometer range, scaling alone is not the solution anymore. In the past, there were a few times when Moore’ law was seriously questioned, but every time, some innovative ideas were proposed to make the breakthrough the industry needed to keep up with the roadmap and continue pushing forward.

Looking back, the structure of a semiconductor transistor has undergone many changes to meet the continuously developing demands for performance and cost. Numerous improvements including strained Si (for improved mobility), high-*k* dielectric/metal gate (to suppress leakage current and provide higher gate capacitance) and carefully engineered doping profile (to prevent punch through) can be found in a modern transistor. Recent technological advances have allowed us to transform transistors from their original structure to the FinFET with tri-gate structure, marking the era of 3-D transistors. Now that the devices size has approached tens of nanometers, and we are faced with new obstacles that call for creative thinking again.

In large scale manufacturing, a top-down approach, where the critical dimension is lithographically defined and etched from a thin film, has been the mainstream since the very beginning. The top-down approach is capable of delivering precise size/location control, but its resolution is heavily dependent on the lithography and etching tools. A more fundament limit is posed by the wavelength of the photons used in the lithography tool. Without breakthroughs in advanced techniques such as e-beam and extreme ultraviolet (EUV) lithography, it will become more challenging and more importantly, less economical to define nanoscale features in modern devices using photolithography. In modern transistors, one or more dimensions is confined to the nanometer scale to gain various performance boosts. Ultimately, such aggressive scaling will evolve to nanowire channels in which carrier motion becomes largely one-dimensional. Aside from offering performance enhancement, nanowires are technologically promising since they can be fabricated through a bottom-up approach, in which they are chemically-synthesized, or grown. With this approach, critical dimensions such as diameter are controlled by process parameters, so that atomic resolution can be achieved without lithography.

Being able to grow nanowires with different compositions, well controlled size, various crystal orientation and morphology plays an important role in recent developments of nanowire devices. The versatility of nanowires has been demonstrated in many applications where they are used as building block for electronics[1]–[11], photonics[12]–[23], solar cells[24]–[28], batteries[29]–[33], nanogenerators[34], [35] and biological/chemical sensors[36]–[43]. A wide range of materials can be synthesized in nanowire form, including but not limited to Si[44], Ge[45], III-V[16], [46]–[48], II-VI[49]–[51] and nitrides[52]. Different structures such as core/shell[53], [54], superlattice[16], [55] and branched nanowires[56], [57] can be realized and tailored to unique requirements. Figure 1 highlights a few notable applications for nanowire devices.[44], [58]–[60]

Not only are nanowires attractive for fundamental scientific research as they provide an excellent low dimension platform, they are promising candidates in future mass-produced electronics as well.

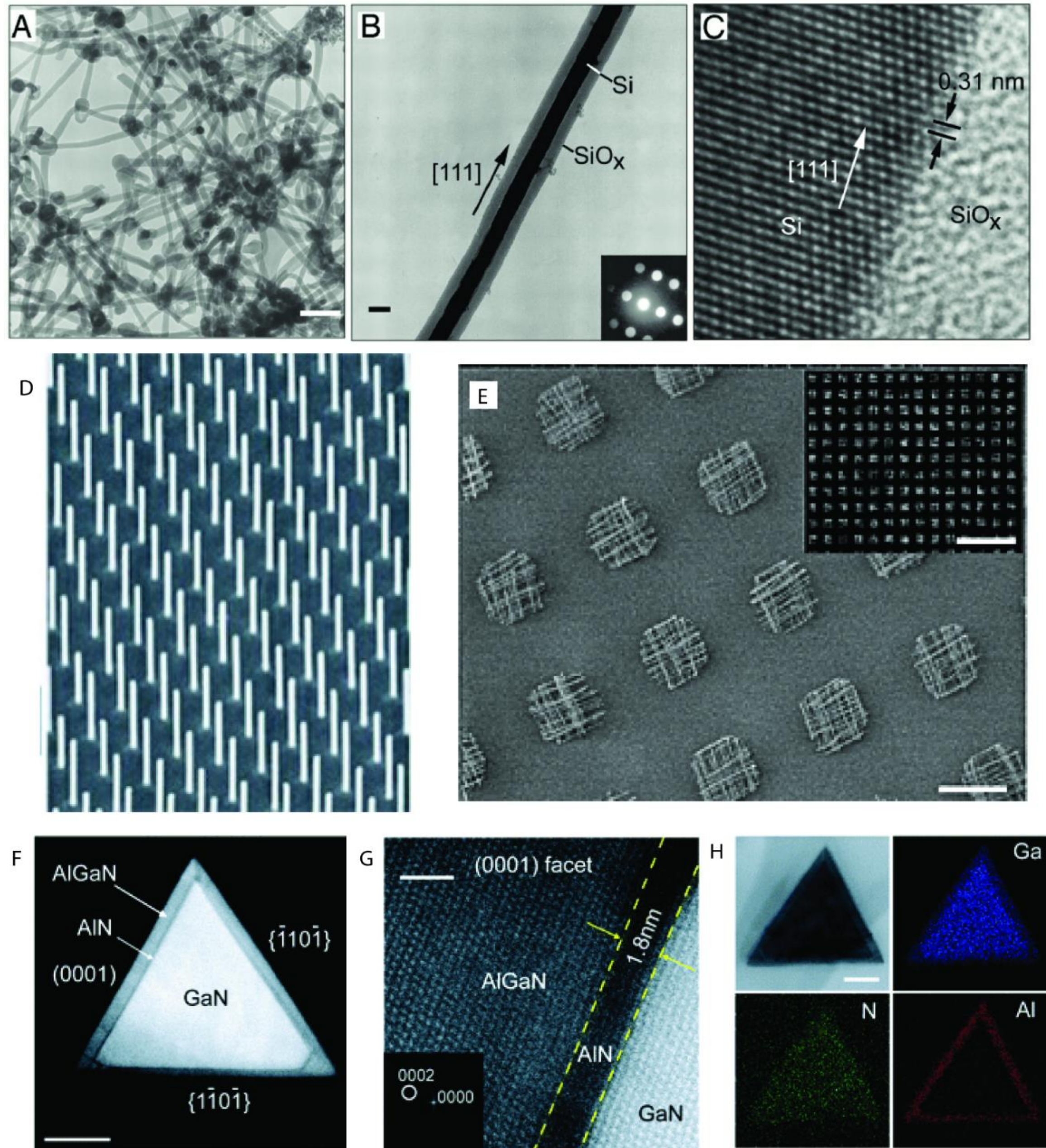

Figure 1. Overview of semiconductor nanowires and their applications. (A) TEM image of Si nanowires produced after ablation of a $Si_{0.9}Fe_{0.1}$ target. Scale bar: 100 nm. (B) Diffraction contrast TEM image of a Si nanowire. Crystalline material (the Si core) appears darker than amorphous material (SiO_x sheath) in this imaging mode. Scale bar: 10 nm. Inset: electron diffraction pattern recorded along the [211] zone axis perpendicular to the nanowire growth axis. (C) HRTEM image of the crystalline Si core and amorphous SiO_x sheath. The (111) planes (black arrows) (spacing

0.31 nm) are oriented perpendicular to the growth direction (white arrow). (D) Tilted SEM image of a vertical InAs nanowire array grown on an InAs (111)B substrate. The spacing between nanowires is 0.5 µm. (E) SEM image of patterned crossed nanowire arrays. Scale bar: 10 µm. Inset: large area dark field optical microscopy image of the crossed arrays. Scale bar: 100 µm. (F) high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) image of the cross section of a GaN/AlN/AlGaN nanowire. Scale bar: 50 nm (G) lattice-resolved HAADF-STEM image recorded at the (0001) facet of the nanowire. Dashed lines highlight the heterointerfaces between layers. Scale bar: 2 nm. (H) bright field STEM image and corresponding EDS elemental mapping of the same nanowire, indicating spatial distribution of Ga (blue), Al (red) and N (green), recorded on a GaN/AlN/AlGaN nanowire cross section. Scale bar: 50 nm. From [44]. Reprinted with permission from AAAS. Adapted with permission from [58]–[60]. Copyright 2003, 2004, 2006 American Chemical Society.

One major concern with continuous scaling is the need to suppress the short channel effect (SCE).[61] SCE such as drain induced barrier lowering (DIBL) starts to appear when gate gradually loses control over the channel in a scaled transistor. Essentially, as the channel length reduces, the gate capacitance needs to be enhanced proportionally to offer sufficient control over the underlying channel and ensure correct transistor operation. Usually this is achieved through scaling the gate oxide thickness along with other structural dimensions. However, this is not a sustainable approach as the gate leakage current grows exponentially with thinner oxides. It is found that the minimum channel length without incurring severe short channel effect is determined by factors such as channel thickness, oxide thickness, relative dielectric constant and gate structure.[62] By moving from planar transistors as shown in Figure 2A, to a partial/full depleted channel (Figure 2B), or 3-D FinFET (tri-gate, Figure 2C), gate control can be improved without reducing the oxide thickness. The best gate control is achieved when the whole channel is surrounded by gate dielectric (surrounding gate, or gate all around, GAA). However, GAA structures are technologically challenging to fabricate in a planar device, primarily due to difficulty of depositing material underneath the channel, which typically requires a sacrificial layer, a suspended channel and techniques like atomic layer deposition (ALD). To this end, nanowire devices can offer an interesting option to simplify the process by aligning the channel in the vertical

direction. As shown in Figure 2D, by depositing a thin metal film, surrounding gate can be readily achieved. Coupled with high-k dielectric, this may provide the boost needed for future high performance electronics.

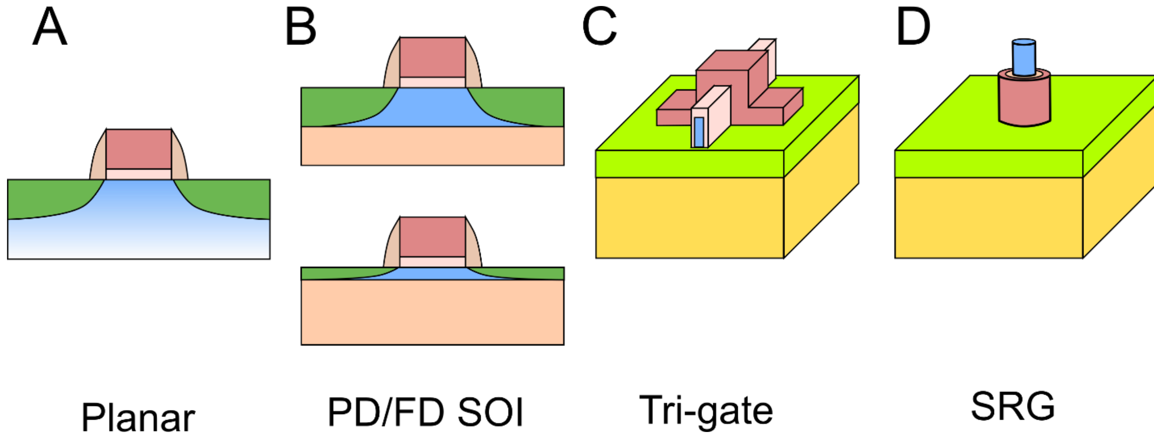

Figure 2. Various gate structures for transistors. (A) Planar channel. (B) Partially and fully depleted channel on SOI substrate. (C) FinFET, or Tri-gate. (D) Vertical nanowire with surrounding gate. Gate control is improved from (A) to (D).

Another serious problem today's integrated circuit faces is increased power consumption. As shown in Figure 3A, with size reduction and the consequent increase in device density, power consumption per area increases at a fast pace.[63] Further increase in power consumption is not sustainable since the increased cost for associated packaging and cooling peripheral would render integrated circuits less economical. Power consumption in CMOS mainly consists of two components, active power $P_{active} \propto V_{dd}^2$ when the device is switching and passive power $P_{passive} = I_{off}V_{dd}$ when the device is idle. While it is obvious that scaling V_{dd} can reduce both active and passive power consumption, it requires V_{th} to be lowered proportionally to compensate for the reduction in I_{on}, because I_{on} must be proportional to $(V_{dd} - V_{th})^2$ in first order approximation to maintain competitive circuit speed. The reduction in V_{th}, on the other hand, increases the passive power drastically due to the exponential dependence of I_{off}^{-1} on V_{th}. In actual circuits, the situation is somewhat better since normally threshold voltage is not scaled as

aggressively, but substantial increase in leakage current is still observed. For devices size above 100 nm, active power is the major contributor, as shown in Figure 3B. [64] Now that passive power takes the leading role, we have to seriously re-think our strategy in future circuit design.

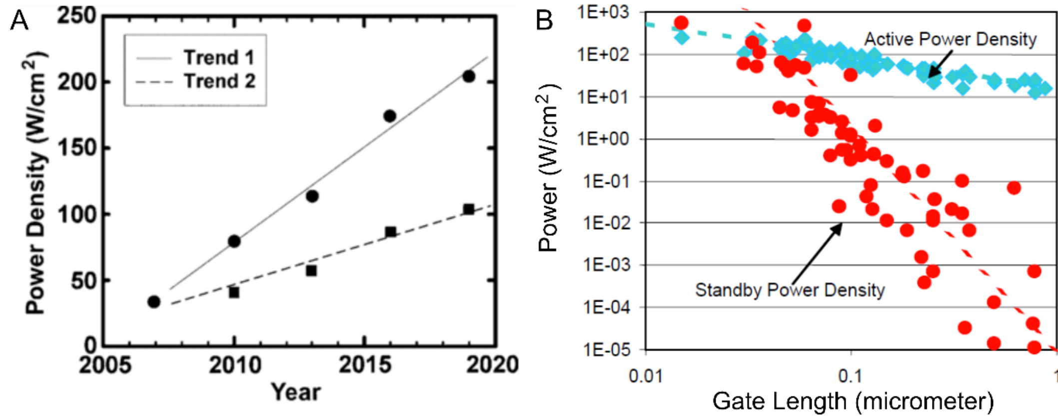

Figure 3. Power crisis in integrated circuits. (A) Trend of power consumption per chip area. Trend 1 is calculated based on ITRS projected integration density and performance. Trend 2 is calcuated based on increase chip size from year 2010. Adapted from [63]. © 2008 IEEE. (B) Comparison of active power and passive power as device scales. Adapted from [64].

The increase of I_{off} poses a severe limit of MOSFET scaling. Physically, this effect is rooted in the finite subthreshold swing (SS), which is the inverse slope of the device transfer (*i.e.*, I_{ds} $vs.$ V_{gs}) characteristics. In essence, SS describes how much gate voltage is needed to turn the device off. It is limited to a minimum of 60 mV/dec at room temperature. This is due to the thermionic emission nature of the carriers in a MOSFET and originates from the tail in the Boltzmann distribution of electrons. Due to this fundamental limit, scaling of V_{dd} and V_{th} has essentially stopped while the device dimensions continue to be reduced, which raises additional problems such as device reliability, increased power dissipation and other high field effects. To address this problem, and to a broader content, the issue of power consumption, device characteristics similar to the green curve in Figure 4 are desired, which requires SS < 60 mV/dec to allow continued V_{dd} and V_{th} scaling. However, this means devices with a different operating mechanism must be developed.

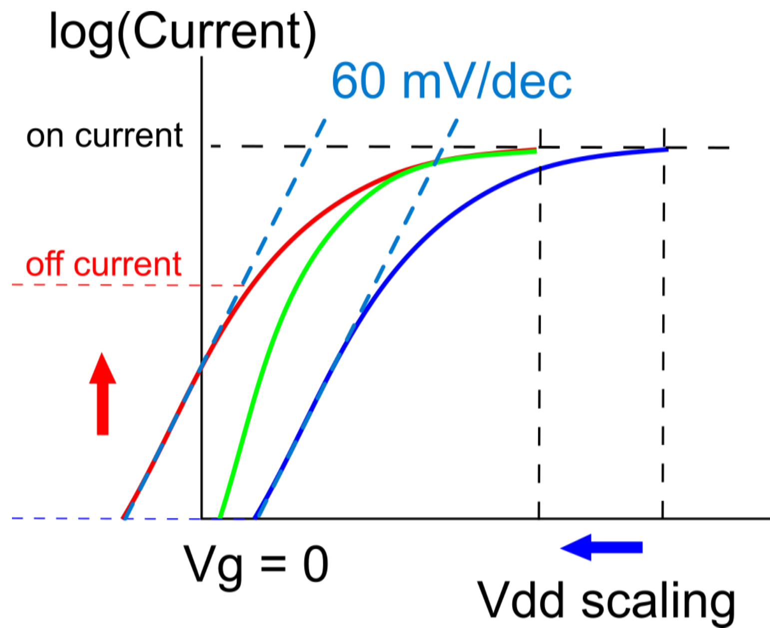

Figure 4. Schematic of supply voltage scaling and its effect on off-state current. . The green curve represents an ideal device with sub-60 mV/dec switching so both high I_{on} and low I_{off} can be achieved simultaneously.

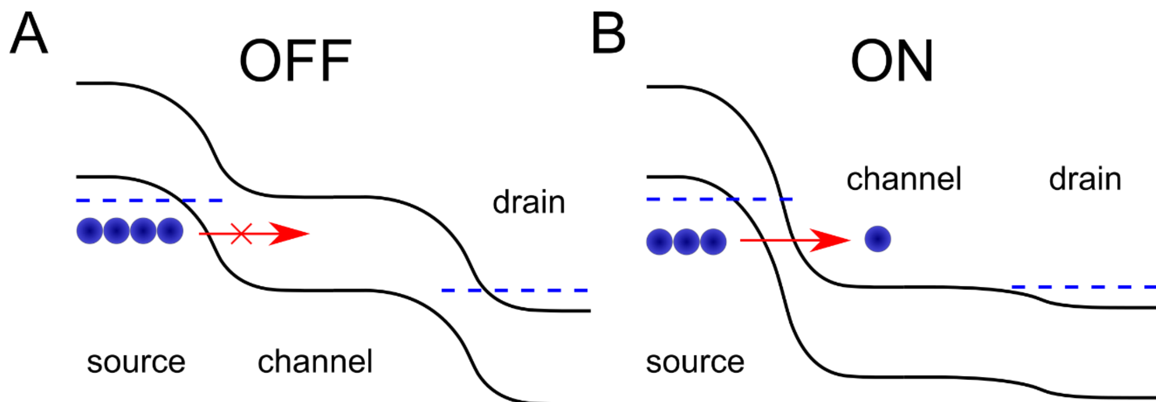

Figure 5. Band diagram of TFET. At OFF state, tunneling from source to channel is not allowed due to lackof available states in band gap. At ON state, band to band tunneling can occur between source and channel provided the electric field is sufficiently high.

For this reason, tunneling based devices have been an active research area in the search for an alternative, presumably low-power building block for integrated circuits. A tunneling field effect transistor (TFET) is essentially a reverse-biased p-i-n diode with a gate covering the intrinsic channel. The basic operation of an n-type TFET is schematically shown in Figure 5. When an overlap of the conduction band and valence band is achieved between the source and channel,

electrons in the valence band in the source can tunnel into the conduction band in the channel and get collected by the drain. Since in a TFET the carriers do not climb *over* a barrier, but tunnel *through* it instead, the turn-off rate is not limited by the Boltzmann distribution on the source side, and SS steeper than 60 mV/dec can potentially be obtained if the gate can change the tunnel junction width efficiently. To obtain a high I_{on} and a steep SS in a TFET, it is of paramount importance to create a high electric field (or equivalently thin tunnel barrier) and having efficient gate control to change the tunnel barrier thickness.

A number of studies have been performed to explore prototype TFET devices. So far, impressive off-currents and subthreshold slopes have been obtained.[65]–[74] In a TFET, the off state leakage current is governed by the thermionic current through a reverse biased p-i-n diode and can be suppressed to as low as 0.12 pA/μm.[69] Experimentally, several groups have achieved subthreshold slopes < 60 mV/dec in different materials and various device structures.[65], [66], [68] However, devices to date suffer from poor on-state performance due to a low band-to-band tunneling probability, which is exponentially dependent on the band gap and the thickness of the tunnel barrier. The highest I_{on} demonstrated to date is 12.1 μA/um at 1 V (with SS < 60 mV/dec),[66] which is still two orders of magnitudes lower than that offered by state-of-the-art CMOS devices. Naturally, employing a narrow band gap material at the source/channel junction will provide improved on-state performance.[75] Additionally, heterostructures with staggered or even broken band alignment further reduces the effective tunneling barrier and could further improve the on-state performance.[76], [77]

In this dissertation, we focus on exploring Ge-nanowire based devices as a candidate for future nanoelectronics. Compared with other competitors such as III-V[8], [78], [79] and carbon based materials[80]–[82], Ge offers several unique advantages as a channel material. First, Ge can

offer both high electron mobility of 3900 cm^2/Vs and hole mobility of 1900 cm^2/Vs at room temperature.[83] Second, since Ge has been already introduced into semiconductor industry as a crucial component in strained Si, Ge is a proven CMOS compatible material more than the other alternatives.[84] Third, even though Ge has a relatively large lattice mismatch (4%) with Si, defect-free epitaxy of Ge nanostructures such as Ge nanowires on Si is possible due to coherent strain relaxation in the reduced volume.[11], [16], [85] Last but not least, with a smaller band gap (0.66 eV at room temperature, compared to 1.12 eV for Si) and lower effective mass for tunneling, Ge promises two orders of magnitude higher I_{on} at the same electric field compared with Si based TFETs.[86]–[88]

Ge nanowires used in this work are prepared via a bottom-up approach. We first focus on the techniques for Ge nanowire synthesis, in particular, engineering their morphology, orientation and composition. Then their potential for electronic devices is evaluated through a series of devices from the most basic pn diode to MOSFETs and TFETs. The goal is to fully understand their operation so we can gain insight for continued device optimization.

Another important field we would like to delve into in this dissertation is vertical integration of nanowire devices. Previous research on nanowire electronics has mostly focused on randomly deposited nanowires that are removed from the original growth substrate. The locations of the nanowires in these studies have to be learned from scanning electron microscopy (SEM) or atomic force microscopy (AFM) imaging and working devices have to be picked by hand.[1] As a result, these studies are limited to the proof-of-concept level, and the process are not sufficient for the fabrication of functional systems needed for real-world applications. Here we use an alternative scheme in which the vertical nanowire transistor structure can indeed provide an approach for nanowire circuit integration, as schematically illustrated in Figure 6. Ideally, vertical

nanowires can be grown on the same substrate with CMOS circuitry, either on the side or directly on top, eliminating the hassles of transferring and locating them after transfer. Since in our scheme the locations of the nanowires are determined by the growth process, full control of nanowire integration is possible. By designing appropriate interconnects, both nanowire/CMOS integration and the integration of different nanowire devices can be achieved for circuit applications.

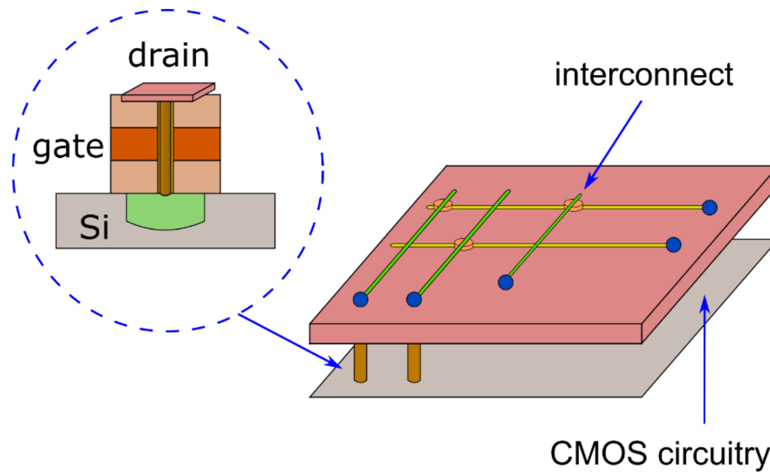

Figure 6. Schematic of 3-D integration of vertical nanowire transistors with CMOS circuits.

The content of this dissertation is organized as follows. Chapter 2 discusses the synthesis of Ge nanowires on Si substrates and various techniques for the fabrication of Ge nanowire based devices. In chapter 3, we study the interface quality of the Ge/Si heterojunction, since device performance relies heavily on a clean, intrinsic interface. Several configurations of two terminal devices with independently tunable doping levels will be discussed in chapter 4, highlighting the flexibility of the Ge/Si system; In chapter 5, we demonstrate vertical Ge nanowire junctionless transistors and analyze their performance. In chapter 6, we propose an analytical model for the tunnel transistor and present some experimental progress towards vertical tunnel transistors based on Ge/Si core/shell nanowires. Finally, in chapter 7, we make some concluding remarks and discuss the future work that can be done after this dissertation.

Chapter 2

Epitaxial growth of vertical Ge nanowire on Si substrate

2.1 Introduction

Semiconductor nanowires usually refer to crystal structures with diameters as small as few nanometers and lengths up to tens of micrometers or even millimeters. As mentioned in the previous chapter, the common techniques to acquire a particular structure in semiconductors can be roughly divided into two categories, a conventional "top-down" method where the shape is etched from a planar film, or "bottom-up" method where the structure is chemically grown, or synthesized. Nanowires are no different. So far, semiconductor nanowires have been demonstrated with both approaches.[10], [89]–[91] In a top-down process, the quality of the nanowires heavily depends on the starting material purity, although damages to crystalline structures are inevitable during size reduction steps such as dry etching, degrading its overall quality. The top-down approach also relies almost solely on the precision of the lithography/etching tools to produce nanoscale structures with good uniformity and consistency. With continuous device scaling, it has become more challenging and less cost-effective to do so. To the contrary, in a typical bottom-up process, the critical dimension of the nanowires (*i.e.*, diameter) is controlled by the chemical synthesis process and atomic resolution can be achieved with ease.

Synthesized nanowires offer many advantages such as small diameter, large surface-to-volume ratio, smooth surface and controlled material composition. For example, the large surface

area and small diameters allowed nanowire electrodes to outperform thin-film electrodes in battery applications with superior charging/discharging rate and better stability,[29] while the nearly-perfect material quality has enabled optical and electrical pumped nanowire lasers.[17], [19] Controlled nanowire growth has also enabled bio-sensors with integrated detectors and electrodes, all achieved in a single nanowire during growth.[41]–[43] Additionally, the suspended nanowire structure allows direct and *in situ* formation of heterostructures such as core/shell and axial heterostructures during growth, which can lead to improved electrical or optical properties tailored to specific applications.[6], [16], [53]–[55]

In this chapter, we discuss semiconductor nanowires fabricated via the bottom-up paradigm, in particular, Ge nanowires grown by Au catalyzed vapor-liquid-solid (VLS) process. In addition to exploring epitaxial integration of vertical Ge nanowires on Si substrates we will also discuss several techniques to either modify the Ge nanowire properties or provide more control over its location and morphology. These techniques are important since they pave the way for fabricating Ge nanowire based electronic devices and allow these devices to serve as building blocks in integrated circuits.

2.2 Overview of the nanowire growth process

The history of VLS growth can be traced back to the 1960s by Wagner who successfully employed this method to grow silicon microwires (whiskers).[92] Whisker research remained a productive field, however, the relatively large size (> 0.1 μm in diameter) of the whiskers produced in these early days offered few practical advantages compared with top-down fabricated structures. In fact, nanometer scale nanowires were not thought possible until the experimental demonstrations in 1998 by Morales *et al*.[44] The early demonstrations employed laser ablation to generate the source vapor needed for VLS growth to obtain single-crystalline Si and Ge nanowires.

Soon the process was expanded to more controllable methods such as chemical deposition (CVD) and VLS has become the dominant option for nanowire growth due to its simple realization yet flexible and excellent control over many aspects of the synthesis process.

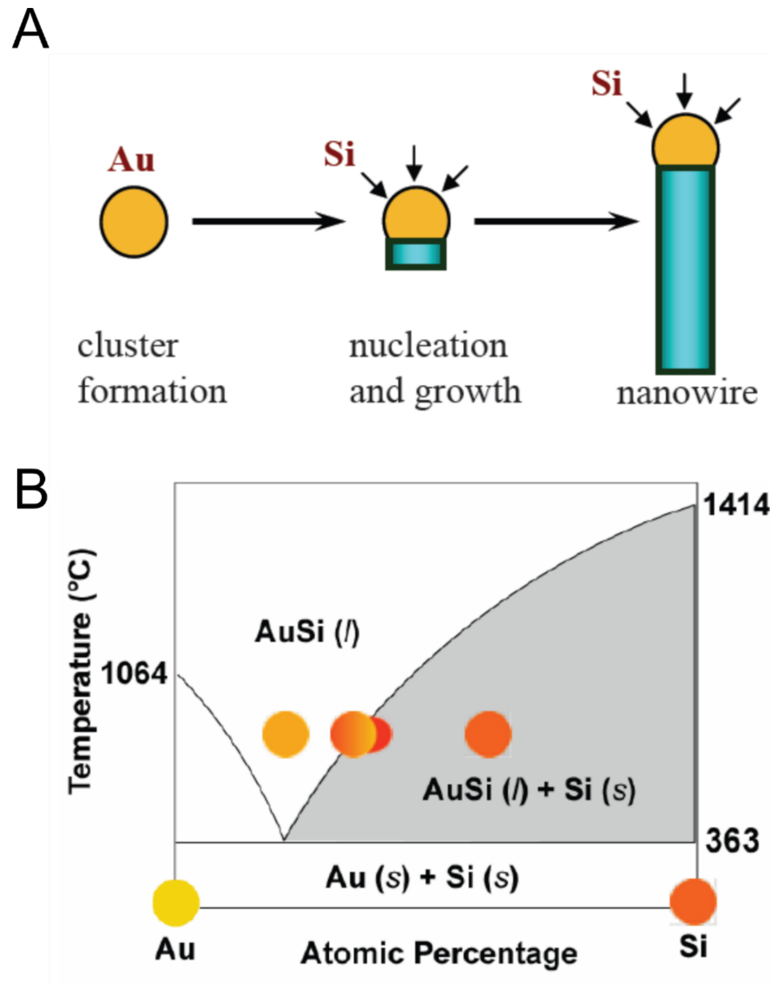

Figure 7. VLS growth mechanism. (A) Schematic of Au assisted VLS growth of Si nanowires. (B) Binary phase diagram of Au-Si system. © IOP Publishing. Reproduced with permission from [89]. All rights reserved.

In a typical VLS growth process, as schematically illustrated in Figure 7A, metal nanoparticles (either elemental particles such as Au, Ag, Cu, Al, Au or their alloys[93]) are employed as a catalyst to initiate and define nucleation, as well as facilitate activation/decomposition of the molecular reactants (if used). During the growth process, the metal nanoparticles are first heated up above the eutectic temperature for the target metal-semiconductor

system to create a liquid metal-semiconductor eutectic alloy. With the presence of the semiconductor source material in its vapor phase, the eutectic alloy will continue to incorporate the semiconductor material through the vapor/liquid interface, ultimately resulting in supersaturation of the semiconductor material in the eutectic alloy. Further addition of the semiconductor source material into the eutectic alloy will eventually result in a nucleation event whereby the semiconductor material precipitates and creates a liquid/solid interface, which is also referred as the growth interface. Nanowire growth is thus achieved via the transfer of the semiconductor material from the vapor source at the vapor/liquid interface into the eutectic alloy, followed by continued solid addition at the liquid/solid interface. In this manner, the name VLS growth accurately captures the essence of the growth process from the starting vapor source stage to the final solid crystal stage. It is also worth noting that as growth continues, the metal catalyst will remain at the tip as the nanowire elongates below the liquid/solid interface, as schematically illustrated in Figure 7A.[89]

The role of the metal nanoparticle is two-fold. First, it is used to form the eutectic alloy with the target semiconductor, and in doing so it also defines the diameter of a growing nanowire. The phase diagram of the Au/Si eutectic system is shown in Figure 7B, with a eutectic temperature of 363 °C with 19% Au in the alloy. This eutectic temperature is much lower than the melting temperature of either Au or Si so the VLS growth of Si nanowires can be carried out with Au catalysts in a low temperature system. Low-temperature growth can be advantageous, for example, by excluding impurities that might otherwise be trapped in growing Si at higher temperatures. Secondly, the metal nanoparticles normally serve as a catalyst that promotes the decomposition of the semiconductor gaseous precursor, thus selectively producing the semiconductor source material at the targeted growth sites. In the case of Si nanowire growth, SiH_4 and Au are normally

used as the precursor and catalyst, although other precursors such as Si_2H_6, SiH_2Cl_2, and $SiCl_4$ have also been employed.[93] The Au catalysts facilitate the decomposition of the precursor (*e.g.* SiH_4 into Si and H_2) near the growth sites, as the Si atoms in turn incorporate into the Au nanoparticles to form the Au/Si eutectic alloy and eventually lead to VLS Si nanowire growth with Si atoms precipitate at the liquid/solid interface.

VLS nanowire growth is typically conducted in a chemical vapor deposition (CVD) chamber (including conventional hot-wall CVD, lamp-heated cold-wall CVD and metal organic CVD (MOCVD) systems) where the precursor materials are introduced in vapor phase. Precursor decompositions and nanowire growth take place at controlled temperatures and pressures. However, momentum and energy transfer methods such as pulsed laser ablation (PLA)[44] or molecular beam epitaxy (MBE)[94] can also be used to produce the vapor phase growth materials from solid targets, and VLS growth of nanowires using MBE and PLA have also been widely studied. The flexibility of the VLS method allows it to be used for the growth of a broad range of nanowire materials other than Si, covering other group IV materials such as Ge[45], group III-V (GaAs[46], GaP[16], InAs[48], InP[47], *etc.*), II-VI materials (ZnS[49], ZnSe[51], CdS[50], *etc.*) and nitrides[52]. This level of flexibility makes VLS the predominant method for semiconductor nanowire growth. In the case of compound material nanowires, the semiconductor reactants are usually provided by metal-organic chemical vapor deposition (MOCVD)[95] or PLA[96].

In a typical VLS-CVD process, the size of the nanowire is to a large extent determined by the size of the catalyst used. Wu *et al.* systematically studied the size distribution of Si nanowires synthesized using SiH_4/H_2 and Au nanoclusters via the VLS method in well controlled conditions and reported that the sizes of the nanowires are consistently slightly larger than those of the catalyst used, which can be explained by the supersaturation of Si in Au which leads to the expansion of

the eutectic alloy volume compared to the starting pure Au nanoparticle.[97] Similar effects have also been reported in other VLS nanowire systems and verified through *in situ* imaging methods.[98] The excellent size control offered by VLS growth mediated with metal nanoparticles, which are commercially available at different specific diameters, offers a significant advantage over other methods such as laser ablation or thermal annealing of a thin metal film, and has become the dominating method of choice, and uniform nanowires with diameter down to a few nanometers can now be reliably obtained in a controlled fashion.

VLS growth is considered to be primarily thermodynamically driven since nanowires are synthesized mostly at near equilibrium conditions. The total free energy of the growth system includes the 'bulk' energy of the nanowire, the catalyst/nanowire (liquid/solid) interface energy, and the nanowire/vacuum (solid/vapor) interface energy and it is highly dependent on the nanowire orientation. As a result, usually a dominant nanowire orientation, determined by the minimum total free energy, can be observed. Note that this direction may also depends on other factors. For example, the preferred growth direction of Si nanowire was found to vary from <111> at larger diameters, to <112> at intermediate diameters (10-20 nm), to <110> at sizes below 10 nm.[97] The understanding and subsequent control of the preferred growth directions in turn allow the design and growth of epitaxial nanowire structures. While VLS growth on an amorphous substrate such as SiO_2 results in nanowires with random directions, epitaxial growth can occur with crystalline substrates, and more importantly, growth may occur along a certain direction that has low interface defect density.

2.2.1 Vertical Ge nanowire growth

Ge nanowires used in this work were grown via the VLS method in a CVD tool (FirstNano Easytube 3000). Au nanoparticles with diameter of 20 nm (Ted Pella, Inc., part number: 15705-

20) were typically used as catalysts while a mixture of GeH_4 and H_2 were used as processing gases. Figure 8A shows the phase diagram of the Au-Ge system where a eutectic temperature of 361 °C and 28% Au composition are indicated. It is worth noting that the low eutectic temperature of Au-Ge alloy allows for low-temperature synthesis of single crystalline materials, which can be particularly interesting for direct integration/growth of nanowire structures with existing CMOS circuits. It has been reported that the state of catalyst alloy depends on the thermal history and can be stabilized in liquid phase below eutectic point (*e.g.* 320 °C with 29% Au composition[99]), which makes low-temperature Ge nanowires attractive for thermally-sensitive substrates. During VLS growth, GeH_4 decomposes at the catalyst/vapor interface with the following reaction:

$$\mathrm{GeH_4 = Ge + 2H_2},$$

which supplies Ge atoms throughout the process.

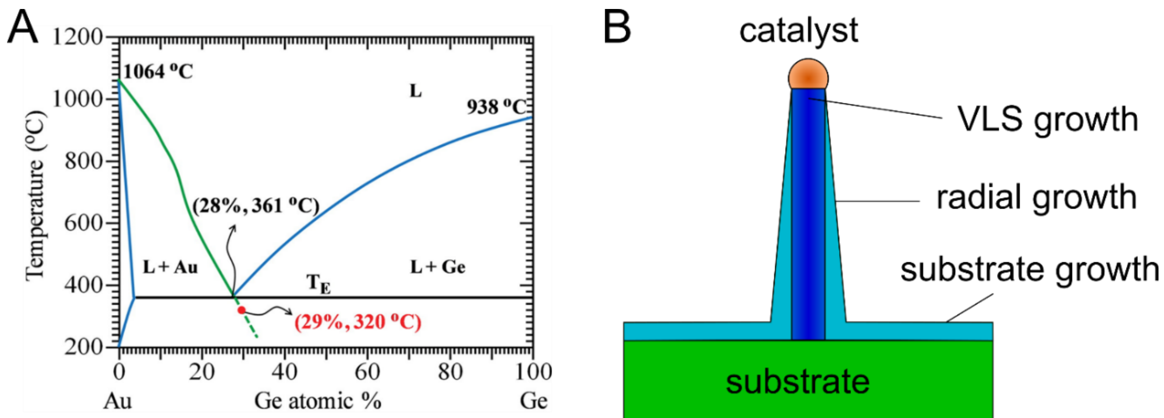

Figure 8. Ge nanowire growth with Au as catalysts. (A) Binary phase diagram of Au-Ge system. From [99]. Reprinted with permission from AAAS. (B) Schematic of different growth modes for the VLS process.

However, nanowire growth is not limited to one direction. As shown in Figure 8B, there are two competing processes in typical metal-catalyzed VLS growth: (1) catalyst-mediated precipitation through the liquid/solid interface which leads to axial elongation and (2) non-mediated direct vapor deposition on the existing nanowire sidewall surface. The latter process

results in radial thickening and eventually leads to tapering as the length of the nanowire increases. Deposition of thin film on the substrate is also possible, if the growth condition permits. Tapered nanowires are generally not preferable for most applications yet radial deposition can occur and may even dominate if growth conditions such as temperature and pressure are not optimized. In the example of Si nanowire growth, since deposition on the radial direction is not catalyzed by metal particles and thus requires a much higher activation energy, radial deposition can be suppressed at low growth temperatures, so the axial growth is the dominating process.[4] Similarly, a cold-wall CVD system with local, rapid heating, as opposed to a hot-wall tube furnace reactor, can promote nanowire growth with minimal tapering.[100]

Thus, a two-step growth recipe was developed to achieve Ge nanowire growth with uniform diameter. First Au nanoparticles were deposited on Si (or SiO_2) substrate after it was properly cleaned (Piranha process followed by diluted-HF treatment). Commercial Au nanoparticles (Ted Pella Inc., part number: 15705-20) are stabilized and suspended in deionized water (DI). They are drop cast (in as received state) on the substrate following the application of surfactant such as Poly-L-lysine (Ted Pella Inc., part number: 18026). Typical application time for Poly-L-lysine is 3-5 min (drop cast on the growth substrate) before the sample is rinsed in DI water and dried with N_2. Au nanoparticles were also rinsed in DI water and dried with N_2 before the sample was quickly transferred to CVD chamber. The first step was carried out at 360 °C, 45 Torr (0.9% GeH_4 in H_2) for 1 min. The purpose of this step is to create the Au-Ge alloy with sufficient yield and help the nanowire nucleate. Thus high temperature is required. The duration was kept to 1 min and remained unchanged for all nanowire lengths, to prevent excessive sidewall deposition which would result in tapered wires at such high temperatures. The subsequent elongation step occurs at 300 °C with the same gas composition for 5-30 min depending on the length required.

The low temperature was key to suppress unnecessary GeH_4 decomposition at the nanowire sidewalls so that tapering can be minimized. A substrate heater was used throughout the process to ensure localized heating to mimic a cold-wall CVD system.

If an amorphous substrate such as SiO_2 is used, nanowires will grow with random orientations. It would be more useful if the growth can be confined to the vertical direction. In fact, vertical growth of Ge nanowires is possible on Si substrates having certain orientations. As explained previously, the VLS process has preferable growth directions due to thermodynamic reasons. In the case of Ge nanowire growth, <111> is the most favorable direction. For example, Jagannathan *et al.* observed that Ge nanowires grew predominately along the <111> direction on crystalline Si substrates.[101] Interestingly, epitaxial <111> Ge nanowire growth is always obtained regardless of the Si substrate orientation. For example, with a (111) Si substrate, most of the Ge nanowires will be vertical; while with a (100) or a (110) Si substrate, the Ge nanowires will instead grow at a tilted angle to maintain the <111> growth direction. For this reason, most of our growth experiments were carried out on (111) Si, to maximize the verticality of the resulting nanowires.

Though vertical growth of Ge nanowire on (111) Si substrate is thermodynamically favorable, good care still must be taken during sample preparation and growth to ensure vertical epitaxy. Similar to the CVD of thin films, high vacuum is generally key to achieve good epitaxy, as the formation of an interfacial native oxide layer will hinder the CVD process and cause degraded yield. It is also found that by adding 0.1M HF into the Au colloid solution (HF concentration is based on total volume) and transferring the sample to the CVD chamber immediately after catalyst dispersion, native oxide formation can be suppressed and high vertical growth yield can be obtained on (111) Si substrates.[45]

By carefully preparing the (111) Si substrate and catalyst solution to eliminate native oxidation, vertical Ge nanowire growth was achieved with a two-step recipe to suppress tapering. Figure 9 shows two scanning electron microscopy (SEM) images taken at 90 and 45 degree tilted angles after 1 min nucleation and 5 min elongation. The growth results showed good vertical yield and uniform height, which means that most of the nanowires were nucleated at roughly the same time. For those non-vertical nanowires, they tend to follow one of the three equivalent <111> directions, which has a fixed 35.3 ° angle with the substrate, indicating good epitaxy from the underlying (111) Si template. Nanowires grown via the two-step recipe indeed showed little tapering as expected. Most of the nanowires still have a slightly wider base, which was formed during the first nucleation step. With 20 nm Au nanoparticles, the diameter of the Ge nanowires obtained was 20.2 ± 1.1 nm (measured near the top of nanowire from SEM). We can observe the remaining Au catalyst on top of the nanowire, with approximately the same diameter as the nanowires. The nucleation yield was not 100%, with un-nucleated catalyst particles scattered across the substrate. The nucleation yield can be improved with a longer nucleation step, which will lead to nanowires with a more tapered shape and more unevenly distributed lengths.

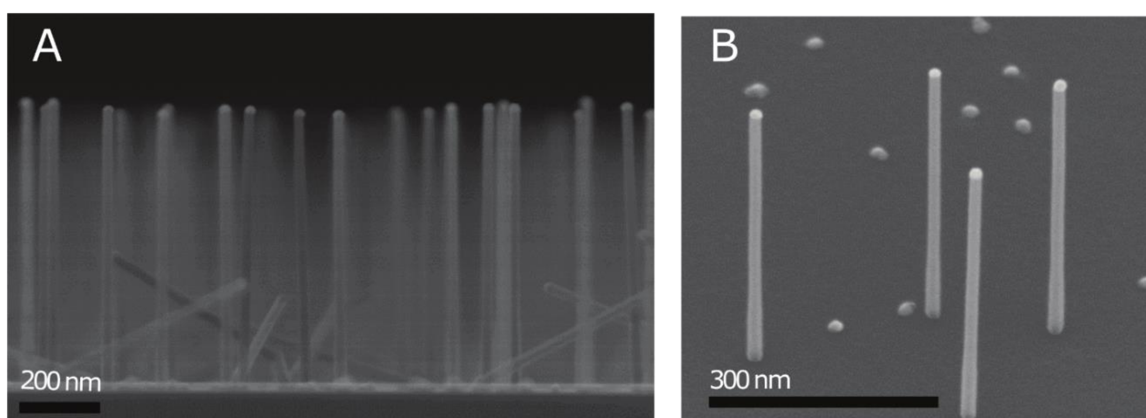

Figure 9. SEM images of as-grown Ge nanowires. SEM images taken from (A) 90 (B) 45 degree tilted angle showing vertical Ge nanowire growth. Adapted with permission from [102]. Copyright 2013 American Chemistry Society.

2.2.2 Si shell deposition

The VLS process can be readily adopted to create atomically sharp heterostructures in a controlled fashion. There are two main categories of nanowire heterostructures: axial heterostructures where segments of nanowires consist of different materials with the same diameter; and radial heterostructures in the form of core/shell or core/multi-shell structures. Similar to the tapering discussed earlier, there are usually two competing deposition processes during VLS heterostructure growth, *i.e.,* decomposition/deposition at the vapor/solid interface of the exposed nanowire sidewalls and precipitation at the liquid/solid interface of the nanowire growth front. The relative growth rates of these two processes determine whether an axial or radial heterostructure will be created: a radial heterostructure will be formed if the sidewall deposition dominates (Figure 10A); while an axial heterostructure can be obtained if reactants are exclusively deposited through the liquid/solid interface (Figure 10B). In the case of radial heterostructure, coating over the catalyst nanoparticle can be observed since sidewall deposition is conformal.

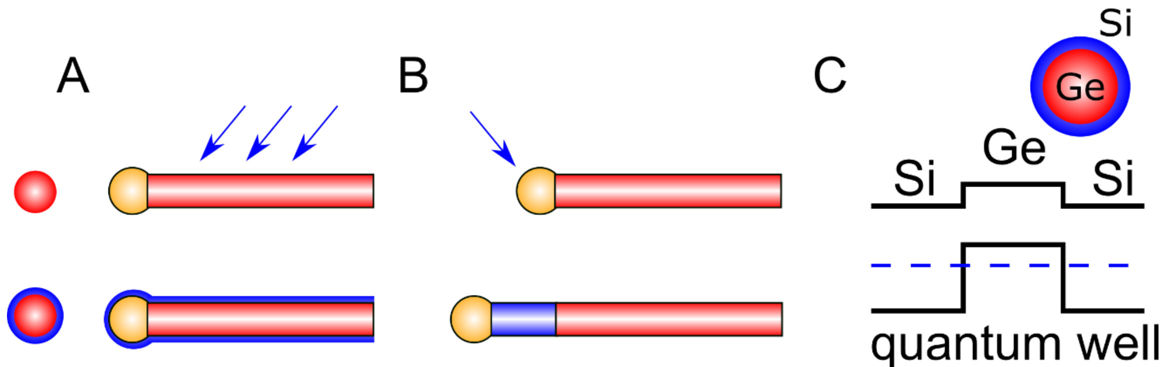

Figure 10. Heterostrcuture formation with VLS method. Schematic of (A) radial and (B) axial heterostructure formation. (C) Band diagram of Ge/Si core/shell heterostructure and quantum well formed in Ge core.

Compared to a homogeneous nanowire, a core/shell nanowire heterostructure can be tailored through band structure engineering to provide better electrical and optical properties. For example, similar to the formation of two-dimensional electron and hole gases in high-electron

mobility transistors (HEMTs), one dimensional electron and hole gases can be obtained in core/shell nanowires by choosing the core and shell materials with appropriate band alignment. As shown in Figure 10C, with a thin Si shell grown epitaxially around a Ge core, a large valence band offset of *ca*. 500 meV between Ge and Si at the interface provides quantum confinement that leads to the accumulation of free holes in the Ge core channel when the Fermi level lies below the valence band of the Ge core. As a result, a Ge/Si core/shell nanowire will act as if it is heavily p-type doped even though both materials are not intentionally doped during the growth.[6] This can be particularly useful since the carriers in the Ge core exhibit a long mean free path and high mobility without dopants acting as scattering centers, making them ideally suited for applications such as high performance nanowire transistors[6] and low-temperature quantum electronics[103]–[105].

In our experiment, the Si shell was deposited *in situ* after vertical Ge nanowires were first grown. The Si deposition process was carried out at a higher temperature (465 °C) to enhance deposition at the vapor/solid interface. A mixture of SiH_4 and H_2, where H_2 is the carrier gas was used (flow rates of SiH_4 and H_2 are 20 and 200 sccm, respectively). The total pressure was kept at 4.5 Torr throughout the shell deposition. It is found that approximately 2 nm of Si shell is conformally coated on a Ge nanowire with 3.5 min of shell deposition.

2.2.3 *in situ* Boron doping

In integrated circuits, semiconductor nanowires can act as versatile building blocks for devices, particularly if different doping types are available with spatial control on an atomic level. The geometry of the nanowires, *i.e.*, high aspect ratio, makes conventional doping methods such as diffusion and ion implantation challenging. Instead, a more practical approach is through *in situ* doping of semiconductor nanowires during growth by adding dopant gaseous precursors to regular

processing gases. The basic principle is simple and both n-type and p-type doping have been realized in commonly used semiconductor nanowires, including Si, Ge, SiC, III-V, II-VI compound and metal oxides.[106]

The doping method is quite similar to VLS nanowire growth. As shown in Figure 8B, dopant atoms can be incorporated into the nanowires at the same time via two modes, namely, radial deposition and axial incorporation through the eutectic alloy. In axial incorporation, dopants enter nanowire through vapor/liquid and liquid/solid interface. The rate of dopant incorporation and final doping concentration are determined by the combined effect of dopant solubility in the liquid alloy and the segregation coefficient at the liquid/solid interface. On the other hand, dopants can enter nanowires radially through adsorption and capture at the vapor/solid interface. This mechanism can probably be described by thin film deposition theory.[106]

The addition of dopant species can also affect nanowire growth depending on the material added and the process conditions. Tapered nanowires due to the unintentional thin film deposition on nanowire sidewalls were usually observed. Such deposition can be minimized by proper tuning of the growth conditions, but enhanced side wall deposition is still often observed, especially in the presence of B_2H_6.[107] This is likely due to catalyzed decomposition of the semiconductor precursor with B_2H_6, a well-known effect in the deposition of Si thin films.[108] Unlike Si nanowires where *in situ* doping by PH_3 and B_2H_6 with minimal morphology change has been demonstrated with optimized growth conditions,[109], [110] *in situ* doping of Ge nanowire often results in tapered nanowires.

We studied the effect of B_2H_6 by adding it to the processing gas with different atomic ratios during the nanowire elongation step. The growth results are shown in Figure 11A-F. The tuning of Ge:B ratio was achieved by replacing part of H_2 carrier gas with B_2H_6 while other process

parameters such as temperature, pressure and time were kept unchanged. Three different ratios were tested, from 100:3 (Figure 11A/B), to 4000:1 (Figure 11C/D) and 40000:1 (Figure 11E/F). The mass flow controller (MFC) that is installed in the CVD system has 200 sccm range with 2 sccm sensitivity. The B_2H_6 (in H_2) source available has B_2H_6 concentration of 99 ppm. Therefore, 40000:1 is the maximum Ge:B ratio we can achieve in the experiment. The details of the growth condition are summarized in Table 1. Nanowires used in these studied were grown on (111) n+ Si substrate which was clean with the standard Piranha process and diluted HF treatment.

	Temperature (˚C)	Total pressure (Torr)	H_2 (sccm)	10% GeH_4 in H_2 (sccm)	1% B_2H_6 in H_2 (sccm)	99 ppm B_2H_6 in H_2 (sccm)	Time (min)	Ge:B ratio
(A-F) nucleation	360	45	200.0	20	-	-	1	n/a
(A-B) elongation	300	45	197.5	20	2.5	-	5	100:3
(C-D) elongation	300	45	197.5	20	-	2.5	5	4000:1
(E-F) elongation	300	45	17.5	200	-	2.5	5	40000:1

Table 1. Process parameters for boron-doped Ge nanowire growth.

The difference in nanowire morphology is evident. Tapering is suppressed by decreasing Boron content. Nanowires shown in Figure 11A-D have a cylindrical base with a large diameter (~96 nm in Figure 11B and ~75 nm in Figure 11D) and cone-shaped body with a Au nanoparticle on top. We hypothesize that the cylindrical part was grown during nucleation while the cone-shaped body was grown during elongation as they are exposed to B_2H_6 gas for different durations. The segment closer to the tip of the nanowire was grown later in the process. As a result, radial coating has a lesser effect on it. Comparing Figure 11B to Figure 11D, the base diameter was reduced for growth with a higher Ge:B ratio while the vertical yield and average nanowire height were almost the same. Nanowires grown in Figure 11E/F have very different morphology,

probably due to non-optimized process parameters since all gas flows were increased ten-fold to achieve 40000:1 ratio. Nevertheless, the nanowires in Figure 11E/F are almost free of tapering. They are much longer than the ones in Figure 11A-D, which were grown with the same duration. These results are consistent with the theory that the presence of B_2H_6 can enhance non-selective decomposition of GeH_4 on nanowire sidewalls.

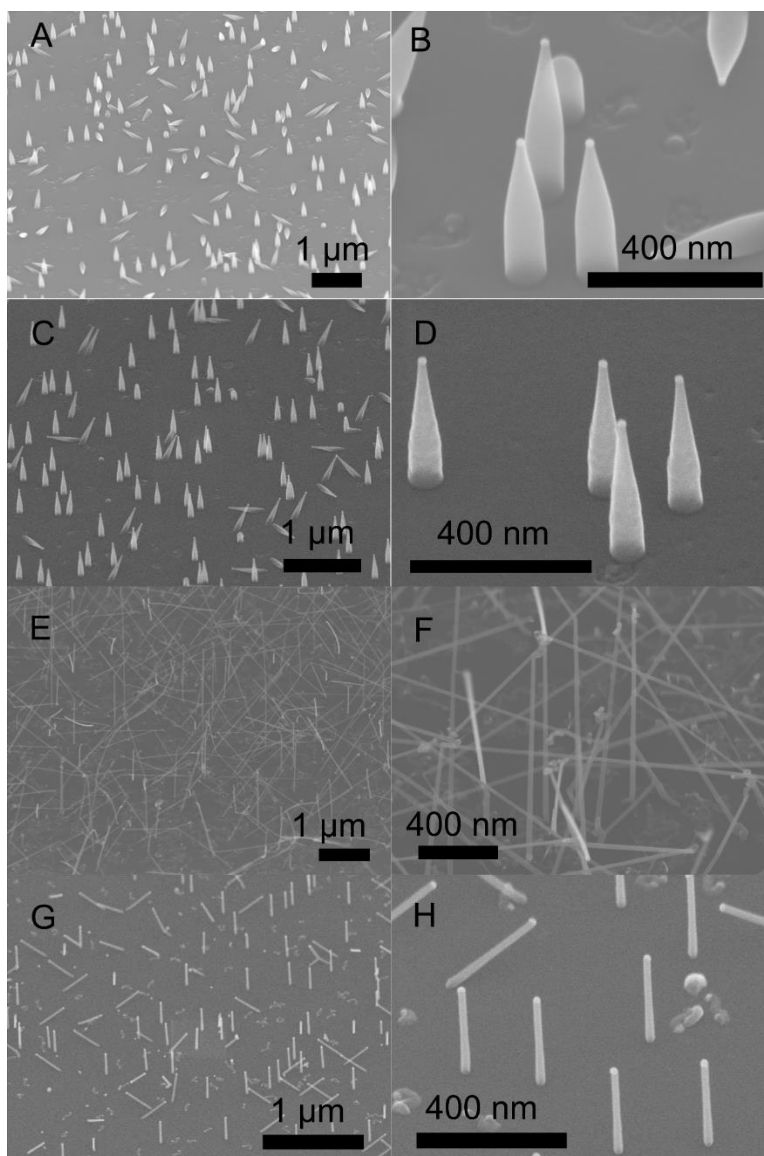

Figure 11. Ge nanowires grown with *in situ* Boron doping. (A-F) B doped NW with different Ge:B ratios of (A-B) 100:3 (C-D) 4000:1 and (E-F) 40000:1. (G-H) Ge nanowire grown with a surface doping layer.

An alternative route to achieve doping without incurring the tapered shape is to dope the nanowire surface without the GeH_4 precursor, eliminating the thin film deposition altogether. For example, Greytak *et al.* successfully doped Ge nanowires, after pure Ge nanowire elongation, with either PH_3 or B_2H_6 in the absence of GeH_4 to produce a self-limiting layer of electrically activated dopant atoms.[100] This approach is verified using our growth chamber too. Figure 11G/H shows vertical taper-free Ge nanowires with B-rich surface on Si substrate. Surface doping was achieved via flowing B_2H_6 (0.05% in H_2) at 380 °C and total pressure of 5 Torr for 1 min *after* normal Ge nanowire growth. This method can be used to dope untapered Ge nanowires using PH_3 or B_2H_6 for electronic devices applications.[100]

2.2.4 Substrate chemistry and Au nanoparticle adhesion

Another important aspect of nanowire growth is control of nanowire density. Since Ge nanowires are catalyzed by Au nanoparticles, a natural solution is to manipulate the Au nanoparticle density until the desired nanowire density is reached. In general, a higher nanowire density can be achieved by keeping Au colloids on the sample for a longer period of time between being drop cast and rinsed off. However, we consistently observed variations in Au nanoparticle density when the doping types of the underlying Si substrate changes, which leads us to consider the effect of substrate on Au nanoparticle adhesion.

Commercially available Au nanoparticle colloids are a very convenient way of acquiring catalysts with a desired size and concentration, but these citrate-stabilized gold colloids do not adhere to Si substrates in the as-received state. The purpose of citrate is to generate a net negative surface charge on the Au nanoparticles to prevent agglomeration. For this reason, a positive charged surfactant such as Poly-l-lysine (Ted Pella Inc. 0.1 % w/v aqueous solution) is often used to treat Si substrate for better Au nanoparticle adhesion.[45] Another and potentially better method

is to add 0.1 M HF into the Au colloid (HF concentration is based on total volume). Not only does the HF help improve vertical yield by preventing native oxide formation, but it can also promote Au nanoparticle adhesion by creating a hydrogen-terminated surface. HF converts the negatively charged citrate ions to neutral citric acid, thus Au colloid solution needs to be prepared immediately prior to use to prevent Au nanoparticles from agglomerating.[45]

We conducted experiments to study the impact of the Si substrate on Au nanoparticle deposition. Four different (111) Si substrates were prepared, with n(p) doped bulk Si wafer and enhanced(reversed) doping at the surface. For fair comparison, undiluted Au colloid with 0.1 M HF added were prepared prior to growth and the Au colloids were kept on the substrates for 5 s for all four samples before rinsing in DI, dried with N_2 gun and transferred to the growth chamber. Growth was carried out following the regular two-step recipe with 1 min nucleation (360 °C at a total pressure of 45 Torr, with 20/200 sccm of GeH_4/H_2, where GeH_4 is diluted in H_2 carrier gas to 10%) and 3 min elongation (300 °C at a total pressure of 45 Torr, with 20/200 sccm of GeH_4/H_2, where GeH_4 is diluted in H_2 carrier gas to 10%).

The growth results are summarized in Figure 12, where SEM images for substrate/surface doping of (A) p/n+, (B) p/p+, (C) n/p+ and (D) n/n+ are shown. Interestingly, Figure 12A/D show very high nanowire density while Figure 12B/C showed the opposite. Thus we can conclude that the surface doping type is responsible for determining Au nanoparticle adhesion and n-type doping facilitates Au adhesion while p-type doping does not. Although we have not extensively studied the exact underlying mechanism, we suspect that the hydrogen-terminated Si substrate can be charged differently at the surface depending on the dopant type (negatively charged for p-type dopant and positively charged for n-type dopant), possibly due to the natural depletion region formed near the surface, which exposes the ionized dopant atoms to Au nanoparticles. The

positively (negatively) charged surface enhances (suppresses) Au particle deposition, since the Au particles are negatively charged due to the surfactants.

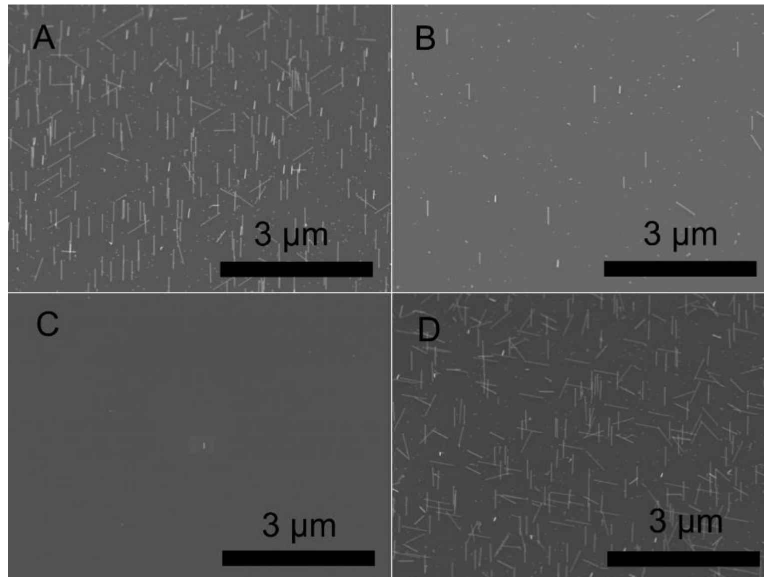

Figure 12. Effect of substrates on nanowire density. Different nanowire density for growth carried out on (A) p/n+, (B) p/p+, (C) n/p+, and (D) n/n+ (bulk/surface) doped substrates. All SEM images are taken with a 45 degree tilt angle.

Depending on the application, sometimes a lower density of nanowires is desired. In this case, simply shortening the Au nanoparticle dispersion time to very short time (*e.g.*, 1-2 s) is not ideal as consistency is hard to maintain. An alternative solution is to dilute the Au colloid with DI water to achieve a lower Au count in the droplet. That way, the dispensing time can be kept at a relatively long time (*e.g.*, > 10 s) for better repeatability and a wider process window.

2.3 Towards vertical device realization

One of the drawbacks of metal-assisted VLS growth is the random distribution of nanowire locations. Currently there is still no easy way to control the distribution of single nanoscale Au particles. Usually a large number of nanowires are grown simultaneously, and then individual ones grown at preferable locations are chosen for subsequent steps. For example, even though we are able to achieve good nucleation yield and desired nanowire density over a large area (typical size

of approximately 1 cm^2), it is still very difficult to grow a single vertical nanowire at a precisely controlled location. While it is acceptable to pick one nanowire and build devices for fundamental studies, the future integration of nanowires with other devices/circuits often requires a more deterministic growth pattern.

2.3.1 Selective area Ge nanowire growth

Since nanowire growth is mediated by metal nanoparticles in the VLS process, it is natural to try to control the nanowire growth sites by controlling the original catalyst nanoparticle positions. For example, Sato *et al.* proposed to use a SiO_2 film as a patterning mask for defining the Au catalyst position in the growth of GaAs nanowhiskers as early as 1995.[111] The concept of patterned growth, or selective area growth has been adopted by several groups in recent years and the results reported are promising with the use of catalyst nanoparticles and advanced lithography techniques such as e-beam lithography.[59], [112] Some other approaches involve the use of nano-manipulation techniques such as atomic force microscopy[113], metal deposition through alumina templates[114], and nanosphere lithography (NSL)[115].

In our study, the goal is not to achieve 100% yield with a precisely designed number of nanowires in each patterned region, but to develop a fast, cost-efficient method to realize selective area growth. The schematic of one approach is illustrated in Figure 13A. First we deposited oxide (~30 nm SiO_2 on top of 20 nm Al_2O_3, SiO2 is deposited through 10% Spin-on-glass 700B from Filmtronics Inc. diluted in IPA) on (111) Si substrate, and then pattern a long stripe (length of ~ 1 cm and width ranging between 2 μm and 10 μm) using photolithography. Wet etch by diluted HF was used to create the trench and expose the Si surface underneath. Dry etching techniques such as reactive ion etch (RIE) was intentionally avoided for fear of damaging the Si surface. Ideally a smooth surface is desired for epitaxy. The wet etch was followed immediately by drying with N_2

gun and Au colloid deposition to mitigate native oxide formation. Since oxide has poor attraction to Au nanoparticles,[45] the majority of the catalysts can be found inside the trench. Then the sample was quickly transferred to the CVD chamber for normal Ge nanowire growth.

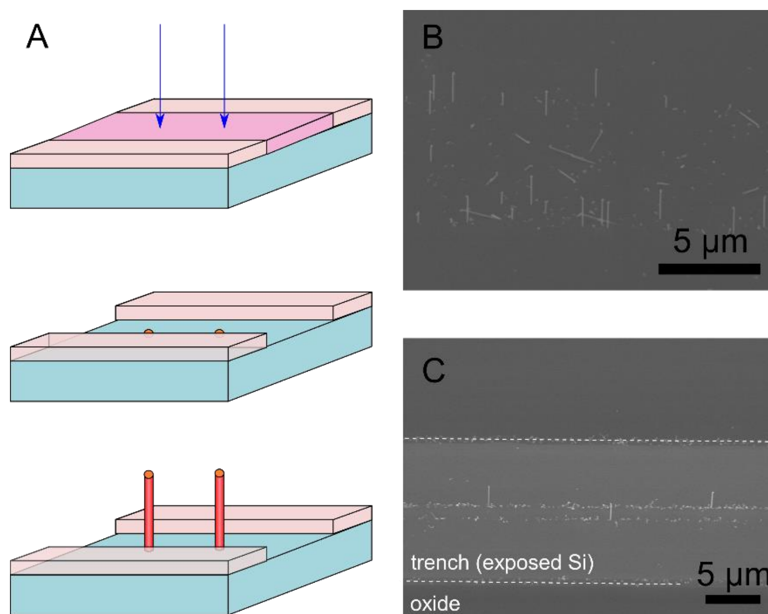

Figure 13. Selective area growth of Ge nanwoires. (A) Schematic of fabrication steps for selective area growth of Ge nanowire inside an oxide trench. (B-C) 45 degree tilted SEM images of patterned region with different nanowire densities.

Representative SEM images of nanowires grown in the trenches are shown in Figure 13B-C, with different densities achieved by changing the Au nanoparticle dispersion time (typical values range from 10 s to 2 min). It is observed that the spacing of nanowires along the length direction of the trench is quite uniform. By varying nanowire density, it is possible to design devices built on a portion of the trench that includes a single nanowire (or a fixed number of nanowires) with good fidelity. Because photolithography was used for oxide patterning, the throughput of this method can be high with a large number of patterns created in parallel. The size of the pattern is limited by the resolution of the lithography tool: trench widths down to 1 μm is achievable within the LNF capability (GCA AS200 AutoStep). The widening seen in Figure 13 was due to the isotropic nature of etching method and can be improved by using a thinner oxide

and a shorter etching time. A multi-step method with RIE first to thin the oxide in the trench down to ~10 nm followed by a short HF etch prior to growth can be potentially employed too. This way it may be possible to preserve a clean, smooth Si surface for nanowire growth while thicker field oxide can still be used. Thicker field oxide helps suppress leakage current in vertical nanowire devices.

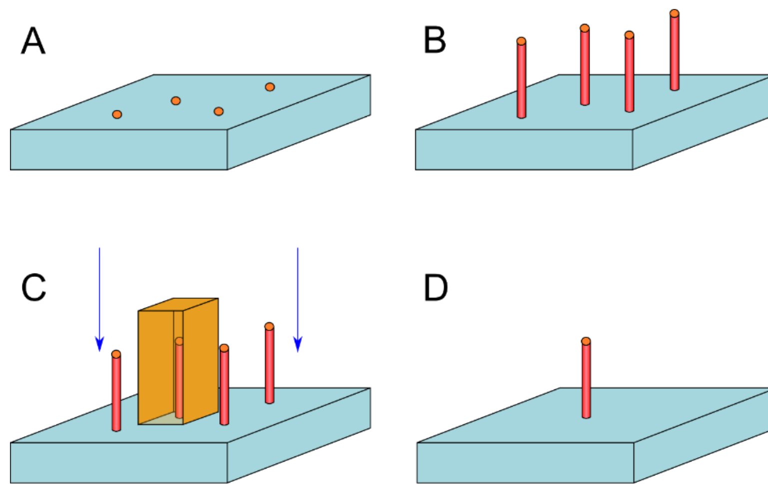

Figure 14. Schematic of controlling nanowire location with post growth RIE.

An alternative, “hybrid”, strategy is to grow nanowires on the whole sample surface first, then selectively etch away the ones that are grown on unwanted portions of the Si substrate (Figure 14). Photoresist is generally sufficient to serve as a mask material since Ge can be etched fairly easily. Additional care need to be taken when stripping the mask material. Due to the high aspect ratio of nanowire structures, critical point drying is the preferable way to dry the samples while preventing them from being accidently knocked down by surface tension. Compared to the previous selective area growth method, this approach has fewer restrictions, since a dry etch can be utilized. It can potentially offer tighter location control since a smaller pattern size can be safely adopted. In contrast, we observed that it became more difficult for Au nanoparticles to deposit inside the oxide patterns as their size reduced (*i.e.,* using narrower trench, or 20×20 μm^2 instead of centimeter-long trench).

2.3.2 Nanowire growth on Ge buffer layer

In addition to site controlled growth, another step towards deterministic VLS growth for 3-D integration is to improve the vertical yield, which is at present in the range of 60-70% in a typical growth. One of the major obstacles to obtaining high vertical yield is native SiO_2 formation. Annealing in H_2 prior to growth can improve epitaxy by removing the native oxide on the surface,[116] but it is not an ideal solution due to the high temperature needed.

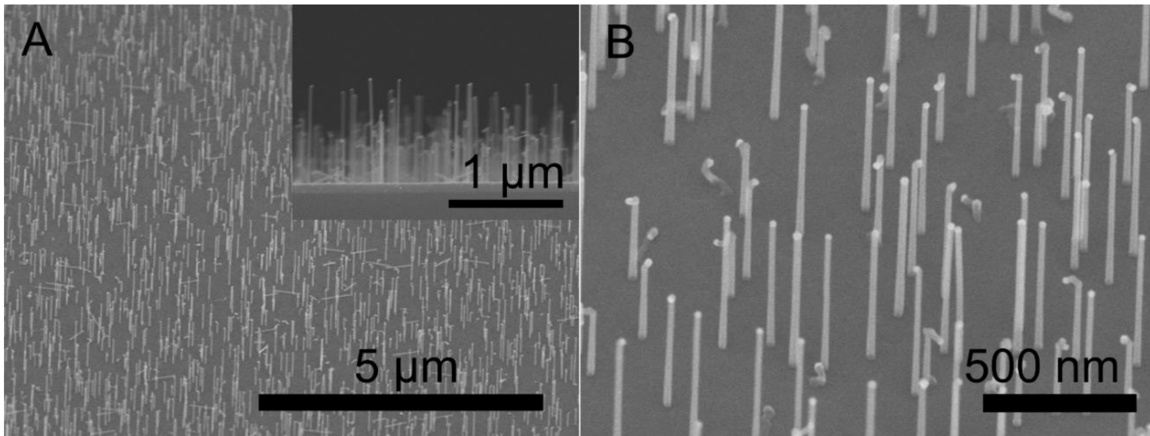

Figure 15. 75 degree tilted SEM images of vertical Ge nanowwires grown on Ge buffer layer. The inset of A is taken from 90-degree angle.

One simple method is to deposit a Ge buffer layer on the Si substrate and use this layer as the epitaxy template.[117] Since GeO_x is much more volatile than SiO_2, it can be readily removed by atomic hydrogen generated during the GeH_4 decomposition, promoting vertical yield. Figure 15 shows SEM images taken after nanowire growth on a Ge buffer layer (deposited for 1 min at 550 °C and 20 Torr, 1% GeH_4 in H_2). Improved vertical yield (> 90%) was demonstrated. From the inset of Figure 15A, the thickness of Ge buffer was determined to be about 80 nm. Due to the relative low process temperature, this Ge buffer likely contained a high density of crystal defects. While it is not suitable for an active device, this Ge buffer layer can serve as a conducting electrode if doped to a high level (*e.g.*, with B_2H_6 or PH_3).

2.4 Summary

In summary, we have achieved VLS vertical Ge nanowire growth on (111) Si substrates with 20 nm Au nanoparticles as catalysts. A two-step temperature profile was adopted for nanowire growth with high nucleation yield, uniform height and suppressed tapering. Several growth modifications were explored and discussed in detail, including radial Ge/Si core/shell heterojunction formation, *in situ* boron doping and controlling nanowire density via Si substrate type. We have also showed progress towards more deterministic nanowire growth, such as controlling the nanowire location via a patterned oxide layer and improving vertical yield with the help of a Ge buffer layer. These results demonstrated that we were able to produce nanowires with the desired composition and morphology. Furthermore, the ability to define nanowire growth location can prove to be very useful in future device fabrication and integration.

Chapter 3

Characterization of Ge/Si heterojunction interface

3.1 Introduction

One of the motivations for this dissertation is the unique properties Ge can offer such as high mobility, low band gap and low tunneling effective mass. Moreover, there are various benefits for the nanowire body, including higher tolerance of lattice mismatch, quasi-1D channel and easier implementation of a surrounding gate geometry. In the previous chapter, we demonstrated the growth techniques for acquiring vertical Ge nanowires on (111) Si substrates. In fact, vertical Ge nanowires on Si substrates provides a very interesting material system that can be useful in many applications.

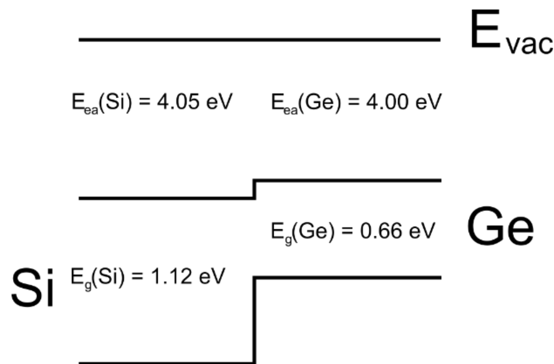

Figure 16. Intrinsic Ge/Si band alignment.

One of the unique properties of this Ge/Si system is the built-in heterojunction. As shown in Figure 16, Ge/Si has type II band alignment with 50 meV (0.56 eV) offset at the conduction (valence) band edges. One of the important applications for type II band alignment is tunneling

based devices, since the tunneling probability is enhanced by the lower effective tunnel barrier. For example, to move from the valence band in Ge to the conduction band in Si, an electron only needs to travel through a 0.61 eV tunnel barrier, lower than the band gap of either Si or Ge. Another important application is the creation of quantum wells, as mentioned in chapter 2. By growing radial Ge/Si core/shell heterostructures, a one dimensional hole gas is induced due to the large valence band offset, which provides carriers even though the nanowire is not intentionally doped.[6]

Considering that our goal is to build Ge nanowire based devices, it is critical to obtain an intrinsic, defect-free Ge/Si interface. For example, the effective tunnel barrier height depends heavily on the *actual* band alignment of the Ge/Si heterojunction, which can be easily distorted by interfacial defects. Thus it is important to characterize the Ge/Si heterojunction properties and ensure the cleanness of the junction before we move on to device level applications.

In this chapter, first we study the Ge/Si heterojunction with transmission electron microscopy (TEM) to verify that the Ge nanowire is indeed epitaxially grown on Si and the interface is defect-free. Second, another important figure of merit for heterogeneous interfaces, the junction abruptness, will be examined with scanning transmission electron microscopy (STEM) and energy dispersive X-ray spectroscopy (EDX). Junction abruptness, which defines how sharp the transition is from one material to another, is important for device applications such as TFET where the high field occurring at from abrupt junctions is beneficial[88].

3.2 Sample preparation

In order to prepare a sample suitable for TEM study, it is necessary to transfer the Ge/Si heterojunction onto TEM grid (lacey formvar/carbon mesh from Ted Pella Inc., part number: 01883-F) while preserving the integrity of the interface. This can be challenging since the Ge/Si

junction is located right at the substrate surface, which happens to be the mechanical weak spot of the whole structure. Attempting direct dry transfer with the as-grown Ge nanowire usually results in breakage at the nanowire base, leaving the Si substrate intact. One approach is to cut a slice of the sample using focused ion beam (FIB). But this method is time consuming and not suitable for imaging multiple nanowire interfaces. Ideally, a simple method to prepare a high density Ge/Si heterojunction structures on one specimen is desired. To this end, we developed a two-step procedure to elevate the Ge/Si heterojunction for the purpose of facilitating dry transfer and subsequent TEM study.

First, the as-grown samples were transferred into a reactive ion etch (RIE) chamber where a short etch was performed to create Si pillars using the Ge nanowires as an etch mask. Etching of Si was achieved through a combination of C_4F_8/SF_6 gas (Pegasus STS 6, pressure is 10 mT at a flow rate of 43/162 sccm, RF power is 600 W and bias power is 40 W). The purpose of this step was to create a neck region (undercut) below the Ge/Si interface so it is no longer the weakest point in the whole structure. Figure 17 shows two representative SEM images of Ge nanowires with etched Si pillars. The pillars have a neck region with an apparently smaller diameter near the Si base.

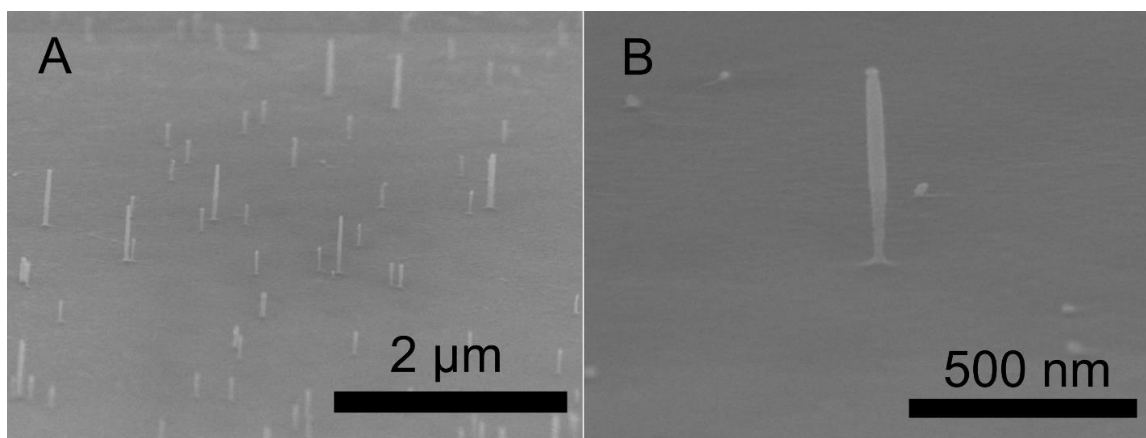

Figure 17. 75 degree tilted SEM images of Ge nanowires on Si pillars after RIE.

To preserve the integrity of the Ge/Si interface, we carefully optimized the etching parameters so that it is primarily an anisotropic etch in vertical direction. Some degree of lateral etch is necessary for creating the neck region, so a delicate balance needs to be found. We observed that the diameter of the Ge nanowires was reduced after this step, likely due to its being etched by C_4F_8/SF_6. The recipe can be further refined by tuning the flow rate of C_4F_8 and SF_6. It is observed that increasing the C_4F_8 content passivates the sidewall, preventing undercut formation. However, with too little C_4F_8, lateral etch can be too aggressive, making the nanowire to fall down and be etched away completely.

After Si pillars were formed, these raised structures were then mechanically cleaved near the neck region and transferred by rubbing the TEM grid on the sample surface. Usually a large quantity of heterojunctions can be found on one TEM grid, as shown in Figure 18A. Figure 18B is a close up view of successfully transferred Ge/Si heterostructures with cone-shaped Si pillar. Note that the Si segment was a little pointy, indicating that the narrower neck region was the break point.

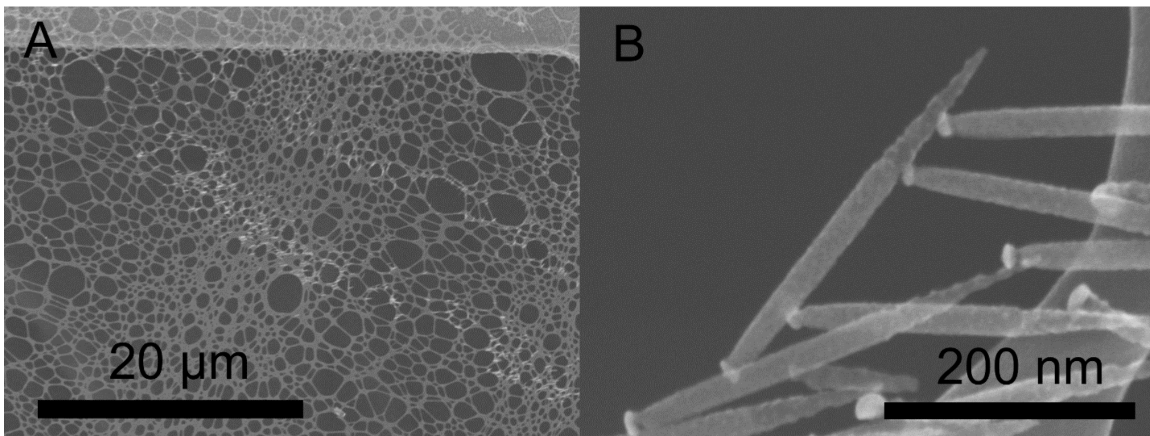

Figure 18. SEM image of Ge/Si heterojunctions transferred on TEM grid.

3.3 Microscopic study on Ge/Si heterojunction interface

3.3.1 HRTEM

Figure 19 shows a representative high-resolution TEM image (HRTEM, JEOL 3011) of the Si/Ge nanowire heterojunction. The epitaxial relationship between Si (brighter region) and Ge (darker region) is evident, and the Ge nanowire clearly inherits the (111) direction from the Si substrate during growth. No obvious edge dislocations were observed at the interface, despite the 4% difference in lattice constants between Si and Ge. These findings are consistent with earlier studies which show that the nanowire geometry can coherently relax the strain and allow efficient heterogeneous integration[11], [16], [85] The thin amorphous layer at the interface (1-2 nm) can be attributed to the native oxide formed prior to Ge nanowire growth. Although various measures were taken to prevent oxide formation, complete elimination was difficult to achieve. However, from HRTEM images, it seems that the thin oxide layer did not prevent epitaxial growth.

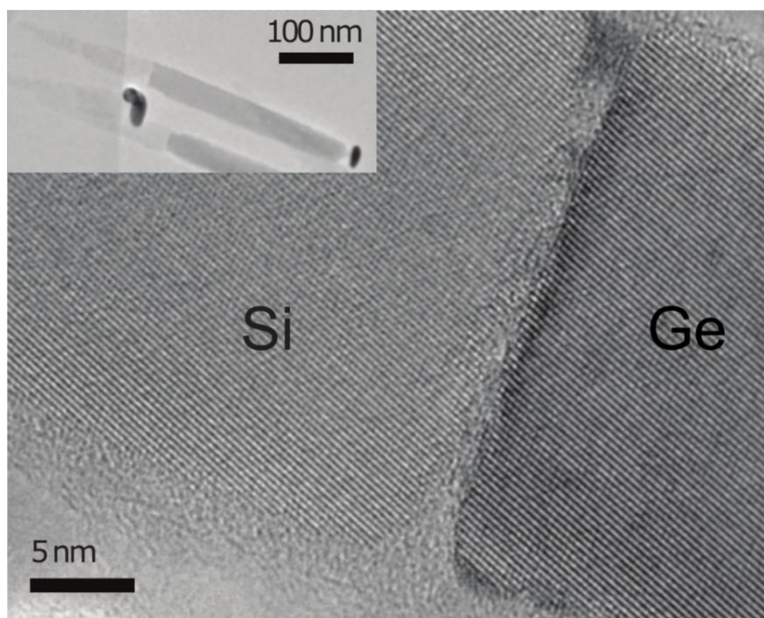

Figure 19. HRTEM image of the nanowire heterostructure showing the Si/Ge interface. Inset is a low-resolution TEM image of the same sample. Adapted with permission from [102]. Copyright 2013 American Chemistry Society.

3.3.2 STEM/EDX line scan

To extract the junction sharpness, we performed elemental mapping using STEM (AEM, JEOL 2010F). Figure 20 shows the EDX line scan for Ge and Si across the Si/Ge heterojunction. A transition width from Si to Ge of about 10-15 nm was obtained, which is on the order of but somewhat smaller than the nanowire diameter. The finite transition width is likely due to the reservoir effect[118] commonly observed in heterostructure nanowire growth since Si has to be depleted from the Au-Si-Ge catalyst alloy before switching to Ge nanowire growth. Although our growth process did not feature a Si nanowire growth step (as done in earlier studies[118]), a liquid Au-Si eutectic was still likely formed during the nucleation step due to the close proximity of the eutectic temperatures of Au-Si (~370 °C) and Au-Ge (~360 °C) [119]. The reservoir effect would cause a trailing edge in the Si composition curve along the nanowire elongation direction, as is evident in Figure 20. To further reduce the transition region width and achieve atomic abruptness, either Vapor-Solid-Solid (VSS) growth[118] or catalysts with low Si solubility can be used[120].

Doping profile is another important parameter for heterojunction based devices. For example, previous simulation studies have shown that a doping gradient of 4 nm/decade (defined as the distance along the junction required for doping concentration to change by one order of magnitude) can degrade the I_{on} in TFET by almost a factor of ten from the ideal junction case[86]. At the low growth temperatures we used, the diffusion of impurities from Si to Ge is estimated to be negligible[121]. Since doping in Ge nanowires is a result of surface effects[122] rather than physically present dopants in the bulk, dopant diffusion from Ge to Si can also be neglected. As a result, the doping gradient of the Si/Ge heterojunction is projected to be in line with the Si/Ge abruptness, from which < 1 nm/decade is estimated from the measured 15 nm transition width (based on the distance between 10% and 90% of maximum Ge/Si counts). With 1 nm/decade, I_{on}

can maintain over 50% of the value in the ideal case[86], thus the Si/Ge system obtained here should be suitable for applications that require abrupt doping profiles such as the TFET.

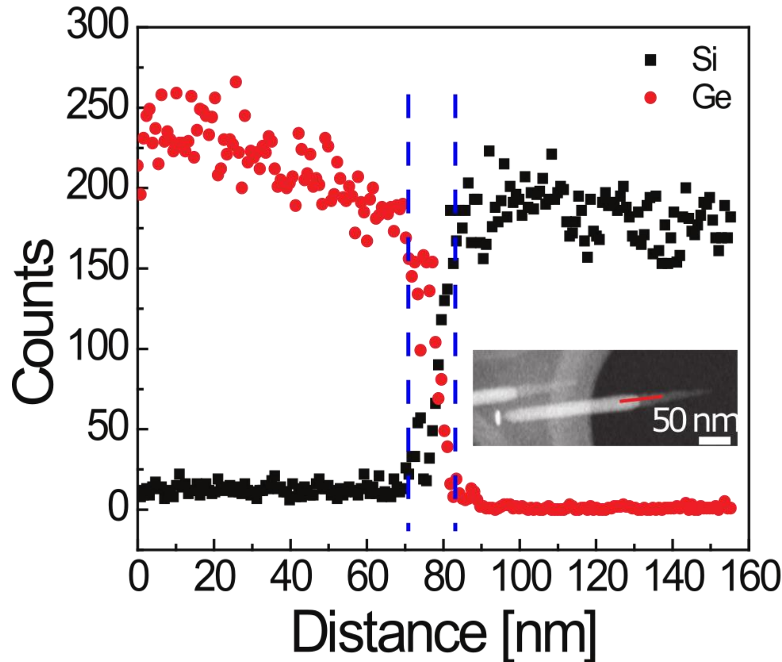

Figure 20. STEM EDX line scan across the Si/Ge heterojunction. The transition region, which are marked by two dashed lines are determined by 10-90% of the maximum count. Adapted with permission from [102]. Copyright 2013 American Chemistry Society.

3.3.3 Additional notes

In the previous sections, we demonstrated that a clean Ge/Si interface can be obtained through a short, post-growth RIE. This technique is not only an approach to characterize the Ge/Si heterojunction with relatively ease, but offers one distinct advantage for device applications as well. Considering that the location of the Si/Ge interface is at the bottom of the nanowire, a potential problem can arise in practice when trying to fabricate a vertical transistor such as a TFET, since there will always be a gate/source offset due to the need to isolate the gate electrode from the substrate (source). While gate underlap can be beneficial for suppressing fringing fields in MOSFETs[123], it degrades both I_{on} and subthreshold swing in TFETs due to reduced electric field and gate control[124].

One way of enabling gate-source overlap and circumvent this problem is to create a raised Ge/Si junction so that gate metal can cover both sides of the junction. However, there is always a concern of Ge nanowire surface damage during etching, especially in thin nanowire devices. In the previous experiments, a slight reduction of the Ge diameter was indeed observed. For certain applications, the nanowire properties can be governed by the surface layer, *e.g.,* in Ge/Si core/shell nanowire. Since the Si shell is typically only 2-3 nm thick, it is very important to protect it from any possible damage. Moreover, because Ge nanowires may serve as the active channel in transistor devices that will be fabricated, we want to minimize damage to the Ge nanowire.

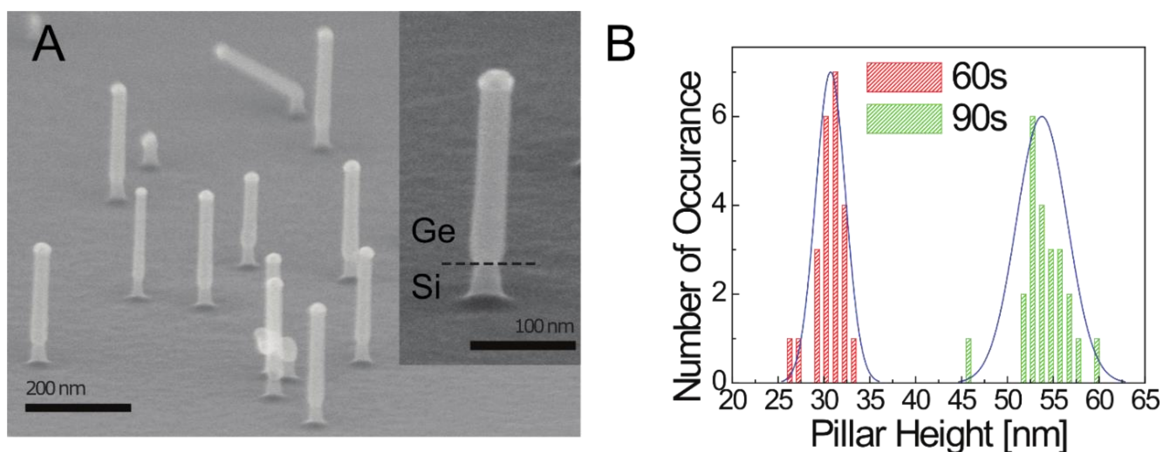

Figure 21. The raised Si/Ge nanowire heterostructure. (A) SEM image of Ge nanowires grown on Si nanopillars. Inset is an enlarged view of one representative nanowire. (B) Distributions of the Si nanopillar heights for 60 and 90 second etch durations. Adapted with permission from [102]. Copyright 2013 American Chemistry Society.

To this end, an alternative process was developed in which the Ge nanowires were epitaxially grown after the etching step, on top of Si pillars. In this process, RIE was performed first to create Si pillars using the Au nanoparticles as self-aligned masks. The flow rate of C_4F_8 /SF_6 was set to 37/168 sccm for straight sidewalls. The Ge nanowires were then grown directly on top of the Si pillars using the same Au particles as catalysts. Due to the use of C_4F_8 gas, an additional etching step with only Ar (20 sccm at the same RF/bias power and pressure, 10 second per 60 second of Si etch) was added to remove potential carbon based polymer that may hinder

epitaxial growth. In our experiment, the last Ar cleaning step was found to be essential for vertical growth. Due to the physical sputtering of Ar, a reduction in Au nano particle size was also commonly seen. For this reason, larger starting Au nanoparticles (~30nm) were used to grow Ge nanowires with ~20 nm diameter.

Figure 21A is a representative SEM image showing the as-grown Ge nanowires on top of the etched Si pillars, with vertical yield similar to the growth on plain Si substrates. The inset in Figure 21A is a zoomed-in view of the resulting structure highlighting the smooth surfaces exhibited by the Ge nanowires. In addition, the height of the Si pillars can be controlled by adjusting the etch time, as shown in Figure 21B, which plots the distribution of the pillar heights for two different etch durations. The ability to control the location of the Si/Ge interface independent of other structural parameters gives us an extra degree of freedom in device design and will thus be desirable in the development of three-terminal vertical nanowire device structures.

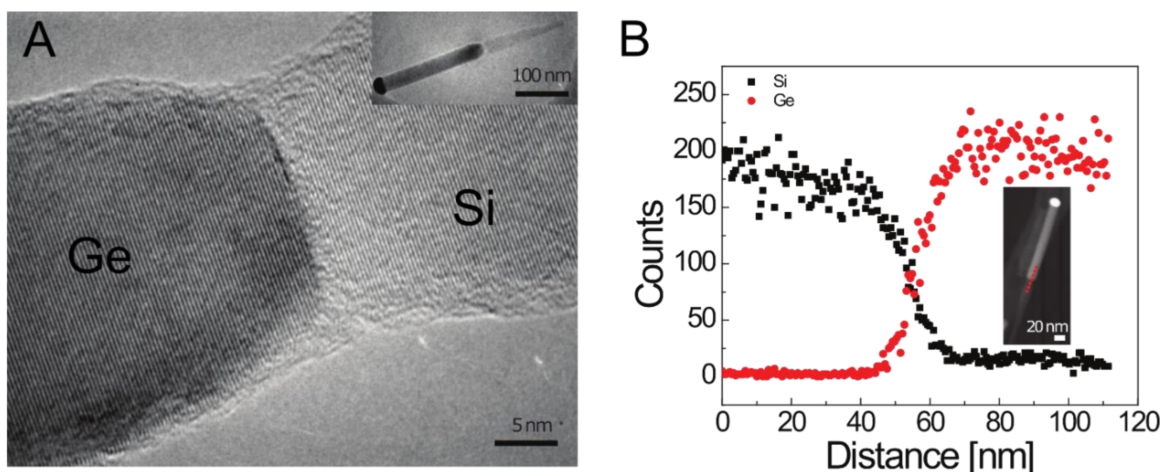

Figure 22. TEM study on Ge/Si heterojunction formed by growing on etched Si pillars. (A) HRTEM image of the Si/Ge interface. (B) STEM EDX line scan data showing Si and Ge concentration *vs*. position acquired from the Si/Ge heterojunction. Adapted with permission from [102]. Copyright 2013 American Chemistry Society.

HRTEM was repeated to examine the interface quality of the heterojunction created in this fashion (For TEM studies, Si pillars are etched with 43/162 sccm of C_4F_8 /SF_6 to create undercut

that allows for successful transfer. Other process parameters such as RF/bias power, pressure and Ar cleaning step remain unchanged.). As shown in Figure 22A, the epitaxial relation between Si and Ge still remains, and results similar to those grown on planar Si substrates were obtained in EDX line scan measurements, as shown in Figure 22B. The parallel lines shown in HRTEM images (Figure 19 and Figure 22A) only serve as indicators of epitaxial relation between two materials. The direction of these lines depends on how the nanowires are placed under electron beam (which is random using the mechanical transfer method). Thus different directions can be observed even though they are of the same crystal orientation. The exact crystal orientation must be determined by selective area diffraction pattern and this is not the focus of our study because we know the Si is (111). Since the etching time is relatively short, we do not expect Au to be etched to a degree where subsequent growth would be affected. Indeed, high vertical yield and good epitaxial relationship can still be obtained.

3.4 Summary

In this chapter, we mainly focus on characterization of Ge/Si heterojunction interfaces in the vertical Ge/Si substrate system. In order to prepare for TEM studies, we developed an etching recipe for creating Si pillars with undercut using Ge nanowires as a self-aligned etching mask. We also demonstrated an alternative method where Si pillars were etched first using Au nanoparticles followed by vertical Ge nanowire growth on top. HRTEM revealed that both methods yielded a clean, epitaxial Ge/Si interface. STEM line scan was used to extract junction abruptness and it was measured to be 10-15 nm, which is on the order of the nanowire diameters. Good interface quality coupled with the ability to control the location of the Ge/Si interface can be very useful in device applications, which we will explore in the following chapters.

Chapter 4

Two terminal devices based on vertical Ge/Si heterojunctions

4.1 Introduction

In chapter 2, we demonstrated vertical growth of Ge nanowires on (111) Si substrate. A thin, optional Si shell can be conformally deposited after the Ge nanowire is formed. Usually Ge nanowire appears to be p-type doped due to surface Fermi level pinning in the absence of *in situ* dopant gas during growth[122]. Its effective doping concentration can be enhanced by creating the Ge/Si quantum well to induce a one dimensional hole gas[6]. We have also studied the impact of the starting substrate on Ge nanowire growth and found that although n-type Si substrates provided better Au adhesion than p-type substrates, the difference in nanoparticle density did not affect growth in terms of nanowire morphology and epitaxy.

In chapter 3, we examined the Ge nanowire/Si substrate heterojunction in detail through TEM. Epitaxial growth was confirmed and junction abruptness of 10-15 nm is extracted from STEM line scan data. These results suggest that the Ge/Si heterojunction formed by VLS process is of high quality and potentially suitable for electronic devices.

In this chapter, we shift our focus from a material system to device demonstration. To verify that a clean, defect-free Ge/Si heterojunction promotes high performance electronics, the simplest semiconductor device structure, a diode, was fabricated and their characteristics carefully

studied. A fabrication process for vertical two-terminal devices will be first presented, and then several device configurations and their behavior will be discussed in detail.

4.2 Fabrication of vertical two terminal heterodiode

The fabrication of vertical devices started with Si substrates with a thick (> 500 nm) thermal oxide layer. Selective area growth mentioned in chapter 2 was used for defining nanowire locations. Trenches (~ 1 cm long and 2-10 μm wide) for nanowire growth were first patterned using photolithography. Using photoresist as mask, the sample was etched in 1M HF to expose the Si surface. After the sample was dried with N_2, Au particles were then drop cast onto the sample, followed by photo resist removal and sample transfer to the CVD system for nanowire growth. First 1 min of nucleation step was carried out at 360 °C (0.9 % GeH_4 in H_2 at total flow rate of 220 sccm and pressure of 45 Torr) followed by 25 min of elongation at 300 °C with otherwise the same processing condition. The duration of elongation step was tuned so the average nanowire length was approximately 1 μm.

25 nm of Al_2O_3 was deposited by ALD (Oxford, OpAL) immediately after the nanowire growth (with H_2O and TMA as precursors at 150°C), followed by spin on glass (SOG, 700B, semiconductor grade, Filmtronics, Inc.) coating and curing at 300 °C for 45 minutes. This Al_2O_3 layer served as an electrical insulation layer to prevent shorting between the top electrode and the Si substrate, while the SOG layer was used as an etch mask to selectively expose the tip of the nanowires during the subsequent wet etching of Al_2O_3 by H_3PO_4 at 36 °C. Then the sample was rinsed in DI water and dried with a critical point dryer to preserve the nanowire verticality. H_3PO_4 etches Al_2O_3 slowly, offering a wide process window while providing good selectivity over SiO_2 and Ge.[125] The use of a wet etch also ensures isotropic etch and prevents ion damage to nanowires during RIE. Figure 23 shows SEM images of vertical nanowires before and after H_3PO_4

etch. In Figure 23A, the properly etched Al_2O_3 coating layer can be seen. In Figure 23B, the sidewall of the vertically standing Ge nanowire is smooth, indicating complete removal of Al_2O_3 and integrity of Ge nanowires.

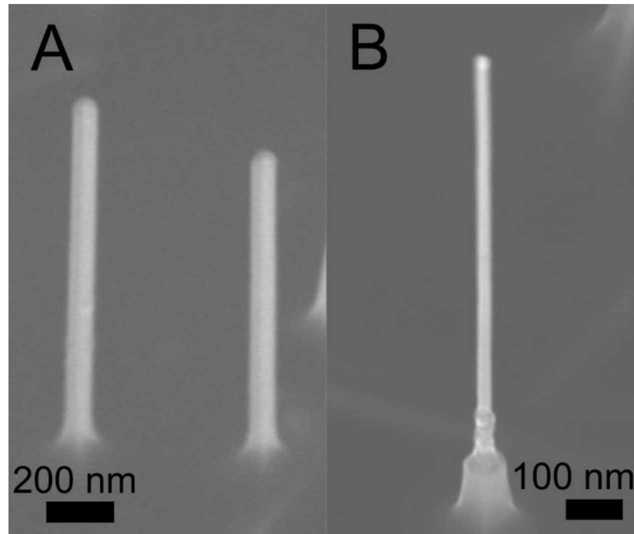

Figure 23. SEM images of Al_2O_3 removal process. 45 degree tilted SEM image of vertical Ge nanowires (A) before and (B) after Al_2O_3 removal.

Afterwards, another photolithography step was used to define the top electrodes (S1813 with thickness of ~1.4 μm from MicroChem was used as photoresist). The sample was then dipped briefly in BHF before being loaded into an ebeam evaporator (Cooke), where 75 nm of Ni was deposited at a 45° angle to contact the nanowire from the sidewall. The purpose of angled evaporation was to provide better metal coverage. A drive-in anneal at 320 °C for 2 minutes in forming gas (5% H_2 in N_2) was performed to form ohmic contacts with the nanowires. The nanowire density was intentionally kept low to ensure that each device (where the top electrode fingers overlap with the patterned region where nanowires grows) only contains one nanowire. For all devices on the same sample, the Si substrate can serve as a global bottom electrode if it is heavily doped. Otherwise, selective areas of the substrate were doped prior to nanowire growth by diffusion and individual electrodes for each device were defined. A schematic of the mask design

and distribution of the electrodes can be found in Figure 24. Major fabrication steps are shown in Figure 25.

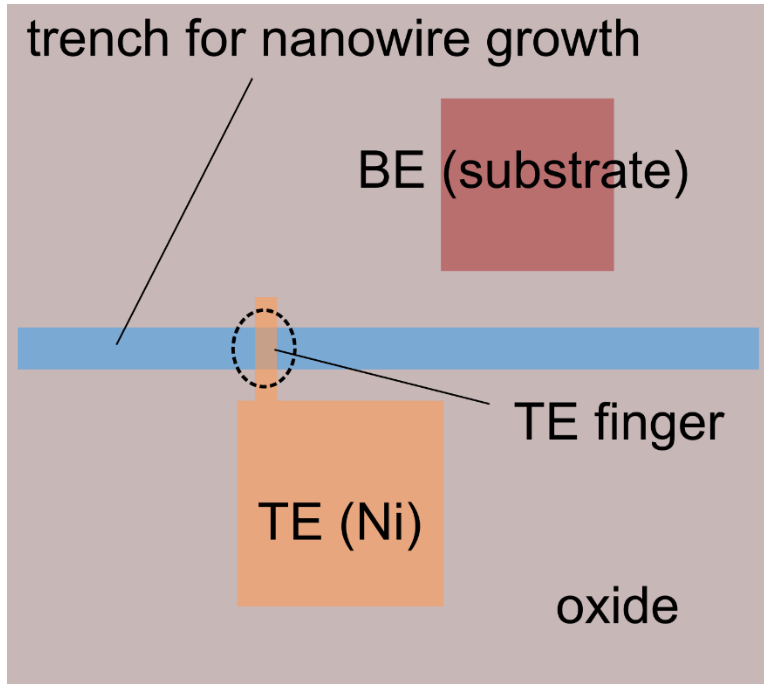

Figure 24. Schematic of the mask design for vertical heterodiodes. The area were the TE finger overlaps with the trench (enclosed by dashed line) contains vertical nanowires this device contacts .

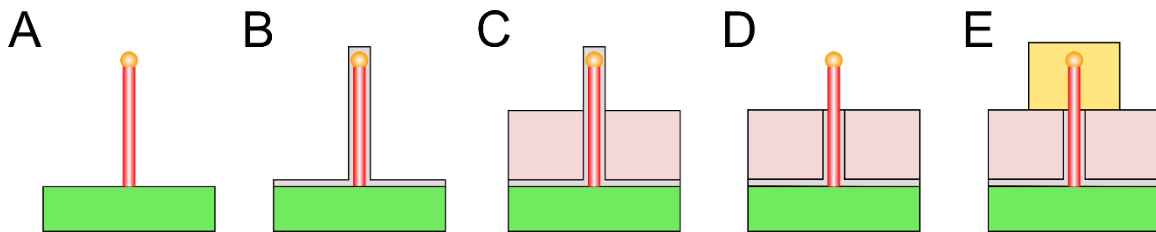

Figure 25. Major steps for the vertical heterodiodes fabrication. (A) Vertical nanowire growth on a Si substrate. (B) Deposition of 25 nm Al_2O_3 as insulating layer via ALD. (C) Planarization with spin-on-glass. (D) Selective removal of Al_2O_3. (E) Deposition of 75 nm Ni as the top electrode.

Three different types of vertical devices were fabricated and characterized. An SEM image of a finished device is shown in Figure 26A. The doping concentration in the Ge nanowire was tuned by using different growth recipes. Due to the surface Fermi level pinning effect, the Ge nanowire usually appears to be p-type doped even though no intentional dopants were introduced

during growth[122]. Furthermore, by coating a thin Si shell around the Ge core (grown by 20/200 sccm of SiH_4/H_2 at 465 °C and 4.5 Torr for 3:30 min), the effective doping level in the nanowire can be greatly enhanced[6], [126] to create p+ doping. On the other hand, the doping type and concentration in the Si segment of the Si/Ge heterojunction can be controlled independently via the choice of substrate doping beforehand. Thus, we were able to tune these parameters independently and create devices featuring different types of Si/Ge heterojunctions. The fabrication process developed is truly very flexible since little change is required to change device configurations.

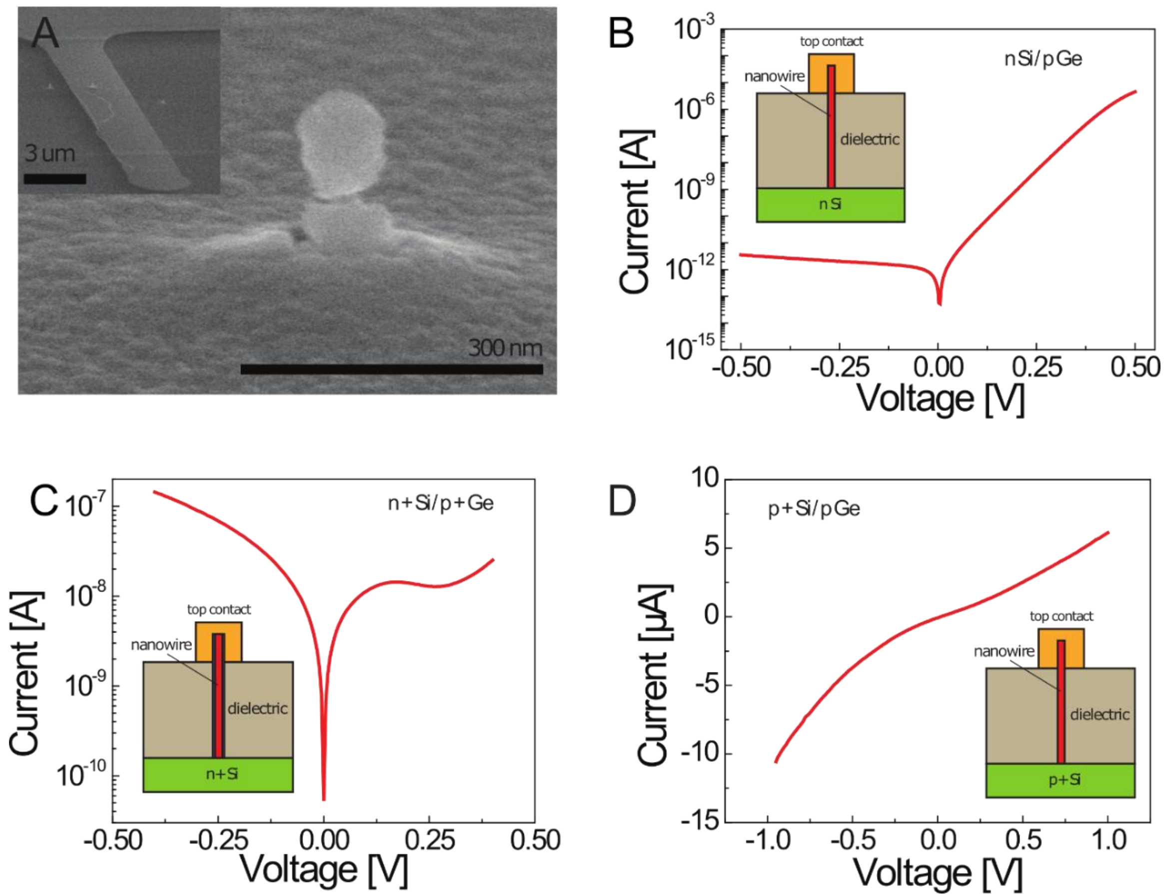

Figure 26. Vertical Si/Ge nanowire heterojunction devices. (A) SEM image of a completed vertical nanowire device covered with Ni top contact. Inset shows that the device contains a single nanowire. (B-D) Representative room temperature I-V characteristics for three different Si/Ge junctions, namely (B) nSi/pGe diode, (C) n+Si/p+Ge Esaki diode, and (D) p+Si/pGe non-ohmic

contact. Insets show corresponding device schematics. Adapted with permission from [102]. Copyright 2013 American Chemistry Society.

Figure 26B-D show the results from 3 different types of devices based on the Si/Ge heterojunction, obtained by systematically changing the doping profile: a Ge/Si pn diode, an Esaki tunnel diode based on a Ge/Si p+/n+ junction, and a rectifying contact (contrary to an ohmic contact) based on a Ge/Si p/p junction. More than 20 devices have been tested and similar behaviors can be consistently obtained for each doping configuration. In the following sections, a detailed analysis and discussion will be presented for each type of device. We would like to point out that electrical characterization and modeling of these devices not only demonstrates the flexibility of this approach and the independent control of the doping profile, but also verified that a nearly-ideal, defect-free Si/Ge heterojunction was obtained using the nanowire epitaxial growth approach, with the desired band lineup.

4.3 Regular PN diode based on Ge/Si p/n heterojunction

The first configuration features an n-Si substrate with moderate doping concentration (resistivity ~0.10-0.16 Ω·cm, which corresponds to a doping level of 4×10^{16} cm^{-3}) and an epitaxially grown p-Ge nanowire. A selective area phosphorus diffusion was performed prior to nanowire growth to enhance the local doping concentration at the electrode contact area to ensure an ohmic contact from the electrode to the Si substrate. The band diagram for the n-Si/p-Ge structure is shown in Figure 27A, from which we can see that the band discontinuities, ΔE_C and ΔE_V, add to the built-in potential for the carriers. The moderate doping on the Si and Ge sides suggests that regular pn diode behavior is to be expected from the device and this was indeed verified by our measurement data, as shown in Figure 26B and Figure 27B at different temperatures.

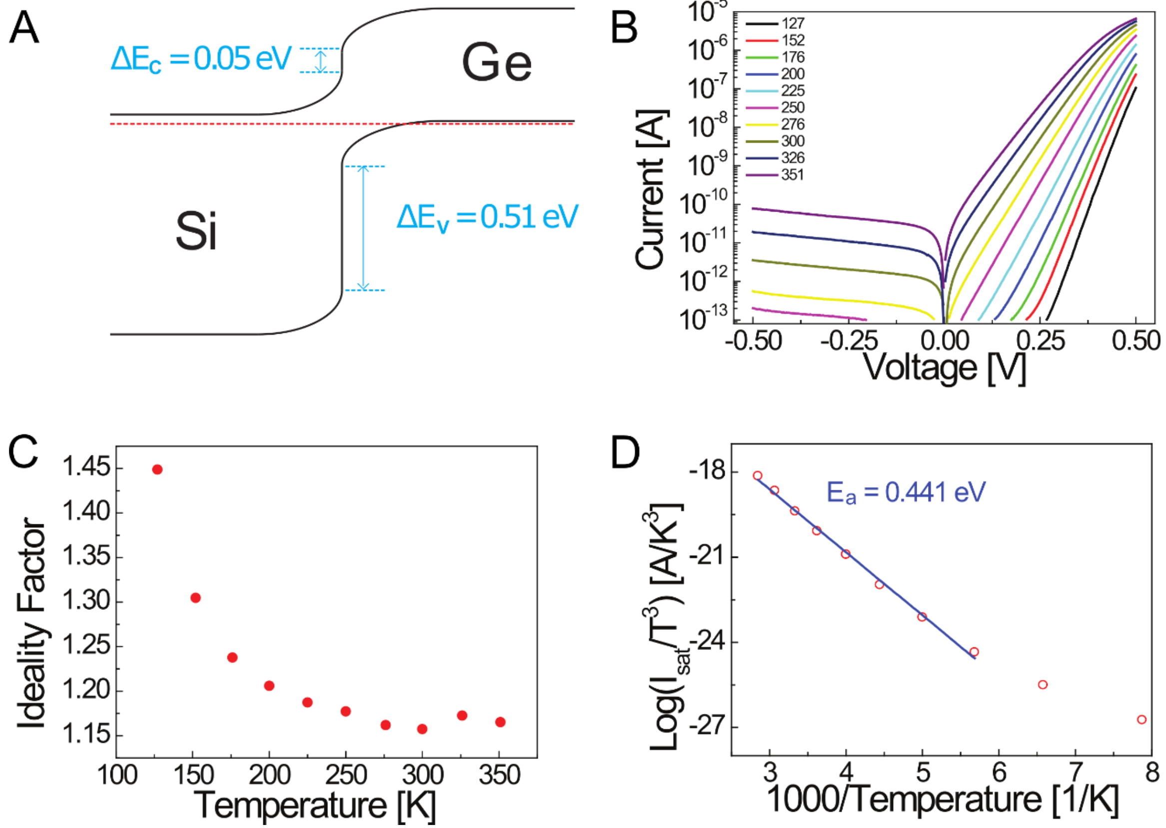

Figure 27. Characteristics of the nSi/pGe diode. (A) Band diagram at zero bias. (B) Logarithmic plot of the measured I-V characteristics at different temperatures. (C) Extracted ideality factor versus temperature. (D) I_{sat}/T^3 *vs*. temperature following Equation (5). An activation energy of 0.441 eV was obtained from the plot. Adapted with permission from [102]. Copyright 2013 American Chemistry Society.

At forward bias, a clear exponential dependence on the applied voltage expected for an ideal pn diode can be seen. At reverse bias, a low leakage current was observed for all temperatures studied here leading to a high rectifying ratio of greater than 10^6 obtained at room temperature. At very high positive biases (*e.g.* > 0.5 V), the current starts to be dominated by series resistance as in conventional diodes and the I-V curve starts to deviate from ideal exponential behavior. Based on the measurement results, the saturation current I_{sat} and the diode ideality factor, n, can be extracted using the well-known pn diode current equation[83].

$$I = I_{sat}(e^{\frac{qV}{nkT}} - 1) \quad \textbf{(1)}$$

Figure 27C plots the extracted ideality factors versus temperature. This device has an ideality factor of 1.16 at room temperature which is very close to the ideal diode condition ($n = 1$) which further verifies the high quality of the Si/Ge heterojunction and the lack of interface defects at the interface. In classical semiconductor device physics, the ideality factor reflects the quality of the diode as a higher generation-recombination current component (*e.g.* mediated by trap states) will result in a deteriorated (larger) ideality factor. The fact that our device showed an ideality factor very close to one indicates that generation-recombination current is small compared to thermionic emission current, which implies a clean Si/Ge interface with low mid-gap trap density. Additionally, the ideality factor n increases as the temperature decreases, since the thermionic emission current scales with n_i^2 while the generation-recombination current scales with n_i. As the temperature becomes lower and n_i becomes smaller, the generation-recombination current will provide an increasingly larger contribution to the overall current, leading to an increased ideality factor at lower temperatures, as has been observed earlier for other pn diodes[127].

We note that the Ge/Si pn devices offer a very low I_{sat} (< 5 pA at room temperature), indicating a lack of significant generation/recombination, tunneling or other types of leakage. The upper bound of the interface trap density can be estimated by assuming all reverse leakage current is contributed by generation through these trap states. Similar to bulk generation-recombination current, generation current at reverse bias due to interfacial trap states can be expressed as follows:[83]

$$J_{it} = en_iS_g \quad \textbf{(2)}$$

Where $n_i = 2.4 \times 10^{13} cm^{-3}$ is the intrinsic carrier density in Ge and S_g is the recombination velocity, which is given by the following:

$$S_g = \sigma v_{th} N_{it}/2 \tag{3}$$

Where σ is the capture cross section area, $v_{th} = \sqrt{3k_B T/m_e^*}$ is the thermal velocity and N_{it} is the trap density. With $m_e^* = 0.12m_0$ and $\sigma = 10^{-13}cm^{-2}$[128], $N_{it} = 1.75 \times 10^{11}cm^{-2}$ can be calculated. Since the exact value for σ is not determined for this particular heterojunction, the estimation of N_{it} may not be accurate. Nevertheless, good ideality factor and low leakage current suggest a nearly ideal Si/Ge interface with very low trap density and prove that vertical integration of Ge devices on Si with high-quality interfaces is indeed feasible. Immediate applications for the Ge/Si pn diode include near infrared photo detectors where Si diodes cannot be used due to their bandgap limitations.

More information on the heterojunction can be obtained by studying the saturation current I_{sat} as a function of temperature. I_{sat} for an ideal heterojunction diode can be expressed similar to that of a homogeneous diode in the following form:[61]

$$\begin{aligned} I_{sat} &= qA\left\{\frac{D_n}{L_n}\coth\left(\frac{W_p^{'}}{L_n}\right)\frac{n_i^2(Ge)}{N_A(Ge)} + \frac{D_p}{L_p}\coth\left(\frac{W_n^{'}}{L_p}\right)\frac{n_i^2(Si)}{N_D(Si)}\right\} \\ &\approx qA\frac{D_n}{L_n}\coth\left(\frac{W_p^{'}}{L_n}\right)\frac{n_i^2(Ge)}{N_A(Ge)} \end{aligned} \tag{4}$$

Or simply (with some approximations),

$$I_{sat} \propto T^3 e^{-\frac{E_g(Ge)}{kT}} \tag{5}$$

Where A is the device area, $D_n(D_p)$ and $L_n(L_p)$ are the diffusion coefficient and diffusion length for electrons (holes), and $W_p{'}$ $(W_n{'})$ is the length of the p (n) section of the junction. The approximation in Equation (5) was justified since the first term dominates given the much higher

n_i for Ge compared to Si ($n_i(Ge)/n_i(Si) \approx 2000$ at room temperature). Equation (5) was obtained by assuming temperature independent doping levels and diffusion lengths. By plotting I_{sat}/T^3 against $1/T$ following Equation (5), a thermal activation process was indeed observed (Figure 27D), with an apparent activation energy of 0.44 eV. The activation energy is lower than that predicted by Equation (5), which is the Ge bandgap of 0.66 eV. The discrepancy may be caused by the fact that the effective doping in Ge, $N_A(Ge)$ in Equation (4) is actually temperature dependent, as earlier studies have observed that the carrier density (effective doping) in Ge nanowires decrease as the devices are cooled down[6]. This effect leads to a slower decrease of I_{sat} compared to predictions by Equation (5), which is based on a constant doping concentration, and thus a smaller apparent activation energy.

4.4 Esaki diode based on Ge/Si p^+/n^+ heterojunction

Since the doping levels of the Ge and Si segments in our approach are decoupled and can be adjusted independently, other vertical nanowire devices can be readily fabricated by tuning the doping profile. For example, by using degenerately-doped Si substrates and by growing degenerately doped Ge nanowires, an n+Si/p+Ge Esaki diode structure with an abrupt doping profile can be obtained. An Esaki diode is a device where band-to-band tunneling (BTBT) current dominates at reverse bias and at low forward bias. Its most significant feature is negative differential resistance (NDR) due to the energy filtering effect of tunneling carriers.[129] As shown in Figure 28, since BTBT requires occupied/empty states to overlap and there is no available states in the bandgap, tunneling current peaks at certain forward bias when overlap is at its maximum. Increasing forward bias further reduces the overlap, and tunnel current decreases as a result. At very strong forward bias, thermionic emission current is dominant, since tunneling is prohibited. In contrast, because increasing reverse bias expands the overlap, reserve current due to

tunneling will simply increase monotonically. Due to the enhance electric field at reserve bias, current can be much higher than that in a forward biased device.

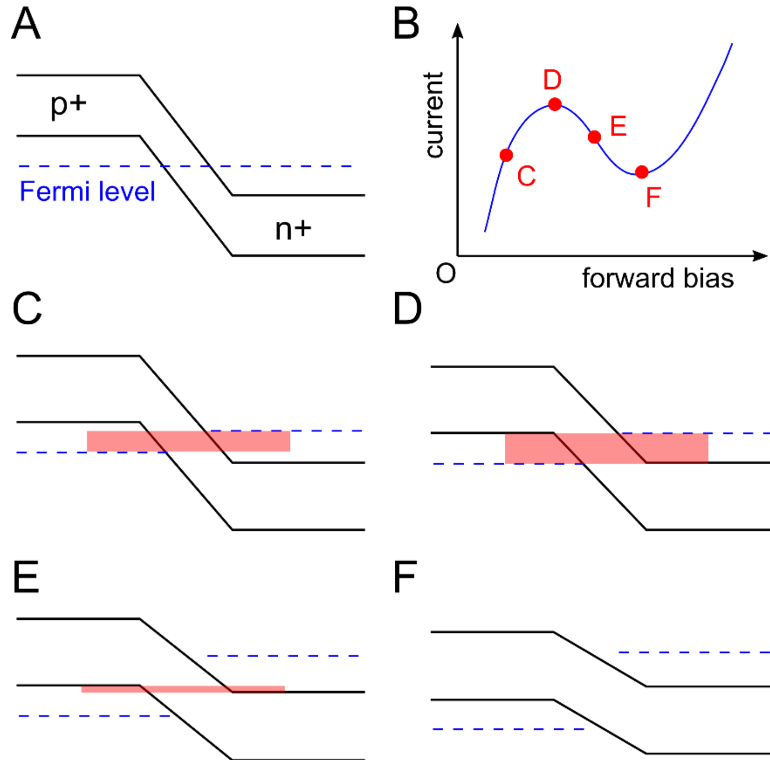

Figure 28. Negative differential resistance in Esaki diodes. (A) Band diagram of an Esaki diode at equilibrium. (B) Schematic of I-V characteristics with NDR. (C-F) Corresponding band diagrams for point C-F in (B). Energy bands where band to band tunneling is allowed are marked with color.

To obtain an Esaki diode, degenerate doping is required on both sides of the junction with an abrupt doping profile. In this work, this requirement was met by using a heavily doped n+ Si substrate (resistivity ~ 0.002 Ω·cm) and epitaxially growing a Ge/Si core/shell nanowire on top of the n+ substrate. Due to the clean Si/Ge heterojunction that offers a narrow tunneling width as a result of the abrupt doping profile and very low excess (*e.g.* generation/recombination, trap assisted tunneling) currents, clear NDR signals were observed in our devices even at room temperature, as shown in Figure 26C. The temperature dependence of the n+Si/p+Ge Esaki diode is plotted in both logarithmic and linear scale in Figure 29B-C. The peak current at room

temperature was measured to be 14.35 nA, which corresponds to a peak current density of 4.57 kA/cm^2 (normalized by nanowire cross-section area, $\frac{\pi}{4}d^2$, where $d = 20\ nm$ is the diameter). Additionally, the tunnel current density measured at -0.5 V reached 3.2 μA/μm (normalized by the nanowire perimeter πd, where $d = 20\ nm$ is the diameter), already among the highest obtained in Si or Ge tunneling devices[69], [130] demonstrated so far at 0.5 V or lower V_{dd}, even without applying a gate voltage.

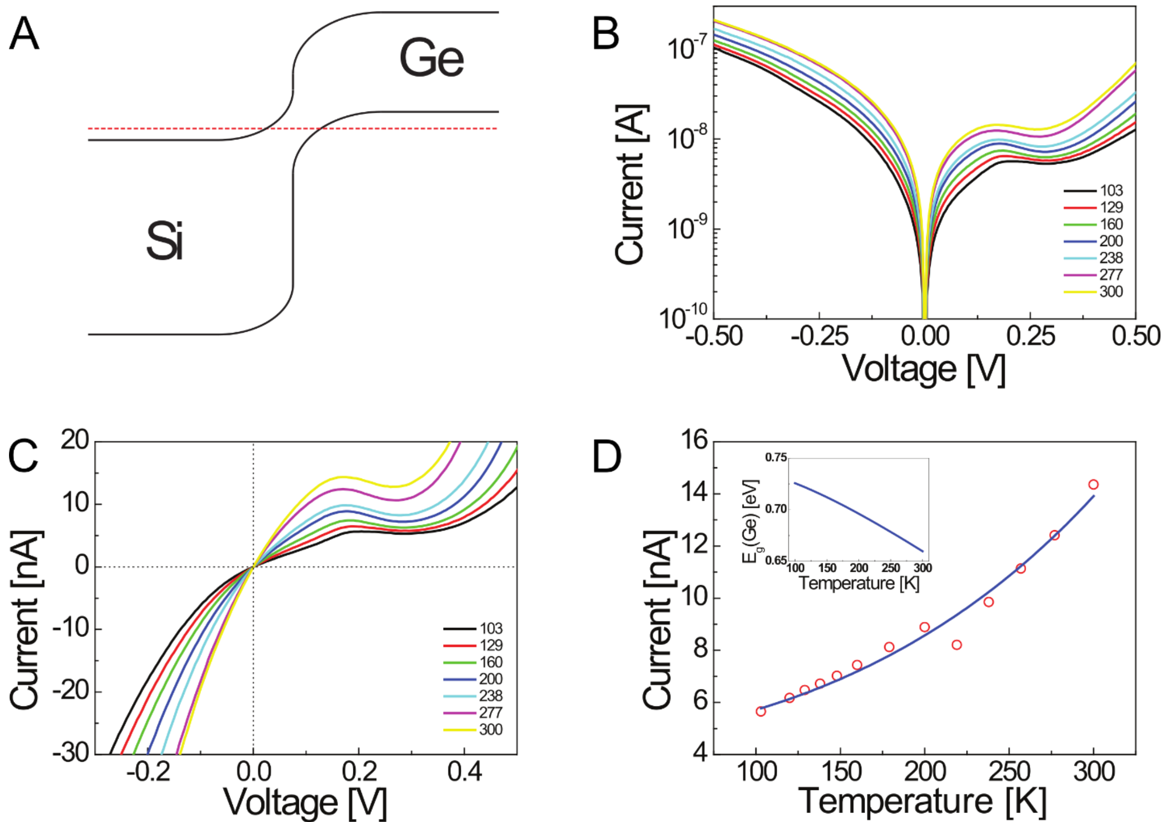

Figure 29. Characteristics of the n+Si/p+Ge Esaki diode. (A) Band diagram at zero bias. (B) Logarithmic plot of the measured I-V characteristics at different temperatures, showing NDR at all temperatures. (C) Linear-scale plot highlighting the peak current and NDR at different temperatures. (D) Extracted peak current (open circles) *vs*. temperature along with results from modeling (solid line). Inset plots the bandgap of Ge at various temperatures. Adapted with permission from [102]. Copyright 2013 American Chemistry Society.

From Figure 29B-C, we observed a weak temperature dependence of peak current, which can be compared with a simple tunneling model as follows[83], [131]:

$$I_p = I_{p0} exp(-\frac{4\sqrt{2m^*}E_g^{\frac{3}{2}}}{3q\hbar F}) \quad \textbf{(6)}$$

Where m^* is the effective tunneling mass, E_g is the effective band to band barrier height and F is the electric field at the junction expressed as:

$$F = \sqrt{\frac{qN(V_{bi} - V_{peak})}{\varepsilon_s}} \quad \textbf{(7)}$$

Where N is the doping level, V_{bi} is the built-in voltage and V_{peak} is the peak voltage.

In this model, the only temperature dependent term is the effective barrier height for band to band tunneling E_g, which is related to the bandgap of Ge through the following equation:

$$E_g = E_g(Ge) - \Delta E_C \quad \textbf{(8)}$$

Where $E_g(Ge) = 0.74 - 4.77 \times 10^{-4} \frac{T^2}{T+235}\ eV$ and $\Delta E_C = 0.05\ eV$ are both calculated from known Ge properties[83].

With $N = 3 \times 10^{19}\ cm^{-3}$, $m^* = 0.037m_0$, $\varepsilon_s = 14\varepsilon_0$, $V_{bi} - V_{peak} = 0.357\ V$ and $I_{p0} = 2.89\ \mu A$, we were able to get a good fit with the extracted peak current, as shown in Figure 29D. These results confirmed that at low bias voltages, band to band tunneling is the dominant term contributing to the total current with negligible contributions from trap-assisted conduction, further supporting the claim that the Si/Ge junction has great potential for use in future tunneling based devices.

4.5 Non-ohmic contact based on Ge/Si p/p heterojunction

The clean Si/Ge interface allows us to study interface properties in these nanostructures in a controlled fashion. Here we use the p+Si/pGe structure as an example. Contrary to an intuitive

picture, the Si/Ge p+/p structure does not lead to an ohmic contact. Due to the presence of a large valence band discontinuity ($\Delta E_V = 0.51\ eV$), the carrier (hole) transport from Ge to Si encounters an abrupt vertical potential wall so that the overall current-voltage characteristics in fact will show rectifying behavior, analogous to the situation in a Schottky junction, as schematically shown in Figure 30A.

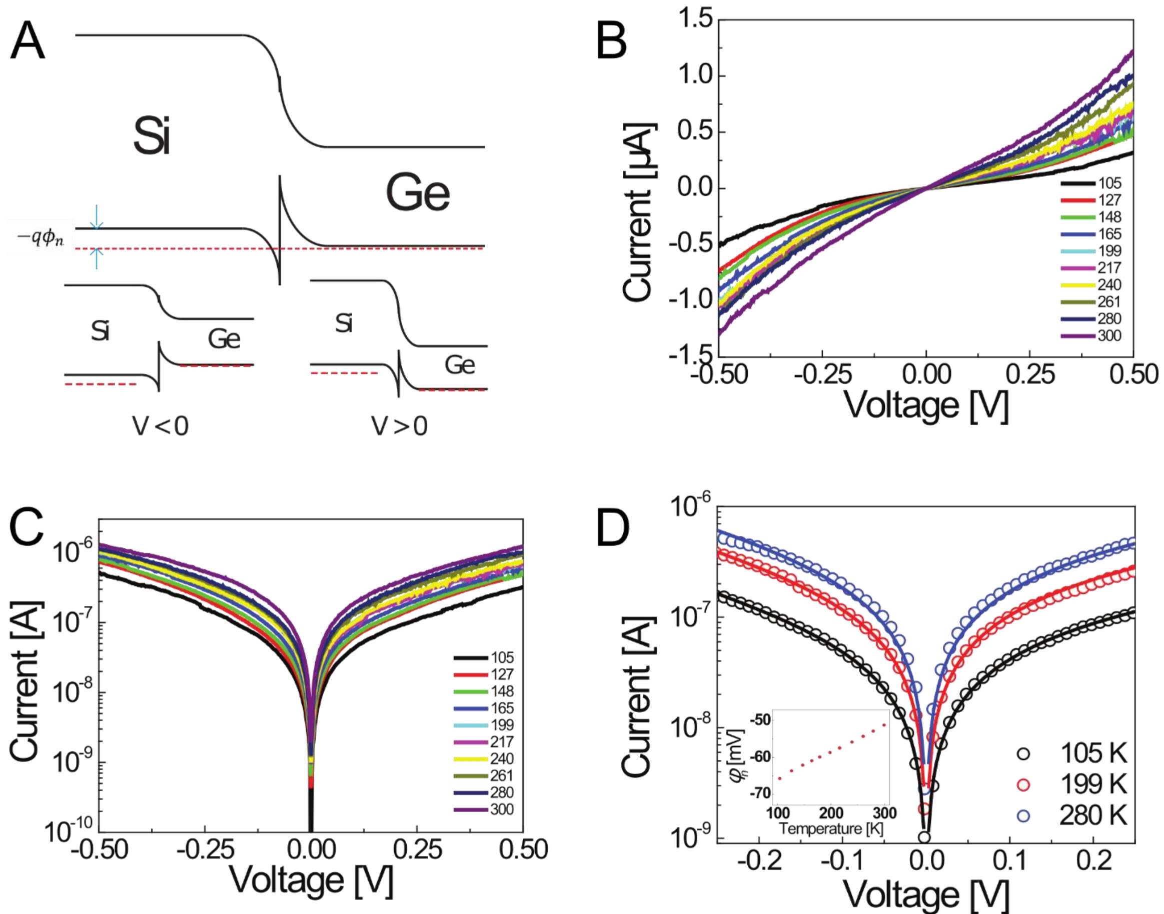

Figure 30. Characteristics of the p+Si/pGe rectifying diode. (A) Band diagrams at equilibrium and (insets) at different bias conditions. (B-C) Linear and logarithmic plots of the measured I-V characteristics at different temperatures. (D) Theoretical calculation results (solid lines) in comparison with measured data (open circles) at different temperatures. Inset shows the calculated ϕ_n *vs*. temperature. Adapted with permission from [102]. Copyright 2013 American Chemistry Society.

We note that this effect can only be systematically studied if the interface is clean as interface states can easily distort the band discontinuity. In this study, a p+ boron-doped Si

substrate (resistivity 0.0022-0.0025 Ωcm) was used and a p-type Ge nanowire was grown epitaxially on top. The insets of Figure 30A show the band diagrams at different bias conditions, with the voltage applied on the Ge nanowire and the Si substrate grounded. From the band diagram the carrier transport is expected to be similar to that of a forward (reverse) biased Schottky barrier when a negative (positive) voltage is applied on the Ge nanowire. This analogy is made by assuming all majority carriers (holes) coming from the Ge side need to be emitted from the bottom of the triangular well formed due to valence band offset at the interface. Similar to a metal in a Schottky contact, the height of the barrier that carriers must overcome is independent of the bias (it is ΔE_V in our device).

A numerical simulation (Sentaurus, Synopsys Inc.) was first performed to verify our hypothesis about the presence of an emission barrier at the pSi/pGe heterojunction. The simulated structure is a 2-D junction composed of Si and Ge. Uniform doping was used on both sides with $N_D(Si) = 10^{20}\ cm^{-3}$ and $N_A(Ge) = 10^{19}\ cm^{-3}$. The junction was assumed to be perfectly abrupt. In addition, band to band tunneling was included in the simulation. The results are shown in Figure 31 where representative I-V curves as well as band diagram at equilibrium, forward bias and reverse bias are included. As expected, features similar to a Schottky contact are evident near the valence band at the Ge/Si heterojunction interface. In addition, the non-ohmic I-V characteristics also confirmed the presence of a barrier. Due to the simplicity of the structure, this simulation was for qualitative demonstration only while quantitative analysis was performed using a more detailed tunneling model described in the following part.

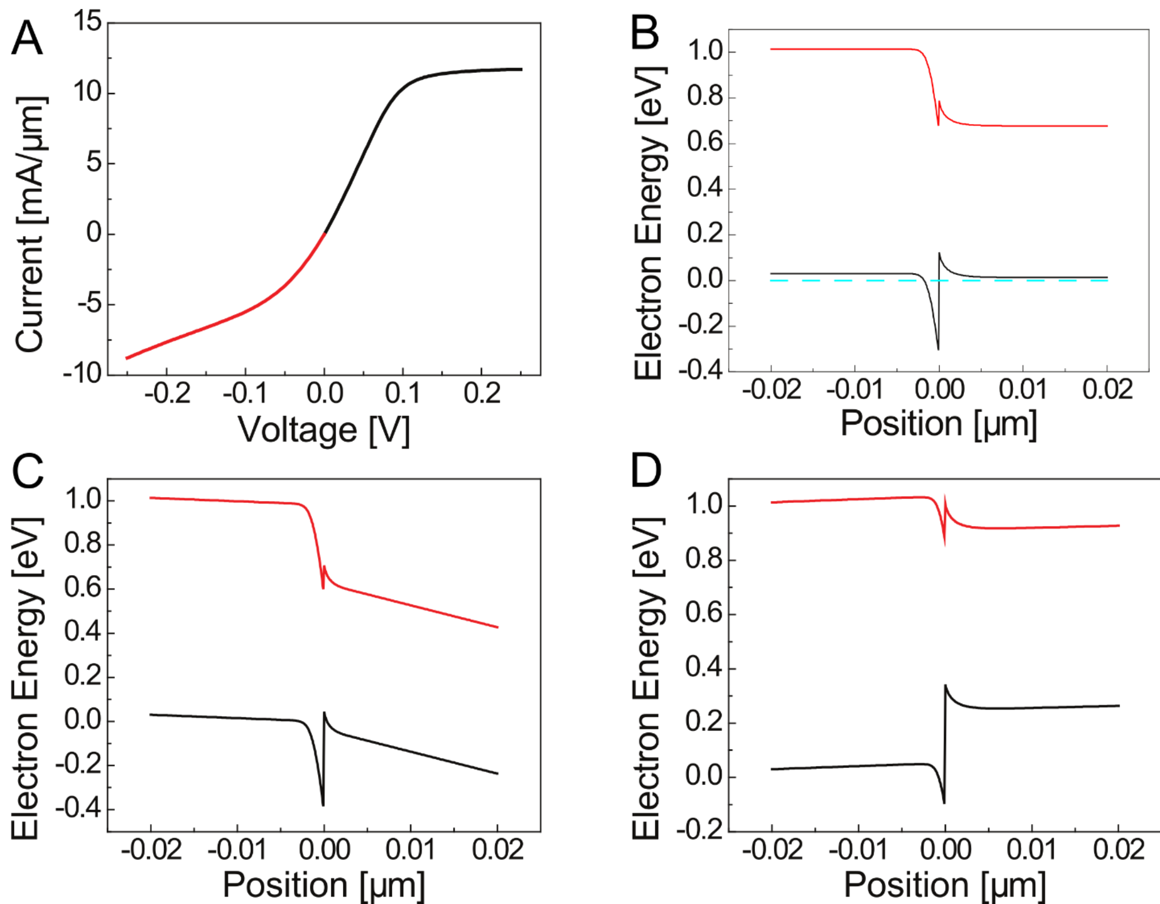

Figure 31. Numerical simulation results of the pSi/pGe structure using TCAD. (A) I-V characteristic showing a "leaky" diode. (B-D) Band diagrams obtained at (B) 0V, (C) +0.25V and (D) -0.25V. Adapted with permission from [102]. Copyright 2013 American Chemistry Society.

As shown in Figure 26D and Figure 30B-C, our measured data indeed revealed a rectifying, as opposed to linear current-voltage characteristics. Note that under reverse bias (when the applied voltage is positive), the current did not saturate but rather increases exponentially as a function of the bias voltage, due to contribution from tunneling through the reverse-biased junction. The I-V characteristics at different temperatures of the Si/Ge p+/p junction have been systematically studied (Figure 30B-C) and compared with a field emission model.[132]

In this model, current through the p+Si/pGe nanowire junction has the following forms:

$$J_{FE} = \frac{A^{**}T\pi exp\,[-q(\phi_{Bn} - V_F)/E_{00}]}{c_1 k sin(\pi c_1 kT)}[1 - exp\,(-c_1 q V_F)] \quad \textbf{(9)}$$

for forward bias. And,

$$J_{FE} = \frac{A^{**}T\pi}{c_1 k sin(\pi c_1 kT)} exp\,[-\frac{2(q\phi_{Bn})^{3/2}}{3E_{00}\sqrt{\phi_{Bn}+V_R}}][1 - exp\,(-c_1 q V_R)] \quad \textbf{(10)}$$

for reverse bias.

Where $V_F(V_R)$ denotes the forward (reverse) bias voltage, A^{**} is the effective Richardson constant, ϕ_{Bn} is the emission barrier height and ϕ_n is the difference between the Fermi level and the valence band edge in Si (negative since it is degenerately doped). The parameters E_{00} and c_1 are defined by:[132]

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N}{m^{*}\varepsilon_s}} \quad \textbf{(11)}$$

$$c_1 \equiv \frac{1}{2E_{00}} log\left[\frac{4(\phi_{Bn} - V_F)}{-\phi_n}\right] \quad \textbf{(12)}$$

for forward bias. And,

$$c_1 \equiv \frac{1}{E_{00}}\sqrt{\frac{\phi_{Bn}}{\phi_{Bn} + V_R}} \quad \textbf{(13)}$$

for reverse bias.

Here N is the doping level in Si, $\varepsilon_s = 11.7\ \varepsilon_0$ is the dielectric constant for Si and m^{*} is the effective mass for tunneling through this particular heterojunction.

Although there seems to be a lot of parameters in these expressions at first glance, most of them can be readily determined from known parameters. For example, the doping level $N = 5 \times 10^{19}\ cm^{-3}$ can be converted from the resistivity-doping curve for bulk silicon and is assumed to

remain unchanged throughout the temperature range in which the measurement took place. This is a valid assumption since the ionization energy for dopants in degenerately doped semiconductor is insensitive to temperature[61]. In addition, ϕ_n can be calculated using the empirical expression $-q\phi_n = E_V - E_f \approx kT[ln\left(\frac{N}{N_V}\right) + 2^{-\frac{3}{2}}(\frac{N}{N_V})]$ [133] for degenerate semiconductors with the bulk Si effective valence band density of states $N_V = 3.5 \times 10^{15}\ T^{1.5} cm^{-3}$. The Schottky barrier height is assumed to be fixed at $\phi_{Bn} = 0.51\ eV$, the same as the valance band discontinuity ΔE_V between Si and Ge.

The calculated results and measured data for the same device at different temperatures is plotted together in Figure 30D. The good agreement between the theoretical prediction and measured data again implies that our Si/Ge system has a clean interface and is free of extrinsic effects such as defect states (which would modify the barrier height as bias changes) and series resistance (which would 'flatten' the overall current-voltage characteristics). The effectiveness of the fitting also verified our prediction of the presence of an emission barrier despite the fact that both Si and Ge were doped the same type. This is an interesting phenomena and calls for additional attention as one tries to obtain ohmic contacts in heterogeneously integrated semiconducting materials.

4.6 Summary

In this chapter, a fabrication process for a two terminal vertical diode based on Ge nanowires integrated on Si was developed. This device structure provides an excellent platform to study the electrical properties of Ge/Si heterojunction interfaces. This approach also allows independent control of the doping type/concentration on both the Si and Ge sides and leads to systematical tuning of device performance. The nSi/pGe heterojunction diode exhibited an ideality

factor of 1.16 and 10^6 rectifying ratio at room temperature, while the n+Si/p+Ge Esaki diode showed NDR at room temperature with a high peak current density of 4.57 kA/cm^2. Analysis of a p+Si/pGe heterojunction revealed the presence of an emission barrier due to the discontinuity of valence band edges at the heterojunction, raising an important question when making contact to heterogeneously integrated nanomaterials. All of these different behaviors can be well explained through theoretical modeling, and suggest a close to ideal Si/Ge heterojunction interface with low defect density.

Chapter 5

Junctionless transistor based on vertical Ge/Si core/shell nanowires

5.1 Introduction

As the scaling of conventional CMOS transistors continues, other technological challenges began to emerge. This time, the problems are rooted in the fundamentals of building blocks of modern integrated circuits, namely MOSFETs. For decades, the basic operating principle of MOSFETs has revolved around multiple p-n junctions, which act as barriers to selectively block current flow. To keep up with the size reduction, heavier doping was implemented for both sides to create narrower junction, which posed a severe limit on the thermal budget to avoid unnecessary diffusion. Moreover, random dopant variation due to statistical fluctuation of their population and location in the channel of a modern transistor can lead to non-negligible variation to device characteristics such as threshold voltage and on-state current.[134] To this end, junctionless transistors, *i.e.*, gated resistors, were re-discovered in recent years.[135], [136] With uniformly doping source, channel and drain, junctionless transistors have eliminated the junctions altogether. The operation principle of a junctionless transistor is actually quite simple. As illustrated in Figure 32, current flows through the heavily doped channel at ON state (Figure 32D) and is cut off by fully depleted channel at OFF state (Figure 32A). The key is to keep the channel thin so that it permits full depletion at a reasonable voltage. Another interesting property with junctionless transistor is that the current mainly flow through the center of the channel (as opposed to surface

conduction in MOSFETs), so it is more resistant to scattering due to surface roughness and interface defects that reduces carrier mobility.

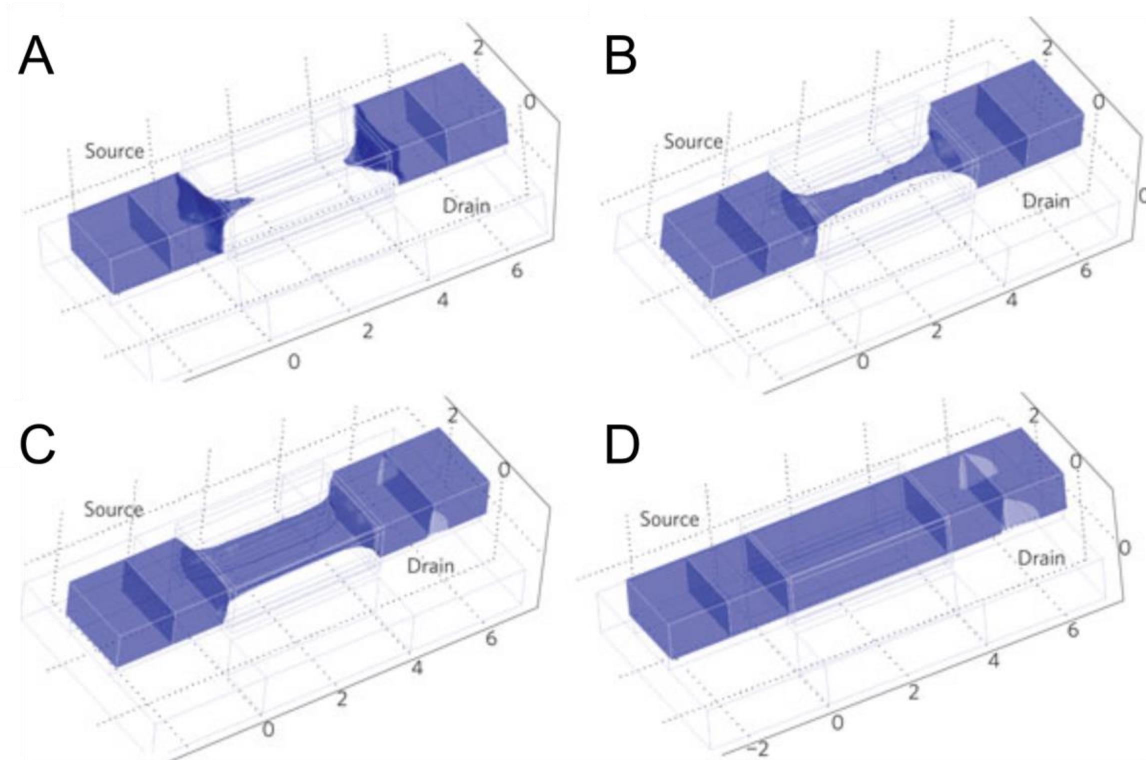

Figure 32. Simulation of electron density for an n-type Si junctionless transistor. The device has a channel width, height and length of 20, 10 and 40 nm, respectively. The n-type doping concentration is 1×10^{19} cm^{-3}. Simulations are carried out for V_{ds} of 50 mV and V_{gs} of different values. The plots were generated by solving the Poisson equation and the drift-diffusion and continuity equations self-consistently. (A) Below V_{th}, the channel region is depleted of electrons. (B) At $V_{gs} = V_{th}$, a string-shaped channel of neutral n-type Si connects source and drain. (C-D) As V_{gs} increases, conduction channel expands in width and thickness until whole channel is used for carrying current. Reprinted by permission from Macmillan Publishers Ltd: Nature Nanotechnology, 5: 225-229, © 2010. [136]

We would like to point out that our Ge/Si nanowire is naturally suitable for junctionless transistor applications for a number of reasons. First, due to the presence of high density one dimensional hole gas in Ge core induced by Si shell, Ge nanowire behaves like heavily doped p-type semiconductor though no intentional dopants were involved during synthesis. Heavily doped body ensures enough carriers in the channel, which allows Ge nanowire to conduct sufficient current to meet the ITRS requirement. Second, thanks to its nanoscale size, Ge nanowire is ideal

for junctionless transistor operation. As mentioned above, the key in successfully turning device OFF is to achieve full depletion, which has been an obstacle for many years after the initial concept was proposed. Until recently, advances in semiconductor manufacture technologies have finally realized Si body with ~10nm thickness, which is sufficiently thin to be full depleted. With diameter of 20 nm, Ge nanowire can reach full depletion at surface potential of less than 200 mV (assuming channel doping of 5×10^{18} cm^{-3}), thus allows proper switching within a reasonable voltage range.

5.2 Fabrication of vertical junctionless transistors

To build a junctionless transistor based on vertical Ge/Si nanowire grown on Si substrate, locations of nanowire need to be defined, which was achieved via the method introduced in chapter 2 where nanowires were first grown then selectively etched. It would be helpful to re-iterate the process here. Initially, nanowires were grown on the whole sample (about 16×16 mm^2). Since active regions (where vertical nanowire is contacted by metal electrodes and used as conduction channel) with size of about 15×15 μm^2 only populate part of the total surface area, the sample was patterned by photolithography and nanowires located outside the active area were etched using diluted HF solution followed by RIE (1 min at pressure of 50 mTorr, TCP/bias power of 500/25 W and 50/20/5 sccm Ar/SF_6/O_2). After that, protective Al_2O_3 oxide was striped and a new layer of 10 nm Al_2O_3 was deposited via ALD as high-*k* gate dielectric.

After depositing gate dielectric, 50 nm of tungsten (W) were sputtered globally to serve as gate electrode. It was found that sputtering resulted in a conformal coverage with sidewall thickness to be about half of the thickness of the flats. To define vertical gate, PMMA (polymethyl methacrylate) was spin coated on to the sample as masking layer while W was etched by SF_6 via RIE. This process was optimized so that the etching was mainly isotropic, ensuring complete W removal around the nanowire tip. The device gate length was the height of remaining W covering

the base of the nanowire, which was determined by the thickness of the mask layer. To investigate the impact of gate length, two concentrations of PMMA were used (in A2 and A4 solutions), which yielded an average gate length of 414 nm and 544 nm, respectively. A second W patterning step was then carried out to form the gate pads using standard photolithography and subsequent RIE. Another layer of 20 nm of Al_2O_3 was then deposited via ALD for electric isolation between gate electrode and future top electrode.

Access to nanowire for top contact was achieved by selectively expose and etch Al_2O_3 near nanowire tip, a process similar to the gate length definition described previously. Spin on glass was spin coated and cured at 300 °C for 45 min in N_2 environment. SOG was diluted to ensure its thickness only allowed vertical nanowires with sufficient height to stand out while everything else was properly covered. Wet etch of Al_2O_3 was carried out in H_3PO_4 stabilized at 36 °C. After DI water rinse and lithographically defining top electrode, 75 nm of Ni was deposited by angled evaporation following a short BHF dip to remove any remaining native oxide. Liftoff of Ni electrodes was followed by a rapid thermal process (RTP) at 320 °C for 2 min in forming gas (5% H_2 in N_2) to achieve ohmic contact. Finally, a pad opening step was performed via lithography and wet etching to allow access the buried gate electrodes. A schematic of the process flow is shown in Figure 33 while the configuration of the masks is given by Figure 34.

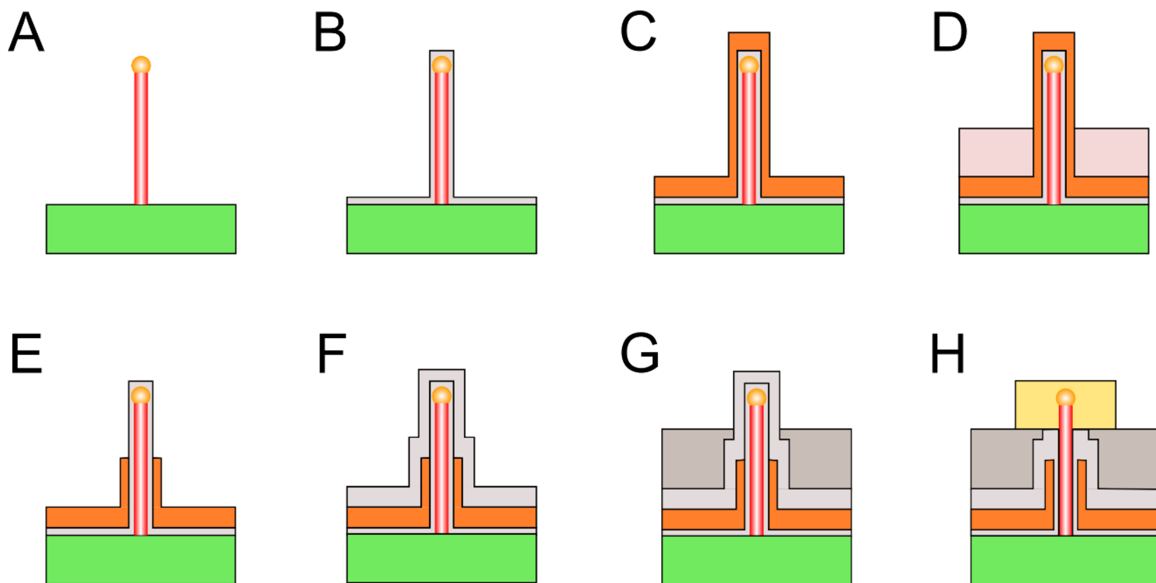

Figure 33. Major steps for the vertical nanowire junctionless transistor fabrication. (A) Vertical nanowire growth on a Si substrate. (B) Deposition of 10 nm Al_2O_3 as high-*k* dielectric via ALD. (C) Deposition of 50 nm of W as gate metal via sputtering. (D) Spin coating of PMMA layer as etching mask for W gate. (E) W gate formation and removal of PMMA. (F) Deposition of 20 nm Al_2O_3 as insulating layer between the gate and the top electrode. (G) Planarization with spin-on-glass. (H) Deposition of 75 nm Ni as the top electrode. Adapted with permission from [137]. Copyright 2015 American Chemistry Society.

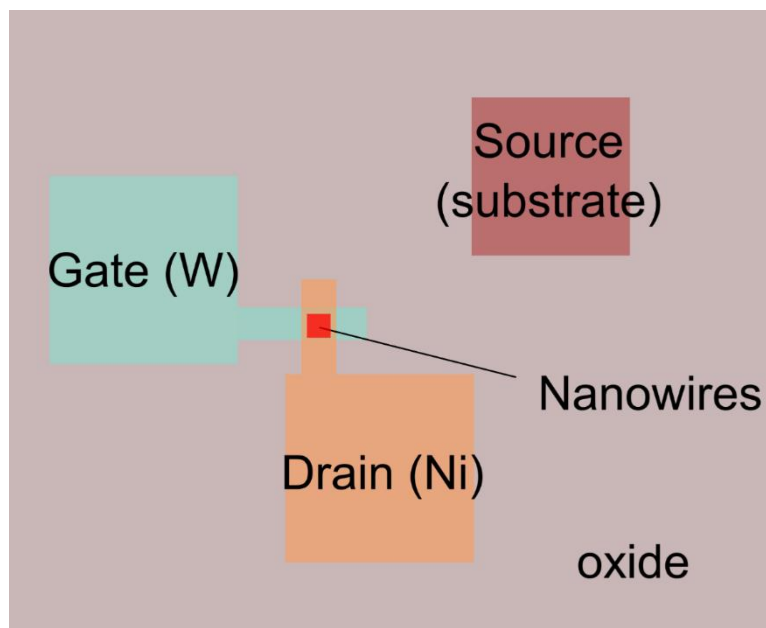

Figure 34. Schematic of the mask design for vertical transistors. The area where nanowires were preserved are marked with red square. The number of the nanowires in this area determines the number of parallel channels one transistor has.

In a complete device, heavily doped Si substrate served as the (global) source terminal while the top electrode was used as drain terminal. The number of vertical nanowires in each device, which determines the number of parallel channels in the device, can be controlled by tuning the original Au nanoparticle density and by controlling the active area size during the lithography step. In general, longer nanoparticle dispensing time leads to higher nanoparticle density and greater number of nanowires in the active area on average and higher device current. In this chapter, we focused on devices based on single nanowires. Figure 35A shows an SEM image taken after the W gate formation step, showing a single vertically standing nanowire after gate metal etch. A cross-sectional view of one finished device can be seen in Figure 35B, where the different layers were marked by different colors, highlighting the GAA structure, the junctionless design and vertical device integration. An up-slope feature was commonly observed in spin coated films near nanowires, and its height must also be considered as part of the film thickness during device design.

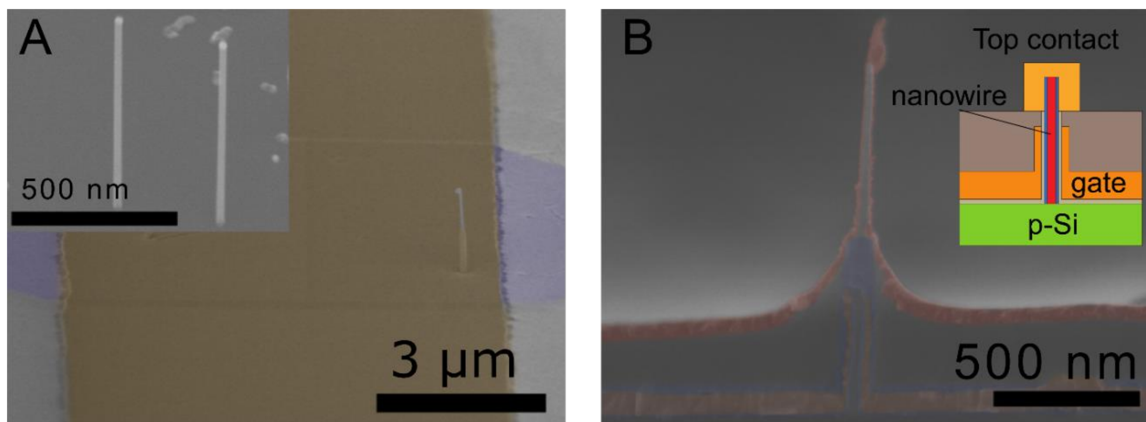

Figure 35. SEM images of vertical nanowire junctionless transistor. (A) 45 degree tilted SEM image of the active area of the vertical nanowire junctionless transistor after the formation of W gate electrode. This device contains only a single free-standing nanowires. Inset is a 45 degree tilted SEM image of the as grown vertical Ge nanowire on Si substrate. (B) Cross section SEM image of a finished vertical nanowire junctionless transistor. Different materials are highlighted with false color for clarity. Inset is a schematic of the device structure. Adapted with permission from [137]. Copyright 2015 American Chemistry Society.

5.3 Vertical nanowire junctionless transistor performance

5.3.1 Experimental characterization of nanowire junctionless transistors

The current-voltage (I-V) characteristics of the vertical Ge/Si core/shell nanowire junctionless transistors were measured using a Keithley 4200 semiconductor parameter analyzer. Figure 36 shows typical I_d-V_{ds} family curves and I_d-V_{gs} transfer curves of a device with gate length of 544 nm.

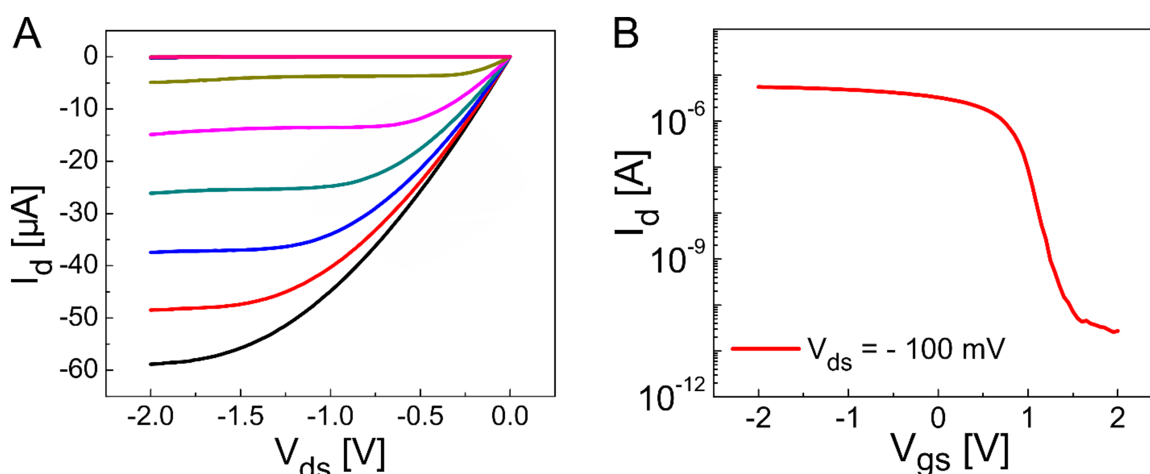

Figure 36. Measurement results of vertical nanowire junctionless transistor. (A) Typical output characteristics of a vertical nanowire junctionless transistor with 544 nm gate length. (B) Typical transfer characteristics of a vertical nanowire junctionless transistor with 544 nm gate length showing subthreshold swing of 125 mV/dec. Adapted with permission from [137]. Copyright 2015 American Chemistry Society.

As expected, the device showed a depletion mode (normally-ON) p-type transistor behavior with a threshold voltage of 0.95 V. The ON state current (normalized by nanowire circumference) was calculated to be 750 μA/μm at 2 V V_{dd}, higher than previously reported values for other vertical nanowire transistors based on Si, Ge and III-V materials, including both chemically-synthesized nanowires[7], [9], [138]–[142] and top-down nanofabricated devices[143], [144]. Such a high current level achieved at a moderate gate length (544 nm) is due to the high density hole gas formed in the Ge/Si core/shell structure.[6] Additionally, the device exhibited

excellent current saturation behavior at high V_{ds} (Figure 36A), indicating minimal short-channel effects due to the use of the GAA structure and the thin nanowire channel at moderate gate lengths. We note that I_{on} exceeding 2 mA/μm was reported for planar Ge/Si core/shell nanowire transistors with much shorter gate lengths (190 nm[126] and 100 nm[145]), suggesting that I_{on} of the vertical device may be improved further via gate length scaling.

The device exhibited a subthreshold slope (SS) of 125 mV/dec over 3 decades. Although this value is higher than the theoretical limit of 60 mV/dec at room temperature[61] and the record of 75 mV/dec for vertically orientated transistors[138], [143], it is comparable to typical values (85-120 mV/dec) reported for vertical nanowire transistors[9], [139], [141], [142], [144] and can be reduced via optimizing the nanowire/insulator interface during the processing steps. The low field hole mobility can be extracted using $\mu_{eff} = \frac{g_m L^2}{C_g V_{ds}}$, where the transconductance g_m was measured from the transfer curve shown in Figure 36B and the gate capacitance $C_g = \frac{2\pi\varepsilon_{ox}L}{\ln(1+t_{ox}/R)}$ was calculated using a cylindrical model. A mobility value of 282 cm^2/V·s was extracted for this device while the average mobility for all devices is 255 ± 92 cm^2/V·s. Carrier mobility in vertical transistor devices tends to have a very broad range. Depending on the channel material, mobility as high as 1170 cm^2/V·s was reported for InGaAs nanowire based devices[141] while 102 cm^2/V·s was reported for Si nanowire based devices[9].

5.3.2 Modeling nanowire junctionless transistors

To better understand the device performance, a numerical model based on junctionless transistor operation was developed. This model is based on fully depleted approximation with constant doping concentration and effective carrier mobility in Ge nanowires. Non-ideal effects such as series resistance, velocity saturation and mobility degradation were added after core model

is established. Then the simulation results will be compared against the experimental results. The details will be discussed below.

5.3.2.1 Ideal nanowire junctionless transistor model

First we consider whether quantum effects (*e.g.*, subbands) should be taken into account. Due the cylindrical geometry of the channel, the energies of the carriers (hole) can be approximated using an infinite circular well mode. The exact solution of the quantized energies from the Schrödinger's equation is given by the roots of the Bessel functions. The number of the subbands involved in transistor operation can be determined from the position of the Fermi levels at source and drain terminal.

Robinett plotted the solution to the subband energies in unit of $E = \hbar^2/2\mu R^2$ (where $\hbar$ is reduced Planck's constant, μ is the effective mass and R is the radius of the infinite well) in his previous work.[146] In our Ge nanowire device, $\mu = \left(m_{lh}^{*3/2} + m_{hh}^{*3/2}\right)^{2/3} = 0.29m_0$ where m_0 is the mass of a free electron.[83] Thus $E = 1.3meV$ can be calculated in a nanowire with diameter of 20 nm. Assuming the Fermi level in source terminal resides at the valence band edge, then at $V_{ds} = 500mV$, nearly 50 subbands will be contributing to overall current.[146] Exact number of the subbands will be even higher due to degeneracy. Thus we can safely neglect quantum effects for our device and follow the classic approach in modeling.

As shown in Figure 37, the vertical nanowire transistor is simplified as a heavily doped Ge channel with surrounding gate wrapped around and ohmic contact at both ends. Depending on the bias conditions, nanowire channel may operate in either accumulation, partial depletion or full depletion. Accumulation occurs when the applied gate voltage V_{gs} is lower than flat band voltage

V_{fb}, which results in a thin layer of accumulated holes on the nanowire periphery at the oxide/semiconductor interface.

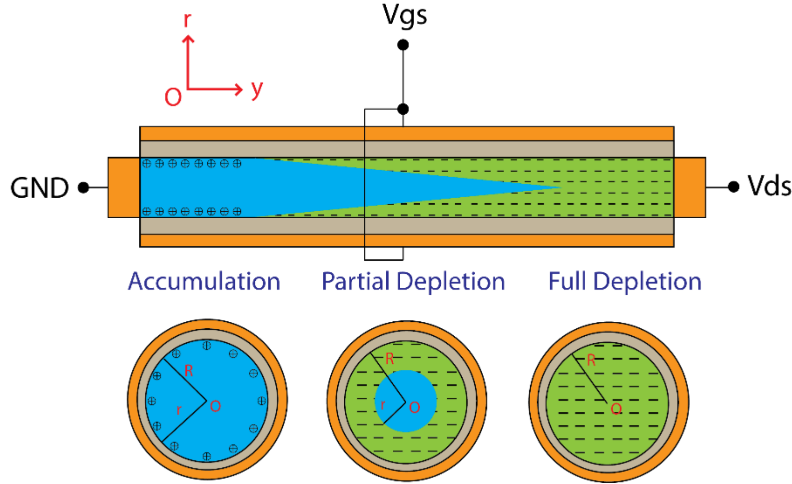

Figure 37. Schematic of the simplified device structure used in modeling. Three different operation regimes, accumulation, partial and full depletion, are shown. Adapted with permission from [137]. Copyright 2015 American Chemistry Society.

In the case of partial depletion, the radius of the remaining quasi-neutral region r_0 can be calculated using the following simplified Poisson's equation with full depletion approximation (FDA) under cylindrical coordinates:

$$\frac{1}{r}\frac{d}{dr}[r\frac{d\psi(r)}{dr}] = e\frac{N_A}{\varepsilon_s} \quad \textbf{(14)}$$

With the boundary conditions given by:

$$\psi(r_0) = 0 \quad \textbf{(15)}$$

$$\psi'(r_0) = 0 \quad \textbf{(16)}$$

$$\psi(R) = \psi_s \quad \textbf{(17)}$$

$$-\psi'(R) = E = \frac{1}{2\pi R}\frac{Q}{\varepsilon_s} \quad \textbf{(18)}$$

$$\psi_{ox} = -\frac{Q}{C_{ox}} \quad \textbf{(19)}$$

$$Q = -e\pi N_A (R^2 - r_0^2) \quad \textbf{(20)}$$

$$C_{ox} = \frac{2\pi\varepsilon_{ox}}{\ln(1 + \frac{t_{ox}}{R})} \quad \textbf{(21)}$$

$$V_{gs} - V_{fb} - \psi_{ox} - \psi_s = 0 \quad \textbf{(22)}$$

Where R and N_A are the radius and acceptor doping concentration of the nanowire channel, ε_{ox} and t_{ox} are the dielectric constant and thickness of the surrounding gate dielectric, C_{ox} is the gate capacitance per unit length, r_0 is the radius of the neutral region under gate voltage V_{gs}, Q is the total charge per unit length, ψ_s is surface potential and V_{fb} is the flatband voltage.

Through integrating Equation (14) twice, it is possible to obtain the following:

$$V_{gs} - V_{fb} - \frac{e\pi N_A}{C_{ox}}(R^2 - r_0^2) - \frac{eN_A}{4\varepsilon_s}\left[R^2 - r_0^2 - 2r_0^2 \ln\left(\frac{R}{r_0}\right)\right] = 0 \quad \textbf{(23)}$$

Where the only unknown variable r_0 can be solved numerically via standard Newton-Raphson method[147].

Full depletion occurs when $r_0 = 0$, *i.e.*, the whole channel is depleted. The gate voltage required to achieve full depletion can be calculated by substituting r_0 with *R* in the above equation, which gives:

$$V_{FD} = V_{fb} + \frac{e\pi N_A}{C_{ox}} R^2 + \frac{eN_A}{4\varepsilon_s} R^2 \quad \textbf{(24)}$$

The available mobile charge (carriers) in partial depletion regime is given by the total number of charges in the neutral region $Q_{PD} = e\pi N_A r_0^2$, while in the case of full depletion, carrier density is 0 under FDA.

We can simply extend this result to accumulation regime by setting $r_0 = R$ and add accumulation charge $-eC_{ox}(V_{gs} - V_{fb})$ to the total mobile charge, which yields:

$$Q_{ACC} = e\pi N_A R^2 - C_{ox}\left[V_{gs} - V_{fb}\right] \quad \textbf{(25)}$$

At $V_{ds} \neq 0$, V_{gs} is effectively modified by a channel potential V_{ch}, which takes the value of 0 at source terminal and V_{ds} at drain terminal, resulting in the following:

$$V_{gs}(y) = V_{gs} - V_{ch}(y) \quad \textbf{(26)}$$

Thus the total current can be computed by:

$$I_{ds} = \mu_{eff} Q(y) \frac{dV_{ch}}{dy} \quad \textbf{(27)}$$

$$I_{ds} = \frac{\mu_{eff}}{L} \int_0^{V_{ds}} Q(y) dV_{ch} \quad \textbf{(28)}$$

Where L is the gate length and μ_{eff} is the effective carrier mobility.

5.3.2.2 Secondary effects

In addition to the core model described above, secondary effects including velocity saturation, mobility degradation and series resistance were added in order to account for non-ideality and obtain more realistic results.

A constant series resistance R_s was added to the drain side (top electrode) to account for the ungated channel and contribution from other sources such as non-ideal metal/nanowire contact. R_s mainly affects the actual drain bias this device sees:

$$V'_{ds} = V_{ds} + R_s I_{ds} \quad \textbf{(29)}$$

Where V_{ds} is the drain to source voltage internally and $V_{ds}{}'$ is the external applied voltage.

In the velocity saturation model, the carrier velocity is given by[61]:

$$I_{ds} = \frac{\mu_{eff}}{L}\int_{0}^{V_{ds}} Q(y)dV_{ch} \tag{30}$$

Where E_C is the critical electric field and $n = 1$ is for holes.

Thus the current is modified by the following relation:

$$I'_{ds} = \frac{I_{ds}}{1 + \mu_{eff}V_{Ds}/v_{sat}L} \tag{31}$$

In the mobility degradation model, effective mobility is reduced due to the transverse electric field[61]:

$$\mu'_{eff} = \frac{\mu_{eff}}{1 + \left(\frac{E_{eff}}{E_{critical}}\right)^{n}} \tag{32}$$

Where $E_{critical}$ and n are fitting parameter and the effective transverse field is computed as follows:

$$E_{eff} = \frac{\int \frac{dQ}{dV_{ch}} E_{transverse} dV_{ch}}{\int \frac{dQ}{dV_{ch}} dV_{ch}} \tag{33}$$

In fact, only carriers induced by surface accumulation experience non-zero transverse field, so mobility degradation will not affect the current unless applied voltage is sufficiently high.

5.3.2.3 Simulation results

It is imperative to first validate the results from the simplified equations. Figure 38 plots the total mobile charge density obtained from solving the full Poisson's equation[83] and the simplified model (under FDA) across a wide range of gate voltages. Excellent agreement was

obtained, justifying the use of the simplified model. However, it is important to note that while good accuracy can be achieved when device is in ON state, it might be problematic to apply this model to devices operating in subthreshold regime where full Poisson's equation must be used to solve for potential. Nevertheless, it can still prove itself a useful tool towards better understanding of the junctionless transistors as long as switching characteristics is not the focus.

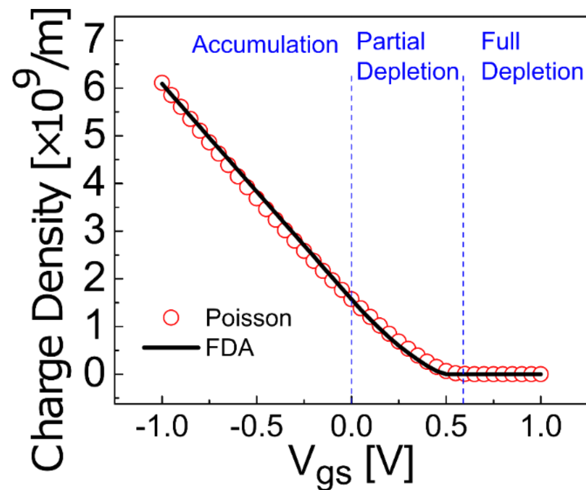

Figure 38. Validation of the simplified equation using total charge density. Comparison of total mobile charge density per unit length from solution to Poisson's equation (open circle) and simplified Poisson's equation under full depletion approximation (solid line). Adapted with permission from [137]. Copyright 2015 American Chemistry Society.

Figure 39 shows the experimentally-obtained I_d-V_{ds} family curves along with simulation results for devices with two different gate lengths (414 nm and 544 nm, respectively) using the model discussed above. It is worth noting that both figures were generated with the same set of parameter except gate length (determined by SEM image), mobility (extracted from transfer characteristics), series resistance R_s and flatband voltage V_{fb}. All parameters were determined by known physical constants or derived from real device dimensions (*e.g.*, gate capacitance) except R_s and V_{fb}, which were treated as fitting parameters (all parameters values are listed in **Error! Reference source not found.**). In general, the simulation results match well with the experimental data, suggesting that the model has captured the key elements of device operation and proving that

the devices indeed work as intended junctionless transistors with excellent electrostatic control and extrinsic effects such as non-linear series resistance due to Schottky metal/nanowire contact were not dominant factors of the device operation.

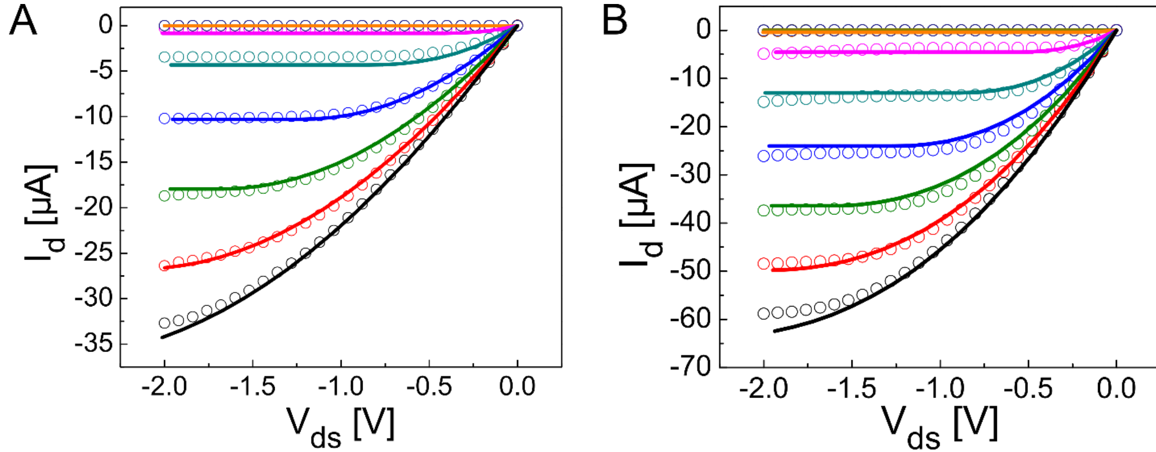

Figure 39. Comparison of measurement results with simulation. (A) Fitting to measurement data of devices with 414 nm gate length. (B) Fitting to measurement data of devices with 544 nm gate length. Adapted with permission from [137]. Copyright 2015 American Chemistry Society.

Symbol	Unit	Description	Case A	Case B
d	nm	diameter	25	25
C_{ox}	pf/m	gate capacitance	852	852
L	nm	gate length	414	544
V_{fb}	V	flatband voltage	0.27	0.55
N_A	/cm^3	effective doping	5×10^{18}	5×10^{18}
μ_{eff}	cm^2/Vs	effective mobility	94	282
v_{sat}	cm/s	saturation velocity	6.3×10^4	6.3×10^4
$E_{critical}$	V/cm	critical field	7×10^6	7×10^6
R_s	kΩ	series resistance	15	7

Table 2. Parameters used in the simulation of junctionless transistors. Adapted with permission from [137]. Copyright 2015 American Chemistry Society.

5.3.3 Gate length modulation and its impact

One advantage of the vertical transistor configuration is that the transistor gate length is no longer determined by lithography, but rather by the thickness of the masking layer which in principle can be readily changed and controlled at the atomic level without having to re-design expensive masks. In our process, PMMA was used as the masking layer during the W etch and gate formation process. To test the capability of gate length control, several PMMA masking layer deposition conditions were carried out and a positive correlation was clearly found between the remaining W film thickness (corresponding to the gate length of the vertical transistor) and the masking film thickness, as shown in Figure 40.

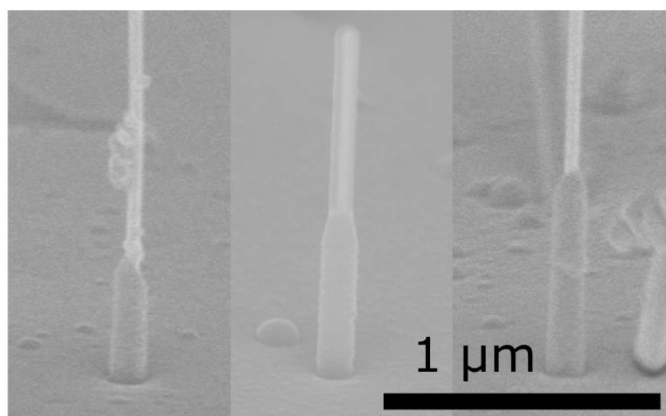

Figure 40. Controlling gate length by tuning the thickness of masking layer. 75 degree tilted SEM image showing the height of remaining W on nanowire using different masking layers. PMMA A2/A4/A6 were used as masking layer for nanowire from left to right. Adapted with permission from [137]. Copyright 2015 American Chemistry Society.

SEM images of devices after the W gate etching step using different PMMA solutions (leading to different PMMA masking layer thickness) clearly show that the W gate length is controlled by the masking layer thickness, with thicker PMMA masking layer (produced by resists with higher PMMA concentration, *e.g.* PMMA A6 *vs*. PMMA A2) leading to longer gate length. The average gate length produced via this method was 414 ± 69 nm (A2), 544 ± 36 nm (A4) and 772 ± 24 nm (A6), as determined from SEM measurements. (Also summarized in Table 3.)

Additional parameters such as the spinning speed and time during PMMA deposition can also be used to control the mask layer thickness and achieve desired gate length tuning without relying on aggressive lithography steps. To further fine tune the masking layer thickness (and consequently the device gate length), an additional etch back step such as oxygen plasma etch can be performed after the film deposition to obtain the desired masking layer thickness. 100 nm gate length has been demonstrated using this approach.[139] Alternatively, the gate length can be controlled directly during gate metal deposition using an anisotropic deposition method (*e.g.,* evaporation) and gate length down to 14 nm has been demonstrated.[144]\

PMMA used	A2	A4	A6
Average L_g (nm)	414	544	772
Standard deviation (nm)	69	36	24

Table 3. Relation between PMMA concentration and resulting gate length.

The statistical distribution of device performance for devices with different gate lengths are shown in Figure 41. Several interesting observations can be made. First, both cases exhibited a dominant peak current (33 ± 6 μA for case A with 414 nm gate length, and 58 ± 12 μA for case B with 544 nm gate length) in the histogram, with a large number of devices aggregated around the peak. Assuming each nanowire was grown independently and had the same probability to land in one of the active device regions, the chances for contacting n nanowires in one device can be denoted as Y^n where Y is the chance of obtaining a single nanowire in the device. Since the nanowire density was deliberately kept low during Au nanoparticle dispensing, the average number of nanowires in an active area was below 1, *i.e.* $Y < 1$.Thus the probability of contacting multiple nanowires in one device will be lowered further due to the power law dependence on nanowire number. As a result, the dominant peak value in the distribution plot can be regarded as

the typical single nanowire current. In both cases, fitting the distribution histogram with a Gaussian distribution resulted in a relatively small standard deviation (~ 20 % of the average I_{on}), indicating good uniformity in nanowire properties and reliability of the fabrication process. The small deviations from the peak (average) value can be explained by small variations in series resistance, threshold voltage (affected by effective doping level), nanowire diameters and gate lengths. Besides the dominate peak, a few isolated occurrences can also be found at much higher current levels, probably originating from devices containing multiple-nanowires.

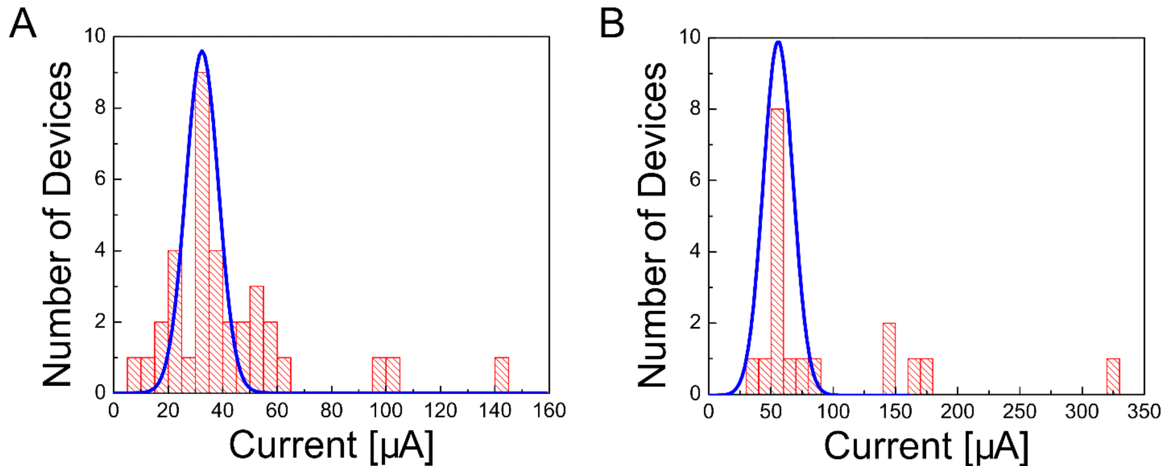

Figure 41. Variation of device characteristics. (A) Histogram of current difference of devices with 414 nm gate length between ON and OFF states. Solid line is Gaussian distribution with mean of 33 μA and standard deviation of 6 μA. (B) Histogram of current difference of devices with 544 nm gate length between ON and OFF state. Solid line is Gaussian distribution with mean of 58 μA and standard deviation of 12 μA. Adapted with permission from [137]. Copyright 2015 American Chemistry Society.

Comparing Figure 41 A-B, it can be seen that the peak current level is considerably lower for the $L_g = 414\ nm$ device. This is somewhat counterintuitive as in MOSFET devices scaling towards shorter gate lengths generally yields higher I_{on} since the on-state resistance is reduced. However, in our design, the total channel length (distance from the bottom source contact to the top drain contact) was unchanged and did not scale with the gate length.

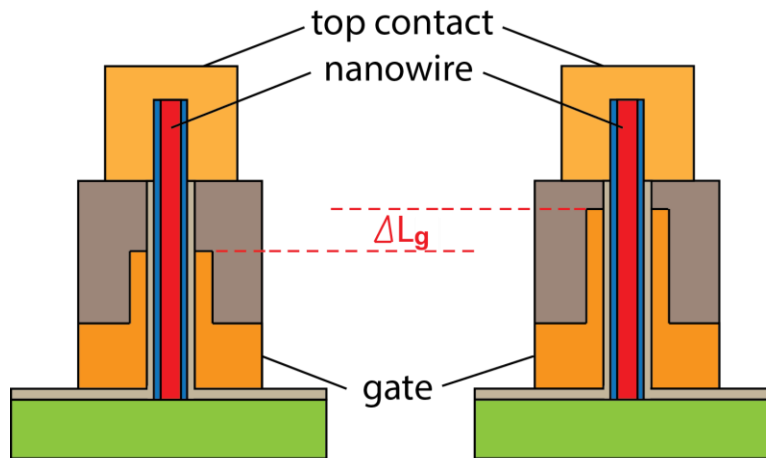

Figure 42. Schematic of devices with the same total height but different gate lengths. Adapted with permission from [137]. Copyright 2015 American Chemistry Society.

As shown in Figure 42, reduction of the gate length leads to an increase in lengths of the ungated region, and in turn leads to an increase in series resistance. The effect of the series resistance is more pronounced in the ON state, where most of the device resistance originates from the ungated regions. As a result, the shorter gate-length device will actually have a higher ON state resistance than the longer gate-length device due to the longer ungated region and consequently lower on-current. This result is a consequence of the junctionless design where the concept of self-aligned gate structures is not applicable, although scaling of the ungated regions along with gate length scaling in future device optimizations should result in the expected increase in ON-current. The effect of the ungated region was also verified in the model (Figure 39 and Table 2**Error! Reference source not found.**), where a larger series resistance (15 kΩ *vs*. 7 kΩ) was indeed found to exist in devices with 414 nm gate length. The difference in the series resistance values in the two cases can also be quantitatively explained by the different lengths of the ungated regions. From the resistivity of the Ge nanowire estimated from the doping concentration used in the model (3.8 mΩ·cm at 5×10^{18} /cm^3)[148], a difference in series resistance of ~10 kΩ was expected from the different lengths of the ungated region in the two cases. This estimated value agrees well with the

parameters used in our model and supports the hypothesis that the current discrepancy can be attributed to the differences of the gate length in the devices.

5.4 All vertical nanowire junctionless transistor inverter

The use of nanowires in the vertical transistor structure also allows additional freedom in the circuit design. For example, in an all-PMOS logic (inset in Figure 43), an inverter consists of a driver transistor T_1 functioning as an active switch and a load transistor T_2 acting as a resistor. The output high V_H is determined by the voltage dividing effect between the on-state resistances of T_1 and T_2 such that $V_H = V_{dd}\frac{R_{T2}}{R_{T1}+R_{T2}}$. As a result, to achieve rail-to-rail operation, it requires $R_{T2} \gg R_{T1}$. Usually this condition is satisfied by designing transistors with very different geometries (*i.e.,* T_1 having a much larger $\frac{W}{L}$ than T_2) which increases design complexity and limits the minimal size of such logic gates. In our devices, however, the ON state current is not determined by the width of gate electrodes, but rather by the number of nanowires inside the active region. As a result, optimized circuit performance can be achieved by optimizing the number of nanowires used in different devices, while maintaining uniform transistor geometry design.

This concept was tested in a PMOS inverter based on the vertical nanowire junctionless transistors with 414 nm gate length. The inverter schematic and bias conditions are shown in Figure 43A. The input voltage V_{in} was fed to the gate of T_1 while the output voltage V_{out} was read out from the drain of T_1 (source of T_2). Two different driver transistors were chosen and their output characteristics were plotted in Figure 43B. While both driver transistors exhibited similar I_{off}, their $I_{on}'s$ differed by almost 3 times. One of them (Device A, blue lines) exhibited I_{on} of 33 μA, consistent with the typical value for device with a single nanowire at this gate length, and the other (Device B, red lines) exhibited I_{on} of 105 μA and was thus likely formed by 3 nanowires.

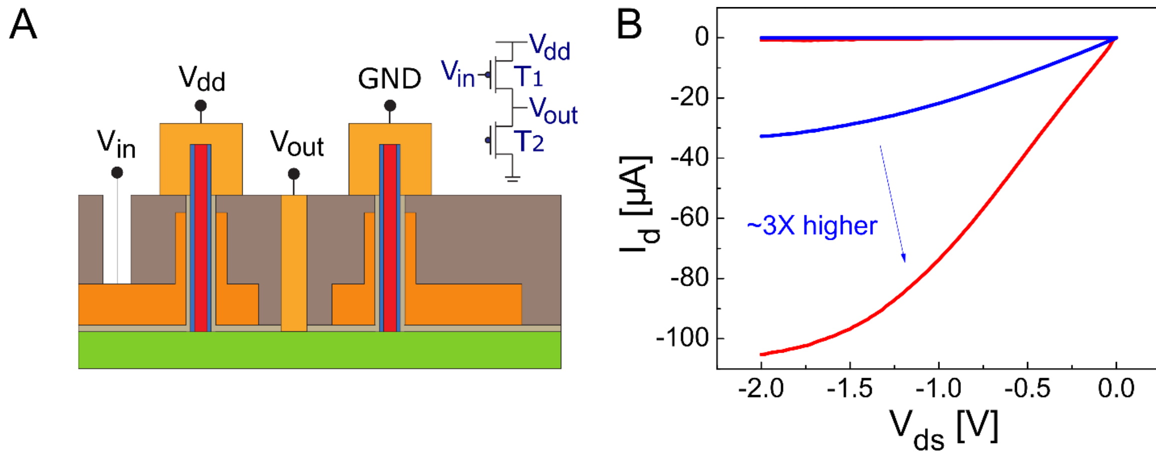

Figure 43. Inverter consists of two vertical nanowire junctionless transistors. (A) Schematic of the PMOS inverter with a common bottom contact shared by its two transistors. Inset: circuit diagram of the inverter. (B) Comparison of the output characteristics between Device A (blue lines, most likely based on a single nanowire) and Device B (red lines, most likely based on 3 nanowires) in ON (V_{gs} = -2 V) and OFF (V_{gs} = 2 V) states. Adapted with permission from [137]. Copyright 2015 American Chemistry Society.

The voltage transfer characteristics (VTC) of two inverters composed of these driver transistors and the same load transistor are shown in Figure 44. During measurements V_{dd} was set to 2 V while V_{in} was swept from 0 to 3.5 V. The higher value of V_{in} required in the measurement is due to the positive threshold voltage of the driver transistor although it is possible to offset the input waveform to obtain a 2 V window (bounded by the dashed lines in Figure 44) such that the input and output signals have the same peak-to-peak amplitude. From the VTC measurement, it was evident that both inverters function correctly although the inverter with a more conducting driver transistor (Device B, Figure 44B) was able to achieve better rail-to-rail operation (0-1.94 V) than the one with a less conducting driver transistor (0-1.83 V, Device A, Figure 44A). Additionally, the inverter in Figure 44B based on Device B also exhibits a much larger gain (11.7 *vs*. 4.4), supporting the idea that better matching can be achieved by controlling nanowire numbers in the vertical nanowire transistor circuits.

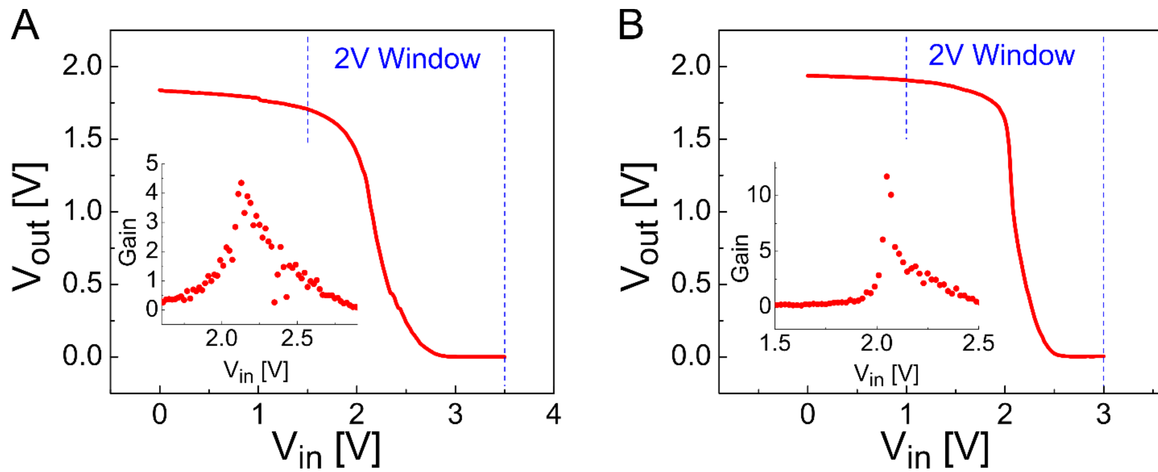

Figure 44. Voltage transfer characteristics of the inverter. (A) VTC of an inverter using Device A as the driver. Inset: inverter gain *vs.* input voltage. (B) VTC of an inverter using Device B as the driver. Inset: inverter gain *vs.* input voltage. The dashed lines in (A)-(B) highlight the 2 V operation window of the inverters. Adapted with permission from [137]. Copyright 2015 American Chemistry Society.

Finally, the transient behavior of the inverter logic was studied. The output waveform using a train of 1 ms pulses as input was plotted in Figure 45. Both input and output waveforms were read by Oscilloscope (TDS3000B, Tektronix) while the input signal was generated by arbitrary function generator (AFG3101, Tektronix). The output high of the inverter was slightly degraded, probably due to the finite input impedance (1 MΩ) of the oscilloscope used, while output low still remained near zero. The inverter devices tested could respond to 500 Hz input signals with reasonable output waveforms, which is far below the predicted capability of nanowire transistor[145]. We would like to note that the operation frequency was mainly limited by unoptimized device design. More specifically, the large gate to drain capacitance C_{gd} at the output node contributed a long RC delay. With better design to reduce the parasitic capacitance and device scaling, better RF characteristics could be achieved.

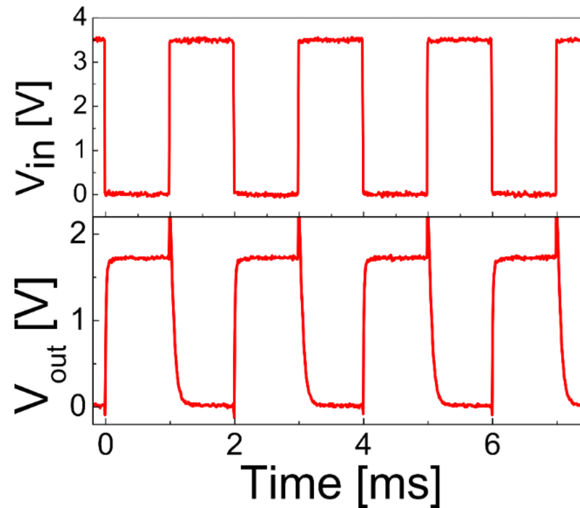

Figure 45. Transient behavior of the inverter circuit at frequency of 500 Hz.

5.5 Summary

In summary, we demonstrated the fabrication and characterization of single nanowire-based, vertical, GAA junctionless transistors epitaxially integrated on Si substrates. Excellent output characteristics with very good SCE suppression were obtained. Different gate lengths were achieved using a simple method of controlling the thickness of the etch mask film. A numerical junctionless transistor model was developed to analyze the experimental data and good agreements were obtained using known physical parameters. Statistical analysis of the devices indicated good uniformity and single-nanowire operation. An all vertical nanowire inverter was demonstrated using two nanowire junctionless transistors on the same chip and optimized by selecting high conductance driver transistors with multiple nanowire channels, with inverter gain > 10 and near rail-to-rail operation. Pulse measurement showed that the inverter can respond up to 500 Hz, which can be further improved by reducing C_{gd} and other parasitic capacitors. Such vertical Ge/Si core/shell nanowire junctionless transistors may be an integral part in future low cost, high density, high performance electronics based on hybrid-integrated circuits.

Chapter 6

Tunnel transistor based on vertical Ge/Si core/shell nanowires

6.1 Introduction

In chapter 1, we briefly touched upon tunnel field effect transistor (tunnel transistor, or TFET), which can potentially beat 60 mV/dec thermionic limit ($ln10kT/e$) and help reduce the devices' static power consumption. TFET has become an active research topic in the semiconductor industry as a path towards "green electronics". In this chapter, we discuss our attempts of fabricating Ge-based TFETs on Si substrates based on vertically grown Ge/Si core/shell nanowires.

As shown in Figure 46, current flow in transistors is controlled via the modulation of carrier density moving through the channel region due to the gate voltage. In a MOSFET, carriers with sufficient energy can overcome the source/channel junction barrier and be swept away by the longitudinal electric field in the channel. Due to the tail in the Boltzmann distribution, there is always a portion of high energy carriers that can overcome the barrier, resulting in a finite subthreshold slope (SS) and non-zero I_{off} floor. On the other hand, in a TFET, the carriers that enter the channel will first travel *though* the source/channel barrier via band to band tunneling (BTBT). Since the onset of this tunneling process requires one occupied state on one side and one unoccupied state with equivalent energy on the other side, it inherently prohibits carriers transiting if conduction/valence bands separated by the barrier have no overlap. As a result, switching off in

TFET can be both complete and sub-thermionic. For this reason, TFET is particularly attractive in application that requires low power consumption since lowering SS suppresses I_{off} and standby power, $I_{off} \sim I_{on} \exp(-V_{th}/SS)$. TFET becomes even more advantageous when device temperature elevates (*e.g.,* due to Joule heating) as tunneling process is generally insensitive to temperature change while MOSFET degrades as $SS \propto T$. Effectively, reducing SS in transistors is equivalent to driving them at a lower temperature without the need to actually cool them down.

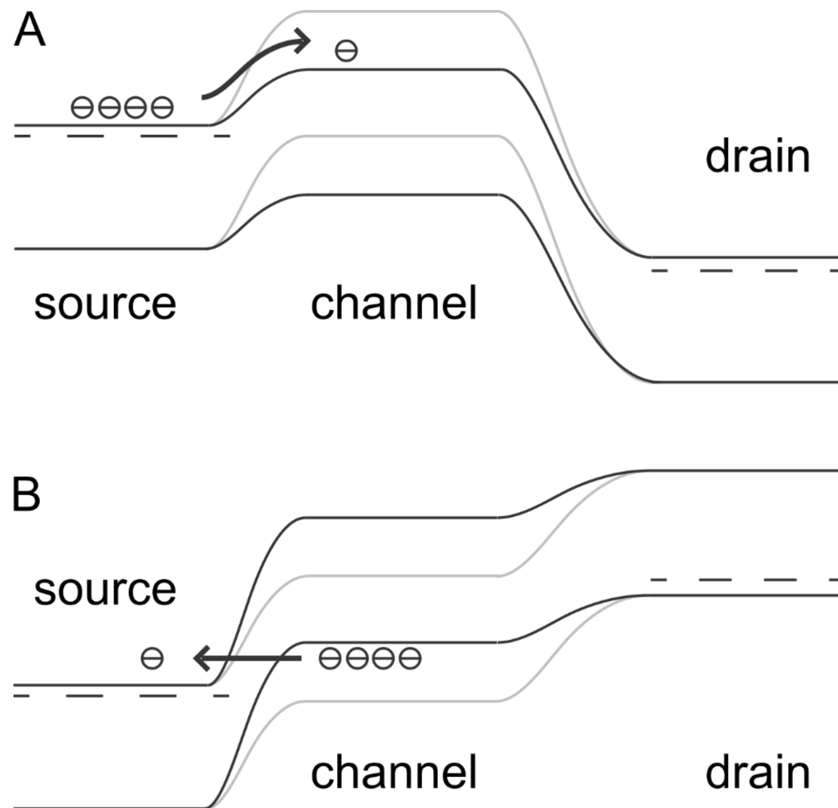

Figure 46. Comparison of the operation principles between MOSFET and TFET. (A) Schematic of carrier motion in MOSFET at ON (black) and OFF (grey) states. (B) Schematic of carrier motion in TFET at ON (black) and OFF (grey) states.

There have been a number of studies that demonstrated sub-60 mV/dec TFET in recent years with materials including Si, Ge, carbon nanotube, *etc*. [65]–[74] However, for TFETs to truly replace MOSFETs as the standard low power component in large scale integrated circuits, a number of issues have to be addressed. First, while a TFET has potentially lower SS, the SS

typically degrades as current starts to increase. In other words, a TFET may have sub-60 mV/dec at very low current, but above-60 mV/dec over the entire ON/OFF transition, if not designed properly. Second, being an indirect bandgap material, Si has limited BTBT probability due to the need for an additional phonon to satisfy momentum conservation. As a result, Si based TFETs usually suffer from low I_{on} and reduced performance. For this reason, other materials are being actively investigated, including Ge[67]–[69], III-V compounds[72], [73] and carbon nanotubes[65]. The latter two benefit from their direct band gap hence improved tunneling probability, but lack the capability of mass manufacturing and integration with Si. On the contrary, Ge can be used in conjunction with Si relatively ease. In addition, it has much smaller band gap (indirect band gap of 0.66 eV and direct band gap of 0.8 eV) compared to Si, which is promising for TFET with high I_{on}.

Figure 47. Comparison of published TFET drain current density *vs*. gate voltage. Experimental demonstration of both p-type (left) and n-type (right) transistors are included. Adapted from [149]. © 2014 IEEE.

Figure 47 compares the performance of recently reported TFETs to FinFET-type CMOS Si MOSFETs.[149] It clearly shows that while some TFETs demonstrated higher-than-CMOS I_{on} and some TFETs showed sub-thermionic SS, there is no working TFET that can achieve both high Ion and sub-thermionic SS at the same time. Pathfinding for optimal material and device design is still largely work in progress in both academia and industry. It is worth noting that relatively fewer reports were focused on p-type TFET than n-type ones.

In chapter 3, we showed that the VLS grown Ge/Si heterojunction is of high quality and has a very narrow transition width. Junctions with abrupt sharpness can enhance the electrical field across the junction, thus reducing barrier width and increase tunneling probability.[86] Due to the type II band alignment between Ge/Si, this heterojunction could potentially offer even higher tunnel current than homogeneous Ge devices thanks to the reduced barrier height. In chapter 4, we showed that Esaki tunnel diodes can be successfully fabricated based on vertical Ge/Si core/shell nanowire and room temperature NDR as well as high tunneling current density can be obtained. Combined with the fabrication process we developed in chapter 5 for vertical junctionless nanowire transistors, we now have a suitable material system (Ge/Si heterojunction) and good device structure (nanoscale channel with surrounding gate) to probe the potential of Ge nanowires in TFET applications. In this chapter, TFET based on nanowire channel will be studied theoretically and experimentally. We will first focus on developing TFET models, then present some preliminary measurement results.

6.2 Tunnel transistor simulation

Unlike MOSFETs, TFETs do not have current expression with a closed form. Due to its quantum mechanical nature, TFET operation is difficult to describe in simple equations without incurring significant approximations. The lack of device models that are easily understandable yet

physically correct also hampers the development of TFETs, more specifically, in circuit design that involves TFETs as active components. Simulations of TFETs were usually carried out numerically, either through commercial device simulators[86], [150]–[154] or using a fully atomistic approach[155], [156]. Both methods can be very compute intensive, thus are not suitable for applications on a larger scale. For this reason, a simpler current expression that can capture the key characteristics of TFET operation becomes very useful and desirable.

6.2.1 Overview of existing analytical TFET models

There are many attempts at obtaining a semi-analytical, or compact models for TFETs in the literature.[69], [86], [153], [157]–[160] The key in modeling TFET is to find a proper expression for tunneling probability. It is generally accepted that Wentzel–Kramers–Brillouin (WKB) approximation can be used to estimate the tunneling probability for an electron to tunnel through the source/channel barrier.[83] Depending on the shape of the barrier assumed, WKB theory yields different results. For example, if triangular barrier is assumed, the tunneling probability can be approximated as:

$$T = \exp(-\frac{4\sqrt{2m_t}E_g^{3/2}}{3e\hbar F}) \quad \textbf{(34)}$$

Where m_t is the effective mass for tunneling and F is the amplitude of the electric field along the tunneling direction. If the barrier is assumed to be parabolic, the tunneling probability is given by Equation (35):[83]

$$T = \exp(-\frac{\pi\sqrt{m_t}E_g^{\frac{3}{2}}}{2\sqrt{2}e\hbar F})\exp(-\frac{2E_\perp}{\overline{E_\perp}}) \quad \textbf{(35)}$$

Where $E_\perp$ is the transverse energy (electron energy perpendicular to tunneling direction) of the electron and $\overline{E_\perp} = \frac{4\sqrt{2}e\hbar F}{3\pi\sqrt{m_t E_g}}$.

Another method is to use the Kane's model[161] and treat the tunneling process as additional carrier generation at the source/channel junction with rate given by Equation (36):

$$G = A\frac{E^2}{\sqrt{E_g}}exp(-\frac{BE_g^{3/2}}{E}) \quad \textbf{(36)}$$

Where E is the electric field along the tunnel junction and $A(B)$ are parameters associated with materials and device structures.

It is important to note that the Kane's model is derived for tunneling process in a direct band gap semiconductor under uniform electric field, which is typically not the case in real TFETs. Generalization to more realistic conditions can be achieved by tuning the values of the fitting parameters. Another pitfall with Kane's model is its non-zero and non-directional tunneling probability regardless of bias conditions. According to Equation (36), tunneling can occur even under band alignment that normally prohibits band to band tunneling, and non-zero tunneling current would be calculated even if V_{ds} is set to zero.

By approximating the electrical field F as $F = (E_g + \Delta\Phi)/\lambda$, where λ is the natural length[62] (characteristic length depending on device geometry and gate structure) and $\Delta\Phi = -q(V_{gs} + V_{th})$ is the energetic difference between the conduction band and the valence band in the channel, Björk *et al.* was able to arrive at Equation (37) to calculate current in a Si nanowire p-i-n tunnel transistor.[157]

$$I_d = \frac{16e\sqrt{m_t}}{3\hbar^2}\left[-e\left(V_{gs}+V_{th}\right)\right]^{\frac{3}{2}} exp\left\{-\frac{4\lambda\sqrt{2m_t}E_g^{\frac{3}{2}}}{3\hbar\left[E_g - e\left(V_{gs}+V_{th}\right)\right]}\right\} \quad \textbf{(37)}$$

A similar expression (Equation (38)) was used by Kim *et al.* where the electric field E_s was approximated as the transverse field at the source/channel junction at the threshold condition.[69] Both analytical expressions used an approximated electric field in the current calculation, and are applicable only in the saturation regime where V_{ds} is sufficiently high.

$$I_d = AE_s\, exp\left[-\frac{\pi m^{\frac{1}{2}}E_g^{\frac{3}{2}}}{2\sqrt{2}q\hbar E_s}\right] = AE_s\, exp(-\frac{B}{E_s}) \quad \textbf{(38)}$$

A more accurate representation of the electric field can be obtained through numerical solver. Zhang *et al.* extracted the electric field profile from SYNOPSYS TCAD and then used the maximum electric field ξ in the following equation to calculate the tunnel current density:[86]

$$J = \frac{q^3\xi V_R}{4\pi^2\hbar^2}\sqrt{\frac{m}{2E_g}}\, exp\left(-\frac{4\sqrt{2m}E_g^{\frac{3}{2}}}{3q\hbar\xi}\right) \quad \textbf{(39)}$$

Where the reverse bias $V_R(i.e., V_{ds})$ was added to the prefactor to circumvent the issues with non-zero current at equilibrium.

Similar work was reported by Bardon *et al.*, in which the potential profile was approximated analytically and total current was obtained by integrating the generation rate in the channel region numerically according to the Kane's model:[158]

$$I_d = e\int G_{btb}dV \quad \textbf{(40)}$$

Where G_{btb} is given by Equation (36) and V includes the whole volume of the channel.

6.2.2 Modeling tunnel transistors

As discussed previously, while TFET is an important candidate towards future low power electronics, there is still no universally accepted model for current computation. The aforementioned models all share similar forms, *i.e.*, the exponential dependence on the electrical field and the band gap, while differing in other aspects. The purpose of this section is to derive a (semi) analytical TFET model that originates from fundamental physical processes, yet is simple enough to be evaluated quickly. More specifically, this model should be able to capture the key features characteristics in TFET operations and include some fitting parameters to allow benchmarking against experimental results.

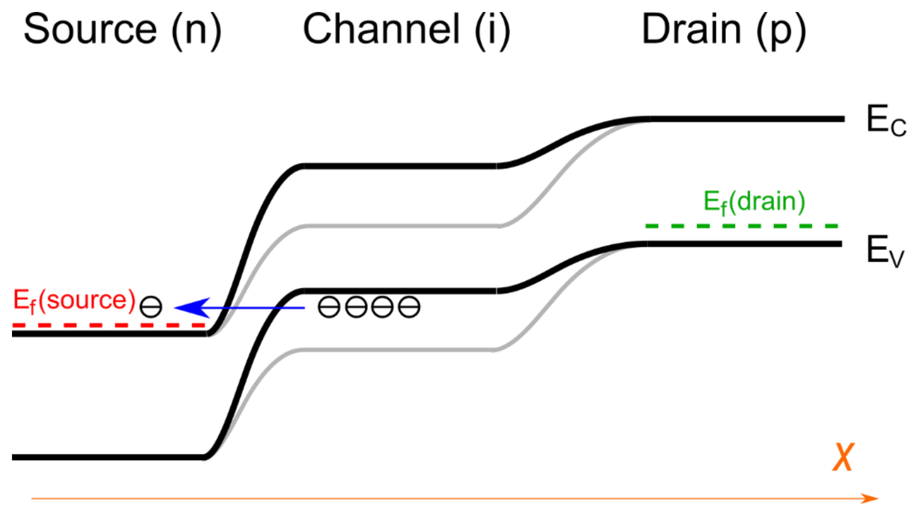

Figure 48. Schematic of the p-type TFET used in modeling. This transistor consists of n-type doped source, intrinsic channel and p-type doped drain.

The band diagram of a p-type TFET chosen for the modeling study is illustrated in Figure 48. This device consists of source (n-type), channel (intrinsic) and drain (p-type). At equilibrium, the position of the band edges in different regions can be calculated using Joyce-Dixon approximation[133] (for better accuracy since degenerate doping is likely) as the following:

$$E_{fs} = E_{fd} = E_f \quad \textbf{(41)}$$

$$E_f - E_C^s = kT[\ln\left(\frac{N_d}{N_C}\right) + \frac{N_d}{\sqrt{8}N_C}] \quad \textbf{(42)}$$

$$E_V^{ch} - E_f = kT[\ln\left(\frac{N_a}{N_V}\right) + \frac{N_a}{\sqrt{8}N_V}] \quad \textbf{(43)}$$

$$E_V^{ch} - E_C^s = kT[\ln\left(\frac{N_d}{N_C}\right) + \frac{N_d}{\sqrt{8}N_C} + \ln\left(\frac{N_a}{N_V}\right) + \frac{N_a}{\sqrt{8}N_V}] \quad \textbf{(44)}$$

Where $N_d(N_a)$ is the donor (acceptor) concentration in n(p) type semiconductor, and $N_C(N_V)$ is the effective conduction (valence) band density of states.

Under gate voltage $V_{gs} < 0$, a negative surface potential $\psi_s < 0$ is induced to raise the band energies in the channel region, which modifies Equation (44) to the following:

$$E_V^{ch} - E_C^s = kT[\ln\left(\frac{N_d}{N_C}\right) + \frac{N_d}{\sqrt{8}N_C} + \ln\left(\frac{N_a}{N_V}\right) + \frac{N_a}{\sqrt{8}N_V}] - e\psi_s \quad \textbf{(45)}$$

At $V_{ds} \neq 0$, we can assume that the majority of the longitudinal voltage drop falls on the source/channel junction so that the Fermi level at drain E_{fd} can be used to describe the electron population in the channel. Essentially, this assumption states that current is solely governed by the number of carriers tunneling through the source/channel junction and backscattering in the channel is ineffective. In this case, V_{ds} simply causes a difference between Fermi levels in source and drain (channel), *i.e.*, $E_{fs} = E_{fd} - eV_{ds}$.

6.2.2.1 Current model for 2-D devices

For a 2-D tunnel transistor (such as SOI with very thin channel), the number of incident carriers per unit *width* per unit time (along the +*x* axis in Figure 48) assuming isotropic effective mass m_t for both conduction/valence band is given by:[162], [163]

$$dj_{xi} = \frac{1}{2} \times 2 \times \frac{dk_x dk_y}{4\pi^2} \frac{\hbar k_x}{m_t} ef(E_{fs}) \quad \textbf{(46)}$$

Where $\frac{1}{2}$ in the prefactor represents the portion of carriers moving towards right and 2 comes from spin degeneracy.

The total current due to tunneling can then be calculated as the following using the difference between the number of carriers moving towards +*x* and -*x* directions:

$$\begin{aligned} I_d &= W \iint \frac{dk_x dk_y}{4\pi^2} \frac{\hbar k_x}{m_t} eT(E)\{f(E_{fs})[1 - f(F_{fd})] - f(E_{fd})[1 - f(F_{fs})]\} \\ &= W \iint \frac{dk_x dk_y}{4\pi^2} \frac{\hbar k_x}{m_t} eT(E)[f(E_{fs}) - f(F_{fd})] \end{aligned} \quad \textbf{(47)}$$

Where W is the channel width, $f(E)$ is the Fermi distribution function and $T(E)$ is the tunneling probability through the source/channel barrier. By adopting a simple yet effective approximation assuming a triangular tunnel barrier, Equation (34) can be used to calculate the tunneling probability $T(E)$.

To obtain an analytical expression for Equation (47), several additional approximations are required. First, the Fermi distribution function $f(E)$ is substituted with a step function to carry out the integration. Second, the electric field F in Equation (34) is estimated using the natural length so that $F \approx \frac{E_g + E_V^{ch} - E_C^s}{e\lambda}$, where $\lambda = \sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}} t_{Si} t_{ox}}$ is the natural length for SOI structure.[62], [157] Further simplifications lead to $E_V^{ch} - E_C^s = -e(V_{gs} + V_{th})$ and $F = \frac{E_g - e(V_{gs} + V_{th})}{e\lambda}$, assuming good gate coupling in a fully depleted channel.[157] Lastly, without loss of generality, we can set $E_f = E_V^{ch} = E_C^s$ at equilibrium. By integrating in parts, Equation (47) can thus be rewritten as follows:

$$I_d = \frac{We\sqrt{2m_t}}{8\pi^2\hbar^2} T \int_{E_C^s}^{E_C^s - eV_{ds}} [f(E_{fs}) - f(E_{fd})] \int_0^{E - E_C^s} \frac{1}{\sqrt{E_y}} dE_y \, dE$$

$$= \frac{We\sqrt{2m_t}}{8\pi^2\hbar^2} T \int_{E_C^s}^{E_C^s - eV_{ds}} [f(E_{fs}) - f(E_{fd})] \sqrt{E - E_C^s} dE \quad \textbf{(48)}$$

When saturation occurs, *i.e.,*

$$|eV_{ds}| \geq E_V^{ch} - E_C^s \quad \textbf{(49)}$$

The upper limit of the integral in Equation (48) is replaced by E_V^{ch} and the following expression can be obtained:

$$I_{sat} = \frac{We\sqrt{2m_t}}{6\pi^2\hbar^2} \left[-e(V_{gs} + V_{th})\right]^{3/2} \exp\left(-\frac{4\lambda\sqrt{2m_t} E_g^{3/2}}{3\hbar[E_g - e(V_{gs} + V_{th})]}\right) \quad \textbf{(50)}$$

6.2.2.2 Current model for 3-D devices

Similar to Equation (47), the current density per unit *area* in a 3-D tunnel transistor can be expressed as:

$$j_d = \int \frac{dk_x 2\pi k_\perp dk_\perp}{8\pi^3} \frac{\hbar k_x}{m_t} eT(f_s - f_d) \quad \textbf{(51)}$$

Where $E = E_x + E_\perp$ is the total electron energy including both longitudinal and transverse components, T is the tunneling probability at the junction, f_s and f_d represent Fermi distribution at two Fermi levels $f_s = f(E_{fs})$, $f_d = f(E_{fd})$.

<u>Case 1: Triangular barrier</u>

If the tunnel probability and the Fermi distribution are approximated as Equation (34) and a step function, respectively, then Equation (51) can be simplified to an analytical expression as follows:

$$j_d = \frac{em_t}{4\pi^2\hbar^3}\exp(-\frac{4\sqrt{2m_t}E_g^{\frac{3}{2}}}{3e\hbar F})\int_{\max(E_C^s,E_{fs})}^{\min(E_V^{ch},E_{fd})}(E - E_C^s)dE$$

$$= \frac{em_t}{4\pi^2\hbar^3}\exp(-\frac{4\sqrt{2m_t}E_g^{\frac{3}{2}}}{3e\hbar F})(\frac{1}{2}E^2 - EE_C^s)|_{\max(E_C^s,E_{fs})}^{\min(E_V^{ch},E_{fd})} \quad \textbf{(52)}$$

Which can be further reduced to the following form if similar conditions as the ones under which Equation (48) is derived are met:

$$I_{sat} = A\frac{em_t}{8\pi\hbar^3}\exp\left(-\frac{4\sqrt{2m_t}E_g^{\frac{3}{2}}}{3e\hbar F}\right)\left(E_V^{ch} - E_C^s\right)^2$$

$$= A\frac{e^3m_t}{8\pi\hbar^3}\exp\left(-\frac{4\lambda\sqrt{2m_t}E_g^{\frac{3}{2}}}{3\hbar\left[E_g - e\left(V_{gs} + V_{th}\right)\right]}\right)\left(V_{gs} + V_{th}\right)^2 \quad \textbf{(53)}$$

Where *A* is the device cross section area.

<u>Case 2: Parabolic barrier</u>

If the tunnel barrier is approximated to be parabolic, the tunneling probability (whose expression is then given by Equation (35)) will be further reduced due to the requirement to match the transverse momentum (energy).[83] Substituting the Fermi distribution with a step function, Equation (51) can be reduced to the following form:

$$j_d = \frac{em_t}{4\pi^2\hbar^3}\exp\left(-\frac{\pi\sqrt{m_t}E_g^{\frac{3}{2}}}{2\sqrt{2}e\hbar F}\right)\frac{\overline{E_\perp}}{2}[E + \frac{1}{2}\overline{E_\perp}\exp(-2\frac{E - E_C^s}{\overline{E_\perp}})]|_{\max(E_C^s,E_{fs})}^{\min(E_V^{ch},E_{fd})} \quad \textbf{(54)}$$

The integration in the above equation can be carried out via an approach similar to that used in case 1. Equation (55) can be obtained for saturation current in a tunnel transistor:

$$I_{sat} = A\frac{em_t}{4\pi\hbar^3}\exp\left(-\frac{\pi\lambda\sqrt{m}_t E_g^{\frac{3}{2}}}{2\sqrt{2}\hbar\left[E_g - e\left(V_{gs}+V_{th}\right)\right]}\right)\frac{\overline{E_\perp}}{2}\{-e\left(V_{gs}+V_{th}\right)$$
$$+\frac{\overline{E_\perp}}{2}[\exp(\frac{2e\left(V_{gs}+V_{th}\right)}{\overline{E_\perp}})-1]\} \quad \textbf{(55)}$$

Where A is the device cross section area and $\overline{E_\perp} = \frac{4\sqrt{2}e\hbar F}{3\pi\sqrt{m_t E_g}} = \frac{4\sqrt{2}\hbar\left[E_g - e\left(V_{gs}+V_{th}\right)\right]}{3\pi\lambda\sqrt{m_t E_g}}$

6.2.2.3 Additional notes for modeling nanowire tunnel transistors

Applying the model discussed in this section to TFETs based on Ge/Si core/shell nanowires requires only minor modifications. For example, due to the surrounding gate geometry and a cylindrical channel, the natural length λ of a different form needs to be used:[164]

$$\lambda = \sqrt{\frac{2\varepsilon_s d_{nw}^2 \ln\left(1+\frac{2t_{ox}}{d_{nw}}\right) + \varepsilon_{ox} d_{nw}^2}{16\varepsilon_{ox}}} \quad \textbf{(56)}$$

Where d_{nw} is the nanowire diameter. Moreover, $A = \frac{\pi d_{nw}^2}{4}$ needs to be used in Equation (55) to calculate the current analytically.

We have used the approximation that $E_V^{ch} - E_C^{s} \approx (V_{gs} + V_{th})$ throughout the previously discussed models. However, this assumption is not always true. Figure 49 plots the surface potential and the central potential at different V_{gs} for a cylindrical channel with 20 nm diameter, 5×10^{18} cm^{-3} doping concentration and 10 nm Al_2O_3 as dielectric. It is clear that the linear relation is only valid at sufficiently high (and positive) V_{gs}, *i.e.*, when the channel is fully depleted. To be more accurate, the movement of the energy bands (and local electrical field $F = \frac{E_g + E_V^{ch} - E_C^{s}}{e\lambda}$) needs to be evaluated by solving the Poisson's equation along the nanowire radial direction. Due to the

cylindrical symmetry, the total current can be obtained by numerical integrating the current densities according to the following:

$$I_d = \int 2\pi r j_d(r) dr \tag{57}$$

Some TFET models assume evenly distributed current so that the total current is calculated by $I_d = Aj_d$. Since the potential distribution along the radial direction is not uniform with surface potential being the highest in amplitude and most sensitive to V_{gs}, simply multiplying current density at the perimeter by the device cross section area tends to overestimate the current level and underestimate the SS.

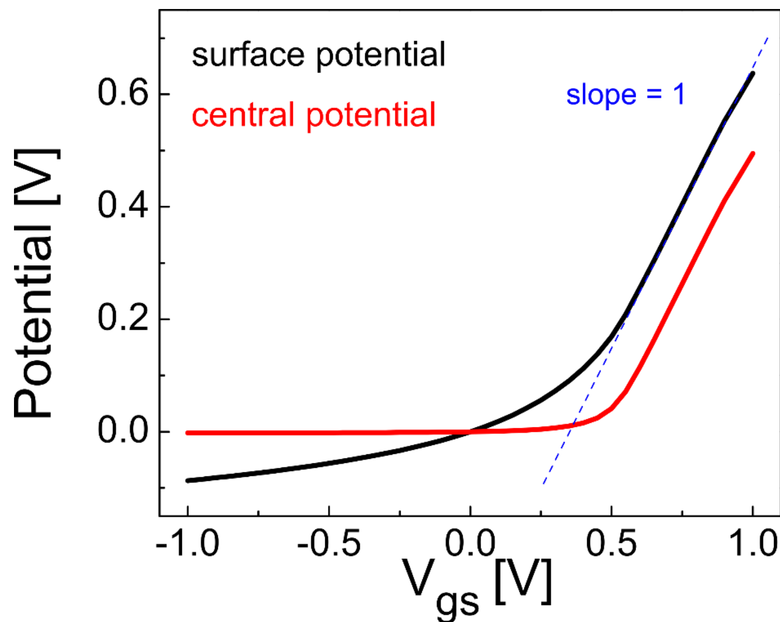

Figure 49. Potential profile at different gate voltages. Surface potential (black) and central potential (red) as a function of V_{gs} in a cylindrical nanowire channel. The channel is uniformly doped to 5×10^{18} cm^{-3} with diameter of 20 nm and surrounded by 10 nm of Al_2O_3.

For better accuracy and computing current other than I_{sat}, the following equation needs be evaluated numerically:

$$j_d = \frac{em_t}{4\pi^2\hbar^3} exp\left(-\frac{\pi\sqrt{m_t}E_g^{\frac{3}{2}}}{2\sqrt{2}e\hbar F}\right)\int_{E_C^S}^{E_V^{ch}}\left[1 - exp\left(-2\frac{E-E_C^S}{\overline{E_\perp}}\right)\right](f_s - f_d)dE \quad \textbf{(58)}$$

Which is derived from Equation (51) without the use of step-wise Fermi distribution.

6.2.3 Qualitative study on nanowire tunnel transistor performance

Current-voltage characteristics of a nanowire tunnel transistor were simulated with Equation (58) assuming non-uniform current distribution along radial direction. The nanowire tunnel transistor consists of a heavily doped source (n-type, 5×10^{19} cm^{-3}), a cylindrical channel (diameter of 20 nm, doped with p-type) with surrounding gate (10 nm Al_2O_3) and a heavily doped drain (p-type). Effective tunnel mass m_t is assumed to be $0.12m_0$, same as the effective conduction mass in Ge. Figure 50 plots the transfer and output characteristics of the device under study. P-type transistor behavior with varying SS in the subthreshold regime is evident. In the on-state, the saturation current I_{sat} increase slows down at higher V_{gs}, due to the screening of the accumulated carriers near the nanowire/oxide interface at high V_{gs}.

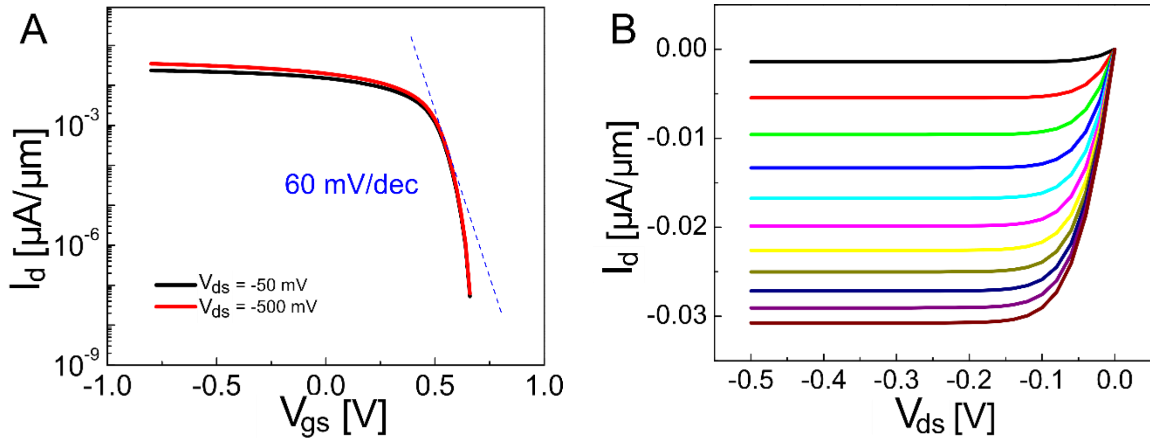

Figure 50. Simulated TFET characteristics. (A) Transfer curves with V_{ds} of -50 mV and -500 mV. (B) Output curves with V_{gs} between -0.5 V and 0.5 V, in 0.1 V step. This calculation is performed with the following parameters: channel diameter of 20 nm, gate dielectric of 10 nm Al_2O_3, effective tunnel mass of 0.12 m_0, source doping of 5×10^{19} cm^{-3} and channel doping of 5×10^{18} cm^{-3}.

The effect of gate dielectric scaling was studied by changing the dielectric constant and thickness while keeping other parameters unchanged. The calculated results are plotted in Figure 51. With progressively better gate dielectric (from 10 nm Al_2O_3 to 5 nm ZrO_2, with dielectric constant of 23.0), both the current density and SS improve substantially, leading to better I_{on}/I_{off} ratio and smaller average SS. These trends can be understood from improved gate control and enhanced electric field at the junction (due to reduced natural length).

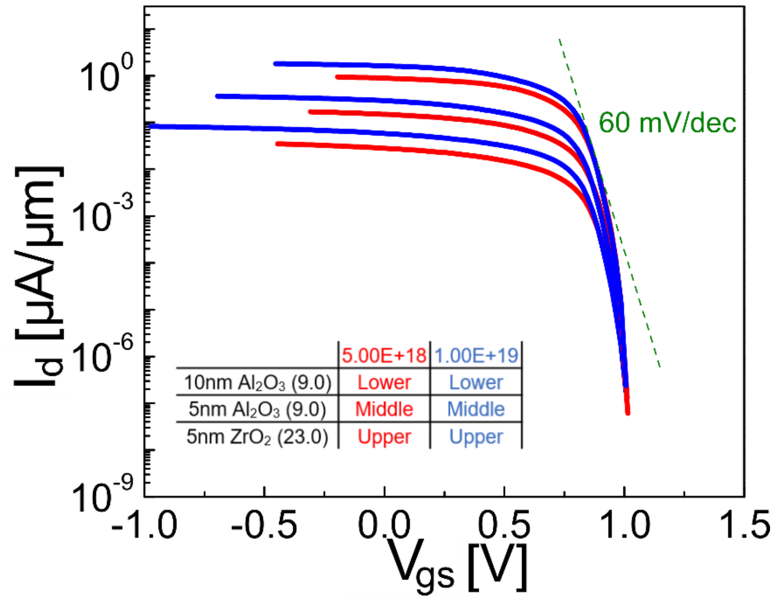

Figure 51. Simulated tunnel transistor performance with various gate dielectric. Simulated transfer characteristics of a TFET with different channel doping (red, 5×10^{18} cm^{-3}, blue, 1×10^{19} cm^{-3}) and gate dielectric (from bottom to top, 10 nm Al_2O_3, 5 nm Al_2O_3 and 5 nm ZrO_2). Other parameters are set as the following: channel diameter of 20 nm, effective tunnel mass of 0.12 m_0 and source doping of 5×10^{19} cm^{-3}. Curves are shifted horizontally for clarity.

The effective tunnel mass m_t is also an important parameter to be considered when designing a high performance TFET. Due to the exponential dependence of the tunnel probability on m_t, materials with smaller m_t inherently carries higher tunneling current. Figure 52 shows the effect of varying m_t on the performance of a nanowire tunnel transistor, in which the exponential boost of I_{on} by reducing m_t can be clearly seen.

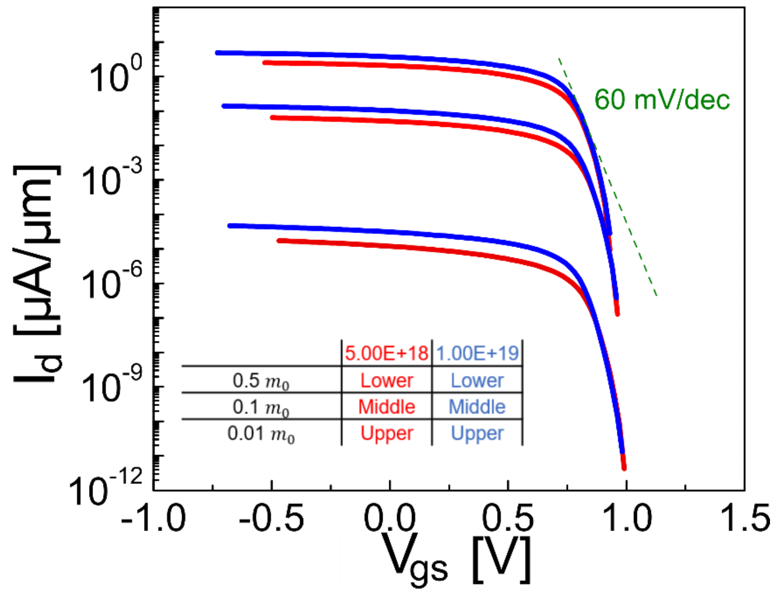

Figure 52. Simulated tunnel transistor performance with various effective tunnel masses. Simulated transfer characteristics of a TFET with different channel doping (red, 5×10^{18} cm^{-3}, blue, 1×10^{19} cm^{-3}) and effective tunnel mass (from bottom to top, $0.5m_0$, $0.1m_0$ and $0.01m_0$). Other parameters are set as the following: channel diameter of 20 nm, gate dielectric of 10 nm Al_2O_3, and source doping of 5×10^{19} cm^{-3}. Curves are shifted horizontally for clarity.

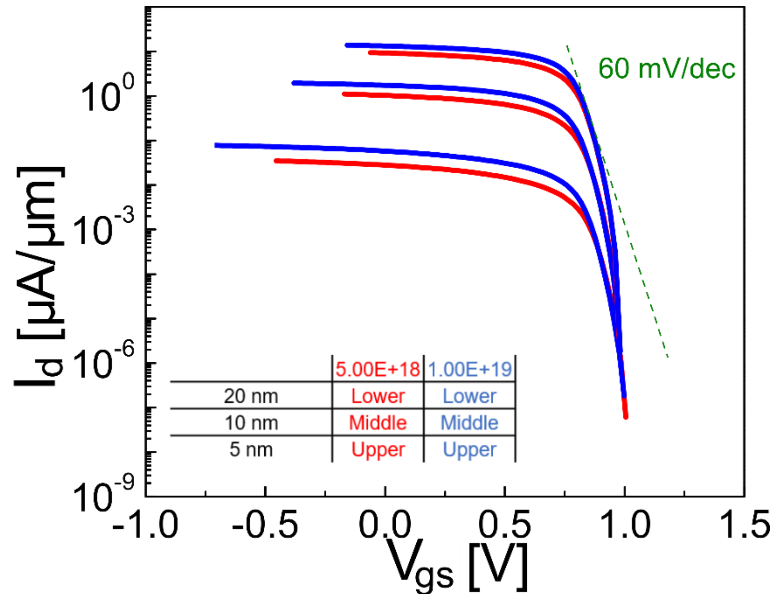

Figure 53. Simulated tunnel transistor performance with various nanowire diameters. Simulated transfer characteristics of a TFET with different channel doping (red, 5×10^{18} cm^{-3}, blue, 1×10^{19} cm^{-3}) and channel diameter (from bottom to top, 20 nm, 10 nm and 5 nm). Other parameters are set as the following: gate dielectric of 10 nm Al_2O_3, effective tunnel mass of $0.12m_0$ and source doping of 5×10^{19} cm^{-3}. Curves are shifted horizontally for clarity.

Finally, we investigated the effect of device dimensions by varying the nanowire diameters. The simulated results are presented in Figure 53. By adopting smaller nanowires, the electric field at the junction is enhanced due to the reduced natural length λ, an effect similar to thinning down the gate dielectric thickness. This effect can be rather dramatic, as a ten-fold boost is achieved by using 5 nm nanowires instead of 10 nm ones, although the actual current enhancement would be smaller, due to reduced conduction area (width). However, this can be offset by using multiple nanowires in one device to create parallel channels.

6.3 Experimental characterization of vertical nanowire tunnel transistor

Due to the one dimensional hole gas in Ge/Si core/shell nanowire, which acts as effective p-type dopants, tunnel transistors can be constructed using the nanowires as conduction channel. P-type tunnel transistors are realized if the nanowires can be integrated on heavily n-type doped Si substrate. In this design, the channel region is also p-type doped, which differs from the original p-i-n structure. However, as long as the surrounding gate can maintain a strong coupling to the nanowire channel and efficiently modulate the band energies, it would not be an issue for functional TFET operation.

Similar to the vertical nanowire junctionless transistors discussed in chapter 5, vertical nanowire tunnel transistors can be fabricated following almost the same process as described in Figure 33, with the exception of starting with an n-type Si substrate rather than a p-type substrate. In the finished device, the Si/Ge substrate/nanowire heterojunction will be used as the source/channel junction. Due to the type-II band alignment, the actual tunnel barrier height will be lowered, which can potentially lead to improved tunnel probability and current level.

Typical output and transfer characteristics for tunnel transistors with a 20 nm nanowire diameter and 10 nm Al_2O_3 gate dielectric are shown in Figure 54, where p-type behavior can be confirmed. Current density was extracted to be 62.2 μA/μm (12.7 μA/μm) at $V_{ds} = V_{gs} = -2V$ $(-1V)$, which is a respectable value compared with other TFETs in Figure 47.[149] DIBL was found to be negligible from Figure 54B and SS of 178 mV/dec was extracted.

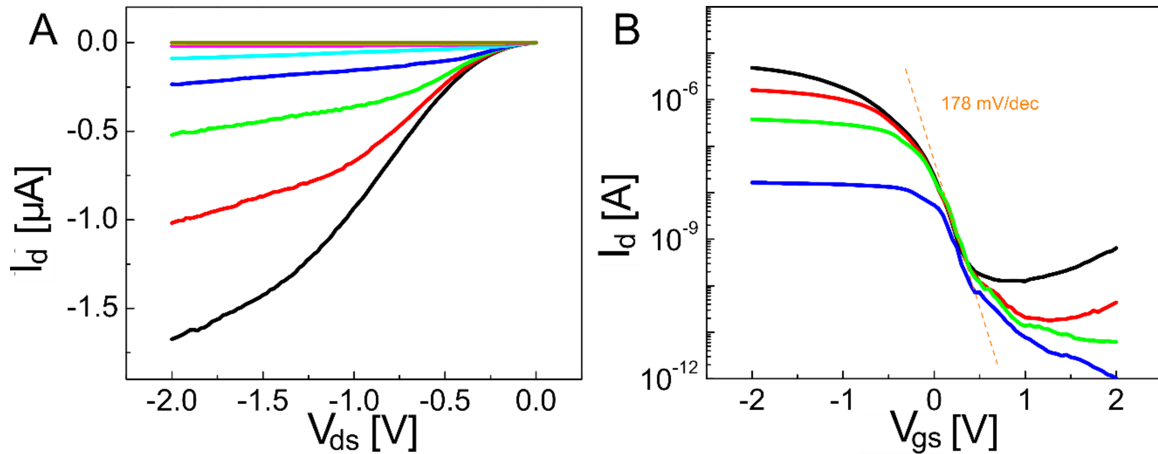

Figure 54. Measured data of vertical nanowire tunnel transistors. (A) Output characteristics of TFET with V_{gs} from -1 V to 0.4 V, in 0.2 V step. (B) Transfer characteristics of TFET with V_{ds} of -2 V, -1 V, -0.5 V and -0.1 V.

The tunnel transistor performance was further investigated at different temperatures. Figure 55A-B shows the output and transfer characteristics of the same device at 100 K where a lower SS of 38 mV/dec can be extracted. This trend is more clearly seen from Figure 55C in which the measured current at different temperatures are compared. While I_{on} did not change much, I_{off} and SS improved quite significantly when the device was cooled down. The extracted SS values at various temperature are plotted in Figure 55D, where a superliner relation can be found between SS and temperature. Different temperature dependence in ON state and subthreshold/OFF state suggests that different mechanisms may be responsible for this behavior. We did not observe any noticeable difference when the device was measured either in vacuum, or ambient environment. Shielding ambient light did not affect the device characteristics either. Moreover, in our tunnel

transistor, source and drain are doped with opposite type (source is n type doped while drain is p type doped) and reversely biased. Thus, it is unlikely that other thermionic conduction mechanisms (*e.g.,* conduction through surface states) will play an important role due to the high energy barrier at the source/channel junction (ON state, Figure 56A) or drain/channel junction (OFF state, Figure 56B). So we conclude that device current is due to the tunneling process.

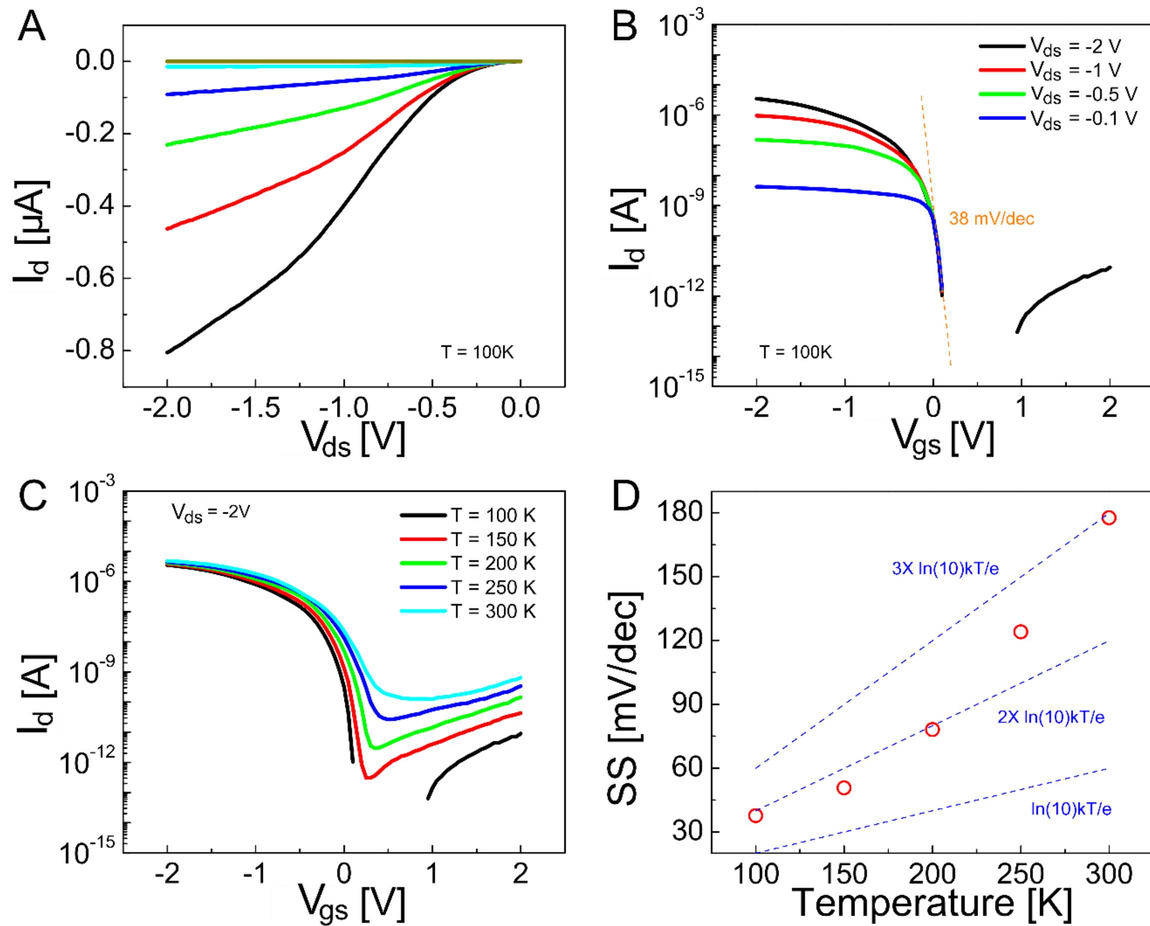

Figure 55. Study of vertial nanowire tunnel transistos at various temperatures. (A) Output characteristics at 100 K with V_{gs} from -1 V to 0.4 V, in 0.2 V step. (B) Transfer characteristics at 100 K with V_{ds} of -2 V, -1 V, -0.5 V and -0.1 V. (C) Transfer characteristics of TFET with V_{ds} of -2 V. measured at temperatures between 100 K and 300 K. (D) Extracted SS values at between 100 K and 300 K. The dashed lines are 1×, 2× and 3× thermal limit of $\ln(10)\ kT/e$.

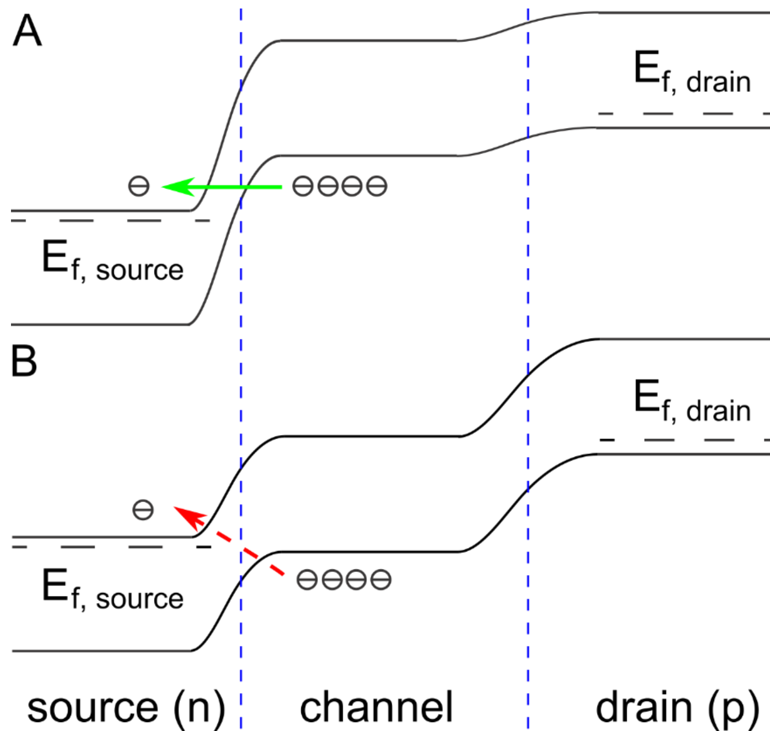

Figure 56. Schematic of band diagrams of a TFET. (A) At ON state, band to band tunneling is permitted. (B) At OFF state, band to band tunneling is prohibited.

Theoretically, tunnel transistor should have a very weak temperature dependence since the tunneling process does not require thermal activation, but the presence of interface states may introduce trap assisted tunnel (TAT) current in subthreshold region, which allows tunneling across energy band gaps and deteriorate device performance.[150], [163], [164] As shown in Figure 57A, while direct tunneling from point 1 to point 2 is forbidden (due to energy conservation requirement), electrons are free to move onto a trap state at point 3 (with energy gain) then tunnel to point 2 (or in a similar process with an alternative route 1→4→2).[83] Such a tunneling process through intermediate trap states involves additional, thermally-activated trapping/de-trapping process and thus it has a non-negligible and positive temperature coefficient. Activation energies were extracted for different bias conditions and the results were displayed in Figure 57B. E_a started very small at negative V_{gs} since BTBT current is dominant in the ON state, while increasing E_a was observed in the subthreshold regime, caused by a larger contribution from the TAT current.

E_a dropped again at higher positive V_{gs}, which is attributed to the ambipolar conduction in tunnel transistor when tunneling through channel/drain occurs.

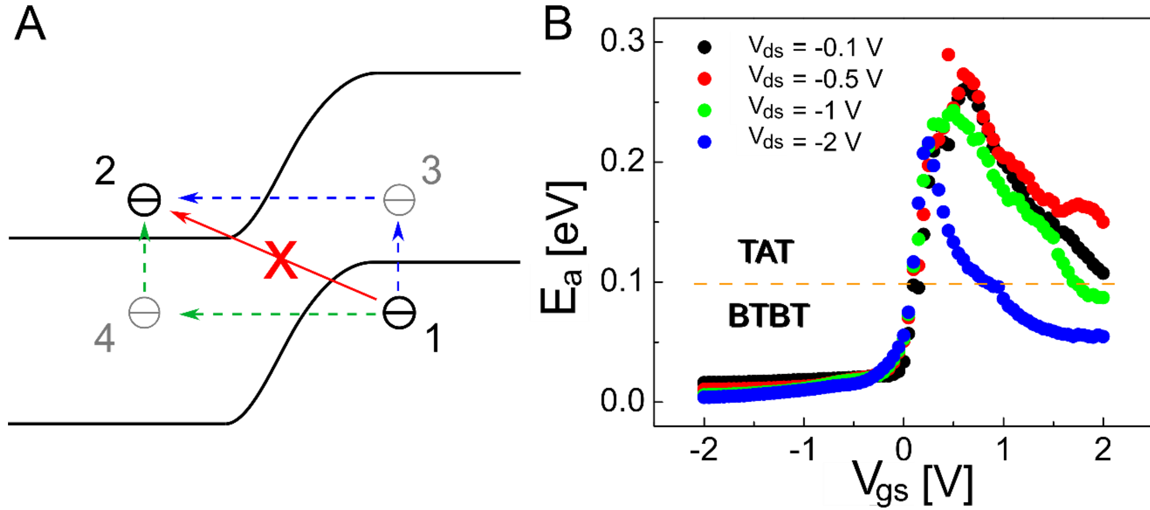

Figure 57. Trap assisted tunneling in TFET. (A) Schematic of TAT process at the source/channel junction. (B) Extracted activation energy E_a for different bias conditions. Dashed line separates two regimes where TAT and BTBT dominates.

Poole-Frenkel (PF) mechanism can be used to model the electrons escaping process from trap states and moving into the conduction band in the source.[152] In PF conduction, the current has the following dependence:[165]

$$I \propto Fexp(-\frac{\psi - e\sqrt{eF/\pi\varepsilon}}{kT}) \quad \textbf{(59)}$$

Where ψ is the effective energy barrier for the trapped electron, F is the electric field and ε is the dielectric constant of the semiconductor material. A quick estimation of the electric field yields $F = \sqrt{eN(V_{bi} - V_{ds})/\varepsilon}$ between 6.22×10^5 V/cm and 1.23×10^6 V/cm (assuming $N \sim 5 \times 10^{18} cm^{-3}$, $V_{bi} \sim 0.5V$) for V_{ds} ranging from -0.1 V to -2 V. By adding $e\sqrt{eF/\pi\varepsilon}$ to the activation energy extracted in Figure 57B, ψ between 0.4 to 0.5 eV was obtained. Thus we conclude that the trap states indeed reside in the mid-gap, which is consistent with the TAT mechanism.

The origin of these interface traps is still not thoroughly investigated. Bessire *et al.* reported TAT current at an InAs/Si heterojunction and attributed the trap states to dislocations and point defects stem from the high lattice mismatch between the two materials.[166] We did not observe any pronounced effect due to interfacial traps in our Ge/Si heterojunctions (both regular pn diode and Esaki diode) in chapter 3.[102] It is likely because that the nanowires used in those devices were patterned using the oxide trench method, thus they were immediately passivated after growth and protected throughout the process. On the contrary, in vertical transistor (both junctionless transistor and tunnel transistor) fabrication, we employed an RIE step to remove the nanowires outside the active area (marked area in Figure 34), so it is possible that nanowires and the heterojunction interface might get damaged during the process. For junctionless transistors, interfacial traps should not affect the device performance since both Ge and Si are heavily doped thus most of the device resistance comes from nanowire channel. In contrast, for tunnel transistors, interfacial traps can cause degraded performance as we observe now. Additional experiments and process optimizations would be necessary to uncover the causes of these trap states and help eliminate TAT current.

In addition to optimizing the fabrication process, device performance can be boosted by improved design. As shown in Figure 58A, one noticeable flaw in the original device design is the underlap between gate and source/channel junction due to the presence of high-k dielectric. Ideally, a perfectly aligned, or overlapped gate/source is desired to allow V_{gs} to efficiently modulate the band energy in the channel to maximize electrical field and tunnel probability at the tunnel junction. For this reason, vertical tunnel transistor can benefit from the raised Ge/Si heterojunction as shown in Figure 58B. Figure 58C shows an SEM image of Ge nanowires grown on ~ 50 nm Si pillars, which allow for ~ 40 nm overlap between gate and source if 10 nm Al_2O_3 is used as gate dielectric.

These Si pillars are etched with 30 nm Au nanoparticles as masks, in Plasmastherm 790 at a pressure of 30 mTorr with 18/6/6 sccm SF_6/CF_4/CH_4 and power of 300 W for 60s, followed by 20 sccm Ar treatment for 20 s at the same pressure/power settings. As discussed in chapter 3, the purpose of the second Ar treatment is to clean the Au surface and promote vertical growth.

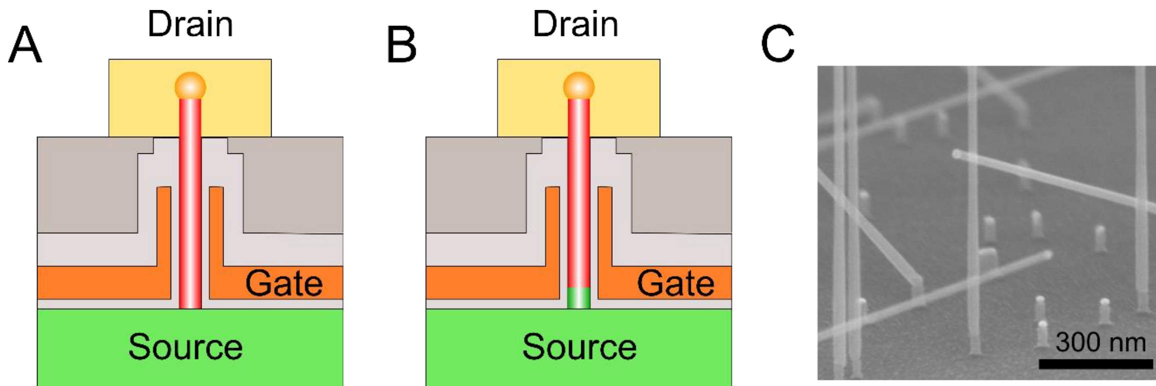

Figure 58. Schematic of improved TFET design. (A) TFET with G/S underlap. (B) TFET with G/S overlap due to raised Ge/Si heterojunction. (C) SEM image of Ge nanowires grown on Si pillars created via RIE.

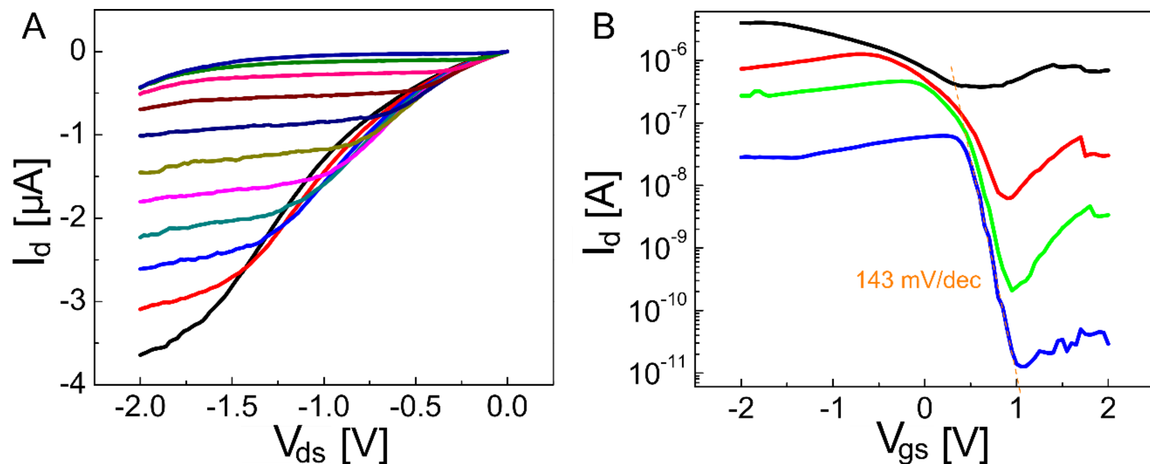

Figure 59. Measured data of vertical nanowire tunnel transistors with raised Ge/Si junction. (A) Output characteristics of TFET with V_{gs} from -1 V to 1 V, in 0.2 V step. (B) Transfer characteristics of TFET with V_{ds} of -2 V, -1 V, -0.5 V and -0.1 V.

A prototype tunnel transistor with the raised Ge/Si junction is fabricated and characterized. The device performance is shown in Figure 59. Due the poor Al_2O_3 gate dielectric quality because of a tool problem, this device suffers from abnormally high gate leakage current. Nevertheless, an

improvement of both I_{on} and SS are observed, which can be attributed to enhanced electrical field profile.

6.4 Summary

In this chapter, the operation of tunnel transistor was investigated and a physics based analytical model for tunnel transistors was developed. Several approximations made during the derivation were discussed in detail and a more accurate, numerical model was proposed as well. This model overcomes the major flaws of previous analytical models reported (*e.g.*, non-zero current at zero V_{ds} and applicable to I_{sat} calculation only) while being able to capture the key features of the operation of tunnel transistors (current saturation, sharp transition with varying SS, trend with varying parameter values). Preliminary experimental results of a vertical tunnel transistor based on Ge/Si core/shell nanowires were also presented. P-type behavior was verified and band to band tunnel current was found to be dominant in the device ON state. The device performance is still not optimal, largely due to the contribution of trap assisted tunneling in subthreshold regime, which deteriorates subthreshold swing. While the measured results demonstrated in this chapter is just a prove of concept, further improvement is still underway. Acquiring a high performance TFET with dominant BTBT current in both ON/OFF states will open up the possibility to fit and calibrate the proposed TFET model, which be a very useful guide for future nanowire based tunnel transistors designs.

Chapter 7

Conclusion and future work

In this dissertation, we have achieved some experimental advances towards integration of VLS grown nanowires, in particular, vertical Au-catalyzed Ge nanowires on (111) Si substrate and demonstrated several electronic devices based on this vertical Ge/Si system including heterojunction diodes, junctionless transistors and tunnel transistors. We have also made an effort towards developing device models for both transistors with cylindrical channel and surrounding gate. In this chapter, we will conclude the progress made so far and discuss some of the possible directions we can work on to further extend these progresses.

7.1 Vertical Nanowire growth on (111) Si substrate

In chapter 2, we established Ge nanowire growth on (111) Si substrate with suppressed tapering and good vertical yield. Growth was achieved via Au-catalyzed VLS process with GeH_4/H_2 gas. A two-step growth was adopted to prevent aggressive conformal coating and confine growth to the axial direction. A nucleation step was introduced first at higher temperature to promote Ge-Au alloy formation and initialize growth while a second elongation step was carried out at lower temperature to suppress uncatalyzed sidewall deposition.

We also demonstrated several modifications to the original growth recipe to achieve a different material composition and morphology in a well-controlled fashion. A thin Si shell can be deposited after Ge nanowires were grown and this Ge/Si core/shell radial heterostructure can be

used to quantum mechanically induce high density one dimensional hole gas as carriers. Another way to adjust the doping level in Ge nanowires is through *in situ* doping by adding B_2H_6 during growth. Enhanced sidewall deposition due to B_2H_6 was observed as tapering is more severe at higher Boron concentrations. By diluting B_2H_6 to a Ge:B ratio of 40000:1, tapering can be largely eliminated. An alternative strategy to increase the doping level with a surface layer deposited by B_2H_6 alone was also shown. In addition, we carried out a systematic study on the impact of Si substrate on Au nanoparticle attraction and found that Au nanoparticles had a tendency to adhere better on n+ Si substrate than p+ ones under otherwise identical conditions, which resulted in a higher Au nanoparticle (and nanowire) density. While growth mechanism and results were not seen to be affected by the substrate difference, this factor must be taken into consideration when nanowire density needs to be controlled.

One major concern of incorporating chemically synthesized nanowires in mainstream industry is the lack of deterministic growth method. With vertically orientated nanowires, many interesting ideas including 3-D stacking and integration can be realized. However, a few technologically challenges must be overcome. In essence, VLS growth (or bottom-up approach in general) needs to develop control over growth location, orientation with nanoscale precision and good yield before this method can be used at a larger scale. With vertical device integration in mind, we showed progress towards improved growth techniques, such as selective area growth by patterning Au nanoparticles and the use of Ge buffer layer to improve vertical yield. Although further optimization is still required to meet precision required for scaling up, we believe these results will be beneficial to the development of integration techniques of vertical nanowire devices with mainstream CMOS circuits.

7.2 Characterization of Ge/Si heterojunction interfaces

In chapter 3, we focused on the interface properties of Ge nanowire/Si substrate since all Ge/Si heterojunctions revolve around this interface. In most applications, a clean interface with low defect density is desirable. By proper surface treatment and optimizing growth recipe, vertical Ge nanowire growth can be achieved on (111) Si substrate. While verticality is a hint to epitaxy, a more detailed study using TEM was still required to obtain more decisive information about the heterojunction quality, such as defect density and junction abruptness.

To better characterize Ge/Si heterojunction, a RIE process was developed to produce a short Si pillar with a neck region using vertical nanowire as etching mask. This etching step allowed subsequent mechanical transfer of the Ge/Si structure on copper grid for TEM studies. Without the Si pillar, dry transfer was not possible since nanowire almost always broke at the weakest spot, which happened to be the Ge/Si interface. We have also optimized an alternative process so that Au can also be used as etching mask and Ge nanowires can be grown on top of the created Si pillars while retaining vertical growth direction.

HRTEM study on both samples confirmed epitaxial relation between Ge and Si with no apparent edge dislocation, indicating an intrinsic and clean interface. An interfacial amorphous layer was observed, probably due to the evitable native oxide formation even though we strived to minimize the time between sample preparation and growth. A more important finding came from STEM EDX line scan, in which we mapped the Ge(Si) concentration along the growth direction. A narrow transition width of 10-15 nm was extracted, suggesting a sharp Ge/Si interface, which can be particularly useful in tunneling diode or tunnel transistors where high electric field from abrupt junction is crucial for high tunneling current.

7.3 Two terminal devices based on vertical Ge/Si heterojunction

In chapter 4, we begin to explore the potential application for vertical Ge nanowire on Si substrate. We started by developing a fabrication process for vertical two terminal devices where Si substrate act as a global electrode while another top electrode was deposited on the single vertical nanowires. Three different types of Ge/Si heterodiodes with independently tuned doping profile on both sides were fabricated and their performance was analyzed by classical theories.

First, vertical Ge/Si heterogeneous pn diode was fabricated. Ge nanowire is naturally p-type due to surface Fermi level pinning in the absence of intentional dopants. Si substrate was chosen to be moderately n-type doped with localized, heavily doped area next to each device for electrical contact. We demonstrated diode devices with an ideality factor of 1.16 and 10^6 rectifying ratio at room temperature. Notably this heterodiode exhibited a very low leakage and close to unity ideality factor, both of which are signs for a good Ge/Si interface with low defect density.

Then we raised the p-type doping in Ge nanowire by coating with a thin Si shell and switched to heavily n-type doped (111) Si substrate. Due to the degenerate doping on both sides, an Esaki diode was formed and NDR was observed at room temperature. This hetero tunnel diode showed high tunneling current (3.2 μA/μm at 0.5 V reserve bias), thanks to type-II band alignment and narrow transition region in Ge/Si heterojunction. Temperature dependent measurement was also performed and the trend of peak current can be modelled by a band-to-band tunnel theory with good agreement. Room temperature NDR is generally difficult to achieve in indirect bandgap material such as Ge and Si due to low tunneling probability in those materials. As a result, BTBT current would be effortlessly screened by current due to defect-related mechanisms such as trap assisted tunneling and generation-recombination. However, thanks to our high quality Ge/Si

interface and consequently suppressed current through defects, this signature behavior of tunnel diode was observed.

Finally, we were able to verify the existence of a barrier at Ge/Si interface due to large valence band offset. Numerical simulation was used to predict non-ohmic behavior then followed by experimental demonstration. A model based on field emission through Schottky barrier was used to fit the measurement results and good agreement was obtained for I-V characteristics at different temperatures.

Through these devices, we have shown that Ge/Si system is indeed very flexible as it can be transformed into several configurations with very different characteristics. More importantly. Such change only introduces minimal modification to the fabrication process. In addition, we would like to point out that good agreement between experimental results and theoretic prediction also proved that our Ge/Si system has a high quality interface without many non-ideal factors.

7.4 Vertical Ge/Si core/shell nanowire junctionless transistor

In chapter 5, we continued to explore the potential applications of vertical Ge nanowire and moved on to vertical junctionless transistors. Junctionless transistor is essentially a gated diode where gate is used to control the thickness of the depletion region in the channel, which in turn determines whether current flow is allowed or blocked. Vertical Ge/Si core/shell nanowire is a promising platform for junctionless transistor since it can provide high carrier density thanks to one-dimension hole gas induced by Si/Ge/Si quantum well and its nanoscale body coupled with surrounding gate architecture that allows fully depleted body at low gate voltage.

To capitalize on the benefits Ge/Si core/shell nanowire can offer, we fabricated and characterized vertical junctionless transistor based on this very material system. High I_{on} of 750

μA/μm with little short channel effects and subthreshold swing of 125 mV/dec were demonstrated in junctionless transistor with single Ge nanowire.

A junctionless transistor model based on simplified Poisson's equation was also developed and used for comparing with the measured results. By using mostly known parameters and experimentally extracted quantities, good agreement was obtained for two sets of devices with different gate lengths.

One potential advantage with vertically orientated channel is that the gate length is no longer determined by lithography (which happens to be the bottle neck in modern transistors), but the deposited film thickness (which can be controlled with atomic precision). We also showed that by controlling the thickness of a masking layer, the gate length in our vertical devices can be tuned in a consistent way. By studying the statistics of devices with two different gate lengths, we observed a single peak in ON/OFF state current difference for both devices, which indicates good uniformity and indirectly confirmed single nanowire operation. Devices with shorter gate length exhibited lower I_{on}, which can be attributed to the longer ungated length since distance between source and drain was constant in our design regardless of gate length.

In addition, an all-PMOS inverter with two junctionless transistors were demonstrated. Near rail-to-rail output with up to 500 Hz operation frequency was obtained. We also showed that by choosing multi-nanowire devices as the driver, both output range and inverter gain can be improved. This feature can be realized by scaling up the nanowire density during growth without the change in device size. Low cut-off frequency was likely due to large parasitic gate to drain capacitance, thus improvement of circuit speed should be possible with optimized design.

7.5 Tunnel transistors based on vertical Ge/Si core/shell nanowires

In chapter 6, we focused on understanding the operation mechanism of tunnel transistors. Due to the inherent energy filtering effect in band to band tunneling, devices who base their conduction mechanism on it is not bound by the 60 mV/dec limit of subthreshold swing at room temperature. The Ge/Si system we have been developing in the previous chapters can offer some unique advantages such as smaller bandgap, type-II band alignment and high quality heterojunction towards TFET applications.

One barrier for tunnel transistor to gaining more popularity is its lack of analytical device model. Simulational study on TFET is usually computer intensive and time consuming as a result. Some previous reported work proposed simpler analytical models, although they were not without limitations. Thus we proposed a model based on the fundamental tunneling process, and simplified with some justified approximations. We also demonstrated that this model is able to reproduce some key features in TFET operation. This model could also become a useful tool if calibrated with experimental data, which would also be a direction for future work.

Preliminary experimental results on vertical tunnel transistor based on Ge/Si core/shell nanowires were presented. The fabrication process remained largely the same as vertical nanowire junctionless transistor except the starting Si substrate was changed from p-type to n-type. P-type TFET behavior was confirmed with subthreshold swing of 178 mV/dec at room temperature. Measurement at lower temperatures reveled different temperature dependences in different operation regimes, which was caused by BTBT and competing trap assisted tunneling mechanism. The fabricated devices proved that the Ge nanowire can be used as the conduction channel in a tunnel transistor, although further optimization is still required for better performance.

7.6 Some directions for future work

By TEM characterization, we verified the presence of a high quality heterojunction interface in vertical Ge nanowire epitaxially grown on Si substrate. Through various heterodiodes and junctionless transistor, we demonstrate that this material system is capable of serving as the foundation of high performance electronics. Simple circuit component such as inverter built with vertical transistors were also shown to function correctly, although further optimization is still required to deliver faster speed. Despite all the progress, this study on vertical devices is by no means complete. There is still a long road ahead and a lot of work that can be done for extending its impact and usefulness. Here, we will discuss a few of them and present some preliminary results obtained so far.

7.6.1 Deterministic site-control for nanowire integration

In chapter 2, we touched upon the idea of controlling the nanowire growth sites by patterning Au colloid. This method was used in chapter 4 to obtain single nanowire diodes based on Ge/Si heterojunctions. However, this selective area growth method is still not optimal. More specifically, it only allows for patterning a fairly large area (μm scale due to wet etching used) and the exact number of Au nanoparticles is not precisely controlled. Positioning nanoparticles is not trivial and often times it requires manipulating the surface properties to attract nanoparticles to predefined sites. For example, one successful demonstration of arranging Au particles into periodic arrays is achieved with selectively functioning Si surface with positive charge to attract negative charged Au nanoparticles.[167]

The other, perhaps more traditional, approach is to use advanced lithography tools to pattern and deposit metal catalyst on desired growth sites. To this end, ebeam lithography (JEOL JBX-6300FS) was used to define arrays of nanodots with diameters ranging from 20 nm to 80 nm

on (111) Si substrate. 20 nm of Au was then deposited by evaporation and lift off process. After a brief BHF dip, the sample was loaded in the CVD system for Ge nanowire growth. Figure 60 shows an SEM image of the nanowires grown from 30 nm Au nanodots.

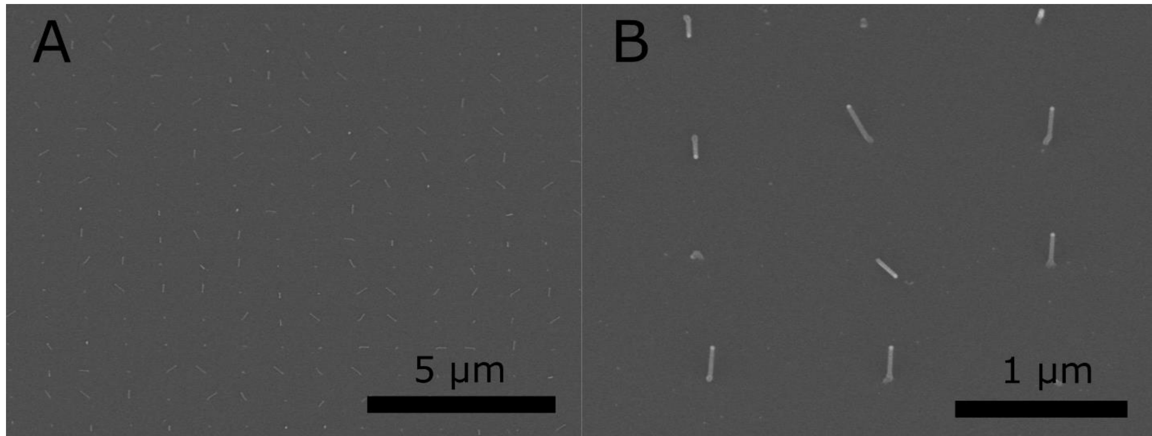

Figure 60. SEM image of nanowires grown from an array of Au nanodots. Au nanodots were defined by ebeam lithography. The diameter of the Au dots was designed to be 30 nm. The pitch of the array is 1 μm.

Although the size of the Au dots was very well controlled and close to designed value (SEM image not shown here), the nanowires were grown along multiple orientations and the nucleation yield was not satisfying. Random growth direction is typically a sign for non-epitaxial growth. Although the time between developing resist and transferring to evaporator chamber was kept as short as possible, native oxide formation before evaporator chamber reaches sufficiently low vacuum level still seemed inevitable. This interfacial layer will likely destroy the epitaxial relation from Si to Ge and cause non-uniform growth directions in nanowires. One potential solution is to process the sample in oxygen free environment such as a N_2 glove box. Another possible method is to use Ge buffer layer to promote vertical yield and restore epitaxy. As discussed in chapter 2, GeO_x can be relatively easily removed by atomic hydrogen produced in growth process,[117] so overall vertical yield could be improved. The ability to precisely and

deterministically define the location of Au nanoparticles for vertical Ge nanowires growth would be a crucial step towards integrating Ge based device on existing CMOS circuits.

7.6.2 Optimization of tunnel transistor based on Ge/Si heterojunction

In chapter 6, we demonstrated the operation of vertical nanowire tunnel transistor. These results should be treated as proof-of-concept. Further optimization is obviously required to truly realize the potential of the Si/Ge heterojunction. The ultimate goal is to demonstrate Ge nanowire based TFET with I_{on} comparable to state-of-art CMOS and sub-60 mV/dec switching at a lower supply voltage. Aside from perfecting fabrication process, a few changes in device design can be beneficial too. For example, gate dielectric with higher k value such as ZrO_2 can be used to boost gate capacitance and help suppress gate leakage current by allowing for thicker dielectric. A shorter gate length should be helpful to improve I_{on} as well. The seemly large temperature dependence of SS is also an issue. A detailed study on the origin of defects near tunnel junction and approaches to minimize or eliminate its impact would be necessary for achieving the goal too.

7.6.3 Vertical nanowire flash memory

In chapter 5, we demonstrated the operation of junctionless transistor based on vertical Ge nanowires. By simply replacing Al_2O_3 gate dielectric with other insulating materials, vertical flash memory can be realized. A tentative candidate for such gate stack is $Al_2O_3/ZrO_2/Al_2O_3$, which has been shown with planar Ge/Si core/shell transistors in previous publications.[168], [169] Deposition of $Al_2O_3/ZrO_2/Al_2O_3$ can be carried out sequentially in ALD tool with the help of our collaborator in Prof. Neil Dasgupta's group.

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