Yttrium and Scandium in Solution-processed Oxide Electronic Materials

by

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To my mom and dad,

for their unconditional love.

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Abstract

Yttrium and Scandium in Solution-processed Oxide Electronic Materials

by

Wenbing Hu

Chair: Becky (R. L.) Peterson

Large area electronics are critical for many novel applications such as smart windows, wearable electronics and Internet of Things. Among candidate materials, metal oxides have relatively good performance and stability and can be deposited by low-cost solution processes.

This thesis explores the roles of rare-earth elements yttrium and scandium in solution-processed metal oxide thin films including semiconducting scandium- or yttrium-doped ZTO, conducting scandium- or yttrium-doped zinc oxide, and insulating yttrium-scandium oxide. Yttrium and scandium can act as oxygen getters and stabilizers, and the use of higher-order alloys can improve film thermal stability and electrical performance.

First, thin film transistors (TFTs) are used to characterize undoped ZTO films as a baseline. The device performance of solution-processed ZTO TFTs depends on ink Zn to Sn ratio and annealing temperature, optimized to be 7:3 and 480°C, respectively. The

optimized ZTO has a shallow donor energy level of 7meV and a steep exponential subgap band tail with a percolation energy of 3meV. Sputtered Mo forms an excellent ohmic contact to solution-processed ZTO with a width-normalized contact resistance of 8.7Ω·cm and a transfer length of 0.34μm, making the technology suitable for future sub-micron channel length devices.

Yttrium enhances performance of ZTO TFTs at low concentrations (<1at%), but compromises device DC performance at high concentrations (>3at%). High yttrium concentrations slightly improve TFT negative bias illumination stress stability by reducing oxygen vacancy-related defects.

Second, the introduction of scandium or yttrium in solution-processed ZnO decreases the conductivity by three orders of magnitude, which is ascribed to formation of insulating structures along grain boundaries. Scandium or yttrium also make the resistivity of ZnO more thickness-dependent than undoped ZnO after forming gas anneal, by causing surface depletion and grain disruptions in the film.

Third, solution-processed $(Y_xSc_{1-x})_2O_3$ insulating alloys have comparable dielectric performance to vacuum deposited $(Y_xSc_{1-x})_2O_3$, with high breakdown field > 4MV/cm, low leakage current and low dielectric frequency dispersion. Even after 900°C anneals induce crystallization, the alloys maintain a high breakdown field.

The yttrium- and scandium- doped solution-processed oxides developed here form a complete suite of electronic materials suitable for fabrication of future large-area electronic devices.

Chapter 1 Introduction

1.1 Oxide electronic materials

Oxides are widely used in a variety of applications because of their unique mechanical, chemical, optical and electrical properties. Electrically, oxides can be used as dielectrics (SiO_2, Al_2O_3, HfO_2, ZrO_2), conductors (indium tin oxide (ITO), Al:ZnO, CdO), semiconductors (ZnO, SnO_2, Cu_2O, InGaZnO, ZnSnO), superconductors ($YBa_2Cu_3O_{7-d}$, $HgBa_2Ca_2Cu_3O_{8+\delta}$), ferroelectrics ($BaTiO_3$, $SrTiO_3$, PZT), piezoelectrics (PZT, ZnO), and as optoelectronic materials (Y_2O_3:Eu^{3+}, Nd:$Y_3Al_5O_{12}$) [1]–[9]. As can be seen, metal oxides are typically used for electronic applications. In fact, metal oxides are the most abundant materials in the Earth's crust [10]. In general, metal oxides are relatively stable in air, have a large band gap (>2eV) and have a high melting temperature (>1000K). With these properties, metal oxides have become the core of many traditional and novel devices such as transistors, diodes, memory devices, power devices, photo sensors, lasers, and other sensors and actuators which enable novel applications in lighting, high power, energy, artificial intelligence, health care and consumer electronics, as shown in Figure 1-1.

A big proportion of the oxide electronic materials are multi-component oxides, which are high order alloys of binary oxides (i.e. MO_x), for example, ternary oxide ITO or quaternary oxide $YBa_2Cu_3O_{7-d}$. Different binary oxides are often alloyed to obtain properties that a binary oxide does not have, such as keeping an oxide in an amorphous

phase to achieve uniformity over large areas, eliminating non-stoichiometric defects to enable stable performance, maintaining a perovskite crystal structure with ferroelectric properties, doping a semiconducting oxide to form a conductor, and intentionally introducing certain atomic/electronic energy levels for light emission and absorption.

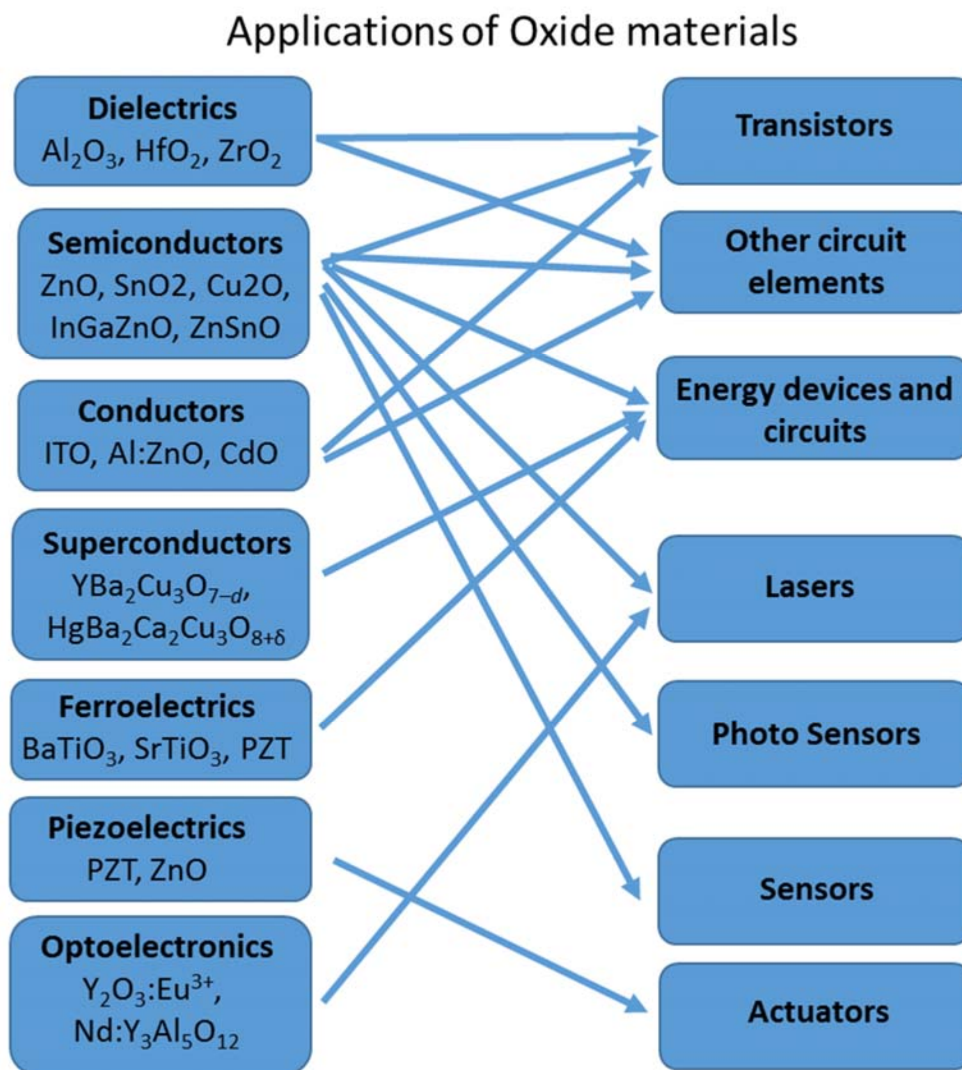


Figure 1-1. Common oxide materials and their applications in electronic devices.

One of the missing pieces of oxide electronic material studies is a deep understanding of the roles of certain binary oxides components in a multi-component alloy oxide. Binary components often have more than one role in alloys. Being able to identify the roles could help predict material behavior, preventing unexpected complications during material design.

Another challenge is stoichiometry control in oxides. Most oxides are non-stoichiometric, meaning that the atomic ratio of the elements is not ideal. The non-stoichiometric oxides exhibit defects such as vacancies and interstitials of both cations and oxygen. These defects can drastically affect the electrical properties of these materials. For example, Zn interstitials in ZnO form shallow donor states, making the material more conductive. Being able to control the stoichiometry and to identify the factors affecting stoichiometry is also an important question to study.

1.2 Large area electronics

A growing field in electronics is large area electronics (LAE) [11]–[13], where devices are made on a large surface. Typical LAE applications include display and lighting, smart windows, photovoltaics, wearable and/or flexible electronics, sensors and actuators, and communications (Figure 1-2). Contrary to traditional electronics, which focuses on making smaller devices, LAE requires the materials and devices to be inexpensive, easy to deposit over large areas, uniform, and with high and stable performance. Current candidate materials include 2-D materials, organic materials, and metal oxides. Among these, metal oxides are promising, but as stated in Section 1.1, they require further development to

achieve higher performance and more stable devices. These concerns can be addressed by better understanding the roles of binary components and the influence of process conditions.

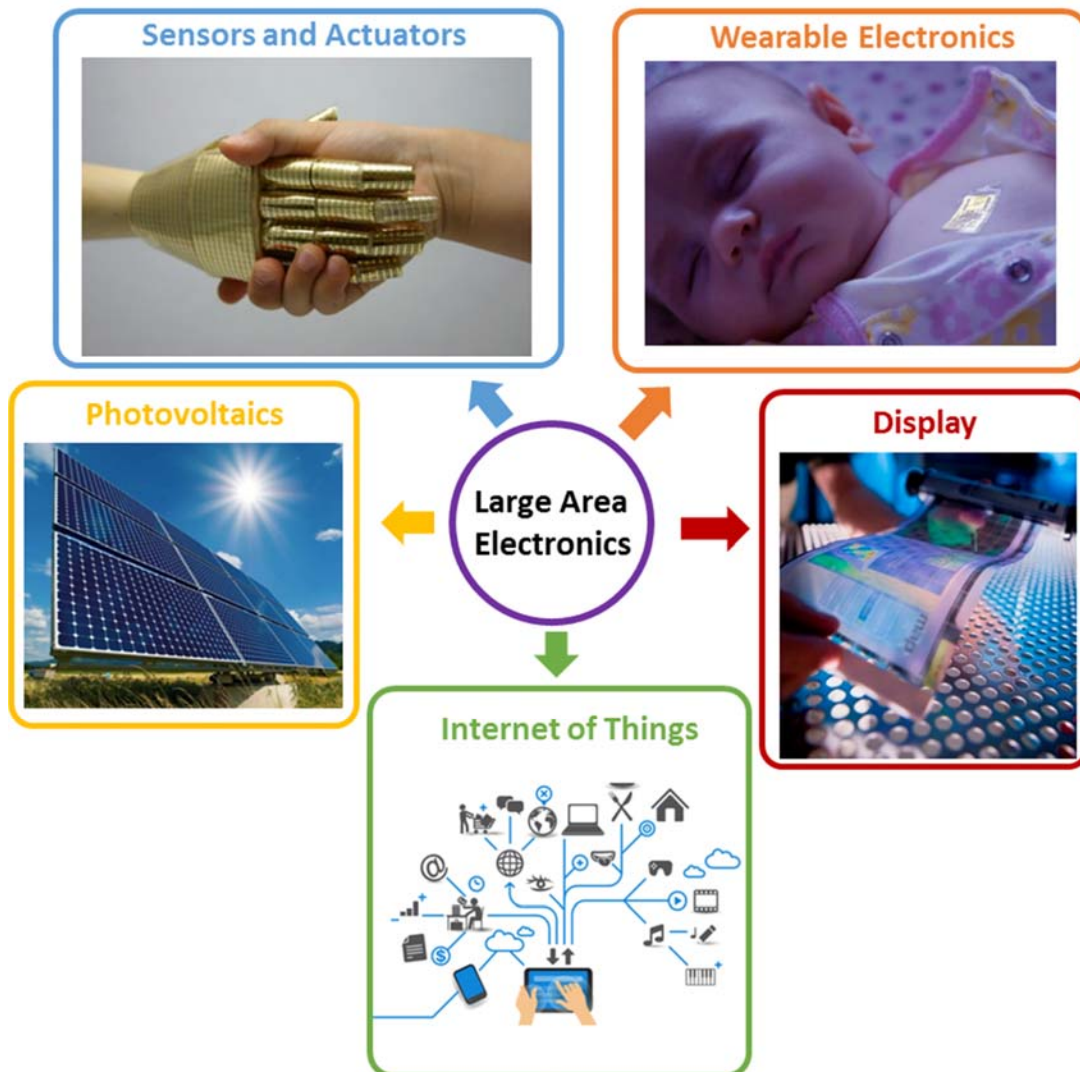


Figure 1-2. Selected applications of large area electronics (LAE).

1.3 Solution process thin film deposition technique

Metal oxides thin films can be deposited by a variety of processes during micro/nano-fabrication. Vacuum-based thin film deposition techniques, such as evaporation, sputtering, atomic layer deposition and pulsed laser deposition, have been extensively used for oxide deposition. Each technique has its own advantages, making it suitable for certain materials or certain applications. What these techniques have in common is the need for a vacuum deposition chamber for (toxic) gas and/or material confinement, oxidation prevention, reaction rate control and uniformity improvement. The requirement for vacuum chambers makes these techniques unsuitable for large area or roll-to-roll thin film deposition applications. In addition to the cost and physical restrictions of vacuum chambers, most of these techniques, especially physical vapor deposition, are highly costly because a large portion of the raw material (as much as 70% or more) ends up on the chamber wall, wasted [14], [15].

As the need for low cost and large area thin film deposition grows, solution-based deposition techniques are drawing an increasing attention [12], [16], [17]. In general, a solution process includes the following steps (Figure 1-3): (1) coating solution/ink preparation by dissolving precursors in solvents, (2) ink deposition onto the desired surface and/or locations using various deposition techniques, (3) film formation by evaporating solvent and by inducing chemical reactions/physical transformation through pyrolysis/annealing/combustion [16], [18]. During these steps, a vacuum environment is usually not required, and the amount of material waste can be minimized by carefully controlling the ink deposition. Solution processes are therefore a promising group of

techniques for low cost, large area, high throughput roll-to-roll material deposition. Currently, a variety of solution deposition techniques are available, including spin-coating, inkjet printing, spray-coating, dip-coating, screen printing, blade coating and gravure printing [16], [19].

Solution processes are suitable for inorganic multicomponent oxide thin film deposition. Since oxides are the final products, most of the process steps, especially the film drying and formation step (step 3), can be conducted in air. Another advantage of using solution processes is that these processes allow flexible control of elemental stoichiometry and preserve chemical homogeneity, ideal for alloy materials [16], [20].

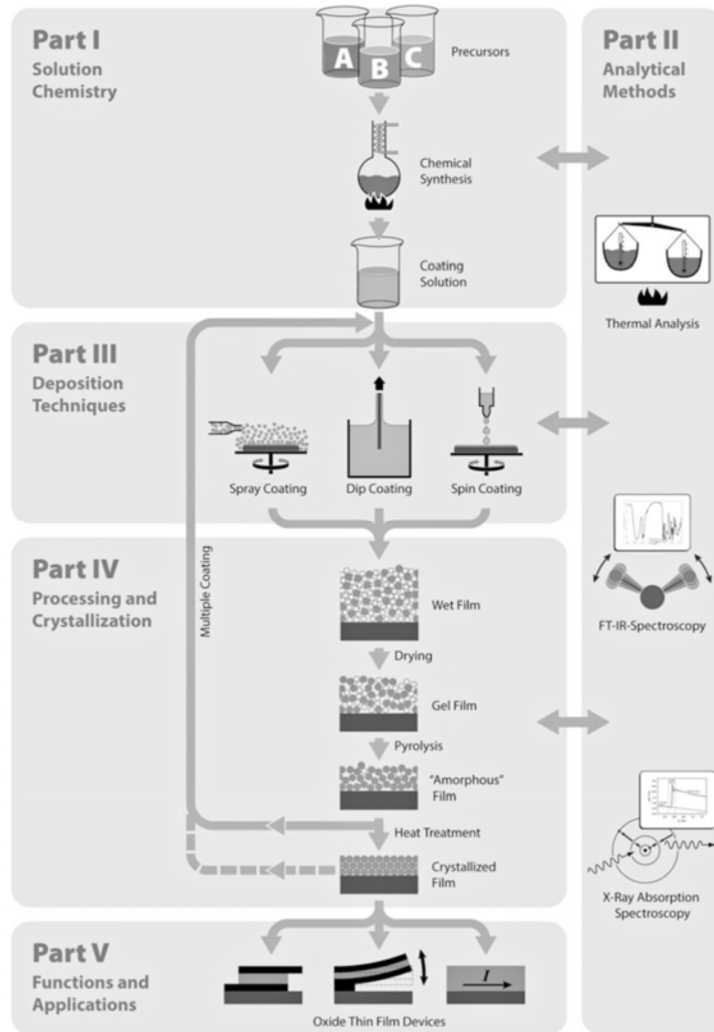


Figure 1-3. Typical steps of a solution-based thin film deposition process. From [16].

To synthesize the coating solutions for oxides, multiple routes can be taken. The most common precursors are metal alkoxides (M-$(OR)_z$) and metal salts (chlorides, acetates, nitrates, sulfides and so on). These precursors can be dissolved in various solvents, such as water or organic liquids (usually an alcohol). Historically, metal alkoxides, derivatives of alcohols, have been the most popular precursors due to their high solubility in organic solvents, high chemical reactivity to form metal oxides, and ease of purification [16], [20].

However, metal alkoxides are usually more expensive and relatively difficult to handle due to their high reactivity and thus short shelf-life. (They are usually hygroscopic). Metal acetates (or other metal carboxylates) are also soluble in many solvents, and are fairly inexpensive, stable and non-toxic. Therefore acetates are also widely used [21]–[27].

When acetates are dissolved and mixed in organic solvents, they could go through a series of chemical reactions. For example, the carboxyl group can either chelate with one metal ion, or bond to two different metal ions, as shown in Figure 1-4 (a) [16]. The stabilizers used in the solutions to further prevent metal salt recrystallization, premature hydrolysis and precipitation, usually alkanolamines, can also bond to a single metal ion or multiple metal ions [20]. The precursors can also go through alcohol interchange (ligand exchange) with organic solvents and partial hydrolysis to form complexes, where different precursors are well mixed on the molecular level [16], [20]. These chemical reactions make solution processes suitable for multi-component oxides.

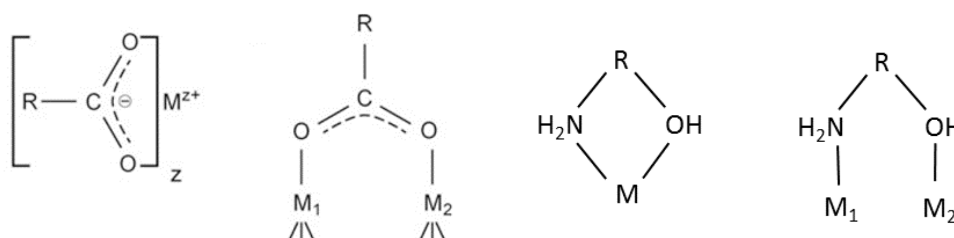
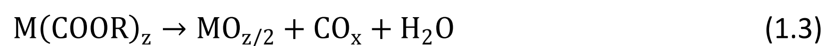


Figure 1-4. Different bonding modes between metal and (a) carboxylate groups [16], and (b) alkanolamines. The two oxygen atoms in a carboxyl group (R-COO) can either bond to the same metal atom M, or bond to different metal atoms M_1 and M_2 in a solution. The coordination also applies to metal-alkanolamines (HO-R-N_2H) [16], [20]. These complexes help with molecular level mixing in a solution process of multi-component metal oxide.

After dispensing the solutions onto the substrate, the sol is turned into xerogel (wet film) through solvent evaporation and gelation (Figure 1-5). The xerogel is further sintered to form a dense film. During these steps, heat or another form of energy is applied to induce gelation, hydrolysis, condensation and thermal decomposition. Reactions 1.1 to 1.3 illustrate the thermal decomposition process where *M* is the metal, *R* is the radical group, and the metal oxide is $MO_{z/2}$. For zinc acetate dihydrate, *M* = Zn, *R* = CH_3, and *z* = 2. Other, more complex reactions such as ether and ester elimination, can also occur.

$$\mathrm{M(COOR)_z + H_2O \rightarrow M(OH)_z + RCOOH} \quad (1.1)$$

$$\mathrm{M(OH)_z \rightarrow MO_{z/2} + H_2O} \quad (1.2)$$



$$\mathrm{M(COOR)_z \rightarrow MO_{z/2} + CO_x + H_2O} \quad (1.3)$$

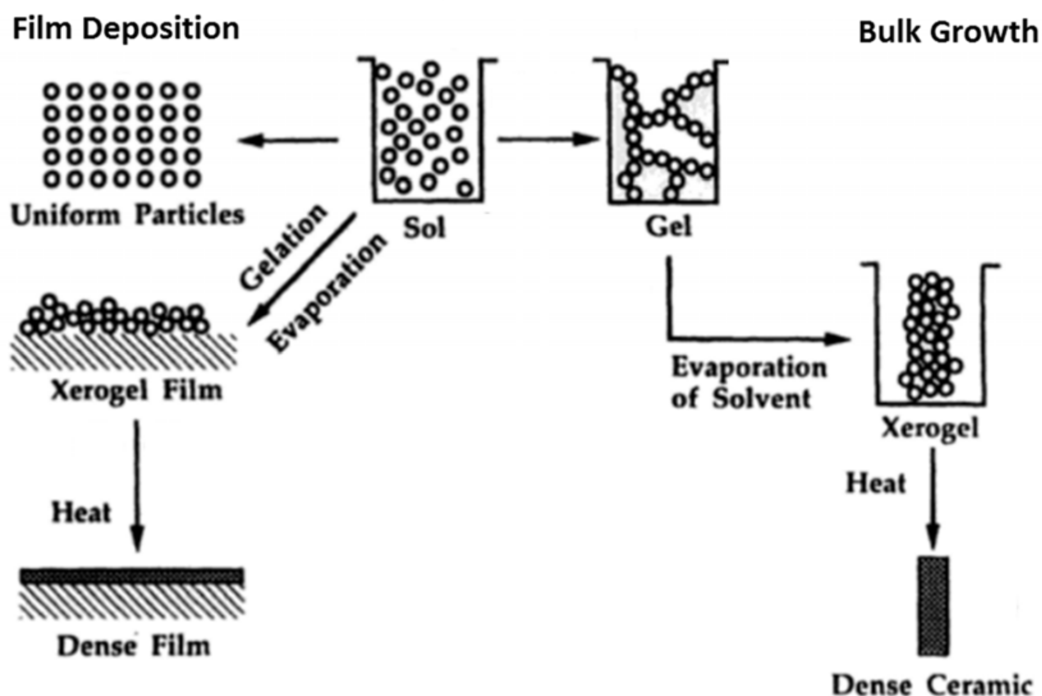


Figure 1-5. Schematic of sol-gel processes for thin films and bulk materials. Adapted from [28].

The solution process of metal oxides dates back to the mid-1900s driven by the development of ferroelectric oxide thin film devices for various applications such as memory and piezoelectric actuators, and also by thin-film coatings [16], [20]. Nowadays, the number of oxide materials that can be deposited by solution processes has expanded extensively, with almost all the oxides mentioned above possible. New solution-based deposition technologies are being developed and some of the solution-processed materials have already been used commercially [29]–[31]. For emerging multi-component oxide materials deposited by sol-gel process as well as devices made from these oxides, the influence of process conditions on materials properties and device performance are key areas of research.

1.4 Scandium and yttrium alloyed oxide materials

Scandium (Sc) and yttrium (Y) are two Group IIIB (Group 3 in the new column numbering system) and Period 4 and 5 transition metals, as shown in the periodic table in Figure 1-6. These two elements are categorized as rare earth elements together with the lanthanides, because they are often found in the same ore deposits, and they have similar atomic structures and chemical properties as the lanthanides. The chemical properties of Sc and Y are determined by their electronic configuration, which for Sc is $[1s^2 2s^2 2p^6 3s^2 3p^6] 3d^1 4s^2$ and for Y is $[1s^2 2s^2 2p^6 3s^2 3p^6 3d^{10} 4s^2 4d^6] 4d^1 5s^2$. When forming ionic compounds, both elements lose their $(n)d^1 (n+1)s^2$ electrons and become triply charged Sc^{3+} and Y^{3+} ions.

Figure 1-6. Periodic table. From [32].

The three valence electrons give the binary compounds Sc_2O_3 and Y_2O_3 cubic bixbyite crystal structures, where the Sc and Y atoms are 6-fold coordinated and the O atoms are 4-fold coordinated, similar to the situation for In_2O_3. Sc_2O_3 and Y_2O_3 are important functional materials with unique optical, chemical, mechanical and electrical properties. Electrically, they are both high-*k* insulators, because of their strong ionic polarization. With a high dielectric constant and a large optical band gap, they are possible candidates for high quality high-*k* dielectric materials.

Besides binary oxides, both Sc and Y play important roles in a number of multi-component oxides. The atomic structures of Sc and Y make them crucial components in the high temperature superconductor such as yttrium barium copper oxide, fast oxide ion conductors such as yttria- or scandia-stabilized zirconia, phosphors such as rare-earth

metal doped Y_2O_3 and solid-state laser materials such as Nd:YAG , where they can act as host material, structural stabilizer or stoichiometry controller [33]–[35].

Sc and Y have a very strong oxygen affinity compared with other common metals. Oxygen affinity can be described by various parameters, including the enthalpy of formation, Gibbs free energy and total lattice potential energy of the oxide. These values are tabulated in Table 1-1 for common metal oxides. The enthalpies of formation of several oxides are visualized in Figure 1-7. The enthalpies of formation and Gibbs free energies of yttrium and scandium oxide are large negative quantities and the oxide lattice enthalpy (lattice potential energy) is a large positive value. This means that Y_2O_3 and Sc_2O_3 are energetically easy to form and their formation is thermodynamically favorable compared to other metal oxides [36], [37].

Due to their strong oxygen affinity, Sc and Y can possibly be used as stabilizing elements, or oxygen getters, in transparent amorphous oxide semiconductors (TAOS) [37], [38], [38]–[42], by reducing the amount of oxygen vacancy-related defects in TAOS. TAOS, which will be further introduced in Chapter 2, 3 and 4, are a group of multi-component semiconducting oxide materials that usually contains two or more metal oxide components including In_2O_3, ZnO, SnO_2 and Ga_2O_3. TAOS are suitable for high performance flat panel display applications due to their high mobility compared to conventional hydrogenated amorphous Si. Their high mobility, wide bandgap/optical transparency and simplicity of deposition make TAOS suitable for potential applications such as RFID and sensing systems. As mentioned before, TAOS have oxygen vacancy-related defect states that can compromise electrical performance, especially threshold

voltage stability under electrical stress. It may be possible to reduce or eliminate these sub-gap states in TAOS by alloying with Sc and/or Y.

Table 1-1 also lists the metal solid-state energies (SSEs), which for cations is defined as the average electron affinity for their binary compounds [43]. Cations with SSE values close to the universal energy reference of -4.5eV can act as electron donors (dopants) whereas metals with SSE significantly above -4.5eV will act as free-electron suppressors. For example, Sn and In have SSE of -4.4 and -4.6eV, respectively, indicating their important role in free-carrier generation in indium tin oxide, a transparent conducting oxide, and in semiconductor metal oxides such as In-Zn-O or Zn-Sn-O. For comparison, Zn and Ga have SSE values of -4.0 and -3.9 eV, respectively. This is consistent with our understanding of metal oxide band structure: the conduction band in these materials is formed via the spherical *s* orbitals. The larger *5s* metal orbitals of In and Sn, compared to the Zn and Ga *4s* orbitals, improves electron conduction via greater orbital overlap (Figure 2-1) [44]. In nano-crystalline zinc oxide, column IIIA (column 13) elements such as Ga and Al (SSE = -3.9eV and -2.1 eV, respectively) have been successfully used as *n*-type dopants. With three valence electrons, Y ([Ar]$3d^1 4s^2$) and Sc ([Kr]$4d^1 5s^2$) have SSE values of -3.6 and -3.4 eV, indicating their possible role as electron donors in ZnO-based materials.

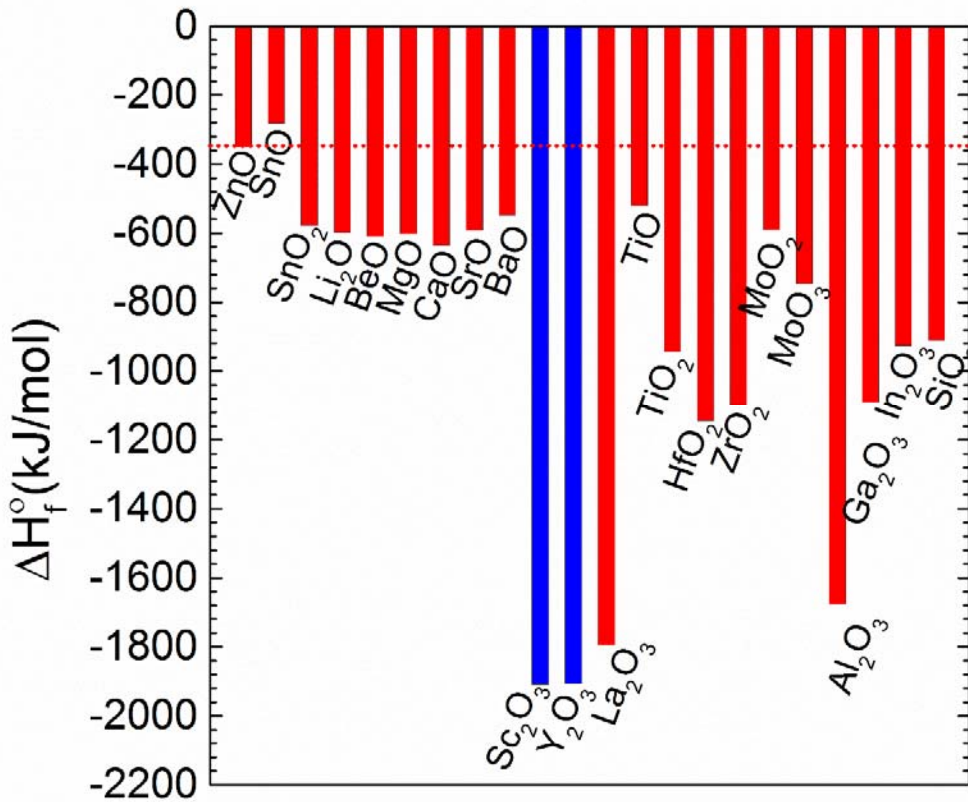


Figure 1-7. Enthalpy of formation of oxides of various metals. Sc_2O_3 and Y_2O_3 have large negative enthalpies, indicating their strong oxygen affinity. From [45].

Finally, based on their strong oxygen affinity and ability to form high-*k* insulators, Y and Sc dopants in ZnO-based materials could also form insulating or charge trapping structures that could hinder charge transport.

Table 1-1. Oxide enthalpy of formation, Gibbs free energy, total lattice potential energy of various metal oxides and atomic solid state energy of the metal [46][47]

Oxide	Enthalpy of formation (kJ/mol)	Gibbs free energy at 298.15K (kJ/mol)	Total lattice potential energy (kJ/mol)	Atomic solid state energy of the metal element (eV)
ZnO	-350.5	-320.5	4,142	-4.0
SnO	-280.7	-251.9	3,652	-4.4
SnO_2	-577.6	-515.8	11,807	
Li_2O	-597.9	-561.2	2,779	-0.8
BeO	-609.4	-580.1	4,514	
MgO	-601.6	-569.3	3,795	-3.1
CaO	-634.9	-603.3	3,414	-1.6
SrO	-592.0	-561.9	3,217	-1.6
BaO	-548.0	-520.3	3,029	-1.0
Sc_2O_3	-1,908.8	-1,819.4	13,557	-3.4
Y_2O_3	-1,905.3	-1,816.7	12,705	-3.6
La_2O_3	-1,793.7	-1,705.8	12,452	-2.5
TiO	-519.7	-495.0	3,832	-4.2
TiO_2 (rutile)	-944.0	-888.8	12,150	
HfO_2	-1,144.7	-1027.2		-2.0
ZrO_2	-1,097.5	-1,039.7	11,188	-2.6
MoO_2	-588.9	-533.0	11,648	-2.2
MoO_3	-745.1	-668.0		
Al_2O_3 (s-alpha corundum)	-1,675.7	-1,582.3	15,916	-2.1
Ga_2O_3	-1,089.1	-998.3	15,590	-3.9
In_2O_3	-925.8	-830.7	13,928	-4.6
SiO_2	-910.7	-856.3	13,125	-2.3

In a word, with all these properties, Sc and Y can have one or multiple roles in different oxides, as summarized in Figure 1-8. Being able to identify these roles is crucial for multi-component oxide material and device design.

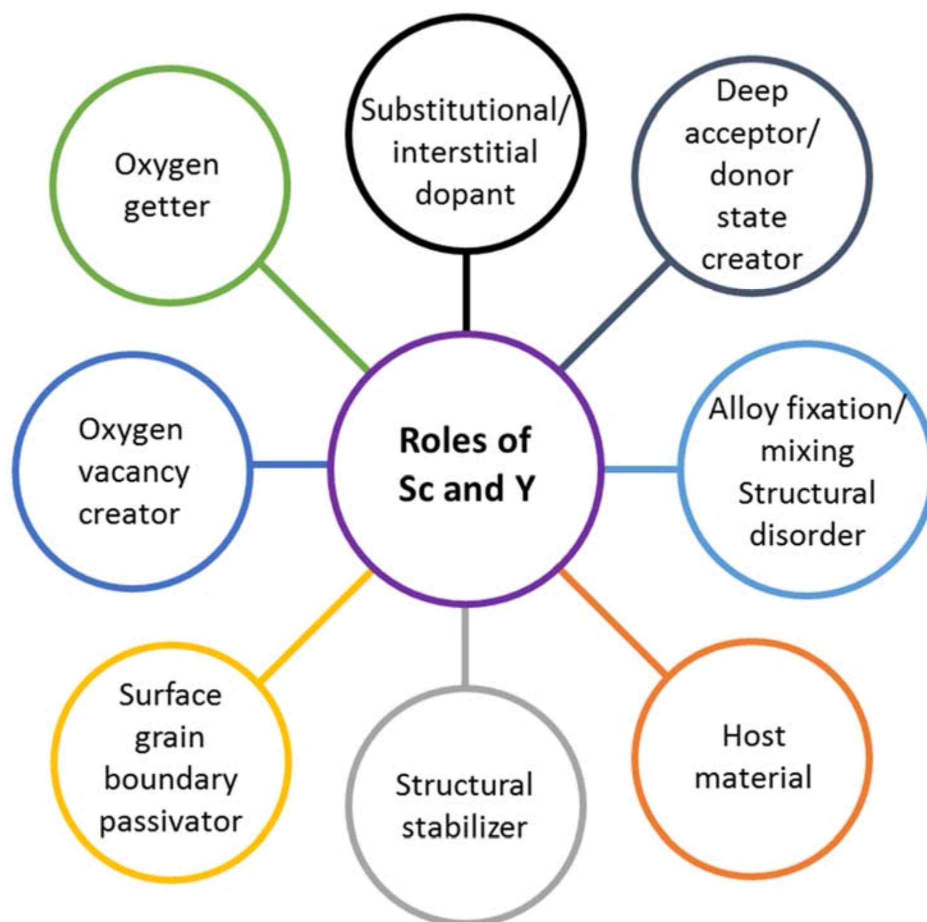


Figure 1-8. Roles of Sc and Y in oxide electronic materials.

1.5 Thesis Goals and Objectives

Since Sc and Y can play multiple, complicated roles in oxide films, in this thesis we seek a clear understanding of these roles in a variety of oxide-based electronic materials, including semiconductors (TAOS), transparent conducting oxides (doped ZnO), and dielectrics (Y-Sc-O alloys), in order to facilitate future design, fabrication, and use of these and other related materials in solution-processed electronics.

The research objectives of this thesis are:

- to study the influence of process conditions on the electrical properties and charge transport of solution-processed ZTO,
- to optimize solution-processed ZTO TFTs for baseline device structures,
- to identify the effect of Y doping in solution-processed Y:ZTO on transistor performance and stress stability,
- to clarify the roles of Sc and Y in solution-processed Sc:ZnO and Y:ZnO,
- and to identify the effect of alloying Sc_2O_3 and Y_2O_3 on the dielectric properties and thermal stability.

This thesis aims to demonstrate several solution-processed alloy oxide electronic materials that incorporate the rare earth metals Sc and Y, to study material properties and device performance as a function of Sc and Y concentration, and to thereby determine the roles of Sc and Y in these materials. For simplicity, spin-coating was used for oxide thin film depositions. The materials synthesized, devices fabricated and mechanisms/physics studied are summarized in Table 1-2.

Table 1-2. A summary of the materials, devices and physics studied in the thesis.

	Semiconductors	Conductors	Insulator
Materials	ZTO Sc:ZTO Y:ZTO	ZnO Sc:ZnO Y:ZnO Al:ZnO	Y-Sc-O
Devices	TFTs	(none)	MIM and MIS caps
Mechanisms/ Physics	• Semiconductor properties • Charge transport • Contact properties	• Transparency • Conductor properties • Doping effects	• Dielectric properties • Dielectric relaxation • Interface properties • Thermal stability

	• Stress stability and passivation	• Grain boundary passivation • Surface depletion	

1.6 Thesis Overview

Chapter 2 presents a baseline solution process for Zn-Sn-O (ZTO) TFTs. The process and material stoichiometry are optimized. Cryogenic TFT measurements are used to explain the band structure and charge transport of the ZTO semiconductor.

Chapter 3 studies the contact resistance of various metallic materials to solution-processed ZTO, in order to form high-quality source/drain ohmic contacts.

Chapter 4 discusses the stability of solution-processed ZTO TFTs under various conditions, the possible origins of the instability, and the effects of Y on Y:ZTO TFT device performance and stability.

Chapter 5 describes the multiple roles of Sc and Y in solution-processed Sc:ZnO and Y:ZnO in the context of transparent conductive oxides. These roles were identified by Hall measurements as well as SEM, XPS and CAFM.

Chapter 6 introduces solution-processed ternary alloy Y-Sc-O as high-k dielectrics. The effects of alloying Y_2O_3 with Sc_2O_3 on dielectric properties and thermal stability are studied with different film stoichiometry.

Chapter 7 concludes the thesis and suggests future research work to build upon this thesis.

Chapter 2 Solution-processed zinc tin oxide semiconductor

2.1 Introduction

As the display industry pushes toward larger, faster, and higher-resolution displays, the performance demands on the thin film transistor (TFT) backplane are rapidly increasing. New technologies such as thin flexible substrates for lightweight or curved design, active matrix organic light emitting diodes (AMOLEDs) for color and brightness, and fully transparent displays for windows and heads-up display applications have even more stringent backplane requirements. The currently dominant materials, amorphous and poly-crystalline silicon, suffer from lack of transparency, marginal electronic performance and poor threshold voltage stability (amorphous silicon), and require vacuum-deposition fabrication which may lead to uniformity issues over large areas (poly-Si) [48].

Recently, transparent amorphous oxide semiconductors (TAOS), namely ZnO-based materials, have drawn significant interest for these applications. In *n*-type zinc oxide alloys, the metal *s*-orbitals form the conduction band. Due to the *s*-orbital's spherical symmetry, good electron conduction and high mobility can be achieved even for amorphous films [49], as shown in Figure 2-1 (a) and (b). These materials, particularly amorphous indium gallium zinc oxide (IGZO), have already demonstrated their capability for next generation displays [50]–[53]. However, the price of indium is rapidly increasing

due to its scarcity and widespread use for indium tin oxide (ITO) transparent conductors [54], [55], driving the need for other high performance TAOS alloys. Zinc tin oxide (ZTO) is one promising alternative. ZTO can be deposited in vacuum, typically by RF magnetron sputtering and pulsed laser deposition [56]–[58]. However, these vacuum deposition techniques are costly since they require a high vacuum system and generally waste a large portion of the raw materials. By avoiding these drawbacks, solution processes are very attractive for further lowering the cost of large area material deposition. Solution processes based on liquid inks, such as spin-coating and ink jet printing, have been used for ZTO deposition using metal chlorides or metal acetates or a combination of these precursors, to demonstrate material and device feasibility [59]–[67]. For solution-processed ZTO thin film transistors (TFT), the highest reported [68] field effective mobility is 27.3 $cm^2V^{-1}s^{-1}$.

Since the successful demonstration of TAOS, the application of these materials have been rapidly moving beyond display backplanes toward new fields such as arrays of sensors and actuators, distributed energy harvesting, and wireless communications systems [69]–[72]. The need for large-area and high-frequency digital and analog circuits has also created interest in TAOS materials, not only because of their high electron mobility in the amorphous state compared to amorphous silicon or organic semiconductors [73], but also their large optical band gap of approximately 3.4eV and low leakage current.

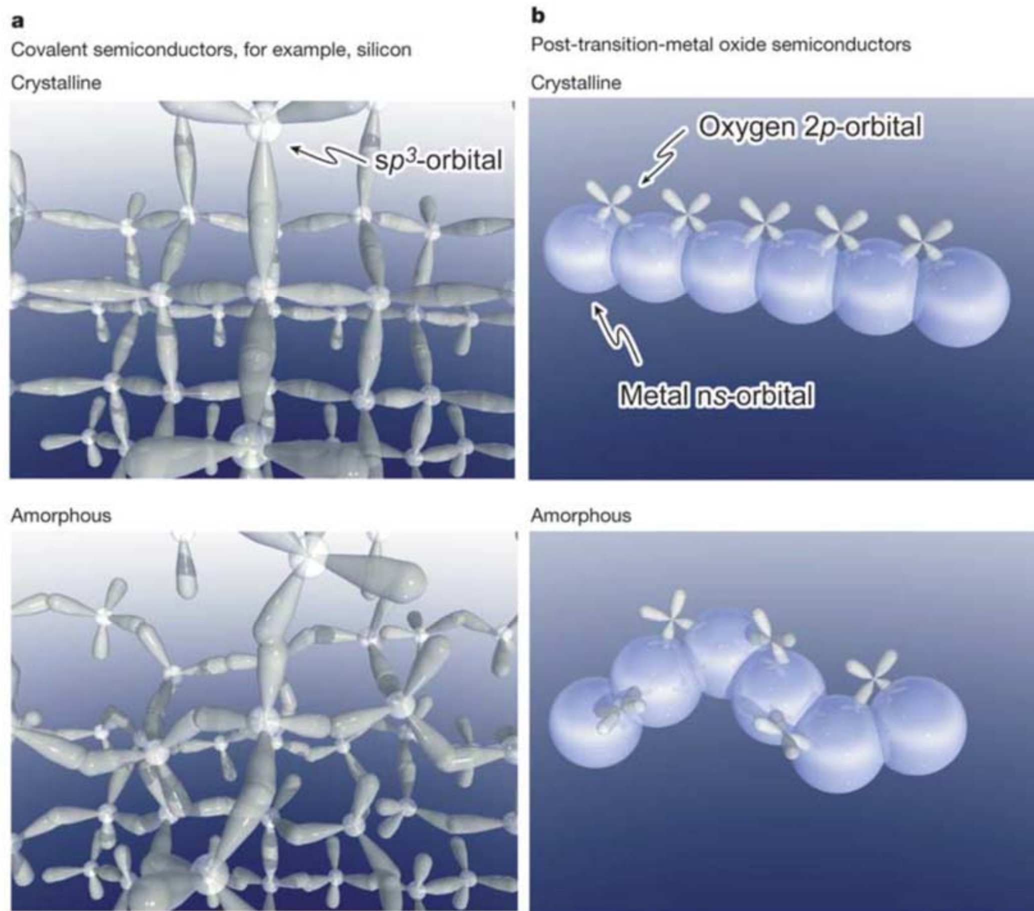


Figure 2-1. (a) Schematic of conduction paths in a single crystalline and amorphous Si, showing that the amorphous state severely disrupts the conduction paths. (b) Schematic of conduction paths in a single crystalline and amorphous transition metal oxide semiconductor, showing that the amorphous state does not severely disrupt the conduction paths. From [49].

The charge transport mechanisms of these materials and the band structure and origin of sub-conduction band tail states are still being investigated. These properties are crucial to successful device simulation and device stability studies [74]–[79]. A generic band structure of IGZO is shown in Figure 2-2. Charge transport in these disordered materials depends greatly on the band structure and the position of the Fermi level. The charge

transport can be described using two main categories: transport via extended (delocalized) states and transport via localized states. For transport via extended states, i.e. band-like transport, the mobile charges move at energies above the mobility edge that separates localized states and extended states, similar to the charge transport in single crystalline semiconductors (Figure 2-3 (d)). In this case the conductivity usually exhibits an Arrhenius temperature dependence and a high mobility (> 1 $cm^2 \cdot V^{-1} \cdot s^{-1}$).[80] Charges can also transported via localized states inside the band gap by hopping, percolation, and/or Poole-Frenkel mechanisms (multiple trap and release), as shown in Figure 2-3. Localized transport typically has a strongly temperature-dependent charge-carrier mobility. For example, variable-range hopping conductivity is proportional to exp ($-T^{-1/4}$). Localized carriers typically exhibit a field-dependent mobility and anomalous transient response [81]. Percolation conduction is an extreme case of variable range hopping, where the hopping distances between charges marginally overlap, forming long range conduction paths [81]. An illustration of percolation is shown in Figure 2-4.

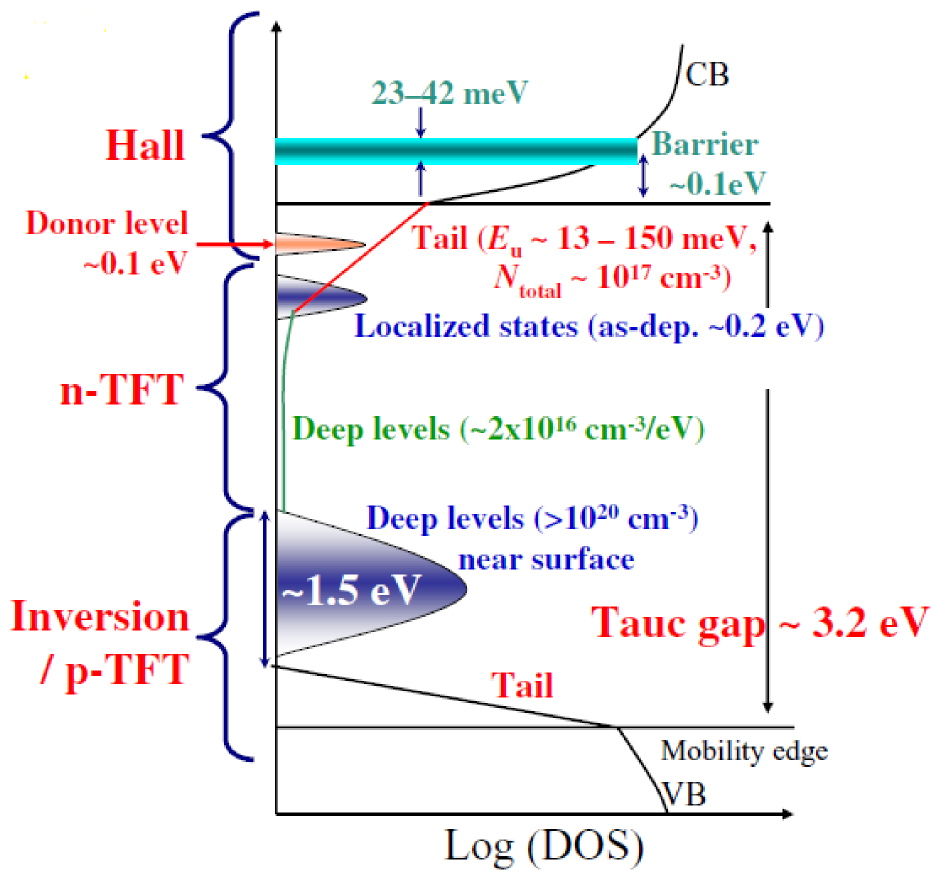


Figure 2-2. A generic band structure of InGaZnO. From [48].

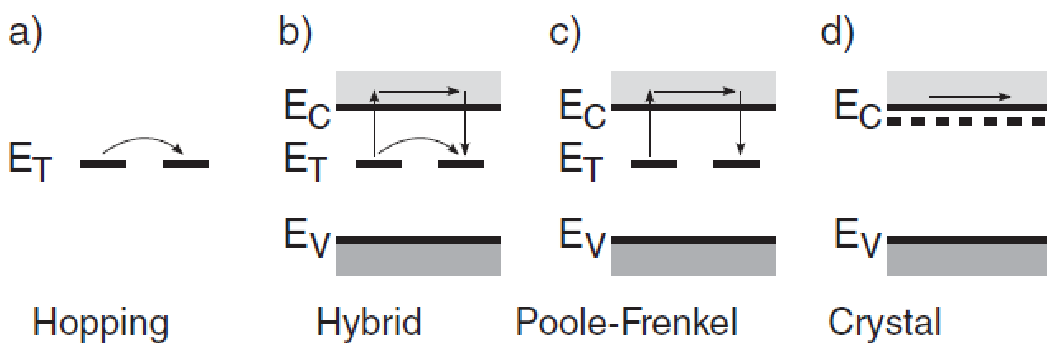


Figure 2-3. Common charge transport theories in an *n*-type disordered materials: (a) hopping/percolation transport, (b) hybrid of hopping and Poole-Frenkel transport, (c) Poole-Frenkel (multiple trap and release) transport, and (d) band-like transport. [81]

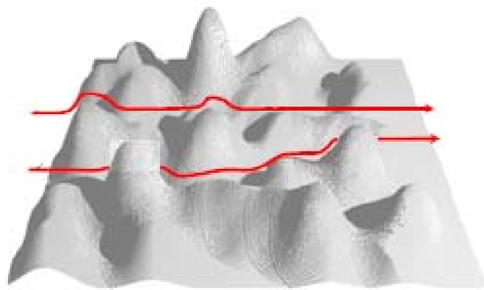


Figure 2-4. Percolation conduction of charges around energy barriers. From [48].

For both single-crystal and amorphous IGZO, percolation conduction over potential barriers in the vicinity of the conduction band edge has been proposed [82]–[85]. There have been limited studies of charge carrier transport in ZTO [68], and few studies of solution-processed metal oxides of any type. It is not yet established whether the transport mechanism and donor levels are similar to those of vacuum-deposited amorphous IGZO. Furthermore, it is well known for vacuum-deposited IGZO and ZTO that process conditions and chemical composition have significant effects on the room temperature performance of TFTs [60], [86]–[88], but the source of these variations, i.e. changes in donor or defect state energy levels, is not well understood. Here, cryogenic measurements of solution-processed ZTO thin film transistors were used to study the influence of ternary alloy composition and fabrication process variables on charge transport and band tail states. The results show that the carrier transport mechanism in ZTO at low temperature is similar to that of IGZO, percolation conduction, and that the location of donor like states and the shape of conduction band tail states can be

engineered by varying annealing temperature of the solution process and varying stoichiometric ratio of the material to obtain high-quality films.

2.2 Experimental

Bottom gate top contact ZTO TFTs are fabricated. Heavily doped *p*-type Si wafer is used as the gate electrode, with a 200-nm thermally grown SiO_2 layer as the gate dielectric. Using a process similar to that in Ref. [60], the active layer is deposited by spin coating a metal acetate precursor solution and subsequent annealing. The solution is prepared by dissolving zinc acetate dihydrate and tin (II) acetate in 2-methoxyethanol, with a total metal precursor concentration of 0.5 M and various zinc to tin ratios, stirring the mixture at room temperature for 12 h, and finally filtering the mixture through 0.22-μm syringe filter before spin coating. Here, the Zn:Sn ratio refers to the atomic metal ratio in the liquid ink. The solution is spin-coated at a speed of 3000 rpm for 30 s. The samples with zinc to tin ratio of 7:3 are annealed at different temperatures varying from 480 to 300°C in air with a controlled relative humidity of 20% for 1 h, while samples with other zinc to tin ratios are all annealed at 480 °C. This temperature is high enough to ensure complete decomposition of the molecular precursors [60] while also being low enough to avoid crystallization of the ZTO film.32 We find that low relative humidity of the anneal ambient is critical to achieve good device performance. Multiple layers are spin-coated onto the samples to increase the active layer thickness. After each spin-coating step, the sample is annealed at the given anneal temperature in air at 20% relative humidity for 1 min to begin the drying process. Upon spinning the final layer, the sample is annealed under the same conditions for 1 h. Source/drain electrodes of 100 nm Al are then deposited by

thermal evaporation through a shadow mask. The channel width/length of the transistor is 3000 lm/200 lm. The active layer is patterned by wet etch using dilute hydrochloric acid (1:100). The device structure is shown in Figure 2-5.

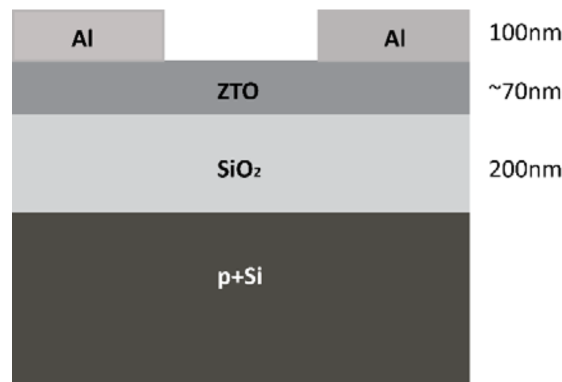


Figure 2-5. Cross-sectional structure of ZTO TFT.

Film morphology is investigated using scanning electron microscopy (SEM), transmission electron microscopy (TEM), selected area electron diffraction (SAED), and atomic force microscopy (AFM). The nominal TFT electrical performance is tested in ambient air and light using an HP4155A semiconductor parameter analyzer (Agilent Technologies, Inc., Santa Clara, CA). Low-temperature current–voltage TFT measurements are conducted using a Lakeshore FWP6 vacuum probe station (Lake Shore Cryogenics, Inc., Westerville, OH) cooled by continuous flow of liquid nitrogen. The substrate temperature is varied from 77 to 300 K using a Lakeshore 340 temperature controller (Lake Shore Cryogenics, Inc., Westerville, OH).

2.3 Results and discussions

The room temperature transfer curves of drain current versus gate voltage for different Zn to Sn ratios and different annealing temperatures are shown in Figure 2-6 (a)

and (b), and the extracted transistor parameters are listed in Table 2-1. The best performance is seen for ink [Zn]:[Sn] ratios of 7:3 and anneal temperature of 480˚C. Samples with higher Zn content exhibit lower mobility and reduced on/off current ratios. When only zinc precursor is used, the resulting film is conductive, exhibiting very weak field-effect. This may be due to the formation of nano-crystallites in the binary film. Lower [Zn]:[Sn] ratios show larger sub-threshold slopes and lower mobility. Other work on solution-processed ZTO made from acetates has similarly found that the optimal [Zn]:[Sn] ratio is 7:3 with mobility of 1.1 cm^2/V-s with a maximum anneal temperature of 500˚C [60], [63]. The higher mobility of our optimal devices, 2.7 cm^2/V-s, may be due to the low humidity anneal ambient utilized. The device performance also depends on anneal temperature as shown in Figure 2-6 (b). The higher the anneal temperature, the greater the mobility. Devices annealed at 450 ˚C or greater show mobility of ~2 cm^2/V-s or more. Transistors prepared at 350˚C or less are characterized by low on/off current ratios, likely due to incomplete reaction of the precursors [60]. An output curve for the optimum device is shown in the Figure 2-6 (a) inset. Clear linear and saturation regions are observed.

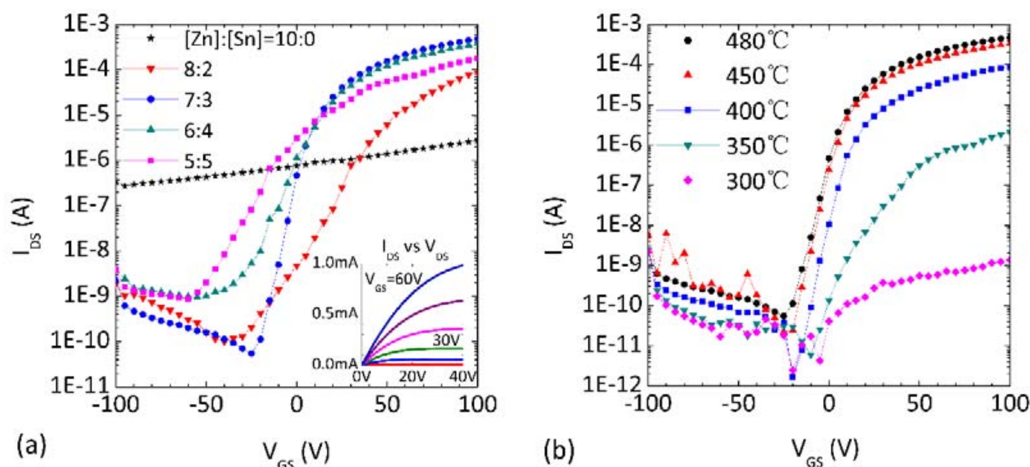
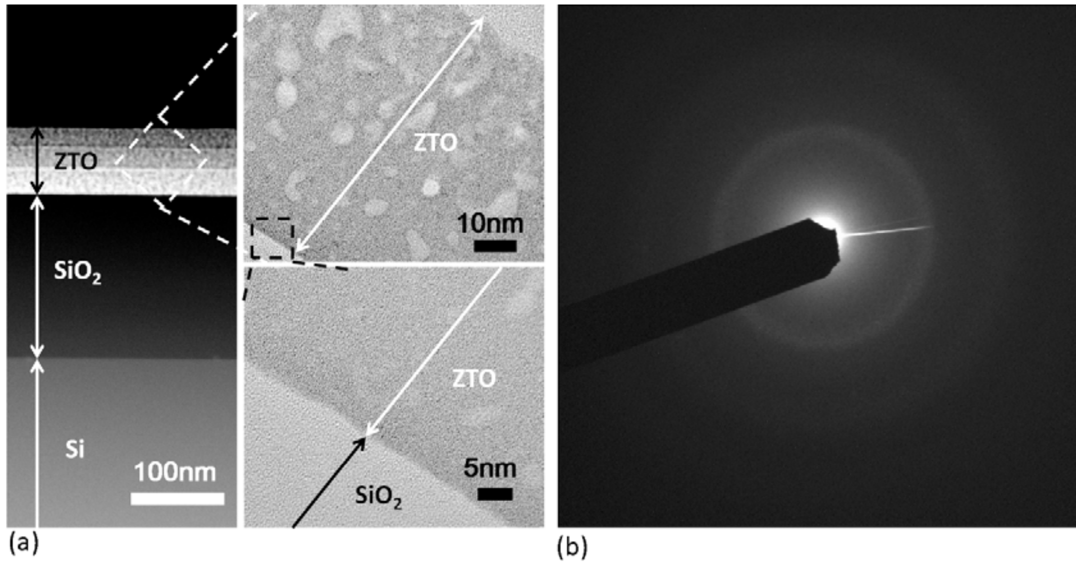


Figure 2-6. (a) Transfer curves of ZTO TFT with different solution precursor [Zn]:[Sn] ratios, annealed at 480˚C. Inset, an output curve of a ZTO TFT with precursor ratio [Zn]:[Sn]=7:3, annealed at 480˚C, with V_{GS}=60V, 50V, 40V, 30V, 20V, 10V and 0V. (b) Transfer curves of ZTO TFT with precursor [Zn]:[Sn]=7:3, annealed at different temperatures. All transfer curves were taken at V_{DS}=5V.

The cross-sectional view of the optimal ZTO solution-processed film obtained by transmission electron microscopy (TEM) is shown in Figure 2-7 (a). The total film thickness for three layers is about 72nm. The films are non-porous, with very fine texturing on the order of ~5nm. The surface of ZTO is characterized by AFM and shown in Figure 2-7 (c). The film is very smooth, with *rms* surface roughness of 1.5 nm. The observed texturing may be due to solvent evaporation dynamics during film formation. Selected area electron diffraction (SAED) was also performed on the TEM samples, and the diffraction pattern is shown in Figure 2-7 (b). The diffraction results and TEM images confirm that the ZTO film is amorphous after 480˚C annealing.



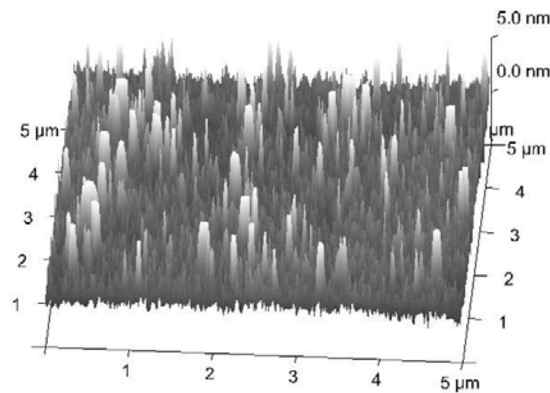


Figure 2-7. (a) Cross-sectional TEM views of a three-layer ZTO film. The lower right image shows the amorphous and nonporous ZTO film at its interface with SiO_2. (b) SAED of the ZTO layer, indicating amorphous structure. (c) AFM image of the ZTO film surface.

Table 2-1. Electrical parameters of ZTO TFTs fabricated at different annealing temperatures or from different zinc to tin ink ratio.

Annealing temperature(˚C)	[Zn]:[Sn] ink ratio	Linear mobility μ_{lin} ($cm^2/(V{\cdot}s)$)	Turn on voltage V_{ON}(V)	On-off current ratio	Sub-threshold slope SS (V/dec)
480	10:0	0.01	N/A	N/A	N/A
480	8:2	0.97	-30	~1×10^6	15.6
480	7:3	2.71	-23	~5×10^6	4.4
480	6:4	2.26	-42	~4×10^5	6.8
480	5:5	1.28	-61	~2×10^5	7.7

300	7:3	9.5e-6	-6	~400	N/A
350	7:3	0.02	-6	~2×10^{4}	13.8
400	7:3	0.53	-16	~5×10^{6}	5.0
450	7:3	1.95	-19	~1.5×10^{7}	4.4

Figure 2-8 (a) shows the transistor transfer curves for temperatures ranging from 300K to 77K. As temperature increases, the threshold voltage shifts to more negative values. This effect has been previously been observed experimentally and confirmed by simulation for ZTO and IGZO by other groups [68], [77], [89]–[91]. It is thought that the threshold shift is due to thermal excitation of electrons from localized traps in the conduction band tail into higher energy mobile states. For our optimal device, the threshold voltage shift only occurs for 160K-300K; for lower temperatures the turn-on voltage does not significantly change, indicating that for certain localized trap states the trapped electrons require k_BT of more than approximately 15meV to escape the trap. The effective mobility, calculated from transconductance, increases as gate voltage increases and as temperature increases, as shown in Figure 2-8 (b). The effective mobility gradually plateaus for high V_{GS}-V_{ON} values.

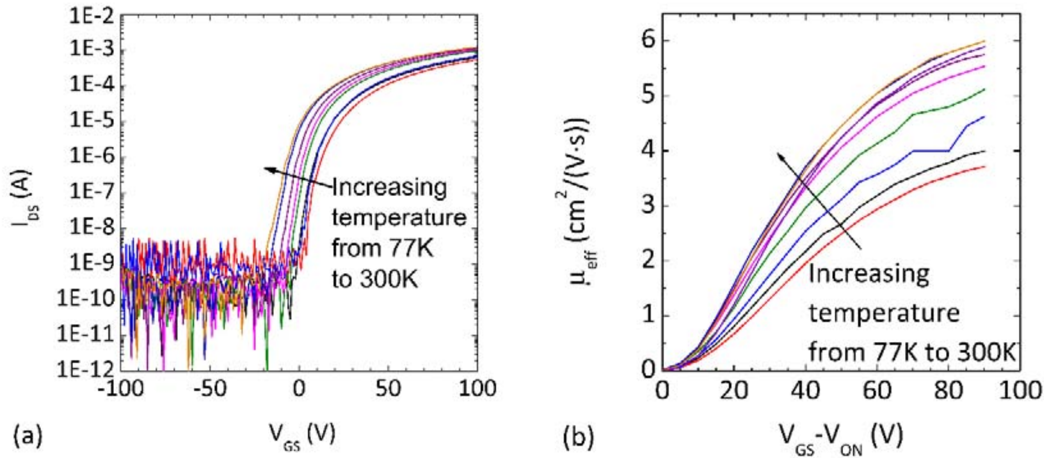


Figure 2-8. (a) Measured transfer curves at various temperatures for a transistor with W/L = 3000 μm/200 μm on a sample with zinc to tin ink ratio of 7:3 and annealed at 480 °C. (b) Effective mobility at various temperatures. For both (a) and (b), curves are shown for 77, 100, 140, 180, 220, 240, 260, 280 and 300 K.

To gain deeper understanding of the band tail structure, the temperature dependence of linear mobility as a function of stoichiometry and anneal temperature was examined. As shown in Figure 2-9 (a) and (b), for all samples mobility increases as temperature increases according to the Arrhenius equation

$$\mu = \mu_0 \exp\left(-\frac{E_A}{k_B T}\right) \tag{2.1}$$

where μ_0 is band transport mobility, E_A is the activation energy, k_B is the Boltzmann constant and T is temperature. The mobility increase is caused by thermally exciting more electrons from the band tail states to energy levels above the mobility edge. The activation energy, E_A, the slope of the semi-log plot of mobility versus temperature, corresponds to the location of the donor-like states below the mobility edge. By fitting the curve from 160K to 280K, the values of E_A are calculated and listed in Table 2-2 and

the fits are shown in Figure 2-9 (a) and (b). All samples have shallow donor-like states that are close to the mobility edge [91], with activation energy smaller than 20meV, i.e. less than k_BT at room temperature. The plot shows that with higher annealing temperature and for zinc to tin ratio near 7:3, the donor-like state is closest to the conduction band edge. This may be due to a reduced amount of disorder or improved bonding in these films [82], [83]. The low E_A value of 7 meV explains the reasonably high room temperature mobility measured.

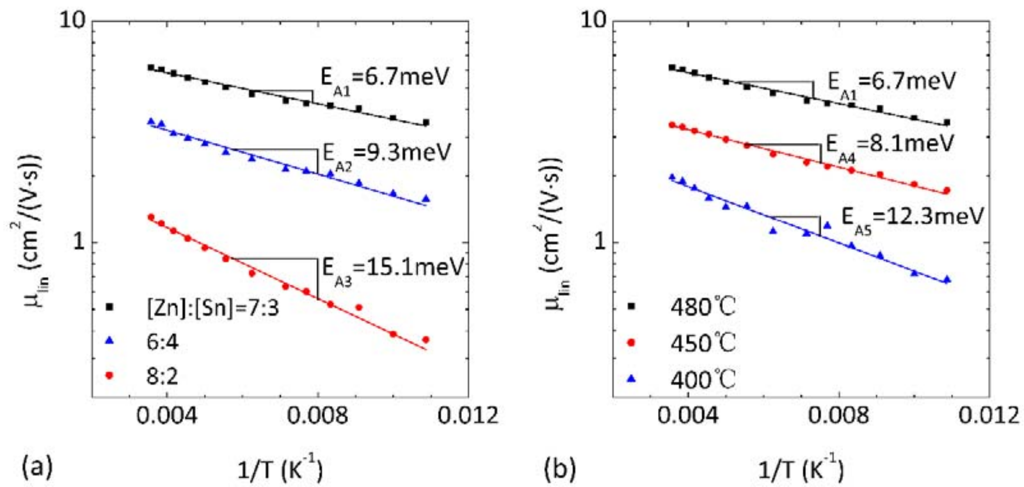


Figure 2-9. (a) Thermal activation energy of mobility vs zinc to tin ratio, for TFTs annealed at 480˚C. (b) Thermal activation energy of mobility vs anneal temperatures, for TFTs with a [Zn]:[Sn] precursor metal ratio of 7:3.

To first order the band tail states can be extracted from low temperature measurement following a technique adapted from [82]. Sheet charge carrier concentration, N, is calculated as

$$N = \frac{1}{q} C_{ox}(V_{GS} - V_{ON}) \tag{2.2}$$

where q is the elementary charge, V_{GS} is the voltage applied between gate and source and V_{ON} is the turn on voltage of the transistor. By plotting the carrier concentration and thermal activation energy of drain current for each V_{GS}-V_{ON} value, the band tail states can be approximated (Figure 2-10 (a)). The curves show exponential decay, which indicates percolation conduction below the mobility edge. The percolation energy is estimated by an exponential decay [82]

$$D(E) = \frac{N}{E_0}\exp\left(\frac{E_C - E}{E_0}\right) \tag{2.3}$$

where $D(E)$ is the density of states, N is the carrier concentration, $E_C - E$ is the difference between the conduction band energy level and the charge carrier energy, here equal to E_A, and E_0 is defined as the percolation energy which characterizes the band tail shape. The percolation energy is also found to be dependent on process and stoichiometric composition of the film.

Table 2-2. Arrhenius energy and percolation energy of ZTO TFTs fabricated at different annealing temperatures or from different zinc to tin ink ratio.

Annealing temperature (°C)	[Zn]:[Sn] ink ratio	Arrhenius energy, E_A (meV)	Percolation energy, E_0 (meV)
480	8:2	15.1	7.2
480	7:3	6.7	3.2
480	6:4	9.3	9.4
450	7:3	8.1	5.5
400	7:3	12.3	13.3

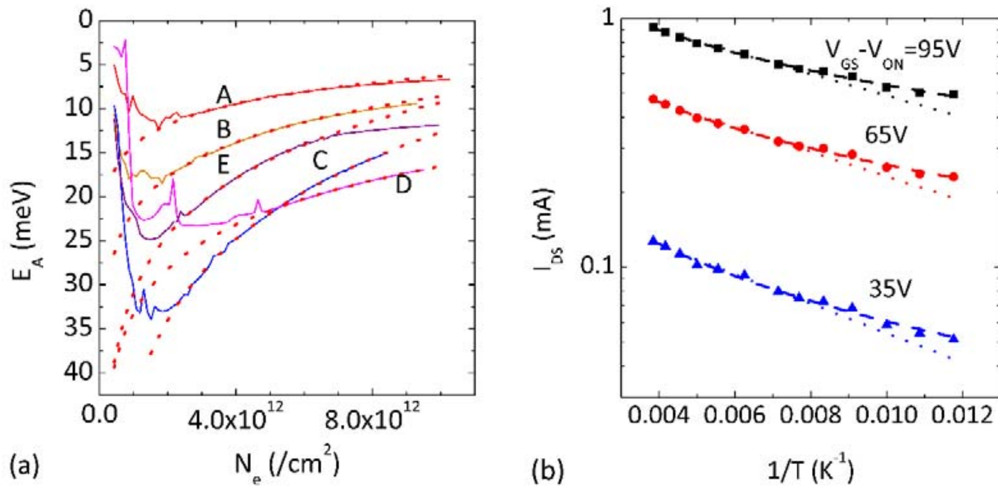


Figure 2-10. (a) Bandtail states extracted from measured data (solid lines) and percolation energy fits (dotted lines) for various TFTs: A, B, and C, have ink ratio of [Zn]:[Sn]=7:3, annealed at 480˚C, 450˚C, and 400˚C, respectively. D, E were annealed at 480˚C with [Zn]:[Sn]=8:2 and [Zn]:[Sn]=6:4, respectively. (b) Comparison of exp(T^{-1}) (dotted) and exp($T^{-1/4}$) (dashed) fit lines to measured drain current vs temperature for various V_{GS}-V_{ON} values, for a ZTO TFT fabricated with 7:3 [Zn]:[Sn] metal ink ratio and annealed at 480˚C.

The optimal samples with maximum annealing temperature and 7:3 zinc to tin ratio exhibit the steepest band tail with a percolation energy of only 3.2meV. Even for a sample annealed at 400˚C, the percolation energy is ~13 meV, much less than that measured for crystalline IGZO (32 meV in [82]). The locations of the donor-like state and percolation energies of different samples are listed in Table 2-2, and the fits are shown in Figure 2-10 (a).

The band structure indicated by these results is shown in Figure 2-11. Well below the conduction band, there are band tail states with a density that increases exponentially with electron energy. These states are filled as bands bend under the application of a gate electric field, and as temperature increases. As the electron energy approaches the

conduction band, the density of states expands to hold a large concentration of carriers at a specific energy level. As has been shown, this energy level, equal to E_A and equivalent to a pinned Fermi level, is determined by film stoichiometry and anneal temperature, and probably also by other variables not explored here. The electron energy cannot rise continuously above this level but must be thermally activated across this small (E_A=7-20meV) gap into mobile, band-like states above the mobility edge. The plateau of the activation energy at high charge carrier concentrations can also be seen in Figure 2-11.

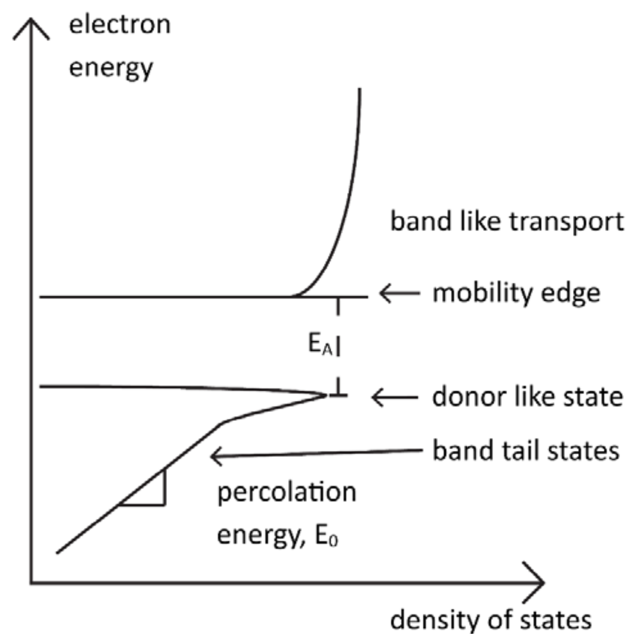


Figure 2-11. Schematic of the band diagram of solution-processed ZTO.

The model just described fits the measured data for temperature from 160K and higher. For lower temperatures, more complex behavior exists. Figure 2-10 (b) illustrates this. Measured drain current is plotted as a function of temperature and is fit using the Arrhenius model (Equation 3.1) and the exponential $T^{-0.25}$ model. The Arrhenius equation

fits well in the medium to room temperature range (dotted lines), while the exponential $T^{-0.25}$ model fits well across the entire temperature range (dashed lines). The latter model can be indicative of a multiple trap and release (MTR) model, which was previously observed for solution-processed ZTO [68], or a Gaussian distribution of percolation states, as observed in single-crystal IGZO [82]. This may indicate that multiple charge transport mechanisms are possible in these materials, and the dominant mechanism may depend on the temperature and charge carrier concentration, with other states frozen out such that they do not play a role in that regime.

2.4 Conclusions

In conclusion, solution processed zinc tin oxide thin film transistors were fabricated with different annealing temperature and different stoichiometric composition. Low temperature current-voltage measurements were done on the transistors and the donor-like states, characterized by a thermal activation energy E_A, and band tail states inside the band gap, characterized by an exponential percolation energy, E_0, show process and composition dependency. An annealing temperature of 480˚C and optimal film stoichiometry ([Zn]:[Sn] ratio in ink of 7:3) brings the donor-like state level closer to the mobility edge (E_A=7meV) and makes the band tail states steeper (E_0=3.2meV). The sharpness of the band tail states correlates directly with the relatively large room temperature electron mobility of 2.7 $cm^2/V\cdot s$. The film also has a large density of states near E_A such that its Fermi energy is pinned inside the bandgap. These charge transport mechanisms observed and the band structure parameters are comparable to or better than those achieved for vacuum-deposited amorphous metal oxide semiconductors,

showing the potential of solution-processed methods to form high-quality inorganic amorphous semiconductor films. More work is needed to explain the physical origin of the observed band tail structure in these materials.

Chapter 3 Contact resistance of zinc tin oxide transistors

3.1 Introduction

3.1.1 Transistor scaling

The needed operating frequency of circuits is constantly increasing. This demands transistors with a higher cut-off frequency f_T. Since f_T of an ideal transistor is inversely proportional to the square of the transistor channel length L, as indicated in Equation 3.1 [92], the channel dimensions of transistors have historically been scaled down with each succeeding CMOS technology node.

$$f_T = \frac{\mu V_{DS}}{2\pi} \cdot \frac{1}{L^2} \tag{3.1}$$

During the scaling down, the electrical field inside the transistors is kept constant by scaling down the device dimensions, scaling down the operating voltage while scaling up the doping concentrations [93]. This way, most device and circuit parameters are under control. However, some of the non-scaling factors start to dominate the device performance when the channel length is short (usually at the sub-micron level), which results in undesired short channel effects. These undesired effects include drain induced barrier lowering (DIBL) and punchthrough, surface scattering, velocity saturation, impact ionization, hot carrier effect, gate induced drain leakage, gate oxide leakage (which will be elaborated in Chapter 6), and source and drain contact resistance. In transparent

amorphous oxide semiconductor (TAOS) thin-film transistors (TFTs), the source and drain (S/D) contact resistance is one of the major issues, as will be discussed in Section 3.1.3.

3.1.2 Source and drain contact resistance in power electronic devices

Besides high speed transistors, high power semiconductor devices also require high quality metal-semiconductor (MS) contacts. In high power electronic applications, diodes and transistors are used as rectifiers and switches. Ideally during the on state of these devices, when the devices are passing high current (typically from 10s mA to 10s kA), the voltage drop across these devices is zero due to a zero on resistance R_{on}, resulting in a zero power loss. However, in real devices, a non-zero R_{on} causes voltage drops across the devices, resulting in power consumption. The on state power loss is directly proportional to R_{on}, i.e. $P_{loss} = V_{on} \cdot I_{on} = I_{on}^2 \cdot R_{on}$. To minimize the power loss, R_{on} needs to be minimized. One of the components that contributes to R_{on} is the metal-semiconductor contact resistance R_c. Typically, for high performance power devices, a low specific contact resistance of $1 \times 10^{-5} \Omega \cdot cm^2$ is required [94].

3.1.3 Source and drain contact resistance in TAOS TFT scaling

Traditionally, active thin film electronics were mainly used in display backplanes, but they are rapidly moving towards use in new applications such as arrays of sensors and actuators, distributed energy harvesting, wireless communications systems and power electronics [69]–[72]. The need for large-area, high-frequency and high-power digital and analog circuits has created interest in transparent amorphous oxide semiconductors, such as indium gallium zinc oxide (IGZO) or zinc tin oxide (ZTO), due to their wide bandgap

(~3.4eV) and high electron mobility in the amorphous state compared to amorphous silicon or organic semiconductors [95]. Here we pursue ZTO due to the increasing scarcity and cost of indium [96], and use solution-processed ZTO deposition to enable future low-cost printed active electronics. For solution-processed ZTO thin film transistors (TFTs), the highest reported [97] field effective mobility is 27.3 $cm^2V^{-1}s^{-1}$.

In order to make TAOS TFTs that operate at radio-frequencies, sub-micron channel length, *L,* is generally required. Sub-micron (*L*=0.5μm) IGZO TFTs have been realized [98] with f_T = 135 MHz. As in planar MOSFETs, when TAOS TFTs are scaled down, non-scaled parameters begin to dominate and deteriorate device performance. However, unlike conventional Si MOSFETs, whose ohmic S/D MS contact is realized by heavily doping the semiconductor S/D region, as shown in Equation 3.2 [94] (where ε_S is the dielectric constant of the semiconductor, m^* is the effective mass for electrons, and h is Plank's constant, Φ_{bn} is the interface barrier height and N_D is the semiconductor doping concentration), the S/D contact resistance in TAOS TFTs is directly controlled by the MS interface, as shown in Figure 3-1.

$$R_C = exp\left[\frac{2\sqrt{\varepsilon_S m^*}}{h}\left(\frac{\phi_{bn}}{\sqrt{N_D}}\right)\right] \tag{3.2}$$

Therefore, in practice, the cut-off frequency is limited by the parasitic gate-to-source/drain overlap capacitance (C_{OV}) and by the contact resistance of the source/drain (S/D) electrodes to the semiconductor channel. Self-aligned TFT processes have begun to address C_{OV} [98]–[101], although overlap dimensions are still relatively large [98] (1.55 µm).

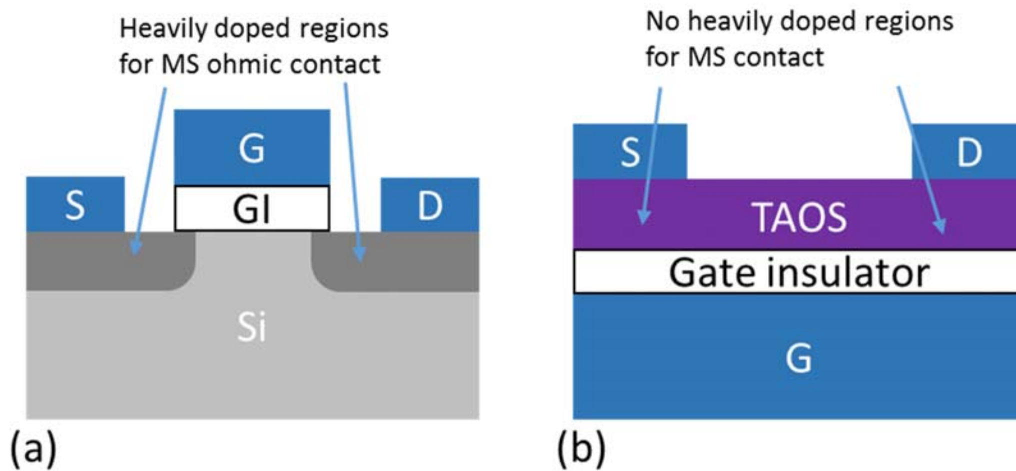


Figure 3-1. The difference of metal-semiconductor (MS) contact formation between (a) a conventional Si transistor and (b) a TAOS TFT.

3.1.4 Solution-processed ZTO TFT scaling and contact resistance

Contact resistance to ZTO, which is affected by a number of factors including the choice of the S/D material and the interface properties, has not yet been addressed within the context of TFT scaling. It still remains a question whether solution-processed ZTO TFTs have the capability of scaling down to a submicron channel length. This work is motivated by the use of molybdenum (Mo) to form a contact to IGZO with low contact resistance of 5.6-85.5 Ω·cm [102]–[106], as summarized in Figure 3-2. Molybdenum is a promising electrode material due to its relatively low resistivity of ~5×10^{-6} Ω·cm, a relatively low work function of 4.3-4.9 eV, and the fact that it does not readily oxidize at room temperature [107].

Here, we present ZTO TFTs made with sputtered Mo (Mo-s) S/D. The transmission line method is used to compare S/D contact properties of sputtered Mo to indium tin oxide

(ITO), gold/titanium (Au/Ti) and evaporated molybdenum (Mo-e). Previous studies of ZTO contacts (Table 3-1) have been limited to Al, IZO and Cu which have contact resistance of > 100 Ω·cm [57], [108]–[113]. Our sputtered-Mo/ZTO contacts exhibit a very low width-normalized contact resistance of 8.7 Ω·cm, opening a pathway toward future radio-frequency (RF) circuitry using sub-micron ZTO TFTs.

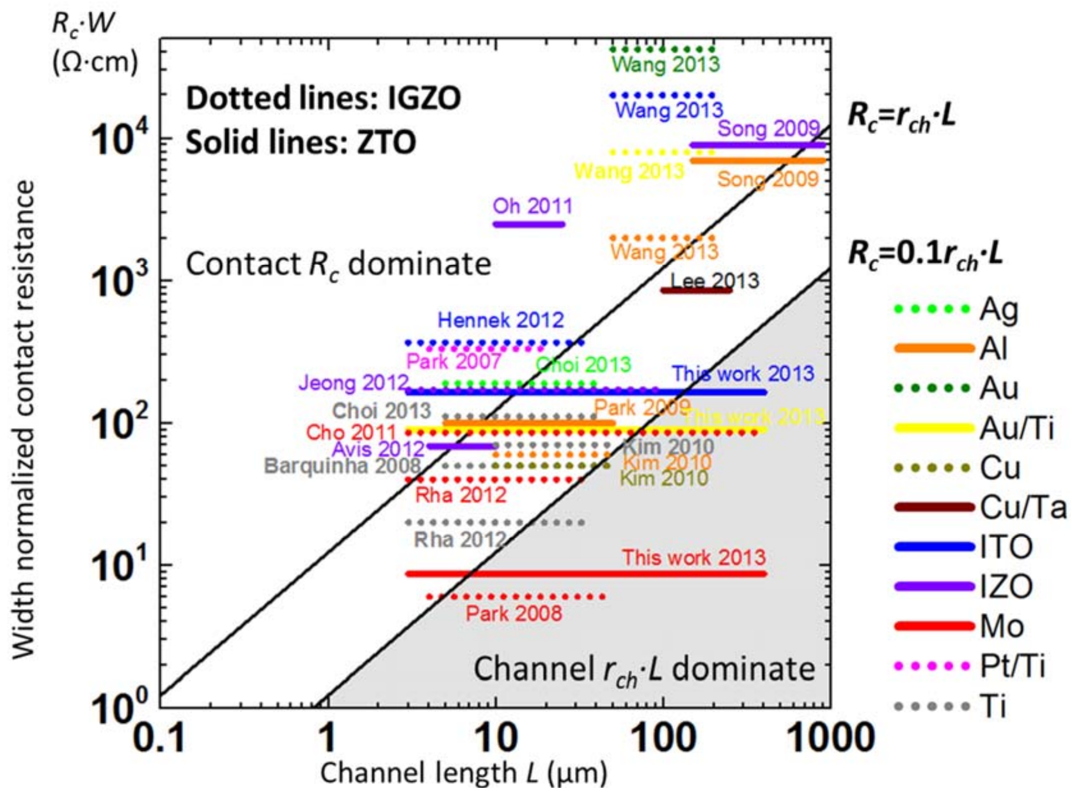


Figure 3-2. Reported TAOS contact resistance studies, showing Mo and Ti generally form contacts to TAOS with lower contact resistance, more suitable for short channel devices.

3.2 Experimental

Heavily doped n-type silicon wafer was used as the substrate and gate electrode, with 100-nm of thermally grown silicon oxide as the gate dielectric. A zinc tin oxide layer was

deposited by spin-coating a premixed acetate-based solution, followed by drying and annealing. A detailed description of solution preparation, ink process and ZTO film characterization can be found in Section 2.2 and our previous paper [114]. The ZTO layer was patterned by photolithography and wet etching using a mixture of HCl, HNO_3 and DI water, with a volume ratio of 1:10:90. To form S/D electrodes, 100-nm Mo was sputtered at 600 W for 260 seconds (labelled "Mo-s"), 100-nm ITO was sputtered at 140 W with 2.5% oxygen partial pressure for 580 seconds, or 90-nm/10-nm Au/Ti or 60-nm Mo were e-beam evaporated (labelled "Mo-e"). The evaporation of Mo was halted at 60-nm thickness in order to limit substrate heating. The S/D electrodes were patterned by liftoff. The channel width *W* of the transistors varies from 3000 µm to 100 µm, and the channel length *L* varies from 400 µm to 3 µm, with W / L ratios of 10 to 30. A cross sectional schematic of the resulting bottom gate, top contact TFT is shown in the Figure 3-4 (a) inset, and TFT top views from an optical microscope are shown in Figure 3-3 (a) (b) and (c) for Mo (sputtered), Au/Ti and ITO source and drain electrodes, respectively. The top contact architecture is chosen to avoid high-resistance end contacts at the edge of the source-drain electrodes [115].

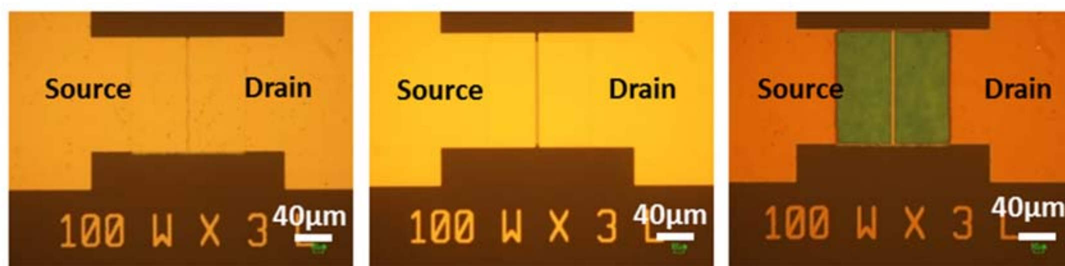


Figure 3-3. Optical micrographs of spin-coated ZTO TFTs of *W*/*L*=100µm/3µm with (a) Mo, (b) Au/Ti, (c) ITO source and drain electrodes.

The electrical performance of the transistors was tested at room temperature in ambient air and light using an HP4155A semiconductor parameter analyzer.

3.3 Results and discussion

3.3.1 Mobility degradation

The I_{DS}-V_{GS} transfer curves of transistors with different source and drain materials are shown in Figure 3-4 (a). The transistors have on-off current ratios > 10^6, turn on voltages of -5 V to -8 V, sub-threshold slopes of ~ 1V per decade, and moderate hysteresis, except for the TFT with evaporated Mo S/D. The relatively large subthreshold slope and hysteresis for the evaporated Mo S/D TFT may result from charge trap states at the semiconductor-insulator interface induced during sample heating during the Mo evaporation. The TFT with sputtered Mo S/D exhibits the largest drain current, due to superior contact properties.

The field-effect mobility, μ_{FE}, of each transistor is extracted from the linear region according to $\mu_{FE} = g_m \left(C_{ox}\frac{W}{L}V_{DS}\right)^{-1} = \frac{\partial I_{DS}}{\partial V_{GS}}\left(C_{ox}\frac{W}{L}V_{DS}\right)^{-1}$. For transistors with the same S/D material, μ_{FE} decreases as L shrinks (Figure 3-4 (b)). This trend is observed in TFTs with all S/D materials, although the degrees of mobility degradation differ, with the sputtered Mo TFTs showing the least change.

The apparent degradation of μ_{FE} results from voltage division between the channel resistance $r_{ch} \times L$ and the contact resistance R_c, where the total source-to-drain resistance is $R_{Total} = r_{ch} \times L + R_c$ (Figure 3-4 (a) inset). As L decreases, $r_{ch} \times L$ becomes smaller while R_c does not scale and thus becomes a larger portion of R_{Total}. This reduces the effective

voltage across the channel from drain to source. The effective mobility of a TFT with non-negligible contact resistance, $\mu_{FE,c}$, can be expressed as $\mu_{FE,c} = \mu_{FE,0}(1 + R_c/r_{ch}L)^{-1}$ where $r_{ch} = \left(\mu_{FE,0}C_{ox}W(V_{GS} - V_{TH0})\right)^{-1}$ is the contact-independent channel unit length resistance, as shown in Figure 3-5. Here $\mu_{FE,0}$ and V_{TH0} are the mobility and threshold voltage for long-channel transistors (i.e., when R_c is negligible). C_{ox} is the gate insulator capacitance and V_{GS} is the applied gate-source voltage, neglecting any voltage drop at the source [103], [106], [112]. To extract an R_C value for Mo-e, the data in Figure 3-4 (b) was fit to the $\mu_{FE,c}$ equation, using $\mu_{FE,0}$ and V_{TH0} from sputtered Mo transmission line method (see below). The S/D R_C value for Mo-e is quite high, ~5200Ω·cm. The fit R_C value for Mo-s found by fitting $\mu_{FE,c}$ is several orders of magnitude smaller, < 10Ω·cm.

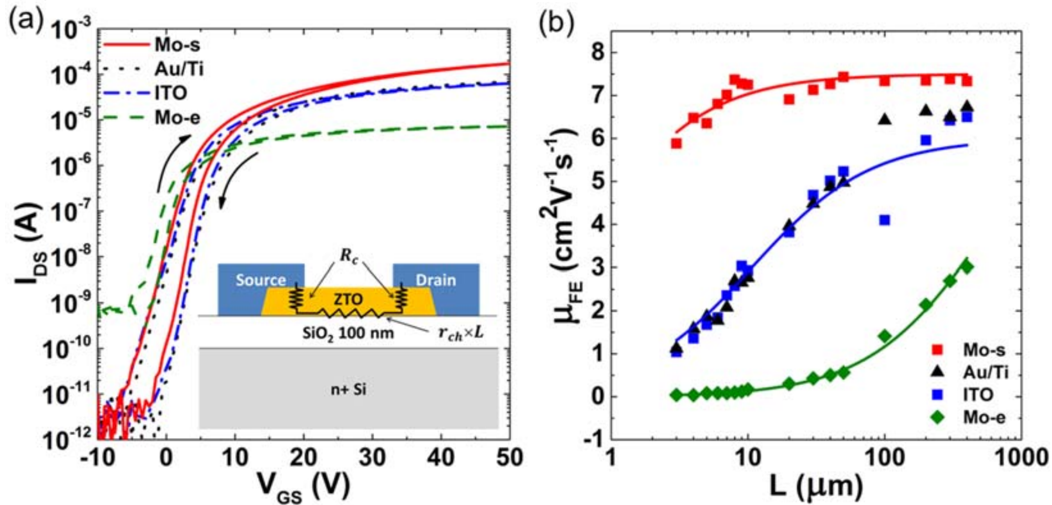


Figure 3-4. (a) Transfer curves of ZTO TFTs with different S/D materials, for W/L = 100μm/5μm, V_{DS} = 1V. (b) Symbols: TFT field-effect mobility extracted from the linear region of the transfer curves. Lines: fits to $\mu_{FE,c}$ equation, using $\mu_{FE,0}$ and V_{TH0} from transmission line method. Mo-s refers to sputtered Mo, Mo-e to evaporated Mo.

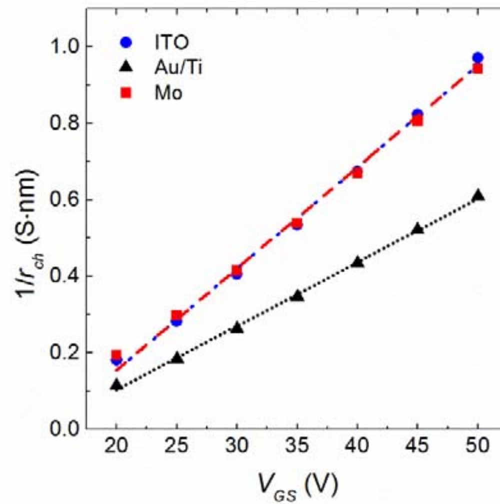


Figure 3-5. Contact-independent ZTO unit length channel conductance $1/r_{ch}$, showing all ZTO TFTs have similar channel properties when de-embedded from contacts.

3.3.2 Contact resistance

To better quantify contact properties, the transmission line method (TLM) was used in the lateral two-contact, two-terminal geometry. This method is described in Refs. [115], [116] and is commonly used to analyze contact resistance in metal oxide TFTs [101]–[106], [108], [109], [111]–[113], [117], [118]. $R_{Total} = V_{DS} / I_{DS}$ is extracted in the linear region. Output curves for Mo-s (Figure 3-6 (a)), ITO and Au/Ti S/D show linear current-voltage (I-V) behavior and no non-linearities at low V_{DS}, indicating an ohmic contact to ZTO. TFTs with evaporated Mo S/D (Figure 3-6 (b)) show non-linear I-V behavior, indicating the formation of a Schottky barrier. For a given V_{GS}, $R_{Total} \times W$ is plotted against L, as shown in Figure 3-7 for TFTs with (a) sputtered Mo S/D (b) with Au/Ti S/D and (c) with ITO S/D. A linear fit yields a slope of $r_{ch} \times W$ and y-intercept of $R_c \times W$, both of which are V_{GS} dependent. Values of $\mu_{FE,0}$ and V_{TH0} can be extracted using a linear fit of $1 / r_{ch} \times W$ to V_{GS}.

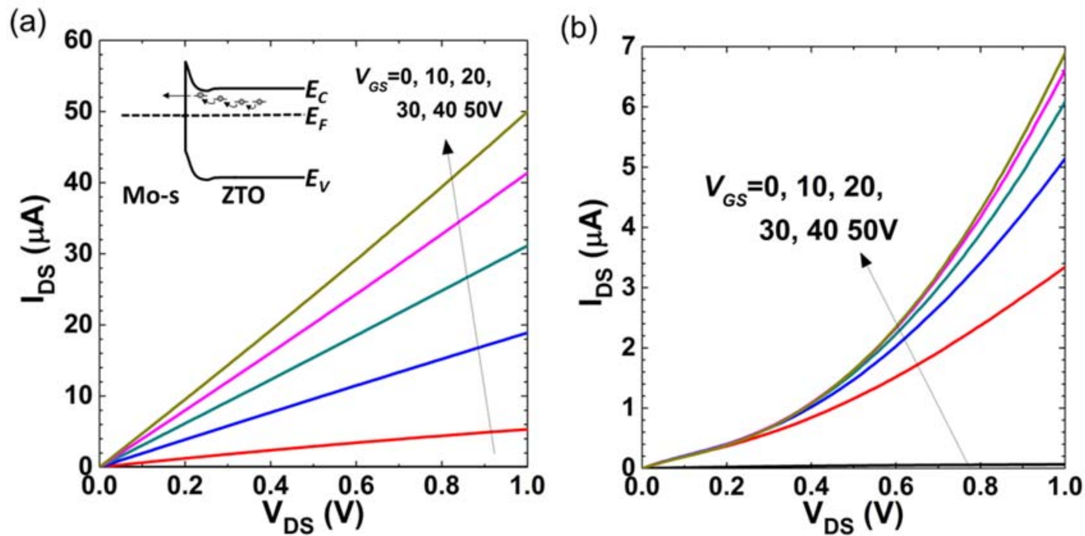


Figure 3-6. (a) Output curves of sputtered Mo TFT. Inset shows band diagram of metal-doped semiconductor interface with trap-assisted tunneling. (b) Output curves of an evaporated Mo TFT.

The width normalized contact resistance, $R_c \times W$, is plotted versus V_{GS} in Figure 3-7 (d). The contact resistance is not a strong function of V_{GS}, indicating that interfacial contact resistance dominates over ZTO bulk resistance. When the TFTs are fully turned on (V_{GS} = 50 V), TFTs with sputtered Mo S/D have the smallest $R_c \times W$ = 8.7 Ω·cm, in agreement with the estimate derived from $\mu_{FE,c}$ earlier. The sputtered Mo contact resistance is more than ten times smaller than that of Au/Ti S/D ($R_c \cdot W$ =91 Ω·cm) and almost twenty times smaller than ITO S/D ($R_c \times W$ = 163 Ω·cm). The ITO/ZTO value agrees closely with previously published results ($R_c \times W$ = 100-191 Ω·cm) [57], [110]. Compared with other materials such as IZO, Cu, Al used in ZTO TFTs previously reported, shown in Table 3-1, the sputtered Mo-ZTO reported here has the smallest contact resistance.

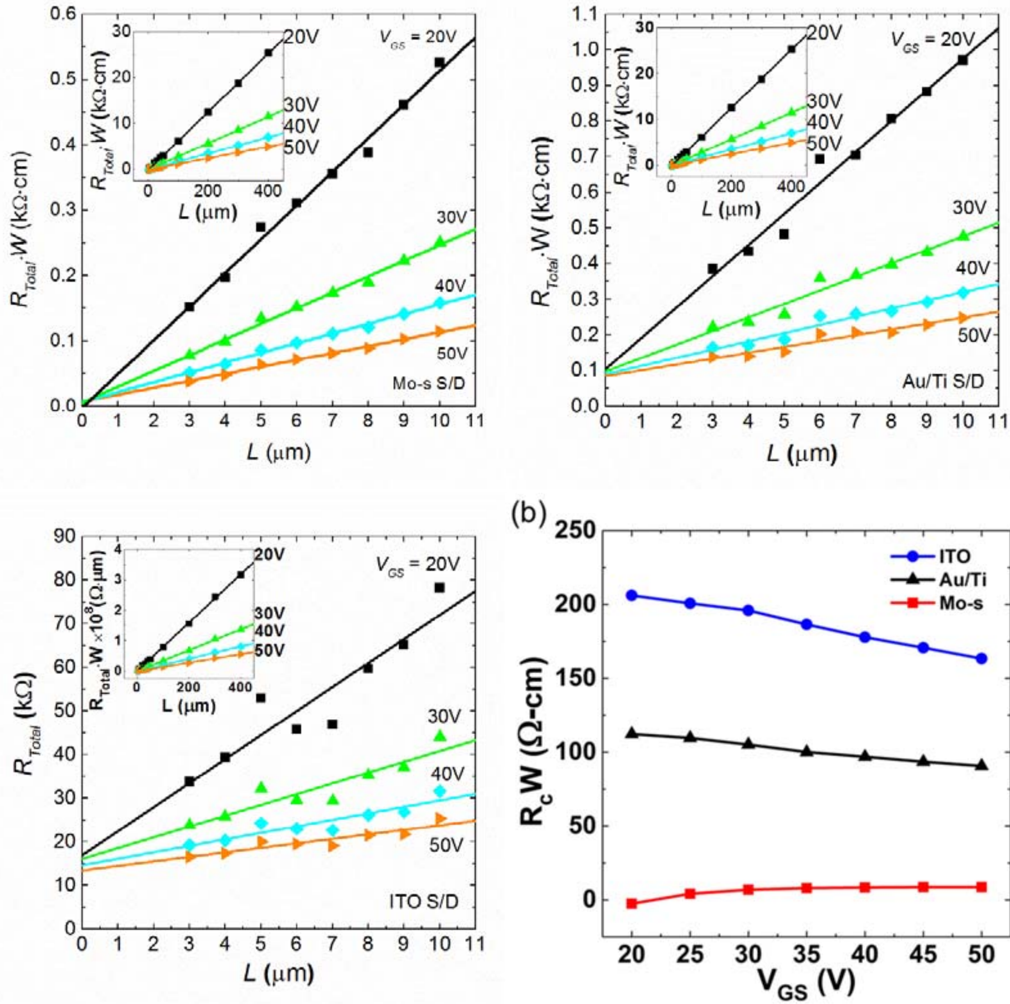


Figure 3-7. Transmission line method data: total width-normalized resistance of ZTO TFTs with (a) sputtered Mo S/D, (b) Au/Ti, (c) ITO, for L = 3 to 400 μm; (d) width-normalized contact resistance of TFTs with sputtered Mo, Au/Ti and ITO S/D.

Table 3-1. Width-normalized contact resistance and specific contact resistivity of zinc tin oxide TFTs with various source/drain (S/D) electrode materials.

Reference	Active layer	S/D layer material	$R_c\times W$ (Ω·cm)	ρ_c (Ω·cm)
This work [119]	sol-gel ZTO	sputtered Mo	8.7	1.5×10^{-4}
		evaporated Au/Ti	91	1.2×10^{-2}
		sputtered ITO	163	5.3×10^{-2}
		evaporated Mo	5200	-
[57]	sputtered ZTO	sputtered Al	3000	-
		sputtered ITO	100	-

[108]	sol-gel ZTO	evaporated Al	-	10^{-3}-10^{-4}
[109]	sol-gel ZTO	evaporated Al	7000	-
		printed IZO	9000	-
[110]	sputtered ZTO	sputtered ITO	190.9	-
[111]	sol-gel ZTO	sputtered IZO	31	-
[113]	sputtered ZTO	sputtered IZO	2500	-
[112]	sputtered ZTO	sputtered Al/Ta/Cu/Ta	857	-

To explain the trends in contact resistance, it is noted that Mo has a relatively small work function (4.3-4.9 eV) [120] that lines up well with the ZTO electron affinity (4.35-4.6 eV) [109], [121]. Other published S/D materials such as ITO, Cu and IZO have larger work functions (ITO: 4.3-5.2 eV [122], Cu: 4.5-5.1 eV [120] and IZO: 4.8-5.6 eV [109]), resulting in a larger energy barrier. Our ZTO results agree with ref. [122], which found that contact resistance in IGZO systems is generally determined by the work function lineup. We have shown already that ZTO, like IGZO, has localized tail states close to the conduction band edge [114]. Trap-assisted tunneling into these states combined with Schottky barrier inhomogeneity may allow formation of ohmic contact even when large barrier heights are expected, as observed in IGZO (Figure 3-6 (a) inset) [123], [124].

However this cannot explain why Ti, with a smaller work function (~4.3 eV [120]), does not form a better contact. In studies of IGZO TFTs, the formation of a TiO_x interfacial layer has been proposed [104], [105], [122] and experimentally observed [117], [125]–[127] (Figure 3-8 (a)). Interfacial TiO_2 is energetically favorable due to its relatively large enthalpy of formation: $\Delta_f H^{\Theta}_{298}$ = -944, -350.5, and -578 kJ/mol for titanium dioxide (TiO_2),

zinc oxide, and tin oxide (SnO_2), respectively [120]. Since TiO_2 is usually an insulator, it may form an energy barrier for charge injection and extraction, resulting in large contact resistance, despite its smaller work function [128]. In contrast, molybdenum oxide has only been observed to form at Mo/IGZO interfaces when anneals ≥ 400°C were performed post-metallization [105], [129]. The lack of a molybdenum(VI) oxide (MoO_3) interlayer may be due to its relatively smaller enthalpy of formation of -745 kJ/mol [120]. Even if formed, MoO_3 may improve the device performance via formation of intermixed chemical states [130]. Therefore, an insulator-free Mo/ZTO interface may contribute to its small contact resistance.

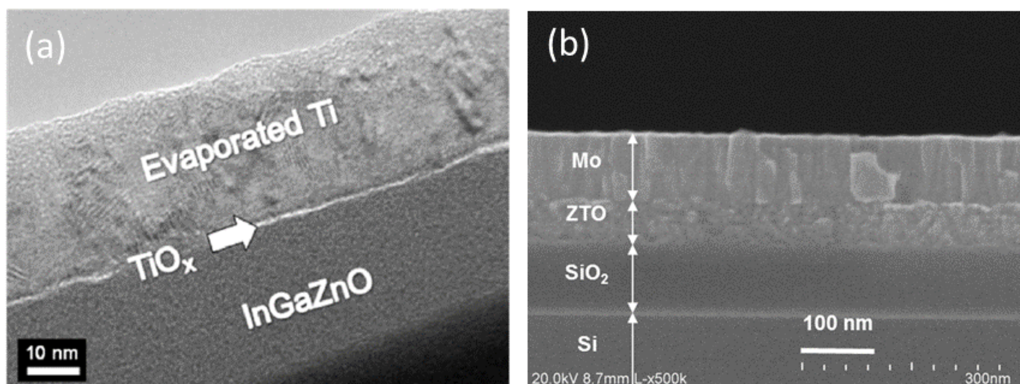


Figure 3-8. (a) The interface of Ti/IGZO showing possible TiO_x formation [117]. (b) The interface of Mo/ZTO may be oxide-free.

In addition, the sputtering process may help form the superior Mo-s/ZTO contact. Mo is usually sputtered using argon at a higher power or longer times compared to other materials. Since the resistivity of oxide semiconductors can be reduced by argon or hydrogen plasma treatment, possibly due to the formation of metal interstitials or other doping states [99], [100], [113], [118], [131], [132]. Therefore it has been proposed that

Mo forms a quasi-ohmic contact to IGZO because of the heavy atom bombardment of the active layer during Mo sputtering [104],[133]. Likewise for ZTO, Mo sputtering may change local chemical states and create a conductive region at the Mo/ZTO interface or deeper in the ZTO film. The impact of sputtering is seen by comparison to TFTs with evaporated Mo. These did not experience a plasma process and thus the Schottky barrier between Mo and ZTO remains, resulting in a non-ohmic contact.

3.3.3 Transfer length

To determine whether the Mo-ZTO system is suitable for sub-micron TFT, the transfer length, L_T, is calculated. The transfer length is the effective distance that the channel extends under the source and drain due to current crowding under diffusive transport, and it defines the effective contact area. It is calculated as $L_T = \sqrt{\rho_c/(r_{ch}W)}$ using a distributed model that includes specific contact resistance, ρ_c (Ω-cm^2) and channel resistance, r_{ch} [115], [116]. If the overlap between the contact metal and semiconductor (~50µm in our case) is > 2.3 L_T, and the resistance is measured at the edge of the contact, then the total contact resistance for two contacts is $R_c \cong 2\rho_c/(L_T W)$. This equation can be combined with the definition of L_T to yield $L_T = R_c/2r_{ch}$. $2L_T$ represents a critical channel length above which R_c dominates R_{Total} and $\mu_{FE} < \mu_{FE,0}/2$. L_T thus provides a guideline for TFT design and scaling. At V_{GS} = 50 V, L_T for Mo/ZTO TFTs is 0.34 µm, much smaller than that for Au/Ti/ZTO (2.6 µm) and ITO/ZTO (6.5 µm) TFTs. The sputtered Mo/ZTO system thus opens a pathway toward sub-micron TFTs for future high performance thin film circuits. For the three metals used here, the calculated specific contact resistivities, ρ_c, are 1.5×10^{-4} Ω-cm^2 (Mo), 1.2×10^{-2} Ω-cm^2 (Au/Ti) and 5.3×10^{-2} Ω-cm^2 (ITO).

3.4 Conclusions and future work

3.4.1 Conclusions

In summary, sputtered Mo, alongside Au/Ti, ITO and evaporated Mo, were used as contact materials for solution-processed ZTO TFTs. TFTs with sputtered Mo source/drain showed the best electrical performance and smallest width-normalized contact resistance of 8.7 Ω·cm, comparable to the best reported vacuum-processed IGZO TFTs. The good contact quality is attributed to molybdenum's low work function along with trap-assisted tunneling, an insulator-free interface between Mo and ZTO, and ZTO surface damage during Mo sputtering. The 0.34 µm transfer length of the Mo/ZTO system makes sputtered Mo a candidate contact material for high performance sub-micron ZTO TFTs.

3.4.2 Outstanding scientific questions and future works

Future work include (1) better understanding of the physical origin of this low contact resistance between sputtered Mo and spin-coated ZTO, (2) investigating other materials and methods that might have smaller contact resistance, (3) implementing sub-micron TFTs and circuits.

(1) The physical origin of the low contact resistance is not yet fully understood. The proposed origins might not all be the dominating factor(s) of the low contact resistance. These hypotheses could be further studied by material characterization techniques and temperature dependent electrical measurements.

(2) Other materials and processes that could have smaller contact resistance are needed. While sputtered Mo forms a good contact to spin-coated ZTO, it still limits the

theoretical working channel length to several hundred nanometers. In addition, it is undesirable if ZTO surface damage during Mo sputtering is required to achieve low contact resistance. Therefore other materials and processes that push the transfer length L_T to a lower value, ideally tens of nanometers, are desired. Sputtered tungsten is one possible material [134].

(3) Sub-micron ZTO TFTs could be fabricated and characterized. These TFTs could be made into radio-frequency circuits for future application demonstrations. Scientifically, these TFTs could also be used to study other short channel effects in TAOS TFTs, providing a better understanding of these materials and devices, opening up pathways toward more complicated material and device systems.

Chapter 4 Solution-processed yttrium/scandium-doped zinc tin oxide TFTs

4.1 Introduction

4.1.1 Stability of TAOS TFTs

The study of TAOS materials and TFTs has become mature, but several important issues still need to be better understood and addressed. One of these issues is the stress-induced instability of TAOS TFTs. During practical operations, different types of stresses are applied to the TFTs, including positive gate bias stress, negative gate bias stress, dynamic bias stress, current stress, temperature stress, illumination stress, mechanical stress, and combinations of these stresses [135]. The stress can induce various device performance degradations, such as a mobility, μ, decrease or a turn-on voltage, V_{ON}, or threshold voltage, V_{TH}, shift, which would lead to undesirable changes in the TFT circuit and system performance. For example, in an active matrix organic light emitting diode (AMOLED) flat-panel TV system where a TFT drives an OLED in a pixel, a 0.1V V_{ON} shift in the TFT could change the OLED brightness by as much as 16%, causing non-uniformities that are detectable by the human eye [136].

Positive bias stress (PBS) and negative bias illumination stress (NBIS) are the two most common stress conditions. During PBS, a constant positive gate bias V_{GS} is applied to a TFT to keep the TFT in the on state. This positive V_{GS} may induce a positive shift in the

turn on voltage, V_{ON}, a decrease in mobility, μ, and an increase in subthreshold slope, *SS*. NBIS, on the other hand, keeps the TFT in the off state by applying a negative V_{GS} while simultaneously stressing the device with illumination. It has been observed that even when the photon energy is smaller than the optical band gap of the TAOS, the TFT will still suffer from degradation, such as a negative V_{ON} shift.

4.1.2 Origin of the instabilities

The physical origins of the instabilities are mainly charge trapping and/or defect creation/redistribution. As shown in Figure 4-1, these charges or states could be found near the channel at the semiconductor-insulator interface, Q_{it}, inside the bulk of the semiconductor, Q_{bulk_AOS}, or at the back channel interface, Q_{bc}. Multiple instability mechanisms can co-exist and can simultaneously affect TFT performance.

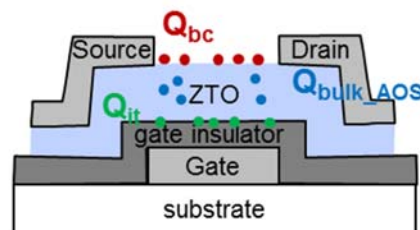


Figure 4-1. A schematic cross section of a ZTO TFT, illustrating possible physical locations of charges/states that cause instability.

PBS instability in TAOS has been explained by charge trapping at the semiconductor/insulator interface, acceptor-type defect creation inside the bulk, and/or field-induced back channel reaction with the ambient. To a large extent, PBS instability

has been satisfactorily addressed using post-deposition annealing and back-channel passivation.

NBIS instability, however, remains an issue for TAOS devices. When a TAOS TFT is subjected to simultaneous negative gate bias and illumination stress (Figure 4-2 (a)), the TFT suffers from a negative V_{ON} shift. The shifts occur even for photon energies that are smaller than the band gap energy of the TAOS, e.g. 2.3eV. Such shifts can decrease the TAOS film resistivity, causing a high TFT off current. The physical origins of NBIS and solutions to address this instability are still being explored [43], [48]. One of the proposed origins of NBIS instability is the ionization of deep gap oxygen vacancies (Figure 4-2 (b)), based on observations by photoluminescence (PL) and *C-V* measurements [137]–[140]. The charge-neutral deep-gap oxygen vacancy states can be singly or doubly charged by holes during illumination stress. Atomically, this occurs via an outward structural relaxation at the oxygen vacancy site [141] or oxygen vacancy migration [142]. The generation of positively charged deep-gap states, induced by the simultaneous illumination and negative bias stress, causes the channel to be accumulated by electrons, lowering the channel resistance.

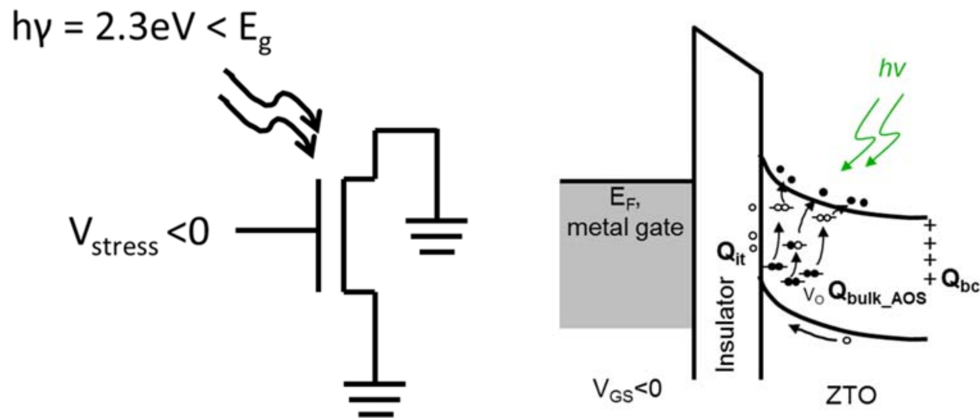


Figure 4-2. (a) NBIS configuration (b) Band diagram of a TAOS TFT under NBIS.

4.1.3 TAOS with oxygen getters

NBIS instability is unique to TAOS materials. It has been hypothesized that this is due to the instability's origin in oxygen vacancy-related defects. This hypothesis is supported by the fact that TAOS NBIS instability can be improved by using "oxygen sufficient" TAOS films (obtained by oxygen plasma or ozone treatment) or by incorporating oxygen getter elements [143]–[147]. Oxygen getter incorporation is of particular interest because it offers improved control of film stoichiometry and possibly better long-term chemical and stress stability. Various oxygen getters have been used for such purpose, including Li, Mg, Ca, Sr, Ba, Al, Y, Sc, La, Ti, Zr, Hf, and Si, as shown in Table 4-1. These elements were alloyed with TAOS, forming quaternary or quinary alloys, to reduce free carrier concentration and control the turn-on voltage. Most studies focused on PBS stability, but a few studies have shown that getters may also improve TFT NBIS stability [143], [144], [148].

As stated in Chapter 1, Sc and Y have a stronger oxygen bonding capability than most other elements. Therefore, Sc and Y should be among the most effective oxygen getters. There have only been a few studies on Sc/Y:TAOS [37], [38], [40]–[42], and these have mainly focused on their carrier suppressing behavior. Questions that remain unclear include: (1) how Sc and Y affect the DC performance of solution-processed ZTO; (2) whether Sc and Y can be effective NBIS stabilizers in solution-processed ZTO; and (3) whether Sc and Y have other roles in the film, such as electron donors or whether they will create extra deep-level defects, especially as the doping concentration rises. In this chapter, we explore these questions.

Table 4-1. TAOS alloyed with oxygen getter elements

Element	References for IZO or IGZO incorporation	References for ZTO incorporation	Effects reported			
			Free carrier suppressor	Oxygen vacancy suppressor	PBS stabilizer	NBIS stabilizer
Li	[39]			X		
Mg	[149]	[150] [151]	X			
Ca	[152]				X	
Sr	[36]			X	X	
Ba	[36]			X	X	
Sc	[42][37]		X			
Y	[37][38][41][40]		X		X	
La		[153]	X		X	
Ti	[154]		X			
Zr		[143]				X
Hf	[148][144]					X
Al		[155][156][157][158][159][160], [161]	X	X		
Si	[162]		X			

4.2 Experimental

The fabrication and testing of Y:ZTO follow the same process as undoped ZTO transistors described in Section 3.2. The addition of Y was achieved by adding solutions of yttrium nitrate hexahydrate in 2-methoxyethanol and ethanolamine into the solutions of zinc acetate, tin (II) acetate in 2-methoxyethanol and ethanolamine. The Y concentration was varied from 0at% to 20at%. A cross sectional diagram of the Y:ZTO TFT is shown in Figure 4-3. The channel width and length of the transistors are varied from *W/L*=3000µm/100µm to *W/L*=3000µm/400µm. Some transistors were passivated by various materials including 40-nm atomic layer deposited Al_2O_3. The passivation layers were etched to access the underlying electrical contacts.

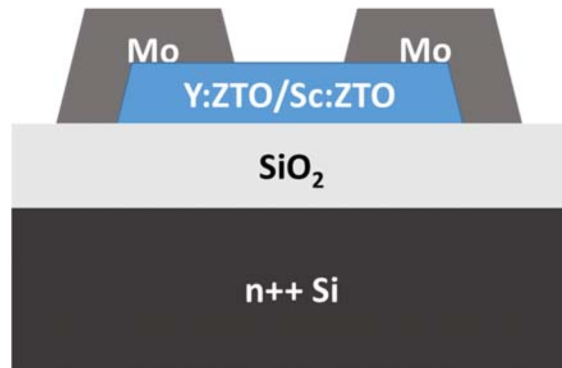
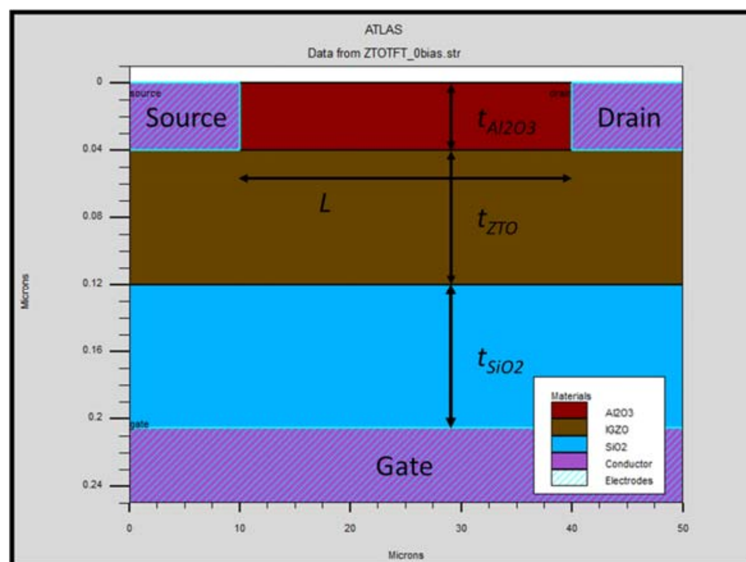


Figure 4-3. A cross-sectional diagram of Y:ZTO or Sc:ZTO without passivation.

DC measurements and PBS were conducted in the dark in air at room temperature. During PBS, V_{DS} was kept at 0V and V_{GS} was kept at +20V. NBIS was conducted in air at room temperature, with a green LED used as the light source. The LED emission spectrum

is 520-535nm (2.38-2.32eV). The optical power density used was 0.9mW/cm^2. During NBIS, V_{DS} was kept at 0V and V_{GS} was kept at -20V.

To understand the physical origin of the observed instabilities, Silvaco ATLAS was used to conduct 2-D numerical simulations of the TFTs. The device structure and the band structure of ZTO used in the simulation are shown in Figure 4-4 (a) and (b). The density of states in the ZTO layer contains two states with exponential distributions, g_{TA} and g_{TD}, and two states with Gaussian distributions, g_{GD} and g_{GA}. In addition, fixed (trapped) charged densities of Q_{it} and Q_{bc} are applied to the bottom and top (back) insulator – semiconductor channel interface, respectively. The simulation parameter values used are summarized in Table 4-2. The values for near conduction band subgap density of states (N_{TA} and W_{TA}) were taken from cryogenic measurements of ZTO, reported in Section 2.2.



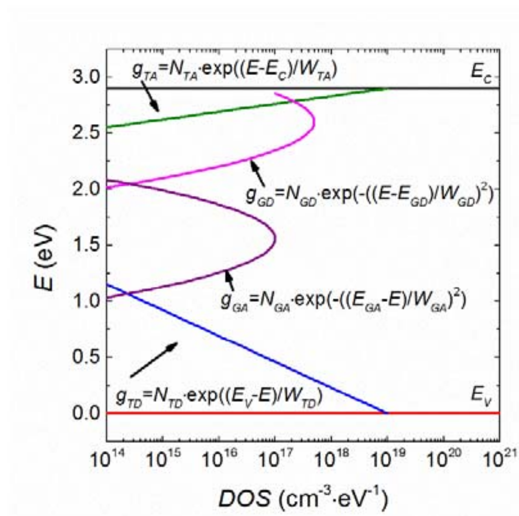


Figure 4-4. (a) Silvaco Atlas TFT structure used for simulation (b) A generic band structure of ZTO used in the simulation, with two tail states and two Gaussian states.

Table 4-2. Parameters used in ZTO TFT simulations

TFT physical dimensions		
t_{Al2O3}	Al_2O_3 passivation layer thickness	40nm
t_{ZTO}	ZTO layer thickness	80nm
t_{SiO2}	SiO_2 gate dielectric thickness	84nm
L	Channel length	30µm
Material electronic properties		
μ_n	Electron mobility	$5cm^2/(V\cdot s)$
N_C	Conduction band effective density of states	$1\times10^{19}cm^{-3}$
N_V	Valence band effective density of states	$1\times10^{19}cm^{-3}$
E_g	Band gap	2.9eV
N_{TA}	Acceptor tail state peak density	$1\times10^{19}\ cm^{-3}\cdot eV^{-1}$
W_{TA}	Acceptor tail state width	0.003eV
N_{TD}	Donor tail state peak density	$1\times10^{19}\ cm^{-3}\cdot eV^{-1}$
W_{TD}	Donor tail state width	0.1eV
N_{GD}	Donor Gaussian state peak density	varied (default=0)
E_{GD}	Donor Gaussian state peak position	varied
W_{GD}	Donor Gaussian state peak width	0.05eV
N_{GA}	Acceptor Gaussian state peak density	varied (default=0)
E_{GA}	Acceptor Gaussian state peak position	varied
W_{GA}	Acceptor Gaussian state peak width	0.05eV
Q_{it} (cm^{-2})	Fixed charge density at the bottom channel interface	varied (default=0)
Q_{bc} (cm^{-2})	Fixed charge density at the top (back) channel interface	varied (default=0)

4.3 Results and discussion

4.3.1 DC performance

The DC electrical performance of Y:ZTO TFTs with various Y doping concentrations are shown in Figure 4-5 (a) and (b), and are summarized in Table 4-3. From the table, it can be seen that a small Y doping concentration, of up to 1at%, slightly improved the device performance. In contrast, Y doping concentrations greater than 1 at% decreased the

mobility, shifted the turn on voltage to more positive values, and increased the subthreshold slope. Beyond 10 at%, the TFTs perform poorly, with low mobility and large subthreshold slope.

The performance improvement at small Y doping concentrations could be due to the creation of shallow donors in ZTO, such as substitutional Y on Zn sites or zinc or tin interstitials, or could be due to a reduction in ZTO defects, such as oxygen vacancies. As the Y doping concentration goes up, Y-related defects might be created, via increased structural disorder or the formation of insulating Y compounds, which may degrade device performance. The increasing subthreshold swing indicates an increase in bulk sub-gap defects or semiconductor-insulator interfacial traps. The decrease in mobility and shift in turn on voltage could also result from an increase in defect density.

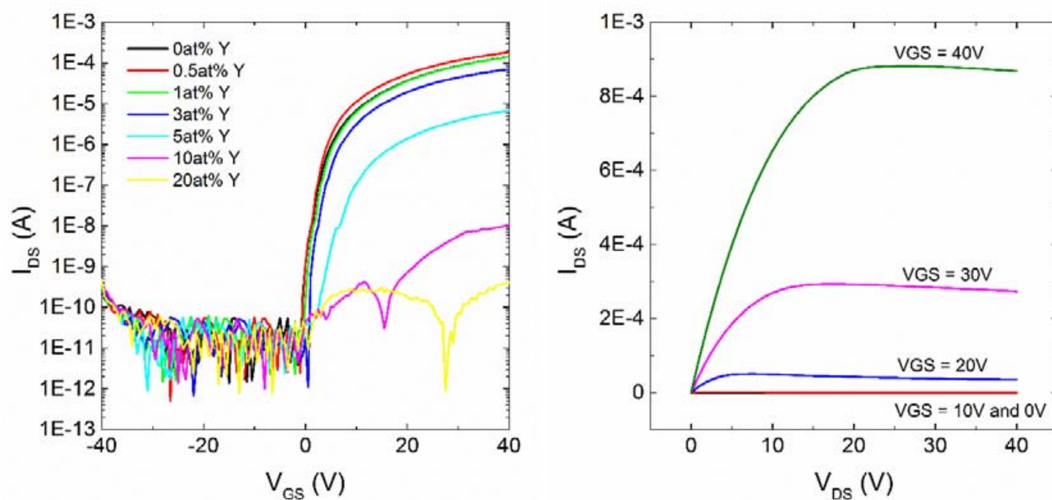


Figure 4-5. Transfer curves of Y:ZTO with various Y doping concentrations, with V_{DS}=1V and W/L=3000μm/100μm. Output curves of 0.5at% Y:ZTO TFT with W/L=3000μm/100μm.

Table 4-3. Y:ZTO DC performance summary

Y concentration (at%)	Linear mobility μ_{lin} (cm^2/(V·s))	Turn on voltage V_{ON} (V)	Sub-threshold slope SS (V/dec)	On-off current ratio
0	4.3	-0.5	0.6	4.8×10^6
0.5	5.3	-0.5	0.7	6.3×10^7
1	4.3	0.0	0.6	6.4×10^6
3	2.1	1.0	0.76	1.0×10^8
5	0.23	3.0	1.51	2.3×10^4
10	4.3×10^{-4}	5.0	1.21	25
20	1.0×10^{-5}	N/A	N/A	N/A
30	N/A	N/A	N/A	N/A

4.3.2 Long term storage stability

The long term storage stability of ZTO TFTs was tested over a span of up to 391 days. The ZTO TFT tested was not passivated and was stored in regular lab ambient with no intentional control of air composition, temperature, humidity or lighting. As shown in the transfer curves and parameter extraction in Figure 4-6 (a) and (b), respectively, the transistor showed a slight change in performance over the first month (22 days) of storage, after which the DC performance remained very stable for more than a year. The excellent long term storage stability of our TFTs shows the reliability of solution-processed ZTO as an electronic material.

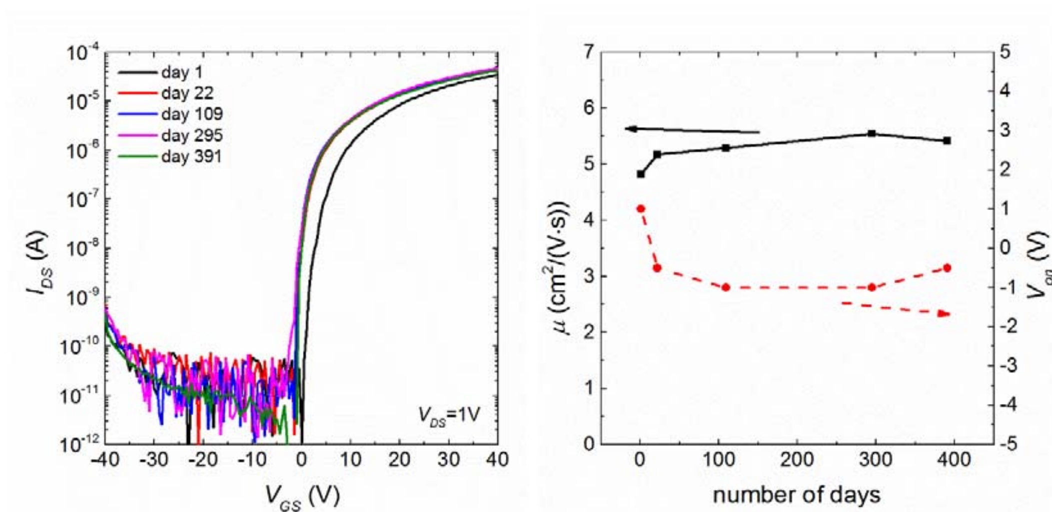


Figure 4-6. (a) Transfer curves of a ZTO TFT with W/L=3000µm/400µm, taken at several dates during more than a year of lab storage. In between tests, the sample was stored in the lab, with no intentional control of ambient conditions. (b) Extracted mobility and turn on voltage versus number of days in storage.

4.3.3 The effect of passivation on DC performance and PBS

Even though ZTO is stable during storage, it is still subject to bias stress. For example, during DC testing, TFTs can undergo voltage and current stress, resulting in hysteresis between forward and reverse voltage sweeps. One way to minimize this hysteresis is to put down a passivation layer on top of the back channel, to minimize the interaction between the back channel and the environment. The passivation layer can minimize changes in back channel charge Q_{bc}, as well as Q_{bulk_AOS} and Q_{it}, that might occur due to film interactions with the environment.

Various passivation layers were deposited onto ZTO TFTs including 20-nm ALD Al_2O_3, 40-nm ALD Al_2O_3, 40-nm evaporated Al_2O_3, and 1-µm parylene. The results are shown in Figure 4-7. Among these, 40-nm ALD Al_2O_3 seem to be the best passivation layer, since it

minimizes hysteresis and enhances mobility. However the turn on voltage is shifted to a slightly more negative voltage (i.e., from -1V to -15V), possibly due to the existence of positively-charged states inside Al_2O_3 or at the ZTO/ Al_2O_3 interface.

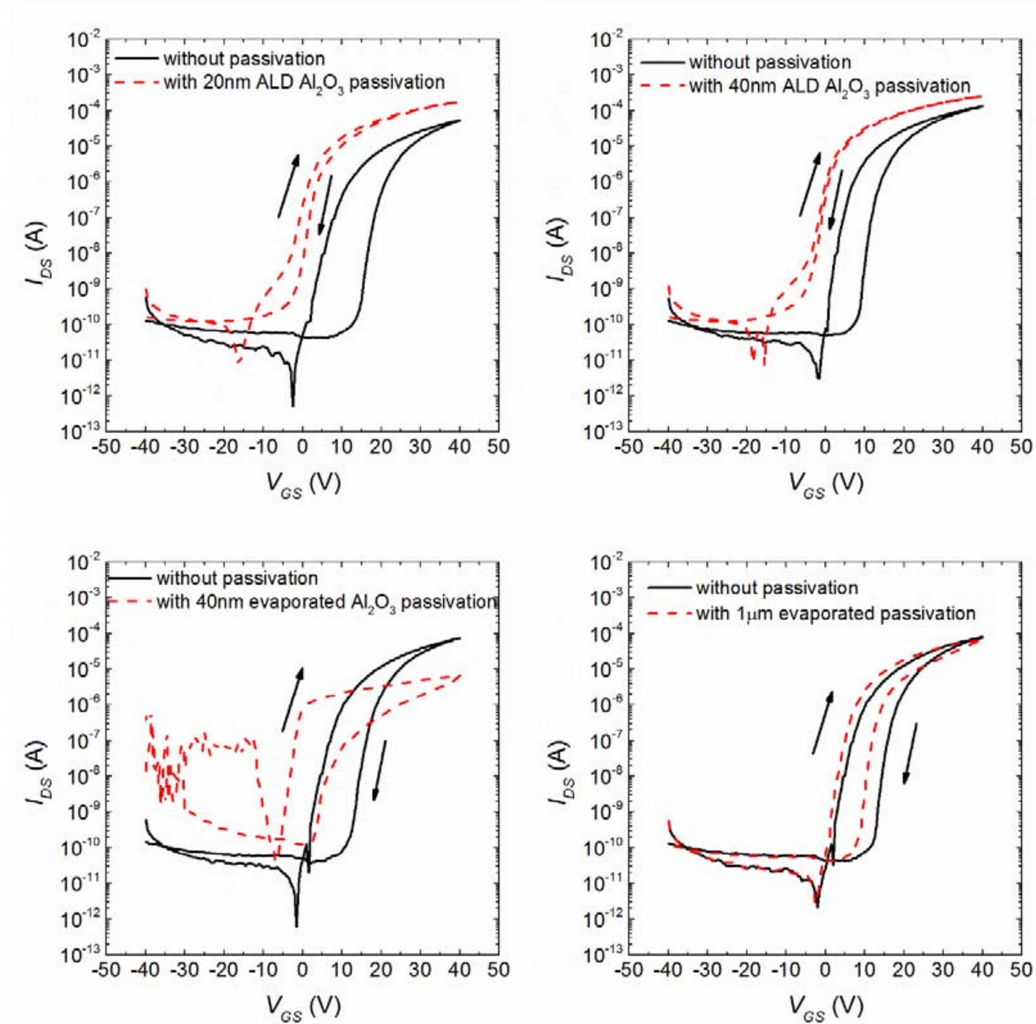
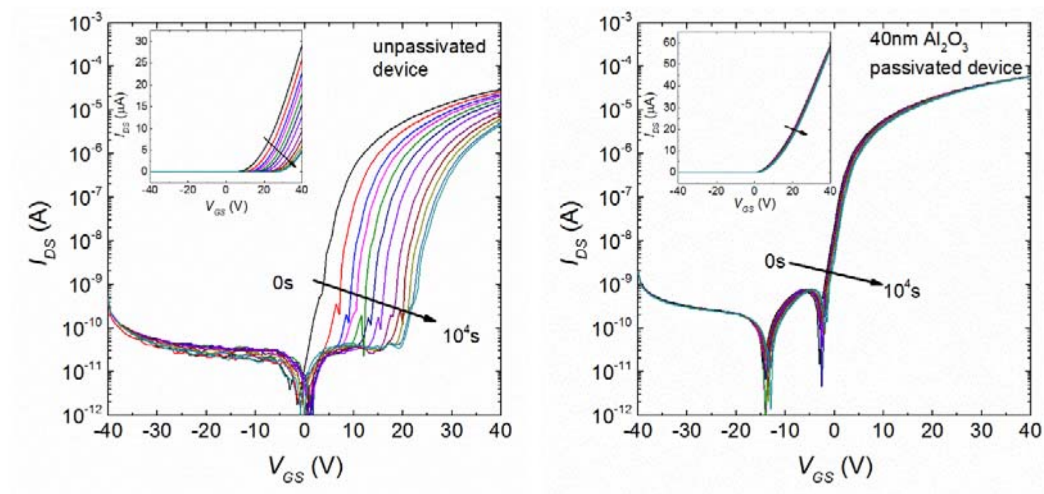


Figure 4-7. ZTO TFT transfer curves before and after back channel passivation with (a) 20-nm ALD Al_2O_3, (b) 40-nm ALD Al_2O_3, (c) 40-nm evaporated Al_2O_3, (d) 1-μm evaporated parylene.

Passivation also improves positive bias stress (PBS) stability. As mentioned before, a number of PBS instability mechanisms have been proposed and demonstrated, such as

charge trapping, defect creation and back channel chemisorption. Multiple mechanisms can co-exist depending on the material, process and device structure. PBS testing results on spin-coated ZTO TFTs are shown in Figure 4-8 (a) and (b) without or with passivation, respectively. During the PBS tests, V_{DS} was kept at 0V and V_{GS} was kept at +20V. The device without passivation showed a drastic positive shift of the turn on voltage (Figure 4-8 (c)), a decrease in the mobility (Figure 4-8 (d)) but no obvious change in the subthreshold slope (Figure 4-8 (e)), indicating that the instability is due to charge trapping. In contrast, the device with 40-nm ALD Al_2O_3 back channel passivation showed trivial changes in TFT performance under PBS. These results show that the main origin of PBS instability in solution-processed ZTO TFTs is field-induced back channel chemisorption. Therefore, passivating the back channel with a layer that blocks this absorption can be highly effective in minimizing PBS instability.



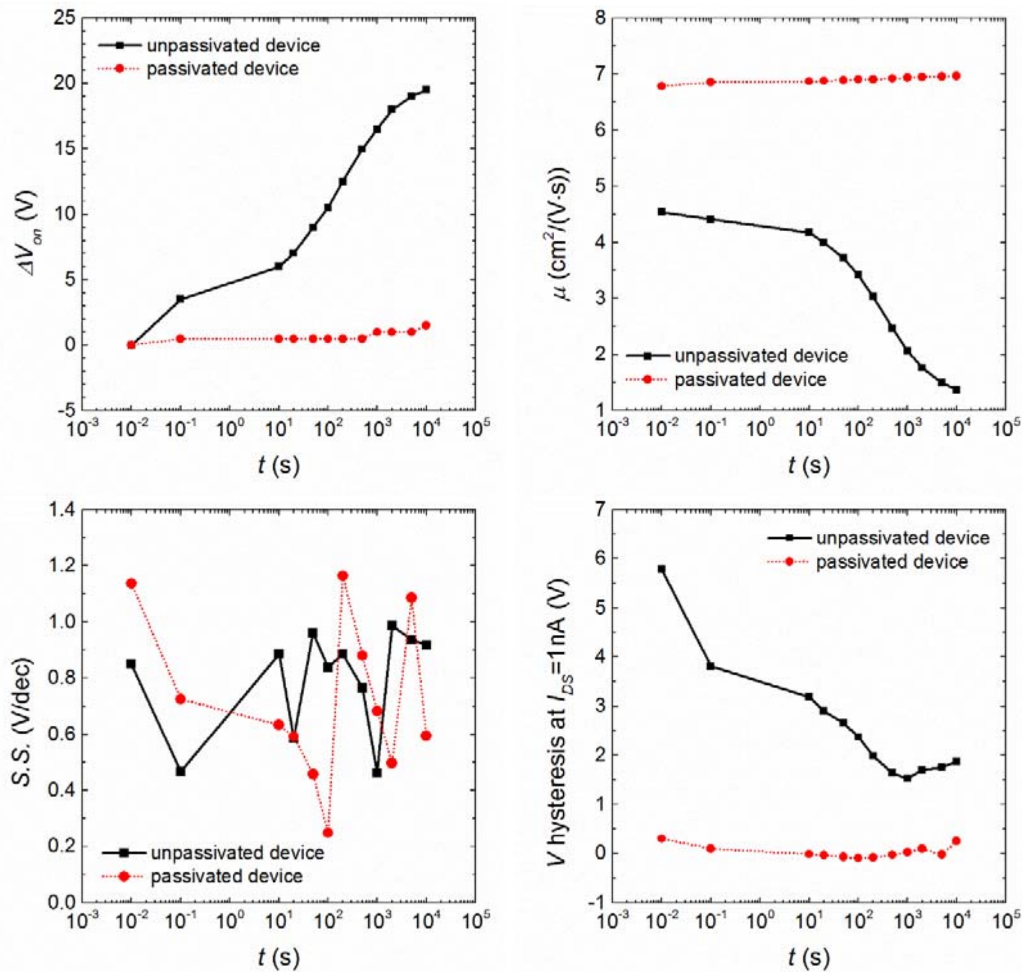
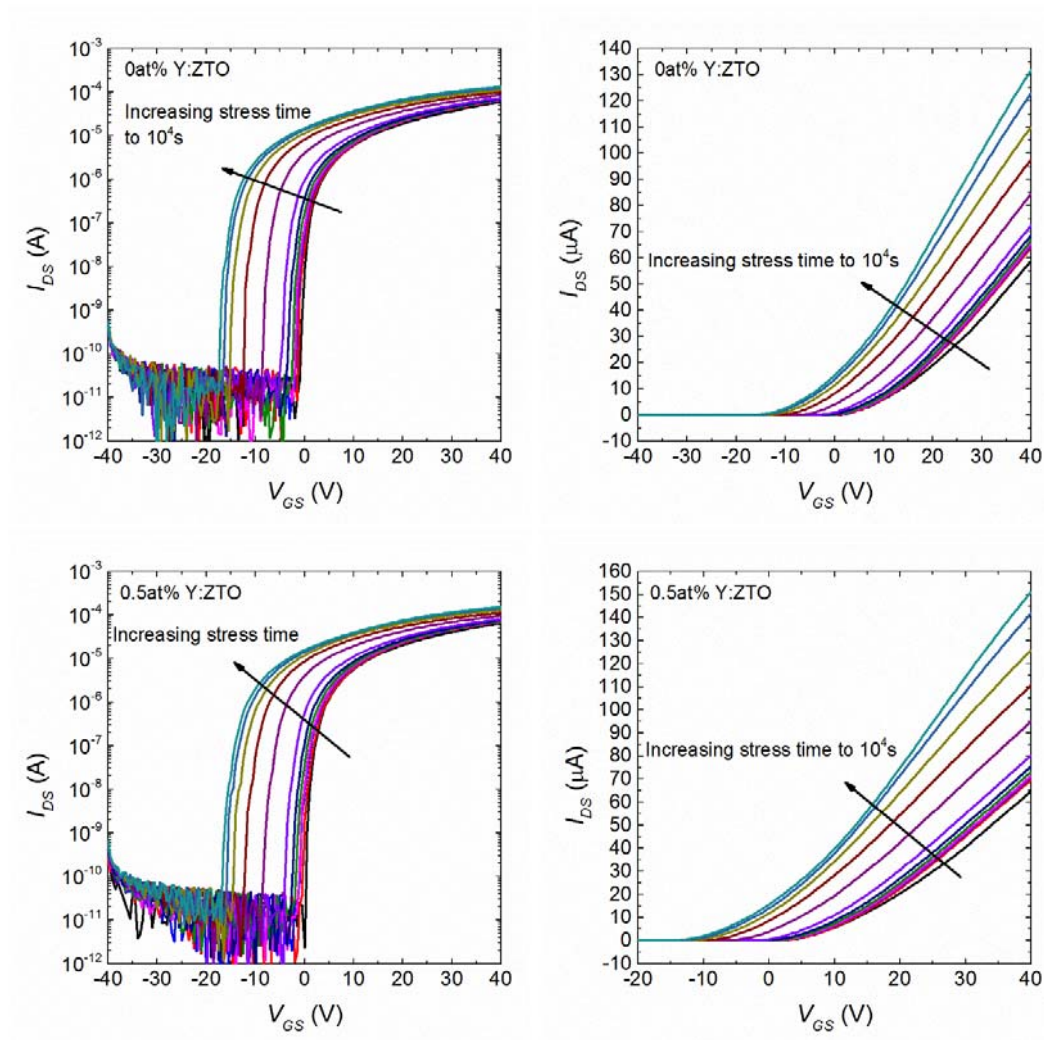


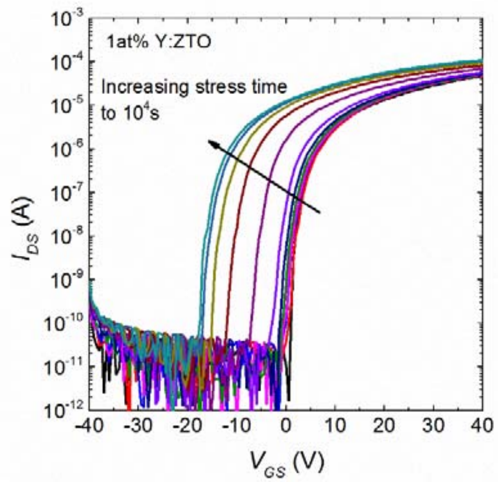
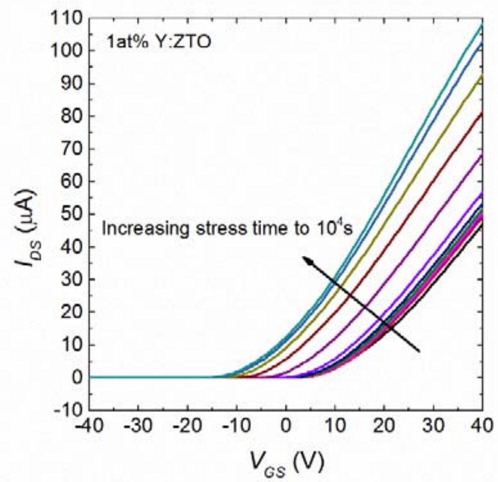
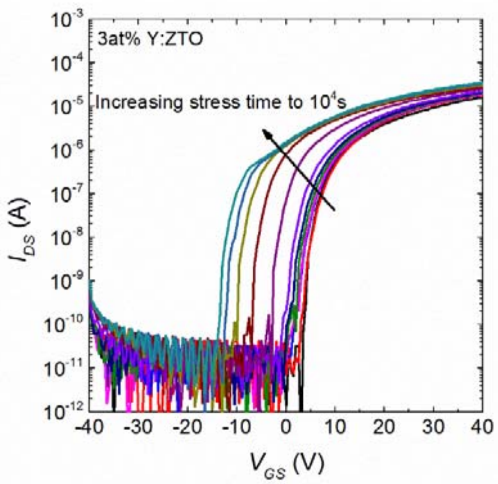
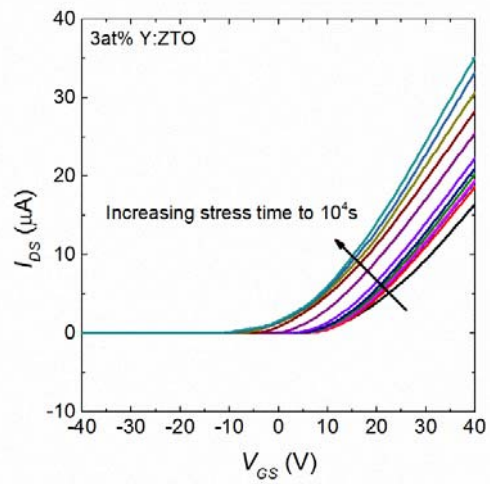
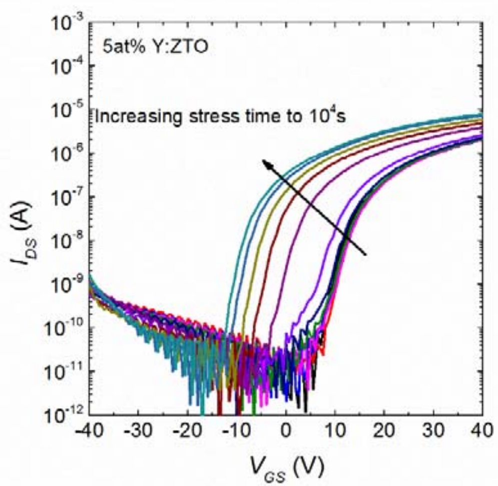
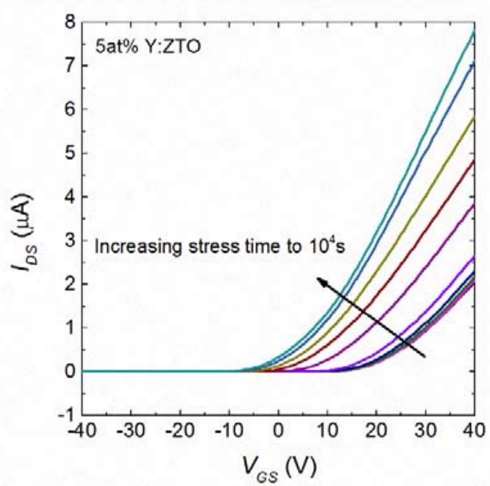
Figure 4-8. Transfer curves of positive bias stressed (PBS) TFTs (a) without back channel passivation and (b) with 40-nm ALD Al_2O_3 as passivation. Extracted parameters showing the PBS change in (c) turn on voltage, (d) subthreshold swing (e) mobility and (f) hysteresis in both passivated and unpassivated devices. Note that the transfer curve measurements at 0.01s and 0.1s are taken back-to-back immediately before stress testing, in order to capture the DC bias stress that occurs during measurement. All transistors have W/L=3000μm/300μm.

4.3.4 Negative bias illumination stress stability

For NBIS, the TFTs were subject to simultaneous negative bias stress (V_{DS} = 0V and V_{GS} = -20V) and illumination stress (green LED with λ = 520-535nm (2.38-2.32eV), I_{light} = 0.9mW/cm^2). The TFT transfer curves shift to more negative voltages. Without

passivation, the transfer curves showed a parallel shift by around -17V for all TFTs regardless of the Y concentration (Figure 4-9).




1at% Y:ZTO
Increasing stress time
to 10^4s
I_{DS} (A)
V_{GS} (V)

1at% Y:ZTO
Increasing stress time to 10^4s
I_{DS} (μA)
V_{GS} (V)

3at% Y:ZTO
Increasing stress time to 10^4s
I_{DS} (A)
V_{GS} (V)

3at% Y:ZTO
Increasing stress time to 10^4s
I_{DS} (μA)
V_{GS} (V)

5at% Y:ZTO
Increasing stress time to 10^4s
I_{DS} (A)
V_{GS} (V)

5at% Y:ZTO
Increasing stress time to 10^4s
I_{DS} (μA)
V_{GS} (V)

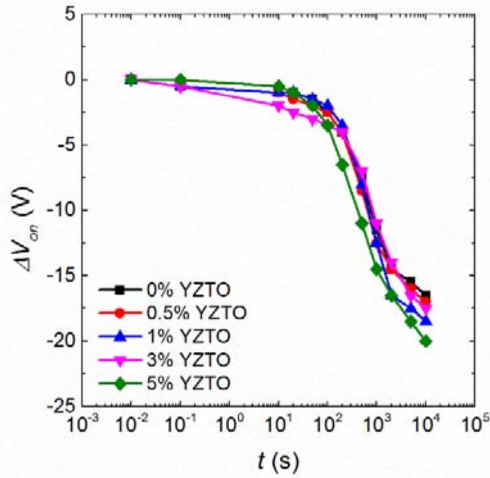
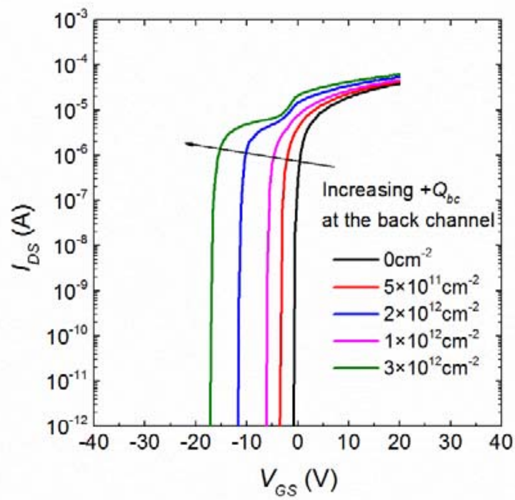


Figure 4-9. NBIS of Y:ZTO TFTs with W/L=3000μm/300μm without passivation. (a) (c) (e) (g) (i) are semilog transfer curves of 0at%, 0.5at%, 1at%, 3at% and 5at% Y:ZTO TFTs under NBIS, respectively, showing V_{ON} shift. (b) (d) (f) (h) (j) are linear plots showing V_{th} shift. (k) V_{ON} shift versus time for devices with different Y concentrations.

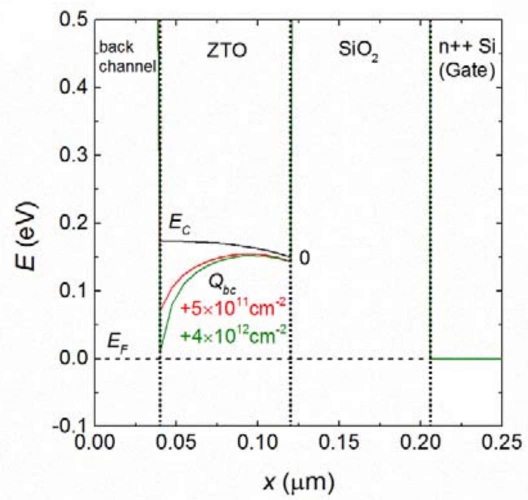
The origin of the NBIS shift for unpassivated devices could be: (1) back channel positive trapped charges; (2) formation of donor states in the bulk; (3) channel interface trap states. In order to determine the possible origins, 2-D numerical simulations were conducted of each of these mechanisms.

(1) Back channel trapped charge. Simulated transfer curves and band diagrams for back channel charge density ranging from 0 to $+3\times10^{12}$cm^{-2} are shown in Figure 4-10 (a) and (b), respectively. A back channel charge density, Q_{bc}, of $+3\times10^{12}$cm^{-2} induces a negative V_{ON} shift of approximately -17V. For Q_{bc}, greater than ~1×10^{12}cm^{-2}, the transfer curve features two turn-ons: one with a more negative V_{ON} and a smaller on-current, the other with a more positive V_{ON} and a larger on-current. This phenomenon can be understood by examining the band structure and current conduction paths for a device with Q_{bc} of $+3\times10^{12}$cm^{-2} under various gate

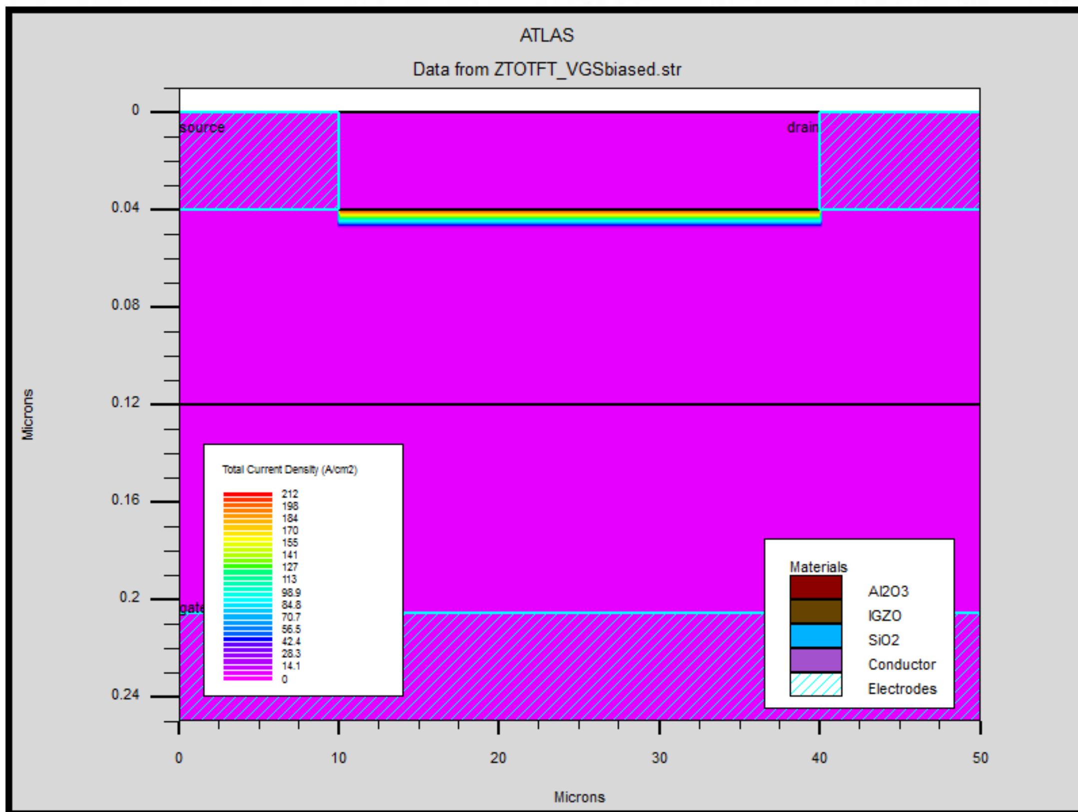
biases. The results are shown in Figure 4-10 (c) and (d). The large, positive Q_{bc} induces severe band bending at the back channel, creating an accumulation layer of mobile electrons. This creates a drain-to-source current path even at V_{GS} = -10V, as visualized in Figure 4-10 (c). As V_{GS} increases, the bottom channel becomes more conductive. At V_{GS} = 20V, the current is mainly conducted through the bottom channel, as shown in Figure 4-10 (d). The top (back) and bottom channels have different on-current levels. This can be explained by the difference in effective capacitance. In the standard FET equation, channel charge and thus I_D is proportional to C_{ox}. At low V_{GS}, when the main conduction path is at the back (top) channel, and the semiconductor and bottom insulator act as series capacitors: $C_{ox} = (C_{SiO2}^{-1} + C_{ZTO}^{-1})^{-1}$, i.e. C_{ox} is smaller than C_{SiO2}. At high V_{GS}, the main conduction path is at the bottom channel and $C_{ox} = C_{SiO2}$. In other words, the bottom gate has much stronger electrostatic influence over the bottom channel compared to the top (back) channel, and therefore the bottom channel carries more current once it is turned on.



I_{DS} (A)
V_{GS} (V)
Increasing $+Q_{bc}$
at the back channel
0cm^{-2}
5×10^{11}cm^{-2}
2×10^{12}cm^{-2}
1×10^{12}cm^{-2}
3×10^{12}cm^{-2}



back channel
ZTO
SiO_2
n++ Si (Gate)
E_C
E_F
Q_{bc}
+5×10^{11}cm^{-2}
+4×10^{12}cm^{-2}
E (eV)
x (μm)



ATLAS
Data from ZTOTFT_VGSbiased.str
source
drain
gate
Microns
Total Current Density (A/cm2)
Materials
Al2O3
IGZO
SiO2
Conductor
Electrodes

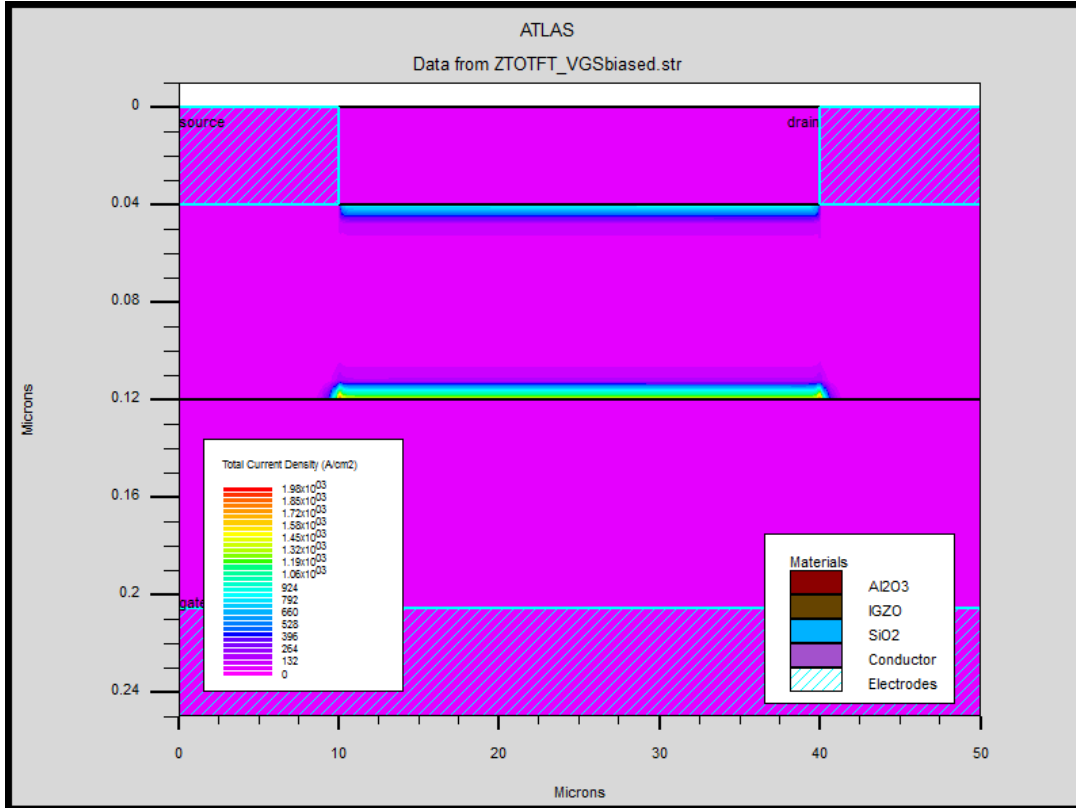
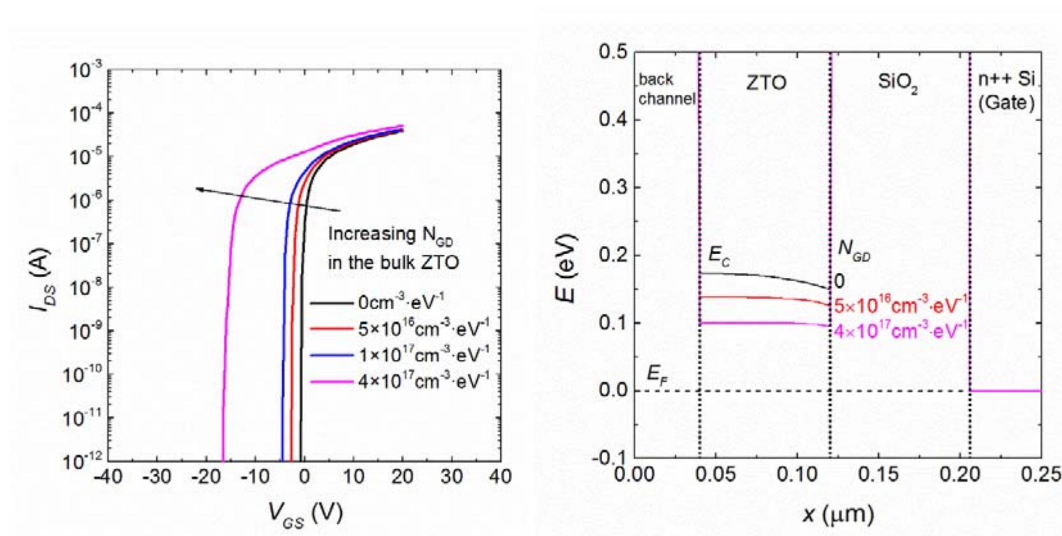
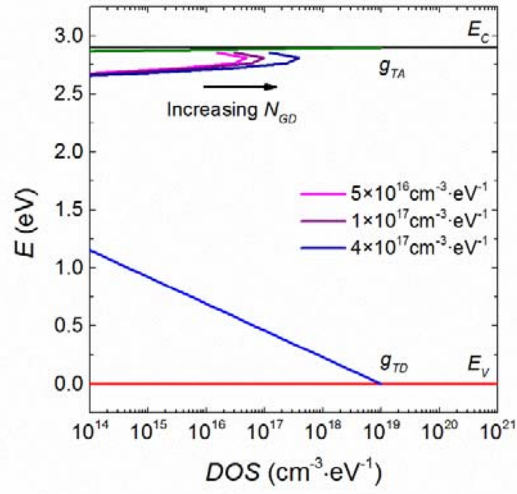


Figure 4-10. (a) Simulated transfer curves of unpassivated ZTO TFTs with back channel trapped charge densities, Q_{bc}, from 0 to $+3\times10^{12}$cm^{-2}. (b) Simulated band diagrams. Simulated current conduction paths of a ZTO TFT with Q_{bc} = $+3\times10^{12}$cm^{-2} with V_{DS} = 1V and (c) V_{GS} = -10V and (d) V_{GS} = 20V. All simulations have N_{GD} = 0, N_{GA} = 0 and Q_{it} = 0.

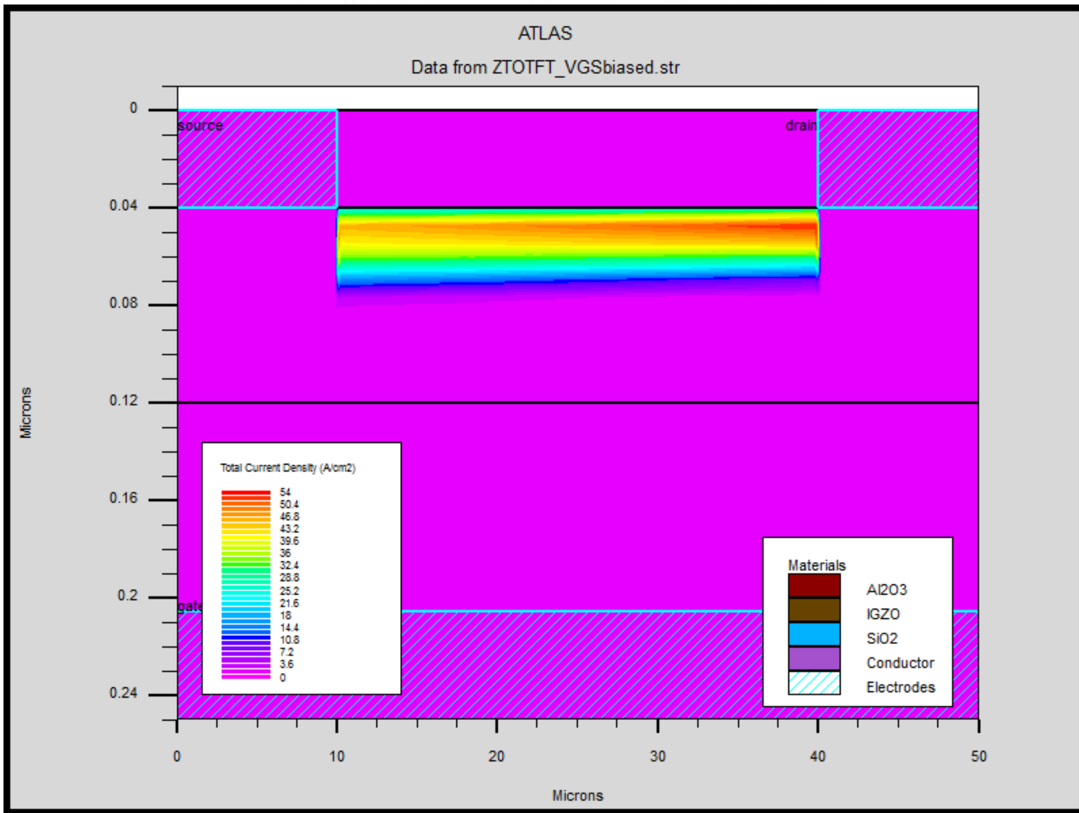
(2) Bulk donor states. Simulated transfer curves, band diagrams and band structures for bulk shallow Gaussian-type donor states with a peak density, N_{GD}, of 0 to 4×10^{17}cm^{-3}·eV^{-1} are shown in Figure 4-11 (a), (b) and (c), respectively. As the density of bulk shallow donors increases, the threshold voltage shifts to more negative voltages. For large donor concentrations, N_{GD}, of greater than ~4×10^{17}cm^{-3}·eV^{-1}, two turn-ons are observed. This can be explained as follows. If a sufficient concentration of bulk shallow donor states exist, they create a bulk ZTO channel which conducts even when the bottom channel, at the semiconductor-gate insulator interface, is turned-off, i.e. at negative gate voltages. The

bulk channel turns on as soon as the gate bias becomes unable to deplete the entire ZTO thickness. This occurs at negative gate biases, as shown in Figure 4-11 (d). The bulk channel is separated from the bottom gate by the (depleted) ZTO and thus has weak capacitive coupling to the gate, and a correspondingly low on current. As the gate bias becomes more positive, electrons are accumulated in the bottom channel, as shown in Figure 4-11 (e). This channel is strongly gate-coupled and thus has a high on-current. These two channels give rise to the two turn-ons observed in the N_{GD} = 4×10^{17}cm^{-3}·eV^{-1} curve in Figure 4-11 (a).





E_C
g_{TA}
Increasing N_{GD}
5×10^{16}cm$^{-3}\cdot$eV^{-1}
1×10^{17}cm$^{-3}\cdot$eV^{-1}
4×10^{17}cm$^{-3}\cdot$eV^{-1}
g_{TD}
E_V
E (eV)
DOS (cm$^{-3}\cdot$eV^{-1})



ATLAS
Data from ZTOTFT_VGSbiased.str
source
drain
gate
Total Current Density (A/cm2)
Materials
Al2O3
IGZO
SiO2
Conductor
Electrodes
Microns
Microns

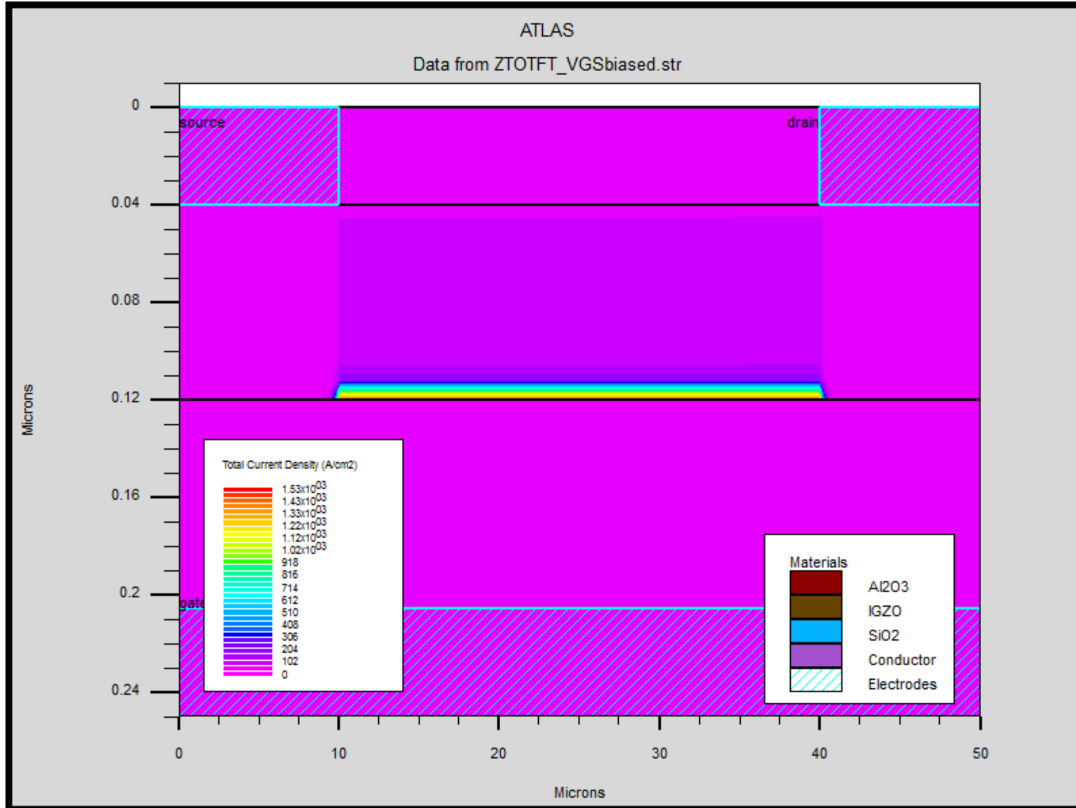
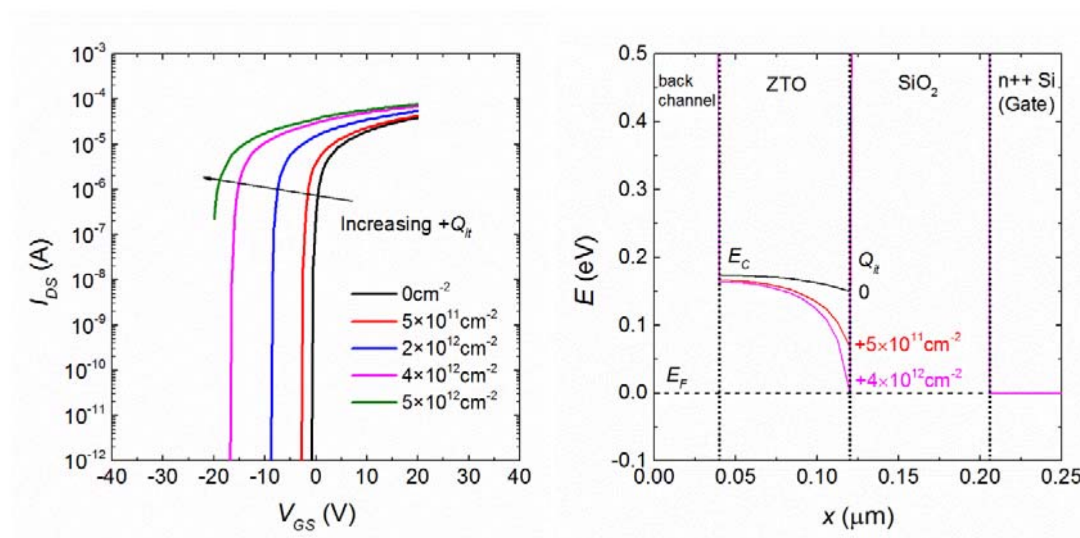
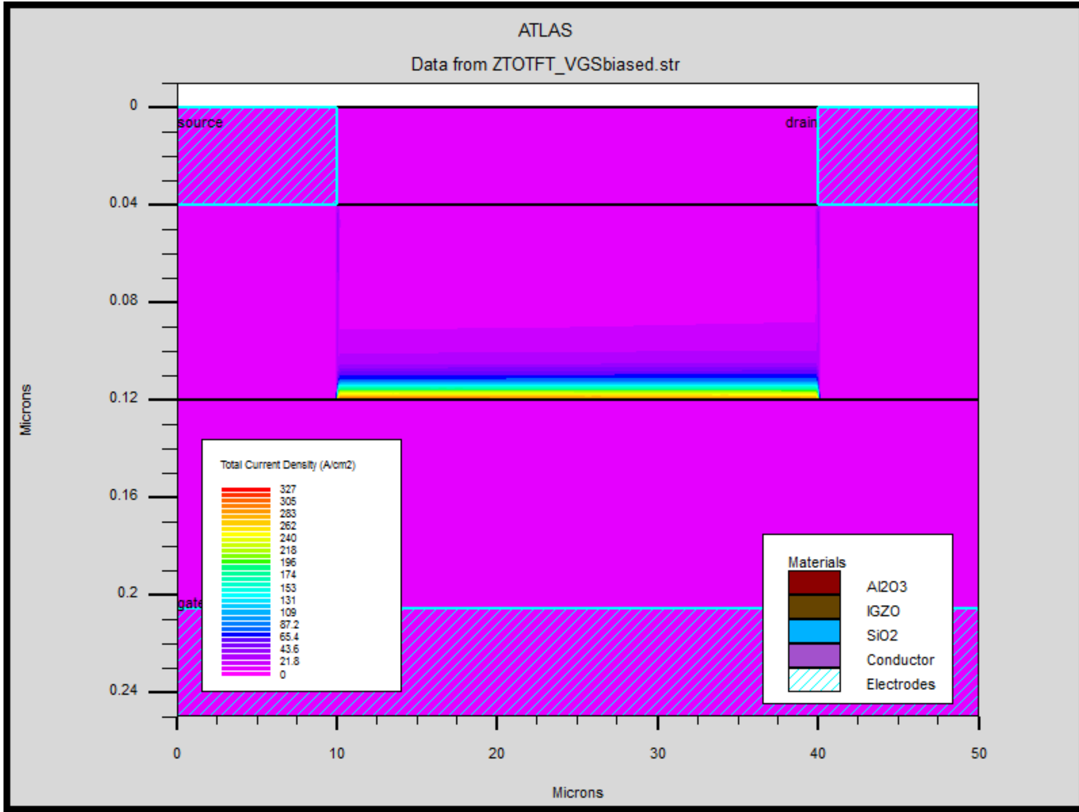


Figure 4-11. (a) Simulated transfer curves of unpassivated ZTO TFTs with increasing bulk shallow Gaussian type donor state densities, N_{GD}, from 0 to $4\times10^{17}cm^{-3}\cdot eV^{-1}$ ($E_{GD} = E_C$ - 0.1eV, W_{GD} = 0.05eV). (b) Simulated band diagrams. Simulated current conduction paths of a ZTO TFT with $N_{GD} = 4\times10^{17}cm^{-3}\cdot eV^{-1}$ with V_{DS} = 1V and (c) V_{GS} = -10V and (d) V_{GS} = 20V. All simulations have N_{GA} = 0, Q_{it} = 0 and Q_{bc} = 0.

(3) Bottom channel interface trapped charge. Simulated transfer curves and band diagrams for bottom semiconductor-insulator interface trapped charge with a density, Q_{it}, equal to 0 to $+5\times10^{12}cm^{-2}$ are shown in Figure 4-12 (a) and (b), respectively. A positive Q_{it} induces a parallel negative shift of the transfer curves, with no secondary turn-on, because the conduction path is always at the bottom channel which is controlled by V_{GS} through C_{SiO2}, as shown in Figure 4-12 (c) and (d).

From the simulation results, it seems that neither trapped charge at the back channel nor the creation of shallow donor states is the dominant origin of the observed NBIS, as the shapes of the simulated transfer curves do not agree with the experimental results. However positive trapped charge at the bottom semiconductor-gate oxide channel interface, with a fixed charge density on the order of $+10^{12}cm^{-2}$, is a possible cause of the observed NBIS instability in unpassivated ZTO and Y:ZTO TFTs. It is noted that the 3at% Y:ZTO TFT transfer curves do show a double turn-on during NBIS, which indicates back channel trapped charge and/or the creation of shallow donor states could exist in these TFTs. The instability is independent of the Y concentration in the film, which indicates that its physical origin is not likely to be related to film chemical composition, but rather to the TFT-environment interaction, similar to the PBS instability described previously in Section 4.3.3.




ATLAS
Data from ZTOTFT_VGSbiased.str
source
drain
gate
Microns
0
0.04
0.08
0.12
0.16
0.2
0.24
Total Current Density (A/cm2)
327
305
283
262
240
218
196
174
153
131
109
87.2
65.4
43.6
21.8
0
Materials
Al2O3
IGZO
SiO2
Conductor
Electrodes
0
10
20
30
40
50
Microns

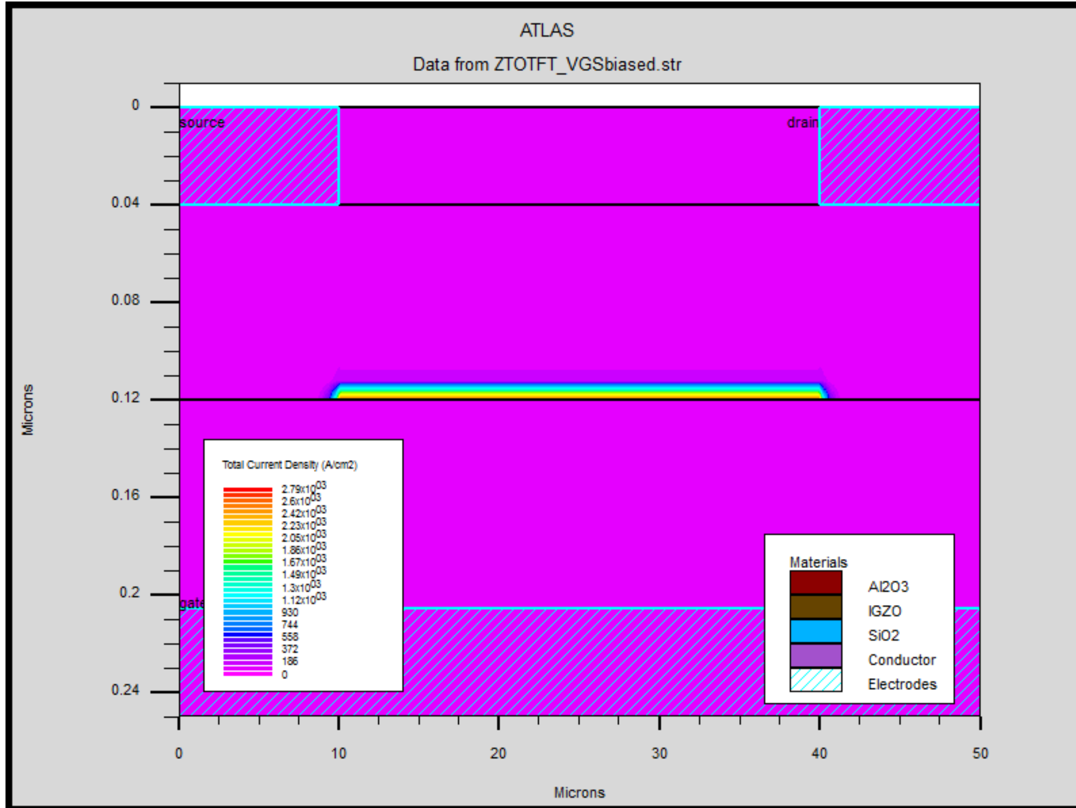
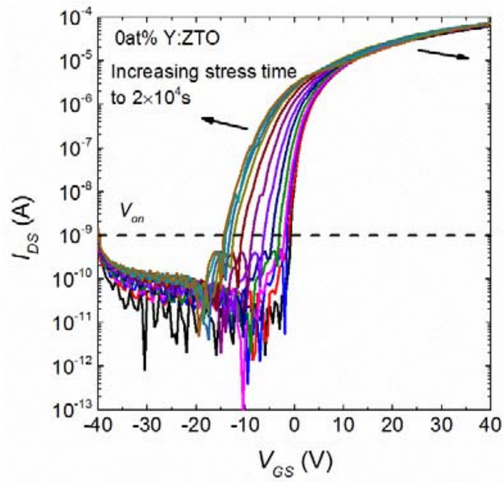
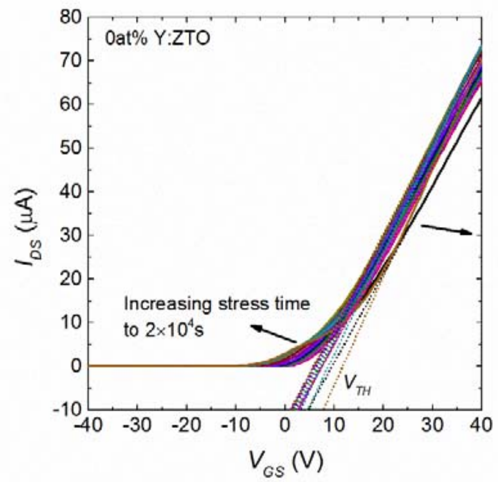


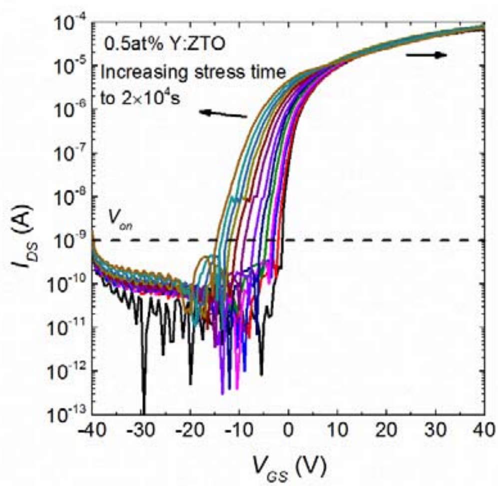
Figure 4-12. (a) Simulated transfer curves of unpassivated ZTO TFTs with bottom channel interface charge densities, Q_{it}, ranging from 0 to $+5\times10^{12}$cm^{-2}. (b) Simulated band diagrams. Simulated current conduction paths of a ZTO TFT with Q_{it}=$+4\times10^{12}$cm^{-2} with V_{DS} = 1V and (c) V_{GS} = -10V and (d) V_{GS} = 20V. All simulations have N_{GD} = 0, N_{GA} = 0 and Q_{bc} = 0.

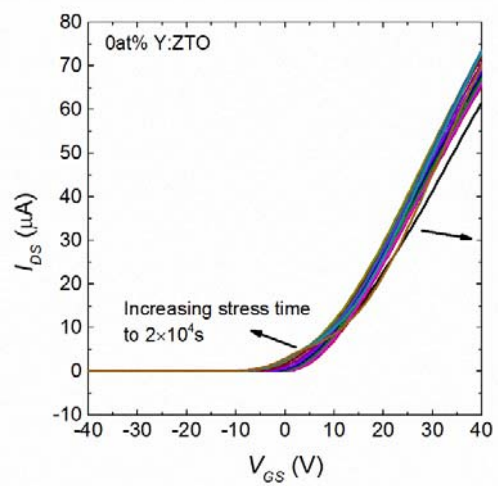
In order to minimize the NBIS threshold voltage shifts induced by environmental interactions, we characterized NBIS for Y:ZTO TFTs with 40-nm ALD Al_2O_3 passivation. As shown in Figure 4-13, after passivation, the stressed TFT transfer curves show a double turn-on. The voltage shifts due to NBIS are affected by two competing mechanisms: in the subthreshold region, V_{ON} shifts negatively, while in the linear region, V_{TH} shifts to slightly more positive voltages. (V_{ON} is the V_{GS} at I_{DS} = 1nA and V_{TH} is extracted in the linear region using $I_{DS} = \mu_n C_{ox}(W/L)(V_{GS} - V_{TH})V_{DS}$.) The existence of these competing mechanisms

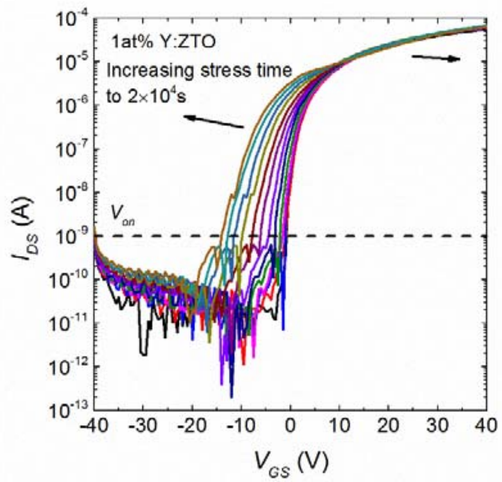
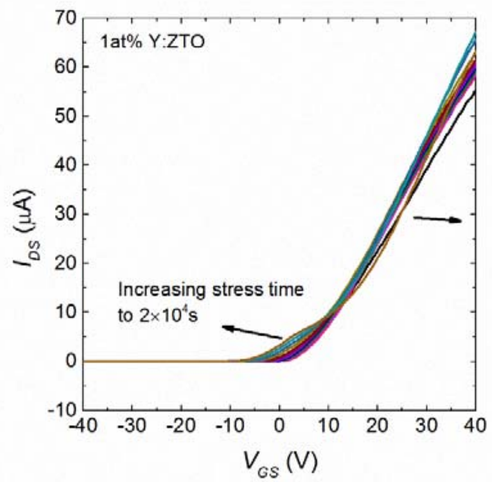
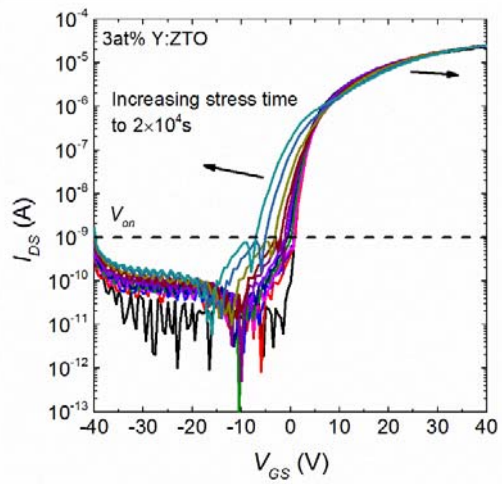
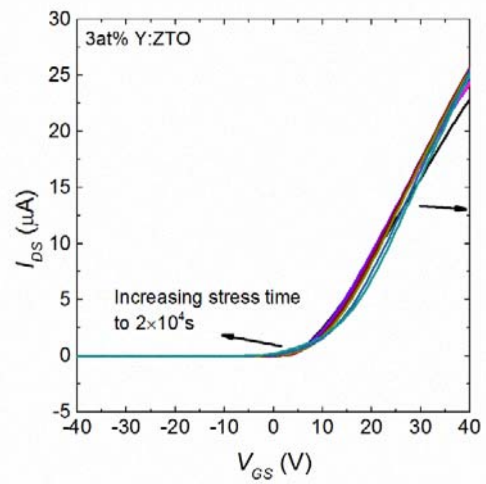
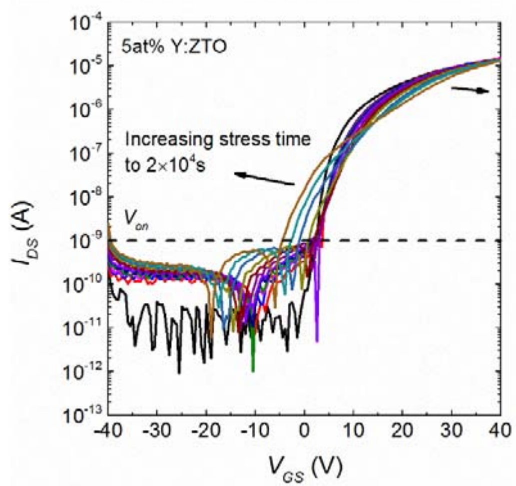
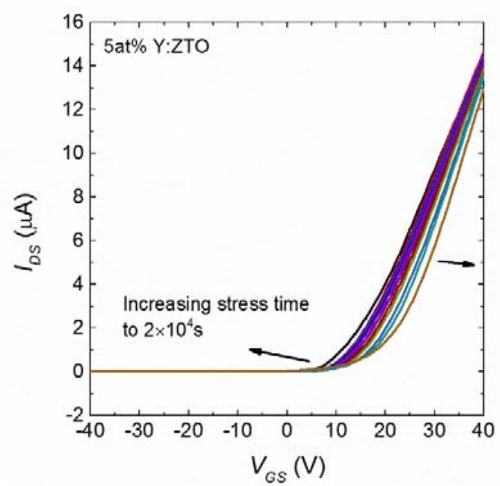
indicates that NBIS instabilities in passivated Y:ZTO TFTs are likely due to multiple processes with different physical origins.










1at% Y:ZTO
Increasing stress time to 2×10⁴s
V_{on}
I_{DS} (A)
V_{GS} (V)

1at% Y:ZTO
Increasing stress time to 2×10⁴s
I_{DS} (μA)
V_{GS} (V)

3at% Y:ZTO
Increasing stress time to 2×10⁴s
V_{on}
I_{DS} (A)
V_{GS} (V)

3at% Y:ZTO
Increasing stress time to 2×10⁴s
I_{DS} (μA)
V_{GS} (V)

5at% Y:ZTO
Increasing stress time to 2×10⁴s
V_{on}
I_{DS} (A)
V_{GS} (V)

5at% Y:ZTO
Increasing stress time to 2×10⁴s
I_{DS} (μA)
V_{GS} (V)

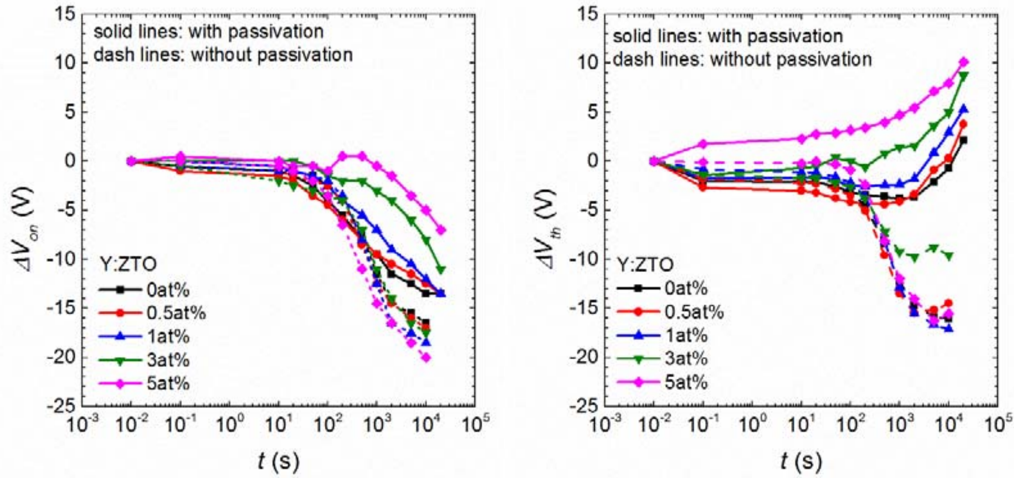


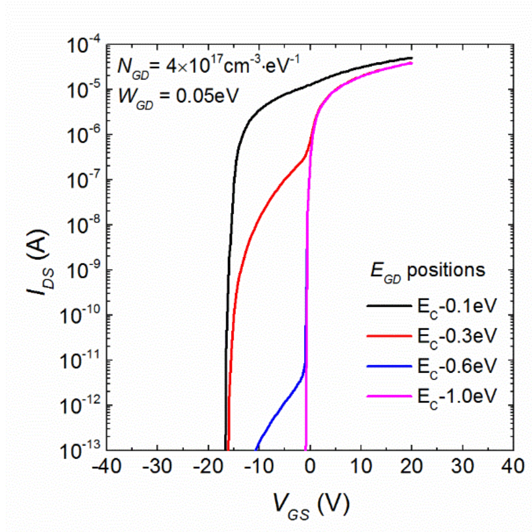
Figure 4-13. NBIS of Y:ZTO TFTs with W/L=3000μm/300μm with 40-nm ALD Al_2O_3 passivation. (a) (c) (e) (g) (i) are semi-log transfer curves of 0at%, 0.5at%, 1at%, 3at% and 5at% Y:ZTO TFTs under NBIS, respectively, showing V_{ON} shift. (b) (d) (f) (h) (j) are linear plots showing V_{TH} shift. Summary plots of: (k) V_{ON} shifts (l) V_{TH} shifts versus stress time.

From the previous simulations, it was seen that a double turn-on in the transfer curves could be caused by bulk Gaussian donor states and/or by back channel interface trapped charge. Therefore, more simulations were carried out to interpret the double turn-on and the negative V_{ON} shifts observed for passivated Y:ZTO TFTs under NBIS stress. In particular, we used 2-D numerical simulations to analyze the effect of possible NBIS-induced changes in sub-gap states and the roles of Y on density of states.

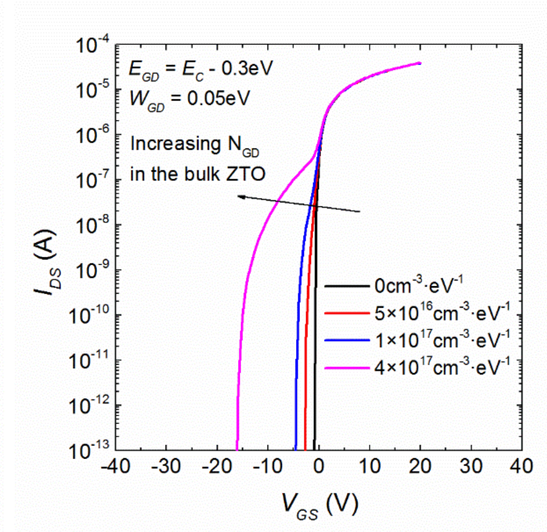
We first modeled TFT behavior for bulk Gaussian donor states with various peak positions (E_{GD}) and peak concentrations (N_{GD}). As shown in Figure 4-14 (a), the peak position of the bulk Gaussian donor states, E_{GD}, strongly influences the current in the bulk channel (i.e., the current after the first turn-on, before the second turn-on occurs). The further away the donors are from the conduction band, the lower the current of the first turn-on. This is because, at a given temperature, a larger E_C to E_{GD} gap means that fewer

electrons are thermally activated into the conduction band, where they can contribute to conduction as mobile charge carriers. By quantitatively comparing the ratio of the on-current in the bulk and bottom channels in simulation versus experimental results, we conclude that NBIS creates bulk Gaussian donor states that are energetically centered at an E_{GD} between E_C - 0.2eV and E_C - 0.3eV.

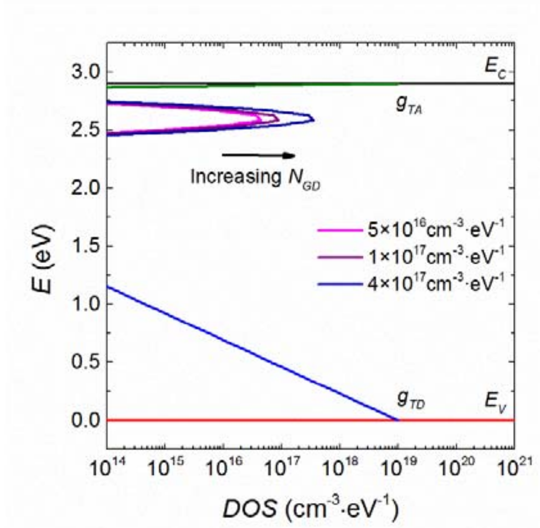
At a given peak energy level, the magnitude of the negative V_{ON} shift is directly related to the peak donor state density, N_{GD}. A peak density of 4×10^{17}cm$^{-3}\cdot$eV^{-1} or larger is needed to shift V_{ON} by more than -10V (Figure 4-14 (b) and (c)). Instead of severely bending the energy bands, these states only slightly shift the Fermi level closer to the conduction band (Figure 4-14 (d)), and therefore do not significantly affect the on current level. By plotting the 2-D spatial distribution of current density for different gate biases, we confirm that the dual turn-on is due to a shift in the main current conduction path from the bulk, close to the back channel, toward the bottom channel (Figure 4-14 (e), (f) and (g)). That is to say, even though the Gaussian donor states modelled here fall deeper in the bandgap, $E_{GD} = E_C$ - 0.3eV, than the previous simulations shown in Figure 4-11, $E_{GD} = E_C$ - 0.1eV, the same conduction mechanisms apply.



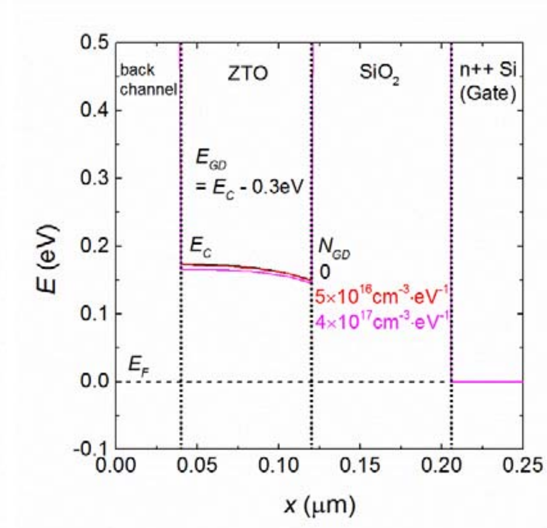
N_{GD}= 4×10^{17}cm^{-3}·eV^{-1}
W_{GD} = 0.05eV
E_{GD} positions
E$_C$-0.1eV
E$_C$-0.3eV
E$_C$-0.6eV
E$_C$-1.0eV
I_{DS} (A)
V_{GS} (V)



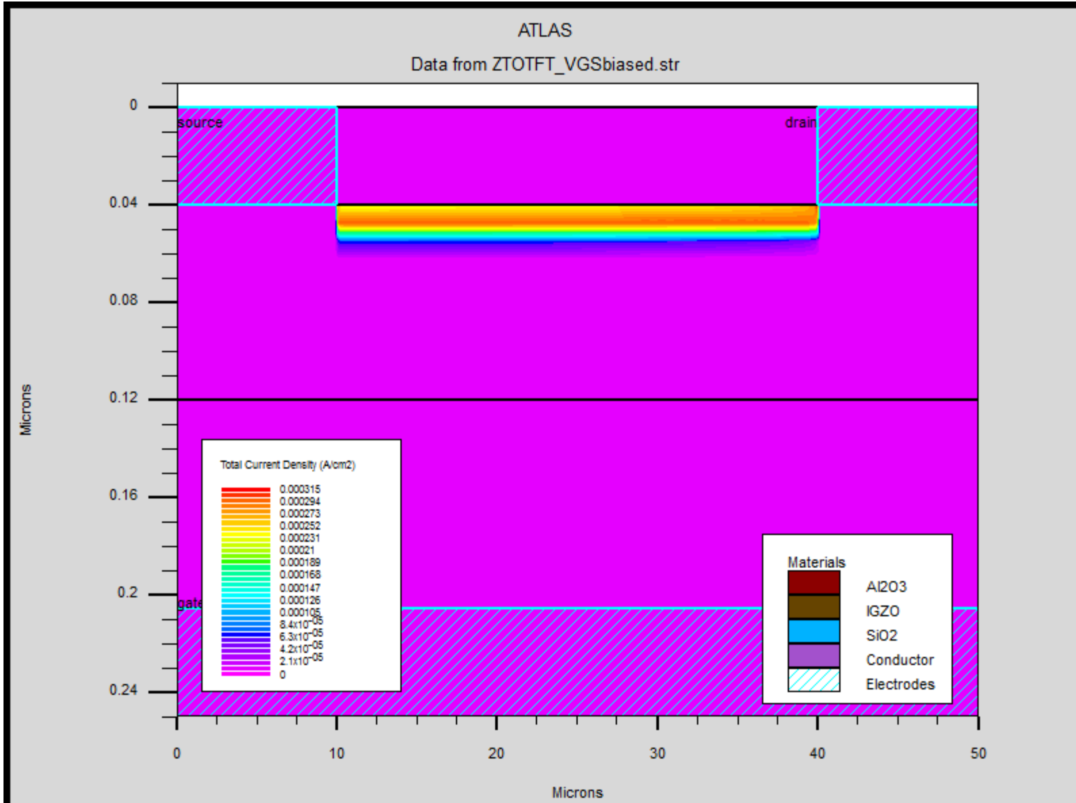
E_{GD} = E_C - 0.3eV
W_{GD} = 0.05eV
Increasing N$_{GD}$
in the bulk ZTO
0cm^{-3}·eV^{-1}
5×10^{16}cm^{-3}·eV^{-1}
1×10^{17}cm^{-3}·eV^{-1}
4×10^{17}cm^{-3}·eV^{-1}
I_{DS} (A)
V_{GS} (V)

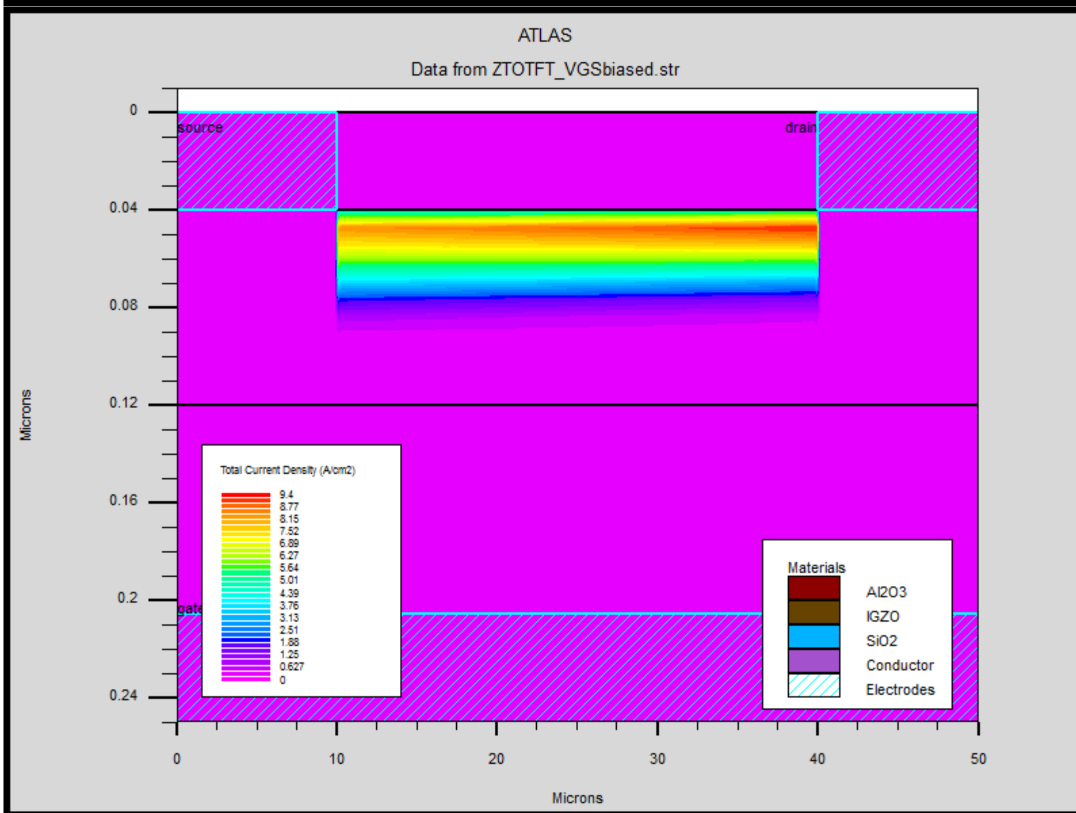


E_C
g_{TA}
Increasing N_{GD}
5×10^{16}cm^{-3}·eV^{-1}
1×10^{17}cm^{-3}·eV^{-1}
4×10^{17}cm^{-3}·eV^{-1}
g_{TD}
E_V
E (eV)
DOS (cm^{-3}·eV^{-1})



back channel
ZTO
SiO$_2$
n++ Si (Gate)
E_{GD} = E_C - 0.3eV
E_C
N_{GD}
0
5×10^{16}cm^{-3}·eV^{-1}
4×10^{17}cm^{-3}·eV^{-1}
E_F
E (eV)
x (μm)


ATLAS
Data from ZTOTFT_VGSbiased.str
0
0.04
0.08
0.12
0.16
0.2
0.24
Microns
source
drain
Total Current Density (A/cm2)
0.000315
0.000294
0.000273
0.000252
0.000231
0.00021
0.000189
0.000168
0.000147
0.000126
0.000105
8.4x10-05
6.3x10-05
4.2x10-05
2.1x10-05
0
Materials
Al2O3
IGZO
SiO2
Conductor
Electrodes
0
10
20
30
40
50
Microns


ATLAS
Data from ZTOTFT_VGSbiased.str
0
0.04
0.08
0.12
0.16
0.2
0.24
Microns
source
drain
Total Current Density (A/cm2)
9.4
8.77
8.15
7.52
6.89
6.27
5.64
5.01
4.39
3.76
3.13
2.51
1.88
1.25
0.627
0
Materials
Al2O3
IGZO
SiO2
Conductor
Electrodes
0
10
20
30
40
50
Microns

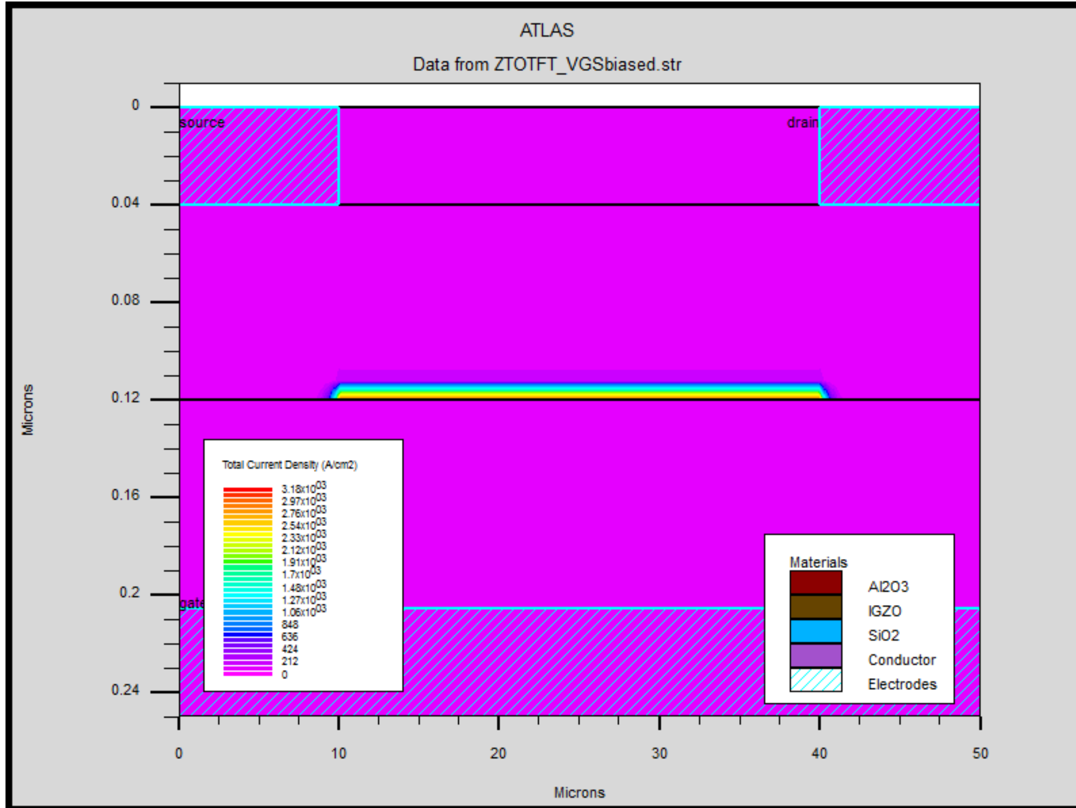


Figure 4-14. Simulated transfer curves of passivated ZTO TFTs with (a) different bulk Gaussian donor state peak positions from E_{GD} ranging from E_C - 0.1eV to E_C - 1eV, with N_{GD} fixed at 4×10^{17} $cm^{-3}\cdot eV^{-1}$, and (b) with increasing bulk Gaussian type donor state densities, N_{GD}, from 0 to $4\times10^{17} cm^{-3}\cdot eV^{-1}$, with E_{GD} fixed at E_C - 0.3eV. (c) Simulated band structures and (d) band diagrams with E_{GD} = E_C - 0.3eV. Simulated current conduction paths of a ZTO TFT with $N_{GD}=4\times10^{17} cm^{-3}\cdot eV^{-1}$ with V_{DS} = 1V and (e) V_{GS} = -15V, (f) V_{GS} = -5V and (g) V_{GS} = 20V. For all simulations, W_{GD} = 0.05eV, as listed in Table 4-2.

Another potential cause of the dual turn-on is a Gaussian distribution of states at the back channel Al_2O_3/ZTO interface (in addition to a fixed trapped charge Q_{bc}). This is shown in the simulations of Figure 4-15. A Gaussian distribution of donor states at the back channel, with a peak position of E_C - 0.1eV and a density on the order of $10^{12} cm^{-2}\cdot eV^{-1}$ at the interface could cause a V_{ON} shift similar to the experimental results. From the present experimental data, it is not possible to conclusively determine whether the observed NBIS

behavior for passivated devices is due to Gaussian-distributed donor states within the bulk ZTO or a similar Gaussian DOS at the back channel interface.

No matter what the origin, this dual turn-on is undesirable for practical TFT applications. As can be seen in Figure 4-13, with > 1at% Y, the V_{ON} shift is reduced for the same amount of stress time, indicating that Y incorporation may suppresses the formation of bulk or back-channel Gaussian donor states. Based on the propensity of yttrium to strongly bond with oxygen, these states are likely related to ionized oxygen vacancies.

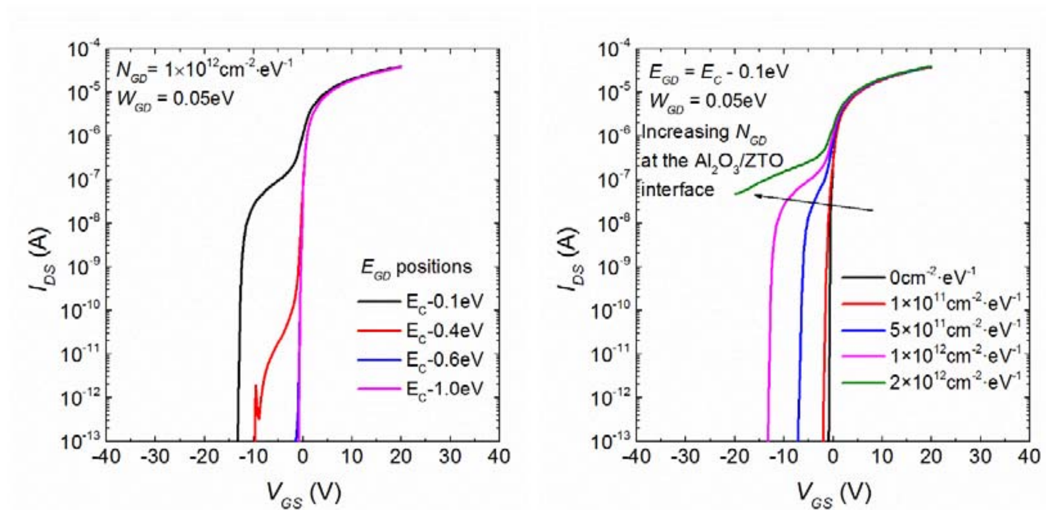


Figure 4-15. Simulated transfer curves of unpassivated ZTO TFTs with (a) different back channel interface Gaussian donor state peak positions from E_C - 0.1eV to E_C - 1eV and with (b) increasing back channel interface Gaussian type donor state densities from 0 to $2\times10^{12}cm^{-2}\cdot eV^{-1}$ (E_{GD} = E_C - 0.1eV, W_{GD} = 0.05eV).

The observed simultaneous positive V_{TH} shift under NBIS can be related to an increasing density of deep level Gaussian acceptor-like states [163] (Figure 4-16). These acceptor states, either created in the bulk semiconductor or at either semiconductor-

insulator interface, could deplete the free electrons, causing a positive V_{TH} shift. Simulation showed that the peak density of these acceptor-like states needs to be on the order of $10^{17}cm^{-3}\cdot eV^{-1}$ to cause a V_{TH} shift of several volts. Higher concentrations of Y in ZTO tends to increase the rate at which these acceptor states are generated, which indicates these defects are likely not related to oxygen vacancies, but rather related to structural disorder or loosely bonded oxygen/water species.

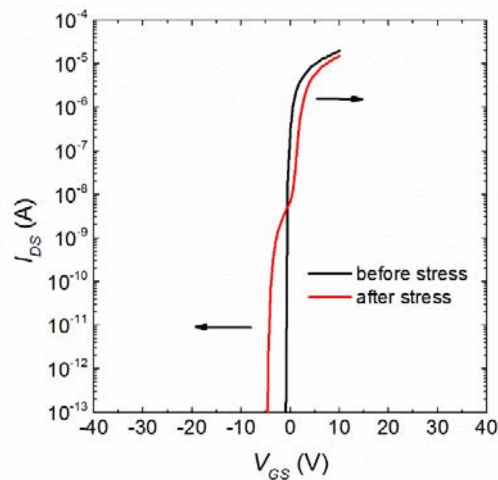
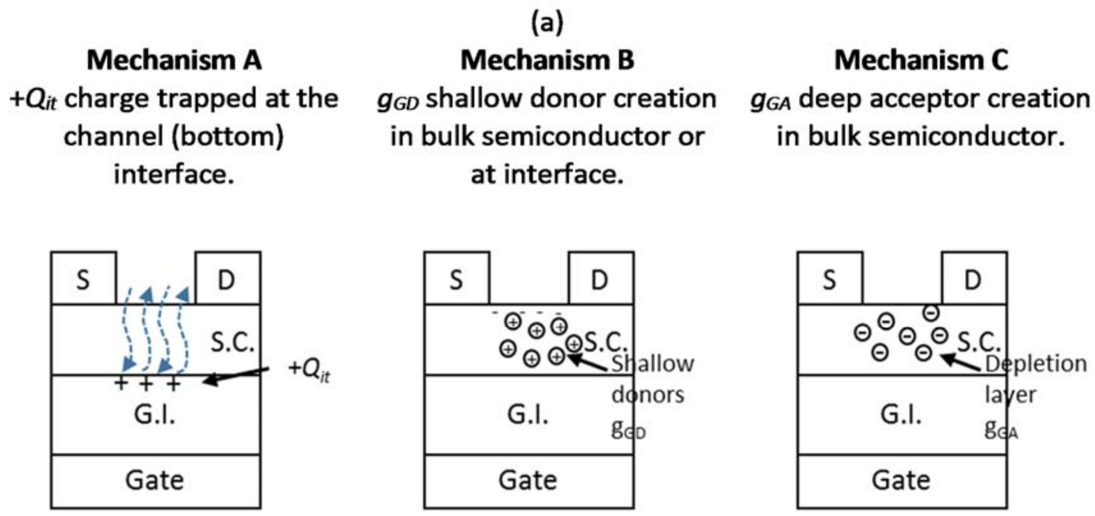


Figure 4-16. Simulated shift of both V_{ON} and V_{TH} in a ZTO TFT under NBIS. The device before stress is modelled with $N_{GD} = N_{GA} = Q_{it} = Q_{bc} = 0$. The device after stress is modelled with two additional Gaussian distributions of states: a shallow, narrow distribution of donor states (E_{GD} = E_C - 0.3eV, $N_{GD} = 2\times10^{17}cm^{-3}\cdot eV^{-1}$, W_{GD} = 0.05eV), and a deep, broad distribution of acceptor states (E_{GA} = E_C -1.34eV, $N_{GA} = 1\times10^{17}cm^{-3}\cdot eV^{-1}$, W_{GD} = 0.2eV) in the bulk ZTO.

In summary, the NBIS instability of solution-processed Y:ZTO TFTs can mainly be attributed to three mechanisms, illustrated in Figure 4-17: (A) $+Q_{it}$ charge trapped at the channel (bottom) interface; (B) g_{GD} shallow donor creation in bulk semiconductor or at interface; (C) g_{GA} deep acceptor creation in bulk semiconductor. Mechanisms A and B both shift V_{ON} negatively. Mechanism A dominates when the devices are not passivated,

whereas mechanism B becomes more obvious when the devices are passivated. Mechanism C counteracts mechanisms A and B, positively shifting V_{TH} and V_{ON}. Mechanism B is weakened by Y doping, but mechanism C is enhanced by Y doping. Therefore, a careful selection of Y concentration is essential to obtaining stable Y:ZTO TFTs.



Results:	Results:	Results:
• Negative V_{ON} and V_{TH} shift. • Worse in unpassivated devices. • Limited effect in passivated devices.	• Negative V_{ON} shift. Only affects V_{ON}. • Top channel turns-on before bottom channel, with carrier density n_e << n_{ch}. • Shift is weaker for higher Y concentration.	• Positive V_{ON} and V_{TH} shifts. • Shifts are larger for higher Y concentration.

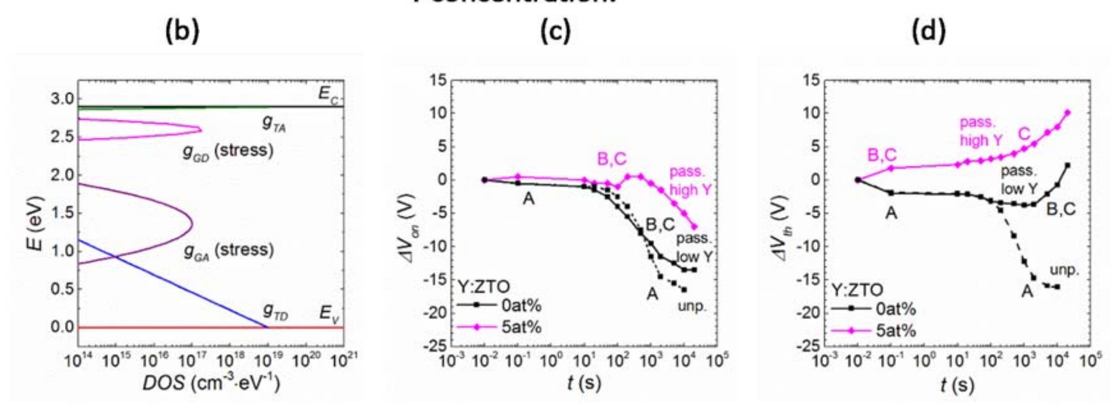


Figure 4-17. (a) Mechanisms A, B, and C and (b) band structure components causing Y:ZTO NBIS instability. (c) and (d) illustrate the contributions of the three mechanisms to the observed NBIS instability.

4.4 Conclusions and future work

4.4.1 Conclusions

The effects of Y on solution processed ZTO TFTs have been studied using DC and electrical bias stress measurements. The addition of a low Y concentration (<1at%) slightly improves TFT DC performance, while a higher Y concentration compromises TFT performance, likely due to increased structural disorder and formation of electrically insulating phases with the oxide film. Without passivation, both positive bias stress (PBS) and negative bias illumination stress (NBIS) cause large positive and negative voltage shifts in the transfer curves, respectively. Passivation of the backchannel with 40-nm ALD Al_2O_3 virtually eliminates positive bias stress (PBS) effects for both Y-doped and undoped ZTO TFTs. Under NBIS, the presence of Y in ZTO stabilizes the negative shift of V_{ON}, likely due to yttrium's suppression of the formation of ionized oxygen vacancies. However, V_{TH} extracted from the linear region is shifted positively, possibly due to the formation of deep-level acceptor states. Y act both as oxygen getter and as acceptor-type defect creator. Therefore using a high concentration of Y in Y:ZTO is a trade-off between device DC performance and device stress stability. It is crucial to carefully choose the doping concentration to achieve optimal device performance.

4.4.2 Outstanding scientific questions and future work

Several outstanding scientific questions remain:

(1) Structurally, what do Sc and Y do in ZTO? Even though the effects of Y on the band structure close to the conduction band were studied via stress measurements, the

physical origins of these effects are still unclear. Further material analyses such as atomic probe tomography or theoretical analysis such as band-structure calculations via density functional theory could better connect the atomic structures with the electronic properties.

(2) What is the effect of Sc and Y on deep-level subgap states in ZTO? Even though the NBIS stability study offers some insight, it cannot provide accurate band structure information. A combination of optical and electrical characterization techniques may be able to reveal more about the deep-level band structures, such as deep-level transient spectroscopy (DLTS) or optical-DLTS.

(3) How can we achieve better stability without compromising device performance? As can be seen, there is a tradeoff between NBIS stability and device performance. Whether there is an optimal film stoichiometry or deposition process and whether other materials or techniques would provide better electrical performance, remain open questions. For instance, co-doped films such as Y:In-Zn-Sn-O may provide higher mobility due to the incorporation of indium while yttrium provides improved stability.

Chapter 5 Yttrium and scandium in zinc oxide as transparent conductive oxides

5.1 Introduction

Transparent conductors are crucial for applications that require simultaneous optical transparency and electrical conductivity, such as interconnect on flat-panel displays and solar cells. At present, the most widely used material is the transparent conducting oxide (TCO) indium tin oxide (ITO), which typically has a resistivity of 1-3×10^{-4}Ω·cm and an average transparency of 90% throughout the visible range [164]. However, the scarcity and price of indium has become a barrier to expanded use of ITO [165]. Compared with ITO, zinc oxide (ZnO)-based TCOs have lower cost, are non-toxic and are more stable in hydrogen plasma [166]. ZnO-based TCOs are also readily deposited through solution processes, such as spray coating, dip coating and ink-jet printing, which could enable lower cost, large area and roll-to-roll TCO fabrication.

ZnO is typically an n-type semiconductor due to intrinsic doping related to hydrogen and oxygen states as well as zinc interstitials [167], [168]. To control and lower the resistivity of ZnO, typically electron donors with three valence electrons are added to ZnO. To facilitate conduction, these donors should substitute for Zn in the lattice and thermally release a mobile electron. Group III A elements, including B, Al, Ga and In, have been successfully used as electron donors in ZnO [169], [170].

As the first two elements in Group III B, Sc and Y have similar ionic radii to Zn, making them suitable atoms for substitutional doping. They strongly bond to oxygen due to their large negative Gibbs energy of formation compared with other oxides (Table 5-1). This may reduce undesirable oxygen vacancy defects in the film. Moreover, yttrium and scandium oxide are chemically resistant and relatively non-hygroscopic compared to other Group III B oxides such as La_2O_3 [171]. Only a few studies have focused on electrical properties of Sc or Y doped ZnO, notated here as Sc/Y:ZnO, which is sometimes co-doped with aluminum, as summarized in Table 5-2. Other group III B rare earth elements suffer from weaker oxygen bonding or hygroscopic behavior, and have not been extensively studied as ZnO electrical dopants [172], [173]. There is a discrepancy in the observed Sc or Y doping effect on ZnO electrical properties. Some studies showed that ZnO resistivity could be minimized by doping with a low weight or atomic percentage of Sc or Y, while other studies showed a trivial change or even an increase in resistivity when Sc or Y are added [174]–[176]. According to density-functional theory (DFT) studies, Y doping is expected to result in a decrease in conductivity. Imai and Watanabe [177] found that 0.9 at% Al doping or 0.9 at% Y doping of ZnO cause a similar shift of the Fermi level into the conduction band (CB), likely due to a shift of the Zn 3d and O2p-based valence bands to lower energies [178]. However the composition of the CB is very different in the two materials. Al (or Ga or In) doping results in a broad, delocalized Al3s (Ga4s, In 5s) state and hybridized Al3p (Ga4p, In 5p) state, in addition to the Zn 4s and 4p states, i.e. the Al (or Ga, or In) donates a mobile electron to the ZnO. In contrast, for Y-doped ZnO the hybridized Y 4d and 5p electron states are predicted to be at energies far above the CB.

That is, the ytrrium $4d^1$ electron may be highly localized and cannot act as a mobile electron. Furthermore, increasing Y doping in ZnO from 0.9 at% to 2.8 at% is predicted by DFT to increase free charge carrier localization, causing a concurrent decrease in conductivity [178].

To understand and clarify these conflicting trends in theoretical predictions and experiments, here we investigated the role of Sc and Y in solution processed Sc:ZnO and Y:ZnO thin films. We found that, as predicted by theory, Sc or Y doping decreases film conductivity. Using x-ray photoelectron spectroscopy (XPS) and scanning spreading resistance microscopy (SSRM), we attribute the decrease not only to charge localization but also to phase segregation of insulating oxides at nanocrystalline grain boundaries. After annealing the films in forming gas, the Sc/Y:ZnO films were still more resistive than undoped ZnO and showed a stronger thickness dependence of resistivity. Using electrical modeling and XPS depth profiles, we found that the variation in thickness dependence of resistivity may be due to depletion of the top surface and grain-boundaries of Sc/Y:ZnO nanostructures by Sc and Y oxide formation.

Table 5-1. The Gibbs energy of formation of ZnO and Group III A and Group III B oxides, from [45]

Oxide	**$\Delta_f G^0$ (c) (kJ/mol)**
Sc_2O_3	-1819.4
Y_2O_3	-1816.6
Al_2O_3	-1582.3
Ga_2O_3	-998.3
In_2O_3	-830.7
ZnO	-320.5

Table 5-2. Electrical and optical properties of previously published Sc:ZnO and Y:ZnO. The starred studies (*) did not show a decrease in resistivity when the dopants were introduced.

Material	**Deposition tech**	**Post deposition annealing**	**Doping fraction**	***ρ* (Ω·cm)**	***T* (%)**	***t* (nm)**	**Ref No.**
			Sol-gel Sc/Y:ZnO				
Sc:ZnO	Spin-coating	-	0.5 wt%	3.5×10^{-4}	90	500	[179]
	Hydro-thermal	-	0.3 at%	5.0×10^{-2}	75	5×10^{5}	[180]
Y:ZnO	Dip-coating	H_2/N_2, 500°C, 1h	0.5 at%	6.8×10^{-3}	90	300	[176]
	Electro-deposition	N_2, 300°C, 3h	9 at%	6.3×10^{-5}	80	400	[181]
	Spin-coating	-	3 wt%	3.5×10^{-2}	85	250	[182]
	Spin-coating	-	3 wt%	5.8×10^{-3}	80	400	[183]
Sc:AlZnO	Dip-coating	Vacuum, 400°C, 30min	0.5 at%	2.9×10^{-2}	73	-	[174]*
Y:AlZnO	Co-precipitation		0.2 wt%	4.6×10^{-3}	-	-	[175]*
			Vacuum-deposited Sc/Y:ZnO				
Sc:ZnO	Sputtering	-	2 wt%	3.1×10^{-4}	85	1040	[184]
	Sputtering	-	2 wt%	7.7×10^{-2}	90	-	[185]
Y:ZnO	Sputtering	-	4 wt%	7.9×10^{-4}	-	-	[184]
Sc:AlZnO	Sputtering	-	1.7 wt%	1.3×10^{-3}	~90	230	[186]

5.2 Experimental

Sc/Y:ZnO thin films were spin-coated on Corning Eagle XG glass pieces, with the exception of the Y:ZnO samples used for scanning spreading resistance microscopy, which was deposited on n-type heavily Sb-doped <100> silicon wafer pieces (ρ = 0.01–0.02 Ω·cm).

The inks were prepared by separately dissolving 0.5M metal precursors zinc acetate dihydrate ($Zn(CH_3COO)_2 \cdot 2H_2O$, Sigma-Aldrich, 99.999%), scandium nitrate hydrate ($Sc(NO_3)_3 \cdot xH_2O$, Sigma-Aldrich, 99.9%), and yttrium nitrate hexahydrate ($Y(NO_3)_3 \cdot 6H_2O$, Sigma-Aldrich, 99.8%) in 2-methoxyethanol ($CH_3OCH_2CH_2OH$, Sigma-Aldrich, anhydrous, 99.8%), with 0.5M ethanolamine ($NH_2CH_2CH_2OH$, Sigma-Aldrich, anhydrous, 99.5%) as a stabilizer. After stirring the individual solutions for more than 4 hours, the Sc solution or the Y solution was added to the Zn solution, to obtain ink mixtures with 0.5wt% and 1.5wt% (0.9at% and 2.7at%) Sc:ZnO, and 1wt% and 3wt% (0.9at% and 2.8wt%) Y:ZnO. All the solutions were prepared at room temperature in nitrogen, as the scandium nitrate and yttrium nitrate precursors are hygroscopic.

Right before spin-coating, the glass pieces were cleaned by acetone and isopropanol alcohol in an ultrasonic bath for 10min each, and then treated by oxygen plasma. The mixed inks were filtered and then spun on to the substrates at 3000 rpm for 40 s in air. The samples were then dried in air at 300°C for 1 min to evaporate the solvents and to initiate chemical decomposition. The spin-coating and drying steps were repeated to obtain samples with 3, 9, 15, or 30 layers. After the final drying step, the samples were

annealed at 500°C for 1 h in air to fully decompose the precursors and form metal-oxygen bonds. We refer to these samples as 'as-deposited'. Some as-deposited samples were further annealed in forming gas (H_2/N_2 = 5/95%) at 300°C for 10 min to further reduce resistivity. These are referred to as 'FG annealed' samples.

The thickness of the films were measured by a Dektak surface profilometer. The results are summarized in Table 5-3. The deposition rate was approximately 10-15 nm per spin for ZnO and 20 nm per spin for Sc/Y:ZnO. The optical absorbance was measured by a Shimadzu UV-vis spectrometer. The resistivity of the films was tested using Van der Pauw structures on 7.5mm square samples with soldered indium contacts on all four corners. Scanning spreading resistance microscopy (SSRM) was performed on a Veeco Dimension 3100 atomic force microscope. Hall measurements were conducted on the Van der Pauw samples using an Accent Hall system. X-ray photoelectron spectroscopy (XPS) and XPS depth profile was done in a Kratos XPS using Al Kα line for the spectra and Ar plasma for sputtering.

Table 5-3. Thickness of different Sc/Y:ZnO films as deposited.

Number of layers	**3**	**9**	**15**	**30**
ZnO	52.2nm	107nm	211nm	318nm
0.5wt% Sc:ZnO	56.6nm	-	-	-
1.5wt% Sc:ZnO	86.7nm	192nm	323nm	653nm
1wt% Y:ZnO	71.9nm	-	-	-
3wt% Y:ZnO	69.2nm	198nm	316nm	571nm

5.3 Results and Discussions

5.3.1 Optical properties

Figure 5-1 (a) shows the UV-vis transmission spectra of FG-annealed 30 layer ZnO, 1.5wt% Sc:ZnO and 3wt% Y:ZnO films. All Sc/Y:ZnO films are highly transparent, with an average transmission of over 93% within the non-absorbing range (400nm – 1100nm), summarized in Table 5-4. The Tauc band gap, E_g, is extracted from Figure 5-1 (b) using the equation $(\alpha h\gamma)^2=B(h\gamma-E_g)$, where α is the absorption coefficient, hγ is the photon energy, and *B* is a constant. The optical bandgaps are between 3.21 and 3.25eV. This is close to that previously reported for ZnO (3.4 eV) and Sc/Y:ZnO (3.2 to 3.4 eV) [176]. The band gap decreases slightly when ZnO is doped with Sc or Y. Normally degenerate doping in ZnO-based TCOs causes band gap widening due to the Burstein-Moss effect [169]. The observed bandgap narrowing may indicate that the Sc or Y dopants are not fully electrically activated. This will be discussed further in Section 5.3.3.

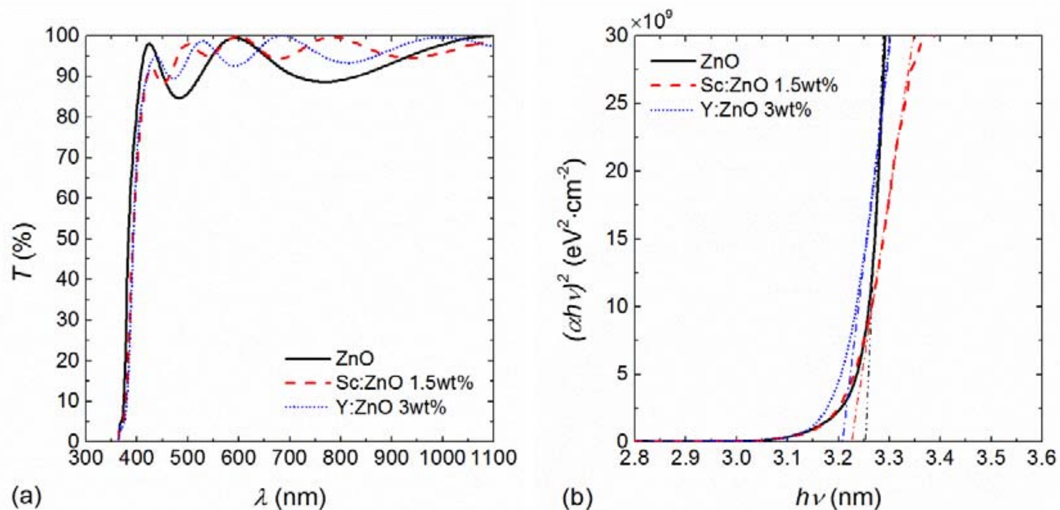


Figure 5-1. (a) UV-vis transmission spectra of FG-annealed 30 layer ZnO, 1.5wt% Sc:ZnO and 3wt% Y:ZnO films. Transmission, T, is calculated from absorbance assuming no

reflection (R=0). The films have an average transmission of > 93% from 400nm-1100nm. (b) Tauc plots from the same measurements. The optical bandgap decreases slightly from 3.25 to 3.23 or 3.21eV when ZnO is doped with Sc or Y, respectively.

Table 5-4. Minimum and average optical transmission of FG-annealed 30 layer ZnO, 1.5wt% Sc:ZnO and 3wt% Y:ZnO films in the non-absorbing range (400nm to 1000nm), and Tauc band gap extracted from Figure 5-1 (b).

Film compositions	T_{min} (%)	T_{avg} (%)	E_g (eV)
ZnO	82.0	93.2	3.25
1.5wt% Sc:ZnO	67.9	94.5	3.23
3wt% Y:ZnO	71.1	94.4	3.21

5.3.2 As-deposited film electrical properties

The resistivity of the films versus Sc or Y concentration is shown in Figure 5-2 (a) or (b), respectively. The as-deposited films are highly resistive, with $\rho > 10^4$ Ω·cm. This is typical for solution-processed TCOs annealed only under oxidizing conditions, and is commonly attributed to a lack of shallow donors, such as zinc interstitials, hydrogen, or hydrogen occupied oxygen vacancies [168]. Doping ZnO with either Sc or Y did not reduce the as-deposited film resistivity. On the contrary, the resistivity was increased by more than two orders of magnitude when even a small concentration of dopants is added. This trend was observed under a wide variety of process conditions: different molecular precursors, different ink treatment (heating/micro-hydrolyzing/aging), different temperature ramp rates for drying and annealing, or different humidity of the drying and annealing environments. This trend is also observed for films that were annealed in forming gas to

obtain lower resistivity (Figure 5-2). Therefore, we conclude that Sc or Y do not act as n-type dopants in solution-processed ZnO.

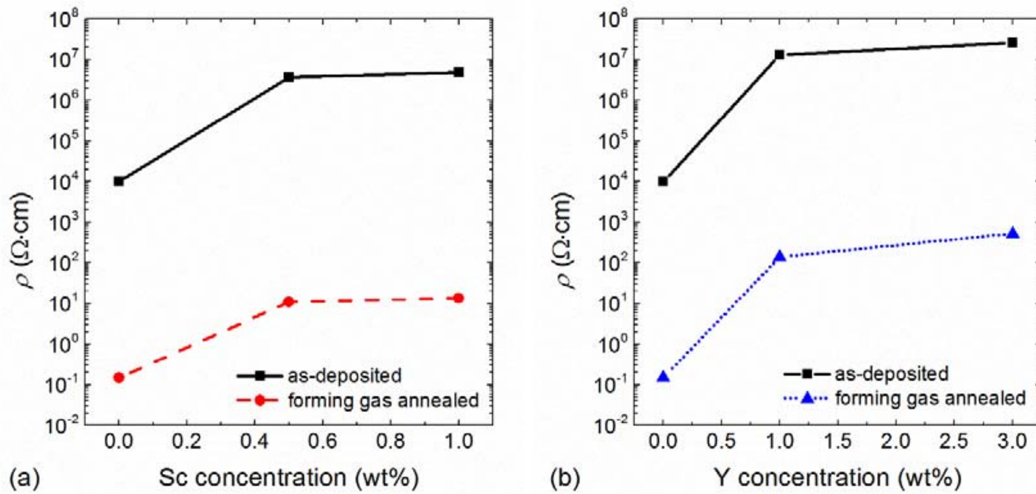


Figure 5-2. Resistivity of three layer (a) Sc:ZnO films and (b) Y:ZnO films before and after forming gas anneal. The as-deposited films were highly resistive. The FG-annealed films were much less resistive. The incorporation of Sc and Y increased film resistivity under all tested process conditions, i.e. they do not act as electron donors.

To investigate the role of Sc and Y in Sc/Y:ZnO, surface XPS was conducted on as-deposited films. The Sc and Y XPS peaks are plotted in Figure 5-3 (a) and (b) for Sc:ZnO and Y:ZnO, respectively. As the ratio of Y or Sc precursor in the ink increases, the XPS peak intensities of Y 3d5/2 and Sc 2p1/2 and 2p3/2 concurrently increase, indicating the presence of Y and Sc in the film with a stoichiometric trend corresponding to the ink concentrations. Both signals can be fit by Gaussian peaks. The Y 3d5/2 peaks are centered between 157.1eV to 157.4eV, close to the known Y_2O_3 peak at 157.0eV [187], indicating that the yttrium is not metallic but oxidized into a +3 state. The Sc 2p3/2 peaks are centered between 400.7 to 400.9eV. This falls between the known Sc(0) 398.5eV and

Sc_2O_3 401.7eV peaks [187], indicating partial oxidation of scandium or formation of sub-stoichiometric oxides.

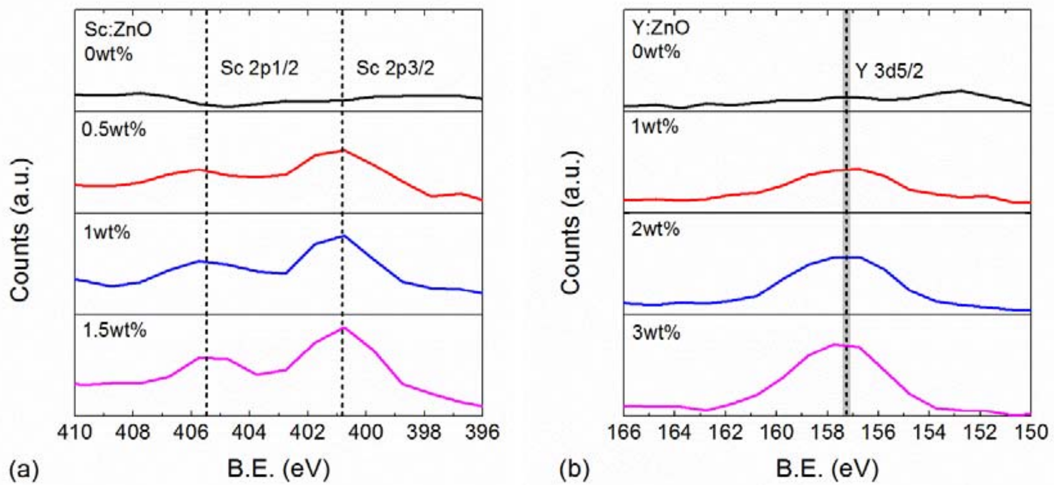


Figure 5-3. Surface XPS of as-deposited Sc:ZnO and Y:ZnO: (a) Sc 2p peaks indicate formation of Sc_2O_3 and/or sub-oxides. (b) Y 3d peaks indicate Y_2O_3.

The Zn XPS peaks are plotted in Figure 5-4 (a) and (b) for Sc:ZnO and Y:ZnO, respectively. The Zn 2p1/2 and 2p3/2 peaks are located at 1044.5 to 1044.6eV and 1021.4 to 1021.5eV, respectively, in the middle of the published ranges of 1044.1 to 1044.7eV and 1021 to 1021.7eV [187]. Since the ZnO peaks significantly overlap with the Zn metal binding energy peaks [187], [188], it is difficult to determine the chemical states of Zn from the binding energy alone. However, others have reported shifts of the Zn 2p3/2 peak position in Al:ZnO as a function of doping [189]. A lack of Zn peak shift, indicating no change in Zn chemical states, might indicate unsuccessful doping of ZnO.

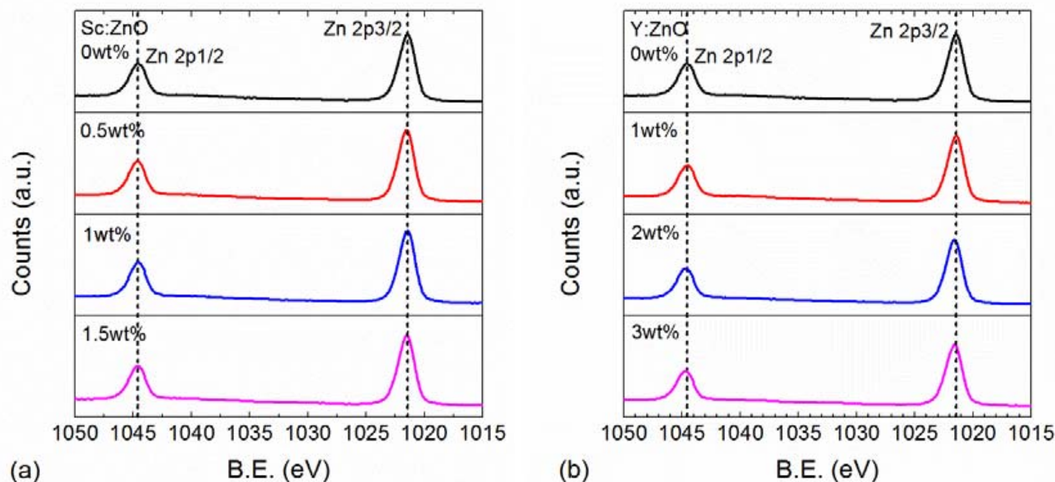
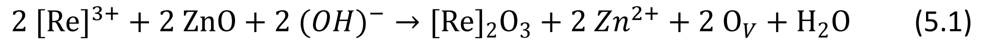


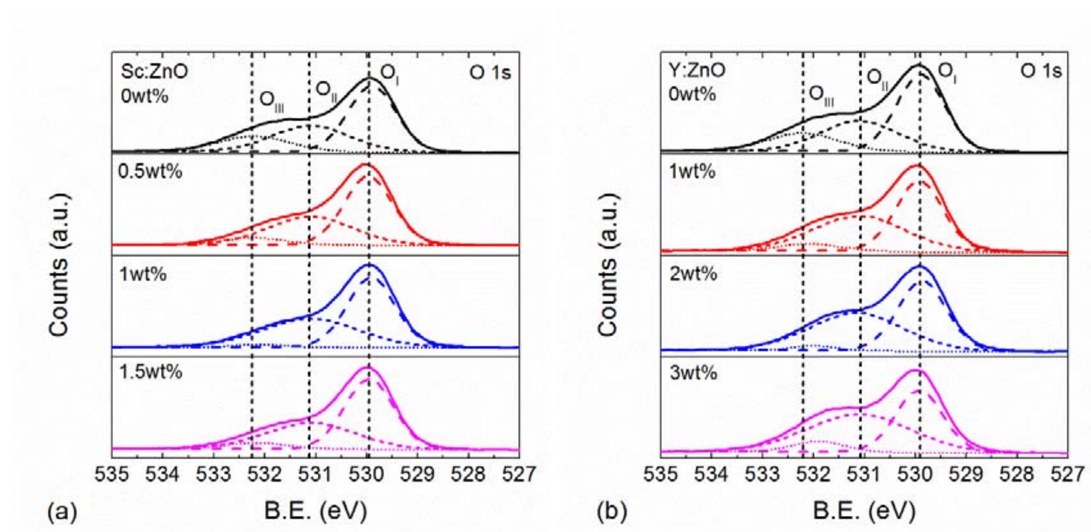
Figure 5-4. Surface XPS of as-deposited Sc:ZnO and Y:ZnO: Zn peaks do not change with (a) Sc or (b) Y addition.

The oxygen 1s peaks were detected and deconvoluted into 3 components: metal oxygen M-O bonds (O_I), oxygen bonds near oxygen vacancies, O_V (O_{II}), and loosely bonded oxygen, which can be attributed to hydroxyl (–OH) groups, carbonates, or water (O_{III}). The results are plotted in Figure 5-5 (a) and (b). The peaks occurred at the standard positions, with O_I at 530.0eV, O_{II} at 531.1, and O_{III} at 532.1eV [187]. The ratio of the area under each peak was calculated and plotted against Sc and Y doping concentrations in Figure 5-5 (c) and (d). For both films, at small doping concentrations, the M-O bond (O_I) ratio was almost unchanged, while the Ov bond (O_{II}) ratio increased and the –OH bond (O_{III}) ratio decreased with increasing Sc or Y concentration. This implies a conversion of Zn-OH to Zn-O_V as the concentration of Sc or Y is increased. Based on the large oxide formation energy of scandium and yttrium oxide, and the experimental detection of oxidized yttrium and scandium in the film, we hypothesize that the following reaction may occur during film formation, where [Re] = Sc or Y:



$$2\,[\mathrm{Re}]^{3+} + 2\,\mathrm{ZnO} + 2\,(OH)^{-} \rightarrow [\mathrm{Re}]_2\mathrm{O}_3 + 2\,Zn^{2+} + 2\,\mathrm{O}_V + \mathrm{H_2O} \qquad (5.1)$$

The results of the reaction are threefold: (1) the formation of Sc_2O_3 or Y_2O_3 in place of ZnO, (2) the concurrent creation of oxygen vacancies in the ZnO matrix (observed as an increase in the O_{II} ratio), and (3) the reduction of carbonates or hydroxyl species (observed as a decrease in the O_{III} ratio) into water, which is likely evaporated during the film anneal. The formation of insulating Sc_2O_3 or Y_2O_3 may increase film resistivity. Oxygen vacancies in ZnO are deep donors, and will not strongly affect the film conductivity [168]. The reduction of O_{III} species could have multiple effects, which will be discussed later in Section 5.3.3.



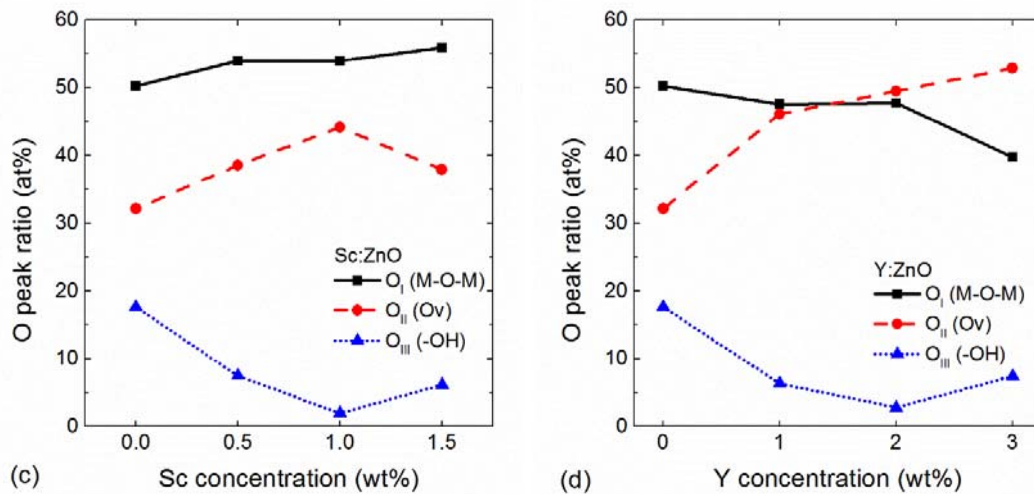


Figure 5-5. Surface XPS of as-deposited Sc:ZnO and Y:ZnO: (a), (b) O peaks and (c), (d) O peak ratios versus Sc, Y concentrations, fit into three sub-peaks: metal-oxygen bonds (O_I), oxygen near oxygen vacancies or deficiencies (O_{II}), and loosely bonded species (O_{III}). The addition of Sc up to 1 wt% or of Y up to 2 wt% causes a decrease in O_{III} and increase in O_{II}, indicating conversion of hydroxyl species to oxygen vacancies.

To identify the physical origin of the high film resistance, SSRM measurements were conducted on 0 wt%, 1 wt% and 3 wt% Y:ZnO on heavily doped Si. Figure 5-6 (a) shows the AFM height images and (b) shows SSRM micrographs of the films. In SSRM, high resistance pathways are indicated by lower output voltages (darker colors). Low resistance pathways are indicated by higher output voltages (lighter colors). All of the films have similar spatial distribution of high and low spreading resistance, with conductive pathways spaced approximately 50 nm apart. These conductive pathways are visible in Figure 5-6 (b) as light colored (bright yellow) traces. The spatial distribution of conductivity corresponds roughly to the 30 to 40 nm ZnO crystallite size observed by AFM in Figure 5-6 (a) and by SEM in Figure 5-9 (a)-(c). This may indicate that conduction in the

vertical direction occurs along grain boundaries (GB), whereas the nanocrystallites are electrically insulating.

The yttrium doping level has no observable effect on the spatial distribution of conductivity. SEM micrographs (Figure 5-9 (e)) show that Y:ZnO doped films have smaller crystallite sizes to similarly-prepared undoped ZnO films. Therefore the lateral distribution of conductivity – assuming it relates to grain boundaries - should have become more tightly spaced as yttrium content increases. However, this is not observed by SSRM. This may be due to the size of the AFM probe tip (~27 nm × 30 nm) which makes it difficult to image particles or grains that are sized < 40 nm.

To further analyze the SSRM data, histograms of the output voltages for each sample are plotted in Figure 5-6 (c). The histograms agree with the in-plane electrical measurements, showing a shift toward lower output voltages (higher resistance) for samples with more yttrium. The overall shape of the histogram peaks is almost unchanged. This implies that yttrium doping increases the resistance of both the (bright and high output voltage) conductive GB pathways and the (dark and low output voltage) resistive ZnO grains. The increased resistance along the GB is perhaps caused by formation of yttrium oxide, as depicted in Figure 5-7 (a) and (b). The increased grain resistance agrees with the conclusions of the DFT studies reviewed in the introduction, i.e., yttrium will not contribute to conductions due to its highly localized *4d* and *5p* electrons when doped in ZnO.

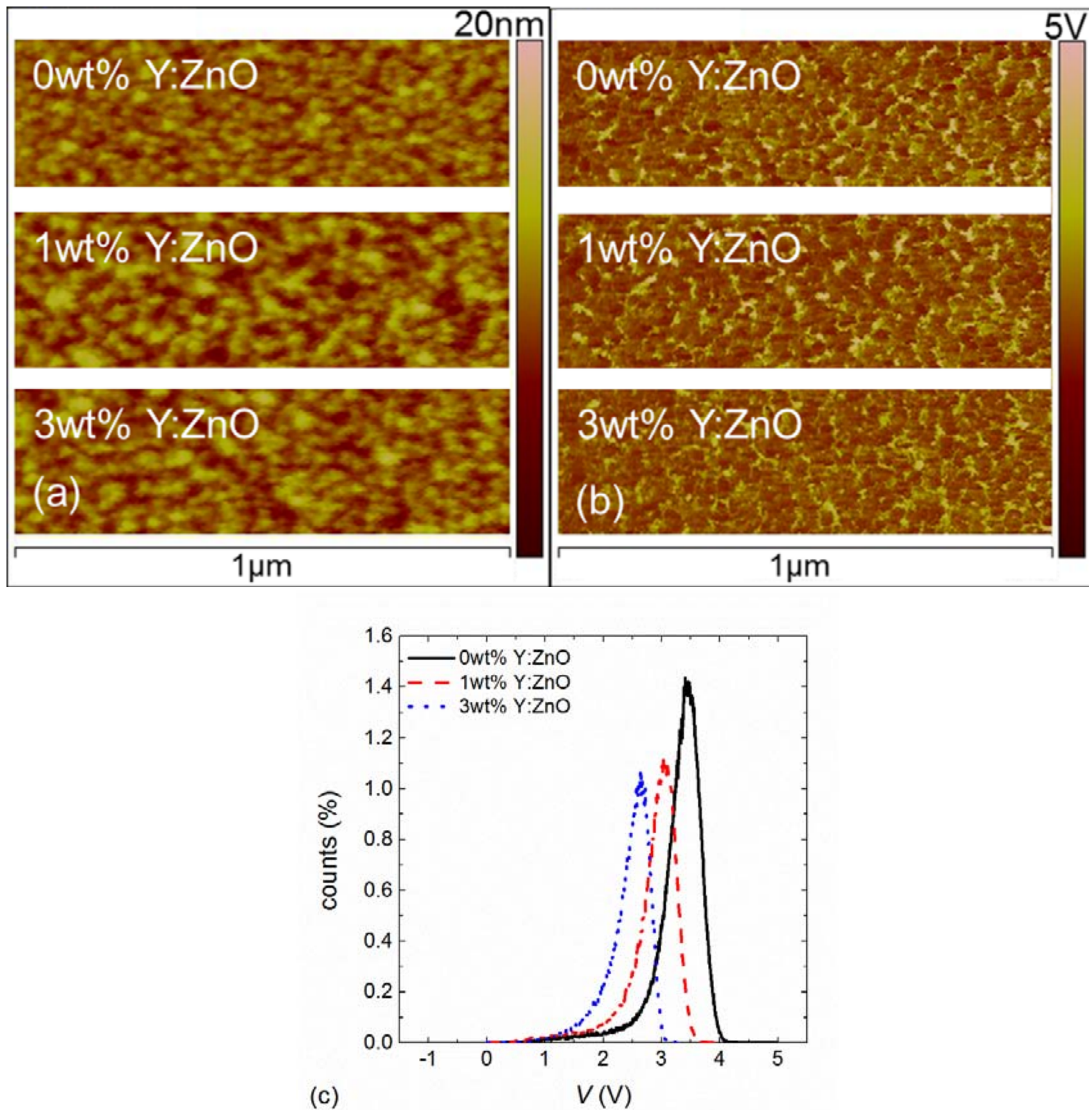


Figure 5-6. (a) AFM topography of and (b) SSRM of as-deposited 3 layer Y:ZnO on heavily doped Si. (c) A histogram of the SSRM.

In summary, the SSRM indicates that in undoped ZnO, the conduction is limited by the grain boundaries, which are highly resistive. Whereas in Y:ZnO, and possibly also in Sc:ZnO, electrical conduction is further limited by the formation of Sc_2O_3 and Y_2O_3 or other insulating compounds at the grain boundaries. This agrees with the 'amorphous phase' observed by TEM at grain boundaries in dip-coated Sc:ZnO [174]. The vertical spreading

resistance results measured by SSRM agree qualitatively with the in-plane resistance measurements performed using van der Pauw method (Figure 5-2). We hypothesize that the formation of the insulating grain boundaries in yttrium-doped ZnO disturbs both in-plane and out-of-plane conduction.

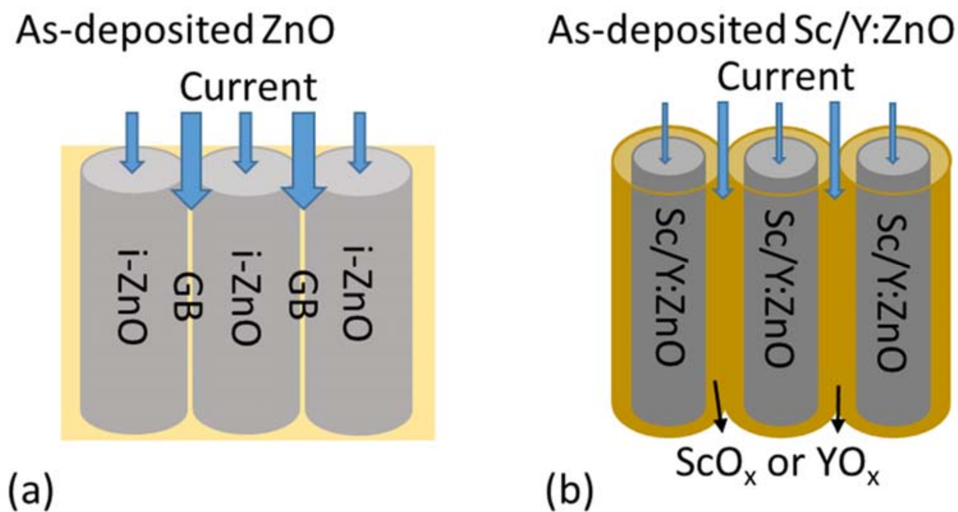


Figure 5-7. Cartoons of current flow for: (d) as-deposited ZnO films; and (e) as-deposited Sc/Y:ZnO films. Here, i-ZnO = intrinsic (undoped) ZnO, GB = grain boundary.

5.3.3 Electrical properties following rapid thermal annealing

After forming gas (FG) rapid thermal annealing, the resistivity of all films decreased by four to five orders of magnitude (Figure 5-2 and Figure 5-8 (a) and (b)), similar to many other TCO studies. This is usually attributed to the introduction of shallow donors, from Zn interstitials, H interstitials, or other species [168].

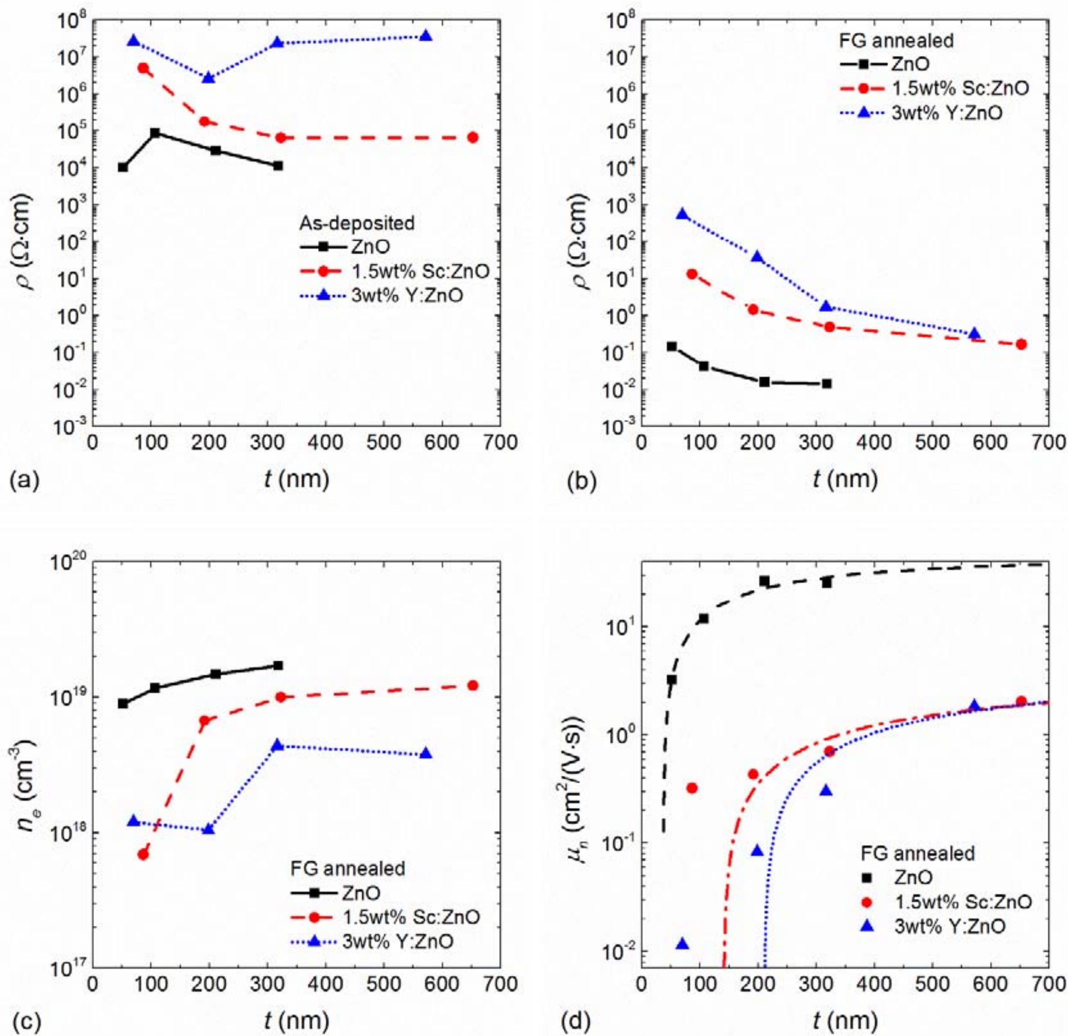


Figure 5-8. Resistivity of (a) as-deposited and (b) FG-annealed Sc/Y:ZnO films with different thickness. The resistivity of as-deposited films showed weak thickness dependence, but the FG-annealed films showed strong thickness dependence, especially for the Sc/Y doped films. The (c) carrier density and (d) mobility of FG-annealed films of different thickness. The dashed/dotted lines indicate fits to a bi-layer depletion layer model [190] , with depletion layer thicknesses of 36.6 nm for ZnO, 140 nm for Sc:ZnO and 210 nm for Y:ZnO.

The resistivity of all films is very thickness dependent, especially for FG-annealed Sc/Y:ZnO films (Figure 5-8 (b)). As film thickness increased from 80nm to 600nm, the resistivity decreased by two (four) orders of magnitude for FG-annealed 1.5 wt% Sc:ZnO

(3 wt% Y:ZnO). In contrast, for FG-annealed undoped ZnO, the film resistivity reaches a minimum value of about 0.02 Ω-cm at < 200 nm and thereafter stays constant.

The observed thickness-dependence of Sc/Y:ZnO resistivity could be due to changes in crystallite grain sizes and/or surface depletion. The grain size of nano-crystalline TCO films usually increases for thicker films. This has been observed in Y:ZnO [183] and other TCOs [190]–[199], and may be due to crystal growth dynamics. For our Sc/Y:ZnO films, thicker films have significantly larger grain sizes than thinner films, as shown by SEM in Figure 5-9. Grain sizes for films with different thickness are listed in Table 5-5. The average grain size increased from < 30nm for three-layer ZnO, and $\leq$ 15 nm for three-layer 1.5 wt% Sc:ZnO and 3 wt% Y:ZnO to 44 nm for 15-layer ZnO and > 30 nm for 30-layer Sc:ZnO and Y:ZnO. An increase in grain size may result in improved conductivity, due to the reduction of grain boundary scattering during charge transport. Therefore the observed changes in grain size may contribute to the thickness-dependence of resistivity.

Table 5-5. Average grain sizes for ZnO, Sc:ZnO and Y:ZnO films with different thickness, obtained by SEM. Each layer corresponds to 10-15nm film thickness, as indicated in Table 5-3.

FG-annealed films	Average grain size 3 layer films (nm)	Average grain size 15 layer films (nm)	Average grain size 30 layer films (nm)
ZnO	29 nm	44 nm	-
1.5wt% Sc:ZnO	13 nm	-	31 nm
3wt% Y:ZnO	15 nm	-	35 nm

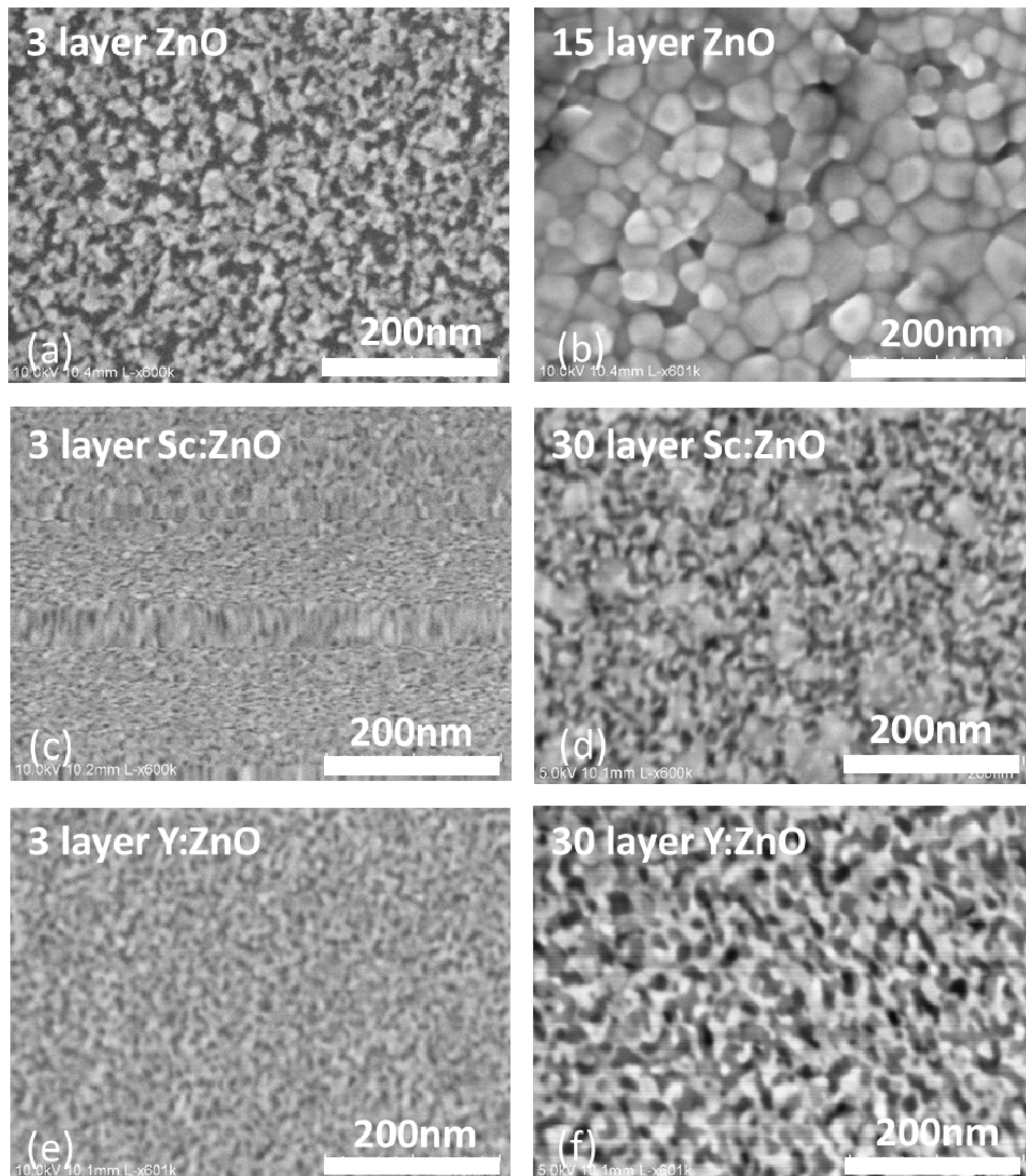


Figure 5-9. SEM micrographs of FG-annealed (a) three-layer ZnO, (b) 15 layer ZnO, (c) three-layer 1.5 wt% Sc:ZnO, (d) 30 layer 1.5 wt% Sc:ZnO, (e) three-layer 3 wt% Y:ZnO, (f) 30 layer 3 wt% Y:ZnO. The grain size of Sc/Y:ZnO increases with film thickness.

However, the resistivity of Sc/Y:ZnO shows much greater thickness dependence than that of undoped ZnO, while the ZnO shows much greater change in grain size. Therefore, the change in grain size cannot fully explain the observed thickness-dependence of

resistivity. Another mechanism must also be at play. One possibility is surface depletion, which can be caused by surface chemical reactions with the environment, such as oxygen or water exchange. Positive surface charges can induce a depletion region in the film, reducing the thickness of the ohmic (charge-carrying) region [200], [201]. As film thickness increases, the surface depletion effect becomes less important, leading to an effective reduction in film resistivity, as observed experimentally. Such a depletion region could be located at either the top interface (where the film is open to ambient) or the bottom interface with the underlying substrate.

To assess whether surface depletion is occurring, we used Hall measurements (Figure 5-8 (c) and (d)). The carrier concentration, n_e, for FG-annealed ZnO was only slightly affected by film thickness and has a value of approximately 1×10^{19} cm^{-3}. Other ZnO-based TCO studies have shown both dependence and independence of n_e-t [190]–[199], [202], [203], most likely due variations in film morphology and surface depletion induced by different materials and deposition methods used. Here, the almost thickness-independent carrier concentration indicates that there is very little surface depletion in ZnO, i.e. the depletion width is much smaller than 60 nm. The Hall mobility of undoped ZnO increased sharply as film thickness increased and has a maximum value of almost 30 $cm^2V^{-1}s^{-1}$. A bilayer model of TCO surface depletion [190] can be used to explain these results. The model assumes that the overall film resistance is a combination of the parallel resistance of the depleted surface with a constant thickness and of the bulk. The model fits are shown in the dashed/dotted lines in Figure 5-8 (d). Using a fitted value for depletion thickness of 36.6nm, the model provides a good fit to the measured ZnO Hall

mobility. Therefore the slight thickness-dependence of ZnO film resistivity we observed can be attributed to a surface depletion region with thickness on the order of tens of nm.

In contrast to the ZnO results, the n_e for FG-annealed Sc/Y:ZnO increased sharply by a factor of four to ten as the film thickness increased from 60nm to > 600nm (Figure 5-8 (c)). In general, n_e(ZnO) > n_e(Sc:ZnO) > n_e(Y:ZnO). This trend is in accordance with the optical absorption results (Figure 5-1 (b)): a larger charge carrier concentration in ZnO corresponds to the observed broadening of the bandgap via the Burstein-Moss effect.

The Hall mobility of the doped Sc/Y:ZnO has a maximum value of about 2 $cm^2V^{-1}s^{-1}$, much lower than that of undoped ZnO. The Y:ZnO mobility changed significantly with thickness (by > 100×) compared to the ZnO and Sc:ZnO, which changed by about 10× for the thickness range characterized here. This may be due to the fact that Y is more hygroscopic than Sc, and thus Y:ZnO may be more strongly affected by surface reactions with water. Additionally, the bi-layer model could not be fit to the Sc/Y:ZnO films, as shown by the dashed/dotted lines in Figure 5-8 (d). This points to the possibility of three-dimensional depletion throughout the Sc/Y:ZnO nanocrystalline grains.

To understand the chemical origin of the Sc/Y:ZnO thickness dependent resistivity, and the physical position of the depletion layer (bottom or top surface), XPS depth profiles on an FG-annealed 15-layer undoped ZnO sample and an FG-annealed 15-layer 3wt% Y:ZnO sample were conducted. The oxygen signal was de-convoluted into O_I, O_{II} and O_{III} Gaussian peaks using the same peak locations as Section 5.3.2. The results are shown in Figure 5-10. The FG-annealed ZnO and 3wt% Y:ZnO showed significant differences in

oxygen states. A hydroxyl O_{II} peak (and corresponding metal-oxygen O_I deficit) exists at the top surface of both films, due hydrogen reaction with the surface during FG anneal. Throughout the bulk of the ZnO films, the oxygen content is split about 95 at% in metal-oxygen bonds (O_I peaks), 3-5 at% in oxygen vacancies (O_{II} peaks), and 0-2 at% in loosely-bound oxygen (O_{III} peaks). In other words, the vast majority of the ZnO bulk is stoichiometric ZnO. In 3wt% Y:ZnO, this stoichiometry is only seen deep in the bulk, for thickness >180nm. In the top 180nm of Y:ZnO, the oxygen states are dramatically different: only 80-85 at% M-O bonds, 10-15 at% oxygen vacancies, and ~5% loosely bound oxygen. The relatively high level of oxygen vacancies may act as deep-level states, which, if charged, can contribute to film depletion [168]. The O_{III} peaks, which could originate from -OH, $-CO_3$ or even loosely bonded O_2, could form either shallow donors [204] or shallow (close to the conduction band) acceptor-like trap states inside ZnO [200]. In the case of Y:ZnO, trap states related to both O_{II} and O_{III} are probably formed at the surface or 3-D grain boundaries, decreasing the free carrier concentrations and depleting the nano-crystals, which results in the lower carrier concentration and lower mobility measured for thin Y:ZnO films (Figure 5-8 (c) and (d)). The peak positions and intensities of the Zn 2p and Y 3d peaks did not change with depth. The XPS observation of the depleted top layer in Y:ZnO and not in ZnO indicates the multiple roles yttrium plays in ZnO, due to its ability to strongly bond to oxygen. In Sc:ZnO, a similar mechanism is expected, but with a thinner depletion thickness compared with Y:ZnO since Sc is less hygroscopic.

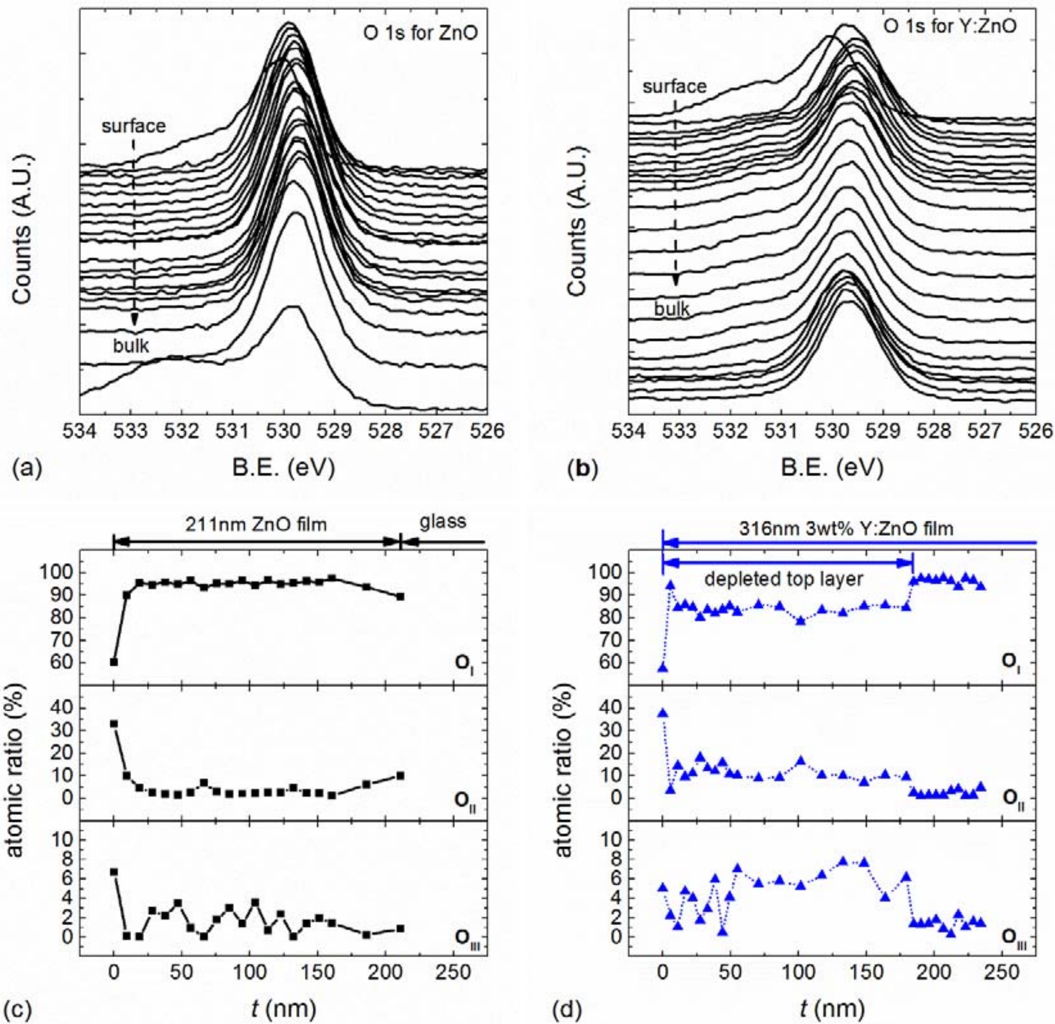
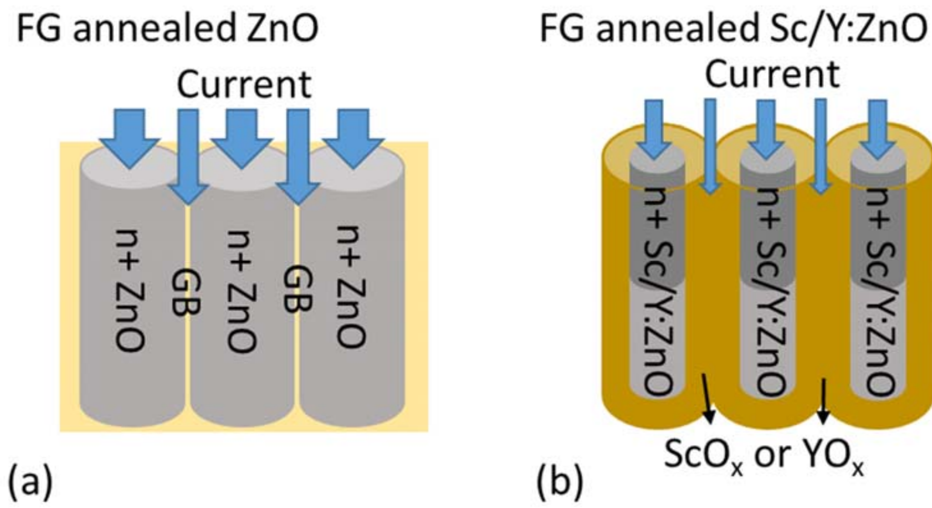


Figure 5-10. XPS depth profile of O 1s peaks on (a) 15 layer ZnO and (b) 15 layer 3wt% Y:ZnO. The oxygen peaks O_I (M-O-M), O_{II} (O_V) and O_{III} (-OH) were de-convoluted for (c) ZnO and (d) Y:ZnO, with the Y:ZnO showing clearly an elevated level of oxygen vacancies and hydroxyl groups/loosely bonded oxygen in a top layer of approximately 180-nm thickness.

In summary, as-deposited ZnO exhibits high resistance and charge transport occurs largely via grain boundaries. Forming gas anneals dope the ZnO nanocrystals by introducing shallow donors. The ZnO grains become more conductive, reducing the overall resistivity by four orders of magnitude (Figure 5-8 and Figure 5-11 (a)). In addition,

using a thicker ZnO film will significantly increase grain size (Figure 5-9 (a) and (b)), decreasing the importance of surface depletion and thus further facilitating charge transport. For as-deposited Sc/Y:ZnO films, the GB are insulating, likely due to preferential formation of insulating Sc_2O_3/Y_2O_3 at the GB during film processing. As with undoped ZnO, FG-anneals increase the conductivity of the core ZnO grain, but due to the insulating grain boundaries, the net conductivity of the doped Sc/Y:ZnO is still less than that of FG-annealed ZnO. The Sc/Y:ZnO films also show much greater thickness-dependence of charge carrier concentration, Hall mobility, and film conductivity than undoped ZnO. Moreover, the Sc/Y:ZnO films do not exhibit significant grain growth as film thickness is increased (Figure 5-9), perhaps due to slowing of growth kinetics at the insulating grain boundaries. We hypothesize that the nanostructured Sc/Y:ZnO morphology (present even in thick layers), combined with the insulating grain boundaries, causes 3-D depletion of the grains, creating a depleted top layer of > 100-nm thickness. This layer is observed in XPS as a region of increased loosely bonded oxygen (hydroxyl/carbonate groups) and increased oxygen vacancies, combined with decreased metal-oxygen bonds. The 3-D nature of surface depletion in these films means that the Hall data cannot be fit by simple planar bi-layer models that were previously used to model TCOs. Finally, Sc:ZnO and Y:ZnO seem to operate via similar mechanisms but the reduced hygroscopicity of Sc may lead to less surface reactivity and thus a thinner depletion region, resulting in the higher Hall mobility observed for thin films and higher charge carrier concentration observed for thick films. A band diagram of a thick Sc/Y:ZnO film is plotted in Figure 5-11 (c), illustrating shallow doping in the bulk grain and surface depletion in the top layer and GB regions.

The sheet resistance of the FG-annealed 325-nm thick ZnO is approx. 600 Ω per square (ρ ≅ 0.02 Ω-cm), while the sheet resistance of a 650-nm thick 1.5 wt% Sc:ZnO layer is approx. 3.1×10^3 Ω per square (ρ ≅ 0.2 Ω-cm)



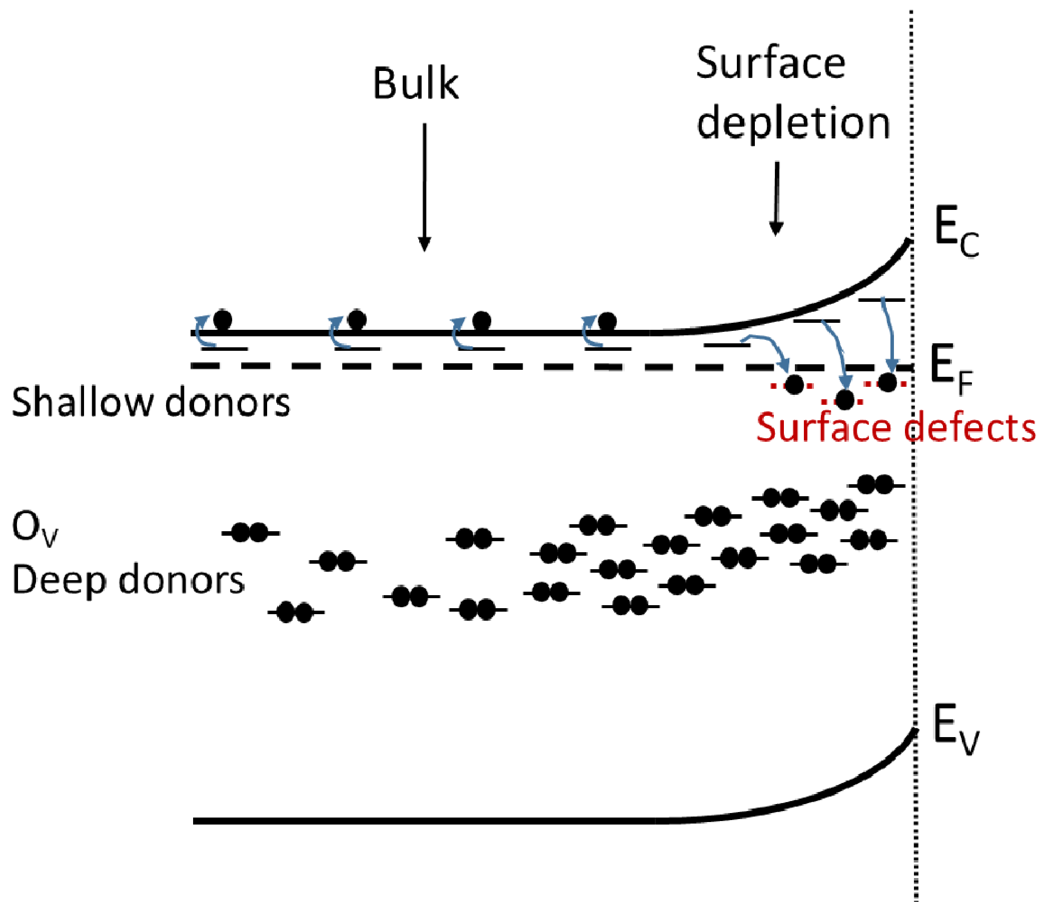


Figure 5-11. Conduction mechanisms of FG-annealed (a) ZnO and (b) Sc/Y:ZnO. The additional conduction paths in undoped ZnO are within the grains due to the introduction of shallow donors and the growth of grains. A similar mechanism occurs in Sc/Y:ZnO, but is less effective due to surface depletion (shaded top layer) within the small grains. (c) A band diagram of a thick Sc/Y:ZnO film, showing surface depletion and bulk.

5.4 Conclusions

Solution-processed Sc/Y:ZnO thin films were fabricated and evaluated as potential transparent conductive oxides. Addition of Sc (Y) with up to 1.5 wt% (3 wt%) did not result in substitutional doping, but instead increased the resistivity of the films by three orders

of magnitude. X-ray photoelectron spectroscopy and scanning spreading resistance microscopy showed the formation of insulating layers at the grain boundaries, which are hypothesized to be scandium oxide and yttrium oxide. These insulating GBs reduce film conductivity and slow down grain growth as film thickness increases. Forming gas anneals reduced the resistivity of both Sc/Y doped and undoped ZnO TCOs by four orders of magnitude, likely due to shallow n-type doping of the ZnO grains. The Sc/Y:ZnO films showed much stronger thickness-dependence of resistivity after forming gas anneals. Using depth-profile XPS, this was attributed to a higher concentrations of hydroxyls and/or loosely bonded oxygen inside a top layer of 180-nm thickness for 3wt% Y:ZnO. This depletion layer may result from three-dimensional depletion of the small nanocrystals present in Sc/Y:ZnO. Differences observed between Sc:ZnO and Y:ZnO may be due to increased hygroscopicity of Sc. In general, doping ZnO with Sc or Y in solution processes increases the sheet resistivity from 440 Ω per square for 318-nm thick ZnO to 2.6×10^3 Ω per square for 653-nm thick Sc:ZnO, making the materials unsuitable for high performance TCO applications, which typically require < 100 Ω per square or better, as shown in Table 5-6. Nonetheless, Sc:ZnO and Y:ZnO may be useful for building non-metallic thin film resistors where tuning of resistivity is needed (similar to doped poly-silicon in CMOS), or for fabricating complex device structures where the insulating grain boundaries and concurrent limit on grain growth caused by the *in situ* grain boundary passivation by Sc_2O_3 /Y_2O_3 may be advantageous. The solution deposition approach also means that we could potentially use aerosol or another conformal method to deposit Y:ZnO or Sc:ZnO on non-planar surfaces.

Table 5-6. Summary of the resistivity and transparency of the Sc/Y:ZnO thin films and a comparison with those of commercially available ITO.

Work	Material	Resistivity (Ω·cm)	Thickness (nm)	Sheet resistance (Ω/□)	Transparency @550nm (%)
This work	ZnO	1.4×10^{-2}	318	4.4×10^{2}	95
	1.5wt% Sc:ZnO	1.7×10^{-1}	653	2.6×10^{3}	96
	3wt% Y:ZnO	3.2×10^{-1}	571	5.6×10^{3}	97
Commercially available films (Sigma-Aldrich)	ITO	1.4×10^{-4}	140	10	84

Chapter 6 Solution-processed ternary yttrium scandium oxide

6.1 Introduction

6.1.1 High-k dielectric materials

The dimensions of transistors are constantly scaled down in order to increase the upper operating frequency and to decrease the power dissipation, as has been mentioned in Section 3.1.1. Besides scaling the transistor dimensions such as channel length and width, the thickness of the gate insulator is also scaled down by the same factor as the channel length. When the gate insulator scales down below 2nm, a problem arises where the gate leakage current increases drastically due to quantum mechanical tunneling effects, rendering the transistor useless. To address this problem, high-k dielectrics are used, because a high k (dielectric constant) allows for the gate capacitance to scale accordingly without decreasing the film thickness to below 2nm.

6.1.2 Binary and ternary dielectric materials

High-k dielectric materials are needed as gate insulators in state-of-the-art high-speed silicon transistors and in thin film transistors with novel semiconductors, and as passivation materials in various electronic devices, including high-power devices [205], [206]. Binary transition metal oxides and rare-earth oxides such as HfO_2, ZrO_2, TiO_2, Ta_2O_5 and La_2O_3 as well as their silicate alloys or bi-layers with SiO_2 have been adopted for use in CMOS logic and memories. For electrical insulators, amorphous films are preferred over

nano-crystalline films, because crystalline grain boundaries can act as current leakage paths, elemental diffusion paths or defect/breakdown centers [205]. A high crystallization temperature, T_{cryst}, is required to keep the film amorphous during back end of line (BEOL) CMOS processing or extreme environment operating conditions. Unlike SiO_2, which has a T_{cryst} above 1200°C, most high-*k* binary transition metal oxides have T_{cryst} below 600°C, and thus need to be formed and maintained at lower temperatures. For example, evaporated Y_2O_3 crystallizes at 425°C [207]; metalorganic chemical vapor deposition (MOCVD) deposited Sc_2O_3 crystallizes at 500°C [208]; La_2O_3 and HfO_2 crystallize at below 600°C [209]; ZrO_2 crystallizes at below 500°C [210]; and Ta_2O_5 crystallizes at around 600°C [211].

In contrast, ternary oxides typically have higher crystallization temperatures due to the disruption of crystallite formation by phase mixing. For example, ternary oxides $YScO_x$, $HfSiO_x$, $HfAlO_x$, $HfLaO_x$, $LaTaO_x$, and $LaLuO_x$, have T_{cryst} ranging from 600°C to 1000°C [205], [212], [213]. Non-silicate ternary oxides are generally preferred due to their higher relative dielectric constants, in addition to higher crystallization temperatures [214].

6.1.3 Ternary alloy yttrium scandium oxide

Here we investigate one ternary material: scandate ternary oxides, *i.e.* [Re]ScO_x, where [Re] is a rare earth metal. Scandate ternary oxides are of great interest because they are thermodynamically insensitive to moisture [171], providing a highly-stable passivation layer and enabling aqueous fabrication processes. In particular, vacuum-deposited yttrium scandium oxide, $(Y_xSc_{1-x})_2O_3$, has been observed to have a relatively high T_{cryst} of

800°C-1000°C, due to its small Goldschmidt tolerance factor [212], [213]. Its binary components, Y_2O_3 and Sc_2O_3, have conduction band and valence band offsets of > 1 eV [215]–[218] and interface defect densities of $10^{11}eV^{-1}cm^{-2}$ to $10^{12}eV^{-1}cm^{-2}$ [218]–[224] with many semiconductors, making them effective for gate insulation. With its binary compounds Y_2O_3 and Sc_2O_3 proven to be compatible with a variety of devices [218]–[227], ternary $(Y_xSc_{1-x})_2O_3$ may be a strong candidate for high performance high-*k* gate dielectrics and passivation layers in these devices.

Previously-reported scandate ternary dielectrics have been deposited by vacuum techniques such as atomic layer deposition (ALD) or pulsed laser deposition (PLD) [212], [213], [220], [228], [229]. For large area and low cost electronics, solution-based deposition methods, such as spray-coating, spin-coating and ink-jet printing, are preferred. Previously-reported solution-processed ternary alloy dielectric films have mainly focused on zirconates and titanates, and have had relatively low T_{cryst} of < 800°C [214], [230]–[235] (see Table 6-1 for details).

Table 6-1. Properties of selected high-*k* dielectrics

Ref. No.	Material	Deposition technique	Dielectric constant @ (Hz)	Thickness (nm)	Leakage current (A·cm^{-2})@ (MV·cm^{-1})	Breakdown Field (MV·cm^{-1})	Crystallization temperature (°C)
Sc-Y-O Dielectrics							
This work	*$(Y_{0.6}Sc_{0.4})_2O_3$*	*Sol-gel*	*9.6 (100k)*	*63.9*	*3.4×10^{-8} (@0.25) 1.6×10^{-7} (@1) 3.2×10^{-7} (@1.25) 6.4×10^{-6} (@2)*	*4.0-4.8*	*600-700*
[228]	$YScO_3$	ALD	16 (500k)	40	1×10^{-8} (@0.25)	1.1	900-1000
[220]	$YScO_x$	E-beam evaporation	12	8	4.4×10^{-8} (@1.25)	-	-
[229]	$YScO_3$	Sputtering	17	4	2.0×10^{-5} (@2.7)	-	-
[219]	Y_2O_3	Sol-gel	15.9 (1M)	188	8.6×10^{-7} (@2)	-	600-700
[236]	Sc_2O_3	ALD	16.9 (100k)	5.5	3×10^{-6} (@1)	3.5	-
					3×10^{-10} (@2)		

Selected Sol-Gel Ternary Dielectrics							
[230]	$Ti_{0.5}Si_{0.5}O_2$	Sol-gel	32 (1M)	200	2.1×10^{-7} (@0.1)	-	-
[231]	$NiTiO_3/SiO_2$	Sol-gel	41.4 (100k)	14/5	-	-	550-600
[232]	$SrZrO_3$	Sol-gel	25 (2M)	240	-	-	700-800
[233]	Al_8TiO_x	Sol-gel	15 (100k)	100	1.4×10^{-6} (@1)	>2.5	>400
[234]	$CaZrO_3$	Sol-gel	20 (100k)	140	9.5×10^{-8} (@2.5)	2.5	600-650
[214]	TiO_2-Ta_2O_5	Sol-gel	30	22	1.9×10^{-4} (@1)	>1.5	-
	TiO_2-La_2O_3	Sol-gel	31	18	3.3×10^{-6} (@1)	>1.7	-
	ZrO_2-Ta_2O_5	Sol-gel	17	20	9.6×10^{-8} (@1)	>2	-
	ZrO_2-La_2O_3	Sol-gel	19	18	3.1×10^{-6} (@1)	>1.5	-
Selected Vacuum-Deposited high-*k* Dielectrics (for comparison)							
[237]	HfO2	CVD		1.6	2×10^{-8} (@1)	>25	
	Al2O3	CVD		1.6	3×10^{-8} (@1)	>25	
[238]	ZrO_2+SiO_2	ALD	23	4+1.5	1×10^{-9} (@1)	>5.4	
[239]	Al_2O_3	Reactive atomic beam	9-10	20	2×10^{-7} (@0.5)		
[240]	$SrHrO_3$	ALD	17 (1M)	4.6	1×10^{-5} (@1)	>3.3	
[241]	TaHfON	Sputtering	17.7 (1M)	13.2	1×10^{-4} (@1)	>1.9	

Here we report, for the first time, successful fabrication of spin-coated $(Y_xSc_{1-x})_2O_3$ ternary alloy thin films with *x* varied from 0 to 1, and demonstrate the ability of our solution process to achieve the full range of alloy composition and form a smooth, amorphous film. We investigate the role of alloy composition on film dielectric properties and crystallization temperature, and compare the results to solution-processed binary Y_2O_3 and Sc_2O_3 and to previously-reported vacuum-deposited $(Y_xSc_{1-x})_2O_3$ alloy films. Our ternary alloy films show a low leakage current density of 10^{-8} A·cm^{-2}, a high breakdown electric field of 4 MV·cm^{-1} and a moderate interface trap density of 10^{12} cm^{-2}·eV^{-1}. Increasing the fraction of yttrium in the film lowers the dielectric constant from 26.0 to 7.7, but significantly reduces frequency dispersion. The ternary alloys are found to crystallize at 600°C to 700°C, higher than T_{cryst} of most non-silicate binary dielectrics, but lower than reported T_{cryst} of 800°C-1000°C for vacuum-deposited $(Y_xSc_{1-x})_2O_3$ [212], [213], [228].

6.2 Experimental

$(Y_xSc_{1-x})_2O_3$ thin films with different yttrium fractions (x=0, 0.2, 0.4, 0.6, 0.8 and 1) were made by spin-coating inks onto silicon substrates. The ink was prepared by dissolving yttrium acetate hydrate ($Y(CH_3COO)_3{\cdot}H_2O$, Sigma-Aldrich) and/or scandium acetate hydrate ($Sc(CH_3COO)_3{\cdot}H_2O$, Sigma-Aldrich) in 2-methoxyethanol ($CH_3OCH_2CH_2OH$, Sigma-Aldrich). The total metal molarity, [Y]+[Sc], was 0.5 M. To stabilize the ink, 0.5 M ethanolamine ($NH_2CH_2CH_2OH$, Sigma-Aldrich) was added. The ink was then stirred at room temperature for 8 to 12 h.

To form the bottom electrode in metal-insulator-metal capacitors (MIM caps), we used *n*-type <100> silicon substrates. For electrical measurements, heavily antimony-doped silicon (ρ = 0.01-0.02 Ω·cm) was used. To study interface states, metal-insulator-semiconductor (MIS) capacitors were prepared on lightly phosphorous-doped (ρ = 1-10 Ω·cm) silicon wafers. The same substrate was used for crystallization studies, in order to avoid dopant out-diffusion from the silicon wafer during high temperature anneals.

Right before spin-coating, the silicon substrates were cleaned in an ultrasonic bath in acetone and then in isopropanol alcohol for 10min each, and the solutions were filtered through 0.22 µm syringe filters. The filtered solution was spin-coated onto silicon pieces in air at 3000 rpm for 40 s. The samples were dried at 500°C in air for 1 min to allow for solvent evaporation and to initiate chemical reactions. After two more spinning and drying cycles, the samples were further annealed at 500°C in air for 1 h to allow the precursors to fully decompose and form metal-oxygen bonds [242], [243]. We call these

films "as-deposited." In order to study the crystallization process and the thermal stability of $(Y_xSc_{1-x})_2O_3$, some as-deposited films were further annealed in N_2 at 600°C to 900°C for 10 min. The MIM and MIS caps were made by e-beam evaporating 10 nm Ti and 90 nm Au onto the dielectric film. The metal was patterned by lift-off. The area of the square capacitors is defined by the area of the top metal, which ranged from 30 μm × 30 μm to 400 μm × 400 μm. A cross sectional schematic of the devices is shown in Figure 6-1.

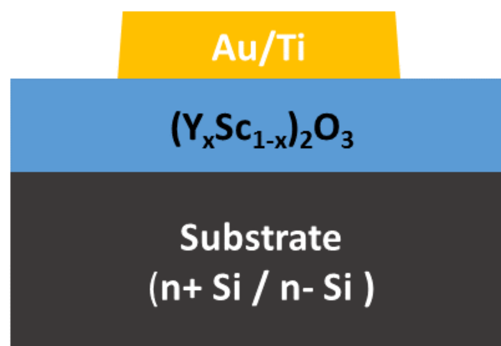


Figure 6-1. A cross sectional schematic of $(Y_xSc_{1-x})_2O_3$ MIM or MIS capacitors.

The thickness of the as-deposited films was obtained by fitting spectroscopic ellipsometry spectra (J. A. Woollam M-2000) at the non-absorbing wavelengths from 600 nm to 1700 nm using the Cauchy model. The native oxide SiO_y thickness was determined to be 1.4 nm by measuring a bare Si piece. The thickness of the three-layer as-deposited $(Y_xSc_{1-x})_2O_3$ films, listed in Table 6-2, ranges from 53 nm to 80 nm, with the yttrium-rich films being slightly thicker. The variation in thickness with alloy composition may be due to differences in yttrium and scandium precursor solubility or ink reaction kinetics.

Film composition was analyzed by EDS (Energy-dispersive X-ray Spectroscopy) in a Hitachi 8000 SEM. Surface roughness was measured using a Bruker AFM in tapping mode. Grazing Incident X-Ray Diffraction (GIXRD) was performed on a Rigaku Ultima IV with an incident angle of 0.5°, a step of 0.05° from 20° to 70°, and an integration time of 5 s. All electrical measurements were performed in ambient in the dark. Current-voltage (I-V) was measured using an HP4156A semiconductor parameter analyzer. Impedance measurements were conducted using an HP4284A LCR meter and a Keithley 4200-SCS semiconductor parameter analyzer. The dielectric constant was measured using 10 mV ac voltage and 0 V dc voltage at 100 kHz, averaged over 100 points.

6.3 Results and discussions

6.3.1 As deposited film characteristics

Spin-coating of mixed-metal inks yielded the desired stoichiometry in the solid films. In Figure 6-2 (a), the [Y]:[Sc] atomic ratio in the thin film observed by EDS largely follows the metal ratio present in the ink with some deviations, which may result from inaccuracy in ink preparation, differences in yttrium and scandium precursor solubility or ink reaction kinetics. Spin-coating also resulted in films with locally and globally smooth surfaces. Figure 6-2 (b) shows that the RMS roughness of all films is below 1.6 nm.

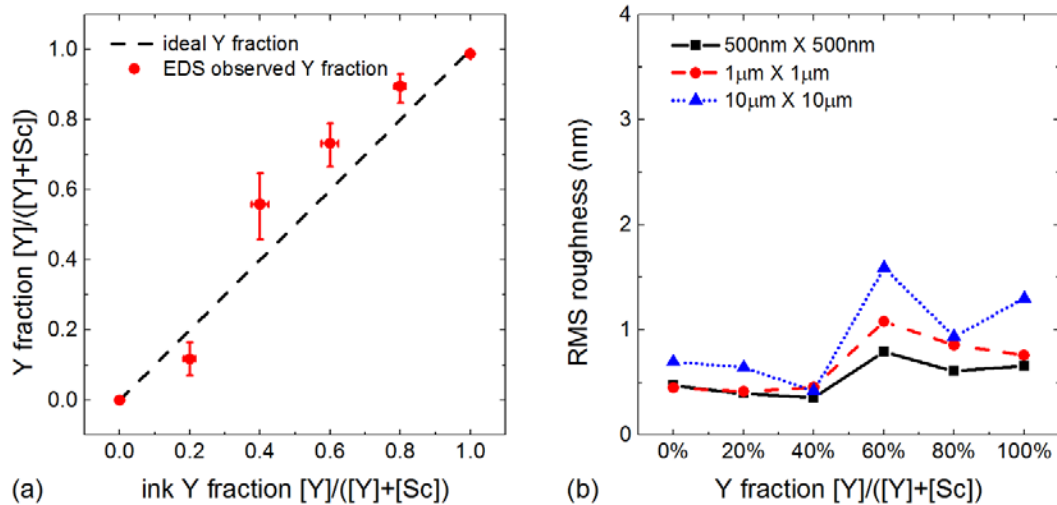


Figure 6-2. (a) Yttrium fraction detected by EDS versus yttrium fraction in the ink, showing that the stoichiometry of the film largely follows that of the ink. (b) AFM-measured RMS roughness for different yttrium fractions over three different scanning areas: 500 nm × 500 nm, 1 µm × 1 µm and 10 µm × 10 µm. All films have a smooth surface.

The crystallinity of as-deposited films varied with stoichiometry. As shown in Figure 6-3 (a), the as-deposited binary films Sc_2O_3 (0% Y) and Y_2O_3 (100% Y) have well-defined diffraction peaks, indicating a nano-crystalline morphology. In contrast, the as-deposited ternary film $(Y_{0.6}Sc_{0.4})_2O_3$ (60% Y) is amorphous, showing only one broad (222) peak. The degree of crystallization of the as-deposited films was analyzed using the Scherrer equation [244]. As shown in Figure 6-3 (b), the as-deposited binary films have average crystallite sizes of 5-10 nm, with Sc_2O_3 having a larger crystallite size, while the ternary film has a crystallite size of < 2 nm, indicating its amorphous or nearly-amorphous morphology.

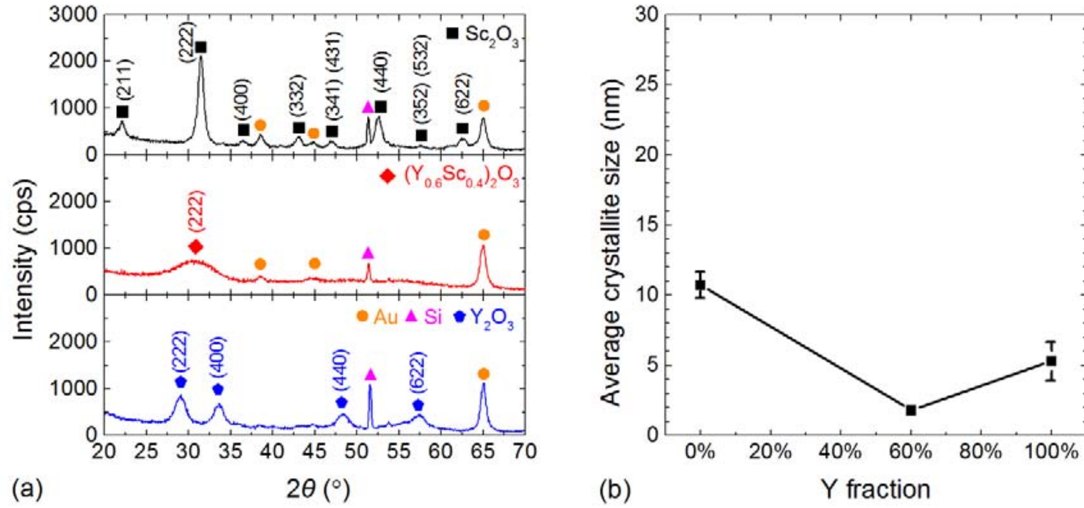


Figure 6-3. (a) GIXRD on as-deposited Sc_2O_3 (top, crystal plane peaks indicated by squares), $(Y_{0.6}Sc_{0.4})_2O_3$ (middle, diamond symbols) and Y_2O_3 (bottom, pentagon symbols) films. Note that the peaks at 37°, 45° and 65° are from Au (circles) and the peak at 52° is from the Si substrate (triangle). (b) Average crystallite size of as-deposited films, calculated using the Scherrer equation.

6.3.2 Dielectric properties of as-deposited films

Impedance spectroscopy of the MIM caps from 100 Hz to 100 kHz verified that the $(Y_xSc_{1-x})_2O_3$ films exhibit capacitive behavior: the measured impedance magnitude is proportional to f^{-1} and the impedance angle is close to -90°, as shown in Figure 6-4. From the measured impedance we calculated the frequency-dependent complex relative dielectric constant: $1/Z(\omega) = Y(\omega) = (1/R_p(\omega) + j\omega C_p(\omega)) = j\omega C_0 (\varepsilon_r'(\omega) - j\varepsilon_r''(\omega))$, with $C_0 = \varepsilon_0 \cdot A / t$, where ω is the angular frequency, $R_p(\omega)$ is the measured parallel resistive component, $C_p(\omega)$ is the measured parallel capacitive component, $\varepsilon_r'(\omega)$ is the real part of the relative dielectric constant, $\varepsilon_r''(\omega)$ is the imaginary part, A is the MIM capacitor area and t is the dielectric film thickness. The $(Y_xSc_{1-x})_2O_3$ film relative dielectric constant $\varepsilon_{r(Y\text{-}Sc\text{-}O)}'$ was obtained using a series capacitance model, i.e. $C_{(Y\text{-}Sc\text{-}O)}^{-1} + C_{Si\text{-}O}^{-1} = C_p^{-1}$ with $C_{(Y\text{-}Sc\text{-}O)}$

being the $(Y_xSc_{1-x})_2O_3$ film capacitance and $C_{Si\text{-}O}$ being the interfacial (native) SiO_y oxide capacitance. As shown in Table 6-2, as the yttrium fraction increased from 0 to 100%, the relative dielectric constant of $(Y_xSc_{1-x})_2O_3$ at 100 kHz decreased from 26.0 to 7.7. These $\varepsilon_{r(Y\text{-}Sc\text{-}O)}'$ values are comparable to those of $(Y_xSc_{1-x})_2O_3$ films deposited using vacuum techniques [220], [228], [229], indicating the high quality of solution-processed films. Since each film was fabricated with three spins, the equivalent oxide thickness (EOT) per spin, calculated by $t / 3 \times \varepsilon_{SiO2} / \varepsilon_{r(Y\text{-}Sc\text{-}O)}'$, was 2.6 to 13.6 nm. Even smaller EOT values may be achievable by using a different ink, a more dilute solution, and/or a higher spin-coating speed.

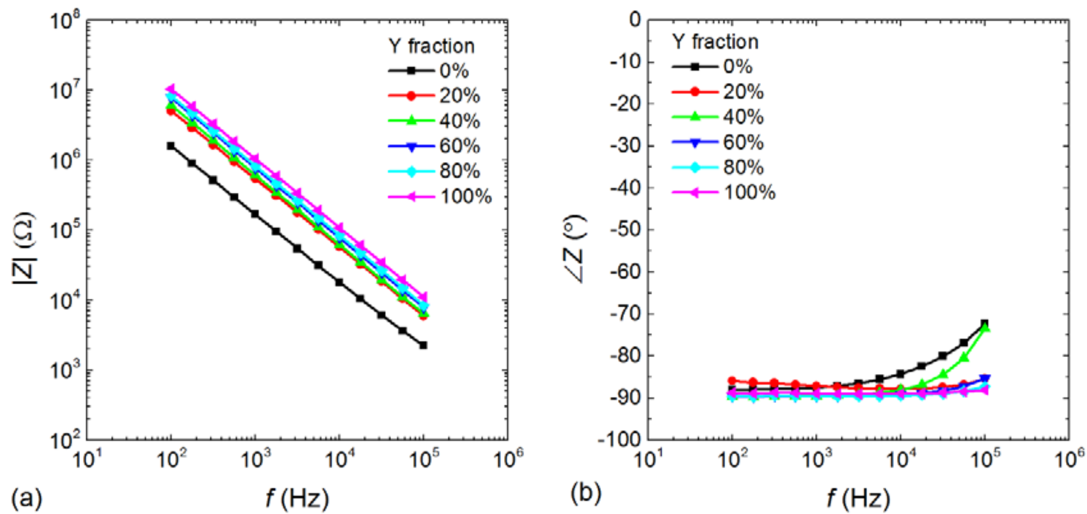


Figure 6-4. The impedance (a) magnitude and (b) angle of $(Y_xSc_{1-x})_2O_3/SiO_y$ MIM caps with different yttrium fraction, x. The magnitude is proportional to f^{-1} and the angle is close to -90°, indicating capacitive behavior.

Table 6-2. The physical thickness t, real part of the relative dielectric constant and equivalent oxide thickness (EOT) per spin of $(Y_xSc_{1-x})_2O_3$ films.

Yttrium fraction	**0%**	**20%**	**40%**	**60%**	**80%**	**100%**
Thickness t (nm)	52.8	56.9	55.1	63.9	67.5	80.3
$\varepsilon_{r(Y\text{-}Sc\text{-}O)}'$ (100 kHz)	26.0	12.6	10.3	9.6	9.4	7.7

EOT per spin (nm)	2.6	5.9	7.0	8.7	9.3	13.6

As shown in Figure 6-5 (a) and (b), the complex dielectric constant, $\varepsilon_r^* = \varepsilon_r' - j\varepsilon_r''$, of the $(Y_xSc_{1-x})_2O_3/SiO_y$ films showed different degrees of frequency dispersion. For clarity, only Sc_2O_3, $(Y_{0.2}Sc_{0.8})_2O_3$, $(Y_{0.6}Sc_{0.4})_2O_3$ and Y_2O_3 are shown in the figure. The $(Y_{0.4}Sc_{0.6})_2O_3$ and $(Y_{0.8}Sc_{0.2})_2O_3$ films show results similar to the $(Y_{0.6}Sc_{0.4})_2O_3$ dielectric film. For all films, ε_r' increased at low frequency, while ε_r'' decreased to a minima and then increased again at low frequency. In general, Sc_2O_3 and scandium-rich ternary oxides showed higher ε_r' and ε_r'' values and a higher level of dispersion than Y_2O_3 and yttrium-rich ternary oxides. Quantitatively, the $\varepsilon_r^* - f$ relations from 100 Hz to 100 kHz fit a combination of the Curie-von Schweidler (CS) law and the Havriliak-Negami (HN) law [245]:

$$\varepsilon^* = \varepsilon_\infty + \chi_{CS}^*(\omega) + \chi_{HN}^*(\omega) - \frac{i\sigma_{DC}}{\omega\varepsilon_0} \tag{6.1}$$

$$\chi_{CS}^*(\omega) = A(i\omega)^{n-1} \tag{6.2}$$

$$\chi_{HN}^*(\omega) = \frac{\varepsilon_0 - \varepsilon_\infty}{[1+(i\omega\tau)^{1-\alpha}]^\beta} \tag{6.3}$$

where ε_0 and ε_∞ are the DC and high frequency dielectric constant, respectively, χ_{CS}^* and χ_{HN}^* are the susceptibility of the CS law and the HN law, respectively, σ_{DC} is the DC conductivity, A is a constant, n is a constant indicating the frequency dependence, τ is the Debye relaxation time, and α and β are related to the width and the asymmetry of the loss peak, respectively. The fitting parameters for all $(Y_xSc_{1-x})_2O_3$ films are listed in Table 6-3.

Table 6-3. Parameter values for the Curie-von Schweidler – Havriliak-Negami (CS-HN) model fitted to measured $\varepsilon^* - f$ data for $(Y_xSc_{1-x})_2O_3/SiO_y$ films

Yttrium at%	ε_∞	ε_0	α	β	τ [s]	A	n	σ_{DC} (S/cm)
0%	11.00	29.75	0.39	1.00	1.64e-6	9.20	0.87	2.39×10^{-12}
20%	8.48	10.40	0.75	0.96	0	21.88	0.79	1.44×10^{-12}
40%	9.63	19.77	0.21	0.01	3.48e-7	2.71	0.98	1.55×10^{-12}
60%	4.03	4.24	0.04	1.00	8.35e-7	5.53	0.99	9.11×10^{-13}
80%	8.30	8.76	0	1.00	2.14e-6	0.93	0.92	7.67×10^{-13}
100%	6.10	7.56	0.63	1.00	7.43e-8	1.08	0.89	1.06×10^{-12}

The CS law is also referred to as the universal dielectric response (UDR) [246]–[248], which has been observed in a variety of dielectric and ferroelectric films [246], [247], [249]–[254]. The power relation of $\varepsilon_r^* - f$ in the CS law can indicate the existence of hopping charge transport in the films [247]–[251], [253]–[255], which has already been observed in Sc_2O_3 thin films [249]. On the other hand, the HN law model is an empirical modified Debye-model, which could result from either interfacial polarization or bulk dipole polarization [245], [247]. Interface polarization could occur at the film top and bottom surfaces, grain boundaries or inter-phase boundaries [245], [247], [255]. Since the combined CS-HN law applies to the frequency dispersion of these solution-processed $(Y_xSc_{1-x})_2O_3$ thin films, multiple relaxation mechanisms may coexist in our films. Further investigations such as temperature-dependent impedance spectroscopy could be undertaken in the future to provide additional insight into the relaxation mechanisms.

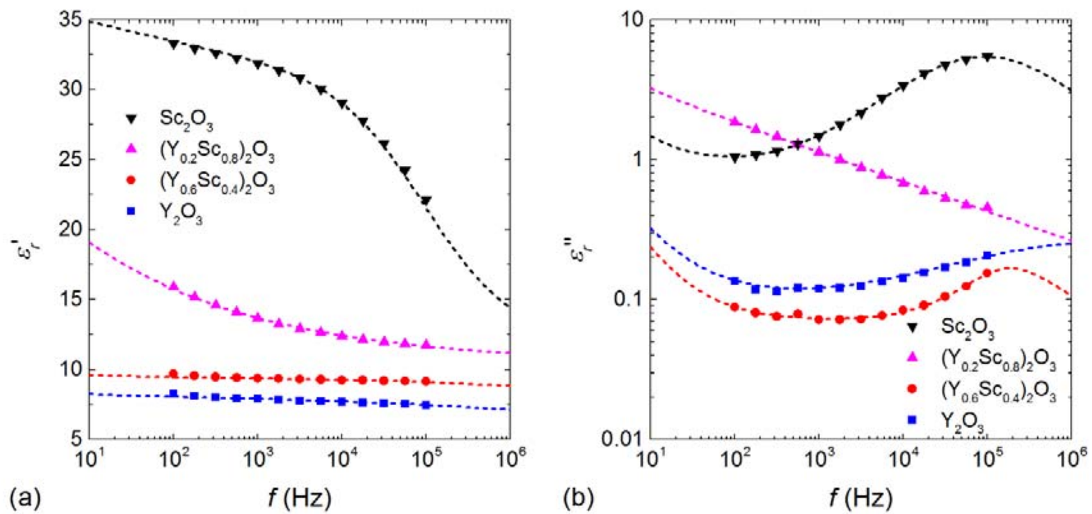


Figure 6-5. Frequency-dependence of (a) the real part and (b) the imaginary part of the dieletric constant of Sc_2O_3, $(Y_{0.2}Sc_{0.8})_2O_3$, $(Y_{0.6}Sc_{0.4})_2O_3$ and Y_2O_3 films with interfacial (native) SiO_y. Dashed lines indicate models; symbols indicate measured data. Nanocrystalline Sc_2O_3 shows strong dielectric relaxation, which may be due to interface polarization or charge trapping. Amorphous ternary alloys and nanocrystalline Y_2O_3 show weak dielectric relaxation.

The degree of $\varepsilon_r{*} - f$ dispersion is strongly related to the stoichiometry: Sc_2O_3 and scandium-rich alloys have a higher level of dispersion than Y_2O_3 and yttrium-rich films. We attribute this phenomenon to the difference in film morphology. The Sc_2O_3 film may have the strongest dispersion due to the extra charge carrier transport/polarization induced by its nano-crystalline morphology and/or film inhomogeneity. As Y_2O_3 is alloyed with Sc_2O_3, the film becomes amorphous and thus dispersion is reduced. Improvement in dielectric relaxation by ternary alloying of solution-processed oxides has also been observed in La:ZrO_x [256]. In our films the improvement in dielectric relaxation comes at the cost of a reduced relative dielectric constant, due to the lower ε_r value for binary Y_2O_3 compared to Sc_2O_3. Optimizing between these two trends, the $(Y_{0.6}Sc_{0.4})_2O_3$ film has the most advantageous properties out of all our films: a moderately high ε_r' value of 9.6

combined with the smallest dielectric loss, ε_r'', and the smallest frequency dispersion of ε_r'.

To further examine the quality of solution-processed $(Y_xSc_{1-x})_2O_3$ as a dielectric material, the $(Y_xSc_{1-x})_2O_3$ / Si interface trap density D_{it} was characterized using high-frequency and low-frequency capacitance-voltage (C-V) measurements [257]. The high and low-frequency C-V of a $(Y_{0.6}Sc_{0.4})_2O_3$ MIS capacitor is shown in Figure 6-6 (a). The D_{it} level of Sc_2O_3/Si, $(Y_{0.6}Sc_{0.4})_2O_3$/Si and Y_2O_3/Si in the depletion regime are 2.4×10^{12}, 1.3×10^{12} and 1.9×10^{12} $cm^{-2} \cdot eV^{-1}$, respectively, comparable to that of evaporated $YScO_3$ on Ge (1.0×10^{12} $cm^{-2} \cdot eV^{-1}$) [220]. The as-deposited binary films have slightly higher D_{it} levels than the ternary film, which could possibly result from the grain boundaries of the nano-crystalline binary films acting as extra charge traps at the oxide-semiconductor interface.

Figure 6-6 (b) shows the hysteresis of high-frequency C-V curves for Sc_2O_3, $(Y_{0.6}Sc_{0.4})_2O_3$, and Y_2O_3. The counter-clockwise hysteresis is likely caused by the redistribution of mobile ions such as Na^+ in the oxide under electrical stress or oxide trapped charge [257], [258]. In multi-layer amorphous materials, hysteresis could also be caused by mid-bandgap trap states arising from structural disorder or interface defect layers. In ref. [228], the hysteresis of atomic-layer-deposited (ALD) amorphous Y-Sc-O dielectrics was greatly reduced to < 0.1V by changing the ALD precursor, even though the choice of precursor did not significantly impact the impurity level or degree of disorder. Therefore hysteresis in amorphous Y-Sc-O is probably not related to inherent structural disorder. The hysteresis may instead be caused by local variations in stoichiometry, chemical bonding,

or microstructure. Quantitatively, the total mobile/trapped charge density, ($Q_M + Q_{ox}$) = -C_{ox}·ΔV_{FB}, for Sc_2O_3, $(Y_{0.6}Sc_{0.4})_2O_3$, and Y_2O_3 is +2.2 × 10^{11} cm^{-2}, +1.6 × 10^{11} cm^{-2} and +4.7 × 10^{11} cm^{-2}, respectively. The ternary oxide has the lowest ($Q_M + Q_{ox}$), possibly due to its amorphous morphology.

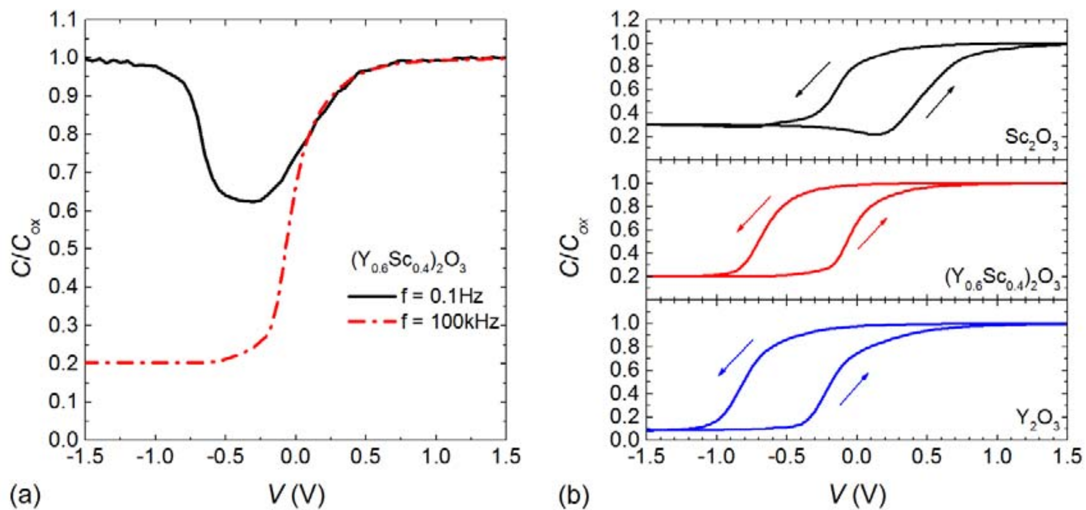


Figure 6-6. (a) High frequency (100 kHz) and low frequency (0.1 Hz) C-V curves for a Au/Ti/$(Y_{0.6}Sc_{0.4})_2O_3$/Si MIS capacitor. (b) Hysteresis of Sc_2O_3, $(Y_{0.6}Sc_{0.4})_2O_3$, and Y_2O_3 high frequency C-V curves. The total mobile charge plus oxide trapped charge is on the order of 10^{11} cm^{-2}, with the ternary oxide having a slightly lower value than binary oxides. The area of the capacitors is 400μm × 400μm.

The leakage current and breakdown properties of the films were characterized. All films have relatively low DC leakage current density of approximately 10^{-8} A·cm^{-2} for applied voltages of less than 2 V (Figure 6-7). The scandium-rich films have slightly higher leakage current density, possibly due to parasitic conduction along nanocrystalline grain boundaries. The higher leakage current of Sc_2O_3 and scandium-rich films agrees with the larger dielectric loss measured by ac impedance spectroscopy for these films.

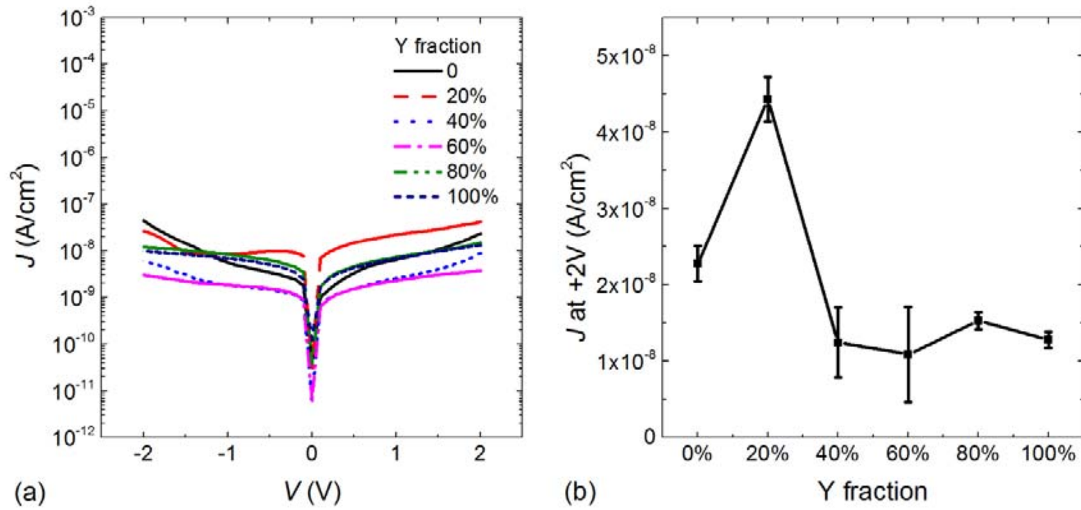


Figure 6-7. (a) *J-V* of films with different yttrium fraction. $J_{leakage}$ of all films at ±2 V is approximately 10^{-8} A·cm^{-2}. (b) Average $J_{leakage}$ at +2 V for films with different yttrium fraction. A minimum of four capacitors were measured for each yttrium fraction. Scandium-rich films show slightly higher $J_{leakage}$, perhaps due to the higher level of film crystallization.

Irreversible breakdown occurs for all as-deposited films at electric fields of 4.0 to 4.8 MV·cm^{-1} (Figure 6-8). Before breakdown, ternary alloys with 40% and 60% Y generally have lower current density compared with other yttrium fractions, perhaps due to their amorphous morphology. Sc_2O_3 has a higher leakage current density, probably due to its nano-crystalline structure. Compared to previously reported Y_2O_3/Sc_2O_3/$(Y_xSc_{1-x})_2O_3$ films or other sol-gel dielectric films [219], [220], [222], [228], [229], [236], [259], our as-deposited films exhibit significantly higher breakdown field and comparable leakage current density (Figure 6-8 and Table 6-1). This indicates the high quality of the $(Y_xSc_{1-x})_2O_3$ films formed by our spin-coating process.

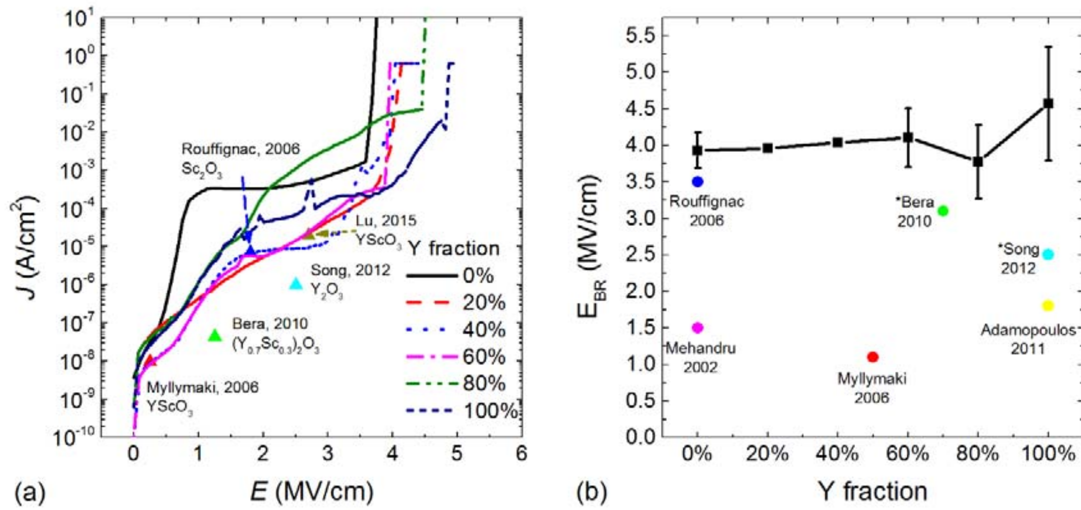
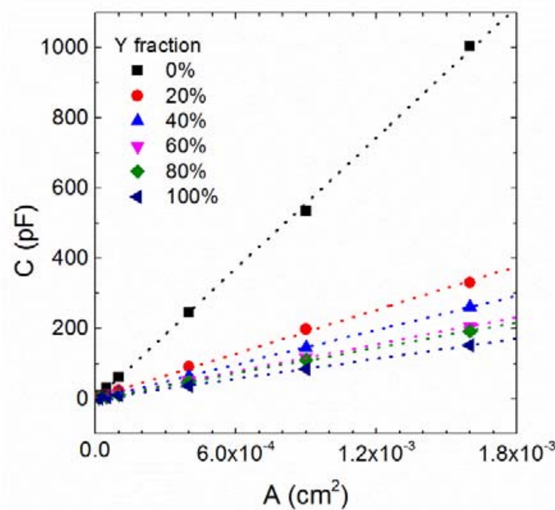


Figure 6-8. (a) Current density versus electrical field (*J-E)* for films with different yttrium fractions, showing irreversible breakdown. Films with 40% and 60% Y have lower *J* at the same *E*. (b) Breakdown field, E_{Br}, versus yttrium fraction. Typical E_{Br} of as deposited films is 4 MV·cm^{-1}. *Bera [220] and Song [219] did not report E_{Br}. Starred symbols in (b) indicate the largest reported applied field.

Both the capacitance and the leakage current are proportional with the MIM cap area for all $(Y_xSc_{1-x})_2O_3$ films, as shown in Figure 6-9. This further indicates that these spin-coated films are of high quality without pin-holes.



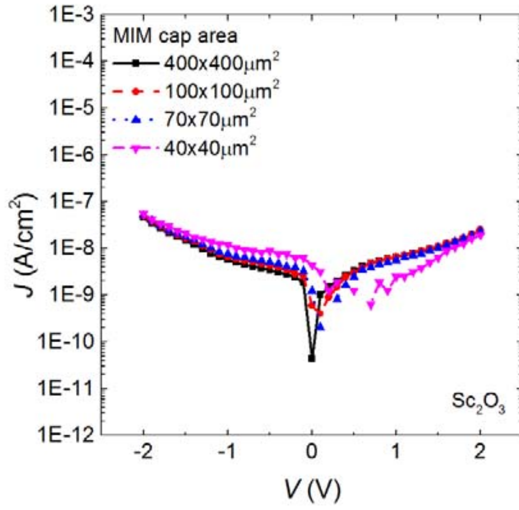
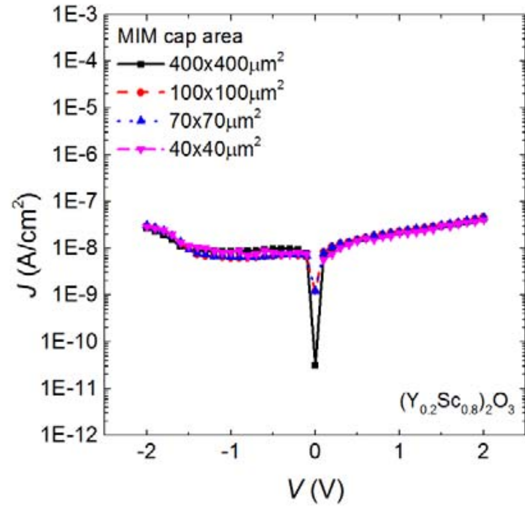
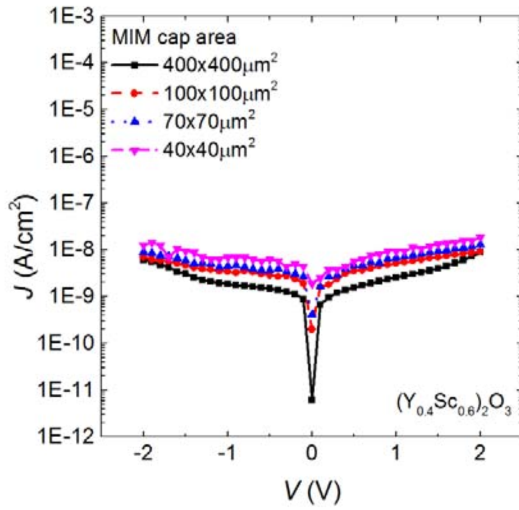
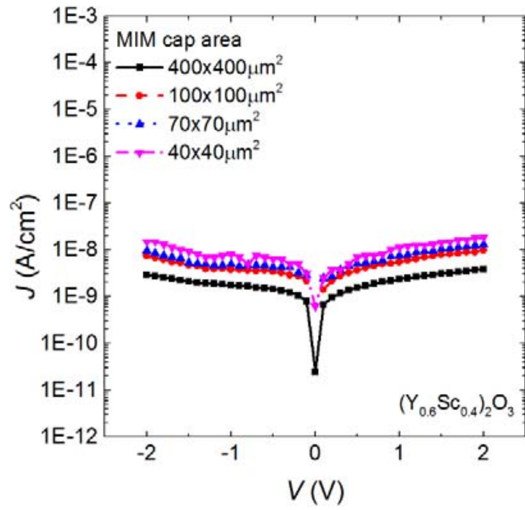
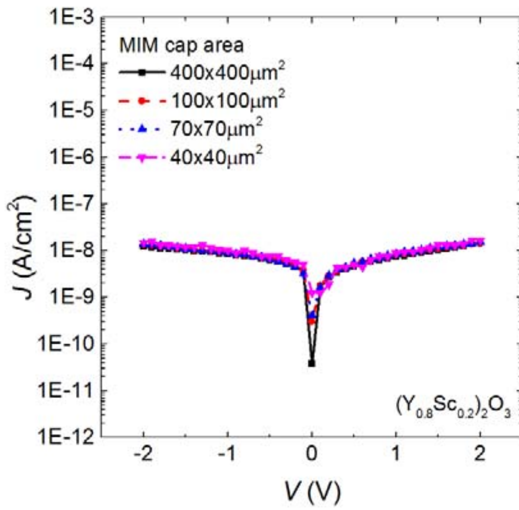
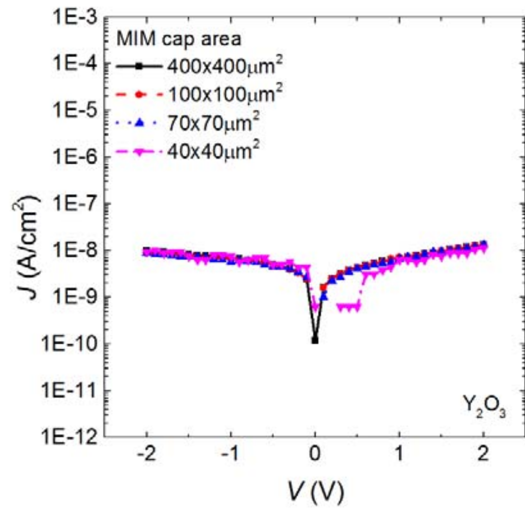
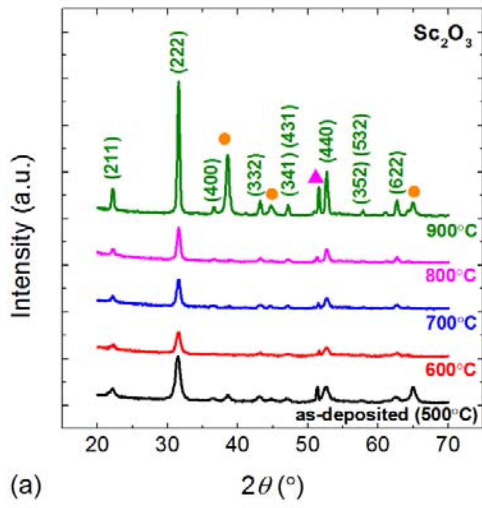

MIM cap area
400x400μm²
100x100μm²
70x70μm²
40x40μm²
J (A/cm²)
V (V)
Sc₂O₃

MIM cap area
400x400μm²
100x100μm²
70x70μm²
40x40μm²
J (A/cm²)
V (V)
(Y0.2Sc0.8)2O3

MIM cap area
400x400μm²
100x100μm²
70x70μm²
40x40μm²
J (A/cm²)
V (V)
(Y0.4Sc0.6)2O3

MIM cap area
400x400μm²
100x100μm²
70x70μm²
40x40μm²
J (A/cm²)
V (V)
(Y0.6Sc0.4)2O3

MIM cap area
400x400μm²
100x100μm²
70x70μm²
40x40μm²
J (A/cm²)
V (V)
(Y0.8Sc0.2)2O3

MIM cap area
400x400μm²
100x100μm²
70x70μm²
40x40μm²
J (A/cm²)
V (V)
Y2O3

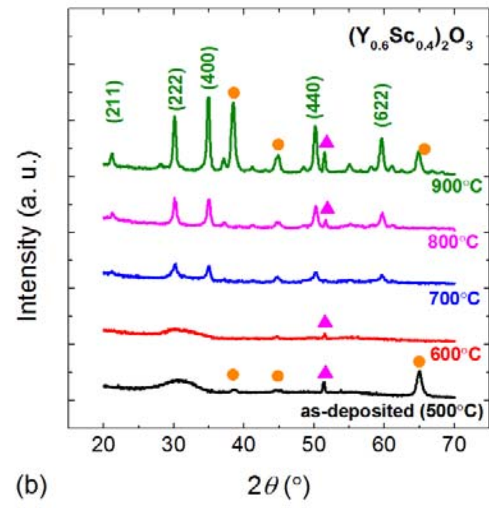
Figure 6-9. (a) Capacitance versus MIM cap area for films with different yttrium fractions. (b) – (g) Leakage current density versus voltage with different MIM cap areas for all yttrium fractions. Both the capacitance and the leakage current are proportional to the MIM cap area, showing pin-hole free high quality $(Y_xSc_{1-x})_2O_3$ films.

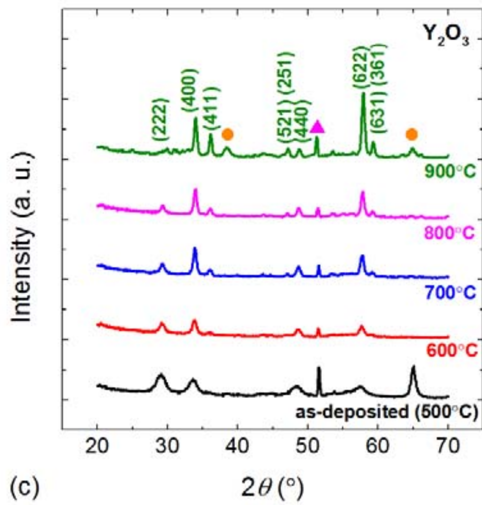
6.3.3 Crystallization and thermal stability

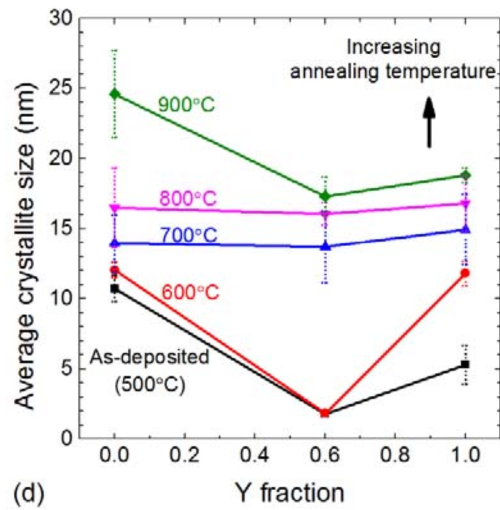
To study the film crystallization, Sc_2O_3 (0% Y), $(Y_{0.6}Sc_{0.4})_2O_3$ (60% Y) and Y_2O_3 (100% Y) films were annealed at 600°C, 700°C, 800°C, and 900°C in N_2 for 10 min. The GIXRD of these films are shown in Figure 6-10. In the as-deposited state, the binary oxides were already crystallized whereas the ternary oxides were amorphous, as shown in Figure 6-3. The binary oxide diffraction peaks grew sharper as the annealing temperature increased. In contrast, the ternary oxide showed no obvious diffraction peaks at 600°C but showed well defined peaks at 700°C, indicating a T_{cryst} between 600°C and 700°C. The crystallization of the ternary oxide is indicated by a change in average crystallite size (Figure 6-10 (d)) from 1.8 nm at 600°C (unchanged from as-deposited) to 14 nm at 700°C. The GIXRD peak positions for the crystallized alloy indicate that a *c*-type cubic solid solution of Y_2O_3 and Sc_2O_3 was formed (Figure 6-10 (e)), as was also observed for $YScO_3$ deposited by vacuum techniques [212], [228]. The ternary alloy T_{cryst} value of between 600-700°C, although higher than the T_{cryst} of both binary films, is lower than that found for $YScO_3$ deposited by vacuum deposition techniques (refs. [212], [213], [228] measured T_{cryst} of >800°C, 1000°C, and between 900°C and 1000°C, respectively). These results seem to indicate that the film deposition process plays a role in determining the film crystallization temperature. The mechanisms underlying the deposition-dependence of T_{cryst} require further investigation.

Interestingly, the spin-coated ternary alloy maintains its high E_{Br} after crystallization. After being annealed at 900°C, the breakdown field of the $(Y_{0.6}Sc_{0.4})_2O_3$ increased from 4.0 MV·cm^{-1} to > 5.2 MV·cm^{-1}, and the leakage current density decreased (compare Figure 6-8 (a) and Figure 6-11). In contrast, after 900°C annealing both binary oxides break down at a much lower electric field (0.5-3.5 MV·cm^{-1}), with large device-to-device deviation. This shows that solution-processed ternary $(Y_xSc_{1-x})_2O_3$ maintains its high-quality dielectric properties over a much wider temperature range than binary oxides, allowing a much greater thermal budget for subsequent processes.


Sc$_2$O$_3$
(211)
(222)
(400)
(332)
(341)
(431)
(440)
(352)
(532)
(622)
900°C
800°C
700°C
600°C
as-deposited (500°C)
Intensity (a.u.)
20 30 40 50 60 70
2θ (°)
(a)


(Y$_{0.6}$Sc$_{0.4}$)$_2$O$_3$
(211)
(222)
(400)
(440)
(622)
900°C
800°C
700°C
600°C
as-deposited (500°C)
Intensity (a. u.)
20 30 40 50 60 70
2θ (°)
(b)


Y$_2$O$_3$
(222)
(400)
(411)
(521)
(251)
(440)
(622)
(361)
(631)
900°C
800°C
700°C
600°C
as-deposited (500°C)
Intensity (a. u.)
20 30 40 50 60 70
2θ (°)
(c)


Increasing
annealing temperature
900°C
800°C
700°C
600°C
As-deposited
(500°C)
Average crystallite size (nm)
0 5 10 15 20 25 30
0.0 0.2 0.4 0.6 0.8 1.0
Y fraction
(d)

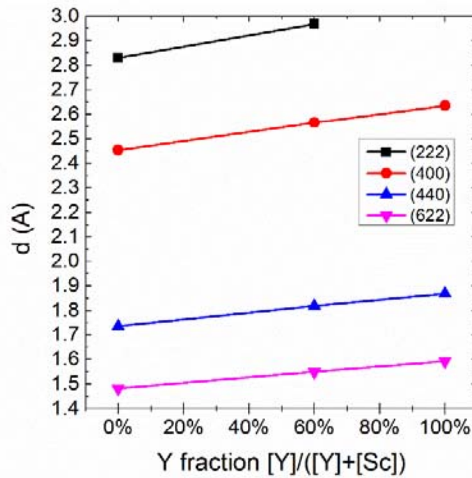


Figure 6-10. GIXRD of (a) Sc_2O_3 (0% Y) films, (b) $(Y_{0.6}Sc_{0.4})_2O_3$ (60% Y) films, and (c) Y_2O_3 (100% Y) films as-deposited and annealed at 600°C to 900°C. Note that the peaks at 37°, 45° and 65° are from Au (circles) and the peak at 52° is from the Si substrate (triangle). (d) Calculated average crystallite size for films with 0%, 60% and 100% yttrium fractions annealed at different temperatures. Binary films (0% and 100% Y) have T_{cryst} below 500°C, whereas the ternary film (60% Y) has a T_{cryst} between 600°C to 700°C. (e) The linear shift of *d* values of the diffraction peaks with regard to the stoichiometry indicates the ternary oxides are solid solutions of Y_2O_3 and Sc_2O_3.

Furthermore, it is interesting to note that ALD-deposited $YScO_3$ crystallizes at higher temperatures than our solution-processed ternary alloys (at 800 to 1000°C), but suffers from a *reduced* breakdown field following crystallization [228]. Our solution-processed films behave differently. They have a reduced T_{cryst} of 600 to 700°C, but maintain a high breakdown field and low leakage current after crystallization. The difference in film crystallization between the solution-processed and vacuum-deposited ternary yttrium-scandium dielectrics may be driven by different chemical co-ordination within as-prepared films or differences in film surface, substrate interface or defects, i.e. differences in crystallite nucleation sites. For solution-processed ternary films,

crystallization does not adversely affect the dielectric properties and thus their thermal budget may be even higher than the maximum anneal temperature of 900°C used here.

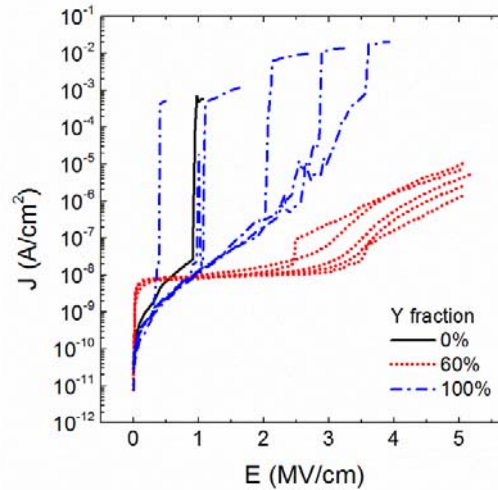


Figure 6-11. Current density versus electrical field (*J-E)* curves of Sc_2O_3 (0% Y), $(Y_{0.6}Sc_{0.4})_2O_3$ (60% Y) and Y_2O_3 (100% Y) films after a 900°C anneal that induced film crystallization. Each line represents measurement of a single device. Nano-crystalline $(Y_{0.6}Sc_{0.4})_2O_3$ maintained a high E_{Br}, whereas Sc_2O_3 and Y_2O_3 films on average broke down at much lower applied fields.

6.4 Conclusions and future work

6.4.1 Conclusions

In conclusion, $(Y_xSc_{1-x})_2O_3$ (x=0, 0.2, 0.4, 0.6, 0.8 and 1) binary and ternary alloy oxides were successfully fabricated by spin-coating. The as-deposited films had < 1.6 nm RMS roughness and the ink metal ratio had a close to 1:1 correspondence with the film stoichiometry. All films had relatively low dc leakage current density of 10^{-8} A·cm^{-2}, high breakdown field of 4 MV·cm^{-1}, and interface trap density of 10^{12} cm^{-2}·eV^{-1} with Si. The dielectric constant varied from 26.0 to 7.7 as the yttrium fraction in the film increased.

Ternary alloy oxides showed weaker dielectric constant frequency dispersion and better thermal stability, with a crystallization temperature between 600°C to 700°C, compared with <500°C for binary oxides. Even after crystallization, ternary alloys maintained their high breakdown field, whereas the breakdown field for binary oxides was severely degraded. In summary, spin-coated amorphous $(Y_xSc_{1-x})_2O_3$ films showed excellent dielectric properties that are preserved even when high temperature processing causes film crystallization. Solution-coated ternary scandates such as $(Y_xSc_{1-x})_2O_3$ are good candidates for large area and low cost high performance dielectric materials.

6.4.2 Outstanding scientific questions and future work

Future work include: (1) investigating the origin of the dielectric relaxation, (2) understanding the crystallization process, (3) further film thickness scaling, (4) integrating the $(Y_xSc_{1-x})_2O_3$ film with novel electronic materials.

(1) The origin of the dielectric relaxation in the $(Y_xSc_{1-x})_2O_3$ films could be further investigated by techniques including high resolution imaging combined with temperature dependent impedance spectroscopy, since different types of relaxation might react to temperature change differently. These studies would help further determine the origin of the high frequency dispersion of the dielectric constant of the Sc_2O_3 and Sc-rich films.

(2) The observed crystallization temperature of the solution-processed $(Y_xSc_{1-x})_2O_3$ films was much lower than reported vacuum-deposited $(Y_xSc_{1-x})_2O_3$ films. This discrepancy has not been investigated. Neither is there any study on the differences in the crystallization process between solution-processed films and vacuum-deposited films,

which could possibly be studied by in-situ high resolution microscopy. Further investigation into this topic might also reveal why crystallized solution-processed ternary alloy $(Y_xSc_{1-x})_2O_3$ was still a good dielectric material with low leakage current and high breakdown field.

(3) Since the ultimate goal of high-k dielectric materials is to obtain an *EOT* of sub 2nm, it is yet to be demonstrated that solution-processed $(Y_xSc_{1-x})_2O_3$ is able to achieve the goal. Theoretically, films with lower *EOT* could be realized by using dilute solutions and high spin-coating speeds. Practically, whether these films are continuous and pin-hole free with high dielectric constant and are still thermally stable are yet to be proven by experiments.

(4) Now that the high dielectric quality of the $(Y_xSc_{1-x})_2O_3$ films have been demonstrated, integrating these films with novel electronic materials as gate dielectric materials and/or passivation materials would make solution-processed $(Y_xSc_{1-x})_2O_3$ more applicable.

Chapter 7 Conclusions and Outlook

7.1 Conclusions

This thesis studied the roles of scandium and yttrium in solution-processed alloy oxide semiconductor, transparent conductor and insulator thin films, and demonstrated the broad device applications of these oxides.

The main contributions of this research are as follows:

1) We have optimized the process conditions and ink (film) stoichiometry for solution-processed semiconductor zinc tin oxide (ZTO) to improve ZTO thin-film transistor (TFT) device performance. Using cryogenic measurements, all ZTO devices show similar charge transport mechanisms, with band-like transport at room temperature and percolation conduction at low temperature. With an optimum Zn to Sn ratio of 7:3 and an annealing temperature of 480°C, the donor energy level is as shallow as 7meV and the subgap band tail (the density of states near the mobility edge) is steep with percolation energies of 3meV.
2) We have shown that sputtered Mo forms a high quality ohmic contact to solution-processed ZTO with a width normalized contact resistance of 8.7 Ω·cm, a transfer length of 0.34μm and a specific contact resistance of 1.5×10^{-4} Ω-cm^2. These contact resistance values are the lowest ever reported for ZTO, and are comparable to the

best contacts reported for vacuum-deposited IGZO. The superior contact properties between solution-processed ZTO and sputtered Mo are attributed to good band alignment, an oxide-free interface, trap-assisted tunneling through the interface energy barrier and ZTO doping due to the Mo sputtering process. This metal-semiconductor contact technology can be used for submicron channel length TAOS TFTs or oxide power devices.

3) Solution-processed, unpassivated ZTO TFTs show excellent long term storage stability for more than a year. However positive bias stress (PBS) can induce shifts in device performance, which are attributed to back channel chemical absorption/desorption. PBS shifts are eliminated by adding a 40-nm thick atomic layer deposited Al_2O_3 back channel passivation layer.

4) Y:ZTO TFTs are demonstrated for the first time. The addition of small concentrations of yttrium to solution-processed ZTO improves DC TFT performance, while larger concentrations of yttrium reduce negative bias illumination stress (NBIS) instability. This is important because NBIS of ZTO TFTs cannot be fully remedied by back channel passivation. Using device simulations, the main origin of NBIS instability for unpassivated ZTO TFTs was identified to be an accumulation of positive trapped charges at the semiconductor-gate insulator interface, whereas the major cause of NBIS instability for passivated ZTO TFT may be the creation of shallow donor states (0.1 to 0.3eV below E_c) either in the bulk or at the semiconductor-passivation layer interface. The creation, during NBIS, of shallow states, likely positively ionized oxygen vacancies, can be slowed down by

incorporating yttrium into ZTO. However, a high yttrium concentration (> 3at%) significantly compromises TFT DC performance due to increased stoichiometric disorder and/or possible formation of nano-scale insulating regions. Yttrium can act by gettering oxygen to eliminate oxygen vacancy defects and by creating acceptor-type defects in solution-processed ZTO. Due to the multiple roles of Y in ZTO, careful film composition selection is required for Y:ZTO TFTs.

5) The roles of Sc and Y in the solution-processed transparent conducting oxides Sc:ZnO and Y:ZnO have been clarified. Their primary roles include passivation of surface/grain boundaries and creation of oxygen vacancies in ZnO grains. Despite having three valence electrons, Sc and Y do not act as free electron donors like Al or Ga in Al:ZnO or Ga:ZnO. The addition of Sc/Y in solution-processed Sc/Y:ZnO results in highly resistive films (10^7 Ω·cm) due to ineffective doping and insulating structure formation along the grain boundaries. Sc and Y also cause surface depletion and/or grain disruption in more conductive Sc/Y:ZnO films obtained using forming gas anneal. While the resistivity of the Sc:ZnO and Y:ZnO is too high for use as interconnect to replace ITO, nonetheless Sc:ZnO and Y:ZnO may be useful for building non-metallic thin film resistors, or for fabricating complex device structures where the insulating grain boundaries and concurrent limit on grain growth caused by the *in situ* grain boundary passivation by Sc_2O_3 /Y_2O_3 may be advantageous.

6) High quality high-k dielectric $(Y_xSc_{1-x})_2O_3$ alloys have been fabricated by solution process for the first time. Alloying Sc_2O_3 and Y_2O_3 disrupts the formation of

nanocrystallites, resulting in an amorphous morphology for as-deposited alloys. This results in a higher crystallization temperature of 600°C to 700°C for the ternary alloys compared to <500°C for binary Sc_2O_3 and Y_2O_3. The ternary $(Y_xSc_{1-x})_2O_3$ alloys also have a weaker frequency dispersion of dielectric constant, a lower interface trap density with Si and a lower mobile charge density than nano-crystalline Sc_2O_3 and Y_2O_3. Even after crystallization, the low leakage current and high breakdown field in the $(Y_xSc_{1-x})_2O_3$ alloys are preserved due to the formation of a solid solution in the ternary dielectric thin film.

In addition to these technical achievements, the research work in this thesis has also resulted in three journal publications [260]–[262], three conference oral presentations [263]–[265] and two conference poster presentations [266], [267].

7.2 Outlook

Beyond the scope of this thesis, a number of potential studies could be conducted to gain a better understanding of the materials, processes and devices, and to further utilize these materials and devices for more complicated systems.

The materials could be better understood by further mapping of the band structure and defect density of states within the band gap using coupled electrical and optical methods such as optical-DLTS or optical Hall measurements. As was seen for the ZTO-based semiconductors, both the device performance and stress stability are greatly affected by the sub gap defect states. The same applies to Sc:Y/ZnO and Y-Sc-O. Being

able to probe these states would enable better material/device performance modeling and prediction, which is the basic requirement for implementing more complex device structures.

Besides understanding the materials, a thorough understanding of the influence of process variables on the electrical properties of the films is also needed. Some process variables such as precursor and solvent selections, type and amount of additives, temperature and aging during solution preparations, ink dispensing environment conditions, drying and annealing temperatures, environment and time, and post deposition treatments can greatly affect the electrical properties of the films. Being able to associate the process variables to the materials properties is essential to consistent material fabrication. With an improved understanding of the current process, new processes, such as using different inks, ink-jet printing, or UV/IR radiation-assisted annealing, could be successfully and quickly developed.

From an engineering point of view, the oxides studied in the thesis could be combined into various devices and systems. For example, using the high-k Y-Sc-O as a gate dielectric and possibly also a passivation layer for ZTO TFTs may produce TFTs with low operating voltage, and could also improve the TFT NBIS stability. The combination of doped and undoped Sc/Y:ZnO and Sc/Y:ZTO could possibly yield interesting heterostructures.

Furthermore, this work opens up new ways to understand the electronic properties of multi-component oxides by looking at the various roles of additives such as Sc and Y. With these knowledge, new devices based on solution-processed oxides could also be developed, such as diodes, memristors, sensors, photonic devices and power switches.

The materials and devices developed could be used in a various applications, such as display circuits, flexible circuits, high frequency circuits and high power circuits.

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