LOW POWER TECHNIQUES FOR

ANALOG BUILDING BLOCKS OF THE

ULTRA LOW POWER SYSTEM

by

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ABSTRACT

By the Moore's law of technology scaling and Bell's Law of prediction on the next generation small form factor computer class, the mm-scale sensor nodes are widely considered to be the next generation of computer class. With the limited size of the sensor nodes, the capacity of the battery is extremely small or can be even battery less. Therefore, the ultra-low power design technique is critical for those sensor nodes to sustain reasonable lifetime.

Among all the building blocks of those sensor nodes, power consumption of analog parts benefits least from the technology scaling compared to the digital and the memory counterparts and widely becomes the dominant part of the power consumption of the system. Therefore, this thesis is focus on bringing down the power consumption of the analog circuits. The following techniques are described in this thesis with the order: First, an advanced sample and hold technique for bandgap voltage reference to duty-cycled the blocks and reducing the power consumption is presented. Second, a technique for reducing leakage power of the ESD clamp circuits by addressing both GIDL leakage and subthreshold leakage is presented. Third, a new trade-off technique between noise and bandwidth for the amplifier design is established in an ECG amplifier example. Fourth, an ECG sensor system shows the possibility to bring down the analog power consumption and balance the power consumption between analog and digital blocks by co-design with digital algorithm.

CHAPTER 1

Introduction

1.1 The Requirement of Power Reduction of Analog Building Blocks

One of the most well-known quotes from the computer industry is the one formulated by Gordon Bell in 1972. It is the Bell's Law [1] of computer classes: "Roughly every decade, a new, lower priced computer class forms based on a new programming platform, network, and interface resulting in new usage and the establishing a new industry." After roughly 40 years of development of the computers industry, as shown in the Figure 1.1, we indeed have 4 computer classes: From the workstations, personal computers, laptops to the portable smart phone devices. The ongoing advances in both the process technology and the design technique enable the smart sensors or IoT (Internet of things) devices to be considered the next generation of the computers in the near future. Several prototype have been proposed and developed by both the academy and the industry. For example, [90] demonstrated a system to monitor soil moisture, [91] proposed a sensor to measure the pressure inside car tires, [92] developed a neural monitoring and stimulation systems, [93] illustrated a MEMS sensor for gas detection.

Noted that the lower price of computer is mainly come from the smaller size and high density of transistors thanks to the contributing from the technology scaling [3] predicted by the

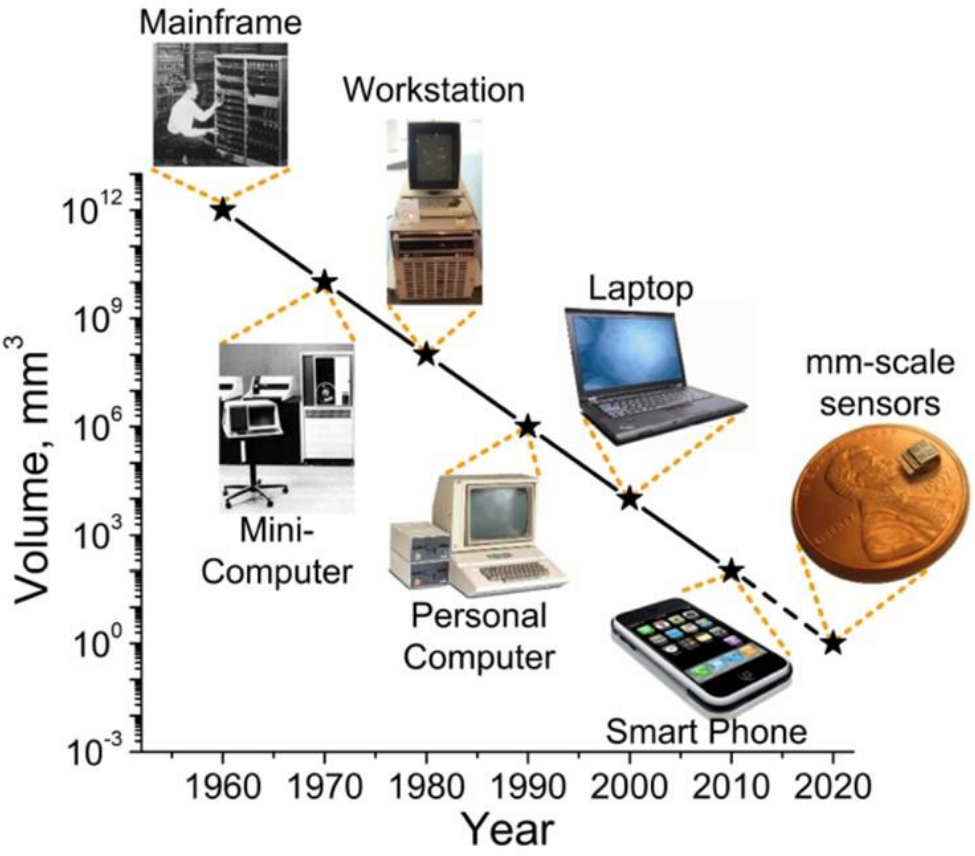


Figure 1.1 The Bell's Law of computer classes

Moore's Law [2] —famously observed by Gordon Moore, co-founder of Intel Corporation, in 1965. Thus, the size of the computers is about 100 times smaller in every consequent computers class [4]. However, the improvements on the power source such as batteries and the energy harvesters are much slower than the computers, and the amount of energy stored inside the battery is scaled roughly proportionally to the battery physical size. Therefore, with the size scaling of the computers, the battery volume also scaled accordingly [95]. As a result, although the advance classes of the computers has lower price, scaled into smaller size, larger complexity but they require smaller power consumption to sustain similar battery lifetime.

Moreover, since these next generations sensing systems are most likely to be embedded into location that is hard to access, shorter lifetime will lead to higher maintenance costs and reduce the feasibility of such systems. For example, [55, 96] is implanted under human skins and have a longer lifetime to reduce the recharge requirement is extremely important. To meet the battery volume constraint and the lifetime requirement of such systems, low power consumption technique on both the digital and analog blocks are a critical issue.

While the digital processor power scaled down with the prediction of the Gene's Law [5], the analog counterparts fall behind of the scaling. Moreover, if we foresee the next generation of the computer, the mm-scale sensors [6-12], the power consumption budget can be as lower as 10nW [12]. Therefore, power reduction on the analog circuits is an active topic [13, 14]. And following this trend, the topic on reducing the power consumption of the analog building blocks will be the critical one for the next generation computer.

1.2 The Challenge of Power Reduction of Analog Building Blocks

People may wonder when the power consumption of the digital blocks scaled well with the technology scaling [3], what is the reason behind the failure of the scaling of the analog block?

For the active power of the circuits, the power consumption of digital block can be written as follows:

$$Power \propto V_{DD}^2 \times f_{clk} \times C_{gate} \quad (1.1)$$

We also know that:

$$C_{gate} \propto W_g \times L_g \propto L_g^2 \quad (1.2)$$

Where L_g is the channel length of the devices. The above equation (1.1-1.2) shows that the active power consumption of the digital blocks are directly proportion to the area of the

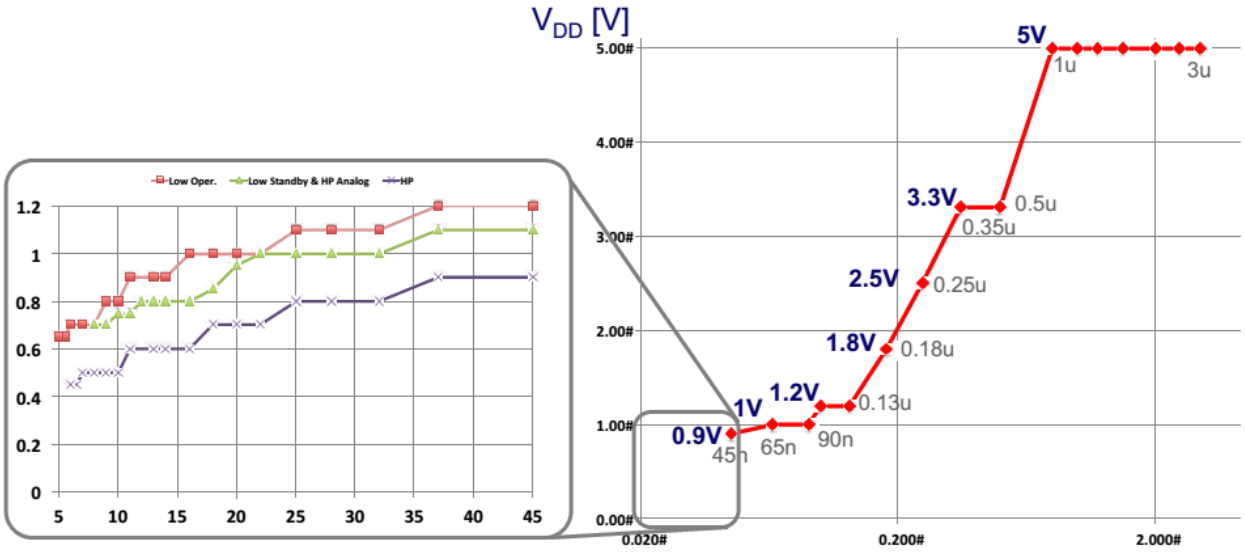


Figure 1.2 Scaling trend of the power supply voltage

transistors and directly benefited from the transistor scaling under fixed operating frequency while the active power of the analog blocks are usually limited by other factors such as signal to noise ratio(SNR), gain and bandwidth requirement. For the amplifier limited by the SNR, we have the following equation (1.3-1.4):

$$SNR \propto \left(\frac{V_{Signal}^{2}}{4kT \times \gamma \times (1/g_m) \times Bandwidth}\right) \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots . (1.3)$$

$$g_m \propto I \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots . (1.4)$$

Therefore, we can get:

$$Power = I \times V_{DD} \propto 4kT \times \gamma \times Bandwidth \times SNR \times V_{DD} \dots \dots \dots \dots \dots \dots \dots \dots \dots \dots . (1.5)$$

Those requirements (SNR, bandwidth) are often set by the application specifications instead of technology. Obviously, the power is not directly benefit from the channel scaling but only benefit from the power supply voltage V_{DD} scaling. However, the V_{DD} scaling is heavily slow down as shown in the Figure 1.2. Moreover, for the amplifier limited by the gain and

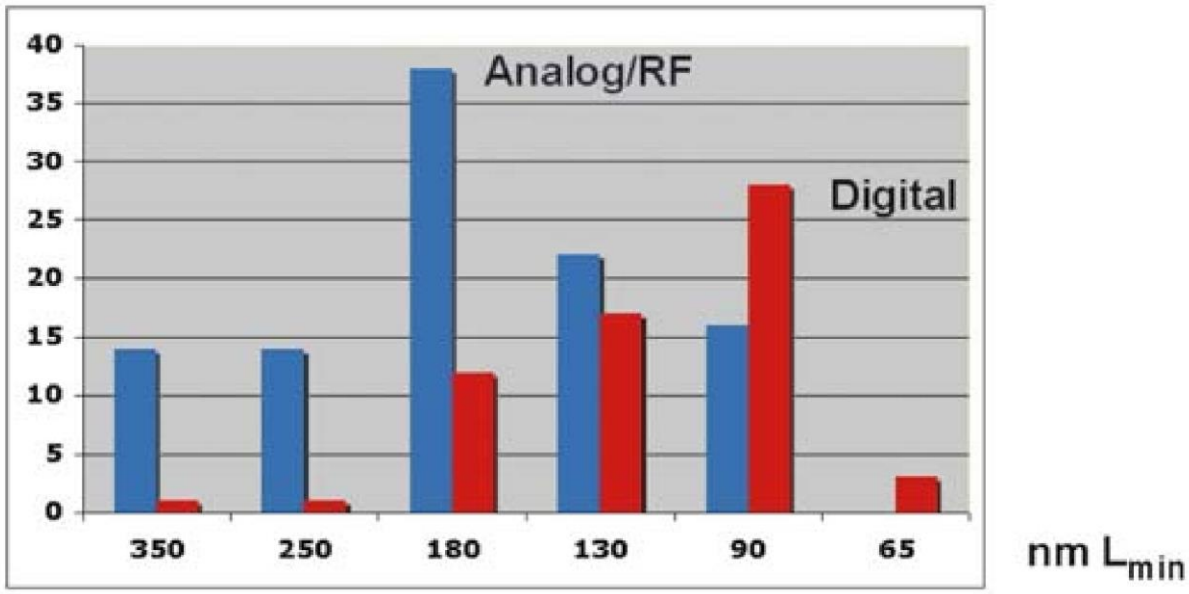


Figure 1.3 Distribution of the ISSCC paper in 2005 [15]

bandwidth requirement, the harsh gain requirement even enforce the analog blocks to use the channel length larger than the minimum value, as a result, the analog blocks prefer to use older technology as it is shown in Figure 1.3 [15].

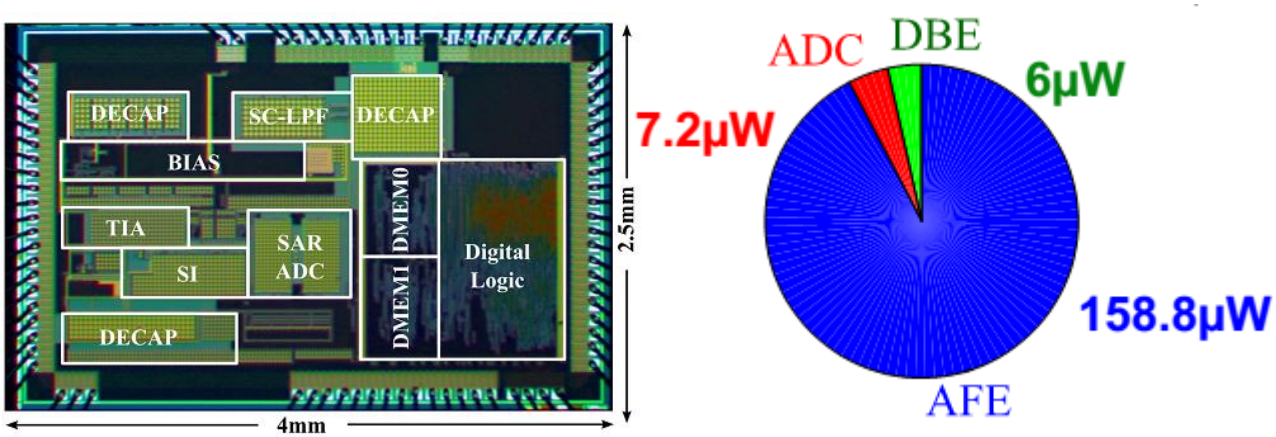


Figure 1.4 Power breakdown example of a biomedical processor [94]

For the leakage power of the circuits, while the digital blocks utilize the smallest possible channel width of each technology, the analog blocks require to use larger channel width for reducing flicker noise, maintain in the saturation region and conduct large active current. Therefore, the analog blocks usually have larger leakage current than the digital blocks. Also, while the digital blocks usually power gated and consume only leakage power. The analog blocks such as sensor interface, wakeup receiver and voltage reference are required to be always on and consume active power instead of sleep power [11-14]. As a result, the power consumption of the entire IoT system are usually dominate by the analog blocks. Figure 1.4 shows an example of the power breakdown of such a system.

In conclusion, the analog blocks power scaled little compared to the digital block, and the development on the technique to reduce the power consumption is vital for the next generation computers.

1.3 Methods to Reduce the Power Consumption of the Analog Blocks

To address of the power consumption problems of the analog building blocks as mentioned in the section 1.2. This thesis is targeting on reducing the power consumption of the analog blocks. As it is shown in the Figure 1.5(a), for the ultra-low power system, the power consumption of the analog builds blocks usually consist of two parts: the leakage power and the active power (Equation 1.6).

$$Total\ Power = Active\ Rate \times Active\ Power + Sleep\ Power \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1.6)$$

As it is shown in the Figure 1.5(b), in chapter 2, the main focus will be on reducing the duty cycle of a bandgap voltage reference which is an essential building block for the system. In chapter 3, it is focus on reduce the leakage power of the ESD pad, which is the dominant leakage

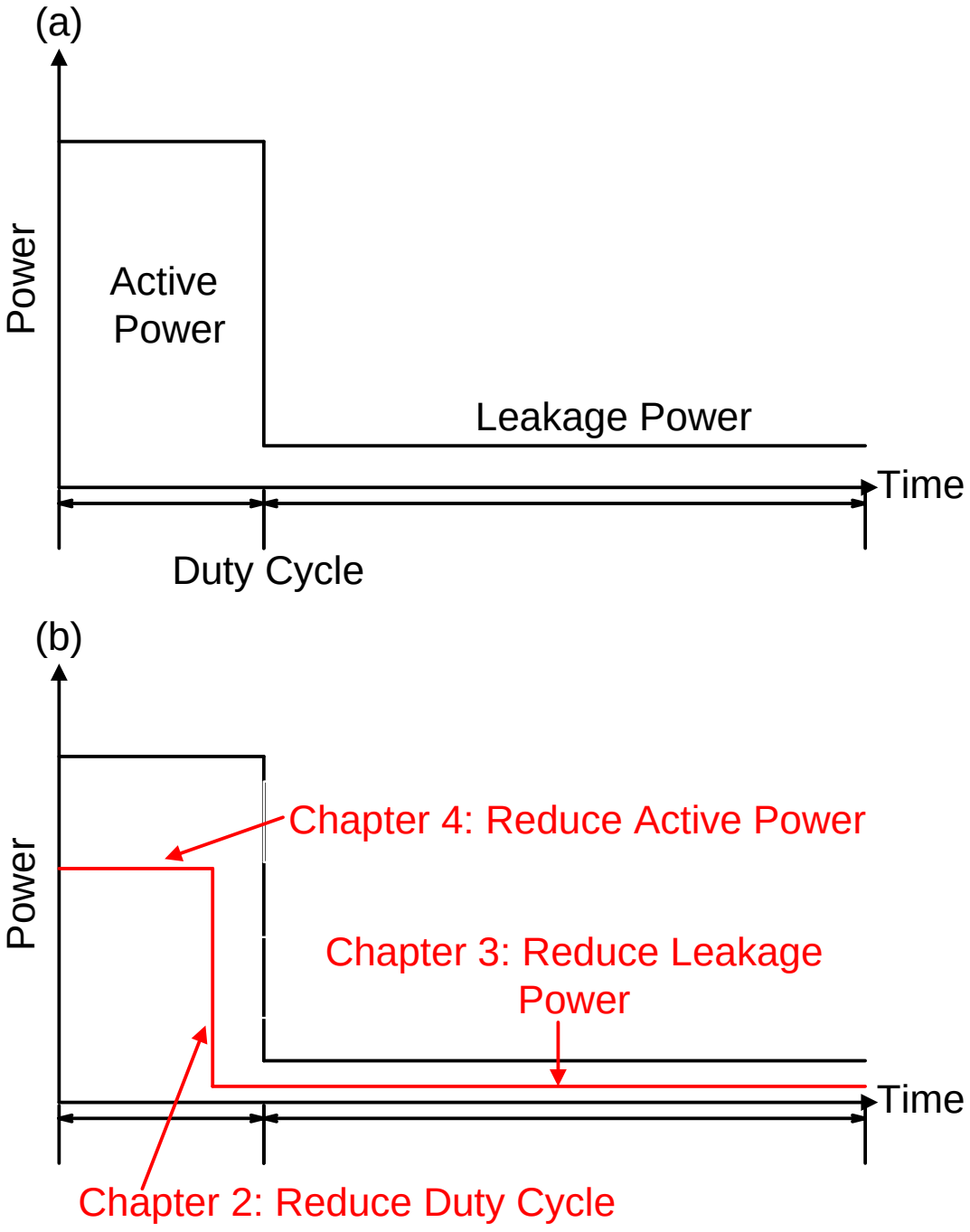


Figure 1.5 Methods to reduce power consumption of analog building blocks

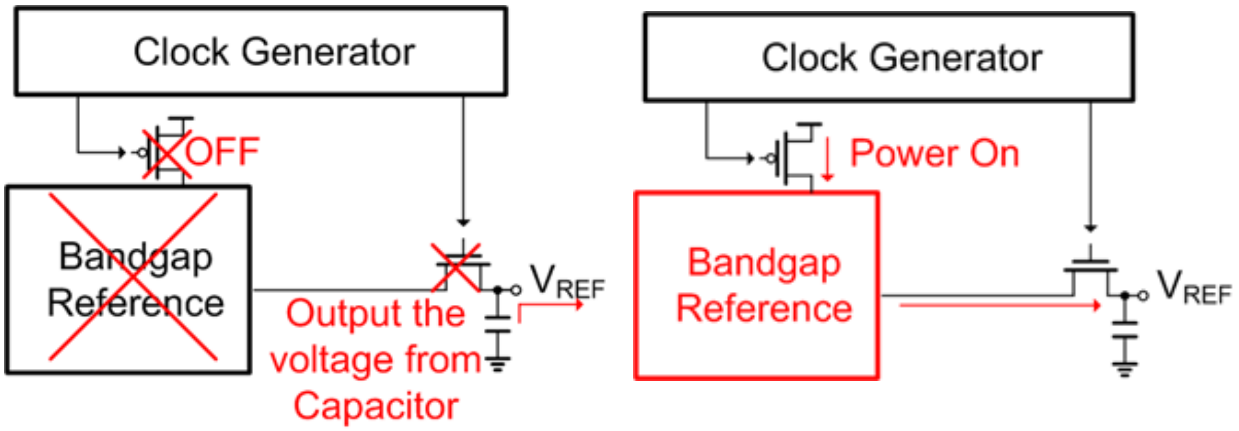


Figure 1.6 Basic concept of the sample and hold bandgap voltage reference

for the ultra-low power mm^3 system [11-12]. In chapter 4, the goal is to reduce the active power consumption while maintain the same SNR for a biomedical amplifier. In chapter 5, we provide a example co-design with the digital blocks showing a system level optimization for reducing the SNR constraint and the power consumption of the analog blocks by advance algorithm on the processor. More detail about each chapter is described in the following section.

1.4 Contributions and Organization

This thesis explores analog power consumption reduction based on the method described in the lase section. The study begins from chapter 2, a novel low power technique to reduce the bandgap voltage reference (which is usually an always-on block in the ultra-low power mm^3 scale system) is presented [16]. The basic idea of the design is to utilize a sample and hold structure to duty cycle the bandgap reference and hence reduce the power consumption as shown in Figure 1.6. The technique also utilized an ultra-low leakage sample and hold circuit with self-calibrating wake up control and leakage compensation makes the voltage reference block duty

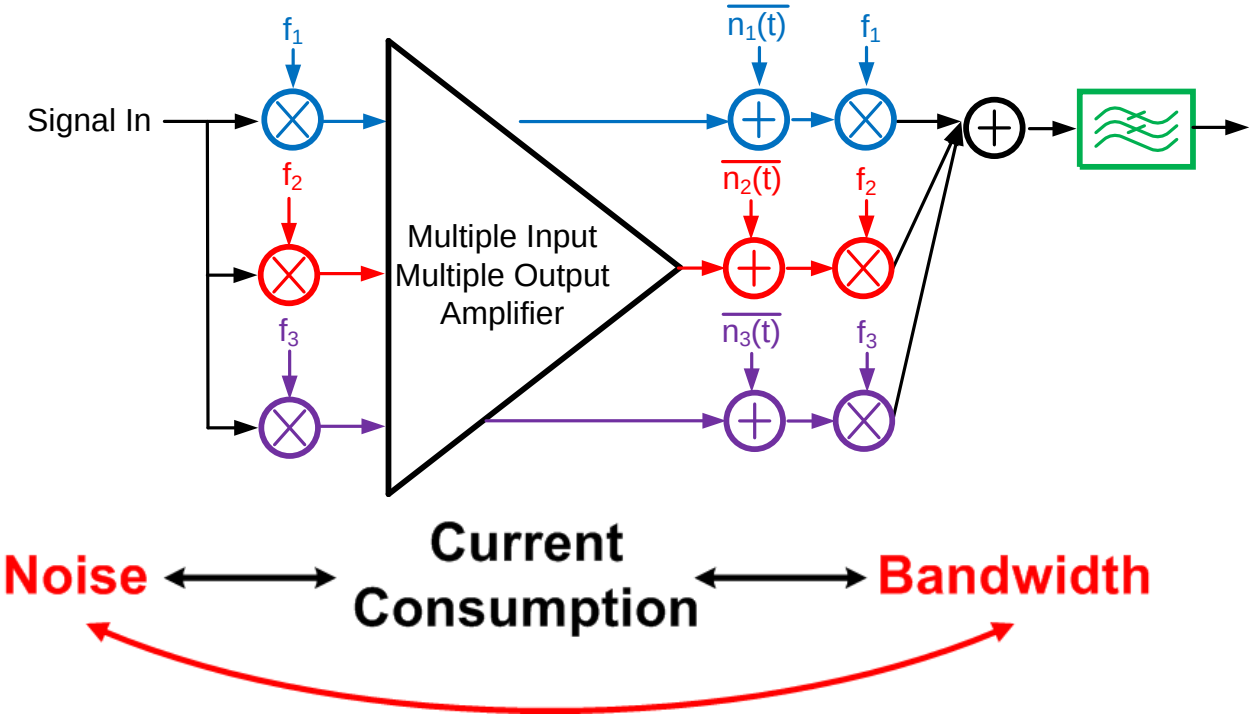


Figure 1.7 The concept of the multi-chopper amplifier

cycled with extremely low active rate. The proposed circuits is implemented in 180nm CMOS, and it shows a temperature coefficient of 24.7ppm/℃ and power consumption of 2.98nW which marks a 251× power improvement over the best prior bandgap voltage reference.

In chapter 3, an ultralow-leakage electrostatic discharge (ESD) power clamp designs for wireless sensor applications are proposed and implemented in 0.18μm CMOS is presented [17]. The ESD Structure is required to be always active to have minimum response time to discharge the electrostatic events. Also, due to the nature of the ESD clamp needs to have relative larger width for conducting massive electrostatic current, the ESD clamp experience almost largest leakage among all the blocks. The power consumption of typical ESD pads are at nano watt range and the total power consumption from all the pads are easily excess the 10nW budget of the ultra-low power system. While a typical ESD power clamp structure consume at nano watt

Table 1.1 The theoretical performance scaling with the proposed N frequency multi-chopper amplifier technique

	Typical Amplifier	Proposed N frequency Multi-Chopper Amplifier
Gain	A	$N \times A$
Output Noise	$A \times V_{input\_referred\_noise}$	$\sqrt{N} \times A \times V_{input\_referred\_noise}$
Input Referred Noise	$V_{input\_referred\_noise}$	$\frac{V_{input\_referred\_noise}}{\sqrt{N}}$
Normalized NEF	1	$\frac{1}{\sqrt{N}}$
Required Bandwidth	BW	$BW \times (2^N + 1)$

range [18-20], by using new biasing structures to limit both the subthreshold and GIDL leakage, the proposed design consumes as little as 43pW at 25˚C and 119nW at 125˚C with 4500V HBM and 400V MM protection level, marking an 18-139× leakage reduction over conventional ESD clamps.

In chapter 4, a newly developed technique to establish the trade-off between the bandwidth and noise is presented to better utilized the current efficiency and hence reducing the overall power consumption. The basic idea is shown in Figure 1.7. By implement multiple chopper and chop the signal into different frequency domain and utilize the current reuse technique which is widely use in the RF circuits, the noise floor can be deduced under the same current level with the sacrifice on the bandwidth. A low power high efficiency neural signal

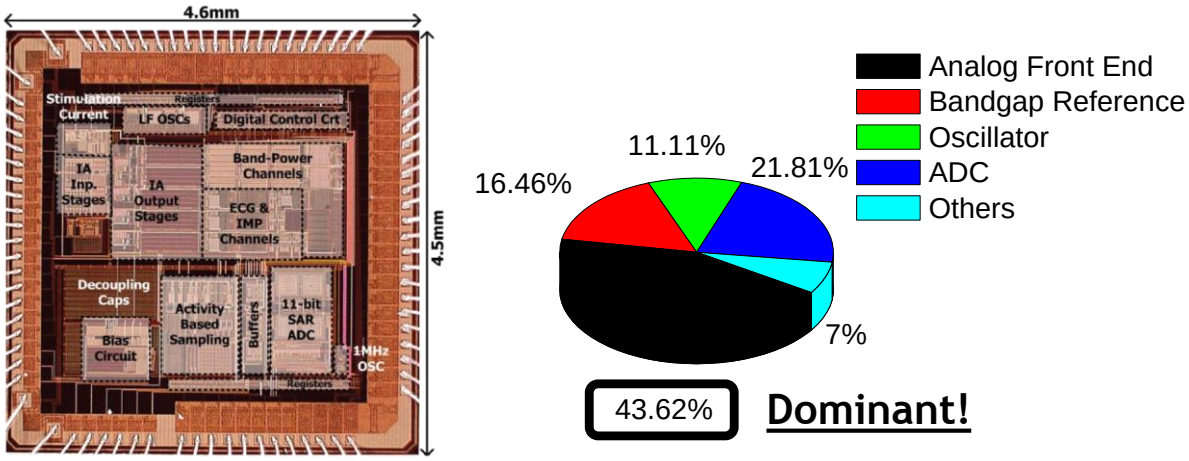


Figure 1.8 Power consumption breakdowns of [23]

recording amplifier with the above novel multi-chopper technique is proposed and implemented in 180nm CMOS to demonstrate this technique [21]. The input referred root mean square noise is 1.54μV (1-500Hz) with 266nA tail current. The result corresponds to a 1.38 noise efficiency factor, which is the best reported among current state-of-the-art amplifiers and is lower than the theoretical limit of the differential amplifier (NEF = $\sqrt{2}$). Table 1.1 shows the summarized results of this technique.

In chapter 5, a syringe-implantable electrocardiography (ECG) monitoring system is proposed [22]. The optimization on the algorithm and the advance circuit techniques in the analog front end (AFE) enable 31nA current consumption while a minimum energy computation approach in the digital back end reduces digital energy consumption by 40%. The proposed SoC is fabricated in 65nm CMOS and consumes 64nW only while successfully detecting atrial fibrillation arrhythmia and storing the irregular waveform in memory in experiments using an ECG simulator, a live sheep, and an isolated sheep heart. Compared to the previous system as [23] and the biomedical system shown in Figure 1.4 have unbalance power consumption between

analog and digital blocks as shown in Figure 1.8 the analog front end power and digital power are well balanced thanks to the co-optimize on the system level.

Several techniques are developed in this thesis and offered new insights on the low power analog circuits design. All the presented projects and possible future works are concluded in chapter 6.

To summarize, this work makes the following new contributions:

- Develop a technique to reduce the duty cycle of the bandgap voltage reference.
- Demonstrate a technique to reduce the leakage power of the ESD pads which is the dominant leakage source in many low power systems.
- Discuss the theoretical limit of the power consumption of the amplifier due to the noise requirement and develop a technique to push the limit with the cost of the bandwidth
- Present a whole ECG system design to show how to balance and optimize the power consumption between the analog and digital block

CHAPTER 2

Sample and Hold Bandgap Voltage Reference for Ultra Low Power System

A precision voltage reference that is insensitive to process, voltage, and temperature fluctuations is a key building block in mixed-signal and analog systems. Given a recent emphasis on low-power battery-operated systems, including wireless sensors, ultra-low power voltage references are needed. Many low power voltage reference circuits have been presented [24]-[28]. In [24, 25], different V_{th} devices are used to achieve low power consumption while the output voltage of the design in [26] is equal to V_{th}. However, V_{th} can vary substantially (particularly across device flavors), and is highly technology dependent. The voltage of Bandgap references are set by fundamental parameters and therefore exhibit lower process spread. However, their power consumption is higher; a prior work on low power bandgap reference presented in [27] consumes 1μW, which is large relative to recent ultra-low power microsystems [12] with nW power budgets. New structures for bandgap references have been developed [28], but power remains in the μW range. Some duty cycled bandgap reference is presented [29-30]. However the large noise [29] and specialized fabrication requirements [30] of these works are design goal to avoid in this work.

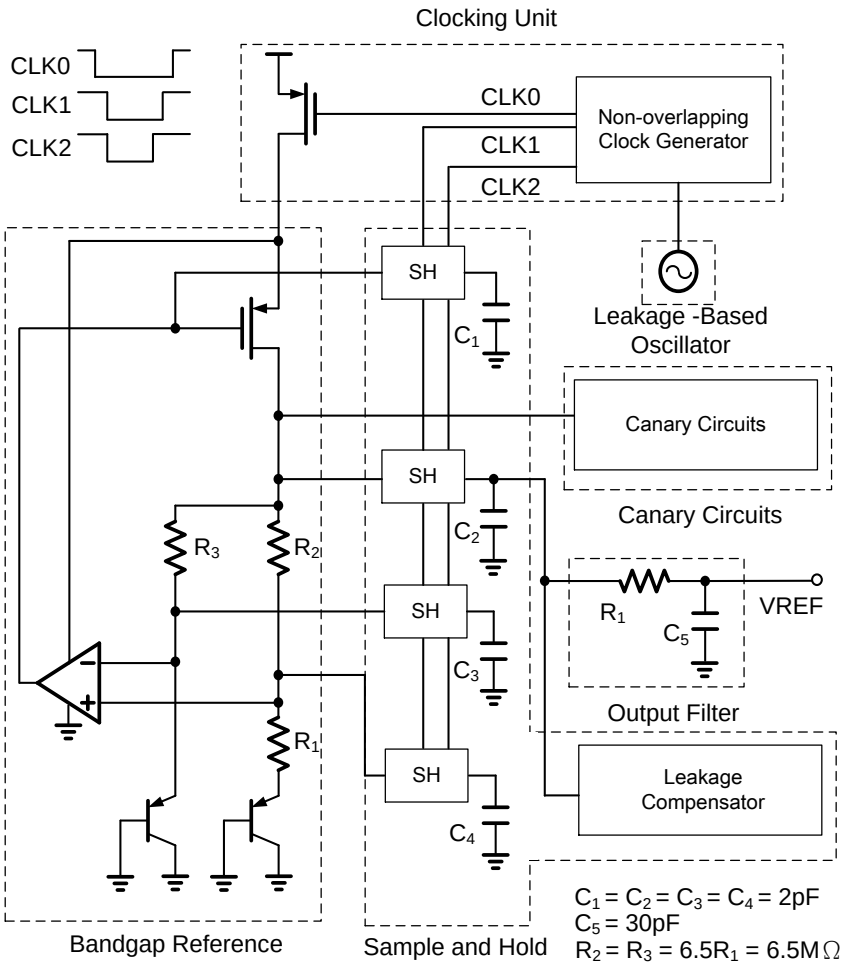


Figure 2.1The structure of the proposed sample and hold bandgap

In this chapter, we present a low power reference that consumes 2.98nW at room temperature in 180nm CMOS. The reference uses a sample and hold technique where the bandgap is duty-cycled to save power consumption. A low (0.015 at 25℃) duty cycle is achieved through three methods: 1) Sampling, holding and restoring the internal node voltages of the bandgap reduces the refresh time by 11.5×; 2) Equalizing the voltage across the sample and hold switch using a subthreshold opamp, increases the sleep time by three orders of magnitude; 3)

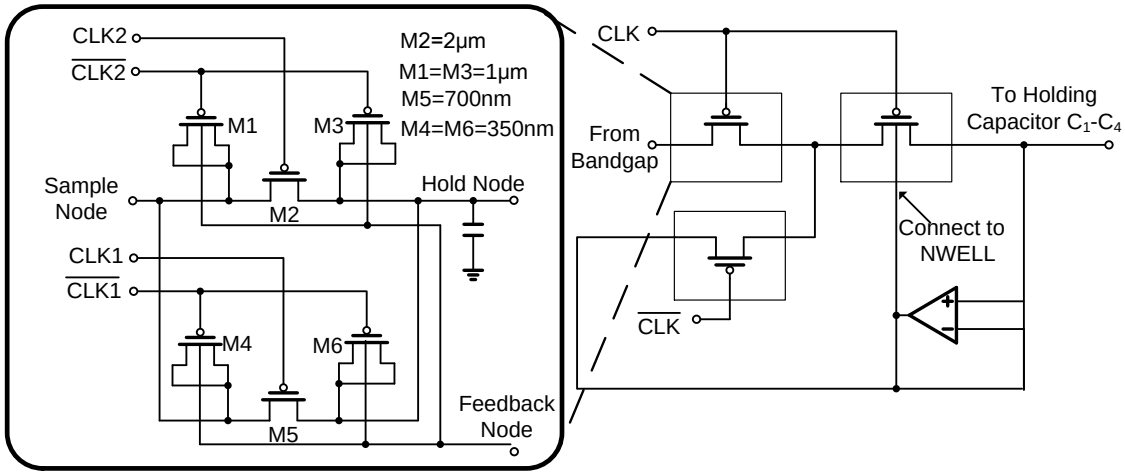


Figure 2.2 Low injection error switches and the structure of sample and hold block

Automatic tuning of sleep time and a gate leakage compensation capacitor using a canary circuit maintains optimal power consumption across temperature. Finally, a new low injection error switch structure reduces noise from the sample and hold circuits. Each of these methods will be explained in more detail below.

2.1 Overview of Sample and Hold Bandgap Reference

Figure 2.1 shows the structure of the proposed sample and hold bandgap. The bandgap itself is a traditional design with single point trimming of the resistor. In active mode, the bandgap is ON (CLK0 is low) and the output and intermediate node voltages are stored on sample and hold capacitors C1–C5. In sleep mode CLK0 goes high to power gate the bandgap, while the sample and hold circuits continue to output the reference voltage. A delay line generates clocks for the sample and hold switches and bandgap power gate using an on-chip leakage-based oscillator, periodically waking the bandgap and refreshing the voltage levels.

2.2 Technique to Decrease Duty-Cycle of Bandgap Reference

Power consumption during the active and sleep modes is dramatically different (aft), making average power heavily dependent on achievable bandgap duty cycle. The two critical factors determining duty cycle are bandgap wake-up time and leakage in the sample and hold circuits. To speed bandgap wakeup and stabilization time, three internal nodes are sampled in addition to the reference output voltage using capacitors C1- C4 (Figure 2.1). Once the bandgap enters wake-up mode, these stored values drive the nodes inside the bandgap, speeding wake-up by 11.5× (from 55ms to 4.8ms) based on simulation.

To reduce leakage in the sample and hold circuits, a feedback structure is used as shown in Figure 2.2. The main sources of leakage in the sample and hold circuit are shown in Figure 2.3. And the following equation shows the leakage for each source and its formula (2.1)-(2.4):

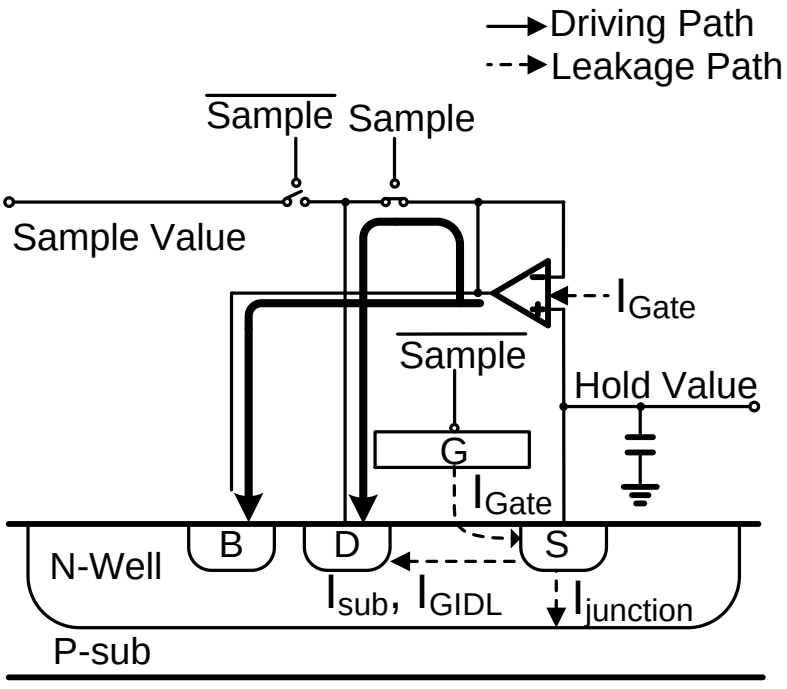


Figure 2.3 The primary leakage sources of the sample and hold circuits

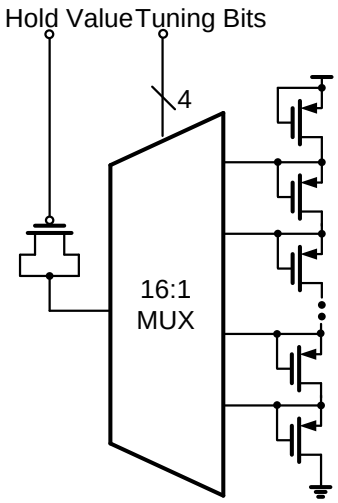


Figure 2.4 Gate leakage compensator

$$I_{subthreshold} \sim 20fA \propto \left(1 - e^{\left(\frac{V_{ds}}{C1}\right)}\right) \quad (2.1)$$

$$I_{junction} < 1fA \propto \left(e^{\left(\frac{V_{bd}}{C2}\right)} - 1\right) \quad (2.2)$$

$$I_{GIDL} < 1fA \propto \frac{V_{db}^3}{C3 + V_{db}^3} \quad (2.3)$$

$$I_{gate} \sim 150aA \quad (2.4)$$

To eliminate junction and subthreshold leakage in sleep mode, a unity gain buffer drives the PMOS pass transistor source voltage onto its body and drain. This reduces V_{bs}, V_{db}, and V_{ds} to very small values dependent on amplifier gain and offset. From simulation, the subthreshold opamp consume 1.22nW with an offset of approximately 1mV (10K Monte Carlo runs).

Measured results show that the subthreshold, junction, and GIDL leakage sources are reduced to the same magnitude as gate leakage at room temperature using this method. To minimize gate leakage, thick oxide I/O devices (t_{ox} >5nm) are used in the subthreshold amplifier and pass transistors.

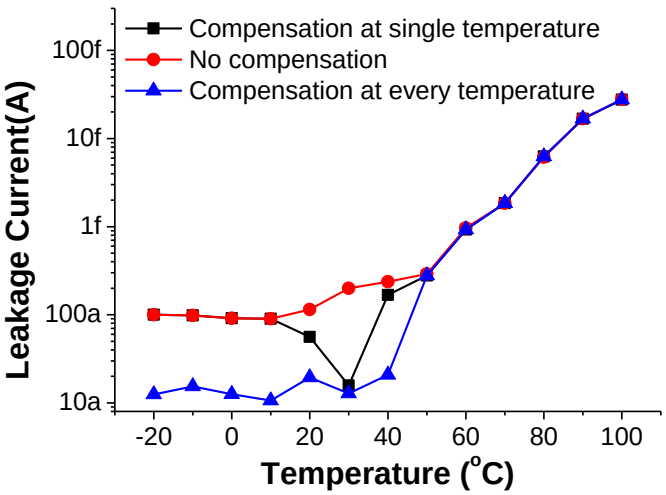


Figure 2.5 Hold time and equivalent leakage in the holding circuits for 100μV error

To further reduce gate leakage, a compensation capacitor with selectable voltage drop is connected to the sample and hold storage node (Figure 2.4) reducing the residual gate leakage to as little as 0.01fA based on measurements. Figure 2.5 shows the total leakage across temperature computed from silicon measurements when no compensation is used and with a fixed compensation setting that minimized leakage at 25℃. The graph shows that while effective, the fixed compensation is capable of improving leakage in only a small range of temperature. To increase this range, an on-chip canary circuit is used to dynamically generate the compensation

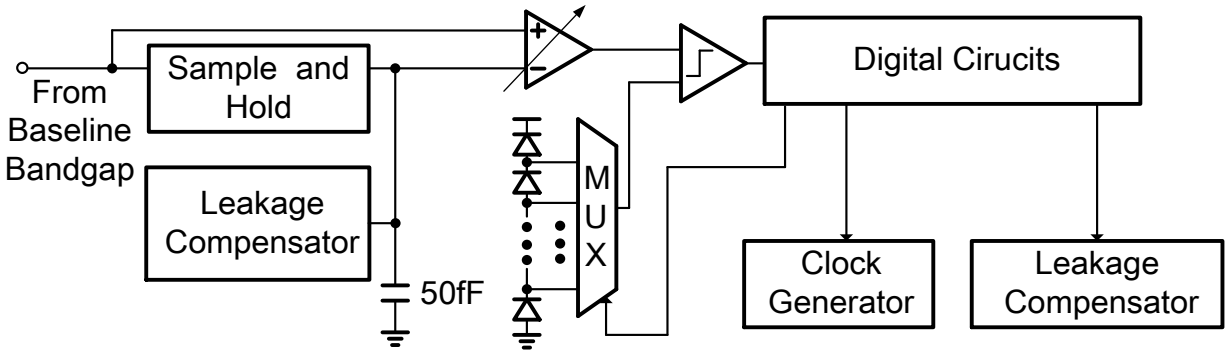


Figure 2.6 Structure of canary circuits and the automatically tuning loops

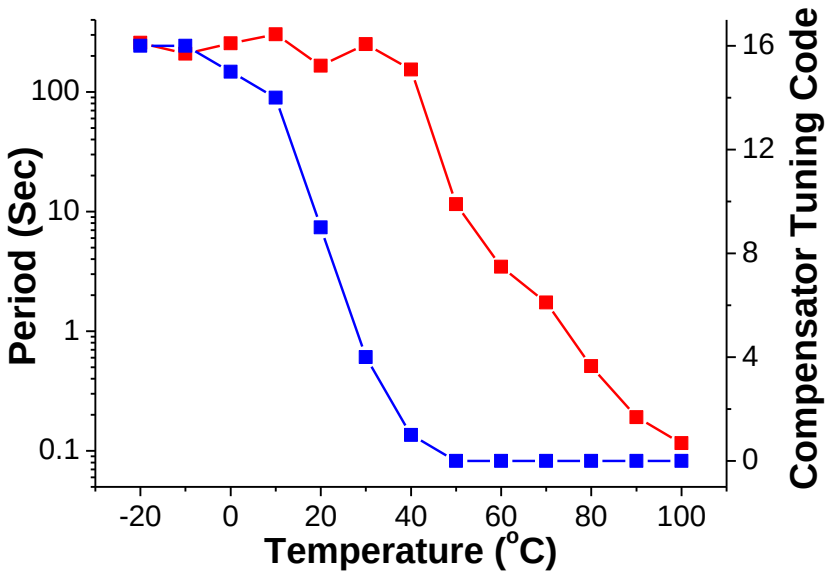


Figure 2.7 Hold time and automatically tuning code with canary circuits

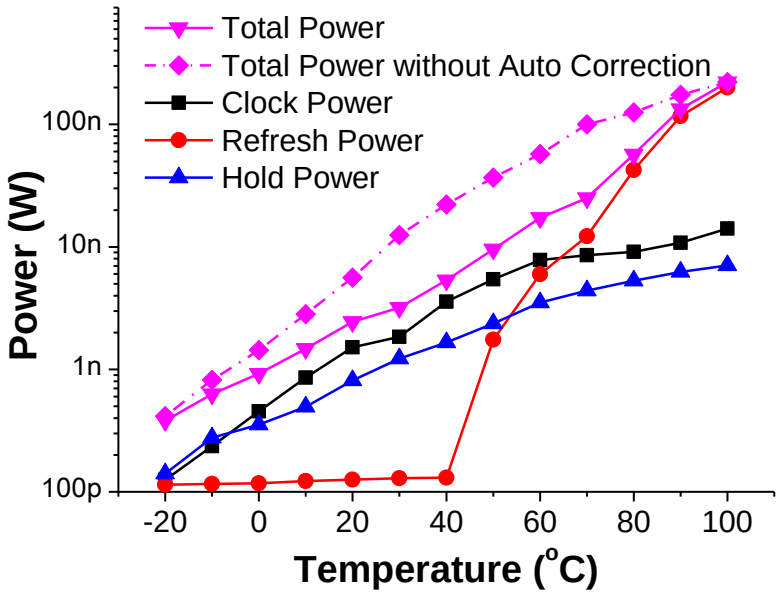


Figure 2.8 Power consumption with canary tuning and comparison with the circuits without canary

tuning. Figure 2.6 shows the canary circuit implementation, which includes an identical copy of the sample and hold circuit, but with a smaller storage capacitor (50fF) to generate an amplified voltage drift. Whenever the bandgap enters wakeup mode, the voltage difference between active bandgap and canary output are compared to a programmable threshold. The output of the comparator drives control logic (implemented off-chip for experimentation purposes) that control the leakage compensation setting dynamically. Figure 2.7 shows that using this method, the effective compensation range is extended from -20℃ to 40℃. Above 40℃ subthreshold leakage becomes dominant and the gate leakage compensator would have to be increased to remain effective.

The canary circuit was also used to automatically set the length of the refresh period. If the voltage difference between the canary and bandgap exceeds a specified threshold, the refresh period is automatically reduced, and vice versa. Figure 2.7 shows the refresh period and compensation tuning code across temperature when a flat 100μV sample voltage error is maintained across temperature using this approach. Figure 2.8 shows the corresponding power

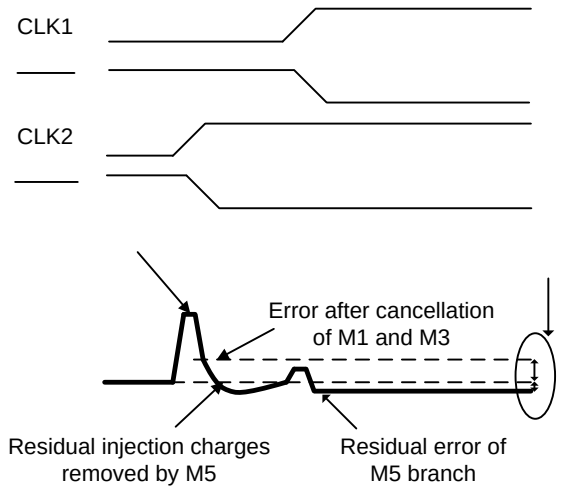


Figure 2.9 Waveform of noise injection of the proposed voltage reference

breakdown. At 27℃, a total power of 2.98nW is achieved, which is a 2.75× improvement over the power consumption without canary based tuning of compensation code and refresh period.

2.3 Technique to Address Clock Injection Issue from Sample and Hold

Finally, to reduce clock noise injected onto the reference by the sample and hold circuits, a low injection error sample and hold switch is proposed in Figure 2.2. M1, M3, M4 and M6 are sized to cancel out injection error from M2 and M5. However, transistor mismatch still introduces random injection charges onto the holding capacitor. To minimize this mismatch-induced injection, two switches, a large switch M2 and a small switch M5, are used in parallel. Initially, both are turned on providing fast sampling. M2 is then turned off; while M5 remains on to remove injected charge. Since M5 is smaller the final injected charge is reduced by 1.89× without increasing sampling time. Finally, an RC filter is added to eliminate high frequency switching noise. The waveform is shown in Figure 2.9.

2.4 Noise Analysis on Proposed Voltage Reference

Since the power consumption of newly developed voltage reference sit in the nW range, the noise issue which is not a concern for the traditional bandgap voltage reference is arise for these low power voltage reference. To address this issue, in this paper, the noise performance on the major low power voltage reference is analysis and compared in this section.

Considering a simple bandgap voltage reference shown in Figure 2.10 as a baseline, the thermal noise of the bandgap voltage reference is (the detail is shown in Appendix A.1):

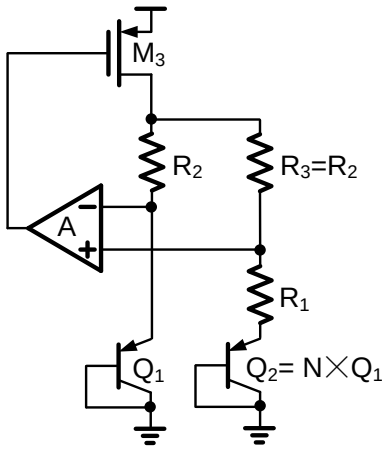


Figure 2.10 The baseline bandgap voltage reference

$$V_{n,total}^2 = \frac{\left(\left(4kTR_1 + \frac{2qI}{g_{m1}^2}\right)\left(\frac{g_{m3}}{g_{m1}}A - 1\right)^2 + 4kTR_2\left(\left(g_{m3}A\left(R_1 + \frac{1}{g_{m1}}\right) + 1\right)^2\right)\right)(g_{m1}R_2 + 1)^2}{\left(g_{m1}g_{m3}AR_1R_2 + (2g_{m1}R_2 + g_{m1}R_1 + 2)\right)^2}$$

$$+ \frac{\left(4kTR_2\left(\frac{g_{m3}}{g_{m1}}A - 1\right)^2 + \frac{2qI}{g_{m1}^2}(g_{m3}AR_2 + 1)^2\right)(g_{m1}R_2 + g_{m1}R_1 + 1)^2}{\left(g_{m1}g_{m3}AR_1R_2 + (2g_{m1}R_2 + g_{m1}R_1 + 2)\right)^2}$$

$$+ \frac{(V_n^2\frac{g_{m3}^2}{g_{m1}^2}A^2 + 4kT\gamma\frac{g_{m3}}{g_{m1}^2})(g_{m1}R_2 + 1)^2(g_{m1}R_2 + g_{m1}R_1 + 1)^2}{\left(g_{m1}g_{m3}AR_1R_2 + (2g_{m1}R_2 + g_{m1}R_1 + 2)\right)^2} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.5)$$

Noted that I is the current in either BJT branch, A is the gain of the amplifier and the amplifier noise is V_n. Also since R_2 is equals to R_3, the current at the two branch are equals. Therefore, $g_{m1} = \frac{I_{Q1}}{V_t} = \frac{I_{Q2}}{V_t} = g_{m2}$ and there is no R_3 and g_{m2} in the equation. By considering every g_mR term is larger than 1 and the amplifier gain is also much larger than 1, we can simplify the equation to be:

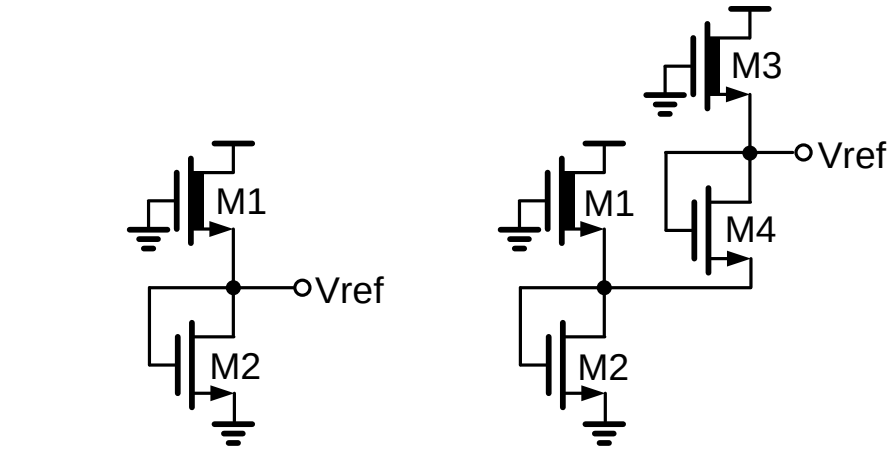


Figure 2.11: The 2 transistor and 4 transistor threshold voltage based voltage reference

$$\mathrm{V}_{\mathrm{n,total}}^2 \cong 4kTR_2 + \frac{2qI}{g_{m1}^2}\left(1+\left(\frac{\mathrm{R}_2+\mathrm{R}_1}{\mathrm{R}_1}\right)^2\right) + \left(\frac{\mathrm{R}_2+\mathrm{R}_1}{\mathrm{R}_1}\right)^2 \mathrm{V}_\mathrm{n}^2 \quad (2.6)$$

In this design, the current of the amplifier is set to be equal to the sum of the two branches of the bandgap voltage reference to balance the noise contribution, and the design point is $V_{ov,amplifier} = 0.1$, $V_{out} = 1.2$ and $V_{BE1} = 0.6$. Therefore, $I = I_{total}/4$, $V_n^2 = 4 \times 4kT\gamma \frac{1}{g_m} = 6.4kT/3I_{total}$, $R_2 = 2.4/I_{total}$, $R_2 = 6.5R_1$ and $2qI/g_{m1}^2 = 8qV_t^2/I_{total}$. And the equation becomes:

$$V_{n,total}^2 \cong \frac{9.6kT}{I_{total}} + \frac{86.5qV_t^2}{I_{total}} + \frac{270.4kT}{3I_{total}} \quad (2.7)$$

To also compare with other threshold voltage (Figure 2.11) based voltage reference, the noise performance of such reference is also being analysis in Appendix A.2. The following equation shows the noise performance of 2-T and 4-T based voltage reference:

$$V_{noise,2T}^2 \cong \frac{qn^2V_t^2}{I} \quad (2.8)$$

$$V_{noise,4T}^2 \cong \frac{2qn^2V_t^2}{I_2} \quad \dots\dots \text{(2.9)}$$

Note that the current I$_2$ is the current pass through transistor M3 and M4, which is typically at least 10x smaller than the total current. The equation shows that the noise current relationship of the voltage reference is similar to the amplifier and the normal bandgap voltage reference with different scaling constant.

For a voltage reference consume 2.98nW at 1.8V VDD, the baseline bandgap voltage reference has noise V_n around $15.9\mu V/\sqrt{Hz}$ while the 2-T and 4-T voltage reference have $1.30\mu V/\sqrt{Hz}$ and $0.278\mu V/\sqrt{Hz}$ respectively. For the sample and hold voltage reference will

Figure 2.12 The calculated noise performance of the sample and hold bandgap voltage reference

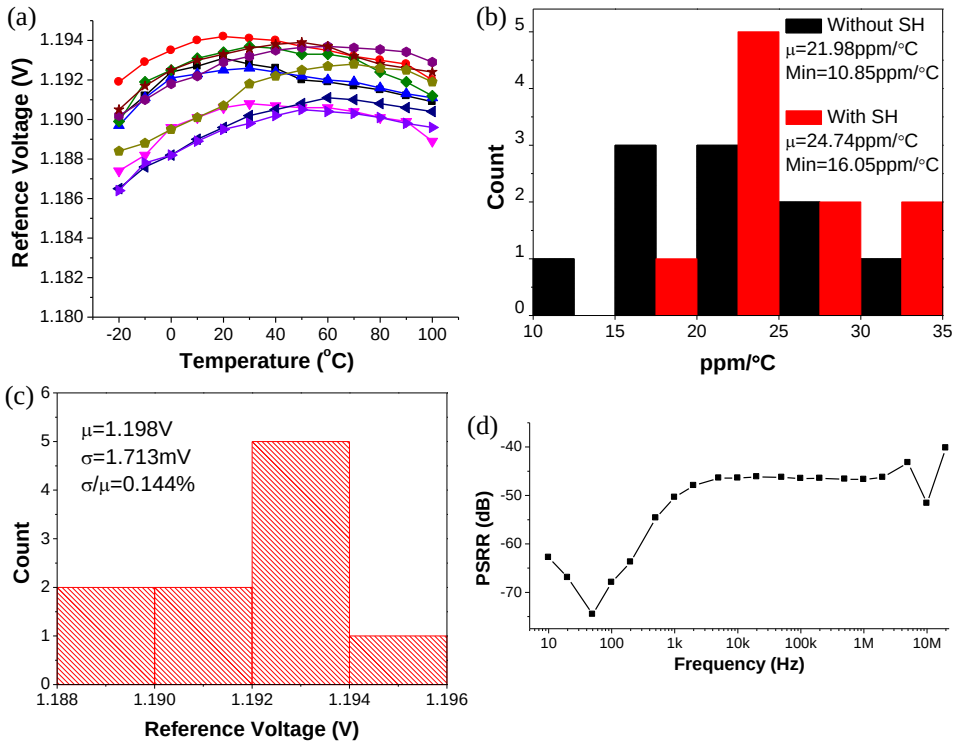


Figure 2.13 (a) Measured output voltage across temperature and ppm/^{o}C (b) Measured output ppm/^{o}C with and without the sample and hold circuits (c) Distribution of the output reference voltage (d) Measured power supply rejection ratio (PSRR)

add up kT/C noise and noise due to the leakage inside the capacitor which is equals to $11.7\mu V$ (with 30pF output capacitor) and $57.74\mu V$ (root mean square value of sawtooth wave with $100\mu V$ amplitude) respectively to the baseline voltage reference. Figure 2.12 shows that the noise performance between the sample and hold bandwidth, baseline voltage reference 2-T voltage reference and 4-T voltage reference across different bandwidth. Noted that the noise of the sample and hold bandgap voltage reference coming from the voltage reference itself is reduced due to the fact that the larger current can be used in the sample and hold voltage reference with the same power budget thanks to the sample and hold technique. As a results, with

Table 2.1 Performance summaries and comparison to other previous works of voltage reference

Parameters	This work	[24]	[25]	[26]	[27]	[28]
Process	180nm	350nm	350nm	350nm	300nm	1.5µm EEPROM
Power	2.98nW	36nW	300nW	1µW	0.75µW	< 2.5µW
TC	24.74ppm/℃	10ppm/℃	7ppm/℃	57.7ppm/℃	370ppm/℃	<1ppm/℃
LS	0.062%/V	0.27%/V	0.002%/V	N/A	N/A	N/A
Duty Cycle	0.015%	N/A	N/A	N/A	0.01	Nearly 0
PSRR	-67dB@100Hz	-47dB@100Hz	-45dB@100Hz	N/A	N/A	< 5dB@10kHz
σ/µ	0.144% (10 dies)	0.82% (20 dies)	7% (17 dies)	2% (60 dies)	N/A	N/A
Area	0.098mm^2	0.45mm^2	0.55mm^2	0.63mm^2	0.45mm^2	1.2mm^2
Type	Bandgap	Δ Vth	Vth Based	Bandgap	Bandgap	Programmable Value

larger desired bandwidth, the sample and hold bandgap voltage reference has better noise performance compared to the normal bandgap voltage reference.

2.5 Summary

The proposed bandgap reference was implemented in standard 180nm CMOS. Figure 2.13(a) shows the measured temperature coefficient (TC) of a standalone bandgap (using the design at left of Figure 2.1) and the proposed sample and hold bandgap (complete Figure 2.1). Figure 2.13(b) shows the distribution of ppm/℃ for the same two cases across 10 dies. The sample and hold circuits have a negligible effect (2.76ppm/℃ change) on TC. Figure 2.13(c)

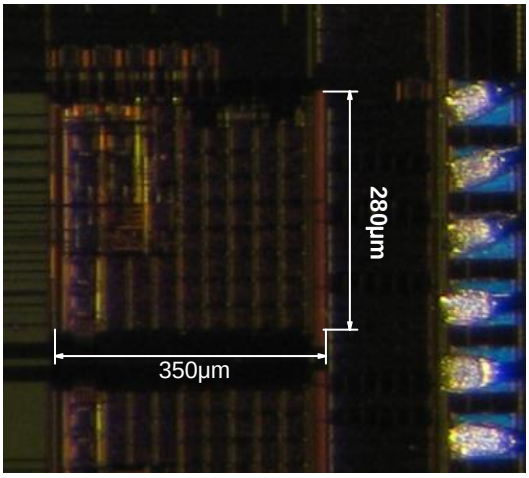


Figure 2.14 Die photo of proposed reference

shows a histogram of bandgap output voltage across 10 dies. The single trimmed mean output value is 1.1918V with of 1.713mV, and σ/μ of 0.144%.. Measured power supply rejection ratio (PSRR) is also shown in Fig. 2.13(d). Since the only injection path is through the PMOS pass transistor and kickback noise in the amplifier, PSRR is small throughout the entire frequency range. The chip micrograph is given in Figure 2.14. Table 2.1 summarizes the testing results, including a comparison to the most relevant prior work.

CHAPTER 3

Low Power ESD Clamp Circuits for Ultra Low Power System

Robustness against electrostatic discharge (ESD) is a critical reliability issue in advanced CMOS technologies. To prevent circuit damage due to ESD events (which can expose the circuit to kV range voltages), ESD clamp circuits are typically incorporated in supply pad library cells. These circuits use extremely wide devices (100s of μm) and thus exhibit leakage currents of 10nA to 10μA (at 25°C and 125°C, respectively) despite the use of various low power approaches [18-20, 31,32]. Recently, there has been increased interest in ultra-low power wireless sensor node systems [6-12, 33] with constrained battery sizes and system standby power budgets as low as 10-100nW. Considering the need for multiple power pads, these systems cannot use existing ESD structures due to their high leakage, thereby compromising their reliability. To address this

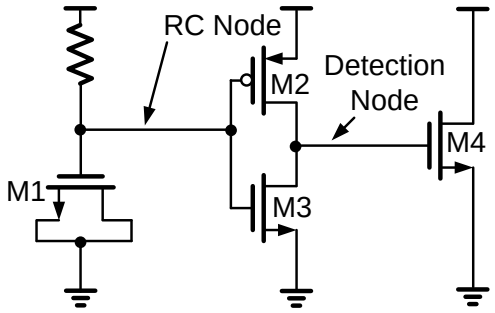


Figure 3.1 Standard ESD schematic

challenge, we propose three ultra-low leakage ESD circuits that use special biasing structures to reduce subthreshold leakage and gate-induced drain leakage (GIDL) while maintaining ESD protection. In 180nm silicon test results, we demonstrate 10s of pA (nA) operation at room temperature (125℃), which is a >100× improvement over prior state of the art.

A standard commercial ESD clamp circuit is shown in Figure 3.1 and consists of an RC filter and inverter to detect the ESD event, as well as a large MOSFET to remove electrostatic charge. All transistors are thick-oxide high Vt devices. When a high voltage is applied to the supply rail due to an ESD event, transistor M2 turns on, pulling up the detection node and allowing the electrostatic charge to be dissipated through the large M4 shunt device. Waveforms for a 7kV Human-Body Model discharge are shown in Figure 3.2. The key parameters associated with achieving high voltage protection are M4 size and the speed at which the detection node is pulled up. After the charge is dissipated, the resistor pulls up the inverter input to turn off the clamp.

Figure 3.3 gives the simulated power breakdown of this conventional design, with two major components: 1) Detection circuits, and particularly, pull up device M2, which dominates

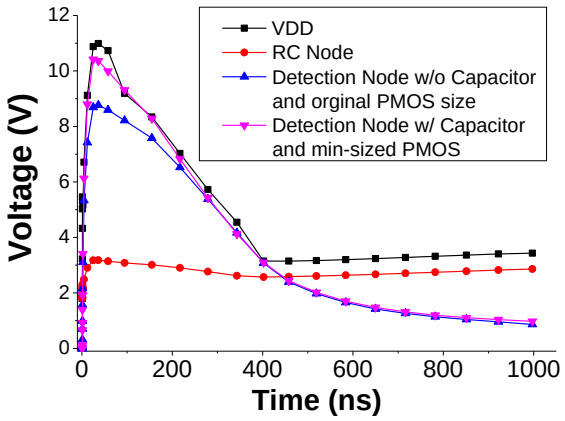


Figure 3.2 Simulation waveform of the modified BJT based structure

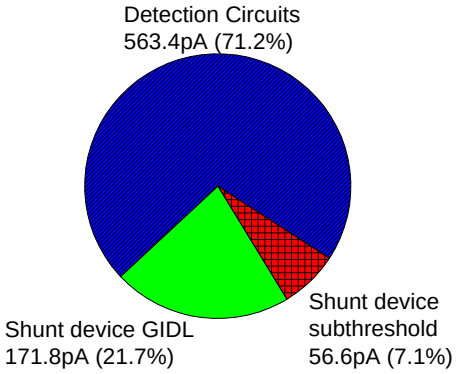


Figure 3.3 Power breakdown of standard ESD schematic

leakage as it is sized up to speed detection and also exhibits poorer subthreshold slope compared to NMOS; 2) the large shunting device M4. Due to the high supply voltage (≥1.8V), GIDL of M5 is larger than its subthreshold leakage.

3.1 Overview of Proposed Technique for ESD Protection Structure

To reduce these leakage sources, we propose and test three circuit structures. The first and most straightforward approach is shown in Figure 3.4. To address M2 leakage, an assisting capacitor is added. At the onset of an ESD event, the supply voltage rises rapidly and this

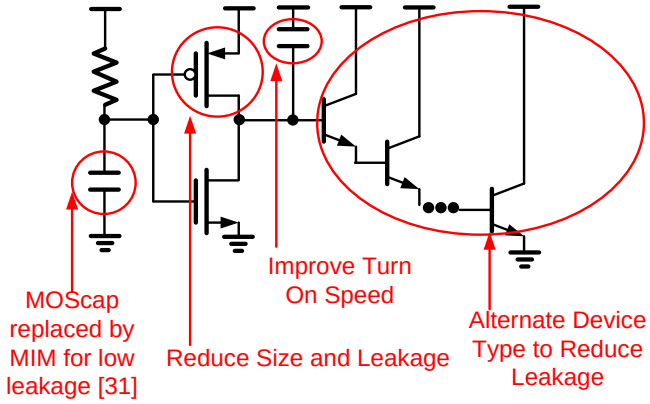


Figure 3.4 The modified BJT based structure

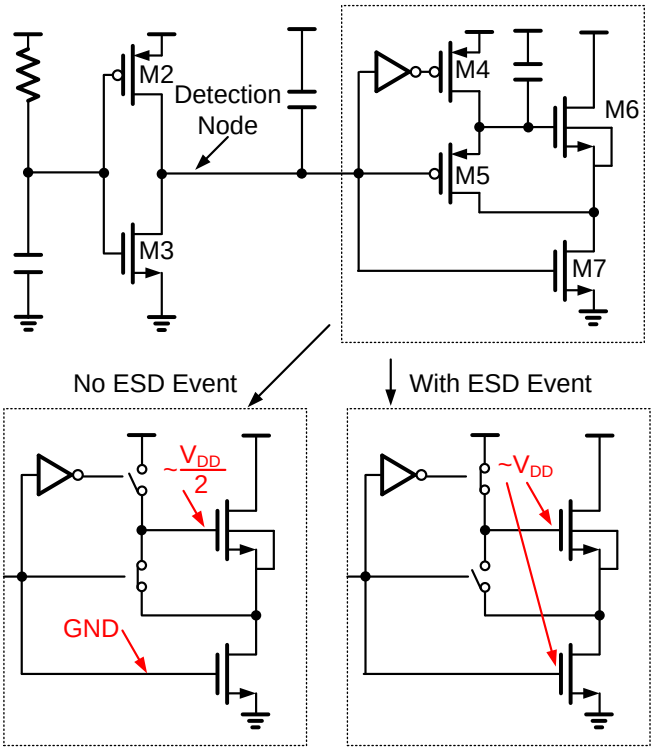


Figure 3.5 Proposed GIDL reduction scheme

assisting capacitor couples the detection node up, allowing the PMOS to be down-sized (near min-size), while maintaining the same effective turn-on speed and ESD robustness.

Simulated waveforms of the detection node in Figure 3.2 show that the assisting capacitor with downsized M2 slightly improves response time. Note that although leakage through the MOS capacitor in this technology is small (<2pA), for a scalable low-leakage approach, a MIMCAP is used in the RC filter (as in [31]). To limit M4 leakage we employ a BJT, which provides lower off-current than MOSFETs. However, in standard CMOS technologies only parasitic BJTs with small current gains are available, making it necessary to use a Darlington-like structure. Overall, these modifications offer 10 - 104× leakage reduction at 25 - 125℃ (silicon measurements below). However, the parasitic BJTs introduce several technology scaling concerns that make MOS-based solutions preferable. In particular, from simulations the base-emitter

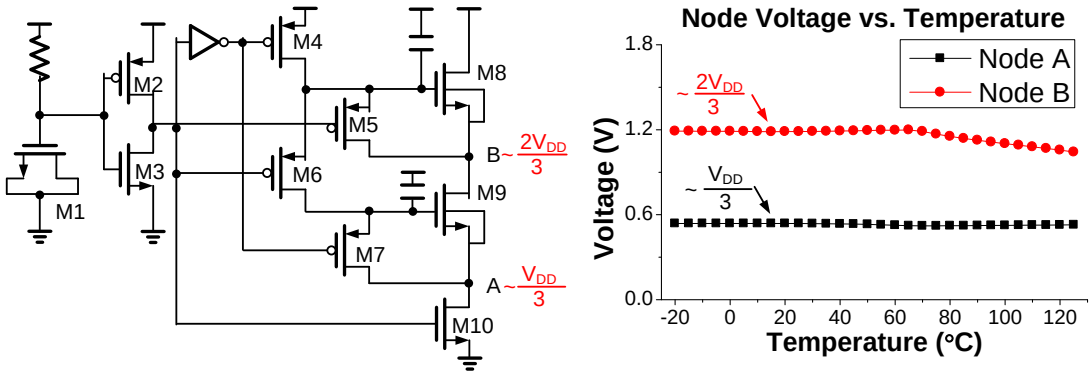


Figure 3.6 GIDL reduction scheme for 3-stack (GIDL-1) with simulated internal node voltages across temperature at 1.8V

current gain drops from 25 in 180nm to 5 in 65nm. Also, bipolar **c**lamp snapback voltage decreases with technology scaling more rapidly than MOSFETs [34], reducing effectiveness for ESD protection.

3.2 Proposed Technique for ESD Protection Structure under CMOS Technology

Due to reason states in the end of section 3.1, we therefore also propose two MOS-based structures that offer similar leakage reduction gains with better scalability and improved density. A well-known approach to reduce MOSFET leakage is stacking, which yields a 2.9× subthreshold leakage reduction in 180nm CMOS. However, as noted earlier, GIDL dominates leakage in the shunt device and hence stacking alone only reduces total leakage by 17%.

The first method to address GIDL in an MOS shunt device is shown in Figure 3.5 and has similarity with [35]. When there is no ESD event the gate and source of M6 are shorted and the stacked shunt transistors M6 and M7 act as a voltage divider. As a result, the key GIDL parameter V_{dg} is reduced by half for both transistors, lowering GIDL by 5.4×. When an ESD event occurs,

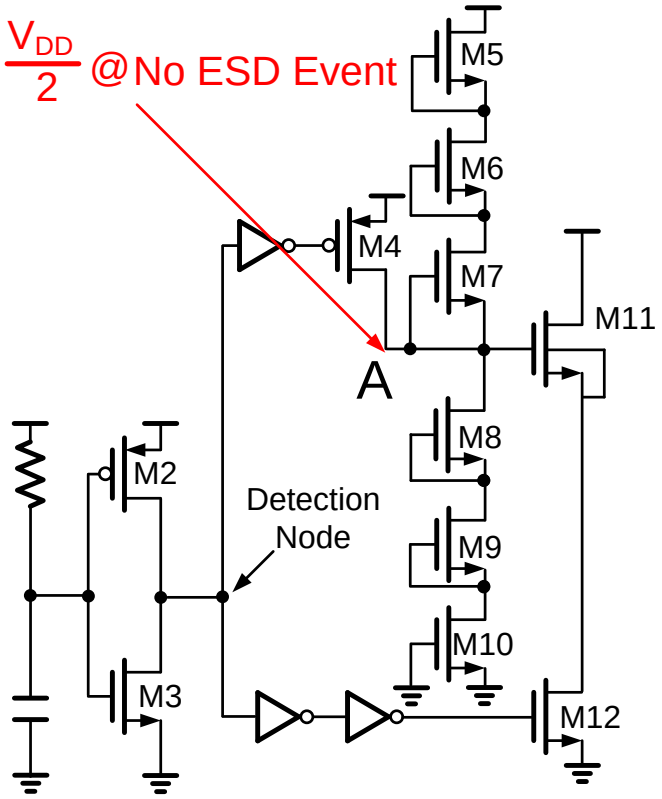


Figure 3.7 Leakage-based GIDL reduction methods (GIDL-2)

the two MOS shunts fully turn on to remove the electrostatic charge. The same concept can be extended to a stack of 3 devices; simulations across temperature in Figure 3.6 show temperature stability across a wide range (-20˚C to 125˚C). The 3-stack structure provides minimum leakage for this approach (denoted GIDL-1). Further extending the method to a 4-stack degrades shunt on-current, requiring device up-sizing for sufficient ESD protection and leading to higher leakage.

The second GIDL reduction approach (denoted GIDL-2) is given in Figure 3.7. In this structure, a bias voltage of approximately $V_{DD}/2$ is generated by a diode stack (M5-M10), which is then applied to the topmost stacked output device (M11) to reduce GIDL in M11 and M12. Since there is no need for leaky PMOS switches in GIDL-2, total transistor area and overall leakage is reduced. Note that diode-connected NMOS M5-M10 have minimum W (with increased

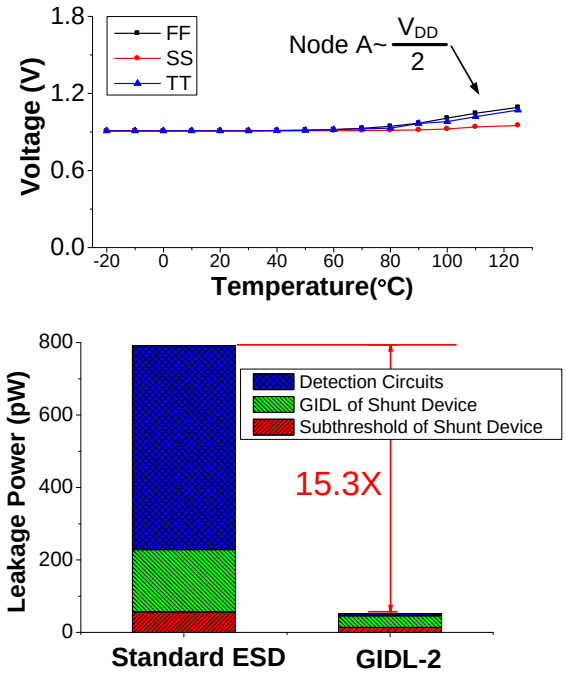


Figure 3.8 Simulated internal node voltage across temperature and corners as well as leakage power breakdown of GIDL-2

L) since they only need to overcome the subthreshold leakage of M4 and gate leakage of M11 to maintain $V_{DD}/2$ at node A. As a result, the diode stack leakage is negligible. Simulations across temperature/process show the stability of node A voltage (Fig. 8). During an ESD event node A is charged to V_{DD} through M4 and then slowly discharges to $V_{DD}/2$ through the diode stack. During this relaxation time (350s in simulation) the ESD clamp experiences substantial GIDL. However, since ESD events are rare, the impact on total energy is minimal and the low quiescent current of the structure far outweighs it. Simulated leakage power breakdown of GIDL-2 is shown in Figure 3.8, showing a 15.3 - 115× reduction (25 - 125℃) compared to a conventional commercial clamp.

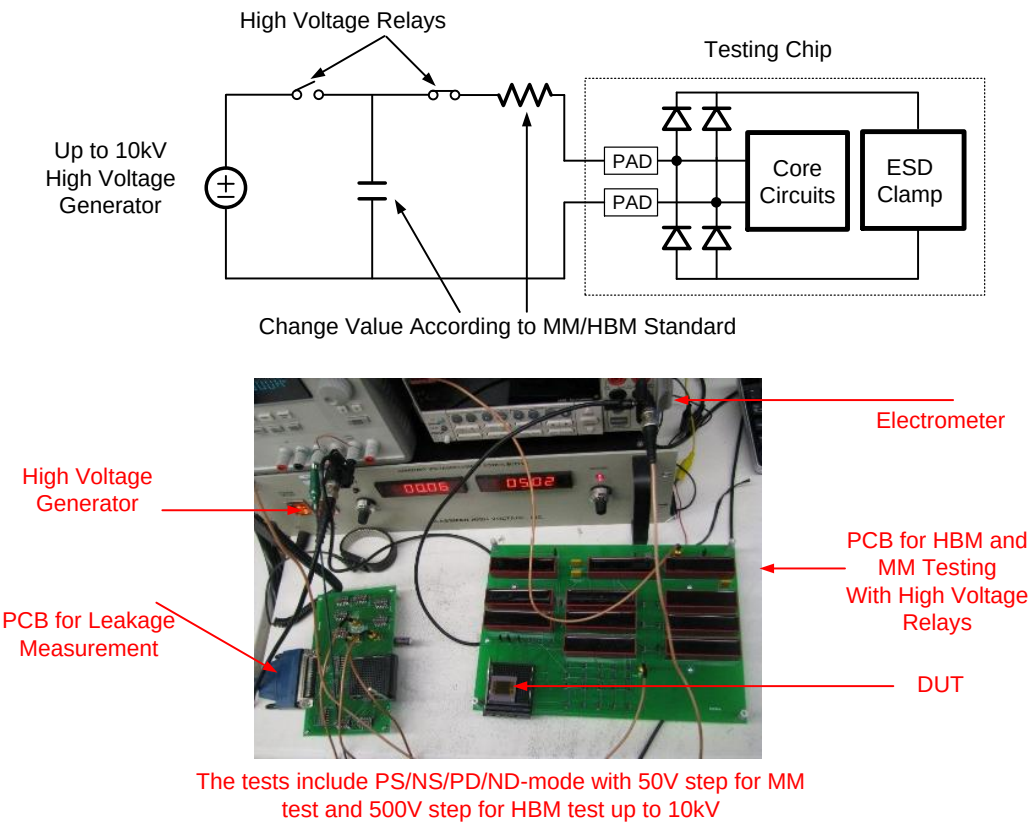


Figure 3.9 Testing setup with high voltage generator for human body model (HBM) and machine model (MM)

3.3 Measurement Results

The three proposed ESD structures (BJT, GIDL-1, GIDL-2) and a commercial ESD clamp circuit (baseline) were fabricated in a standard 180nm CMOS process. In addition, an ESD structure using smaller devices and offering a lower protection level was integrated with a mm-scale microsystem [12] to meet its nW system power budget. The human body model (HBM) and machine model (MM) are evaluated on the ESD structures (Figure 3.9). Device leakage current is measured after each discharge of the HBM or MM test. We use a conventional definition of failure, namely the smallest voltage at which either 1) the structure exhibits a 30% increase in leakage or 2) an analog block connected to the ESD pads functionally fails.

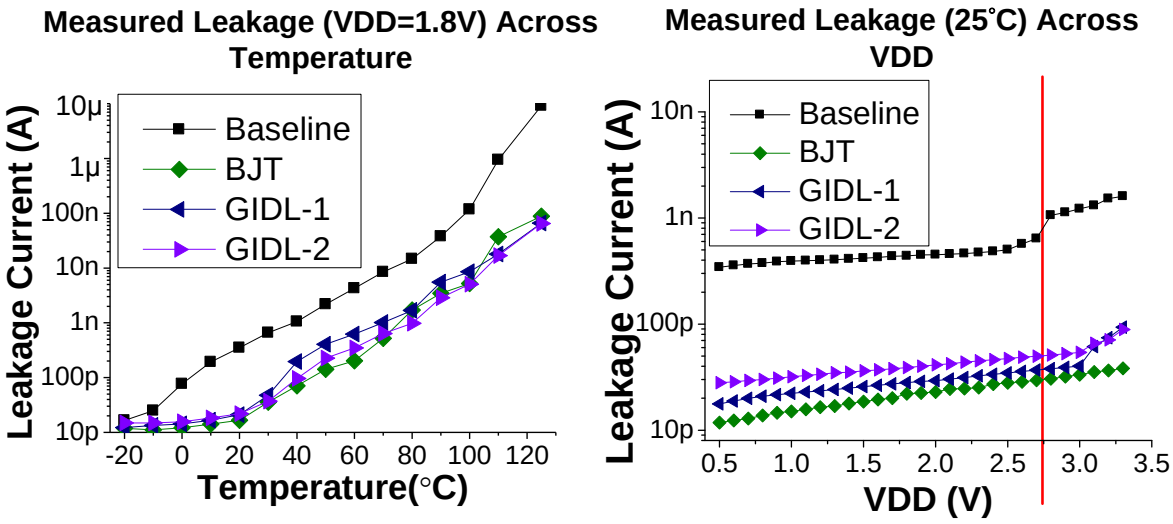


Figure 3.10 Measured leakage results across temperature and power supply

The measured leakage of each structure across temperature and V_{DD} is shown in Figure 3.10. The proposed clamps have lower leakage than the baseline design throughout the temperature range of 0℃ to 125℃ and V_{DD} from 0.5V to 3.3V. The BJT structure has the lowest leakage (22pA) at room temperature, a 20× reduction over the baseline. At 125℃, GIDL-1

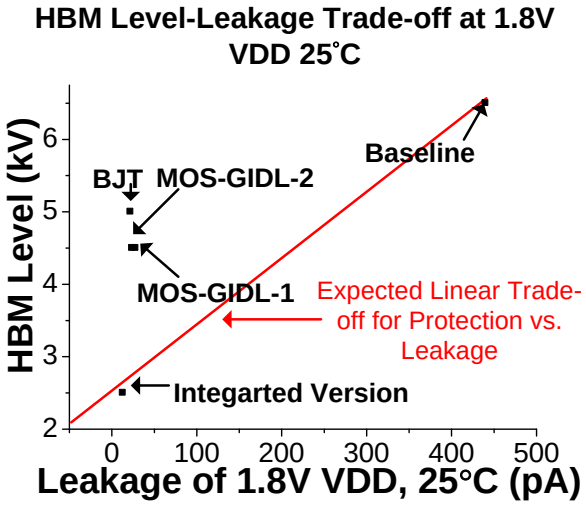


Figure 3.11 Measured scatter plot of baseline and 3 proposed structures

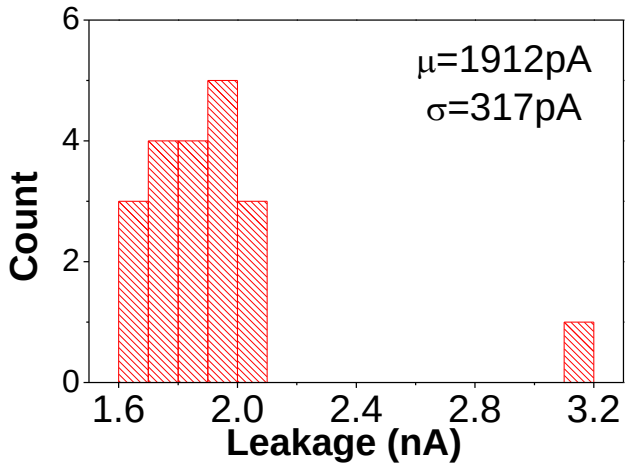


Figure 3.12 Measured histogram of leakage for GIDL-2 across 20 measured dies

and GIDL-2 structures consume 67.8nA and 66nA, respectively, compared to 16.52μA for the baseline. A scatter plot showing ESD protection and leakage (25℃) of the 4 measured structures is also given in Figure 3.11. The expected linear trend between protection level and leakage highlights the gains achieved by the proposed structures beyond straightforward device down-sizing. A histogram of leakage current for GIDL-2 at 85℃ and 1.8V across 20 measured dies from one wafer is shown in Figure 3.12. Nearly all dies consume 1.6−2.1nA with average leakage of 1.91nA and standard deviation of 317pA. The integrated version shows 13pA leakage at 25℃ with 2.5kV HBM level and 300V MM level.

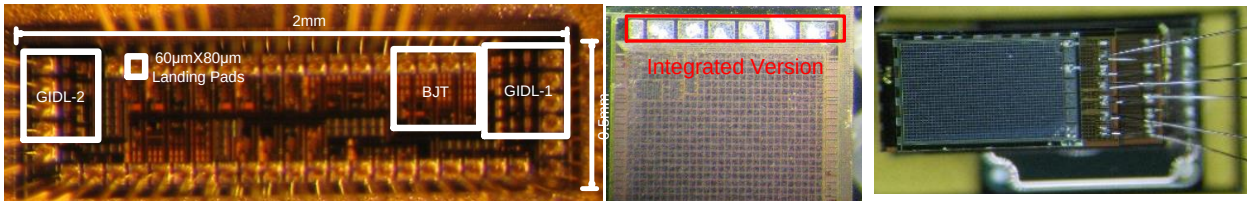


Figure 3.13 Die photo. The BJT, GIDL-1 and GIDL-2 version are shown in the left, and the integrated version is shown in mid. The whole system of mm3 is shown in the right and commercial device is measured in the same run different die

Table 3.1 Summary table of proposed ESD clamp circuits

ESD Structure	Technology	Area (μm^2)	HBM Level (kV)	MM Level (V)	Leakage 1.8V, 25˚C	Leakage 1.8V, 125˚C
Baseline Commercial Clamp	0.18µm	17500	6.5	400	440pA	9.18µA
BJT	0.18µm	67200	5.0	350	**22pA**	88.1nA
GIDL-1	0.18µm	67200	4.5	400	**28pA**	**67.8nA**
GIDL-2	0.18µm	44800	4.5	400	**24pA**	**66nA**
Integrated Version For mm3 system [12]	0.18µm	35000	2.5	300	13pA	41nA
[18]*	65nm	1029 (7891)**	7.0	325	96nA (1V)	1.02µA (1V)
[19]	65nm	N/A	4.0	350	358nA (1V)	1.91µA (1V)
[31]*	0.13µm	N/A	6.5	400	N/A	N/A
[32]*	65nm	N/A	>8.0	750	228nA (1V)	3.14µA (1V)

* Uses special SCR devices

**Normalized to 0.18µm using ideal scaling

3.4 Summary

Overall the proposed GIDL-2 structure provides 18-139× leakage reduction over commercial ESD clamps with 70-100% of ESD protection levels while avoiding special devices such as SCR. Die photos are given in Fig. 3.13. Summary table is given in Table 3.1.

CHAPTER 4

Multiple-Choppers Technique to Increase the Noise Efficiency of the Low Noise Amplifier

Recently, the recording of human body electrical signals has attracted growing attention. Specifically, several low power high density recording devices have been proposed [36]-[38]. Although digital power consumption scales well with technology improvements, the noise requirements of these systems restrict front-end amplifier power improvements due to the fundamental noise efficiency factor (NEF) limits (fundamental limit = 1 with an ideal single BJT amplifier). As a result the analog front-end power limits the number of channels in neural recording arrays, effectively holding back major advances in brain machine interfaces.

4.1 Overview of the Fundamental Noise Limit of the Amplifier

The fundamental power consumption limit of the analog front-end amplifier arises from the white noise of the input transistors. The amplifier NEF is given by:

$$NEF = V_{rms}\sqrt{\frac{2 \times I_{total}}{\pi \times V_T \times 4kT \times Bandwidth}} \tag{4.1}$$

State-of-art neural recording systems typically employ high accuracy amplifiers with a

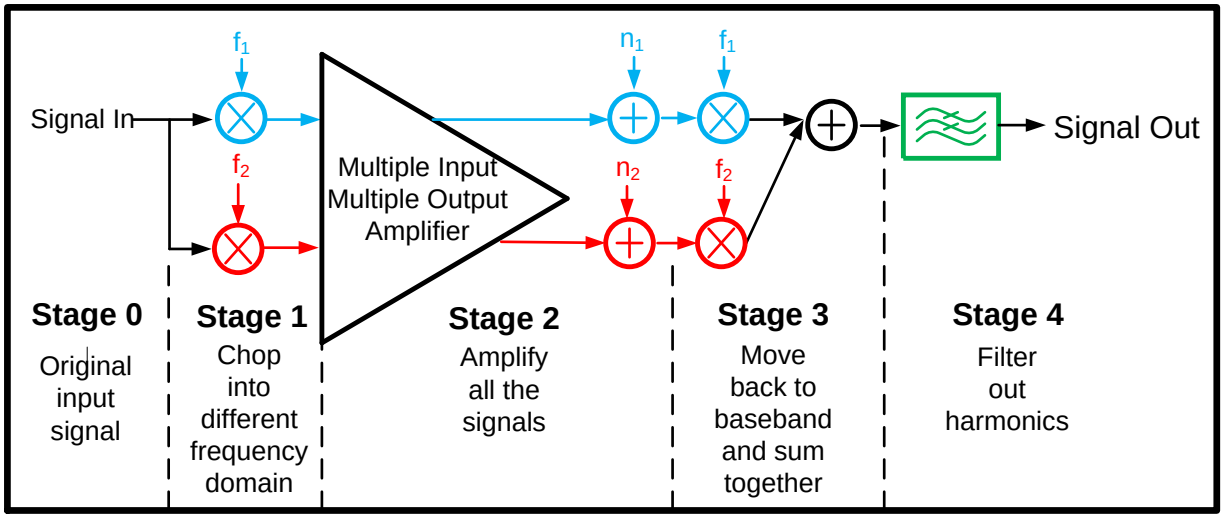


Figure 4.1 Conceptual diagram of the multiple-chopper amplifier (2-stack version)

differential topology and high (> 100dB) power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR). In this case the typical NEF value is 3 [39] while amplifiers with relaxed PSRR and CMRR specifications (> 80dB) exhibit NEFs of ~1.5 [38].

In a traditional front-end amplifier, the current must be sufficiently large to achieve the target noise level. In setting the current to this level, amplifier bandwidth increases beyond the requirement of neural recording, translating to wasted power consumption. For example, setting the current to match a requirement of <5V root mean square noise for ECG signal in 180nm will increase amplifier bandwidth to approximately 20kHz, which exceeds the sub-kHz ECG bandwidth requirement. To reduce the front-end amplifier power consumption, this chapter proposes a novel multi-chopper technique to establish a new trade-off between bandwidth and white noise, and achieves a best-reported NEF.

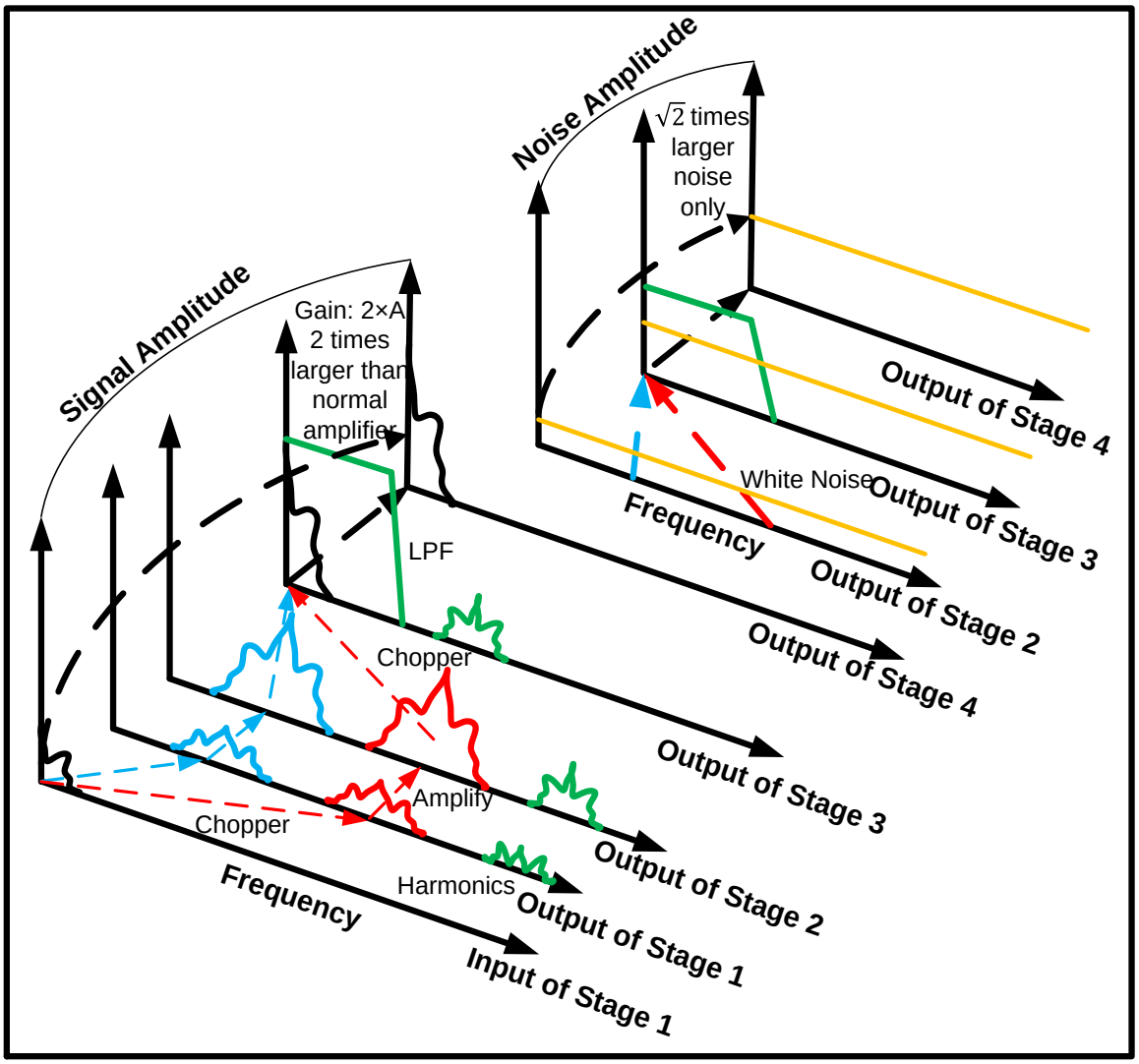


Figure 4.2 Signal and noise flow for each amplifier stage (2-stack version)

4.2 Proposed Multiple Chopper Scheme

Figure 4.1 shows the concept of the multi-chopper technique. First consider a typical chopper amplifier with a single chopping frequency, in which the signal is modulated into a higher center frequency to avoid amplifying 1/f noise. After amplification, a second chopper demodulates the signal back into the baseband. In this case the noise added to the signal is the amplifier noise around the chopper frequency bandwidth.

In the multi-chopper scheme, multiple chopper switches are used along with a multiple-input / multiple-output current-reuse core amplifier. The target of the chopper here is both 1/f noise and white Gaussian noise. The amplifier operates as follows: 1) The input signal is modulated up into N different center frequencies by the different chopper switches (N=2 in Figure 4.1 for clarity); 2) In the amplifying process, the signal is amplified by A for each of the N center frequencies. The output signal consists of the signal, which is A times larger than the input signal, plus the added amplifier noise at each center frequency; 3) Each chopper demodulates the amplified signal and added noise back into the baseband frequency; 4) A summing amplifier combines all N signals producing an output signal that is N×A times larger than the input. However, as explained shortly, the summed noise sources are uncorrelated and therefore sums only as $\sqrt{N}$, providing the key benefit of the approach. Since the clock of the chopper is a square wave rather than a sine wave the center frequencies are selected to be even multiples, thus avoiding coinciding harmonics. Figure 4.2 shows the signal flow of the amplifier.

To quantify the benefits of the proposed scheme, the SNR improvement is calculated assuming a flat gain A throughout the entire amplifying bandwidth: 1) for N different chopper frequencies, the final output signal is N×A times larger. 2) Since the noise is uncorrelated in each chopper frequency domain, the summing amplifier sums the power rather than voltage amplitude. Hence, the power of the noise will be N times larger while the noise amplitude increases by only $\sqrt{N}$. 3) Since the gain of the signal is N×A while the gain in noise is $\sqrt{N}$, the proposed scheme improves SNR by $\sqrt{N}$. The choice of the number of chopper switches represents a trade-off between signal bandwidth (since the signal bandwidth f will be reduced by $\frac{1}{2^N+1}\times$ and Gaussian noise.

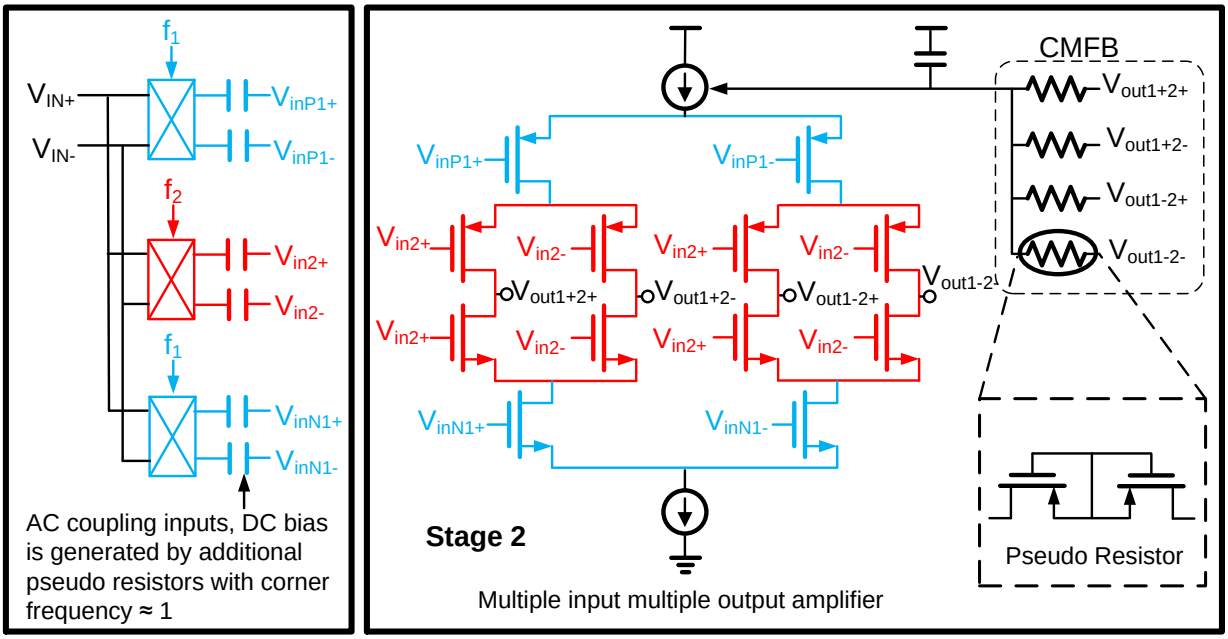


Figure 4.3 Schematic of stage 1 (left) and stage 2 (right) of the amplifier (2-stack version)

4.3 Implementation of Proposed Multiple Chopper Amplifier

Figure 4.3 shows the detailed implementation of the technique, focusing on a 2 chopper frequency version of the amplifier (N=2). The input signal is modulated up by a standard chopper switch and fed into corresponding input pairs of the multiple-input, multiple-output current-reuse core amplifier. AC coupling is used to achieve high CMRR. Figure 4.3 also includes the schematic of the stacked differential pairs, which is similar to [40]. In this work, however, we implement the differential pairs in both NMOS and PMOS (rather than just PMOS [41]) to further reduce the noise introduced by the current reuse scheme; With both NMOS and PMOS inputs, the design operates similarly to an inverter-based technique [41], further improving NEF by$\sqrt{2}$. To avoid the low PSRRs commonly found in inverter-based amplifiers, power and ground are isolated by a current source as shown in Figure 4.3. The design also uses a simple common mode feedback scheme to balance the current mirror at PMOS and NMOS side.

Figure 4.4 gives the small signal analysis of the amplifier. The top differential pairs operate as the traditional pairs. The output current of the topmost differential pair flows into the next pair, equally distributed to the positive and negative paths. A similar current is generated by the NMOS side and passes through the output resistor Rout to generate the output voltage. Note that the input signal at each pairs must be in different frequency domains or the signals will cancel each other, rendering the approach invalid.

Note that this scheme using N=2 yields 4 (or generally 2N) output signals. By connecting the outputs with the correct polarity, as shown in Figure 4.5, the output signals at the desired bandwidths can be collected, demodulated, and summed through the following summing

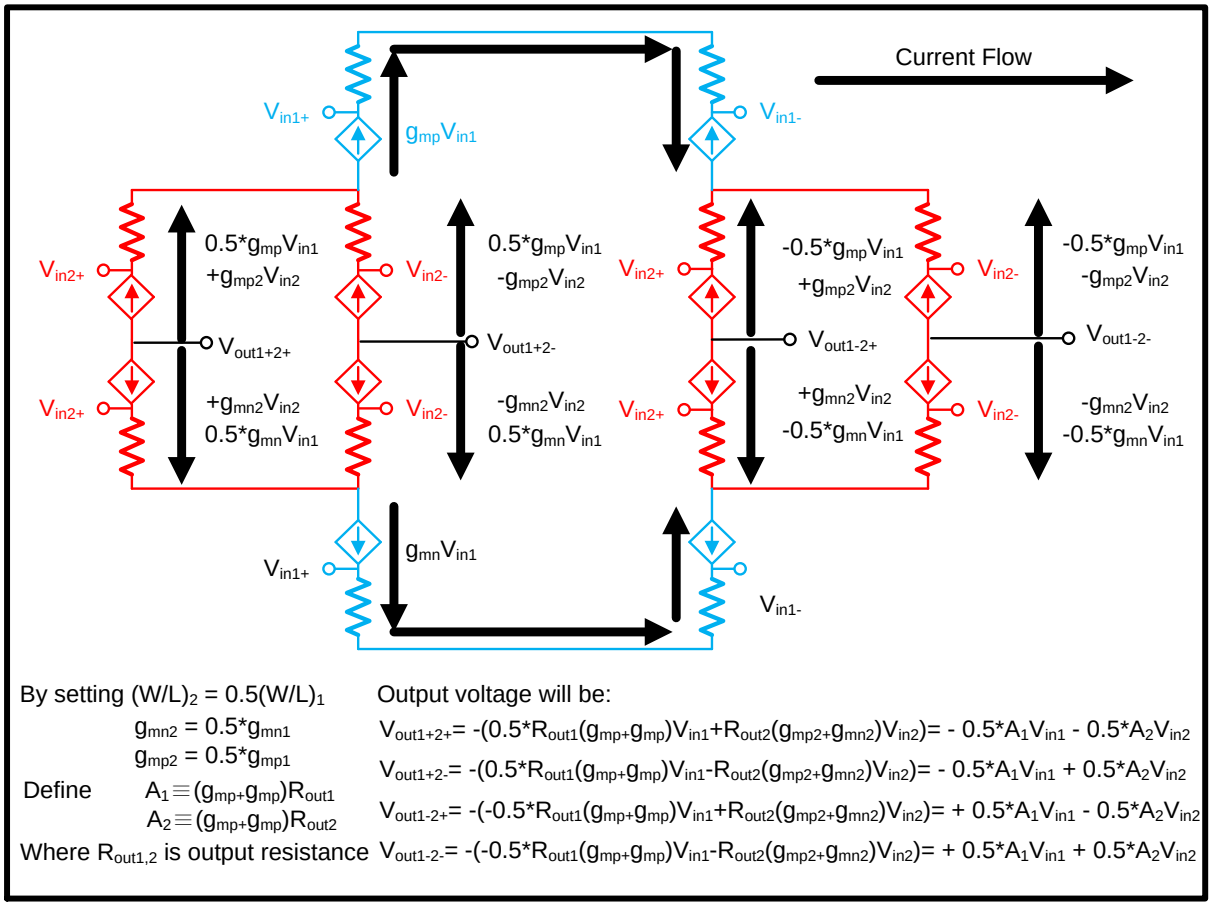


Figure 4.4 Small signal analysis of the amplifier (2-stack version)

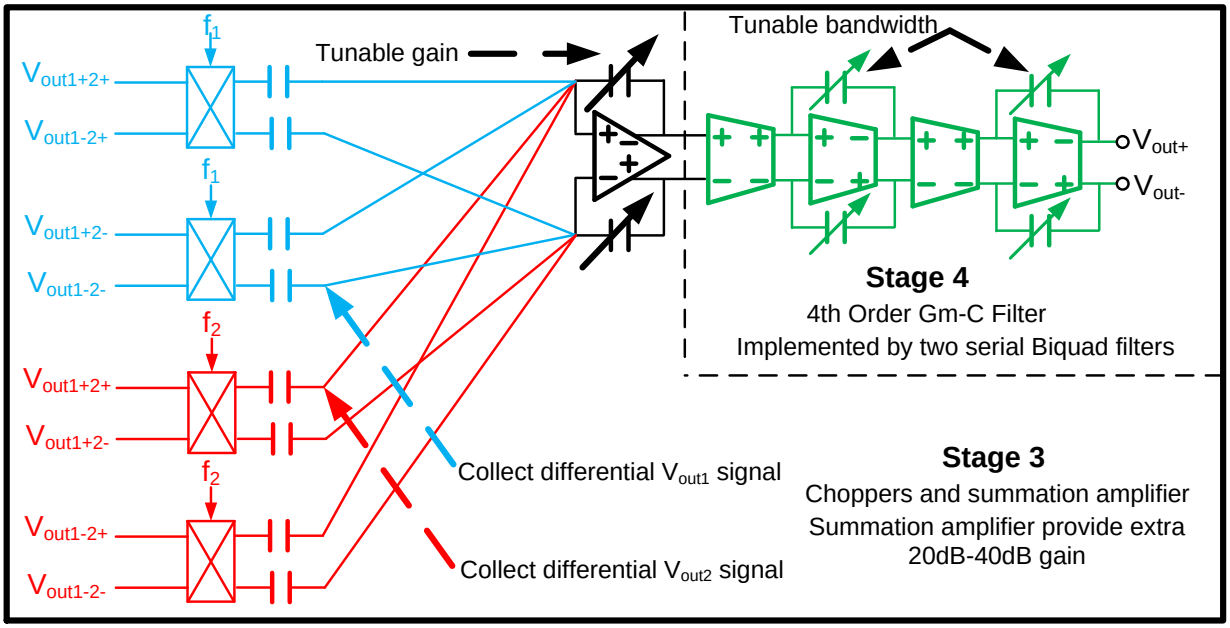


Figure 4.5 Schematic of stage 3 and stage 4 of the amplifier (2-stack version)

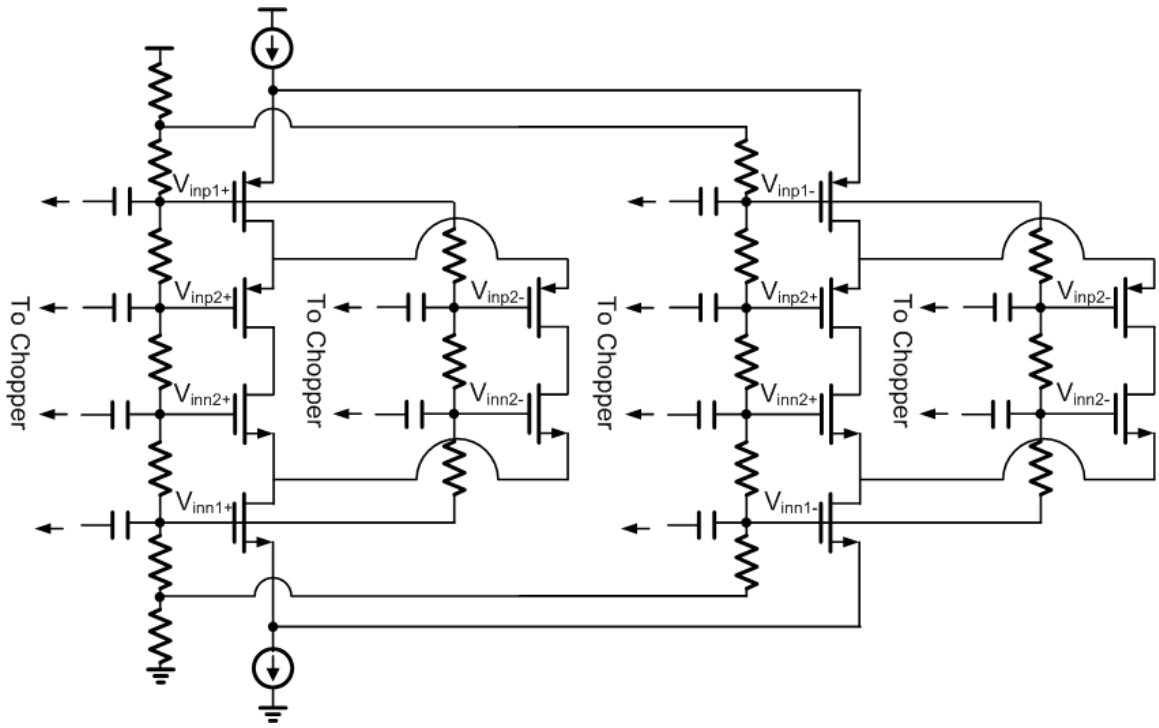


Figure 4.6 Bias of the design (2-Stack Version) Noted that all resistor are made by pseudo resistor

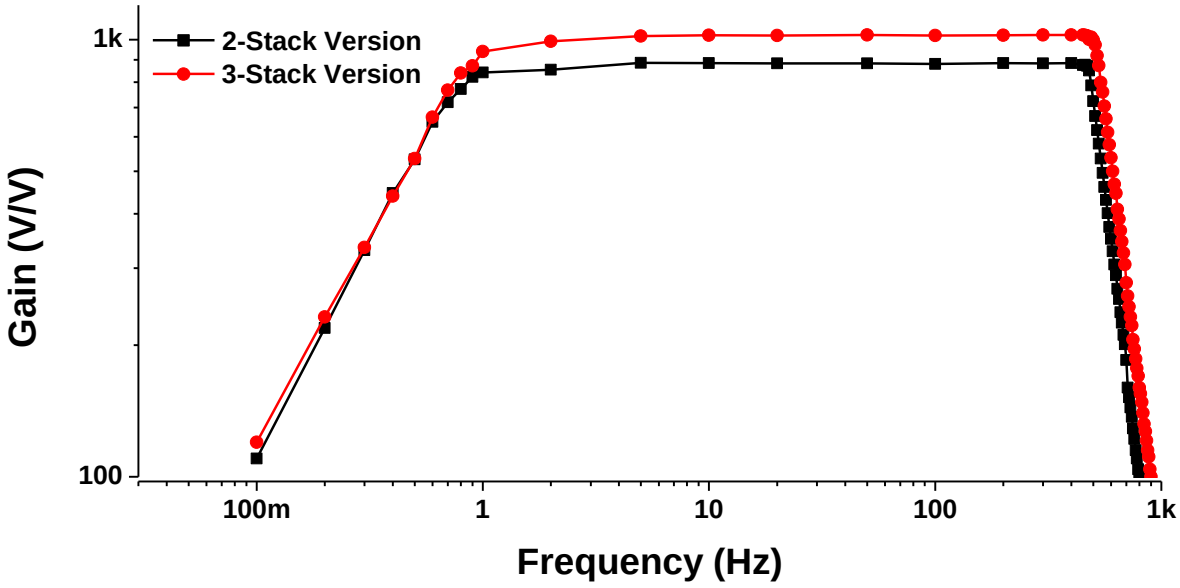


Figure 4.7 Measured gain across frequency range with 500Hz bandwidth

amplifier. All transistors are biased in the subthreshold region (V_{th}=300mV with <150mV V_{gs}) to maximize current efficiency. As in other chopper amplifiers, the output signal contains ripple at both the capacitors inside the summing amplifier and the G_m-C filter can be tuned to retarget the amplifier to other applications. This allows the appropriate signal bandwidth and the chopper signal itself. This is removed with a 4th-order filter after the summing amplifier using two biquad G_m-C filters connected in series (Figure 4.5).gain to be selected to match system requirements. Higher gain and lower bandwidth can be selected for EEG measurements while ECG will employ lower gain and higher bandwidth.

4.3 Implementation of the Bias of the Amplifier

All the bias of the input and the common mode feedback is implemented with pseudo resistor as shown in the Figure 4.6. However, since the pseudo resistor model is tend to be inaccurate and the variation is usually larger than expected, a separate die to observe the pseudo resistor value for better design the corner frequency is tapeout and measured. The detail of the measurement results is shown in Appendix B. Noted that since the resistance of the pseudo resistors is extremely high, some tiny current can create huge voltage drop across the pseudo resistors and make huge impact to the circuits. When using the pseudo resistors to generate the DC bias, it is important to be aware of all the leakage source that is not modeled well. Therefore, MOS capacitor is not used in the design and the even leakage of the metal-insulator-metal capacitor (The leakage is about 0.08fA/um^2 at 0.5V) can create a current large enough to pull the bias to be 100mV off the design point and need to be aware of.

4.4 Summary

To verify the efficacy of the proposed technique, 2-stack (N=2) and 3-stack (N=3) versions are implemented in 180nm standard CMOS. The 3-stack version is identical to the 2-stack version but includes one additional stack in the differential pair and sums 8 output signals.

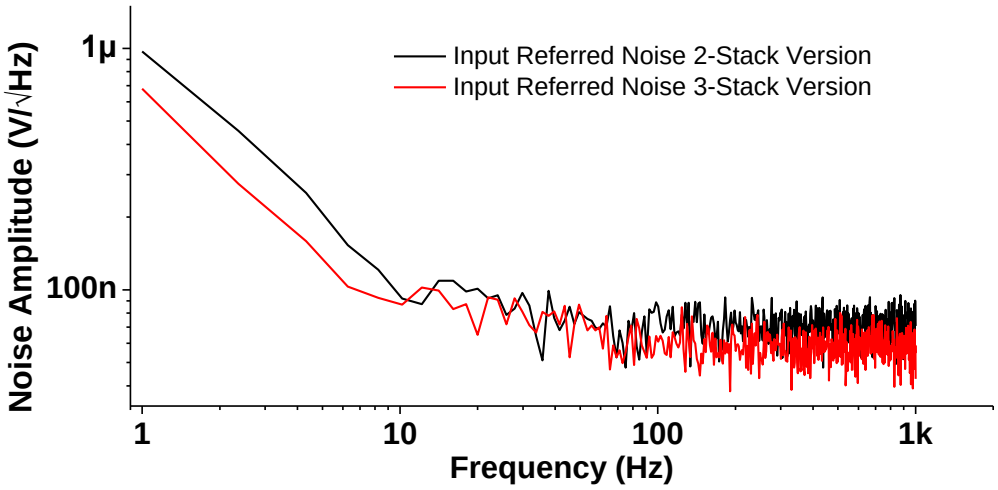


Figure 4.8 Measured noise across 1Hz - 1kHz

Table 4.1 Summary table of the proposed amplifier and previous works

	2 Frequency	3 Frequency	[38]	[39]	[40]	[41]
Process	180nm	180nm	180nm	65nm	130nm	500nm
Power	**273nA@1V**	**266nA@1V**	0.73uW	1.8uA@1V	3.9µW	805nA@1V
Noise	1.91µV (1-500Hz)	1.54µV (1-500Hz)	3.2uV	1uV	3.7uV	3.6µV (0.3-4.7kHz)
Gain(dB)	38.91-56.53 (Tunable)	41.76-59.15 (Tunable)	52	40	40	36.1
Bandwidth(Hz)	407.1-815.5 (Tunable)	402.9-804.3 (Tunable)	10k	100	19.9k	4.7k
NEF	**1.71**	**1.38**	1.57	3.3	1.64	1.80
PSRR(dB)	93 at 60Hz	92 at 60Hz	73	120	80	5.5
CMRR(dB)	87 at 60Hz	89 at 60Hz	N/A	134	78	Single-Ended
THD	0.47% @ 1mVpp	0.54% @ 1mVpp	N/A	N/A	1% @ 16.7mVpp	7.1% @ 1mVpp
Area(mm^2)	0.15	0.25	N/A	0.1	0.125	0.046

Figure 4.7 shows gain and bandwidth for the 2-stack and 3-stack amplifiers. Figure 4.8 shows their noise spectrum. The measured root mean square noise is 1.73µV and 1.45µV for the 2-stack

and 3-stack versions, respectively, at a current consumption of 273nA and 266nA. From measurement results, the amplifier NEF is 1.71 and 1.38 with PSRR/CMRR of 93/87dB and 92/89dB for N=2 and N=3, respectively. Table 4.1 compares the amplifier performance to other designs. Figure 4.8 shows the test chip die photo.

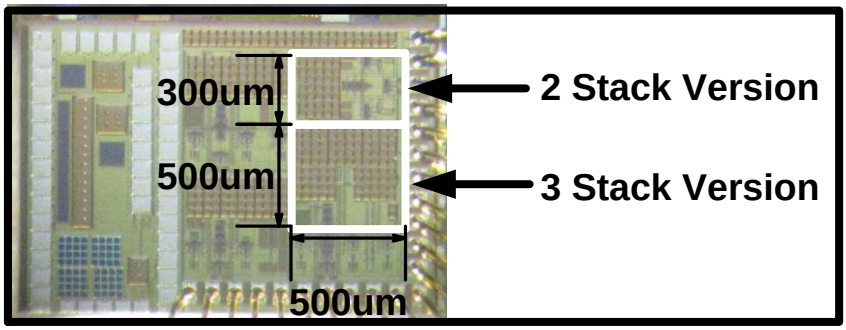


Figure 4.9 Die photo in 180nm CMOS

CHAPTER 5

An Injectable 64nW ECG Mixed-Signal SoC in 65nm for Arrhythmia Monitoring

Electrocardiography (ECG) is the record of electrical activity in the heart and serves as a critical source of information for the diagnosis and study of many heart disorders. Arrhythmia is one of the most prevalent heart diseases; and in particular, according to a 2010 National Institutes of Health report [42] 2.7 million people suffers from atrial fibrillation (AF), which is the most common type of arrhythmia, and the number of people impacted continues to increase over time [42].

In ECG waveform with AF, normal-shaped peaks (dubbed QRS complexes) corresponding to the ventricles are seen, but with an irregular rhythm, but the peaks corresponding to the atrial activity (dubbed P waves) are either abnormal in shape and/or size, appear at fast irregular rates and/or non-discrete. Therefore, by monitoring the rate and shape irregularities on the ECG, AF can be detected. However, arrhythmia can occur very rarely (e.g., only a few times a day) with each event lasting only for a handful of seconds. Consequently, in arrhythmia studies and treatment, long-term but fast observation is essential to assess the abnormality and its severity [43].

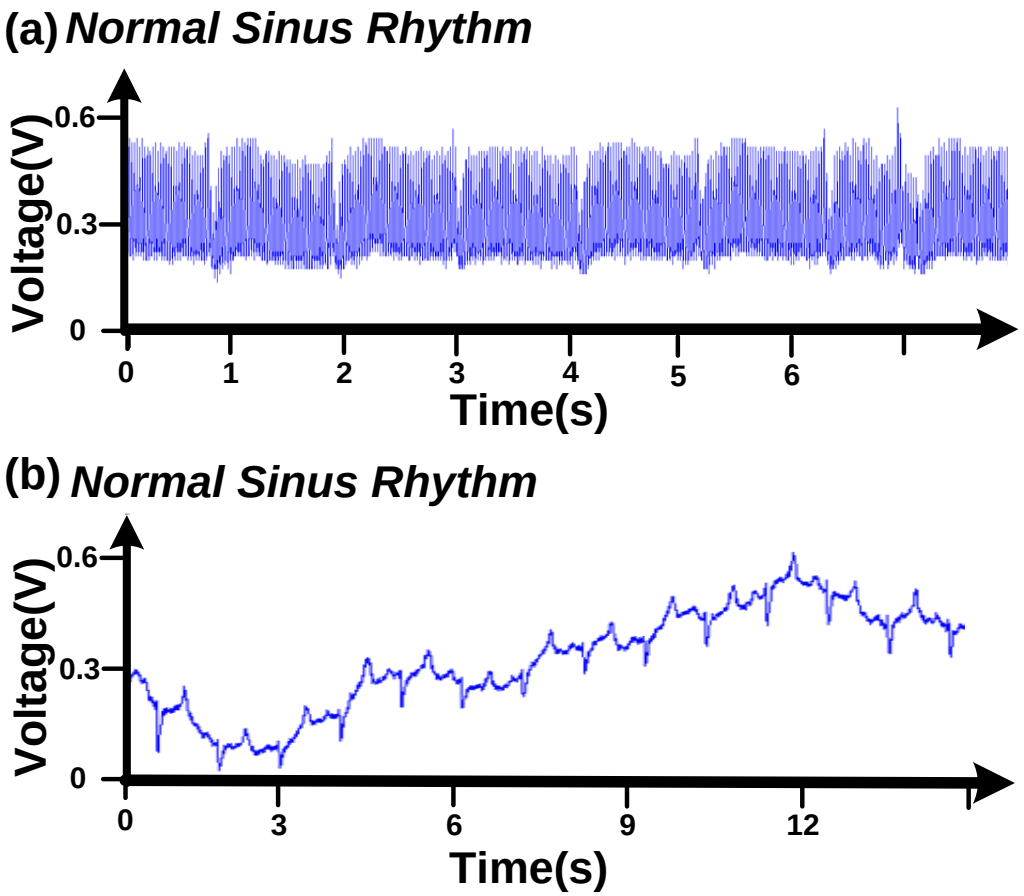


Figure 5.1 (a) ECG waveform showing 60Hz interfering noise as recorded by proposed system. (b) Sheep ECG waveform suffers from low frequency drift (measured by proposed system). Note that the gain is reduced by 10× in this measurement

To enable ECG monitoring, body-wearable systems are a widely-used solution for long term observation. Two or more of patches are attached to the skin and connected to a body-wearable device for continuously monitoring the ECG and storing the waveform on demand. However, there are some challenges in arrhythmia monitoring when using such an approach. First, even small body-wearable systems severely impact a patient's everyday life. Second, physical contact between patches and the skin can suffer from impedance changes due to body

movement, which results in low frequency baseline wander of the output voltage, degrading signal quality and even saturating the amplifier [44-46]. Third, the signals captured using such systems is prone to coupled noise from outside sources such as 60Hz noise from power lines. Example ECG waveforms showing interference from 60Hz noise and exhibiting low frequency wandering are shown in Figure 5.1.

In contrast, implanted systems can be an attractive alternate solution; modern devices have a form factor roughly comparable to a USB flash drive [47]. Since these devices are inserted under the skin, the impact on patient daily life is dramatically reduced once installed. This approach also offers stable physical contact between electrodes and the tissue. The signal strength and quality degradation due to the smaller electrode spacing relative to a surface patch-based recording approaches is compensated by subcutaneous embedding and proximity to the heart, yielding similar signal quality to wearable devices as will be shown later. Moreover, the subcutaneous device is less susceptible to noise sources outside the body. However, the major drawback of implanted systems is the need for expensive and risky surgery. Device lifetime is also critical and is often required to be several years; as a result, a large battery and low power system are needed. To extend lifetime for both body wearable and implantable systems, there has been a significant focus on low power ECG systems, for example in [23, 48-55].

To address this set of challenges, this chapter we proposes a small form factor syringe-injectable ECG recording and analysis device targeted primarily at atrial fibrillation arrhythmia monitoring. The device can be injected under the skin near the heart using a syringe needle to avoid surgery while retaining the benefits of an implantable system.

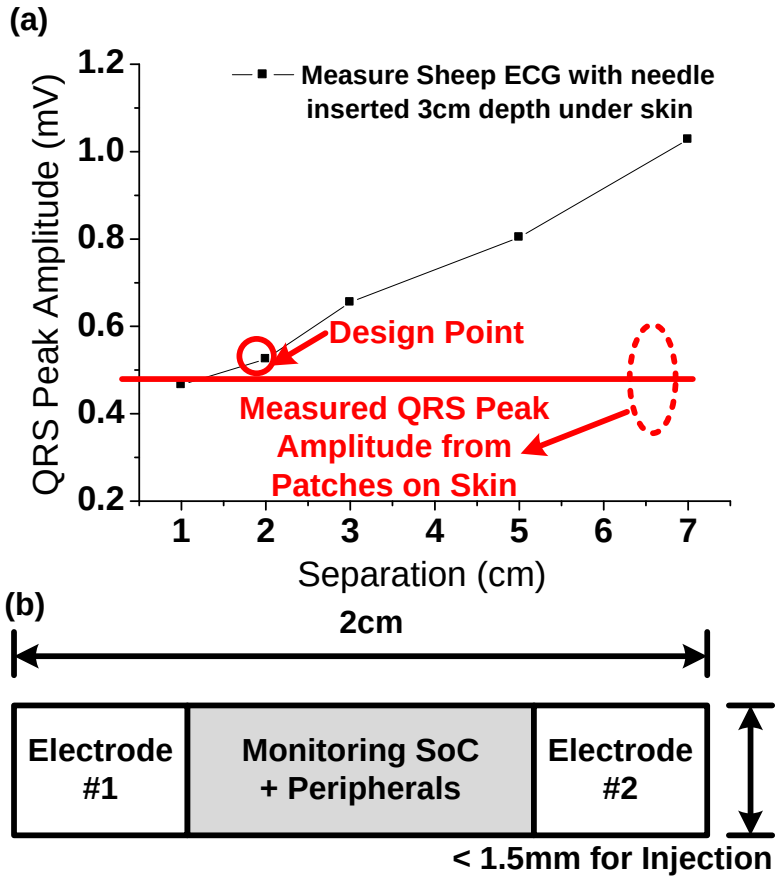


Figure 5.2 (a) Measured QRS peak amplitude versus electrode (use needles as the electrodes directly) separation under the skin in a sheep experiment. Note that with >2cm separation, the amplitude is larger than the traditional approach with two patches attached to neck and wrist. (b) Dimensions of the proposed system

5.1 Overview of the System

5.1.1 Dimension of the System

System size is determined as follows: to achieve a syringe-implantable design, the entire system must pass through the 14-gauge syringe needle during the implantation. Hence, the

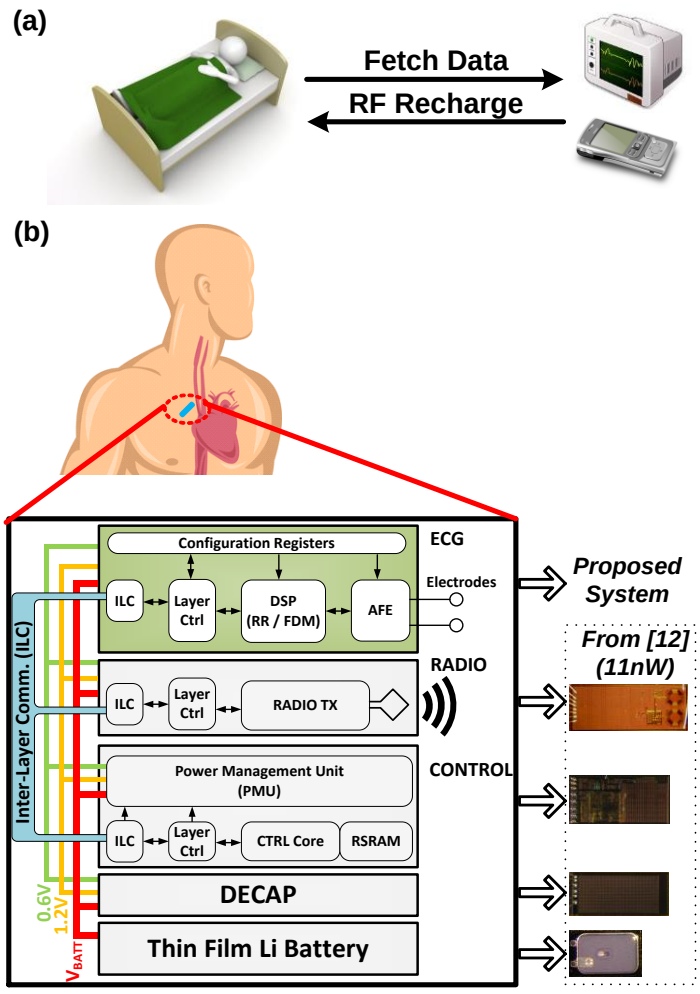


Figure 5.3 (a)Proposed nightly readout and recharge of the system. (b) Other required peripheral

device width is limited to 1.5mm. In contrast, the length is less constrained and the two electrodes attached to either side of the device require 2cm separation (Figure 5.2(a)) in order to provide sufficient separation to yield an acceptably large potential difference. The target dimensions of the proposed system are shown in Figure 5.2(b).

Furthermore, the size constraint also severely limits battery size and hence its capacity. Therefore, in contrast to surgically implanted devices such as pacemakers with large batteries, the proposed device is designed for daily wireless recharging, enabling a much smaller battery.

While the patient sleeps, a host station (depicted in Figure 5.3(a)) near the bed could recharge and retrieve the stored data through a wireless channel. The lifetime between recharging is set to be 5 days to provide a safety margin. Matching battery size to device size allows for a 5uA*hr, 3.7mm2 Li battery, which constrains system power consumption to be less than 167nW. This represents a challenging power constraint given that comparable systems in the literature typically consume 1~30μW [23, 48-54].

5.1.2 System Overview

The proposed ECG monitoring SoC is 1.4mm wide and consumes 64nW while continuously monitoring for arrhythmia. The ability of the system is focus on low power consumption and arrhythmia monitoring depends in part on efficient algorithms. The system consists of analog signal acquisition and digital back end blocks. The signal from electrodes is filtered, amplified, and converted to the digital domain by an analog front end (AFE). A digital signal processing (DSP) module analyzes the waveform within a 10-second search window and detects abnormal cardiac events. Whenever an abnormal event is detected, the device stores the current search window waveform (10× down sampled) into local memory; it can then be transferred to an external device through means such as a wireless transceiver for further analysis by clinicians. It is also compatible with other ultra-low power sensor node peripherals as shown in Figure 5.3(b) [12].

5.2 Implementation of the AFE

Figure 5.4 shows the AFE top level block diagram. The AFE consists of three blocks: a low noise instrumentation amplifier (LNA), a variable gain amplifier (VGA), and a successive approximation register analog-to-digital converter (SAR ADC). To reduce power consumption,

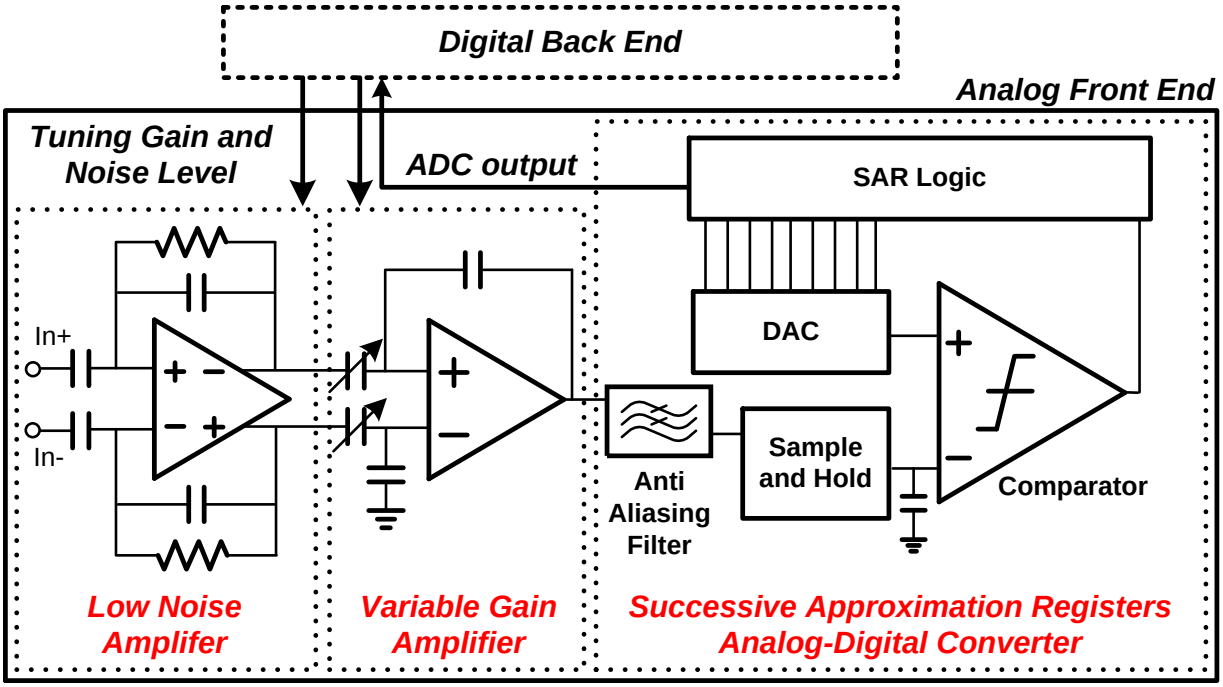


Figure 5.4 Top level diagram of the analog front end.

the AFE supply voltage is 0.6V and all building blocks except the ADCs clocked comparator are biased in the subthreshold regime for low power and high current efficiency. Note that the low supply voltage may incur non-linearity in the final output signal, especially in the amplifier stage. However, based on simulation results final arrhythmia detection is unaffected with <3.5% (THD) nonlinearity. Therefore, the nonlinearity design target is set to 3% for the AFE to best balance system performance and power consumption.

5.2.1 Noise Specification

Similar to other noise-limited amplifier designs [38], the total power consumption of the analog front end is dominated by the first stage of the LNA. Typical ECG designs usually target extremely low input referred noise level (around 3 μV [56-57]; see red dashed line in Figure

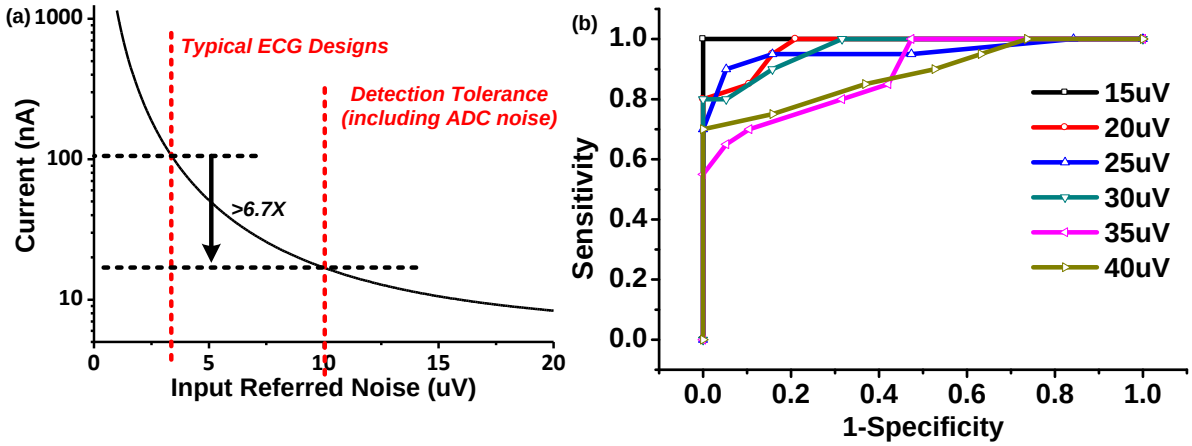


Figure 5.5 (a) The trade-off between amplifier current consumption and input referred noise assumed constant (NEF). (b) The error rate across different noise levels with sweeping threshold. In this plot the X-axis is true negative rate and the Y-axis is true positive rate. The line pass through (X,Y) = (0,1) shown in the 15μV case imply that there is a threshold existed without any error in detection. Other line without passing (X,Y) = (0,1) imply there is at least one false alarm when all the a-fib arrhythmia is detected for any possible threshold

5.5(a)) for best signal quality. However, due to the direct relationship between current consumption and input referred noise, this leads to currents of larger than 100nA assuming a noise efficiency factor (NEF) of 3 and 500Hz bandwidth. In order to reduce total power, we optimize amplifier performance by observing its impact on the final proposed arrhythmia detection accuracy. The effect of noise levels on the accuracy of binary classification between atrial fibrillation and normal sinus rhythm was assessed by applying our atrial fibrillation detection algorithms [58] (see Figure 5.14 and Section 5.3.2 below) on the collected ECG waveforms with artificial additive white Gaussian noise(AWGN) at various levels(from 0 to 40μV). The collected ECG waveforms were collected from 40 un-discriminated patients that

were referred to the University of Michigan hospital for diagnosis and treatment of atrial fibrillation and the noise levels added was designed to surpass the typical ECG noise level (ECGs were recorded during an EP procedure under supine and sedation condition by an EP-Med System (St. Jude Medical, St. Paul, Minn.)). Figure 5.5(a) shows that with a relaxed noise constraint, AFE power consumption reduces significantly, but the Receiver Operating Characteristics curves in Figure 5.5(b) demonstrate that the detection accuracy drops as well. Nevertheless, the proposed system and detection algorithm suffers no performance degradation (100% sensitivity and specificity) with up to 15 μV input referred noise. As a result the design is targeted to 15μV input referred noise to minimize power consumption while maintaining high atrial fibrillation detection accuracy. In the final design, the amplifier specification is tightened to 10μV input referred noise across process corners to allow for a 10μV ADC noise budget. This optimization reduces AFE power by 6.7× from 132nW to 17nW and system power by 2.45× from 177nW to 72nW, compared to typical ECG signal acquisition designs that require noise levels of ≤ 3μV. Due to the resulting high performance variability and the possibility of the environmental and process changes, the amplifier gain, bandwidth, and input referred noise can be adjusted by the digital blocks to maximize the useful signal range.

5.2.2 Amplifier Implementation

As shown in the AFE top level diagram, two amplifiers are used in series to provide low noise and high gain. The first amplifier focuses on low noise while the second amplifier enables tunable gain. Due to the large tissue-electrode impedance (measured to vary from 1MΩ to 5MΩacross different instances of the same model of electrodes, with ~4 MΩ average) the input amplifier requires very high input impedance. In addition, the signal is located in the flicker

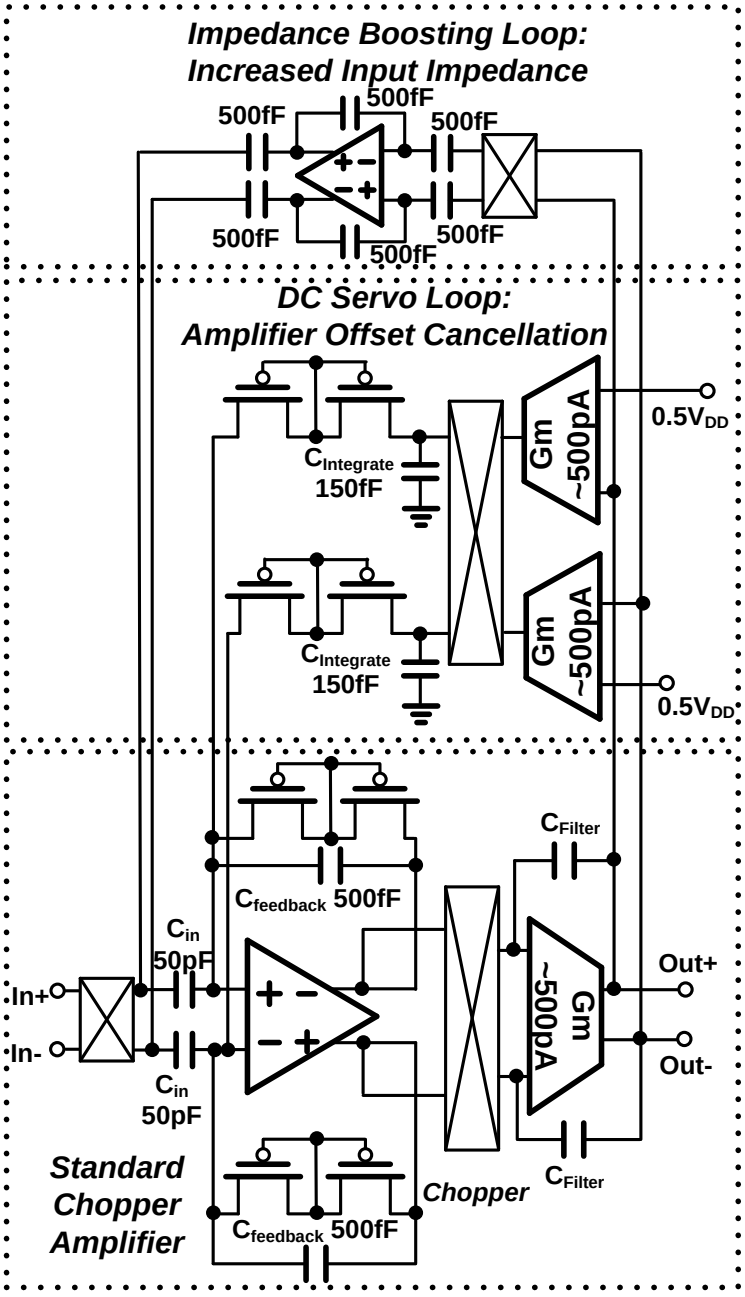


Figure 5.6 The first stage of the low noise amplifier, including all building blocks: chopper, DC servo loop, and impedance boosting loop

noise bandwidth and requires chopper stabilization [59]. Therefore, a capacitive feedback chopper-stabilized instrumental amplifier (CCIA) topology is employed for the first-stage

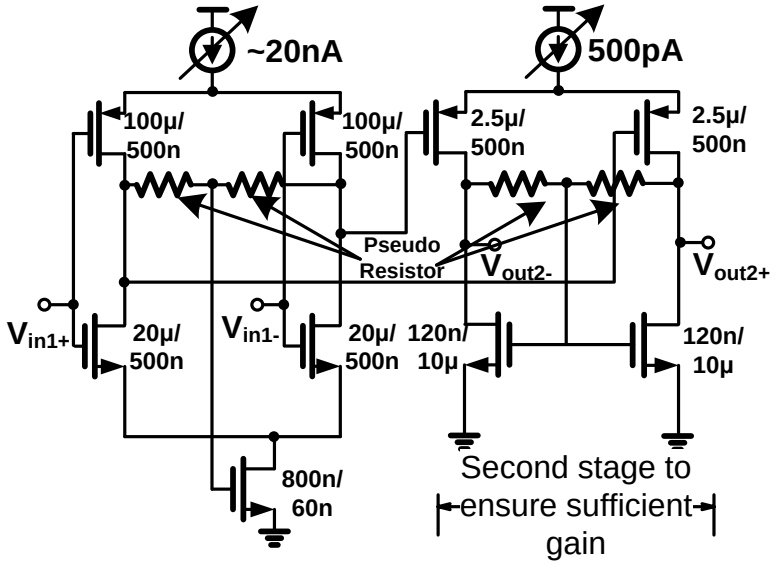


Figure 5.7 Core amplifier insides the CCIA

amplifier to ensure high input impedance and low noise. The design targets of the CMRR and PSRR are set to be higher than 80dB as the standard requirement of the ECG amplifier [56-57]. The target input impedance is set to be larger than 10MΩ to have enough signal amplitude similar to [39]. The target gain is set to be 72dB and design to be tunable to provide enough gain to amplify the 1mV peak to peak signal to rail to rail output and tunable dynamic range. The amplifier also target at handling the DC offset up of the electrodes to 300mV as required standard [57] by capacitive input. Figure 5.6 provides a diagram of the CCIA. The capacitive feedback provides fixed 40dB gain and parallel resistive feedback generates the high pass corner to filter out DC offset and low frequency drift of the signals. To generate a <0.5Hz ultra-low high pass corner with reasonable chip area, a pseudo-resistor is employed.

To further boost input impedance, a positive feedback impedance boosting loop (IBL) similar to [39] is implemented. The IBL generates a current similar to the input current to the core amplifier and feeds it back to the input to compensate the input current and increase the

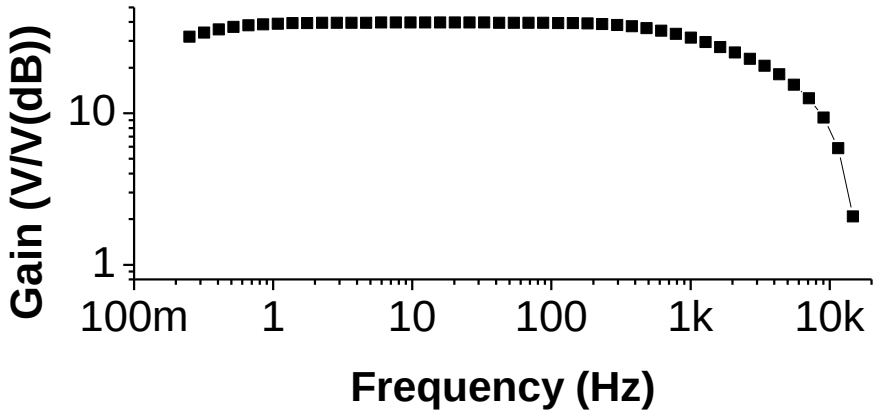


Figure 5.8 Simulated CCIA gain versus frequency (without G_m-C filter)

input impedance. The amplifier shown in the figure in the impedance boosting loop serves is design to avoid unwanted signal feeding through the feedback path. Since the input of the amplifier in the IBL is an amplified signal, this amplifier is not noise limited. Therefore, 500pA is allocated with little impact on the overall power budget.

To remove harmonics from the chopper, a G_m-C filter is implemented in the next stage with 250Hz bandwidth. Note that the chopper is inserted in front of C_{in} to reduce the mismatch of C_{in} and improve the CMRR of the amplifier, as in [60].

Figure 5.7 shows the core amplifier of the CCIA. The first stage amplifier uses 20nA current to meet the noise requirement discussed in Section III.A. This current can be tuned by a 4-bit binary code from the digital back end to match the desired noise level (ranging from 3μV to 12μV). To efficiently use the current, an inverter-based amplifier topology, similar to [41-61], is adopted to achieve low NEF. Common mode feedback is provided by both the bottom NMOS and the pseudo resistors (used to implement a <0.1Hz filter), guaranteeing the output common mode stays at half V_{DD}.

Table 5.1 Simulated specifications of the CCIA together with G_m-C filter

Topology	CCIA
V_{DD}	0.6V
Midband Gain	36.92dB
Input Referred Noise	8.4uV (with chopper)
	5.8uV(without chopper)
Input Impedance	> 110 MΩ (with IBL)
	> 10 MΩ (without IBL)
offset	0.071mV (with DSL)
	1.52mV (without DSL)
Low 3dB	0.117Hz
High 3dB	547.7Hz
NEF	2.258
PSRR	>80dB for < 500Hz
CMRR	>80dB for < 500Hz
THD	2.24%

From simulation, the first stage amplifier gain is 32dB, which is not sufficient to provide the overall 40dB gain target through the feedback network. Therefore, a second amplifier stage is required within the core amplifier. Since the subsequent amplifier receives an amplified signal, the noise constraint is significantly relaxed; this stage consumes only 500pA and allows the CCIA to achieve 61dB gain overall. Simulation results of the CCIA overall gain are shown in Figure 5.8.

A common issue with inverter-based amplifier design is vulnerability of the bias point to PVT variations. Therefore, a DC servo loop (DSL), similar to [39], is adopted to stabilize the differential output and reduce offset by fixing the DC output to half VDD. From simulation results, the DSL reduces DC offset from 1.52mV to 0.071mV.

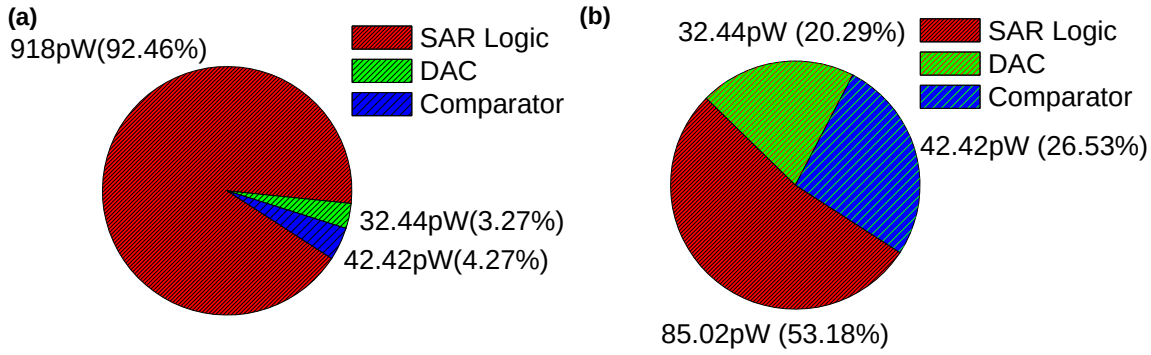


Figure 5.9 (a) SAR ADC power breakdown with ADC logic implemented using HVT standard cells. Note that SAR logic consumes 92% of total power when operating at 500Hz. (b) SAR ADC power breakdown with custom asynchronous logic

Table 5.1 summarizes the performance of the simulated CCIA. The midband gain is 39dB with 250Hz bandwidth (limited by the G_m-C filter for the choppers). Through the use of chopping, the impedance boosting loop, and the DSL, all ECG amplifier requirements are met.

5.2.3 ECG SAR ADC Overview

The system's analog to digital conversion is performed by an 8-bit single-ended asynchronous SAR ADC with 500Hz sampling rate. To avoid alias from other frequency band, a 250Hz anti-aliasing G_m-C filter is built with a 500pA amplifier in front of the ADC.

Although SAR ADC consumes less power compared to amplifier in the ECG system, the long term goal of the mm3 system [12] is to build a platform for all the available sensors. Therefore, the minimizations of the power consumption are conducted at each building part separately including the ADC. Power consumptions of the SAR ADCs are well studied in recent years. However, most prior work focuses on high sampling rates that far exceed the requirements of this ECG system.

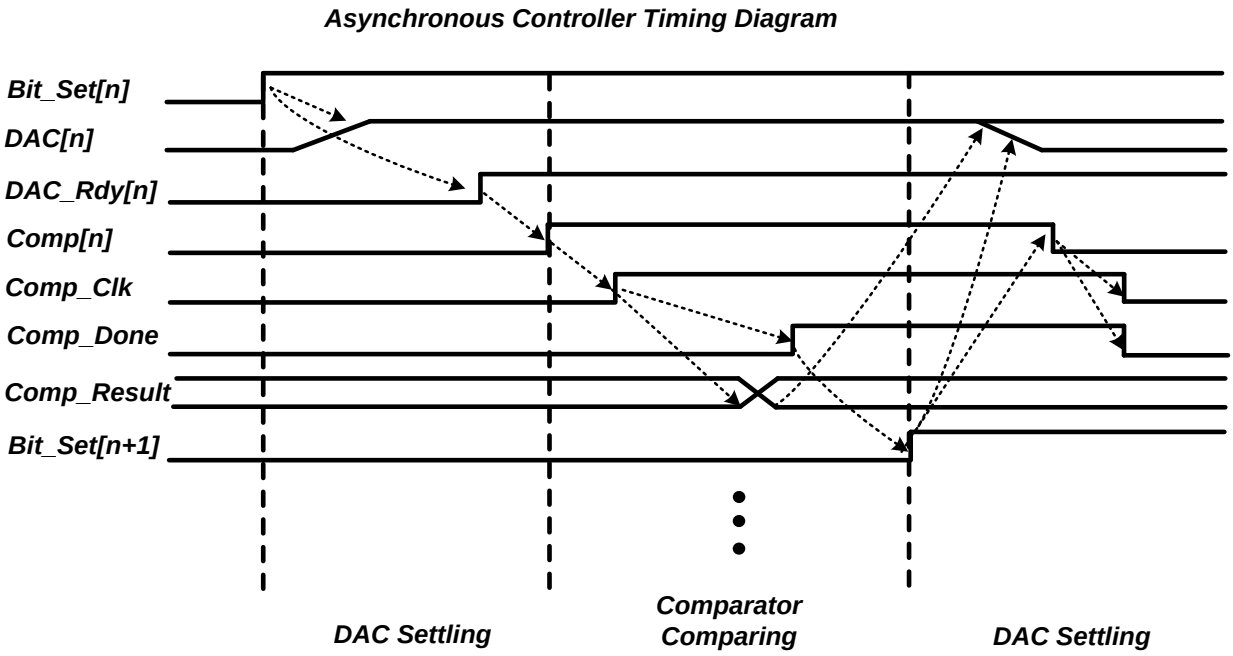


Figure 5.10 Detailed signal flow diagram of the asynchronous controller inside the SAR ADC

Among those SAR ADCs that operate in the kHz range and offer nW-level power consumption [62-64], it is found that approximately 50% of total energy consumption comes from digital logic due to leakage and long cycle times. This is in contrast to most SAR ADCs which operate at much higher sample rate and hence have power dominated by DAC switching. The importance of digital logic in this application will be heightened due to the sub-kHz sampling rates; simulated power consumption of a standard 8b 500S/s SAR ADC is shown in Figure 5.9(a). Here standard cells are used for the digital logic and leakage is the main source of power consumption in the digital block.

5.2.4 Implementation of SAR Control Logic

To reduce digital power consumption, a novel asynchronous logic is proposed to reduce transistor count and hence the leakage power of SAR logic. Conventional asynchronous logic is

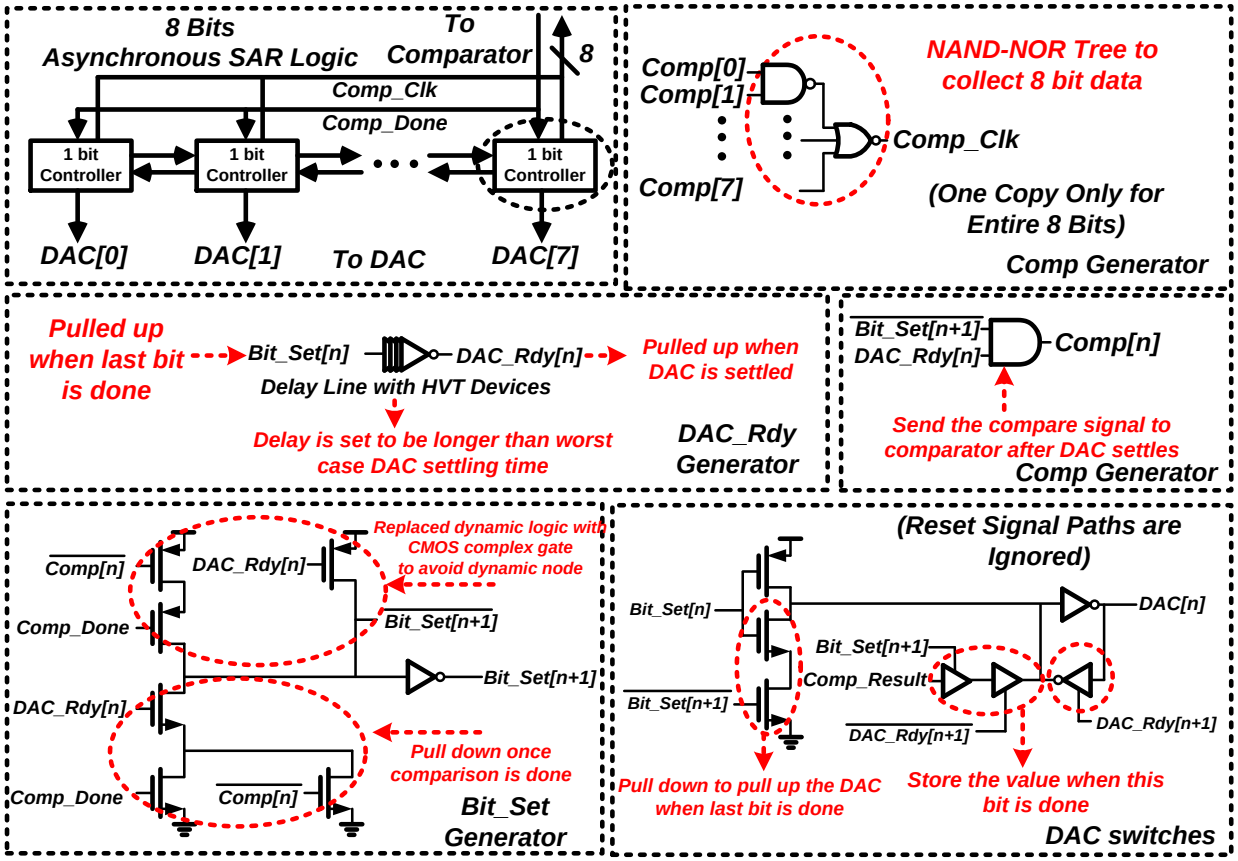


Figure 5.11 Detailed diagram of asynchronus logic in the SAR ADC. Note that some of the reset

typically implemented with dynamic logic to achieve peak energy efficiency [65]. However, dynamic logic is not well suited to low frequency applications due to leakage. Therefore, in this work, all dynamic nodes are implemented with latches clocked by internal signals and delay lines.

Figure 5.10 shows the detailed signal flow of a one-bit controller as an example. There are four internal signals: 1) the "bit_set" signal implies the operation of the previous bit is done; path and the double stacked transistors (to reduce leakage) are not shown2) the "DAC" signal is connected to the DAC and toggles the DAC directly; 3) the "DAC_rdy" signal is triggered after the DAC is settled and ready for comparison; 4) the "comp" signal requests a compare event in the comparator.

Once the result of the last bit comparison is done, the “bit_set” signal is pulled up by the previous stage. The circuit to pull up the “bit_set” signal is shown at bottom left of Figure 5.11. The “DAC” signal is then set to 1 by the circuit shown in the bottom right of Figure 5.11 (note that the DAC is set to 0 initially and floating nodes are completely avoided through the use of latches). Once the DAC is settled, “DAC_rdy” goes high. Since direct detection of the DAC settling to 8 bit accuracy would consume significant energy, the circuit triggering the “DAC_rdy” signal is implemented with a delay line set to be longer than the expected DAC settling time across all corners. Since a long delay line can also consume high power, I/O HVT devices are used to reduce the number of stages and save power. Once the DAC has settled, the “Comp” signal goes high and sends a comparator clock signal to trigger the comparison. After the comparison result is generated, “comp_result” and “comp_done” are sent by the comparator. The controller saves the result into the DAC and raises the “bit_set” signal for the next stage.

The transistors count of the proposed design is 34 compared to the 48 transistors of the traditional 2 DFF design and 29% of reduction is achieved. To further reduce power all leakage paths are double stacked, reducing subthreshold leakage by 1.92× from 163pW to 85pW. As shown in Figure 5.9(b), the proposed asynchronous logic reduces simulated power consumption to 85pW, marking a 10.79× (from 918pW to 85pW) improvement compared to SAR logic using synthesized standard cells.

5.2.5 Implementation of DAC and Comparator

Considering the impact of mismatch [66] and thermal noise on ADC accuracy, a 10fF DAC unit capacitor and typical split capacitor array topology are chosen. Further, the comparator is a clocked 1-stage design that is chosen for its low dynamic power consumption. However, the combination of first stage clocked comparator and small capacitor array make the comparator

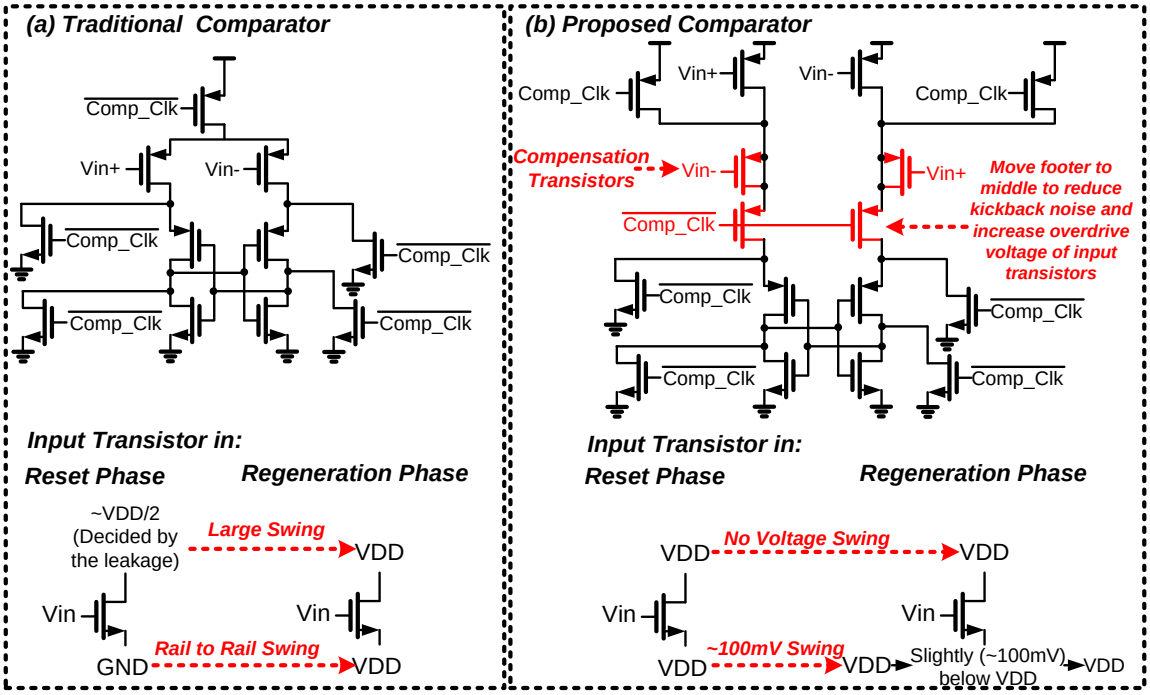


Figure 5.12 (a) Traditional comparator and source of kickback noise. (b) The proposed comparator with suppressed kickback noise sources

input vulnerable to kickback noise. The proposed design uses a split footer comparator [67] combined with cross-coupled compensation to address this issue. Figure 5.12 shows the schematic of the proposed comparator. Noted that the kickback noise mainly stems from the rapidly change drain and source voltages of the input transistor. In the proposed design, these changes are limited to ~100mV and the residual kickback noise is reduced by the compensation transistors. In the simulation results of Figure 5.13, the kickback noise is reduced by 84.9× (from 19.8mV to 0.2mV) in the proposed comparator design. Table 5.2 shows the power breakdown of the complete analog block. Note that ADC power is dominated by the antialiasing filter due to the use of low-power asynchronous logic.

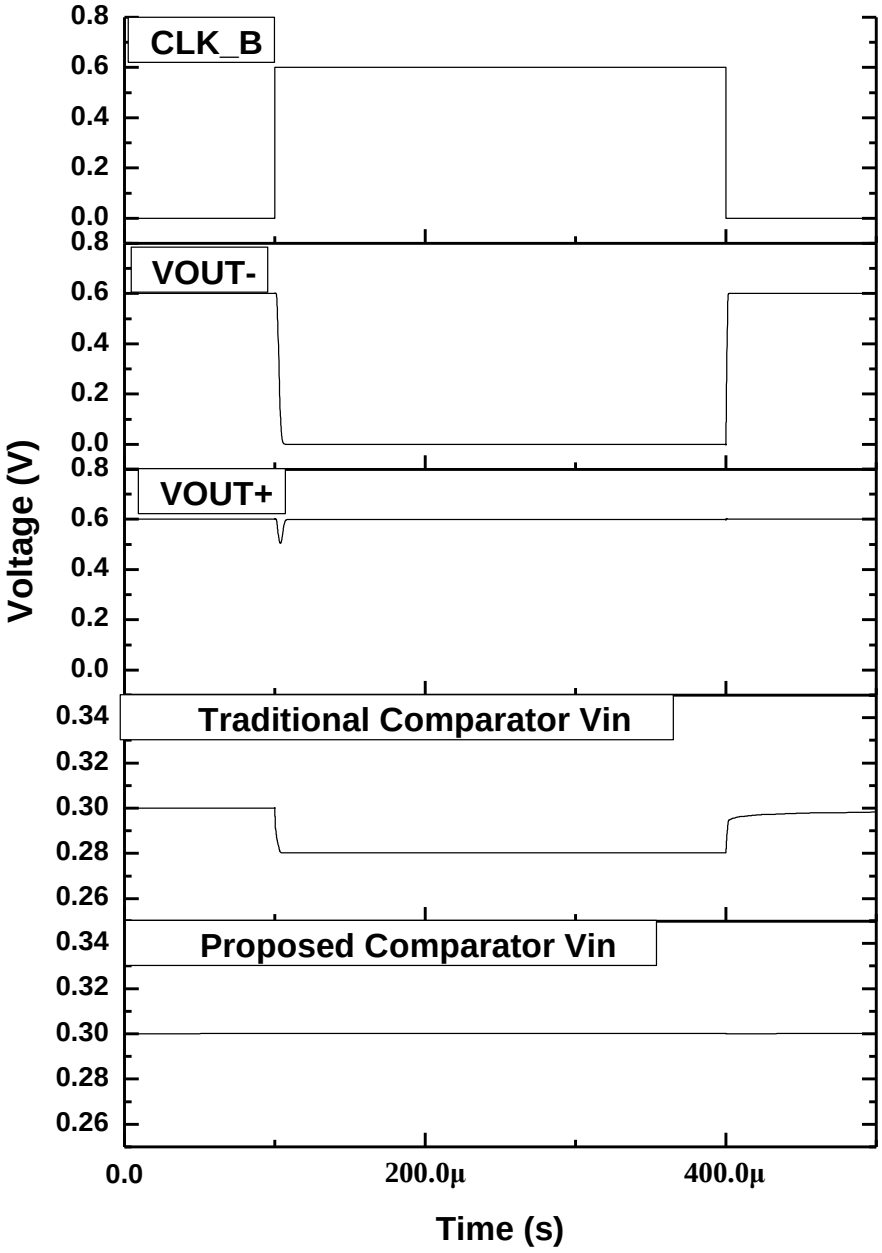


Figure 5.13 Simulated waveforms of kickback noise in the proposed and traditional comparators. Kickback noise in the traditional amplifier is 19.8mV and is reduced to 0.2mV in the proposed design

Table 5.2 Simulated power breakdown of analog front end

LNA		12.5nW
LNA	Core: First Stage	10.9nW
	Core: Second Stage	0.3nW
	Impedance Boosting Loop	0.3nW
	DC Servo Loop	0.6nW
	Gm-C Filter	0.3nW
VGA		3nW
SAR ADC		0.46nW
SAR ADC	Anti-Alias Filter	0.3nW
	SAR Logic	85.02pW
	Comparator	42.42pW
	DAC	32.44pW

5.3 Implementation of the Digital Back End

5.3.1 Overview of the Digital Algorithm

The back-end digital block first detects the incoming signal amplitude and tunes AFE gain accordingly to set the waveform to full range. Arrhythmia detection is performed in a moving 10-sec window, as shown in Figure 5.14(a). Since the irregular session lasts several seconds. There is no overlapping between the windows. If an arrhythmia is detected in a window, the 10× down sampled 10 second waveform is temporarily stored in the memory and an interrupt signal is sent out for further processing.

The first implemented detection algorithm is conventional time domain detection [68]. This approach first detects the largest QRS peaks and then calculates the peak-to-peak time interval. The variance of peak-to-peak intervals is then calculated. As the peaks are generated more irregularly during arrhythmia, we apply a simple thresholding technique to the variance to detect an abnormal activity. As a second approach we perform arrhythmia detection in the

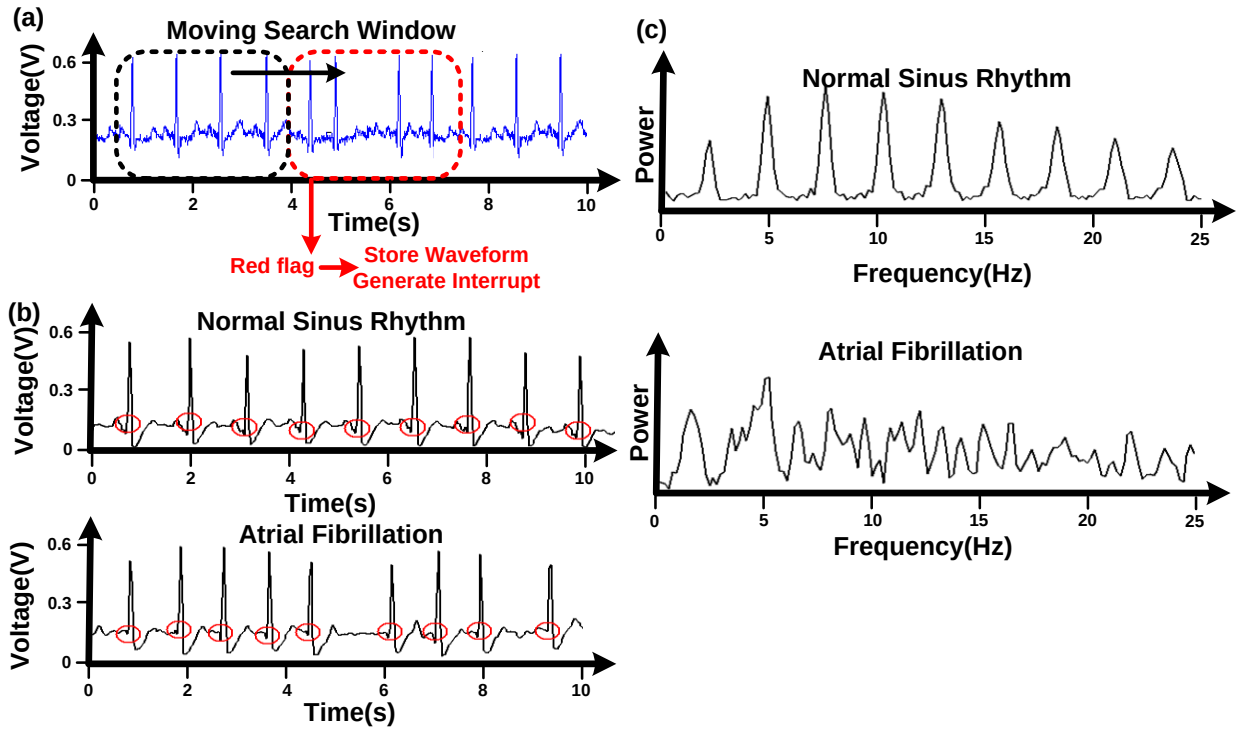


Figure 5.14 (a) Search windows of the proposed algorithm. (b) Example waveform of normal ECG waveform and the arrhythmia ECG waveform (c) Corresponding power spectrum of the ECG waveforms shown in (b). Noted that the block floating point scheme is implemented and the y-axis is showing relative numbers without unit

frequency domain. Under normal conditions, peaks are generated at approximately constant intervals, which translate to a clear dominant frequency and harmonics in the frequency spectrum. However, as shown in Figure 5.14(b), under abnormal rhythm a single dominant frequency is less prominent and the frequency spectrum shows more dispersion. Therefore, under arrhythmia such as atrial fibrillation, peaks have varying intervals in the frequency domain and the arrhythmia can be detected by inspecting the variance of intervals. The stored 50Hz-sampled waveform is sufficient for detection of fast rhythms such as atrial fibrillation in the frequency

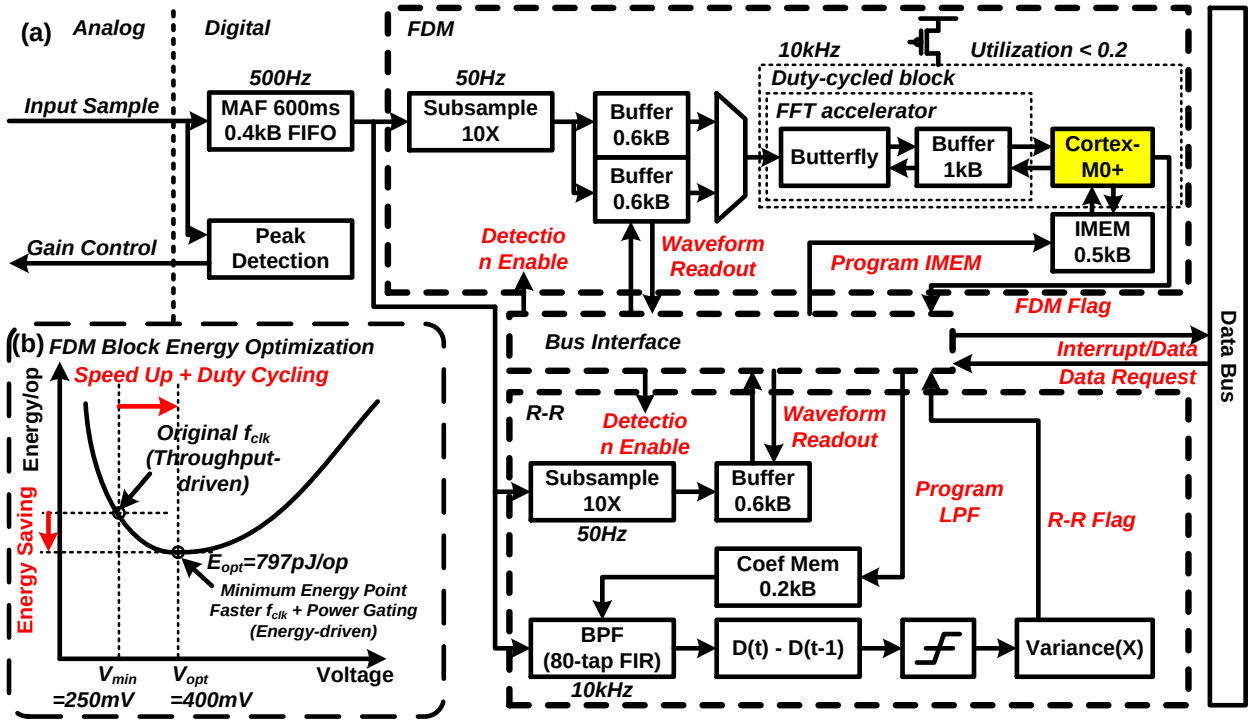


Figure 5.15 (a) Top level of the proposed digital back end. (b) Energy/operation versus voltage shows the minimum energy point of the FDM block

domain, where cardiac activation rate is always <25Hz, but it is not suitable for time domain analysis where precision of <40ms is required, such as in sequential QRS intervals detections. Thus, the stored 50Hz-sampled waveforms may not be suitable for some clinical interpretations.

Figure 5.15(a) is an overview of the digital back end based on the two detection algorithms described earlier. First, input samples taken from the ADC output pass through the moving average filter (MAF) of 600ms to remove slow baseline wandering by subtracting the output of MAF from the original input to obtain filtered result. At the same time, the input codes the input codes from the ADC and are sensed tunes the gain such that the swing is within 75% to 90% of the ADC output range. There are two separate processing paths for the frequency domain and time domain algorithms. In the time domain R-R algorithm, the feature is the distance

between adjacent QRS peaks and it uses the variance of these intervals to detect irregular peaks. The frequency domain FDM algorithm [58] directly looks at the frequency spectrum and checks if there exists clear peaks which represent constant intervals. Further details are given below in section 5.3.3.

5.3.2 Implementation of R-R Detection

The proposed design can also perform standard QRS-peak detection [68] (R-R block), which uses peak-to-peak distances to determine ECG signal regularity. The input signal goes through the bandpass filter based on an 80-tap FIR filter. The signal is then differentiated to obtain the slope. If the signal slope exceeds a threshold a QRS peak is declared. The variance of R-to-R intervals is directly used as a decision value in arrhythmia detection. The bus interface can program the algorithms and retrieve the stored data when an arrhythmia is detected. This data is passed to peripherals on the other chips through the data bus. The implemented design allows for one of the two different algorithms to be run, allowing for power savings by power gating the unselected processing path.

5.3.3 Implementation of the Frequency Dispersion Metric (FDM)

The proposed FDM detects an arrhythmia in the frequency domain. The input is first down-sampled by 10×, and stored in one of two 0.6kB ping-pong buffers. A 512-point real-valued FFT accelerator is implemented with a radix-4 256-point complex-valued FFT shown in Figure 5.16. First, the Blackman-Harris window observing the 3~15Hz frequency range is applied to the signal and then the FFT block will calculates the frequency spectrum and the ARM Cortex-M0+ core performs the actual detection algorithm to observe the existence of the dominant peaks in a specific frequency range, which represents a stable heartbeat. Once an arrhythmia is detected, the ping-pong buffer storing the last search window no longer accepts

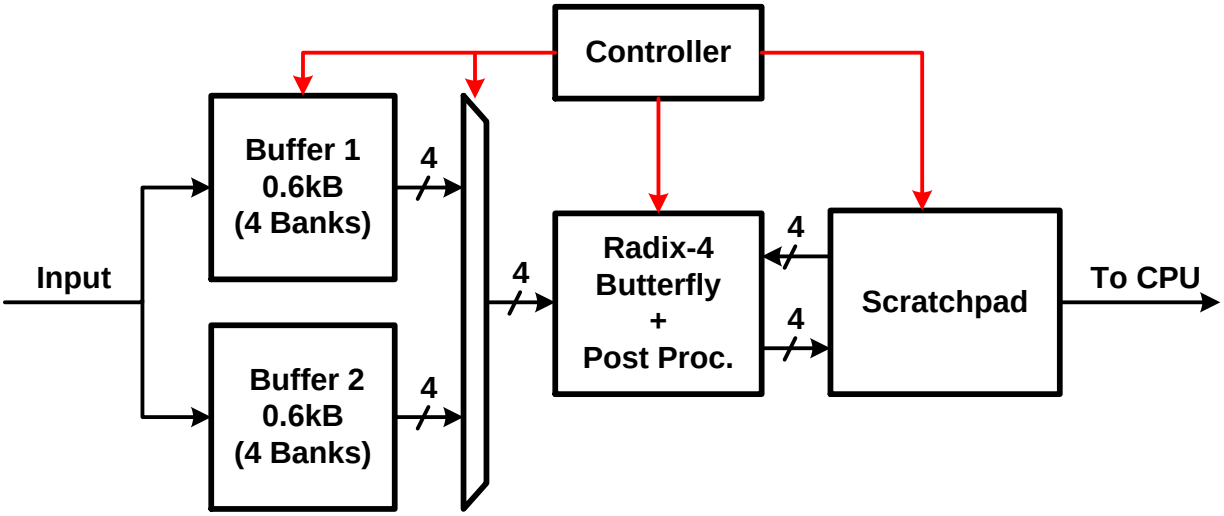


Figure 5.16 Block diagram of FFT, peripheral buffers, and controller

new samples until the waveform is fully read out through a data bus. During this time the other buffer acts as the primary input data channel. Therefore, the ping-pong buffers, along with the local buffer of the FFT, make continuous arrhythmia detection possible while temporarily storing any previous abnormal activity. Note that the ARM core instruction memory can be user-programmed to provide added flexibility such as changes to the peak detection algorithm in the frequency spectrum or the frequency monitoring window. To deal with false alarm of changes in the heart rate due to changing levels of activity, since the irregular peaks from arrhythmia usually generate faster and abrupt changes compared to normal changes from changing levels of activity. The algorithms can distinguish it by choosing right decision values in the threshold stage.

5.3.4 Optimization for Minimum Energy Computation

To further reduce energy consumption of the FDM block a technique called minimum energy computation [69-70] is applied. As the supply voltage is lowered both leakage and dynamic power reduce. However, the system clock is slowed and the leakage energy per cycle increases. Eventually the leakage energy increase overcomes the dynamic energy savings and total energy starts to increase. Therefore, it has been shown that an optimal point exists, i.e., the

minimum point of the plot in Figure 5.15(b). In simulation, Vopt and Vmin are 300mV and 250mV whereas we could achieve the same performance as Vopt in simulation at 400mV in measurement due to discrepancy between simulation and measurement. And the energy per operation is 797pJ/op at Vopt. Arrhythmia detection is done only once in a 10-sec window and each detection takes approximately 500 cycles. Hence, 500Hz input sampling frequency is sufficient to meet performance constraints and is chosen for the proposed system. However, the minimum supply voltage that matches this frequency constraint lies below the energy optimal point and therefore consumes substantial leakage energy due to the corresponding long cycle time. Therefore, we use a faster (10kHz) clock and operate the detection in burst-mode (20× faster than required). After the detection event completes the entire block, including the FFT and M0+ core, is power gated with an NMOS header using a boosted enable signal. Although a higher operating voltage is needed for this faster clock frequency, the leakage energy per computation is greatly reduced and minimum possible energy consumption is achieved.

Compared to the supply voltage corresponding to just-in-time computation, this technique increases supply voltage by 50mV while reducing energy by 40%.

5.4. Measurement Results

5.4.1 Proposed AFE Measured Results

Figure 5.17 (a) is the chip microphotograph of the proposed SoC and the Figure 5.17 (b) shows the chip inside the syringe needle. It is fabricated in 65nm LP CMOS technology. The amplifier achieves 2.64 NEF with 31nA current consumption and 6.52μV input referred root mean square noise. The measured amplifier gain ranges from 51 to 96dB with 250Hz bandwidth. The frequency response of the amplifier is shown in Fig. 18. The amplifier CMRR and PSRR are

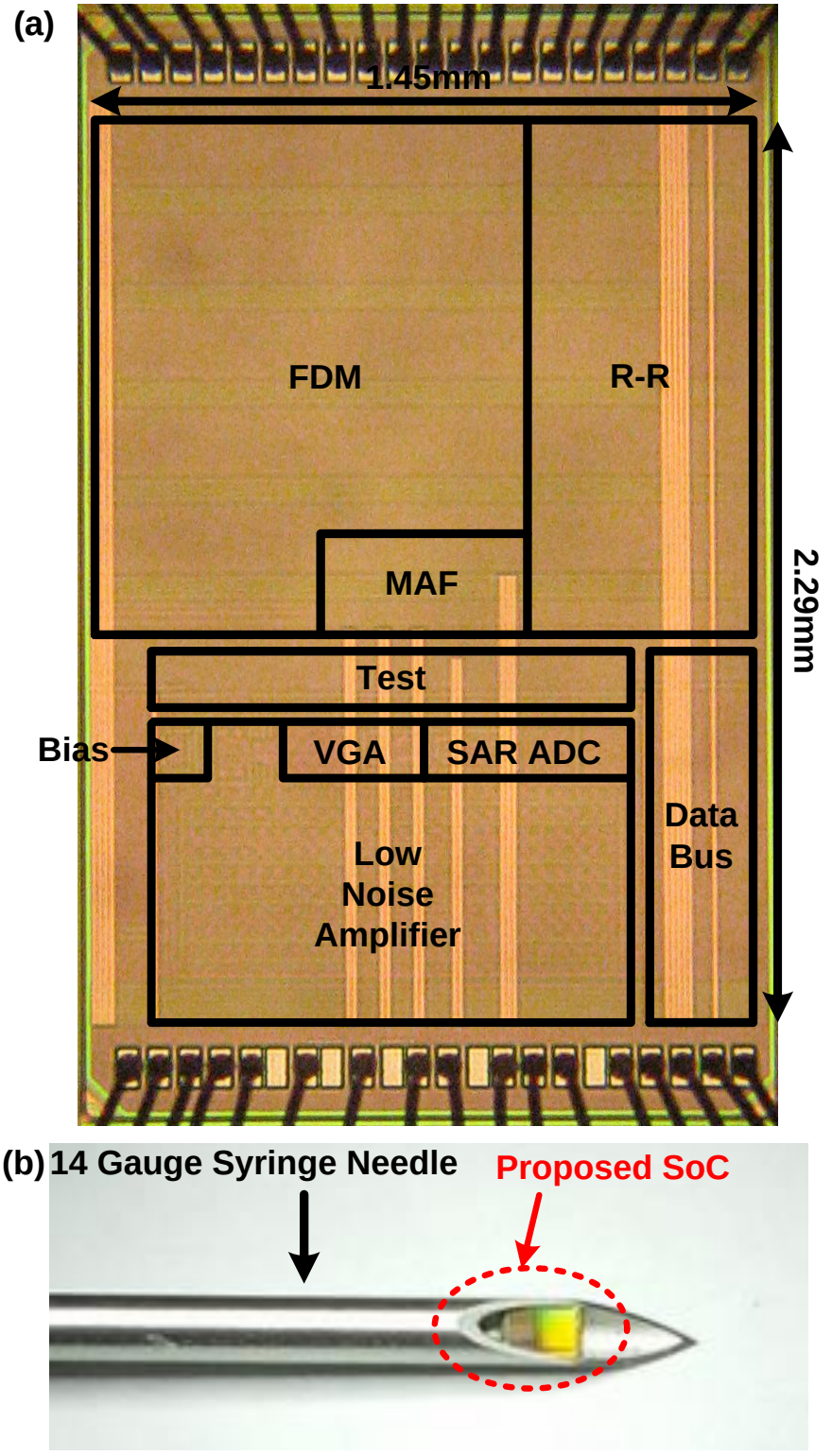


Figure 5.17 (a) Die photo of proposed SoC in 65nm LP CMOS. (b) Photo of proposed SOC and a 14 gauge syringe needle.

measured to be 55dB and 67dB, respectively. The measured SNR and THD with 0.5mV peak topeak input sin wave with rail to rail output are 48.6dB and 2.87% (-30.8dB).

The measured maximum DNL and INL of the SAR ADC are ±1.0 and ±1.8 respectively. Note that the nonlinearity resulted from the DNL and INL are still less than the amplifier non linearity as shown in the SNDR. The SNDR and the ENOB are 44.8dB and 7.14 bits respectively. The FOM of the ADC is 25.5fJ/conv-step. The SNDR of the entire AFE are 30.7dB which is dominated by the nonlinearity of the amplifier.

5.4.2 Proposed SoC Measured Results

Table 5.3 shows the overall measured system results. The digital back end operates at 0.4V with a clock frequency of 10kHz. The digital power consumption (including the clock

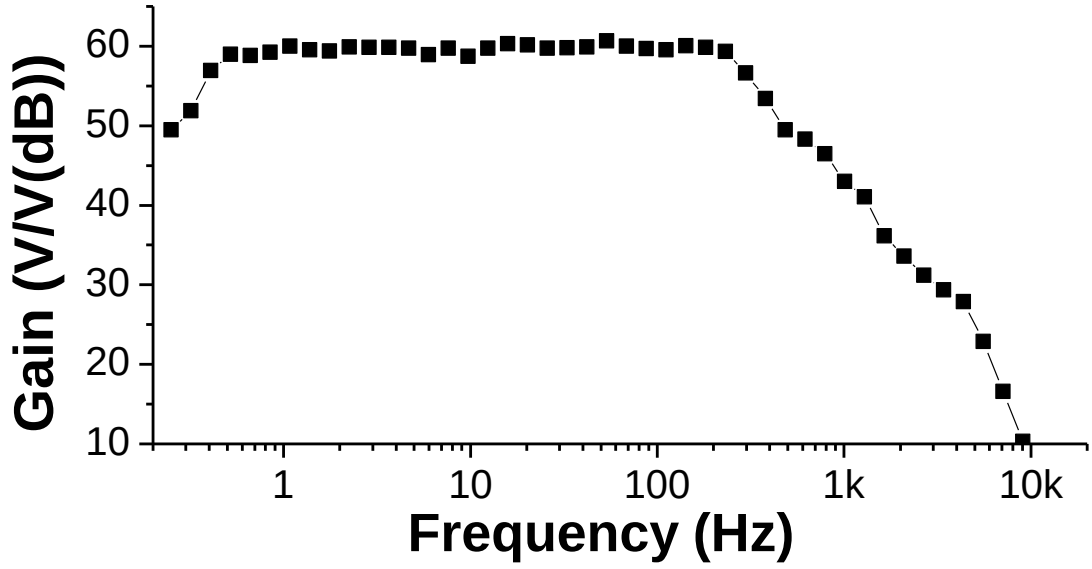


Figure 5.18 The measure frequency response of the amplifier with the midband gain set to 59dB

Table 5.3 Summary of measured results for SoC

Technology		65 nm
Die Area		1.45 × 2.29 mm^2
AFE	V_{DD}	0.6 V
	Current	28 nA (LNA + VGA) 3 nA (ADC)
	Gain	51 ~ 96 dB
	Bandwidth	250 Hz
	Input Impedance	> 100 MΩ for <500hz
	Input Referred Noise	253 nV/$\sqrt{Hz}$ (Noise Floor) 6.52 μV (RMS)
	Amplifier SNR	86dB
	NEF	2.64
	NEF×VDD^2	0.95
	CMRR@60Hz	55dB
	PSRR@60Hz	67dB
	THD	2.87%
	ADC Bits	8 Bits
	Sampling Frequency	500 Hz
	ADC Max DNL/INL	±1.0/±1.8
	ADC SNDR	44.8dB
	ADC ENOB	7.14
	ADC FOM	25.5fJ/conv-step
	AFE SNDR	30.7dB
DSP	V_{DD}	0.4 V
	Clock Frequency	10 kHz
	Total Memory	3.7 kB
	Power Consumption	45 nW (FDM) 92 nW (R-R)
	Main Processing Units	ARM Cortex-M0+ 16-b 512-pt RV FFT 80-tap FIR

power) is either 45nW (FDM) or 92nW (R-R), depending on the detection algorithm used. The proposed SoC consumes 64nW (110nW) in total when running the FDM (R-R) algorithm, enabling >5 day lifetime with a 3.7mm2 (5μA·hr) thin-film battery. The functionality of the digital block and the analog front end are tested with an atrial fibrillation signal generated by the ECG signal simulator (PS410 Patient Simulator, Fluke Biomedical, Everett, WA). The recorded waveform from the entire system is shown in the Figure 5.19(a). The system successfully

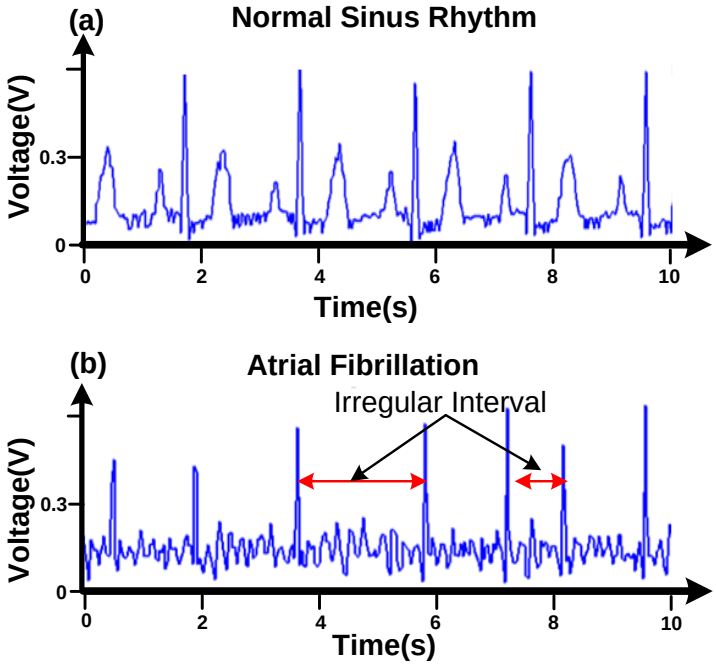


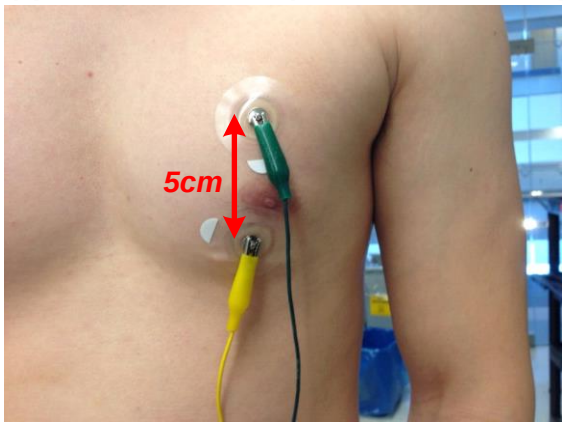
Figure 5.19 (a) Normal ECG waveform generated by ECG simulator and recorded by the proposed system. (b) An arrhythmia waveform generated by ECG simulator andrecorded and detected by the proposed system

captures the arrhythmia signal in Figure 5.19(b) under noisy supply and signals. As shown in the Figure 20, the system also tested with human body on the chest and commercial standard ECG electrode with 5cm separation.

5.4.3 Measurement Result with Peripherals

To build a complete electronics system, several other peripherals are needed including a power management unit and wireless module. The stacked microsystem of [12] includes a radio layer, control layer, and decap layer and is used in system-level testing in this work together with the proposed SoC (Figure 5.3(b)). The components of [12] consume 11nW in the default monitoring mode and the wireless module is activated (which consumes 20uW) only when

(a) Human Chest Experiment Test Setup



(b) Amplified Waveform

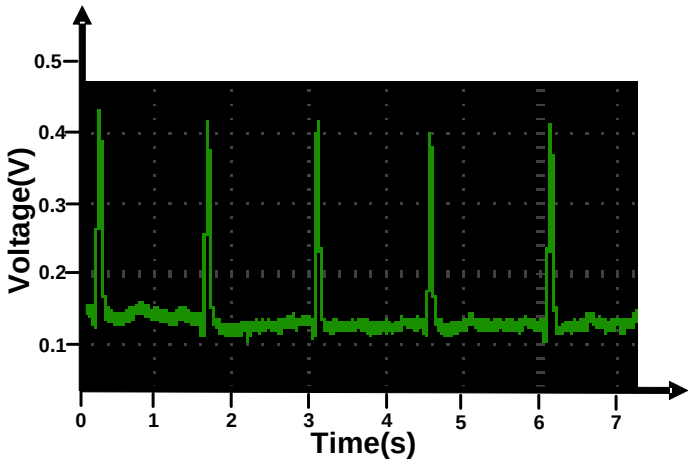


Figure 5.20 (a) Test setup of the Human Chest Experiment. (b) The amplified waveform observed from the amplifier output terminal by the Agilent oscilloscope. The Vol/Div is 100mV/Div and the Time/Div is 0.5sec/Div

needed during recharging and data retrieval. After the proposed SoC is programmed through the control layer and radio layer, other layers go into sleep mode and consume 11nW. When an arrhythmia is generated by the ECG simulator, the proposed SoC sends an interrupt signal to the control layer. The control layer then wakes up to retrieve the waveform and store it into memory. Moreover, the radio layer also wakes up and is able to send out an RF transmit signal at 915MHz.

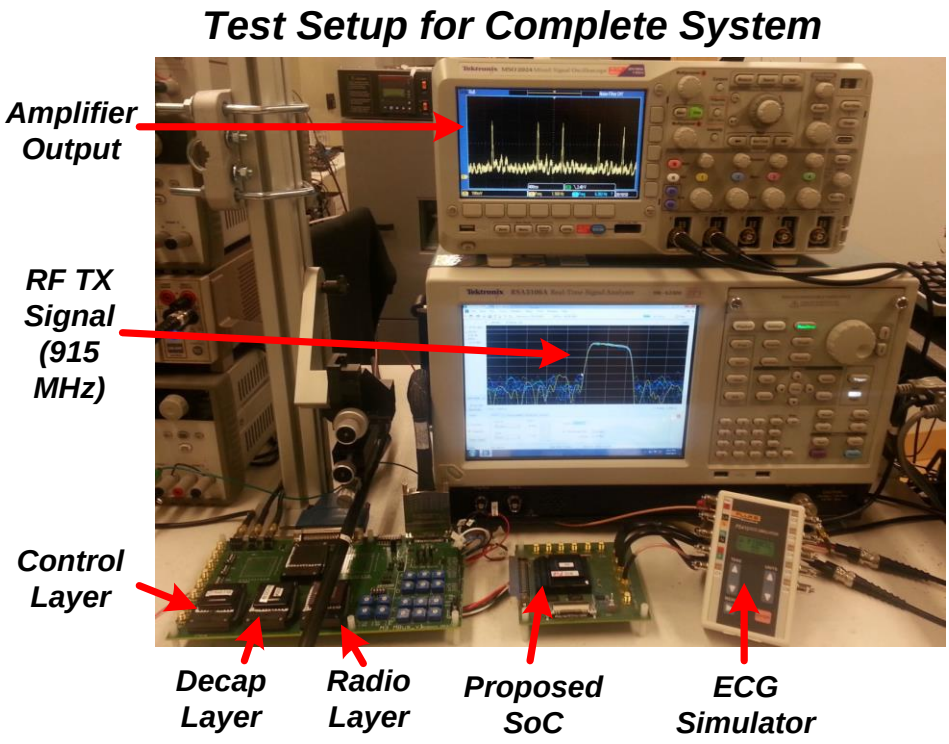


Figure 5.21 Test setup of complete system with simulator, proposed SoC, and [12]

The proposed SoC successfully communicates with other chips, including a power management unit and external memory from [12], over a data bus; the complete system configuration is shown in Figure 5. 21. Measured waveforms are taken by the SoC under different scenarios including an ECG simulator (Figure 5.19), a live sheep (Figures 5.22(a) and 5.22(b)), and an isolated sheep heart (Figures 5.22(c) and 5.22(d)). The isolated live sheep heart is immersed in conductive saline fluid to mimic the implantation environment. The electrodes connected to the analog front end are separated by 2cm and located near the heart. Note the low frequency wandering and 60Hz noise present in the measured waveform from a live sheep (which represents a patch-based approach as the electrodes are placed on the skin) compared to the isolated heart test. These signals demonstrate the signal quality improvement of a syringe-implantable approach. Table 5.4 provides a comparison table to related prior work.

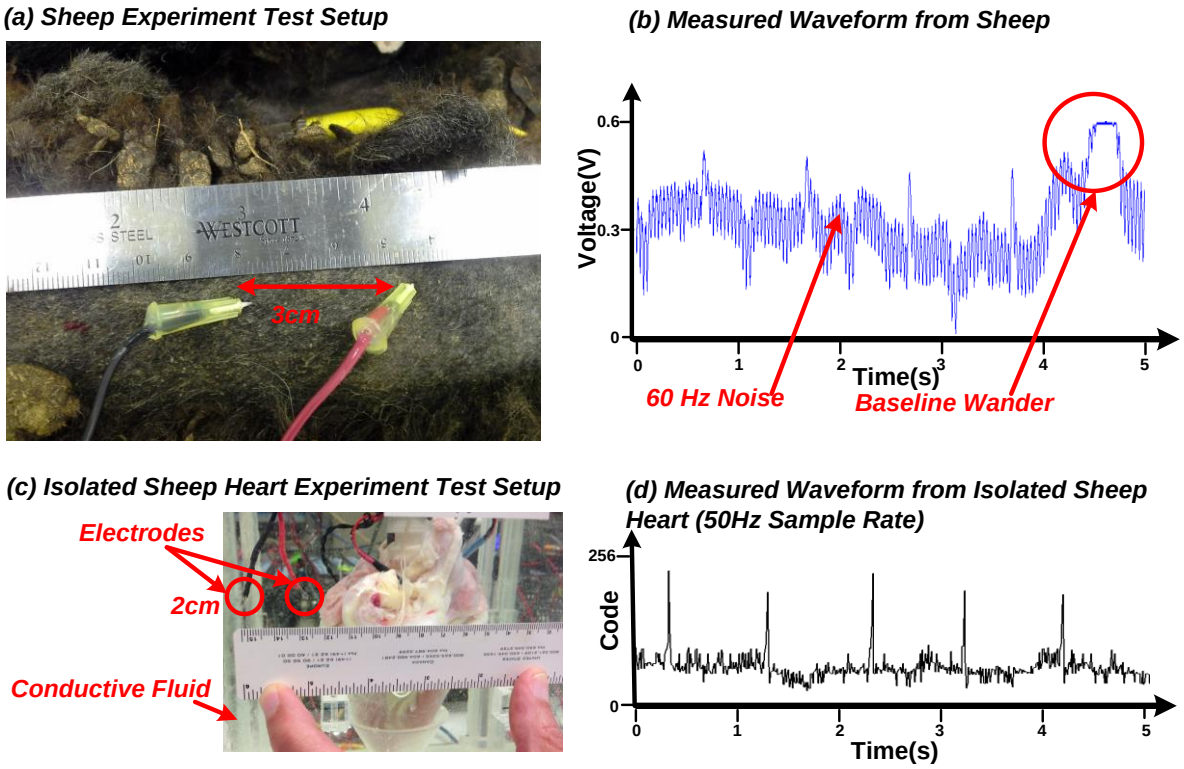


Figure 5.22 (a) The test setup of the sheep experiment. (b) The measure waveform of the experiment. (c) The test setup of the isolated sheep heart experiment. (d) The measure waveform of experiment from digital readout buffer. (downsampling by 10×)

5.5 Summary

This work presents an ultra-low power syringe-implantable long-term observation and arrhythmia detection ECG SoC fabricated in 65nm CMOS technology. The design trades off noise and power using analog-digital co-optimization and employs several amplifier techniques, asynchronous SAR logic, and minimum energy digital computation to achieve 64nW power consumption. The proposed circuit and new algorithm are verified under different scenarios ncluding an ECG simulator, a live sheep, and an isolated sheep heart. The SoC consumes state-of-the-art power compared to all other works with similar functionality.

Table 5.4 Comparison table for the proposed ECG system

		This Work	Zhang, JSSC'13[71]	Hsu, VLSI'12[50]	Kim, ISSCC'13 [51]	Liu, ASSCC '13 [52]	Deepu, ASSCC '13 [53]	Long, ISSCC'14[14]
Target Signals		**ECG**	ECG, EMG, EEG	ECG, VCG, PCG	ECG, Bio-Impedance	ECG	ECG	ECG
AFE	Technology	**65 nm**	130 nm	90 nm	180 nm	180 nm	350 nm	180 nm
	V_{DD}	**0.6 V**	1.2 V	0.5 V	1.8 V	0.5V	2.4V~3V	1.3V~1.8 V
	Current	**31 nA**	4 µA	20.44 µA (8-Bit, 2kHz Sampling)	-	22.7 nA (Amplifier Not Included)	12.5µA	680nA
	Gain	**51 ~ 96 dB**	40 ~ 78 dB	40 ~ 64 dB	40 ~ 64 dB	-	47 ~ 66 dB	20 ~ 44 dB
	Bandwidth	**250 Hz**	320 Hz	0.5 ~ 1 kHz	0.5 ~ 1 kHz	-	35 ~ 175 Hz	130Hz
	Input Referred Noise	**6.52uVrms**	-	-	200 $nV/\sqrt{Hz}$	-	1.4 µVrms	4.9 µVrms
	ADC Resolution	**8 Bits**	8 Bits	8/12 Bits	9.3 Bits (ENOB)	8.1 Bits (ENOB)	9.3 Bits (ENOB)	7-10 Bits
	ADC Sampling Frequency	**500 Hz**	-	250 Hz ~ 100 kHz	-	3kHz ~ 6kHz	256/512Hz	-
DSP	V_{DD}	**0.4 V**	0.3 ~ 1.2 V	0.5V (1.0V for SRAM)	- (Analog Signal Processing)	0.5V	2.4V~3V	- (Analog Signal Processing)
	Power Consumption	**45 nW**	2.1 µW	-		435nW	0.89 µA	
	Clock Frequency	**10 kHz**	2 kHz ~ 1.7 MHz	25 MHz		250Hz ~ 500Hz	-	
Memory for Waveform Storage		**10x Down sampled waveform in buffer**	Fully stored in processor memory	Fully store in 4kB data memory	Fully store in signal path	Store in full sized output buffer	Stored lossless compressed waveform	Not storing the waveform
System Total Power Consumption		**64 nW**	6.9 µW	22.6 µW	11.3 µW	457nW	32 µW	884 nW
Power Calculation Configuration		**AFE + DSP Arrhythmia Detection (FDM)**	AFE + DSP R-R Extraction	AFE (BSI) + DSP + OSC Arrhythmia Detection	AFE (3ch ECG + RA) + ASP + OSC Arrhythmia Detection	ADC + DSPE + Feature Extraction	AFE + DSPE + Feature Extraction	AFE + ASP + QRS Extraction

CHAPTER 6

Conclusion

6.1 Conclusion

Since the invention of the transistors and the integrated circuits, the continuous development on scaling for decades have resulted in smaller and smaller electronics devices surrounding the world. Nowadays, the mainstream devices have been changed from the desktop computers and laptops to the tablets and cellphones. And eventually technological advances might lead the next generation computer to minature sensor nodes for the internet of things (IoT).

There are many challenges have raised for the small form factor minature sensor nodes. The most critical one is the low power requirement since the limits form the small battery capacity directly caused by the severe physical size constraints on the battery. As a result, better power efficiency and power saving techniques is required to allow these systems to operate under extreme low power budget. In such systems the better power efficiency of the digital blocks can usually achieved by the benefit of the scaling. However, the power efficiency of the analog part is limited by the fundamental requirement of the signal to noise ratio (SNR) and become a key issue for low power design. To address this issue, in this dissertation, several new techniques are introduced and discussed to reduce the power consumption and improve the efficiency to achieve longer lifetime for the entire systems.

The power consumption can usually be written as follows:

$$Total\ Power = Active\ Rate\ \times Active\ Power + Sleep\ Power \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (6.1)$$

Each chapter in this dissertation has a focus on the equation. In chapter 2, a sample and hold bandgap voltage reference is presented. The main focus of the design on the bandgap voltage reference design is on reducing the "active rate" of the block. In order to decrease the active rate, the fast turn-on technique is used to reduce the wakeup time by 11.5× (from 55ms to 4.8ms) while the low leakage switch (decrease the leakage by more than 1000×) and the gate leakage compensator (decrease the leakage by 2.75× after low leakage switch) is used to lengthen the sleep time. And self-timing canary circuits is used to control the time period. As a results, the proposed marks 251× power improvement over the best prior bandgap voltage reference and is still 9.73× less power than the voltage reference published in 2015[84,85].

In chapter 3, an ultralow-leakage electrostatic discharge (ESD) power clamp designs for wireless sensor applications are proposed and implemented in 0.18μm CMOS is presented. The design is emphasis on reducing the leakage which is the "sleep power' of the entire systems in the sleep mode since the ESD is required to be always-on for the system protection. By applying porper choice of device size the capacitor, double stacking (2.9× leakage reduction) and GIDL reduction (5.4× more leakage reduction after double stacking)the overall leakage is reduced by 139×.

In chapter 4, a low power high efficiency neural signal recording amplifier is presented. The major improvement of it is developing a novel multi-chopper technique to establish the trade-off between the bandwidth and noise and break the fundamental limit of the power consumption due to the SNR requirement. Hence it is on reducing the "active power". The input

referred root mean square noise is 1.54μV (1-500Hz) with 266nA tail current corresponding to a 1.38 noise efficiency factor, which is the best reported among current state-of-the-art amplifiers.

Finally, in chapter 5, a system level design on syringe-implantable electrocardiography (ECG) monitoring system is proposed which is beyond the scope of the equation. The co-optimize power consumption with digital building blocks and the circuit techniques in the analog front end (AFE) enable 31nA current consumption. The proposed SoC is fabricated in 65nm CMOS and consumes 64nW while successfully detecting atrial fibrillation arrhythmia and storing the irregular waveform in memory in experiments using an ECG simulator, a live sheep, and an isolated sheep heart.

The aforementioned low power techniques in this dissertation can be generally used to overcome the low power design challenge and extend the system lifetime.

APPENDIX A

Noise Analysis on Voltage Reference

A.1 Noise analysis on bandgap voltage reference

The small signal model of the traditional bandgap reference is shown in Figure A.1, Noted that the following calculation on the noise analysis will all be done by the equation:

$$i_1 + i_2 + i_3 = 0 \quad (A.1)$$

And since the noise cannot be added in the voltage domain, all noise source are calculated separately and added up in the power domain in the end.

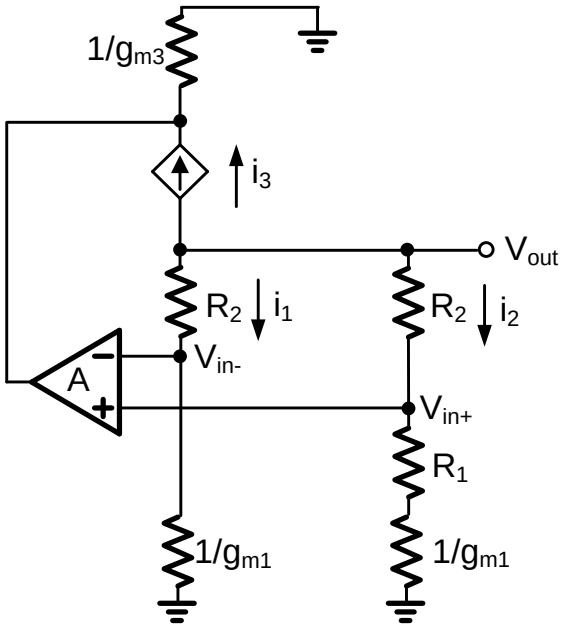


Figure A.1 The small signal model of the bandgap voltage reference

Now, consider the noise from each noise source respectively. For R_1 the voltage noise is equal to $\sqrt{4kTR_1}$. Therefore:

$$V_{in-} = V_{out}\frac{\frac{1}{g_{m1}}}{R_2+\frac{1}{g_{m1}}} \ldots\ldots\ldots\ldots\ldots\ldots (A.2)$$

$$V_{in+} = V_{out}\frac{R_1+\frac{1}{g_{m1}}}{R_2+R_1+\frac{1}{g_{m1}}} + \sqrt{4kTR_1}\frac{\frac{1}{g_{m1}}}{R_2+R_1+\frac{1}{g_{m1}}} \ldots\ldots\ldots\ldots (A.3)$$

By applying (A.2) and (A.3) into (A.1), we get:

$$V_{out}\frac{g_{m3}AR_1R_2+(2R_2+R_1+\frac{2}{g_{m1}})}{(R_2+R_1+\frac{1}{g_{m1}})(R_2+\frac{1}{g_{m1}})} + \sqrt{4kTR_1}\frac{\frac{g_{m3}}{g_{m1}}A-1}{R_2+R_1+\frac{1}{g_{m1}}} = 0$$

$$\rightarrow V_{out} = -\sqrt{4kTR_1}\frac{(\frac{g_{m3}}{g_{m1}}A-1)(R_2+\frac{1}{g_{m1}})}{g_{m3}AR_1R_2+(2R_2+R_1+\frac{2}{g_{m1}})} \ldots\ldots\ldots\ldots (A.4)$$

For R_2, the voltage noise equals to $\sqrt{4kTR_2}$:

$$V_{in-} = \left(V_{out}-\sqrt{4kTR_2}\right)\frac{\frac{1}{g_{m1}}}{R_2+\frac{1}{g_{m1}}} \ldots\ldots\ldots\ldots\ldots\ldots (A.5)$$

$$V_{in+} = V_{out}\frac{R_1+\frac{1}{g_{m1}}}{R_2+R_1+\frac{1}{g_{m1}}} \ldots\ldots\ldots\ldots\ldots\ldots (A.6)$$

By applying (A.5) and (A.6) into (A.1), we get:

$$V_{out}\frac{g_{m3}AR_1R_2+(2R_2+R_1+\frac{2}{g_{m1}})}{(R_2+R_1+\frac{1}{g_{m1}})(R_2+\frac{1}{g_{m1}})}+\sqrt{4kTR_2}\frac{\frac{g_{m3}}{g_{m1}}A-1}{R_2+\frac{1}{g_{m1}}}=0$$

$$\rightarrow V_{out}=-\sqrt{4kTR_2}\frac{(\frac{g_{m3}}{g_{m1}}A-1)(R_2+R_1+\frac{1}{g_{m1}})}{g_{m3}AR_1R_2+(2R_2+R_1+\frac{2}{g_{m1}})}\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(A.7)$$

For R_3, the voltage noise also equals to $\sqrt{4kTR_2}$:

$$V_{in-}=\ V_{out}\frac{\frac{1}{g_{m1}}}{R_2+\frac{1}{g_{m1}}}\ \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots.(A.8)$$

$$V_{in+}=(V_{out}-\sqrt{4kTR_2})\frac{R_1+\frac{1}{g_{m1}}}{R_2+R_1+\frac{1}{g_{m1}}}\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(A.9)$$

By applying (A.8) and (A.9) into (A.1), we get:

$$V_{out}\frac{g_{m3}AR_1R_2+(2R_2+R_1+\frac{2}{g_{m1}})}{(R_2+R_1+\frac{1}{g_{m1}})(R_2+\frac{1}{g_{m1}})}-\sqrt{4kTR_2}\frac{g_{m3}A(R_1+\frac{1}{g_{m1}})+1}{R_2+R_1+\frac{1}{g_{m1}}}=\ 0$$

$$\rightarrow V_{out}=\sqrt{4kTR_2}\frac{(g_{m3}A(R_1+\frac{1}{g_{m1}})+1)(R_2+\frac{1}{g_{m1}})}{g_{m3}AR_1R_2+(2R_2+R_1+\frac{2}{g_{m1}})}\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(A.10)$$

For Q_1 the voltage noise equals to $\frac{\sqrt{2qI}}{g_{m1}}$:

$$V_{in-}=\ \left(V_{out}-\frac{\sqrt{2qI}}{g_{m1}}\right)\frac{\frac{1}{g_{m1}}}{R_2+\frac{1}{g_{m1}}}+\ \frac{\sqrt{2qI}}{g_{m1}}=V_{out}\frac{\frac{1}{g_{m1}}}{R_2+\frac{1}{g_{m1}}}+\frac{\sqrt{2qI}}{g_{m1}}\frac{R_2}{R_2+\frac{1}{g_{m1}}}\ldots.\ldots\ldots(A.11)$$

$$V_{in+} = V_{out}\frac{R_1 + \frac{1}{g_{m1}}}{R_2 + R_1 + \frac{1}{g_{m1}}} \tag{A.12}$$

By applying (A.11) and (A.12) into (A.1), we get:

$$V_{out}\frac{g_{m3}AR_1R_2 + (2R_2 + R_1 + \frac{2}{g_{m1}})}{(R_2 + R_1 + \frac{1}{g_{m1}})(R_2 + \frac{1}{g_{m1}})} - \frac{\sqrt{2qI}}{g_{m1}}\frac{g_{m3}AR_2 + 1}{R_2 + \frac{1}{g_{m1}}} = 0$$

$$\rightarrow V_{out} = -\frac{\sqrt{2qI}}{g_{m1}}\frac{(g_{m3}AR_2 + 1)(R_2 + R_1 + \frac{1}{g_{m1}})}{g_{m3}AR_1R_2 + (2R_2 + R_1 + \frac{2}{g_{m1}})} \tag{A.13}$$

For Q_2, the voltage noise also equals to $\frac{\sqrt{2qI}}{g_{m1}}$:

$$V_{in-} = V_{out}\frac{\frac{1}{g_{m1}}}{R_2 + \frac{1}{g_{m1}}} \tag{A.14}$$

$$V_{in+} = V_{out}\frac{R_1 + \frac{1}{g_{m1}}}{R_2 + R_1 + \frac{1}{g_{m1}}} + \frac{\sqrt{2qI}}{g_{m1}}\frac{\frac{1}{g_{m1}}}{R_2 + R_1 + \frac{1}{g_{m1}}} \tag{A.15}$$

By applying (A.14) and (A.15) into (A.1), we get:

$$V_{out}\frac{g_{m3}AR_1R_2 + (2R_2 + R_1 + \frac{2}{g_{m1}})}{(R_2 + R_1 + \frac{1}{g_{m1}})(R_2 + \frac{1}{g_{m1}})} + \frac{\sqrt{2qI}}{g_{m1}}\frac{\frac{g_{m3}}{g_{m1}}A - 1}{R_2 + R_1 + \frac{1}{g_{m1}}} = 0$$

$$\rightarrow V_{out} = -\frac{\sqrt{2qI}}{g_{m1}}\frac{(\frac{g_{m3}}{g_{m1}}A - 1)(R_2 + \frac{1}{g_{m1}})}{g_{m3}AR_1R_2 + (2R_2 + R_1 + \frac{2}{g_{m1}})} \tag{A.16}$$

For the voltage noise inside the amplifier equals to V_n:

$$V_{in-} = V_{out}\frac{\frac{1}{g_{m1}}}{R_2 + \frac{1}{g_{m1}}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (A.17)$$

$$V_{in+} = V_{out}\frac{R_1 + \frac{1}{g_{m1}}}{R_2 + R_1 + \frac{1}{g_{m1}}} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (A.18)$$

By applying (A.17) and (A.18) into (A.1), we get:

$$V_{out}\frac{g_{m3}AR_1R_2 + (2R_2 + R_1 + \frac{2}{g_{m1}})}{(R_2 + R_1 + \frac{1}{g_{m1}})(R_2 + \frac{1}{g_{m1}})} + V_n g_{m3}A = 0$$

$$V_{out} = -V_n\frac{g_{m3}A(R_2 + \frac{1}{g_{m1}})(R_2 + R_1 + \frac{1}{g_{m1}})}{g_{m3}AR_1R_2 + (2R_2 + R_1 + \frac{2}{g_{m1}})} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (A.19)$$

For the current noise of M_3 equals to $\sqrt{4kT\gamma\frac{1}{g_{m3}}}$

$$V_{in-} = V_{out}\frac{\frac{1}{g_{m1}}}{R_2 + \frac{1}{g_{m1}}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (A.20)$$

$$V_{in+} = V_{out}\frac{R_1 + \frac{1}{g_{m1}}}{R_2 + R_1 + \frac{1}{g_{m1}}} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (A.21)$$

By applying (A.20) and (A.21) into (A.1), we get:

$$V_{out}\frac{g_{m3}AR_1R_2+(2R_2+R_1+\frac{2}{g_{m1}})}{(R_2+R_1+\frac{1}{g_{m1}})(R_2+\frac{1}{g_{m1}})}+\sqrt{4kT\gamma g_{m3}}=0$$

$$\rightarrow V_{out}=-\sqrt{4kT\gamma g_{m3}}\frac{(R_2+\frac{1}{g_{m1}})(R_2+R_1+\frac{1}{g_{m1}})}{g_{m3}AR_1R_2+(2R_2+R_1+\frac{2}{g_{m1}})}\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(A.22)$$

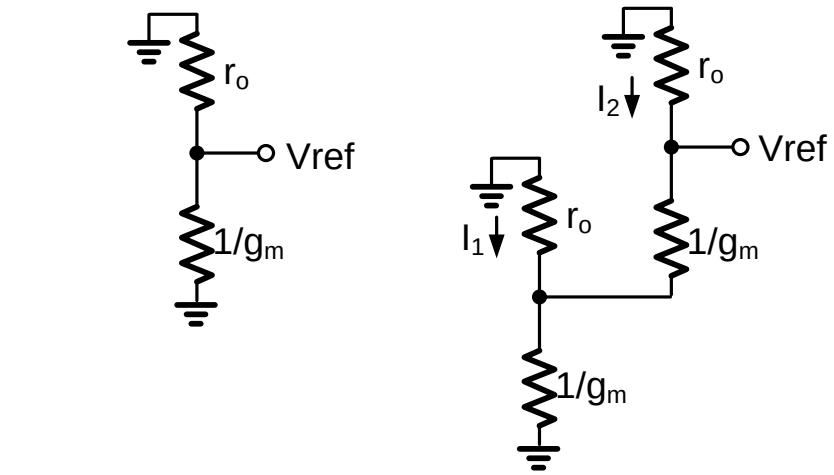
Combine all the noise equations: (A.4), (A.7), (A.10), (A13), (A.16), (A.19) and (A.22) together by summing all the noise in the power domain. The total noise of the entire reference is:

$$V_{n,total}^2$$

$$=\frac{\left(\left(4kTR_1+\frac{2qI}{g_{m1}^2}\right)\left(\frac{g_{m3}}{g_{m1}}A-1\right)^2+4kTR_2\left(\left(g_{m3}A(R_1+\frac{1}{g_{m1}})+1\right)^2\right)\right)(g_{m1}R_2+1)^2}{\left(g_{m1}g_{m3}AR_1R_2+(2g_{m1}R_2+g_{m1}R_1+2)\right)^2}$$

$$+\frac{\left(4kTR_2\left(\frac{g_{m3}}{g_{m1}}A-1\right)^2+\frac{2qI}{g_{m1}^2}(g_{m3}AR_2+1)^2\right)(g_{m1}R_2+g_{m1}R_1+1)^2}{\left(g_{m1}g_{m3}AR_1R_2+(2g_{m1}R_2+g_{m1}R_1+2)\right)^2}$$

$$+\frac{(V_n^2\frac{g_{m3}^2}{g_{m1}^2}A^2+4kT\gamma\frac{g_{m3}}{g_{m1}^2})(g_{m1}R_2+1)^2(g_{m1}R_2+g_{m1}R_1+1)^2}{\left(g_{m1}g_{m3}AR_1R_2+(2g_{m1}R_2+g_{m1}R_1+2)\right)^2}\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(A.23)$$



(a) 2-T voltage reference (b) 4-T voltage reference

Figure A.2 The small signal model of the 2-T and 4-T voltage reference

A.2 Noise analysis on 2-T and 4-T voltage reference

The small signal model of the 2-T and 4-T voltage reference is shown in Figure A.2.

Since all the MOS is expected to operate in the subthreshold region, the current noises of all these transistors are expected to be 2qI. For the 2-T voltage reference, it is easy to calculate:

$$V_{noise,M1}^2 = 2qI \times \left(r_o // \frac{1}{g_m}\right)^2 \quad (A.24)$$

$$V_{noise,M2}^2 = 2qI \times \left(r_o // \frac{1}{g_m}\right)^2 \quad (A.25)$$

Combine the equation (A.24) and (A.25) by summing the noise in the power domain. we can get:

$$V_{noise}^2 = 2qI \times \left(r_o // \frac{1}{g_m}\right)^2 + 2qI \times \left(r_o // \frac{1}{g_m}\right)^2 \cong 4qI \frac{1}{{g_m}^2} = 4qI \frac{n^2 V_t^2}{4I^2} = \frac{qn^2 V_t^2}{I} \quad (A.26)$$

For the 4-T voltage reference, the following equations show the noise performance. Noted that due to requirement of the design, $I_1 \gg I_2$.

$$V_{noise,M1}^2 = 2qI_1 \times \left(r_o // \left(\frac{1}{g_{m2}} // \left(\frac{1}{g_{m4}} + r_o\right)\right)\right)^2 \cong 2qI_1 \left(\frac{1}{g_{m2}}\right)^2 \ldots\ldots\ldots\ldots\ldots\ldots\ldots (A.27)$$

$$V_{noise,M2}^2 = 2q(I_1 + I_2) \times \left(r_o // \left(\frac{1}{g_{m2}} // \left(\frac{1}{g_{m4}} + r_o\right)\right)\right)^2 \cong 2q(I_1 + I_2) \left(\frac{1}{g_{m2}}\right)^2 \ldots\ldots (A.28)$$

$$V_{noise,M3}^2 = 2qI_2 \times \left(r_o // \left(\frac{1}{g_{m4}} + \left(\frac{1}{g_{m2}} // r_o\right)\right)\right)^2 \cong 2qI_2 \left(\frac{1}{g_{m2}} + \frac{1}{g_{m4}}\right)^2 \ldots\ldots\ldots\ldots\ldots (A.29)$$

$$V_{noise,M4}^2 = \left(\sqrt{2qI_2} \frac{1}{g_{m4}} \frac{r_o}{r_o + \frac{1}{g_{m4}} + \left(\frac{1}{g_{m2}} // r_o\right)}\right)^2 \cong 2qI_2 \left(\frac{1}{g_{m4}}\right)^2 \ldots\ldots\ldots\ldots\ldots\ldots\ldots (A.30)$$

Combine the equation (A.24) and (A.25) by summing the noise in the power domain. we can get:

$$V_{noise}^2 \cong 2qI_1 \left(\left(\frac{1}{g_{m2}}\right)^2 + \left(\frac{1}{g_{m2}}\right)^2\right) + 2qI_2 \left(\left(\frac{1}{g_{m2}}\right)^2 + \left(\frac{1}{g_{m2}} + \frac{1}{g_{m4}}\right)^2 + \left(\frac{1}{g_{m4}}\right)^2\right)$$

$$= \frac{qI_1 n^2 V_t^2}{(I_1 + I_2)^2} + qI_2 n^2 V_t^2 \left(\frac{2}{(I_1 + I_2)^2} + \frac{2}{{I_2}^2} + \frac{1}{I_2(I_1 + I_2)}\right)$$

$$\cong \frac{qn^2 V_t^2}{I_1} + \frac{2qn^2 V_t^2}{I_2} \cong \frac{2qn^2 V_t^2}{I_2} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (A.31)$$

APPENDIX B

Pseudo Resistors Measured Results

B.1 Introduction

Pseudo resistor is a common technique to generate very high impedance (>GΩ) widely used in many biomedical circuits required low bandwidth. Figure 1 shows the typical structure of the pseudo resistor. It is consists of two back to back off transistors to ensure that it is symmetric. The current equation can be written as follows if there is a voltage V across the pseudo resistor:

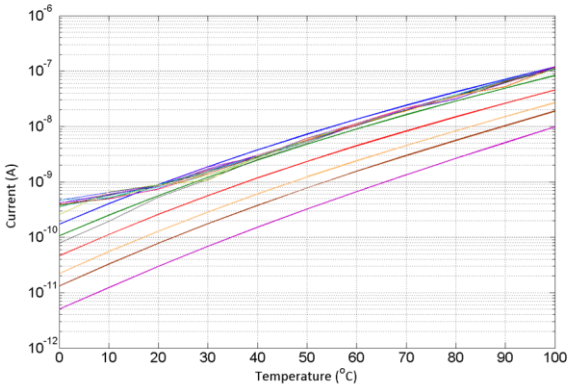
$$\mathrm{I} = \mathrm{I_o}\left(\frac{\mathrm{W}}{\mathrm{L}}\right)\mathrm{e}^{\frac{\mathrm{V_{GS}}-\mathrm{V_{th}}}{\mathrm{nkT/q}}}\left(1-\mathrm{e}^{-\frac{\mathrm{V_{DS}}}{\mathrm{kT/q}}}\right)\ldots\ldots\ldots\ldots\ldots\ldots\ldots(\mathrm{B.1})$$

$$\mathrm{I} = \mathrm{I_o}\left(\frac{\mathrm{W}}{\mathrm{L}}\right)\mathrm{e}^{\frac{\mathrm{V/2}-\mathrm{V_{th}}}{\mathrm{nkT/q}}}\left(1-\mathrm{e}^{-\frac{\mathrm{V/2}}{\mathrm{kT/q}}}\right)\ldots\ldots\ldots\ldots\ldots\ldots\ldots(\mathrm{B.2})$$

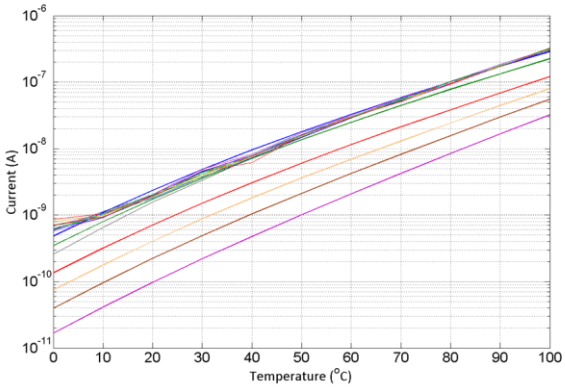
$$\frac{1}{\mathrm{R}} = \frac{\partial \mathrm{I}}{\partial \mathrm{V}} = \mathrm{I_o}\left(\frac{\mathrm{W}}{\mathrm{L}}\right)\mathrm{e}^{\frac{-\mathrm{V_{th}}}{\mathrm{nkT/q}}}\left(\mathrm{e}^{\frac{\mathrm{V/2}}{\mathrm{nkT/q}}}\frac{\mathrm{q}}{2\mathrm{nkT}}\left(1-\mathrm{e}^{-\frac{\mathrm{V/2}}{\mathrm{kT/q}}}\right)+\mathrm{e}^{\frac{\mathrm{V/2}}{\mathrm{nkT/q}}}\left(-\mathrm{e}^{-\frac{\mathrm{V/2}}{\mathrm{kT/q}}}\right)\frac{\mathrm{q}}{2\mathrm{kT}}\right)\ldots\ldots\ldots(\mathrm{B.3})$$

From the above equation, the resistor is heavily depending on the voltage across the pseudo resistor and the threshold voltage of the devices which is highly nonlinear and tends to be

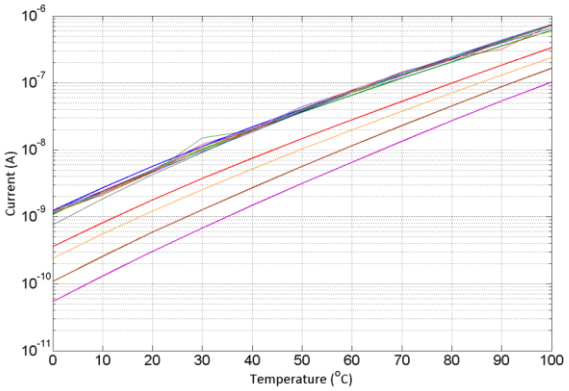
Figure B.1 Structure of a standard pseudo resistor



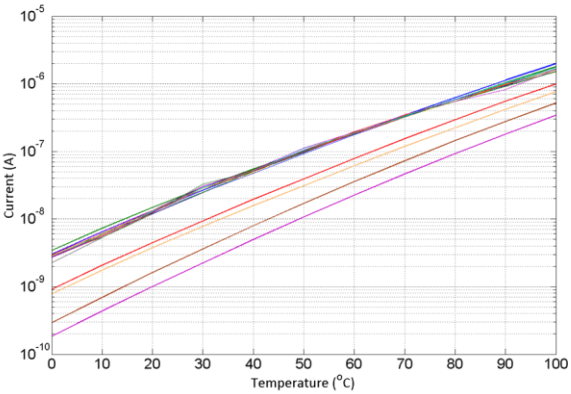
(a) With 0.1V across the pseudo resistor



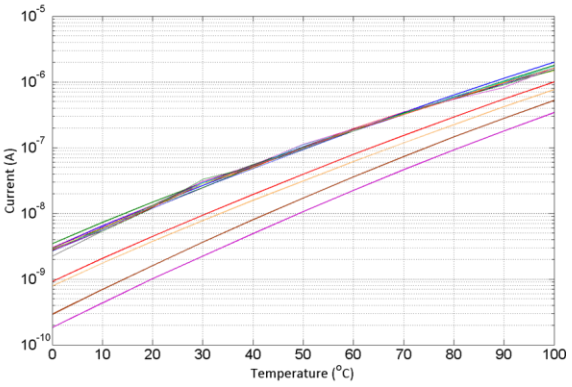
(b) With 0.2V across the pseudo resistor



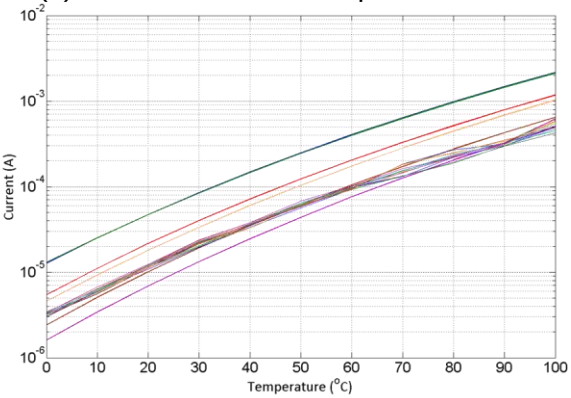
(c) With 0.3V across the pseudo resistor



(d) With 0.4V across the pseudo resistor



(e) With 0.5V across the pseudo resistor



(f) With 1V across the pseudo resistor

Figure B.2 Measurement and simulation results of the pseudo resistor across different temperature. Blue: FF(BSIM3), Green: FF(BSIM4), Red: TT(BSIM3), Orange: TT(BSIM4), Brown: SS(BSIM3), Purple: SS(BSIM4) Others: 14 dies at the same run

Table B.1 Measurement results across different voltage

Voltage	Current(nA)	σ	σ/μ
0.1	0.752	0.0263	3.50%
0.2	2.239	0.07672	3.43%
0.3	6.122	0.1907	3.12%
0.4	16.76	0.5193	3.10%
0.5	46.59	1.417	3.04%
0.6	132.9	3.942	2.97%
0.7	389.8	19.32	4.96%
0.8	1059	53.65	5.07%
0.9	4306	187.9	4.36%
1	15050	919.1	6.11%

suffered from process variation. Recently, there are some other approach rather than the normal pseudo resistors [86, 87] to generate high impedance. However, the design in [86] require an extra amplifier and the duty cycled approach in [87] might suffer from leakage problem in the advanced technology. Therefore, pseudo resistors are still widely used in most of the low frequency design [36-41].

One of the most common issues for the pseudo resistors design is that the inaccuracy of the model. For the same transistor in the same technology node from the same foundry, the simulation between different version of the models (BSIM3 [88] or BSIM4 [89]) can have large difference. Since the design in the chapter 4 requires pseudo resistor for the biasing and the

CMFB, a separate die to observe the pseudo resistor value for better design the corner frequency is tapeout and measured.

B.2 Measurement Results and Conclusions

Figure B.2 and Table B.1 show the simulation and the measurement results of the pseudo resistors. From Table B.1, the resistance is clearly highly nonlinear as it is shown in the equation (B.3). Noted that under the same bias voltage the resistance is usually follow one of the model correctly. At small voltage bias (<0.1V) to medium range voltage (around 0.5V which is the usual bias point for full swing output), it follows the FF corner of the BSIM3 model. While biased at high voltage (>1V), it follows SS corner of the BSIM3 model. The above results also show that the current is expected to be larger at low bias and smaller at higher bias. From equation (B.3), it implies that the coefficient n is not modeled well in the subthreshold region.

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