Straintronics: A Leap towards Ultimate Energy Efficiency of Magnetic Memory and Logic

By:

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Dedicated…

To my mother, who read me "the Giving Tree" when I was a child and taught me lessons in love, sacrifice, morality, and responsibility

To my father, who took me to work with him in summers of my childhood and bought me ice-cream after to teach me good things never come easy

To my sister, who asked mom and dad for a little brother, then taught him the value of friendship and stayed by his side through every single up and down in life

And to the big guy above, at whom I yelled sometimes when the rollercoaster of life was falling dawn, only to realize later that it was indeed accelerating to reach even higher climaxes…

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ABSTRACT

After decades of exponential growth of the semiconductor industries, predicted by Moore's Law, the complementary metal-oxide semiconductor (CMOS) circuits are approaching their end of the road, as the feature sizes reach sub-10nm regimes, leaving electrical engineers with a profusion of design challenges in terms of energy limitations and power density. The latter has left the road for alternative technologies wide open to help CMOS overcome the present challenges.

Magnetic random access memories (MRAM) are one of the candidates to assist with aforesaid obstacles. Proposed in the early 90's, MRAM has been under research and development for decades. The expedition for energy efficient MRAM is carried out by the fact that magnetic logic, potentially, has orders of magnitude lower switching energy compared to a charge-based CMOS logic since, in a nanomagnet, magnetic domains would self-align with each other. Regrettably, conventional methods for switching the state of the cell in an MRAM, field induced magnetization switching (FIMS) and spin transfer torque (STT), use electric current (flow of charges) to switch the state of the magnet, nullifying the energy advantage, stated above. In order to maximize the energy efficiency, the amount of charge required to switch the state of the MTJ should be minimized. To this end, straintronics, as an alternative energy efficient method to FIMS and STT to switch the state of a nanomagnet, is proposed recently. The method states that by combining piezoelectricity and inverse magnetostriction, the magnetization state of the device can flip, within few nano-seconds while reducing the switching energy by orders of magnitude compared to STT and FIMS.

This research focuses on analysis, design, modeling, and applications of straintronics-based MTJ. The first goal is to perform an in-depth analysis on the static and dynamic behavior of the device. Next, we are aiming to increase the accuracy of the model by including the effect of temperature and thermal noise on the device's behavior. The goal of performing such analysis is to create a comprehensive model of the device that predicts both static and dynamic responses of the magnetization to applied stress. The model will be used to interface the device with CMOS controllers and switches in large systems. Next, in an attempt to speed up the simulation of such devices in multi-megabyte memory systems, a liberal model has been developed by analytically approximating a solution to the magnetization dynamics, which should be numerically solved otherwise. The liberal model demonstrates more than two orders of magnitude speed improvement compared to the conventional numerical models.

Highlighting the applications of the straintronics devices by combining such devices with peripheral CMOS circuitry is another goal of the research. Design of a proof-of-concept 2 kilo-bit nonvolatile straintronics-based memory was introduced in our recent work. To highlight the potential applications of the straintronics device, beyond data storage, the use of the principle in ultra-fast yet low power true random number generation and neuron/synapse design for artificial neural networks have been investigated.

Lastly, in an attempt to investigate the practicality of the straintronics principle, the effect of process variations and interface imperfections on the switching behavior of the magnetization is investigated. The results reveal the destructive aftermath of fabrication imperfections on the switching pattern of the device, leaving careful pulse-shaping, alternative topologies, or combination with STT as the last resorts for successful strain-based magnetization switching.

CHAPTER 1: INTRODUCTION

As minimum feature sizes in CMOS scale below 65 nm and system frequencies increase, the need for static and dynamic power reduction becomes more crucial in digital design. The active power in digital systems decreases rapidly due to smaller parasitic capacitances in newer technologies [1]. The leakage power, however, does not decrease at the same pace [2]. In fact, as the feature size in CMOS scales below 22 nm, static power dissipation due to multiple sources of leakage (weak inversion current, drain induced barrier lowering (DIBL), gate induced drain leakage (GIDL), gate tunneling, etc.) becomes significantly large in digital circuits. Further, newer technologies do not scale the supply voltage proportionately. Therefore, the shorter channel length along with the higher supply voltage leads to higher leakage power dissipation [3]. Thus, integrated circuits (ICs) are facing a growing leakage to active power ratio [4]. Leakage is more pronounced in low speed applications like biomedical devices and environmental sensors, since their nominal operating frequencies are usually limited to below megahertz [5]. Another obstacle that newer technologies are facing is high power density of the systems [6], which requires expensive packaging of the chips or alternative cooling solutions. Furthermore, in the past few decades, the battery and harvesting technologies have not advanced nearly as fast as CMOS technologies, which leave the millimeter-sized integrated circuits with a low energy budget to live on. Finally, the ultimate Physics laws will prevent the conventional CMOS scaling to go much beyond 10 nm [7]. In order to push the integration density as prophesized by Moore's Law and fuel the demands of information, computing, and

communication technologies (ICCT), the CMOS process and packaging technology must fabricate three-dimensional (3-D) chips. Again, pure CMOS dissipates high leakage power, posing serious challenges for thermal management and hot-spot failures for fine-grained 3-D integration. The above obstacles, visually demonstrated in Fig. 1-1 [8-10], call for novel solutions to enable the industry to keep up with Moore's law [11].

The issues pertaining to low energy (Joule/op) demand of sub-45 nm CMOS technologies can be independently tackled by an assortment of CMOS device and circuit techniques [12-15] such as (a) tunneling FET with steep sub-threshold slope, (b) high-K gate dielectrics, (c) fin-shaped vertical channels, (d) wraparound (Omega) gates, (e) multi-threshold transistors (MTCMOS), (f) power gating, (g) sleep transistors, (h) PMOS/NMOS sizing, (i) reduced signal swings, (j) reduction of glitches, (k) adaptive body biasing (Reverse, Forward, and Zero Body Biasing) as well as architectural techniques like (l) pipelining and replication of circuit blocks for reduced supply voltage operation, (m) clock gating and reduced clock voltage, and (n) dynamic voltage and frequency scaling (DVFS). However, these solutions do not fully remedy the high leakage

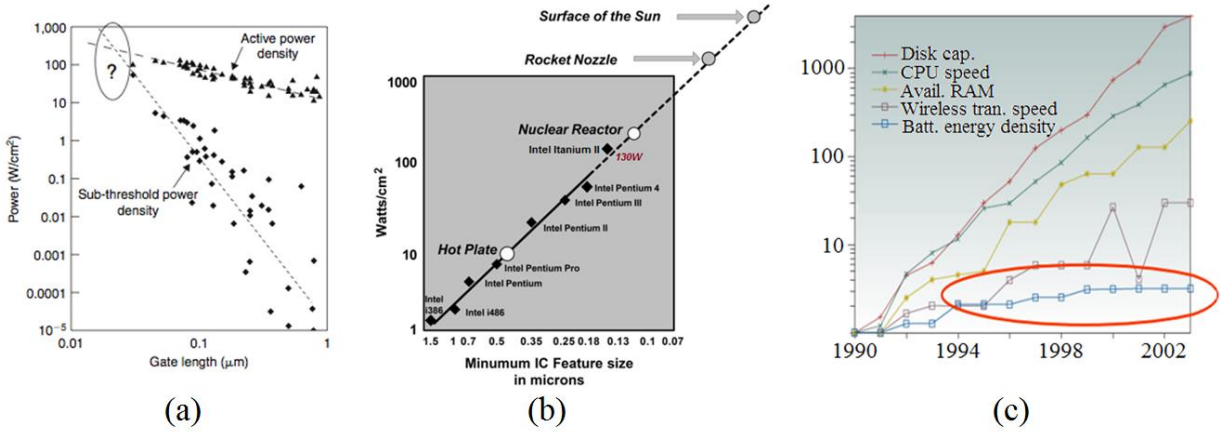

Figure 1-1 - (a) Increasing the leakage to active power ratio as CMOS technologies continue to scale down is one of the major obstacles that circuit designers are facing [8], (b) The increasing energy density at smaller nodes with higher frequencies of operation requires expensive packaging and complicated cooling solutions [9], and (c) Battery technologies have not progressed as fast as integrated circuits, leaving millimeter sized circuits with few micro-amperes of power to live on [10]

current, high power density and battery limitations of CMOS circuitry as the technology approaches its end of the road.

During the past two decades, the US Government has invested several billion dollars through multiple federal agencies to discover the new Boolean switch that will replace CMOS as it was prognosticated to hit the brick wall at nearly 100 nm technology nodes. A plethora of emerging devices such as single electron transistors [16], quantum dots [17], nanowires [18], spin transistors [19], plasmon transistors [20], and phonon devices [21] have looked promising in limited applications, but they do not have the versatile features of CMOS to replace it lock, stock and barrel. A more pragmatic approach is to invent CMOS+X technology that can compensate the shortcomings of charge-based technology like CMOS enabling the accelerated growth of VLSI chips to fuel the insatiable demands of information technology, computing, communication, and consumer electronics. The main shortcomings of CMOS that CMOS+X technology can remedy are: i) CMOS is charge-based and, therefore, volatile. It loses information if the power supply is turned off; ii) CMOS's static leakage currents dominate as the technology nodes shrink, posing difficulties in dense three-dimensional packaging. Thermal management can alleviate if the system states can be stored in non-volatile devices and power supply can be selectively turned off; iii) CMOS's reliability exacerbates as technology nodes reduce [22] due to cosmic rays, temperature-induced static leakages, and on-chip sources of noise such as substrate activity, signal coupling, simultaneous switching by synchronized clock signals, power and ground voltage fluctuations, etc.; and iv) On-chip memory devices such as SRAM are very large, especially at near and sub-threshold power supply applications where up to 10 transistors per cell is used in order to achieve reasonable Read noise margin under widely varying process, voltage and temperature (PVT) parameters. These shortcomings preclude the

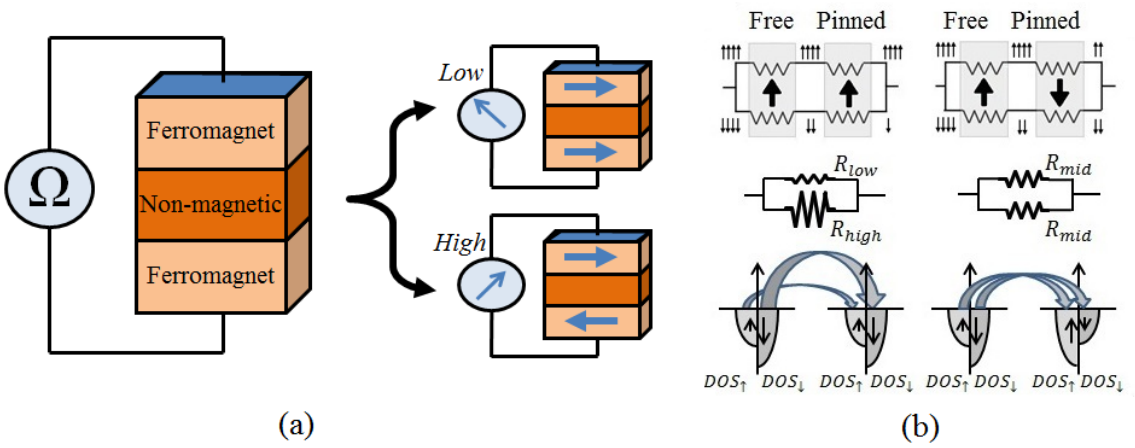

Figure 1-2 - (a) Tunnel magnetoresistance effect observed in a magnetic tunneling junction; maximum and minimum resistance states are observed in antiparallel and parallel orientations, respectively, and (b) Resistance changes is mainly due to the difference in the DOS for parallel and antiparallel oriented electrons

reliable use of distributed logic in memory (LIM) architectures that offer multiple advantages over conventional consolidated CPU and cache/primary memory architectures. This is where CMOS+X technology comes to play to remedy the aforementioned obstacles. Given the data retention and inherent energy advantages of the magnetic-based logic and memory [23, 24], the use of magnetic tunneling junction (MTJ), a hybrid technology, has been the focus of research in the past decades. The promising developments of this technology within the past decade can open new doors to designing tightly coupled logic and non-volatile device circuits to overcome the above-mentioned limitations of CMOS-only technology.

Tunnel magnetoresistance (TMR) in MTJ was first discovered by Julliere in 1975 in Fe/GeO/Co junction [25]. As demonstrated in Fig. 1-2, Julliere noticed that the resistance across the MTJ has a high value when the magnetization orientation of the two layers is antiparallel, while the minimum resistance is observed in the parallel orientation. It may be noted that in parallel orientation a higher density of state (DOS) is available for electrons with opposite polarization. Therefore, by flipping the free magnet from parallel to anti-parallel orientation, the

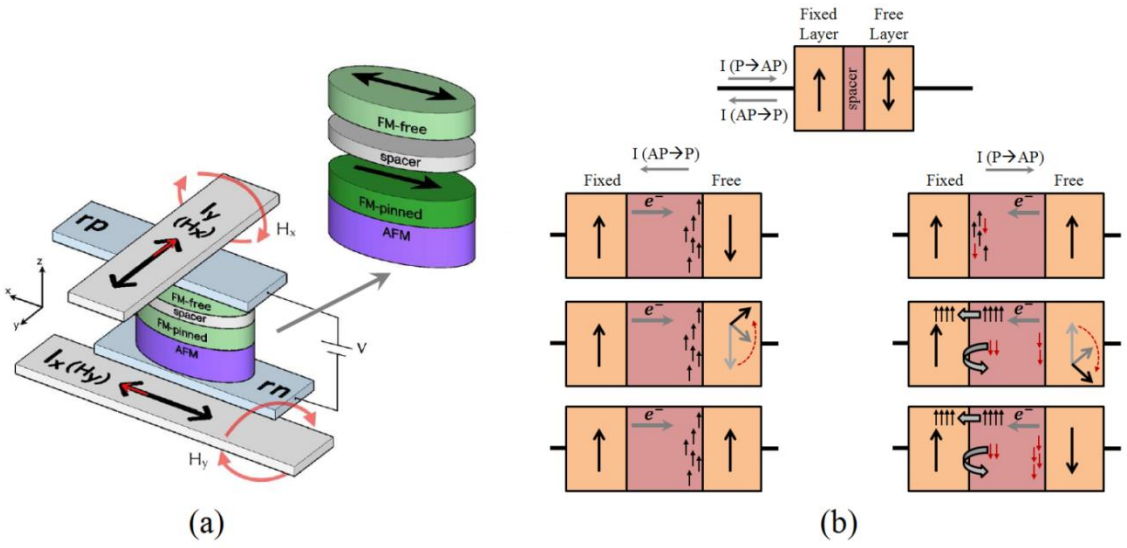

Figure 1-3 - Demonstration of (a) field induced magnetization switching [36] and (b) switching based on the spin transfer torque exerted on the free layer

resistance state of the MTJ can change. These states, high and low resistance, denote the binary logics 0 and 1 in a memory cell. Soon after the discovery of TMR, this phenomenon became the fundamental of magnetic random access memory (MRAM) [26-28]. It is theoretically shown that charge based logic has the switching energy limit of *NkTln(1/p)* where *N* is the number of charge carriers, *T* is the operating temperature, and *p* is the bit error probability [23]. However, for a magnetic based memory this number lowers to *kTln(1/p)* due to the magnetic coupling. Therefore, by theory, magnetic storage devices are expected to be way more energy efficient than their charge-based peers. Unfortunately, conventional magnetic memories use electrical current flow for their read/write operations which eventually nullifies the energy superiority discussed earlier. Therefore, although MRAM looked appealing at the first glance and attracted a lot of attention in research labs, industry did not warmly welcome it due to its low energy efficiency, area overhead, and speed limitations. Even the recent works [29, 30] in literature still fail to fully compete with CMOS peers [31].

Two methods are conventionally proposed for switching the state of the MTJ. Field induced magnetization switching (FIMS) uses the external magnetic field due to a current flow through a neighboring wire. This method consumes a lot of energy. Due to the high current values, the transistors need to be wide and the MTJs need to be placed far apart to avoid inter-cell magnetic field interference. Another method of magnetization flipping, called spin transfer torque (STT) flipping, uses spin-polarized current flow through the device, and therefore, is more scalable with CMOS technologies. Both methods are demonstrated in Fig. 1-3. The STT-MTJ, itself, has three main sub-methods:

i) *Conventional in-plane STT [32]*: The orientation of the magnetic layer's magnetization vectors is parallel to the plane of the MTJ. This method is the first proposed STT method and is much more energy efficient compared to the FIMS. However, the required current is still far beyond the theoretical limits for the magnetic logic. The current requirement for this method is a few hundreds of micro-amperes and the delay can be from few nano-seconds to a few tens of nano-seconds.

ii) Perpendicular-to-plane STT [33]: In order to make the previous method more energy-efficient, the magnetic orientation can be perpendicular to the plane. The current requirements for this method is lower than the conventional STT and can be as low as few tens of micro-amperes for few nano-seconds of switching delay.

iii) Domain Wall Magnet STT [34]: The DWM STT is a recent technology improved for more energy efficiency. A long magnet is placed in between two pinned magnetic layers. With a few microamperes of spin-polarized current flow, the domain wall can move from one end to another leading to the change of the free layer's magnetization orientation. Due to the long shape of the DW, the energy requirement is much lower.

However, this higher energy efficiency comes with a lower noise margin, which is a drawback of the DWM. The low energy barrier and very low current requirement can make DWM vulnerable to noises and fluctuations in integrated circuits. It also requires complicated design and fabrication approaches. Alternative methods are proposed to avoid the noise vulnerability in expense of a much more complicated cell design [35].

In order to overcome the energy and reliability issues of the FIMS and STT, alternative approaches can be taken. The electric-field-assisted switching of the MTJ has been proposed recently [37-39]. This approach, which manipulates the coercivity of the magnetic layers, is usually employed in perpendicular-to-plane MTJs. Although it is shown that the use of electric field at the interface of MgO/ CoFeB can be energy efficient, it still requires an external bidirectional magnetic field to assist with the switching. Creating this field can be power consuming, might require complicated design procedures, and might lead to field interferences, leading to limited scaling. In order to maximize the energy efficiency, the amount of charge

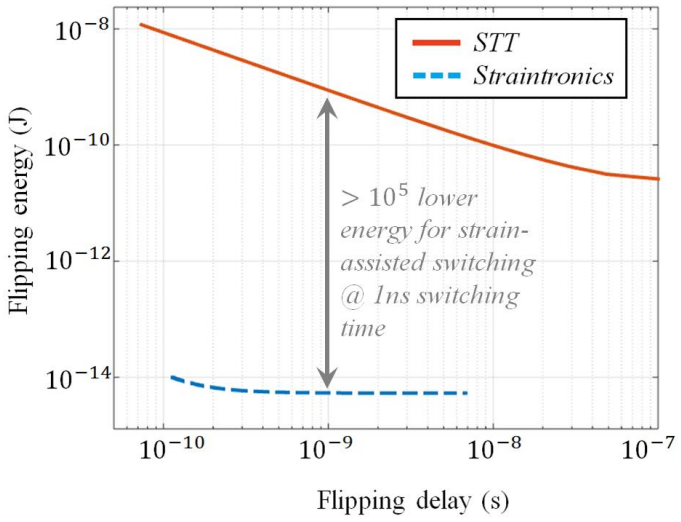

Figure 1-4 - A comparison between the energy-delay tradeoff of STT MTJ and straintronics MTJ; for 1ns switching time, straintronics can be 1000X more energy efficient

required to switch the state of the MTJ should be minimized. To this end, straintronics, as an alternative energy efficient method to switch the state of the MTJ, is proposed recently [40-44]. The use of voltage pulses instead of static current makes the straintronics device highly energy efficient as demonstrated in Table I. Interestingly, it is worthwhile to observe the energy-speed trade-off of the straintronics MTJ and its STT peer. The MTJ switching delay, t_{sw}, in a STT-MTJ is expressed using the current-delay equation [45], $t_{sw}^{-1} = (\alpha\gamma/\ln(\pi/2\theta_i))(H + H_k + 2\pi M_s)\times(I/I_C - 1)$, where, I is the current passing through the device, I_C is the critical switching current, H and H_k are external and anisotropy fields, respectively, M_s is the saturation magnetization of the free layer, α is the Gilbert damping factor, γ is the gyromagnetic ratio, and θ_i is the initial magnetization angle due to thermal fluctuations. Given the high requirements of current for STT switching (in the order of few hundreds of micro-ampere for in-plane MTJ and few tens of microampere for perpendicular-to-plane MTJ), fast switching will require high energy investments, as demonstrated in Fig. 1-4. This trade-off is much less severe for straintronics devices with the same thermal stability, where, the application of a voltage slightly higher than the critical voltage, switches the magnetization state. Switching delays, as fast as few hundreds of pico-seconds, can be accomplished by merely investing near femto- joule energies.

This thesis focuses on analysis, modeling, design, and system implementation of straintronics-based energy efficient MRAM and applications beyond data storage. The first step is to perform an in-depth analysis on the static and dynamic behavior of the device. Such studies along with the study of the effect of stress on magnetic susceptibility of the device are published in our recent work [43]. Next, to increase the accuracy of the model, the effect of temperature variations and thermal noise on the device's behavior are studied, the results of which are reported in our recent publication [46, 47]. Mathematical calculations on the dynamic behavior

of the device are performed [42, 43, 48] to derive a compact liberal model for fast simulation of large-scale systems. Comprehensive and liberal models of the straintronics MTJ are developed, the former being suited for accurate simulation of the device's behavior against stress, temperature, material properties, etc., while the latter being meant for fast simulation of top level chips.

Highlighting the applications of the straintronics devices by combining such devices with peripheral CMOS circuitry is another goal of the research. Design of a proof-of-concept 2 kilo-bit nonvolatile straintronics-based memory was introduced in our recent work [42]. Exploiting the unique features of straintronics devices in other applications comes next. Developing a true random number generator (TRNG) that exploits the metastable state of the stressed straintronics device, and working toward the design of straintronics-based neurons are among the recent accomplishments. Minimizing the change required to switch the state of the magnetic logic brings ultimate energy efficiency to such applications.

While many theoretical milestones are accomplished in strain-assisted switching, practicality of this emerging technology is debated. Recent attempts to practically prove the concept led to negligible success rates with low endurance [49]. In an attempt to uncover the possible sources behind this failure, the effect of fabrication imperfections are inspected by analyzing the aftermath of axis misalignment between the piezoelectric and the nanomagnet, the results of which are highlighted in the last section.

The rest of the thesis is organized as follows. Section II introduces the concept of straintronics switching and the intrinsic magnetic energies of the free layer of the MTJ. The effect of stress on the magnetic energy of the device, via the magnetostriction property of the free layer is

introduced. Section III discusses the modeling of the dynamic behavior of the straintronics MTJ. The tensor-based analysis and the approximate solution to the magnetization dynamics, which are the backbone of the compact liberal model for fast simulation of the large systems, are discussed. Section IV is dedicated to the study of the effect of temperature and thermal noise on the device's behavior, the latter being a crucial metric in straintronics switching. Section V introduces our recently published straintronics-based magnetic random access memory (STR-RAM). The read and write methodologies and the advantages of the STR-RAM compared to the present magnetic and CMOS memories are highlighted in this section. Section VI highlights the straintronics-based true random number generator (TRNG) in order to demonstrate the applications of this futuristic technology beyond data storage. Finally, Section VII discusses the effect of naturally occurring process variations on the switching mechanism of the device.

CHAPTER 2: THE STRAINTRONICS MAGNETIC TUNNELING JUNCTION

For decades, a combination of magnetostriction and piezoelectricity has been used in order to generate an electric voltage when the device is subject to an external magnetic field or vice versa [50-52]. This is done by interfacing a magnetostrictive layer and a piezoelectric layer (PZT) so as to transfer mechanical stress between the layers. Most of the works in this area focus on the use of the magneto-electric effect by sensing a voltage change across PZT as a result of the magnetization changes in the magnetostrictive layer as shown in Fig. 2-1a. This can be widely used in sensor design. Recently, the principle of using an applied voltage across PZT to assist with the flipping of the magnetization vector in a magnetostrictive layer has been the subject of academic research [40-44]. This is the basis of the straintronics principle, which is used to avoid

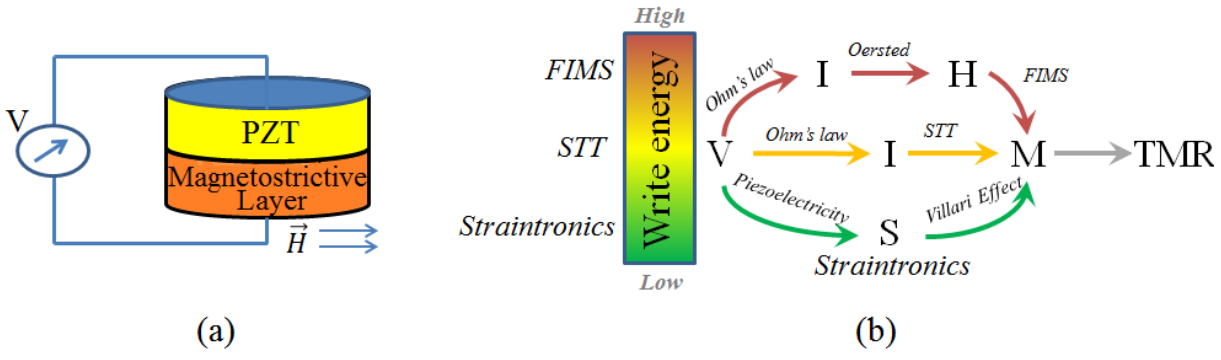

Figure 2-1 – (a) Demonstration of the magneto-electric effect; the magnetic field alters the shape of the magnetostrictive layer, leading to compression or expansion of the PZT, and therefore, a voltage is detected across the device, (b) Using piezoelectricity and Villari effect (inverse magnetostriction), high energies of FIMS and STT approaches are avoided. V: voltage, I: current, H: magnetic field, S: strain, M: magnetization

high static currents in FIMS and STT while switching the MTJ's state. This establishes a bridge to get closer to the theoretical energy limit of magnetic logic discussed earlier, as demonstrated in Fig. 2-1b.

Although straintronics has attracted a lot of research attention recently, most of the focus has been on the proof of concept and single magnet flipping. In order to be able to exploit straintronics in ubiquitous ICs, PZT needs to be incorporated with the MTJ. In this section we thoroughly explore the static behavior of the PZT-MTJ straintronics device in order to establish a unique model that can be used to interface the straintronics MTJ (STJ) with CMOS circuitry in ICs. Different magnetostrictive material with extremes in terms of magnetostriction expansion at saturation, Gilbert damping factor, and saturation magnetization are analyzed.

We will first introduce the principle of straintronics by going through the steps of magnetization flipping in the device. Next, the intrinsic and stress energies that act on the straintronics device will be introduced and the concept of energy barrier will be discussed. Lastly, we will investigate the effect of stress on different magnetostrictive materials by updating the susceptibility model by Nagata [53] for our ferromagnetic materials. The model developed in this section analyzes the magnetostrictive effect in detail and shows how the energy barrier of the straintronics device vanishes as a uniaxial stress is applied across the device.

A. The straintronics-based magnetic tunneling junction

Fig. 2-2 shows the physical view of a STJ comprising an interface of piezoelectric material with a free layer of the MTJ. The binary storage unit, MTJ, is formed by placing a tunnel barrier and a small pinned layer on top of the free layer as already discussed in Fig 1-3. The MTJ is modeled as a variable resistance. The PZT, placed on top of the MTJ, can be modeled as a parallel plate capacitance. The fringing effects are ignored in this model due to the large plane

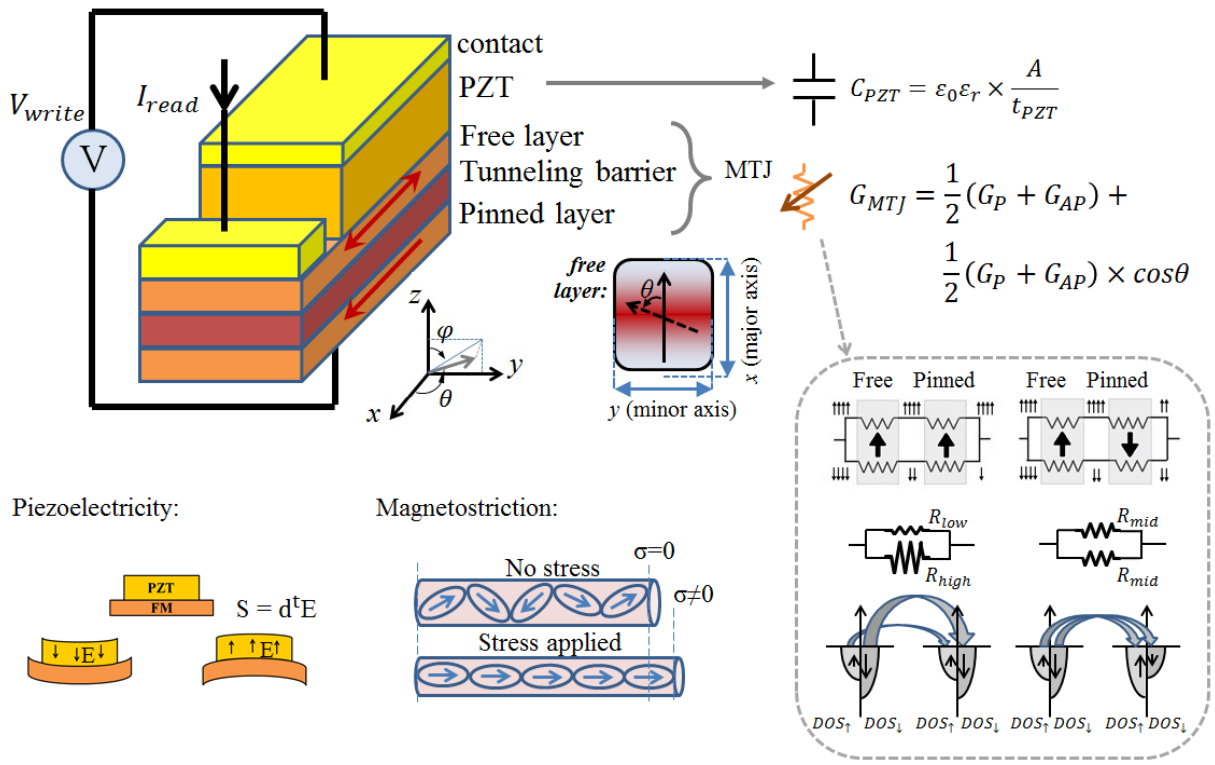

Figure 2-2 - The straintronics device, its equivalent electric model, with the piezoelectricity and Villari effect demonstrated

interface of the PZT and the free layer. Hence, the STJ has an equivalent electrical model of a resistance-capacitance (RC) circuit. The PZT in the STJ is comprised of Lead-Zirconate-Titanate ($Pb(Zr,Ti)O_3$). Unless specified, cobalt is the primary choice for the free layer for our simulations in this section. The STJ is a cylindrical rectangle (sometimes it has the shape of an ellipse, like in Fig. 2-1). having major and minor axes of $a = 205\,nm$ and $b = 195nm$, respectively. The thickness ratio of the PZT to the free layer is $40\,nm/10\,nm$ providing a large plane interface in order to ensure a perfect transfer of strain [40, 54]. The values of a and b are chosen such that the free layer acts as a single-domain nanomagnet [55]. High endurance of the PZT can be achieved since the applied pulse across the PZT is unipolar [56].

B. The magnetic energies and magnetization flipping based on the straintronics principle

In the absence of any external stress, the free layer's magnetization vector settles along the major axis due to the energy minimum. We can detect the magnetization state of the device (P or AP) by sending a current through the MTJ and sensing the resistance level.

An applied voltage across the PZT generates an electric field that leads to a strain, S, which appears as a change of length, L, since $S = \Delta L/L$. This physical length change of the PZT layer transfers a mechanical energy to the free magnet. Depending on the polarity of the applied voltage, the magnetostriction effect can create an energy minimum along the *y*-axis (minor axis), allowing the magnetization to rotate freely towards this axis. We will now explain the switching steps in detail:

a. E-Field generation

Given the equivalent RC model of the device in Fig. 2-2, a voltage applied across the device generates an electric field, $E = \frac{V_a}{d}$, where V_a is the supply voltage, and d is the thickness of the PZT. MTJ can be modeled as a variable resistance, and PZT can be modeled as a parallel plate capacitance. The MTJ's conductance is defined as [46]:

$$G_{MTJ} = \frac{1}{2}(\mathrm{G_P} + \mathrm{G_{AP}}) + \frac{1}{2}(\mathrm{G_P} + \mathrm{G_{AP}}) \times \cos\theta \qquad (2\text{-}1)$$

where, $\mathrm{G_P}$ is the high conductance state (low resistance), in which free and pinned layers have parallel magnetization orientation; G_{AP} is the low conductance state (high resistance), in which they have parallel orientation; and θ is the angle of the magnetization vector of the free layer with respect to the major axis.

b. Strain generation due to piezoelectricity

The relationship between the *E*-field and its resulting strain is demonstrated by the modified Hooke's law for piezoelectricity:

$$\{S\} = s\{\sigma\} + d^t\{E\} \tag{2-2}$$

where, s is the compliance matrix, σ is stress, and d is the 3×3 piezoelectric effect's tensor. We use Lead-Zirconate-Titanate as the piezoelectric layer, in which the d_{31} coefficient converts the electric field along the *x*-axis to a strain in the *y*-*z* plane.

The PZT is chosen to be four times thicker than the free nano-magnet (NM) while keeping a large plane interface between the two layers. This assures that the strain can almost completely transfer to the NM.

c. Stress anisotropy in the NM due to magnetostriction

In the absence of stress, the intrinsic magnetic energy of the device is mainly dominated by shape anisotropy and uniaxial anisotropy. The total intrinsic magnetic energy of the free layer is given by:

$$E_{int-mag}(\theta,\varphi) = \frac{\mu_0}{2} M_s^2 N_{sh}(\theta,\varphi) + K_u \sin^2\theta \tag{2-3}$$

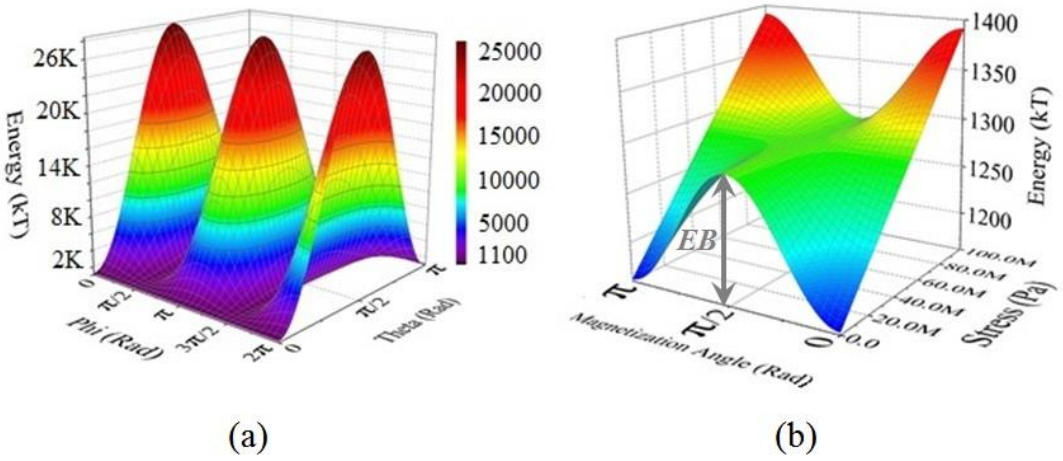

Figure 2-3 - (a) The free layer's intrinsic magnetic energy as a function of the magnetization vector's orientation and (b) Energy barrier vanishes as the applied voltage across the device increases

where, the first term indicates shape anisotropy energy and the second term is the uniaxial anisotropy energy. In the above equation μ_0 is the permeability of vacuum; M_s is the saturation magnetization of the magnet; and K_u is the uniaxial anisotropy coefficient. $N_{sh}(\theta, \varphi)$ is the demagnetization factor, which assumes its maximum and minimum along the z-axis and x-axis, respectively, and has a saddle point along the y-axis. In fact, N_{sh} can be defined as $N_{sh} = N_{zz}\cos^2\theta + N_{yy}\sin^2\theta\sin^2\varphi + N_{xx}\sin^2\theta\cos^2\varphi$. The parameters N_{xx}, N_{yy}, and N_{zz} are shape dependent parameters. Typically, for a thin layer, we have: $N_{xx} >> N_{yy},\ N_{zz}$. When the device is a cylindrical rectangular, these parameters are defined by the following expressions, in which a, b, and l are the magnet's major axis, minor axis, and thickness:

$$N_{zz} = \frac{\pi}{4}\frac{l}{a}\left(1 - \frac{1}{4}\left(\frac{a-b}{a}\right) - \frac{3}{16}\left(\frac{a-b}{a}\right)^2\right) \quad \text{(2-4a)}$$

$$N_{yy} = \frac{\pi}{4}\frac{l}{a}\left(1 + \frac{5}{4}\left(\frac{a-b}{a}\right) + \frac{21}{16}\left(\frac{a-b}{a}\right)^2\right) \quad \text{(2-4b)}$$

$$N_{xx} = 1 - (N_{yy} + N_{zz}) \quad \text{(2-4c)}$$

The free layer's magnetic energy level is therefore, a function of the magnetization orientation, which is simulated and visually demonstrated in Fig. 2-3a. The shape anisotropy will force he magnetization to stay mainly in the $x - y$ plane. Furthermore, within this plane, there is an energy barrier between the minor axis and the major axis of the device, as demonstrated in Fig. 2-3b (at *Stress = 0*). This makes the parallel and antiparallel orientations, the *preferred* orientations of the free layer's magnetization vector in the absence of an external stress. It should be noted that the energy barrier is material dependent and among the five simulated materials in Fig. 2-4, Nickel shows the lowest energy barrier due to its low M_s value while Galfenol has the highest level of energy barrier mainly due to its high M_s.

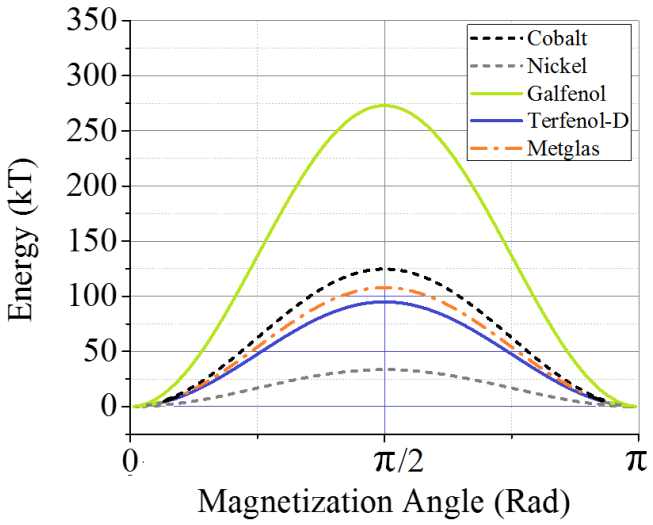

Figure 2-4 - Different material used as the free layer demonstrate different energy barriers; Galfenol has the highest EB due to the dominance of its saturation magnetization in the shape anisotropy, while Nickel has the lowest EB given its low saturation magnetization value

When a stress, σ, is applied to the magnetostrictive material, the stress anisotropy energy density, E_σ, due to the Villari effect, is given by:

$$E_\sigma = \frac{3}{2}\lambda_s \sigma \sin^2 \theta_\sigma \tag{2-5}$$

where, λ_s is the magnetostriction expansion at saturation, and θ_σ is the angle between the magnetization vector and the minor axis. As mentioned previously, when $\sigma = 0$, the magnetization vector tends to retain its orientation along the major axis (P orientation state or AP orientation state) due to the energy barrier. As we apply stress, the energy barrier reduces as demonstrated in Fig. 2-3b. At some stress value, called critical stress, the energy barrier vanishes. For Cobalt as the NM with our selected device geometries, this value is $\sigma_{critical} = 54.5$ MPa. Any stress higher than the critical stress forces the magnetization vector to rotate and then align itself along the minor axis. If the duration of the applied stress is within *successful pulsewidth* (analyzed in detail in Sections III and V), the magnetization vector will continue to rotate and settle at the opposite orientation of the starting state. This is the principle of the magnetization vector's flipping due to straintronics. For a clearer understanding of the readers,

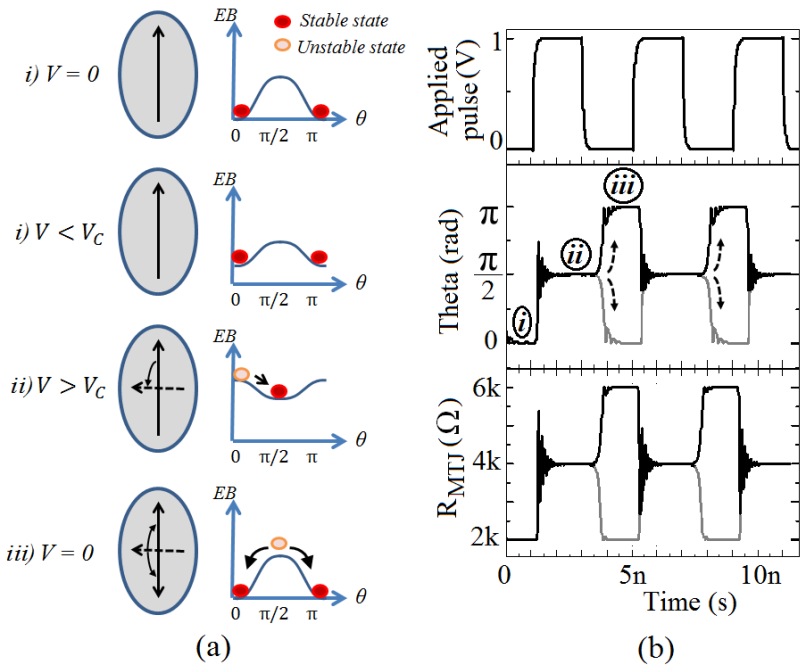

Figure 2-5 - Demonstration of magnetization flipping in a straintronics device; when the voltage reaches the critical value, the magnetization tends to settle along the minor axis. If the voltage is retained, the magnetization settles along the minor axis, leading to a metastable state upon the removal of stress. However, the dynamics of the magnetization assures a certain pulsewidth, called successful pulsewidth (analyzed in Section III), within which, the magnetization can successfully rotate to the opposite state

the steps of magnetization flipping in a straintronics device are visually demonstrated in Fig. 2-5.

C. Flipping of the magnetization vector due to uniaxial stress

The elimination of the energy barrier in a straintronics device is due to the magnetostrictive response of the free layer to the applied stress. A uniaxial stress will manipulate the directional magnetic susceptibilities of the free layer (and therefore, manipulating $N_{sh}(\theta,\varphi)$), reducing its parallel magnetic susceptibility, $\chi^{||}$, while slightly increasing the perpendicular susceptibility, $\chi^{\perp}$, as predicted by [43, 53]:

$$\chi^{||}(\sigma) = \frac{\chi_0}{1+\beta\sigma} \tag{2-6}$$

$$\chi^{\perp}(\sigma) = \frac{\chi_0}{1+\sqrt{k^2+\frac{1}{4}\beta^2\sigma^2}-\left(k+\frac{1}{2}\beta\sigma\right)} \tag{2-7}$$

The parameters β and k depend on material properties and are given as follows:

$$\beta = \frac{3\lambda_s}{\mu_0 N_{sh} M_S^2 + \frac{4K_u}{3\pi}} \tag{2-8}$$

$$k = \frac{\frac{4K_u}{2\pi}}{\mu_0 N_{sh} M_S^2 + \frac{4K_u}{3\pi}} \tag{2-9}$$

The values of β and k for our magnetostrictive materials range between 10^{-9}~10^{-7} and 10^{-4}~10^{-2}, respectively. According to (2-6) and (2-7), parallel susceptibility decreases and approaches zero for very high values of stress. Perpendicular susceptibility, however, increases and reaches a final value for high values of stress. Since the value of k is very small, at high values of stress, Taylor series approximations can be applied to obtain: $\chi^{\perp}(\sigma)|_{\sigma\to\infty} = \quad 1 + k$.

Five magnetostrictive materials are analyzed in this section: Nickel with a low M_S; Cobalt with a low Gilbert damping factor; Metglas with a high Gilbert damping factor and a low λ_s; Terfenol-D with a high λ_s; and Galfenol with a high M_S and a relatively high λ_s. The values of

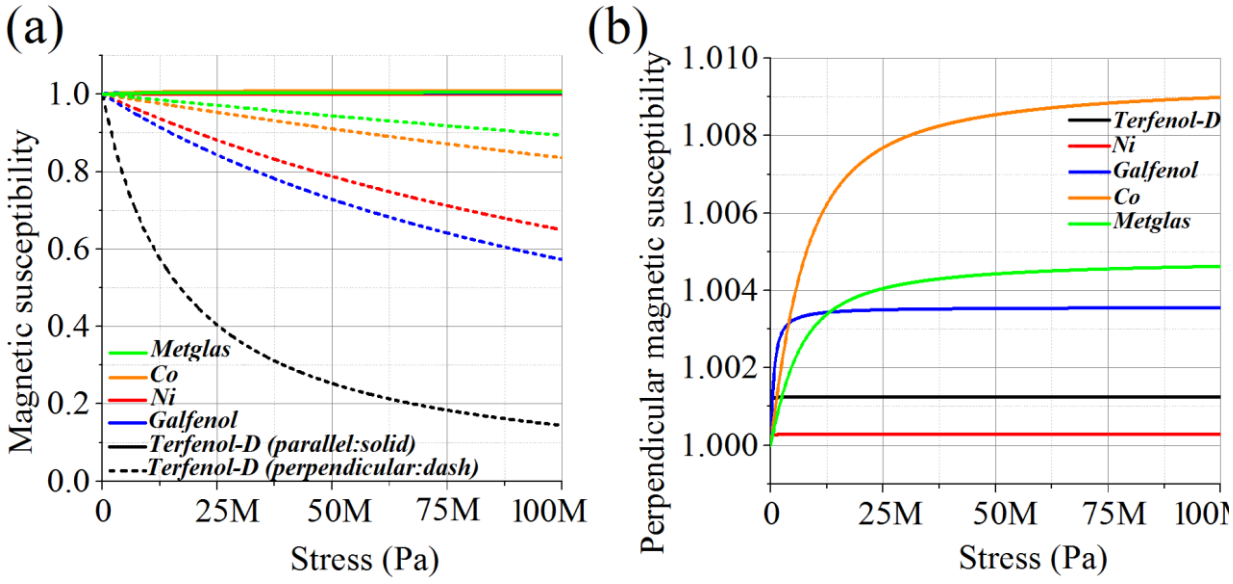

Figure 2-6 - (a) Directional magnetic susceptibility vs. applied stress for different magnetostrictive materials. Values are normalized to χ_0, (b) Perpendicular component of magnetic susceptibility shows different saturation levels for different materials

these parameters for different materials [4, 57-60] are listed in Table 2-1. Given these parameters and by using (2-6) and (2-7) we can obtain the directional susceptibilities of different magnets when a stress is applied across the device. This is plotted in Fig. 2-6a, where the values of susceptibilities are normalized to χ_0. Terfenol-D shows the fastest drop in the value of $\chi_{v||}$ due to its high magnetostriction expansion at saturation. Metglas, on the other hand, shows a slow reduction of $\chi_{v||}$ since it has a very small magnetostriction expansion at saturation. Due to the negligible variations of $\chi_{v\perp}$ compared to $\chi_{v||}$, the dependency of $\chi_{v\perp}$ on stress is portrayed in Fig. 2-6b to show the final value of perpendicular susceptibility for different materials. Nickel, Tefenol-D, and Galfenol reach the final value faster since the value of k is much smaller for these materials. The values of directional susceptibilities for different materials at $\sigma = 100MPa$ are given in Table 2-2.

The intrinsic magnetic energy of the free magnet is mainly due to the shape anisotropy energy, E_{sh}, and the uniaxial anisotropy energy, E_u. In the absence of stress, magnetization tends to align itself along the major axis since it is the intrinsic magnetic energy minimum as already shown in Fig. 2-3. As we apply stress on the free layer, $\chi_{v||}$ starts to decrease, while $\chi_{v\perp}$ increases slightly. This leads to an increased shape anisotropy energy along the major axis and decreased shape anisotropy energy along the minor axis. This change continues until the total magnetic energy barrier between the major axis and the minor axis vanishes.

Table 2-1 - Material properties of different magnetostrictive materials simulated in this section

Property	Description	Terf-D	Nickel	Galfenol	Cobalt	Metglas
$M_S(kA/m)$	Saturation magnetization	800	484	1300	800	800
$K_u\ (J/m^3)$	Uniaxial anisotropy coefficient	60	5	400	450	230
$\lvert\lambda_s\rvert\ (ppm)$	Magnetostriction coefficient	600	20	200	20	12
α	Gilbert damping factor	0.1	0.045	0.04	0.01	0.2

When a stress is applied across the magnet, the value of the shape anisotropy starts to decrease along the *y*-axis and starts to increase along the *z*-axis. This is because $E = -m.B$, $B = \mu_0(1+\chi_v)H$, and $E_{sh} = \frac{\mu_0}{2} M.H_d$, with m beign the magnetic depole moment, B being the magnetic flux density, and H_d being the the demagnetization filed. As a result we will have:

$$E_{sh,z} = \frac{\mu_0}{2}\left(\frac{1+\chi^{\perp}}{1+\chi_0}\right)M_S^2 N_z \tag{2-10}$$

$$E_{sh,y} = \frac{\mu_0}{2}\left(\frac{1+\chi^{||}}{1+\chi_0}\right)M_S^2 N_y \tag{2-11}$$

$$\Delta E_{sh} = E_{sh,y} - E_{sh,z} \approx \frac{\mu_0}{2} M_S^2 \left(N_y \frac{\chi^{\perp}}{\chi_0} - N_z \frac{\chi^{||}}{\chi_0}\right) \tag{2-12}$$

The last equality stands since $\chi_v, \chi^{||}, \chi^{\perp} \gg 1$. The energy barrier vanishes when E_{tot} reaches zero. Since $E_{u,z} = K_u$ and $E_{u,y} = 0$, we will have:

$$\left\{\frac{1}{2}\mu_0 M_S^2 \left(N_z \frac{\chi_{\perp}(\sigma)}{\chi_0} - N_y \frac{\chi_{||}(\sigma)}{\chi_0}\right)\right\} \approx K_u \tag{2-13}$$

Equation (2-13), along with (2-6) and (2-7) can numerically predict the critical stress, for which the intrinsic energy barrier disappears. The values of σ_c for different materials are listed in Table 2-2. As expected, Terfenol-D shows the lowest critical flipping stress, while Metglas has the highest flipping stress.

Alternatively, the critical stress, required to switch the state of the nanomagnet can be obtained using the energy equations in (2-3) and (2-5). By equating anisotropy energies, it is concluded that:

$$\sigma_C = \frac{\left(\frac{\mu_0}{2} M_s^2 \left(N_{yy} - N_{zz}\right) + K_u\right)}{\frac{3}{2}\lambda_s} \tag{2-14}$$

The values of critical stress for different materials with the same cylindrical rectangular

Table 2-2 - Magnetic susceptibility values at 100MPa stress and critical flipping stress based on variable susceptibility model and LLG model

Simulated property	Terfenol-D	Nickel	Galfenol	Cobalt	Metglas
$\left(\frac{\chi_\perp}{\chi_0}\right)_{\sigma=100Mpa}$	1.0013	1.0003	1.0036	1.009	1.0046
$\left(\frac{\chi_\parallel}{\chi_0}\right)_{\sigma=100Mpa}$	0.145	0.650	0.573	0.836	0.895
σ_c from susceptibility model (Pa)	1.33M	14.86M	11.79M	52.33M	77.08M
σ_c from LLG model (Pa)	1.38M	14.64M	11.88M	54.45M	78.46M
V_c (V)	12m	16m	48m	65m	165m

geometry of Fig. 2-2 (where, $a = 205nm, b = 195nm,$ and $t = 10nm$) are tabulated in Table 2-2. The results, obtained from (2-14), closely follow the susceptibility model's critical stress, confirming the accuracy of the latter.

CHAPTER 3: DYNAMIC MODELING OF THE MAGNETIZATION BEHAVIOR IN THE STRAINTRONICS DEVICE

This chapter focuses on the dynamic analysis and modeling of the straintronics device. This is especially necessary for generating a model in VerilogA to interface the device with CMOS circuitry. By establishing such model, the following goals can be achieved:

- The value of the critical flipping stress (and voltage) can be obtained from the dynamic model. The results can be compared to the analytical critical stress values and the values obtained from the susceptibility model, all of which discussed in the last section.
- The dynamic model, upon completion, can be used to model the device's instantaneous resistance at any time under any stress condition. This is done through the dependency of the MTJ resistance on the magnetization state of the free layer in the MTJ as predicted by (2-1).
- The dynamic model can be used to obtain the delay values of the device. These delays include the flipping delay, also called the alignment delay, which is the time required for the magnetization under stress to switch towards minor axis, and the relaxation delay, the time needed for the magnetization to settle back along the

major axis upon removal of stress.

- The dynamic model can also be used for analyzing the device's write error and hold error probabilities when the device is subject to thermal noise.
- And lastly, the dynamic analysis creates the fundamentals of the device's modeling in VerilogA, a common coding language used in Cadence to model devices to interface with CMOS circuitry.
- By simplifying the magnetization dynamics, an analytical solution to the dynamic behavior can be obtained, through which, the dependency of delay on the applied stress and the material properties and shape can be observed. The latter can help the designer engineer the device's dimensions and stress to achieve a certain speed-energy trade-off.
- Using the aforesaid analytical approach, a compact liberal model can be developed for fast simulation of large scale systems, where, the conventional magnetization dynamics, solved numerically, becomes impractical due to complications.

The above points are the focus of this section. We will fist introduce the dynamic behavior of the device and obtain the critical equations, required for VerilogA modeling. Next, using some basic approximations on the magnetization's initial orientation, we will develop a general solution to the cumbersome numerical dynamics of the device. Using the latter, the flipping delay is analytically obtained and a compact liberal model is developed. Lastly, we will discuss the concept of *successful pulsewidth*, the amount of time required to retain a pulse across the device to assure successful flipping to the opposite state.

A. The magnetization vector's dynamic behavior predicted by the Landau-Lifshitz-Gilbert differential model

The basis of the dynamic behavior of the magnet is the famous Landau-Lifshitz-Gilbert (LLG) equation. It can be given in the Gilbert form as [61]:

$$\frac{dM}{dt} = -\frac{\gamma}{(1+\alpha^2)}(M\times H) - \frac{\gamma}{M_S\times\left(\alpha+\frac{1}{\alpha}\right)}(M\times(M\times H)) \tag{3-1}$$

where, α is the Gilbert damping factor, γ_0 is the gyromagnetic ratio, $\vec{M}$ is the magnetization vector, and $\vec{H}$ is the net effective magnetic field. The net effective magnetic field is mainly due to shape anisotropy, uniaxial anisotropy, and stress anisotropy. By expressing the net effective magnetic field in terms of the (r,θ,φ) components and by performing vector and algebraic operations, (3-1) can be turned into the following coupled equations for θ and φ angles of the magnetization vector:

$$\frac{d\theta}{dt} = \frac{\gamma_0}{1+\alpha^2}(H_\varphi + \alpha H_\theta) \tag{3-2a}$$

$$\frac{d\varphi}{dt} = \frac{\gamma_0}{1+\alpha^2}\frac{1}{sin\theta}(\alpha H_\varphi - H_\theta) \tag{3-2b}$$

where, the two factors, H_φ and H_θ, will be expressed as:

$$H_\varphi = -\frac{1}{\mu_0 V M_S}\frac{1}{sin\theta}\frac{\partial E}{\partial \varphi} \tag{3-3a}$$

$$H_\theta = -\frac{1}{\mu_0 V M_S}\frac{\partial E}{\partial \theta} \tag{3-3b}$$

where, $E = E_{sh} + E_u + E_\sigma$ expressed in (2-3) and (2-5). Regarding (2-5), it should be noted that if $\lambda_S\sigma > 0$ the stress to the magnet is tensile, while $\lambda_S\sigma < 0$ leads to a compressive stress. In this work, the direction of the applied voltage is chosen such that stress type is compressive, and therefore the magnetization vector is forced to rotate towards the minor axis under an applied

stress.

The angle between the magnetization vector and the minor axis, θ_σ, can be re-written in terms of θ and φ. Since we choose *z*-axis as the major axis in Fig 2-2, we have:

$$cos\theta_\sigma = sin\theta \times sin\varphi \tag{3-4}$$

$$E_\sigma = \frac{3}{2}\lambda_s \sigma V(1 - \sin^2\theta \sin^2\varphi) \tag{3-5}$$

By combining the energies and incorporating the effective fields together, we have:

$$H_\varphi = -\frac{1}{\mu_0 V M_S}\left(\frac{\mu_0}{2}M_S^2 V\left(N_x - N_y\right) + \frac{3}{2}\lambda_s \sigma V\right) sin\theta sin2\varphi \tag{3-6}$$

$$H_\theta = -\frac{1}{\mu_0 V M_S}\left(\frac{\mu_0}{2}M_S^2 V\left(N_y \sin^2\varphi + N_x \cos^2\varphi - N_z\right) - \frac{3}{2}\lambda_s \sigma V \sin^2\varphi + K_u V\right) sin2\theta \tag{3-7}$$

Equation (3-2) is used to obtain the instantaneous magnetization vector's angles (θ, φ) at any time with any given voltage across the STJ.

A sufficient stress will induce the magnetization vector to rotate from the major axis towards

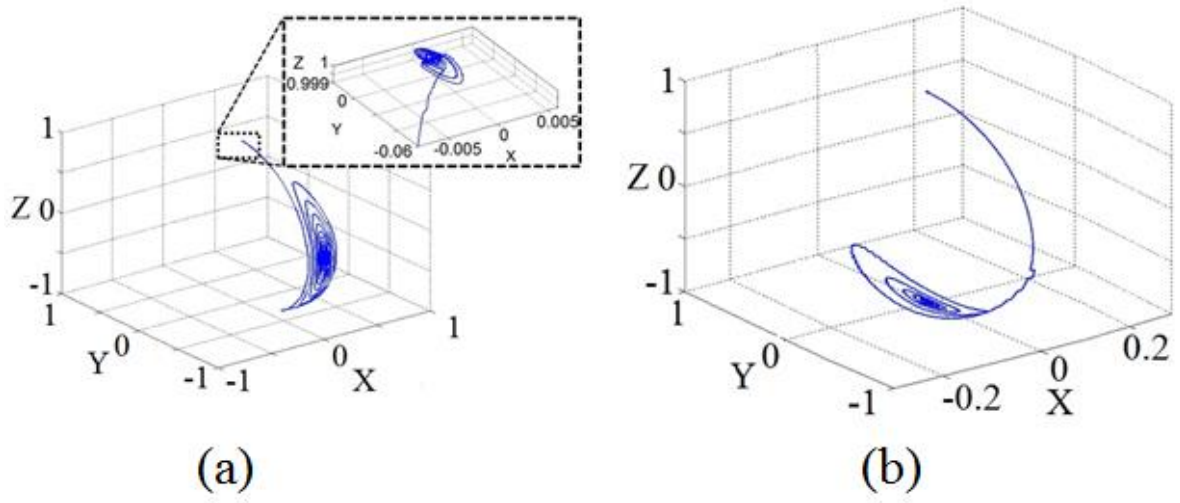

Figure 3-1 - 3D flipping of the device's magnetization vector: (a) When a high stress is maintained across the device, the magnetization vector will flip to the minor axis, while at lower stress it oscillates around the major axis due to the thermal noise, (b) Successful flipping; magnetization vector continues rotating and damps to the opposite state at $\theta = \pi$

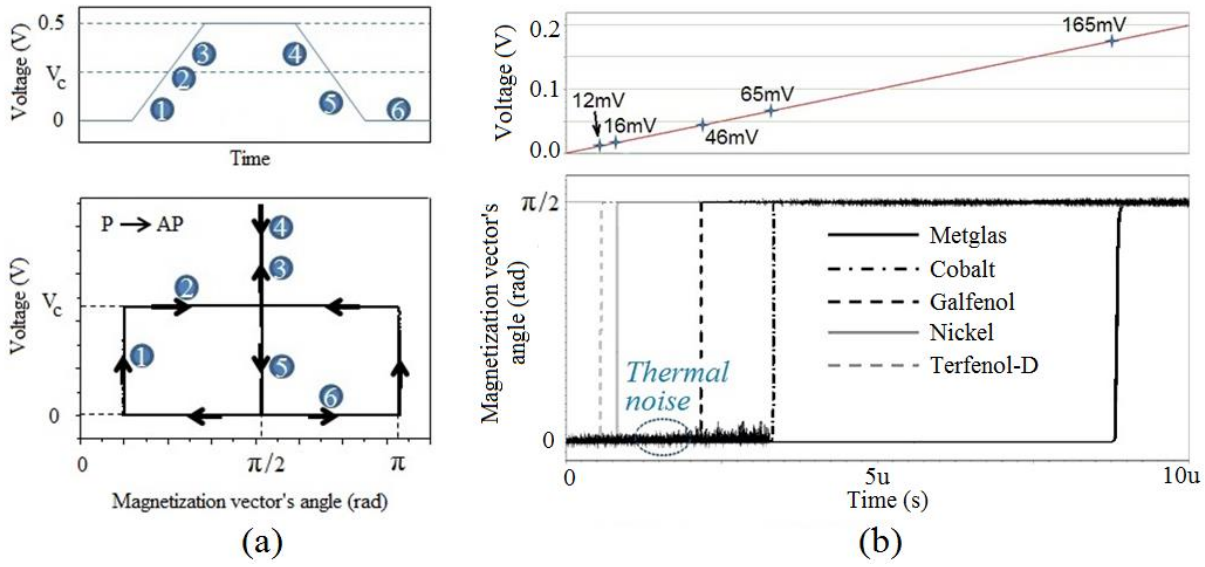

Figure 3-2 - (a) Phase diagram of the magnetization vector's flipping from parallel to antiparallel state, (b) The dynamic response of different materials to a slow ramp voltage across the device

the minor axis (also known as the "stress-easy" axis for an elliptical or rectangular magnet). If the stress is maintained, the magnetization vector will oscillate and damp at $\theta = \frac{\pi}{2}$. This is illustrated in Fig. 3-1a. It may be noted that if the applied stress is lower than its critical value, the magnetization vector fluctuates about the *z*-axis, which is exposited in Fig. 3-1a. However, if the pulse width is selected appropriately to remove the stress, the magnetization vector will continue rotating before settling at the minor axis. This switching of the magnetization vector from +*z*-axis to –*z*-axis is demonstrated in Fig. 3-1b, denoting a switching of MTJ's state from a low to a high resistance. Flipping of the magnetization vector is further illustrated using a phase diagram in Fig. 3-2a. As the applied pulse to the STJ attains the critical voltage, the magnetization vector settles at the minor axis, $\theta = \frac{\pi}{2}$. As the pulse ends, the magnetization vector continues rotating to settle at $\theta = \pi$, thereby switching to the opposite state.

We simulated different types of candidate magnetostrictive materials using the conservative model to study their dynamic behavior. Fig. 3-2b shows the dynamic response of the five selected materials when a slow ramp is applied across each device. The result shows that

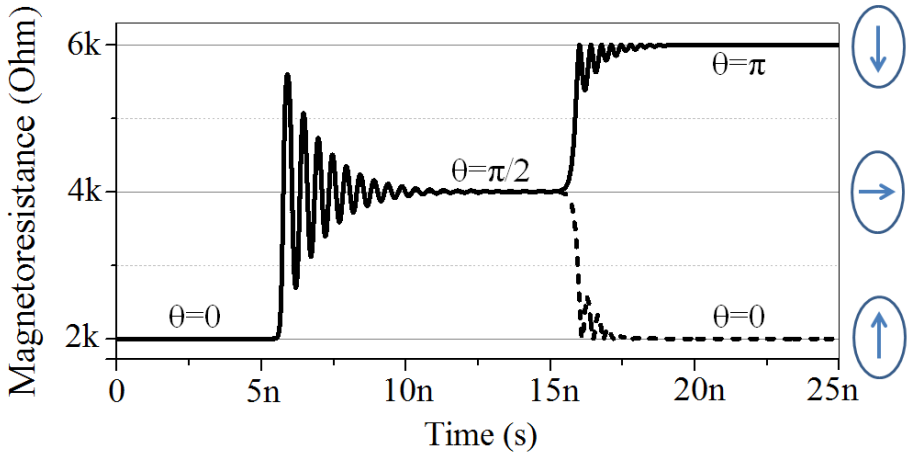

Figure 3-3 - Magnetoresistance value when a 0.2V pulse is applied at t=5ns and removed abruptly at t=15ns

Terfenol-D and Nickel tend to flip at low voltages. Consequently, these two materials are less useful in nonvolatile memory applications owing to their poor noise margin. Although Metglas has slow response time precluding its use in upper-tier memories such as caches and primary memory, Metglas with high noise immunity is a good candidate for solid-state buffer to improve the performance of magnetic hard disk drives (HDD). For general-purpose nonvolatile memory applications, Cobalt is more suitable due to its fast response and relatively high noise immunity. The material properties of these devices along with their static and dynamic results are reported in Table 3-1.

With the instantaneous value of θ, the MTJ resistance (also called magnetoresistance) in our electrical model can be calculated using (2-1). Fig 3-3 demonstrates the dynamic waveform of cobalt's magnetoresistance value as we apply a 200mV pulse at $t = 5ns$. Before the pulse is applied, the magnetization vector is relaxed along the major axis parallel to the fixed layer's magnetization orientation; as a result, magnetoresistance is low. When a voltage higher than the critical voltage (associated with the critical stress) is applied, the magnetization vector aligns along the minor axis and the resistance value settles at the mid value between high and low

Table 3-1 – Magnetic properties and dynamic and static responses of different magnetostrictive materials used as the free layer of the MTJ

	Nickel	Cobalt	Terfenol-D	Galfenol	Metglas
$Y\ (GPa)$	214	209	30	55	110
Energy barrier (kT)	35	92	110	125	273
$V_C(mV)$	16	65	12	46	165
Alignment delay (ns)	0.435	0.286	0.240	0.217	2.89
Relaxation delay (ns)	2.53	0.675	2.36	1.09	4.18

states. When the pulse is removed abruptly at $t = 15ns$, the magnetization vector will settle to either +z-axis or –z-axis, due to the energy barrier, leading to a low or high resistance value.

In order to study the straintronics principle better, we simulated the effect of the magnetostriction expansion at saturation on the alignment delay. The results are shown in Fig. 3-4a, where a 0.5V voltage is abruptly applied across the device and the alignment delay is observed. For each plot in the graph, all of the magnetic properties of a material (except for λ_s) are kept constant and different values of λ_s are simulated. The points on the graph that are associated with the materials are starred. The graph indicates that the alignment delay decreases

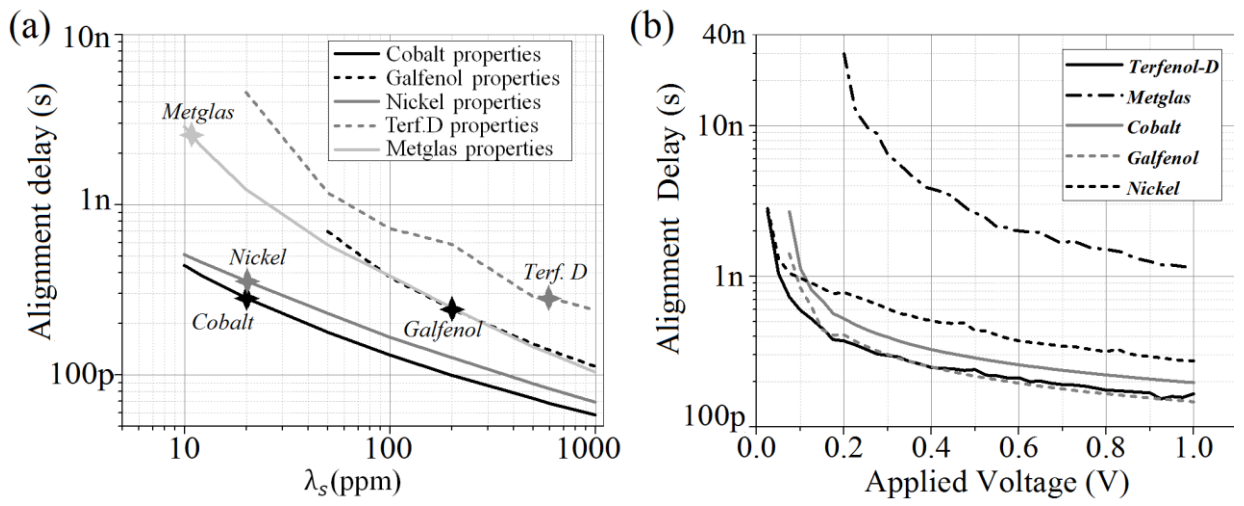

Figure 3-4 - (a) Alignment delay as a function of magnetostriction expansion at saturation. For each plot, the magnetic properties of a magnet is kept the same while sweeping its λ_s value, (b) Alignment delay of the materials decrease as the amplitude of the applied voltage increases

as λ_s increases. According to the graphs, a magnetostrictive material with magnetic properties of cobalt and λ_s of Terfenol-D (if existed) would guarantee a very fast response.

Equation (3-2) also predicts the dependency of the alignment delay on the amplitude of the applied voltage across the device, which is simulated and plotted in Fig. 3-4b for the five materials. Higher voltages lead to faster response, while voltages close to critical voltage lead to high delays.

The modeling methodology, discussed above, creates the backbone of the VerilogA model, developed for the STJ, to interface the device with CMOS peripherals and simulate the system in Cadence.

B. A general solution to the LLG dynamics: the pathway to developing a liberal model for fast simulation of large scale systems

The LLG equation, although providing an accurate solution to the magnetization dynamics, needs to be solved numerically to obtain the dynamic status of the strained MTJ . Hence, when it comes to verification of straintronics memories with more than few kilo-bytes of capacity [42] using the LLG-based models might require many hours of simulation time even on multi-core processors. When it comes to such large circuits and systems, designers usually tend to employ liberal models of the circuit elements in order to accelerate the simulation of the ultra-large scale systems at the cost of a lower accuracy. Such models are mainly used to test the system's functionality and are barely meant to report the performance or power metrics. Developing such liberal model is the focus of the rest of this chapter. Next, we obtain the analytical delay of the straintronics MTJ from the LLG dynamics using a tensor-based approach. Then, by combining it to the general solution of the LLG dynamics, we create a compact liberal model to accelerate the

simulation of the straintronics-MTJ. The general solution to the LLG dynamics, provided in this work, also provides an understanding on the damping behavior of the nanomagnet under stress and the effect of applied stress level and material properties on the settling time of the magnet. The latter will help the device engineers with the selection of the material and applied stress in order to obtain a certain settling speed of the magnetization. The tensor-based approach, besides leading to the delay analysis, provides understanding on the static response and critical flipping voltage of the strained nanomagnet, and gives insights on the inter-exchangeable role of uniaxial and shape anisotropies in the free layer of the MTJ.

The magnetic energy can be expressed in terms of the internal product of the magnetic moment, $\vec{m}$, as:

$$E = M_s^2 V \vec{m}.\overleftrightarrow{T}.\vec{m}\,. \tag{3-8}$$

Tensor $\overleftrightarrow{T}$ has a diagonal form in the Cartesian coordinates, $\overleftrightarrow{T} = \mathrm{diag}(T_x, T_y, T_z)$. By introducing $\widetilde{K_u} = K_u/M_s^2$ and $\widetilde{\lambda_s} = \lambda_s/M_s^2$ we obtain:

$$T_x = \frac{1}{\mu_0}\left(\frac{\mu_0}{2}N_{xx} + \widetilde{K_u} + \frac{3}{2}\widetilde{\lambda_s}\sigma\right), \tag{3-9a}$$

$$T_y = \frac{1}{\mu_0}\left(\frac{\mu_0}{2}N_{yy} + \widetilde{K_u}\right), \tag{3-9b}$$

$$T_z = \frac{1}{\mu_0}\left(\frac{\mu_0}{2}N_{zz} + \frac{3}{2}\widetilde{\lambda_s}\sigma\right). \tag{3-9b}$$

It follows from (3-9) that shape anisotropy and uniaxial anisotropy have similar effects on the magnetization dynamics, and therefore, are interchangeable, meaning that by altering the shape

of the free layer, lack or excess of uniaxial anisotropy can be compensated to some extent. Understanding this can give the designer some degree of freedom in the choice of material and device dimensions to meet a certain static or dynamic criteria.

The easy axis corresponds to the smallest eigenvalue of $\overleftrightarrow{T}$ and is found by comparing T_y and T_z. In the absence of stress ($\sigma = 0$), we have $T_z < T_y \ll T_x$, mainly due to the shape anisotropy since $N_{zz} < N_{yy} \ll N_{xx}$, which means the magnetization prefers to stay along the major axis. As stress increases, the value of T_z starts to increase, while the value of T_y stays constant. Upon achieving the critical stress, σ_C, the relation changes and we have $T_y < T_z$, meaning that the magnetization vector now prefers to stay along the minor axis. From (3-9) it is concluded that:

$$\sigma_C = \frac{\mu_0\left(N_{yy} - N_{zz}\right) + 2\widetilde{K_u}}{3\widetilde{\lambda_s}}. \tag{3-10}$$

The critical stress in (3-10) complies with what was obtained in the last section from energy analysis, which is intuitively expected as $\overleftrightarrow{T}$ is driven from magnetic energies. Note that in obtaining (2-14), we assumed the magnetization only stays within the *y*-*z* plane. Examining (3-9a) reveals that when stress is applied T_x rises as well, meaning that the application of stress increases the magnetization's tendency to stay within its plane, confirming the aforementioned assumption.

The relationship between the applied voltage and the stress on the free layer of Fig. 2-2a should be noted here. An applied voltage, V, leads to an electric field, $|E| = V/t_{PZT}$, with t_{PZT} being the thickness of the PZT. The electric field leads to the strain, $\vec{s} = \overleftrightarrow{d^t}.\vec{E}$, with d^t being the PZT tensor with $d_{31} = 1.8{\times}10^{-10}\ m/V$ for Lead-Zirconate-Titanate, the piezoelectric material

of choice in this work. Assuming the large plane interface between the PZT and the free layer, the strain is majorly transferred to the free layer [40, 44, 54], and the stress is obtained as $\vec{\sigma} = Y\vec{s}$, with Y being Young's modulus of the free layer.

The evolution of the magnetization, $\vec{M}$, described by LLG equation, is re-expressed below:

$$\frac{\partial \vec{M}}{\partial t} = g\vec{H}_{eff} \times \vec{M} - \frac{g\alpha}{M_s}\vec{M} \times \left(\vec{M} \times \vec{H}_{eff}\right), \tag{3-11}$$

where $g = \frac{\gamma_0}{1+\alpha^2}$, with $\vec{H}_{eff} = \frac{1}{\mu_0 V M_s}\, \partial E / \partial \vec{m}$ is the effective field due to the total magnetic energies in (2-3). Due to the nonlinearity of the equation of motion, it has to be solved numerically, and hence is not practical for simulating large systems such as multi-megabyte memories. A liberal model, obtained from (3-11) can accelerate the simulations drastically. By obtaining the delay equation from the LLG dynamics, a compact liberal model can be achieved.

For a general case, assuming the time dependence of the magnetization angle, θ, in the form $\theta(t) = a_1 e^{-i\omega_1 t} + a_2 e^{-i\omega_2 t}$, with a_1 and a_2 being set by the initial conditions, we will find the exponents ω_1 and ω_2 from (3-11). Since $\vec{H}_{eff} = -\frac{1}{\mu_0 V M_s}\, \partial E / \partial \vec{m}$, we have:

$$\vec{H}_{eff} = \frac{1}{\mu_0 V M_s}\frac{\partial E}{\partial \vec{m}} = \frac{2M_s}{\mu_0}\overleftrightarrow{T}.\vec{m}\,. \tag{3-12}$$

with $\overleftrightarrow{T}$ being a diagonal tensor in the Cartesian frame defined above. In a general case, we define $\overleftrightarrow{T} = \mathrm{diag}(T_0, T_1, T_2)$, where T_k's with $k = 0, 1, 2$ are related to the diagonal matrix elements of the energy tensor, introduced in (3-8). The relation depends on the choice of the initial direction, e_0; and then e_1 and e_2 are chosen in the plane perpendicular to e_0 so that (e_0, e_1, e_2) form right-handed basis.

Assuming the initial orientation along e_0, we have:

$$g\overrightarrow{H_{eff}}\times\vec{M} = \frac{2gM_s}{\mu_0}(\overleftrightarrow{T}.\vec{m})\times\vec{m} \tag{3-13}$$

Approximating $\vec{M} \approx M_s\hat{e_0}$ in the second term of the right hand side of (3-11), the LLG dynamics can be expressed along (e_0, e_1, e_2) as:

$$\begin{pmatrix}\dot{m}_0\\ \dot{m}_1\\ \dot{m}_2\end{pmatrix} = \frac{2gM_s}{\mu_0}\begin{pmatrix}(T_1-T_2)m_1m_2\\ (T_2-T_0)m_2m_0\\ (T_0-T_1)m_0m_1\end{pmatrix} + \alpha\frac{2gM_s}{\mu_0}\begin{pmatrix}0\\ -(T_0-T_1)m_0^2m_1\\ (T_2-T_0)m_2m_0^2\end{pmatrix}. \tag{3-14}$$

Since originally $\vec{M}$ is oriented along e_0, the variations of $\overrightarrow{\Delta M}$ will be mainly composed of m_1 and m_2. Hence, the following equation should be solved to obtain a solution to the LLG dynamics:

$$\begin{pmatrix}\dot{m}_1\\ \dot{m}_2\end{pmatrix} = \frac{2gM_s}{\mu_0}A\begin{pmatrix}m_1\\ m_2\end{pmatrix}, \qquad A = \begin{pmatrix}-\alpha(T_0-T_0) & (T_2-T_0)\\ (T_0-T_1) & \alpha(T_2-T_0)\end{pmatrix}, \tag{3-15}$$

Having e^{ut} response of the magnetization, by setting $\det(uI-A)=0$ we can find the eigenvalues:

$$\begin{aligned}\det(uI-A) = u^2 + \alpha(2T_0-T_1-T_2)u + (T_2-T_0)(T_1-T_0)\\ -\alpha^2(T_0-T_1)(T_2-T_1) = 0,\end{aligned} \tag{3-16}$$

Assuming the time dependence in the form of $e^{-i\omega t}$ the above equation yields:

$$\frac{\omega_{(1,2)}}{gM_S} = -i\frac{\alpha}{2}(T_1+T_2-2T_0) \pm \sqrt{(T_1-T_0)(T_2-T_0) - \frac{\alpha^2}{4}(T_1-T_2)^2}, \tag{3-17}$$

where, the constant $2/\mu_0$ in (3-9) is incorporated into the expressions of T_k's. Once again, (e_0, e_1, e_2) are chosen based on the right hand rule with e_0 indicating the initial condition of the magnetization under analysis. Hence, when analyzing the magnetization behavior around the major axis, $(e_0, e_1, e_2) \equiv (\hat{z}, \hat{x}, \hat{y})$ and when around the minor axis $(e_0, e_1, e_2) \equiv (\hat{y}, \hat{z}, \hat{x})$.

If $\sigma < \sigma_c$, the magnetization returns to the major axis (the z-axis) monotonously or oscillating. Similarly, when $\sigma > \sigma_c$, the magnetization will travel and settle along the minor axis (y-axis) either monotonously or oscillating. Whether or not this behavior is overdamped (monotonous) or oscillatory depends on the applied stress level and material properties. Here, we will analytically find the stress levels, at which, the magnetization's behavior transitions from oscillatory to overdamped.

a) Settling back along the major axis when $\sigma < \sigma_C$

In this case, we consider the re-alignment case, where, the initial magnetization angle is along the z-axis and the magnetization is slightly deviated from the major axis. In this case $(e_0, e_1, e_2) = (z, x, y)$ and hence, $T_0 = T_z, T_1 = T_x, and\ T_2 = T_y$. If $\sigma > \sigma_C$, assuming the initial condition along the *z*-axis, the term under the square root in (3-17) is negative, and the magnetization will leave the major axis exponentially. This case is used for delay analysis in the next section. When $\sigma < \sigma_C$, the magnetization will return to the major axis. This return will be overdamped, if (3-17) is completely imaginary, or when:

$$\frac{\alpha^2}{4}(\sigma + \sigma_1)^2 > \sigma_2(\sigma_C - \sigma), \tag{3-18}$$

where:

$$\sigma_1 = \frac{\mu_0\left(N_{xx} - N_{yy}\right)}{3\widetilde{\lambda_s}}, \tag{3-19a}$$

$$\sigma_2 = \frac{\mu_0(N_{xx} - N_{zz}) + 2\widetilde{K_u}}{3\widetilde{\lambda_s}}, \tag{3-19b}$$

Note that $\sigma_C = \sigma_2 - \sigma_1$. Inequality (3-18) can be solved [48] to obtain the low-marginal stress, σ_{ML}, the margin between the oscillatory and overdamped regimes, below which the magnetization will oscillate to return to the major axis:

$$\sigma_{ML} = \sigma_C - \frac{\alpha^2}{4}\sigma_2, \tag{3-20}$$

b) Settling along the minor axis when $\sigma > \sigma_C$

We now investigate the settling along the minor axis when the stress is above critical. Assuming the magnetization is moving towards the minor axis and is preparing to settle down along this axis, we analyze the behavior around this orientation, which means $(e_0, e_1, e_2) = (y, z, x)$. Using the same methodology and solving (3-18), the high-marginal stress, σ_{MH}, can be obtained as:

$$\sigma_{MH} = \sigma_C + \frac{\alpha^2}{4}\sigma_2, \tag{3-21}$$

The effects of low and high marginal stresses are visually demonstrated in Fig. 3-5. Assuming the magnetization's initial angle, is somewhere between 0 and $\pi/2$, then: i) when $\sigma < \sigma_{ML}$, the magnetization returns to the major axis while oscillating; ii) when $\sigma_{ML} \leq \sigma < \sigma_C$, the magnetization monotonously returns to the major axis; iii) for $\sigma_C < \sigma \leq \sigma_{MH}$ the magnetization

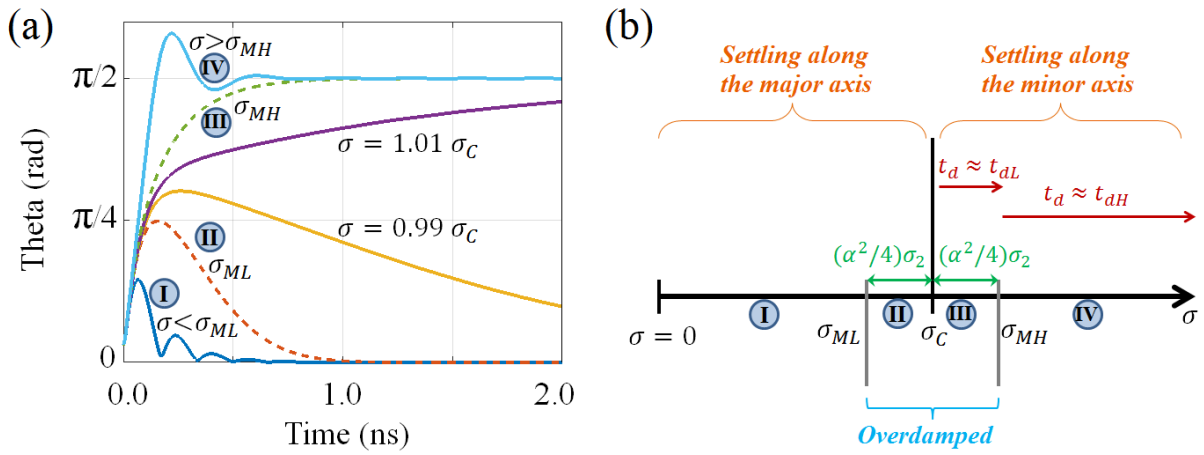

Figure 3-5 - (a) Effect of stress level on the orientation (or re-orientation) of the magnetization; when stress is below critical, the magnetization returns to the minor axis either monotonously or oscillating depending on the stress level, and when stress is above critical, the magnetization moves toward and settles along the minor axis either monotonously or oscillating depending on the stress level, and (b) A qualitative demonstration of the magnetization's reorientation and damping behavior as the stress increases, relating the regions of oscillation and monotonous damping to the dynamic figure on the left

settles along the minor axis without any oscillations whatsoever; and lastly iv) when $\sigma > \sigma_{MH}$, the magnetization will settle along the minor axis while oscillating, as portrayed in Fig. 3-5.

Observing (3-20) and (3-21), it can be concluded that:

$$\frac{\Delta\sigma_M}{\sigma_C} = \left|\frac{\sigma_{M(L,H)} - \sigma_C}{\sigma_C}\right| = \frac{\alpha^2}{4}\frac{\sigma_2}{\sigma_C}, \tag{3-22}$$

which, in the log-log form, predicts a linear dependency of $\Delta\sigma_M$ on the damping factor. This is highlighted by simulating the LLG-based numerical model in Fig. 3-6 for both low and high marginal stresses and comparing it to the analytical expectation in (3-22). The results of Fig. 3-5 and 3-6 are for Terfenol-D as the free layer and Fig. 3-6 keeps the magnetic materials of Terfenol-D while sweeping its damping factor to demonstrate the effect of α on the marginal stresses. The discrepancy in the absolute values of (3-22) versus the LLG simulations is plotted in the inset of Fig. 3-6, highlighting the accuracy of the predicted model for $\alpha < 0.1$.

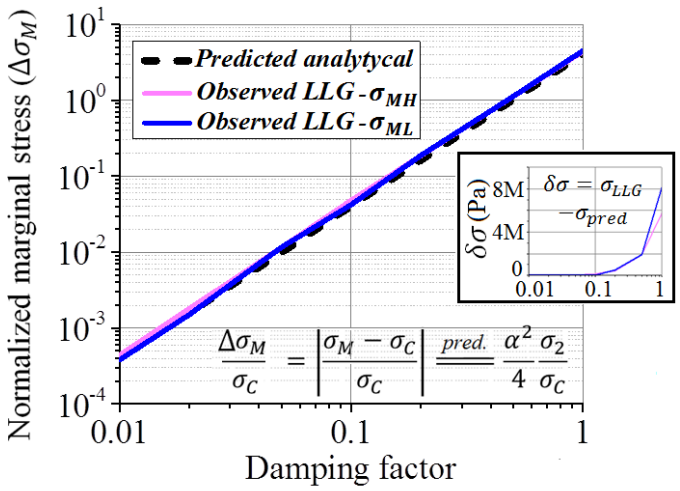

Figure 3-6 - The effect of damping factor on the normalized marginal stresses

Furthermore, Fig. 3-6 suggests that for $\alpha < 0.1$ (which is the case for most of the magnetostrictive materials), $\Delta\sigma_M \ll \sigma_C$, indicating that except for a small stress margin above critical, the magnetization will almost always oscillate to settle along the minor axis. The latter is also confirmed when looking at the critical and marginal voltages of the four simulated materials, enumerated in Table 3-2.

C. Flipping delay of the straintronics device

When $\sigma > \sigma_C$, assuming the magnetization's original orientation is along the major axis (z-axis), meaning that $(e_0, e_1, e_2) = (z, x, y)$ and hence, $T_0 = T_z, T_1 = T_x, and\ T_2 = T_y$, the term under the square root in (3-17) becomes negative and there are two imaginary frequencies $\omega_{1,2} = \pm i\Gamma_{\pm}$ with $\Gamma_{\pm} > 0$ and:

$$\Gamma_+ = gM_S\sqrt{(T_1 - T_0)(T_0 - T_2) + \frac{\alpha^2}{4}(T_1 - T_2)^2} - \frac{gM_S\alpha}{2}(T_1 + T_2 - 2T_0), \qquad (3\text{-}23)$$

The solution $\propto \exp(\Gamma_+ t)$ describes magnetization exponentially deviating from the z-axis. Defining, somewhat arbitrarily, flipping time by the relation $\theta(t_d) = \pi/4$, and taking into account that the projection of the magnetization on the x-axis is small, we obtain

$$t_d = -\frac{1}{\Gamma_+}\log\left[\frac{2H(\sigma)\frac{\delta M(0)}{M_S}}{\pi/4}\right], \tag{3-24}$$

where, $\delta M(0)$ is the initial deviation of the magnetization and in the case of the thermally-agitated initial condition[26] we have $\frac{\delta M(0)}{M_S} \approx \theta_i$. $H(\sigma)$ gives the projection of the initial state onto exponentially growing solution:

$$H(\sigma) = \frac{1}{2} - \frac{\alpha(T_1 - T_2)}{\sqrt{4(T_1 - T_0)(T_0 - T_2) + \alpha^2(T_1 - T_2)^2}}, \tag{3-25}$$

Equation (3-24) gives a general form of the delay. Next, two cases are separately considered for simplicity. First we consider the case, where, the stress is higher but close to critical, where, the two terms under the square root of (3-23) are comparable. This can be associated with the overdamped regime. Next, we consider the case where, the stress is higher than the marginal stress, where, the first term under the square root becomes significantly higher than the second term:

a) t_{dL}: Flipping delay when $\sigma_C < \sigma < \sigma_{MH}$

When stress is above critical the expression under the square root in (3-17) becomes negative and thus:

$$\frac{\omega_{(1,2)}}{gM_S} = -i\frac{\alpha}{2}\left((T_1+T_2-2T_0) \pm (T_1-T_2)\sqrt{1-\frac{(T_1-T_0)(T_2-T_0)}{\frac{\alpha^2}{4}(T_1-T_2)^2}}\right), \tag{3-26}$$

Defining $\epsilon = \frac{(T_1-T_0)(T_2-T_0)}{\left(\frac{\alpha^2}{4}(T_1-T_2)^2\right)}$ and simplifying $\sqrt{1-\epsilon} \approx 1-\frac{\epsilon}{2}$, the two answers above are:

$$\frac{\omega_{(1,2)}}{gM_S} = -i\begin{cases} \alpha T_1\left(1-\frac{\epsilon}{4}\right) \approx \alpha T_1 \\ \alpha\left(T_2-T_0+\frac{(T_1-T_2)\epsilon}{4}\right) \approx \frac{T_2-T_0}{\alpha}, \end{cases} \tag{3-27}$$

Taking into account that the time dependence is of the form $e^{-i\omega t}$ one can see that the first expression corresponds to a decaying solution and is of importance only for specific initial conditions of zero probability in the thermally-agitated case. The second expression proposes an exponentially growing deviation of magnetization. Taking into account that in the overdamped regime $\sigma \approx \sigma_C$ (since $\Delta\sigma_M \ll \sigma_C$), we can simplify (3-25) to:

$$H(\sigma)|_{\sigma\approx\sigma_C} = H_\alpha(\sigma) \approx \frac{(T_1-T_0)(T_0-T_2)}{\alpha^2(T_1-T_2)^2} \ll 1, \tag{3-28}$$

which, suggests the dependency on the voltage and the damping factor. Now since when initiating along the z-axis $T_0 - T_2 = T_z - T_y = \frac{3\widetilde{\lambda_s}}{\mu_0}(\sigma-\sigma_C)$, the delay time to reach $\pi/4$ can be estimated as:

$$t_d = t_{dL} \approx \frac{\alpha\mu_0 M_s}{3g\lambda_s(\sigma-\sigma_c)}\ln\left(\frac{\pi/4}{2\theta_i H_\alpha(\sigma)}\right), \tag{3-29}$$

b) t_{dH}: Flipping delay when $\sigma > \sigma_{MH}$

In the underdamped regime, the first expression under the square root becomes larger than the second term. In fact as the stress increases, the first term becomes more dominant. On the other hand, for most materials $\alpha \ll 1$, meaning that when stress becomes only slightly higher than critical, we have $(T_x - T_z)(T_y - T_z) \gg \frac{\alpha^2}{4}(T_x - T_y)^2$. Hence, making an aggressive approximation of negligibility of the damping factor (the legitimacy of this assumption is later confirmed using the LLG simulations), the general form is simplified to:

$$\frac{\omega_{(1,2)}}{gM_S} \approx \pm\sqrt{(T_1 - T_0)(T_2 - T_0)}, \tag{3-30}$$

Initiating along the z-axis and since $T_x \gg T_y$ and $T_x \gg T_z$ and since due to the device geometry usually $N_{xx} \gg N_{yy}, N_{zz}$, the above expression simplifies to:

$$\omega_{(1,2)} \approx \pm i\frac{g}{\mu_0}\sqrt{3\lambda_s\mu_0 N_{xx}(\sigma - \sigma_C)}, \tag{3-31}$$

The first response provides an exponentially growing response while the second is exponentially decaying. Simplifying (3-25) by assuming $\sigma \gg \sigma_C$, gives $H(\sigma)|_{\sigma \gg \sigma_C} \approx 1/2$. Hence, the flipping delay to reach $\pi/4$ can be expressed as:

$$t_d = t_{dH} \approx \frac{\mu_0}{g\sqrt{3\mu_0 N_{xx}\lambda(\sigma - \sigma_c)}}\ln\left(\frac{\pi/4}{\theta_i}\right), \tag{3-32}$$

Note that in (3-29) and (3-32), the flipping delay is defined as the 50% transition of the magnetization angle when travelling towards the minor axis. Once again since $\Delta\sigma_M \ll \sigma_C$, except

for a small region of stress above critical, (3-32) can almost always be used to predict the flipping delay.

Equations (3-29) and (3-32) suggest that the switching delay is material and stress-dependent. Fig. 3-7a demonstrates this dependency for the four simulated materials. To confirm the accuracy of the obtained delay equations, the results from the LLG-based numerical model are also plotted. It is interesting to observe that at higher stress levels, the log-log relation between the delay and the applied stress becomes fairly linear. As follows from (3-32), when $\sigma \gg \sigma_C$, we have $\log(t_d) \approx K - 0.5\times\log(\sigma)$, where K is a material and shape dependent constant.

Due to the thermal fluctuations of the magnetization vector, the flipping delay is a random quantity with a distribution demonstrated in Fig. 3-7b for Galfenol at 1 V applied voltage level. Two histograms are obtained through Monte-Carlo simulations of the analytical model in (3-32) and the LLG model. The histograms have the shapes of the logs of magnitudes of random variables with Gaussian distributions. This is due to the fact that the thermally-agitated initial

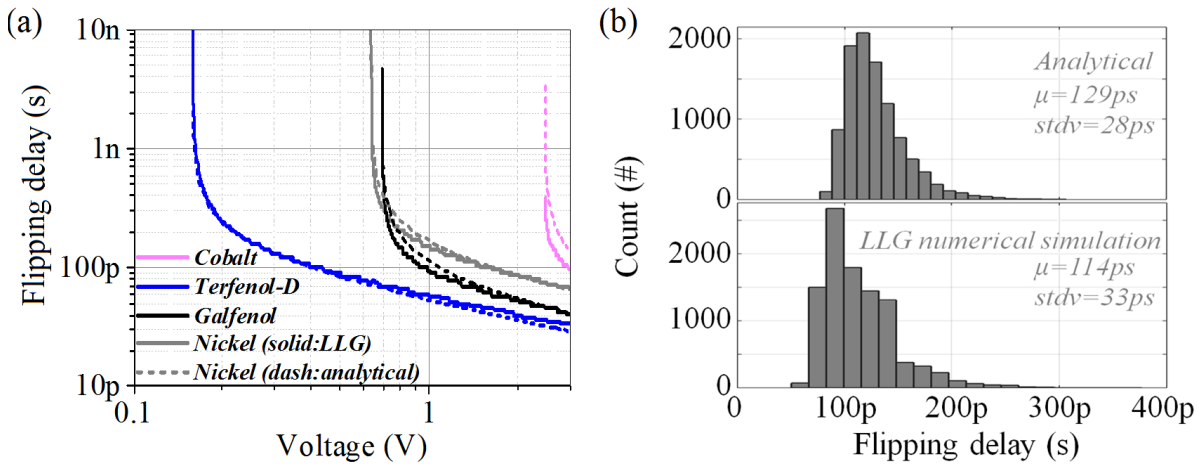

Figure 3-7 - (a) Dependency of the flipping delay on the choice of material and applied voltage; the solid lines are the result of numerical simulation and the dashed lines are predicted analytical delay developed in this work, (b) Histograms of delay on N=10000 Monte-Carlo runs for the analytical equation in (29) and the LLG numerical simulation; for each simulation, the initial angle is set to a thermally agitated random value with Gaussian distribution

magnetization angle in (3-32), has a Gaussian distribution, which will be discussed in the next section.

Equation (3-32) demonstrates no dependency of the flipping delay on the damping factor, α, which is due to the approximation in (3-17), where, since usually $\alpha \ll 1$, when $\sigma > \sigma_{MH}$ we have $(T_1 - T_0)(T_2 - T_0) - (\alpha^2/4)(T_1 - T_2)^2 \approx T_1(T_2 - T_0)$. This approximation becomes more accurate as the stress increases. In order to verify the legitimacy of ignoring α in (3-32), we simulated the numerical LLG model for the flipping delay by sweeping the voltage and the damping factor and observing the flipping delay. The results, demonstrated in Fig. 3-8a, confirm that for values of $\alpha < 0.1$, which is the case for most of the magnetostrictive materials, the delay becomes almost independent of the damping factor. A *y*-*z* projection of Fig. 3-8a for $\alpha < 0.1$, plotted in Fig. 3-8b, shows that the predicted analytical results closely follow the LLG-based behavior. Furthermore, the prediction becomes more accurate as the stress increases; and when $\sigma > 2\sigma_C$, the predicted results from (3-32) almost exactly follow the LLG simulation results. The latter is because a higher stress suppresses the effect of the damping factor in (3-17).

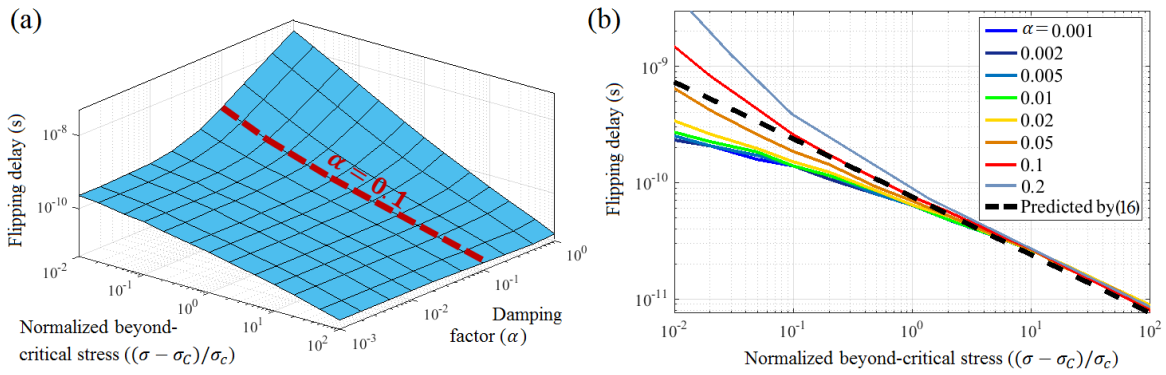

Figure 3-8 - (a, b) Investigating the effect of the damping factor on the switching delay by keeping the material properties of Terfenol-D and sweeping the applied stress and α; (a) When $\alpha < 0.1$ the delay becomes almost independent of the damping factor; interestingly, the dependency of delay on the damping factor is even less when the stress is increased well above the critical voltage, (b) planar projection of the 3D graph to clearly demonstrate that as stress increases, the predicted delay almost exactly follows the LLG simulation

The properties of the simulated materials, along with their critical switching voltage and their predicted and simulated switching delays under 3V applied voltage are enumerated in Table 3-2. Galfenol and Terfenol-D are generally considered as good candidates for memory applications due to their fast response and low to moderate critical switching voltages.

D. A compact liberal model for fast simulation of large systems

The dynamic behavior of the magnetization in the straintronics MTJ under stress can be analytical solved using (3-17) when the magnetization is settling along the minor axis. By incorporating the delay of (3-32) into the solution of the LLG dynamics in (3-17), the analytical model for the magnetization damping can be expressed as:

$$\theta(t) = \frac{\pi}{2} - \frac{\pi}{4} e^{-\zeta\omega_0(t-t_d)} \cos\big(\omega_d(t-t_d)\big), \qquad \omega_d = \omega_0\sqrt{1-\zeta^2} \tag{3-33}$$

where, ω_d is the oscillating frequency and ζ and ω_0 are the general damping factor and the natural frequency, respectively, and are given by:

Table 3-2 - Material properties of different magnetostrictive materials simulated in this section

Property	Description	Nickel	Cobalt	Terf.-D	Galfenol
$M_S\ (kA/)$	Saturation magnetization	492	1400	800	1300
$K_u\ (kJ/m^3)$	Uniaxial anisotropy coefficient	12	16	1.6	5
$\lvert\lambda_s\rvert\ (ppm)$	Sat. magnetization at expansion	20	20	600	200
α	Gilbert damping factor	0.045	0.01	0.1	0.04
$V_C\ (V)$	Critical switching voltage	0.638	2.47	0.158	0.692
$V_{MH}\ (V)$	Marginal voltage (high)	0.640	2.48	0.164	0.696
$t_d\ (ps)$	Flipping delay expected from LLG numerical simulation under 3V applied voltage	68	96	34	41
$t_d\ (ps)$	Predicted flipping delay from (29) under 3V applied voltage	66	140	29	41

$$\zeta = \frac{\alpha\left(T_z + T_x - 2T_y\right)}{\sqrt{4(T_z - T_y)(T_x - T_y) - \alpha^2(T_z - T_x)^2}} \tag{3-34}$$

$$\omega_0 = \frac{\sqrt{4(T_z - T_y)(T_x - T_y) - \alpha^2(T_z - T_x)^2}}{2} \tag{3-35}$$

Using (3-33), the dynamic response of the strained MTJ can be modeled analytically, leading to a much faster solution compared to the LLG-based numerical simulations. Simulations results on the analytical (liberal) model when the straintronics MTJ is stressed at $t = 0$ with $1V$ voltage pulse are illustrated in Fig. 3-9 and compared to the results of the LLG-based numerical simulations. The similarity of the waveforms demonstrates the capability of the liberal model for the functionality testing of the straintronics-based systems. The slight discrepancy between the graphs is the overshoot ($PO = exp(-\pi\zeta/\sqrt{(1-\zeta^2)})$), which is expected due to different general damping factors between the two models.

Due to its analytical nature, the liberal model leads to much shorter simulation times compared

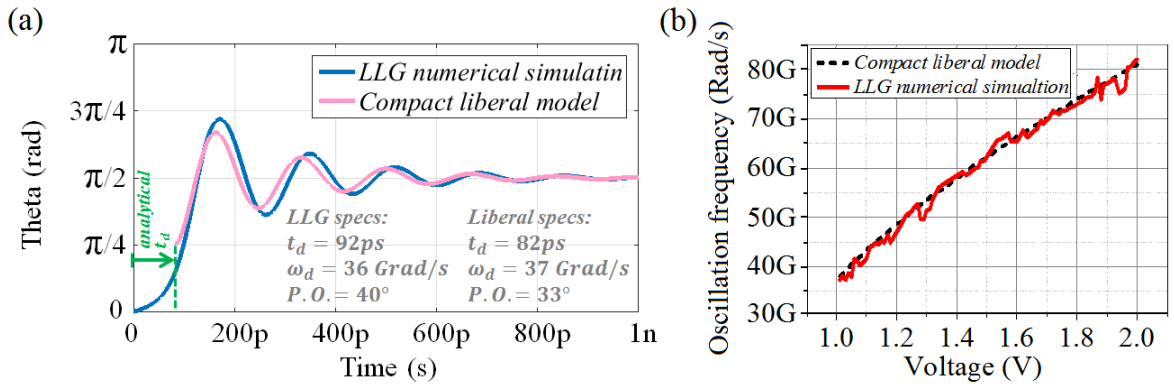

Figure 3-9 - (a) The simulation results of the liberal and conservative (LLG) models when the straintronics MTJ with Galfenol as free layer is stressed at $t = 0$ with a 1V voltage pulse. The oscillation frequencies, the overshoot values, and the delay values to reach $\pi/4$ (50-50 delay) are listed on the graphs, (b) The oscillation frequency for damping as a function of the applied voltage for the liberal (compact analytical) and the conservative (numerical LLG) models, demonstrating the capability of the analysis to closely follow the expected dynamics from the LLG equation; the minor fluctuations in the reported LLG frequency is due to the random thermal noise, included in the LLG model

to the LLG-based model. Our simulations on a 2 kilo-bit straintronics-based memory system shows at least two orders of magnitude (>100X) simulation speed improvement when the numerical LLG model is replaced with the liberal model. The speed advantage creates a platform for simulation of ultra-large spin-based straintronics systems.

E. Flipping delay vs. settling time

The discussion on the oscillatory behavior when $\sigma > \sigma_{MH}$ necessitates the inspection of the settling time. While in electronics, the delay is defined as the time different between the output and input when they reach half of the final value (50% to 50%), when major oscillations occur, the designer needs to assure that the magnetization will settle along the final state within a defined tolerance, δ, before the removal of stress. Hence, the settling time (also called switching time), t_{sw}, defined as the time required for the magnetization to settle within $\delta = 10\%$ of the final steady state ($\theta = \pi/2\ (1 \pm 0.1)$) will have a higher value than the flipping delay, t_d, defined as the 50% transition of the magnetization ($\theta = \pi/4$). In other words:

$$t_{sw} = t_d + \Delta t_s\ , \tag{3-36}$$

where, Δt_s in the extra time, required by the magnetization to settle along the final state. Approximating the damping behavior of the magnetization with that of a second order control system, we have:

$$t_{sw} = -\frac{\ln(\delta\sqrt{(1-\zeta^2)}}{\zeta\omega_0}, \tag{3-37}$$

The strong dependency of the oscillatory behavior, and hence t_{sw}, on the damping factor and stress level, predicted by (3-37), is demonstrated in Fig. 3-10. In these set of LLG simulations,

the material properties are those of Terfenol-D's and the damping factor is varied to observe the effect of this metric. Fig. 3-10a visually emphasizes on the great difference between t_d and t_{sw}. While the flipping in the third case (when $\alpha = 0.005$) is faster than the first case (when $\alpha = 0.1$), due to the major oscillations in the third case, the switching time becomes much larger. The dependency of the flipping delay and switching time on the damping factor is further highlighted in Fig.3-10b at three different voltage levels (here, $\sigma_C = 0.157V$). It is interesting to observe that, in the presence of oscillations, a lower damping factor leads to a faster flipping, but slower settling, which is due to the major oscillations when $\alpha \to 0$. Fig 8b also highlights the independence of the delay on the damping factor for smaller values of α, which was discussed earlier.

It can also be observed in Fig. 3-10b that when the damping factor becomes really high, the switching delay increases again, which is due to the slow flipping delay of the magnetization in the overdamped regime. Essentially, the slow switching is not because of oscillations, but is because of much higher t_d when $\alpha \to 1$. Hence, there is a range for the damping factor, which

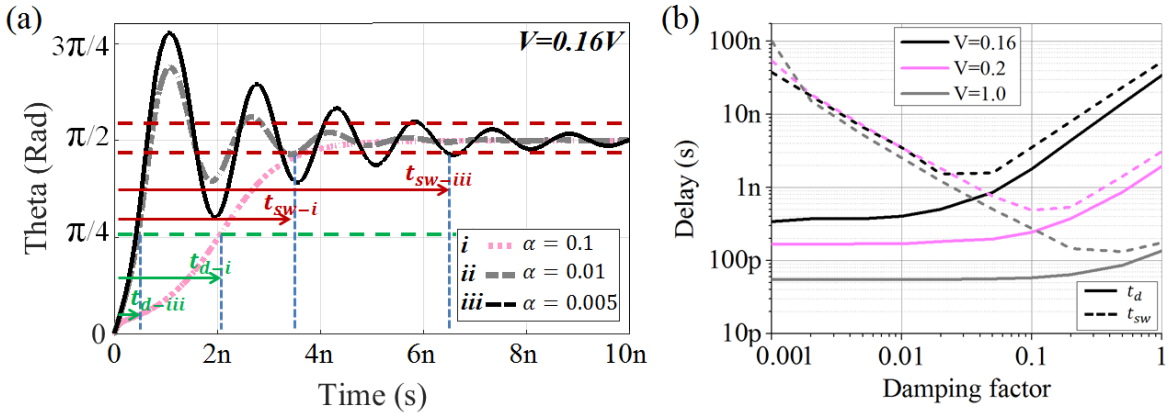

Figure 3-10 - (a) Dynamic flipping of the magnetization and the dependency of the flipping delay and settling time on the damping factor when stress is near critical; as the damping factor reduces, oscillations become more severe and the switching delay increases; (b) Quantitative demonstration of the dependency of the switching time on the damping factor.

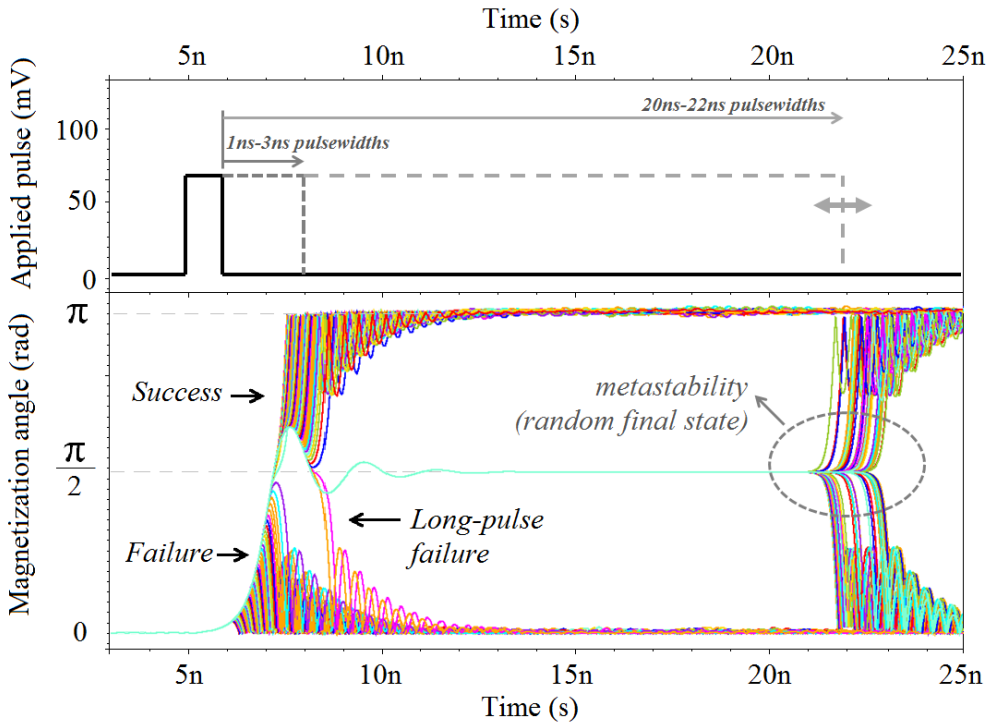

Figure 3-11 - Illustration of the successful pulsewidth with varying the pulsewidth (top) and showing the equivalent dynamic waveforms for different pulsewidth values (bottom). The pulsewidth is once swept between 1ns and 3ns and the results are shown for short-pulse failure, success, and long-pulse failure. Then the pulse is kept for 15-16ns to show the metastability, where the final state is randomly 0 or π.

gives the lowest switching time.

Lastly, ζ in (3-34) also shows a dependency on the applied stress via T_x and T_z; however, it can be shown that when $\sigma \gg \sigma_C$, $\zeta \to \alpha$, meaning that for a fixed material, dramatically increasing stress will not alter the damping behavior of the magnetization. Nevertheless, increasing stress will still lead to a faster settling since when $\sigma \gg \sigma_C$, $\omega_0 \propto \sigma$ and hence $t_{sw} \propto 1/\sigma$. Understanding this matter gives the designer a perspective to establish a tradeoff between material selection and applied stress.

F. The concept of pulse shaping: successful pulsewidth

Writing into the STJ is performed by applying a voltage pulse on the top plate of the PZT, while keeping the Read port inactive. The pulse that initiates flipping must be tailored carefully.

If the voltage pulse across the device is maintained, the magnetization vector will settle into a metastable state along the minor axis, i.e. $\theta = \frac{\pi}{2}$. After the pulse is removed, the magnetization vector will settle either at $\theta = 0$ or $\theta = \pi$ due to thermal noise. Therefore, the pulse duration associated with successful flipping to a final bistable state from the intermediary metastable state is critical. This is demonstrated in Fig. 3-11 for successful flipping (i.e. $\theta = \pi$) and metastable flipping (i.e. $\theta = randomly\ \pi\ or\ 0$) by applying a pulse of 75 mV amplitude and varying the pulsewidth. For the former, the pulsewidth is varied between 1ns and 3ns through 100 steps. It is demonstrated that if the pulse is too short, the magnetization vector will not have enough time to travel and cross the minor axis, and hence, it will bounce back to the initial state. If the pulse is tailored carefully within the value of successful pulsewidth, the magnetization will continue to rotate and settle along the opposite state. If the pulse is retained longer than the success margin, the magnetization will bounce back to the initial state. The successful pulsewidth is illustrated further using the timing diagram in Fig. 3-12a, where, our simulations on Cobalt with 75mV pulse amplitude show that a pulsewidth between 1.7ns and 2.7ns can assure flipping from P →AP. Shorter or longer pulses can cause failure. As we increase the applied voltage across the device, two phenomena are observed:

a) The success margin, demonstrated in Fig. 3-11a, narrows. This is mainly due to the fact that the *general damping factor* of the magnetization (ζ), discussed earlier, reduces as we increase the voltage across the device. The success margin of cobalt and Metglas as a function of applied pulse amplitude across the device is demonstrated in Fig 18b. Pulse amplitudes above 0.3V are not demonstrated in the plot, as they lead to many failure gaps, which will be discussed in the next bullet-point. Metglas shows a lower margin due to its higher value of ζ, resulted from the high Gilbert damping factor.

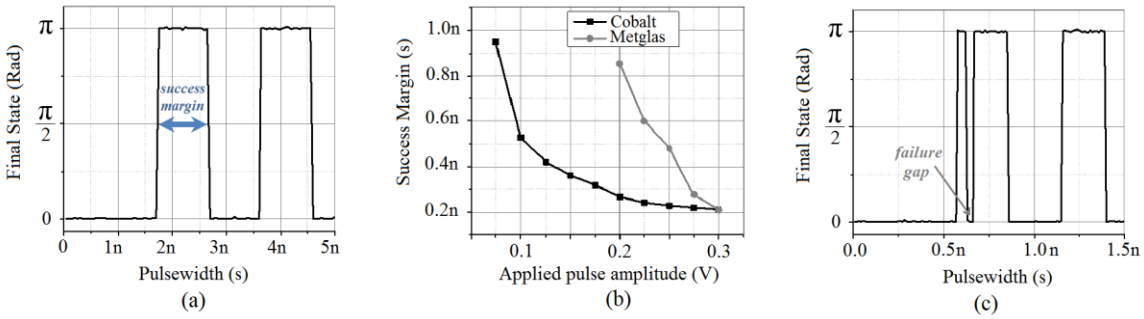

Figure 3-12 - (a) Successful pulsewidth required for flipping the magnetization vector from θ=0 to θ=π for cobalt with 75mV pulse amplitude, (b) As the pulse amplitude increases, the success margin decreases due to lower general damping factor, (c) Success margin demonstrates gaps at higher voltages due to lower general damping factor

b) A higher voltage and, therefore, a lower effective damping factor, leads to failure gaps in the success margin. This is demonstrated in Fig. 3-11c for cobalt when a 200mV pulse is applied across the device. As a result, higher voltages lead to uncertain success margins. However, they provide a much faster alignment of the magnetization vector along the minor axis.

The concept of successful pulsewidth can be handy when it comes to the deterministic applications of the straintronics devices. However, incorporation of the STJ into CMOS circuitry can reduce the success rate due to node fluctuations and rise/fall time limitations. This will be discussed in detail in Section V of the proposal.

CHAPTER 4: EFFECT OF TEMPERATURE VARIATIONS AND THERMAL NOISE ON THE STATIC AND DYNAMIC BEHAVIOR OF STRAINTRONICS DEVICES

Temperature variations can severely impact both static and dynamic responses of straintronics devices. The former is affected due to the strong dependency of the saturation magnetization, shape anisotropy, magnetocrystalline anisotropy, and magnetostriction coefficient on temperature [62-64]. While these parameters assume a fairly fixed value at low temperatures, when approaching the Curie temperature, T_C, they fall dramatically, bringing the free layer close to a paramagnetic state. Hence, the energy barrier of the free layer in the straintronics device, is a strong function of temperature. The critical voltage is also temperature dependent, the behavior of which across temperature needs to be investigated. It is specifically worthwhile to investigate the variations of the above parameters at temperature ranges between 200K and 400K, as this is the operating range of a wide variety of integrated circuits [65].

The dependency of the device's dynamic response is realized by incorporating the Langevin thermal noise field, representing the thermal noise, into the LLG equation. The random noise field has three important impacts on the dynamic behavior: i) It assists with the magnetization

vector's flipping. Without it, the magnetization will stagnate at relaxation state and will not respond to the applied stress; ii) A larger thermal noise leads to larger fluctuations of the magnetization vector, resulting in a faster response and reducing the write error probability (WEP); and iii) Fluctuations can also lead to hold error probabilities (HEP), also known as retention errors, which are hazardous to straintronics-based MRAM design.

Due to its crucial importance, the effect of thermal noise on the dynamic behavior of the magnetization in a nanomagnet has been the subject of the study in literature [39, 66, 67]. A general study of the dynamics in a single domain magnet under Langevin thermal noise has been published previously [66], providing a comprehensive statistical analysis on the magnetization dynamics with and without the effect of external magnetic field. Analysis of the dynamics in strain-induced multiferroics has also been the subject of study recently [67]. These works mainly focus on the effect of dynamic thermal noise on the switching behavior of a single magnet under stress and investigate the switching reliability under different stress removal conditions. While the study of the thermal noise is of significant importance, a comprehensive model that investigates the effect of temperature fluctuations and thermal noise on both static and dynamic behavior of the straintronics device is yet to exist.

In this chapter, we perform an in-depth analysis on the temperature dependency of the static and dynamic metrics of the straintronics MTJ. In search for the proper material for straintronics-based integrated circuits, we investigate four common magnetostrictive materials. The effect of the Langevin thermal field on the initial magnetization angle and the delay metrics of the straintronics device, and the resulting WEP and HEP are studied in detail. The flipping energy and the energy-delay trade-off for the straintronics-based system design are analyzed. First, the dependency of the magnetic anisotropies on temperature is introduced, followed by analysis of

the energy barrier and the critical voltage and their variations with temperature. The effect of thermal noise is modeled next by incorporating the Langevin thermal noise field into the model. WEP, HEP and energy-delay trade-off as important metrics for memory design will be investigated, and an energy efficient write method will be proposed to conclude this section.

A. Dependency of static behavior on temperature

In order to study the static metrics of the straintronics device, the variations in the magnetic parameters and energy levels should be examined [62]. Modeling the effect of temperature on the saturation magnetization of the free layer is analyzed first to create the groundwork for the rest of the chapter.

Conventionally, the temperature dependency of saturation magnetization at temperatures well below Curie level is predicted using Bloch's law [68]. However, the incorporation of the straintronics devices in integrated circuits will require operation at temperatures well above absolute zero, where the conventional Bloch's law does not provide an accurate estimation. Most of the integrated circuits operate at temperature ranges between 200K and 400K. It is experimentally shown that Brillouin function predicts the temperature dependency of the saturation magnetization accurately up to temperatures close to T_C. We have [62]:

$$\frac{M_s(T)}{M_{s0}} = \frac{2J+1}{2J}\coth\left(\frac{2J+1}{2J}x\right) - \frac{1}{2J}\coth\left(\frac{1}{2J}x\right), \tag{4-1}$$

where, J is the total angular momentum, $B_J(x)$ is the Brillouin function of order J, and x is defined as:

$$x = \frac{M_{s0}\left(H + N_w\mu_0 M_s(T)\right)}{NkT}, \tag{4-2}$$

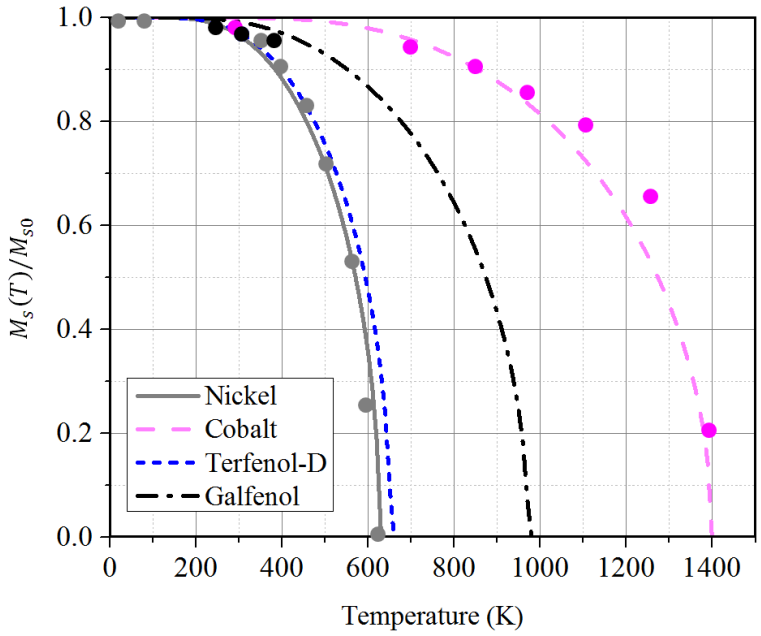

Figure 4-1 - The dependency of the saturation magnetization on temperature with the experimental points demonstrated on the graph from the literature

Here, H is the external magnetic field (zero for ferromagnetic materials), N is the number of atoms per unit volume, and N_w is a material-dependent constant. By graphically intersecting $M_s(T)/M_{s0}$ in (4-1) and (4-2), the dependency of the saturation magnetization on temperature can be obtained, which is demonstrated in Fig. 4-1. In order to confirm the accuracy of the model, the experimental data from literature [46, 62, 69-71] are also included in the graph. Furthermore, the predicted behavior of $M_s(T)/M_{s0}$ for Terfenol-D and Galfenol closely follow the reports from previous works [46].

Next, we will inspect the temperature dependency of different terms in the total magnetic energy of the straintronics device. Here, the downfall of exchange interactions at temperatures close to Curie temperature is not accounted for. The latter can compromise the single domain assumption of the nanomagnet at temperatures around T_C and should be handled with care whenever necessary.

a) Shape anisotropy

Shape anisotropy, as formulated in (2-3) (right hand side, first term), is one of the major decision makers of the free layer's energy barrier. From (2-3), the variations in M_s^2 with temperature can be predicted using the Brillouin function. However, the variations of N_{sh} and V due to thermal expansion should also be further investigated.

Variations in temperature, T, will lead to compression or expansion. However, the relative ratio of t/a and $(a-b)/a$, which are decision makers in (2-4) for N_{sh} will stay constant, assuming a linear thermal expansion ($\Delta L/L = \alpha_L \Delta T$, α_L being the material's expansion coefficient, L and ΔL being the length and change in length, respectively, and ΔT being the temperature variations).

Lastly, due to the small value of α_L, the variations in volume due to thermal expansion is negligible compared to the changes in $M_s(T)$. For example, Nickel exhibits merely 0.4% increase in its volume for every 100 degree increase in temperature.

As a result of the above discussion, the shape anisotropy's dependency on temperature can be summarized as:

$$\frac{E_{sh}(T)}{E_{sh0}} = \left(\frac{M_s(T)}{M_{s0}}\right)^2 \tag{4-3}$$

where, E_{sh0} is the value of shape anisotropy at near-zero temperatures.

b) Magnetocrystalline anisotropy

According to Callen and Callen's theory [72], the dependence of the uniaxial anisotropy constant on temperature originates from the changes in $M_s(T)$, and can be expressed as [72]:

$$\frac{K_u(T)}{K_{u0}} = \left(\frac{M_s(T)}{M_{s0}}\right)^m \tag{4-4}$$

where, K_{u0} is the uniaxial anisotropy's constant near absolute zero temperature. For cubic and uniaxial crystals $m = 3$ and $m = 10$, respectively [73]. Therefore, Nickel and Cobalt will have the powers of 3 and 10 in the above equation, respectively.

Although Callen and Callen's theory predicts the temperature dependency of the Magnetocrystalline anisotropy fairly well for pure element crystals, it is shown that it fails to predict the temperature dependency of K_u for alloys [73]. Hence, the variations in the uniaxial coefficient for Galfenol and Terfenol-D should be investigated separately.

Given the crystal structure of Galfenol ($Fe_{1-x}Ga_x, 0.13 \leq x \leq 0.24$), using the power $m = 2.1$ provides a fairly accurate estimation [74-78]. Terfenol-D ($(Tb, Dy)Fe_2$), however, is considered as a rare-earth 3d-transition-metal alloy. For these alloys, the magnetic anisotropy

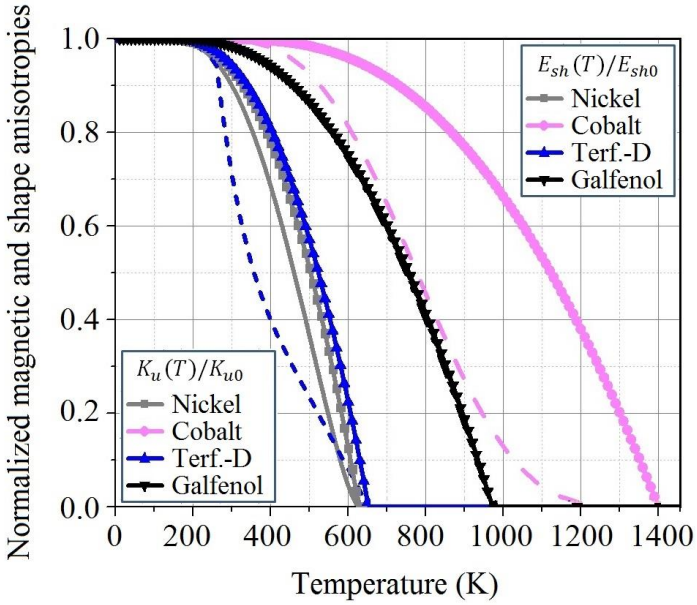

Figure 4-2 - The dependency of shape and uniaxial anisotropies on temperature up to the Curie levels for different materials; as the Curie temperature is reached, the materials lose their intrinsic magnetic energies and approach a paramagnetic state

transits through three different phases [79, 80]:

i) When the temperature of the alloy is below the spin reorientation temperature, T_{SR}, the magnetic anisotropy follows the famous power law in (4-4), in which: $m = l(l+n-2)/(n-1)$. For lowest order anisotropy $l = 2$, and assuming a planar model in which $n = 2$, we will have $m = 4$. The value of T_{SR} for Terfenol-D is ~ -10 ℃ [80, 81], which means that, up to this temperature, the power law is enforced.

ii) For the values above spin-reorientation temperature, the behavior is mostly dominated by the rare-earth elements and is given by [79]:

$$\frac{K_u(T)}{K_{u0}} = \frac{J_{SR}^2}{n(n+2)k^2T^2}, \tag{4-5}$$

where, k is the Boltzmann constant and J_{SR} is an alloy-dependent constant and can be obtained by assuming a continuous transition of $K_u(T)$ at the spin reorientation temperature.

iii) When the temperature approaches the Curie temperature, (4-5) fails to predict the behavior. The behavior, at this point, can be expressed as [79]:

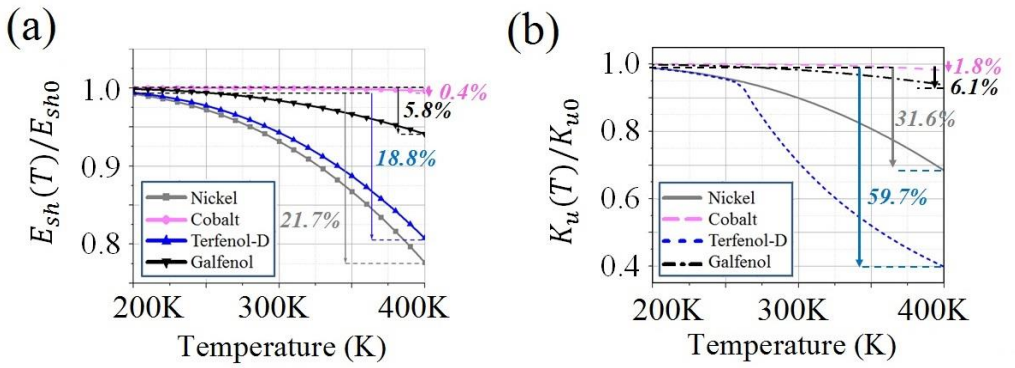

Figure 4-3 - Further demonstration of the (a) shape and (b) uniaxial anisotropies' variations within 200K and 400K

$$\frac{K_u(T)}{K_{u0}} = 1 - \frac{T}{T_C} \tag{4-6}$$

By combining the three regions above, the uniaxial anisotropy of Terfenol-D can be predicted. Our simulations on the magnetic anisotropy of Terfenol-D closely follow the reports in literature [80, 81].

Fig. 4-2 contains the simulation data on the normalized variations of shape and uniaxial anisotropies, as the temperature increases for four materials. The values are also re-plotted for 200 K to 400 K IC temperature range in Fig. 4-3, and the percentages of anisotropy reduction for the four materials along with their magnetic properties [82-87] used in our simulations model are listed in Table 4-1. Dramatic reductions of both shape anisotropy and uniaxial anisotropy reveal the critical influence of temperature on the device's energy barrier, an important metric for non-volatile memory design.

c) Magnetostriction expansion at saturation

The magnetostriction expansion at saturation, λ_s, plays a major role in determining the critical stress required for flipping the magnetization state of the straintronics device. The dependency of this parameter on temperature is expressed using the reduced hyperbolic Bessel function [88,

Table 4-1 – Materials' properties and the percentage of reduction in shape, uniaxial, and stress energies of different magnetostrictive materials when the temperature is raised from 200K to 400K

	Nickel	Cobalt	Terfenol-D	Galfenol
$M_s\ (kA/m)$	510	1400	912	1340
$K_u\ (kJ/m^3)$	12	16	1.6	5
$\lvert\lambda_s\rvert\ (ppm)$	20	20	600	200
$T_C\ (K)$	627	1400	652	972
$E_{sh}\ (\%)$	21.7	0.4	18.8	5.8
$E_u(\%)$	31.6	1.8	59.7	6.1
$E_\sigma\ (\%)$	30.8	0.6	26.6	8.2

89]:

$$\frac{\lambda_s(T)}{\lambda_{s0}} = \widehat{I_{\frac{5}{2}}}(u) \tag{4-7}$$

Where, $\coth(u) - 1/u = M_s(T)/M_{s0}$. The simulation results are plotted in Fig. 4-4 for the four magnetostrictive materials. The simulation results are in fair accordance with the reported behavior in literature [88-91]. In fact, it is demonstrated that the hyperbolic Bessel function in molecular-field approximation holds accurately at all temperatures up to Curie temperature [72], while, at low temperatures, the magnetostriction coefficient follows the same power laws as magnetic anisotropy. The percentages of variations in E_σ due to λ_s variations, when temperature rises from 200K to 400K, are tabulated in Table 4-1 for the sake of comparing different materials.

From the obtained metrics in Table 4-1, it is understood that Cobalt and Galfenol show the least amount of variation in the temperature range of interest, while Nickel and Terfenol-D show dramatic variations in their magnetic parameters. This is mainly due to the high Curie

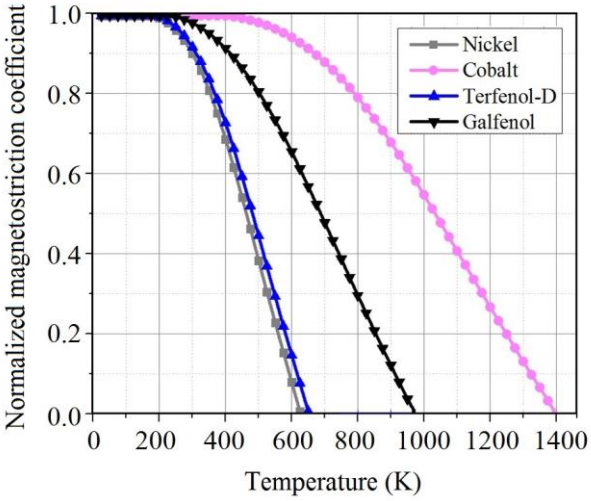

Figure 4-4 - The dependency of the magnetostriction coefficient on temperature as predicted by the Hyperbolic Bessel Function

temperature of Cobalt and Galfenol, which might make them the preferred candidates to be integrated into electronic circuits. Terfenol-D, although demonstrating fast response and low switching voltage, is not an ideal candidate for temperature-sensitive straintronics-based integrated circuits, as its magnetic properties vary dramatically with temperature variations, a phenomenon that frequently occurs in circuit chips.

B. Energy barrier and critical flipping voltage

Assuming the rotation of the magnetization vector within the *y-z* plane, which is enforced by shape anisotropy, the intrinsic energy barrier is defined as: $EB = E_{mag}(\theta = \pi/2) - E_{mag}(\theta = 0\ (or\ \pi))$. From the discussions in Section A, it is naturally expected that the barrier will reduce as the temperature increases due to the fall in the magnetic anisotropies. This is demonstrated in Fig. 4-5a, where the energy barrier is plotted for Nickel as a function of temperature in the absence of stress. A contour map of the energy barrier's graph is re-plotted in Fig. 4-5b to further demonstrate the energy behavior as a function of temperature. From the two

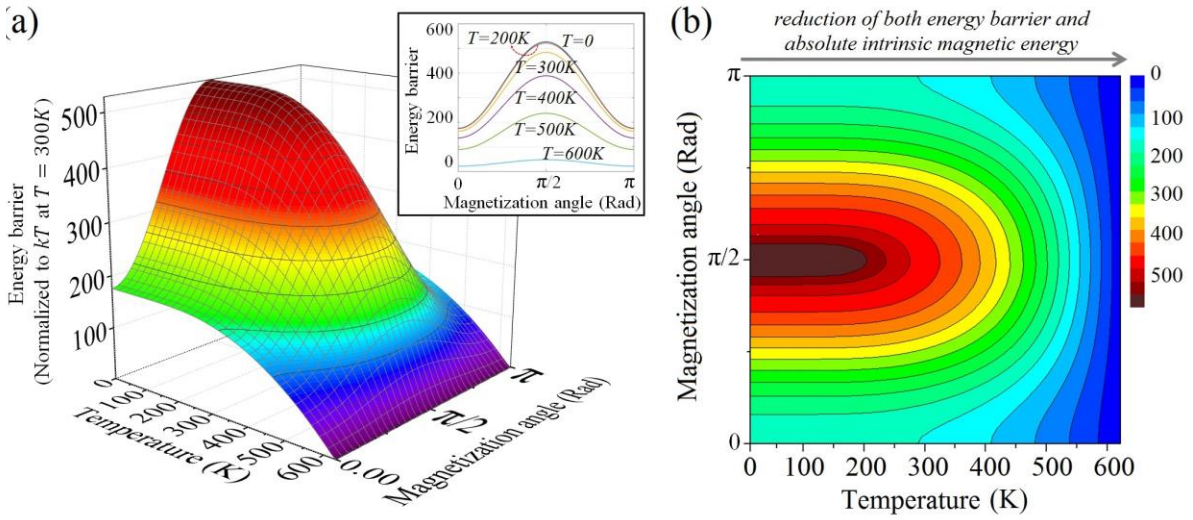

Figure 4-5 - (a, b) The dependency of the energy barrier of Nickel on temperature; as the temperature rises, both the energy barrier and the absolute values of energy reduce

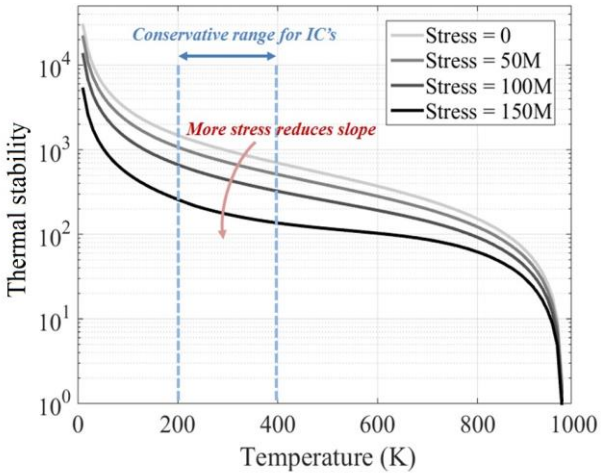

Figure 4-6 - The dependency of thermal stability of Galfenol on temperature and applied stress; the graph shows two fast regions: i) at low temperatures where the parameter *kT* rises, and ii) at temperatures close to T_C where the energy barrier approaches zero

graphs, the following conclusions can be drawn: i) The intrinsic magnetic energy assumes its minimum in the parallel and antiparallel orientation and its maximum when the magnetization is oriented along the minor axis; ii) The energy barrier reduces and eventually vanishes as the temperature approaches the Curie level, where the material reaches a paramagnetic state; and iii) The absolute value of the energy at any orientation of the magnetization vector (for example at $\theta = 0$) also reduces as temperature increases. For example, from Fig. 4-5a, at $\theta = 0$, the magnetic energy at near-zero temperature, is eliminated as the temperature approaches T_C.

It is particularly worthwhile to investigate the effect of stress and temperature on the device's thermal stability, $\Delta = EB/kT$, which is an important data retention metric in non-volatile memory design. Usually, a thermal stability factor, larger than 40 is required for storage class memories [92]. The thermal stability of the straintronics device, with Galfenol as the magnetostrictive material, is demonstrated as a function of temperature for different stress values in Fig. 5-6. It is observed that, as the temperature merges T_C, a sharp reduction in the thermal stability is observed. Further, increasing stress reduces the thermal stability linearly, which is

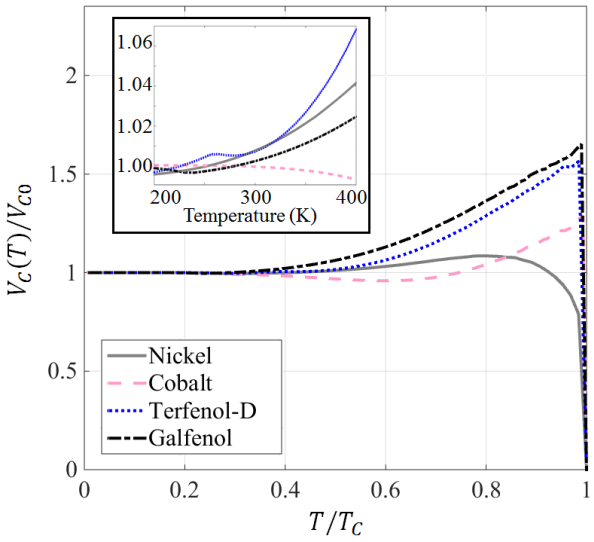

Figure 4-7 - The dependency of the critical flipping voltage on temperatures up to the Curie levels for four magnetostrictive materials; the variations within 200K to 400K are demonstrated in the inset of the figure, showing that the four materials maintain an almost-constant critical voltage within the range of interest; the results are normalized to V_{C0}, the critical flipping voltage near absolute zero temperature

expected intuitively given (2-3) and (2-5). In general, it is observed that Galfenol keeps its thermal stability well above 40, within 200K to 400K temperatures range, even at stress values closer to its critical stress ($\sigma_C \approx 180\ MPa$ for Galfenol in our simulations).

Lastly, the effect of temperature on the minimum voltage required for the magnetization flipping, also called the critical voltage, V_C, should be analyzed. Given the critical stress in (2-14) and the relationship between voltage and stress as $\sigma = Yd^tV/t_{PZT}$, the critical voltage is expressed as:

$$V_C = \frac{\left(\frac{\mu_0}{2}M_s^2\left(N_{yy} - N_{zz}\right) + K_u\right)t_{PZT}}{\frac{3}{2}\lambda_s Y d_{31}}, \tag{4-8}$$

where, d_{31} is PZT's d^t coefficient element, translating the electric field towards a stress in the z-direction. The dependency of V_C on temperature is simulated in Fig. 4-7 for different magnetostrictive materials. By observing the graphs closely, the critical voltage goes through

two different slope phases as the temperature increases. First, at low temperatures, V_C slightly reduces as temperature increases. Then, an increase in the value of the critical voltage is observed at higher temperatures. This behavior can be analyzed by taking the derivative of (4-8) with respect to temperature:

$$\frac{dV_C}{dT} = \frac{A\frac{dM_s}{dT} + B\frac{dK_u}{dT} - C\frac{d\lambda_s}{dT}}{\left(\frac{3}{2}\lambda_s Y d_{31}\right)^2} \tag{4-9}$$

$$A = \frac{3}{2}\lambda_s Y d_{31}\,\mu_0\left(N_{yy} - N_{zz}\right)M_s t_{PZT} \tag{4-10a}$$

$$B = \frac{3}{2}\lambda_s Y d_{31} K_u t_{PZT} \tag{4-10b}$$

$$C = \frac{3}{2} Y d_{31}\left(\frac{\mu_0}{2}M_s^2\left(N_{yy} - N_{zz}\right) + K_u\right)t_{PZT} \tag{4-10c}$$

The saturation magnetization starts degrading at lower temperatures compared to the magnetostriction coefficient. As a result, when $T \ll T_C$, we have $dV_C/dT < 0$, and a slight reduction of the critical voltage is observed. This behavior is more noticeable for Cobalt on the graphs, mainly due to its high M_s and very low λ_s. As the temperature rises, λ_s starts decreasing according to (4-9) while M_s and K_u continue to fall as predicted by the saturation magnetization's behavior and (4-10), respectively. When the slope of $d\lambda_s/dT$ is large enough to fulfill $A{\times}dMs/dT + B{\times}dK_u/dT - C{\times}d\lambda_s/dT > 0$, the critical voltage will begin to rise.

From the inset of Fig. 4-7, it is also concluded that Galfenol and Cobalt keep their critical voltage at a fairly constant level, while Terfenol-D and Nickel show roughly 7% and 4% increase of V_C within 200K to 400K temperature range, respectively. Nevertheless, it is concluded that the variations in critical voltage (and also thermal stability) within 200K and 400K are negligible, which is good news for circuit design applications.

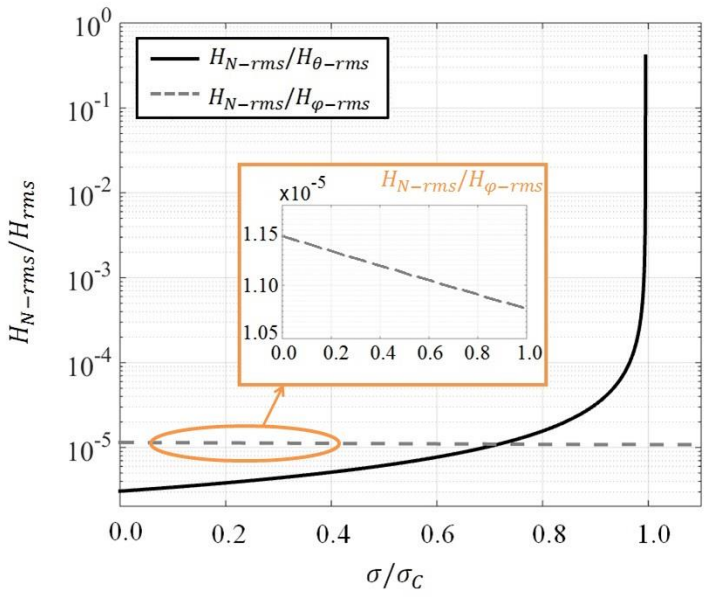

Figure 4-8 - The effect of stress on the relative strength of the thermal noise; as the stress increases, H_N/H_θ rises, leading to more fluctuations around the *z*-axis, while H_N/H_φ decreases slightly (inset), increasing the magnetization vector's tendency to stay within the *y-z* plane

C. Dynamic thermal noise field

The dynamic response of the magnetization vector in a straintronics device is predicted using the LLG equation in (3-1). The effect of thermal noise is modeled by following the same procedure developed by Brown [93] and Grinstein [94]. The thermal flux density can be incorporated in (3-1) by including the Langevin thermal noise field, H_N, in the total magnetic field; i.e. $H_{tot} = H + H_N$, where, H_N is a Gaussian random noise field variable with a strength of $D = 2kT\alpha/\mu_0\gamma_0 M_s V$, and a correlation of:

$$< H_i(x,t)H_j(x',t') > = D\delta_{ij}\times\delta(x-x')\delta(t-t') \qquad (4\text{-}11)$$

Therefore, the thermal noise field to be incorporated in the LLG dynamics can be expressed as:

$$H_{N,i} = \sqrt{\frac{2\alpha kT}{\mu_0\gamma_0 M_s V}}X_i(t), \qquad i = (x,y,z), \qquad (4\text{-}12)$$

where, $X_i(t)$'s are uncorrelated zero-mean unit-variance Gaussian random variables in the direction of Cartesian axes.

The relative ratio of the thermal noise field to the net magnetic field of the device (i.e. H_{N-rms}/H) can be simulated to observe the strength of the thermal noise. It is expected that as we increase the stress level, the net magnetic field forcing the magnetization vector to stay along the easy axis (H_θ) becomes weaker [46]. It can also be shown [46] that as we increase the stress, the value of H_φ, which forces the magnetization to stay in plane (within the *y*-*z* plane of Fig. 2-2), increases slightly. Therefore, an increase of stress increases H_{N-rms}/H_θ as demonstrated in Fig. 4-8, allowing the magnetization to fluctuate easier around the easy axis. As the stress approaches its critical value, the thermal noise becomes significantly stronger owing to the fact that in (3-7) $\lim_{\sigma \to \sigma_C} H_\theta = 0$. It is also observed from Fig. 4-8 that, as we increase the stress,

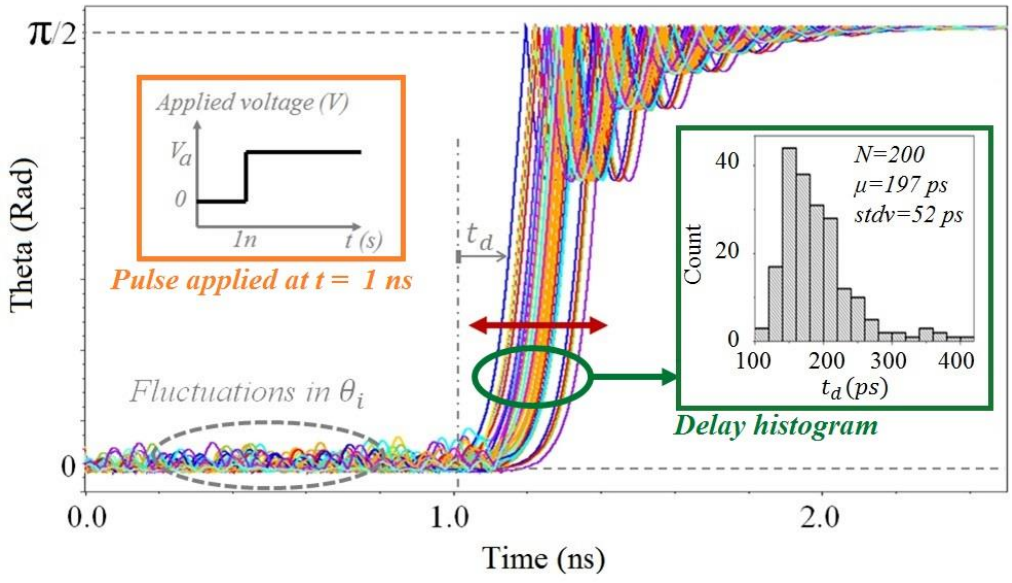

Figure 4-9 - Due to the random nature of the initial angle, the flipping delay varies with a skewed Gaussian distribution as demonstrated in the inset of the figure; at room temperature, the mean value of the delay is observed to be $197ps$ with merely $52ps$ of standard deviation; the left inset is the voltage pulse, applied at $t = 1\ ns$, and the right inset shows the histogram of the delay values on 200 plotted dynamic waveforms

H_{N-rms}/H_{φ} slightly reduces. This means that, while the magnetization vector's fluctuations around the major axis (*z*-axis) increase at higher stress levels, its tendency to stay within the *y*-*z* plane increases slightly, leading to more in-plane fluctuations.

The flipping delay of the straintronics device (also called the alignment delay in some works) is a strong function of the initial magnetization angle, θ_i, which is mainly due to the thermally stimulated agitations. It is shown that the initial magnetization angle has a zero-mean Gaussian distribution with the strength of [95]:

$$\theta_{i-rms} = \sqrt{\frac{kT}{\mu_0 V M_s H}} \tag{4-14}$$

Due to the dependency of the flipping delay on the initial magnetization angle, Gaussian fluctuations of θ_i lead to variations in the flipping delay, t_d. This is demonstrated in Fig. 4-9, where our thermally-incorporated model based on LLG dynamics with (4-12) is simulated at

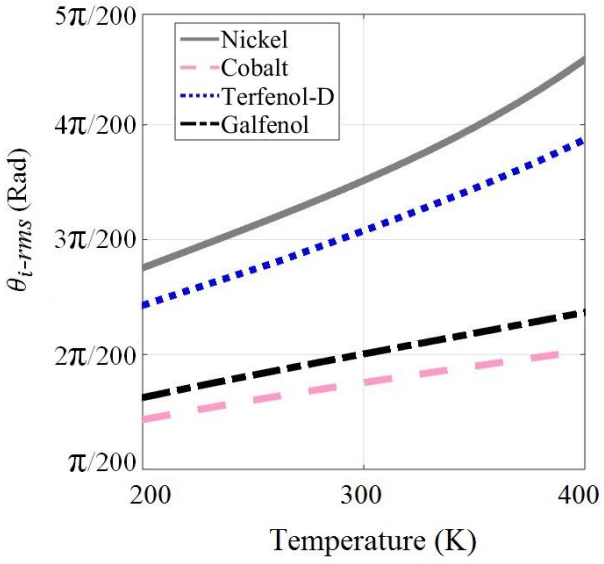

Figure 4-10 - The dependency of the initial magnetization angle on temperature; a higher temperature leads to more fluctuations due to the higher thermal noise

room temperature. The dynamic waveforms of the magnetization flipping for $N = 200$ samples and the resulting histogram for the flipping delays are demonstrated. The results indicate an average delay of 197 ps with a standard deviation of 52 ps. The delay histogram is slightly skewed due to the lower limit on the flipping delay.

Fig. 4-10 illustrates dependency of θ_{i-rms} on temperature. As the temperature increases and approaches the Curie level, it is expected that the fluctuations increases since $H \to 0$ as temperature approaches T_C. By plotting the value of θ_{i-rms} between 200K and 400K in Fig. 4-10, it is observed that Nickel and Terfenol-D demonstrate more fluctuations mainly owing to their lower T_C values. The higher fluctuations will assist with the easier flipping of the magnetization vector. Another parameter that can dramatically alter the value of θ_{i-rms} is the applied stress, as demonstrated in Fig. 4-11a. As the stress levels reach their critical value for the four simulated materials, the initial angle approaches the value of $\pi/2$, owing to the stress-reduced energy barrier. From the basics of the straintronics principle, it is expected that when

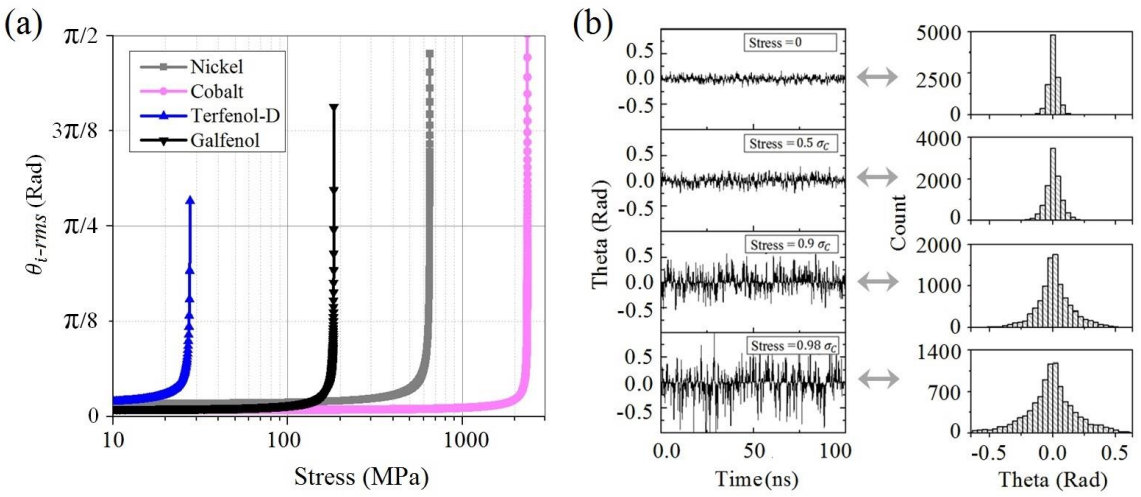

Figure 4-11 - The dependency of the initial magnetization angle on the applied stress; as the stress approaches the critical values, the initial angle approaches $\pi/2$, as predicted by the stress anisotropy (b) dynamic waveforms and histograms of the initial angle of Galfenol for different stress levels, showing much larger fluctuations at high stress values

$\sigma > \sigma_C$ the magnetization settles along the minor axis where $\theta = \pi/2$ and the magnetization vector will now fluctuate around this axis. The dynamic waveforms and histograms of the magnetization's fluctuations around the major axis along with their histograms at different stress levels below critical stress are also plotted in Fig. 4-11b.

The dependency of the flipping delay on θ_{i-rms} is simulated and demonstrated in Fig. 4-12 for temperature ranges between 200K and 400K. As we increase the temperature, the value of θ_{i-rms} increases, leading to easier magnetization flipping, and therefore, a lower delay. The analytical data on the graph are the expected results from (4-14) and the simulated data is obtained from our Verilog-A model based on the thermally incorporated LLG dynamics. The accuracy of the developed model can also be confirmed by comparing the analytical and simulated results.

The flipping delay of different materials, besides depending on the initial angle, is a strong

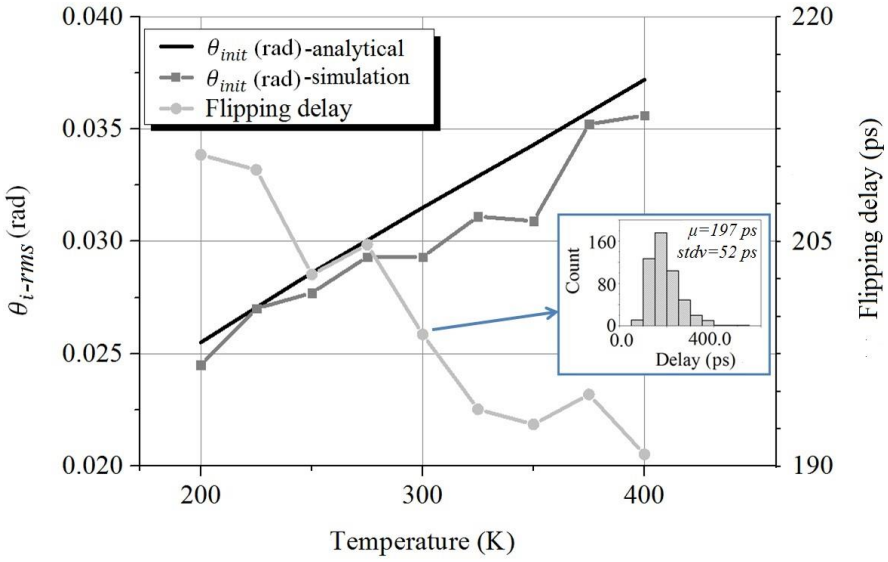

Figure 4-12 - Simulations results on Galfenol, showing the dependency of the initial angle and flipping delay on temperature along with the analytical data from (18); as temperature rises, the initial angle increases and the delay decreases slightly

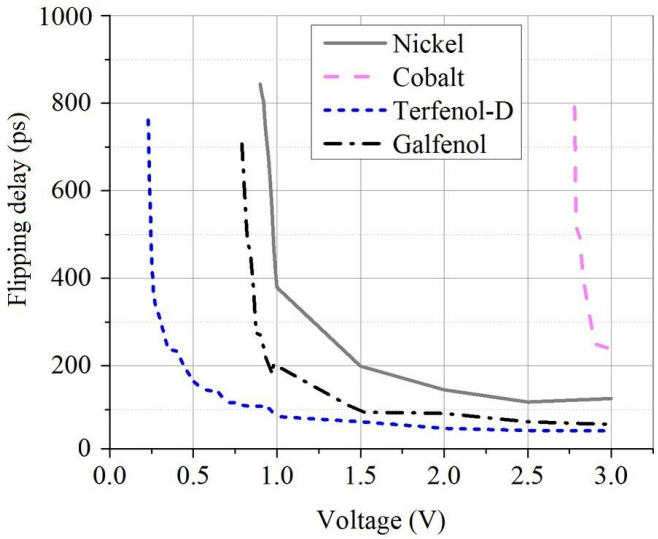

Figure 4-13 - Flipping delay for different magnetostrictive materials as a function of applied voltage's amplitude, showing the significant effect of high stress on flipping time of the nanomagnet

function of the applied voltage (and therefore stress) across the straintronics device. Here, we analyzed the voltage dependency while including the materially-dependent thermal noise. The four materials are simulated at room temperature and the results are recorded in Fig. 4-13, where, it is observed that Terfenol-D has a very fast response owing to its high θ_{i-rms} (as expected from Fig. 4-10) and λ_s, while Cobalt shows a slow response due to its low θ_{i-rms} and λ_s. Nickel, although demonstrating a higher initial angle in Fig. 4-10, fails to compete with Galfenol and Terfenol-D due to its low λ_s. This confirms the suitability of Galfenol for integrated circuits applications due to its low critical flipping voltage, low flipping delay, and low variations of static features across temperatures between 200K and 400K as discussed earlier in Section C.

D. Temperature dependency of dynamic metrics

In the last section of this paper, some of the important metrics related to non-volatile memory design, an important application of straintronics devices, will be discussed. The effect of thermal noise and temperature variations on WEP and the speed-WEP trade-off will be analyzed. A write method that improves the energy and performance of the straintronics-based memories will be

proposed. The effect of stress on the flipping delay and the HEP of the device will be analyzed in order to investigate the reliability and advantages of the proposed method.

a) Write error probability

One of the important obstacles in memory design is the probability of write error during the write operation, abbreviated as WEP. Consider any memory with a certain write pulsewidth, demonstrated in the inset of Fig. 4-14a. The duration of the pulsewidth indicates the write speed of the memory. If a higher speed is desired, the pulsewidth can be reduced. However, since the speed of writing in any memory cell is limited, there is a lower bound, beyond which, the pulsewidth cannot be reduced. This lower bound is usually selected according to the memory's write error tolerance. For example, consider a straintronics device of Fig. 2-2a. The application of a pulse with an amplitude higher than V_C will force the magnetization vector to settle along the minor axis ($\theta = \pi/2$). Due to the random nature of the Langevin thermal noise, the flipping delay can take a range of values as demonstrated in Fig. 4-14a. Write error is associated with

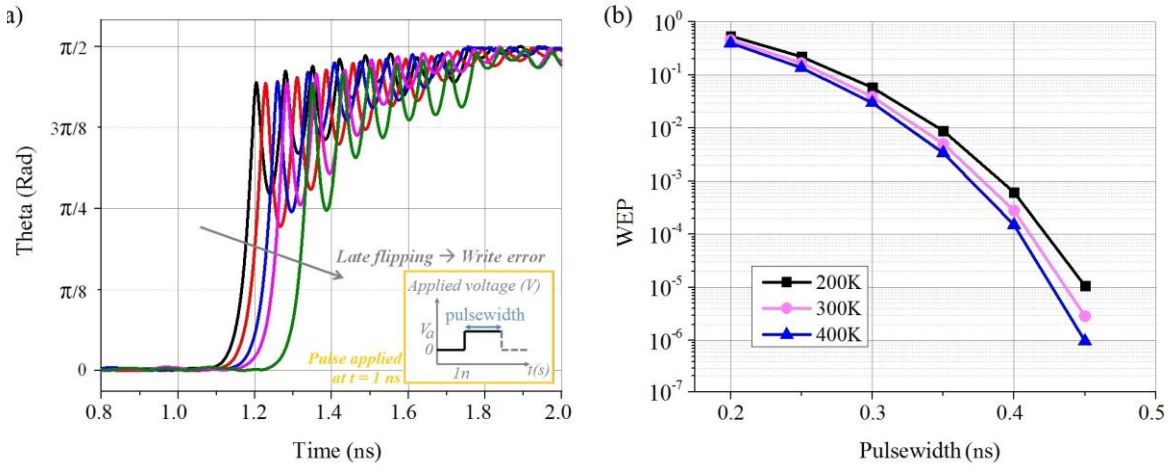

Figure 4-14 - Dynamic waveforms for Galfenol demonstrating the possibility of write error due to late flipping; the inset of the figure shows the voltage pulse, applied at $t = 1\ ns$, and (b) WEP as a function of pulsewidth and temperature; it is evident that as the pulsewidth is increased, the WEP decreases dramatically; increasing temperature will also reduce the WEP slightly for a given pulsewidth due to the dependency of the initial angle of temperature in (4-14)

cases, where the delay is higher than the write pulsewidth, in which; the magnetization vector will fail to flip.

Due to the Gaussian distribution of the flipping delay, demonstrated in Fig. 4-9, the WEP is expected to reduce significantly as we increase the write pulsewidth, which is demonstrated in Fig. 4-14b. On the other hand, a longer pulsewidth is associated with a slower memory. Therefore, there is a trade-off between speed and WEP. As can be seen in the graphs, a reduced write speed from 0.2ns to 0.4ns, leads to more than 1000X lower WEP at room temperature. In memory applications, the pulsewidth does not need to be increased further than the system's WEP requirements.

The effect of temperature on WEP can also be observed in Fig. 4-14b, where we simulated Galfenol for different pulsewidths at different temperatures. A lower WEP at higher temperatures is mainly due to the increased θ_{i-rms} from 200K to 400K, as expected from (4-14).

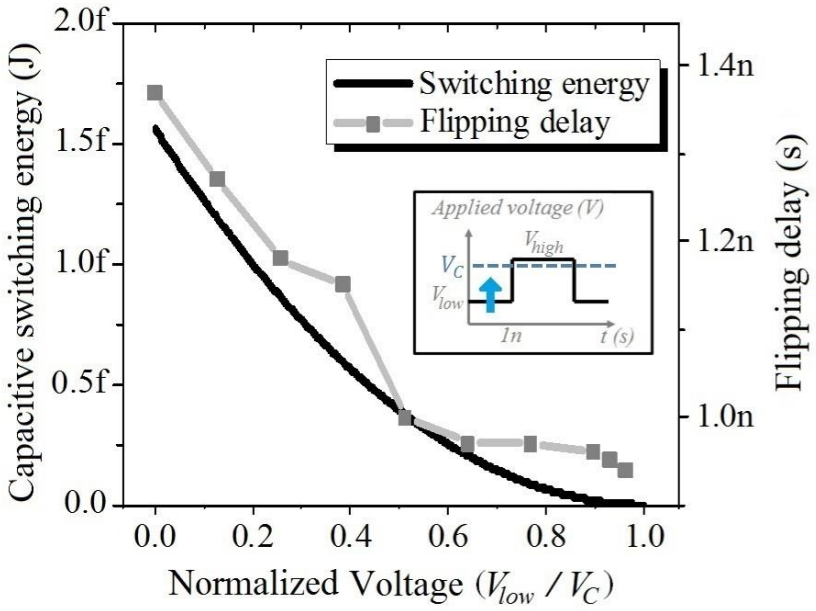

Figure 4-15 - By increasing the value of V_{low} closer to the critical voltage of Galfenol, the capacitive switching energy and flipping delay decrease

b) A proposed write method, the energy-performance trade-off, and hold error probability

When it comes to memory design, energy and performance are two of the most important metrics. A considerable amount of research has been going on to reduce the write energy while retaining the speed of the MTJ-based memories [96-99].

The switching energy, associated with the flipping of the straintronics device, can be formulated as [40]:

$$E = C_{PZT}\Delta V^2 + E_d, \tag{4-15}$$

where, C_{PZT} is the capacitance of the piezoelectric layer, ΔV is the voltage swing across the device, and E_d is the dissipated energy due to the Gilbert damping [100]. For the devices with high energy barriers, the critical voltage is high enough to assure that the capacitive switching will consume the majority of the total switching energy. The switching energy can be significantly reduced if the voltage swing across the device is reduced, as demonstrated in the

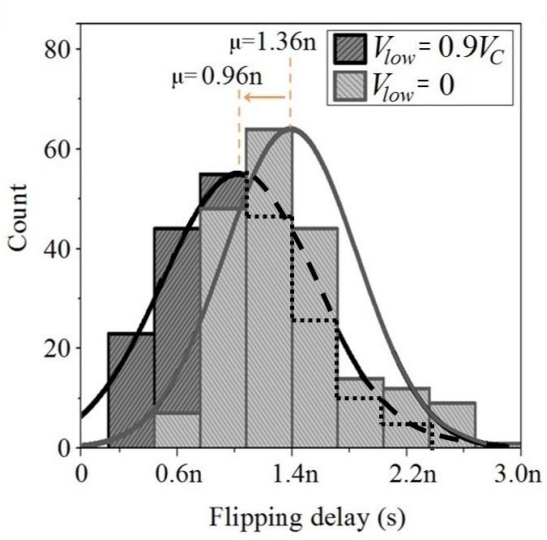

Figure 4-16 - Histograms of the flipping delays demonstrating the reduction in the flipping delay due to higher V_{low}

inset of Fig. 4-15. Increasing the value of V_{low} to the levels closer to V_C has two main advantages: i) As $\Delta V = V_{high} - V_{low}$ reduces, the capacitive switching energy will drop as demonstrated for Galfenol in Fig. 4-15, where we fixed V_{high} slightly above V_C and started sweeping $V_{low}$from 0 to V_C. When $V_{low} \approx V_C$, the capacitive switching will consume negligible energy; ii) The flipping delay will reduce as V_{low} increases as demonstrated in Fig. 4-15. The latter is expected since a higher V_{low} will create some stress across the device, reducing the energy barrier and increasing θ_{i-rms} according to (4-14). Therefore, a higher V_{low} leads to a higher θ_{i-rms}, which is associated with a faster flipping. This is further demonstrated in Fig. 4-16, where the delay histograms are plotted. The mean of the distributions moves towards smaller delays when the value of V_{low} is raised. Note that, in the simulations of Fig. 4-15 and Fig. 4-16, V_{high} is set to be slightly higher than V_C. Should the value of V_{high} be increased, the delay will reduced significantly, as already discussed in Section V.

In order to analyze the reliability of the proposed method, we simulated the HEP of our straintronics device, as an important data retention related property for non-volatile memories. It

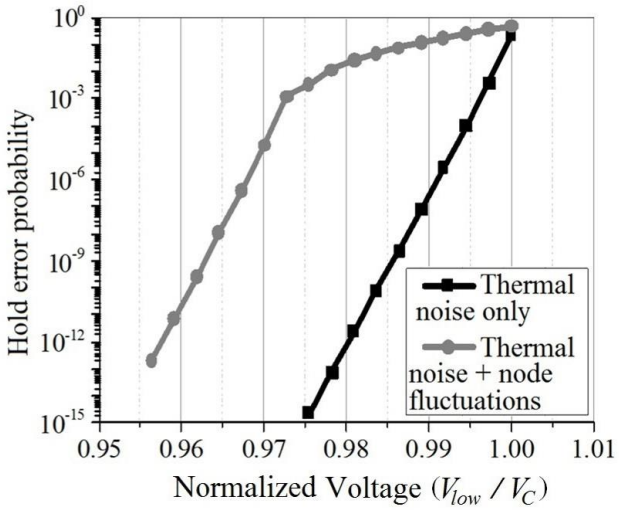

Figure 4-17 - HEP as a function of V_{low} in the presence of thermal noise only, and in the presence of both thermal noise and 1% voltage node fluctuations

is expected that, as we increase V_{low}, the HEP will reduce due to the increased thermal noise fluctuations. This phenomenon is demonstrated in Fig. 4-17, where we increased V_{low} to values close to V_C and plotted to resulting HEP in two cases. First, we only assumed the presence of the Langevin thermal noise, and then we included 1% fluctuations of the applied V_{low}, which can frequently happened due to clock feedthrough in the ICs [1]. In the first case, the HEP is negligible as long as V_{low} is kept below $0.97V_C$. In the second case, the HEP is noticeably higher compared to the first case, but reduces to negligible values as V_{low} goes below $0.95V_C$.

In the above simulations, the possibility of dimension changes due to process variations is not considered. Assuming that the effect of process variations on the device's dimensions are included, the value of V_{low} will decrease accordingly. In any event, from the above discussions, it can be concluded that reducing the voltage swing while retaining the value of V_{low} reliably below V_C will increase the energy efficiency and performance of the system while providing enough noise margin to keep the HEP well below the system's error tolerance. Nevertheless, it should be noted that the value of HEP is a strong function of the device's energy barrier. Should the energy barrier be decreased, the value of HEP in Fig. 4-17 will increase.

CHAPTER 5: AN ENERGY EFFICIENT STRAINTRONICS-BASED RANDOM ACCESS MEMORY

The growing demand for non-volatile semiconductor memories has propelled a frenetic pace of research on emerging memory technologies by exploiting a host of novel materials and fundamental physical phenomena at nanoscale structures such as phase changes in chalcogenide materials [101], ionic transport in binary and ternary oxide materials [102], nanomagnetism in ferroelectric materials [103], and electron spin in composite magnetoresistance materials [104]. Because of the following superior concomitant *electrical properties* of magnetoresistance materials, MRAM memories have garnered a tremendous amount of interest in the design of commercial, military and space systems: i) Ultra-high *endurance* that denotes the number of times a memory cell can be written; ii) High *data retention* property to preserve stored information for several years; iii) Low *switching energy* (about 200 *kT* as opposed to 30,000 *kT* in CMOS memory cells) to change the binary state in a memory cell; and iv) High *reliability* of the memory array due to improved sneak inter-cell leakage currents.

Conventional approaches to switch the state of an MTJ, discussed in Section I, are to use an electrical current flow through field induced magnetic switching [105] or spin transfer torque switching [33, 106]. This dependency on static current flow in order to store information into an

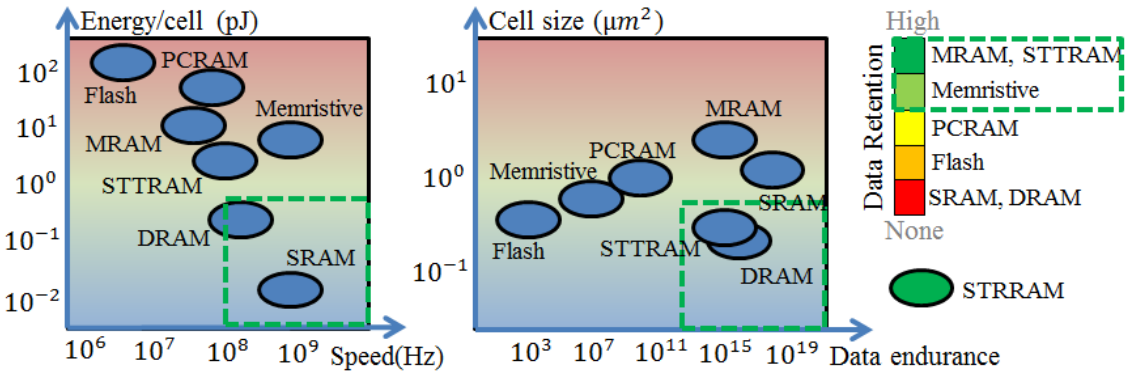

Figure 5-1 - Different memory types in terms of energy efficiency, speed, cell size, data endurance, and data retention. The ideal regions are specified with dashed green lines.

MTJ nullifies the superiority of low-energy magnetic storage as discussed above. In order to maximize the energy efficiency and leverage the inherent energy advantage of the magnetic logic, the amount of charge required to switch the state of the magnetic cell should be minimized.

Typical magnitude of the accompanying electric current varies from several mA for spin valve and toggle MRAM cells to a few hundred μA for in-plane STT [106] and less than a hundred μA for perpendicular STT memory cells [33]. Although the perpendicular STTRAM can almost compete with the CMOS static RAM (SRAM) [31] in terms of energy efficiency, it is still far away from the MTJ's theoretical switching energy limit. Furthermore, the STT current is highly dependent on the error tolerance of the system [33].

In this section, we use STJ along with CMOS switches and peripheral circuitry to propose a proof-of-concept energy-efficient random access memory. The inherent energy, speed, data retention, and endurance advantages of STJ can assist the future circuit designers to overcome the obstacles of the progressing CMOS technologies.

Different memory types [107-111] in terms of energy per cell, speed of operation, cell size, data endurance, and data retention are demonstrated in Fig. 5-1. The dashed regions in the diagrams demonstrate the ideal regions in which a memory can operate. The term "universal

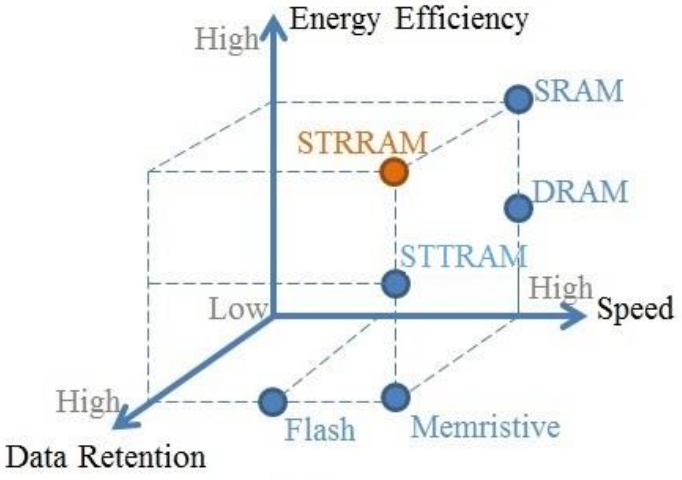

Figure 5-2 - Comparative merits of straintronics compared to STT and FIMS. As the figure indicates, while SRAM and DRAM currently meet the demanding speed requirement, they are volatile memories prone to leakages and therefore consuming high static energy. Memristive memories are non-volatile but use charge trapping into oxide materials and are generally high power, low endurance, and prone to sneak path leakages and poor reliability. Flash memories have poor speed and require high energy due to charge pump circuits that provide higher-voltage programming and erasing pulses.

memory" identifies a memory that lies within the dashed regions of Fig. 5-1, implying good energy efficiency, speed, data density, data endurance, and data retention. While SRAM lies in the ideal region of energy per cell and speed, it lacks the high density and data retention properties. DRAM shows acceptable data endurance and cell size but is not energy efficient and fails to demonstrate data retention due to volatility. Spin Transfer Torque RAM (STTRAM) fails to fulfill all the requirements due to its energy efficiency and write error rate obstacles. This is because high static currents are required for reliably switching the binary state of the magnetic cell. The STTRAM in [33] requires more than 100uA to assure MTJ switching within 4ns for less than 10^{-5} error rate. Therefore, an approach that can switch the state of the magnetic cell without requiring high static currents can help in taking a step forward towards creating the universal memory. The latter is achieved using the straintronics principle. Here, the STJ is used to build a high speed energy efficient memory cell and a memory array, highlighted in Fig. 5-2, as straintronics RAM (STRRAM).

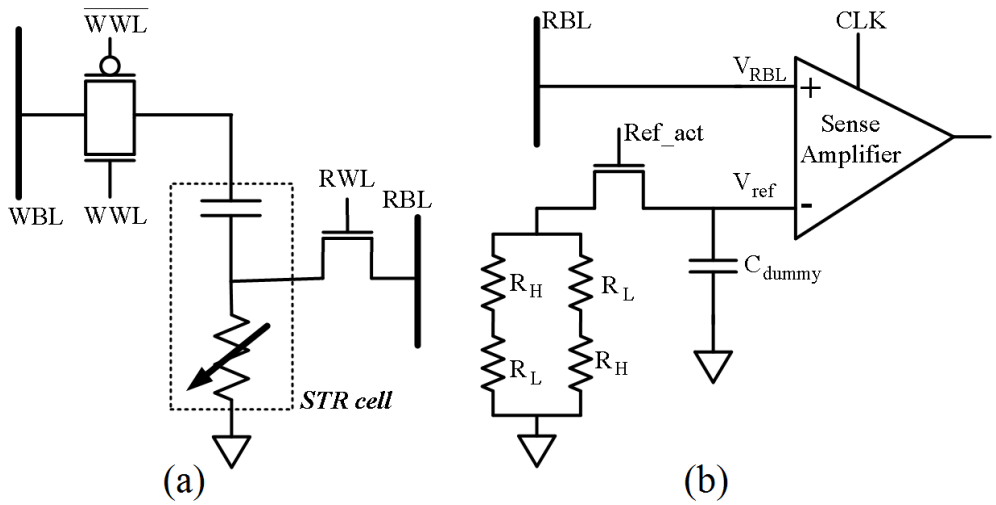

Figure 5-3 - (a) Proposed bitcell architecture, (b) Topology of reference cell and connection of RBL and reference line to SA

A. STRRAM bitcell design

Fig 5-3a shows the proposed bitcell architecture of the STRRAM. The read port of the STJ cell on the right side is connected to the free layer of the MTJ already demonstrated in Fig 2-2. An NMOS is used to access read bit line (RBL) as the RBL's voltage level is low. A transmission gate (TG) is used to access write word line (WWL) since high and low voltages are applied to the cell through this line.

Read operation is performed by sending a current through RBL and comparing the resulting voltage to the reference voltage (V_{ref}), using a sense amplifier (SA). The reference cell, demonstrated in Fig 5-3b, is made with MTJs that are pinned at high/low states leading to a reference resistance of $R_{ref} = \frac{R_H + R_L}{2}$. A dummy capacitance is used to relax the clock feedthrough from SA. The current through RBL is generated using voltage controlled current sources (VCCS) and is kept limited to a few micro-amperes. This leads to higher energy efficiency and avoids the STT effect. SA has a dynamic latched topology [112] in order to avoid static power dissipations. Differential pair transistors in SA are oversized in order to alleviate

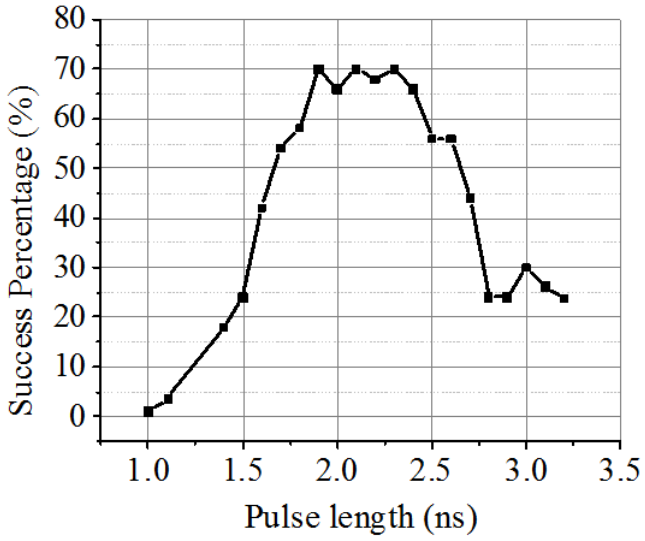

Figure 5-4 - successful flipping for different pulsewidth for a memory cell; it is interesting to observe that, while a pulse with a duration of 1.7ns~2.7ns guarantees flipping of the STJ on its own, when the device is incorporated into the memory cell, the success rate reduces to merely 65% for durations between 1.9ns~2.4ns

offset. At 1V supply level, SA has a delay of 106ps and an energy per operation of 24fJ. This assures that SA will neither be a speed nor an energy blockage for the entire system.

B. The write algorithm

The concept of successful pulsewidth was introduced in Section III as a measure for the pulse duration to *guarantee* magnetization flipping in the STJ. When the STJ is incorporated with CMOS, due to the limited rise/fall time of the pulse, circuit variations, node fluctuations, and timing skews, the final state is not always the same as what is expected from Fig 3-11.

In order to show this, we simulated P to AP switching in a memory bitcell for different pulsewidths. The results are shown in Fig 5-4. In the best case, pulsewidths between 1.9ns and 2.4ns have ~65% success. Therefore, a read operation should always be performed after a write attempt to check for flipping success.

As a result of above discussion, two write approaches are possible:

i. Apply 75mV pulse for 2.2ns, then let the magnetization vector relax and read. This approach has ~65% flipping success as discussed earlier.

ii. Apply 1V pulse for 200ps and go to the metastable point (where the magnetization vector settles along the minor axis), then let magnetization relax and read. This approach has a 50% flipping success.

Approach (i) takes almost 6ns while approach (ii) takes almost 4ns. While, in the long run, the two approaches provide almost the same write error probability ($0.35^{\frac{t_{write}}{6ns}} \approx 0.5^{\frac{t_{write}}{4ns}}$), approach (ii) leads to a simpler design. Therefore, we adopted this approach.

An attempt to write is called a "write-cycle". Multiple write-cycles might be required to achieve successful writing. This establishes a tradeoff between the total Write-time (i.e. the number of write-cycles) and the write error probability. The aforementioned tradeoff is analyzed in detail in

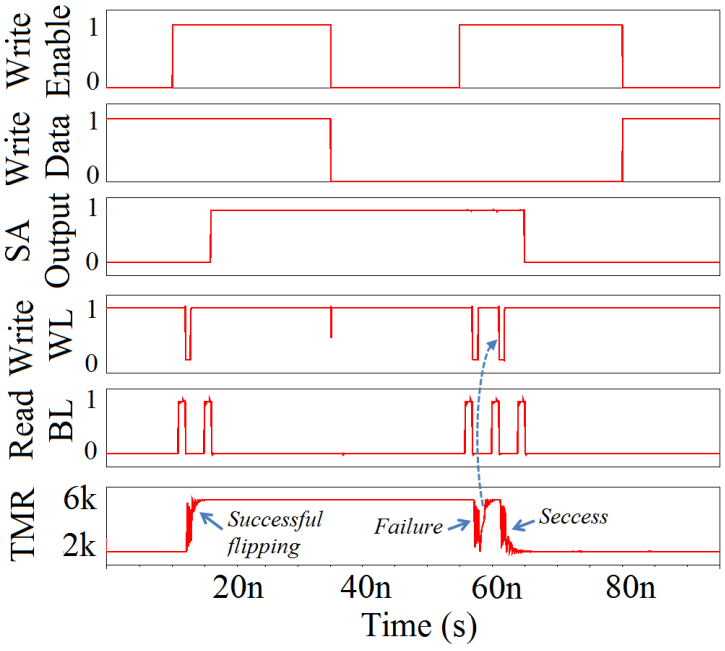

Figure 5-5 - Dynamic waveforms for write operation of logic 1 and 0; Upon receiving the write command, the memory performs a read to see if there is a necessity for writing. The logic 1 is successfully written into the memory on the first attempt. The logic zero, however, requires a second attempt as the first attempt fails to write.

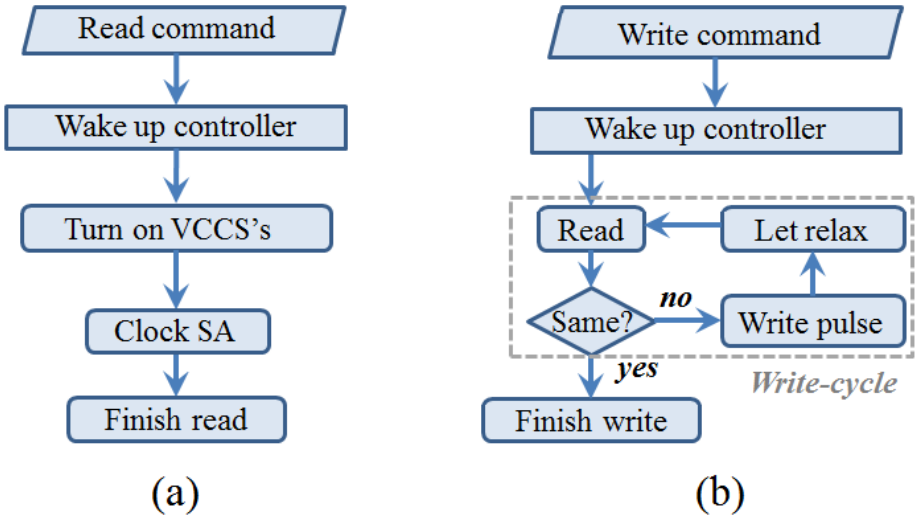

Figure 5-6 - (a) Read algorithm, (b) Write algorithm with the Write-cycle demonstrated

the simulation results of this section. Notably, other nonvolatile memories such as flash, resistive RAM and phase change RAM also require iterative methods.

Fig 5-5 illustrates the write operation for logic 1 and 0. Upon receiving the command to write logic 1, the memory performs a read to see if the bitcell data is different from the write data. Since it is the case, memory performs a write attempt, which is successful, and therefore, no more write-cycles occur. Writing logic 0 follows the same algorithm, however, this time the first write-cycle fails to write the data, and therefore, memory performs a second write attempt, which successfully writes the data into the cell.

The read and write algorithms are demonstrated in Fig 5-6. In order to maximize the energy efficiency and take advantage of the memory's non-volatility, the controller shuts off the entire memory when there are no read or write commands. Upon receiving any commends, the wake up controller fires a signal to turn the entire memory on and perform the operation, and upon finishing the read or write operation, the memory goes back to sleep mode.

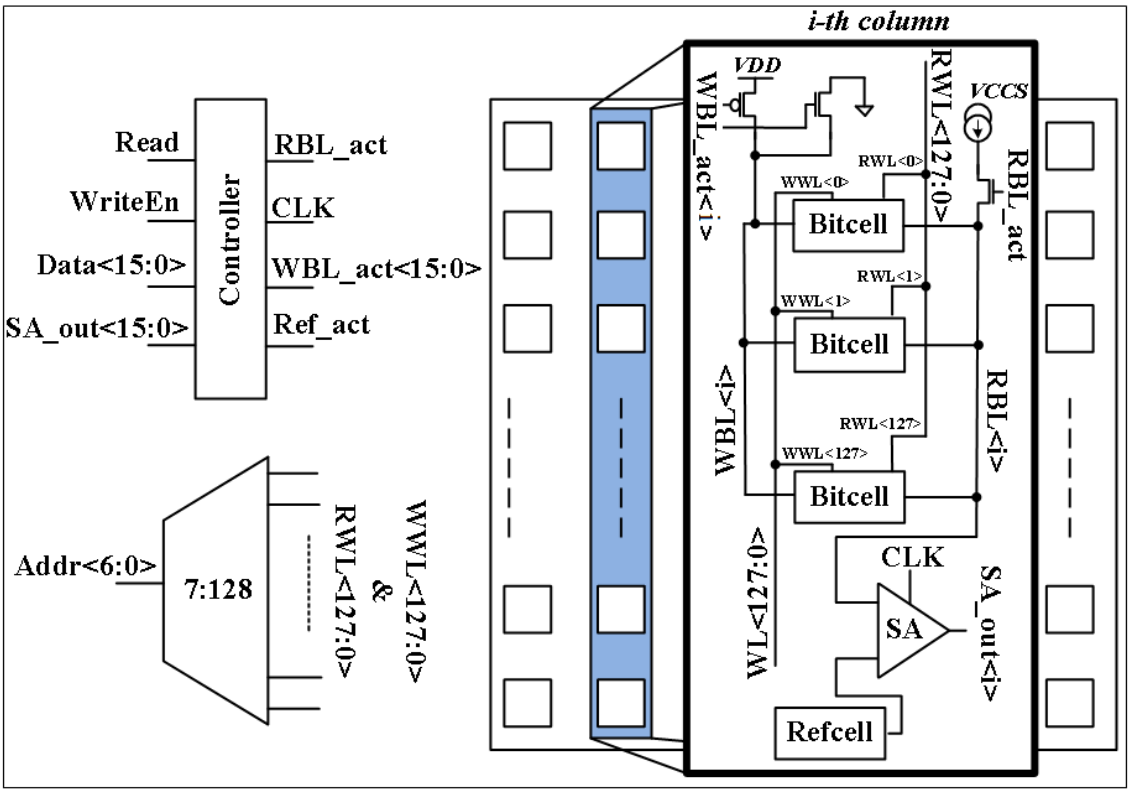

Figure 5-7 - 2 kilo-bit STRRAM architecture

C. Memory architecture

A 2k-bit memory is designed using the straintronics cells combined with the CMOS devices. The memory consists of 128 rows and 16 columns. Read and write operations are performed on 16-bit columns simultaneously. Fig 5-7 shows the topology of the memory. The controller uses a ring oscillator to generate the required signals, which automatically clock-gates itself when the read or write commands are performed. When reading from a cell, read word line (RWL) is activated, and the MTJ's state is detected using the VCCSs and the reference cell. When writing, write word line (WWL) is activated through the decoder. When not writing, the WBL is kept connected to ground to make sure that the top plates of the straintronics device will not reach the critical voltage due to leakage.

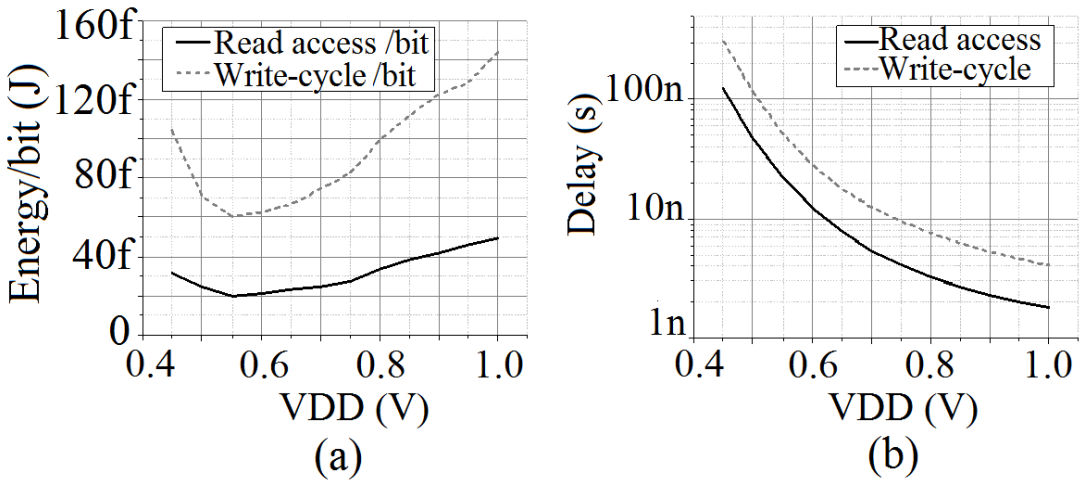

Figure 5-8 – (a) Read-access and write-cycle energies per bit versus VDD, and (b) Read-access and write-cycle delays versus VDD

D. Simulation results and comparison

The memory is designed and simulated in 65nm CMOS process with a 1V supply voltage. The axes of the device are chosen to be 205nm and 195nm. This provides an energy barrier of 125kT, which promises a storage class memory [113]. Given the cell architecture in Fig 5-3a, the cell size is limited to the CMOS devices and can be as small as 0.2 μm^2 as MTJ can be placed on top

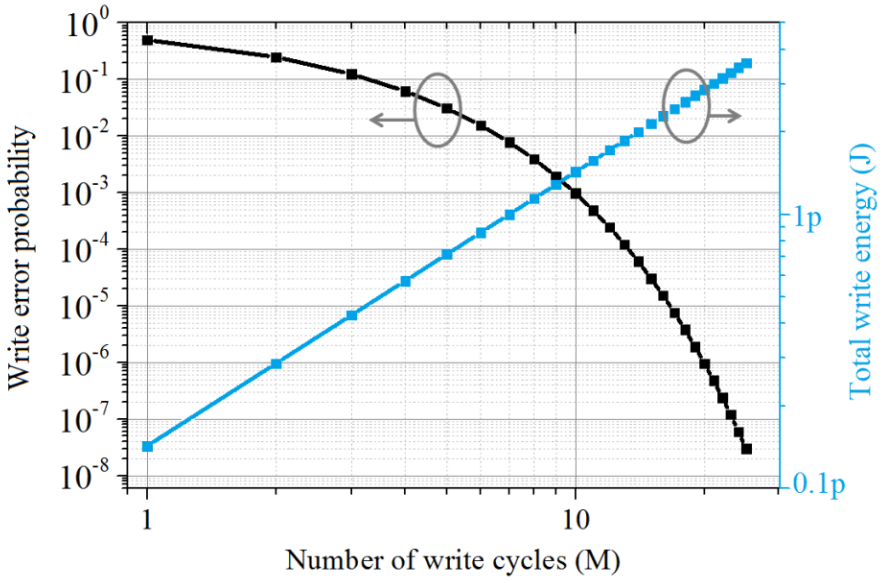

Figure 5-9 - The WEP – Write energy – Write speed trade-off due to the multiple Write cycle requirements

of the access transistors [114].

Fig 5-8a shows the energy/read-access/bit and the energy/write-cycle/bit as a function of the power supply level. Multiple write-cycles might be required to achieve successful flipping, as discussed earlier. The plots show their minimums at VDD=0.55V. Values below this supply level, lead to high leakage energy dissipations due to large delays, and therefore are not energy efficient. The energies reported here include the entire memory and are mostly due to the CMOS controllers. The straintronics device, on its own, dissipated only a small portion (less than %10 for write operation and less than %2 for read access) of these energies. Read and write delays significantly increase with the reduction of VDD as demonstrated in Fig 5-8b, mainly due to the slower ring oscillator in the controller block.

Having multiple Write-attempts establishes a trade-off between the number of Write cycles, M, the Write error probability (WEP) and the total Write energy, E_{write}, as demonstrated in Fig. 5-9. We have:

$$E_{write} = E_{write-cycle} \times M, \qquad E_{write-cycle} = E_{write-pulse} + E_{read}, \tag{5-1}$$

where, $E_{write-cycle}$ is the energy consumed in one Write cycle. As Fig. 5-9 indicates, within 20 Write cycles (equivalent to 80 ns total Write time, each Write cycle taking ~4 ns) a WEP less than 10^{-6} is achieved. This is much more efficient than the non-volatile charge based Flash memory, taking few micro-seconds for Writing. For example, the flash memory presented in [115] takes 20 μs for Write operation. Therefore, in a STRRAM, the Write error probability significantly decreases by adaptively adjusting the number of the Write attempts.

Table 5-1 - Comparison of STRRAM with different memories in literature

	Type	Tech	VDD	Cell Area (um^2)	E_{read} /bit (pJ)	Freq. (Hz)‡
[31]	SRAM (V)	65	0.4V	---*	0.011	475k
[115]	Flash (NV)	130	0.9V	0.276	2.38	50M
[116]	MRAM (NV)	90	1V	1.25	28.1	66M
[117]	DRAM (V)	65	1V	0.115	---	500M
STR [42]	STRRAM (NV)	65	1V	0.2**	0.049	562M

*A 6T SRAM cell for this technology typically takes $0.71um^2$
**Approximation, since MTJ lands on top of CMOS
‡Read frequency; Write-time for Flash in [115] is 20µs and for STRRAM and STTRAM is variable depending on the system tolerance on WEP.
⊥ The speed can be adjusted with varying current and error tolerance. The values are for 4ns delay with less than 10^{-6}error probability.

From the graphs in Fig. 5-9, it should be noted that while the Write energy increases linearly with M, the WEP decreases exponentially. For example, increasing the number of Write-cycles from $M = 10$ to $M = 11$ will halve the WEP in the expense of merely 10% increase in the Write energy. Therefore, a higher M is desirable for low-speed error-intolerant applications.

Fig. 5-10 demonstrates the STRRAM's performance as a function of the supply voltage. Even when operating in near threshold, the memory can read as fast as 10MHz.

We tabulated our results in comparison with the state-of-the-art present memory types in

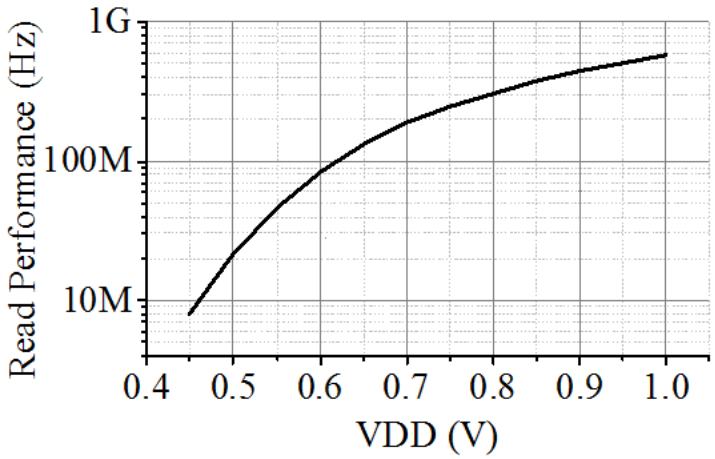

Figure 5-10 - Read performance of STRRAM when operating at different supply levels

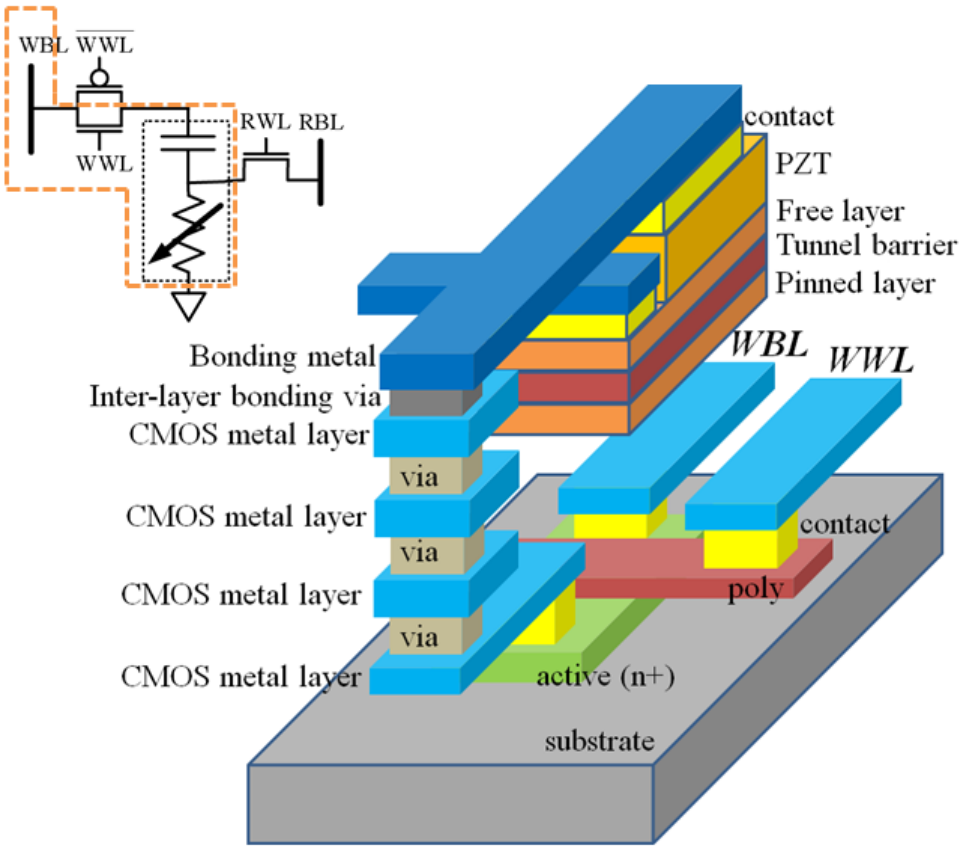

Figure 5-11 - Demonstration of the physical connection of the STJ to the NMOS access transistor as part of the bitcell layout

literature in Table 5-1. Various memories are designed for different applications. The SRAM in Table 5-1 shows a very low energy due to its sub-threshold operation. However, it operates at very low frequencies and cannot be used for high speed energy-limited applications. The flash memory has a moderate energy; but it should be noted that it has much lower data endurance than magnetic memories and has a large Write-time. The MRAM shows high energies and a large cell area. The DRAM, along with SRAM suffers from its lack of data retention in the absence of the supply voltage. The STTRAM has a moderate energy level that can be further improved using straintronics. STRRAM proves its capability to be the candidate for the future's universal memory.

Furthermore, in order to provide a fair comparison between the proposed memory and the emerging STTRAM technology, we have compared our memory specifications with the recent work in [97] in Table 5-1. While STTRAM is slightly more area efficient (1T1MTJ bitcell), it consumes a much higher energy for fast Write operation, leading to 170X higher energy delay product (EDP) for STTRAM. However, it should be mentioned that STTRAM performs Writing within one cycle, making it a faster memory compared to STRRAM. Read speed for both memories is about the same and is mostly limited by sensing circuitry since both designs performs reading by sensing the state of the MTJ.

Due to the low operating voltage of the STJ, the entire system can operate in deep sub-threshold regime. The full compatibility with deep sub-threshold operation while being immune to CMOS noise and fluctuations (due to the energy barrier) is one of the salient features of the straintronics device, which is not easy to achieve with FIMS and STT due to their high critical current values.

It has been practically demonstrated that MTJ can be fabricated on top of the CMOS circuitry to achieve higher design density [97]. Following the same design architecture, we demonstrated the proposed physical connection of the STJ and the NMOS access device in Fig. 5-9b. For simplicity

Table 5-2 - A comparison between STTRAM and STRRAM

	STTRAM [97]	STRRAM
Technology	45 nm CMOS	65nm CMOS
Operating voltage	1 V	1 V
Bitcell area†	$23F^2$	$42F^2$
Read delay	0.8 ns	2ns
Write cycle delay*	10.4 ns	4 ns
Write frequency	96 MHz	12.5 MHz at 10^{-6} WEP
Write energy	958 pJ at 96 MHz	2.86 pJ at 12.5 MHz
Write EDP	9.9 aJ.s	0.23 aJ.s

† Assuming minimum size access transistors for STRRAM since there is no high current flow limitations (F being the technology's feature size)

and ease of demonstration, the figure does not contain the entire layout of the memory cell and only includes the memory cell's NMOS access device connected to the STJ's PZT.

STRRAM, as introduced, proposed, and simulated, has the potential to push the energy limits of the nonvolatile memories further, while retaining the high read and write speeds. Due to non-volatility, STRRAM can be activated when computations are required, provide or store data at low energy costs, and go back to sleep. The memory also shows a high density with the cell size as small as 0.2 um^2. High energy efficiency, speed, data endurance, and data density makes STRRAM the perfect candidate to deliver the promise of the universal memory.

CHAPTER 6: PROPOSAL OF A PROOF OF CONCEPT TRUE RANDOM NUMBER GENERATOR

The concept of random number generation is easily understood from early childhood when we look into our experience of rolling a die, flipping a coin, or playing cards. As a matter of fact, if the coin or the die is flawless, a truly random outcome is expected. This is associated with the idea of a true random number generator (TRNG). Physical damage to the coin or the die can make the results more predictable, leading to a less reliable random number generator (RNG). In communication and cryptography, a predictable RNG will expose the sensitive data to the possible attackers. While the randomness of the output is the most important quality of an RNG, in real systems other qualities are also of crucial importance. For example, if an RNG consumes a significant amount of energy, takes up a large area or operates at very low speeds in order to achieve high randomness, it will not be practical in many applications. Lack of speed in random number generation can cause performance issues in web and mail servers [118]. As a result, a design for high speed, area efficient, and low power TRNG has been a focus of both software and hardware research for decades.

RNG's can be implemented using software algorithms [119-121]. While these algorithms usually produce pseudo-random numbers with many fewer design complications than hardware-based RNGs, they employ a general processor for their operation. This makes these software-

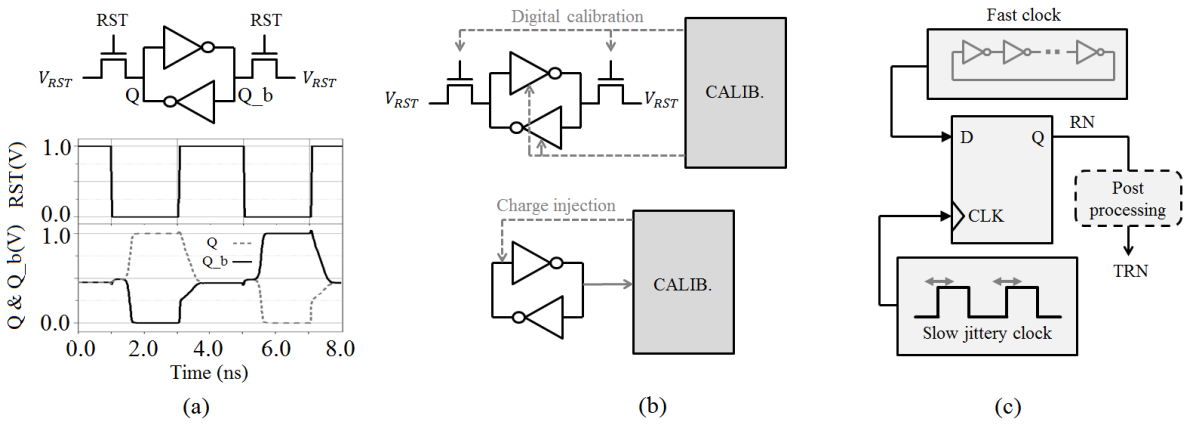

Figure 6 -1 - Taking the advantage of the metastability of the back-to-back inverter loop to generate random data, (b) Calibration of the back-to-back inverter loop using a controller circuitry or charge injection, (c) Use of fast clock and slow jittery clock to generate random numbers

based approaches power hungry and area inefficient. Also, since a general processor is not specifically designed for the purpose of random number generation, it will be generating random numbers at much lower speeds than the RNG hardware.

Integrated circuits (ICs) are widely used to implement RNGs in hardware. A variety of application-specific ICs are solely designed for the purpose of true random number generation [122-132] or pseudo-random number generation [133, 134]. They provide random numbers at much higher speeds, with much lower power and area overhead compared to their software-based peers. TRNG ICs use two popular approaches in order to generate random data: i) A metastable structure with a high gain can be used in order to amplify a small noise into a random digital binary data [122, 123]. This is demonstrated in Fig. 6-1a, where a back-to-back inverter is reset into a metastable state. Then, in the next cycle, the RST signal is removed and evaluation occurs. Due to the high gain of the back-to-back loop, one side randomly settles to logic one, while the other side settles at logic zero. However, due to mismatch and process variation, a single back-to-back loop will almost never generate a truly random number; and therefore, calibration is required. Different approaches are proposed for calibration. The work in [122] uses

a digital calibration scheme with delay elements and the inverter's pull-up and pull-down adjustments in order to achieve randomness as shown in Fig. 6-1b. Another approach is to use a feedback loop and inject charges to one side of the back-to-back loop in order to balance out the mismatch effect [123], which is also demonstrated in Fig. 6-1b. Both of these approaches, however, invest a significant amount of energy on calibration circuitry, and the core RNG (the back-to-back loop) ends up consuming a small portion of the total energy; ii) A high frequency clock can be combined with a low frequency jittery clock to generate a random sequence as demonstrated in Fig. 6-1c. The slow and fast clock generators usually consume a great deal of power and occupy a large area on the chip. The work in [126] uses this approach and consumes 0.23 nJ for each generated random bit. The work in [127] combines (i) and (ii) with discrete-time, chaos-based systems in order to achieve a better randomness. However, this makes the system area and energy inefficient, leading to 1.5 mm^2 area and 3.9nJ/bit energy consumption.

As we recall, the principle of straintronics states that in the presence of physical stress, the straintronics MTJ will settle into a metastable point, and upon removal of stress, it relaxes back at high or low resistance states. While this metastability can be bothersome for memory and logic design, it can be handy in the design of the TRNGs. Here, we exploit the metastable state of straintronics MTJ in order to build a TRNG. The modeling of thermal noise and the effect of process variation are analyzed. We interface our straintronics device with CMOS circuitry and use a time-interleaving approach to push the speed of the system to a few gigahertz.

A. Proposal of TRNG using the straintronics principle

As we recall, an applied voltage across the STJ creates an electric field, which leads to a strain in the PZT due to piezoelectricity. The strain is transferred to the free layer as a physical stress. If

the applied voltage is higher than the critical flipping voltage, V_C, the energy barrier will completely disappear; and the stress will force the magnetization vector to settle along the minor axis. Upon settling of the magnetization along the minor axis, portrayed in Fig 3-11, if the stress is removed abruptly, the device will suddenly enter a metastable state since the minor axis is now the magnetic energy maximum. The thermal noise will now push the magnetization vector towards the parallel or antiparallel orientation. The dynamic waveforms of the above steps were already demonstrated in Fig. 2-5, and the reader is encouraged to review it before proceeding with this chapter to get a clearer recall of the concept of metastability on straintronics devices. The applied voltage will make the magnetization vector settle along the minor axis ($\theta = \pi/2$). Upon removal of the applied pulse, the magnetization will randomly settle into either a parallel or antiparallel state, leading to a low or high R_{MTJ}, respectively. This is the basis of our proposed TRNG based on the straintronics principle. Due to the capacitive nature of the PZT, the amount of leakage current flowing through the MTJ, while applying the voltage, is within few nano-amperes; and therefore, STT effects are neglected.

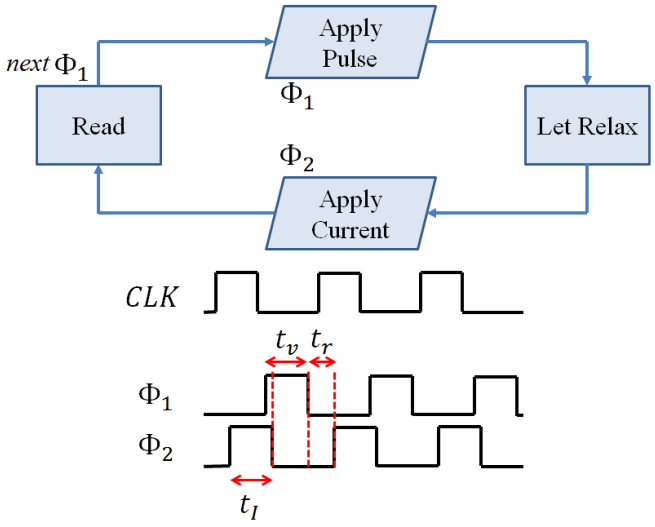

Figure 6-2 - Algorithm of the proposed TRNG with the control pulses

The proposed algorithm along with its timing information is demonstrated in Fig. 6-2. Two pulses, $\Phi_1$and Φ_2 with the same frequencies and different phases are used throughout the process. The pulses are generated in a controller unit using a clock signal. There are four different phases for generating a random bit. In the first phase, the Φ_1 pulse is applied across the device until the magnetization vector of the STJ settles along the minor axis. Then, the applied voltage is removed abruptly, allowing the magnetization vector to relax back along the major axis into either a parallel or antiparallel state. Depending on the parallel or antiparallel orientation, the MTJ will have a high or a low resistance value. Next, in order to read the final state of the STJ, we apply a current through the MTJ and evaluate the voltage. A high or low voltage is associated with the logic bits 1 or 0, respectively. After reading the state, the same procedure for random bit generation continues to output the next bit

B. TRNG performance and the choice of magnetostrictive material

Three different delays contribute to the timing diagram of Fig. 4 and dominate the speed of the TRNG:

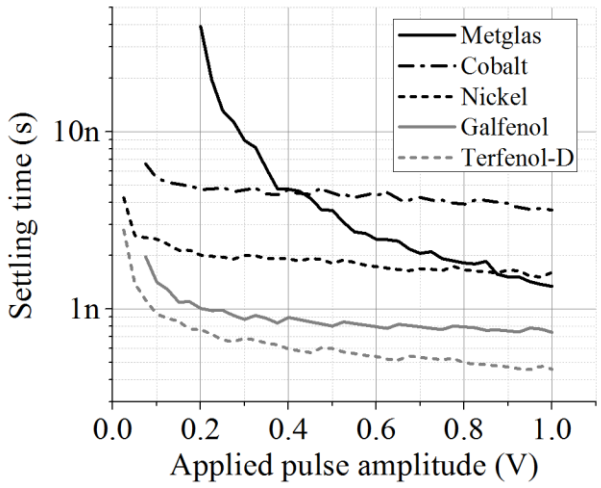

Figure 6-3 - Settling time as a function of the applied voltage amplitude for different materials.

a) t_v*:* The time required for the magnetization vector to rotate and settle along the minor axis. This delay is material and voltage dependent as demonstrated in Fig. 6-3, where we simulated the flipping delay of five different materials as a function of applied voltage. Due to the parameters in the LLG dynamics of (3-1), various materials demonstrate different delays. Metglas and Cobalt show slower responses while Galfenol and Terfenol-D are the faster candidates, mainly due to their higher magnetostriction coefficient. However, it should be noted that a higher applied voltage can contribute to more oscillations of the magnetization vector while settling along the minor axis [48]; and therefore, it is not always helpful to increase the voltage level to get a faster response.

b) t_r*:* The time required for the magnetization vector to relax along the major axis after the pulse is removed. There is no voltage dependency here, and t_r is solely material-dependent. The values of t_r for different materials are enumerated in Table 6-1, where, Galfenol is observed to relax back towards the major axis much faster than the other materials owing to its higher shape anisotropy energy.

c) t_I*:* The time required to reach a steady voltage on top of the MTJ when the current is flown through the device. This is a function of the resistance of the MTJ and the capacitance of the read-line, which mainly consists of the PZT capacitance. Therefore, t_I does not mainly depend on the magnetostrictive material.

Table 6-1 – Settling and relaxation time for different materials

	Terfenol-D	Nickel	Cobalt	Galfenol	Metglas
$t_r(ns)^*$	2.62	2.76	2.06	1.16	4.66
$t_v(ns)^*$	0.60	1.90	4.55	0.80	3.60

* The settling criteria is set to $\pi/10$ of the final state

As a result of the above discussions, Galfenol is chosen as the primary choice of the magnetostrictive material due to its fast response to the applied voltage and its quick relaxation time. This assures a fast pace for the random bit generation in our proposed TRNG.

C. TRNG Cell Design

CMOS circuitry can be used in order to generate the required control signals of Fig. 6-2 and to assist with reading the state of the MTJ. The proposed cell design that generates one random bit per clock cycle is demonstrated in Fig. 6-4. The signals V_{cont}, Φ_1 and Φ_2 are generated from a clock using a delay block. The STJ is a 3-port device as demonstrated in the figure, where the top plate voltage, , V_{cont}, is used to apply a high voltage across the device and push the STJ into the metastable state. The side port is solely used for reading the MTJ resistance and is inactive when V_{cont} is pushing the cell into metastability. Upon removal of V_{cont}, the device will settle randomly either into a parallel or antiparallel state. Then the current that is generated in voltage controlled current sources (VCCS) will flow through the MTJ in Φ_2 phase. Then the comparator will determine the state of the STR by comparing it to the reference cell. The VCCS current level

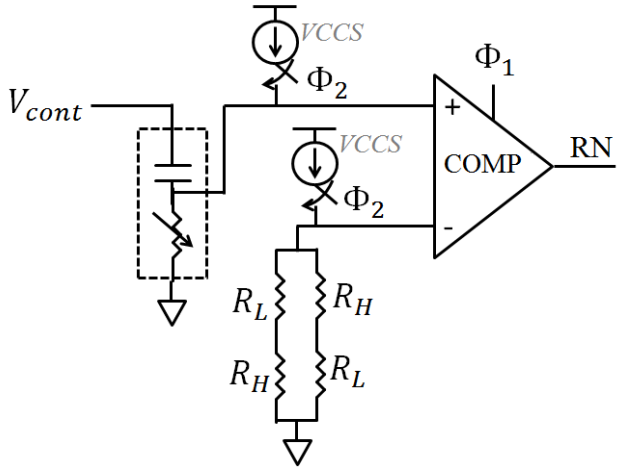

Figure 6-4 - The proposed schematic of the TRNG bitcell

is maintained within a few micro-amperes for two purposes: i) To keep the read energy low by restricting the total current driven from the VCCS over the entire read operation; ii) To assure that no spin transfer torque (STT) effect will happen [135]. The STT effect can cause an unwanted change in the state of the MTJ (read disturb). The reference cell is made with MTJs that are pinned into parallel and antiparallel states; therefore, the equivalent reference resistance will be $\frac{R_H+R_L}{2}$.

Fig. 6-5a demonstrates the random resistance generation (high or low) using the proposed bitcell. When the voltage V_{cont} goes high, the magnetization vector rests on the minor axis, where $\theta = (2i+1)\pi/2$. This means the MTJ resistance will settle to its middle value. Upon resetting V_{cont}, θ will settle along $2i\pi$ or $(2i+1)\pi$, leading to a low or high resistance value. For clarity, the final resistance level is also demonstrated on the figure.

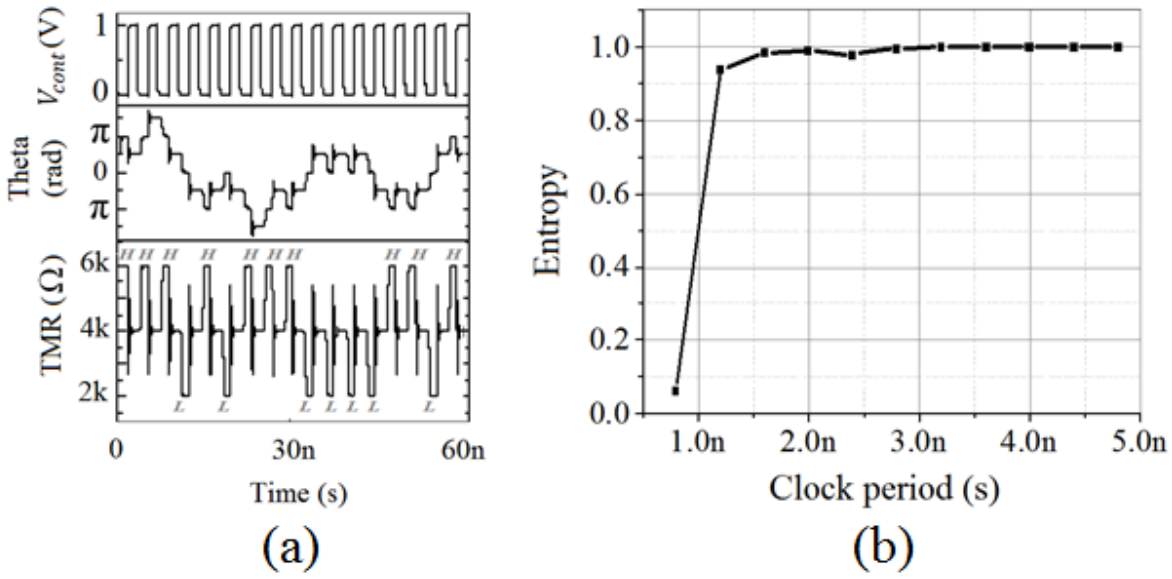

Figure 6-5 – (a) Demonstration of the random final resistance state of the MTJ when a rail of pulses is applied across the device, (b) Entropy of the TRNG bitcell as a function of the clock period

The highest rate at which the bitcell can generate random numbers is dictated by t_v, t_r, and t_I. This sets a minimum value on the clock period. If the period is shortened further, the magnetization vector of the free layer under stress will not have enough time to settle along the minor axis (shortage of t_v). Therefore, random number generation will not be guaranteed at very small clock period values since the system will not settle into the metastable state. This dependency of the randomness on the clock period is demonstrated in Fig. 6-5b, where, the entropy, H, of the random number generation is defined as:

$$H = -p(1)\times log_2 p(1) - p(0)\times log_2 p(0) \quad (6\text{-}1)$$

where, $p(0)$and $p(1)$are the probabilities of observing logic 0 and 1. As a result, the clock periods below 2ns can cause low entropy values and are avoided.

D. The Gigahertz TRNG

The single-bit TRNG demonstrated in Fig. 6-4 can be time-interleaved with similar single bit TRNGs in order to produce random numbers at a much higher rate. A single TRNG can generate random numbers reliably with a clock period of at least 2ns. This leads to a generator with 500MHz speed. Time interleaving these blocks can provide a random number generator with a few gigahertz of throughput. Here, we use a ring oscillator in order to generate the time

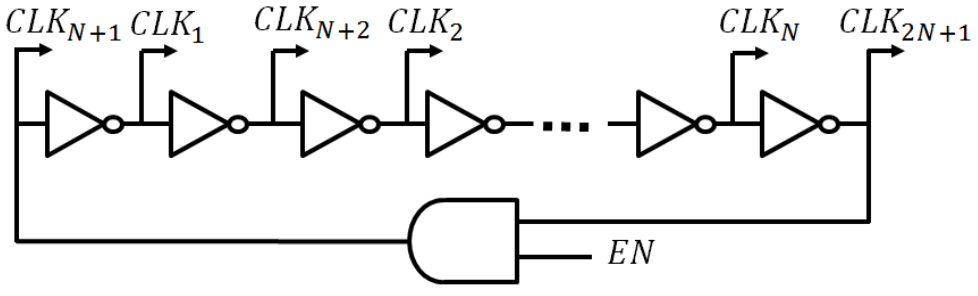

Figure 6-6 - The ring oscillator architecture used to generate the time-interleaved clock signals

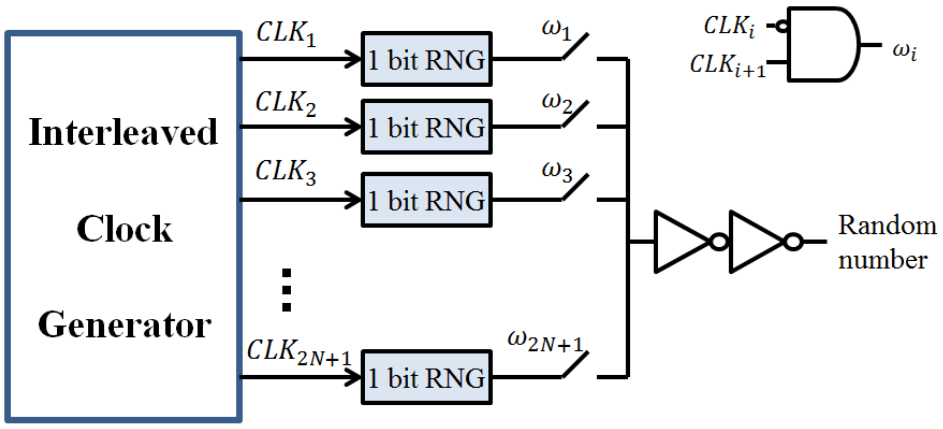

Figure 6-7 - The architecture of the time-interleaved gigahertz TRNG

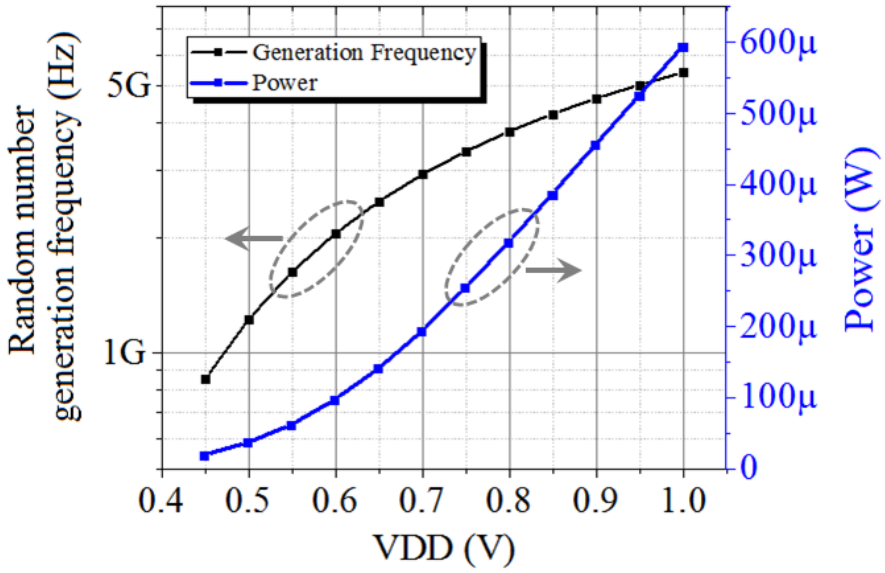

Figure 6-8 - The TRNG frequency and power as a function of VDD

interleaved clock signals for each RNG as demonstrated in Fig. 6-6. The devices in the oscillator are aggressively oversized both in length and in width in order to reduce the mismatch effects, which can cause timing errors.

The overall topology of the time-interleaved TRNG is shown in Fig. 6-7. The outputs of the single bit TRNGs are combined, using time-interleaved switches. The final output is buffered to assure the rail-to-rail swing of the output signal. The signals, $\omega_i, i = 1{\sim}2N + 1$ are used for the

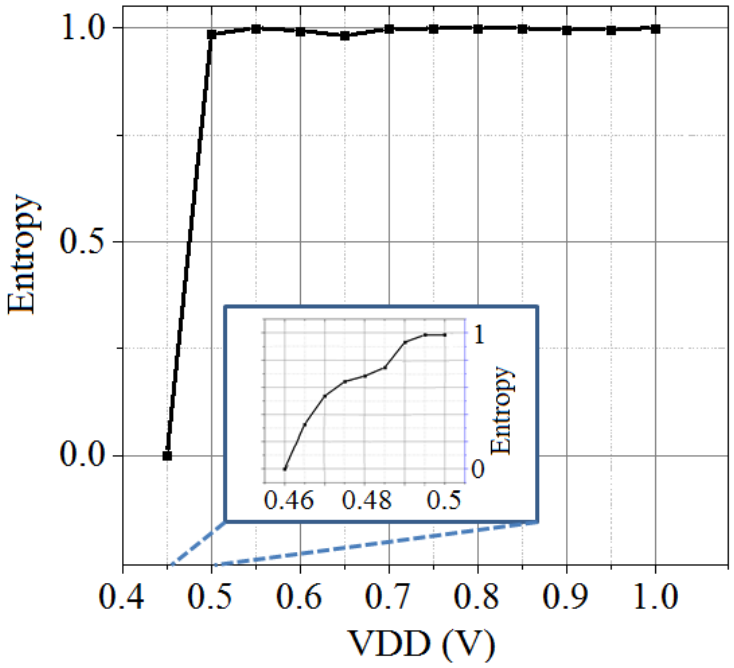

Figure 6-9 - Probability of logic one and the entropy as a function of VDD

time interleaved switches and are generated, using the time-interleaved clock signals as demonstrated in Fig. 6-7.

In this design we chose N=10, and thus, 21 time-interleaved blocks. This assures a few gigahertz of throughput for the TRNG while keeping the energy overhead small since every single TRNG is highly energy efficient.

E. Simulation Results

The time interleaved circuit demonstrates high performance, while retaining low values of energy and power dissipation. It is necessary to mention that the leakage power through the STR will be low as well due to the capacitive nature of the PZT. Therefore, the main source of leakage will be the CMOS control circuitry. At 1V supply level, the circuit generates random bits at 5.4GHz rate, while dissipating 594uW total power. The system consumes 110fJ/bit for random bit generation which is approximately 26x lower than the state of the art CMOS random number

Table 6-2 – A comparison of the proposed TRNG with the works in the literature

	[122]	[124]	[128]	This work	This work
Method	Back-to-back inverter loop	Fast clock and slow jittery clock	Synthesized 3-satge ring osc.	Straintronics metastability	
CMOS process	45nm	180nm	28nm	65nm	65nm
VDD (V)	1.1	1.8	0.9	1	0.5
Energy/bit (J)	2.9p	230p	23p	0.11p	0.03p
Throughput (Hz)	2.4G	10M	23M	5.4G	1.23G
Area(mm^2)	0.004	0.0016	0.000375	0.015	0.015

generator [122]. The entropy at 1V and 5.4GHz is simulated to be 0.999988.

The total power and the bit generation frequency of the system as a function of VDD are demonstrated in Fig. 6-8. Even at 0.5V, the frequency is still very high, showing a value of 1.23GHz, while consuming merely 30fJ/bit. The system merely dissipates 37uW at 0.5V VDD. However, it may be noted from Fig. 6-8 that reducing VDD to values below 0.6V leads to large delays. A comparison between the straintronics TRNG and the state-of-the-art TRNG hardwares in terms of speed, energy efficiency, and area are provided in Table 6-2. Major energy savings are accomplished due to the inherent energy efficiency of the straintronics devices.

We did not reduce the supply level to values below 0.45V since the system does not generate random bits for very low values of supply level as demonstrated in Fig. 6-9. This is mainly because the straintronics device does not have enough time to settle into the metastable state since the on-chip clock generator does not provide enough time margin for the device. As Fig. 6-9 indicates, the entropy quickly drops to zero when going down from 0.5V to 0.45V, which means the system will no longer operate as a random number generator.

Table 6-3 – NIST randomness test on 100 Kbits of the proposed straintronics TRNG

Test	Proportion*	Result?
Frequency	10/10	PASS
Block Frequency	10/10	PASS
Cumulative sums (forward)	10/10	PASS
Cumulative sums (reverse)	10/10	PASS
Runs	10/10	PASS
Longest run of ones	10/10	PASS
Rank	10/10	PASS
FFT	9/10	PASS
Non-overlapping templates	All sub-tests PASS	
Overlapping template	10/10	PASS
Approximate entropy	9/10	PASS
Serial	10/10	PASS
Linear Complexity	10/10	PASS

* Minimum passing rate of 8 for a sample size of 10 binary sequences, according to NIST test suit.

In order to test the reliability of the generated random numbers, the straintronics TRNG was tested using the NIST standard platform and the results are reported in Table 6-3. The proposed TRNG passes the performed NIST tests (meant for high security cryptographic systems), indicating the true randomness of the generated data. Due to the high energy efficiency and high performance, the straintronics-based TRNG can be the optimal candidate for both high speed and energy limited applications.

CHAPTER 7: EFFECT OF NANOMAGNET MISALIGNMENT ON THE FEASIBILITY OF THE MAGNETIZATION SWITCHING IN STRAINTRONICS DEVICES

Thus far, we have discussed major advantages of the strain-assisted switching over the conventional methods such as STT and FIMS. The energy and speed advantages and the incredible EDP trade-off was highlighted in Chapter 3 and Chapter 5. At this point, a bright engineer's mind would ask: Despite all the theoretical advantages, how practical is the principle? To answer this question, the reader should bear in mind that the straintronics technology is a very recent proposal with less than a decade of research and development. Hence, there is a long road to the maturity of this technology. Nevertheless, practical demonstration of the straintronics principle is a subject of research [136, 137]. Demonstration of the single nanomagnet's switching, regrettably, has not produced promising results [49]. The recent efforts to switch the state of nanomagnets that are placed on a PZT bed have demonstrated poor success rates with low endurances, as portrayed in Fig. 7-1, possibly due to piezoelectric layer (PZT) breakdown because of the application of high electric field to assist with switching. Investigation of the origin of such low yields is necessary in order to assure high success rates, required for adoption of the straintronics MRAM and logic by industries.

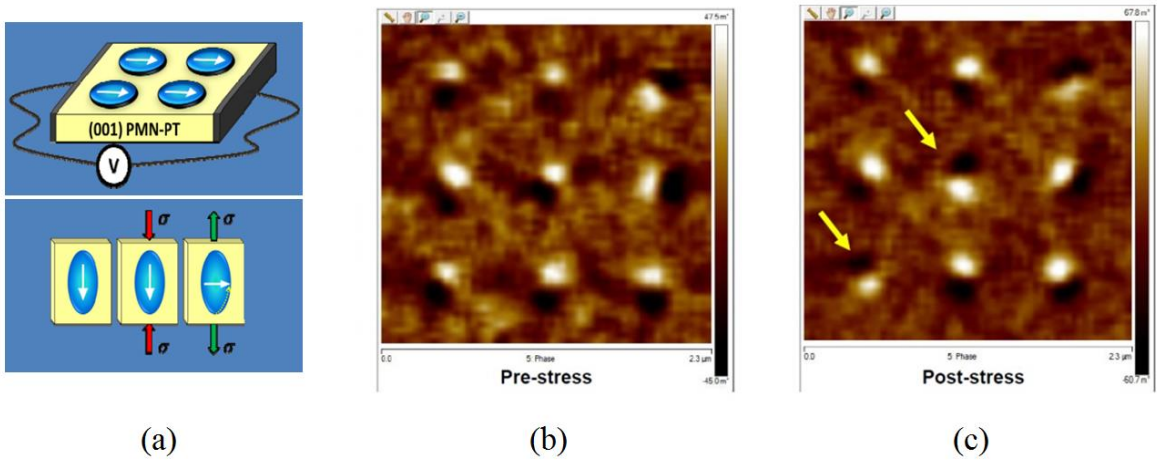

Figure 7-1 - (a) array of nanomagnets, placed on a PZT bed, demonstrating the test arrangement for practical demonstration of the straintronics device [49], (b) Micrograph of the nanomagnets before stress, and (c) micrograph of the nanomagnets after stress, showing merely 2 out of 9 successful switching [49]

Process variation is a naturally-occurring inevitable phenomenon when fabricating devices. The latter is more pronounced at smaller sub-100nm process nodes [138], mainly due to the large variations compared to the full length of the fabricated device. Such process variations, which can cause performance dissimilarities at chip-level designs, are modeled and studied well for conventional CMOS devices. Similarly, fabrication imperfections are inevitable when dealing with nanomagnets, and hence, the effect of them should be studied and modeled carefully. While the common theoretical assumption in the straintronics switching is that the nanomagnet's symmetry axis lies along the PZT's stress axis, perfect alignment is not guaranteed upon fabrication of the device. As a result, there will be some misalignment between the PZT's stress axis and the nanomagnet's minor axis, the effect of which on the functionality and magnetization switching needs to be studied.

This Chapter discusses the aftermaths of the process variations by analyzing the effect of misalignment between the nanomagnet's axes and those of the PZT. Through this analysis we realize that in the presence of misalignment, the magnetization switching pattern changes

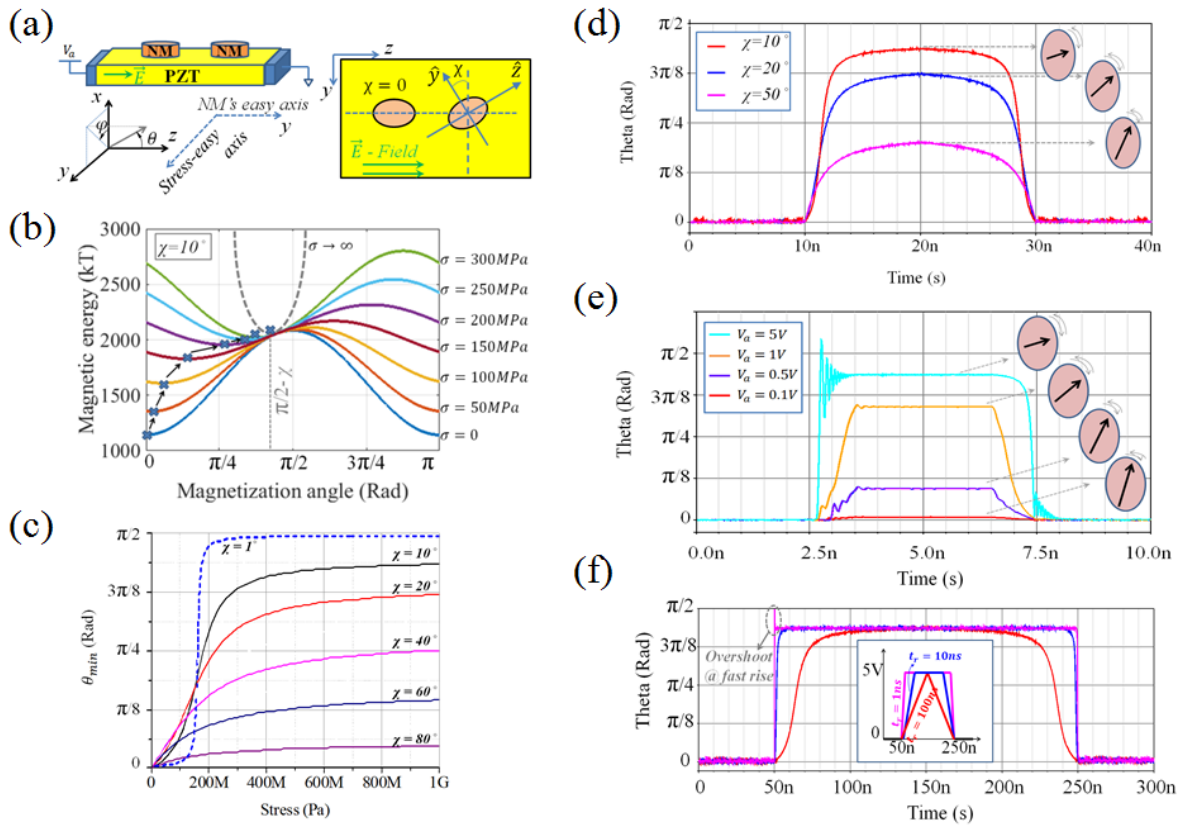

Figure 7-2 - (a) The left magnet is the ideal case and the right magnet is the case of misalignment; intuitively, the magnetization will want to align along the old y-axis, and hence, the nanomagnet's minor axis is no longer the favorite orientation under stress, (b) The magnetic energy of the misaligned nanomagnet, showing the smooth transition of the minimum point as stress increases, (c) The minimum energy point as a function of stress for various χ values, (d-f) Dynamic waveforms obtained by solving the numerical LLG dynamics, showing the dependency of the switching behavior on (d) χ, (e) V_a, (f) and t_r and t_f, the rate at which the pulse is applied and removed, respectively

drastically, leading to high switching failure probability, which can explain the low switching yields, observed in recent practical demonstrations of the straintronics principle [49].

A. Misalignment between PZT and free layer and its aftermath

The concept of misalignment between the stress axis of the PZT and the minor axis of the nanomagnet is portrayed in Fig. 7-2a. Ideally, the stress-easy axis lies along the minor axis of the nanomagnet, which is the case for the left nanomagnet on the PZT bed. This means, in the presence of stress, the magnetization's tendency to align along the minor axis increases.

However, due to fabrication flaws, the axis of the PZT and the free layer can misalign, characterized by an angle χ between the minor axis and the stress-easy axis, which is the case for the right nanomagnet in Fig 7-2a. Hence, defining the new *y*-*z* axes in Fig 7-2a, the stressed magnet will now have its magnetization tend to orient along $\theta_\sigma = \pi/2 - \chi$.

In the presence of misalignment, it can be obtained from Fig 7-2a that $\sin(\theta_\sigma) = \cos(\theta + \chi)$. Hence, the stress anisotropy of (2-5) now becomes $E_\sigma = \frac{3}{2}\lambda_s \sigma V \cos^2(\theta + \chi)$.

In the ideal condition, where $\chi = 0$, the qualitative magnetic energy, shown as a function of θ in Fig. 2-5 of Chapter 2, is symmetrical, and changes its minimum point from $\theta = 0$ to $\theta = \pi/2$ when stress reaches its critical point. The results for $\chi > 0$ are plotted in Fig 7-2b, where, it can be observed that as the stress increases, the minimum energy point smoothly shifts away from $\theta = 0$ and increases with stress. Eventually, as can be intuitively understood from Fig 7-2a, the final angle should be $\theta = \frac{\pi}{2} - \chi$. Hence, by observing Fig 2b, the following conclusions can be obtained:

I. In the presence of misalignment, there is no longer a sudden transition from major to minor axis at the critical stress level. Instead, as the stress increases, the energy minimum smoothly shifts from the minor axis towards $\theta = \frac{\pi}{2} - \chi$. The opposite happens as the stress is removed.

II. The orientation of the magnetization's easy axis (the minimum point in Fig 7-2b) is stress and χ – dependent. This is demonstrated in Fig 7-2c, where, a lower χ shows a more sharp transition and a higher final value. The minimum point, θ_{min}, is found by

combining (2-3) and including $E_\sigma = \frac{3}{2}\lambda_s \sigma V \cos^2(\theta + \chi)$ to obtain $E_{tot} = E_{sh} + E_u + E_\sigma$. When $\frac{dE_{tot}}{d\theta} = 0$, the minimum energy point is obtained:

$$\theta_{min} = \frac{1}{2}\tan^{-1}\left(\frac{\sigma \sin 2\chi}{\sigma_{Ci} - \sigma \cos 2\chi}\right), \tag{7-1}$$

With $\tan^{-1}$ defined between $(0, \pi)$. In (7-1), σ_C is the critical stress under ideal condition, obtained in Chapter 2. Note that the stress level, at which the denominator in (7-1) vanishes, $\sigma = \sigma_C / \cos 2\chi$, simply corresponds to the stress at which the magnetization easy axis passes through $\theta_{min} = \pi/4$.

III. Reaching $\theta = \frac{\pi}{2} - \chi$ requires the stress to be infinitely strong. This can also be observed from (7-1), where, as $\sigma \to \infty$, $\theta_{min} \to \frac{\pi}{2} - \chi$.

The above points manifest themselves in the magnetization dynamics simulated by solving the LLG equation numerically. Figure 7-2d demonstrates the effect of χ on the dynamic switching, where, a pulse with $V = 5$ V amplitude is applied across the device. Figure 7-2e shows the effect of applied voltage (associated linearly with the applied stress, as discussed earlier) on the dynamics when $\chi = 10°$. Note that even in the presence of very small voltages, the magnetization rotates slightly as expected from (7-1). Figure 7-2f shows the effect of stress's rise/fall time on the dynamic response. When the stress is applied and removed slowly, the transition of the magnetization is smooth; however, when high stress is applied rapidly, as observed from both Figs 7-5e and 7-5f, an overshoot is observed. This overshoot can be used to promote the successful magnetization switching in the presence of misalignment, as we will discuss below.

The fatal aftermath of misalignment on the straintronics magnetization switching is qualitatively portrayed in Fig 7-3a. While in the ideal condition, the magnetization suddenly rotates to the minor axis when $\sigma > \sigma_C$ and successfully switches with 50% probability, in the presence of even the slightest misalignment, the magnetization, in the absence of other factors affecting the magnetization dynamics, is doomed to return to its original orientation. Regrettably, such misalignments are inevitable due to naturally-occurring process variations, and perfect alignment of the nanomagnet and PZT can almost never happen.

In the presence of such conditions, when the magnetization settles along the final orientation,

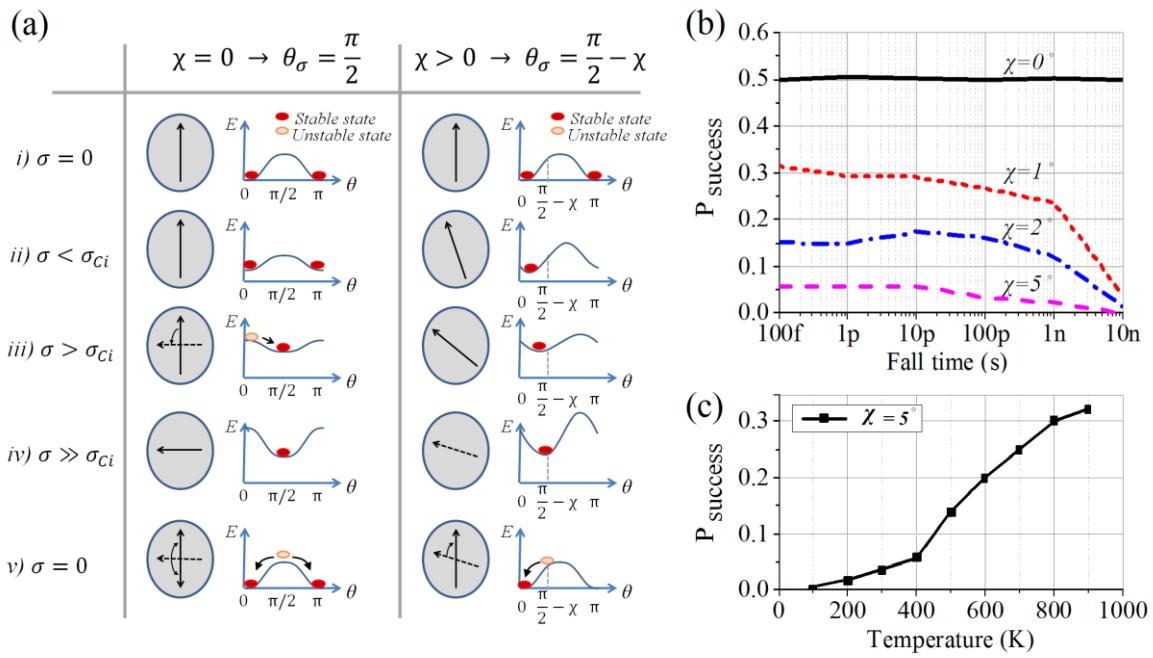

Figure 7-3 - (a) Qualitative demonstration of the magnetization behavior in the ideal case and in the presence of misalignment, showing the fatal aftermath of process variations, which forces the magnetization to return to its original orientation upon removing the stress, (b) Success probability using Monte-Carlo simulation results for when stress is retained to allow the magnetization to fully settle along its steady state and then stress is removed, in the ideal condition, success rate is 50%; however, as χ increases, the success rate shows a severe drop; the results also show that slow removal of pulse reduces the success rate, and (c) Effect of temperature on success rate, showing that more severe fluctuations at higher temperatures can assist with magnetization switching. Voltage of 1V is used for simulations in parts (b) and (c).

successful switching is only possible due to thermal noise. In other words, when the stress is removed abruptly in Fig 7-3a, even though the magnetization tends to return to $\theta = 0$, thermal fluctuations can push the magnetization above the hill and let it settle at $\theta = \pi$. Hence, the success will be temperature and χ – dependent, which is portrayed in Fig 7-3b, where, a 5 V pulse is applied, the magnetization is allowed to settle, and the stress is removed at different rates. It is observed that even $\chi = 1°$ dramatically reduces the chance to succeed and for $\chi > 5°$ failure is almost always guaranteed. It can also be concluded from Fig 7-3b that if the pulse is removed slowly, the magnetization switching has much lower chance of success. Success rates from Fig 7-3b can explain the low yields, below 30% in the best case, observed in the recent experimental attempts to demonstrate the straintronics principle.

The effect of temperature on the switching success of the magnetization is demonstrated in Fig 7-3c. As temperature increases, higher success is observed since more severe thermal fluctuations of the magnetization happen. The latter is because of higher thermal magnetic field and lower energy barrier at higher temperatures.

B. Pulse-shaping: The last resort

From the above discussion, it is understood that the straintronics magnetization switching has negligible chance of success in the presence of process variations if the magnetization is allowed to settle along the stress-easy axis. The latter can happen within nanoseconds. The mere success is due to thermal fluctuations. However, as observed in Figs 7-2e and 7-2f, sharp application of high voltages leads to significant overshoot. The dynamic waveform of the magnetization with perfect alignment, when a 1 V voltage is applied with 10 ps rise time is demonstrated in Fig 7-4a (top). In the presence of misalignment, the designer can take advantage of the overshoot in order

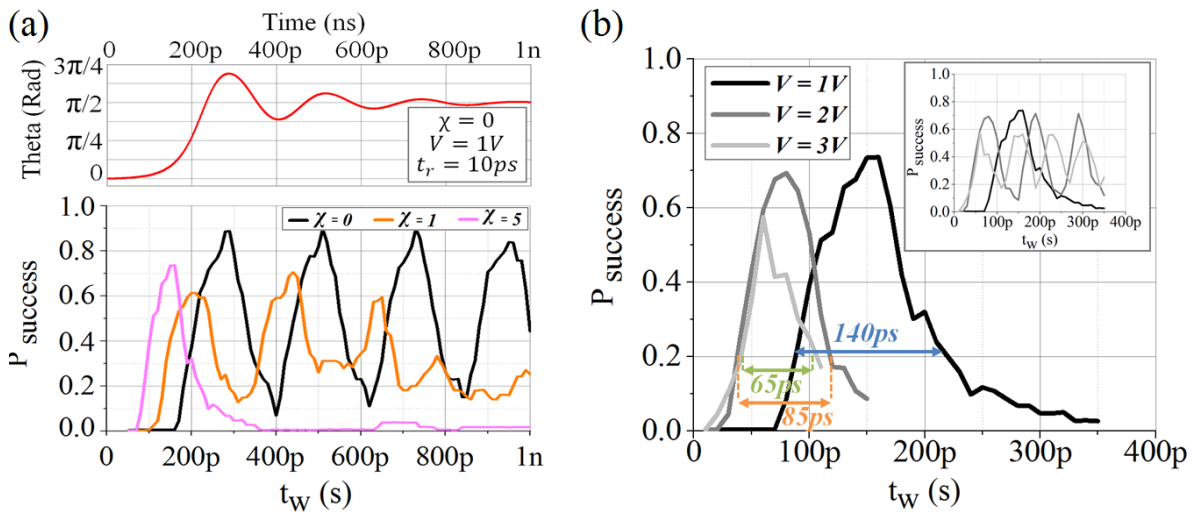

Figure 7-4 - (a) (top) Dynamic waveform of the magnetization when a 1V voltage is applied abruptly, showing multiple decaying overshoots, which can be exploited to achieve successful flipping in the presence of misalignment, (bottom) Switching success probability when the pulsewidth is tailored while keeping the amplitude at 1V and $t_r = t_f = 10ps$, demonstrating the peaks of success following the lobes of the top figure; note the perfect alignment of the top and bottom peaks at $\chi = 0$; as χ increases, the success peaks become weaker, (b) The effect of voltage amplitude on the success probability; showing that aggressively increasing the voltage would decrease success rate and width

to accommodate with switching. Switching success in the presence of misalignment can be accomplished if: i) Misalignment is small, typically less than 10 degrees; ii) A stress much higher than critical is applied fast (small pulse rise time, t_r), retained momentarily and tailored properly (small and adjusted pulsewidth, t_w), and removed abruptly(small pulse fall time, t_f) so that the magnetization, when overshooting, can swing and go over the energy hill in Fig 3a-*v* upon removal of stress. The effect of the latter approach on the successful switching probability is demonstrated in Fig 7-4a (bottom), using Monte-Carlo simulations. A 1 V pulse with $t_r = t_f = 10$ ps is applied with variable pulsewidth, and the success probability is recorded. The success pattern follows the top waveform pattern, which can be intuitively explained: If the pulsewidth is tailored such that the stress is removed at the peak of θ, then switching is highly likely. Note the perfect alignment of the peaks of the dynamic waveform on top and the success probability at $\chi = 0$ in the bottom figure. The switching success rate reduces as misalignment

increases, especially for the third overshoot and beyond. Also, as observed in the figure, the peak shifts to the left as χ increases, mainly because of a faster magnetization rotation in the presence of misalignment. The effect of voltage amplitude on the success rate (due to the first overshoot) when $\chi = 5°$ is compared in Fig 7-4b, demonstrating that having the voltage set too high would not necessarily benefit the system as it will make the overshoot very sharp, leading to a lower switching success within a narrower pulsewidth region. Nevertheless, obtaining successful magnetization switching, in the presence of misalignment, requires careful pulse shaping. Having a narrow range of allowable pulsewidth, demonstrated in Fig 7-4, makes the design of a circuit that generates this pulse a major challenge.

To recapitulate, despite the ideal case of PZT-nanomagnet alignment, where, the magnetic energy minimum abruptly switches between the major and minor axes at the critical stress, any slight misalignment will transform the switching pattern, forcing the magnetization to smoothly travel through a continuum of minimum energy points from $\theta = 0$ to $\theta = \frac{\pi}{2} - \chi$, as stress increases, and travel back as stress is removed. Hence, misalignment significantly hampers switching. Small success rates, when misalignment is minor, can be achieved due to thermal fluctuations. Furthermore, at the cost of careful pulse shaping, the designer can take advantage of the magnetization's overshoot in order to accommodate with the magnetization switching. Nevertheless, the principle of straintronics can still be employed in alternative device topologies, such as straintronics-assisted STT magnetization switching [139], magnetic domain wall propagation [137], and Bennett clocking of STT neural networks [44], exploiting its strain-driven magnetic force to assist with energy savings.

CHAPTER 8: CLOSING REMARKS AND FUTURE PATH

The research on straintronics devices and the straintronics random access memories, thus far, has focused on the analysis, modeling, and applications of the devices and their interface with CMOS circuitry as proof-of-concept designs. However, as highlighted in the previous chapter, the practicality of the straintronics principle, on its single nanomagnetic form, is not proven with high yields to grasp the industry's attention. Furthermore, as discussed in Chapter 7, any misalignment between the PZT and the free nanomagnetic layer can be a killer to the operation of the straintronics device. Hence, in order to remedy the latter, alternative device topologies should be employed or other magnetic forces, such as spin transfer torque current should be somehow combined with straintronics switching. Examples of the latter are investigated in some of the recent works [44, 139].

The straintronics research and development, as a result, should take a three pronged approach:

i) The physics of the device needs to be investigated in detail to realize other causes of the failure in recent attempts to demonstrate the principle [49, 136]. Besides process variations and misalignment, there are many possibilities that can contribute further to the failure of the magnetization switching. Examples of other imperfections can include possible pinning of the magnetization at the interface of the PZT and the nanomagnet.

Further, the strain transfer between PZT and the nanomagnet can be subject to lattice mismatch. Thus far, the theoretical assumption is that if the PZT-nanomagnet interface is large and PZT is much thicker than the nanomagnet, majority of strain will transfer from the PZT to the nanomagnet [40, 44, 54]. This assumption should be examined first by micro-analysis of the interface and later by atomistically modeling the interface to obtain the exact measure of the magneto-electric coefficient.

ii) Alternative device topologies that exploit the energy efficient straintronics principle should be investigated further. For example, Bennett clocking of the STT logic using straintronics will greatly save the switching energy of the STT method while speeding up the magnetization switching [44, 139]. In this method, a voltage is applied on the free layer to bring the magnetization close to the minor axis, and then, by applying a small current, the magnetization can switch very fast with a low energy overhead, owing to the high initial angle of the magnetization and the dependency of the STT's switching current and delay on θ_i. Other device topologies, such as mCell and mLogic [35], proposed recently for STT, can be implemented at much lower energy costs using the straintronics principle.

iii) Data storage capability of STJ should be further investigated. In this thesis, STR-RAM, as an energy efficient alternative to STTRAM was proposed. The proposed MRAM required iterative writing. However, alternative topologies, such as Bennett clocking of STT, stated above, can be used to re-design the STR-RAM and achieve deterministic writing at a low energy cost. Note that given the discoveries in the last Chapter, the iterative operation for STR-RAM would actually require many more write attempts since successful writing probability, in the presence of misalignment, degrades

dramatically. Hence, incorporation of straintronics into STT, not only will assist STT with the initial switching angle, and hence speed and power, but will also help with the functionality of the STJ.

iv) Applications beyond data storage can be the focus of future research and development. The use of straintronics in energy efficient neuron design [44], logic design [140], and random number generation [141] has been demonstrated. The use of the principle in large scale artificial neural networks (ANN) and further applications of the principle in other ASIC applications can be studied.

The above points can assist with ultimate implementation of straintronics in high-speed computer architectures. As portrayed in Fig. 8-1, the current generation of memory and storage suffers from speed inequality between volatile RAM (SRAM in cache and DRAM on main memory) and nonvolatile hard disk drive (HDD). While SRAM interfaces with central processing unit (CPU) at hundreds of pico-seconds of latency and DRAM operates at nano-seconds, HDD can store the permanent data no faster than few micro-seconds, leaving at least three orders of magnitude speed gap between RAM and HDD. Regrettably, flash memories also suffer from low speed of operation, and hence, replacement of HDD with high density flash memories would not solve the speed inequality. To this end, development of non-volatile memory and logic, using STT, straintronics, and the combination of two, stated above, can assist with filling the speed gap. Essentially, as demonstrated in Fig 8-1, the future big data storage will potentially incorporate spin-based computation into the CPU. Ultra-fast STTRAMs and STR-RAMs with low energy barriers, and hence, low data retentions (limited to seconds to minutes) will directly interface with CPU, and lastly, high speed non-volatile MRAM will be used to permanently store the data, removing the speed gap, and improving the performance of computer

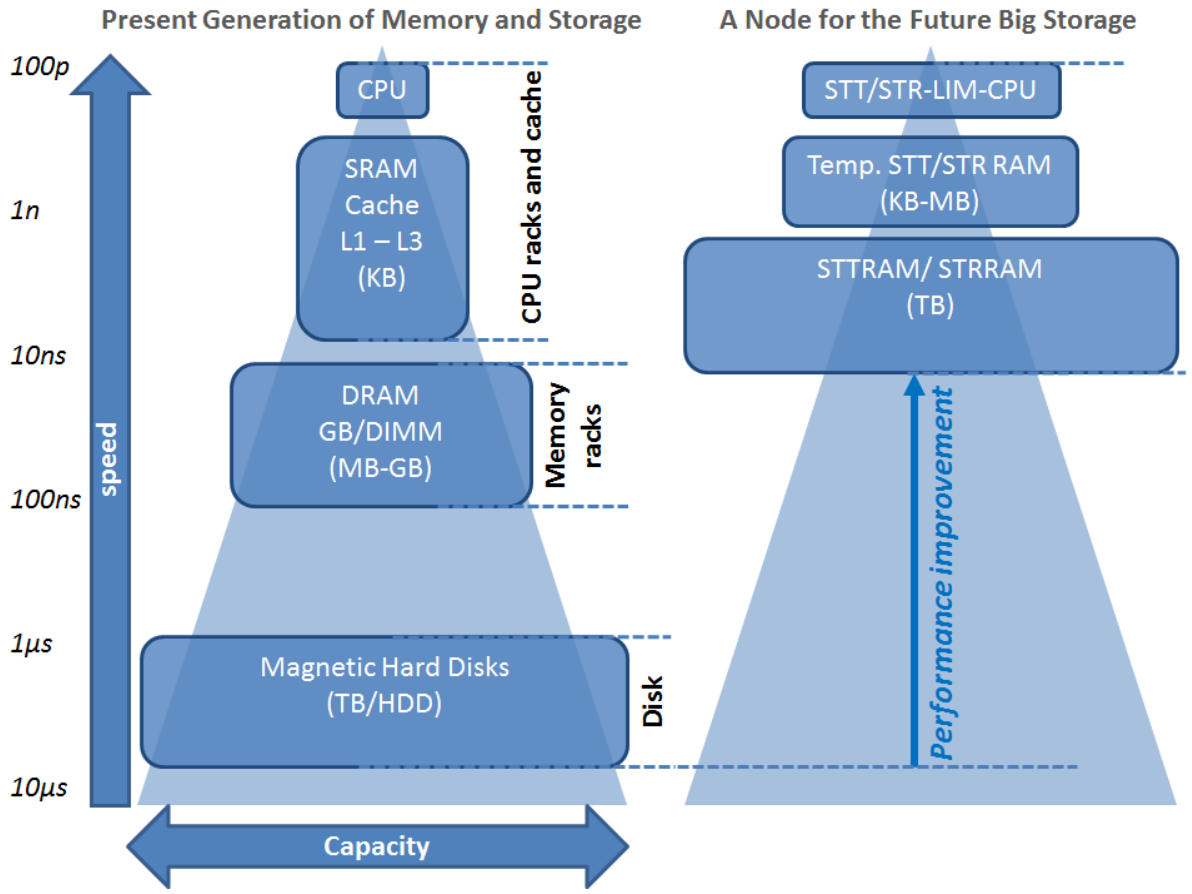

Figure 8-1 - (left) Present generation of memory and storage, demonstrating a large speed gap between RAM and HDD, and (b) A node for future big storage, where, spin-based computation remedies the speed inequality of volatile RAM and non-volatile HDD

systems drastically. The latter, while being a legacy with CMOS-only technologies, can be a dream-come-true thanks to the advances of post-CMOS STTRAM and STR-RAM.

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