LOW-NOISE ENERGY-EFFICIENT

SENSOR INTERFACE CIRCUITS

by

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To my family

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CHAPTER 1

Introduction

1.1 Sensors in the Internet of Things (IoT)

Continuous advances in semiconductor technologies have led to the era of the internet of

things (IoT). When the terminology is defined first, IoT was referred to network and devices
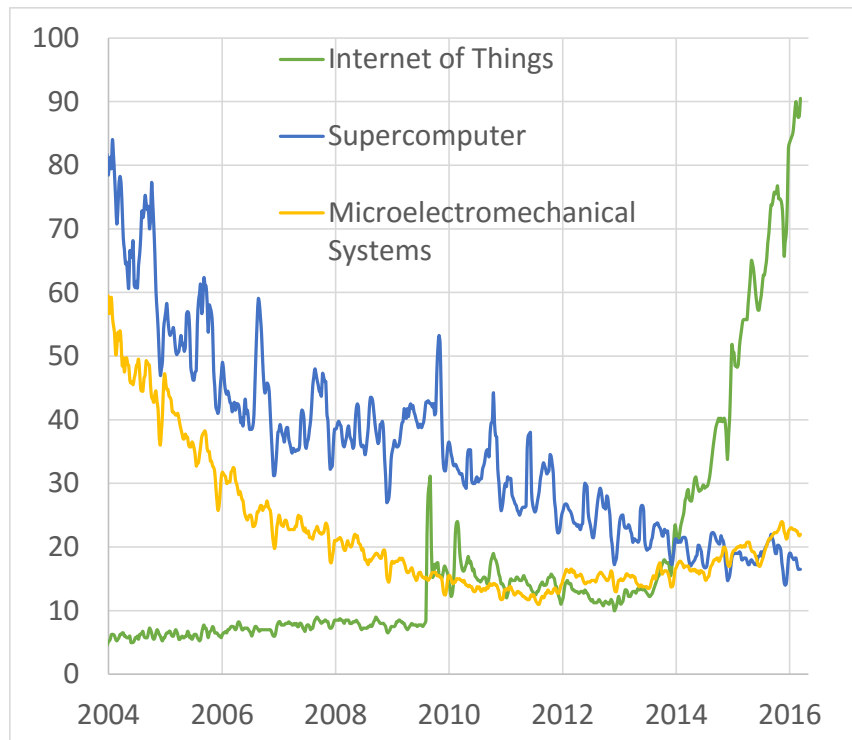
Figure 1.1. Interest over time, Web Search, Worldwide. Historical trends in Internet of

Things, Supercomputer, and Microelectromechanical Systems. (Source: Google Trends)

collecting data about RFID tagged objects. Today, the IoT is not only confined to RFID but is used as a concept of connecting any devices on the network where the environmental data around us are collected by sensors and shared across platforms [1], [2]. Figure 1.1 shows worldwide interest over time in IoT, supercomputer, and microelectromechanical systems (MEMS) in 2004-2016. The interest in the IoT has risen steeply by +900% during 2004-2016, but the interest in conventional high-performance computing has changed by -80% over the same period. We can also check the interest in MEMS, which is often used for an IoT sensor implementation, has rebounded with a recent IoT wave.

The IoT system is composed of sensors, processors, memories, power management units, and RF (Figure 1.2). The collected environmental data are analyzed, processed, and transmitted to other sensor nodes. Among them, it is largely relying on sensor technologies that enable all the smart objects to interact with the real world.
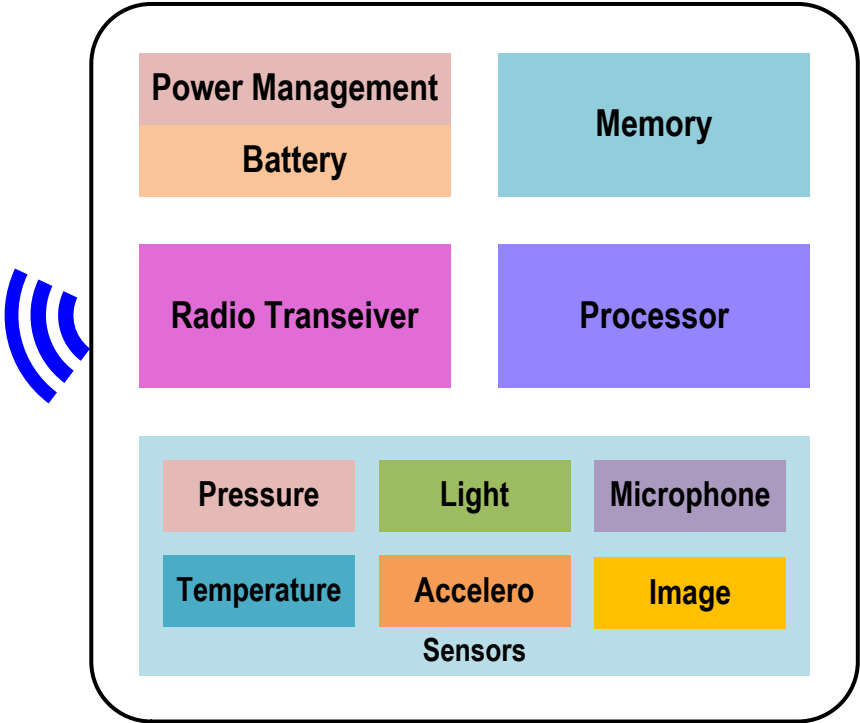
Figure 1.2. IoT Wireless Sensors.
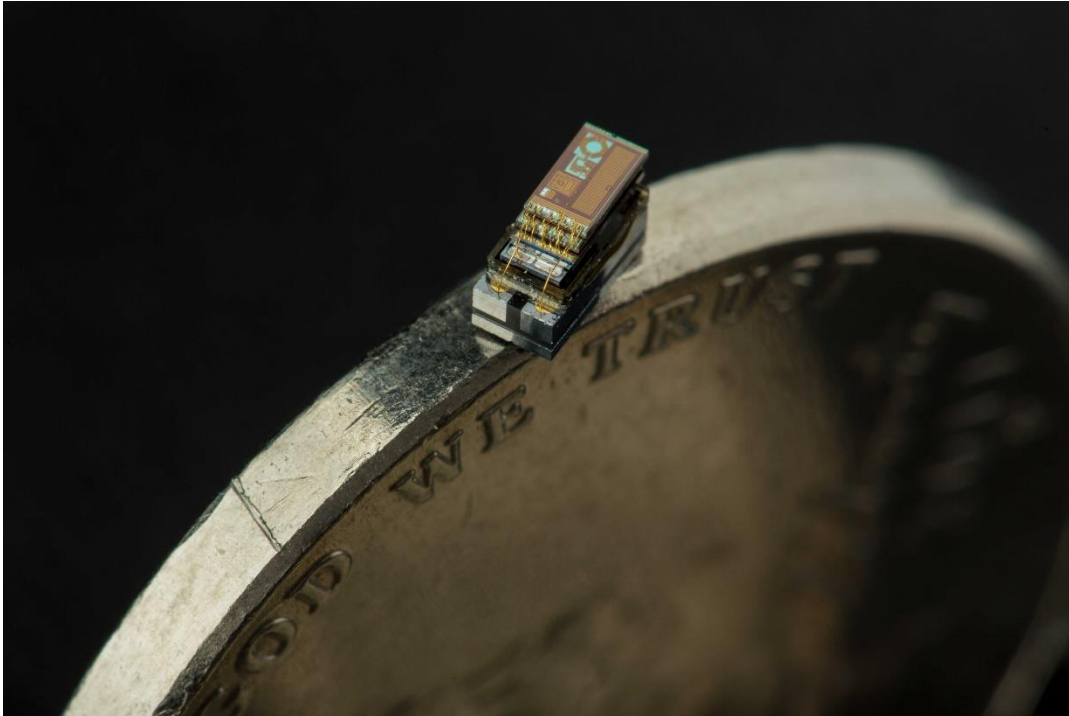
Figure 1.3. Pressure sensing millimeter sensor node

on the edge of a US Nickel.

One recent IoT trend is to integrate more sensors in a device. For instance, Galaxy S in 2010 only has 6 sensors but Galaxy S5 in 2014 has 16 sensors including fingerprint, heart rate, cameras, infrared gesture, microphones, magnetometer, proximity, RGB light, pressure, temperature, humidity, hall-effect sensor, accelerometer, and gyroscope. These sensors performance is being improved every year as well. They offer more features and user-friendly interfaces. Another trend and big challenge is a small form factor [3]. The size of a recent smart watch is approximately ten cubic centimeters, and the volume of the latest computing systems can be few mm^3 (Figure 1.3) [4]–[6] and the battery capacity is just a few µAh because of their size [7].

MEMS sensors are usually used for the system implementation because of small size and low price. Sensor interface circuits are placed next to the MEMS sensors and in the frontline of an application-specific integrated circuit (ASIC). Since sensor signal magnitude is small, the sensor

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output usually needs amplification as well as digitization and it may also include filtering. Because they should have low noise and often need an always-on operation, the sensor interface circuits can consume dominate system power. Therefore, low-power sensor interface circuit designs are critical in the system. An architecture of the interface circuits is chosen by based on sensor output characteristics such as resistive, capacitive, inductive, piezoelectric, thermocouple, and photodiode. The sensor interface circuits in the IoT collect and process sensor raw data from environment such as pressure [5], [6], [8], light [9], [10], microphone [11], [12], temperature [13], gyroscope [14], accelerometer [15], humidity [16], chemical [17], and magnetometer [18].

1.2 Outline of the Dissertation

The dissertation proposes sensor interface circuit techniques for a MEMS capacitive pressure sensor, infrared thermopile, and capacitive microphone.

In chapter 2, a dual-slope capacitance-to-digital converter for pressure-sensing is presented and demonstrated in a complete microsystem. The design uses base capacitance subtraction with a configurable capacitor bank to narrow down input capacitance range and reduce conversion time. An energy-efficient iterative charge subtraction method is proposed, employing a current mirror that leverages the 3.6V battery supply available in the system. Dual-precision comparators are also proposed to reduce comparator power while maintaining high accuracy during slope conversion, further improving energy efficiency. The converter occupies 0.105mm^2 in 180nm CMOS and achieves 44.2dB SNR at 6.4ms conversion time and 110nW of power, corresponding to 5.3pJ/conv•step FoM. The converter is integrated with a pressure transducer, battery, processor, power management unit, and radio to form a complete 1.4mm×2.8mm×1.6mm pressure sensor system aimed at implantable devices. The multi-layer system is implemented in 180nm CMOS.

The system was tested for resolution in a pressure chamber with an external 3.6V supply and a serial communication bus, and the measured resolution of 0.77mmHg was recorded. It is demonstrated that the wireless readout of the pressure data on the stack system operating completely wirelessly using an integrated battery.

Chapter 3 discusses an incremental zoom-in capacitance-to-digital converter (CDC). By using a 9b successive approximation registers (SAR), the oversampling ratio (OSR) can be reduced to only 32, significantly improving conversion energy. We show how amplifiers are bypassed during SAR phase further reducing energy and propose a novel matrix based 512-element unit-cap structure for dynamic element matching. The CDC achieves 94.7dB SNR and 33.7μW power consumption with 175fJ/conv-step at 1.4V supply.

Chapter 4 describes a low-power infrared motion detection system suitable for smart devices such as wearables. The system incorporates instrumentation chopper amplifiers (ICA), LPFs, ADCs, and a DSP. The low-noise ICAs amplify very low frequency μV-level thermopile outputs with 2.0 NEF and provide programmable gain modes. To reduce standby power the ICA uses lower current when the system is in idle mode. Wakeup can be triggered by detection of a simple gesture. For the LPF, source degeneration by pseudo-resistors and g_m division techniques are used for both improved linearity and 30Hz bandwidth. The DSP employs a motion history image technique to achieve low-power detection. The system consumes 260μW in active mode and 46μW in idle mode while processing 16×4 infrared data at 30fps. A complete system demonstration is shown.

Chapter 5 proposes a switched-bias preamplifier for a MEMS capacitive microphone. It utilizes switched-MOSFET, periodic on/off switching of a MOSFET between strong inversion and accumulation, to reduce 1/f noise inherently. The preamp achieves 6.3μVrms input-referred noise

(A-weighted) with 7.6μA, improving the best-reported NEF by 3x. The preamp is integrated with a MEMS sensor on a chip-on-board and tested in an anechoic chamber. Acoustic test shows 61.8dBA SNR and -29.5dBV sensitivity at 94dB SPL.

Lastly, chapter 6 summarizes the contributions in this dissertation and proposes future directions.

CHAPTER 2

A Dual-Slope Capacitance-to-Digital Converter

for an Implantable Pressure-Sensing System

2.1 Introduction

Implantable systems are increasingly in demand for emerging biomedical applications, and yet they face stringent power budgets because battery capacity is limited due to their small volume [4], [5]. These systems collect and analyze sensor data, which is often measured in the form of capacitance. Capacitive sensor interfaces are widely used because of their inherent energy benefit; i.e., they do not draw static current, unlike resistive sensors. However, a capacitive sensor interfacing circuit could dominate system power, and hence an energy-efficient capacitance-to-digital converter (CDC) is required. Capacitive sensors, along with a corresponding CDC, are used in diverse applications such as pressure-sensing [19], humidity-sensing [16], proximity-sensing [20], and microphones [21].

Pressure-sensing is a key technique used in implantable devices with applicability to glaucoma treatment [5], [22], blood pressure monitoring [23], and tumor diagnosis, among others. These systems typically use a MEMS capacitive sensor and they require a moderate-resolution (9-10b), low-power CDC. Dual-slope converters are well-known for their simplicity, accuracy, and low power consumption [24], [25]. However, their nominal base capacitance is often quite large
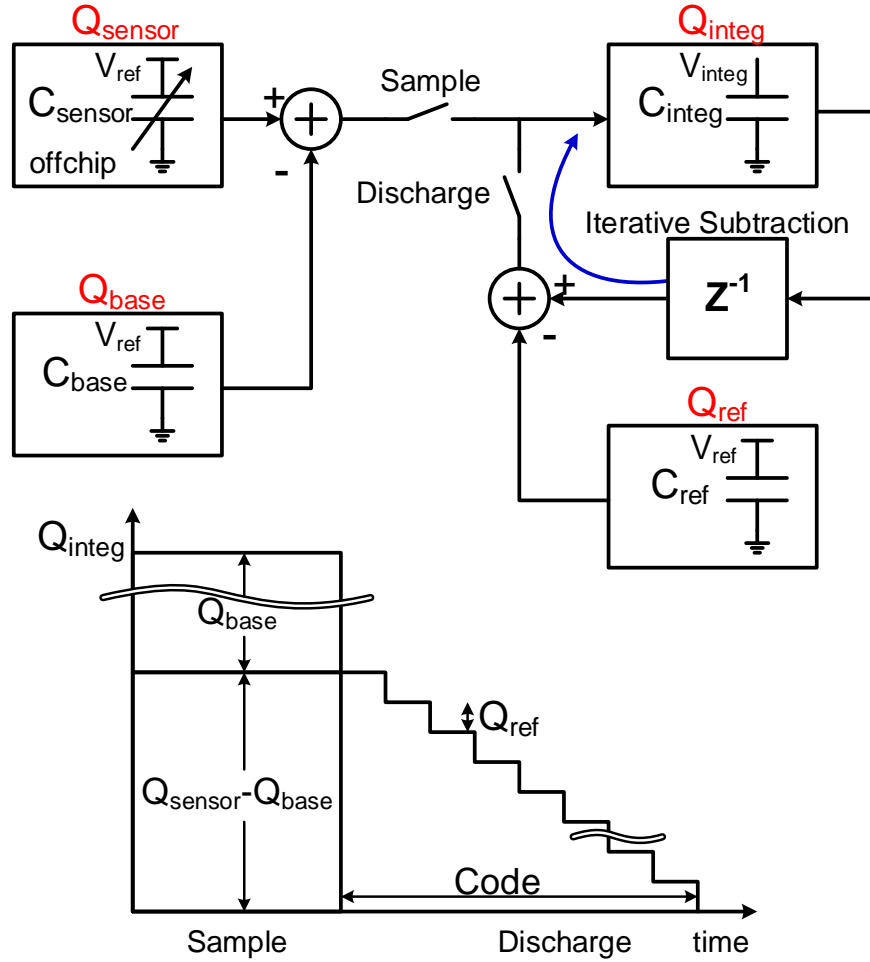
Figure 2.1. Block diagram of the proposed CDC and an associated waveform.

compared to the capacitance changes due to pressure variations. The need to charge and discharge the large base capacitance in dual-slope CDCs (DS-CDC) makes it difficult to achieve sufficient resolution with high energy efficiency.

To address this challenge, we employ iterative charge subtraction/accumulation using a configurable capacitor bank to cancel base capacitance, and to zoom in and amplify the variable input region [16], [20]. This reduces the conversion time and energy for the DS-CDC (Figure 2.1). The design also uses dual-precision comparators to achieve the high-resolution of a fine comparator with the low power consumption of a coarse comparator [6], [19]. It does this by
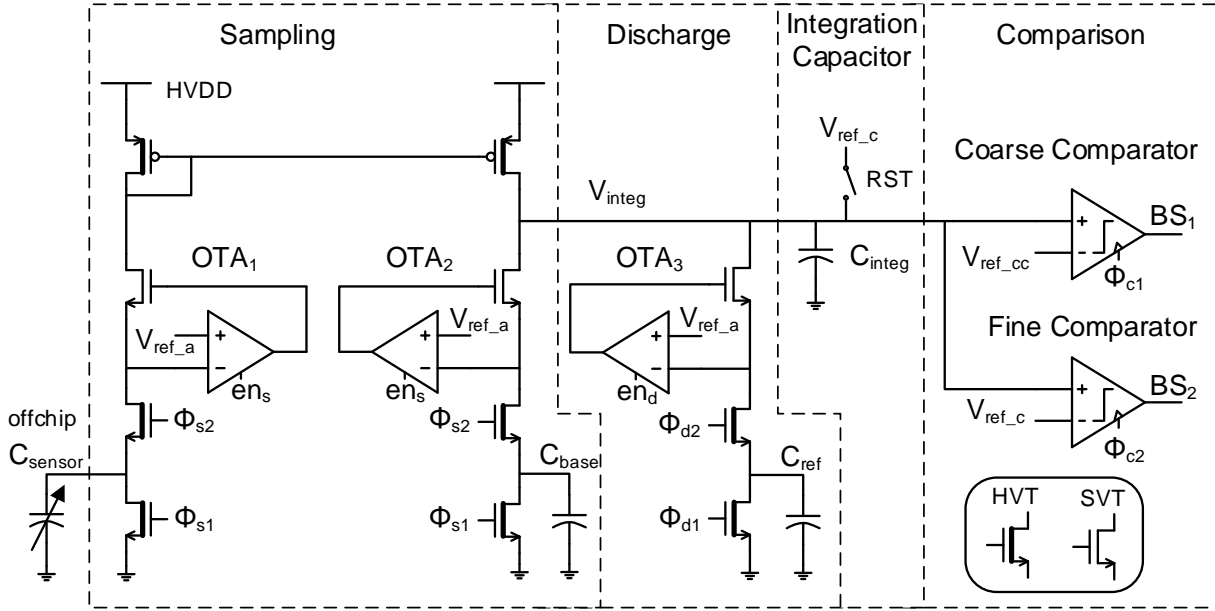
Figure 2.2. Circuit diagram of the dual slope CDC.

enabling the fine comparator only in the final stages of conversion. The CDC has a low power consumption of 110nW, which makes it compatible with ultra-small batteries that often suffer from low peak current capacity. We demonstrate CDC operation that is integrated with a complete pressure-sensing system using a MEMS pressure sensor, processor, memory, battery, and radio.

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2.2 Dual-Slope Operation

Figure 2.1 shows a simplified block diagram of the proposed DS-CDC. The sampled charge difference between C_{sensor} and C_{base} is transferred to C_{integ}, and the transferred charge is removed by iterative subtraction using C_{ref}. The CDC circuit consists of a current mirror, charge subtraction/accumulation devices, and two comparators (shown in Figure 2.2), followed by a ripple carry counter and digital control logic.
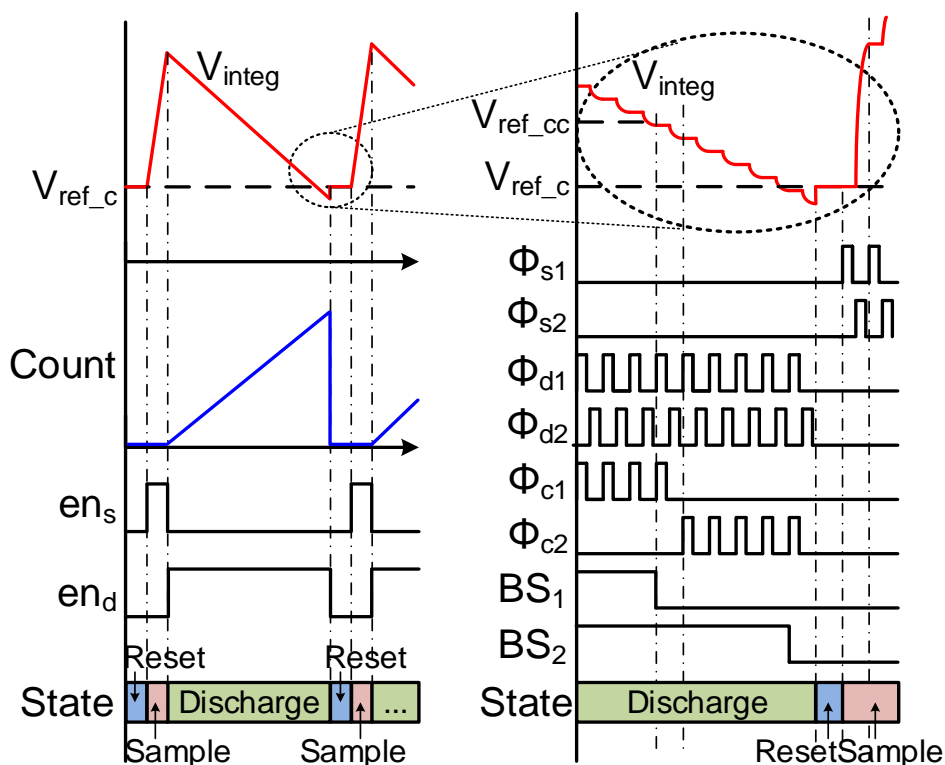
Figure 2.3. DS-CDC waveforms.

Figure 2.3 shows the waveforms in the DS-CDC. During the reset state, all of the OTAs are disabled, and the RST switch is closed to set the voltage of C_{integ} to V_{ref_c}. In the next sampling state, the OTA$_1$ and OTA$_2$ are enabled. While Φ_{s1}=1, the charge is removed from C_{sensor} and C_{base} by shorting both nodes of the capacitors to ground. With Φ_{s2}=1, the top plate nodes of these capacitors are set to V_{ref_a} due to the feedback of the OTA and the device gated by Φ_{s2}. Since Φ_{s1}=0 in this phase, all current conducted by the source followers is accumulated on C_{sensor} or C_{base}. The

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OTAs drive the source followers to track V_{ref_a} with little error, and a current mirror above the source followers flips the direction of current from C_{sensor}. As a result, the amount of transferred charge Q_{add} added to C_{integ} (4pF) for each Φ_s cycle is:

$$Q_{add} = (C_{sensor} - C_{base}) \times V_{ref\_a} \tag{2.1}$$

The full sampling operation consists of $4\Phi_s$ cycles, during which $4Q_{add}$ is transferred, thus providing 4× charge amplification.

In the following discharge state, OTA3 and one of the two comparators is turned ON. Similarly, the amount of charge that is subtracted from C_{integ} for each Φ_c cycle (denoted Q_{sub}), and the value of V_{integ} at the end of nth cycle of the discharge stage are given by:

$$Q_{sub} = C_{ref} \times V_{ref\_a} \tag{2.2}$$

$$V_{integ}(n) = V_{ref\_c} + (4Q_{add} - n \cdot Q_{sub})/C_{integ} \tag{2.3}$$

C_{ref} (18fF) is composed of two MIM capacitors in series. The discharge state ends when V_{integ} becomes smaller than V_{ref_c}; the total number of required cycles is recorded by a ripple carry counter as the digital code.

$$Code \cong 4Q_{add}/Q_{sub} = 4(C_{sensor} - C_{base})/C_{ref} \tag{2.4}$$

In the proposed CDC, C_{sensor} is an off-chip sensor capacitor, and C_{base} is a programmable on-chip MIM capacitor bank composed of capacitors and NMOS switches, allowing for adjustment of the capacitance measurement range. V_{ref_a} is 300mV and each C_{base} has a 4pF linear range, and thus the maximum $4Q_{add}$ difference is 4.8pC between the smallest and largest inputs from (2.1). ΔV_{integ} and $\Delta Code$ are 1.2V and 890 from (2.3) and (2.4), respectively, and the LSB voltage is 1.35mV. Although C_{sense} and C_{base} can be larger than C_{integ} since both C_{sense} and C_{base} are simultaneously clocked, V_{integ} is not saturated as long as $4 \cdot (C_{sense} - C_{base}) < C_{integ}$. The sensor

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capacitance changes due to an environment signal such as pressure. Because environmental signals change fairly slowly, a slow speed is typically acceptable for CDCs. Clocks Φ_{s1}/Φ_{s2} and Φ_{d1}/Φ_{d2} are non-overlapping 125kHz clock pairs. To save power, 0.6V is used for non-overlapping clock generation and digital control logic. When the 0.6V signals pass on to the 1.2V domain, level converters are used to shift up the voltage domain (Figure 2.4).
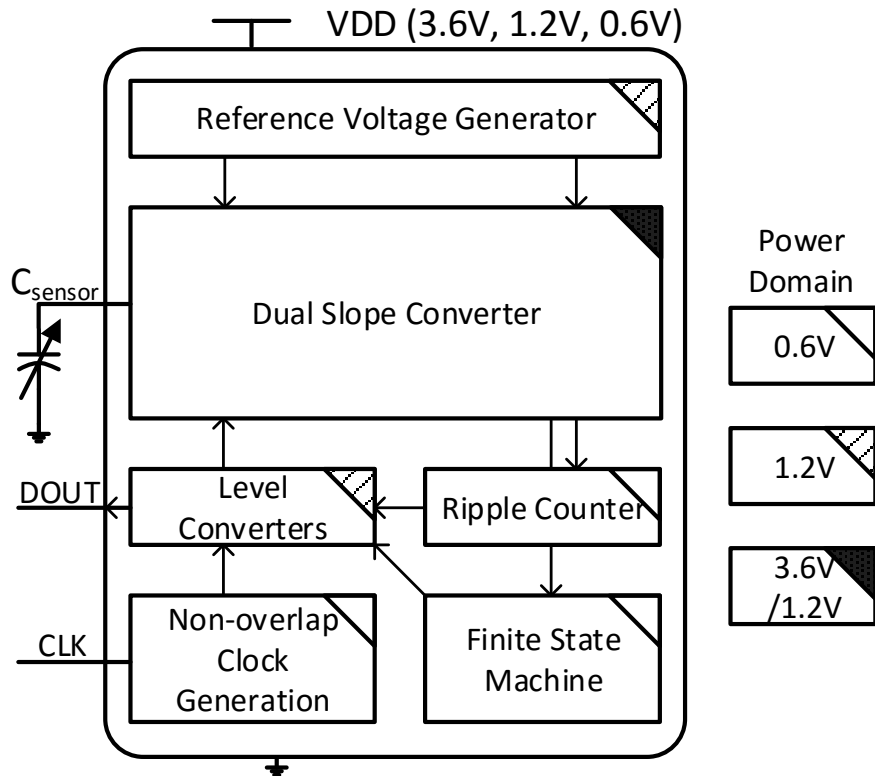
Figure 2.4. CDC Block diagram with power domain.

2.3 Energy-Efficient Charge Subtraction

The OTAs are responsible for a significant portion of the CDC's total energy consumption, and so its bandwidth should be appropriately chosen to optimize energy. Unity gain bandwidth (ω_u) of an OTA is generally $g_{m,OTA}/C_L$ for a single-stage design where $g_{m,OTA}$ is the transconductance of the OTA input transistor pair and C_L is the OTA output load capacitance. The

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unity gain bandwidth is unchanged even when the OTA forms a negative feedback loop ($\omega_{u,cl} = \omega_u$). Its transfer function is $\frac{A_{0,cl}}{(1+s/\omega_{p,cl})}$[26], where $A_{0,cl}$ and $\omega_{p,cl}$ are the DC gain and the dominant pole of the loop, respectively. Assuming the DC OTA gain is much larger than the inverse of the feedback factor ($A_0 \gg 1/\beta$), $A_{0,cl}$ and $\omega_{p,cl}$ are approximated as $1/\beta$ and $\beta g_{m,OTA}/C_L$. The settling time constant of the first-order system is the inverse of $\omega_{p,cl}$:

$$\tau = \frac{C_L}{\beta g_{m,OTA}} \tag{2.5}$$
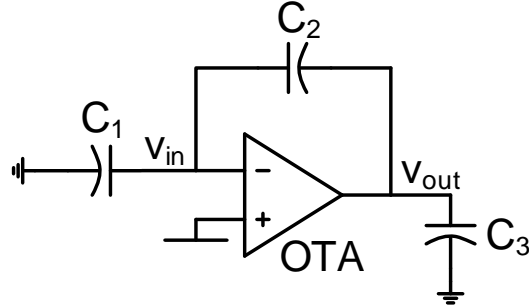
Figure 2.5. Discharge circuit schematic.

When the feedback is capacitive, as shown in Figure 2.5, C_L becomes equal to $C_3 + C_1 C_2/(C_1 + C_2)$) and $1/\beta$ is $(C_1 + C_2)/C_2$. Assuming $C_3 \ll C_1, C_2$, the settling time constant becomes:

$$\tau \cong \frac{C_1}{g_{m,OTA}} \tag{2.6}$$

From this, we see that τ is not related to the feedback capacitor (C_2) and only depends on the input capacitor (C_1).

The proposed DS-CDC opens the sensor capacitor path while only connecting the C_{ref} path during the discharge state as shown in Figure 2.2 and Figure 2.6. The corresponding τ is $C_{ref}/g_{m,OTA}$. C_{ref} is equivalent to the LSB of the DS-CDC. Hence C_{ref} is much smaller than C_{sensor}, allowing for significantly lower OTA tail current for a fixed sampling rate. In the proposed method, the OTA's feedback loop is modified to include a source follower, which isolates the discharge path from C_{integ} as well as C_{sensor}. The OTAs in the proposed design use a single-stage design. The
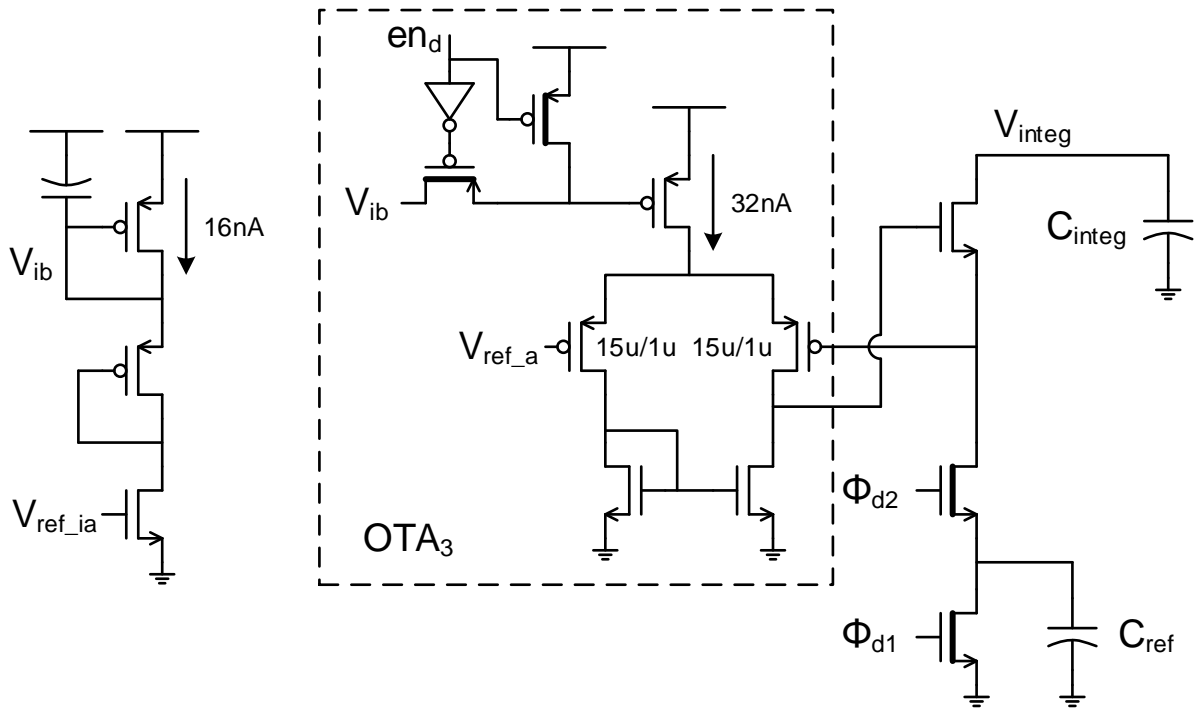
Figure 2.6. Capacitive feedback of an OTA (switches not shown).

OTA bias current (Figure 2.5 left) is generated by a voltage reference described later. Although the OTAs use a 1.2V supply, the current mirror uses 3.6V, which is available in the complete microsystem described later (battery voltage); this increases V_{integ} range while keeping power low. Although the proposed CDC has an energy benefit, a mismatch in the current mirror and injection at the switches can result in offsets and gain errors. These need to be calibrated for each C_{base} to

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obtain a complete, calibrated code over the entire range of the CDC. The power supply rejection

is also limited in the proposed design and the CDC may require a supply regulator.

2.4 Noise Analysis and Dual Comparators

The CDC resolution is determined by the circuit noise, which is composed of sampling

state noise and discharge state noise.

The sampling noise comes from the switched-capacitor integrators. In a typical
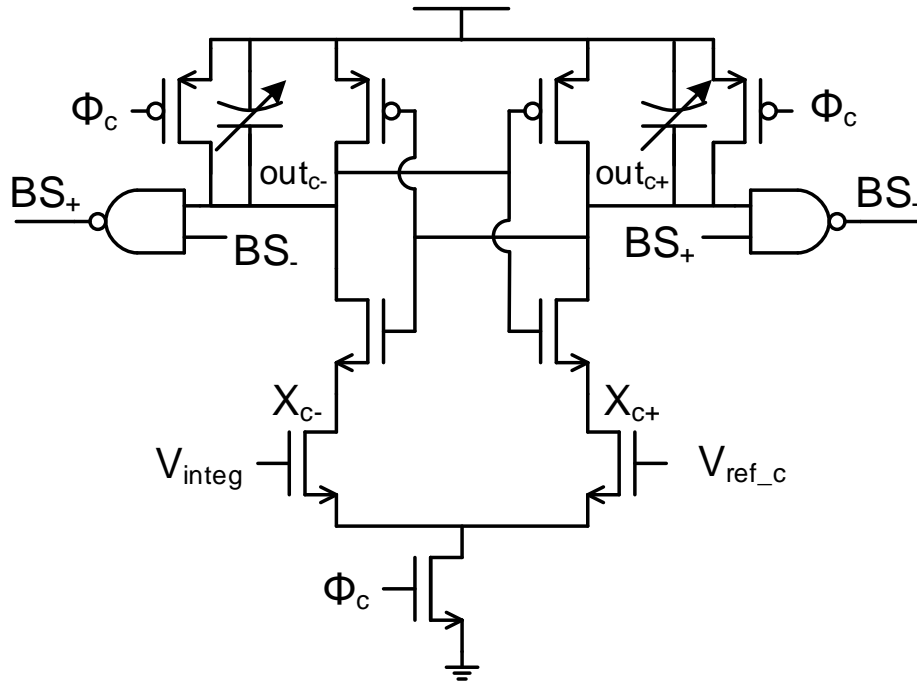
Figure 2.7. Clocked comparator schematic.

implementation, as shown in Figure 2.6, the input-referred noise is represented by $\overline{v_{n,c1}^2} = \frac{7kT}{3C_1}$ and

the output noise is described as $\overline{v_{n,o}^2} = \frac{7kT}{3C_1} \cdot \frac{C_1^2}{C_2^2}$. Here the OTA transconductance is assumed to be

much lower than the switch transconductance [26]. Although the OTA output noise power

spectrum density is proportional to $1/g_{m,OTA}$, the OTA bandwidth is proportional to $g_{m,OTA}$, and

hence the sampled noise of the switched capacitor integrator is independent of $g_{m,OTA}$. This

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equation also applies for the proposed CDC. The noise from the sensor capacitor on the integration

capacitor using the proposed OTA feedback is represented by:

$$\overline{v_{n,OTA,sensor}^2} = \frac{7kTC_{sensor}}{3C_{integ}^2} \tag{2.7}$$

In the worst-case condition where the largest C_{sensor} is used (30.7pF), the noise is 136

µVrms. The current mirror noise can be suppressed by proper transistor sizing (large length).

Similarly, the noise from C_{base} on C_{integ} ($v_{n,OTA,base}$) is 115µVrms (with 22pF C_{base}). The noise

from C_{ref} on C_{integ} ($v_{n,OTA,ref}$) is 3.2µVrms; this is negligible and hardly affects the discharge noise.

The CDC uses clocked comparators (Figure 2.7). The comparator precharges both *outc*

nodes and *Xc* nodes to 1 with Φ_c=0. When Φ_c=1, the comparator discharges those nodes with

input-dependent speeds and makes a comparison decision using regenerative feedback. The main

noise source of the clocked comparator is thermal noise in our simulation; this causes a random

decision error and the error probability follows Gaussian statistics [27].

In the proposed DS-CDC, the probability of obtaining a 1 as a function of the comparator

input *x* can be written in the form of the Q function [28]:

$$P_1(x) = \int_x^\infty \frac{1}{\sqrt{2\pi} \cdot \sigma_{n,i}} e^{-\frac{x^2}{2\sigma_{n,i}^2}} \, dx = Q\left(\frac{x}{\sigma_{n,i}}\right), \tag{2.8}$$

where *x* is the comparator input normalized to LSB, and $\sigma_{n,i}$ is the input-referred

comparator noise normalized to LSB. The discharge process of the CDC involves discrete and

sequential events. Initially, the counter value is 0, and it counts every comparison until the

comparator flips. The first flip of the comparator directly indicates the end of the conversion, while

continuing iterations of the CDC imply the comparator has not yet flipped, and all previous results

were 1's. The probability that the CDC is still performing a conversion at the nth cycle (P_{CDCrun}) is

the cumulative product of $P_1(x)$:

$$P_{CDCrun}(n) = \prod_{i=0}^{n} P_1(i - Code_{ideal}) = \prod_{i=0}^{n} Q\left(\frac{i - Code_{ideal}}{\sigma_{n,i}}\right), \tag{2.9}$$

where $Code_{ideal} = 4(C_{sensor} - C_{base})/C_{ref}$. From (2.9), the probability density function

of the code (final iteration cycle of the CDC conversion) is:

$$p(Code) = P_{CDCrun}(Code - 1) - P_{CDCrun}(Code)$$

$$= \left(1 - Q\left(\frac{Code - Code_{ideal}}{\sigma_{n,i}}\right)\right) \cdot \prod_{i=0}^{n-1} Q\left(\frac{i - Code_{ideal}}{\sigma_{n,i}}\right) \tag{2.10}$$

Equations (2.9) and (2.10) can be numerically solved, and they are shown with example

values in Figure 2.8. From (2.10), the expectation value and variation of *Code* are calculated as:

$$\overline{Code_{comp}} = E[Code] = \sum Code \cdot p(Code) \tag{2.11}$$

$$\sigma_{Code_{comp}}^2 = Var[Code] = \sum Code^2 \cdot p(Code) - \overline{Code_{comp}^2}, \tag{2.12}$$

Figure 2.9 shows calculated $\overline{Code_{comp}}$ and $\sigma_{Code_{comp}}$ with respect to $\sigma_{n,i}$. When $\sigma_{n,i} \ll 1$

(ideal comparator), $\sigma_{Code_{comp}}$ converges to 0.289 ($\cong 1/\sqrt{12}$) representing quantization noise, and

$\overline{Code_{comp}}$ converges to $Code_{ideal} + 0.5$ as expected since comparator flip probability
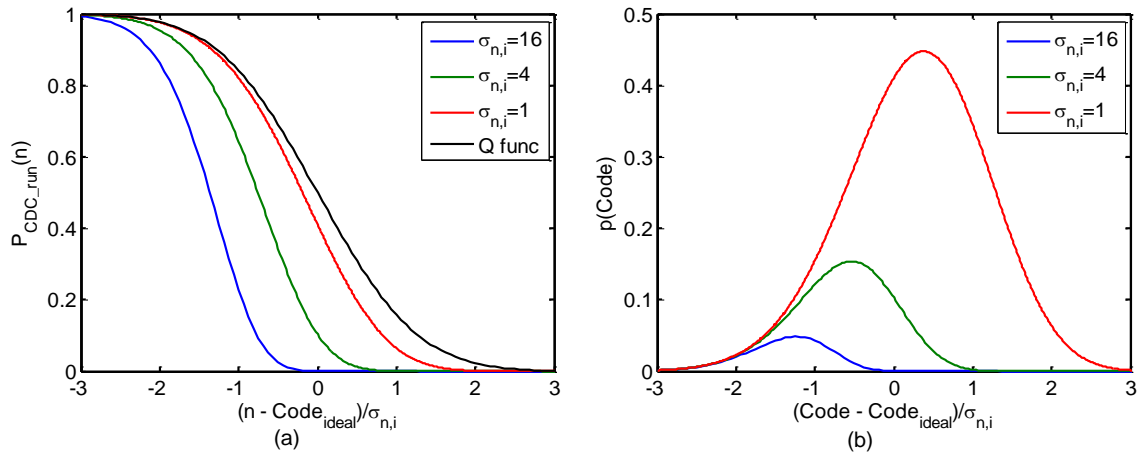
Figure 2.8. (a) Probability that the CDC is still performing a conversion at the nth cycle

(b) Probability density function of the code.
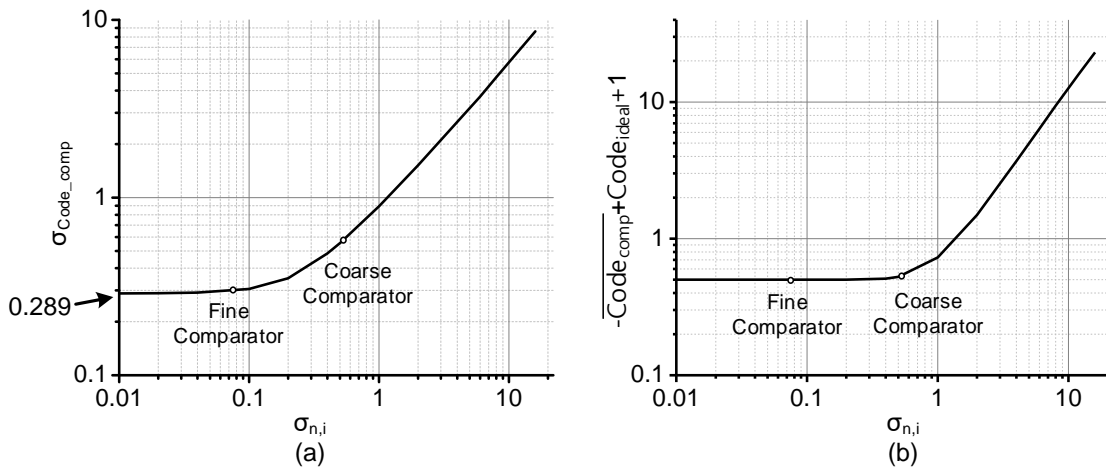
Figure 2.9. (a) Comparison output noise (b) comparison output offset calculated from the

comparator flip probability.
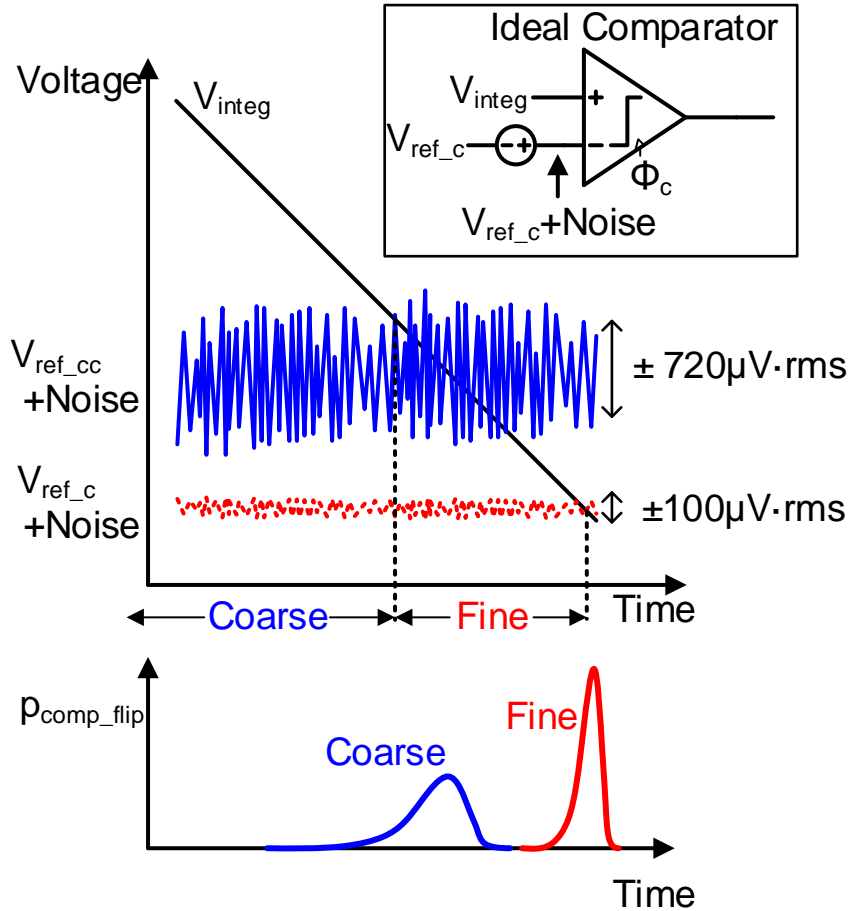
Figure 2.10. Dual comparators operating concept.

is 0.5 at $Code = Code_{ideal}$. When $\sigma_{n,i} \gg 1$, $\overline{Code_{comp}}$ and $\sigma_{Code_{comp}}$ converge to linear expressions.

Comparator energy consumption is reduced by adopting a dual comparator scheme, composed of a coarse comparator and a fine comparator, without impacting the CDC accuracy (Figure 2.2 and Figure 2.10). For the energy reduction, the lower power coarse comparator is used for the most discharge cycles. After the flip of the coarse comparator, the fine comparator makes the final decision that $V_{integ} < V_{ref\_c}$ and determines overall accuracy. To accomplish this, the coarse comparator requires a higher reference voltage (V_{ref_cc}) than the fine comparator (V_{ref_c}) as shown in Figure 2.10. The difference can be generated by two different voltage references. The coarse comparator design (720μV rms input-referred noise, 7.4fJ/comparison, simulated) is constrained
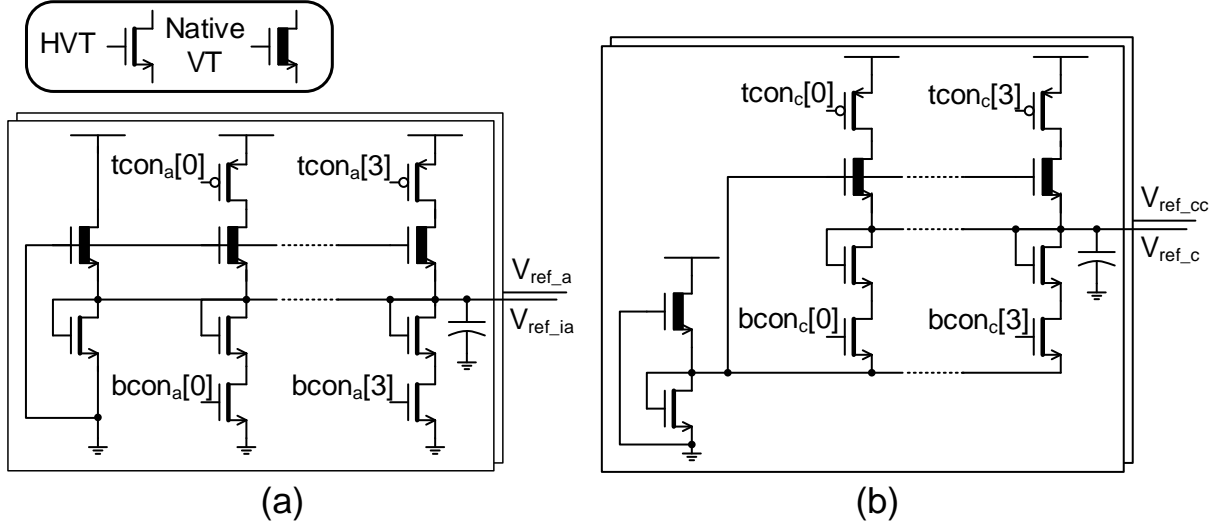
Figure 2.11. 60pW reference voltage generator for (a) the OTAs and (b) the comparators.

by minimum size transistors. The fine comparator (100μVrms noise, 450fJ/comparison, simulated) is designed for $\sigma_{n,i}$=0.1 with 10× larger transistors and output capacitors to balance energy and noise. The converted comparison-output noises $\left(V_{LSB} \cdot \sigma_{Code_{comp}}, \ V_{LSB} = C_{ref}/C_{integ} \cdot V_{ref\_a} \right)$ are 780μVrms (coarse comparator) and 402μVrms (fine comparator, dominated by quantization noise). The reference voltages V_{ref_a} and V_{ref_ia} (300mV for OTAs) as well as V_{ref_c} and V_{ref_cc} (600mV for comparators) are generated using ultra-low power (60pW) voltage references. V_{ref_a} (V_{ref_ia}) is approximately equal to the threshold voltage difference of two different type transistors (Figure 2.11(a)), and the higher reference voltages (V_{ref_c} and V_{ref_cc}) are generated by stacking the two references (Figure 2.11(b)) [29]. The references have <2mV resolution programmability by trimming *tcon* and *bcon*. Each reference voltage is connected to a decoupling capacitor (4pF). The trimming methodology consists of two steps: We initially use a large voltage difference between the two references and measure the resolution, which is determined by the fine comparator. Then, we incrementally lower the threshold voltage difference until resolution starts to degrade and select the last voltage difference where the resolution was still maintained. This methodology ensures

fine-comparator resolution with minimum power consumption. In simulation, a 2-4mV comparator offset difference is sufficient to achieve the resolution of the fine comparator and results in an average usage of the fine comparator of three cycles per conversion. In the test chip implementation, it was not possible to measure the minimum necessary comparator offset difference due to a step size limitation in the testing harness.

The total noise power is calculated by adding the OTA noises and the comparator noise:

$$\overline{v_n^2} = 4\overline{v_{n,OTA,sensor}^2} + 4\overline{v_{n,OTA,base}^2} + \overline{v_{n,comp}^2}, \tag{2.13}$$

where $\overline{v_{n,comp}^2} = V_{LSB}^2 \cdot \sigma_{Code_{comp}}^2$. Based on the design values, $v_{n,rms}$ is calculated to 537μVrms; this corresponds to 7.2fF resolution. Quadruple sampling was chosen to balance the sampling noise and the discharge noise.

2.5 System Integration

The proposed CDC was integrated in a complete pressure sensing system constructed from stacked IC layers to demonstrate CDC operation in an ultra-low power sensor platform [4]. Figure 2.12 shows a system-level block diagram.

The system is powered by a custom 2μAh thin-film battery with 3.6V output, which is down-converted to 1.2V and 0.6V by a switched-capacitor-based power management unit (PMU) in the control layer. The DS-CDC uses all three power domains: 0.6V for digital control logic and non-overlapping clock generator, 1.2V for most analog blocks, and 3.6V for the current mirror. The system also includes an ARM Cortex-M0 processor and 3kB low-power retentive (always

powered on) memory in the control layer, which controls overall system operation. An on-off
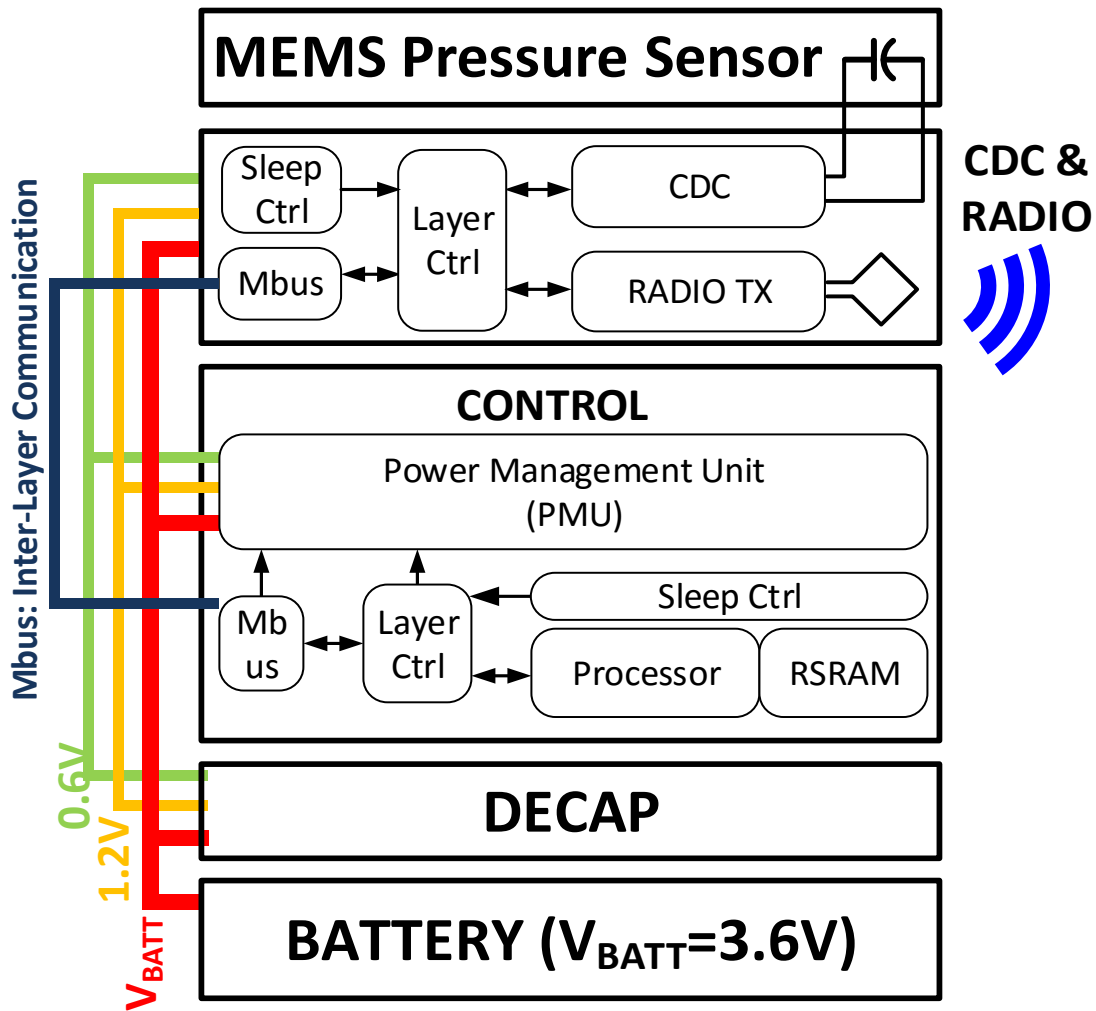
Figure 2.12. System level block diagram of the implantable pressure monitoring sensor with the proposed CDC.

keying (OOK) near-field radio [5] with an on-chip coil is located on the top IC layer to enable users to collect the measured pressure data. The proposed CDC is also located on the top IC layer. The processor on the control layer communicates with the radio and CDC via an inter-layer communication (ILC) bus. A layer dedicated to providing decoupling capacitance (decap layer) is also included to ensure the supply voltages remain stable.
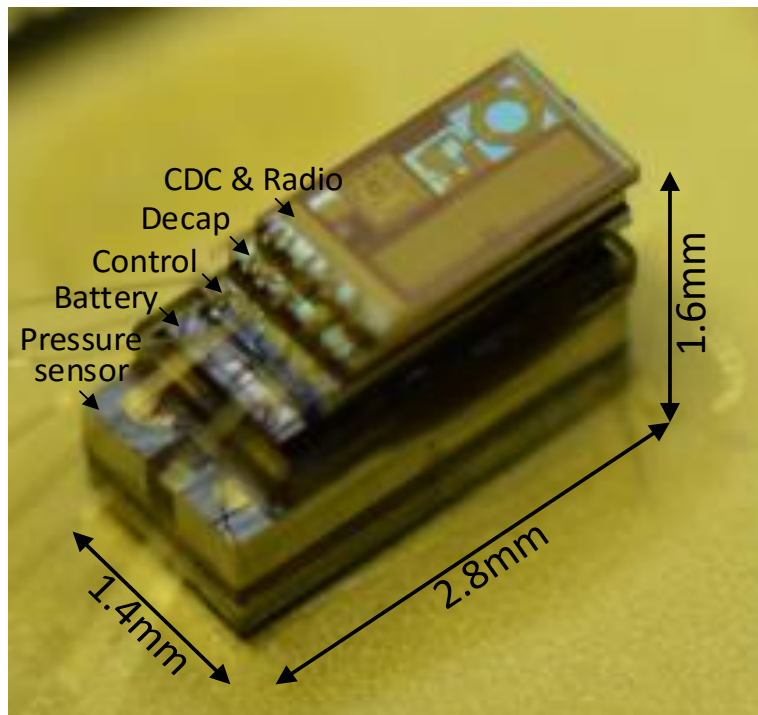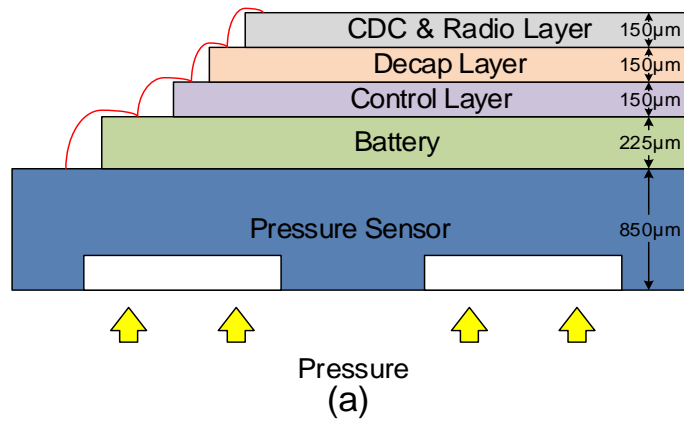
Figure 2.13. (a) Physical structure diagram and (b) picture without encapsulation

of the proposed implantable sensing system.

The entire electronics stack is placed on a MEMS pressure sensor whose two top electrodes are connected to the CDC with bondwires, as shown in Figure 2.13. The sensing diaphragm of the MEMS pressure sensor faces the bottom of the stack so that it can be exposed to the ambient pressure when the upper part of the sensing system is sealed. The entire stack measures 1.4mm ×
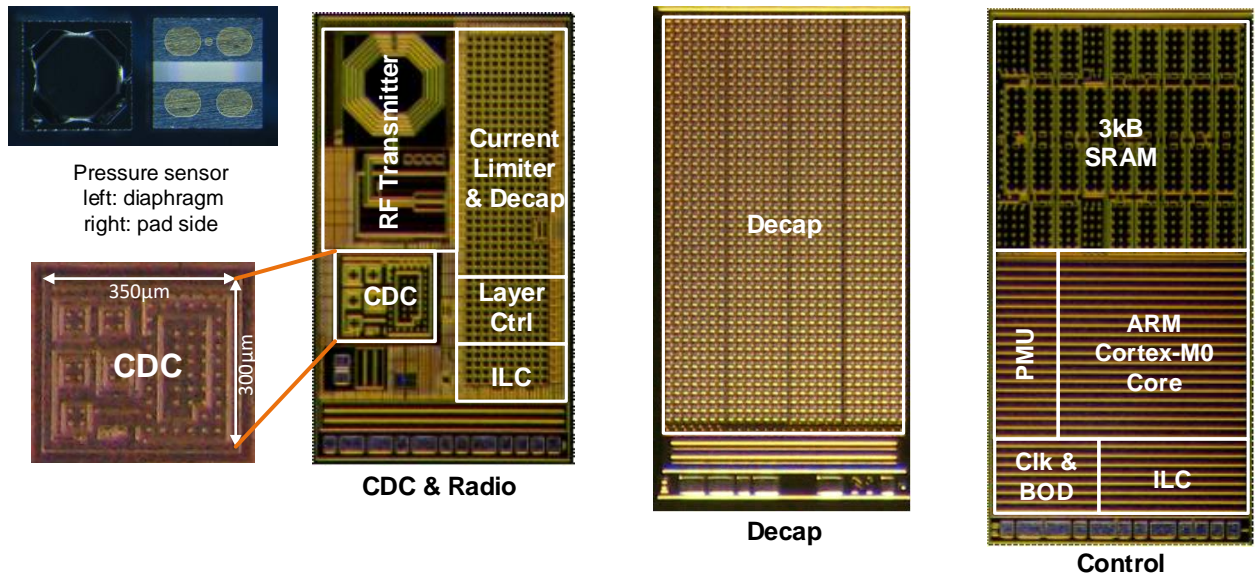
Figure 2.14. Micrographs of the implemented IC layers and MEMS pressure sensor.

2.8mm × 1.6mm, allowing minimally invasive implantation, potentially with a syringe. Figure 2.14 shows die micrographs for each of the implemented IC layers.

2.6 Measurement Results

The CDC is implemented in 180nm CMOS and has an active area of 0.105mm^2. To test CDC linearity, the bottom voltage of C_{sensor} is swept and $C_{sensor} \cdot \frac{(V_{ref\_a} - V_{sens\_bot})}{V_{ref\_a}}$ is regarded as effective capacitance (C_{eff_sensor}). While this test does not include the effect of the OTA loading changes, it is capable of verifying the whole range continuously.

24
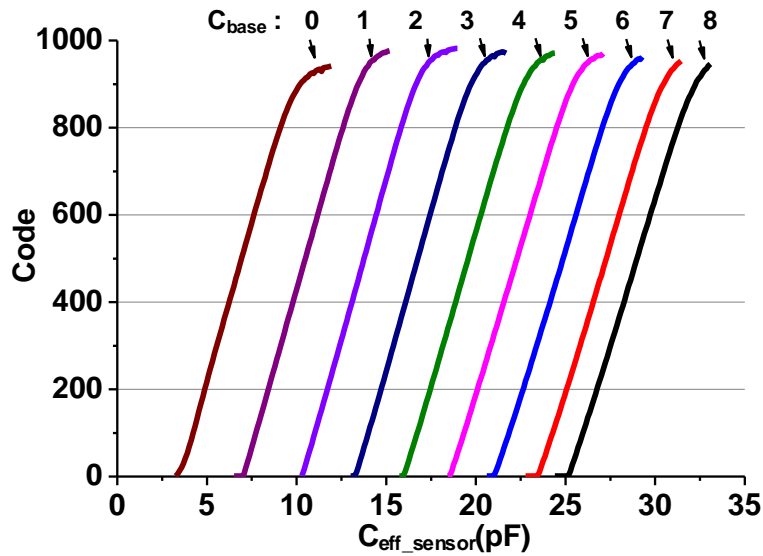
Figure 2.16. Code versus effective sensor capacitor (C_{eff_sensor}) using voltage sweep with various

C_{base} values. $\left(C_{eff\_sensor} = C_{sensor} \cdot \frac{(V_{ref\_a} - V_{sens\_bot})}{V_{ref\_a}} \right)$
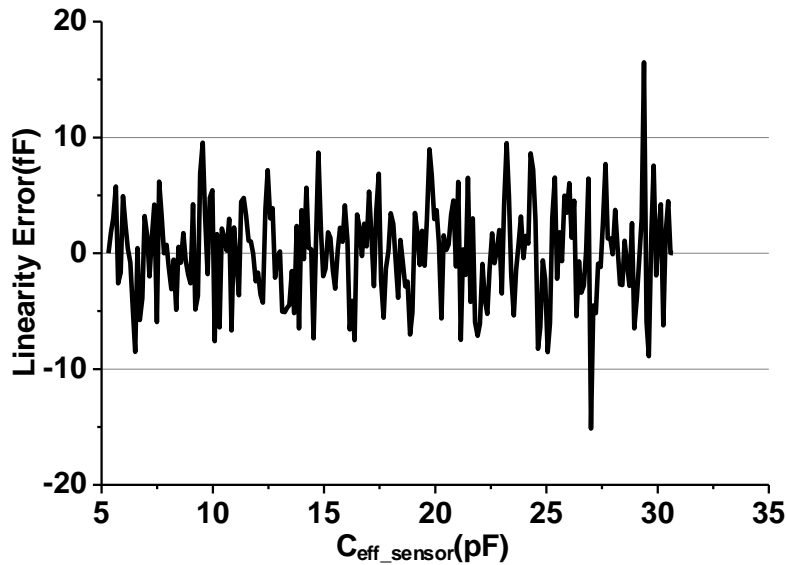
Figure 2.15. Linearity error of the proposed DS-CDC with 9 different C_{base}.

Figure 2.16 shows the measurement result. By changing the C_{base} configuration from 0 to

8, which corresponds to 0pF to 22pF, the CDC covers C_{eff_sensor} ranging from 5pF to 31pF. A

linearity error plot shown in Figure 2.15 combines results from 9 different ranges calibrated by 2
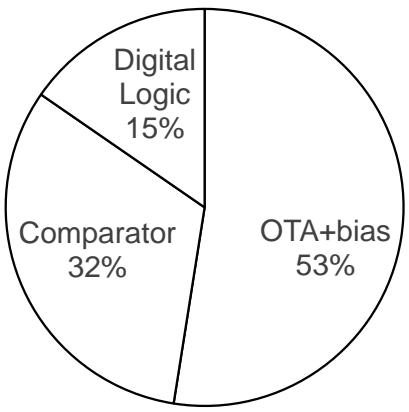
Figure 2.17. Power breakdown of the CDC.

points in each range. The maximum error is found to be 16.5fF. The ranges are configured to

overlap with an adjacent C_{base} value to avoid missing codes. For a given C_{base}, a 4pF range is

measured with a linearity that is less than the maximum error.

Power and resolution are measured at the worst-case maximum input capacitance condition.

Total CDC power is 112nW, consuming 95nW from 1.2V, 17nW from 0.6V, and 0nW from 3.6V,

and the power breakdown is shown in Figure 2.17. This makes it suitable for miniature sensor
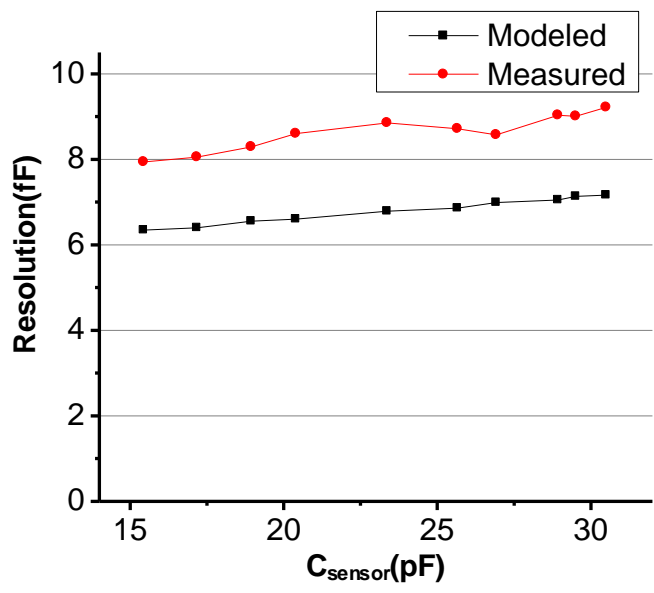
Figure 2.18. Modeled and measured capacitance resolution.

node systems that often have batteries with low peak current capabilities [7]. Power from the 1.2V

supply is reduced by 13% when using the proposed dual-comparator method rather than using the

fine comparator only. Power savings are limited by the parasitic capacitance of the clock network.

The CDC SNR is defined as $20\log\left(\frac{Capacitance\ Subrange/2\sqrt{2}}{Capacitance\ Resolution}\right)$ and the figure of merit (FoM) is

$\frac{Power\times Meas.Time}{2^{(SNR-1.76)/6.02}}$. Here, $2\sqrt{2}$ is the crest-factor [30] for DC-input CDC to compare with sinusoidal-

input ADCs. This SNR definition imagines that a sinusoidal continuous capacitance is given as an

input with an amplitude of $Capacitance\ Subrange/2$, and the signal rms is regarded as

$Capacitance\ Subrange/2\sqrt{2}$. The measured capacitance resolution is 8.7fF, resulting in

5.3pJ/conv·step FoM. Figure 2.18 shows the measured resolution and the modeled resolution with

different C_{sensor}. The measured capacitance resolution is within 20% of the estimated resolution

from (2.13), providing reasonable matching between theory and experiment. Table I summarizes

CDC performance and compares with the previously reported CDCs.

Table 2.1. Performance summary and comparison with prior CDCs.

	This Work	[16]	[20]	[24]	[25]	[31]	[32]	[33]	[34]
Technology(μm)	0.18	0.16	0.35	0.35	0.35	0.13	0.32	0.18	0.18
Method	Dual Slope	ΣΔ	ΣΔ	PWM	PWM	Freq	PWM	SAR	ΣΔ
Input Range(pF)	5.3-30.7	0.54-1.06	8.4-11.6	1-6.8	0.8-1.2	6.0-6.3	0.5-0.76	2.5-75.3	0-24
Meas. Time(ms)	6.4	0.8	0.02	7.6	0.05	1	0.033	4	0.23
Power	110 nW	10.3 μW	14.9 mW	210 μW	15.8 mW	270 nW	84 μW	160 nW	33.7 μW
SNR(dB)	44.2	68.4	84.8	83	45.7	29.4	40.9	55.4	94.7
FoM(pJ/c·s)	5.3	3.8	21	140	5000	11	98	1.3	0.18
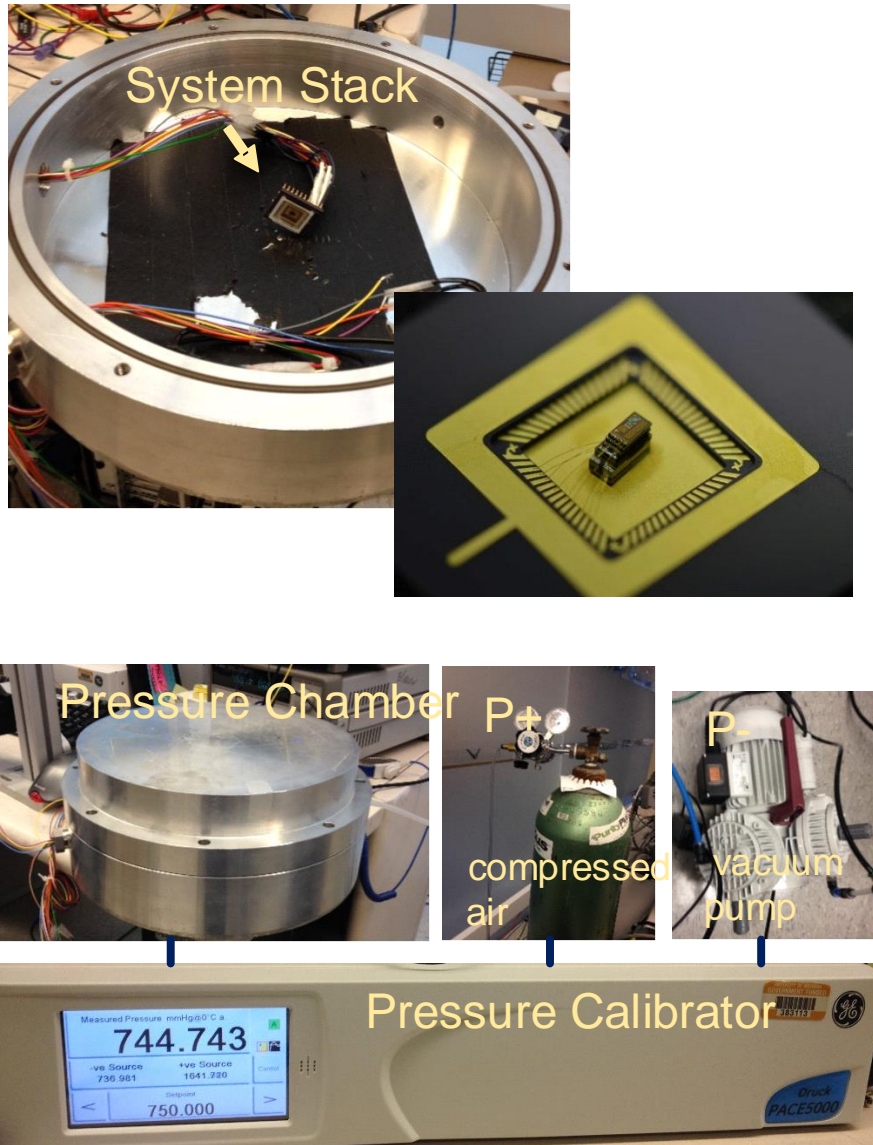
Figure 2.19. Pressure measurement set-up for the CDC integrated

in an implantable pressure sensing system.

The proposed CDC is integrated in a pressure-sensing system as described in Section III and tested as a pressure sensor. Figure 2.19 shows the test set-up for pressure measurement. The sensing system is wirebonded to a PGA socket and it was placed in an aluminum pressure chamber. The pressure inside the chamber was controlled by a pressure calibrator where compressed air and
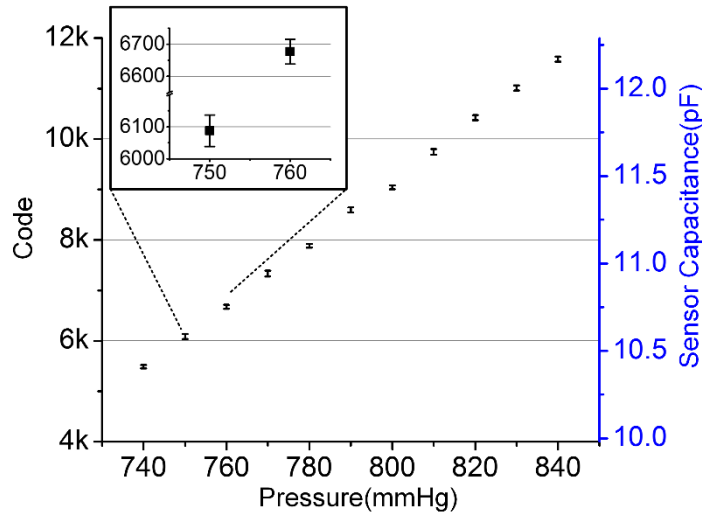
Figure 2.20. Pressure measurement result with $C_{base}=4$ and 32 OSR, taken using the complete pressure-sensing system in a pressure chamber.

vacuum are supplied externally. Using the bonded wires, an external 3.6V supply overrode the battery, and the ILC bus read the CDC data. Figure 2.20 shows the pressure measurement results achieving a linear output response with $R^2=0.9995$. The chamber pressure was swept from 740 to 840mmHg, which is a sufficient range for various body pressure diagnoses, including intra-ocular, intra-cranial, and intra-abdominal pressures [35]. The MEMS pressure sensor used in this experiment has high linearity in this region [36], and the corresponding capacitance range is overlaid in Figure 2.20. During this test, C_{base} was set to 4, and *Code* is the total count. The measured power sensitivity of the system was 0.4mmHg/mV for 3.6V and 4.0V supplies without calibration. During the system measurement, the PMU generated relatively large fluctuations on the power supply nodes and the processor was also running introducing possible additional noise. Given the sensitivity of the CDC to supply variation, the CDC was operated with an oversampling rate (OSR) of 32 and achieved a resolution of 0.77mmHg with 200ms conversion time. The long-term CDC supply sensitivity can be addressed with two-pressure-point calibration as its linearity
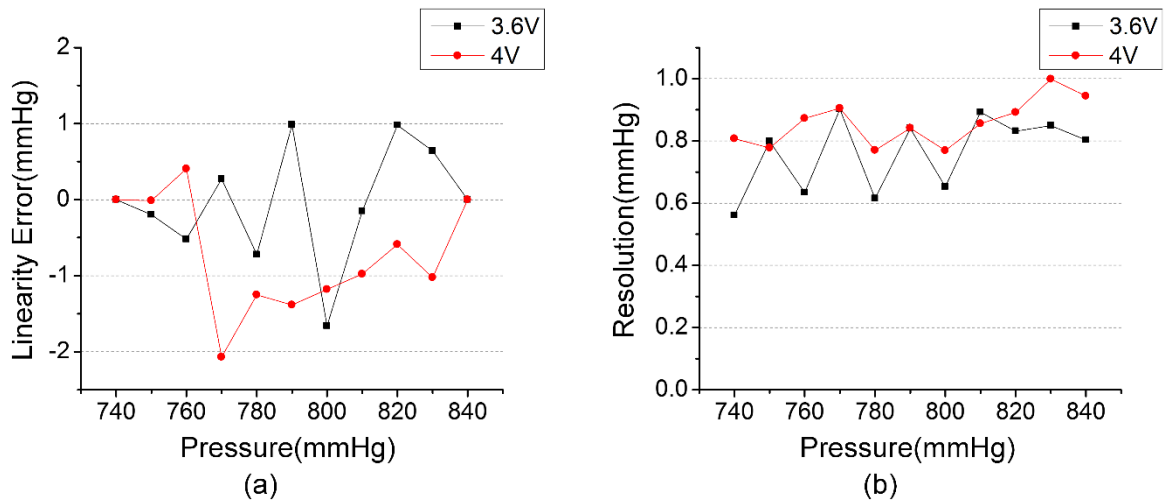
Figure 2.21. Pressure sensing system measurement (a) linearity error with two-pressure-point correction (b) rms resolution for 3.6V and 4.0V operation.

is preserved across voltage. Since a pressure sweep during calibration represents the most time-consuming and expensive process, multiple readings can be taken at different supply voltages for each pressure and then stored in a look-up table. In operation, a low sample rate ADC would read the supply voltage to index into the look-up table. Using this manner of two-pressure-point correction, the linearity error and resolution become less than 2mmHg and 1mmHg, respectively, for 3.6V and 4.0V supply across 740 to 840mmHg as shown in Figure 2.21 with fairly small added
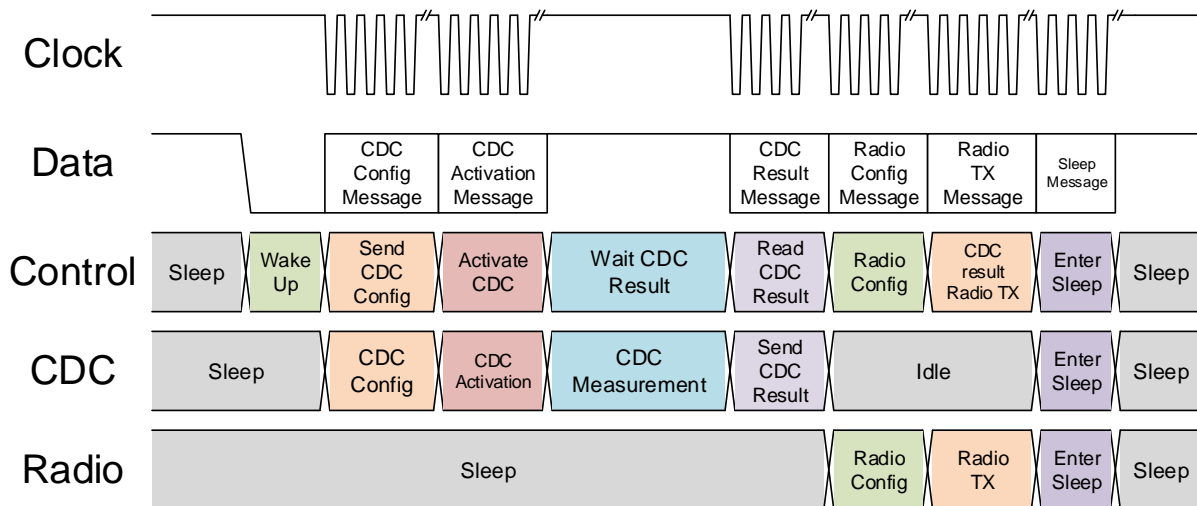
Figure 2.22. Operation sequence of the implantable pressure-sensing system.
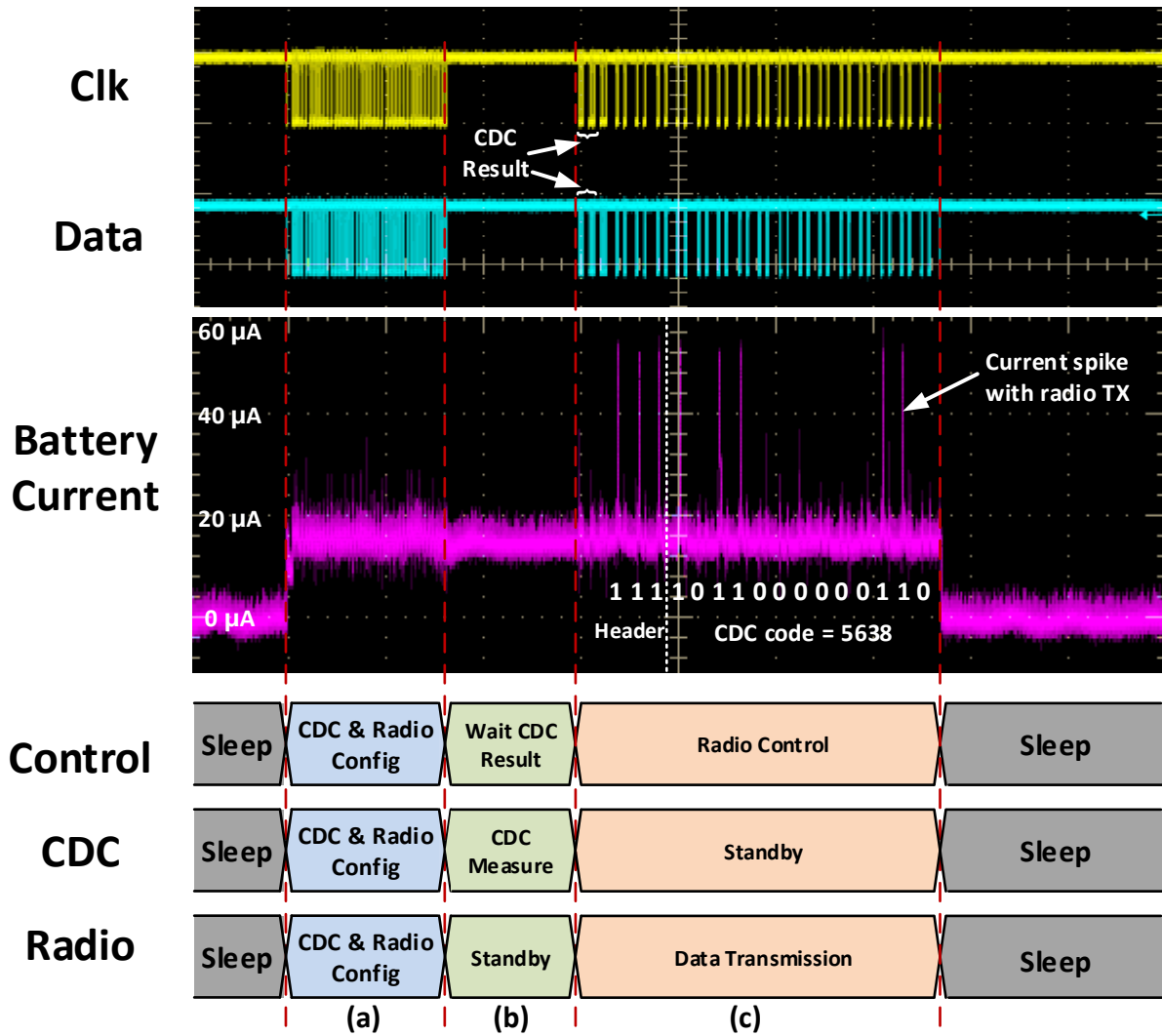
Figure 2.23. Measured waveforms for the sensing system operation.

testing time and cost beyond a single-Vdd dual-pressure calibration. However, since a low sampling rate ADC was not available in our system at the time of testing, the system level performance and power overhead of this supply voltage calibration were not quantified.

Figure 2.22 shows an example operation scenario of the sensing system. The sensor system typically spends most of its time in a low-power sleep mode (<8nW) to save power. Then it periodically wakes up and enters active mode (~50μW) for measurement operation. As the system wakes up, it first initializes the CDC and then initiates pressure measurement. Upon completion,

the digital pressure value is stored in memory and can be accessed for later radio transmission. In this example, the data is immediately transmitted through the radio after each pressure measurement. The system then returns to sleep mode. Each pressure measurement cycle consumes 6.5μJ, and so the 2μAh battery corresponds to 17.7 days of operation capacity (assuming the pressure is recorded every 10 minutes). Figure 2.23 shows measured waveforms of the ILC wires and battery current. The ILC activity indicates the processor in the control layer is interacting with the CDC and the radio on the top IC layer. As the system wakes from the low power sleep mode, the current consumption jumps to ~20μA. The ILC activity in part (a) indicates that the CDC is configured, and pressure measurement is activated. During the CDC activation in part (b), no ILC activity is required until the result is sent back to the memory in the early part of (c). In the remainder of part (c), the processor controls the radio to send out pulses; whenever the radio transmits a pulse, a battery current spike can be clearly observed. After the radio transmission, the current consumption drops to <8nA as the system enters sleep mode to save power.

2.7 Conclusions

This chapter proposed an energy-efficient DS-CDC suitable for implantable pressure sensing systems. Pressure sensors often have large base capacitance, while their variation is small. The CDC removes this base capacitance using a configurable capacitor bank that zooms in on the capacitance variation and reduces conversion time and energy. The CDC uses three different supply voltages (0.6, 1.2, 3.6V) that are available in the system to optimize energy. By isolating the reference capacitance from the relatively large neighboring sensor capacitor, the OTA bias current can be reduced to 32nA. Dual-precision comparators are used in conjunction to achieve the high resolution of the fine comparator and low energy of the coarse comparator. The proposed

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CDC achieves 8.7fF resolution, 5.3pJ/conv·step FoM, which is in reasonable agreement with the theoretical noise analysis for the circuit. In addition, we demonstrated a complete 1.4mm×2.8mm×1.6mm pressure sensor system with a MEMS pressure sensor, processor, memory, PMU, battery, ILC, and radio. This system was tested in a pressure chamber with an external 3.6V supply and OSR of 32 and achieved 0.77mmHg resolution with good linearity (R^2=0.9995).

CHAPTER 3

An Incremental ΔΣ Capacitance-to-Digital Converter

with Zoom-in Asynchronous SAR

3.1 Introduction

Capacitive sensors are widely used in wireless microsystems to measure pressure, proximity [20] and humidity [24]. In these types of applications, battery life is very limited, requiring low conversion energy despite the need for high resolution. SAR CDCs have obtained conversion energies as low as 7.9pJ/c.s. [37], but with limited resolution (ENOB=6.9b). On the other hand, ΣΔ converters can obtain much higher resolution (up to ENOB=13.8b), but at the cost of higher conversion energy (FoM=21pJ/c.s.) [20].

To maintain high accuracy while reducing conversion energy, we propose a zoom-in, incremental ΔΣ CDC. The zoom-in nature restricts the converter to near-DC inputs [4], which is appropriate for sensor nodes where environmental parameters (and hence capacitance readings) change very slowly. A zoom-in ADC with 6b SAR and an oversampling ratio (OSR) of 2000 was previously proposed in [30]. However, due to the modest SAR accuracy, the ΔΣ power remained dominant. In this work, we focus instead on a CDC and also increase the accuracy of the SAR to 9 bits with an OSR of only 32 to create a more balanced and lower overall power budget.
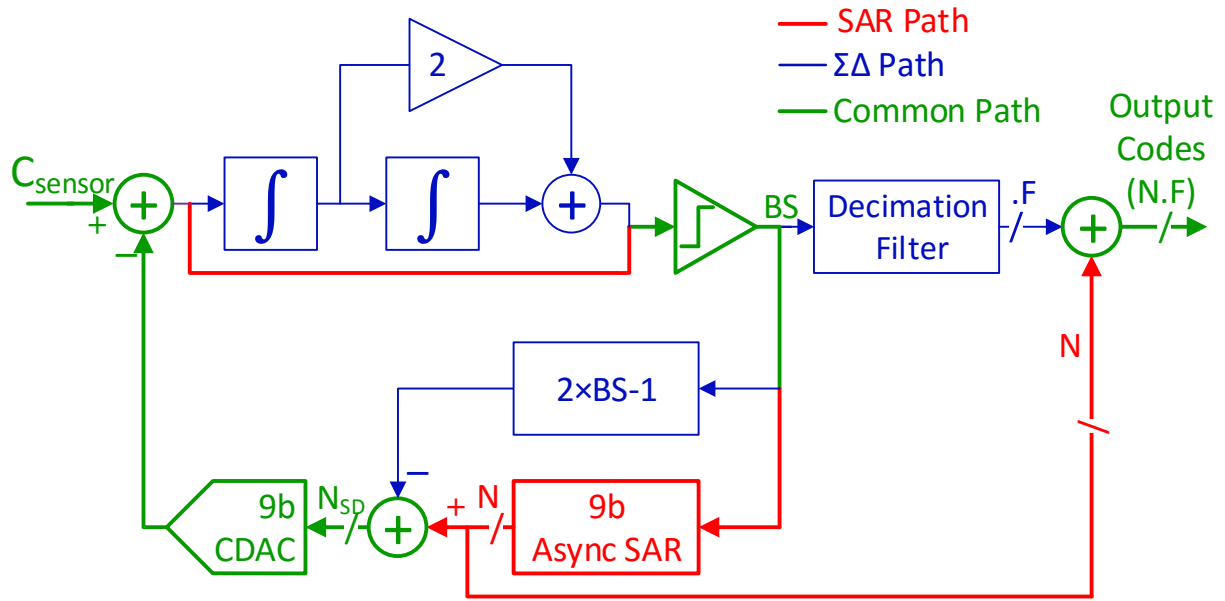
Figure 3.1. Block diagram of the proposed CDC.

While significantly reducing conversion energy, a 9b SAR faces two key challenges: 1) due to the increased importance of SAR power, the OTA that traditionally operates during the SAR phase becomes a major contributor to power. To address this we leverage the unique structure of the CDC and by-pass the OTA in the SAR phase, eliminating its power consumption during this phase. 2) With a 9b SAR, the dynamic element matching (DEM) during the $\Delta\Sigma$ phase requires a 512 element capacitive-DAC (CDAC). This incurs significant area and power overhead. Hence, we propose a new matrix based unit-cap structure with integrated row/column addressing.

3.2 Zoom-in SAR Conversion

Figure 3.1 describes the overall structure of the proposed CDC. During the initial SAR phase, the integration path is bypassed and the 9b SAR creates the integer output component, N.
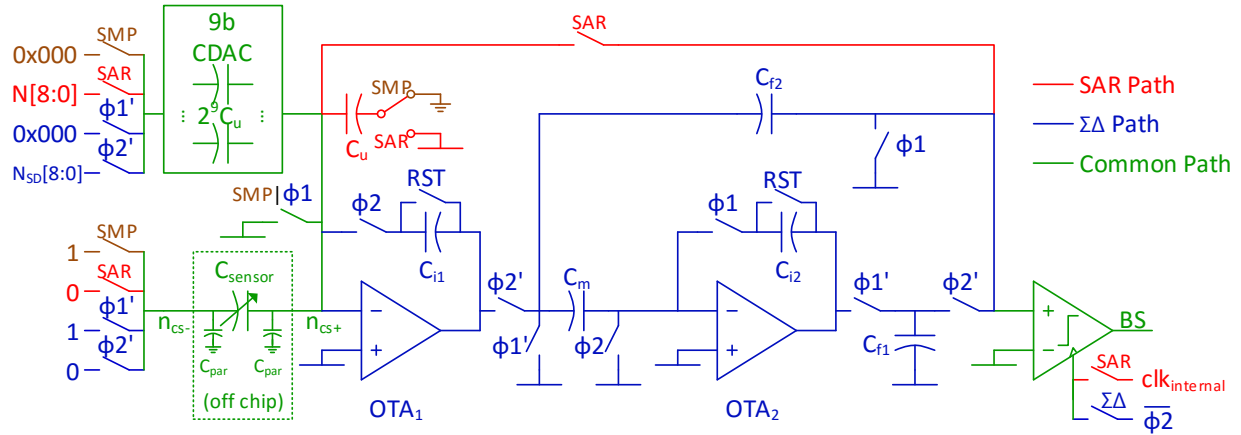
Figure 3.2. Circuit diagram showing the integration of 9b SAR and $\Sigma\Delta$ structure.

This is followed by a high-resolution 2nd order incremental $\Delta\Sigma$ converter that produces the fractional output component, F. For a CDC, the sensed capacitor (C_{sensor}) is an off-chip component and an on-chip CDAC is used as a reference (Figure 3.2). In the sampling phase (Figure 3.3), n_{cs+} and n_{cs-} nodes are set to the common node voltage (VCM) and GND, respectively, and all bottom plates of the CDAC are set to VDD. At the beginning of the SAR phase, n_{cs-} becomes VDD, and a half of the CDAC bottom plates are set to GND. After a comparator determines MSB value of N, the other bottom plates are determined using successive approximation, which results in a near VCM final value for n_{cs+}.

Asynchronous logic gates [38] are used for fast conversion, which allows the SAR conversion to finish within a cycle of global clock, and reduces the static power during SAR conversion by 90%. In order to provide 50% operating margin (-1<F<1) for $\Delta\Sigma$ phase, 0.5-bit is shifted during sampling and the $\Delta\Sigma$ operates with (N-1,N+1) [30]. The 0.5-bit shift is implemented
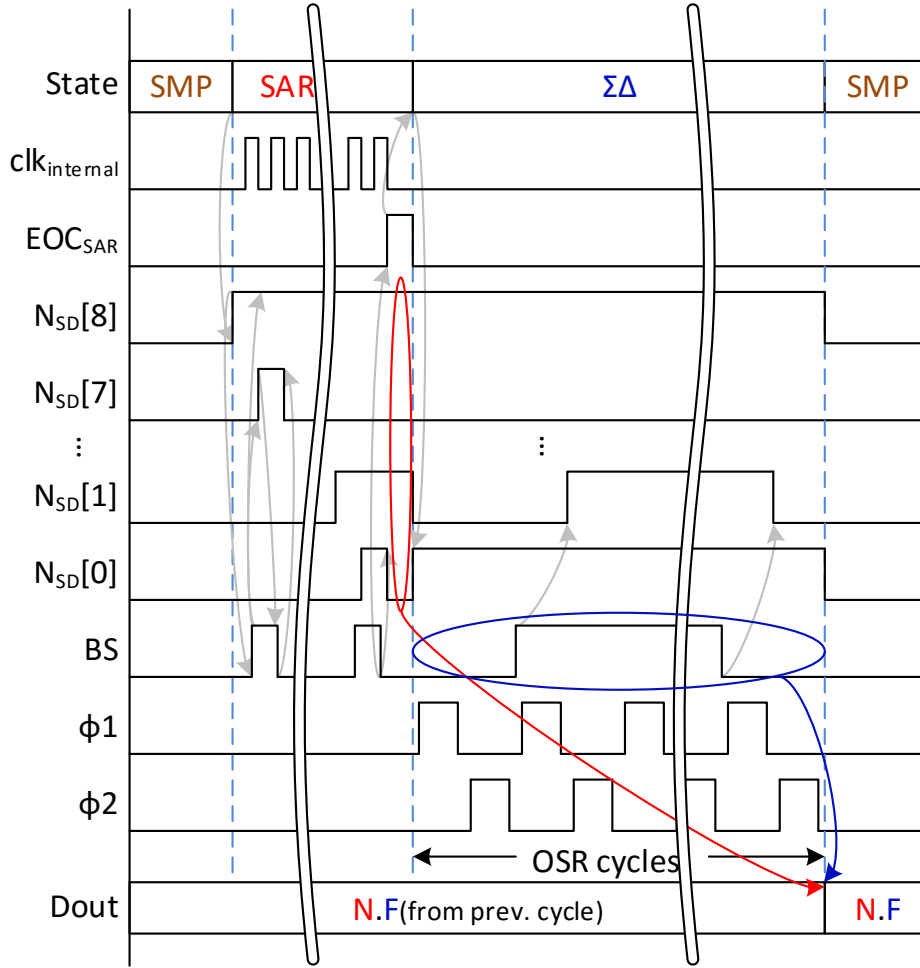
Figure 3.3. Waveform of operation.

with an additional unit-size capacitor (C_u) of the CDAC. The bottom plate of C_u is set to GND during sampling and to half VDD during the SAR phase. Since the OTA is bypassed during initial SAR operation, the SAR bits are obtained with negligible energy compared to bits from the subsequent $\Delta\Sigma$ stage. The comparator is a two-stage sense amplifier [38] with ~100μV resolution for the 9b SAR conversion. The maximum SAR resolution is constrained by CDAC mismatch and comparator noise.

After the SAR phase, the 2nd order incremental converter provides added resolution based on the SAR result (Figure 3.2). The architecture is a 2nd order feed-forward structure, similar to [39]. The SAR output error is already small due to its 9b resolution. As a result, any path mismatch

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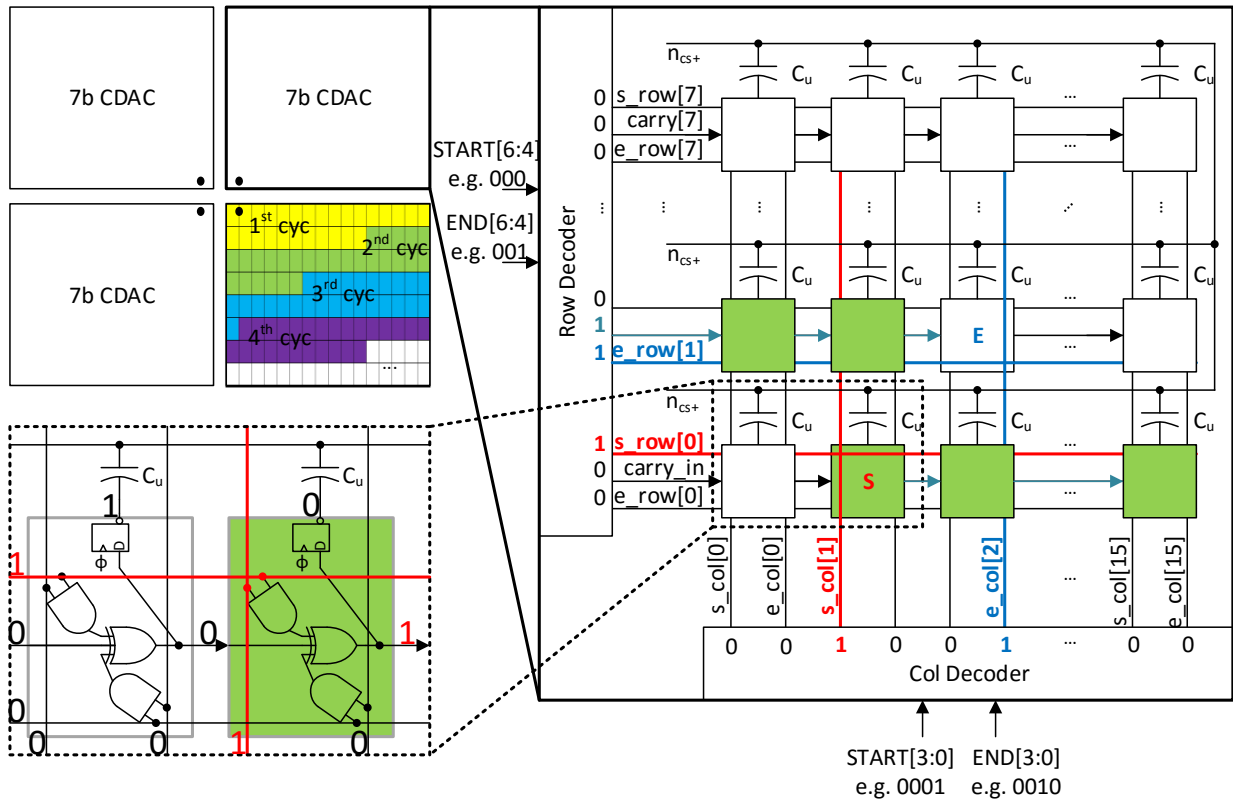
Figure 3.4. 9b Capacitive-DAC implementation with row/column addressing for common centroid layout and dynamic element matching.

between the SAR and ΔΣ will cause the ΔΣ stage output to stick at all ones or all zeroes. By using the same path between SAR and ΔΣ, we minimize the mismatch effect. $\varphi 1$ and $\varphi 2$ are 150kHz non-overlapping clocks. OTAs are cascoded inverter amplifiers as in [30]. OTA_1 and OTA_2 consume 12μW and 1μW, respectively.

In order to suppress CDAC mismatch, we employ 1st order dynamic element matching (DEM) with a new indexing structure (Figure 3.4). DEM uses unit-cap rotation, with every cycle using the next neighboring capacitors. In a conventional design, 512 control lines are required to control the 9b CDAC. The activity ratio of all the lines is 0.5 because of DEM operation. These lines are long and exhibit strong mutual coupling, resulting in a large power overhead. To reduce both power and area, we introduce a matrix unit-cap organization. Each unit-cap is enabled when

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it falls between the asserted column/row *start* and *end* signals. Row and column decode logic generates the *start* and *end* signals (each a 1-hot encoding). The end index changes at the rising edge of $\varphi2$, which reflects the output of the comparator-updated at $\varphi1$. The start index is copied over from the end index at the rising edge of $\varphi1$, which results in turning off of all capacitors. Each unit-cap bottom plate signal is latched with a delayed clock. Signal *carry_in* is used to invert the unit-cap selection, which is necessary when selected unit-caps wrap around from the end to the beginning of the matrix. The complete CDAC is constructed from four 7b unit-cap matrices organized in a common centroid (CC) layout.

The logic controller and digital loop filter are fully synthesized. Since the clock is slow
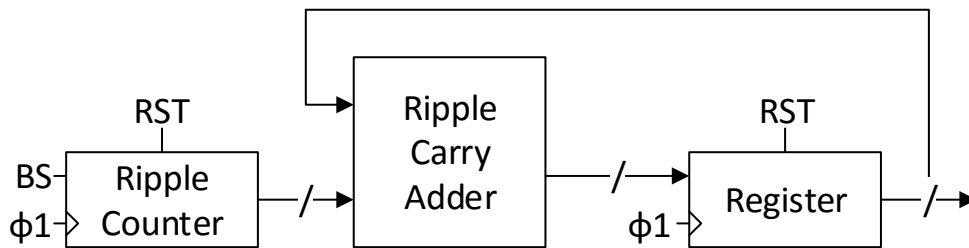
Figure 3.5. Decimation filter.

(150kHz), minimum-size custom-made standard cells are used to reduce clock power. The digital loop filter (Figure 3.5) is a second-order digital integrator which mimics the analog integral path.

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3.3 Measurement Results

The proposed CDC is implemented in 180nm CMOS. Figure 3.6 shows how output codes (N.F) are generated. The SAR output has only a 1 code error and this error is tolerable in the $\Delta\Sigma$ converter.
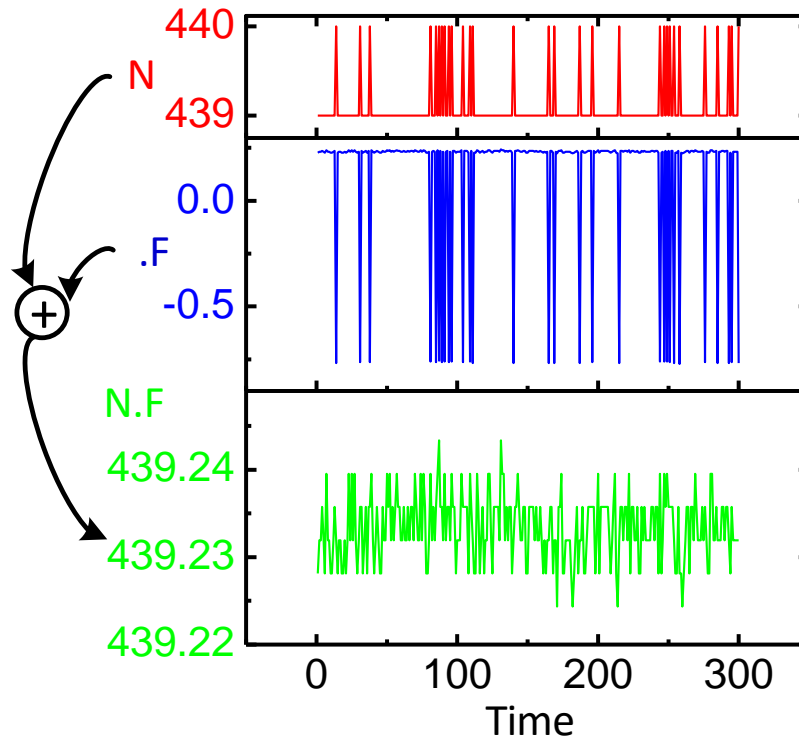
Figure 3.6. Measured output codes (N.F) generation.

CDC linearity test is performed by changing the input voltage of C_{sensor} bottom plate to provide continuous capacitance effectively as in chapter 2. In Figure 3.7, almost all errors are within ±50 ppm (=14.3b) when DEM and CC indexing modes are ON. When CC indexing is OFF, CDC deviates from the $\Delta\Sigma$ working range more often, resulting in more non-linearity. When DEM is OFF, SAR and $\Delta\Sigma$ use different CDAC elements and it loses all bits from the $\Delta\Sigma$ operation because of capacitor mismatch.
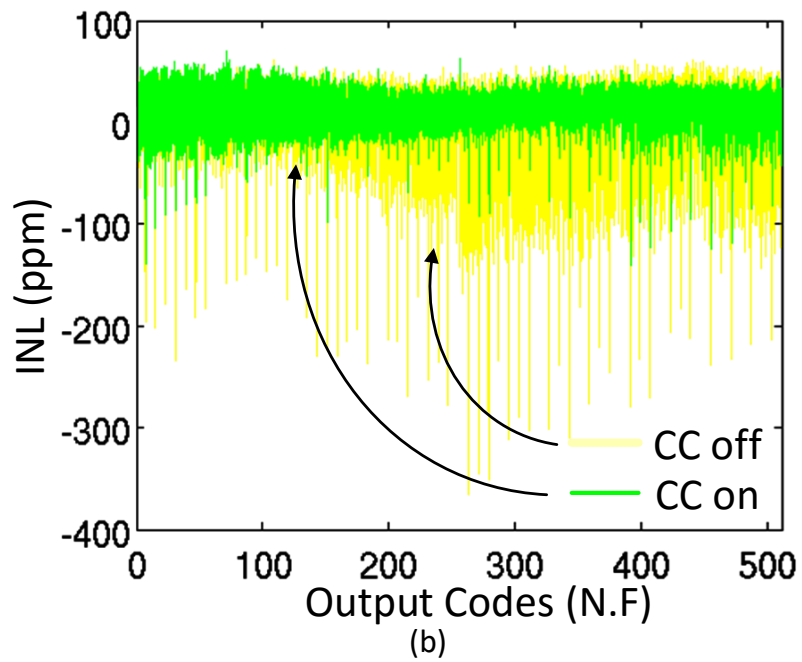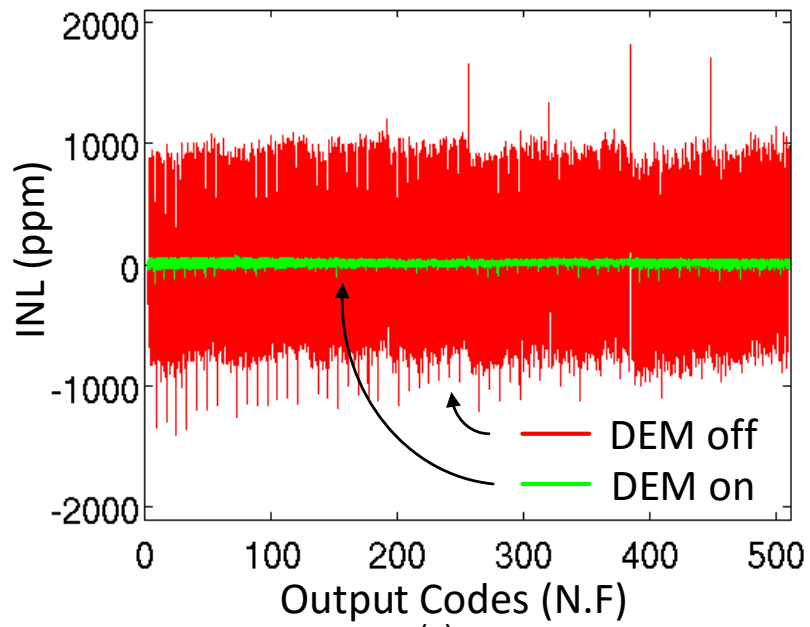
Figure 3.7. INL across modes (a) dynamic element matching on/off with common centroid

indexing on, (b) common centroid indexing on/off with dynamic element matching on.
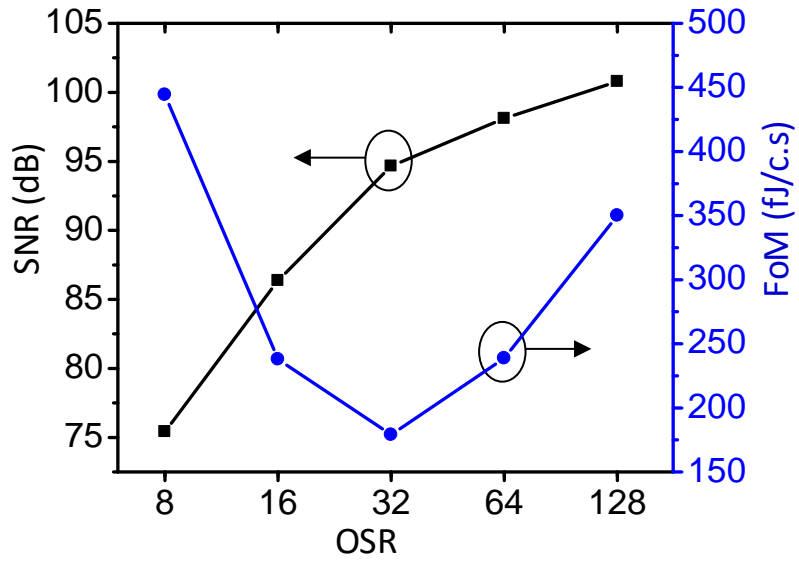
Figure 3.8. SNR and FoM across OSR with 4.29kS/s.
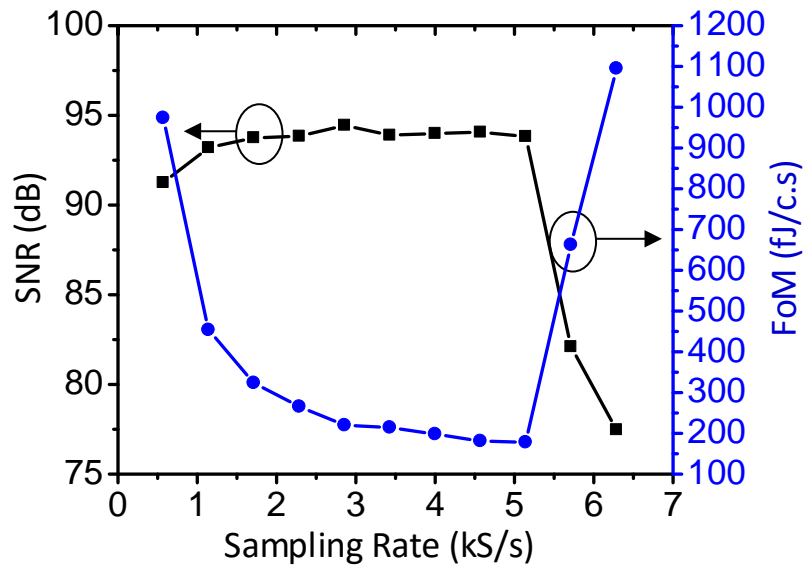
Figure 3.9. SNR and FoM across sampling rate with 32 OSR.

A CDC FoM is defined as $\frac{Power \times Meas.\ Time}{2^{(SNR-1.76)/6.02}}$, where $SNR = 20\log\left(\frac{Capacitance\ Range/2\sqrt{2}}{Capacitance\ Resolution}\right)$.

SNR and FoM across OSR and sampling rate are shown in Figure 3.8 and Figure 3.9. SNR is

obtained through the ratio of effective output range rms value and output rms noise.
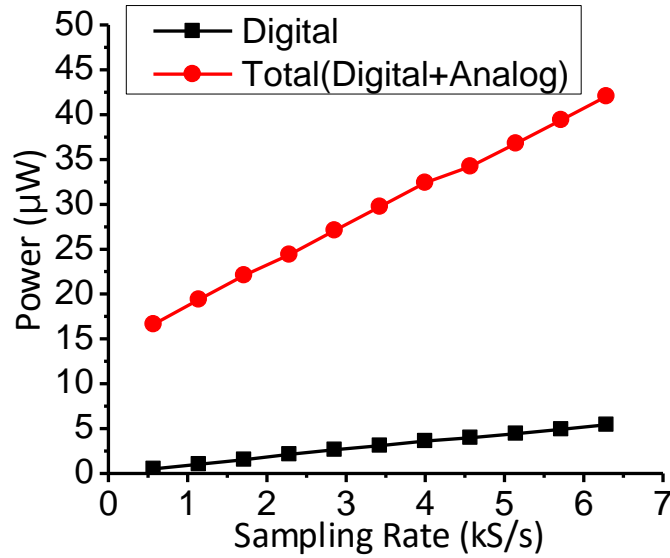
Figure 3.10. Digital and analog power across sampling rate with 32 OSR.
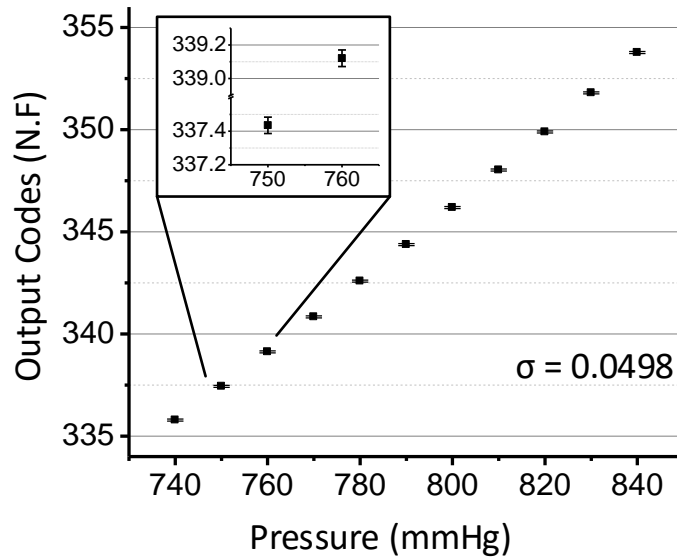
Figure 3.11. Pressure sensor test with the CDC.

Figure 3.10 shows power consumption across sampling rate with 11% being consumed by synthesized digital logic for signal control and decimation filters. Figure 3.11 shows pressure testing results with a MEMS capacitive absolute pressure sensor [36], we obtain 0.28mmHg resolution. The CDC active area is 0.456mm^2 (Figure 3.12).

Table 3.1 compares to other CDCs in the literature. This work achieved 94.7dB SNR, 0.16fF resolution, and 175fJ/c-s FoM at 32 OSR and 4.29kS/s.

Table 3.1. Performance summary and comparison with recent works.

	This Work	[20]	[16]	[32]	[33]	[6]	[40]	[41]	[42]	[43]
Technology(nm)	180	350	160	320	180	180	40	160	40	130
Method	ΣΔ +SAR	ΣΔ	ΣΔ	PWM	SAR	Dual Slope	Delay Chain	PM	SAR +VCO	IΣΔ
Capacitance Range(pF)	0-24	8.4-11.6	0.54-1.06	0.5-0.76	2.5-75.3	5.3-30.7	10.6	8	0-5	1
Meas. Time(ms)	0.23	0.02	0.8	0.033	4	6.4	0.019	0.21	0.001	100
Power	33.7 μW	14.9mW	10.3 μW	84 μW	160 nW	110 nW	1.84 μW	14 μW	75 μW	220 μW
Capacitance Resolution(fF)	0.16	0.06	0.07	0.8	6	8.7	12.3	1.4	1.1	5.4
SNR(dB)	94.7	84.8	68.4	40.9	55.4	44.2	49.7	65.6	64.2	96.3
FoM(pJ/c·s)	0.18	21	3.8	98	1.3	5.3	0.14	1.87	0.055	0.411
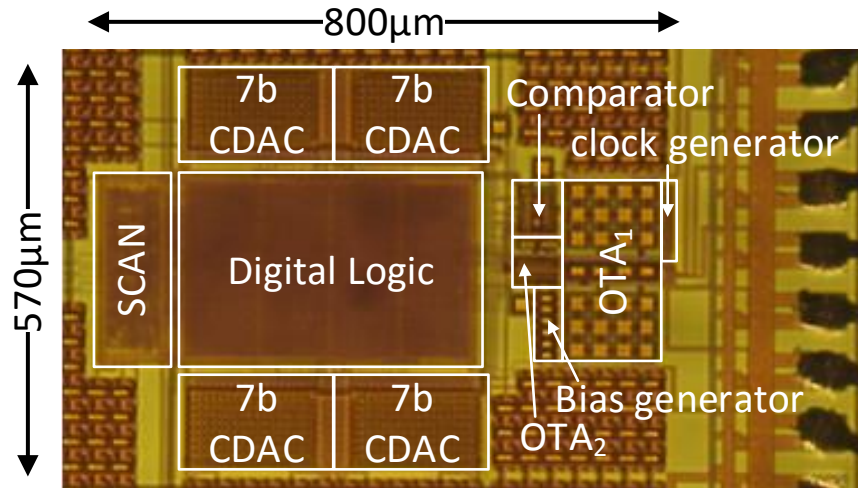
Figure 3.12. Die photo.

3.4 Conclusions

The proposed zoom-in incremental $\Delta\Sigma$ CDC uses 9b SAR conversion in the first phase in advance of $\Delta\Sigma$ conversion. It zooms in capacitance conversion range and improves resolution. The zoom-in approach significantly improved energy efficiency for high-resolution CDCs because the SAR conversion energy is negligible compared to energy from OTAs for the subsequent $\Delta\Sigma$. The proposed 9b DEM with the matrix unit-cap organization successfully suppressed almost linearity errors within 50ppm. The CDC achieved 180fJ/conv.step FoM, 94.7dB SNR, and 0.16fF capacitance resolution at 32 OSR and 4.29kS/s. The FoM is more than 2.3× and 21× better than recently reported high-resolution CDCs having >80dB SNR and <1fF capacitance resolution, respectively. This energy-efficient CDC is suitable for millimeter sensor nodes.

CHAPTER 4

An Infrared Gesture Recognition

System-on-Chip for Smart Devices

4.1 Introduction

Recent demand for natural human-computer interfaces such as gesture recognition has increased, particularly for compact wearable devices. Cameras are currently the most common platform for gesture sensing [44]–[48], but they are highly sensitive to environmental light conditions. Extended range capacitive sensing [49] and ultrasonic techniques [50] have been explored but they consume significant energy due to their excitation source.

In contrast, an infrared sensing system, in which a thermopile array directly converts incoming infrared radiation energy into electrical energy, is an appealing low-power choice since the sensor array itself is passive [51]–[54]. A thermopile is a series of thermocouples, consists of hot and cold contacts. The cold contacts are on a structural heat sink and the hot contacts are on a thin membrane. When the membrane is exposed to a hot object, the infrared radiation from the object heats up the hot contacts, and this makes a voltage by the Seebeck effect [55]. Thermopile pixel structures are p-type and n-type polysilicon pairs and can be fabricated in CMOS technology. By continuously sensing the voltages in the thermopile array, we can get a linear heating map
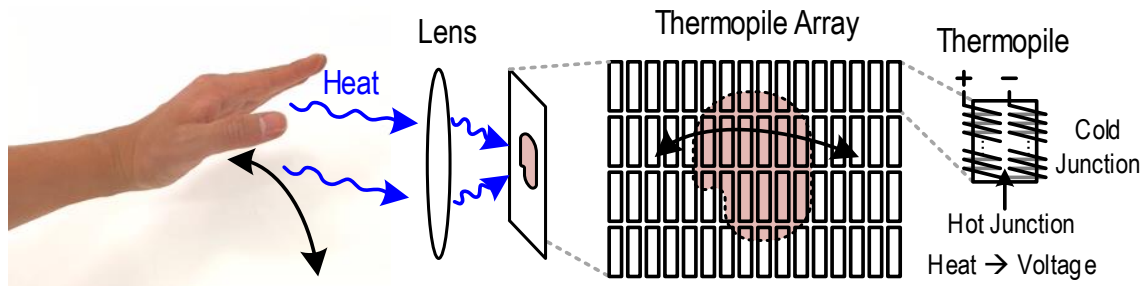
Figure 4.2. Gesture sensing using a thermopile array.
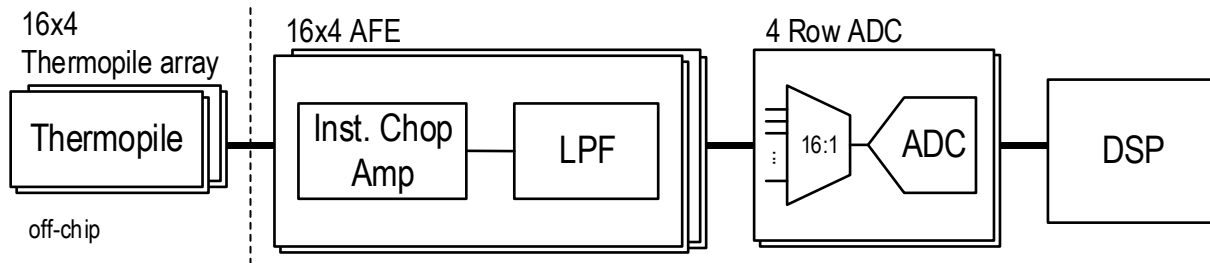
Figure 4.1. Block diagram of the proposed gesture sensing system.

video. However, array sensitivity is just a few µV/°C and its time constant is several ms while sensor noise is a few hundred nV. Therefore, to achieve ultra-low power gesture recognition, we propose an SoC including a low-noise instrumentation chopper amplifier for low-frequency signals, a low-power LPF for filtering out-band noise including the chopper frequency and its harmonics, an ADC, and a motion history image based [56] low-power DSP.

4.2 System Architecture

We target a gesture sensing system using a thermopile array (Figure 4.2 and Figure 4.1). A hand emits infrared radiation with wavelength representing its temperature; this forms an image incident upon a 16×4 thermopile array. Each thermopile signal connects to an AFE path that consists of an ICA and LPF. The four-row ADCs digitize the amplified/filtered signals using time-division multiplexing and the DSP then analyzes the waveform to detect gestures.

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4.3 Instrumentation Chopper Amplifier
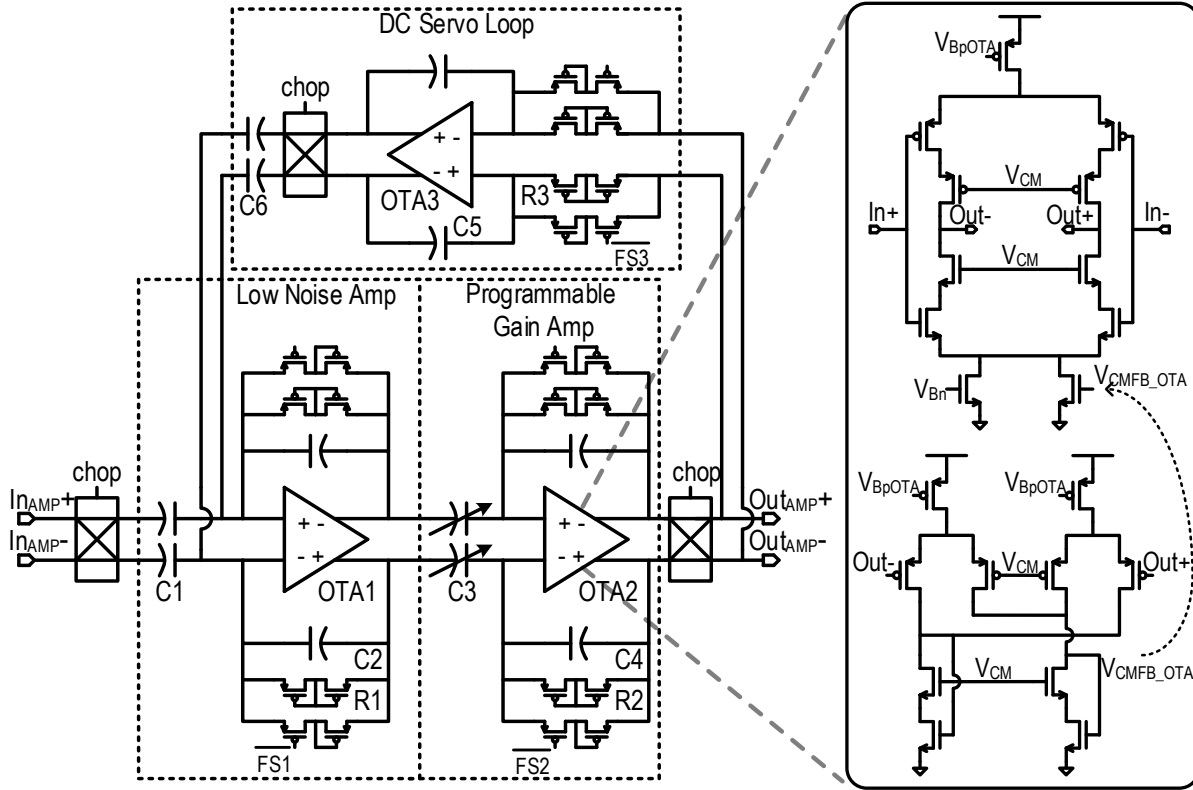
Figure 4.3. Proposed low-noise, programmable-gain Instrumentation Chopper Amplifier.

Figure 4.3 shows the proposed ICA. Since the gesture signals are significantly impacted by 1/f noise, they are chopped to remove this 1/f noise and then sent through two amplifiers. Overall gain needs to be up to 80dB for a power-efficient high dynamic range system. C_1/C_2 (15pF/150fF) and C_3/C_4 (C_4=20fF) set the gains for the Low-noise Amplifier (LNA) and Programmable-gain Amplifier (PGA), respectively. C_3 is programmable (200fF–3pF) for system flexibility. OTA$_1$ and OTA$_2$ are implemented with inverter-based cascode amplifiers to maximize g_m and gain at a given current. The common-mode feedback (CMFB) amplifiers consume a fraction of the power using ratioed transistor sizes. As in typical noise-limited designs, the first amplifier stage consumes the majority of the total power (up to 2.5μA current) to achieve sub-μV

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noise while the PGA consumes just 90nA, constrained by the chopper bandwidth. Transistor sizes are chosen for optimal noise efficiency factor (NEF) and chopper frequency is 1kHz. The ICA high-pass corner is set by $(R_3C_5)^{-1}$ in the DC servo loop. R_1 and R_2 paths set the input common mode voltages and cancel the offsets. Fast-settling switches (FS_{1-3}) are selectively turned on to reduce settling time when ICA settings are changed, decreasing the corresponding resistance by $100\times$ in simulation.
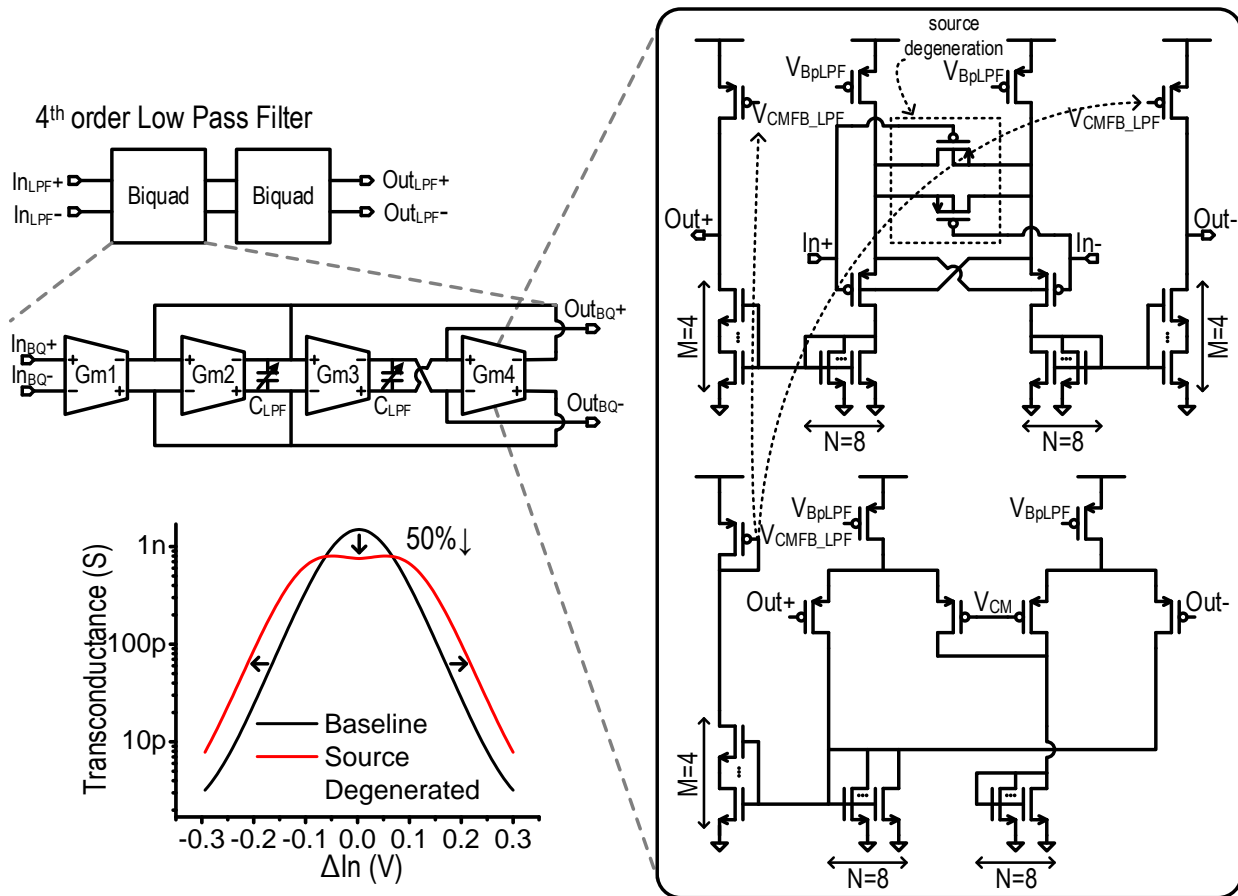
Figure 4.4. Proposed 30Hz Gm-C Low Pass Filter.

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4.4 30Hz Bandwidth Gm-C Low Pass Filter

The ICA outputs show ripple at the 1kHz chopping frequency and its harmonics. These are removed with the proposed Gm-C LPF in Figure 4.4. The two biquads are connected in series to form a 4th order filter. Since the gesture information resides in a low-frequency range, the LPF bandwidth is set to 30Hz to achieve high SNR. C_{LPF} is a capacitor array and is set to 8.9pF to approximately match AFE and thermopile pixel size. Considering $f_{LPF3dB}=g_m/(2\pi C_{LPF})$, g_m in the nS range is required. To achieve this bias current must be extremely low, leading to potentially poor linearity. Thus, source degeneration and g_m division techniques [57] are used in the LPF. The Gm-stage input current is divided by the series-parallel current mirror to effectively obtain $g_m/32$. To enhance linearity, input pair sources are degenerated by pseudo-resistors whose gates are controlled by inputs. Simulation results show the resulting g_m is linear within ±100mV input range (defined by full width at half-maximum). The CMFB amplifier replicates voltages in the main Gm stage and sets the common mode output voltage. LPF outputs in each row are time-multiplexed
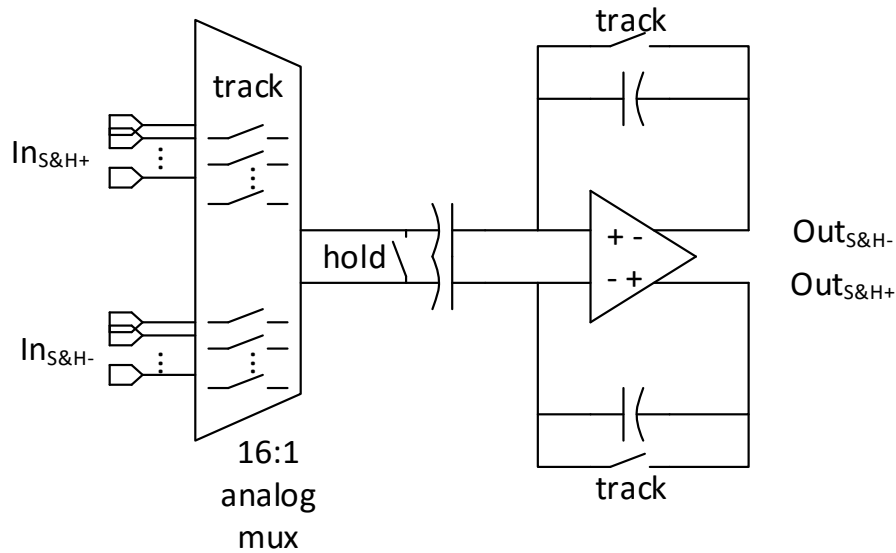
Figure 4.5. 16:1 analog mux with track and hold amplifier.

row1	1	2	3	4	5	...	16
row2	1	2	3	4	5		16
row3	1	2	3	4	5	...	16
row4	1	2	3	4	5		16
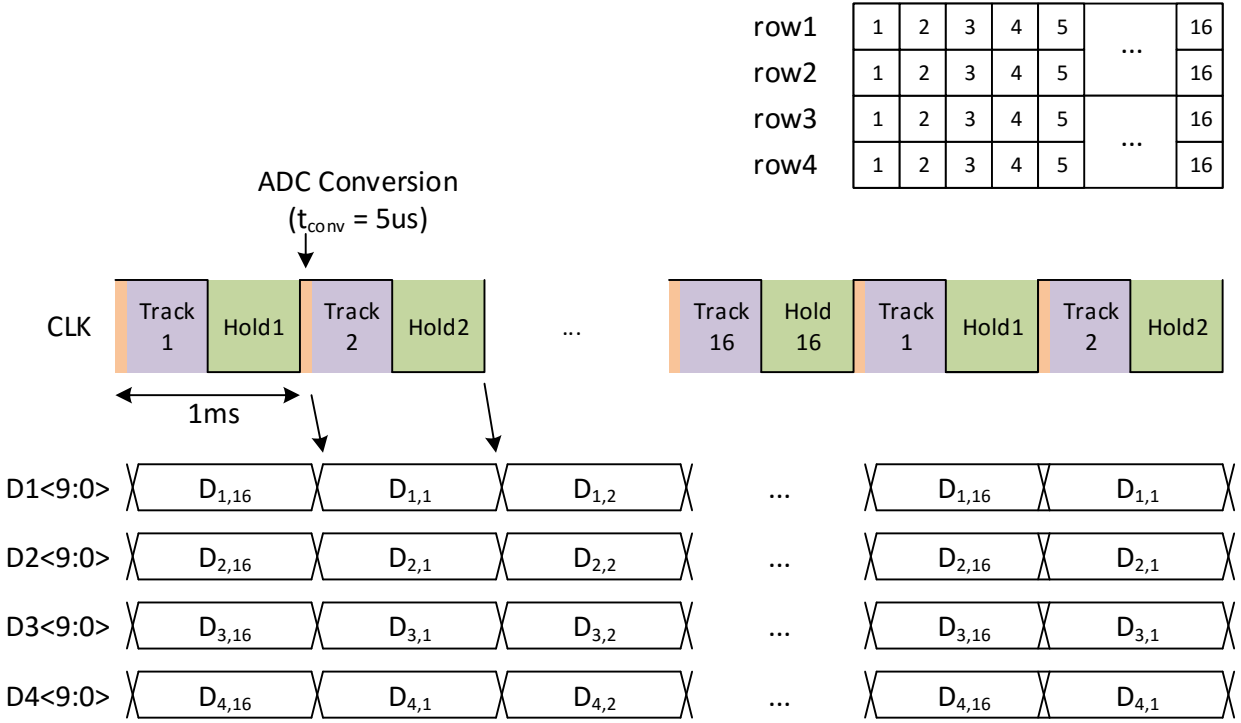
Figure 4.6. Time multiplexing waveform.

via a 16:1 analog multiplexer (Figure 4.5). With every cycle, the sample and hold amplifier transfers the next neighboring column data to a differential 8b SAR ADC (Figure 4.6, Figure 4.7). The ADC sampling rate is 1kS/s.
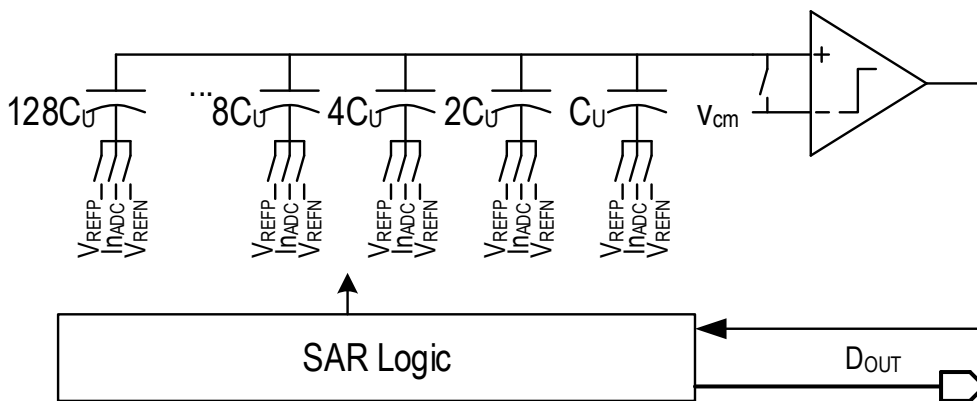
Figure 4.7. 8b SAR ADC schematic (the actual implementation is differential).
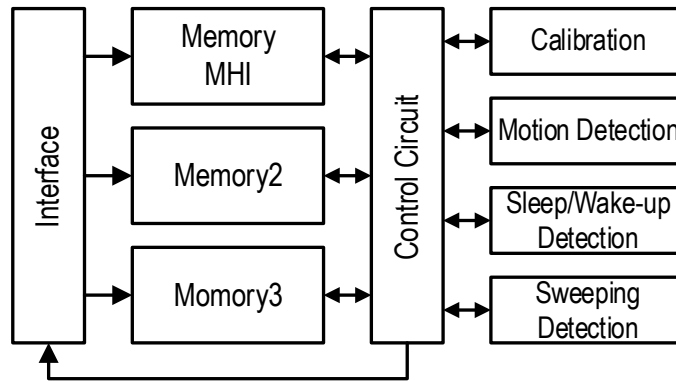
Figure 4.8. Gesture detection processor block diagram.
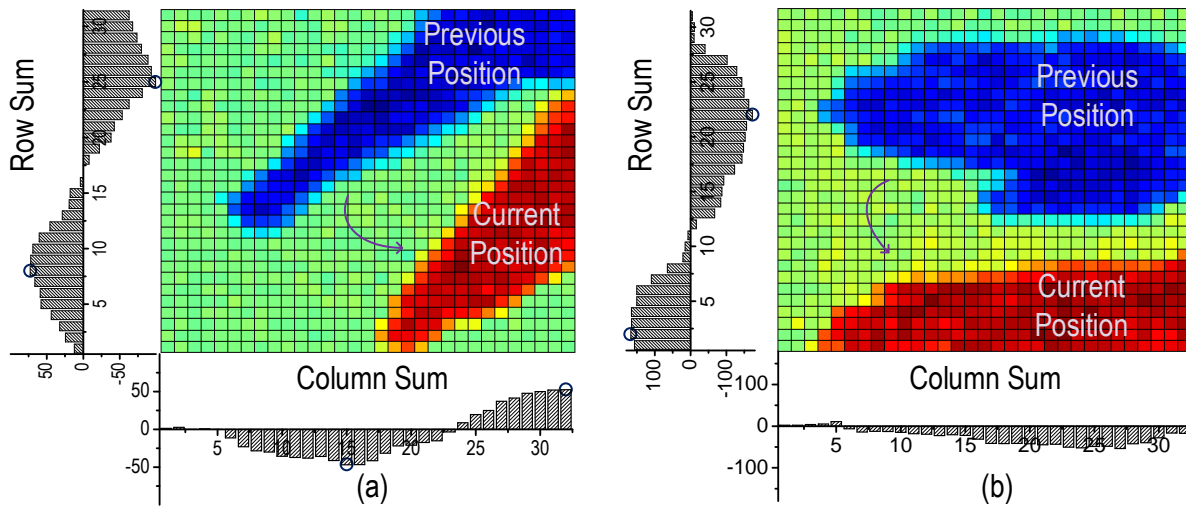
Figure 4.9. Motion history image and row- and column-wise sums for a sweep detection (a) diagonal (b) up→down (simulated).

4.5 Motion Recognition Digital Signal Processor

Figure 4.8 describes the overall structure of the proposed motion recognition DSP. There are three separate memories to store frame data. The first memory contains the motion history image (MHI), which is the difference between the current and previous frames (Figure 4.9). The

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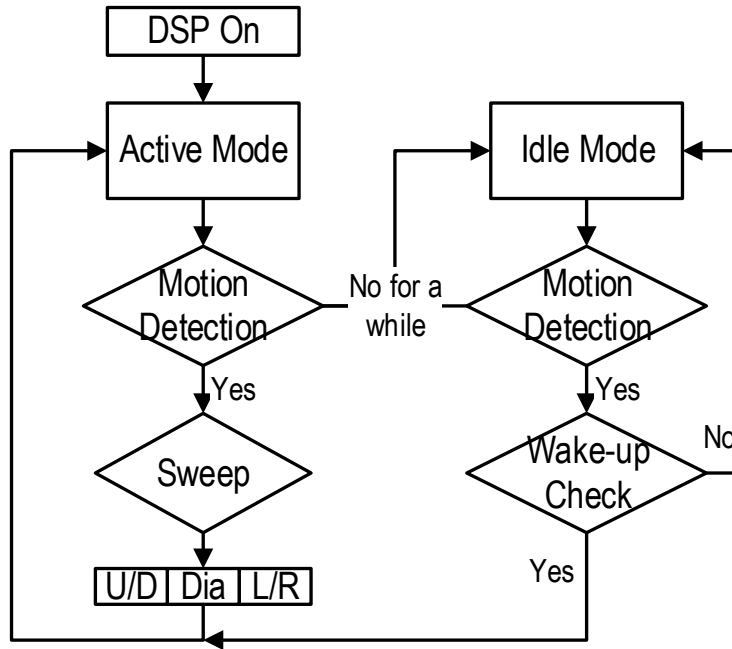
Figure 4.10. DSP Detection algorithms.

second and third memories are used to store two continuous frames once motion is detected. Detection modules use data from the three memories to analyze the gesture. Figure 4.10 shows the top-level design for the proposed gesture detection algorithm. Motion is detected by counting the number of pixels having a significant change in value (i.e., ADC output code) between the current and previous frame. If there is no motion for a period of time the processor goes into an idle mode with only a simpler motion detecting circuit enabled to save power.

When motion is detected, a sweeping algorithm uses two motion history image frames to analyze the motion. In this process, each row and column of the MHI frames are first summed. The type of movement (diagonal, up-down, or left-right) is then discerned based on the number of peaks found in the row- and column-wise sums. In a diagonal sweep, both row and column sums will exhibit clear peaks (i.e., four total peaks detected) whereas in up-down or left-right sweeps only two peaks are observed due to constant behavior in either the horizontal or vertical direction. This is shown in Figure 4.9, which illustrates the principle of detection for sweeping gestures. Up-

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down or left-right direction can be determined based on the relative positions of negative to positive peaks, as seen in Figure 4.9. This approach allows the DSP to accurately identify specific gestures.

4.6 Measurement Results

The proposed gesture recognition SoC is implemented in 65nm CMOS and has an area of 8.1mm^2 (Figure 4.11). The ICA input referred noise density is 31nV/$\sqrt{\text{Hz}}$ in active mode and
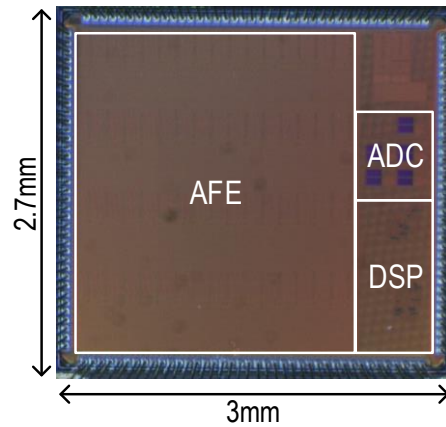
Figure 4.12. Die photo.
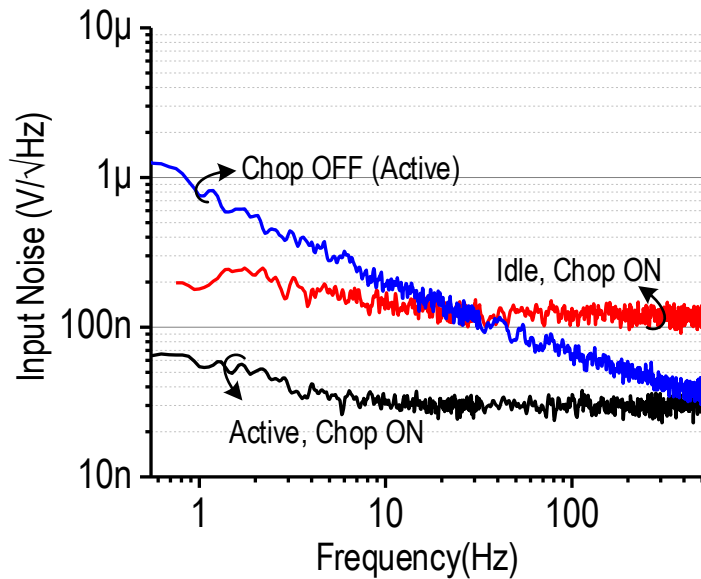
Figure 4.11. Measured ICA input referred noise.

$130nV/\sqrt{Hz}$ in idle mode (Figure 4.12), and chopping successfully suppresses 1/f noise. The ICA gain is programmable by C_3 changes, and the measured range is 57.2-78.3dB. It draws 2.655μA and 0.277μA in the active mode and the idle mode respectively at 1.4V VDD. DC common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) are larger than 130dB. The calculated noise efficiency factor (NEF) is 2.0 for the active mode and 2.7 for the idle mode. The measured HD3 is 48.2dB with 400mVpp and 100Hz ICA input.

LPF bandwidth is adjustable between 10−150Hz by C_{LPF} changes and a 4th order roll-off (80dB/decade) is measured as expected (Figure 4.13). Figure 4.14 shows the LPF noise spectrum. The in-band noise floor is $28μV/\sqrt{Hz}$ and HD3 is 45.5dB with 0.1Vpp and 5Hz LPF input, achieving 0.55% THD. The integrated input referred noise is 154 μVrms at 30Hz bandwidth setting. The LPF draws 140nA at 1.4V VDD.
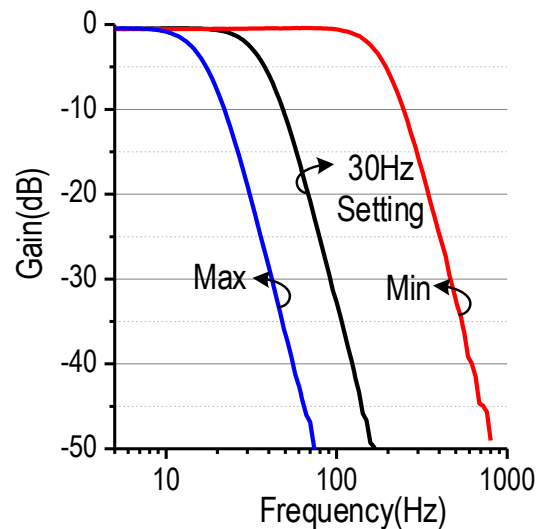
Figure 4.13. Measured LPF frequency response across different C_{LPF}.
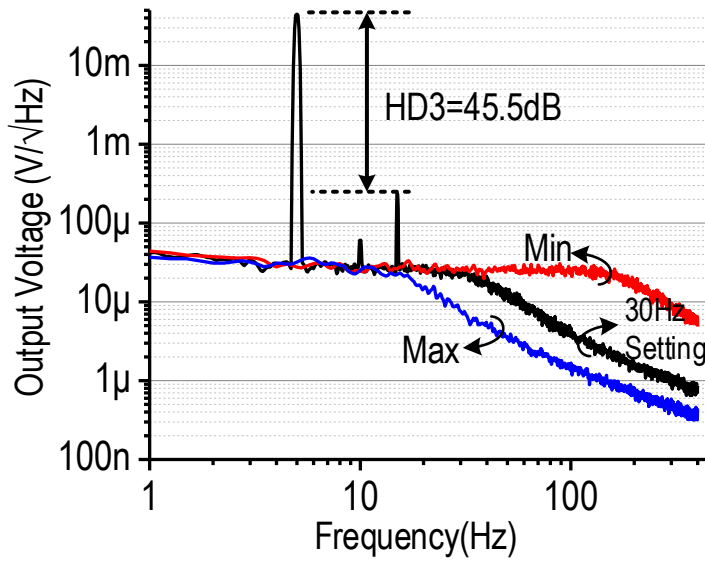
Figure 4.14. Measured LPF output noise with different C_{LPF} (0.56-8.9pF)

Figure 4.15 shows the 8b ADC performance. Maximum DNL and INL are 0.15 LSB and 0.12 LSB respectively. It achieves 48.8dB SNDR with 1kS/s sampling rate and the Nyquist rate input. The measured SFDR is 65.9dB.
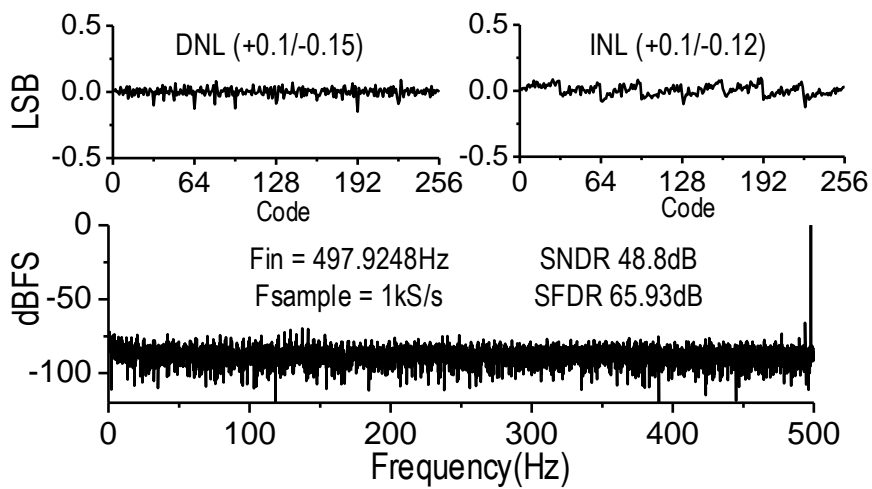
Figure 4.15. Measured ADC DNL, INL, FFT results.
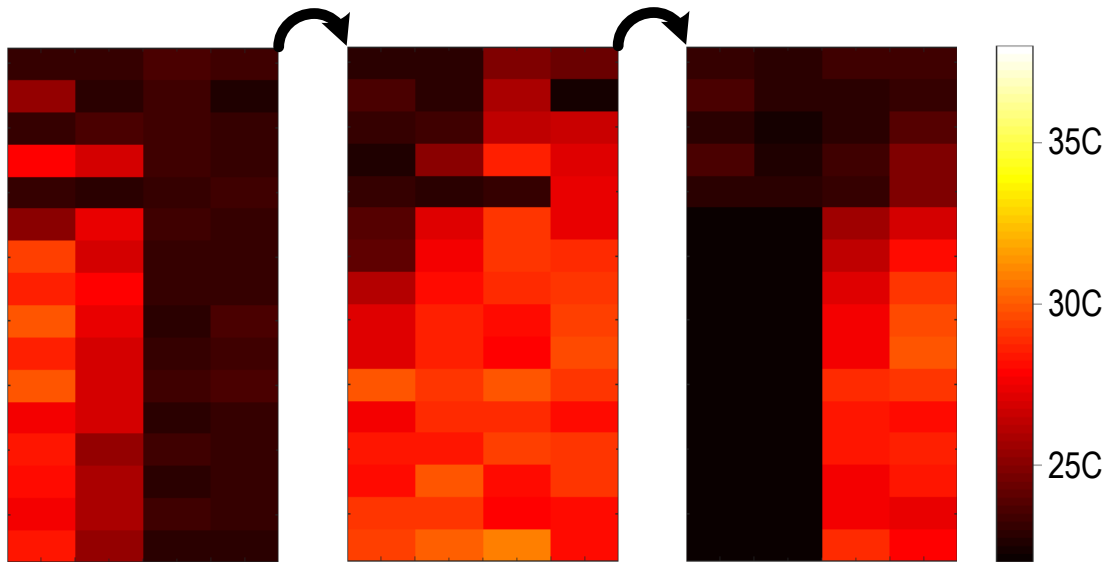
Figure 4.16. Motion snapshot (Left → Right sweep).

The system is demonstrated with an external 16×4 thermopile and lens, and Figure 4.16 shows detection of a hand sweeping across the field of view. Table 4.1 summarizes measured results and compares with recent works.

Table 4.1. Performance summary and comparison with recent works.

Inst. Chop. Amp	Idle	Active	[58]	[59]
Noise (RTI) (nV/rtHz)	130	31	60	59
Gain (dB)	57.2-78.3		40	41.8-59.2*
Chopping Frequency (kHz)	1		5	4,8,12**
Current (µA)	0.277	2.655	1.8	0.266
CMRR (dB)	>130		134	89
PSRR (dB)	>130		120	92
NEF	2.7	2.0	3.3	1.4
Area (mm2)	0.04		0.1	0.25
VDD (V)	1.4		1	1
Low Pass Filter	This work		[60]	[61]

Cut off Frequency Range (Hz)	10-150	1.5-15	250
THD (%) @Vin (Vpp)	0.55 @0.1	1 @1	0.4 @0.1
HD3 (dB) @Vin=0.1Vpp	45.5	N/A	48.9
Current (µA)	0.14	550	0.45
Gain (dB)	-0.5	0	-10.5
Integrated Noise (RTI) (µVrms)	154***	320	340
Order	4	2	5
Area (mm2)	0.04	0.34	0.13
VDD (V)	1.4	3.3	1

ADC		**System**	
Resolution (bit)	8	Technology	CMOS 65nm
SNDR (dB)	48.8	FPS	30
Max INL (LSB)	0.12	Active Power (µW)	260
Power (µW)	0.06	Idle Power (µW)	46
Samplring rate (kS/s)	1	Active Power/ch (µW/ch)	4.06
DSP		Idle Power/ch (µW/ch)	0.72
Power (µW)	5	*open loop gain	
Clock Frequency (kHz)	4	**multi chopper n=3	
VDD (V)	0.7	***measured at 30Hz BW setting	

4.7 Conclusions

We proposed a low power gesture-sensing system for smart devices using a passive 16×4 infrared sensor array. The thermopile-based motion recognition system is light insensitive and uses low power while conventional gesture sensing systems have relied on light sensitive cameras or power hungry excitation sources. The proposed ICA achieved 2.0 NEF by removing flicker noise, which is a dominant noise source of a low bandwidth application. It uses low current to reduce standby power when the system is in the idle mode. By using pseudo-resistor based source degeneration and g_m division techniques, the LPF achieved 154 µVrms integrated input noise and 0.5% THD at 0.1Vpp. The DSP employed motion history image technique for low-power detection. This work represents the first SoC for gesture sensing applications using a thermopile array. Its size (8.1mm²,) and power (260µW and 46µW) are suitable for emerging smart devices.

CHAPTER 5

A Low-Power Switched Bias Preamplifier

for MEMS Microphones

5.1 Introduction

MEMS microphones have become popular for consumer electronics because of their small size, low price, and high sound quality. MEMS microphone market has been growing and is estimated to reach $1.4 billion and 5.4 billion unit shipments in 2017 according to IHS Technology [62]. Among them, high SNR microphones lead the market growth with the appearance of new types of devices such as wearables, biomedical devices, and IoT. High SNR microphones improve far-field audio quality and clarity and enhance voice interface. The voice interfaces are expected to play a dominant role in these types of devices where touch-based interfaces are limited because of small size (wearables) and inaccessibility (medical devices). Enabling audio interfaces in these types of devices calls for low-noise and low-power interface circuits to achieve great far-field audio quality and long battery life. One key challenge lies in the low-power microphone preamplifier implementation; this component represents the most noise/power sensitive block in the entire signal chain.

A MEMS microphone consist of two parallel plates forming a pressure-sensitive capacitor as shown in the left of Figure 5.1. One plate is a fixed rigid electrode, filled with holes allowing air flows, while the other is a movable diaphragm vibrated by a sound wave. The microphone capacitance is given by $C_M = \epsilon \cdot \frac{A}{d}$ where ϵ is air permittivity, A and d are the area of a plate and the distance between plates respectively. The microphone charge is given by $Q_M = C_M \cdot V_B$, where V_B is the bias voltage of the microphone. When the charge on the microphone is constant, the voltage change is given by $\Delta V_B = \frac{V_B}{C_M} \cdot \Delta C_M$. It represents the diaphragm vibration can be detected by the voltage sensing, and the microphone sensitivity is proportional to V_B. Therefore, high bias voltage V_B is generally preferred to achieve high sensitivity, while maintaining safe margin from its pull-in point where two plates snap together because of their electrostatic force.

$$S = \frac{\Delta V_B}{\Delta P} = \frac{V_B}{C_M} \cdot \frac{\Delta C_M}{\Delta P}$$
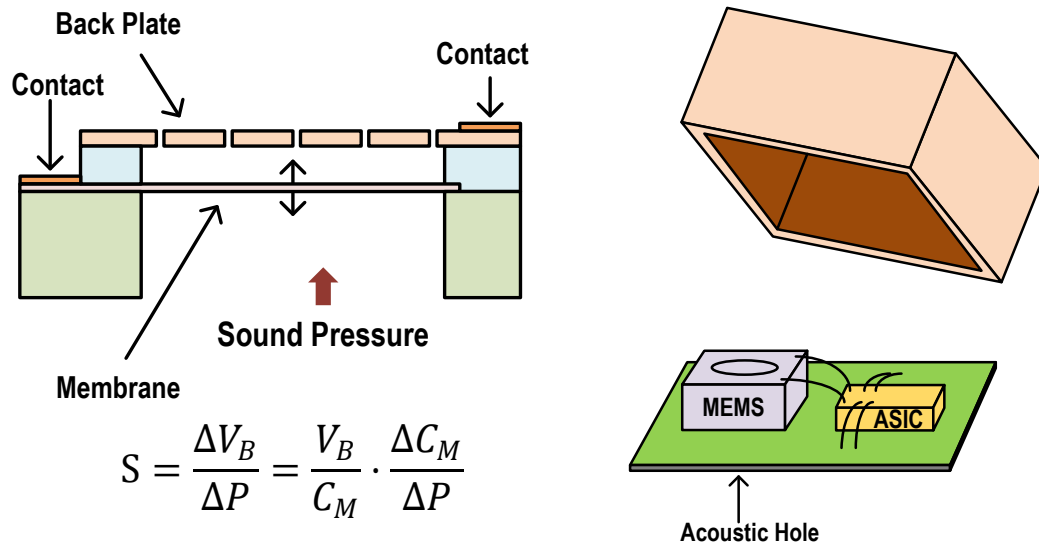
Figure 5.1. Illustration of a MEMS sensor (left) and microphone assembly with ASIC on a substrate board with a lid (right).

5.2 Conventional Readout Schemes with Preamplifiers

Figure 5.2 shows conventional microphone readout schemes with preamplifiers. In Figure 5.2(a), the microphone signal is delivered to the preamp input via C_C coupling [11], [63]. The
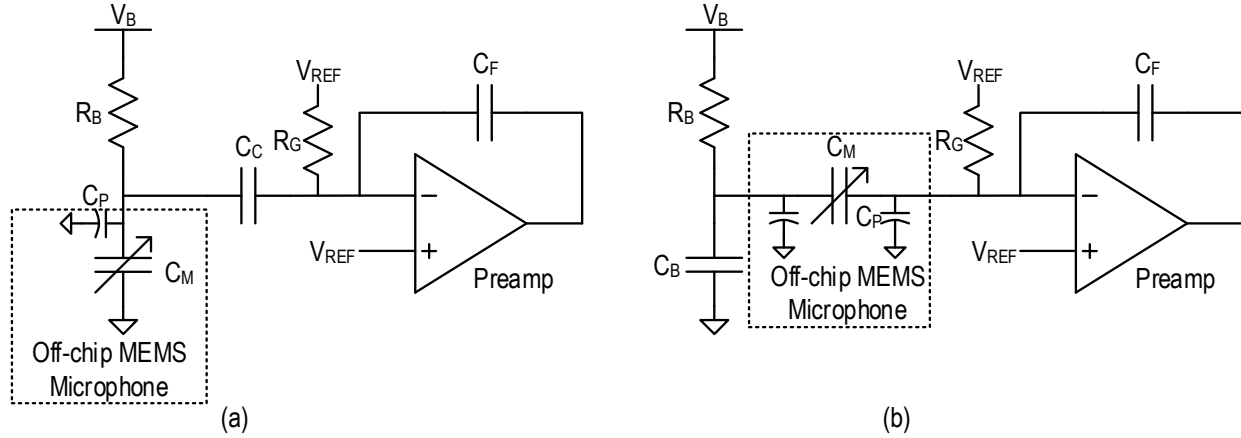
Figure 5.2. Conventional microphone readout circuits with preamplifiers.

microphone top plate is biased at V_B via R_B, which is higher than usual analog VDD, while the bottom plate is connected to VSS. The V_B can be generated with a simple charge pump because R_B and C_F forms a low-pass filter and it filters out the charge pump noise. The input of the preamp is biased at V_{REF} through R_G, and hence (V_B-V_{REF}) is applied to C_C. R_B and R_G have very high resistance and can be implemented with diode connected PMOS. The signal gain is $-\frac{C_C}{C_F} \cdot \frac{C_M}{C_M+C_P+C_C}$ with the C_F feedback assuming an ideal OTA. The gain is dependent on C_C and C_P and it creates nonlinearity. In Figure 5.2(b), (V_B-V_{REF}) is applied to CM and the signal gain is $-\frac{C_M}{C_F}$ and insensitive to C_P [64]. However, C_B needs to be much larger than C_M to filter out V_B noise from a charge pump, and it costs large die area.

5.3 Preamplifier 1/f Noise

The human audible frequency range is 20-20kHz and microphone preamp noise is therefore severely impacted by 1/f noise. Figure 5.3 shows input referred noise of the conventional preamp (Figure 5.2(b)) in spice simulation with 5µA. The noise corner frequency is about 5kHz as shown in Figure 5.3(a). The integrated noise in audio band (20-20kHz) is 7.6µVrms, and the 1/f noise contributes 60%. The A-weighted integrated noise is reduced to 4.7µVrms (Figure 5.3(b)), but the 1/f noise contribution increases to 68%. Therefore, 1/f noise should be reduced to optimize the noise efficiency of the preamplifier.
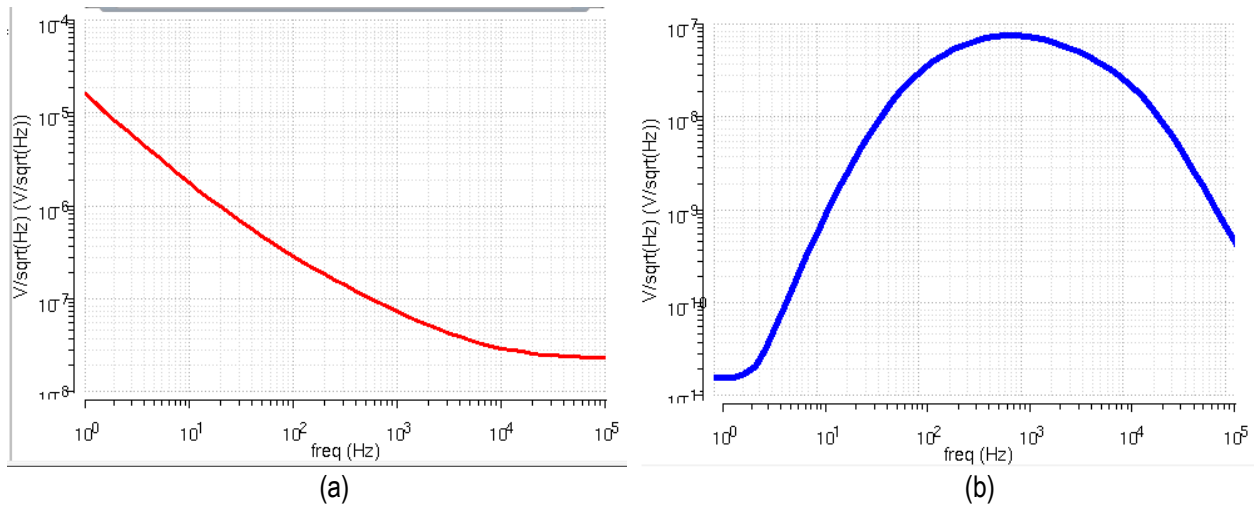
Figure 5.3. Input noise of the conventional preamp. (a) No weighted, (b) A-weighted.

Capacitive coupled chopper amplifiers are often used to remove 1/f noise in low-power time-continuous applications, this approach, however, cannot be used with high impedance input sources such as MEMS microphones (with base capacitance of several pF) since the associated switching current causes high voltage output noise [65]–[67]. Therefore, large input transistors must be used to reduce 1/f noise. However, it also increases gate capacitance and noise gain, and thus degrades noise efficiency factor (NEF) [67], [68]. Another approach provides excitation signals for capacitive sensors to remove 1/f noise [12]. However, the AC bias needs two low-noise

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(e.g. <<10uV) and low-impedance reference voltages which require large area, power or limited allowable DC bias level (e.g. VDD) resulting in low microphone sensitivity (given by $S = V_B/C_M \cdot \Delta C_M/\Delta P$). Also, an additional DC capacitance canceling path for carrier signal removal increases noise gain and NEF by 2×.

To overcome these limitations, we propose a low-power switched-bias preamp for MEMS microphone applications. Periodic on/off switching of a MOSFET between strong inversion and accumulation has been shown to reduce 1/f noise [69]–[73]. 1/f noise is caused by the trapping/de-trapping process of carriers in the gate oxide. The trapping-detrapping process occurs with a wide range of time constants, including very long timeframes. By turning the device on and off, the long-term memory effect of 1/f noise is essentially re-set and low-frequency 1/f noise is inherently reduced. With the switched MOSFET, the proposed preamp achieves 6.3µVrms input referred noise (A-weighted) while consuming 7.6µA.

5.4 Proposed Chopper Preamplifier

Figure 5.4 shows the proposed microphone preamplifier. C_C couples V_B and the preamp input common mode voltage to allow the microphone to benefit from a high bias voltage without C_B while the preamp can use a low VDD for low power. Since V_B noise is low-pass filtered by R_B and C_F, a simple charge pump can be used without additional filtering. The signal gain is $-C_M/C_F$ (9.6dB) and insensitive to C_P, C_C, and C_G, resulting in excellent linearity. The amplifier noise can be expressed in input referred noise, mainly contributed by the input transistor pairs. The noise gain of the feedback loop is $\left((C_M + C_P + C_F + C_G) + (C_M + C_P + C_F) \cdot C_G/C_C\right)/C_F$. Thus, large C_C with small C_P and C_G are needed to minimize the noise gain. C_C is chosen as $3\times C_M$, which is
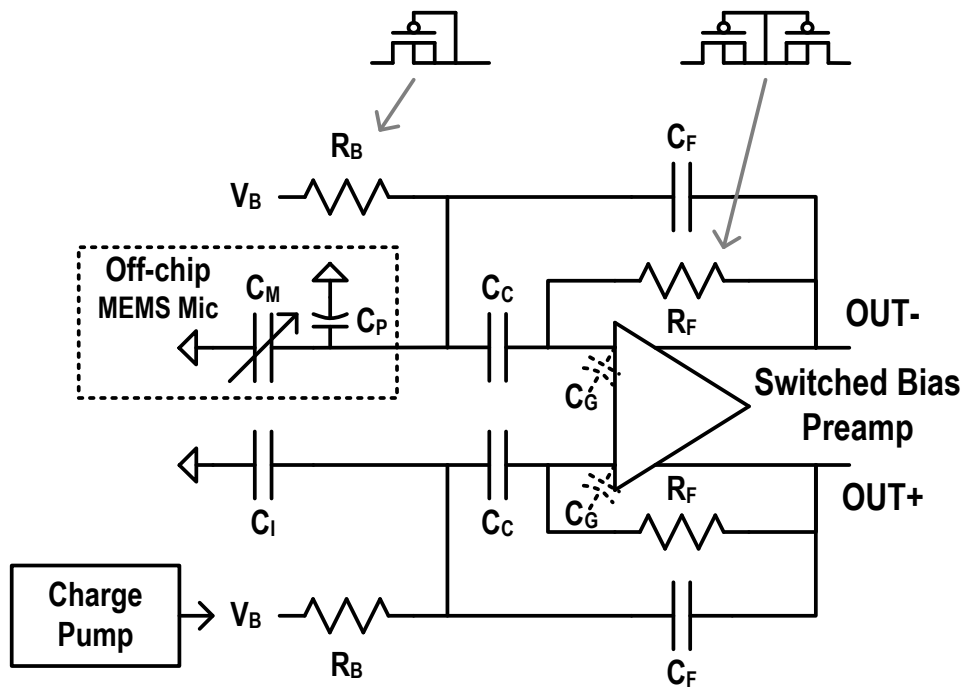
Figure 5.4. Proposed microphone preamplifier.

limited by the fact that C_C parasitics also contribute to C_P and C_G. C_I is a six-bit programmable capacitor array and it is tuned to C_M+C_P to maximize noise efficiency during testing. MOM capacitors are used for C_P, C_C, and C_I to avoid leakage at high voltage bias. R_B and R_F are

implemented with pseudo-resistors to achieve high resistance with small area. These resistances are used to make high-pass poles and must be sufficiently large that they do not impact the low-frequency response (<20Hz) of the microphone. R_F sets the input common mode voltage and cancels the preamp DC offset.

Figure 5.5 shows the detailed implementation of the proposed switched-bias preamp. The preamp consumes 7.6μA and is implemented with an inverter-based cascode amplifier to maximize g_m and gain at a given current. 3dB SNR is enhanced because the same bias current is used for both PMOS and NMOS. CMFB is composed of a differential difference amplifier, which sets output common mode voltage and uses 1/16 current of the main amplifier. Transistor sizes are chosen to optimize noise efficiency with A-weighted filtering. R_F cannot cancel the DC offset between left and right paths, but + and – inputs. Therefore, M_{LIN+} and M_{RIN+} (M_{LIN-} and M_{RIN-}) are interdigitated rather than M_{LIN+} and M_{LIN-} (M_{RIN+} and M_{RIN-}) in the layout.

In the preamp, the left or right path is alternatively used according to the phase of Φ, and cascode and current source devices are shared for all phases. Here Φ is a 140kHz clock, which is set to be out of the audio band. With Φ=0, current flows through the left path of the preamp, while the right pair transistors are clock gated (Figure 5.6). M_{LP1-3} and M_{LN1-3} are ON and M_{LP4-6} and M_{LN4-6} are OFF so that the left input pairs ($M_{LPIN+/-}$ and $M_{LNIN+/-}$) are connected to the cascode and current source devices and used for the signal amplification. Meanwhile, the right input pairs ($M_{RPIN+/-}$ and $M_{RNIN+/-}$) are in the super-cutoff region by connecting M_{RN4-6} to VSS and M_{RP4-6} to

VDD to enhance 1/f noise reduction. While Φ=1, the preamp uses the right path and the left path is similarly clock gated.
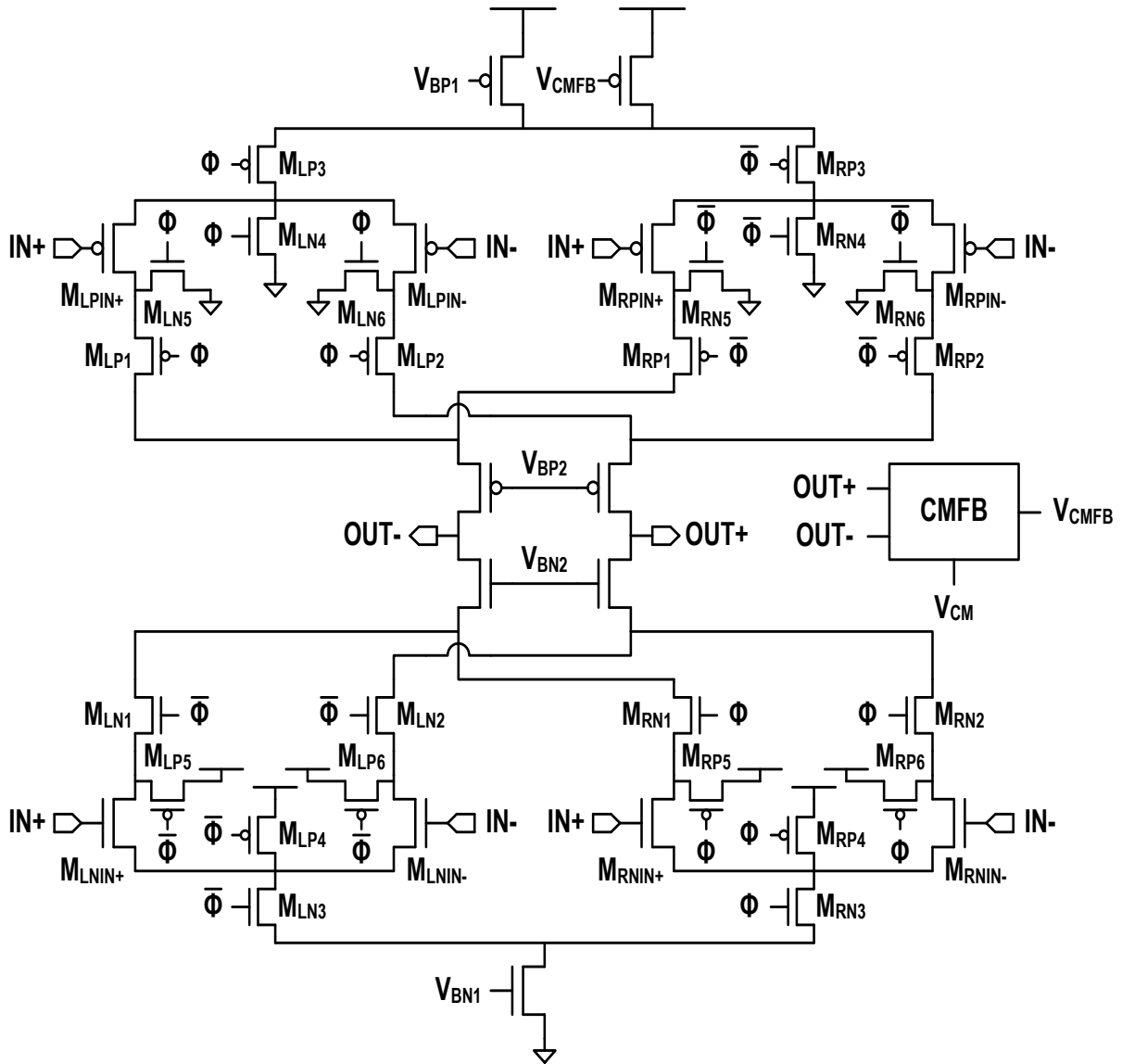
Figure 5.5. Detailed implementation of the switched-bias preamp.
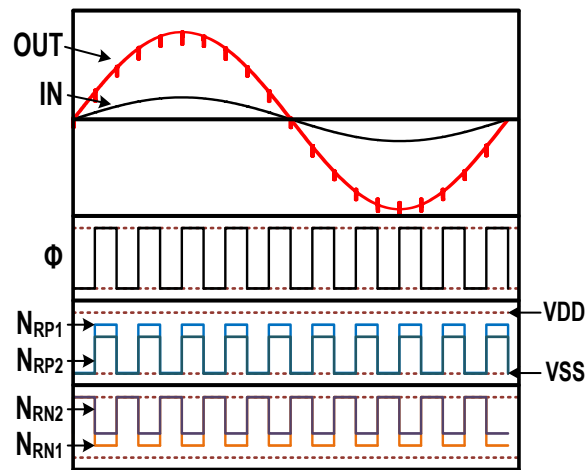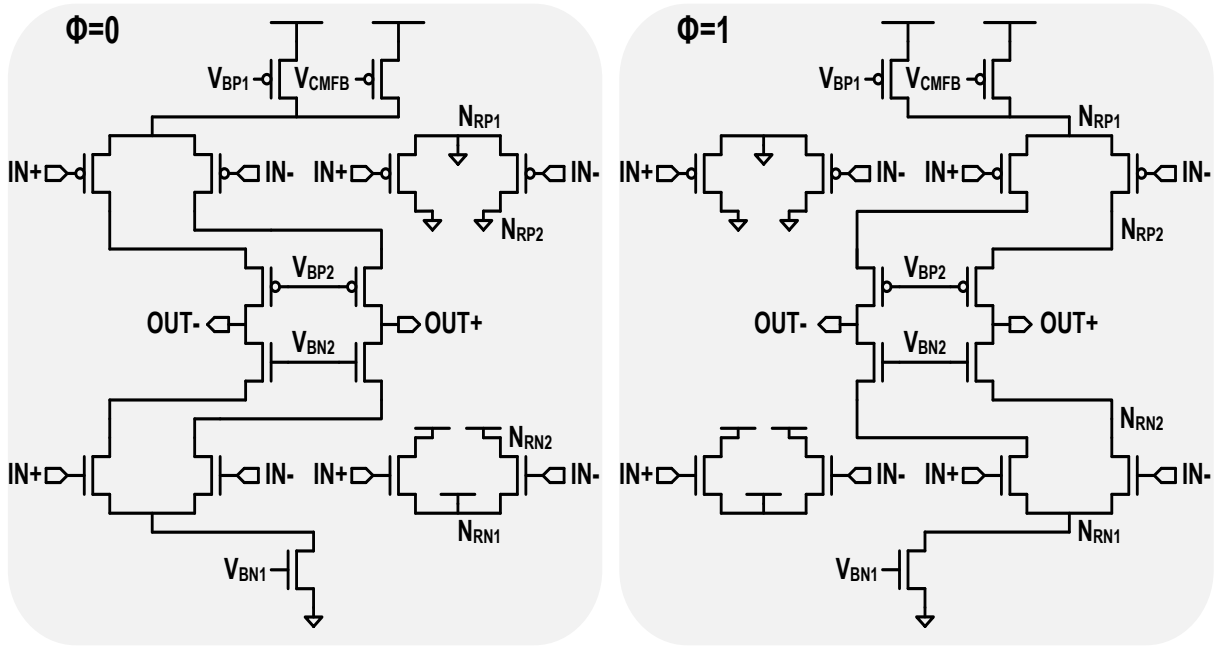
Figure 5.6. Transient behavior of the switched-bias preamp.

5.5 Measurement Results

The microphone preamp is fabricated in 180nm CMOS and tested at 1.4V VDD. Figure 5.7 shows measured frequency response of the preamp. The preamp gain is 9.6dB and high pass corner frequency is 0.4Hz. PSRR in audio band with a 100mVrms tone is >79dB and >66dB with and without the switched bias, respectively, demonstrating significant improvement from the proposed technique.
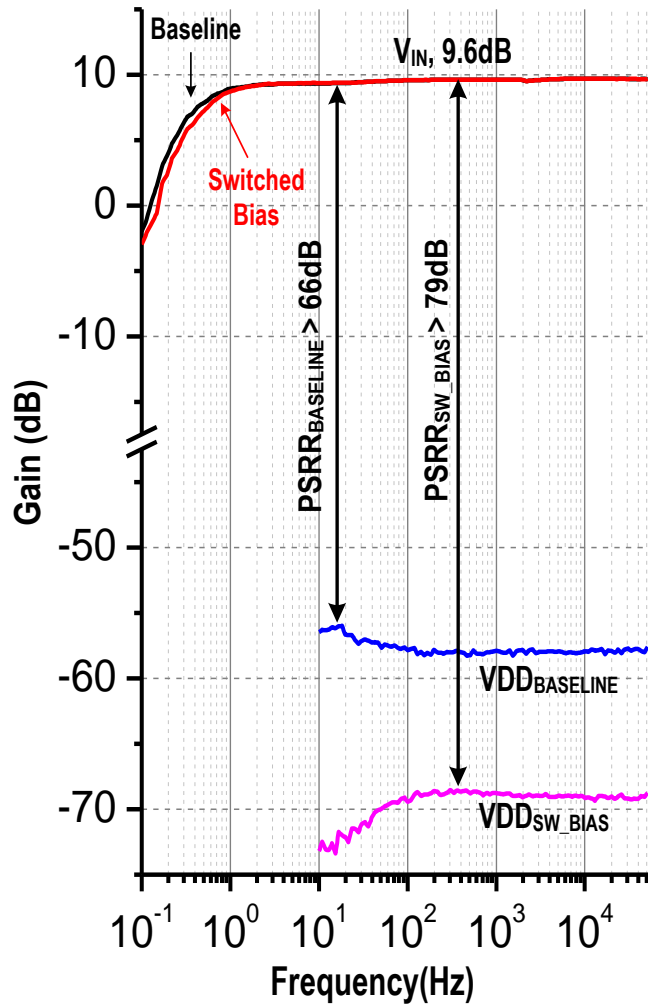
Figure 5.7. Measured frequency response of the preamp.

With the switched bias, the preamp output offset difference between the two paths is 1.2mV and overshoot is 3mV (Figure 5.8 (left)). The offset distribution of 17 parts was tested; its mean is 0.08mV and standard deviation is 3.90mV as shown in the right of Figure 5.8. THD is measured
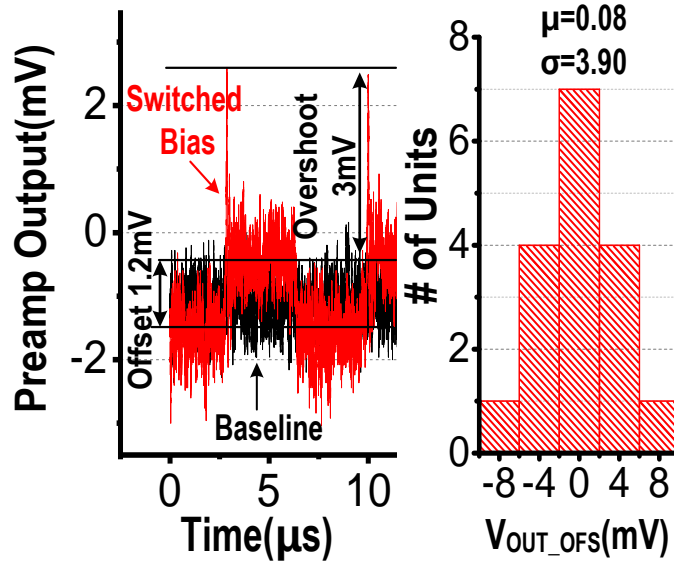
Figure 5.8. Switching ripples showing offset and overshoot from the switched bias (left), and the offset distribution of 17 parts (right).
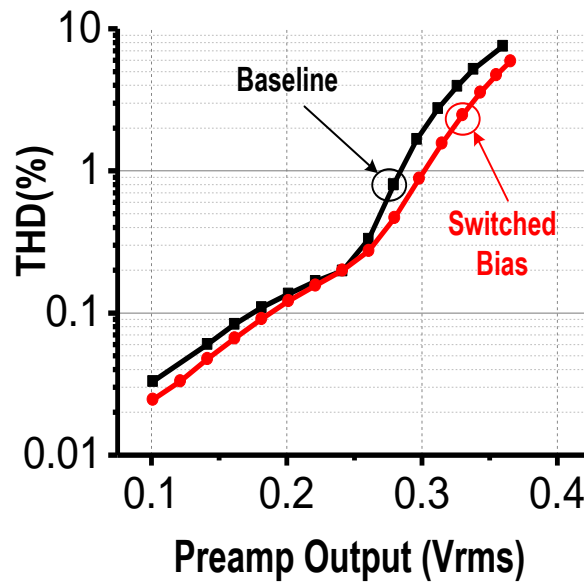
Figure 5.9. THD across preamp output amplitude.

at different output amplitudes. The design exhibits 1% and 2% THD with 300mVrms output magnitude with and without the switched bias at 1kHz, respectively (Figure 5.9).

The preamp output noise spectrum is shown in Figure 5.10. Switched bias reduces the total noise power by 30%, and the A-weighted input referred noise is 6.3µVrms.
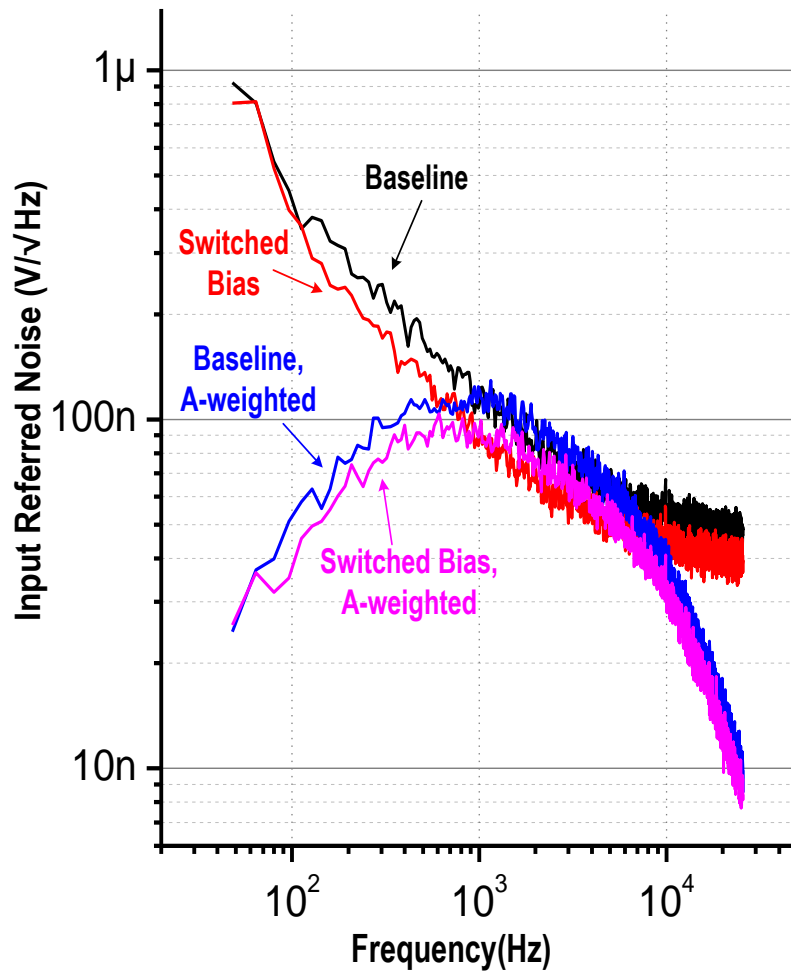
Figure 5.10. Preamp noise spectrum with and without switched bias
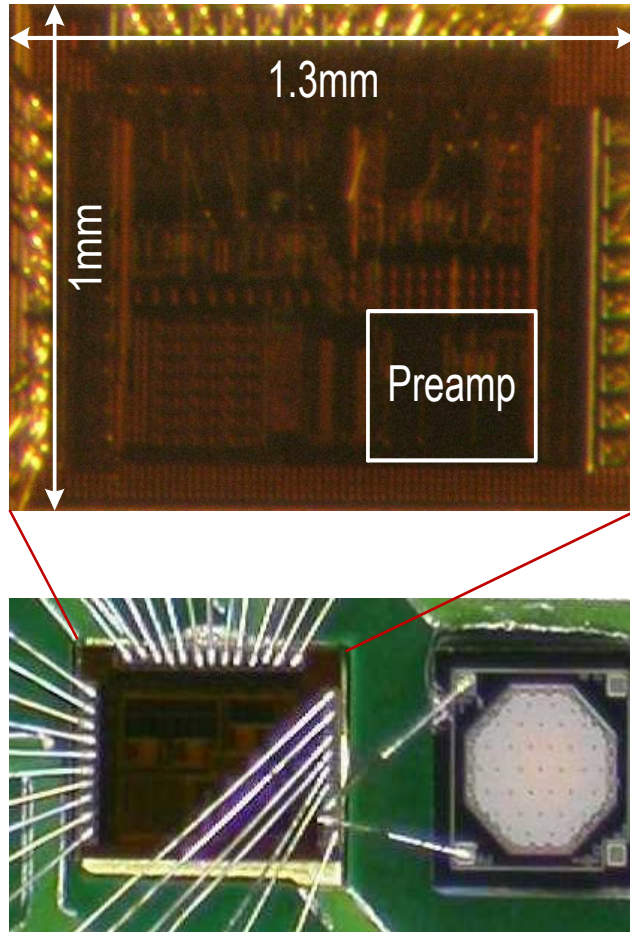
Figure 5.11. Die photo (top) and test module with a MEMS microphone (lid is not shown)

(bottom).

The preamp has an active area of $0.07mm^2$ and is integrated in a chip on board (COB) with a MEMS microphone (Figure 5.11). The microphone is tested in an anechoic chamber. A speaker converts an electrical audio signal, generated by a function generator and audio amplifier, into a corresponding sound (Figure 5.12). The sound pressure level is calibrated using a reference microphone, which is placed close to the test module.
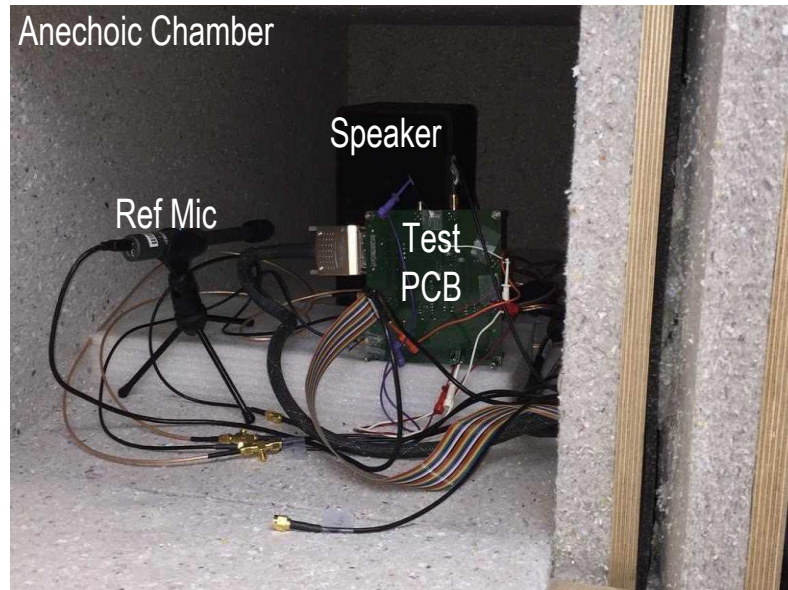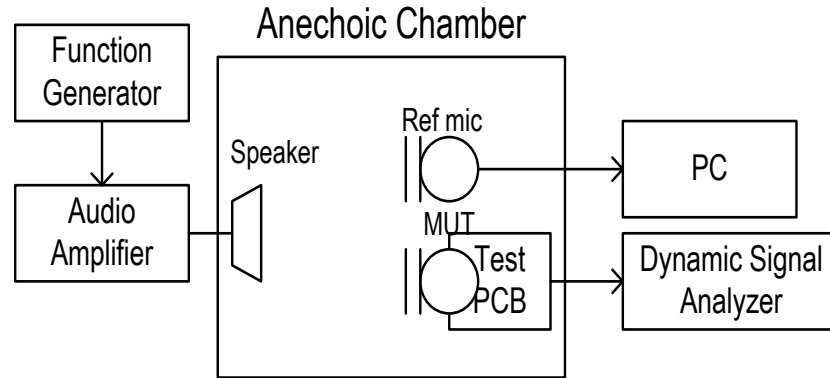
Figure 5.12. Microphone measurement setup.

Figure 5.13 shows THD measurement across sound pressure. It records 0.6% at 94dBA SPL and 5% at 113dBA SPL. Microphone SNR and sensitivity are 61.8 dBA and -29.5dBV with 94dBA SPL input at 1kHz, respectively. Table 5.1 summarizes the microphone and preamp performance and compares with prior works in this area. NEF is defined as $V_{rms,A} \sqrt{\frac{2I}{\pi V_T \times 4kT \times BW_{20K}}}$; BW_{20K} is 20kHz and $V_{rms,A}$ is A-weighted preamp noise. Among those listed, the proposed work achieves the best-reported NEF by 3x.
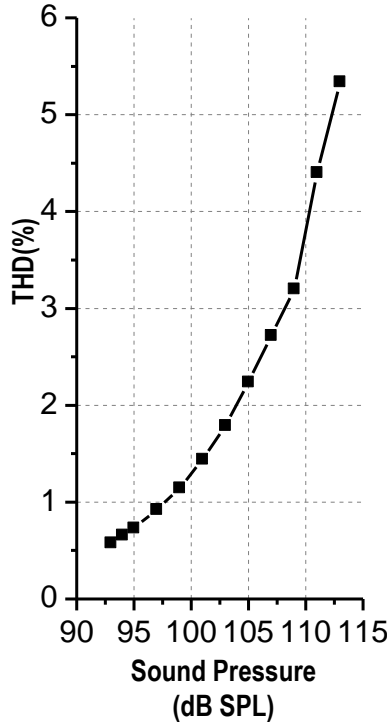
Figure 5.13. THD with different SPL at 11V V_B and 1kHz.

Table 5.1. Performance summary and comparison with recent works.

Parameters	This Work	ESSCIRC 2009 [67]	ISSCC 2013 [12]	ISSCC 2009 [69]
Technology (nm)	180	350	160	180
VDD (V)	1.4	1.8	5	1.8
Preamp Current (µA)	7.6	50	500	120
Power (µW)	10.6	90	2500	216
Preamp Noise (µVrms, A-weighed)	6.3	25	N/A	5
Preamp Gain (dB)	9.6	8.0	N/A	8.5
Preamp NEF	4.7	48.2	N/A	14.9
Active Area(mm2)	0.07	0.9	0.25	2.98
SNR (dBA @1Pa)	61.8	27	58	62.5
Sensitivity (dBV @1Pa, 1kHz)	-29.5	-48	-35.1	-33
THD (% @dB SPL, 1kHz)	0.6 @94	0.2 @120	0.5 @94	0.4 @104

5.6 Conclusions

This chapter proposed a low- 1/f noise switched-bias preamplifier for a MEMS microphone. The preamplifier utilizes switched MOSFET to reduce 1/f noise inherently. By alternatively using the two paths, 1/f noise is reduced by 30%. The preamp achieves 6.3μVrms input referred noise (A-weighted) with 7.6μA, improving the best-reported NEF by 3x. Acoustic test with the ASIC and MEMS sensor shows 61.8dBA SNR at 94dB SPL.

CHAPTER 6

Conclusions

6.1 Summary of Contributions

Continuous efforts to obtain small form factor computing devices have enabled a recent IoT wave. Recent IoT systems largely rely on sensor technologies that allow all the smart devices to interact with environmental signals. Because they should have low noise and often need an always-on operation, low-power sensor interface circuit designs are critical in the system.

This dissertation has addressed the noise and energy issues within the sensor interface circuits for a MEMS capacitive pressure sensor, infrared thermopile, and capacitive microphone. The key contributions of this dissertation are summarized as follows:

Chapter 2 discussed a dual slope CDC for implantable devices. By removing charges relevant to the base capacitance using the configurable capacitor bank, the CDC zooms in capacitance conversion range and reduces conversion time and energy. We use dual-precision comparators and achieved high resolution of the fine comparator and low energy of the coarse comparator. We demonstrated CDC that is integrated in a complete pressure sensing system composed of multiple IC layers including a MEMS pressure sensor, battery, processor, memory, and radio.

Chapter 3 improved the CDC design with a zoom-in incremental delta-sigma conversion to further enhance resolution and energy efficiency. It uses 9b SAR conversion to zoom in

capacitance variable input range in advance of delta-sigma conversion. Since we leveraged the unique structure of the CDC and by-pass the OTA in the SAR phase, the zoom-in architecture significantly reduced conversion energy as well as an oversampling ratio and conversion time. We also showed 9b DEM with the new matrix based unit-cap structure successfully suppressed linearity errors.

Chapter 4 discussed an infrared gesture recognition system suitable for smart devices using a thermopile array. The thermopile-based gesture recognition system is light insensitive and requires no excitation sources. The proposed ICA provided the adjustable gain and removed flicker noise, which is a dominant noise source of a low bandwidth application. It uses lower current to reduce standby power when the system is in the idle mode. To achieve 30Hz bandwidth, the LPF use pseudo-resistor based source degeneration and gm division techniques. We demonstrated the full system; it is the first SoC for gesture sensing applications using a thermopile array.

Chapter 5 discussed a switched-bias preamplifier for a MEMS capacitive microphone. We achieved 1/f noise reduction by using the switched bias amplifier for capacitive sensor interface circuits where the conventional chopping technique is ineffective. Moreover, high sensitivity and linearity were achieved with the AC coupling capacitor by separating two voltage biases for the MEMS microphone and the amplifier.

6.2 Future Works

An architecture of interface circuits is chosen by based on sensor output characteristics such as capacitance, resistance, and diode. Therefore the aforementioned circuit techniques can be readily employed to other sensing applications such as inertia, chemical, humidity, and touch sensors which have similar output characteristics. Moreover, there are other possibilities to further

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improve the proposed circuits. Although the circuits achieved high energy efficiency with low noise, the circuits can be optimized for different aspects. In addition, there are system integration opportunities that actually make the proposed circuits more useful in real life.

The line sensitivity of the dual-slope CDC system can be significantly improved with a linear regulator. Since the current mirror used in the CDC does not provide power supply rejection, supply noise and ripples generated from the switching regulator and digital circuits in the system are reflected in the CDC output codes. We used 32 times more conversion time and energy than we intended for system testing. A linear regulator can reject most of the power supply ripples and increase the energy efficiency of the system.

The zoom-in incremental CDC design can be enhanced with the following techniques. A fully differential structure with a dummy capacitor input can be considered to reduce supply sensitivity. With gain enhanced amplifiers, it would achieve finer capacitance resolution.

A problem with the proposed IR gesture recognition system is a large volume. We used two 16×2 thermopile arrays and each with its own IR lens. The thermopile arrays and ASIC were packaged separately on the PGAs and connected on a PC board. If it uses a single array and vertical integration using such as through-silicon vias, we can directly connect each pixel in the thermopile with the AFE. By doing so, we can tightly integrate more pixels in a smaller form factor, such as a few millimeters. In addition, each pixel size can be scaled down to integrate more pixels and increase resolution. ICA and LPF size can be scaled down with the following techniques: Setting a high chopper frequency allows for a higher noise corner frequency, allowing smaller input transistors and feedback capacitors to be used while maintaining noise efficiency in the ICA. The LPFs can be separated into an analog LPF with smaller capacitors that only eliminates chopper tones and a digital LPF that set the bandwidth to increase SNR.

Finally, the microphone preamplifier design is planned to be integrated into a voice recognition system composed of an audio AFE, audio DSP, processor, memory, RF, and battery. The system power budget is $<10\mu W$, and hence the audio AFE power should not exceed a couple μW. With this condition, we cannot use a conventional preamplifier with a buffer stage consuming tens of μW. Therefore, the proposed preamplifier that has addressed 1/f noise by 30% and provided $3\times$ better noise efficiency compared with the prior works will play an important role in implementing the ultra-low power audio system.

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