Ultra-low Power Circuits for Internet of Things (IOT)

by

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CHAPTER 1

Introduction

Miniaturized sensor nodes offer an unprecedented opportunity for the semiconductor industry which led to a rapid development of the application space: the Internet of Things (IoT). IoT is a global infrastructure that interconnects physical and virtual things (computing devices, mechanical and digital machines, objects, animals or people) that are provided with unique identifiers (e.g. IP) and the ability to transfer data over a network without requiring human-to-human or human-to-computer interaction [1]. IoT have the potential to dramatically improve people's daily lives. One of key aspect that makes IoT special is that the internet is expanding into places that has been ever reachable. Patients are ingesting Internet devices into their own bodies to help doctors diagnose and determine the causes of certain diseases [2]. Extremely small sensors can be placed on plants, animals, and geologic features, and connected to the Internet. Several challenges, however, exist that could possibly slow the development of IoT.

To fully utilize the potential of IoT devices, it should be best to realize them in a very small form factors. They should be also self-sustaining as there will be billions of devices deployed across the application area and thus it would be almost impossible to give an external support to every one of the devices. This necessitates the use of battery as a power source. Ideally, the form factor of the battery should be similar to the sensor size (1 to 10mm^3). Figure 1.1 shows different type of batteries with their sizes in scale and their life time depending on the system power budget. Compared to standard alkaline AA or 20mm Li coin battery, a Li-thin film battery in sub-mm^3 scale creates harsh limits on system power consumption due to limited battery capacity. While a system with $>100\mu$W power budget can run continuously for a year from conventional alkaline

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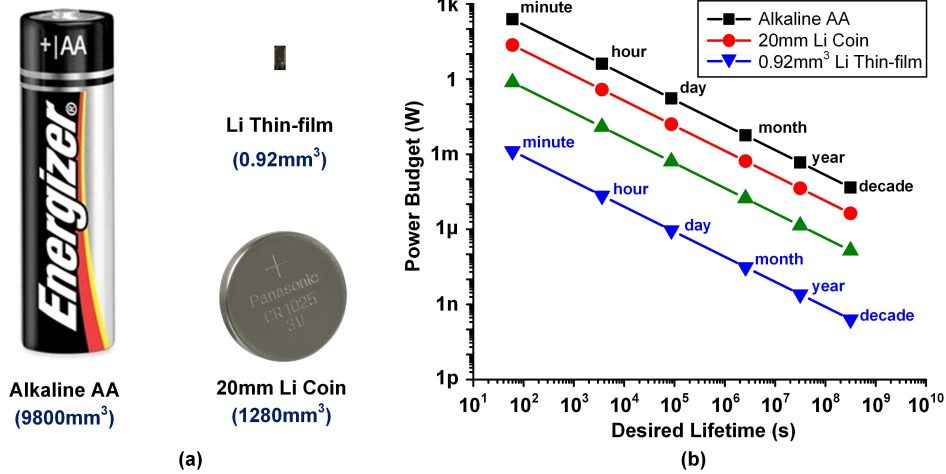
Figure 1.1: (a) Different type of batteries with various size and (b) their life time based on system power budget.

AA and 20mm Li coin batteries, <5nW of power budget is required for the same lifetime when 0.9mm^3 Li thin-film battery is used [3].

Therefore, miniaturized IoT devices should consume low power as possible to extend their life time. It is also important to note that internal resistance of the battery increases to 10s of kΩ as their size gets smaller. Regarding this point, low power consumption also helps to fully utilize the battery capacity by reducing IR drop, preventing battery voltage reaching a cut-off voltage too early. Another way to resolve the limited power budget is operating the system with low duty cycles. For example, as radio transmission typically consumes large power ($\geq$ 100s of μW), the system often operates with heavy duty-cycles to reduce their average power. The ratio of the duty cycle should be adjusted depending on the target application as well as available energy budget. Therefore, IoT devices should have their own reference clock that enables scheduling. The clock reference must exhibit very low power consumption as they represent one of the few components that must remain on during standby mode, while maintain its accuracy.

In this proposal, we describe several circuit techniques as well as system level optimization to meet the challenging energy requirement for the IoT design space.

In Chapter 2, a fully-integrated temperature sensor for battery-operated, ultra-low power microsystems is proposed. Sensor operation is based on temperature independent/dependent current sources that are used with oscillators and counters to generate a digital temperature code. A conventional approach to generate these currents is to drop a temperature sensitive voltage across a

resistor. Since a large resistance is required to achieve nWs of power consumption with typical voltage levels (100s of mV to 1V), we introduce a new sensing element that outputs only 75mV to save both power and area. The sensor is implemented in 0.18μm CMOS and occupies 0.09mm^2 while consuming 71nW. After 2-point calibration, an inaccuracy of +1.5°C /-1.4°C is achieved across 0°C to 100°C. With a conversion time of 30ms, 0.3°C (rms) resolution is achieved. The sensor does not require any external references and consumes 2.2nJ per conversion. The sensor is integrated into a wireless sensor node to demonstrate its operation at a system level.

In Chapter 3, an ultra-low power oscillator designed for wake-up timers in compact wireless sensors is proposed. In a conventional relaxation oscillator, a capacitor periodically resets to a fixed voltage using a continuous comparator, thereby generating an output clock. The reset is triggered by a continuous comparator and thus the clock period is dependent on the delay of the continuous comparator which therefore needs to be fast compared to the period, making this approach power hungry. To avoid the power penalty of a fast continuous comparator, a constant charge subtraction scheme is proposed. As a constant amount of charge is subtracted for each cycle, rather than discharging/charging the capacitor to a fixed voltage, the clock period becomes independent of comparator delay. Therefore, the high power continuous comparator can be replaced with a coarse clocked comparator, facilitating low power time tracking. For precise wake-up signal generation, an accurate continuous comparator is only enabled for one clock period at the end of the specified wakeup time. A wake-up timer using the proposed scheme is fabricated in a 0.18μm CMOS process. The timer consumes 5.8nW at room temperature with temperature stability of 45ppm/°C (-10°C to 90°C) and line sensitivity of 1%/V (1.2V to 2.2V).

In Chapter 4, an 8-bit sub-ranging SAR ADC is proposed that is designed for bursty signals having long time periods with small code spread. A modified capacitive-DAC (CDAC) saves previous samples MSB voltage and reuses it throughout subsequent conversions. This prevents unnecessary switching of large MSB capacitors as well as conversion cycles, reducing energy consumed in the comparator and digital logic and yielding total energy savings of 2.6×. In 0.18μm CMOS, the ADC consumes 120nW at 0.6V and 100kS/s with 46.9dB SNDR.

In Chapter 5, an ultra-low power acoustic sensing microsystem is proposed that is based on active circuits. Several low power techniques are proposed to realize ultra-low power consumption while satisfying the performance specification. The proposed active audio amplifier, for example,

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has been designed with an unconventionally low bias current (≤4nA). The proposed ULP 8-bit SAR-ADC has a unique topology that allows extremely small (≤50fF) input capacitance, which is crucial to achieve a large gain from the preceding amplifier. Based on observations that the targeted audio signal features are mainly concentrated within a relatively narrow bandwidth, we set the bandwidth of all active components to be ≤ 0.5 kHz, and operate the ADC / digital signal processing at a ≤1kHz rate. This low frequency operation is one of the key enabling factors that allows continuous (without duty-cycling) sensing with ultra-low power consumption. The proposed system consumes 12nW while showing >95% of detection accuracy.

Finally in Chapter 6, we conclude this dissertation with a discussion of the proposed works with their their key contributions being summarized. Suggestion for the future work will be made as well to provide possible opportunities.

CHAPTER 2

A Fully-Integrated 71nW CMOS Temperature Sensor for Low Power Wireless Sensor Nodes

2.1 Introduction

Ultra-low power wireless microsystems are emerging as a new class of computing. These systems can be used in a wide range of application areas such as medical, surveillance, and environmental monitoring by equipping them with the appropriate sensors [4–6]. Among various sensor modalities, temperature is one of the most common and therefore low-power temperature sensors become an important design element of such microsystems.

The design of a temperature sensor for these miniaturized wireless microsystems poses several challenges, with many of the limitations arising due to a limited battery size and correspondingly small energy capacity. While average power consumption is critical as a result, the large internal resistance of the battery also limits the maximum instantaneous current that can be drawn from the battery. For example, the targeted thin-film Li battery has a limited maximum current draw of less than $20\mu A$ [3]. Given that the temperature sensor power is only one component of total system power, this limitation is a major bottleneck. Further, the sensor should be fully-integrated and self-contained since accurate external references are not readily available in highly integrated microsystems.

Various types of temperature sensors have been designed in CMOS technology. Most conventional temperature sensors are based on bipolar junction transistors (BJTs). These sensors measure

temperature by comparing a temperature-dependent voltage to a temperature-insensitive voltage. These two voltages are developed using two well-defined temperature characteristics of a vertical PNP transistor; 1) the complementary-to-absolute temperature (CTAT) characteristic of the base-emitter voltage (V_{BE}) and 2) the proportional-to-absolute temperature (PTAT) characteristic of the difference between two base-emitter voltages (ΔV_{BE}). The ratio between the PTAT and reference voltages is fed to an analog-to-digital converter (ADC) to be digitized. With the choice of precision $\Sigma \Delta$-ADCs, these sensors offer high resolution, up to 0.002°C [7–9]. Sensing error in BJT-based sensors mainly arises due to process variation of the saturation current (I_S) [10]. This error can be reduced to less than ±0.2°C after 1-point calibration. One example state-of-the-art temperature sensor achieves 0.02°C resolution with inaccuracy of ±0.15°C by combining two-step zoom ADC, chopping and dynamic element matching (DEM) [11]. However, such sensors show power consumption in μW range, making them unsuitable for miniaturized battery-powered applications.

As a result, MOSFET-based temperature sensors targeted for wireless system have been introduced. For low power operation, time-to-digital [12,13] or frequency-to-digital conversion [14,15] is used instead of ADCs. Temperature can be calculated using a reference clock and a temperature-dependent frequency or pulse. These sensors consume less power than BJT-based sensors at the expense of resolution and accuracy. While power consumption is reduced to hundreds of nW, an external clock is needed as a reference. The performance of these sensors highly depends on the accuracy of the reference clock, which is not typically available in a wireless microsystem. Moreover, the reference clock itself can increase power consumption significantly. On the other hand, a temperature sensor that uses an on-chip time reference while consuming sub-μW has been reported [16]. However, it exhibits larger inaccuracy compared to others due to the non-ideal characteristics of the reference clock. Recently, a temperature sensor based on dynamic threshold MOSTs (DT-MOSTs) is introduced [17]. The sensor achieves high resolution (0.063°C) and accuracy (±0.4°C) after single point trimming, but with sub-μW of power consumption (excluding clock generation power).

This work proposes a new temperature sensor topology that improves temperature inaccuracy while consuming very low power and energy. A novel MOSFET-based sensing element is introduced to translate external temperature into a voltage with pWs of power consumption. Furthermore, conventional voltage-to-current converter and current mirror structures are modified to

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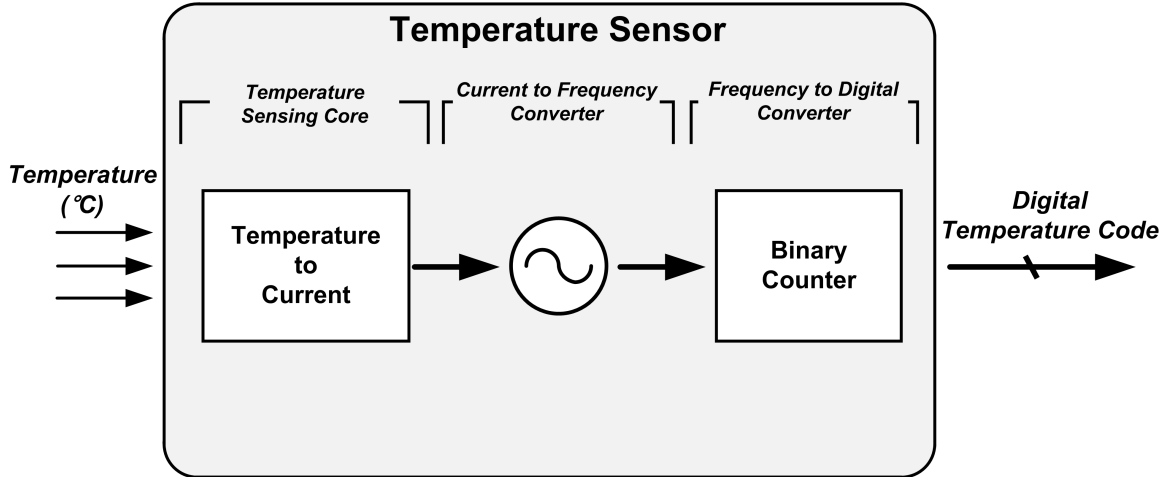
Figure 2.1: Simplified block diagram of a proposed temperature sensor.

reduce the required current consumption by half. With these techniques, the sensor consumes 71nW of power and dissipates 2.2nJ of energy per conversion with inaccuracy of $\pm 1.5°C$ /-$1.4°C$ and resolution of $0.3°C_{rms}$ from 0 to $100°C$ temperature range.

2.2 Temperature Sensor Design and Analysis

Figure 2.1 shows a block diagram of the proposed temperature sensor. The structure has three major components: 1) a temperature sensing core, 2) a current to frequency converter, and 3) a frequency to digital converter. The temperature sensing core converts temperature into a current. An oscillator is then used to convert this current into a frequency. Finally, a binary counter translates frequency into a digital output code. For temperature sensors that use a similar scheme, the total power consumption is dominated by the magnitude of current generated in the sensing core. This is because the generated current determines oscillator frequency, which directly relates to the counter dynamic power consumption. Therefore, generating a small current with well-defined temperature dependency is crucial to designing a low-power temperature sensor.

2.2.1 Temperature Sensing Element

Figure 2.2 shows a conventional approach for generating a temperature-dependent current through a resistor (I_R) using a voltage source (V_{source}). In this structure, the output of a voltage

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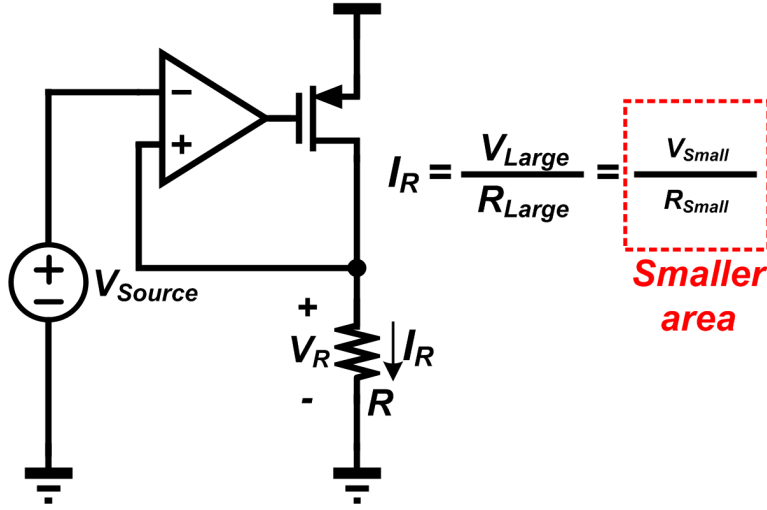
Figure 2.2: Conventional voltage-to-current converter.

source is copied across a resistor to generate a current. With this approach, either a very large resistor or very small voltage is required to achieve low power consumption. Using a typical bandgap voltage reference of $\sim$1V, a resistance of $>$20MΩ is required to achieve sub-100nW power consumption, which is impractical in area-constrained microsystems. To achieve nW range power consumption without incurring a large area penalty, V_R is reduced well below 100mV by introducing a new sensing element (Figure 2.3, right). The sensing element generates a linearly increasing output voltage with temperature while drawing only pA. A key component of the sensing element is based on a 2-Transistor (2T) voltage reference (Figure 2.3, left) [18].

A prior implementation of the 2T voltage reference uses two different types of transistors (with highly disparate threshold voltages) to 1) increase the reference voltage as much as possible ($>$300mV) and 2) compensate output voltage temperature dependence. By equating currents through M_1 and M_2, an analytical solution for the output voltage ($V_{Reference}$) can be obtained as

$$V_{Reference} = \frac{m_1 m_2}{m_1 + m_2}(V_{th2} - V_{th1}) + \frac{m_1 m_2}{m_1 + m_2}V_T ln(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1}). \qquad (2.1)$$

where V_{th} is the threshold voltage, $V_T = kT/q$ is the thermal voltage, m is the subthreshold swing coefficient, μ is mobility, and C_{ox} is gate oxide capacitance of the transistor [18]. From (2.1), it can be seen that compensation is achieved by combining the CTAT characteristic of the threshold voltage and PTAT characteristic of the thermal voltage. The reference output voltage can also be made PTAT or CTAT with proper sizing, which can be used to sense temperature. However,

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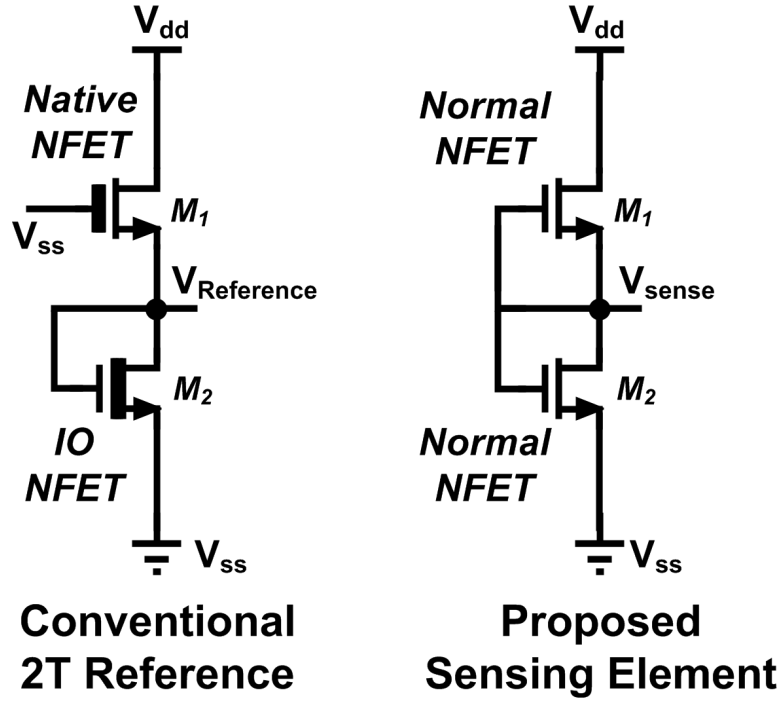
Figure 2.3: Circuit diagram of a conventional 2T reference [18] and proposed sensing unit.

a high reference voltage increases power consumption. Furthermore, the use of different threshold transistors causes its output voltage to vary widely across process, resulting in degraded linearity and sensing error.

We therefore propose to use the same type of transistors for both devices in the 2T reference to eliminate the threshold voltage dependence in (1). The output voltage of the sensing element can be modeled using a subthreshold current equation that considers the body effect and DIBL [19] as follows:

$$I = \mu_0 C_{ox} \frac{W}{L} V_T^2 e^{1.8} e^{\frac{-\Delta V_{th}}{\eta V_T}} e^{(V_{gs} - V_{th} - \gamma' V_{sb} + \eta V_{ds})/mV_T} \left(1 - e^{-V_{ds}/V_T}\right) \tag{2.2}$$

where μ_0 is zero bias mobility, V_{th0} is zero bias threshold voltage, γ' is linearized body coefficient , η is the DIBL coefficient, and ΔV_{th} is a term introduced to account for transistor-to-transistor leakage variations. Assuming an output voltage greater than $3V_T$ ($\sim$75mV), subthreshold current becomes independent of drain to source voltage (V_{ds}). Also, DIBL becomes negligible due to the use of long channel devices.

Therefore, current through each transistor M_1 and M_2 can be expressed as (2.4) and (2.4). The

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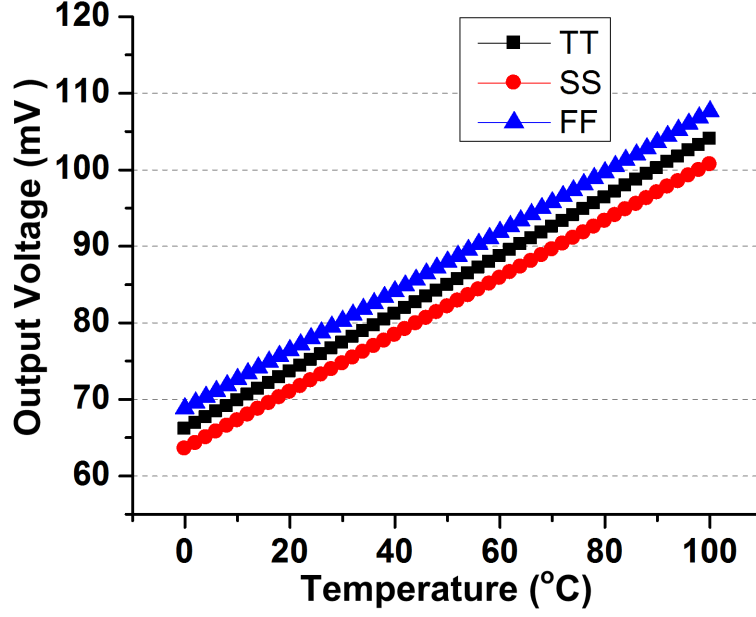
Figure 2.4: Simulated output voltage of proposed sensing element.

resulting output voltage can be found as (2.5) by equating I_1 and I_2, and V_{th1} and V_{th2}.

$$I_1 = \mu_1 C_{ox1} \frac{W_1}{L_1} V_T^2 e^{1.8} e^{\frac{-\Delta V_{th1}}{\eta V_T}} e^{(0-V_{th1}-\gamma_1' V_{sense})/m_1 V_T}. \tag{2.3}$$

$$I_2 = \mu_2 C_{ox2} \frac{W_2}{L_2} V_T^2 e^{1.8} e^{\frac{-\Delta V_{th2}}{\eta V_T}} e^{(V_{sense}-V_{th2}-\gamma_2' 0)/m_2 V_T}. \tag{2.4}$$

$$V_{sense} = \frac{m_1 m_2}{m_1 + \gamma_1' m_2} V_T ln(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_o x2 W_2 L_1}). \tag{2.5}$$

It can be seen that threshold voltage is eliminated and mobility is cancelled out. By eliminating these process/temperature dependent terms, low variability is achieved. As a result, the output voltage shows PTAT behavior with good linearity due to the thermal voltage V_T. Also, compared to the conventional structure, higher temperature sensitivity is achieved by connecting the gate of top transistor (M_1) to the output ($m_2 > \frac{m_1 m_2}{m_1 + m_2}$, when $\gamma = 0$). Figure 2.4 shows simulation results of this 2T sensing element at different corners. The minimum R^2 correlation of the output voltage is 0.99995, observed at the fast corner. The sensing element output voltage is also greatly reduced by removing the threshold voltage term. Additionally, devices are sized with similar gate lengths to avoid threshold voltage discrepancies due to reverse short channel effect. The sensing element

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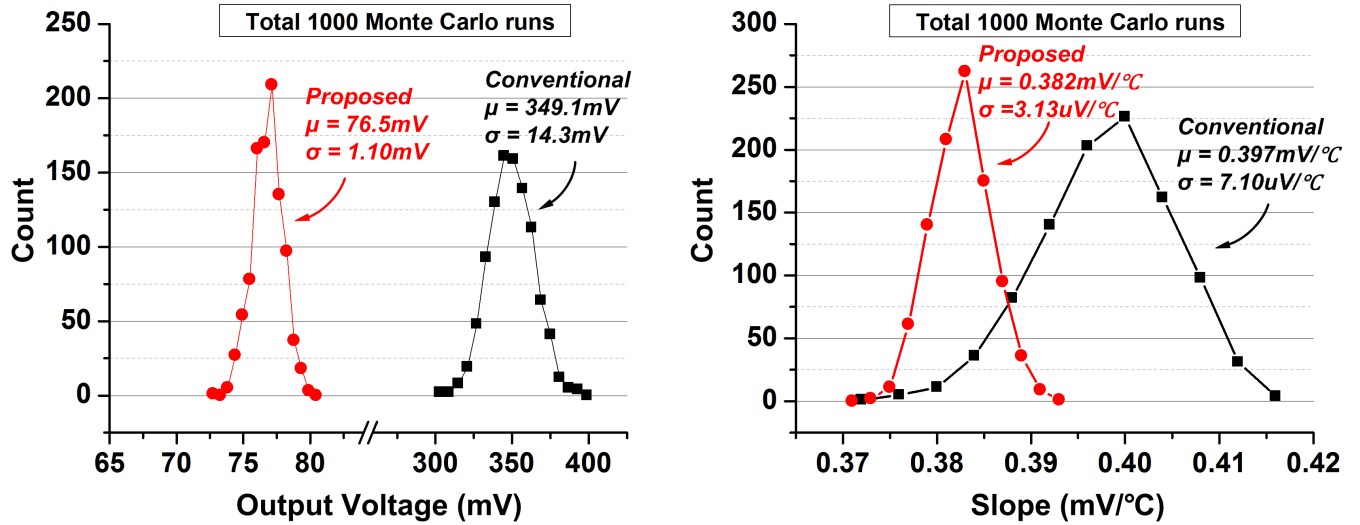
Figure 2.5: Simulated output voltage and slope distribution of conventional 2T and proposed structure.

consumes 8pW at room temperature and shows a supply dependency of 1.814%/V from 1.0V to 1.4V in simulation.

Figure 2.5 compares a conventional 2T structure with the proposed structure. Conventional 2T is sized to match the slope of sensing element in the typical corner. Monte Carlo simulations show that the proposed structure has 5 lower output voltage, enabling a 5× reduction in resistor area for equivalent current. Also, the proposed topology exhibits 2.8× lower output voltage variation (σ/μ) and 2.2× less variation in slope (temperature coefficient or TC variation). Output voltage process dependency and TC variation are important factors since they directly impact the temperature characteristics of the generated current.

2.2.2 Current Generation

For current generation, we first begin with a conventional structure shown in Figure 2.6, (a). In this structure, the sensing element drives a conventional voltage to current converter to generate currents. A negative feedback loop consisting of an amplifier, transistor, and resistor duplicates the sensing elements output voltage across the resistor. The amplifier operates in the subthreshold region to achieve power savings. Using a 2-stage topology, the amplifier shows 105dB open-loop gain and 136pW of power consumption at room temperature (simulated results). The high gain of the amplifier ensures that V_R tracks V_{sense}. Due to the negligible power consumption of the

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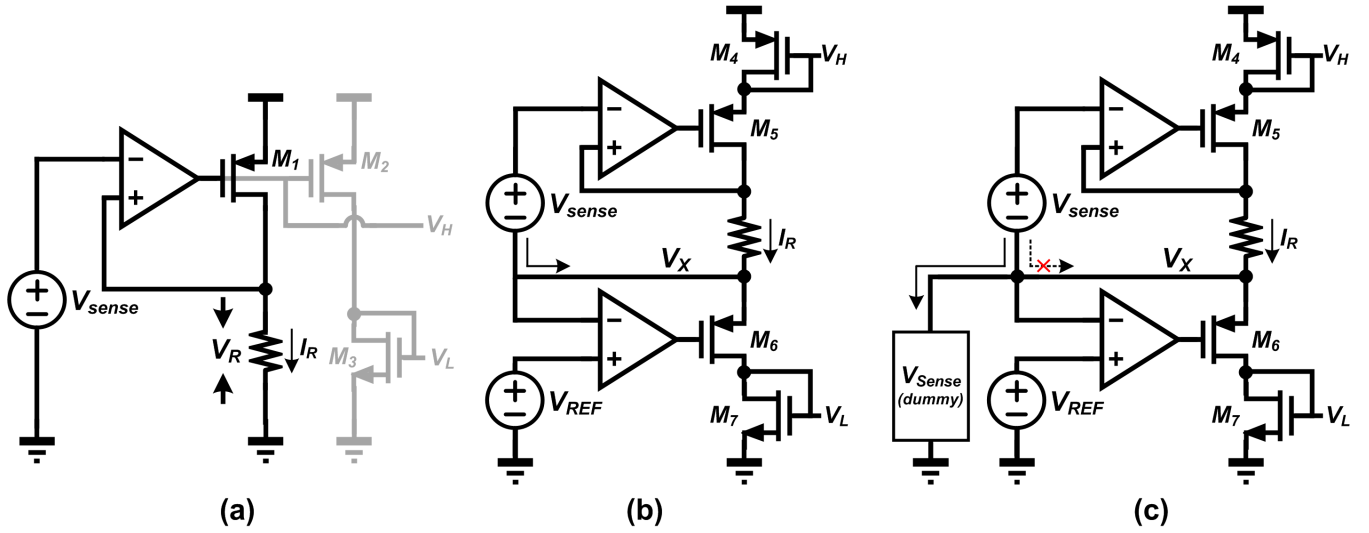
Figure 2.6: Circuit diagram for (a) conventional scheme for current generation with a voltage source, (b) modified structure for low-power operation, and (c) additional current path added for error reduction.

sensing element and amplifier, temperature sensing core power is dominated by I_R (nA range). Conventionally, a current mirror (M_{1-2}) is required to provide control voltages (V_H and V_L) for the subsequent ring oscillators; however, 50% power savings can be achieved by avoiding such a current mirror.

Thus, we introduce a second feedback loop along with a reference generator (V_{REF}) to remove the current mirror (Figure 2.6, (b)). The additional feedback loop allows for the inclusion of a diode-connected transistor M_7 at the bottom of the stack. This structure ensures M_7 is saturated; otherwise, it becomes cutoff due to the sub-100mV output voltage from the sensing element. As a result, V_H and V_L are generated directly from I_R without an additional mirror. The control voltages are generated from M_4 and M_7 rather than from M_5 and M_6 to avoid large loading on the op-amp outputs. This enhances bandwidth and phase margin of the op-amps, and also relaxes the output swing by biasing the output away from the supply rails. The reference generator is made with diode-connected PMOS transistors. It draws 240pA and outputs an intermediate voltage between supply and ground. This structure also helps to obtain an effective common-mode voltage of the amplifier by boosting the sensing elements output voltage by VDD/2. Meanwhile, the voltage dropped across the resistor is maintained, helping to protect I_R against supply variation regardless of the reference generator, which has poor supply regulation. Simulated line sensitivity shows that

Reference Current Generator

PTAT Current Generator

Sensing Element

$V_{sense}+V_X$

M_P

V_H

Reference generator

V_{REF}

Voltage Across Resistor is Limited to Sub 0.1V

I_R

$V_R = V_{sense}$

R

V_X

Second feedback loop

M_n

V_L

Dummy Unit for leakage path

	Sensing Element	
	PTAT	**Reference**
W_{top}/L_{top}	35/10	20/7
W_{bot}/L_{bot}	1/10	40/3
R	7MΩ	2.5MΩ

Unit: µm

2stage op-amp

V-   V+   OUT

BIAS
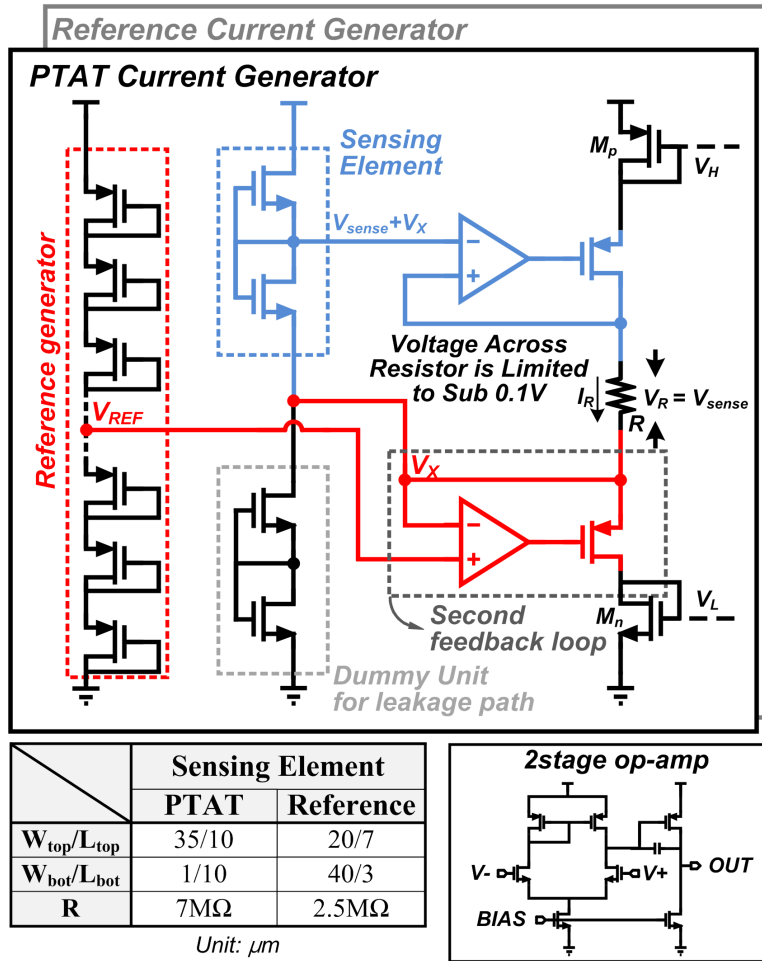
Figure 2.7: Detailed schematic of temperature sensing core.

current changes by 0.974%/V in the 1.0–1.4V range.

However, by connecting the sensing elements ground to V_x, the current flowing through the sensing element moves along the path and is added to I_R. This causes a discrepancy between top and bottom current of the diode-connected devices, which creates error in subsequent stages. To eliminate this problem, a duplicate sensing element that serves as a dummy structure is connected between V_x and ground (Figure 2.6, (c)). Since each element operates over the same voltage range (VDD/2), current flowing through the main sensing element is identical to current through the dummy sensing element. As a result, the dummy sensing element functions as a leakage path for the main sensing element, suppressing unwanted current in the main current generation path.

Figure 2.7 shows the detailed schematic of the temperature sensing core. A temperature insensitive reference current (I_{REF}) and temperature sensitive PTAT current (I_{PTAT}) are generated

from two sets of the previously described structure. Each current is generated using different types of resistors along with different sensing elements. Proper resistor choice for these currents is performed by first characterizing V_{sense} and resistance (R) against temperature. Due to the linear temperature characteristic of the sensing element, only its first-order temperature dependency has been considered, while both first- and second- order dependencies have been considered in modeling resistance. Thus, V_{sense} and R can be expressed as follows:

$$V_{sense} = V_o(1 + \alpha_{V1}T). \tag{2.6}$$

$$R = R_o(1 + \alpha_{R1}T + \alpha_{R2}T^2). \tag{2.7}$$

As a result, the generated current I_R can be modeled by Equations (2.8)-(2.10).

$$I_R = \frac{V_{sense}}{R} = \frac{V_o(1 + \alpha_{V1}T)}{R_o(1 + \alpha_{R1}T + \alpha_{R2}T^2)} = \frac{V_o}{R_o}(1 + \alpha_{I1}T + \alpha_{I2}T^2) = I_0(1 + \alpha_{I1}T + \alpha_{I2}T^2). \tag{2.8}$$

$$\alpha_{I1} = \alpha_{V1} - \alpha_{R1}. \tag{2.9}$$

$$\alpha_{I2} = \alpha_{R1}^2 - \alpha_{R1}\alpha_{V1} - \alpha_{R2}. \tag{2.10}$$

Since the sensing element itself has a positive first order temperature coefficient (α_{V1}), a PTAT resistance that has a positive first order temperature coefficient (α_{R1}) is required to generate the I_{REF}. With proper sizing of the sensing element, α_{V1} can be matched to α_{R1} to set α_{I1} to zero. On the other hand, a resistor with a CTAT characteristic is desired for the temperature sensitive I_{PTAT} in order to increase the temperature dependency. Increased temperature dependency translates into a wider range of digital codes and hence finer resolution. In the chosen process, diffusion resistors and poly resistors meet the above requirements for I_{REF} and I_{PTAT}, respectively. Among diffusion resistors, n+ type is chosen to minimize the second order temperature coefficient α_{I2} due to its $1.8\times$ lower α_{R2} compared to p+ type. Resulting design parameters for the

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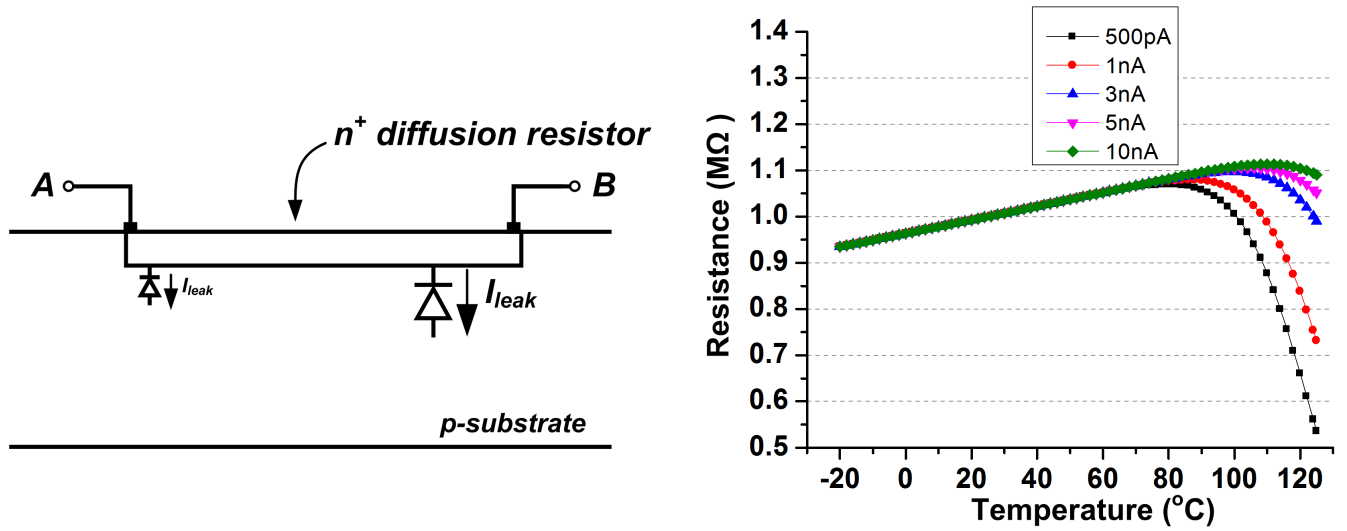
Figure 2.8: Structure of an n+ diffusion resistor (W=840nm, L=15.2mm) and simulated resistance across different amounts of bias current.

I_{REF} are α_{I2}=6.26×10^{-7}/°C^2 and α_{I1}=-7.61×10^{-5}/°C. Among poly resistors, p+ type results in a 1.1× better α_{I2} compared to p- type. However, p- type is chosen due to its area efficiency (3.1× less area for iso-resistance) and 1.2× higher α_{I1}. Resulting design parameters for the I_{PTAT} are α_{I2}=4.00×10^{-6}/°C^2 and α_{I1}=6.58×10^{-3}/°C.

In very low power applications, a diffusion resistor must be considered carefully due to its leakage. Figure 2.8 shows the structure of an n+ diffusion resistor. A reverse-biased junction diode is formed between n+ diffusion and p-substrate. As temperature increases, leakage current through this diode increases exponentially and cannot be neglected. When the lower end of the diffusion resistor is biased at 600mV, simulated results show that the linearity of the resistance is degraded when the amount of current flowing across a resistor decreases sufficiently towards the leakage current value. In this work, lower bound on reference current is set as 3nA in order to maintain low temperature sensitivity in the targeted temperature range of 0°C to 100°C.

Although the sensing element is carefully sized to match its first order temperature coefficient with the resistor, temperature dependency of the amplifier gain will cause a discrepancy between V_{sense} and V_R. To remove this problem, amplifier gain is designed to exceed 98dB across the targeted temperature range, which leads to TC variation below 0.01%. Another source of error comes from non-idealities due to process variation and mismatch. Process variation causes α_{R1} to vary while offset of the amplifier makes α_{V1} to deviate from a designed value. Also, mismatch

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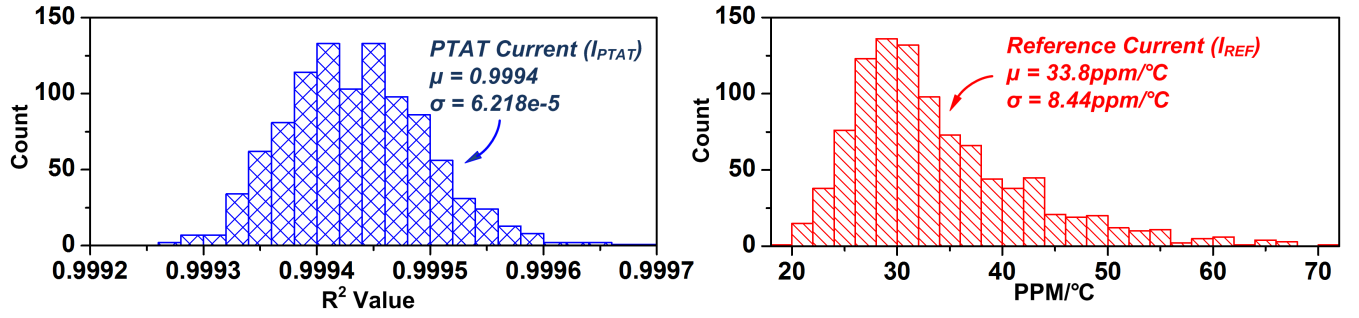
Figure 2.9: Effect of process variation and mismatch on PTAT linearity (top) and reference temperature coefficient (bottom).

between the main and dummy sensing element can result in an error in the generated currents. Among these factors, op-amp offset is the dominant source of error as it directly affects reference current stability ($\alpha_{I1} \neq 0$). PTAT current α_{I1} also deviates from its designed value but can be tolerated using 2-point calibration as its linearity is preserved. In contrast, error due to spread of α_{R1} is not critical as their values are nearly constant with process variation in simulation ($<0.25\%$ over 3σ corners). Sensing element mismatch is also negligible due to 1) large device sizes and 2) small current level compared to I_{PTAT} and I_{REF} ($<0.33\%$). To minimize these errors, large devices and wide resistor widths are used at the expense of area. Figure 2.9 shows the effects of process variation and mismatch on I_{PTAT} and I_{REF} from 1000 Monte Carlo simulations. The calculated resulting average error due to non-linearity is $0.3°C$ with 11% area overhead due to device and resistor sizing.

2.2.3 Ring oscillators

The voltage-controlled ring oscillator shown in Figure 2.10 is used to translate current into frequency. A single stage of an oscillator consists of an inverter followed by a transmission gate (TG). To reduce idle state power consumption, the first stage employs a NAND gate to prevent unnecessary oscillation. Oscillator frequencies are controlled by adjusting the resistance of transmission gates (R_{TG}) with voltages (V_H and V_L) from the previous stage. Using a simple RC model, the delay of each stage t_d can be expressed as [20],

$$g_M = \frac{C_G(1 + g_M R_{TG})}{g_M}.$$

(2.11)
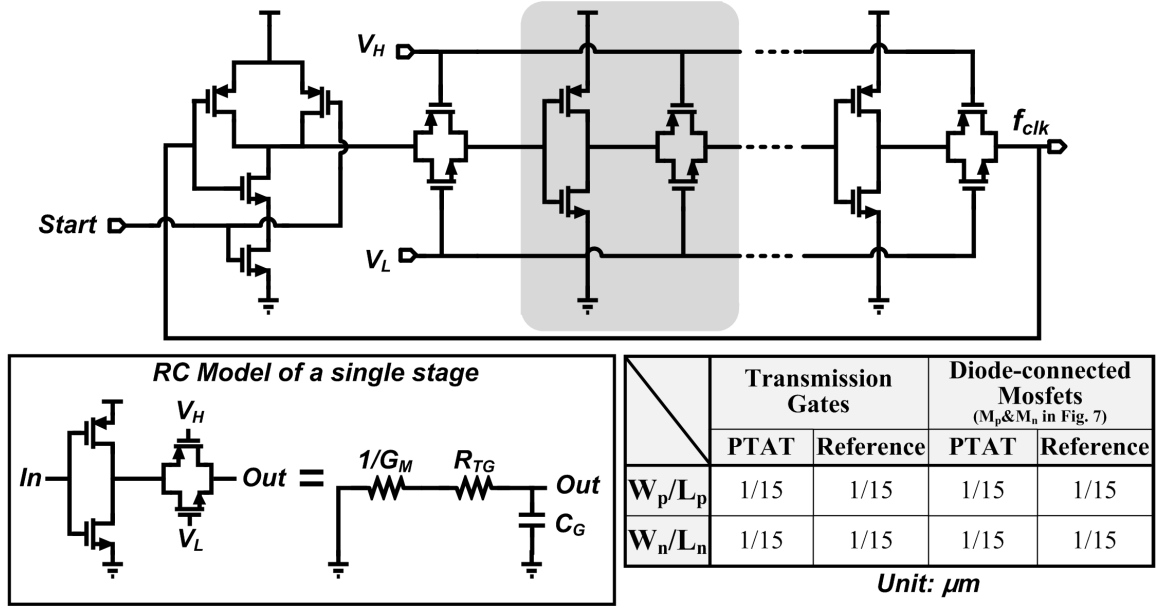
Figure 2.10: Circuit diagram of a voltage controlled ring oscillator.

where g_M is the transconductance of a single inverter and C_G is the total gate capacitance of a stage (including both NMOS and PMOS). It can be seen that for $g_M R_{TG} \gg 1$, each stage delay will be determined by R_{TG}, rendering inverter delay temperature dependence negligible. Effective resistance of R_{TG} is an average value of V_{TG}/I_{TG} during transition, where V_{TG} and I_{TG} are voltage and current across a transmission gate, respectively. Given a step response of a rising input and VDD/2 as a switching point, I_{TG} will remain same during transition as V_{ds} (=VDD/2) is kept above $3V_T$. In this case, effective resistance for a falling transition can be approximated as follows [21]:

$$R_{TG,effective} = \frac{ln2}{V_{DD}/2} \int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_{TG}} dV \approx \frac{V_{DD}}{2I_{TG}}. \tag{2.12}$$

Similar discussion also holds for a rising transition. From (2.11) and (2.12), the oscillation frequency f_{osc} of an N-stage oscillator can be expressed as:

$$f_{osc} = \frac{1}{2Nt_d} = \frac{g_M}{2NC_g g_M R_{TG}} \approx \frac{I_{TG}}{NC_g V_{DD}}, (g_M R_{TG} \gg 1). \tag{2.13}$$

Since I_{TG} tracks the current generated from the sensing core through V_H and V_L, frequency will be determined by I_{REF} and I_{PTAT}. As a result, the two ring oscillators generate a PTAT frequency (clk_{PTAT}) and reference frequency (clk_{REF}).
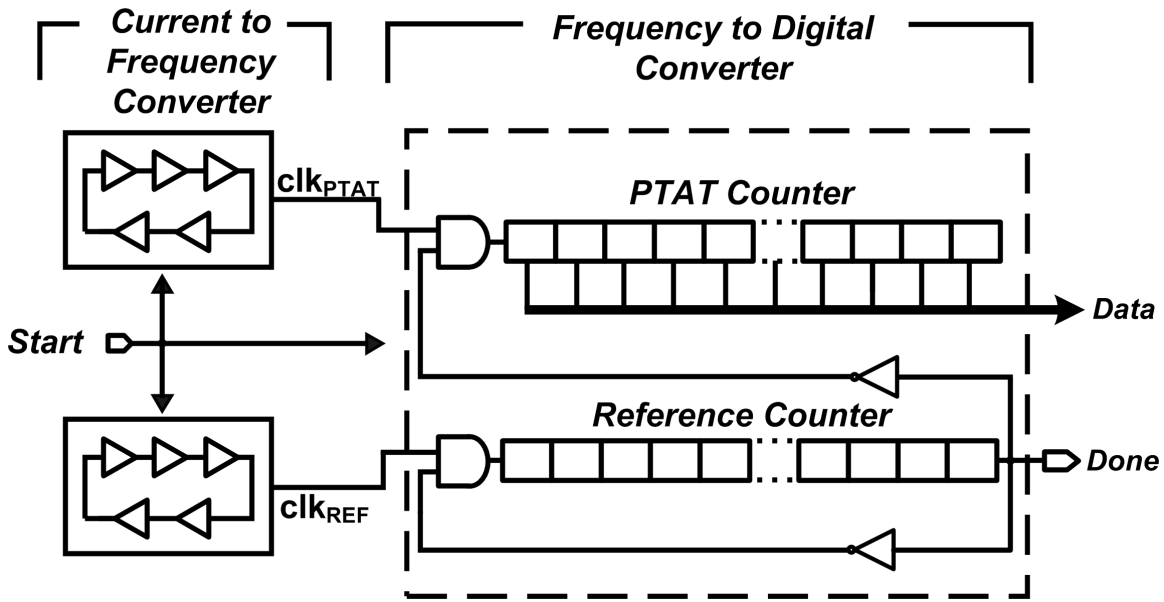
Figure 2.11: Monte Carlo simulation results of PTAT and reference frequency.

For the $g_M R_{TG} \gg 1$ condition, inverters are designed with large width devices for fast transitions while I/O devices are used to minimize short-circuit current. This also increases capacitance seen by the previous transmission gate and enhances the delay difference between inverter and transmission gate in each stage at the expense of power consumption. The inverter delay is set to be less than 5% of the total stage delay.

Although the temperature dependency of the frequency is controlled by the current from the sensing core, the frequency is sensitive to supply variation as shown in (2.13). Supply dependence of R_{TG} causes its value to increase as supply voltage increases, decreasing frequency. Since both clk_{PTAT} and clk_{REF} show the same behavior due to their identical structure, this effect is partially suppressed, however different bias condition leave some residual error. The simulated supply sensitivity is +1.7°C /-2.8°C across 1 to 1.4V range.

Process variation and mismatch make it difficult to accurately match the small current flowing through a resistor to a current flowing through transmission gates, degrading the temperature characteristics of the oscillator. Such degradation is especially critical for the reference frequency. While PTAT frequency maintains linearity despite slope changes, the temperature insensitivity of the reference frequency is not preserved with large mismatch and process variation. Digital output linearity is directly affected by this temperature dependency. Thus, careful layout of large devices

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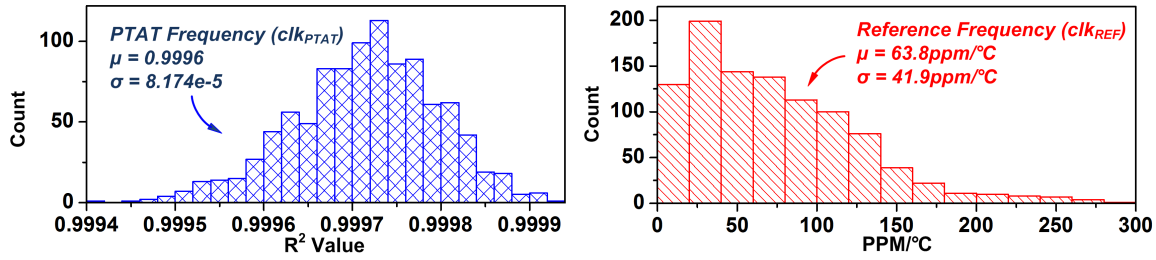
Figure 2.12: Block diagram of a frequency to digital converter.

is used to improve matching. Devices are sized with long lengths and small width to minimize kickback noise and V_{ds} mismatch due to DIBL. Figure 2.11 shows 1000 Monte Carlo simulations of the ring oscillators with the temperature sensing core. When compared with Monte Carlo current simulations, PTAT frequency linearity is preserved while the mean temperature sensitivity for the reference frequency worsens by $1.9\times$. Therefore, most error arises from reference current to frequency conversion while op-amp offset (mentioned in 2.2.2) becomes the next largest component.

2.2.4 Counters

Generated frequencies are converted into a digital output through asynchronous counters. Figure 2.12 shows the block diagram; PTAT and reference frequency are connected to the first stage of PTAT and reference counters, respectively. The reference counter consists of 9 bits whereas PTAT counter has 15 bits. The PTAT counter size is chosen such that it will not overflow, especially at high temperature where PTAT frequency is at its maximum. Adding more bits to the PTAT counter increases static power linearly with little impact on dynamic power since MSB switching activity is very low. Flip-flops use I/O devices to minimize leakage and short circuit current during transitions. As a result, the leakage current of a single flip-flop is measured to be 112fA at room temperature.

When Start signal is triggered, the oscillators start running and both counters begin counting upward. Both counters stop when the reference counter saturates and the Done signal is set. At the same time, the digital code is read from the PTAT counter. The counter is reset by the Start signal. Conversion time is tunable by selecting the size of the reference counter (6 to 9 bits).

	Slope	Output @ 20°C	R^2 Value
μ	0.273mV°C	72.9mV	0.9996
σ	4.65µV/°C	1.17mV	$6.217×10^{-5}$
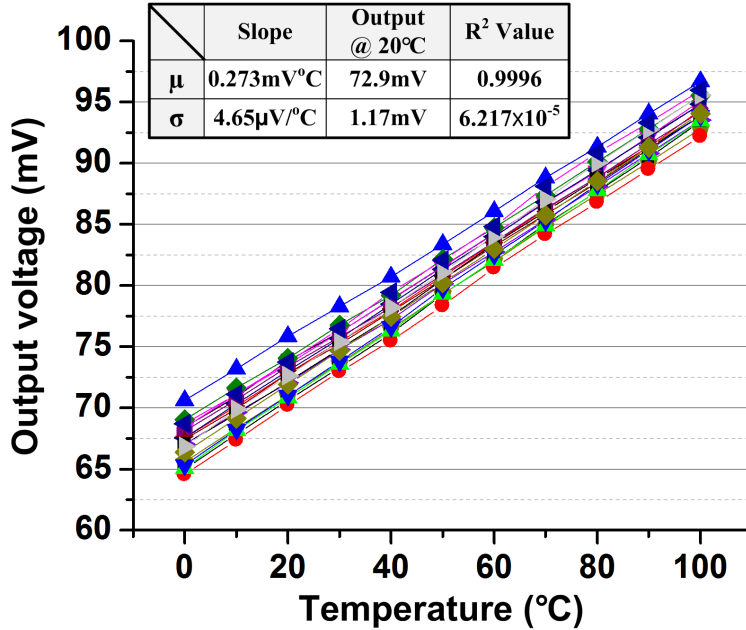
Figure 2.13: Measured output voltage of sensing element.

2.2.5 Noise Analysis

Noise simulation of the sensor shows $0.26°C_{rms}$ of error at room temperature and the dominant noise source (80%) is thermal noise of the op-amps in the temperature sensing core due to their low current consumption. Therefore, to further improve noise performance, op-amp tail current should be increased. Once op-amp thermal noise is decreased (at the expense of power), thermal noise in the sensing element and reference generator becomes the next dominant source of noise. This noise can be decreased by adding capacitors, slowing response time. The next dominant source of noise is flicker noise in the op-amps. Such low frequency noise can be reduced by implementing auto-zeroing or chopping. However, care must be taken with these techniques due to the extremely small current flowing through the sensing element. The addition of MOSFET switches introduces subthreshold and body leakage which degrade the temperature characteristics of the sensing element. Also, clock feedthrough and charge injection will require additional stabilization time for the sensing element.
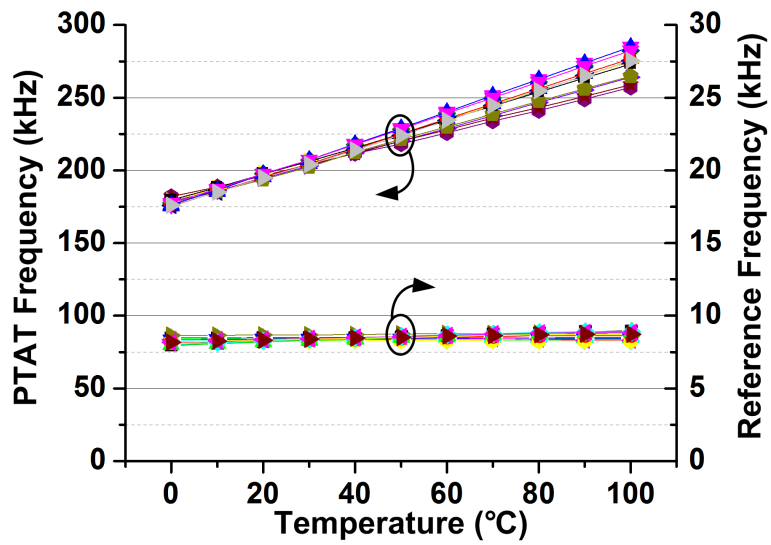
Figure 2.14: Measured PTAT and Reference Frequency.
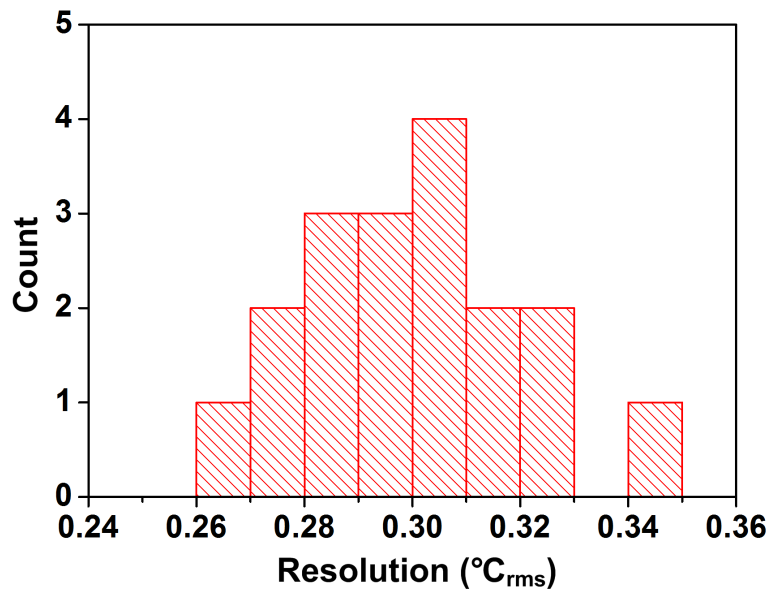
Figure 2.15: Measured resolution of temperature sensor.
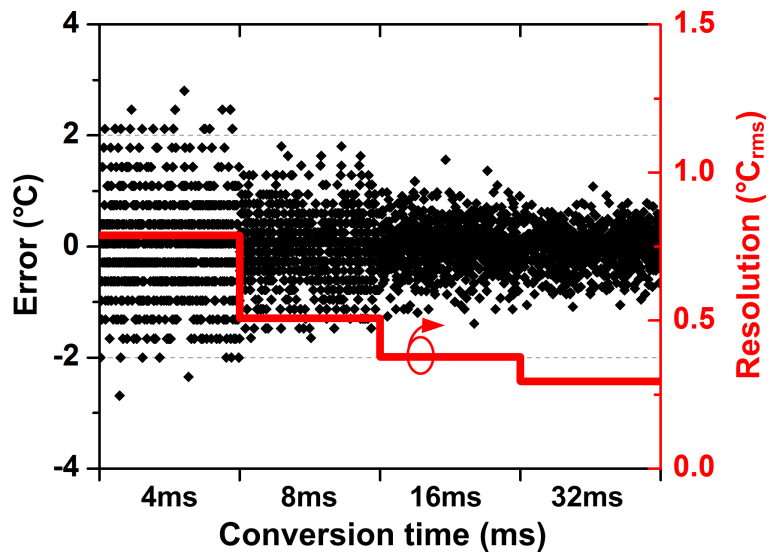
Figure 2.16: Measured temperature uncertainty depending on conversion time.
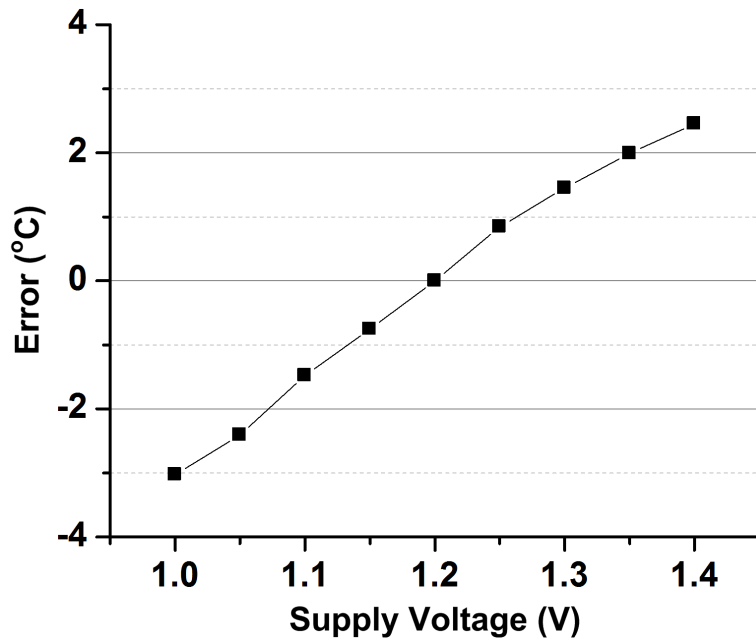
Figure 2.17: Measured supply sensitivity of the sensor at 25°C.
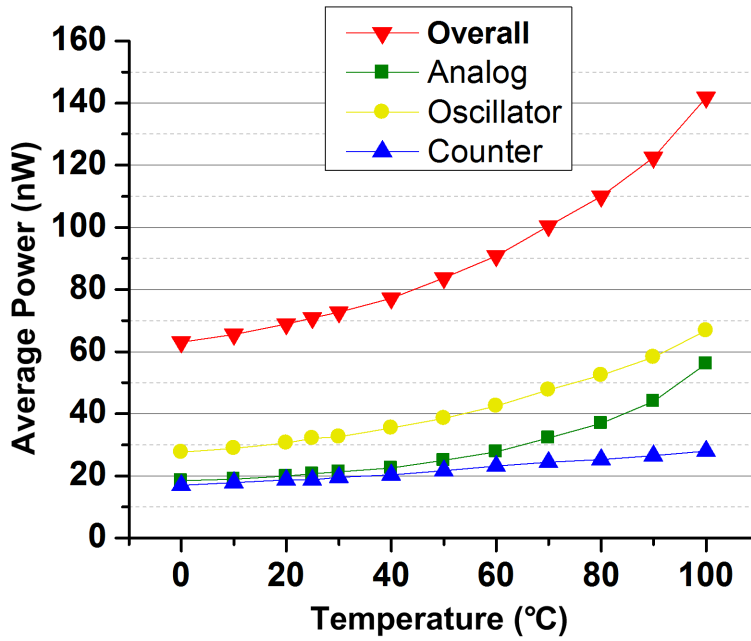
Figure 2.18: Measured average power of the temperature sensor and corresponding breakdown by component.
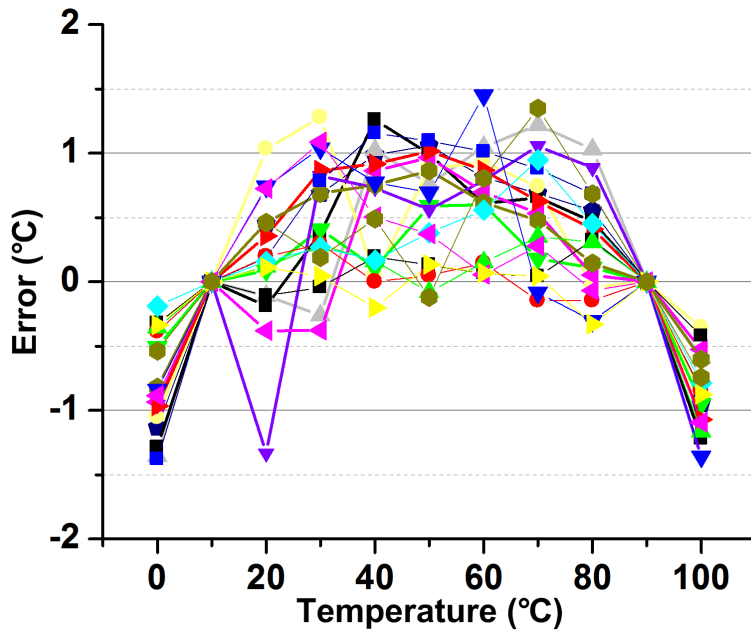
Figure 2.19: Measured temperature error over 18 samples.
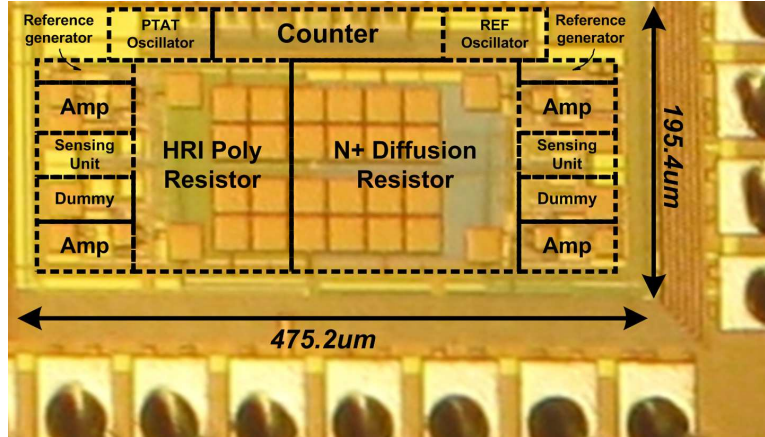
Figure 2.20: Die photo of the proposed sensor in 0.18μm CMOS.

2.3 Measurement Results

The proposed temperature sensor is fabricated in 0.18μm CMOS in 0.09mm^2. Measurements were made on 18 dies, taken from 4 different wafers in two different lots to observe the effect of process variation. Measured sensing element output voltage is given in Figure 2.13. The proposed circuit generates a process-independent slope and output value while maintaining good linearity. Average sensing element power consumption is measured to be only 10pW. Measured average PTAT frequency ranges from 176kHz to 275kHz, leading to a resolution of 0.04°C/LSB with the 8-bit reference counter running at 8.4kHz (Figure 2.14). However, the effective resolution of the sensor is thermal noise-limited. Figure 2.15 shows measured rms resolution across different chips at a conversion rate of 32.8 samples/sec; average resolution is measured as 0.3°C$_{rms}$. Resolution can be improved by using a longer conversion time at the expense of energy. Figure 2.16 shows measured temperature uncertainty with different conversion times. It can be seen that rms error decreases as conversion time increases since high frequency noise is averaged out. Supply sensitivity of the sensor is measured to be +2.5/-3.15°C from 1.0-1.4V supply variations (Figure 2.17). The complete sensor consumes 54nA at room temperature with supply voltage of 1.2V (59nA average across the 18 dies). Figure 2.18 provides the overall power breakdown and shows that the ring oscillator is the largest component. Figure 2.19 gives the measured temperature sensor inaccuracy over 18 different test chips. After 1-point calibration at 50°C, the measured error is +3.7°C/-4.5°C across 0 to 100°C. However, the measured error is reduced to +1.5°C/-1.4°C after 2-point calibration at 10°C and 90°C.

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Parameters	This Work	CICC'08 [16]	ASSCC'07 [15]	TCAS2'09 [13]	TCAS2'12 [14]	ISSCC'14 [17]	JSSC'13 [11]
Process	180nm	180nm	350nm	180nm	180nm	160nm	160nm
Type	MOSFET	MOSFET	MOSFET	MOSFET	MOSFET	MOSFET	BJT
Voltage	1.2V	1V	1.4V, 2.1V	0.5V, 1V	1.2V	0.85-1.2V	1.5V
Temperature Range	0–100°C	0–100°C	35–45°C	-10–100°C	0–100°C	-40–125°C	-55–125°C
Resolution	$0.3°C^1$	$0.1°C^1$	0.035°C/LSB	0.2°C/LSB	0.3°C/LSB	$0.063°C^1$	$0.02°C^1$
Conversion Time	30ms	100ms	100ms	30ms	1ms	6ms	5.3ms
Calibration	2-point	2-point	2-point	2-point	2-point	1-point	1-point
Inaccuracy	+1.5°C/-1.4° C^{2a}	+3°C/-1.6° C^{2a}	+0.1°C/-0.1° C^{2a}	+1°C/-0.8° C^{2a}	+1°C/-0.8° C^{2a}	±0.4° C^{2b}	±0.15° C^{2b}
Relative Inaccuracy[3]	2.9	4.6	2	4.5	1.8	0.48	0.2
Fully Integrated[4]	Yes	Yes	No	No	No	No	No
Power	71nW	220nW	110nW[5]	120nW[5]	405nW[5]	600nW[5]	5.1μW[5]
Energy/ Conversion	2.2nJ	22nJ	11nJ[5]	3.6nJ[5]	0.41nJ[5]	3.6nJ[5]	27nJ[5]
FOM[6]	0.19	0.22	0.013[5]	0.14[5]	0.037[5]	0.014[5]	0.011[5]

1. Degree RMS.
2a. Maximum error value, 2b. 3σ value.
3. Relative Inaccuracy (%) = Max error/Temperature range ×100 [28].
4. The sensor does not require any external references for their operation.
5. Power or Energy for generating external references not included.
6. FOM[nJ/K^2]=Energy/conversion × (Resolution)^2 [28].

Table 2.1: Performance summary and its comparison with recently published low power temperature sensors.

The test chip die photo is shown in Figure 2.20. The two resistors occupy 42% of the total area. 2.1 compares the design with other low-power temperature sensors. The sensors that consumes less than 10w and 100nJ/conversion are highlighted for its possible usage in sensor nodes. The proposed design shows significantly better energy per conversion and relative inaccuracy compared to our previous fully-integrated temperature sensor [16]. The sensor consumes the lowest power even when compared to other MOSFET-based designs that use high accuracy external clocks while achieving comparable resolution and relative inaccuracy.

2.4 System Integration

The proposed temperature sensor was fabricated into a separate chip for integration into an ultra-low power wireless sensor node [6]. Figure 2.21 shows a die photo of the stacked system and corresponding IC layers. The newly designed sensor layer contains the proposed temperature sensor. The other layers are similar to those reported in [6]. After initial programing, the stacked system switches between sleep and active modes to periodically take temperature measurements. Measured data has been successfully retrieved by the processor layer and checked with an external
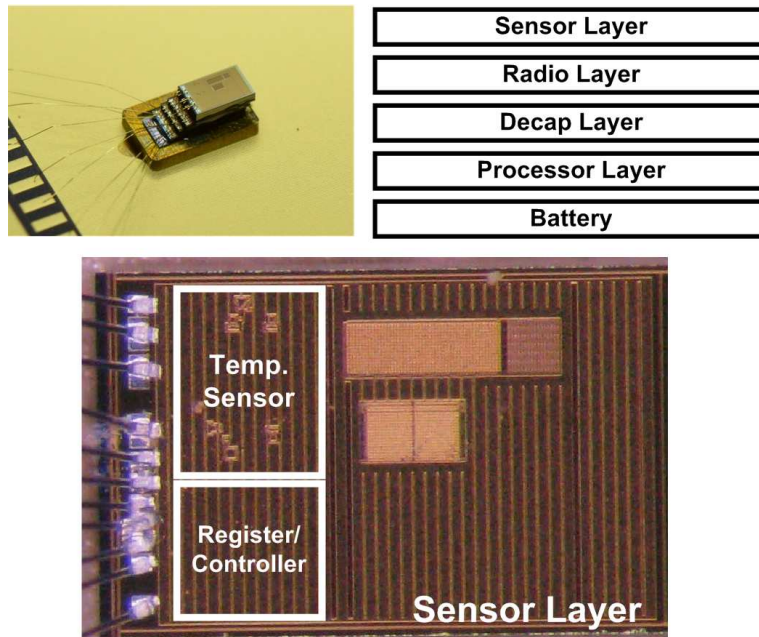
Figure 2.21: Photo of a stacked system with proposed temperature sensor in a sensor layer (top left). Bottom shows a die photo in 0.18μm CMOS of the sensor layer.
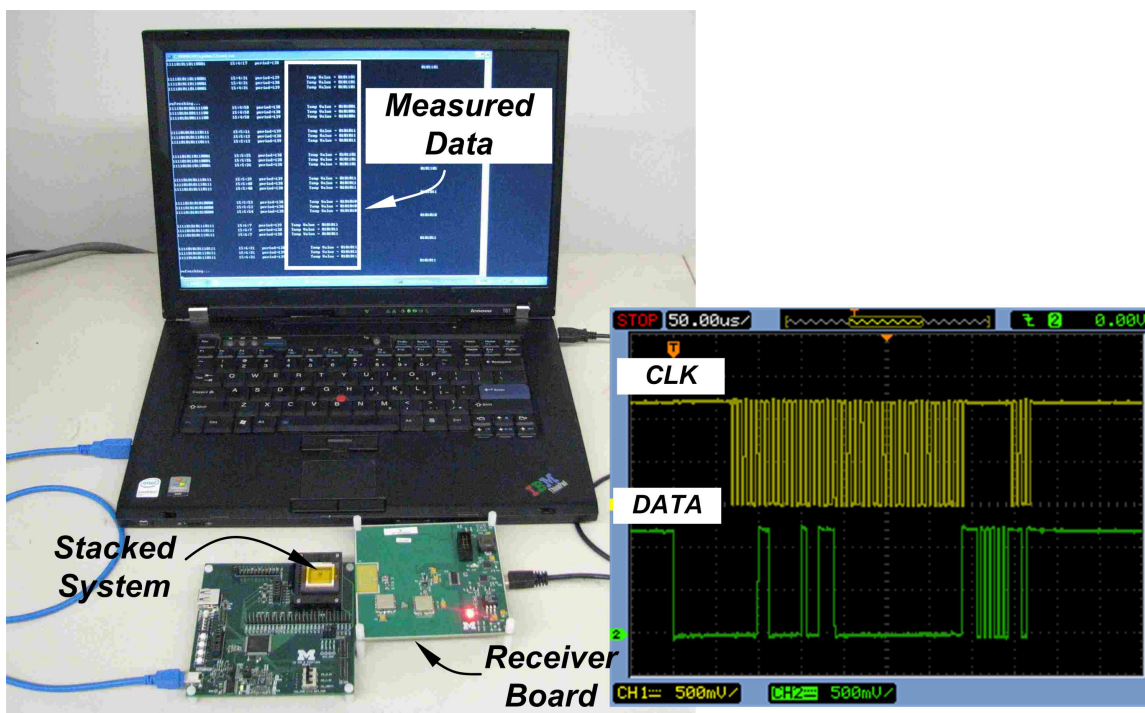
Figure 2.22: Testing setup for the stacked system (Fig. 2.21, top left) and measured waveform.
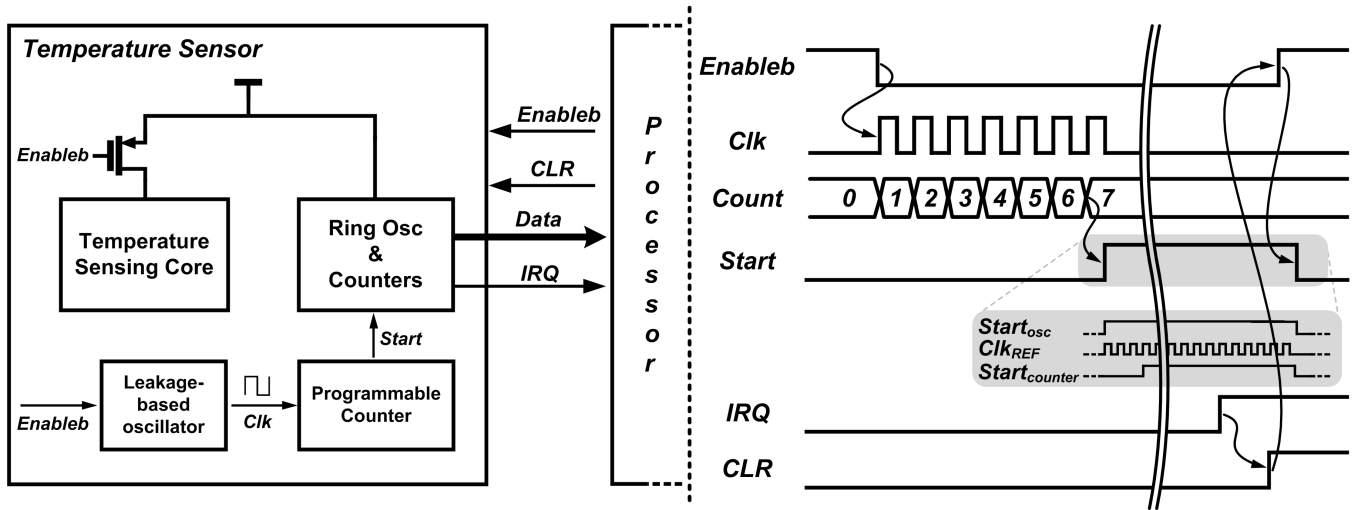
Figure 2.23: Block diagram of a temperature sensor in the system and its timing diagram.
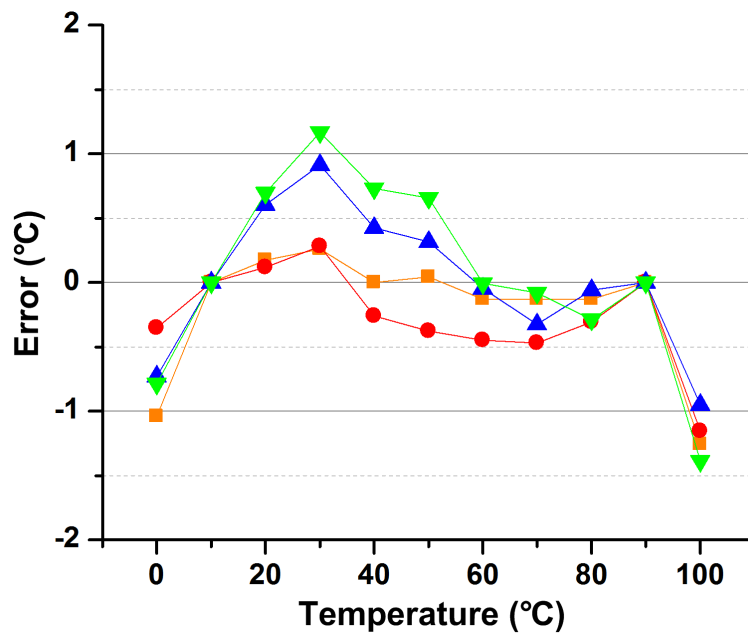
Figure 2.24: Measured temperature error of the stacked system over 4 samples.

debugger. Also, measured data is transmitted and received by using a near-field radio [5] (Figure 2.22).

Figure 2.23 shows a block diagram of the temperature sensor interface with the full system. The temperature sensing core consumes 20nW at room temperature and is power-gated to minimize standby power consumption. However, ring oscillators and counters are not power-gated since they consume negligible power ($\sim$7pW) during standby mode. When power gating is released, a certain amount of startup time is required for the temperature sensing core to stabilize. Stabilization requires 100ms at room temperature with an energy consumption of 1.6nJ (simulated). Since there is no benefit to having the processor running during this time, the processor initially goes to sleep after a temperature measurement request. The start-up delay is generated internally using a leakage-based oscillator [22] and programmable counter. When a temperature measurement is requested, power gating is released and the leakage-based oscillator starts. Frequency of the leakage-based oscillator has comparable temperature dependency to the required stabilization time of the sensing core. After counting up to a pre-configured number of cycles, Start signal is released and oscillation begins. To allow the frequencies to stabilize, conversion starts after a fixed number of cycles of the reference oscillator. When conversion is finished, interrupt is asserted to wake-up the processor for data acquisition. Finally, the CLR signal is set from the processor to reset the temperature sensor and power gating is reasserted.

Figure 2.24 shows measured error of 4 stacked sensor nodes after 2-point calibration at 10°C and 90°C (+1.2°C/-1.4°C). Compared to measurement results shown in 2.3, the accuracy of the sensor is maintained. On the other hand, average resolution is measured to be 0.8°C (rms, 30ms/conversion). The resolution degrades by $\times 2.6$ compared to standalone testing, mainly due to supply voltage ripple when generated by the power management unit (PMU) based on switch capacitor network. However, the resolution is improved to 0.37°C by increasing conversion time ($\times 4$), at the expense of energy.

2.5   Conclusions

This work demonstrated a novel temperature sensor that can be integrated into a battery-driven ultra-low power system. The sensor achieves ultra-low power by introducing a new sensing el-

ement that benefits from low output voltage and process invariant temperature characteristics. Moreover, a second feedback loop is introduced into a conventional voltage-to-current converter to eliminate power consumed in a current mirror. As a result, the sensor consumes only 71nW at room temperature. Without any external components, the sensor achieves $+1.5^\circ$C $/-1.4^\circ$C of inaccuracy from 0°C to 100°C and consumes 2.2nJ/conversion. An example use scenario for the proposed sensor is demonstrated in a battery-operated wireless sensor node.

CHAPTER 3

A 5.8nW CMOS Wake-up Timer for Ultra-Low Power Wireless Applications

3.1 Introduction

There is a growing interest in the design of compact wireless systems with volumes of 1cm^3 or less [6, 29, 30]. Such microsystems could benefit a wide range of application areas, including field of biomedical, military, and environmental investigation. However, the miniaturized size renders power consumption a critical factor in system design due to limited energy storage capacity. To address this issue, the system is often severely duty cycled. Even though the active power of the sensor or radio transmission is large, their average power consumption can be made negligible by having a long idle time between each operation. The idle time or ratio of the duty cycle should be adjustable depending on the target application. A wake-up timer with precise time tracking is useful in that sense as it can be used for scheduling and time-stamping each measurement, as well as synchronizing two different sensor nodes [6]. Since the wake-up timer is one of the few components that must remain on during standby mode, it becomes dominant in determining average power consumption. Therefore, it is vital to reduce wake-up timer power consumption while also maintaining accuracy to ensure proper time keeping.

Quartz crystals are the conventional choice for precision oscillators due to their excellent temperature and frequency stability. Recently, low power operation of these oscillators has been reported [31, 32]. However, the requirement of an external component limits their usage in very

compact wireless systems as they drive up system volume. Alternatively, MEMS-based oscillators have been introduced for integrated silicon-based solution [33, 34]. These works show small form-factor and high accuracy, but high power consumption ($> \mu$W) makes them unsuitable for wake-up timers.

Relaxation oscillators are preferred for their low-power operation and ability to be integrated entirely on-chip. However, they show inferior temperature and voltage insensitivity compared to crystal or MEMS-based oscillators. The basic operation of relaxation oscillators is shown in Figure 3.1. A capacitor (C_{INT}) is charged with a current source (I_{REF}) and repeatedly reset. A continuous comparator is used for triggering the reset signal by comparing capacitor voltage (V_{INT}) against a fixed voltage level (V_{REF}). An inverter chain ensures sufficient reset time to fully discharge the capacitor. As this periodic operation continues, a sawtooth waveform and output clock are generated on the capacitor and comparator output, respectively. The output clock period can be expressed as follow,

$$T_{period} = \frac{C_{INT}V_{REF}}{I_{REF}} + 2t_d. \tag{3.1}$$

where t_d is comparator and buffer delay. In this scheme, even if the charging time ($C_{INT}V_{REF}/I_{REF}$) is perfectly compensated, temperature/supply dependent comparator and buffer delays (t_d) impact the clock period. A simple way to address this issue is to make the comparator and clock buffer bandwidth high enough, making them negligible relative to the overall period. However, this incurs high power consumption.

Several methods have been introduced to increase tolerance of clock period against temperature and supply voltage variation. In [35] and [36], charging time sensitivity is reduced with a chopping technique to eliminate comparator offset. On the other hand, a replica circuit is used with a feedforward period control to remove comparator and buffer delay from the oscillation period [37]. An inverter-based RC oscillator [38] implements switching-point insensitive oscillation and regulates local supply voltage using a replica inverter. As a result, both charging time and delay are held constant. Also, compensation techniques using an external [39] or on-chip [40] clock reference have been proposed to suppress period variations. Even though high accuracy (14 to 104ppm/°C in the kHz range) is achieved with these techniques, their power consumption (120nW

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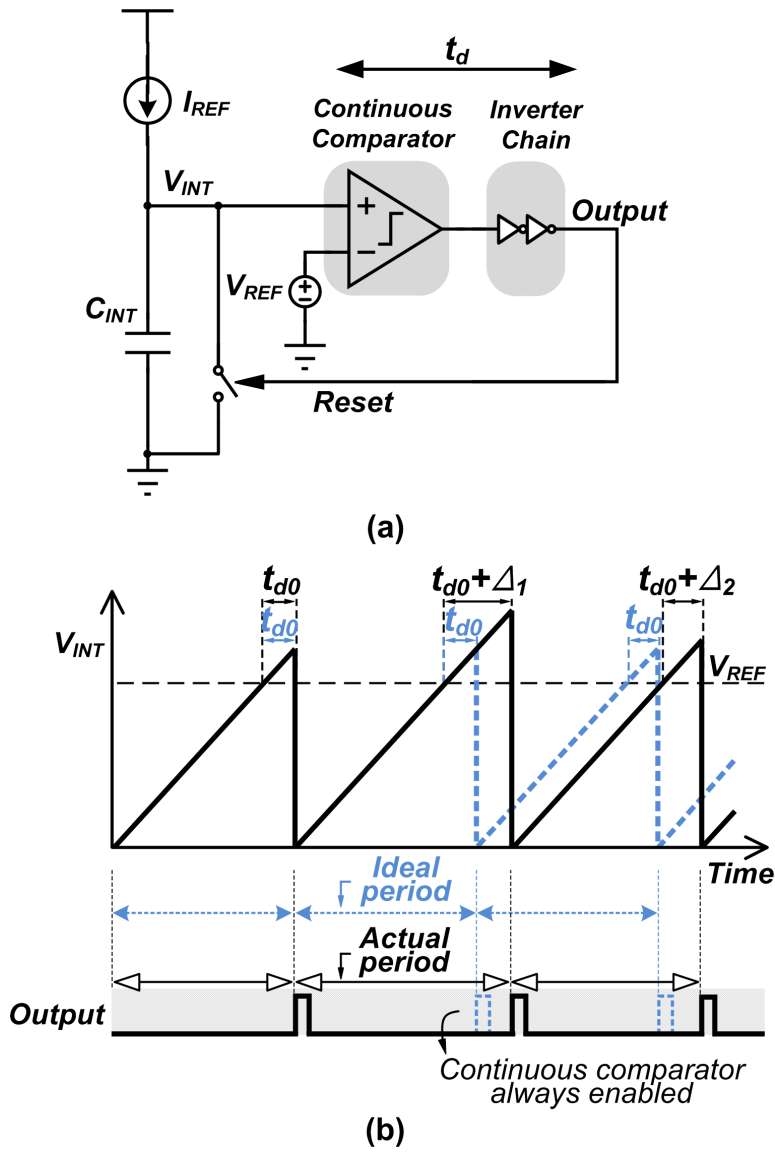
Figure 3.1: (a) Basic structure and (b) concept of a conventional relaxation oscillator.

to 4.5μW) remains high compared to standby power in compact battery-powered systems. Further power reduction can be achieved by slowing the clock frequency, making comparator and buffer delays negligible. A small gate leakage is used as I_{REF} in [41], [42] to reduce clock frequency to Hz range. Alternatively, power consumption in generation of I_{REF} has been minimized with program-and-hold technique [43]. These oscillators consume sub-nW but are highly temperature sensitive ($\geq$375ppm/°C) and offer poor supply stability ($>$40%/V), which is a critical drawback in battery-powered systems with often poor voltage regulation.

To avoid the fundamental trade-off between temperature-dependent comparator delay and comparator power, we introduce a constant charge subtraction scheme along with low-power time tracking topology that eliminates comparator delay from the clock period.

3.2   Proposed Low-Power Topology

Figure 3.2 shows a block diagram of the proposed oscillator and its operating concept. Instead of the conventional approach of fully discharging the integrating capacitor (C_{INT}), a constant amount of charge (CV_{REF}) is subtracted from C_{INT} through an amplifier. The power-hungry continuous comparator is replaced with a coarse, asynchronously clocked comparator to detect the subtraction point (V_{SUB}). While the actual subtraction point varies ($t_{d0} + \delta_i$) due to the asynchronous operation of a clocked comparator, the constant charge subtraction creates a sawtooth waveform that always rejoins the ideal sawtooth waveform. Therefore, the exact subtraction time does not impact the sawtooth waveform and hence the clocked comparator can be slow and inaccurate, allowing its power to be reduced to $\sim$100 pW. The sawtooth waveform period can be expressed as follows:

$$T_{period} = \frac{Q_{Const}}{I_{REF}} = \frac{C}{I_{REF}}(\frac{A}{A+1}V_{REF}).$$

(3.2)

where A is finite amplifier gain. It can be seen that amplifier gain should be temperature-independent and also large to have temperature-insensitive output period.

While this approach requires an amplifier with high gain for accurate charge subtraction, its power consumption can be made very low since the bandwidth can be relaxed to match the os-
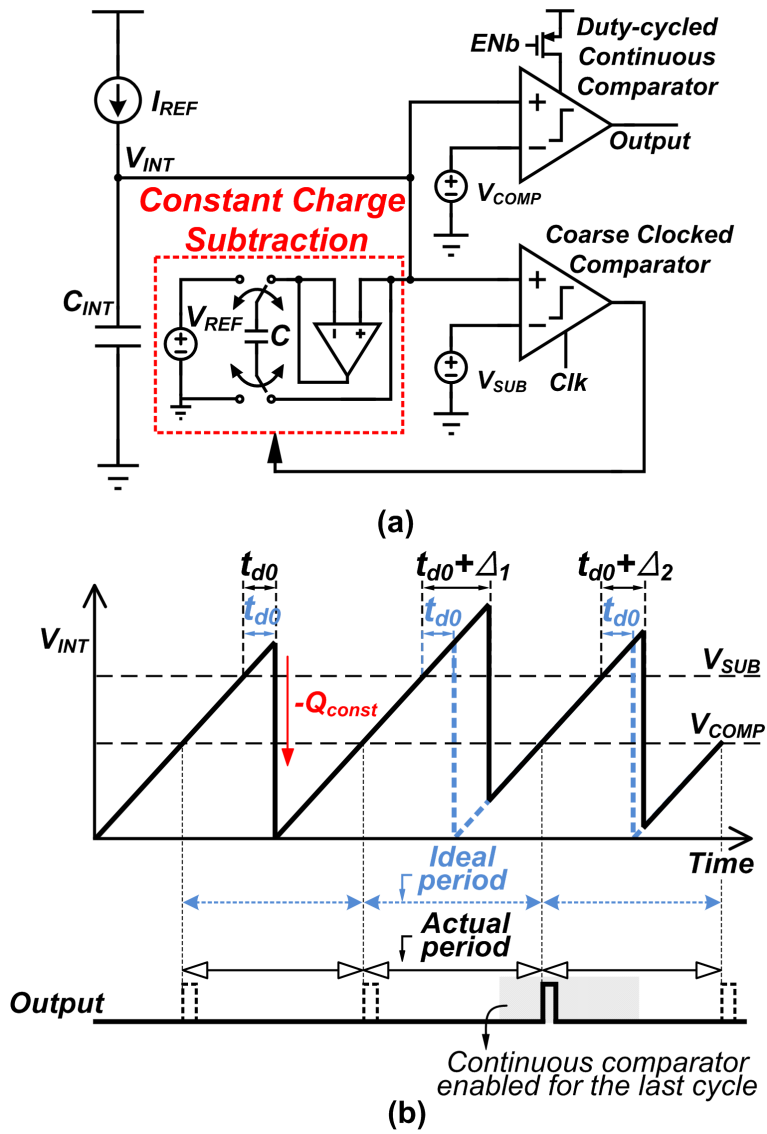
Figure 3.2: (a) Basic structure and (b) concept of low power operation using a constant charge subtraction scheme.

cillator frequency. The constant charge subtraction itself does not output a constant frequency as the interval between subtraction points is not constant. In order to generate a periodic signal, an auxiliary continuous comparator is required. The continuous comparator necessarily consumes high power to guarantee an ideal period as in the conventional scheme. However, since this work targets a wake-up timer rather than an oscillator, a low jitter high frequency clock is unnecessary. This allows the power hungry continuous comparator to be power-gated the vast majority of the time, which is not possible in conventional architectures since the continuous comparator is directly in the oscillation path. A counter is used to control the power-gate by tracking the number of subtraction cycles. As a result, the accurate continuous comparator is only triggered for the last cycle in order to generate a precise wake-up signal. With this scheme, an accurate wake-up signal is generated while the oscillator operates at ultra-low power for all but the final clock period.

The constant charge subtraction scheme can be implemented in different ways, just as there are variants of the relaxation oscillator. The reference voltage, which is used as a threshold for the comparator, can be implemented in two ways; 1) applying a current across a resistor, or 2) directly using a voltage source. When resistor is used, charging time can be made independent of current by mirroring the same current that is used to charge the capacitor. As a result, charging time only depends on resistance and capacitance. Temperature dependence of metal-insulator-metal (MIM) or metal-oxide-metal (MOM) capacitors are negligible, while resistor temperature dependency can be minimized by combining two different types of resistor with opposite temperature coefficients [44]. On the other hand, when a voltage source is used, both voltage and current sources need to be compensated with respect to temperature. Considering that there is only one passive component rather than two active components that need to be temperature compensated, the former approach is preferable. However, the first approach requires a large resistance when targeting power budgets below tens of nW. Even with 100mV of voltage swing on the capacitor, 100MΩ is required to reduce the current to 1nA, which is impractical for on-chip integration. This necessitates the use of both current and voltage sources, which makes the low power design of a wake-up timer more challenging.
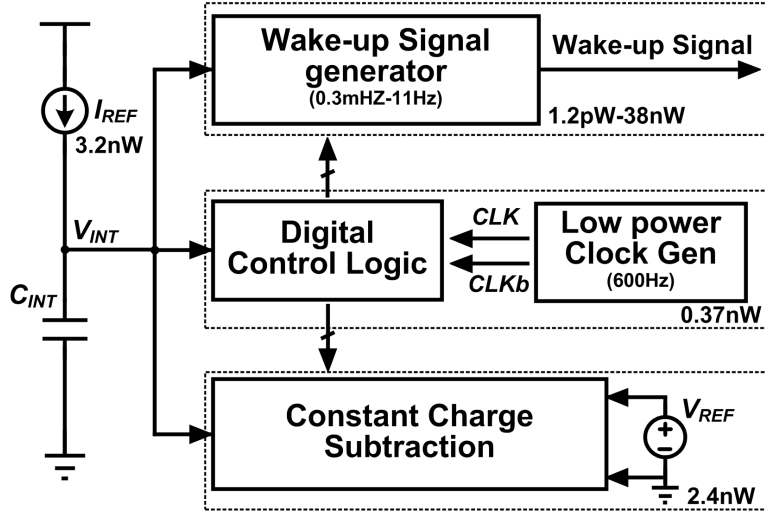
Figure 3.3: Overall block diagram of the proposed timer.

3.3 Circuit Description and Analysis

Overall block diagram of the proposed timer is shown in Figure 3.3. The timer consists of current and voltage references, constant charge subtraction block, wake-up signal generator, digital control logic, and a low-power clock generator. As current reference charges C_{INT}, digital logic observes node V_{INT} and controls charge subtraction. The digital logic also controls the generation of the wake-up signal, while the low-power clock generator provides clocks for the digital logic.

3.3.1 Constant Charge Subtraction

Figure 3.4 describes the detailed operation of the constant charge subtraction method. The structure consists of two operational amplifiers (op-amps), namely the subtraction and charging amplifiers, and two capacitors; integration capacitor (C_{INT}) and subtraction capacitor (C_{SUB}). Initially, C_{INT} is reset to ground with switch configurations Φ_{1R} and Φ_{2R} rather than adding an additional device. This helps to reduce error arising from subthreshold leakage, which is not negligible in low frequency applications, particularly at high temperatures. For example, a minimum-sized I/O device at $80°C$ has 420fA of subthreshold leakage, which leads to 0.51% error in timer period. Following an initial reset, the scheme cycles through two main phases; charge (ϕ_1) and subtraction (ϕ_2). In ϕ_1, C_{SUB} is connected to a voltage reference (V_{REF}) through the charging amplifier. C_{SUB} is charged to a fixed voltage (V_{REF}) as the charging amplifier is configured as a unity-gain buffer. At

Figure 3.4: Detailed structure of proposed constant charge subtraction scheme.

the same time, the subtraction amplifier goes into a sampling phase where offset is stored on C_{az1} to remove offset and 1/f noise of the amplifier. The integration capacitor (C_{INT}) is disconnected from the subtraction amplifier to reduce leakage. By introducing an additional switch for isolation, the number of off-state switches connected to the integration node (V_{INT}) during ϕ_1 is reduced. In a given period, it is preferable to maximize ϕ_1 (i.e., minimize ϕ_2) to reduce the leakage. However, there is a limit as certain amount of time is required for the subtraction to occur. In this work, ϕ_1 has been designed to be 3 times longer than ϕ_2. In simulation, this reduces leakage by 2.2× and improves timer error by 0.14%. In simulation, this reduces leakage by 2.2× and improves timer error by 0.14%. As the current source (I_{REF}) charges up C_{INT}, V_{INT} reaches the subtraction threshold voltage (V_{SUB}), and the next phase (ϕ_2) is triggered. During ϕ_2, C_{SUB} is disconnected from the charging amplifier and connected to C_{INT} through the subtraction amp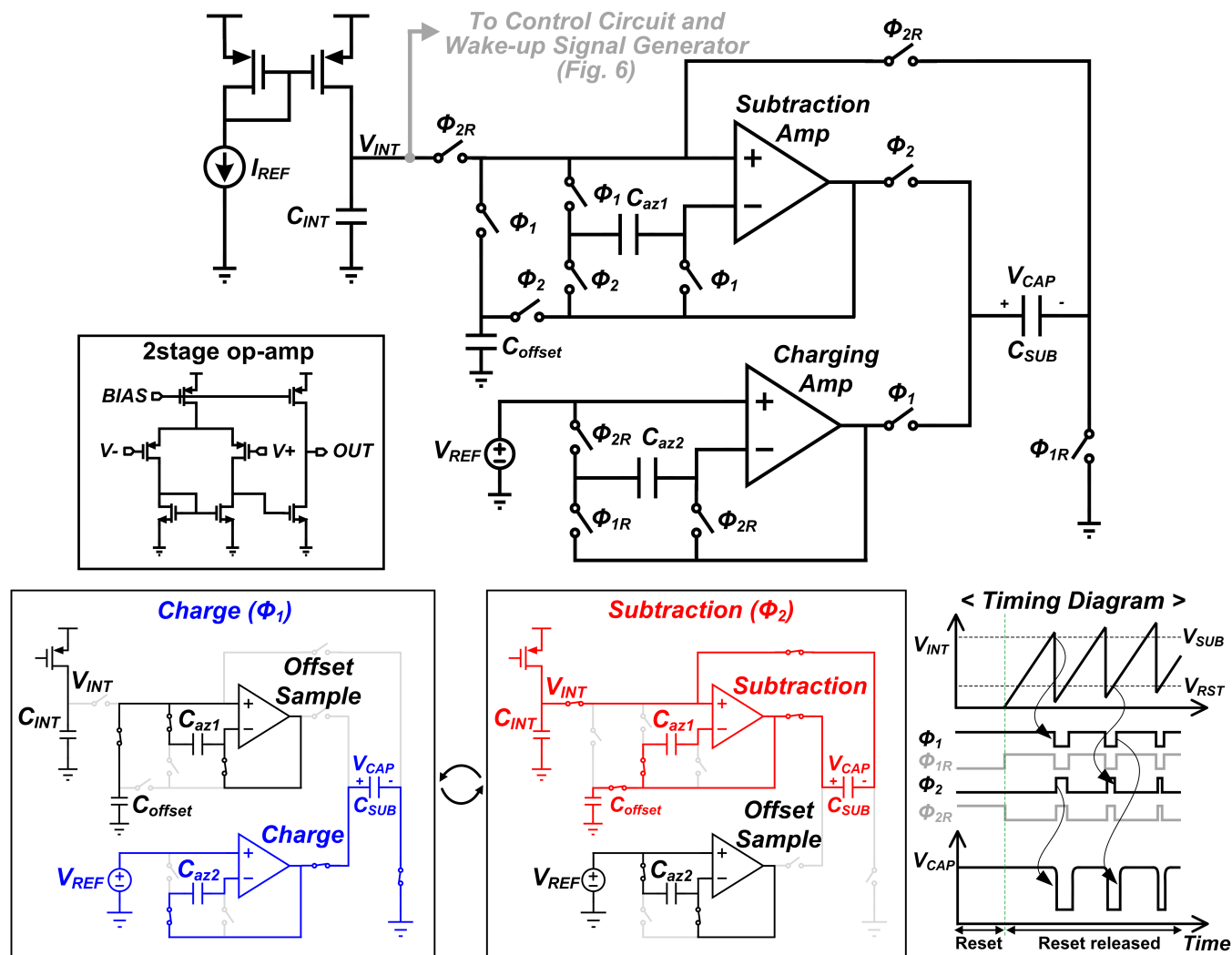lifier. The amplifier therefore subtracts charge in C_{SUB} from C_{INT}. Simultaneously, the charging amplifier goes into a sampling phase and offset is stored on C_{az2} for the next phase. After subtraction, the phase reverts to ϕ_1 when V_{INT} exceeds the reset voltage (V_{RST}). Simultaneously, the voltage on V_{INT} is stored on C_{offset} for offset sampling of the subtraction amplifier during ϕ_1.

A two-stage topology is used for both charging and subtraction op-amps. The amplifiers are designed to have a dominant pole at the second stage due to ∼10pF of C_{SUB}. Otherwise, a large compensation capacitor would be required, which is not preferable as it degrades amplifier bandwidth to the Hz range. Amplifier tail currents should be designed to meet required slew rates for charging/discharging operation. The subtraction amplifier must have sufficient current to pull down the output node at the beginning of ϕ_2 and follow V_{INT} until the end of ϕ_2, while the charging amplifier must be able to pull the discharged V_{CAP} up to V_{REF} within ϕ_1. The subtraction amplifier tail current is boosted to 5.5nA during ϕ_2 to have fast response time and reduced to 500pA during ϕ_1 to save power. On the other hand, the charging amplifier tail current is fixed at 500pA since ϕ_1 is 3 times longer than ϕ_2.

Input- and temperature-dependent amplifier offset and gain can lead to error in the resulting timer period. For the charging amplifier, input-dependent offset is not a concern as it always sees a fixed input voltage. However, due to the asynchronous operation of clocked comparators, the subtraction amplifier sees different values of V_{INT} at the end of ϕ_2. Figure 3.5a shows the dependency of offset and gain on the input level of the subtraction amplifier. It can be seen that
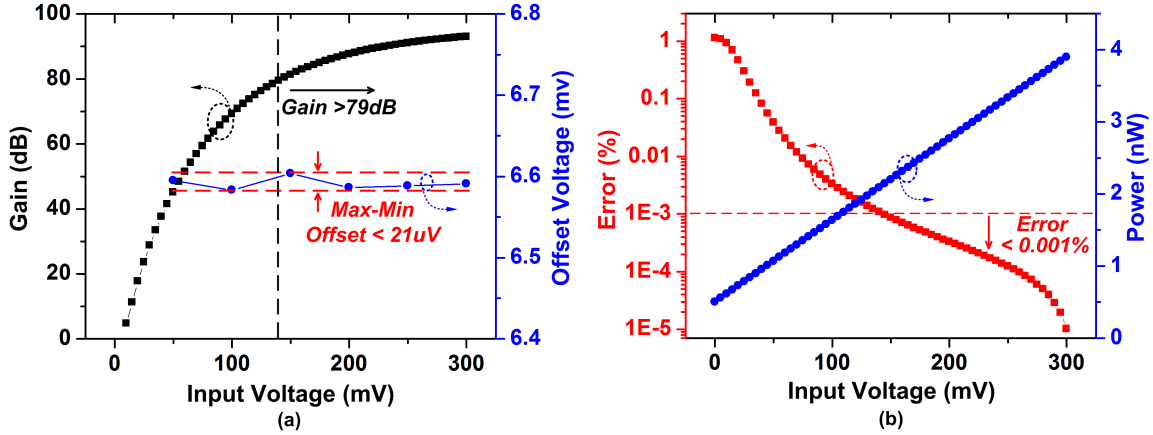
Figure 3.5: (a) Simulated offset and gain of subtraction amplifier depending on input voltage and (b) its effect on the frequency error and power.

while input offset dependency is negligible, the gain increases as the input voltage increases.

Differences in amplifier gain across temperature result in a varying amount of charge being subtracted. Therefore, the absolute value of gain should remain high across the targeted temperature range to minimize error. Simulation results on the frequency error and power consumption depending on input voltage level is shown in Figure 3.5b. The error decreases as input voltage increases, but at the expense of power consumption. Power consumption increases due to a longer subtraction phase (ϕ_2). The results show that the subtraction amplifier input voltage should be higher than 140mV at the end ϕ_2 to maintain <0.001% error. This implies that there is a minimum frequency constraint for the clocked comparator to suppress the voltage variation. To achieve this, an ultra-low power oscillator is used and its design and frequency dependency will be discussed in Section 3.2. The reset voltage (V_{RST}) that sets the input voltage of end of ϕ_2 is designed to be ~175mV considering the worst case offset coming from the clocked comparator. In the targeted temperature range, both amplifiers are designed for open-loop gain of >78dB with unity-gain bandwidth of 20 kHz.

3.3.2 Control Logic

Control logic is used to toggle switches in the charge subtraction scheme as well as to generate the power-gate signal (ENb). Figure 3.6 provides a detailed schematic of this control logic. The 4T voltage reference [18] and PMOS diode stack are used to generate two reference voltages,
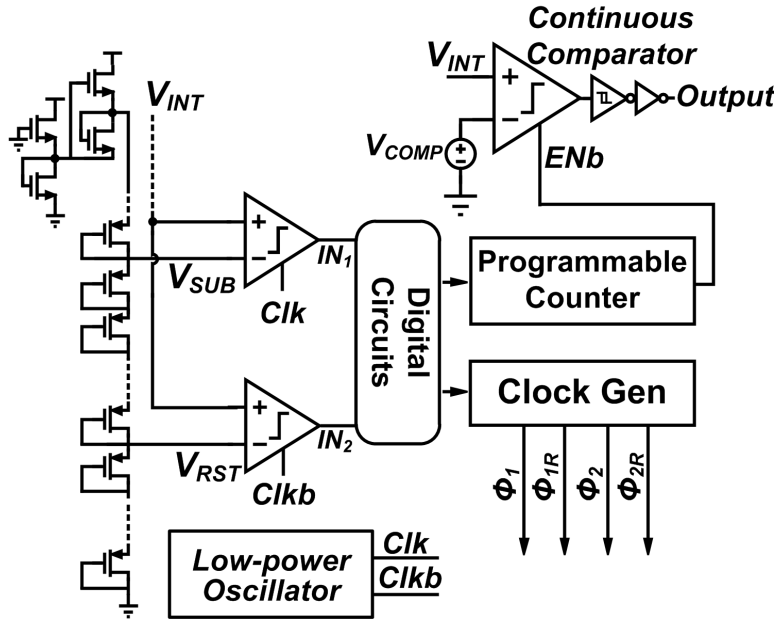
Figure 3.6: Detailed schematic of control circuit for generating wake-up signal and clocks.

V_{SUB} and V_{RST}. Generated voltages are then compared against V_{INT} with clocked comparators. Due to the low input range from near-ground to VDD/2, the comparator uses a PMOS input stage for proper operation. A single-stage comparator uses a regenerative latch [46] for low power operation. In order to minimize kickback, two comparators operate with opposite clock phases. The comparators show 3σ offset of 40mV in simulation which is sufficient to keep the input voltage of the subtraction amplifier $>$140mV.

The comparator clock is generated with a thyristor-based oscillator [47]. The frequency of the oscillator determines the input voltage difference on the subtraction amplifier between two consecutive cycles. The frequency of the oscillator also determines the voltage deviation of V_{INT} from the V_{SUB} at the subtraction point. The voltage deviation should be low enough to prevent V_{INT} being higher than V_{RST} after subtraction which would stop the oscillation. Maximum voltage difference occurs when the comparison is delayed by the entire comparator clock cycle. For example, a 600Hz oscillator frequency can result in 10mV voltage difference in worst case. Higher frequencies guarantee smaller voltage difference, but at the expense of power. Due to its leakage based operation, the oscillator output frequency shows high temperature sensitivity. As shown in Figure 3.7, frequency and power increase by $100\times$ in the targeted temperature range. Therefore, the minimum clock frequency must be set according to the lowest expected operating temperature.
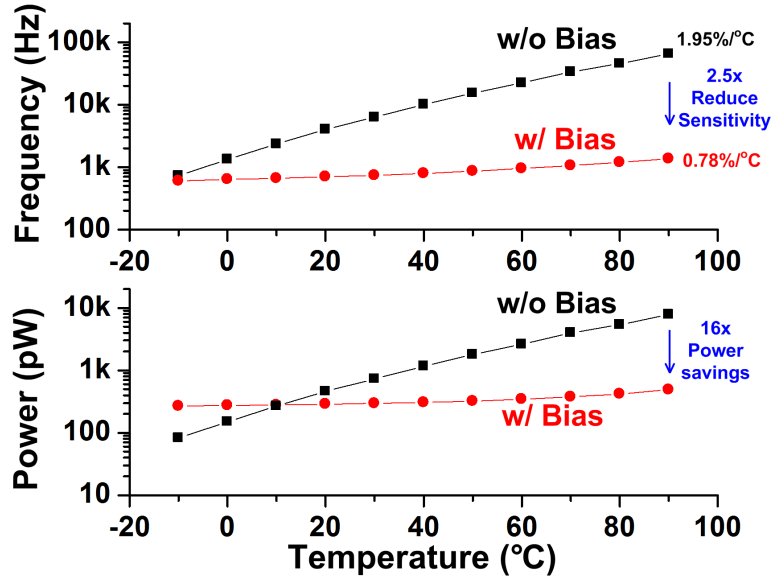
Figure 3.7: Simulated frequency and power consumption of thyristor-based oscillator over temperature.

This will cause unnecessary power consumption, especially at high temperature.

To avoid undesired power consumption, the oscillator has been current starved with a reference current (described in 3.3.4) using a current mirror to tolerate the temperature dependence. Simulation results show that biasing the oscillator with a current reference gives $16\times$ of power savings at high temperature. Although the oscillator temperature sensitivity is reduced by $2.5\times$, the oscillator frequency still varies by 39% across the targeted temperature range. However, overall timer period is not impacted due to the constant charge subtraction scheme. Overall the oscillator consumes 300pW at an operating frequency of 700Hz (25°C).

3.3.3   Wake-up Signal Generator

A 2-stage op-amp serves as an accurate continuous comparator for generating a wake-up signal in the last cycle. The continuous comparator consumes 25nA ($5\times$ the current of the complete timer during all previous cycles), which leads to a comparator delay that is less than 0.1% of the period across the targeted temperature range. The reference current (I_{REF}) is used to bias the continuous comparator to maintain constant delay over temperature variations. A reconfigurable 16-bit asynchronous counter controls the interval between each wake-up. Since the counter runs at the speed of the subtraction cycles, its power consumption is dominated by leakage rather than

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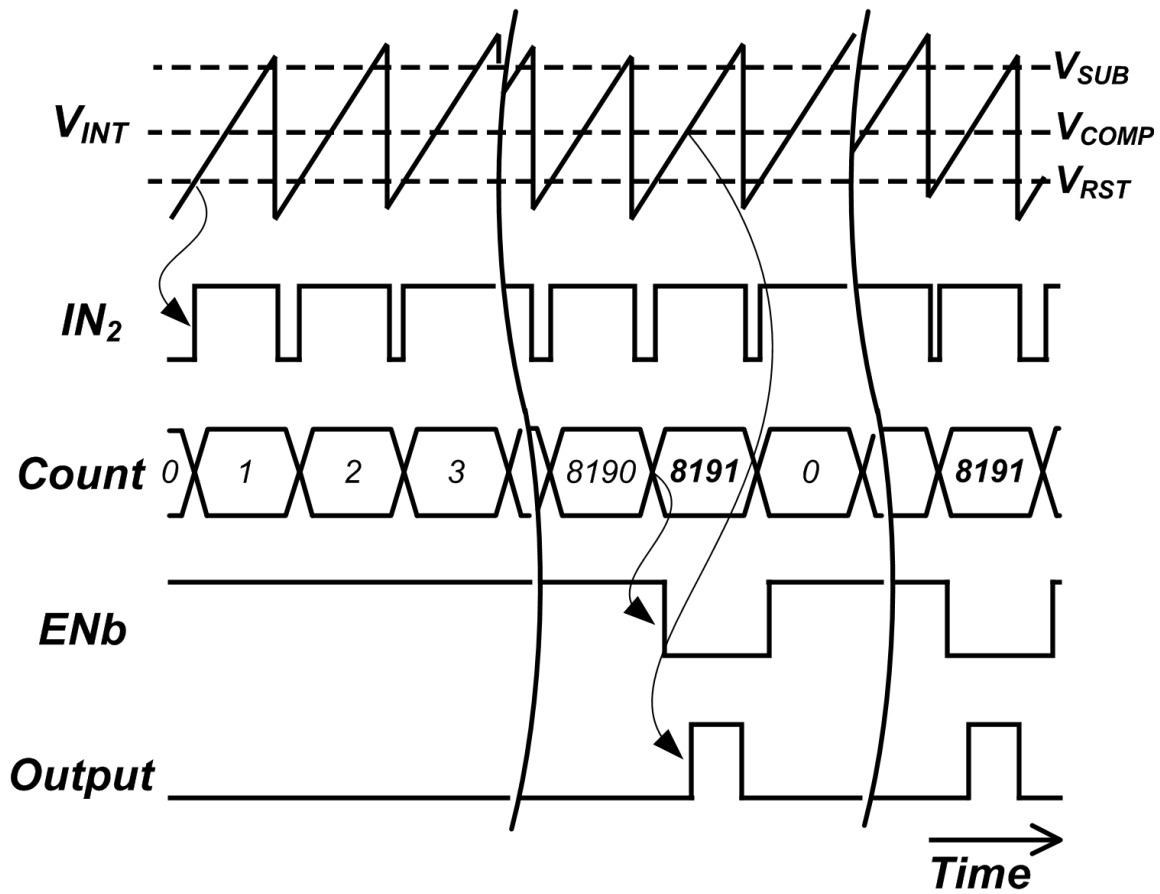
Figure 3.8: A timing diagram that shows an example scenario of a wake-up signal generation with 13-bit counter configuration.
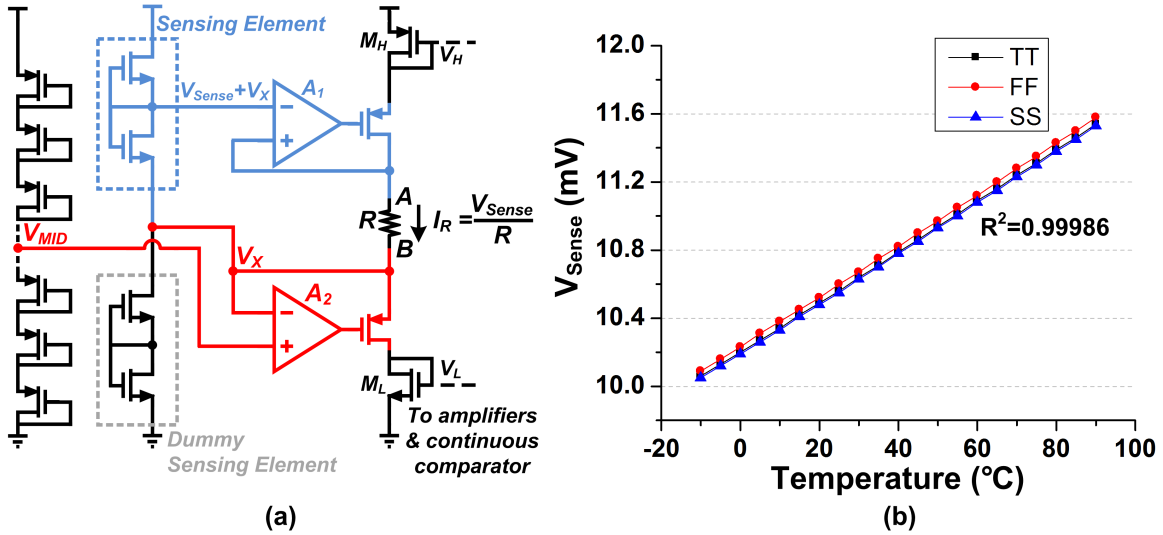
Figure 3.9: (a) A reference current (I_{REF}) generator and (b) simulation results of the sensing element across different corners.

dynamic power. In order to minimize leakage current, D flip-flops are designed with high threshold voltage (HVT) devices. Figure 3.8 provides a timing diagram for the generation of a wake-up signal. When reset is released, the counter counts subtraction cycles. When the counter reaches a preset value, which is equal to 8191 ($=2^{13}-1$) in this case, power gate (ENb) is released. As a result, the comparator is activated just before wake-up and generates a wake-up signal. The counter operates based on the trigger of reset (IN_2) rather than the trigger of subtraction (IN_1) to prevent false triggering of the continuous comparator during start up. Also, the continuous comparator is disabled after subtraction to prevent output glitching. At the same time, the counter resets to 0 and begins to count again for the next wake-up cycle.

3.3.4 Reference Current and Voltage Generator

The reference current (I_{REF}) is generated with a temperature-to-voltage sensing element (V_{Sense}) along with a voltage to current (V-I) converter and a resistor [48] (Figure 3.9a). The sensing element consists of two normal NMOS transistors and the output voltage shows a linear proportional to absolute temperature (PTAT) characteristic while consuming 11pW. Temperature independent current can be generated by applying V_{Sense} across a resistor when the first-order temperature coefficients of the two are matched. Therefore, the sensing element has been sized to match the first-order temperature coefficient of the resistor. The output voltage of the sensing element must

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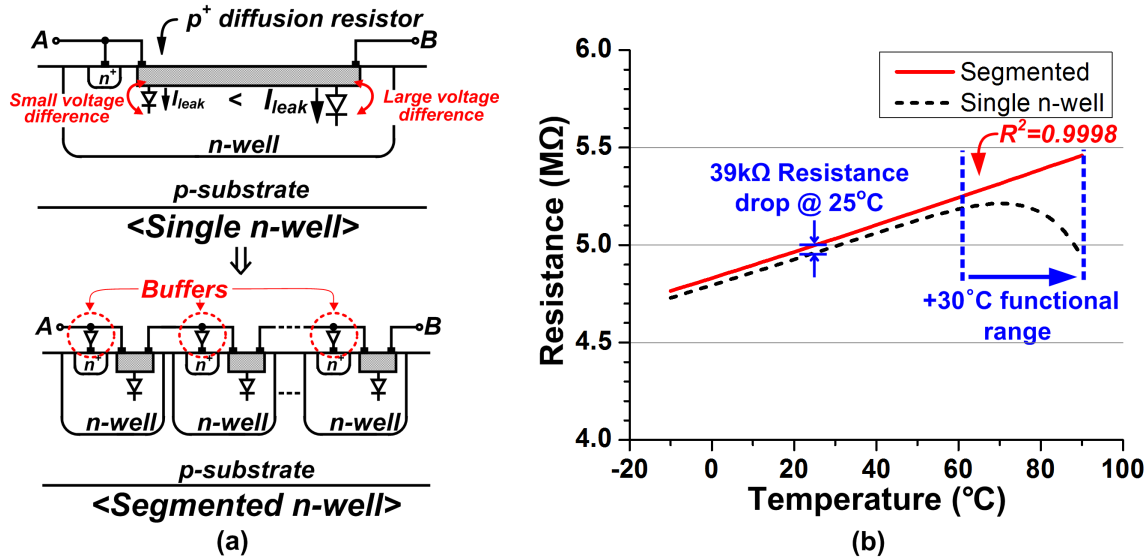
Figure 3.10: (a) A segmented self-biased diffusion resistor and (b) its effect at high temperatures.

be kept $> 3\sim4V_T$ to maintain highly linear behavior over temperature [48], generating temperature insensitive currents. In this work, the output voltage has been reduced to 10mV for low power operation at the expense of temperature insensitivity (8ppm/°C of average degradation after 1k Monte Carlo simulations). A negative feedback loop consisting of an amplifier (A_1) and PMOS transistor ensures that the voltage across the resistor tracks V_{Sense}. The second feedback loop along with the diode stack is used to boost output voltage of the sensing element by V_{MID} (=VDD/2) to obtain effective common mode voltage of A_1. This also allows the inclusion of M_L at the bottom of the current generation path, enabling V_L to be directly generated from I_R. A dummy sensing element is added between node V_X and ground to provide a current path for the main sensing element. This helps to suppress undesired current in the main current generation path. The amplifiers use a 2-stage topology and are designed to have $>$100dB of open-loop gain over the targeted temperature range while consuming 120pW (simulated results). The resistor is a 5MΩ p+ diffusion resistor. In the chosen process, diffusion resistors show highly linear behavior against temperature, which enables accurate compensation. However, in low current applications, junction leakage in the resistor degrades linearity at high temperature. As only $\sim$2nA flows through the resistor nominally, the 10× increase in junction leakage from 25°C to 90°C (to 212pA) causes a non-negligible change in total resistor current.

One way to reduce junction leakage is to minimize the voltage difference across the junction. In

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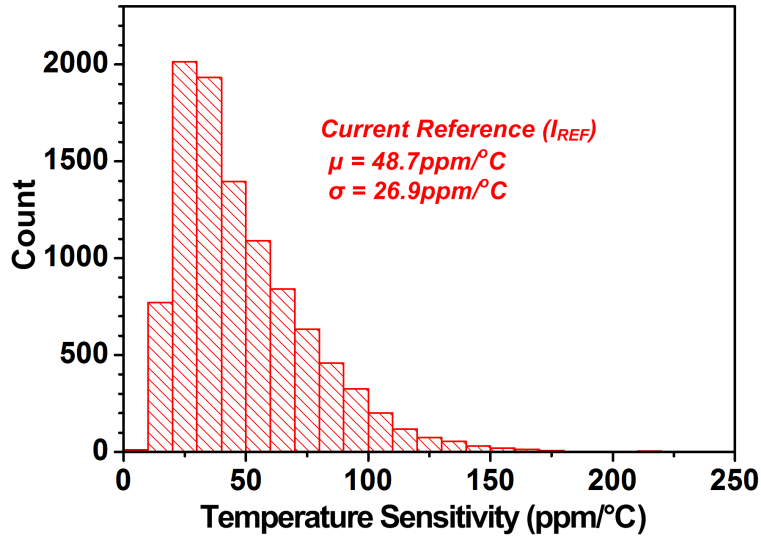
Figure 3.11: Monte Carlo simulation results of reference current (I_{REF}).

previous work, an n+ diffusion resistor is used in which the voltage difference cannot be controlled as it forms a junction with the p-substrate. We therefore use a p+ diffusion resistor to segment the resistor into separate n-wells and tie them to intermediate points to minimize the voltage difference. This solves the leakage problem between two regions but raises a similar problem between n-well and p-substrate. Isolation of n-well to p-substrate leakage can be achieved through biasing segmented n-wells through buffers (Figure 3.9b). Buffers are designed for 1mV offset (10k Monte Carlo simulations), limiting frequency error below 0.02%. Through this technique the functional temperature range increases from 0-60°C to 0-90°C at a 6.1% area penalty and 500pW additional power from the well-biasing buffers (Figure 3.10). It can be seen that even at room temperature junction leakages causes the effective resistance to be lower than the designed value. Based on 10k Monte Carlo simulations, reference current I_{REF} shows an average temperature sensitivity of 48.7ppm/°C with a standard deviation of 26.9ppm/°C (Figure 3.11).

The temperature-independent voltage source used in this work is shown in Figure 3.12a. Its architecture is based on a 4T voltage reference [19]. The basic idea of this structure is to use opposite temperature coefficients of the threshold voltage (V_{th}) and the thermal voltage (V_T) to achieve a temperature-insensitive output voltage. In this work, native and I/O NMOS transistors are used to maximize threshold voltage difference. This helps to achieve required output voltage ($\sim$550mV) with minimum number of 2T voltage reference stacks. A conventional 4T voltage reference shows
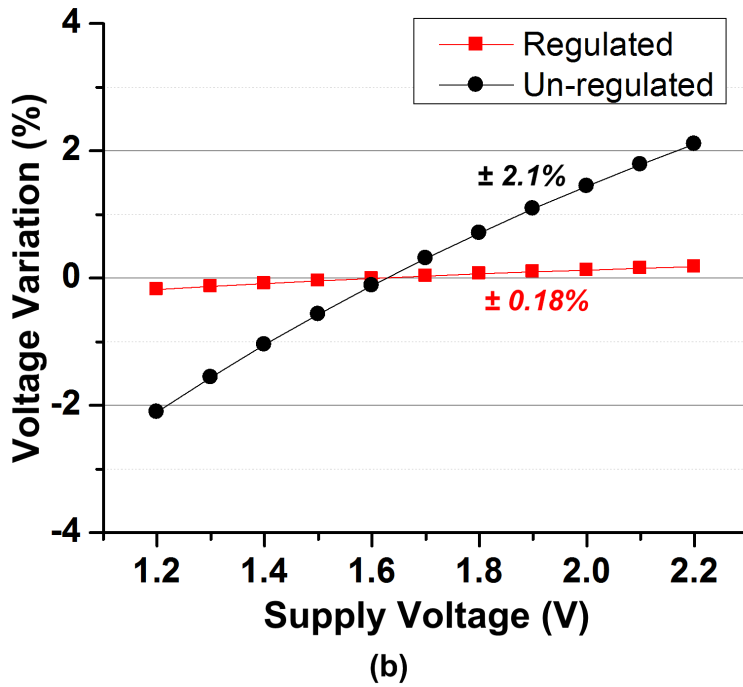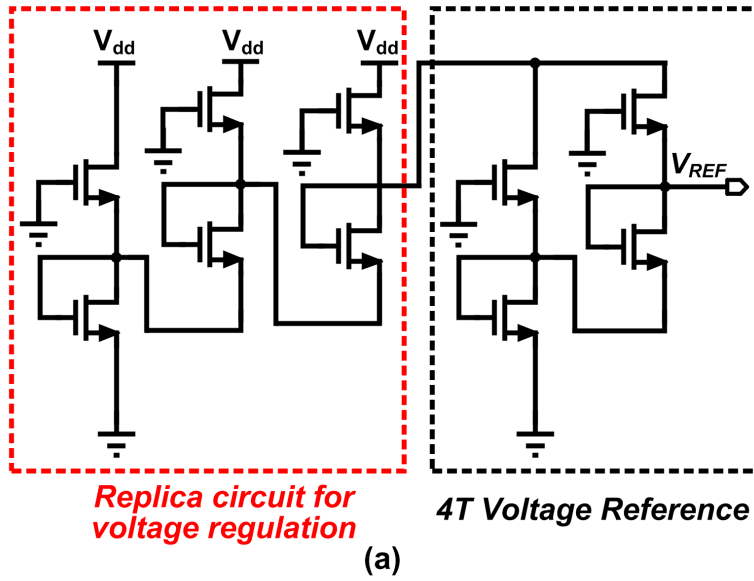
Figure 3.12: (a) Voltage reference with locally regulated supply voltage and (b) its simulated line sensitivity.
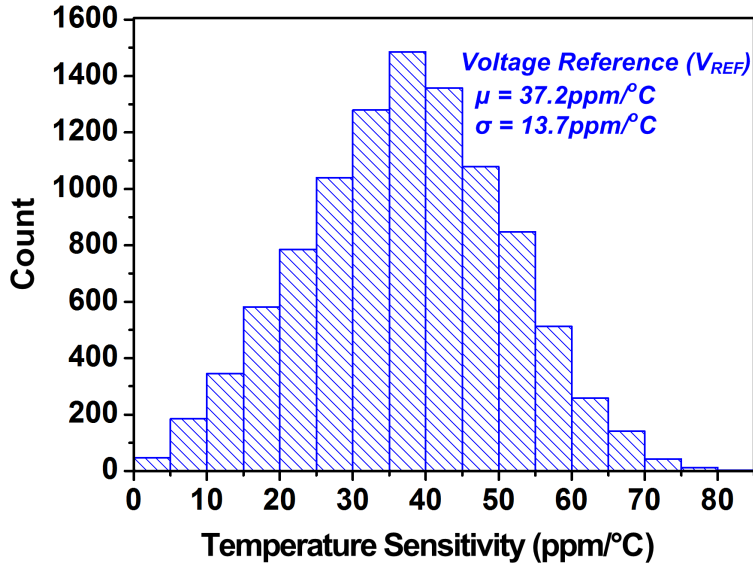
Figure 3.13: Effect of process variations and mismatch on reference voltage (V_{REF}).

2.1% of supply voltage sensitivity across 1.2V to 2.2V in simulation (Figure 3.12b). Major source of error is drain induced barrier lowering (DIBL) effect. The supply sensitivity can be improved by taking an advantage of its low power operation. As only ∼50pA is consumed in the voltage reference, a replica circuit can be designed to provide a regulated voltage to the original circuit while consuming only 300pW. When a sufficient amount of current is supplied, there is negligible effect on the temperature characteristics. Line sensitivity improves by 11.7× after regulating the local supply voltage in this way. Figure 3.13 shows the effect of process and mismatch on the temperature characteristics of the voltage reference. Based on 10k Monte Carlo simulations, the average temperature coefficient is 37.2ppm/°C with standard deviation of 13.7ppm/°C.

3.4 Measurement Result

The proposed wake-up timer is implemented in 0.18m CMOS. Figure 3.14 shows measured stability results across temperature. Operating at 11Hz, measured temperature sensitivity is 45ppm/°C from -10 to 90°C (48ppm/°C average across the 5 dies). Figure 3.15 shows the supply sensitivity of the output frequency from 1.2V to 2.2V. The variation is less than 1%/V. The sensing element in the reference current generator is the major source of error. Measured Allan deviation [49] demonstrates long-term stability (Figure 3.16). As averaging time increases, frequency fluctua-

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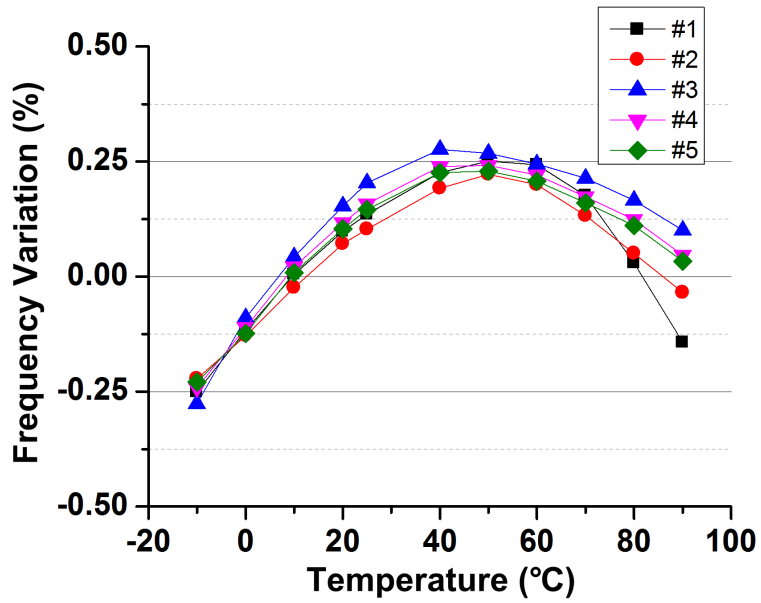
Figure 3.14: Measured temperature stability of the timer.
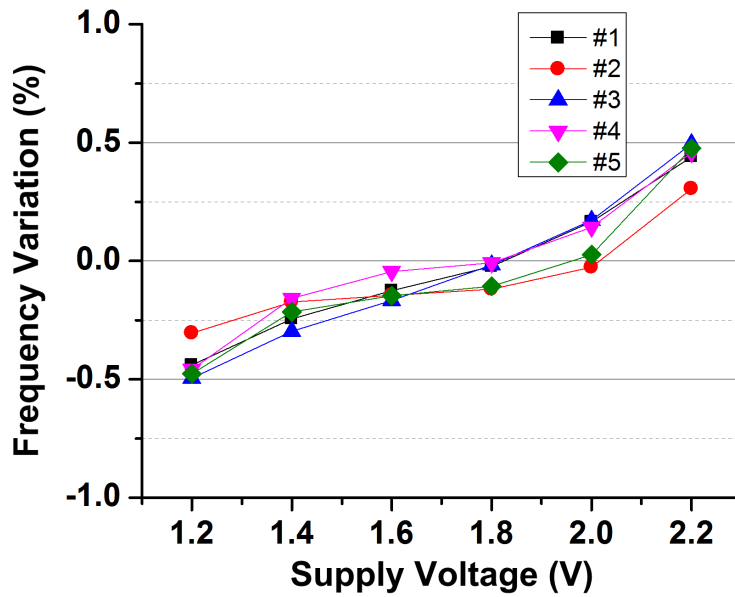
Figure 3.15: Measured line sensitivity of the timer.
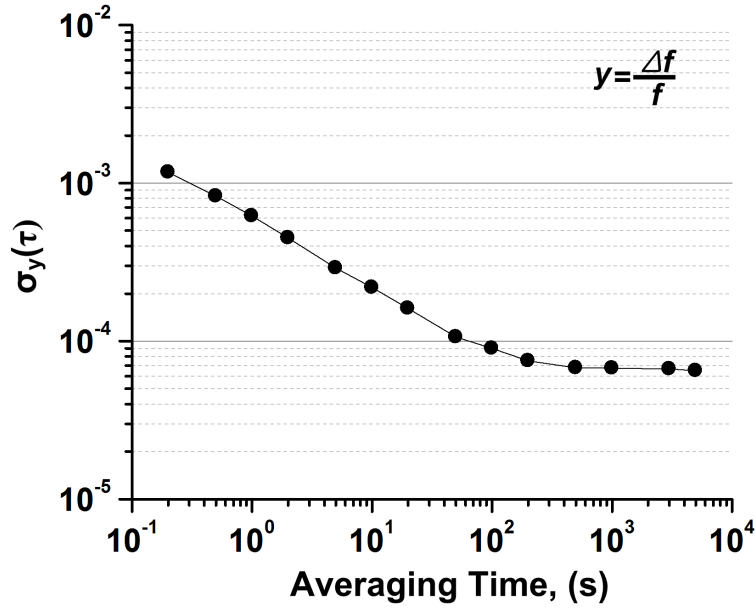
Figure 3.16: Measured Allan Deviation of the timer.

tions decrease as white noise is averaged out until flicker noise dominates and timer performance saturates ($\sim$10mins).

Average power consumption of the timer strongly depends on the wake-up interval of the accurate continuous comparator. Figure 3.17 shows measured average power as a function of wake-up interval. As wake-up interval increases, average power consumption decreases rapidly. Even for wakeup intervals of just 1s, average power remains below 10nW and saturates within 1% of 5.8nW after 50sec. Figure 3.18 provides a breakdown of power consumption across the measured temperature range (1.2V supply, 12 minute wake-up signals). Due to the proposed approach, the continuous comparator power is a negligible portion of total average power consumption ($<$1%). Amplifiers and the continuous comparator show only a small increase in power with temperature due to the current reference (I_{REF}) biasing, while the reference current generator dominates power at high temperatures due to constant voltage biasing of amplifiers. Figure 3.19 shows measured waveforms of V_{INT}, V_{CAP}, and timer output signal with a 10-bit counter configuration. It can be seen that subtraction and charging operation is well-performed without any stabilization issue. The die photo of the test chip is shown in Figure 3.20 with an active area of 0.24mm^2. Table 3.1 compares state-of-art low-power on-chip oscillators ($\leq$ kHz range, $<$10μW). The proposed timer occupies a portion of the design space that had not been previously reported. It can be seen that

Figure 3.17: Measured average power consumption with different wake-up intervals.
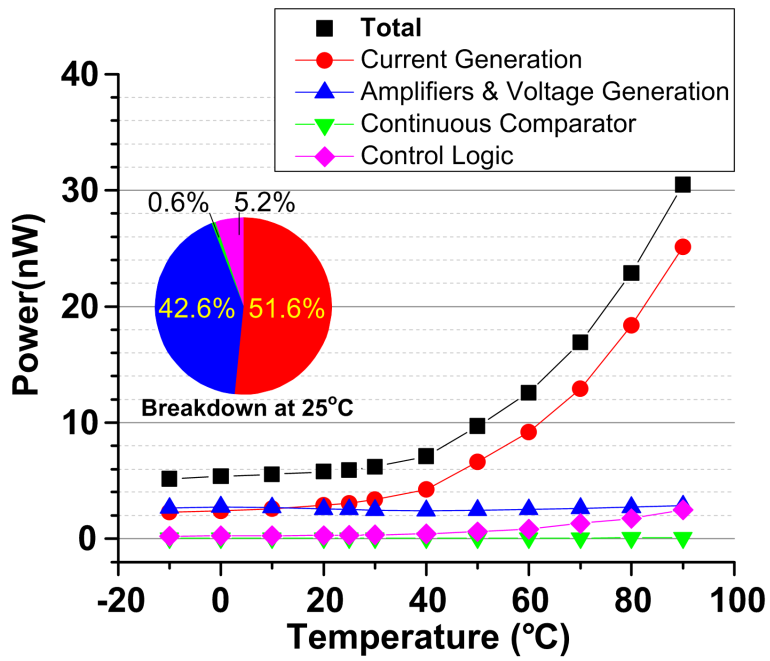
Figure 3.18: Breakdown of average power consumption across the measured temperature range.
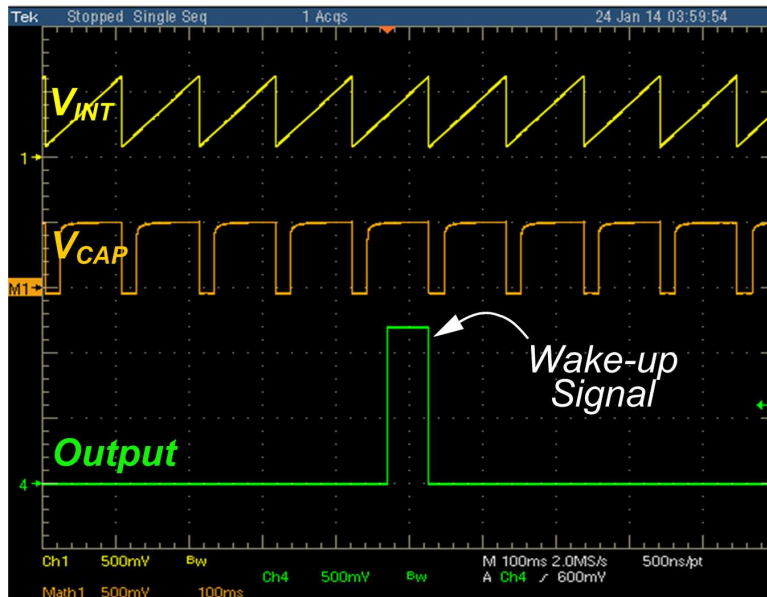
Figure 3.19: Measured waveform of V_{INT}, V_{CAP}, and Output signal.
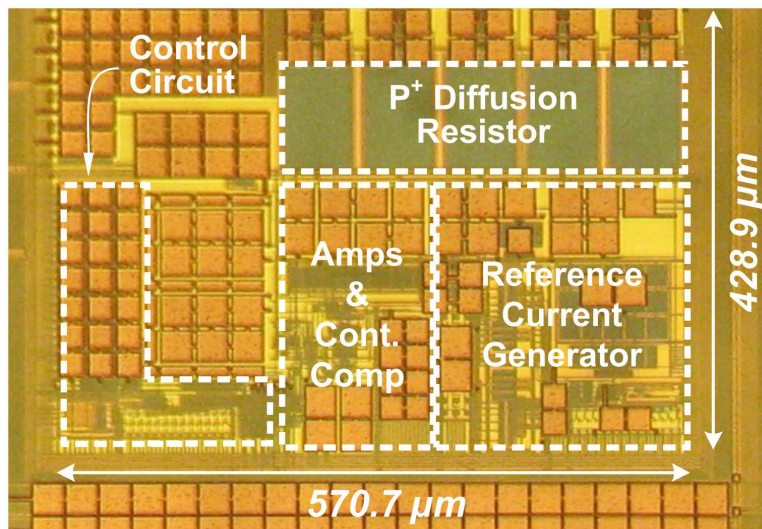
Figure 3.20: Microphotograph of the test chip in 0.18μm CMOS.

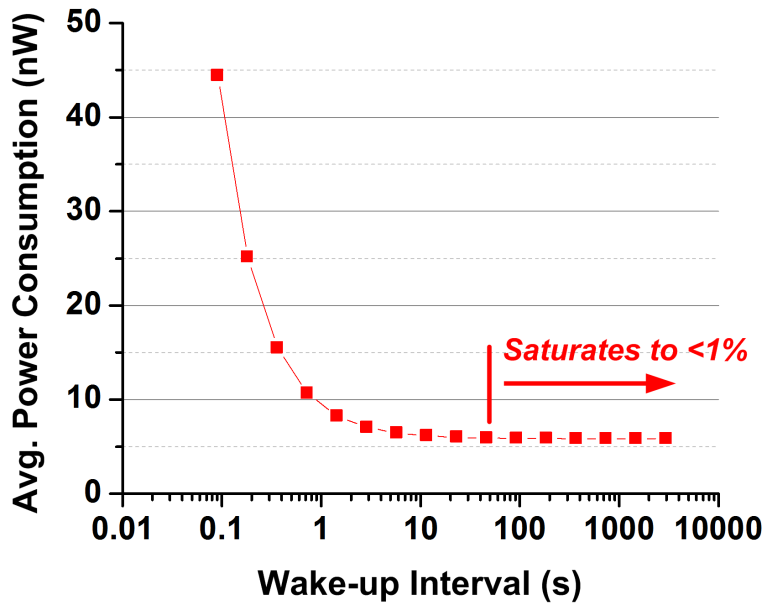|	This Work	CICC'07 [41]	JSSC'13 [42]	ISSCC'09 [43]	ISSCC'13 [35]	ISSCC'14 [38]	VLSI'12 [37]	VLSI'12 [36]
Process	180nm	130nm	130nm	130nm	65nm	65nm	90nm	60nm
Area	0.24mm^2	0.0005mm^2	0.015mm^2	0.02mm^2	0.032mm^2	0.015mm^2	0.12mm^2	0.048mm^2
Frequency	11Hz	0.08Hz	0.37Hz	11Hz	18.5kHz	33kHz	100kHz	32.8kHz
Temperature Range	-10–100°C	0–80°C	-20–60°C	0–90°C	-40–90°C	-20–90°C	-40–90°C	-20–100°C
Temperature Coefficient	45ppm/°C	1600ppm/°	375ppm/°C[1] (31ppm/°C[2])	490ppm/°C	38.5ppm/°C	38.2ppm/°C	104ppm/°C	32.4ppm/°C
Line Sensitivity	1%/V @1.2–2.2V	75%/V @0.4–0.5V	490%/V @1.15–1.25V 420%/V @0.65–0.75V	40%/V @0.55–0.6V	1%/V @1.4–3.3V	0.09%/V @1.15–1.45V	9.3%/V @0.725–0.9V	0.125%/V @1.6–3.2V
Power Consumption	5.8nW	0.12nW	0.66nW[1] (N/A)[2]	0.15nW	120nW	190nW	280nW	4.48μW

[1]Without a temperature sensor
[2]With 10 point calibration using a temperature sensor. Power number with the sensor not available

Table 3.1: Performance summary and Comparison with previous low power timers.

the timer achieves comparable temperature and voltage insensitivity to timers in the 100nW range while consuming sub-10nW.

3.5 Conclusion

This work describes a wake-up timer that can be used in compact wireless sensors. A low-power topology using a constant charge subtraction scheme is proposed. To avoid using a very large resistance, the proposed architecture uses voltage and current references in the architecture. Two op-amps act to repeatedly subtract a constant amount of charge. Since the generated sawtooth waveform is independent of subtraction time, a low-power clocked comparator is used for triggering the subtraction. The final precise wake-up signal is generated by triggering a higher power accurate continuous comparator. The proposed topology separates the continuous comparator from the oscillation path and activates it only for short period when it is required. As a result, both low power tracking and generation of precise wake-up signal is made possible. The timer consumes 5.8nW at room temperature from a 1.2V supply voltage. Temperature sensitivity of 45ppm/°C from -10 to 90°C and supply sensitivity of 1%/V from 1.2V to 2.2V is achieved.

CHAPTER 4

A 120nW 8b Sub-ranging SAR ADC with Signal-Dependent Charge Recycling for Biomedical Applications

4.1 Introduction

Interest in wireless sensor networks has grown recently with ongoing research on low power circuit designs. Application scope of theses sensor nodes include medical devices for continuous monitoring of biomedical signals (ExG) [50], surveillance using audio or image sensors , and environmental monitoring such as temperature and pressure [51]. One of the key component that enables these applications is an analog-to-digital converter. Improvements in their energy efficiency helps sensor nodes to meet their power constraints.

In the sensor nodes, most straightforward and safe way to acquire signal using an ADCs is to set its performance to meet the maximum signal range and resolution. However, a lot of sensor node signals show a varying requirement for input range and resolution over time. One example of such signal is an ECG signal. When closely observed, it shows low activity for most of the time which means that its short term variation is small (Figure 4.1a). Code variation in this range is only 2.7 % of the full code range. It can be also seen that a burst of high activity occurs within a short time window (Figure 4.1b). This QRS complex occupies only 12% of R-R peak interval. Another example of sensor node data with a similar characteristic is ambient temperature profile, as shown in Figure 4.2 for Ann Arbor. As you can see, Ann Arbor has about 53 Celsius of temperature variation throughout the year. However, temperature variation within a single day is only 7.2
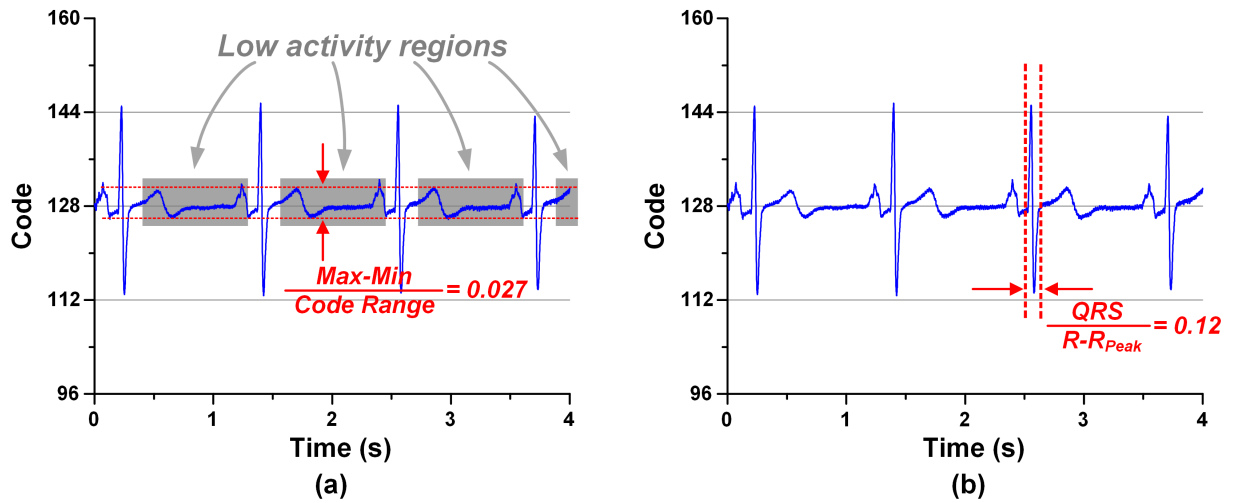
Figure 4.1: Example sensor node data - ECG signal.
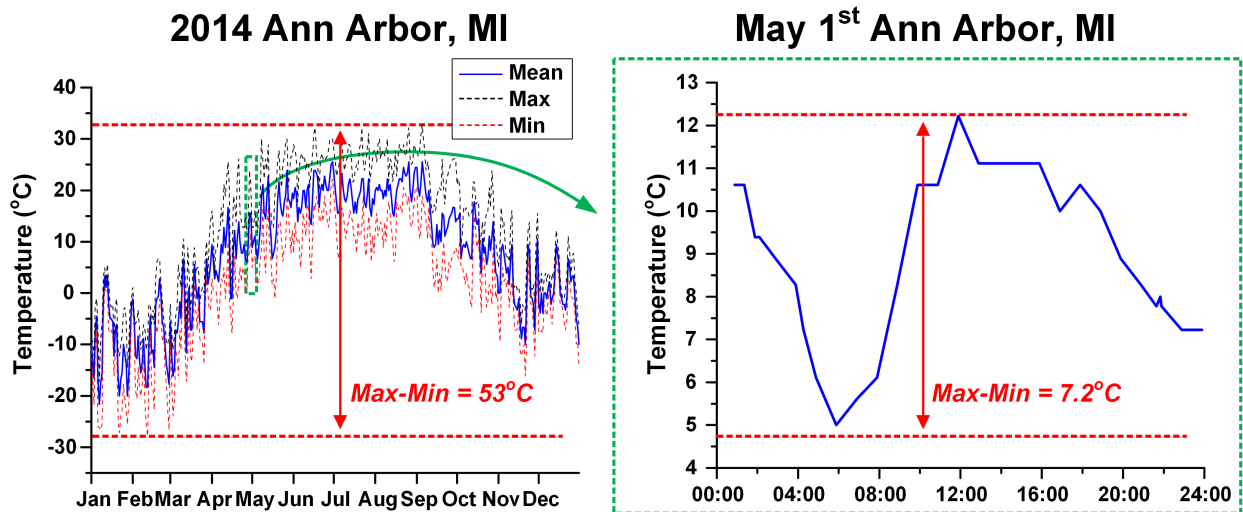
Figure 4.2: Example sensor node data - An ambient temperature profile.

Celsius. And, of course, temperature variation in the minute range will be even smaller. Hence, constantly providing full resolution across the maximum range for the ADC is clearly wasteful and sensor node data with these characteristics provide an opportunity for power reduction.

SAR ADC has been commonly used for sensor node data acquisition due to their low power consumption and high energy efficiency. However, conventional SAR operation does not take an advantage of these aforementioned signal characteristics: 1) Low activity for the majority of the time, i.e., short-term signal variation is small; 2) Long-term signal variation is wide; and 3) Bursts of activity occasionally occur within a short time period, such as a neuron spike. For a N-bit ADC, it always operates through N cycles in a binary fashion. Binary search itself is an efficient algorithm, but the question is whether we could take an advantage of the mentioned signal characteristics and do even better.

Several recent works were proposed to achieve this goal. A bypass window technique [52] uses switching sequences that skip several conversion steps when the signal is within a predefined window. LSB-first approximation [53] uses LSB first in the binary search algorithm. It uses the prior conversion result as an initial guess. Then, bit cycling begins from least significant bit instead of most significant bit. Another approach [54] modulates sampling rate according to signal activity. However, a predefined window cannot track a signals low activity region while the LSB-first approximation toggles MSBs in the DAC every cycle for an initial guess, which limits the obtainable power gain and consuming energy. Modulated sampling rate puts burden and increases complexity in the digital signal processing block to perform FFT/DFT.

In this work, a sub-ranging ADC that uses a moving window and stores the previous MSBs voltage value on a series capacitor is introduced. This enables the MSBs of the CDAC to be held fixed in subsequent cycles. Due to the large MSB capacitors size, substantial energy is saved in the CDAC as well as the comparator and logic. Energy savings are signal dependent; the approach was applied to 39 actual ECG recordings and showed 2.6$\times$ energy savings while fully preserving arrhythmia detection accuracy.
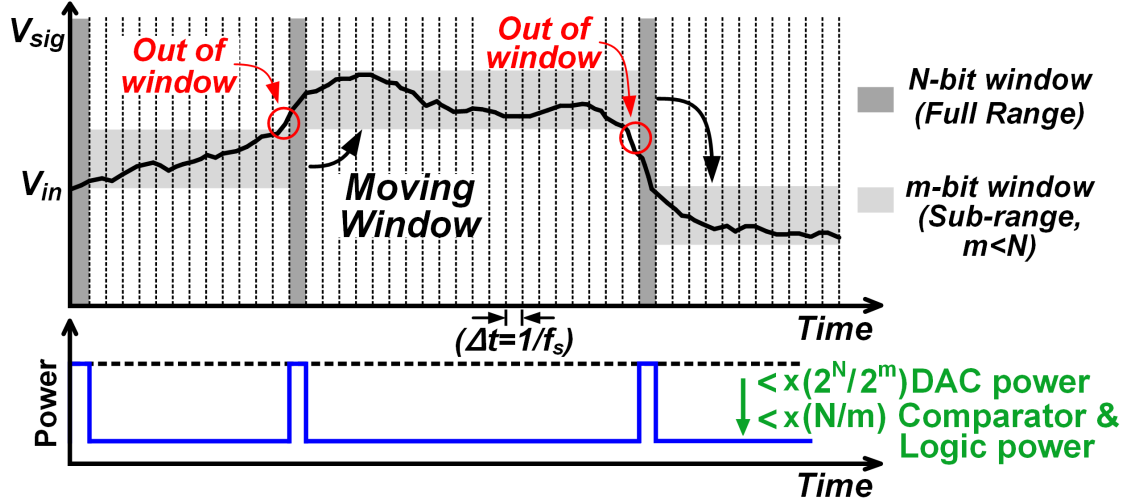
Figure 4.3: Proposed data-dependent moving window concept.

4.2 Proposed Circuit

Figure 4.3 describes the conceptual operation of the proposed N-bit ADC. After an initial N-bit full conversion, a small m-bit sub-ranging window is set for subsequent conversions based on the conversion result. This is done by storing the MSB information, in terms of voltage, on a series capacitor. Then, if signal activity is low and stays within the window, only m-bit conversion is performed by switching only the LSB capacitors, skipping conversion cycles for m MSBs, to get an output code. As time passes and the signal deviates from the sub-range window, another full conversion takes place to adjust the sub-ranging window. In this case, the failed conversion can be either skipped or replaced by an interpolation between its two neighboring values. With this approach, unnecessary energy consumption from MSB switching can be saved as well as comparator and logic energy.

4.2.1 Overall Architecture

The architecture is similar to the conventional SAR ADC except for a series capacitor (C_{MSB}) between CDAC and comparator (Figure 4.4a). C_{MSB} is used to store the voltage corresponding to the most significant m-bits (V_{MSB}) from the previous sample (Figure 4.4b). If the next sample falls within the same sub-ranging window, energy to switch the MSB capacitors reduces dramatically (by $16\times$ for 4 MSBs in an 8-bit SAR) while comparator and logic energy reduces linearly with the

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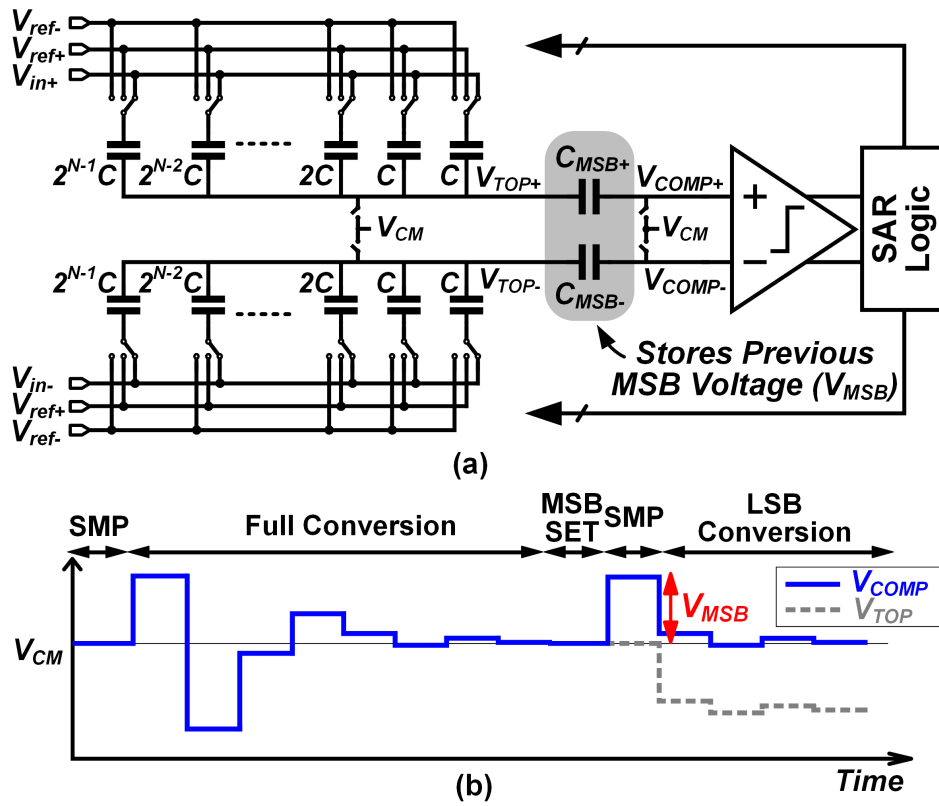
Figure 4.4: (a) Proposed architecture of sub-ranging SAR ADC and (b) operation of MSB recycling.

number of MSBs stored due to reduced conversion cycles. As explained before, the ADC switches back to full-range mode for one cycle to re-acquire the signal when the signal goes out of the predefined window.

4.2.2 CDAC operation

Figure 4.5 shows detailed ADC operation. A single ended version will be used for simplicity although the actual implementation is in differential. In this structure, the green box shows that a 4-bit capacitor array can be formed with the series MSB capacitor being a unit capacitor. Note that unit capacitance is 8 times larger than the unit capacitor of the full 8 bit array.

In MSB configuration phase (MSB phase 1), the bottom plate of the m-bit capacitor array is configured based on the MSBs state of the previous conversion. At the same time, top plates are connected to V_{CM}. Here we show a case where the previous MSBs were 1000. The bottom plates of the capacitors are connected to V_{ref+} and V_{ref-}, accordingly. Resulting net charge (Q) stored in the m-bit capacitor array can be expressed as follows:

$$Q = Q_{1,M}(V_{CM} - V_{ref+}) + (C_{T,M} - C_{MSB} - C_{1,M})V_{CM} \tag{4.1}$$

where $C_{1,M}$ is sum of all capacitance connected to V_{ref+} and $C_{T,M}$ is sum of capacitance of the m-bit capacitor array. The unselected 4 capacitors in the DAC are pre-charged during this phase. This is to prevent the bottom plate voltage from going below ground due to capacitive coupling in the following phases.

In the beginning of phase 2, top plate and unselected capacitors gets disconnected from V_{CM} and V_{ref-}, respectively. Then, all of the selected m-bit capacitors are connected to V_{ref-} for charge redistribution. As a result of charge conservation, the m-bit MSB voltage of the previous sample is stored across C_{MSB} (Equation 4.2).

$$V_{MSB} = V_{COMP} - V_{TOP} = \frac{C_{1,M}}{C_{T,M}}V_{ref+}. \tag{4.2}$$

After the C_{MSB} is set, the input signal is sampled, which is done identically to a conventional SAR where all of the bottom plates are connected to V_{in} while top the top plate is connected to V_{CM}. Resulting V_{COMP} can be expressed as follow as a result of voltage shift.

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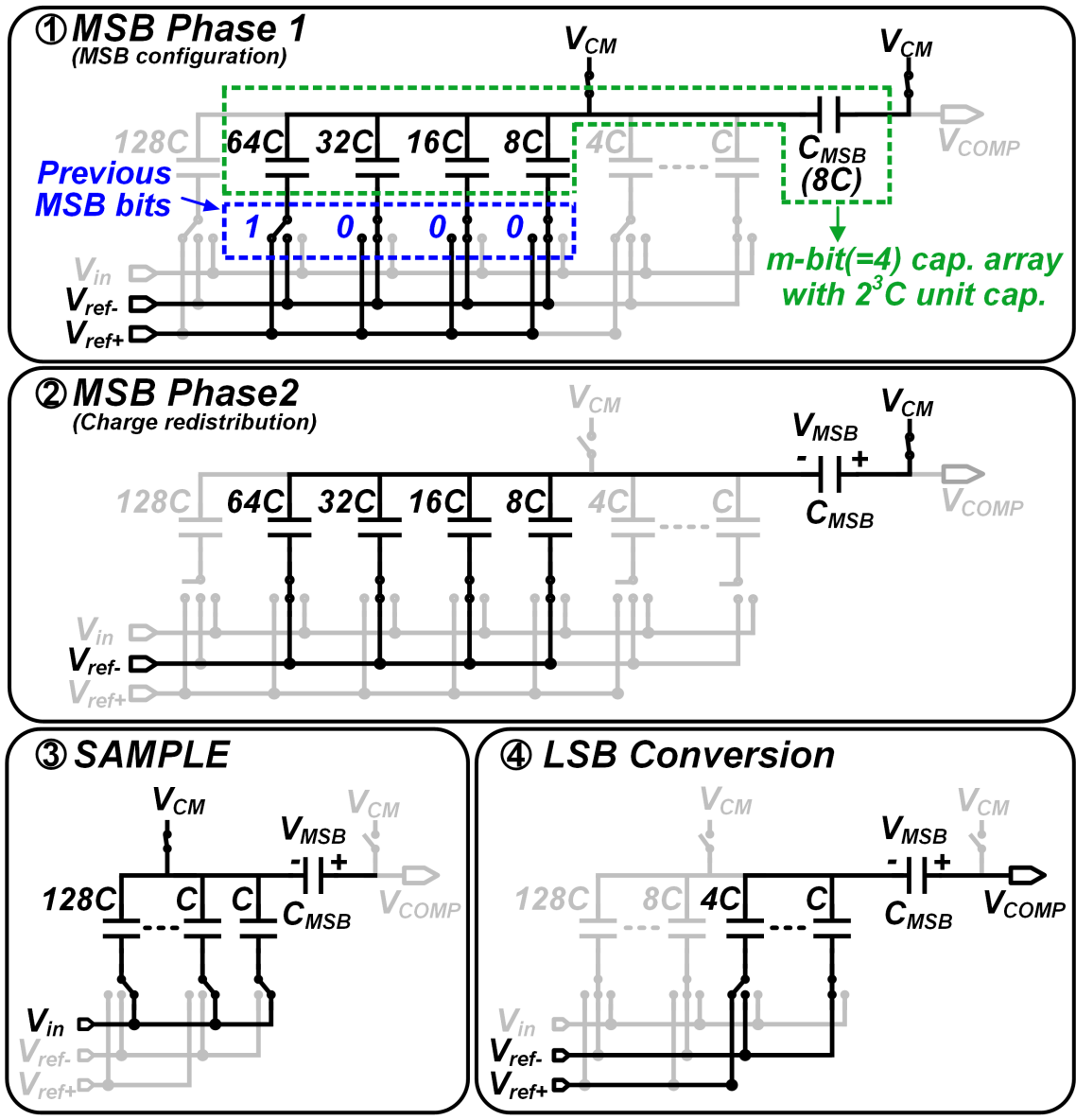
Figure 4.5: Sub-ranging procedure using capacitive DAC.
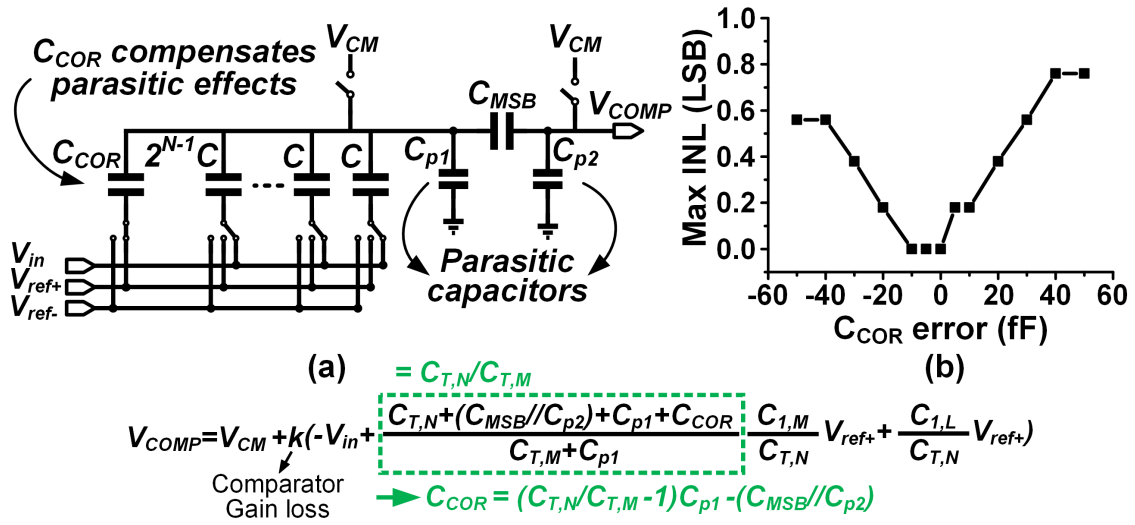
Figure 4.6: (a) Correction capacitor (C_{COR}) for parasitic compensation and (b) effect of correction error on linearity in simulation.

$$V_{COMP} = V_{CM} + \frac{C_{1,M}}{C_{T,M}} V_{ref+} \qquad (4.3)$$

Following LSB search phase is also identical to the conventional approach, except that only LSBs are computed. During this LSB conversion, the comparator input voltage, V_{COMP}, can be expressed as follows:

$$V_{COMP} = V_{CM} + (-V_{in} + \frac{C_{1,M}}{C_{T,M}} V_{ref+} + \frac{C_{1,L}}{C_{T,N}} V_{ref+}) = V_{CM} + (-V_{in} + \frac{\frac{C_{1,M}}{C_{T,M}} C_{1,M} + C_{1,L}}{C_{T,N}} V_{ref+}) \quad (4.4)$$

where $C_{1,L}$ is sum of all capacitance connected to V_{ref+} and $C_{T,N}$ is the sum of capacitance of the N-bit capacitor array during LSB conversions. It can be seen that there is a term reflecting the MSB configuration and a term reflecting the LSB conversions. This conversion process is identical to the conventional SAR approach SAR as the MSB part is scaled up properly. Since total charge at node V_{COMP} remains constant, the voltage across C_{MSB} always returns to V_{MSB} at the end of conversion, enabling reuse of the MSB information.

4.2.3 Error Correction

Until now, the effect of parasitic capacitors has been ignored. However, there exist two parasitic capacitors C_{p1} and C_{p2} on both side of the series capacitor in the proposed architecture. Due to these parasitic capacitances, the stored charge will not be scaled correctly during LSB conversions. This causes non-uniformity between different sub-ranging windows. This issue can be solved by introducing a correction capacitor (C_{COR}), Figure 4.6a). C_{COR} is connected to V_{ref-} during LSB conversions to cancel out this scaling error and is connected to V_{ref+} in MSB phase 1 for pre-charging. The right value of the correction capacitor can be found by computing previous equations 4.1 – 4.4 again while considering two parasitic capacitor C_{p1} and C_{p2}. Resulting equations can be expressed as follows

$$V_{COMP} = V_{CM} + k(-V_{in} + \frac{C_{T,N} + (C_{MSB}//C_{p2}) + C_{p1} + C_{COR}}{C_{T,M} + C_{p1}} \frac{C_{1,M}}{C_{T,N}} V_{ref+} + \frac{C_{1,L}}{C_{T,N}} V_{ref+}), \quad (4.5)$$

where k is a comparator gain loss. Similar to the case without parasitic capacitors, scaling factor must be equal to a ratio between the full-N-bit array capacitance and m-bit sub-range array capacitance (Equation 4.6).

$$\frac{C_{T,N} + (C_{MSB}//C_{p2}) + C_{p1} + C_{COR}}{C_{T,M} + C_{p1}} \frac{C_{1,M}}{C_{T,N}} = \frac{C_{T,N}}{C_{T,M}} (= 2^{N-M}). \quad (4.6)$$

As a result, correct value for the correction capacitor can be found as follows:

$$C_{COR} = (\frac{C_{T,N}}{C_{T,M}} - 1)C_{p1} - (C_{MSB}//C_{p2}). \quad (4.7)$$

When C_{COR} is correctly set, the conversion process becomes immune to parasitic capacitances. Simulated INL across C_{COR} error shows that linearity is relatively insensitive to the absolute value of C_{COR} (Figure 4.6b).

4.2.4 Conversion Algorithm

The overall operation is shown in Figure 4.7. When the signal stays within the sub-ranging window, it will cycles through the inner loop consisting of only Sample and LSB conversion.
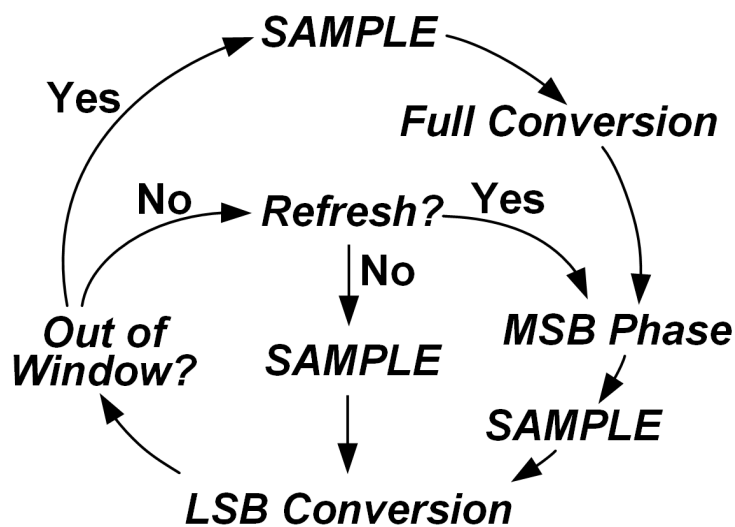
Figure 4.7: Conversion Algorithm.

However, in this case, leakage on the series MSB capacitor (C_{MSB}) can cause errors after a certain period of time. To prevent this, a refresh rate is set to restore the MSB voltage (V_{MSB}) periodically. The refresh rate has been designed to be variable from 0 to 63 cycles for flexibility. Therefore, the rate can be optimized to maximize energy savings depending on the environment (e.g., temperature). When the conversion result is out of the sub-range, an error flag is set and C_{MSB} is reset in the subsequent full-range conversion.

4.2.5 Energy Optimization

Total energy consumed by the proposed ADC depends on the number of MSBs (m) that are stored on CMSB for sub-ranging (Figure 4.8). As m increases, pre-charge energy for the unused capacitors goes down as well as comparator, DAC, and logic energy due to fewer cycles for conversion. However, energy and frequency of storing the MSB voltage increases. Simulation showed a minimum operating energy when m is 4 bits. Note that energy is consumed for storing MSB and pre-charging only when the signal is out of the sub-ranging window (3.7% of total cycle during ECG detection). The selection of the unit capacitance in the m-bit capacitor array also impacts energy. A lower capacitance is preferred to reduce energy during MSB configuration, but comparator energy increases due to the need to compensate for gain loss arising from the series connection of C_{MSB} and C_{p2}.
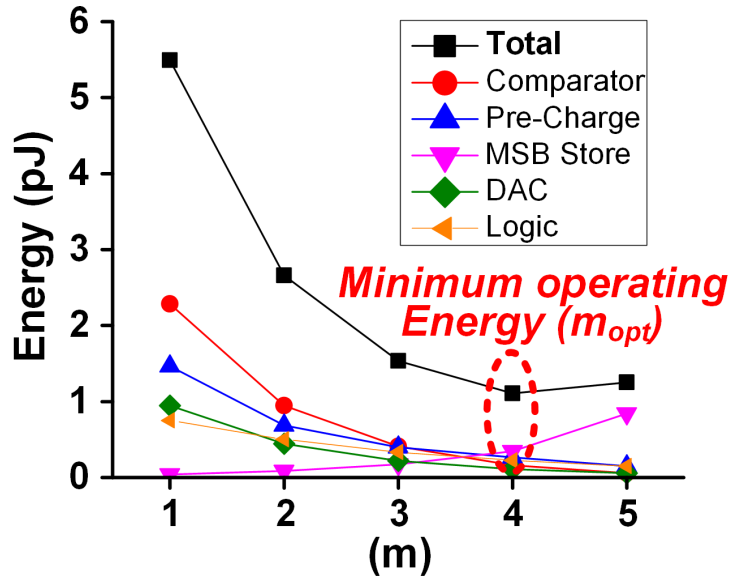
Figure 4.8: Simulated energy consumption versus stored MSBs (m).

4.2.6 Comparator Design

The ADC uses single stage, StrongARM regenerative latch based comparator for ultra-low power operation. 3-sigma offset of ±40mV is calibrated with binary sized 4bit capacitors at the comparator outputs. CDAC is composed of metal-oxide-metal (MOM) capacitors with unit capacitance of 4.5fF

4.3 Measurement

The test chip is fabricated in 0.18μ m CMOS with an area of 0.12mm^2. The proposed design is tested at 100kS/s and operates from a single 0.6V supply voltage. Measured DNL and INL are +0.3/-0.3 LSB and +0.6/-0.6 LSB, respectively (Figure 4.9). Systematic error due to sub-ranging can be observed at every 16th code as 4-bit MSB storage are being used. Figure 4.10 shows the measured power spectrum. Measured SNDR and SFDR are 46.9dB and 63.8dB, respectively.

As this ADC is targeted for biomedical applications, ECG data was used to check its effectiveness for this application. ECG waveforms were collected from 39 un-discriminated patients that were referred to the University of Michigan hospital for diagnosis and treatment of atrial fibrillation. Measured data from an ECG simulator is shown for both conventional and proposed ADC
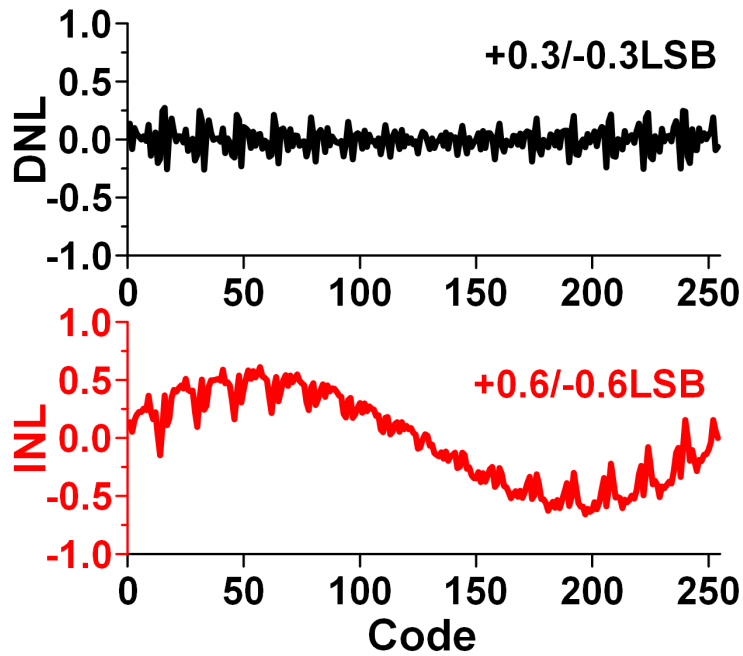
Figure 4.9: Measured DNL and INL.
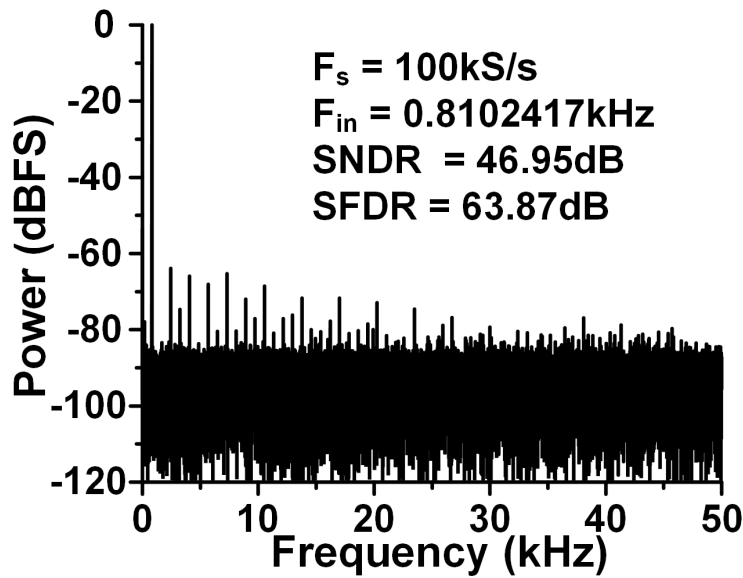
Figure 4.10: Meausred FFT of ADC output data.
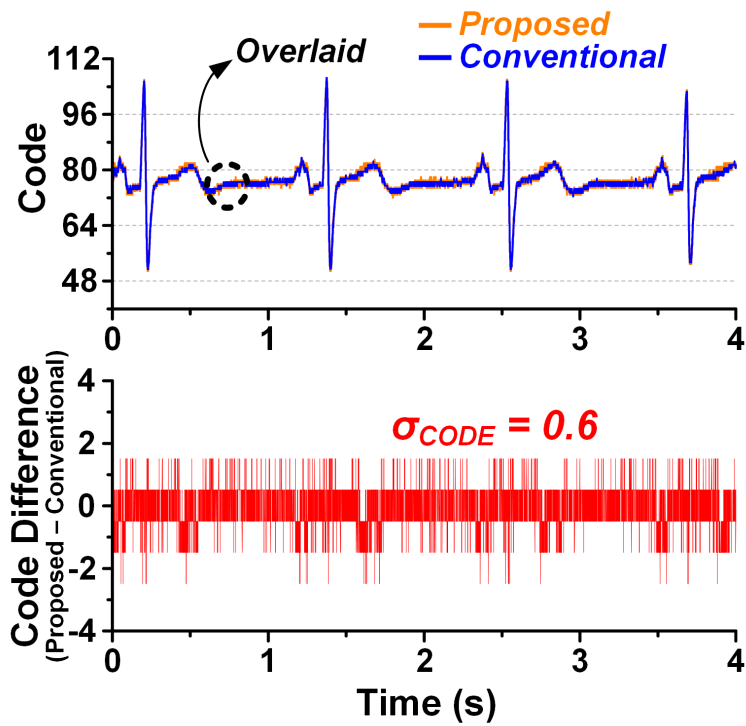
Figure 4.11: Measurement result with ECG simulator sampled at 8kHz.
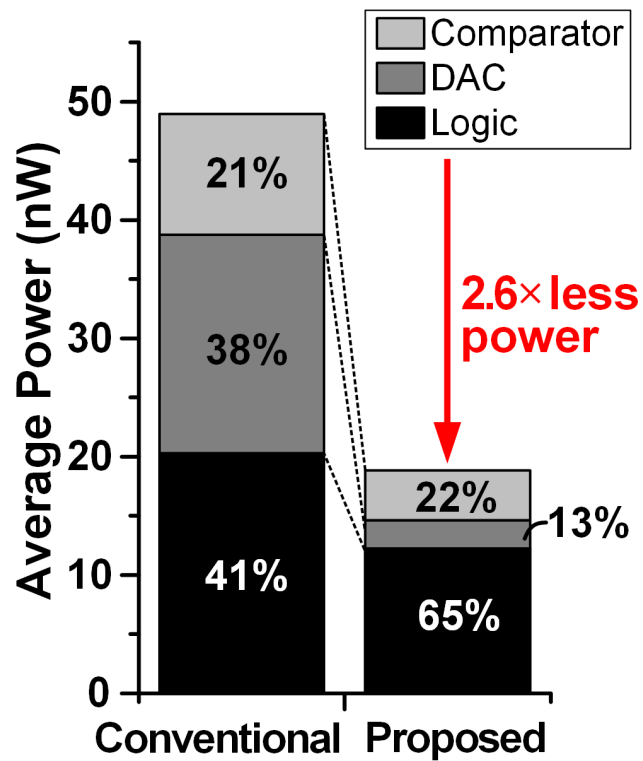
Figure 4.12: Power comparison against conventional 8b SAR ADC
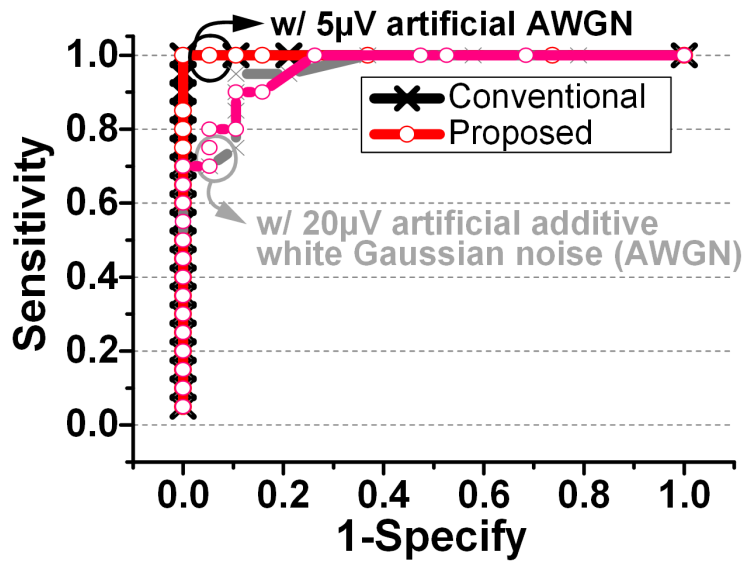
Figure 4.13: Accuracy of classification using atrial fibrillation detection algorithm [56]

(Figure 4.11). When aligned, it can be seen that there is a negligible data loss. Standard deviation of the code difference is measured to be 0.6 codes. When the power consumption is compared, the proposed approach reduces power by $2.6\times$ compared to an 8-bit conventional approach (Figure 4.12). As expected, most of power reduction is from the DAC energy which is diminished by $7.6\times$. However, merely comparing a code difference does not fully verify the proposed ADCs usefulness. Since the primary purpose of the ECG monitoring is detecting arrhythmia, atrial fibrillation detection is also evaluated.

Frequency Dispersion Metric algorithm has been used to evaluate a detection accuracy [56]. This algorithm performs atrial fibrillation detection in the frequency domain. For a normal patient, clear dominant frequency and harmonics can be seen since peaks are generated at approximately constant intervals. However, for a patient with abnormal rhythm, a single dominant frequency is less prominent and more dispersion is observed. Therefore, the arrhythmia can be detected by inspecting the variance of intervals. Resulting error rate of the conventional and proposed ADC with different noise level is shown in Figure 4.13. Here, the X-axis is the true negative rate and the Y-axis is true positive rate, and each point corresponds to a threshold. The line parallel to Y-axis, imply that there is a threshold existed without any error in detection. Other line parallel to X-axis, imply there is at least one false alarm when all the a-fib arrhythmia is detected for any possible threshold. Therefore, it can be seen that there is no performance degradation for both conven-

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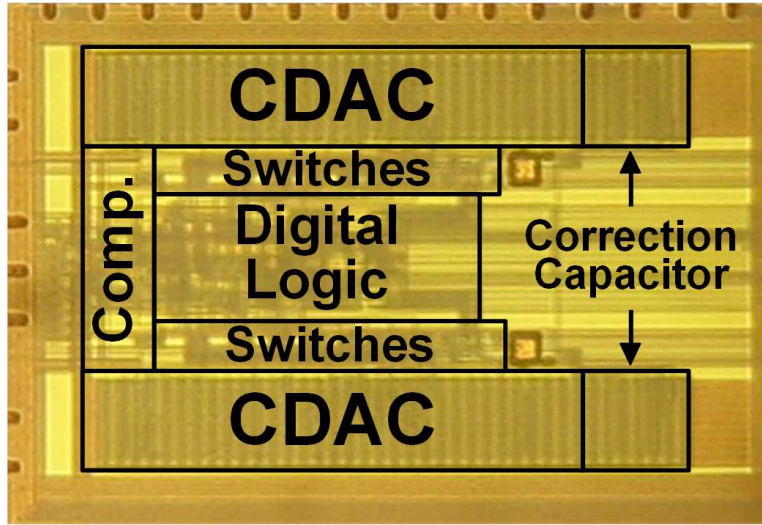
Figure 4.14: Die micrograph

	This Work	JSSC'12 [52]	JSSC'2014 [53]	TCAS1'11 [54]	ISSCC'11 [55]
Technology	180nm	180nm	180nm	180nm	65nm
Area [mm^2]	0.12	0.08	0.12	0.96	0.21
Supply Voltage[V]	0.6	0.6	0.6	0.7	0.55
Sampling Rate[kS/s]	100	200	16	50	20
Resolution [bit]	8	10	10	8	8
Power [nW]	120	1040	47-170*	25000	146
ENOB [bit]	7.5	9.3	9.7	6.9	7.5
FOM [fJ/conv-step]	6.6	8.03	3.5-20*	4186	40

*For best(DC) and worst case (Full Nyquist sinusoid) inputs

Table 4.1: Performance summary and comparisons.

tional and proposed ADC with $5\mu V_{rms}$ input referred noise. A case with $20\mu V_{rms}$ noise level is also shown. Performance degradation is observed and detection accuracy drops. However, classifier output is of a proposed ADC remains similar to the conventional ADC, indicating negligible accuracy degradation with proposed approach, indicating the potential of this approach for biomedical applications.

Figure 4.14 shows the chip micrograph. Table 4.1 summarizes this work and compares against state-of-art SAR ADCs with similar application focus.

4.4 Conclusion

A sub-ranging SAR ADC for biomedical applications is presented that uses modified capacitive DAC to save energy by taking advantage of signal characteristics. Measurement results with actual ECG signal showed that the proposed ADC achieves $2.6\times$ energy saving compared to conventional approach while maintaining its accuracy. This shows the potential of this approach for biomedical and other application areas.

CHAPTER 5

A 12nW Always-On Acoustic Sensing and Object Recognition Microsystem using Frequency-Domain Feature Extraction and SVM Classification

5.1 Introduction

IoT devices are becoming increasingly intelligent and context-aware. Such context-awareness has been enabled by equipping various types of sensors that are 'always-on'. In the past, sensors on mobile platforms were activated periodically or passively by the user to avoid draining battery power. As a result, information on surroundings or activity was limited making them far from being 'ambient intelligent'. On the other hand, recent mobile devices in the market are distinguished by their always-on functionality while adopting full spectrum of sensors, ranging from accelerometers, gyroscopes, magnetometers to acoustic, image and pressure sensors. Among these various sensory inputs to realize context-aware intelligence, sound is an attractive sensory modality that is information-rich but not as computationally demanding as other alternative modalities such as vision. It can bee seen that the usage of always-listening technology has become quite popular and can be easily found in these days (e.g., iPhone Siri, Galaxy S-voice, and Amazon Echo). New applications of always-on intelligent acoustic sensing includes agricultural monitoring to detect pests or precipitation, infrastructure health tracking to recognize acoustic symptoms, and security/safety monitoring to identify intruders or dangerous conditions.

A major impediment for the adoption of always-on, context-aware sensing is power consump-
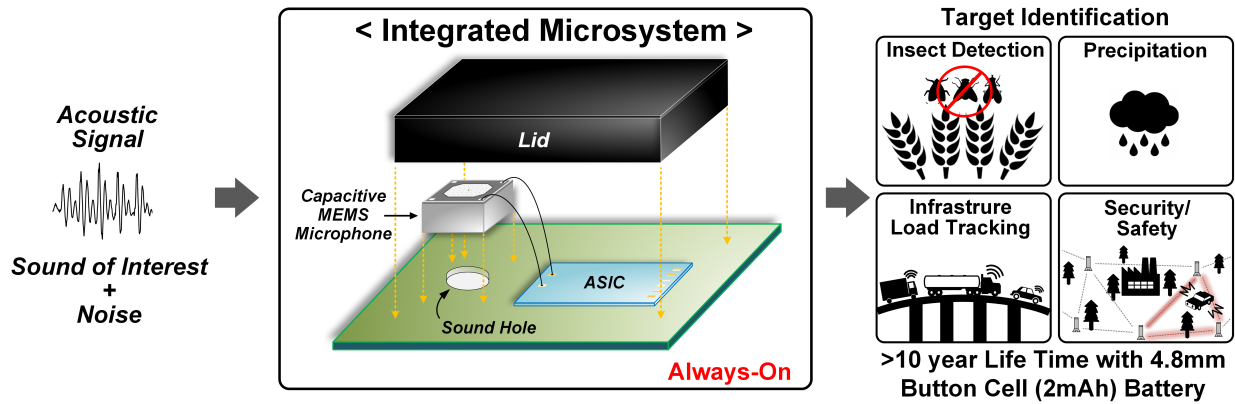
Figure 5.1: Example usage scenario of proposed always-on acoustic sensing and object recognition microsystem.

tion, particularly for ultra-small IoT devices requiring long-term operation without battery replacement. To sustain operation with a $1mm^2$ solar cell in ambient light (100lux) or achieve a lifetime of 10 years using a button cell battery (2mAh), <20nW power consumption must be achieved. Current state-of-the-art acoustic sensing systems [57][58] show power consumption in the μW range which is more than 2 orders of magnitude higher than the target. More broadly a previous ULP signal acquisition IC [59] consumes just 3nW while 64nW ECG monitoring system [60] includes back-end classification, however there are no sub-20nW complete sensing systems with both analog frontend and digital backend.

5.2   System Overview

This work reports an ultra-low power acoustic sensing microsystem that continuously monitors its environment and identifies an event of interest (Figure 5.1). To satisfy stringent power budget without compromising event identification accuracy, we introduce 1) a MEMS microphone integrated in-package with the rest of the electronics to provide a low capacitance interface, 2) an ULP 8-bit SAR-ADC exploiting a unique DAC topology with extremely small ($\leq$50fF) input capacitance to enable sufficient gain-bandwidth product for a frontend amplifier with nW-level power consumption, 3) a serialized discrete Fourier transform (DFT) feature extraction performed only on the discrete tones-of-interest (ToI) to avoid a high-power/area-consuming conventional FFT, and 4) a power efficient classification engine using a programmable support vector machine (SVM).

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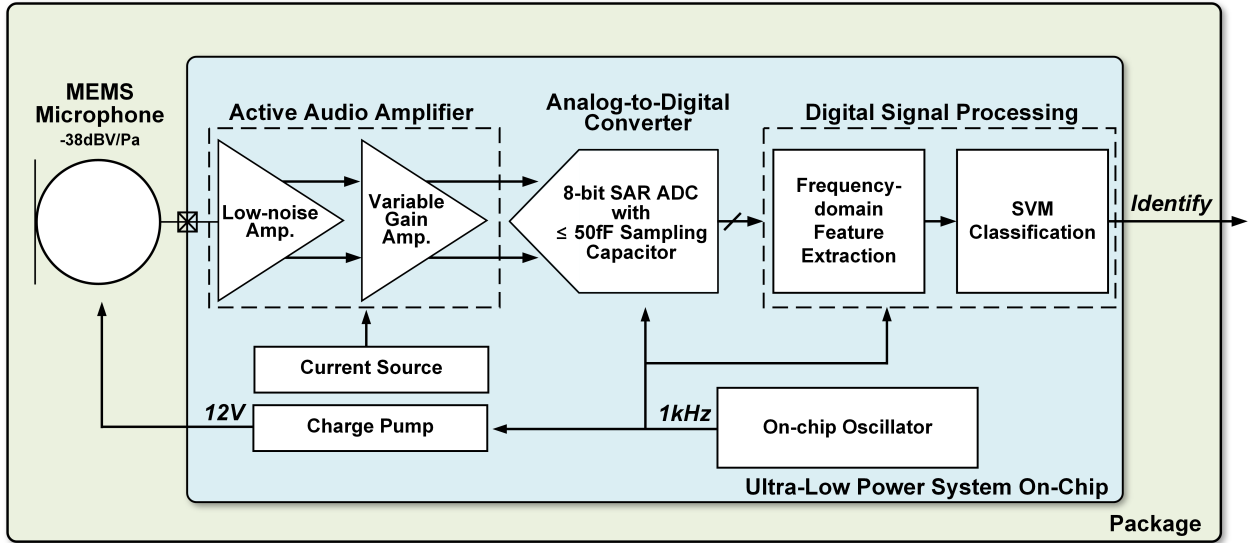
Figure 5.2: Block diagram of the proposed system.

We observe that the target acoustic features are often concentrated within $\leq$0.5kHz bandwidth, allowing a $\leq$1kHz clock for all active components. This low frequency is one of the key factors enabling always-on sensing with 12nW power consumption. A complete system is demonstrated with reliable ($>$95%) object recognition accuracy.

Overall block diagram of the proposed system is shown in Figure 5.2. The datapath of the system consists of a capacitive MEMS microphone, an active audio amplifier, an analog-to-digital converter (ADC) and a digital signal processing unit. Other peripheral circuits include a current source, a charge pump and an on-chip oscillator. For system integration, custom printed circuit board (PCB) is used to minimize the wirebonding length and avoid signal degradation from parasitic capacitance on MEMS-ASIC connection. For packaging, 3D printed lid is used to cover both MEMS and ASIC which provides a back chamber for the MEMS device. Size of the lid (1.4mm$\times$1.4mm) has been chosen so that entire system can fit in to a 4.8mm coin cell battery.

Typically, a capacitive MEMS microphone alone is able to produce approximately 38dBV / Pa sensitivity with SNR larger than 70dB under a 12V$\pm$2V bias voltage with 94dBA (1Pa SPL) sound input without any amplification. As a result, the overall microphone SNR is often dominated by the noise of the electronics. Figure 5.3 shows a relationship between the bias voltage and the overall power consumption of the amplifier and the charge pump. Power estimation of an amplifier assumes 3dB SNR at the amplifier output, noise efficiency factor (NEF) of 2.0 and

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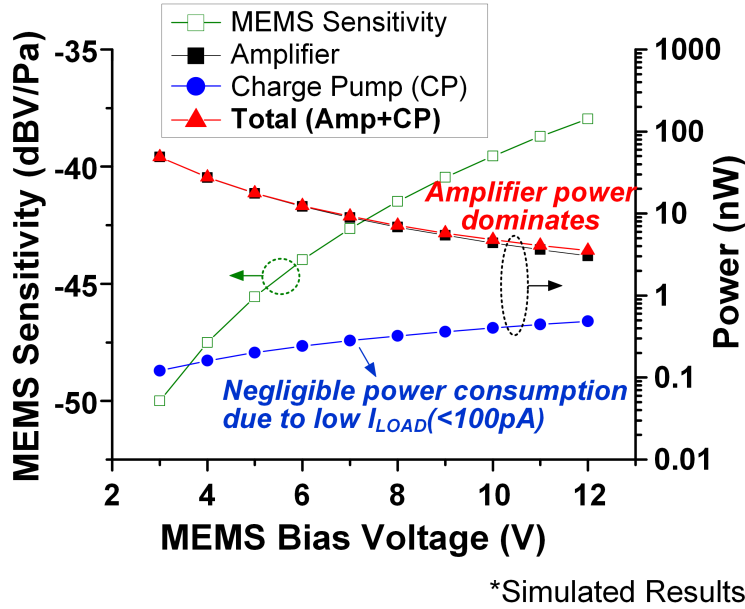
Figure 5.3: Power versus MEMS bias voltage.

500Hz bandwidth. For the charge pump, Dickson charge pump architecture is assumed in power estimation where its power consumption increases linearly with the output voltage. On the other hand, increasing bias voltage helps to reduce power consumed by the amplifier as it alleviates the noise constraints. Since the capacitive MEMS microphone is a passive device, there is a negligible load current ($<$100pA) on the charge pump output. Thus, the charge pump can operate at low frequency while consuming 100s of pWs. Overall power consumed by the amplifier and the charge pump decreases with increased bias voltage as the increase in charge pump power consumption is negligible. In this work, the bias voltage close to the MEMS microphone pull-in voltage (13~14V) has been used.

5.3 Analog Frontend

5.3.1 Amplifier

A system analysis reveals that overall SNR is limited by the first-stage amplifier. To achieve high noise efficiency, the amplifier uses a current-reuse topology. The current consumption of the amplifier is set to 3nA to meet the SNR requirement at the lower bound of the target sound
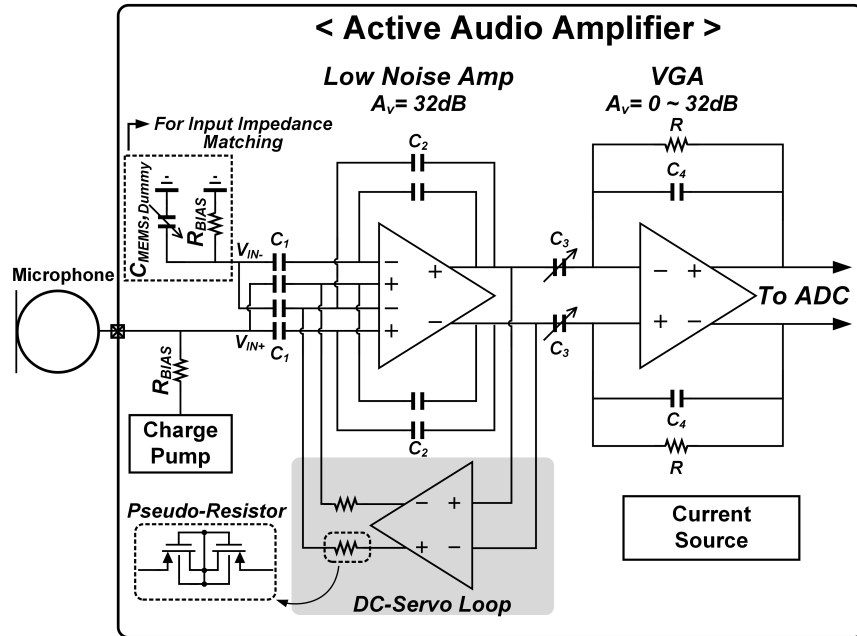
Figure 5.4: Detailed diagram of an active audio amplifier.

pressure level (SPL) of 40dB (equivalent to a very quiet room). Given the resulting gain-bandwidth product, a closed-loop gain of 32dB can be achieved while meeting the target signal bandwidth (0.5kHz). A telescopic structure is used to provide sufficient open-loop gain (>70dB in simulation) to minimize gain nonlinearity errors. Furthermore, P- and N-MOS input transistors are separately biased, increasing headroom and thereby output swing to preserve linearity over the entire dynamic range (0.4%THD at 95dB SPL). A DC servo-loop compensates for DC offset to prevent saturation and sets the high-pass corner to ≤20Hz, covering the low end of the MEMS input frequency range.

The second stage is bandwidth limited, and hence its current consumption is directly impacted by the load capacitance. This motivates the extremely low input loading capacitance (≤50fF) of the proposed ADC, allowing the second stage bias current to be reduced to 100s of pAs.

5.3.2   Analog-to-Digital Converter

Figure 5.5 shows the proposed 8-bit SAR ADC with a new, low input capacitance DAC topology. In low resolution (<10b) SAR ADCs, the unit capacitance of the binary DAC array is usually limited by mismatch rather than kT/C noise. For the 180nm technology used in this work, 4fF unit capacitance is required to maintain worst-case DNL (3σ) of <1LSB (10k Monte Carlo runs),
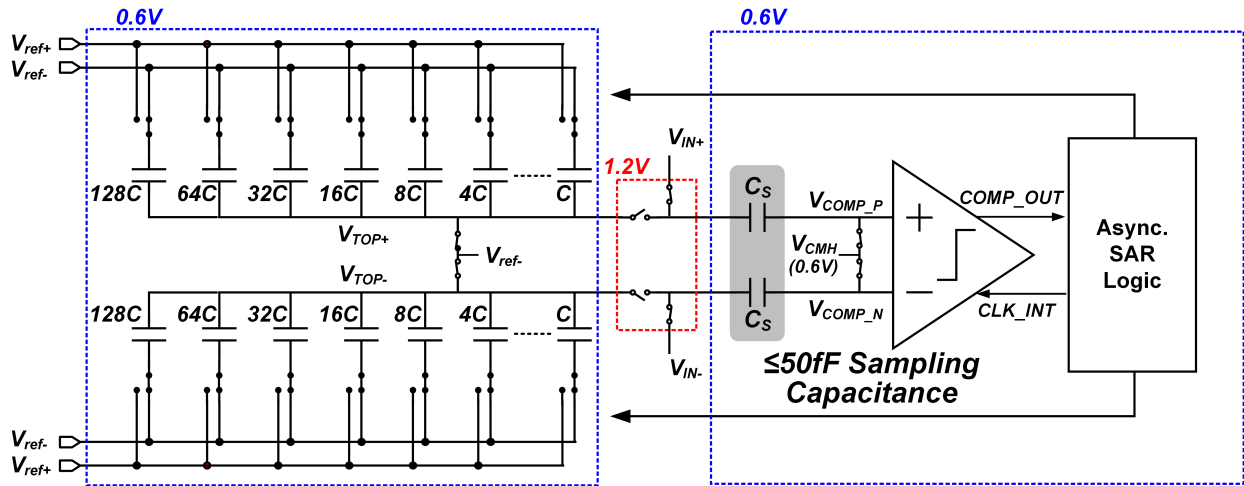
Figure 5.5: Proposed 8bit SAR ADC with low sampling capacitance ($\leq$50fF).

which translates into 1pF of load capacitance. This would require the preceding VGA to consume >10nA to achieve the required performance (32dB gain, settling within 1LSB at 1kHz sampling rate). To overcome this trade-off, we separate the sampling capacitor (C_s) from the capacitive DAC. During the sampling phase, the DAC is disconnected from Cs and purges all of its charge while the input is sampled on Cs. At the beginning of the bit-cycling phase, the DAC top plate (V_{TOP}) is connected to Cs, and the rest of the conversion process is identical to a conventional approach due to charge conservation on node V_{comp}. This proposed scheme creates comparator gain loss and gain error (12.6% and 8.5% after PEX, respectively) compared with the conventional approach. However, comparator gain loss is acceptable in an 8-bit configuration as comparator power is not dominant while gain error causing LSB reduction does not degrade SNR as it is limited by the amplifier. A timing diagram of the ADC is shown in Figure 5.6. ADC operates asynchronously to avoid high speed clock and save power. An on-chip oscillator is used to generate ADC clock ($\sim$1kHz). Sampling time has been designed to be tunable from 50% to 90% of the entire clock period with 10% step by combining different phases of the clock. The ADC operates at 0.6V to reduce power. Since the amplifier operates at 1.2V, the common-mode voltage is shifted during the sample and hold phase to match the dynamic range (Figure 5.7).

Figure 5.6: Timing diagram of the ADC.
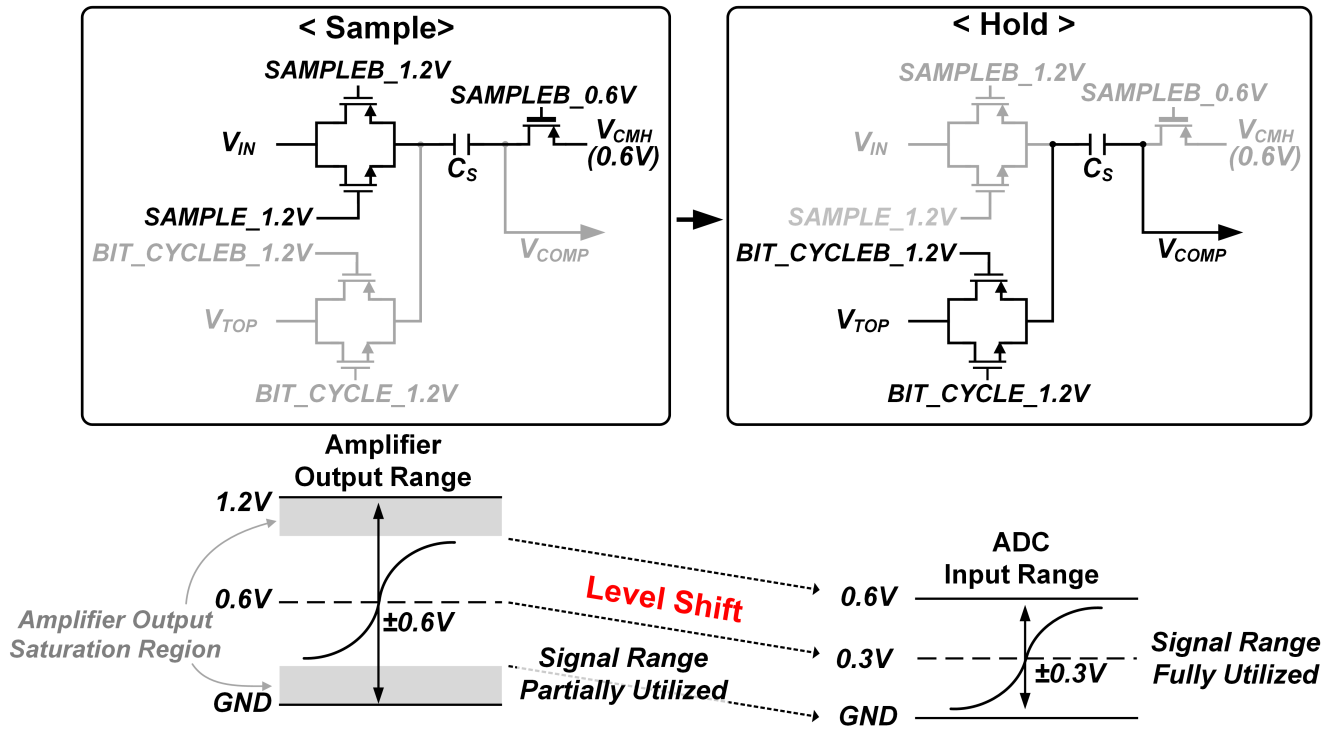
Figure 5.7: Sample and hold circuit.
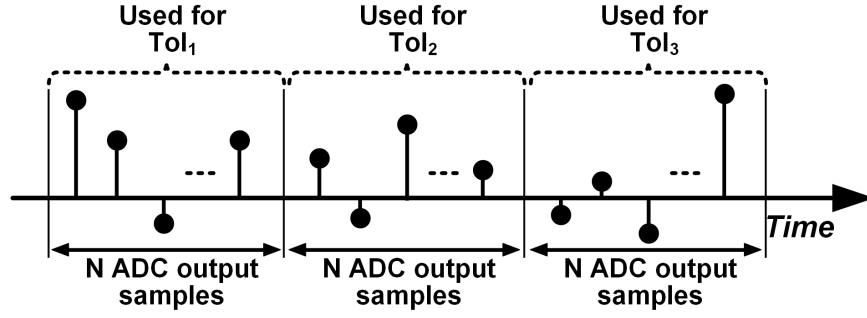
Figure 5.8: Concept of tone-by-tone feature extraction.

5.4 Digtal Backend : Feature Extraction and Classification

The 8-bit ADC SAR output is directly fed into the digital signal processing logic (DSP), which performs frequency domain feature extraction and classification. When a target has disti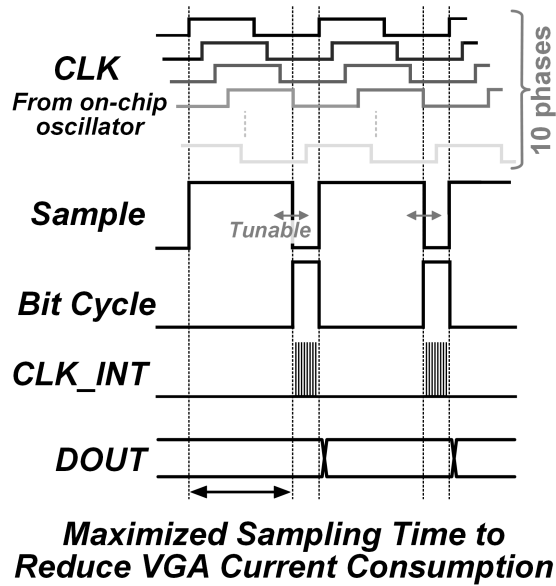nct feature tones, it is wasteful to use a conventional FFT to generate the entire spectrum for object identi- fication. Hence, the proposed feature extraction operates on sparse ToI features using serialized DFT. With an assumption that frequency domain features are stationary, the proposed ToI DFT can be performed on a tone-by-tone basis using serial computation as shown in Figure 5.8. Serial computation is critical to minimize the area of the always-on digital processing logic and thus to minimize leakage power, which can easily dominate at low operating frequencies. The DFT of a particular ToI index k is obtained by the equation 5.1, where N is the DFT size and the set of integer ToI indices is defined as ToI_1, ToI_2, ToI_3, ..., ToI_K.

$$X[ToI_K] = \sum_{n=kN+1}^{(k+1)N} e^{-j\frac{2\pi n ToI_k}{N}} x[n] \tag{5.1}$$

These ToI indices consist of feature tones to detect target objects, and some background noise tones to be used to obtain reference noise level. The ToI DFT output, $X[\text{ToI}_k]$, for the k-th ToI is computed using samples arriving at kN+1, kN+2, ... , (k+1)N time-indices. That is, each ADC sample x[n] is used only once for a particular ToI index and, not for other indices, as depicted in Figure 5.8.

The proposed serialized ToI DFT approach greatly simplifies the computation that needs to be performed at each clock cycle. Figure 5.9 shows the proposed ToI DFT architecture. By sim- ply changing the phase accumulation rate ($\Delta\theta$), the DFT on any particular ToI can be obtained.
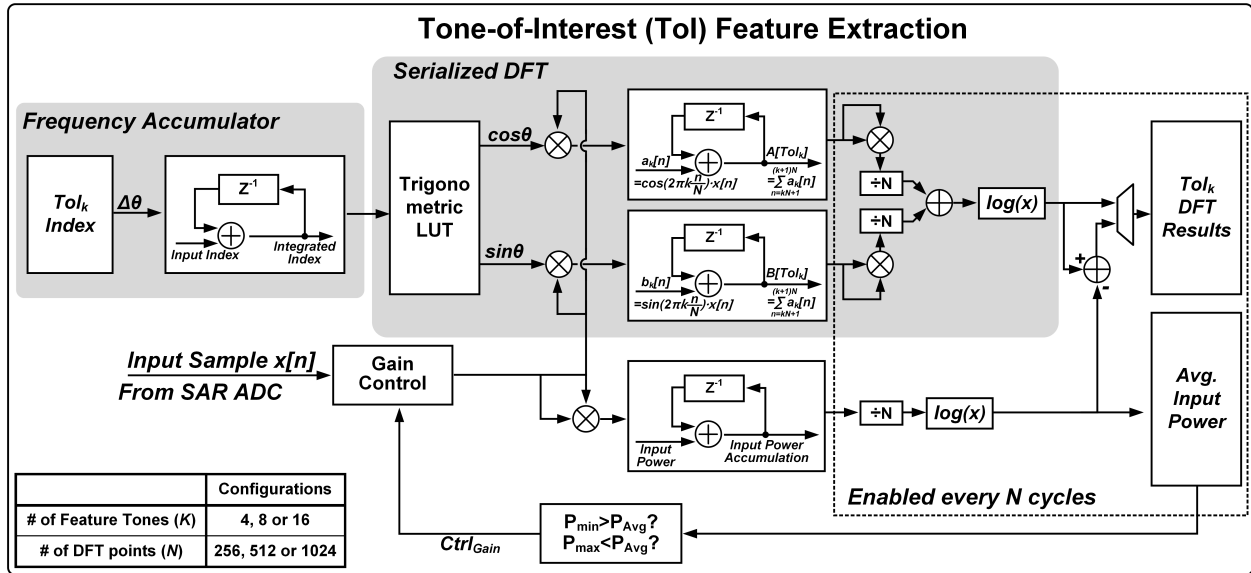
Figure 5.9: Block diagram of a feature extraction based on serialized DFT.
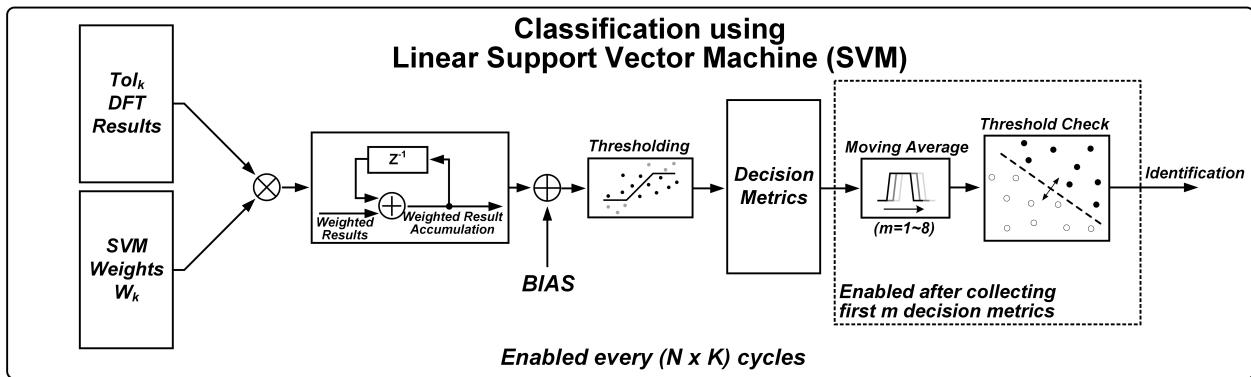
Figure 5.10: Block diagram of a classifier based on linear support vector machine (SVM).

Trigonometric functions (sin and cos) for DFT are implemented using a compact look-up table (LUT) storing only cosθ for $0 \leq \theta \leq \pi/4$. This technique reduces power by 30% (simulation) compared with a CORDIC [61].

While the ToI DFT computation is always-on, the classifier logic can be clock gated until DFT sequentially generates all of the ToI. Due to the low ToI DFT throughput (e.g., a period of 4.096s for 8 ToI, 512 cycles per ToI, and 1 kHz clock), a sophisticated classification scheme such as machine learning based SVM can be used with limited power overhead (Figure 5.10). Computationally demanding SVM training is performed off-line, resulting in a $1 \times K$ weight vector and an offset constant BIAS per object to be classified. These training results are stored in programmable memory. Log2 function is applied on DFT output power for SVM input. The instantaneous SVM

output is low-pass filtered, and a constant threshold is applied to make a final decision. Due to the low clock frequency, leakage power is significant. Therefore, I/O devices are used throughout the entire DSP to reduce leakage by $162\times$ and total power by 92.8%.

5.5   Peripheral Circuits: Charge Pump, Current and Clock Source

The charge pump provides a bias voltage across the MEMS sensor, setting the sensitivity of MEMS device. Pseudo-resistor is used to bias the MEMS as $>G\Omega$ is required to set the high pass corner <20Hz. Output of the charge pump has negligible load current (<100pA) which enables low power operation by lowering its clock frequency. The frequency is designed to be variable from 7.81Hz to 1kHz in a binary fashion (240-840pW). The output voltage of the charge pump is designed to be variable from 10x to 12x configuration (11.19V - 13.35V, simulation results). Current source is based on Nagata current mirror [62]. Instead of using BJTs, subtreshold biased MOSFETs are used to generate 100s of pA of current. Also, pseudo-resistor is used instead of a passive resistor to save area. Resistance is controlled by adjusting the gate voltage of the MOSFET. Voltage control uses 128 stage diode stack from 1.2V supply voltage resulting into 10mV step. Voltage controlled oscillator has been used as a clock source. NMOS header is used to adjust the virtual supply of the oscillator while the unit cell has been implemented with a thyristor-based oscillator [22] to avoid short circuit current.

5.6   Measurement

5.6.1   Block Level

The proposed system is fabricated in 180nm CMOS and its die photo is shown in Figure 5.11. Measurements show an amplifier gain range of 31 to 59dB with 470Hz bandwidth while consuming 5.6nW (Figure 5.12). The low-noise amplifier consumes 3.4nA with $17\mu V_{rms}$ integrated input noise (Figure 5.13), resulting in a 1.8 NEF. The ADC shows peak DNL and INL of +0.3/-0.3 LSB and +0.3/-0.6 LSB, respectively (Figure 5.14). Figure 5.15 shows measured output spectrum of the ADC. Measured SFDR is 60.04dB and SNDR is 48.26dB, which corresponds to 7.7b ENOB.
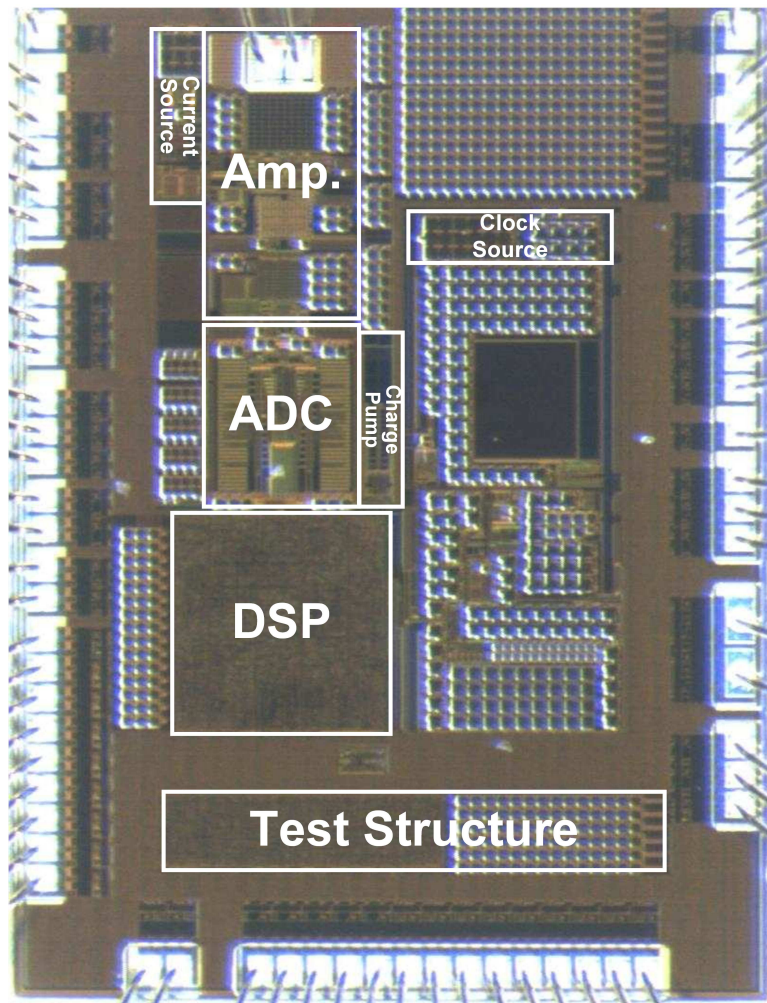
Figure 5.11: Die micrograph of the proposed design
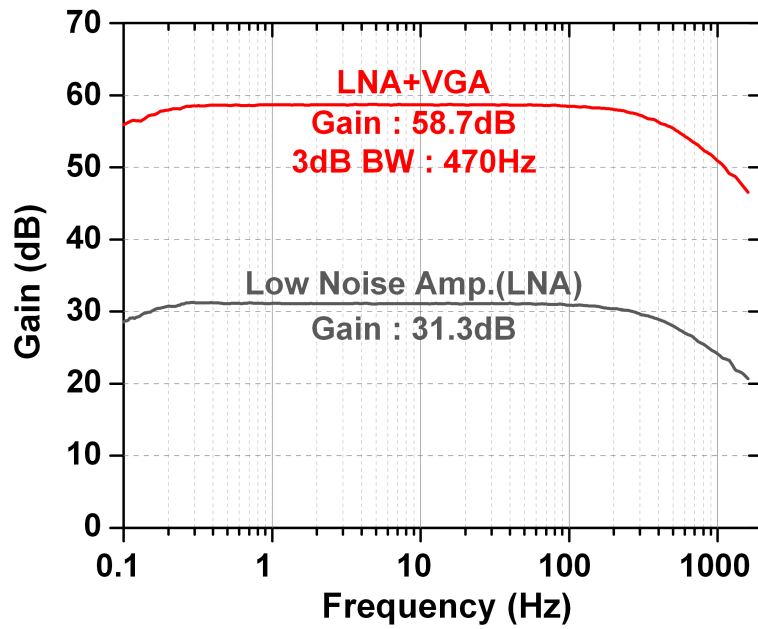
Figure 5.12: Measured amplifier frequency response
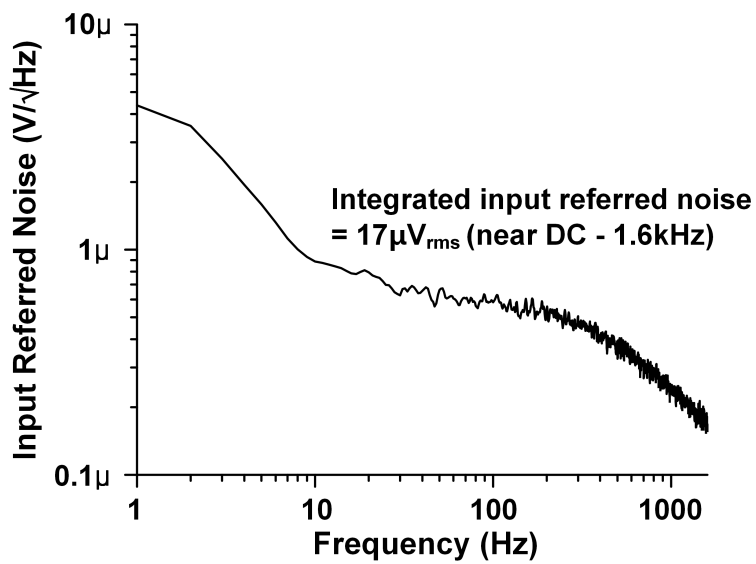
Figure 5.13: Measured amplifier noise
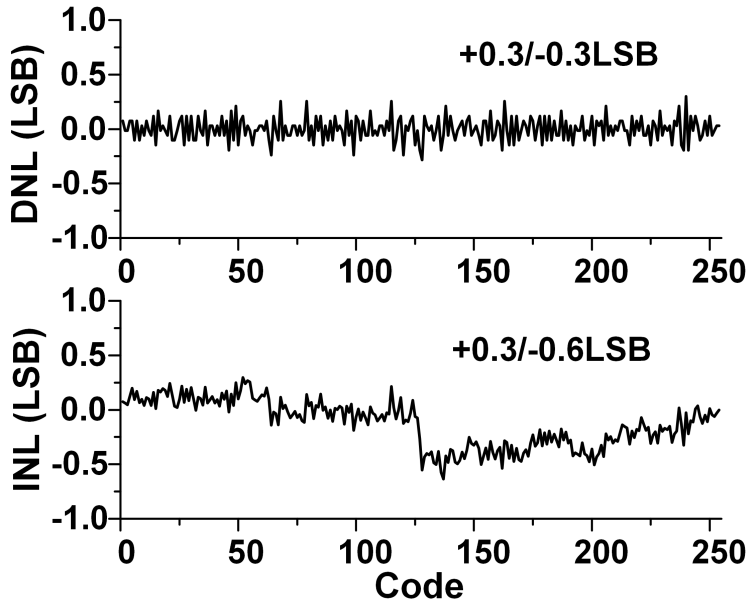
Figure 5.14: DNL and INL measurements
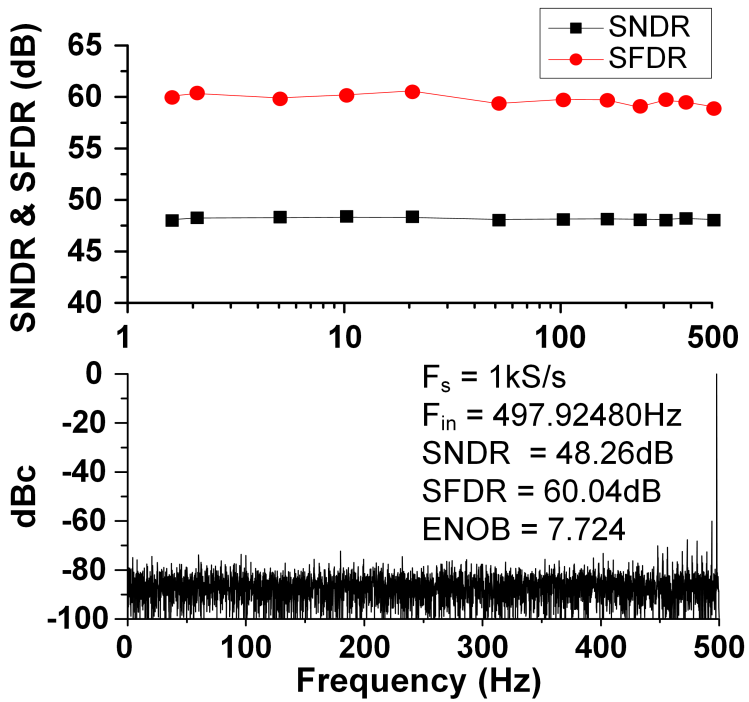
Figure 5.15: FFT of ADC output data
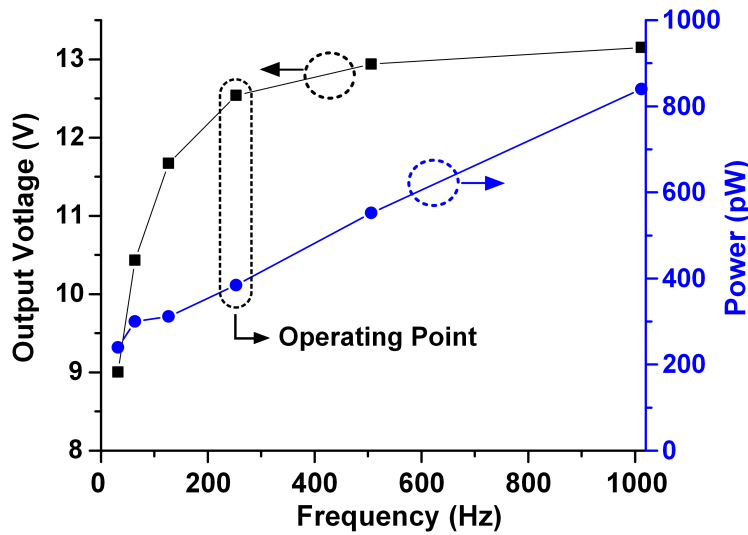
Figure 5.16: Charge pump measurements

Measurement results of the charge pump is shown in Figure 5.16. Operating point of the charge pump has been chosen to output 12.5V while consuming 380pW. The overall power breakdown of the system is shown in Figure 5.17. Proposed system consumes 12.2nW, 46% of which is in the amplifier. Table 5.1 summarizes the performance of this work.

5.6.2 System Level

For system integration, custom PCB and a 3D-printed lid are used to maximize SNR by limiting the parasitic capacitance at the connection between the MEMS membrane and the frontend amplifier. Figure 5.18 shows assembled microsystem. Performance of the proposed system is tested in realistic environment with 68∼72dB(z) SPL background noise. Measurement setup is shown in Figure 5.19. Desktop computer is used to play sound which goes through an audio amplifier to drive a passive speaker. Reference microphone placed near the system to identify an actual sound pressure level at the MEMS microphone. Sound database has been provided by a 3rd party research lab for 3 different target objects (a generator, car, and truck) which are recorded in an anechoic chamber. Figure 5.21 shows the classifier outputs for various test cases, where an identification is triggered when the filtered classification metric exceeds the threshold of 0. The proposed ToI based SVM exhibits reliable performance for our target objects whose features are stationary in time and sparse in frequency domain. The system demonstrates a consistent, >95%
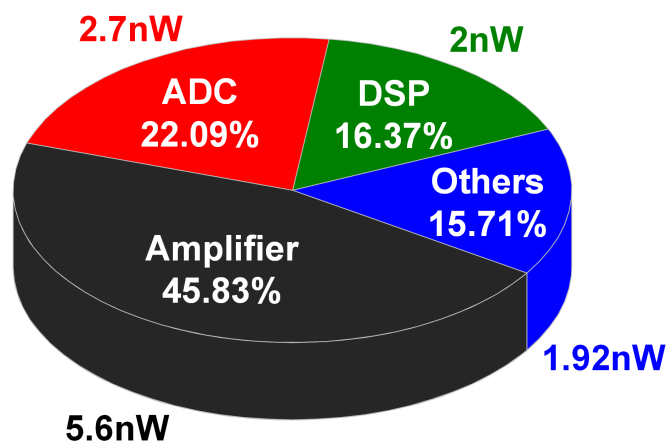
Figure 5.17: System power breakdown
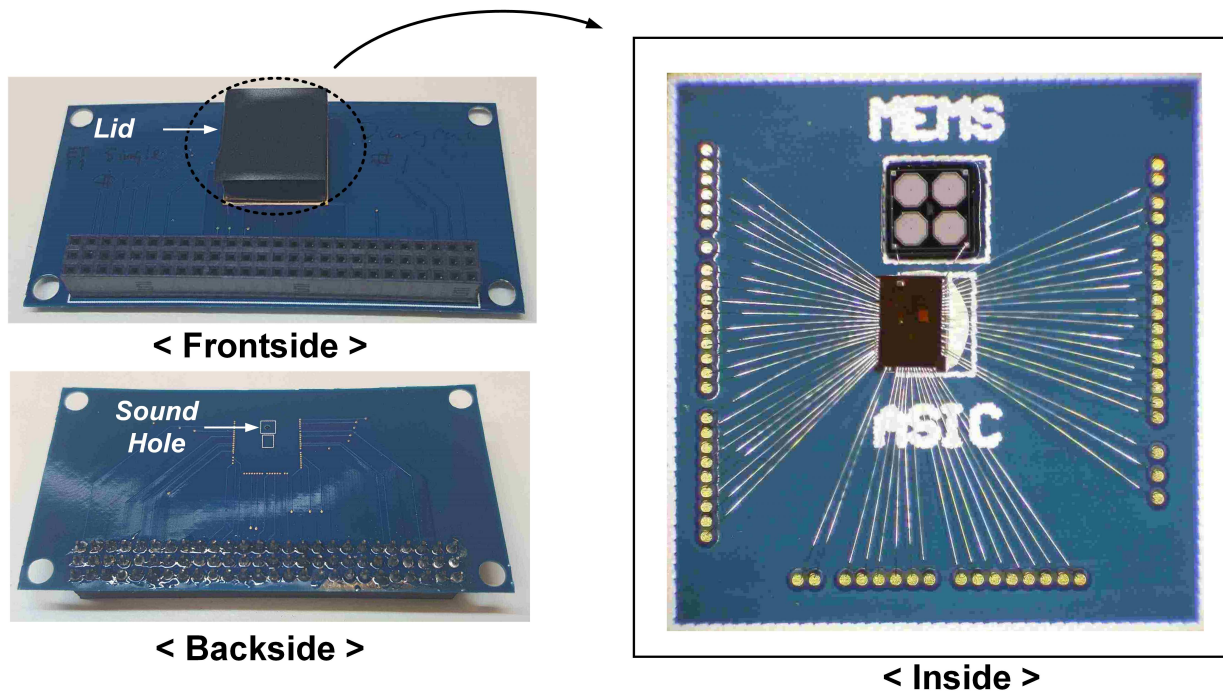
Figure 5.18: Assembled microsystem

Technology			0.18µm
Core Area			0.75mm^2
Signal Chain	Amplifier	Supply Voltage	1.2V
		Power	5.6nW 3.4nA(LNA), 1.2nA(VGA)
		Gain	31 ~ 59dB
		Bandwidth	470Hz
		Input referred Noise	17µV$_{rms}$
		NEF	1.8 (w/o VGA) 2.0 (w/ VGA)
	ADC	Supply Voltage	0.6V
		Power	2.7nW
		Sampling Rate	1kS/s
		Resolution	8bit
		ENOB	7.7
		Linearity	DNL: +0.3/-0.3LSB INL: +0.3/-0.6LSB
		FOM [fJ/conv· step]	13.0
	DSP	Supply Voltage	0.6V
		Power	2nW
		Clock Frequency	1kHz
		Processing	512pt DFT Linear SVM
Other Peripherals (Charge pump, Current/Clock Source)			1.92nW
Total System Power			12.2nW

Table 5.1: Performance Summary
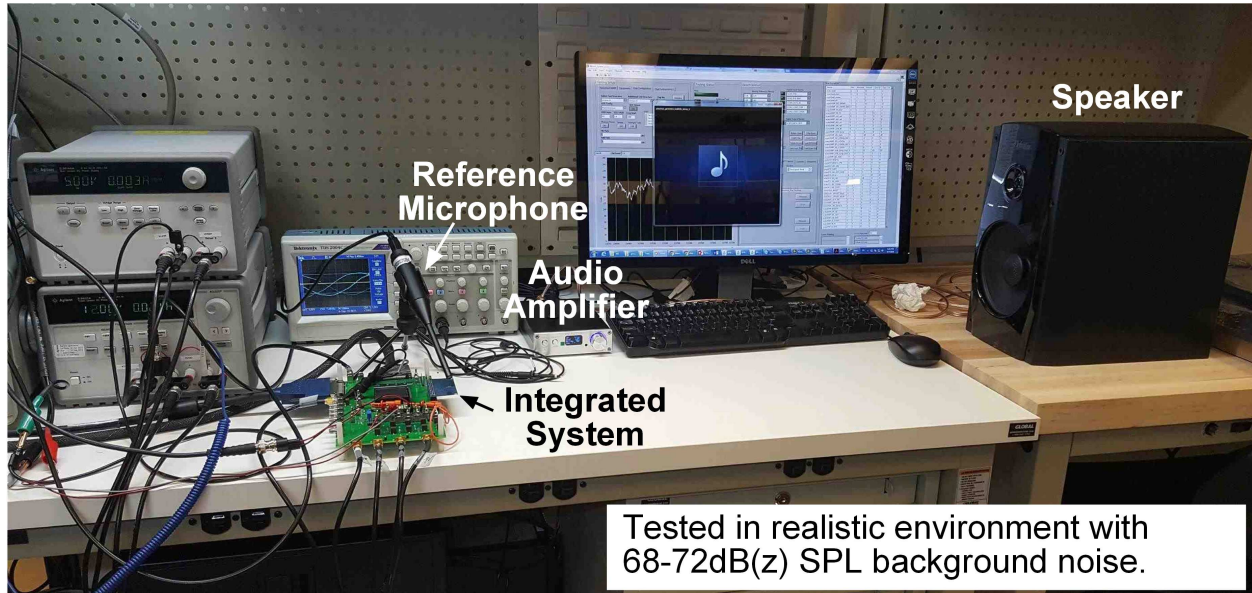
Figure 5.19: Testing environment
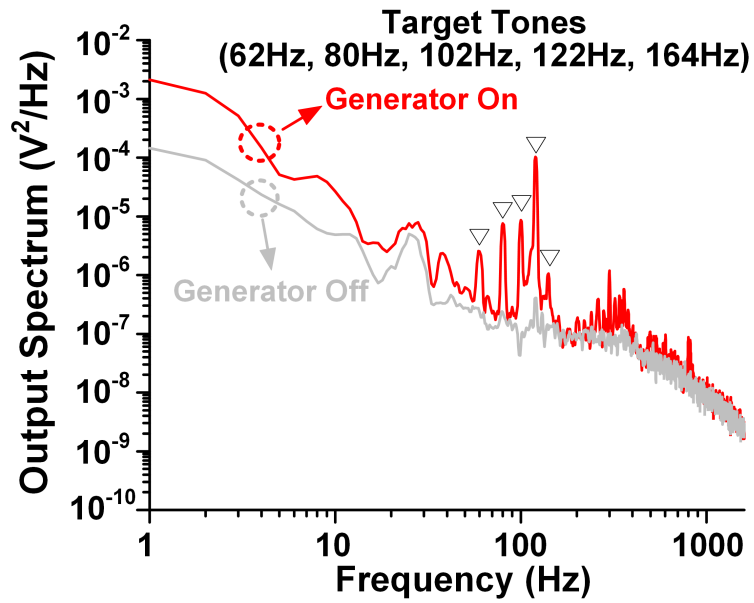
Figure 5.20: Measured amplifier output spectrum
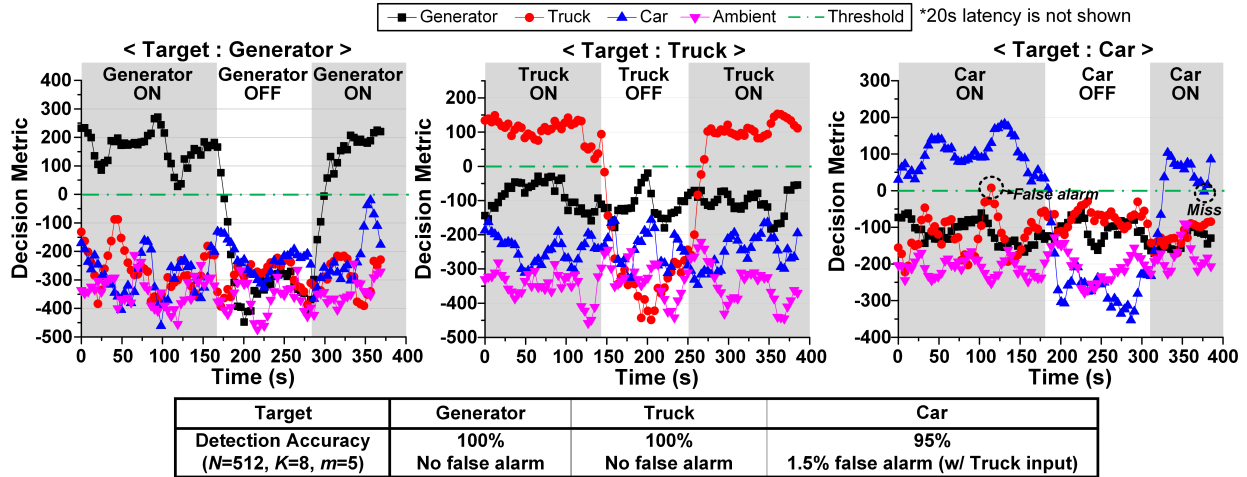
Figure 5.21: Classification results

detection rate for all tests.

5.7 Conclusion

An ultra-low power always-on acoustic sensing and object recognition microsystems for IoT applications is proposed. By introducing ultra-low 8-bit SAR-ADC with 50fF input capacitance, power consumption of the frontend amplifier has been reduced to single digit nW-level. Also, serialized discrete Fourier transform (DFT) feature extraction is proposed in a digital back-end, replacing a high-power/area-consuming conventional FFT. With these approaches, the overall system consumes 12nW and successfully identifies target objects with >95% accuracy.

CHAPTER 6

Conclusion

The Internet of Things (IoT) has been one of the biggest driver of the change in industry market over last decade. Now, the IoT has become a reality and being spotlighted more than ever. It has infiltrated into every part of business and into our daily lives. One of key aspect that makes IoT special and offers great potential is that the internet can expand into places that has been ever reachable. In order to take a full advantage of the IoT applications, small form factor must be met. Also, numerous devices used in random places necessitates the use of battery as their main power source. These two factors suggest challenging requirements for an ideal IoT devices where they should be operating without any external references while consuming minimal power due to limited power budget. In this dissertation, a wide range of ultra-low power circuits for IoT application was covered starting from a block level implementation to a complete system level integration. Main focus has been made on reducing power consumption while avoiding performance degradation. New circuit techniques as well as system level optimizations was explored to achieve this demanding goal.

6.1 Discussion and Key Contributions

An ultra-low power temperature sensor was presented in Chapter 2. Conventional bandgap reference based temperature sensor uses forward biased BJTs which makes them hard to reduce their power consumption below μ level. Instead, a new sensing element composed of only two MOSFETs was introduced which shows great temperature characteristic while consuming 10s of pW.

The sensing element exhibits highly linear output voltage across temperature with its temperature coefficient being robust to process variations. Its low output voltage level ($\leq$100mV) allowed us to use single digit MΩ resisters to generate nAs of current. If conventional bandgap references were used more than 20MΩ is required to achieve similar power consumption which is impractical due to area constraints. Two different sensing element and resister types are used to generate PTAT and reference current. For current generation, we have introduced a second feedback loop to avoid additional current mirror for generating a control voltages for the following current-starved ring oscillator. This allowed 2$\times$ power reduction by eliminating an additional branch. Two current-starved ring oscillators generated PTAT and reference frequency and those frequencies were fed into counters to generate a digital output code. The temperature sensor was implemented in 180nm CMOS technology with an area of 0.09mm^2. Average power consumption of the sensor over 18 samples was 71nW with 31ms of conversion time. Resolution was measured to be 0.3°C with an inaccuracy of +1.5°C/-1.4°C after 2-point calibration. The proposed sensor was also integrated into a mm-cubic scale microsystem and showed successful operation.

On-chip wakeup timer was presented in Chapter 3. We have introduced a charge subtraction scheme that removes constant amount of charge from a integrating capacitor. Compared to a conventional way of resetting the integration capacitor all the way to ground, this scheme removes temperature dependency of a continuous comparator. As a result, a power hungry continuous comparator was replaced with a coarse clocked comparator that consumes only 100s of pW while the generated sawtooth waveform always rejoins the ideal waveform. Since constant frequency cannot be generated from the clocked comparator, a continuous comparator is added to generate a precise wakeup signal. An asynchronous counter was added to control a wakeup period by counting number of sawtooth waveforms and controlling the power-gated continuous comparator. The test chip was implemented in 180nm CMOS process with 0.24mm^2 of area. Measure temperature coefficient was 45ppm/$^\circ$C across 5 samples with line sensitivity of 1%/V. The timer consumed 5.8nW with $>$50s of wakeup interval.

Subranging SAR ADC for biomedical application was presented in Chapter 4. In this chapter, we introduced a new DAC topology that enabled MSB recycling based on a previous conversion result. A series capacitor was added in between capacitive DAC and a comparator which is used to store previous sample's MSB voltage in terms of voltage. As long as the signal stays in the same

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subranging window, the stored voltage can be reused again and again saving more than 50% of DAC energy as well as logic and comparator energy. In order to prevent error coming from the leakage on the series capacitor while staying in the same subranging window, refresh rate can be set based on the environment (e.g. temperature). Number of MSBs were determined to be 4 out of 8bit as it resulted into a minimal energy point. Proposed scheme was implemented in 180nm process with an area of $0.12mm^2$. Measured INL and DNL were ±0.3LSB and ±0.6LSB, respectively. SNDR and SFDR were 46.9dB and 63.8dB, respectively. The ADC consumes 120nW at 100kS/s at 0.6V resulting into a 6.6fJ/conv·step. Usefulness of the proposed scheme in biomedical application was also tested and verified using ECG waveforms collected from 39 un-discriminated patients from the University of Michigan hospital for diagnosis and treatment of atrial fibrillation. With different amount of input referred noise added mimicking a frontend amplifier, the proposed scheme did not show any performance degradation compared to the conventional scheme while consuming $2.6\times$ less power.

Always-on acoustic microsystem for a sensing and object recognition was presented in Chapter 5. Proposed system was built on a custom PCB to minimizes parasitic capacitance in order to place ASIC and MEMS on the same side. This allowed a direct connection between the membrane and ASIC. A custom lid was also implemented using 3D printer which covered both the ASIC and MEMS. Using custom PCB also relaxed pad restrictions on chip and eased debugging. The system was based on active integrated circuits that employ aggressive low power techniques to meet the overall power budget of 12nW while satisfying the target performance specification. It was observed that the targeted audio signal features are mainly concentrated within a narrow bandwidth, allowing a ≤0.5kHz bandwidth and ≤1kHz clock for all active components. This low frequency was one of the key enabling factors that allowed continuous (without duty-cycling) sensing with 12nW power consumption. A system-level analysis revealed that the first-stage amplifier is noise-limited while the second-stage variable gain amplifier(VGA) is bandwidth-limited rather than noise-limited. To enable sufficient bandwidth for the second-stage VGA with a nW power consumption, an ULP 8-bit SAR-ADC with a unique topology that has extremely small ($\leq$ 50fF) input capacitance was proposed. These architecture selections allow the amplifier to be designed with an unconventionally low bias current ($\leq$ 4nA), enabling the 6nW power budget while meeting the required bandwidth with high gain. The digital signal processing logic performs ULP

frequency domain feature extraction while consuming 2nW. A serialized discrete Fourier transform (DFT) that, unlike a high-power / area-consuming conventional FFT, is only performed on the discrete tones-of-interest. For classification linear support vector machine (SVM) provided the necessary performance ($\geq$95%) to detect target objects.

Demand on lower power, smaller form factor and long life time for IoT devices will continue to increase as time passes. All of the works presented in this dissertation give subtle guidance for designing IoT devices in somewhat extreme design space. Such design techniques and approaches for dealing with low power could possibly expedite the development of future low power IoT application space.

6.2   Future Work

There exist possible opportunities to improve the works presented in this dissertation. For a temperature sensor presented in Chapter 2, one could explore using an ADC to generate a digital output code instead of using several steps of conversion (voltage to current, current to frequency and frequency to digital code). The main source of inaccuracy error was coming from a current to frequency conversion where both PTAT and reference frequency showed degradation in linearity and temperature coefficient, respectively, compared to a result from a current generation. By taking an advantage of process robustness of the sensing element, its output voltage could be simply fed in to an ADC, removing errors coming from different elements (resistors, current mirrors, etc). Of course, output voltage of the sensing element cannot be directly connected to and ADC as it has weak drivability and limited output range. However, a switched-capacitor amplifiers, for an example, could be introduced to drive the ADC while providing enough gain while 2T sensing element can act as a voltage reference for the ADC. Timer in Chapter 3 could be further improved by using a temperature insensitive resistor to generate a reference voltage. One of the difficulty in this work for achieving low temperature coefficient came from the fact that both temperature insensitive voltage and current were necessary. As generating both using active circuity in a low power domain is challenging, a voltage for charging a capacitor could be generated with a current flowing through a temperature insensitive resistor. Also, this current should be a copy of a current that is used to charge the main capacitor. With this scheme, temperature stability of the

generated frequency does not get affected by the temperature stability of the current as they cancel out. Temperature insensitive resistor is relatively easy to implement compared to the former two as it is a passive element. One thing to consider in this approach would be a size of the resistor and generating 100s of mV using a pA of current will require significant area. However, this constraint could be relieved by adjusting the charging capacitor size. Subranging SAR ADC in Chapter 4 has discrete window size which does not overlap in adjacent windows. As a result, if the signal toggles near the window boundary the ADC has to operate in a conventional mode for every one out of two which essentially slows down the ADC by $2\times$. This could be avoided by having a subranging window that is always centered on the previous sample. Other approach would be adopting a flexible window size where the window size is adjustable based on how frequent the error occurs. Implementing these two approaches will require additional circuity which would increase power consumption and complexity at the cost of improved operation. Finally, acoustic sensing and object recognition system presented in Chapter Chapter 5 could be further expanded to detect multiple targets without the need of reprogramming. This could be done by implementing the DSP with more sophisticated algorithm. One could adopt neural network for classification for better classification compared to a simple linear SVM. As classification happens once every few seconds, increased complexity would not impact dynamic power significantly. However, depending on the number of layers and weights leakage power could be not negligible which should be considered during implementation. Feature extraction could be also further improved by adopting principal component analysis (PCA). By pre-computing PCA eigen vectors and combining them with the DFT matrix, the combined matrix (feature extraction matrix) has same dimension as before (K$\times$512 where K is the number of features). This approach could potentially reduce number of features for same accuracy and number of post processing window size while maintaining the same number of MAC operations per feature.

BIBLIOGRAPHY

[1] International Telecommunication Union (ITU), "Overview of the Internet of things". ITU-T Y.4000/Y.2060 (http://handle.itu.int/11.1002/1000/11559).

[2] Michael Chorost, "The Networked Pil," *MIT Technology Review*, March 20, 2008.

[3] Cymbet Corporation. [Online]. Available: http://www.cymbet.com

[4] E. Y. Chow, S. Chakraborty, W. J. Chappell, and P. P. Irazoquil, "Mixed-Signal Integrated Circuits for Self-Contained Sub-Cubic Millimeter Biomedical Implants," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 236–237.

[5] H. Ghaed, G. Chen, R. Haque, M. Wieckowski, Y. Kim, G. Kim, Y. Lee, I. Lee, D. Fick, D. Kim, M. Seok, K. Wise, D. Blaauw, and D. Sylvester, "Circuits for a cubic-millimeter energy-autonomous wireless intraocular pressure monitor," in *IEEE Trans. Circuits Syst. I*, vol.60, no. 12, pp. 3152–3162, Dec. 2013.

[6] Y. Lee, S. Bang, I. Lee, Y. Kim, G. Kim, H. Ghaed, P. Pannuto, P. Dutta, D. Sylvester, and D. Blaauw, "A modular 1 mm^3 die-stacked sensing platform with low power I^{2}C inter-die communication and multi-modal energy harvesting," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 229–243, Jan. 2013.

[7] M. A. P. Pertijs,K.A. A.Makinwa, and J.H.Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ±0.1°C from -55°C to 125°C," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2805–2815, Dec. 2005.

[8] A. L. Aita, M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a batch-calibrated 3σ inaccuracy of ±0.25°C from -70°C to 130°C," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 342–343.

[9] F. Sebastiano, L. J. Breems, K. A. A. Makinwa, S. Drago, D. M. W. Leenaerts, and B. Nauta, "A 1.2-V 10-μW NPN-based temperature sensor in 65-nm CMOS with an inaccuracy of ±0.2°C from 70°C to 125°C," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2591–2601, Dec. 2010.

[10] K. A. A. Makinwa, "Smart temperature sensors in standard CMOS," in *Proc. Eurosensors XXIV*, Linz, Austria, Sep. 2010.

[11] K. Souri, Y. Chae, and K. A. A. Makinwa, "A CMOS temperature sensor with a voltage-calibrated inaccuracy of ±0.15°C (3σ) from -55°C to 125°C," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 292–301, Jan. 2013.

[12] M. K. Law, A. Bermak, and H. C. Luong, "A sub-μW embedded CMOS temperature sensor for RFID food monitoring application," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1246–1255, Jun. 2010.

[13] M. K. Law and A. Bermak, "A 405-nW CMOS temperature sensor based on linear MOS operation," *IEEE Trans. Circuits Syst. II*, vol. 56, no. 12, pp. 894–895, Dec. 2009.

[14] A. Vaz, A. Ubarretxena, I. Zalbide, D. Pardo, and H. Solar, "A full passive UHF tag with a temperature sensor suitable for human body temperature monitoring," *IEEE Trans. Circuits Syst. II*, vol. 57, no. 2, pp. 95–99, Jan. 2012.

[15] S. Zhou and N. Wu, "A novel ultra low power temperature sensor for UHF RFID tag chip," in *IEEE Proc. Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2007, pp. 464–467.

[16] Y. S. Lin, D. Blaauw, and D. Sylvester, "An ultra low power 1 V, 220 nW temperature sensor for passive wireless applications," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2008, pp. 507–510.

[17] K. Souri, Y. Chae, F. Thus, and K. A. A. Makinwa, "A 0.85 V 600 nW all-CMOS temperature sensor with an inaccuracy of ±0.4°C (3σ) from -40°C to 125°C," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 222–223.

[18] M. Seok, G.Kim, D. Blaauw, and D. Sylvester, "A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5V," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2534–2545, Oct. 2012.

[19] V. De, Y. Ye, A. Keshavarzi, S. Narendra, J. Kao, D. Somasekhar, R. Nair, and S. Borkar, , A. Chandrakasan, W. Bowhill, and F. Fox, Eds., Design of High-Performance Microprocessor Circuits. Piscataway, NJ, USA: IEEE, 2001, ch. 3, pp. 48–52.

[20] N. Retdian, S. Takagi, and N. Fujii, "Voltage controlled ring oscillator with wide tuning range and fast voltage swing," in *IEEE Asia-Pacific Conf. ASIC*, Aug. 2002, pp. 201–204.

[21] N. H. E. Weste and D. M. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective. Boston, MA, USA: Pearson/Addison-Wesley, 2011, ch. 4, pp. 154–155.

[22] M. Wieckowski, G. Chen, M. Seok, D. Blauuw, and D. Sylvester, "A hybrid DC-DC converter for sub-microwatt sub-1 V implantable applications," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2009, pp. 166–167.

[23] P. Chen, C.-C. Chen, C.-C. Tsai, and W.-F. Lu, "A time-to-digitalconverter-based CMOS smart temperature sensor," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1642–1648, Aug. 2005.

[24] P. Chen, T.-K. Chen, Y.-S. Wang, and C.-C. Chen, "A time domain sub-micro temperature sensor with digital set-point programming," IEEE Sensors J., vol. 9, no. 12, pp. 1639–1646, Dec. 2009.

[25] D. Shim, H. Jeong, H. Lee, C. Rhee, D.-K. Jeong, and S. Kim, "A process-variation-tolerant on-chip CMOS thermometer for auto temperature compensated self-refresh of low-power mobile DRAM," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2550–2557, Oct. 2013.

[26] C. Wu, W.-S. Chan, and T.-H. Lin, "A 80 kS/s 36μW resistor-based temperature sensor using BGR-free SAR ADC with a unevenly-weighted resistor string in 0.18 μm CMOS," *in IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2011, pp. 222–223.

[27] S. Hwang, J. Koo, K. Kim, H. Lee, and C. Kim, "A 0.008 mm^2 500μW 469 kS/s frequency-to-digital converter based CMOS temperature sensor with process variation compensation," *IEEE Trans. Circuits Syst. I*, vol. 60, no. 9, pp. 2241–2248, Sep. 2013.

[28] K. A. A. Makinwa, Smart Temperature Sensor Survey. [Online]. Available: http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls

[29] M. H. Nazari, M. Mujeeb-U-Rahman, and A. Scherer, "An implantable continuous glucose monitoring microsystem in 0.18μm CMOS," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2014, pp. 194–195.

[30] Y. Zhang et al., "A batteryless 19μW MICS/ISM-band energy harvesting body sensor node SoC for ExG applications," in *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 199–213, Jan. 2013.

[31] K.-J. Hsiao, "A 1.89 nW/0.15 V self-charged XO for real-time clock generation," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 298–299.

[32] D. Yoon, D. Sylvester, and D. Blaauw, "A 5.5 nW 32.768 kHz DLL assisted XO for real-time clocks in wireless sensing applications," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 366–367.

[33] M. Perrott et al., "A temperature-to-digital converter for a MEMS based programmable oscillator with ±0.5-ppm frequency stability and 1-ps integrated jitter," *IEEE J. Solid-State Circuits*, vol. 48, no.1, pp. 276–291, Jan. 2013.

[34] S. Z. Asl et al., "A 1.55×0.85 mm^3 3 ppm 1.0μA 32.768 kHz MEMS-based oscillator," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 226–227.

[35] A. Paidimarri, D. Griffith, A. Wang, A. Chandrakasan, and G. Burra, "A 120 nW 18.5 kHz RC oscillator with comparator offset cancellation for ±0.25% temperature stability," in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 184–185.

[36] K.-J. Hsiao, "A 32.4 ppm/ C 3.2 1.6 V self-chopped relaxation oscillator with adaptvie supply generation," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2012, pp. 14–15.

[37] T. Tokairin et al., "A 280 nW, 100 kHz, 1-cycle start-up time, on-chip CMOS relaxation oscillator employing a feedforward period control scheme," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2012, pp.16–17.

[38] D. Griffith, P. T. Roine, J. Murdock, and R. Smith, "A 190 nW 33 kHz RC oscillator with ±0.21% temperature stability and 4 ppm long-term stability," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 300–301.

[39] J. Lim, K. Lee, and K. Cho, "Ultra low power RC oscillator for system wake-up using highly precise auto-calibration technique," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2010, pp. 274–277.

[40] A. Shrivastava and B. H. Calhoun, "150 nW 5 ppm/°C 100 kHz on-chip clock source for ultra low power SOCs," in *Proc. IEEE CICC*, 2012, pp. 14.

[41] Y.-S. Lin, D. Sylvester, and D. Blaauw, "A sub-pW timer using gate leakage for ultra low-power sub-Hz monitoring systems," in *Proc. IEEE CICC*, 2007, pp. 397–400.

[42] Y. Lee, B. Giridhar, Z. Foo, D. Sylvester, and D. Blaauw, "A sub-nW multi-stage temperature-compensated timer for ultra-low-power sensor node," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2511–2521, Oct. 2013.

[43] Y.-S. Lin, D. Sylvester, and D. Blaauw, "A 150 pW program-and-hold timer for ultra-low-power sensor platforms," in *IEEE ISSCC Dig. Tech. Papers*, 2009, pp. 326–327.

[44] B. R. Gregoire and U. Moon, "Process-independent resistor temperature-coefficients using series/parallel and parallel/series composite resistors," in *Proc. IEEE ISCAS*, 2007, pp. 2826–2829.

[45] U. Denier, "Analysis and design of an ultralow-power CMOS relaxation oscillator," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 8, pp. 1973–1982, Dec. 2010.

[46] T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, "A currentcontrolled latch sense amplifier and a static power-saving input buffer for low-power architecture," *IEEE J. Solid-State Circuits*, vol. 28, no. 4, pp. 523–527, Apr. 1993.

[47] I. Lee, "Power management circuits for miniature sensor systems," Ph.D. dissertation, Dept. Electrical Eng., Univ. Michigan, Ann Arbor, MI, USA, 2014.

[48] S. Jeong, Z. Foo, Y. Lee, J.-Y. Sim, D. Blaauw, and D. Sylvester, "A fully-integrated 71 nW CMOS temperature sensor for low power wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1682–1693, Aug. 2014.

[49] D. W. Allan, "Statistics of atomic frequency standards," *Proc. IEEE*, vol. 54, no. 2, pp. 221–230, Feb. 1966.

[50] D. Jeon, Y.-P. Chen, Y. Lee, Y. Kim, Z. Foo, G. Kruger, H. Oral, O. Berenfeld, Z. Zhang1, D. Blaauw, and D. Sylvester, "An Implantable 64nW ECG-Monitoring Mixed-Signal SoC for Arrhythmia Diagnosis," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 416–418.

[51] M. Fojtik, D. Kim, G. Chen, Y.-S. Lin, D. Fick, J. Park, M. Seok, M.-T. Chen, Z. Foo, D. Blaauw, and D. Sylvester, "A Millimeter-Scale Energy-Autonomous Sensor System With Stacked Battery and Solar Cells," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2013, pp.16–17.

[52] G.-Y. Huang, S.-J. Chang, C.-C. Liu, and Y.-Z. Lin, "A 1-μW 10-bit 200-kS/s SAR ADC With a Bypass Window for Biomedical Applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2783–2795, Nov. 2012.

[53] F. M. Yaul, and A. Chandrakasan, "A 10 bit SAR ADC With Data-Dependent Energy Reduction Using LSB-First Successive Approximation," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2825–2834, Dec. 2014.

[54] M. Trakimas and S. R. Sonkusale, "An Adaptive Resolution Asynchronous ADC Architecture for Data Compression in Energy Constrained Sensing Applications," *IEEE Trans. Circuits Syst. I*, vol. 58, no. 5, pp. 921–934, May. 2011.

[55] M. Yip and A. Chandrakasan, "A Resolution-Reconfigurable 5-to-10b 0.4-to-1V Power Scalable SAR ADC," in *IEEE ISSCC Dig. Tech. Papers*, 2011, pp. 190–192.

[56] H. Oral, O. Berenfeld, and G. Kruger, U.S. Patent 201 3019 7380 A1, 2013

[57] K. Badami, S. Lauwereins, W. Meert, M. Verhelst, "Context-Aware Hierarchical Information-Sensing in a 6μW 90nm CMOS Voice Activity Detector," *IEEE J. Solid-State Circuits*, vol. 51, no.1, pp. 240–248, Jan. 2016.

[58] B. Rumberg, D. W. Graham; V. Kulathumani; R. Fernandez, "Hibernets: Energy-Efficient Sensor Networks Using Analog Signal Processing," in *IEEE JETCAS*, vol. 1, no.3, pp. 321–334, Sep. 2011.

[59] P. Harpe, H. Gao; R. van Dommele; E. Cantatore; A. H. M. van Roermund "A 0.20 mm^2 3 nW Signal Acquisition IC for Miniature Sensor Nodes in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no.1, pp. 240–248, Jan. 2016.

[60] Y. Chen, D. Jeon, Y. Lee, Y. Kim, Z. Foo, I. Lee, N. B. Langhals, G. Kruger, H. Oral, O. Berenfeld, Z. Zhang, D. Blaauw, D. Sylvester, "An Injectable 64 nW ECG Mixed-Signal SoC in 65 nm for Arrhythmia Monitoring," *IEEE J. Solid-State Circuits*, vol. 50, no.1, pp. 375–390, Jan. 2015.

[61] J. E. Volder, "The CORDIC trigonometric computing technique," *IRE T.E.C.*, vol. EC-8, no.3, pp. 330–334, Sep. 1959.

[62] K. Kimura, "Low voltage techniques for bias circuits," *IEEE Tran. on Circuits and Systems,* 44(5):459, May 1997.