Circuit and System Designs for Millimeter Scale IoT and Wireless Neural Recording

by

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To my family

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ABSTRACT

The next generation of computing platforms increases proximity to the source of information rather than to humans, allowing much more aggressive miniaturization. The key technology for miniaturization has been process scaling, which has reduced the silicon area, increased computational capability and lowered power consumption. However, the latest deep-submicron technologies do not fit well with mm-scale computing because of the increased leakage current. Therefore, advances in circuit level techniques are critical to realizing networks of mm-scale IoT computing platforms.

Smart sensor nodes have been a popular research topic in recent decades, as the demand for collecting and processing environmental data has grown. Consequently, promising research outcomes have been published in various areas of medical care, environmental monitoring and surveillance. Such wireless sensor nodes (WSNs) require new circuit techniques as they are placed in a very distinct operating environment with specialized purposes compared to conventional applications. Ultra-low power consumption is one of the most challenging constraints resulting from the form factor of the system.

In this dissertation, circuit techniques to reduce power consumption of the system is introduced. A 4.7nW wake-up timer with 13.8ppm/℃ temperature coefficient demonstrated in this dissertation lowers system sleep power while minimizing the energy overhead for peer-to-peer communication. A 2.5ps_{rms} digital phase-locked loop with noise self-adjustment improves the system stability by making the noise of the clock invariant to the environmental changes. A neural

recording amplifier with 1.8 noise efficiency factor enhances the power efficiency of the analog front-end. As a demonstration of the miniaturized sensor system, this dissertation presents a 2.7cm^3 stand-alone global navigation satellite system that can acquire 1791 positions.

CHAPTER 1

Introduction

1.1 Miniaturized Sensor Nodes

Miniaturization and interactive communication are the two main topics that dominate the recent research in the internet-of-things (IoT) [1]–[11]. The high demand for continuous monitoring of environmental and bio-medical information has accelerated sensor technologies as well as circuit innovations. Simultaneously, the advances in communication methods and the wide spread use of cellular and local data links enable the networking of sensor nodes. This potential improvement in machine service for humans could trigger the commercial development of a sensor node with platforms that collect, process and transmit widely spread environmental and bio-medical data.

In the history of computing platforms, from mainframes in the 1950s to workstations in the 1960s, personal computers in the 1980s, laptops in the 1990s and now the current smartphones, one of the most evident trends is the increasing convenience and frequency of access by humans who utilize the computing platform. Miniaturization of the computer is an important factor in this trend, lowering cost, reducing the required space and providing mobility. However, the need for

physical access with an interfacing component like a screen, buttons or a touch surface limits its minimum form factor and therefore inhibits further miniaturization.

On the other hand, the next generation of computing platforms, which is the IoT, increases proximity to the source of information rather than to humans, allowing much more aggressive miniaturization. The key technology of miniaturization has been process scaling, which has reduced the silicon area, increased computational capability and lowered power consumption. However, leakage current of a device has continuously increased with the process scaling so that the latest deep-submicron technologies do not fit well on the mm-scale computing platforms that demand nano-watt levels of sleeping power. Therefore, advances in *circuit level techniques* are critical to realize networks of mm-scale IoT computing platforms. Furthermore, a miniaturized form factor incurs a severely restricted energy budget [12], [13]. For instance the 0.92-mm^3 Li thin-film battery introduced in [14] provides nearly $1/10^6$th the energy capacity of an alkaline AA battery. Therefore, the transition of the circuit design regime from milli-watt to nano-watt level is critical.

The power consumption of a sensor node can be categorized into two types. The active power is usually micro to milli-watt level, which is dominated by processor, sensor interface and data transceiver. The reduction of energy to perform a single operation such as temperature sensing, positioning or data transmission, is emphasized to maximize the frequency of operation given the fixed amount of harvested power. In addition, it is related to the minimum required battery size. Assuming that the active time of a system is short enough to consider that the harvested energy during the time is negligible, the battery capacity must be larger than the energy required for a single operation. This sets the main constraint for a system form factor. The active power consumption is also important for the system perspective. First, the output resistance of a

millimeter-scale battery is large enough to impact the system functionality and the energy efficiency. For instance, a 0.92mm^3 Li thin film battery has a maximum output resistance of 60kΩ, and it can cause 600mV output voltage drop from the 3.2V nominal output voltage with 10μA load current. Such significant voltage drop let significant portion of total energy be wasted by the battery itself. Furthermore, it can cause functional failure of circuit or performance degradation due to the supply noise. The remedy for both of the problems is to incorporate a voltage regulator to provide a stable supply voltage, which also poses power conversion loss. Therefore, circuit techniques to minimize the energy per operation as well as the power consumption are important.

On the other hand, sleep power is usually nano to sub-nano watt level and is affected by the leakage of the power down switches, static random access memory and few always on blocks. The minimization of the leakage current determines minimum sustainable harvestable power using duty-cycled operation. As long as the harvested power is larger than the sleep power, a system can sustain the operation perpetually.

1.2 Outline of the Dissertation

Chapter 2 of this dissertation reviews recent advances in circuit techniques in the implementation of the key building blocks for miniaturized sensor nodes. It includes design challenges associated with sensor front-end circuits. Circuit techniques for analog references and amplifiers are also introduced. Then, system level discussions on capacitive sensor interfaces and bio-medical applications is demonstrated. As one of the key elements for saving sleep power of a miniaturized sensor node, ultra-low power timing references are reviewed. It also review design challenges in data transceiver, energy harvester, power management unit and digital logic gates.

Among key building blocks of a wireless sensor node, the wake-up timer is the key always on block that dominates sleep power if accurate duty cycling is desired. In Chapter 3, a 4.7nW wake-up timer is demonstrated that minimize its power overhead for the system sleep power. The proposed wake-up timer showed 13ppm/℃ temperature coefficient which is the state-of-the art accuracy as a monolithic on-chip oscillator.

Accurate clock generation using a PLL will be highly beneficial for power reduction of wireless transceiver. In Chapter 4, a circuit technique to generate a system clock using a phase-locked loop (PLL) is proposed. As a proto-type design, a 2.5ps_{rms} jitter PLL is demonstrated. It has a noise reconfiguration capability to minimize its power overhead with given noise specification as well.

In Chapter 5 a miniaturized global navigation satellite system (GNSS) is proposed. An energy harvester, a power management unit and RF and optical transceivers are implemented to support energy-efficient, stand-alone operation. A sensor interface layer is also implemented to monitor environmental variables such as temperature and pressure.

Finally, Chapter 6 of this dissertation covers a power efficient front-end scheme using parametric amplification as a future work. Sensor interface circuits, which interacts with pressure, humidity, acceleration, neural signal sensors, are required to exhibit appropriate input referred noise so it can monitor signals with sufficient accuracy. At the same time, power consumption of the interface needs to be as low as possible due to the highly constrained power budget originates from the system form factor. Therefore power efficiency of front-end amplifiers are highly emphasized. This work targets to reduce the power consumption of a neural recording front-end by 2x while maintaining the input referred noise 2-3μW.

CHAPTER 2

Research Trends for Miniaturized Sensor Nodes

2.1 Analog Circuit Techniques

Due to the inherent energy constraints of wireless sensor nodes, reducing the power consumption of the main building blocks that make up such systems is critical. Efficient power management circuits, low-power energy harvesting circuits and communication protocols that minimize energy consumption are emphasized.

The energy budget of a sensor interface is highly limited due to the battery size, and most of the major building blocks need to consume sub-nano to micro watt amounts of power [2]–[4], [9], [15]–[17]. Thus innovative circuit techniques are required to reduce the power consumption of these mW-circuit designs by more than 10^6 times. In this section, useful circuit design techniques aimed at improving voltage reference, current reference and amplifier DC biasing are reviewed.

2.1.1 Voltage References

An accurate voltage reference that is insensitive to process, voltage and temperature (PVT) variations is required in many analog and mixed-mode circuits, such as those found in an amplifier or an analog-to-digital converter (ADC). However, conventional band-gap based voltage

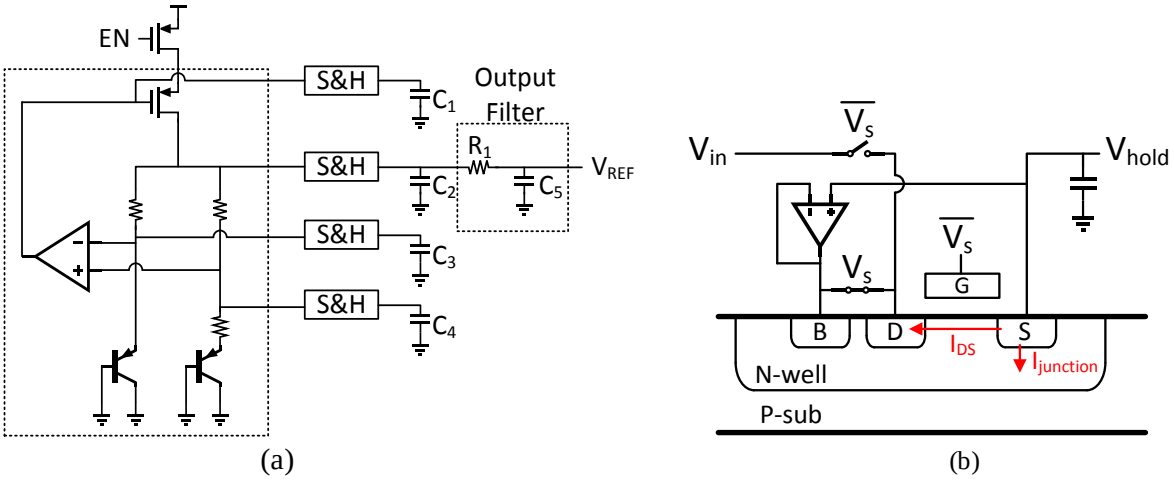


Figure 2.1 (a) A sample-and-hold bandgap circuit proposed in [18]. (b) Schematic of a sample-and-hold switch.

references consume more than 100 nW, making integration into an ultra-low power sensor node system difficult.

The sample-and-hold bandgap proposed in [18] can be a good solution to such problems. As shown in Figure 2.1 (a), the voltages of the bandgap reference are simply sampled at C_1–C_5 and maintained by occasionally enabling the bandgap. The bandgap is heavily duty-cycled so that the on-time of the bandgap is only 0.003% of the off-time. The major factor that determines the minimum duty-cycle is the leakage in the sample-and-hold circuits. The leakage of a sample–and-hold switch consists of the diode leakage of the source-to-body junction and the transistor off-leakage from the source to the drain. These two leakages are minimized by adopting a low power amplifier that biases the drain and body voltages to the source voltage when the sampling transistor is off as shown in Figure 2.1 (b). The proposed work consumes 2.98 nW, which is approximately a 250x reduction, while maintaining the accuracy of the output voltage under temperature and supply variations.

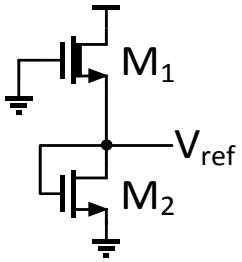


Figure 2.2 A CMOS based voltage reference proposed in [19].

A CMOS-based voltage reference consuming less than 30 pW is proposed in [19]. This work uses two transistors of different sizes, M_1 and M_2, with the sizes shown in Figure 2.2. The output voltage can be calculated by equalizing the current of the two transistors. The subthreshold current of a MOSFET can be calculated using the following equation:

$$I_{sub} = \mu C_{ox} \frac{W}{L}(m-1)v_T^2 e^{\frac{V_{gs}-Vth}{mv_T}}\left(1-e^{\frac{-V_{ds}}{v_T}}\right) \quad (1)$$

where μ, C_{OX}, W, L, V_T, V_{gs}, V_{ds} and V_{th} are the mobility, unit oxide capacitance, width of the transistor, length of the transistor, thermal voltage, gate-to-source voltage, drain-to-source voltage and threshold voltage, respectively. The subthreshold slope factor, m, is expressed as $1+C_d/C_{ox}$ where C_d is the unit depletion capacitance. There exist other sources of static current, such as the drain-induced barrier-lowering (DIBL) current of M_1 and source-to-body junction leakage currents. However, they are typically negligible compared with the subthreshold current. Therefore they are ignored to simplify the solution and provide an intuitive understanding of the operation of the voltage reference. Assuming that V_{ds} is sufficiently greater than V_T so that $\exp(-V_{ds}/V_T)$ can be neglected, the currents though M_1 (I_1) and M_2 (I_2) are as follows:

$$I_1 = \mu_1 C_{ox_1} \frac{W_1}{L_1}(m_1-1)v_T^2 e^{-\frac{V_{th1}-V_{ref}}{m_1 v_T}} \quad (2)$$

$$I_2 = \mu_2 C_{ox_2} \frac{W_2}{L_2}(m_2-1)v_T^2 e^{\frac{V_{ref}-v_{th2}}{m_2 v_T}} \quad (3)$$

Equating (2) and (3) provides V_{ref} as a function of the process parameters as described by the following equation:

$$\mu_1 C_{ox_1} \frac{W_1}{L_1}(m_1-1)v_T^2 e^{-\frac{v_{th1}+V_{ref}}{m_1 v_T}} = \mu_2 C_{ox_2} \frac{W_2}{L_2}(m_2-1)v_T^2 e^{\frac{V_{ref}-v_{th2}}{m_2 v_T}}$$

$$\ln\left(\mu_1 C_{ox_1} \frac{W_1}{L_1}(m_1-1)\right) - \frac{V_{th1}-V_{ref}}{m_1 v_T} = \ln\left(\mu_2 C_{ox_1} \frac{W_2}{L_2}(m_2-1)\right) + \frac{V_{ref}-V_{th2}}{m_2 v_T} \tag{4}$$

$$V_{ref} = \frac{m_1 V_{th1} - m_2 V_{th2}}{m_1+m_2} + \frac{m_1 m_2}{m_1+m_2} v_T \ln\left(\frac{\mu_1 C_{ox_1} \frac{W_1}{L_1}(m_1-1)}{\mu_2 C_{ox_2} \frac{W_2}{L_2}(m_2-1)}\right)$$

Note that the output voltage, V_{ref}, is dependent on the difference between the two threshold voltages and the ratio of the device parameters, making it insensitive to process variation. The optimal device size for minimizing the temperature coefficient (TC) can be determined using the following equation:

$$\frac{dV_{ref}}{dT} = 0 \rightarrow \left(\frac{W_1}{W_2}\right)_{opt} = \frac{\mu_2 C_{ox_2}(m_2-1)/L_2}{\mu_1 C_{ox_1}(m_1-1)/L_1} \tag{5}$$

Note that (4) and (5) are slightly different and corrected versions of equations (3) and (4) in [19].

2.1.2 Current References

The bias current of an amplifier determines its bandwidth. If the bias current is lower than its target, the signal bandwidth is reduced, causing gain attenuation at high frequency. On the other hand, if the current is too large, the noise integration range of the signal is increased unless an accurate filter insensitive to PVT variation is added before the sampling. If the amplifier noise is the dominant noise source, the thermal noise reduction and the noise bandwidth increase cancel

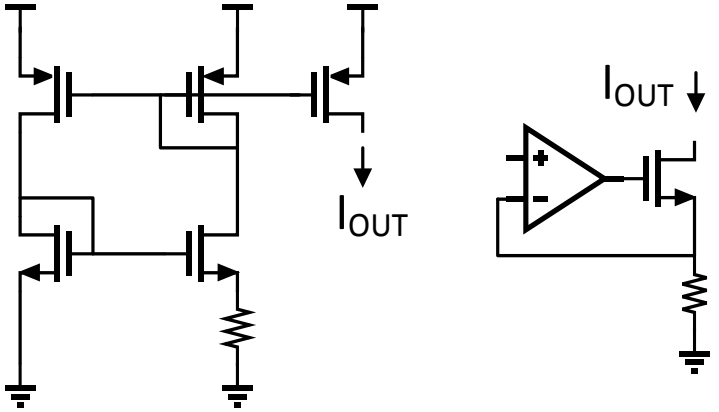


Figure 2.3 Conventional current references (a) constant-g_m (b) resistor regulation.

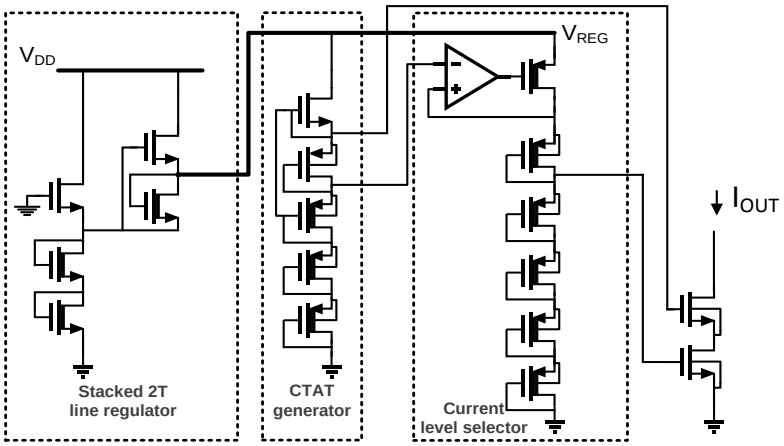


Figure 2.4 A resistor-less current reference proposed in [20].

each other out; thus, the output noise rarely depends on the bias current. However, if the major noise source is the input of the amplifier, an increase in the noise integration range causes a lower signal-to-noise ratio at the output. Energy waste due to the high bias current is another side effect of high bias current. In addition, changing the pole locations can impair the feedback stability of the amplifiers. Therefore, stable bias current generation, insensitive to environmental change, is required.

A current reference is usually implemented using a resistor. Figure 2.3 shows conventional methods used to generate a current reference for a constant-g_m and a current reference using the combination of a voltage reference and a resistor. The challenge of such an implementation in

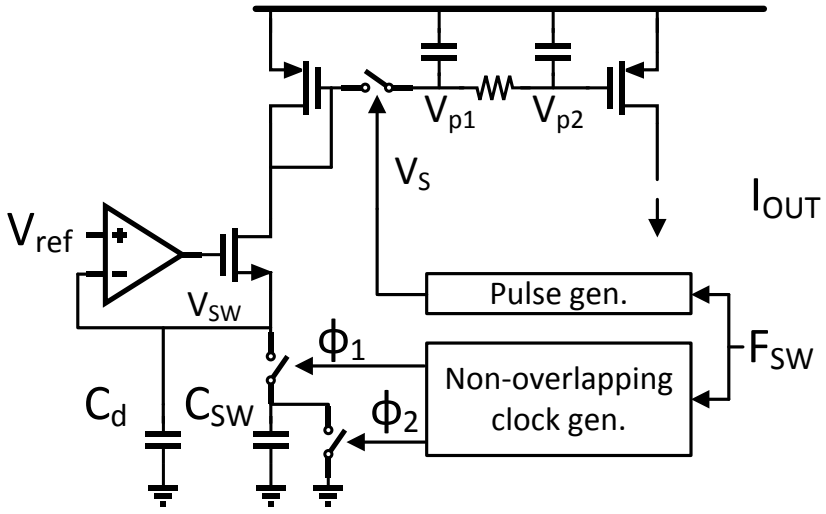


Figure 2.5 A switched capacitor based current reference generation.

ultra-low power sensor nodes is the size of the resistor. Due to power limitations, sensor nodes demand a sub-nA current reference. Thus >100 MΩ is required in order to implement such low current using conventional approaches, which is highly impractical because of the size of the resistor.

[20] proposes a 20-pA resistor-less current reference circuit using a threshold voltage cancellation scheme. A complementary to absolute temperature (CTAT) voltage generator using a diode stack of transistors produces a gate voltage of a subthreshold transistor and compensates for the temperature dependence of the threshold voltage as shown in Figure 2.4. The supply voltage of the CTAT circuit is generated with a 2T voltage reference [19], and its supply dependence is minimized. The output stage is designed with a stack of NMOS transistors to improve the load sensitivity of the output current. The quiescent power consumption of this current reference is 23 pW, which is suitable for low power applications.

Nevertheless, the aforementioned technique relies on precise coefficient matching between the CTAT generator and the NMOS threshold voltage, which is difficult to achieve without multi-temperature trimming. An ultra-low power current reference replacing a resistor with a switched

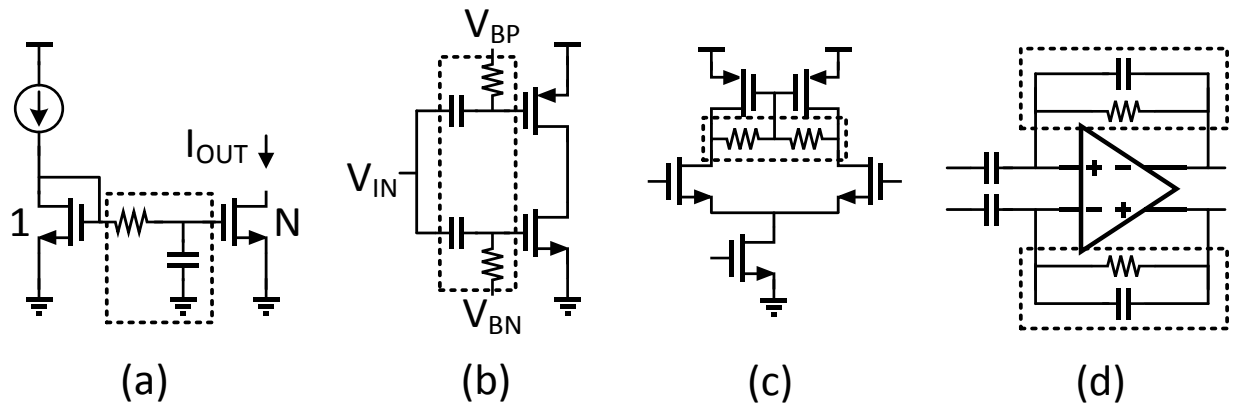


Figure 2.6 Use of pseudo-resistor in (a) noise filtering (b) ac coupling (c) common mode feedback and (d) amplifier servo loop.

capacitor is introduced in [21]. A voltage reference can be implemented in sub-nW power consumption conditions [19]. If stable frequency is available in the sensor node, a stable current reference can be generated by regulating a switched capacitor with a reference voltage as shown in Figure 2.5; its output current is $C_{sw}V_{ref}F_{sw}$. Note that the area occupied by the capacitor is proportional to the output current, making it advantageous for the generation a sub-nW current reference. The voltage ripple generated by the switching operation of the capacitor can be attenuated by the parallel capacitance, C_d, and is further reduced by sampling the mirroring voltage, V_p, with the switching clock or with R-C filtering using a pseudo-resistor. Typically C_d needs to be at least 10 times larger than C_{sw} to sufficiently lower the voltage ripple caused by the switching operation [21].

2.1.3 Resistance Boosting

Often a sensor node measures slowly varying signals, such as voice, pressure or neural signals. Its analog front-end demands time constants of a filter or amplifier that are an order of magnitude larger than the signal changing rate in such cases. A pseudo-resistor, introduced in [22], has been widely adopted to generate very low frequency poles and zeros for low pass filtering, ac

coupling, common mode feedback and amplifier biasing as shown in Figure 2.6 [17], [23]–[26]. A pseudo-resistor can provide a very large resistance with a series of turned-off transistors that occupies only a few micro meter squares. Despite the efficient use of area, the resistance is highly dependent on environmental changes such as temperature and process variations, which makes widespread use of this approach difficult. For instance, in the amplifier biasing circuit shown in Figure 2.6 (d), the small resistance of the pseudo-resistor at high temperature increases the low cut-off frequency, which may even reach the signal bandwidth thereby causing signal attenuation. Furthermore, the current through the resistor is not negligible in such cases, resulting in signal distortion convoluted by the non-linearity of the pseudo-resistor. High resistance also causes side effects such as an increased settling time defined as the time constant of the pseudo-resistance and the parallel capacitance. Sometimes, the resistance is comparable to or even greater than the equivalent resistance of gate and metal-insulator-metal (MIM) capacitors caused by the leakage current due to tunneling, resulting in a shift of the DC operating point.

Adaptive biasing on the gate voltages of the pseudo-resistance has been proposed to improve the robustness of the pseudo-resistance [26]–[28]. The gate voltages of the pseudo-resistances are generated by a bias current combined with a replica transistor to define the impedance of the pseudo-resistor. In such approaches, however, the V_{gs} of the turn-off transistor in the pseudo-resistor varies according to the output voltage, and therefore the linearity becomes worse.

The duty-cycled resistor introduced in [29]–[31] is a viable option for achieving an accurate and linear resistance. Assuming that the switching frequency of a resistor is faster than the frequency of interest, the resistance, usually implemented with poly-silicon or N-well, is boosted

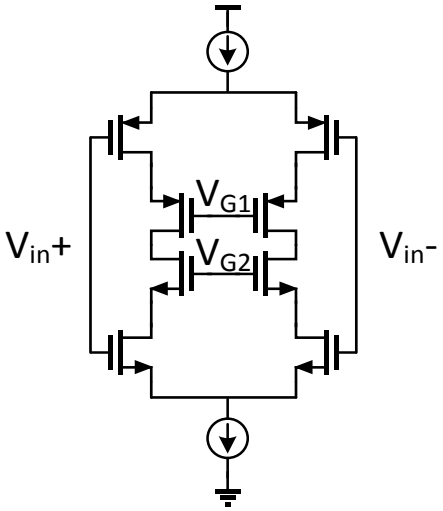


Figure 2.7 A differential current reuse amplifier proposed in [44]

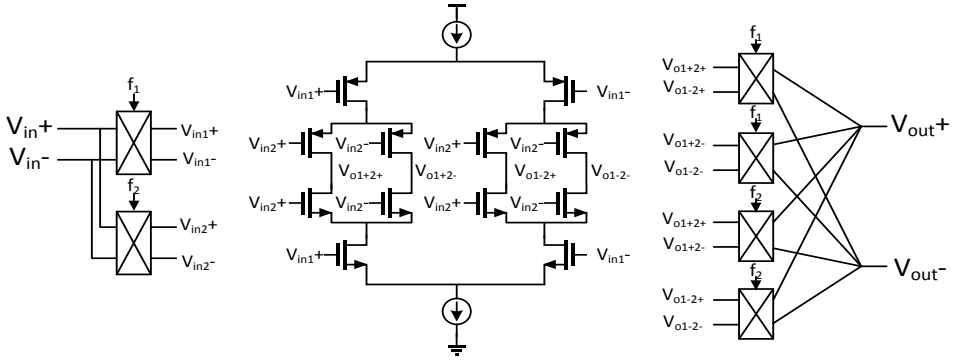


Figure 2.8 A multi-chopper amplifier proposed in [25].

by the factor of the duty cycle. [31] and [30] implemented stable 256 MΩ and 20 GΩ for bias current generation and amplifier biasing, respectively, using on-chip poly-resistors.

A switched capacitor can also provide a large impedance with a small area [32], [33]. The resistance of a switched capacitor is $1/C_{SW}F_{SW}$, as discussed in Section II-B. Therefore, a smaller capacitance and switching frequency, which are advantageous to implement with a smaller area and low power, offer greater resistance. [33] demonstrates a series-parallel charge-sharing technique during the capacitance switching operation that further boosts the equivalence resistance.

2.1.4 Amplifier

The minimum power consumption of an instrumentation amplifier is limited either by the input referred noise or the signal bandwidth, depending on the amplifier specification. Most of the sensor node applications, such as monitoring pressure [34], temperature [2], humidity [35], acceleration [36] or bio signals [17], [22]–[24], [32], [37]–[41], involve slowly varying signals of up to a few kHz; thus, the power consumption is determined by the noise specification rather than the bandwidth. Therefore, it is important to optimize the noise efficiency factor (NEF) of the amplifier, which can be expressed using the following equation [42]:

$$NEF = V_{rms,in}\sqrt{\frac{2I_{tot}}{\pi \cdot V_T \cdot 4kT \cdot BW}} \tag{6}$$

where $V_{rms,in}$, I_{tot}, V_T, k, T and BW are the root-mean-square of input referred noise voltage, total amplifier current, thermal voltage, Boltzmann's constant, temperature and noise integration bandwidth, respectively. NEF indicates the amount of current dissipation required to accomplish an input-referred noise specification. As the noise spectral density at the input of the transistor can be calculated by $4\,kT\gamma/g_m$, the maximization of the transconductance is critical. In this respect, an amplifier using transistors in subthreshold mode is advantageous. The transconductance, g_m, of a transistor is dependent on V_{gs} in strong inversion

$$Strong\ inversion: gm = \frac{2I_{DS}}{V_{gs} - V_{th}} \tag{7}$$

and is maximized when a transistor is in weak inversion[43]

$$Weak\ inversion: gm = \frac{I_{DS}}{V_T} \tag{8}$$

A current reuse scheme that further improves the transconductance is proposed in [44], and a differential version [45] is shown in Figure 2.7. In this scheme, the input voltages are connected to both nmos and pmos differential pairs whose current is shared, so that the devices are connected

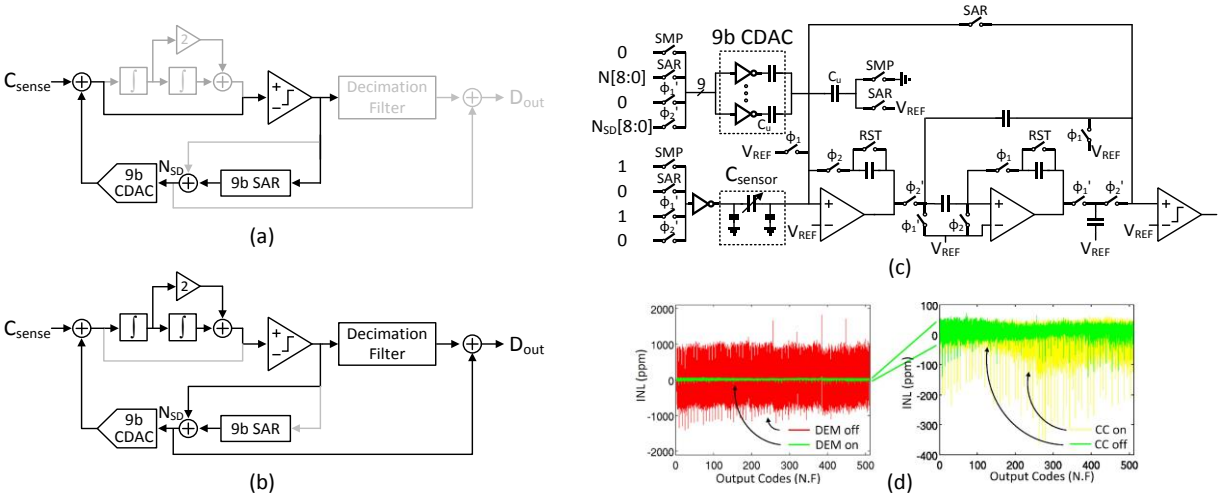


Figure 2.9 An incremental ΣΔ CDC proposed in [49]. (a) SAR mode (b) ΣΔ mode (c) detailed schematic (d) INL measurement with dynamic element matching and common-centroid indexing.

in parallel from an input signal's perspective. Since the transconductance is increased to $g_{mn}+g_{mp}$ while the current remains constant, the input referred voltage noise can be reduced compared to the single-input-pair implementation. This architecture has been widely adopted in instrumentation amplifiers targeting low NEF.

[25] proposes a multi-chopper amplifier that utilizes the excessive bandwidth to reduce the NEF. As noted in the previous paragraph, the current of the amplifier is sufficiently large to reduce the input referred noise, causing excessive bandwidth at the output. This work mixes the input signal to the unused bandwidth using f_1 and f_2 and then reconstructs the signal at the output as shown in Figure 2.8. This work achieved the lowest NEF of 1.38.

Table 2.1 Performance summary of state-of-the-art CDCs.

	[48] Y. He ISSCC 2015	[48] Ha, ISSCC 2014	[49] Oh, VLSI 2014	[16] Oh, ESSCIRC 2014	[35] Tan, JSSC 2013	[46] Xia, ISSCC 2012	[50] Nizza, TCAS-I 2013
Method	PM	SAR	IΣΔ	Dual Slope	ΣΔ	ΣΔ	PM
Power (μW)	14	0.16	33.7	0.11	10.3	14900	84
Input Range (pF)	0 – 8	2.5-75.3[2]	8.4-11.6	5.3-30.7	0.54-1.06	8.4-11.6	0.5-0.76
Meas. Time (ms)	0.21	4	0.23	6.4	0.8	20	0.033
Resolution (Crms, aF)	1443	6000	156	-	70	65	800
SNR (dB) [1]	65.57	60.6	94.7	44.2	68.4	84.83	40.9
FoM (pJ/step)	1.87	0.54-1.3[3]	0.18	5.3[3]	3.8	21	0.52
Area (mm^2)	0.05	0.49	0.456	0.105	0.28	2.6	98
Technology	0.16μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.16μm CMOS	0.35μm CMOS	0.32μm CMOS

[1] $\mathrm{SNR} = 6.02 \times \mathrm{ENOB} + 1.76$
[2] Composed of 8 subranges
[3] FoM with one subrange

2.2 Sensor Interface

2.2.1 Capacitive Sensor Interface

To implement an ultra-low power sensor node, it is important to reduce the power consumption of the sensor itself. Capacitive sensors are suitable in this respect because the capacitive sensors do not consume static current [34]. Many papers have been published utilizing low power capacitive sensors to monitor parameters such as pressure [16], humidity [35], acceleration [36] and displacement [46].

One of the key challenges of such capacitive sensors is the dynamic range of the signal [35], [46]–[50]. The sensors provide up to tens of pF of base capacitance but require aF accuracy to precisely read out the information. Therefore, the delta-sigma modulation method is advantageous for high accuracy applications [35], [46]. However, such an approach requires relatively high power consumption. Figure 2.9 shows a recently published incremental ΣΔ CDC with zoom-in 9-bit asynchronous successive approximation (SAR) [49]. The energy efficiency of the CDC is improved by lowering the oversampling ratio (OSR) through the pre-calibration of the

Table 2.2 Performance summary of analog front-end circuits for neural recording application

	[56] Muller, ISSCC 2014	[30] ChandraKumar, ISSCC 2016	[57] Ng, ISSCC 2015	[58] Lopez, ISSCC 2013	[59] Walker, VLSI 2011	[60] Majidzadeh, TBCAS2011	[61] Abdelhalim, JSSC 2013
Power (μW/ch)	2.3	2	2.8	10.48	68	7.l92	10
Supply (V)	-	1.2	1	1.8	1.2	1.8	1.2
Recoding Signal	ECoG	AP + LFP	AP	AP+LFP	AP+LFP	AP	AP+LFP
Bandwidth (Hz)	500[1]	1-5000	1-8200	0.5-6000	280-10000	10-7200	1-5000
Max Input Offset (mV)	100	40	220	-	15	5.7	-
Input referred Noise (μV)	1.3[1]	2[2] - 7[3]	4.2	3.2[4] – 5.8[5]	2.2	3.5	5.1
Input Impedance (MΩ)	28	300	-	-	-	-	-
NEF	4.76	7[2] – 4.9[3]	2.93	2.72	4.5	3.35	4.4
PSRR (dB)	67	-	78	76	-	63.8	-
CMRR (dB)	88	-	80	60	-	70.1	78
THD (dB)	-	-74	1 (%)	1 (%)	-	1 (%)	-50
Area (mm^2)	-	0.071	0.042	-	0.26	0.0625	-
Technology	0.065μm	0.04μm	0.065μm	0.18μm	0.13μm	0.18μm	0.13μm

[1] Calculated from Fig. 24.1.4
[2] Measured in LFP mode (1-200Hz)
[3] Measured in AP mode (200-5000Hz)
[4] Measured in AP mode (300-6000Hz)
[5] Measured in LFP mode (0.5-200Hz)

capacitance range using 9 bit SAR operating with a capacitive digital-to-analog converter (CDAC). Initially, the integrators are disabled, and the CDAC voltage is directly connected to the comparator to perform a SAR search of CDAC, as shown in Figure 2.9 (a). After the SAR phase, ΣΔ CDC is activated and generates a bit stream of the capacitor comparison result, as shown in Figure 2.9 (b). The detailed schematic of the CDC is shown in Figure 2.9 (c) and consists of two OTAs, one comparator, a 9-bit CDAC and switched capacitor circuits. This work includes the energy efficient dynamic element matching (DEM) method to improve the linearity of the 9-bit CDAC, and the common centroid layout of the capacitor further improves the linearity, as shown in Figure 2.9 (d). The performance of this work and the state-of-the-art CDCs are summarized in Table 2.1.

2.2.2 Bio-signal Monitoring

Bio-signal monitoring SoCs represent one of the most prominent areas of circuit applications in the last decade. The development of bio-signal sensors for use in personal healthcare is expected to greatly improve the quality of human life and help with early detection of disease. For instance, real-time monitoring of electrocardiography (ECG) is an effective method for the diagnosis and study of heart disorders such as arrhythmia [17]. Neural signal monitoring from various regions of the brain enables the detection of neurological disorders such as epilepsy, schizophrenia, Alzheimer's disease, Parkinson's disease and autism [51].

[52] proposed a non-invasive multi-sensor acquisition system with simultaneous ECG, bio-impedance (BIO-Z), galvanic skin response (GSR) and photoplethysmogram (PPG) monitoring. The multi-parameter recording provides a more accurate and reliable health assessment in a comfortable wearable device.

There has been high demand for technologies to enable simultaneous monitoring of a large number of neurons, and multi-electrode neural recording is becoming standard practice [22], [33], [37], [40], [41], [53]–[61]. In this way, it is possible to gather enough information from a specific part of the brain related to motor planning and control, enabling direct control of a robotic manipulator by cortical neurons.

The read-out circuits must be designed to consume ultra-low power in order to avoid tissue damage caused by heat. The area is another challenge of the read-out circuits. The read-out circuit needs to provide sufficient immunity to the environmental noise caused by the electrochemical

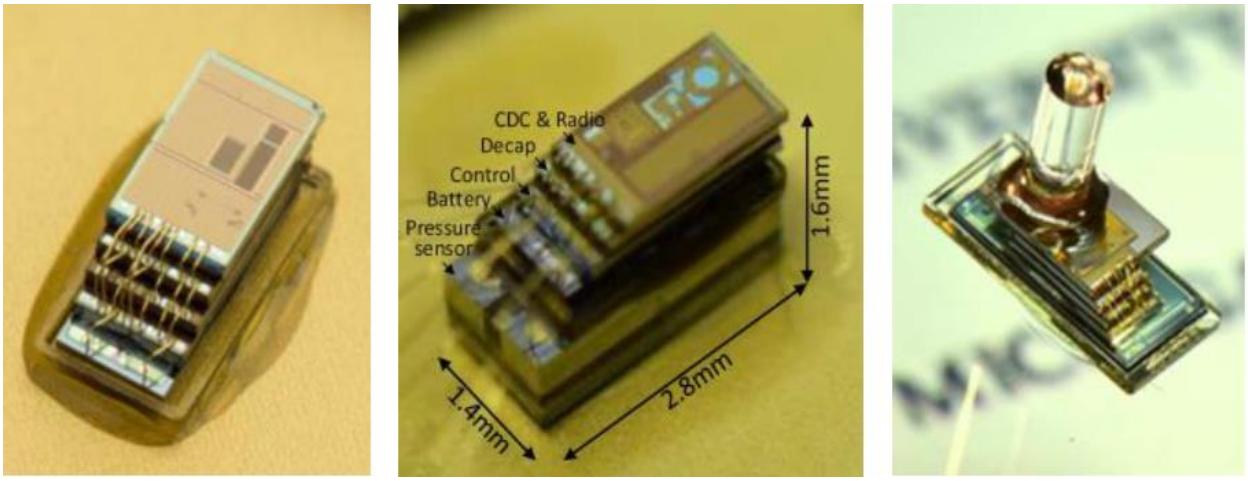


Figure 2.10 Examples of mm-scale sensor nodes for (a) temperature, (b) pressure, and (c) image sensing.

behavior of its surroundings, requiring a high power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR). The input referred noise specification is also challenging. The peak spike voltage of the action potential (AP) of a neuron is 50-500 μV in the 0.1-700 kHz frequency range [62]. Therefore, 2-3 μV_{rms} input referred noise is demanded for neural recoding read-out circuits. The amplitude of the local field potential (LFP) can be as high as 5 mV [63], but its ultra-low frequency near sub-Hz makes it difficult to meet the noise specification due to the large device flicker noise. Pseudo-resistors are widely used to implement large time constants, and the current reuse technique is useful for minimizing power consumption while meeting a low noise specification.

2.2.3 Modular Design

Ultra-low power sensor nodes can be used in a wide variety of applications, but the basic operation mechanisms are similar, requiring common building blocks such as a wake-up timer, RF or optical communication, an energy harvester and a power management unit. Therefore, the modular design of each functional block can reduce the development time, verification overhead

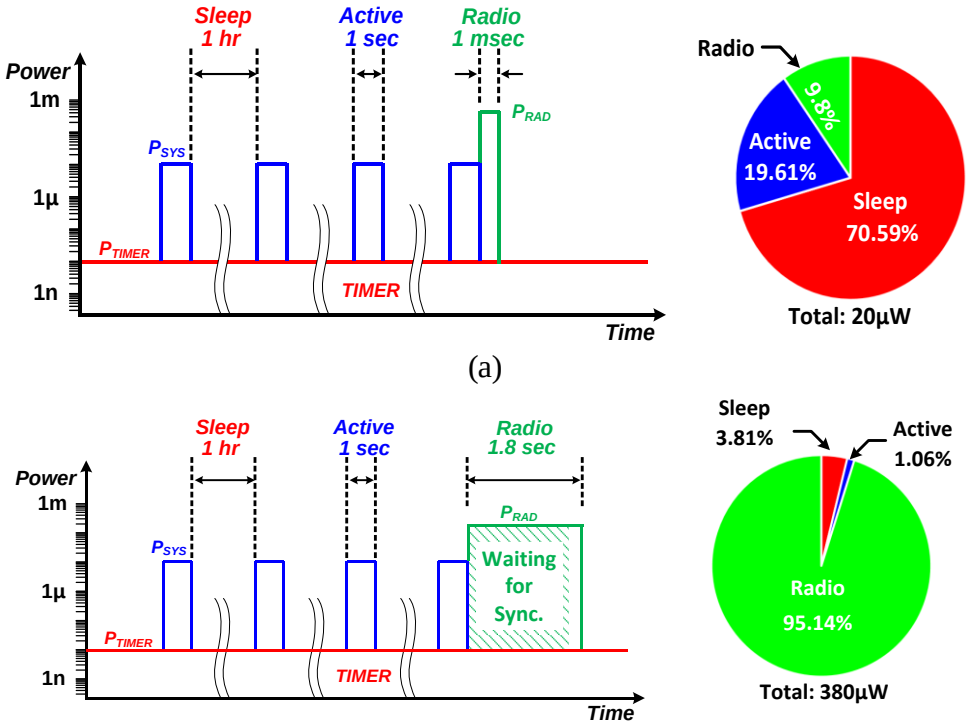


Figure 2.11 Timing diagrams of a wireless sensor node (a) without timing uncertainty (b) with timing uncertainty.

and manufacturing cost. Figure 2.10 shows millimeter-scale wireless sensor node designs for temperature monitoring [2], pressure monitoring [16] and imaging [4] developed based on a generic sensing platform [3].

2.3 Timing Reference

The reduction of sleep power is critical to make a system sustainable with limited harvested energy. Wake-up timers are a key always-on building block that can dominate the sleep power. Therefore, a wake-up timer must be designed with a stringent power budget [21], [64]–[69]. A highly accurate timing reference is also important if the sensor node is required to maintain synchronization for peer-to-peer or asymmetric communications. As an example, Figure 2.11 (a) shows a timing diagram of two wireless sensor nodes that need to communicate with each other.

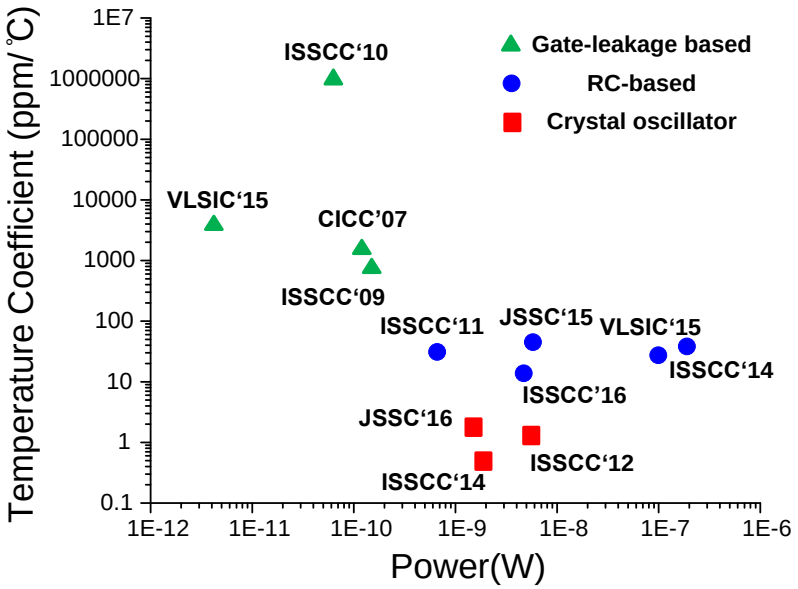


Figure 2.12 Summary of temperature coefficients and the power consumption of the recently published on-chip oscillators.

Each sensor node sleeps for an hour and then wakes up for 100 ms to collect and process data. The data is transmitted every 4 hours. The power consumptions during sleep, active and radio modes are 10 nW, 10 uW and 2 mW, respectively. In this case study, the energy consumption in the sleep mode is the dominant factor, emphasizing the need for an ultra-low power wake-up timer. In contrast, the energy loss due to timing uncertainty is more pronounced with the presence of timing mismatch, as shown in Figure 2.11 (b). When the temperature coefficient is 50 ppm/°C, and the temperature difference is 10°C, the timing uncertainty is 500 ppm, which corresponds to 1.8 sec. This timing uncertainty causes significant energy loss for a sensor node that has to keep transmitting data until its peer responds.

A crystal oscillator is a viable option to achieve such aggressive power and accuracy specifications. Recently, a pulsed driver technique published for 32-kHz crystal oscillators reduced power consumption drastically, allowing crystal oscillators to provide an accurate frequency of less than 100 ppm across wide PVT variations while consuming only a few nanowatts [70], [71].

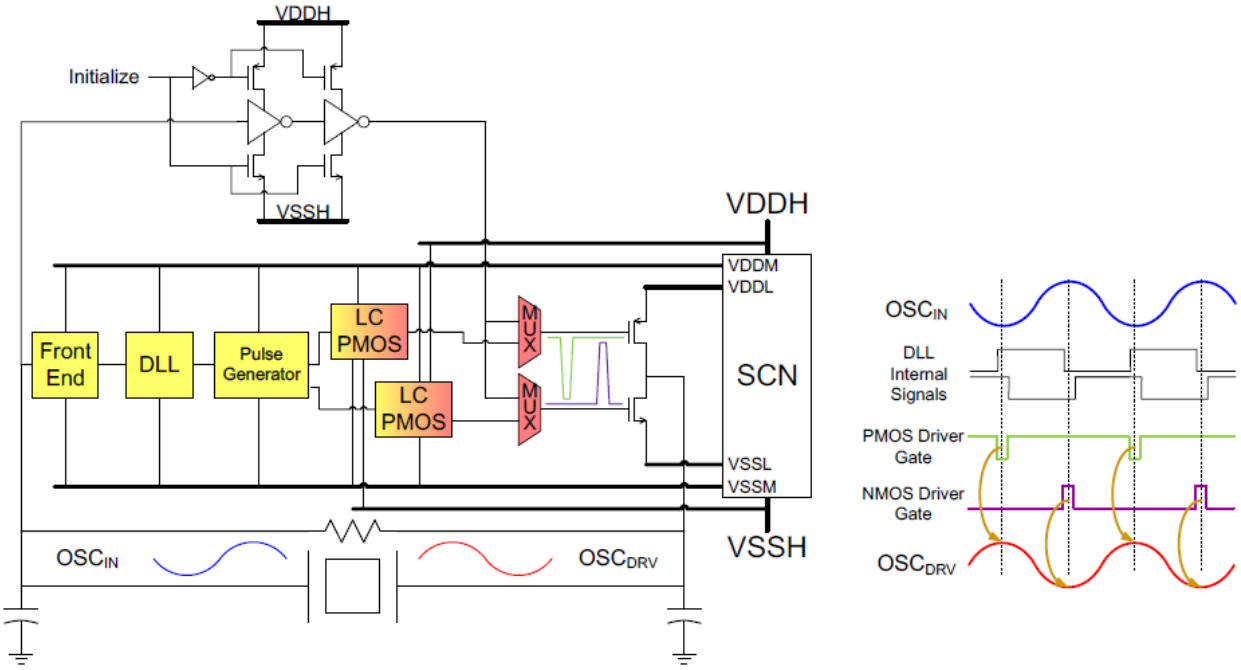


Figure 2.13 Block diagram of a pulse injection based crystal driver proposed in [70].

However, crystal oscillators require an off-chip component, which is difficult to integrate in a millimeter-scale sensor node [67].

On-chip clock generation techniques are useful when the system may allow frequency uncertainty higher than 500 ppm. Figure 2.12 shows the power consumption of recently published on-chip oscillators and their temperature coefficients. Gate leakage-based oscillators offer sub-nW power consumption. However, their oscillation frequencies can be as low as a few hertz, and the frequency uncertainty is very high (>10,000 ppm). Relaxation oscillators using an R-C time constant generally offer moderate temperature coefficients of tens of ppm/°C with nanowatt to microwatt power consumption.

In this section, we will discuss recent developments in crystal and on-chip oscillators and discuss their advantages with respect to use in millimeter-scale wireless sensor nodes.

2.3.1 Crystal Oscillator

Conventionally, a crystal resonator is driven by an inverter-based amplifier in series with a resistor. However, there are many sources of energy waste in such architectures. Most notably, the inverter consumes static power due to the sinusoidal input voltage. The series resistance also dissipates a significant amount of power due to the large voltage imposed on it. A current-starved driver is proposed to minimize the static power and eliminate the series resistor [72]. The limited oscillation amplitude achieved using the current-starved driver reduces the power consumption drastically, but power consumption remains higher than 27 nW [72], [73], which is too large for integration into recent millimeter-scale wireless sensor nodes consuming less than 10 nW during sleep mode [3], [74].

A pulsed driver for an ultra-low power crystal is proposed in [70], [75]. Figure 2.13 shows a simplified circuit diagram of the crystal driver. One of the crystal voltages, OSC_{IN}, is amplified and delivered to a delay-locked loop (DLL). The DLL generates two narrow pulses that are located at the peaks of the crystal voltages, OSC_{IN} and OSC_{DRV}. Then, a level converter shifts those pulses to a higher magnitude, and M_{P1} and M_{N1} are driven by the pulses. There are several advantages provided by this architecture in terms of power consumption. First, the crystal amplitude is restricted to 180 mV, which reduces the power consumption of the crystal series resistance. Second, the static power consumption of the driver switches is very low because the transistors receive rectangular pulses, and only one of M_{N1} and M_{P1} is enabled so that the leakage current though each transistor is very small. Third, the driver switch is only enabled when OSC_{DRV} reaches its peak voltage. Therefore, the voltage across the driver switches is small, and most of the energy derived from the supply, E_{VDD}, is delivered to the crystal to regenerate the waveform. According to eq. (19) and Fig. 12 in [70], when the drivers are properly sized, approximately 90% of the energy is used

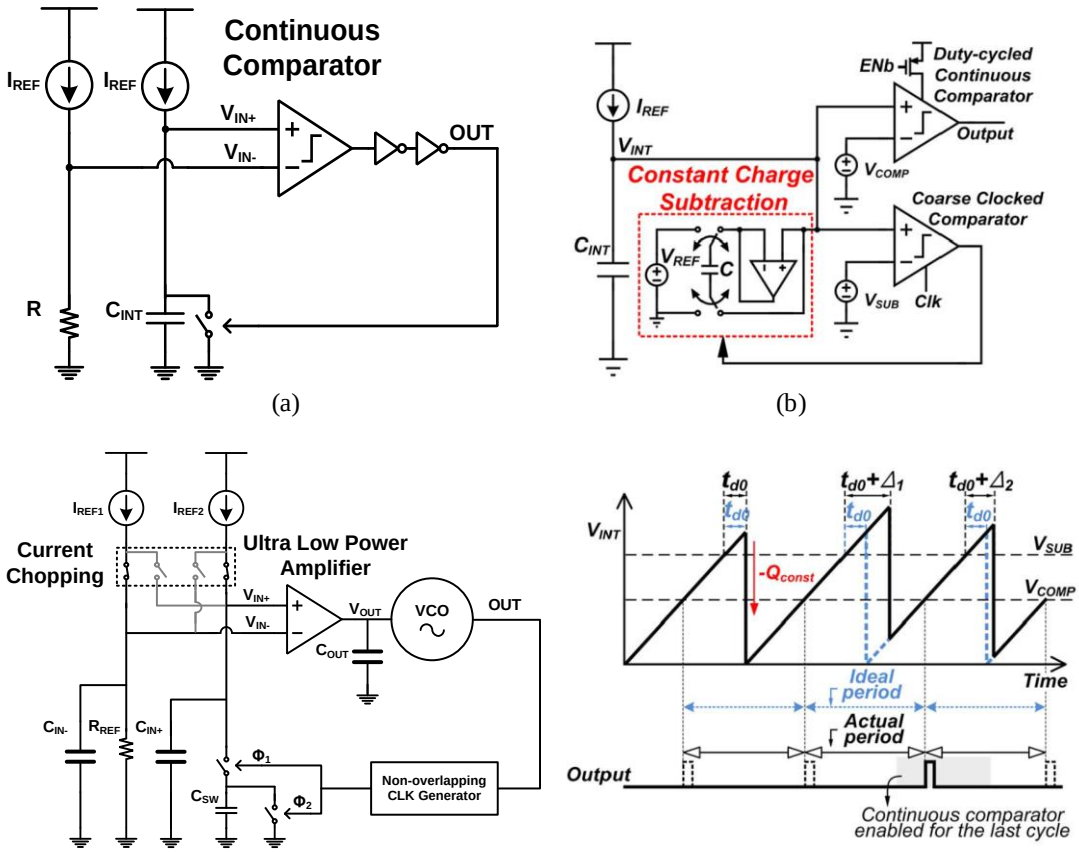


Figure 2.14 (a) Conventional on-chip oscillators (b) An R-C oscillator using constantrror charge subtraction proposed in [63] (c) A timing diagram of the oscillator [64] (d) A resistive frequency-locking scheme proposed in [67].

to regenerate the waveform of the crystal, and only 10% is dissipated by the driver circuit. With the supplementary circuits of a DLL, amplifier, pulse generators and level converters, this work achieved 5.58 nW power consumption, which is a 4.8x reduction compared with prior works.

2.3.2 On-chip Oscillator

Conventionally, on-chip oscillators are developed using a time constant provided by a monolithic resistance and capacitance pair as shown in Figure 2.14 (a). The frequency of the oscillator is dominated by the R-C time constant but still affected by the comparator, buffer and

reset switch delay, all of which are known to be temperature-dependent. Therefore, the delay caused by the supplementary components needs to be negligible compared with the R-C delay, which consumes a substantial amount of power.

[64] introduces a constant charge subtraction method to eliminate the frequency dependency stemming from the comparator delay as shown in Figure 2.14 (b). A constant current, I_{REF}, generated by a temperature-compensated resistor is provided to an integration capacitor, C_{INT}. Instead of the conventional approach of fully discharging the capacitor, a constant amount of charge, $V_{REF} \times C$, is subtracted from C_{INT} when V_{INT} exceeds V_{SUB}. Therefore, the voltage drop by the charge subtraction operation is always $V_{REF} \times C/C_{INT}$, and thus the time moment that V_{INT} crosses V_{COMP} is independent of the comparator delay. The output frequency is generated using a duty-cycled continuous time comparator.

[67] introduces a resistive frequency-locking method that eliminates the comparator as shown in Figure 2.14 (d). In this architecture, the impedance of a switched capacitor is equalized to a temperature-compensated resistor by using a frequency-locked loop implemented with an ultra-low power amplifier. A wake-up timer that further reduces the power consumption using a frequency-locked loop and a duty-cycled resistor is proposed in [21].

The performances of recently published low power on-chip oscillators are summarized in Table-III.

2.3.3 Frequency Synthesizer

A simple ring oscillator used as a frequency generator is acceptable in a processor despite the wide frequency variations observed in response to environmental changes. This observation is true because the throughput of a sensor node is determined by the sensor interface circuits rather than the processor speed. However, the change in the processor frequency results in increased

energy consumed by the processor core because the active time is usually determined not by the workload of the processor core but by the sensor signal acquisition time. Therefore, the core frequency needs to be stabilized by locking it to an accurate wake-up timer.

A phase-locked loop (PLL) using a frequency reference generated by either a crystal or wake-up oscillator is a viable option to reduce the power overhead caused by excessive frequency. A charge-pump PLL, which is the most generic architecture for SoC clock generation, is not well suited for this purpose for several reasons. First, the VCO frequency tuning range is limited due to the low supply voltage. Many wireless sensor nodes operate with a supply voltage close to the MOS threshold voltage to reduce power consumption [76]. Under these conditions, the control voltage range is very limited because of the small charge pump output range resulting from the low supply voltage. Furthermore, the delay cells in the VCO operate in a subthreshold region in order to generate low frequencies, resulting in wide frequency variations depending on the temperature and process changes, thereby requiring an even larger control voltage range to compensate for the frequency change. Second, the size of the loop filter consumes a substantial amount of space. A sensor node wake-up timer typically generates only a few kHz to minimize its energy overhead during the sleep period. The loop bandwidth of a PLL should be smaller than one-tenth of the reference frequency [77] and result in either a very small charge pump current or a very large loop filter capacitance. On the other hand, a digital PLL scales well to the lower loop bandwidth as its loop filter coefficients are represented as digital values. For example, a digital loop filter of an all-digital PLL receiving 32kHz reference clock [78] is implemented with 14-bit words and its area occupation is 7-to-56x smaller compared to the analog implementation mostly due to the absence of the analog loop filter ([78], Table-V). Also, the DCO frequency tuning range is less affected by the low supply voltage. In addition, the frequency tuning code of a digital PLL

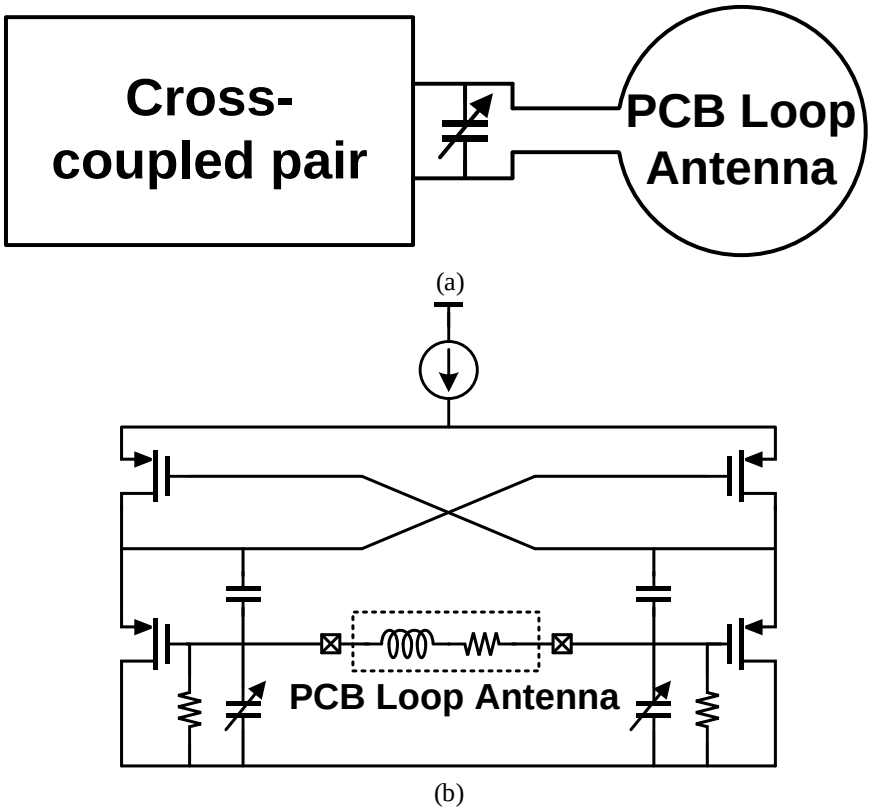


Figure 2.15 (a) Conceptual diagram and (b) Schematic of a power oscillator [11]

can be easily stored in memory and can be directly used when the system wakes up from sleep mode, reducing the lock time. Therefore, a digital PLL is better suited for the frequency synthesizers in miniaturized systems.

2.4 Data Communication

Many wireless sensor node applications require that the size be less than a cubic cm, sometimes nearing a cubic mm. Therefore, there is a basic challenge of degraded antenna radiation efficiency for RF communication due to the small form factor [79]–[85]. Furthermore, an active radio system requires a battery, power management unit, accurate timing reference and processing unit, which are usually too bulky to be integrated into a miniaturized sensor node. Small passive RF tags (12 mm^3) [86] can be an alternative solution to the relatively large active radios. However, the functions of passive RFID tags are limited due to the lack of an integrated power source [87].

Therefore, circuit techniques as well as integration methodologies that will facilitate the miniaturization of the necessary circuit building blocks are critical.

In contrast, optical communication using a light-emitting diode (LED) as the transmitter and a photovoltaic (PV) cell as the receiver can be implemented with high efficiency using very little space, making this approach suitable for line-of-sight (LoS) communication. For instance, LEDs smaller than 0.08 mm^2 are commercially available, and photovoltaic cells can be as small as 0.07 mm^2 [88].

2.4.1 RF Communication

Conventional RF transmitters include a local oscillator (LO) and a power amplifier. An LO is usually implemented using an accurate frequency reference (crystal oscillator) and a phase-locked loop. Although an accurate LO enables advanced communication protocols, certain characteristics make it unsuitable for use in an ultra-low power sensor node. First, the crystal requires a start-up time on the order of milliseconds [89]. This long start-up time wastes a substantial amount of energy because the system is in active mode during this time. The lock time of phase-locked loop (PLL) also contributes to the loading time and therefore also to the energy waste. Second, the base power consumption of such architecture is high due to the limited Q-factor of the monolithic inductor and the complex building blocks. Therefore, there is a need for simpler transmitter architecture.

[10] introduces a minimum-shift keying (MSK) transmitter consuming 350 μW and using a power oscillator as shown in Figure 2.15. The proposed architecture employs a loop antenna on a printed circuit board (PCB) as a resonating component together with an on-chip capacitor array. Several advantages are gained by eliminating the PA and directly resonating the PCB antenna with a negative-gm circuit. The small form factor of an antenna typically results in a high quality factor,

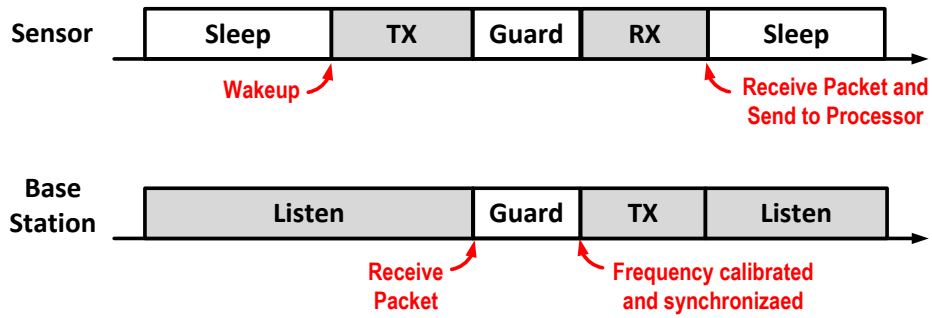


Figure 2.16 A sensor-initiated synchronization protocol proposed in [10], [16] and [23]

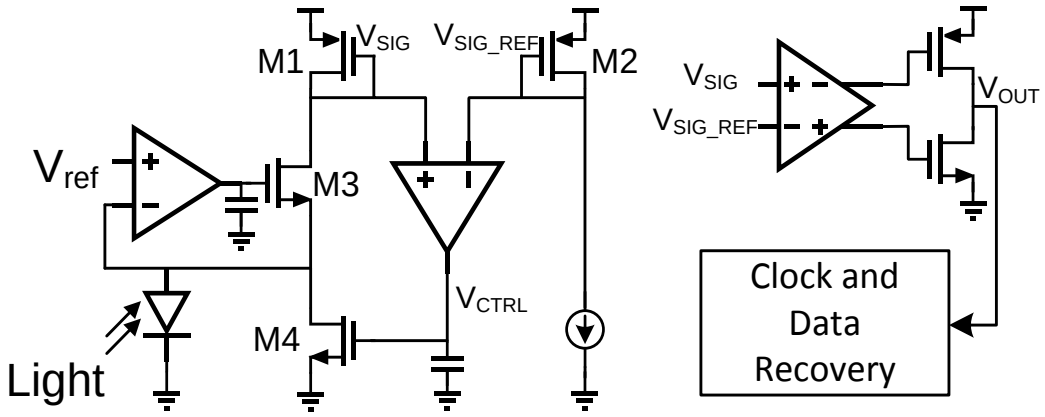


Figure 2.17 Schematic of a background noise cancelling GOC receiver proposed in [24]

and low radiation resistance results in low radiation efficiency [10]. If a conventional power amplifier drives the antenna, the small frequency difference between the carrier frequency and the antenna resonant frequency should cause a drastic reduction in the efficiency of the power amplifier. In contrast, if the antenna is directly resonated in the power oscillator, there is no other frequency component to cause frequency offset. The absence of an LO and power amplifier further reduces power consumption and space requirements. When there is asymmetry in the power and space budget of the sensor node and the base station, the frequency inaccuracy of the power oscillator-based transmitter is compensated in the base station. The power oscillator-based wireless transmitter for sensor node applications is adopted in [11], [90], [91], asserting its benefit.

A complete system including a 2.4-GHz radio transmitter for a medical implant application is proposed in [9], [11]. This work's goal is to operate the transmitter with less than 1 nW energy

harvested from the Endocochlear Potential (EP), which is an electrochemical gradient in the inner ear. This energy limitation restricts the system's average power consumption to 250 pW. To meet such an extreme energy constraint with a small antenna whose radiation efficiency is as low as 0.8%, the system is deeply duty-cycled (0.00002%) and employs an energy harvester with ultra-low quiescent power consumption (544 pW). By assuming that a base station, such as a smart phone or a smart watch, is placed nearby, the communication distance can be restricted to one meter, which helps to reduce the transmitter power. The carrier frequency is also one of the important factors that determine the transmitter power. Due to the small antenna size, a higher carrier frequency is preferred to maximize the radiation efficiency. However, a higher carrier frequency causes larger tissue absorption of the RF signals. [11] reports quantitative research on the antenna efficiency in several Industrial, Scientific, and Medical (ISM) bands and identifies 2.4 GHz as the optimal frequency to minimize the transmitter energy considering both radiation efficiency and tissue absorption.

The next area of potential improvement in the energy efficiency of an ultra-low power radio is a sensor-initiated protocol. Due to the aforementioned energy overhead as well as the size, crystal oscillators are difficult to integrate in a sensor node. The lack of an accurate timing reference in a sensor node forces the inclusion of a wake-up receiver so that the sensor node can wake up at appropriate times to enable its data radio [8]. However, such a wake-up receiver still consumes at least tens of microwatts, limiting the number of sensor node applications that can exploit a wake-up receiver [8], [92]–[95].

A sensor-initiated synchronization protocol to address this is proposed in [87], [91], [96]. Figure 2.16 shows a simplified timing diagram of sensor-initiated synchronization. Initially, a sensor node is in sleep mode, and the base station is in listening mode, waiting for a header from

the sensor node transmission. The sensor node then transmits its acquired data using pulse position modulation (PPM). The data interval of the data packet indicates the frequency of the timer in the sensor node. Then, the base station prepares data to send during the guard time. This guard time is determined by the frequency of the timer in the sensor node so that the sensor node can initiate its receiver exactly when the base station begins the transmission, thereby removing complex base band processing traditionally needed to accommodate the frequency uncertainty of the sensor node and saving power.

2.4.2 Optical Communication

An optical receiver can be much smaller and more power-efficient than that required for RF communication when the communication distance is less than a meter, and the sensor node is located in line-of-sight [88], [97]. Optical receivers adopt a PV cell as a light receiver, which can be integrated in a CMOS die [88] or energy harvester using light [97]. Therefore, such a system can be as small as a cubic mm due to the absence of an RF antenna [2]–[4], [7], [16]. Another advantage of an optical receiver compared with its RF counterpart is the power consumption and the energy-per-bit. A wake-up receiver can consume less than one nW [88], [97], which makes it suitable for use in a mm-scale wireless sensor node, and the energy-per-bit is less than 100 pJ/b, which is over 20-fold less than that of RF receivers.

However, the presence of background light sources such as sunlight, incandescent light and fluorescent light may perturb the communication, resulting in an inferior bit rate. [97] proposes a dual-mode optical receiver that enables sub-nW asynchronous wake-up, a programmable data rate and background light tracking. A simplified circuit diagram of such a receiver is shown in Figure 2.17. Assuming the background light is changing slowly, the background light cancellation loop subtracts the current generated by the background light, I_{NOISE}, from the total output current

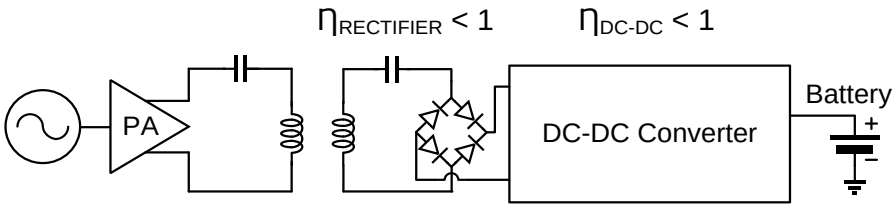


Figure 2.18 Block diagram of the conventional wireless transfer circuits

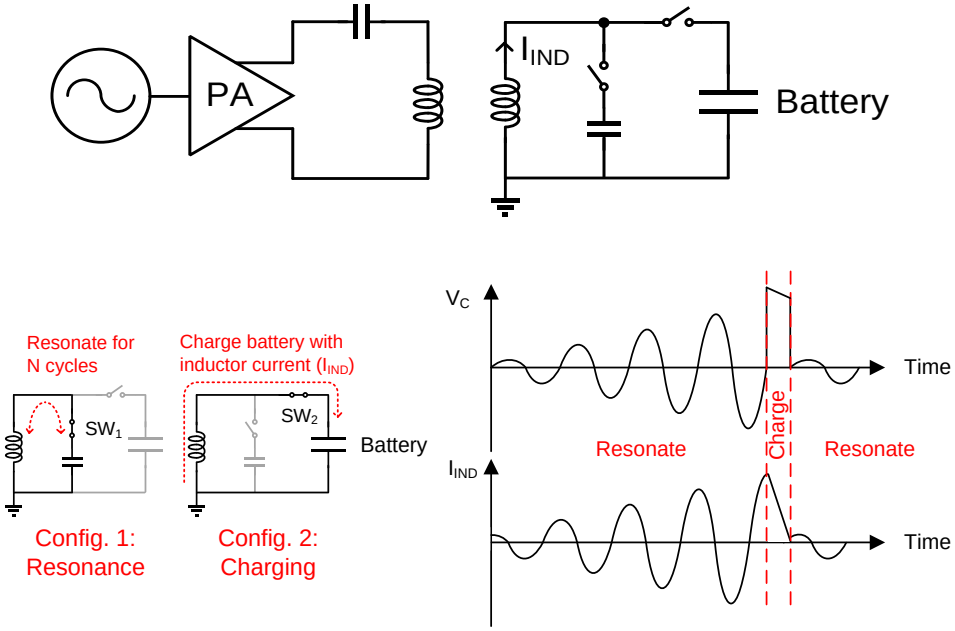


Figure 2.19 A current mode resonant power receiver proposed in [31]. (a) schematic (b) switch configuration (c) voltage and current waveforms

from the PV cell. A fast switching current is then delivered to M1 of Figure 2.17 to be compared with the voltage reference. The signal voltage is amplified by the post amplifier stages, and the data are recovered after oversampling the resulting digital output. Another advantage of this circuit is the maximum bit rate of the signal. A voltage mode optical receiver [88] has a bandwidth limitation that originates from the capacitance-to-current ratio of a PV cell, which is physically constrained. On the other hand, the circuit demonstrated in [97] adopts a current mode architecture in which the diode voltage is regulated to a voltage reference, V_{REF}. The anode of the PV cell,

V_{DIODE}, is virtual ground, so the maximum speed of the receiver is determined by the input impedance of the voltage regulation loop.

2.5 Energy Harvesting

Minimum harvestable input power ($P_{in,min}$) is a critical factor for a miniaturized sensor node to sustain its operation with a duty-cycled operation. Assuming that the system is at a steady state where the input power is equal to the used power, the duty cycle of the system can be determined as the following:

$$\eta_h P_{in} \cdot \left(t_{active} + t_{sleep}\right) = P_{active} \cdot t_{active} + P_{sleep} \cdot t_{sleep}$$
$$\text{Duty Cycle} = \frac{t_{active}}{t_{sleep} + t_{active}} = \frac{\eta_h P_{in} - P_{sleep}}{P_{active} - P_{sleep}} \quad (9)$$

where η_h, P_{in}, P_{active}, P_{sleep}, t_{active} and t_{sleep} are harvester efficiency, input power, active mode power, sleep mode power, active time and sleep time, respectively. It can be seen that a sensor node may sustain its operation as long as the acquired power ($\eta_h \cdot Pin$) is larger than P_{sleep}.

On the other hand, the input power of a miniaturized sensor node is highly constrained due to its small form factor. In this section, we discuss circuit techniques to improve the $P_{in,min}$ and η_h when inductive coupling and photovoltaic cells are used.

2.5.1 Inductive Coupling

Conventional wireless power receivers are designed with a voltage rectifier and a DC-DC converter as described in Figure 2.18. The threshold voltage of the diodes in a voltage rectifier sets the minimum voltage level that the inductive antenna needs to provide, requiring higher input power. In addition, the limited efficiency of the DC-DC converter degrades the efficiency of the harvesters [98].

A resonant current mode wireless power receiver minimizes the energy loss caused by the voltage mode rectifier and the DC-DC converter [99]. Figure 2.19 shows a block diagram of the

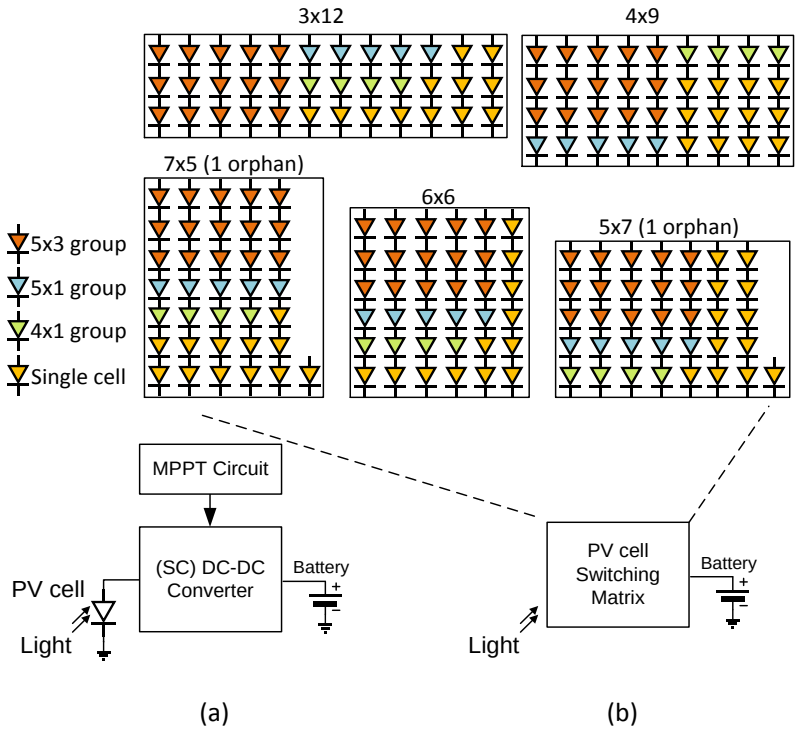


Figure 2.20 (a) Conventional light energy harvester using a PV cell. (b) A reconfigurable PV-cell network proposed in [32].

proposed work, which places a capacitor in parallel with a receiver coil, forming an LC resonator. The received energy accumulates in the parallel LC resonator for multiple cycles and is transferred to a battery in current mode. The transient signal waveform of the voltage of the LC resonator, V_C, and current in the receiver coil, I_{IND}, are plotted in Figure 2.19. The switch that connects the receiver coil to the battery (SW_2) is enabled when the coil current reaches its peak, i.e. all the resonation energy is stored in the inductor as a magnetic field. After the inductor current reaches zero, SW_2 is disabled, initiating a new accumulation of energy in the resonator. This work improves $P_{in,min}$ by eliminating the energy loss caused by the voltage rectifier and the DC-DC converter. The number of accumulation cycles is tunable so that the LC resonator accumulates energy for more cycles when the input power is low, building up enough energy to overcome the

energy loss during the battery charging operation, further improving $P_{in,min}$. The reported $P_{in,min}$ is 0.6 μW, and its peak efficiency is 67.7% at 4.2 μW input power.

2.5.2 Photovoltaic Cell

A light harvester using a photovoltaic cell can provide a much lower $P_{in,min}$, down to sub-nW levels [100]. As shown in Figure 2.20 (a), a conventional light harvester utilizes a photovoltaic cell and a DC-DC converter to charge a battery. The voltage on the diode is determined using a maximum-power-point-tracking circuit.

A direct energy transfer method with a PV cell switching matrix is proposed in [100]. Instead of level converting the voltage from a PV cell to the battery, the PV cells are configured in series so that its output voltage is directly used to charge a battery as described in Figure 2.20 (b). A PV cell network configures the number of series diodes depending on the input light intensity and provides 78-95% efficiency in both dim indoor (100 lux) and direct sunlight (100 klux) conditions.

2.5.3 Battery Management

Battery reliability is one of the key challenges; thus, it is important to design the charging scenario well. As the system size decreases, the battery size should also decrease. The decreased battery voltage increases the internal resistance (R_{BAT}) and therefore the effect of the IR drop. Moreover, R_{BAT} increases as a battery ages over charge/discharge cycles [14], [101]–[103]. The change in R_{BAT} is problematic for sensor systems. To prevent permanent damage to the battery and the sensor system, a low-power battery voltage supervisor (BVS) is implemented [104], [105].

The battery voltage is monitored by a conventional BVS, which includes a battery voltage divider, a comparator and a delay generator, as described in Figure 2.21. There are three important

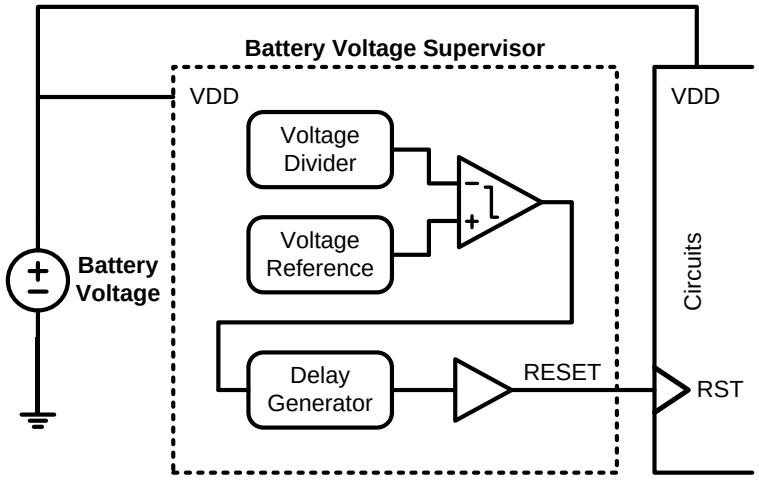


Figure 2.21 Conventional battery voltage supervisor circuit structure

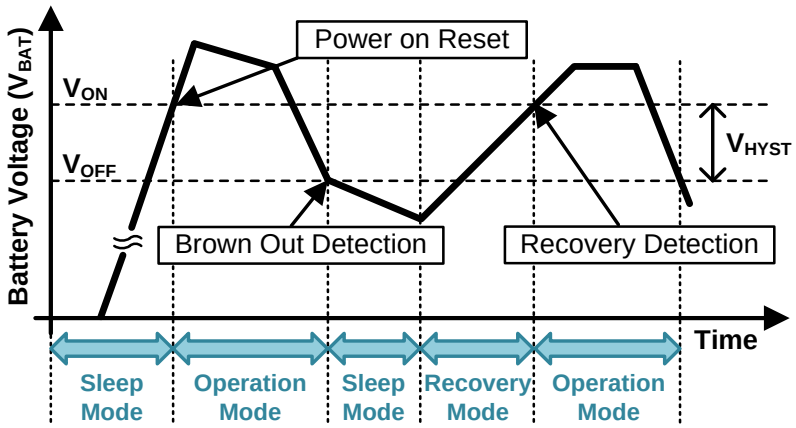


Figure 2.22 Operation of a battery voltage supervisor according to the battery voltage

functions of the BVS, as shown in Figure 2.22. First, Power-on Reset (PoR) generates a reset signal when the battery is initially connected. The system is enabled when the battery voltage exceeds the higher threshold voltage (V_{ON}). Second, Brown-Out Detection (BOD) detects low battery voltages that can damage the battery and the sensor system. When the battery voltage falls below the lower threshold voltage (V_{OFF}), the BVS disconnects the battery from the system. Finally, Recovery Detection reactivates the system when sufficient voltage is sensed. The difference between the threshold voltages provides hysteresis ($V_{HYST} = V_{ON} - V_{OFF}$) to avoid the system oscillating between the operation and sleep modes.

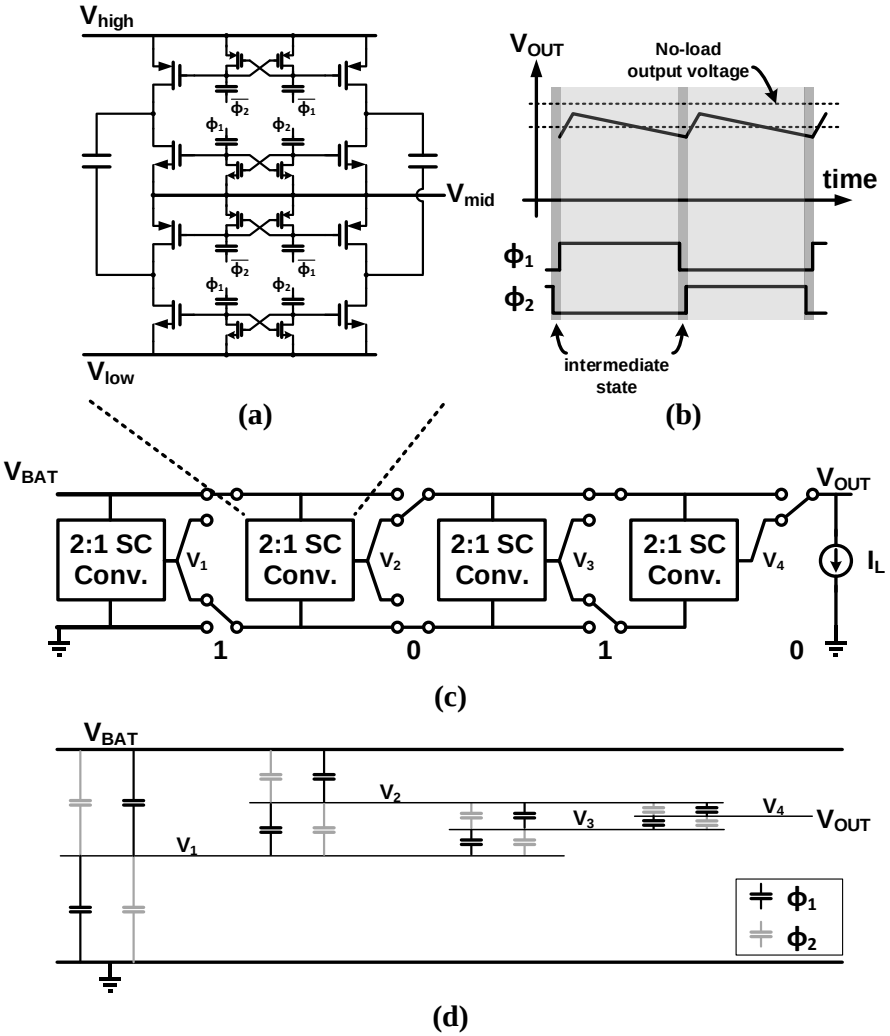


Figure 2.23 A power management unit proposed in [43]. (a) 2:1 switched capacitor unit (b) time domain output voltage (c) a series structure to generate 2^N output votlage levels and (d) output votlages of the 2:1 switched capacitor cells.

However, the constant small V_{HYST} of the BVS is not ideal for advanced miniature sensor systems. The increased IR drop in the minimized systems makes the systems unstable, oscillating between on and off. In [106], a large- constant-hysteresis BVS is proposed to handle the large and constant R_{BAT}, and the large V_{HYST} solves the oscillation problem. The proposed design can handle an R_{BAT} of up to 17 kΩ with 635 pW power consumption at 3.6 V power supply voltage. In addition,

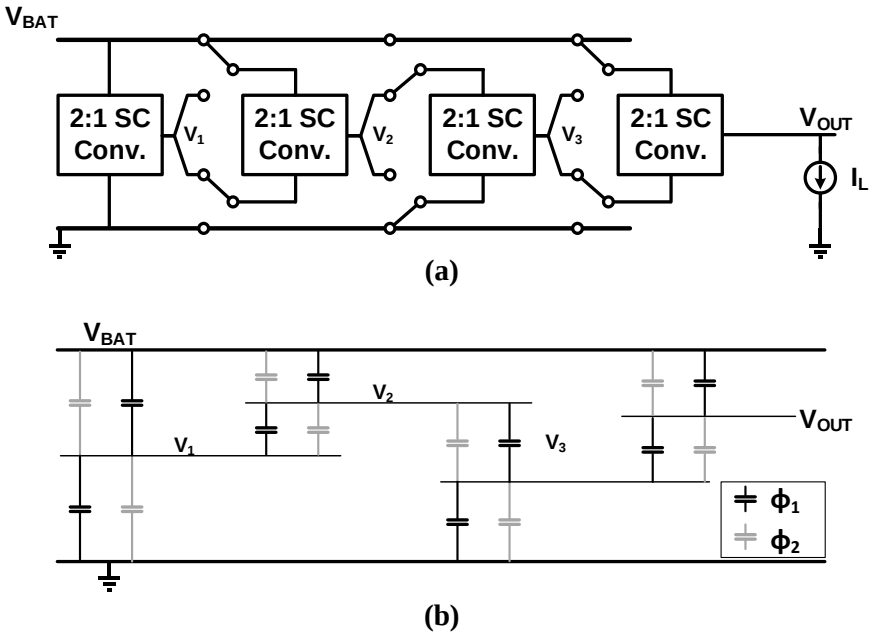


Figure 2.24 (a) A reconfigurable structure proposed in [44] and (b) output votlages of the 2:1 switched capacitor cells.

an adaptive-hysteresis BVS is described that updates V_{HYST} depending on the R_{BAT} measurement results [107]. It can endure a varying R_{BAT} up to 63 kΩ with 3.6 nW power consumption.

2.5.4 Power Management

Monolithic implementation and good efficiency are fundamental requirements for a power management unit (PMU) for miniaturized sensor nodes. In addition, there are several other factors that need to be considered.

Each building block of a wireless sensor node requires different supply voltage levels, which can minimize its energy consumption. For instance, digital logic gates best operate near the threshold voltage to minimize the dynamic power consumption, whereas static random access memory (SRAM) requires more than twice the threshold voltage to maintain a proper noise margin. Also, analog front-end circuitries such as amplifiers, ADCs and filters require various supply

voltages depending on their noise specifications and signal dynamic ranges. Thus, a PMU that generates multiple output voltages is an essential element in a wireless sensor node.

The output voltage resolution of a PMU is also an important factor. A millimeter scale battery typically exhibits a very high output resistance of up to tens of kilo-ohms. Therefore, the IR drop of the battery varies widely according to the static current of the system. In addition, the battery open-circuit-voltage itself varies widely depending on the remaining energy [102]. Therefore, DC-DC converters in the PMU need to provide output voltages with accurate resolution so that the each building block of the system may receive its optimum supply voltage regardless of the battery voltage changes.

Scalability of load power is important to maintain good efficiency depending on the mode of operation. For instance a wireless sensor node consumes nano-watts in sleep mode, micro-watts in active mode and milli-watts in radio communication mode [69], [70]. Quiescent power consumption of the DC-DC converter should adjust to the output power level, making a switched-capacitor based DC-DC converter suitable to the application since its switching loss can be easily scaled by configuring the switching frequency.

The successive-approximation (SAR) switched-capacitor DC-DC converter proposed in [108] utilizes a series of 2:1 converters to realize 2^N output levels. The charge sharing loss is reduced by offering a large number of conversion ratios. The detailed implementation of the SAR operation is explained in Figure 2.23 when the configuration code is 1010_2. Each 2:1 switched converter produces its output, V_{mid}, which is defined as $(V_{high}+V_{low})/2$. When the configuration code of the n^{th} stage is 1, $V_{high,n}$ and $V_{low,n}$ are connected to $V_{high,n-1}$ and $V_{mid,n-1}$, respectively. When the configuration code of the n^{th} stage is 0, $V_{high,n}$ and $V_{low,n}$ are connected to $V_{mid,n-1}$ and $V_{low,n-1}$, respectively. As an example, the switch configurations for a 4-stage DC-DC converter

with the configuration code are shown in Figure 2.23 (c), and the output voltage of each 2:1 switched capacitor is plotted in Figure 2.23 (d). The output voltage, V_{OUT}, is defined as $V_{BAT} \times (Code+1)/2^N$.

A schematic of the 2:1 switched capacitor is depicted in Figure 2.23 (a). This work AC couples the clock to each transistor using capacitors and cross-coupled pairs to make V_{gs} of the switches identical regardless of input and output DC voltages.

[109] proposes a SAR switched-capacitor DC-DC converter that improves the conduction efficiency compared with [108]. In [109], either V_{high} or V_{low} of each 2:1 switched capacitor is directly connected to the supply rails, V_{BAT} or GND, as shown in Figure 2.24. By maximizing the number of connections to the supply rails, the effective output resistance of the DC-DC converter is decreased, and the conduction loss is improved. This approach has been further improved by increasing the number of conversion ratios in [110], providing more fine grained voltage control.

The output voltages of a PMU can be regulated by monitoring them and modulating the switching frequency in order to set them close to the target references [111]–[115]. The switching loss of the DC-DC converter is dynamically adjusted according to the load current in such schemes. The conduction loss is also kept constant as the ratio of $(V_{OUT,NL}-V_{OUT})/V_{OUT,NL}$ where $V_{OUT,NL}$ is the no-load output voltage. Therefore, output voltage regulation using the switching frequency can make the DC-DC converter operate near its maximum efficiency point across wide variation of load current. A feedforward control using the conversion ratio can further improve the regulation, thereby increasing the system reliability [116]. The switching frequency is usually controlled using a voltage-controlled oscillator (VCO) with a feedback loop. Due to the limited response time of such an implementation, a sudden increase of the load current can cause significant voltage droop. This is more critical for a miniaturized system since the high battery resistance further reduces the

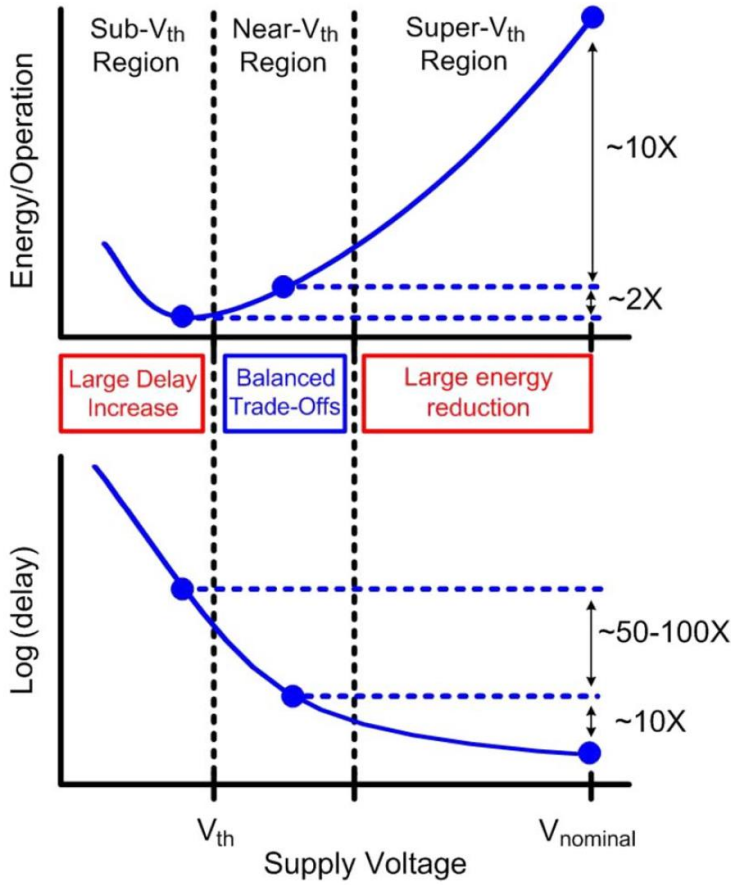


Figure 2.25 Energy-per-operation and delay of logic gates depending on the supply voltage [56].

output voltage by lowering V_{BAT}. [116] proposes a feedforward control of the conversion ratio so that the output voltage can be instantly increased when a sudden voltage droop is detected. A system level design of a PMU for IoT sensor nodes is proposed in [110]. This work generates 0.6V, 1.2V and 3.3V with an output load current range from 20 nW to 500 µW.

2.5.5 Digital Circuits

Process scaling following Moore's law has driven improvements in performance, power reduction and larger scale integration, especially targeting high-performance and strong inversion operation. Although scaling with deep submicron technologies has achieved tremendous gain for high-performance systems, it is also associated with larger leakage, larger interconnect capacitance

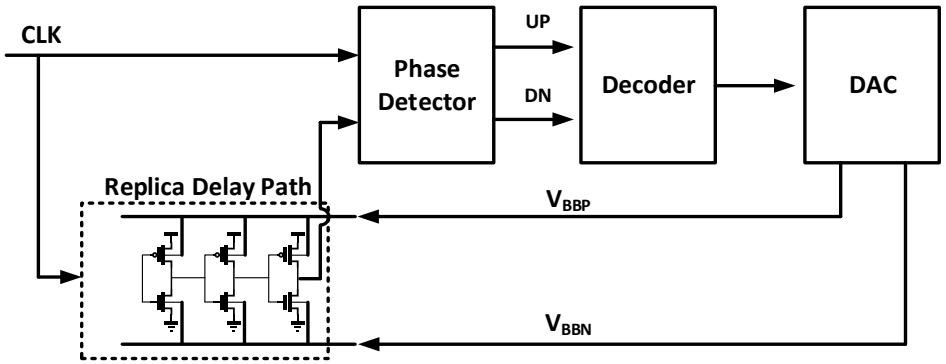


Figure 2.26 Schematic of a delay-locked loop for adaptive body-biasing of logic circuits [62]

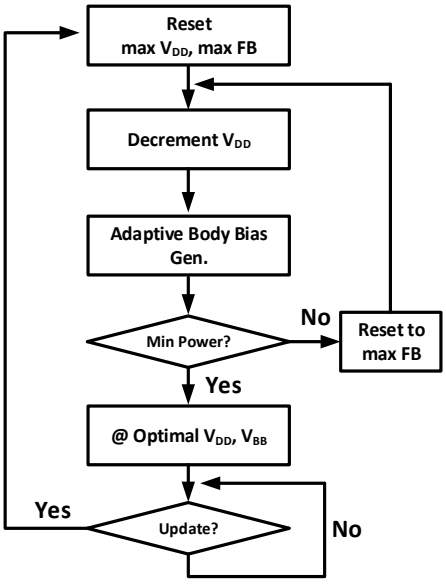


Figure 2.27 A flow chart of the optimization procedure of V_{DD} and body-biasing voltage (V_{BB}) [62]

and lagging supply scaling, which prohibits its use in miniaturized sensor nodes. Instead, for miniaturized sensor nodes, the primary concern is low energy consumption because of the small battery capacity and limited harvestable energy. Digital circuits operating in a near- or sub-threshold region have gained great attention as a way to reduce either the power consumption or energy per operation [76], [117]–[124]. Digital circuits operating under such low supply voltages can exhibit lower energy per operation, primarily benefited by the reduced dynamic power consumption, which is quadratically proportional to the supply voltage. At the same time, the

interval of an operation during which the circuits consume their leakage current increases as a consequence of the slow evaluation time. Hence, the energy overhead from the leakage current is especially pronounced when the supply voltage is reduced below the threshold voltage of the devices due to the exponential relationship between the delay and the supply voltage. Therefore, the energy per operation is optimized when a balance is achieved between the reduction of the dynamic energy and the increase of the leakage energy, as shown in Figure 2.25 [120]–[122], [125]. In addition, the optimal V_{DD} is affected by the idle period [123], process variation [118], body biasing [126], mismatch and activity factor [117]. In this section, recent circuit level techniques for digital circuits are discussed.

A circuit technique for the optimization of the supply and threshold voltages is proposed in [126]. In this approach, the replica path delay of multiply-accumulate (MAC) units are monitored to optimize the threshold voltage of the devices so that the leakage current is minimized given the supply voltage and the operating frequency, as shown in Figure 2.26. The body voltages of PMOS (V_{BBP}) and NMOS (V_{BBN}) are stabilized using a delay-locked loop composed of a phase detector, a decoder, a digital-to-analog converter (DAC) and body-tuned replica delay cells. The replica path delay is equal to the reference period in the steady state. The combination of V_{DD} and body-biasing voltages are further optimized by sweeping the supply voltage to find the optimal combination for minimum power, as shown in the flow chart in Figure 2.27. Initially, V_{DD} is set to maximum, and the body voltages are set to a maximum forward biasing condition. Then, V_{DD} is decreased by one step using a DC-DC converter, and the body voltages are adjusted using the delay locked loop. This procedure is repeated until a minimum power state is achieved.

In addition to minimizing the energy-per-operation, there is also a need to minimize power consumption, sacrificing energy efficiency. Most of the miniaturized sensor nodes adopt duty-

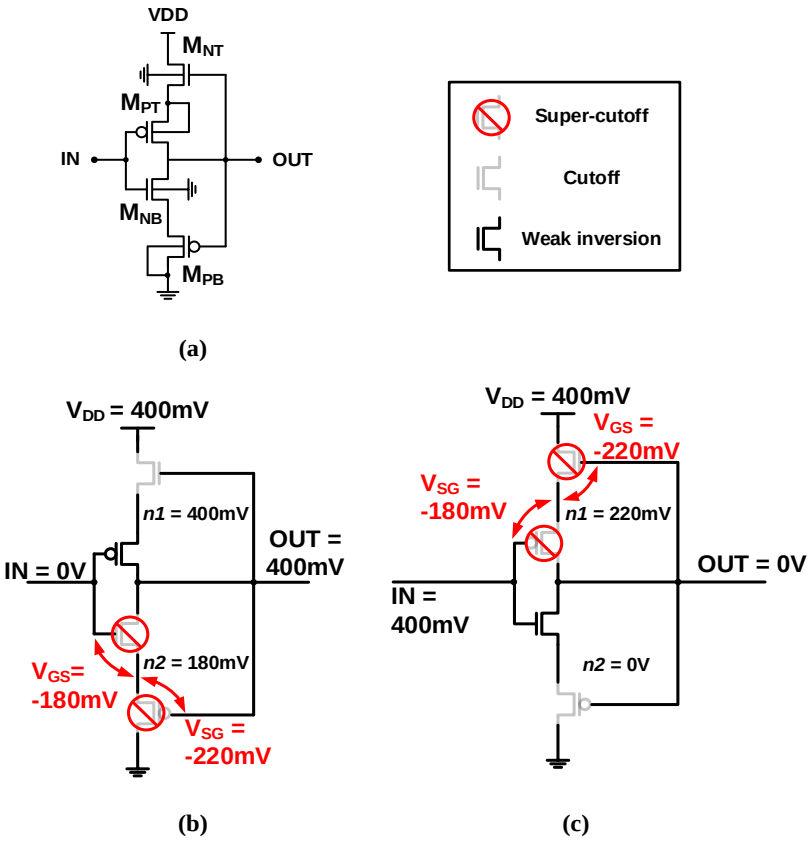


Figure 2.28 (a) Schematic of a dynamic leakage-suppression logic inverter proposed in [63]. Tranasistor states (b) when input is equal to 0 and (c) when input is V_{DD}.

cycling of the active mode in order to reduce the average power consumption to a level of harvestable power, as explained in section VI. However, this scenario is based on the assumption that the system has a reliable battery that serves as an energy buffer during sleep mode. However, such recursive charge and discharge actions degrade the battery reliability and shorten the system life time. For instance the 5,000 discharge cycles reported in [102] with a 30 min wakeup period limit the system life time to 3.5 months [15]. Therefore, a design methodology that lowers the active power consumption to a level of harvestable energy is required.

Power consumption can be decreased by lowering V_{DD}. However, a reduced on/off ratio limits the minimum supply voltage to 200-300 mV for reliable logic operation under PVT

variations. A Schmitt-trigger logic that can operate with 62 mV supply voltage is proposed in [127]. This approach could reduce the power consumption with an extremely low V_{DD}, but the leakage current level is similar to the conventional logic gates, limiting the power reduction level to a linear relationship with V_{DD}.

A dynamic leakage-suppression logic (DLS) that drastically reduces the leakage current is proposed in [15]. The operation principle is explained in Figure 2.28. The bottom PMOS, M_{PB} and top NMOS, M_{NT} are attached as power-gating transistors to an inverter composed of M_{PT} and M_{NB} to guarantee that all of the transistors on the leakage paths are in a super-cutoff state after stabilization. As an example, Figure 2.28 (b) shows the case when 0 V is applied to the input. The intermediate node, n1, is connected to V_{DD} through M_{NT}, and n2 is set to approximately half of V_{DD}. It can be seen that V_{sg} of M_{PB} and V_{gs} of M_{NB} become negative, creating a super-cutoff state. Similarly, both M_{NT} and M_{PT} are in a super-cutoff state when the input is high. As a result, the leakage current of the proposed logic gate is approximately 320 times smaller than that of a standard low-leakage stacked inverter. [15] proposes a prototype design of Cortex-M0+ processor in 180-nm CMOS technology, which consumes 0.295 pW under 550 mV supply.

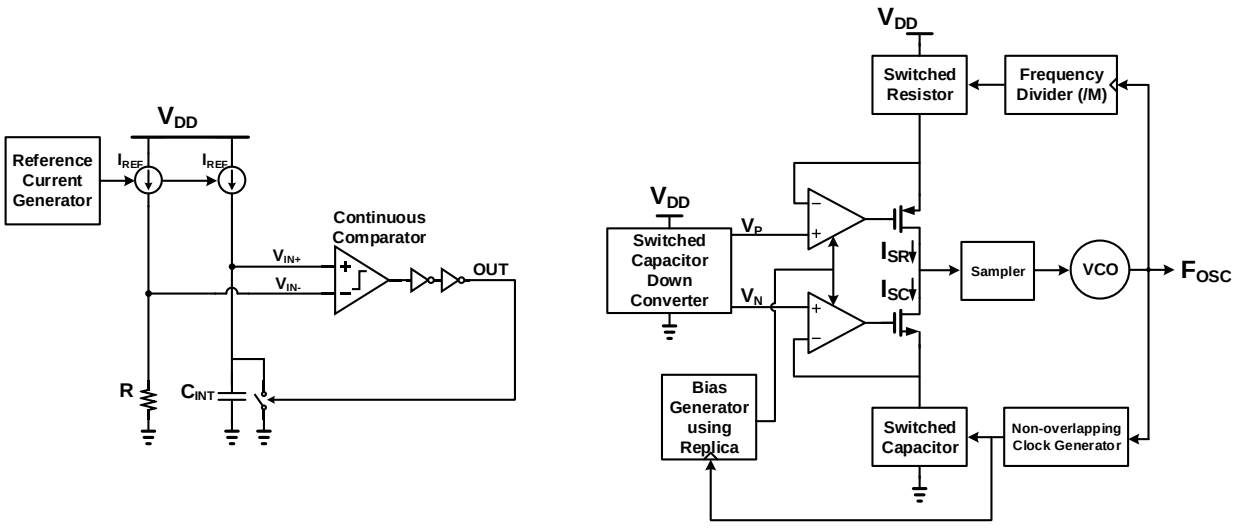
CHAPTER 3

Ultra-low Power Wake-up Timer

3.1 Introduction

Miniaturized computing platforms typically operate under restricted battery capacity due to their size [1]. Due to low duty cycles in many sensing applications, sleep mode power can dominate the total energy budget. Wakeup timers are a key always-on component in such sleep modes and must therefore be designed with aggressive power consumption targets (e.g., <10nW). Also, accurate timing generation is critical for peer-to-peer communication between sensor platforms [1]. Although a 32 kHz crystal oscillator can provide low power [2] and accurate long-term stability, the requirement of an off-chip component complicates system integration for small wireless sensor nodes (WSNs).

As a result, conventional on-chip oscillators for WSN applications utilize RC time constants, which show relatively accurate frequency stability compared to transistor delay dominated ring oscillators. Conventional RC oscillators periodically reset a capacitor using an RC time constant and comparator [3-4]. However, a power-hungry fast continuous comparator is needed to render its own delay negligible compared to the RC time constant and ensure good frequency stability. A timer using a frequency locking technique to allow an ultra-low power amplifier to replace the comparator is proposed in [5]. However, oscillation frequency cannot be



< Comparator based relaxation oscillator >

< Proposed self-biased current reusing frequency locking >

Figure 3.1 Block diagram of the conventional relaxation oscillator using comparator and the ring oscillator using frequency locking scheme and the proposed self-biased current reusing frequency locking scheme without using current reference.

scaled down due to the resistor size, which limits the minimum power consumption. For example, even with a relatively large 55MΩ resistor occupying 0.2mm^2 in 180nm CMOS, the topology consumes 18.2nW at 1V switching amplitude.

To address this challenge and achieve a WSN timer with single-digit nW power consumption, we propose a new timer using a duty-cycled resistor scheme to increase resistance without impacting area. By generating the duty cycle using the frequency from the timer itself, an accurate on/off ratio is ensured. In addition, a current-reuse scheme is proposed to save power and also eliminates the need for chopping the bias current. Finally, a self-biasing technique is proposed to ensure stable operation and low power consumption across process-voltage-temperature (PVT)

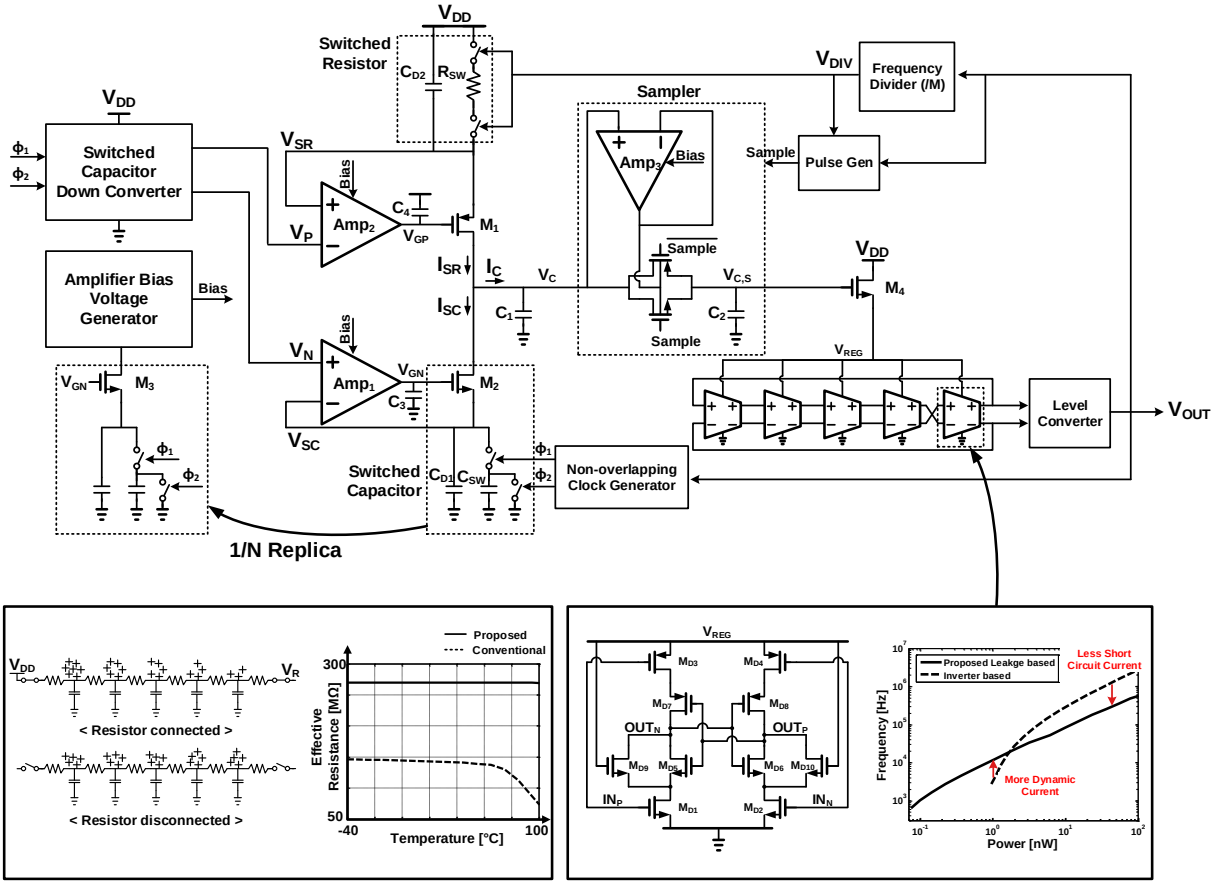


Figure 3.2 Circuit diagram of the proposed oscillator (top). At bottom left, the proposed approach of disconnecting both terminals of the resistor during off events enables wider temperature range operation (simulation results). At bottom right, the leakage-based delay cell used in the VCO shows better scalability to low oscillation frequencies than an inverter-based ring oscillator.

variations. Using these techniques, the timer achieves 13.8ppm/°C (−25 to 85°C) at 3kHz and consumes 4.7nW while showing less than 1.5× power variation across temperature.

3.2 Frequency locked loop using switched-capacitor frequency feedback

Figure 3.1 explains the concept of the proposed timer. A voltage controlled oscillator's (VCO) frequency is sensed using the effective resistance of a switched capacitor. This effective resistance is transformed to current (I_{SC}) by regulating it to a voltage generated by a series of 2-to-

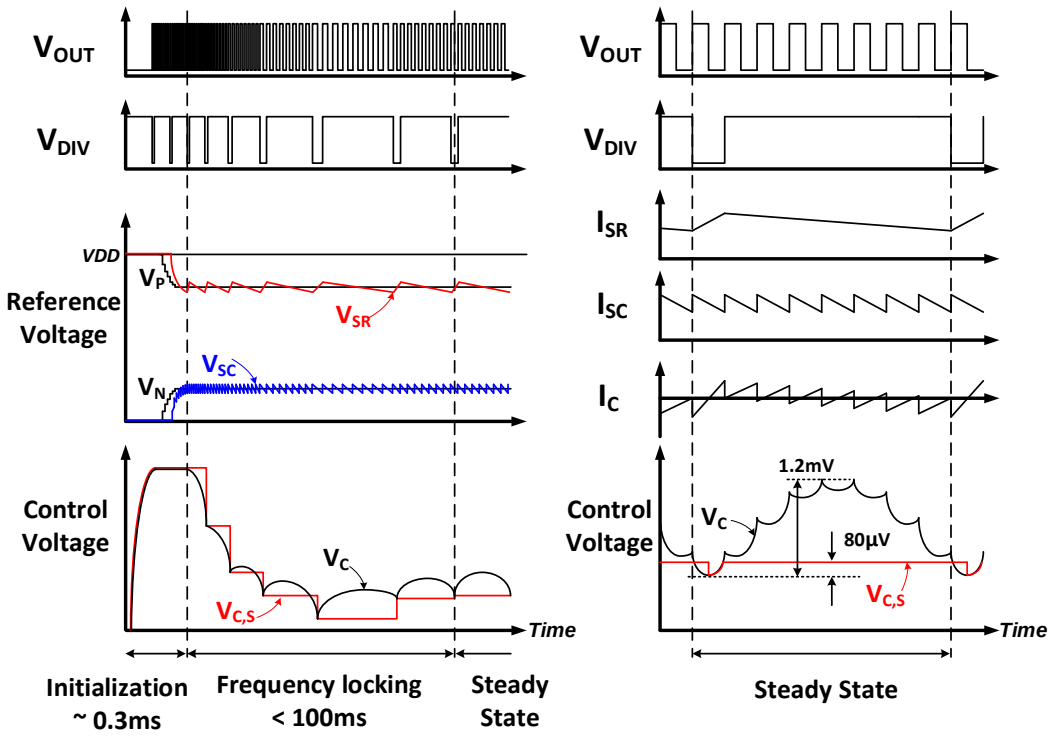


Figure 3.3 Transient locking behavior of the output frequency, reference voltages and control voltages of the proposed oscillator (left) and their steady-state behavior (right)

1 voltage down converters (V_N). I_{SC} is then compared to a current generated by a temperature-compensated switched resistor (I_{SR}) referenced to V_P. The frequency locked loop is stabilized when I_{SC} is equal to I_R, thereby defining the oscillation frequency (F_{OSC}) as $1/(M \times R_{SW} \times C_{SW})$ where M is the duty cycle of R_{SW} switching operation. Placing the switched resistor and switched capacitor in series effectively "reuses" current, reducing power consumption of this component by 2× compared to a conventional topology where they are placed in parallel.

Figure 3.2 shows the detailed circuit implementation. Amp1 and Amp2 regulate voltages on R_{SW} and C_{SW} through M_1 and M_2, respectively. C_{D1} and C_{D2} are connected in parallel with R_{SW} and C_{SW} to reduce the ripple arising from switching events. However, those capacitors can reduce the frequency of the second pole and make the regulation loops unstable. Furthermore, ultra-low power design using subthreshold-biased devices exacerbates sensitivity to PVT variations,

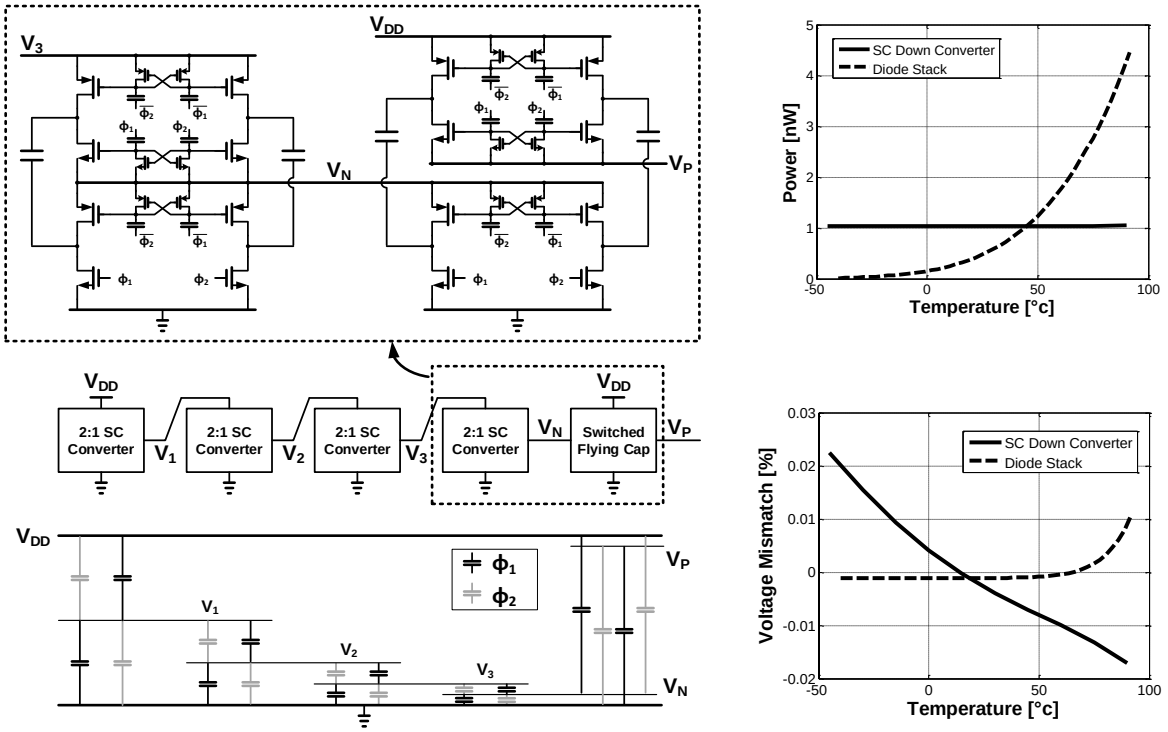


Figure 3.4 Reference voltage generation using switched capacitor based DC-DC (converter) (left) and simulation results of power and accuracy compared to a diode stack (right).

complicating the design. This work proposes a self-biasing scheme that uses a replica of I_{SC} to generate amplifier biasing currents. Assuming near 0dB gain of source follower M_2, the regulation loop phase margin is defined by $\tan^{-1}(gm_1C_3/gm_{amp1}C_{D1})$ where gm_1, and gm_{amp1} are transconductances of M_1 and Amp1's differential pair, respectively. As the phase margin is determined only by the ratio of transconductance and capacitance, stability can be ensured across a wide range of PVT variation. Furthermore, self-biasing acts to maintain relatively constant power consumption of analog building blocks across temperature and removes the need to include an accurate current reference generator, thereby saving power and area.

Figure 3.3 shows the transient signal behavior of the reference and control voltages. V_{DIV} is frequency divided from V_{OUT} and provides an accurate on/off ratio for the switched resistor. V_{SR} and V_{SC} are the voltages on R_{SW} and C_{SW} and are regulated by V_N and V_P, respectively, taken from

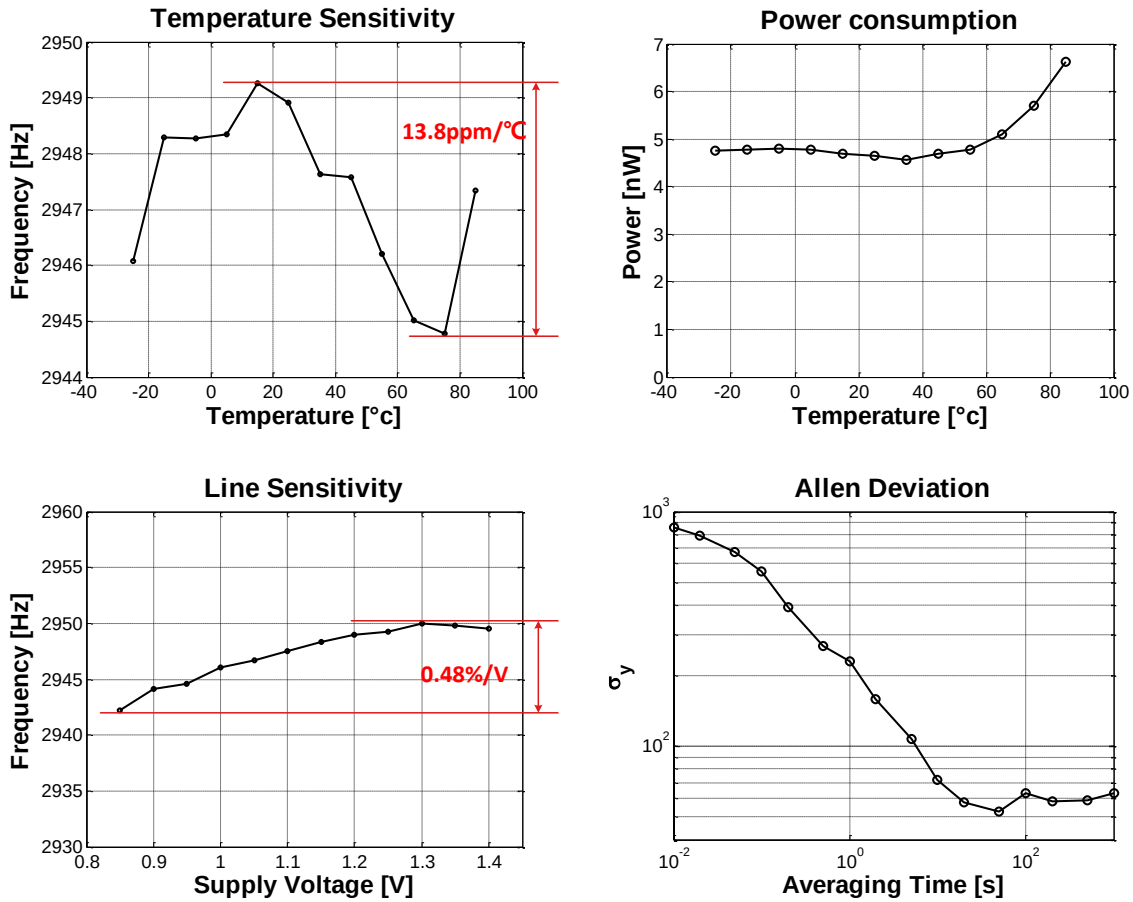


Figure 3.5 Measurement results of wakeup timer temperature coefficient (top left), power consumption (top right), line sensitivity (bottom left), and Allan deviation (bottom right).

the down converter. Voltage ripple on V_{SR} and V_{SC} due to switching operation causes a current ripple on I_{SR} and I_{SC} (Figure 3.3, right). The difference between I_{SR} and I_{SC} is integrated by C_1 and creates a quadratic ripple on V_C. This ripple can perturb the duty cycle of V_{DIV}, creating temperature and supply voltage sensitivity. To mitigate these non-ideal effects, a sampler is placed in front of the VCO so that the control voltage is constant within a divider cycle. Amp3 drives sampling transistor body voltages to remove the drain junction leakage from the sampled voltage, $V_{C,S}$.

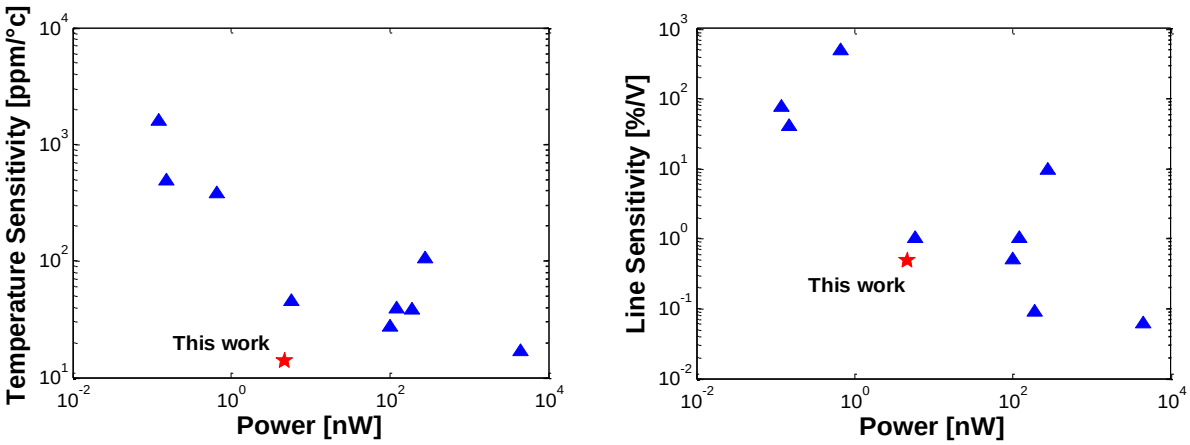


Figure 3.6 Performance summary and comparison to prior work in low-power wakeup timers.

A key part of the proposed low-power scheme is the switched resistor. Resistor current ($I_{SR} = (V_{DD}-V_P)/(M\times R_{SW})$) can be reduced by either lowering the voltage across the resistor or increasing R_{SW}. The lower bound on voltage swing is determined by amplifier input offset. V_N is therefore selected to be $1/16^{th}$ of the supply voltage in order to allow center frequency adjustment after trimming R_{SW} and C_{SW} under wide variation of amplifier offset and process. The practical upper bound of R_{SW} is dictated by area requirements and set to 17M□, with resulting area of $0.065mm^2$. The proposed resistor switching scheme increases the resistor size without increasing area. A switched resistor is usually implemented by placing a switch in series with a resistor [6]. However, current can still flow from the non-disconnected port to parasitic capacitance in the resistor even when the switch is off. This reduces the equivalent resistance and makes it temperature dependent. This effect worsens quadratically with resistor size as the current injected into its parasitic capacitance grows linearly while the current flowing through the resistor reduces inversely with resistance. Instead, we disconnect both resistor terminals so that charges on the parasitic capacitors is only shared while the switch is off. This eliminates injection of additional current from the parasitic capacitor (Figure 3.2, left).

Table 3.1 Performance summary and comparison to prior work in low-power wakeup timers.

	This work	JSSC 2015 [3]	ISSCC 2013 [4]	ISSCC 2014	VLSI 2015 [5]	VLSI 2012	VLSI 2012	ISSCC 2011
Process (nm)	**180**	180	65	65	180	60	90	130
Frequency (Hz)	**3000**	11	18,500	33,000	70,400	32,768	100,000	0.37
TC (ppm/°C)[1]	**13.8**	45	38.5	38.2	27.4	16.7	104.6	375(31[2])
Temp. Range (°C)	**-25 to 85**	-10 to 90	-40 to 90	-20 to 90	-40 to 80	-20 to 100	-40 to 90	-20 to 60
Line sensitivity (%/V)	**0.48**	1	1	0.09	0.5	0.006	9.4	490
Power (nW)	**4.7**	5.8	120	190	99.4	4,480	280	0.66[3]
Energy/Cycle (pJ/Cycle)	**1.6**	527.27	6.49	5.76	1.41	136.72	2.80	1,738.8
Area (mm^2)	**0.5**	0.24	0.032	0.015	0.26	0.048	0.12	0.015

[1] Calculated by $(f_{max} - f_{min})/f_{avg} \times 10^6$.
[2] With 10 point calibration using temperature sensor.
[3] Power consumption of temperature sensor is not included.

Reference voltages V_N and V_P are generated using a series of switched capacitor 2-to-1 downconverter clocked by the oscillator output. The stable oscillator frequency results in a constant current consumption across temperature (Figure 3.4), especially compared to conventional diode stack based voltage dividers as shown in Figure 3.4, right. Even though the voltage mismatch between V_N and V_{DD}-V_P is larger, it is negligible compared to the overall TC of the proposed timer. Furthermore, the mismatch is more linear than that of the diode stack, thus it can be more easily tuned out by trimming TC of R_{SW}. The switching voltages are level converted though coupling capacitors and a pair of cross-coupled transistors so that the clock feedthrough of each switching transistor is balanced and driving capability is constant regardless of the output voltage [7].

Figure 3.2 (bottom right) shows the schematic of the proposed VCO. The delay cell is composed of 1) low leakage transistors (M_{D1}-M_{D4}) that toggle the output polarity, 2) high leakage transistors (M_{D5}-M_{D8}) that provide leakage current to slowly charge/discharge the output, and 3) low leakage tuning transistors (M_{D9}, M_{D10}) that provide delay tunability via the supply voltage.

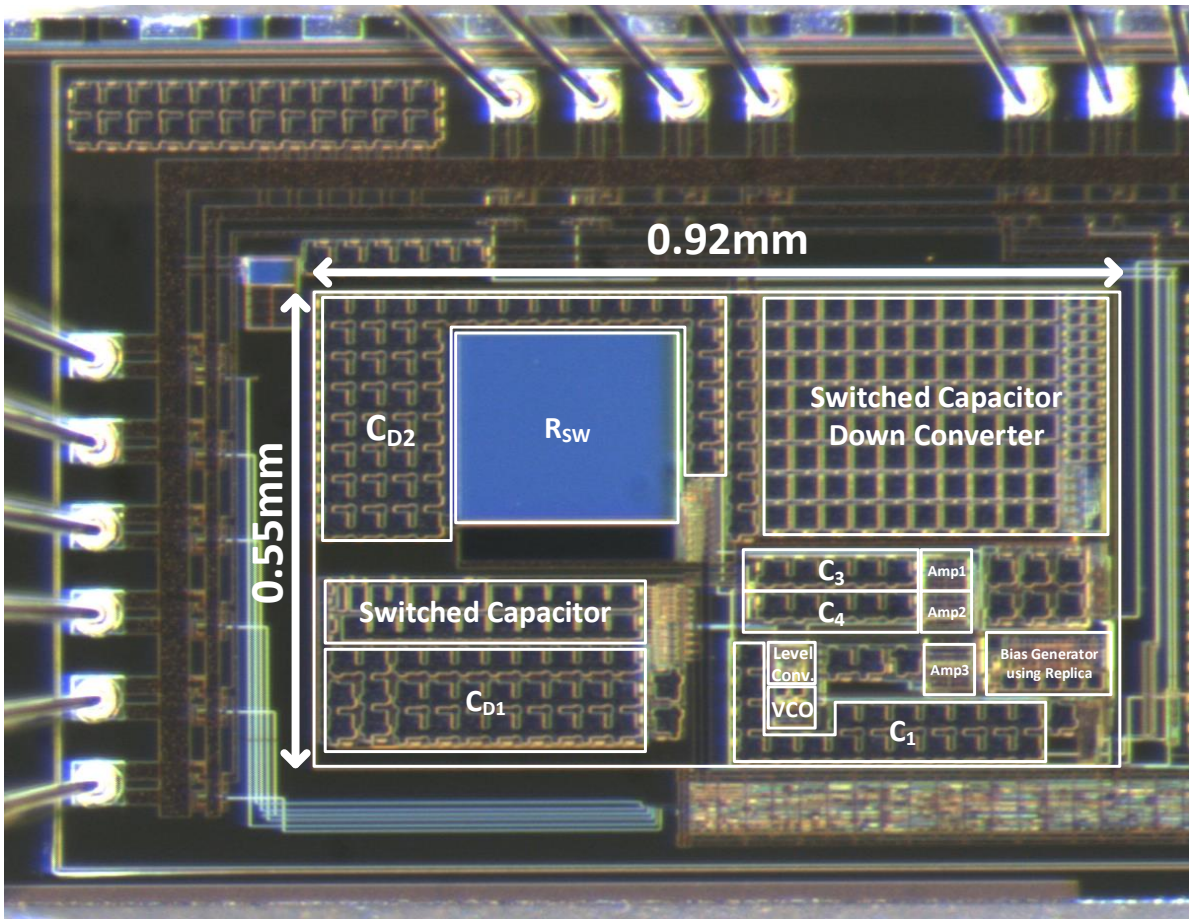


Figure 3.7 Die photo of the proposed wake-up timer.

Simulation results show that the proposed oscillator operates stably down to 630Hz, providing 4.3× lower frequency floor compared to an inverter-based VCO, which is limited in this respect by its small on/off ratio at low V_{DD}.

3.3 Measurement Results

The proposed design is fabricated in 180nm CMOS with an area of 0.5mm^2. It uses only a single supply voltage and does not require additional voltage or current references. Measured results in Figure 3.5 show that the design generates 3 kHz while consuming 4.7nW with a temperature coefficient of 13.8ppm/°C measured from −25 to 85°C. Power consumption varies by <50% across this wide temperature range due to the self-biasing technique. Measured line

sensitivity is 0.48%/V from 0.8V to 1.4V and Allan deviation is less than 63ppm. Figure 3.6 provides a comparison table with other wakeup timers and Figure 3.7 shows a die photo.

CHAPTER 4

Frequency Synthesizer

4.1 Introduction

Recently all-digital phase-locked loops (ADPLLs) have been widely adopted for their small size, configurability and portability [128]–[130]. Although an ADPLL is less susceptible to environmental variation compared with its analog counterparts, it is still affected by process and temperature changes. This leads to overly restrictive design specifications to ensure robust performance over the entire process and temperature range, causing a power penalty. For instance, gain of a digitally controlled oscillator (DCO) and a phase detector are the dominant factors that can cause variation in the loop dynamics. When a time-to-digital converter (TDC) is used as a phase detector, its delay elements are susceptible to environmental variation, so its quantization step represented as unit delay of the TDC is variable [131]–[136]. A 1-bit TDC or bang-bang phase frequency detector (BBPFD) is usually considered to operate independently of environmental changes because it does not have a delay element. However, the output amplitude of a BBPFD is fixed as 1 and 0 regardless of the input amplitude, making the input-to-output ratio dependent solely on the input amplitude [137]–[139]. Thus its gain is dependent on the amplitude of the input signal, which comes from DCO phase noise in a digital PLL. Therefore, the need for a DCO design,

which provides stable gain and noise, is emphasized in a BBPFD based digital PLL in order to ensure robust operation under the environmental changes.

Reusability also contributes to variation in PLL operation. The increased fabrication, design and verification costs in the latest technologies have led to a demand for reusability. Reusability also reduces the development time of a product. However, there is a classic trade-off between productivity and efficiency. A generic PLL should cover a wide range of specifications. Thus, it cannot be optimized for any specific product and will inevitably result in wasted energy.

There are a few requirements for a generic PLL. First, a generic PLL must have a wide frequency range to make it suitable for many products. Noise optimization for both short-term and long-term jitter is required to broaden its application space. Reconfigurability of the PLL mode is beneficial so that it can operate near an energy-optimal point in many applications. A charge-pump PLL is a well-known architecture showing robust operation. However, its analog nature creates problems such as a large loop filter size and limited reconfiguration ability in deep submicron technologies. For instance, digital loop filter reconfiguration is much more flexible with less area overhead compared to a charge-pump PLL using current digital-to-analog converter (DAC) and loop filter switches[135]. In addition, two-point modulation for the spread-spectrum can be done easily without employing addition DAC[140]. DSM noise cancellation in a fractional-N mode is also more straightforward with high accuracy and less overhead, whereas a charge pump PLL requires additional charge pump and pulse width control and suffers from mismatch[133], [141]. A multiplying delay-locked loop (MDLL) offers the advantage of reduced oscillator noise by refreshing the oscillator phase with a reference [142]. Nevertheless, its limited multiplication ratio and large period jitter at edge insertion make the MDLL an undesirable architecture for a generic PLL [143]. On the other hand, a digital PLL can provide robust operation across wide input and

output frequency ranges. In addition, its digital nature helps make it small and reconfigurable in the latest technology. Therefore, a digital PLL offers an attractive architecture to meet the requirements of a generic PLL.

A DCO is considered the most important building block of a generic digital PLL for a couple reasons. First, the output phase noise is mostly governed by DCO noise, especially when a ring oscillator is used. An LC oscillator reduces the noise significantly but is difficult to adopt in a generic PLL due to the frequency range and size requirements. Noise filtering techniques have been proposed to improve the phase noise in a ring oscillator [144], [145]. However, their figure-of-merit (FoM) is still worse than the theoretical limit of a ring oscillator [146] due to the additional power consumption and noise generation of the frequency detection circuit. Therefore a ring oscillator structure that can operate near its theoretical limit [146] is desirable. Second, a DCO's gain and frequency range affect the performance of a PLL significantly. Nevertheless, the gain and frequency range vary significantly because its delay relies on the intrinsic parameters of the transistors. The change in the DCO gain results in variation of the PLL loop bandwidth as it moves away from the optimal point. Therefore, an accurate and linearized frequency tuning curve is required to maintain a constant loop bandwidth.

In this work, we implemented a digital PLL with a nested frequency locked loop (FLL) that linearizes the DCO frequency tuning curve, providing stable gain. Therefore, the loop dynamics are insensitive to environmental variations. We propose a noise reconfiguration scheme using a noise reconfigurable DCO to create a trade-off between power and noise. We furthermore propose a noise detection circuit that uses the statistical behavior of BBPFD to self-adjust the noise depending on the noise specification.

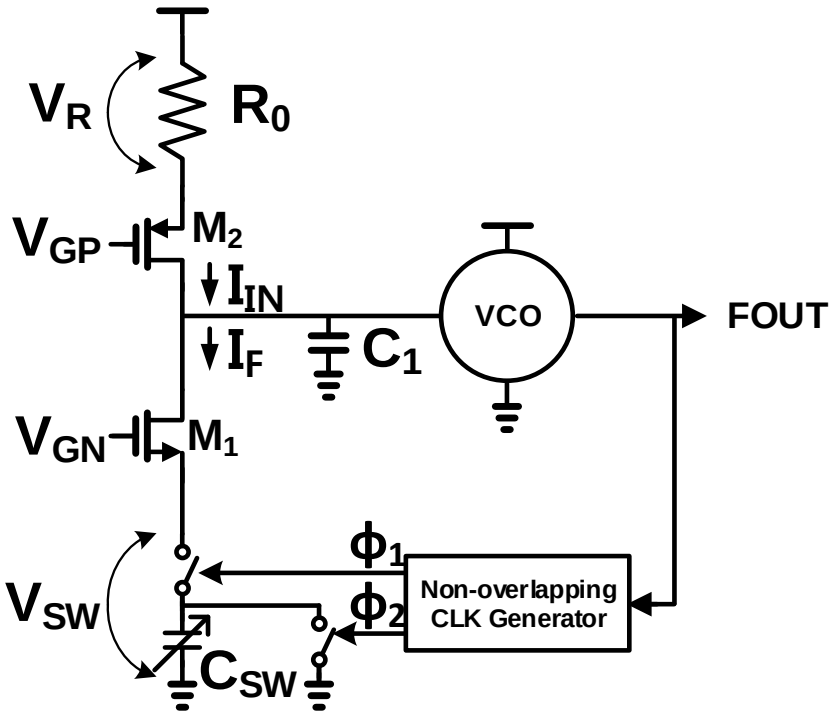


Figure 4.1 A conceptual schematic of a frequency locked loop using a switched capacitor frequency feedback.

4.2 Proposed Approach

4.2.1 Basic Concept

The proposed design adopts an FLL structure using a switched capacitor for the frequency feedback [21], [67], [147]–[151]. Its basic concept is introduced in Figure 4.1. The input current, I_{IN}, is generated by regulating a resistor R_0 with the voltage V_R. The feedback current, I_F, is defined by the following equation.

$$I_F = C_{sw} V_{sw} f_{out} \tag{10}$$

where C_{sw}, V_{sw} and f_{out} are switching capacitance, voltage on C_{sw} and output frequency, respectively. Assuming a large gain from the frequency detection block, I_F should be equal to I_{IN} in the steady state. Therefore the output frequency can be calculated using the following equation.

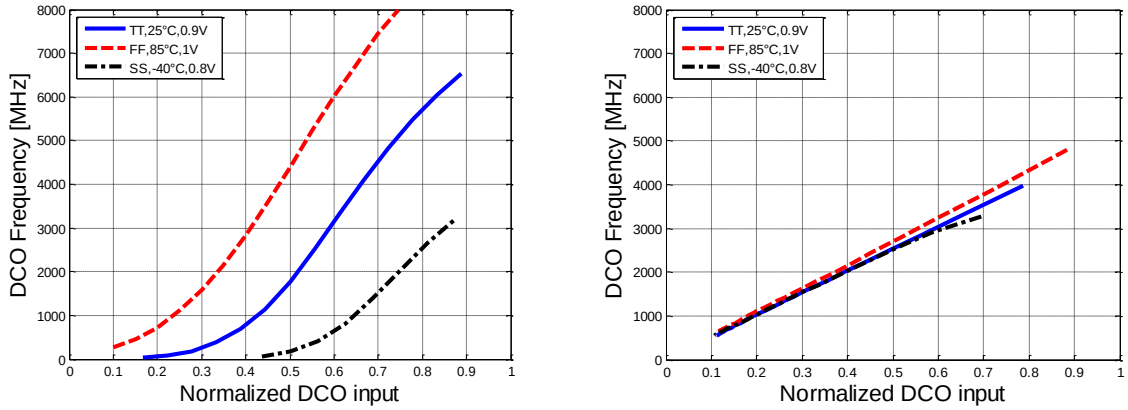


Figure 4.2 Simulated frequency tuning curves (a) with DAC attached to a VCO and (b) proposed FLL using switched capacitor frequency feedback.

$$C_{sw}V_{sw}f_{out} = \frac{V_R}{R_0}$$
$$f_{out} = \frac{V_R}{V_{sw}}\frac{1}{R_0C_{sw}} \tag{11}$$

When the identical voltage is used for V_R and V_{sw}, the oscillation frequency of the FLL is defined in the following equation.

$$f_{out} = \frac{1}{R_0C_{sw}} \tag{12}$$

Conventional methods of DCO implementation includes a gate voltage control of a current starving transistor[152], a series resistance control to load capacitor[153] or to supply voltage[154], a delay cell size control[78] or a digital current control for a current-controlled oscillator[155], all relying on the of physical device characteristics and it is difficult to achieve high linearity or PVT invariance[149]. In contrast, an FLL using switched capacitor can accurately control the output frequency because it is explicitly determined as (12) using a negative feedback loop[21], [67], [147]–[151].

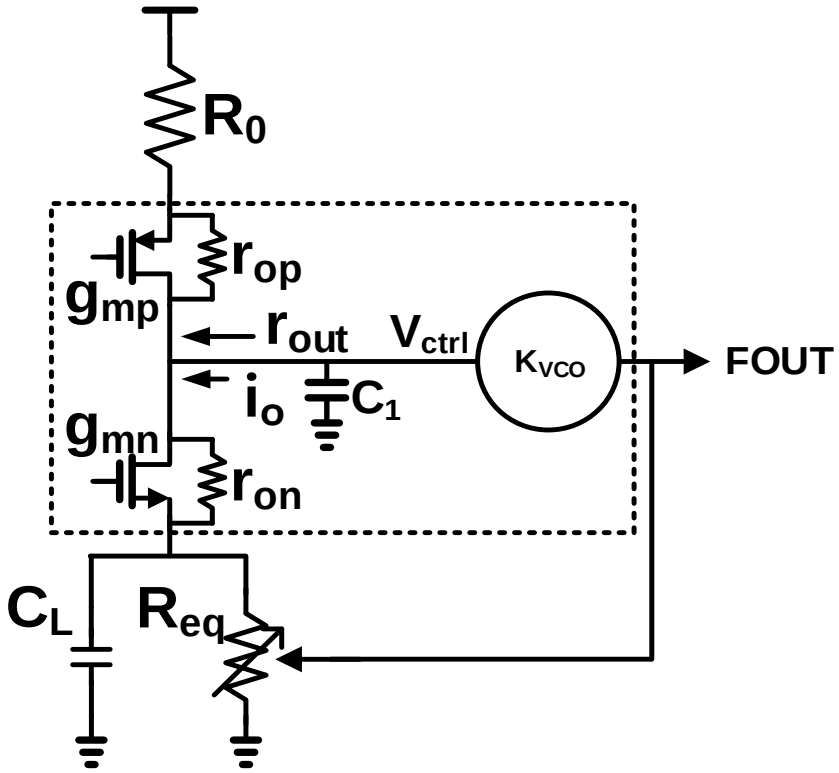


Figure 4.3 A simplified schematic of the proposed FLL for the analysis of the feedforward transfer function.

As an example Figure 4.2 shows simulated frequency tuning curves of conventional and proposed DCOs. Figure 4.2 (a) is a conventional case where a DAC is attached to a current starved voltage-controlled oscillator (VCO) to form a DCO that shows a non-linear and PVT dependent frequency tuning curve. In contrast, a DCO with the proposed scheme demonstrates a highly linear and accurate tuning curve, as shown in Figure 4.2 (b).

4.3 Loop Dynamics of the Proposed FLL

In this section, the loop dynamics of the proposed FLL are analyzed. First, the feedforward path of the FLL is from the output current generated by the frequency detection block to the output frequency of the DCO marked with a dotted line in Figure 4.3. The control voltage, v_{ctrl}, is

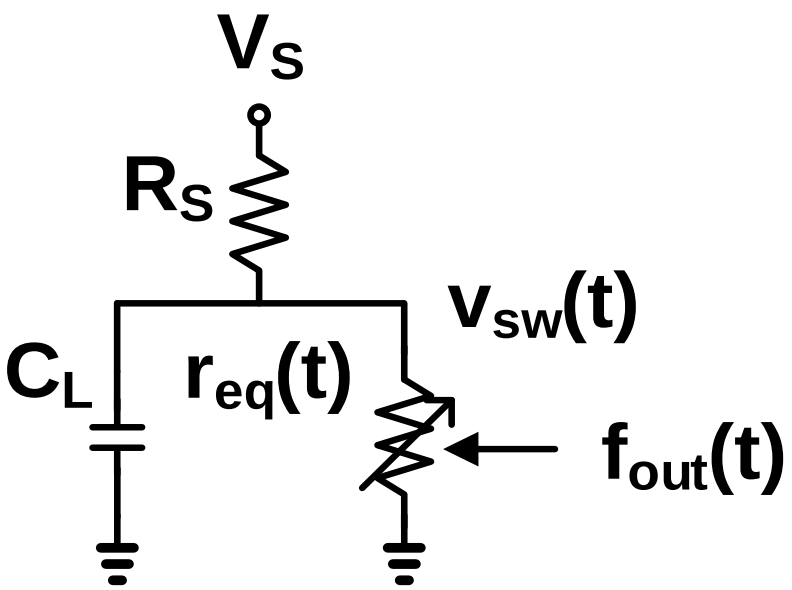


Figure 4.4 A simplified and linearized schematic at the source of the M1 for the analysis of feedback transfer function.

generated by the output current, i_o, multiplied by the output impedance of the detection block as shown in the following equation,

$$r_{out} = \left(R_0 + r_{op}\left(1 + g_{mp}R_0\right)\right) \| \left(R_{eq} + r_{on}\left(1 + g_{mn}R_{eq}\right)\right) \simeq r_{op}R_0 g_{mp} \| r_{on}R_{eq}g_{mn} \qquad (13)$$

where r_{op}, r_{on}, g_{mp} and g_{mn} are PMOS output resistance, NMOS output resistance, PMOS transconductance and NMOS transconductane, respectively. Assuming $r_{op}=r_{on}=r_o$, and M_1 and M_2 are in a subthreshold region so that their transcondutance is maximized to I_{bias}/mv_T, r_{out} can be simplified to $r_o R_0 I_{bias}/2mv_T$ where m is $1+C_d/C_{ox}$ and C_d and C_{ox} are depletion and oxide capacitances respectively.

$$v_{ctrl} = z_{out} i_o = \frac{r_{out}}{1 + s \cdot r_{out} C_1} i_o \qquad (14)$$

The output frequency, f_{out}, can be calculated by multiplying the gain for the VCO, K_{VCO}, to (14).

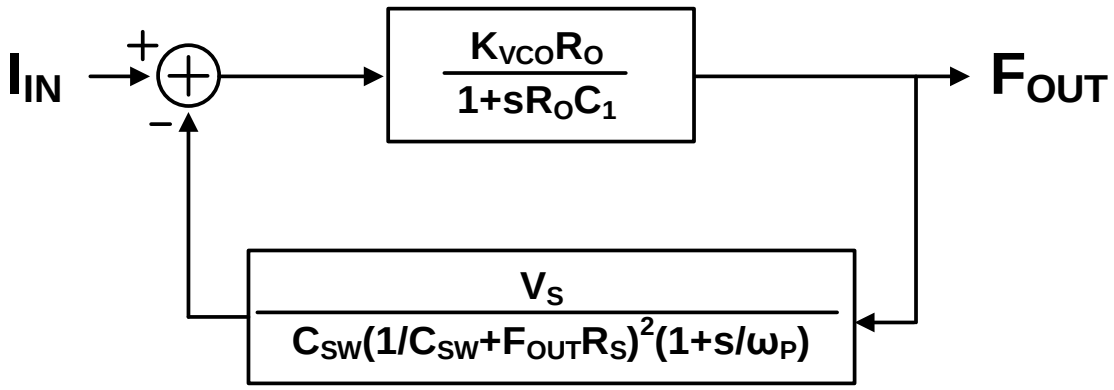


Figure 4.5 Linear model of the proposed FLL.

$$f_{out} = \frac{K_{VCO} r_{out}}{1 + s \cdot r_{out} C_1} i_o \tag{15}$$

Then, the feedforward transfer function from the output current of the frequency detector to the output frequency is

$$H_{ff}(s) = \frac{f_{out}}{i_o} = \frac{K_{VCO} r_{out}}{1 + s \cdot r_{out} C_1} \tag{16}$$

Note that $1/r_{out}C_1$ is the dominant pole of the FLL. To analyze the feedback path of the proposed topology, we first need to analyze the transfer function of the switched capacitor. f_{out} serves as an input to the switched capacitor, and its equivalent resistance, r_{eq}, is the output. Then, the transfer function of the switched capacitor is

$$r_{eq} = \frac{\partial i_f}{\partial f_{out}} = \frac{\partial}{\partial f_{out}} \left(\frac{1}{C_{sw} f_{out}} \right) = -\frac{1}{C_{sw} f_{out}^2} \tag{17}$$

The change in r_{eq} results in a change in the output current of M_1 by modulating its gate-to-source voltage. Figure 4.4 shows the linearized circuit diagram at the source of M_1. R_s is the source resistance of M_1(shown in Figure 4.1), which is expressed as $1/g_{m1}$. C_L is a capacitor connected in parallel to the switched capacitor to lower the ripple magnitude. V_s is a virtual source voltage that provides DC voltage on the switched capacitor. v'_{sw} is the voltage on the switched capacitor, and

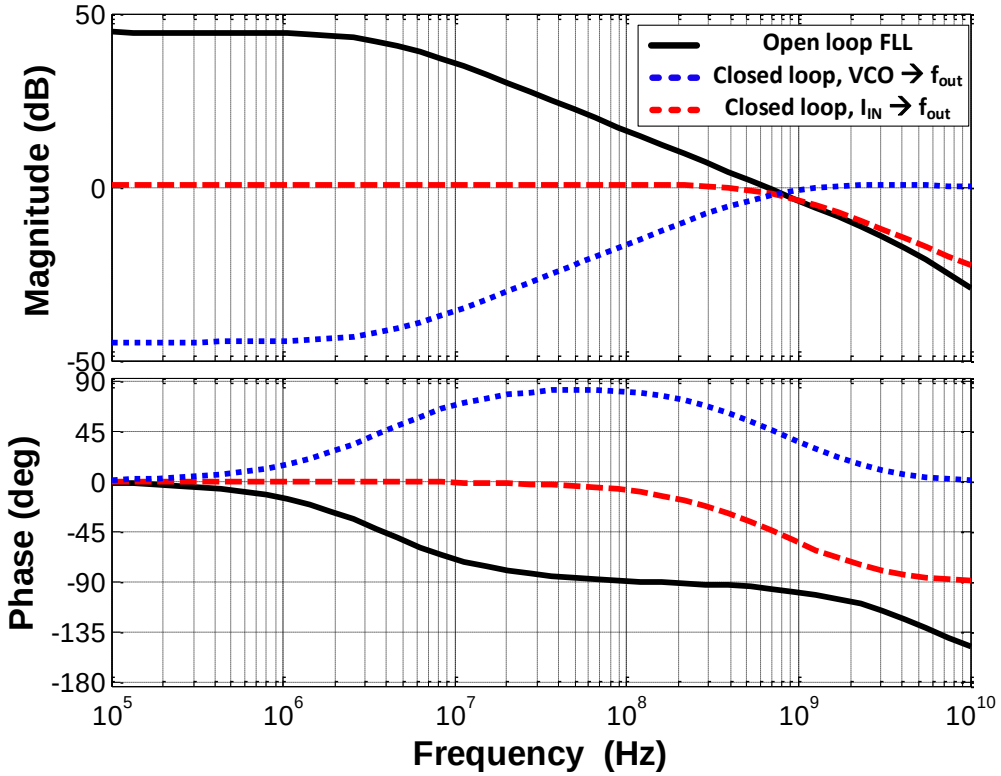


Figure 4.6 A Bode plot of open loop transfer function and closed transfer functions of the proposed FLL when V_s, K_{VCO}, R_s, f_{out} and C_{SW} are 0.25 V, 15 GHz/V, 17 Ω, 2GHz and 7.5pF, respectively.

v_{sw} is the voltage on the switched capacitor excluding the sawtooth ripple caused by the switching operation. Then, V_s can be defined as:

$$V_s = \left(1 + \frac{R_s}{R_{eq}}\right) V_{sw} \tag{18}$$

where V_{sw} is the DC voltage on the switched capacitor, which is 250 mV in this design. Then, v_{sw} can be found as

$$v_{sw}(t) = \frac{r_{eq}(t)}{R_s + r_{eq}(t)} V_s \tag{19}$$

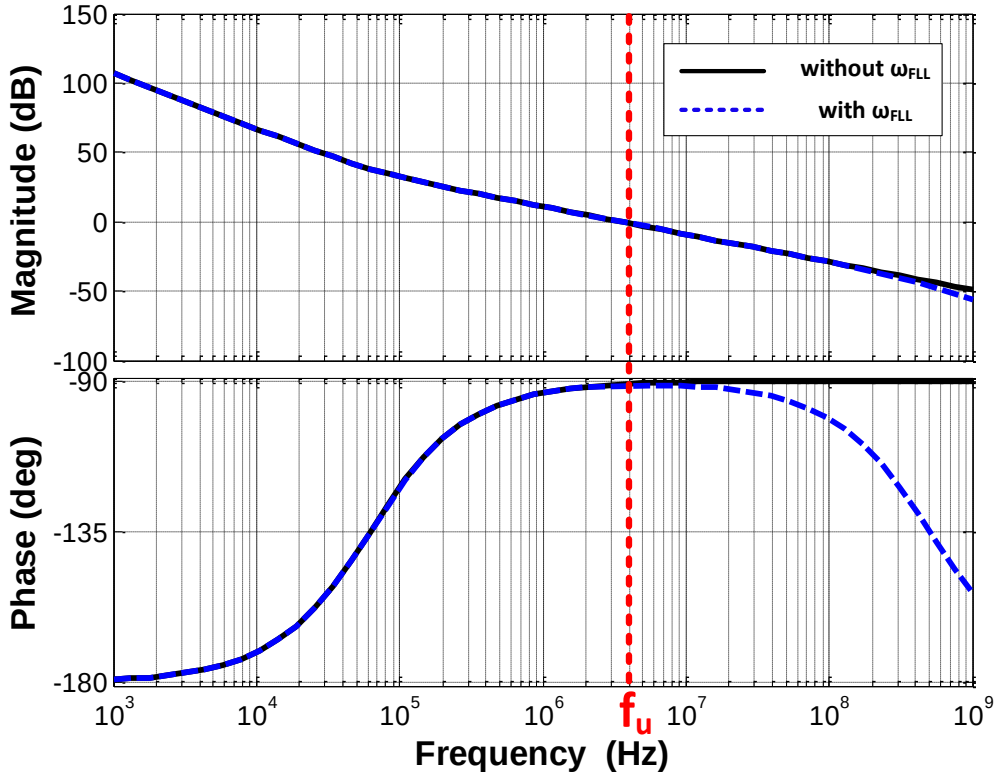


Figure 4.7 Open loop transfer function of the proposed PLL.

Therefore, the transfer function from the change of r_{eq} to the change of v_{sw} is determined using the following equation.

$$\frac{\partial v_{sw}}{\partial r_{eq}} = \frac{\partial}{\partial r_{eq}}\left(\frac{r_{eq}(t)}{R_s + r_{eq}(t)}V_s\right)_{r_{eq}(t)=R_{eq}} = \frac{R_s}{\left(R_{eq}+R_s\right)^2}V_s \tag{20}$$

Note that C_L is ignored for simplicity in (17). The gain from f_{out} to v_{sw} is calculated by combining (17) and (20) as shown in the following equation.

$$\begin{aligned}\frac{\partial v_{sw}}{\partial f_{out}} &= \frac{\partial v_{sw}}{\partial r_{eq}}\frac{\partial r_{eq}}{\partial f_{out}} = -\frac{1}{C_{sw}f_{out}^2}\frac{R_sV_s}{\left(R_{eq}+R_s\right)^2}\frac{1}{\left(1+s/\omega_{p2}\right)} \\ &= -\frac{R_sV_s}{C_{sw}\left(1/C_{sw}+f_{out}R_s\right)^2}\frac{1}{\left(1+s/\omega_{p2}\right)}\end{aligned} \tag{21}$$

ω_{p2} is the secondary pole generated by the C_L and parallel resistance of R_s and R_{eq}.

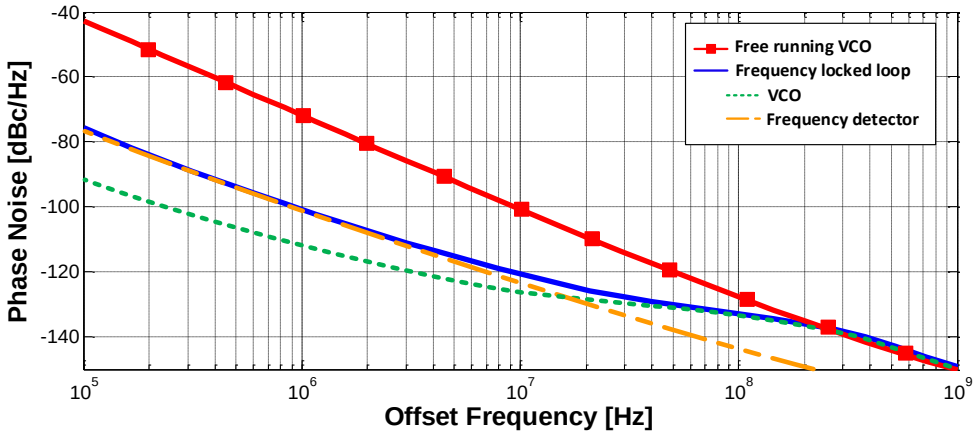


Figure 4.8 Simulated phase noise curves of the free running VCO (red) and the proposed frequency locked loop (blue)

$$\omega_{p2} = \frac{1}{C_L\left(R_s \,||\, R_{eq}\right)} \tag{22}$$

Finally, the feedback transfer function from f_{out} to the feedback current, i_f, is determined by multiplying $-g_{m1}$ by v_{sw}.

$$H_{fb}(s) = -g_{m1}\frac{\partial v_{sw}}{\partial f_{out}} = \frac{V_s}{C_{sw}\left(1/C_{sw} + f_{out}R_s\right)^2\left(1+s/\omega_{p2}\right)} \tag{23}$$

The linear model of the FLL is shown in Figure 4.5, and its open transfer function (black) is plotted in Figure 4.6 when V_s, K_{vco}, R_s, f_{out} and C_{sw} are 0.25 V, 15 GHz/V, 17 Ω, 2 GHz and 7.5 pF respectively. A wide regulation bandwidth (f_{BW}) of more than 500 MHz is achieved.

The closed loop gain is determined by the feedback factor using the following equation assuming a large feedforward path gain.

$$1/H_{fb}(0) = \frac{C_{sw}\left(1/C_{sw} + f_{out}R_s\right)^2}{V_s}\left[Hz/A\right] \tag{24}$$

To minimize the gain from the noise current to the output frequency, R_s must be minimized. However, given the DC bias current of I_{bias}, there is a limit to how much the transconductance can

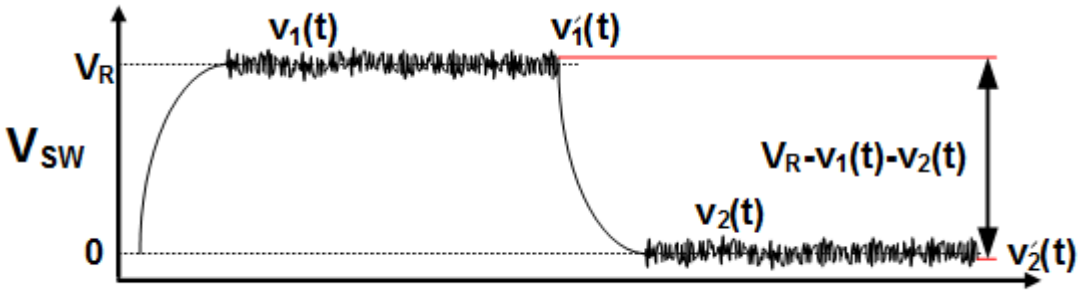


Figure 4.9 A transient waveform at the top node of C_{sw}

be increased, which is subthreshold transconductance, I_{bias}/mv_T. Therefore, the minimum closed loop gain can be found as the following.

$$A_{noise} = \frac{C_{sw}\left(1/C_{sw} + f_{out}R_s\right)^2}{V_s}\frac{I_{bias}}{f_{out}} = \frac{C_{sw}\left(1/C_{sw} + R_s/R_{eq}C_{sw}\right)^2}{\left(1+R_s/R_{eq}\right)V_{sw}}\frac{I_{bias}}{f_{out}}$$
$$= \frac{\left(1+R_s/R_{eq}\right)^2}{\left(1+R_s/R_{eq}\right)C_{sw}V_{sw}}\frac{I_{bias}}{f_{out}} = 1+\frac{R_s}{R_{eq}} \quad (25)$$

$$A_{noise,\min} = 1+\frac{mv_T/I_{bias}}{1/f_{out}C_{sw}} = 1+\frac{mv_T}{V_{sw}} \quad (26)$$

It can be seen that a large V_{sw} results in reduced noise gain; however, it also reduces the control voltage range. Therefore, a trade-off is made in the proposed design to set V_{sw} to 10 times v_T, allowing a 10% increase in noise gain while maintaining 400 mV control voltage range with 1V supply. A bode plot of the closed loop transfer function from the current input to the frequency output is displayed in Figure 4.6. The noise generated by the detection circuits, primarily due to the switched capacitor and biasing resistor, is low-pass filtered at the loop bandwidth.

4.3.1 A Linearized Loop Dynamics of the PLL

The linearized loop dynamics of the proposed PLL follows the conventional formula [138], [139], [156], [157] except for the parasitic non-dominant pole added by the FLL.

$$H_{OLG}(s) = \frac{T_{REF} K_{PD} K_{DCO} K_P}{2 \cdot s \cdot M} \left(1 + \frac{\omega_z}{s}\right) \frac{1}{1 + s/\omega_{FLL}} \tag{27}$$

where $K_{PD} = G \Big/ \sqrt{2\pi\sigma_{PLL}^2}$ [138], $\omega_z = K_I \Big/ \left(K_P T_{REF}\right)$ and σ_{PLL} is the PLL output jitter. G is 1 when the DCO noise dominates σ_{PLL} and 2 when PLL limit cycle dominates σ_{PLL}[138]. M and T_R are the frequency multiplication ratio and the period of reference clock respectively. Note that (27) is half of (7) in [156] because we assume BBPFD output is connected to 1LSB of the DCO control, and K_{DCO} is defined as a frequency step with LSB change. In this case, +1 and -1 outputs of BBPFD corresponds to the DCO frequency change of $+K_{DCO}/2$ and $-K_{DCO}/2$ making effective frequency gain of DCO be $K_{DCO}/2$. $1 \Big/ \left(1 + s/\omega_{FLL}\right)$ is the parasitic pole generated by the FLL, and ω_{FLL} can be approximated to $2\pi f_{BW}$. Note that the closed loop transfer function of the FLL is simplified to a first-order system in (18). As f_{BW} is order-of-magnitude higher compared to the unit gain frequency of $H_{OLG}(s)$, the effect of this parasitic pole is negligible. In Figure 4.7, open-loop transfer function of the proposed PLL is depicted when T_{REF}, K_{PD}, K_{DCO}, K_P, M, ω_z, and ω_{FLL} are 20n, 6.7×10^{10}, 1.3M, 1, 40, 390k and 3.1G, respectively. It can be seen that the effect of ω_{FLL} is negligible in the PLL loop dynamics.

4.4 Noise Analysis

One of the merits of the proposed architecture is that the output noise of the FLL is mostly determined by the frequency detection circuit. The VCO noise is high-pass filtered at the FLL bandwidth so that the noise becomes negligible when calculating the integrated phase noise, as shown in the closed loop transfer function from the VCO noise to f_{out}, Figure 4.6(blue, dotted). The noise generated by the detection circuit dominates the output noise across most of the frequency range because f_{BW} is large. Phase noise simulation results of the proposed FLL (blue)

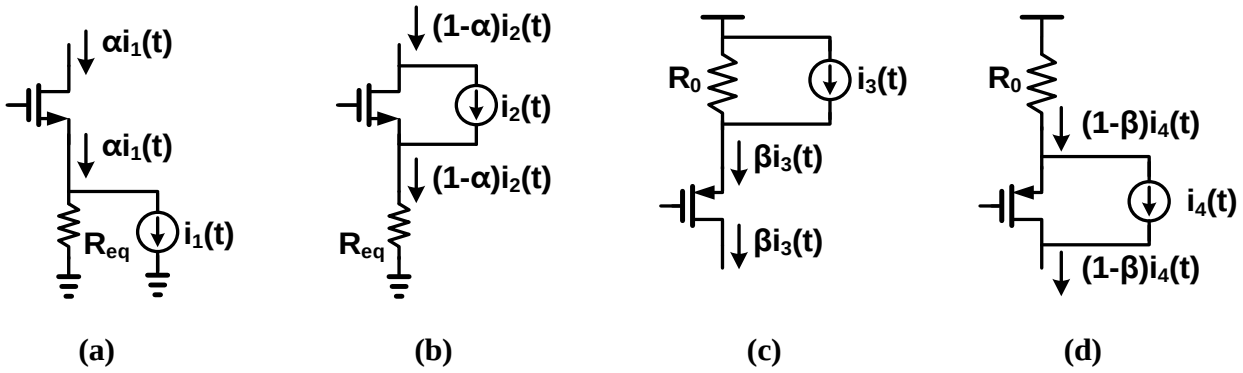


Figure 4.10 Current division branches in the frequency detection block.

and a free funning VCO (red) are plotted in Figure 4.8. The VCO noise is high-pass filtered at the FLL bandwidth (208MHz), and the lower frequency noise is dominated by the detection circuits.

To calculate the noise property of the detection circuit, we first need to analyze the current noise generated by the switched capacitor. Figure 4.9 shows the transient waveform at the top node of C_{sw}, V_c. The sampling operation happens twice per f_{out} cycle, once for charging it to V_{sw} and once for discharging it to ground. In each sampling process, kT/C noise with bandwidth $1/2f_{out}$ is generated, so its power spectral density can be written as

$$S_{v1}(f) = S_{v2}(f) = \frac{2kT}{C_{sw} f_{out}} \tag{28}$$

where v_1 and v_2 are the sampled voltages at V_c. The amount of charge injected at every switching cycle to V_{sw} can be written as $C_{sw}(v_1(t)-v_2(t))$, so the noise current of the switched capacitor can be calculated using the following equation.

$$i_1(t) = C_{sw} f_{out} \left(v_1(t) - v_2(t) \right) \tag{29}$$

As v_1 and v_2 are uncorrelated, the power spectral density of the switched capacitor noise can be written as the following equation.

$$\overline{i_1^2} = 4kTf_{out}C_{sw} = 4kT\frac{1}{R_{eq}} \tag{30}$$

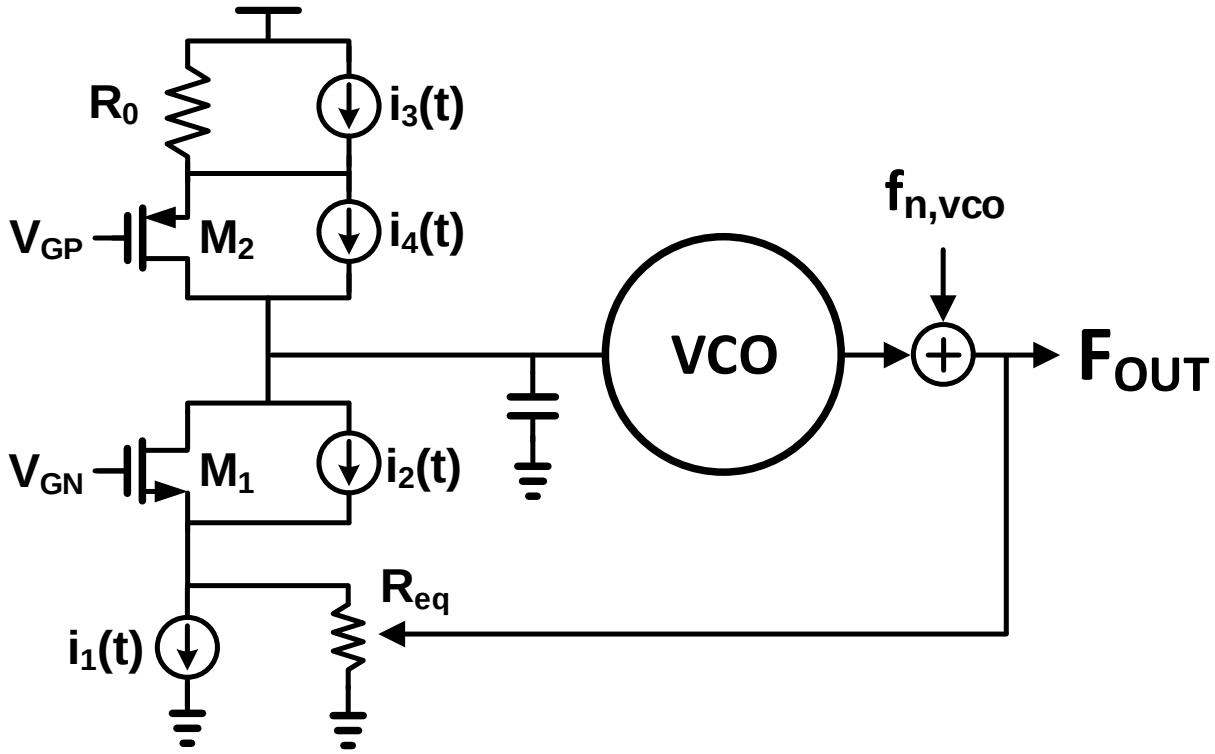


Figure 4.11 A schematic of the proposed FLL with the noise sources.

Note that the noise generated by the switched capacitor is equal to the noise of a physical resistor, whose size is equal to R_{eq}.

Then, we need to analyze the current division branches at the sources of M_1 and M_2. First, the current division ratio at the source of M_1 is analyzed in Figure 4.10. The equivalent current noise from the switched capacitor, $i_1(t)$, is divided by the impedance ratio of R_{eq} and R_s.

$$i_{out,1} = \frac{R_{eq}}{R_{eq} + R_s} i_1 = \alpha i_1 = \frac{1}{A_{noise}} i_1 \tag{31}$$

where $i_{out,1}$ is the amount of current produced at the output of the detection circuit. As mentioned in section 2, it is advantageous to increase the size of M_1 to reduce the noise gain. The current division ratio α is simply

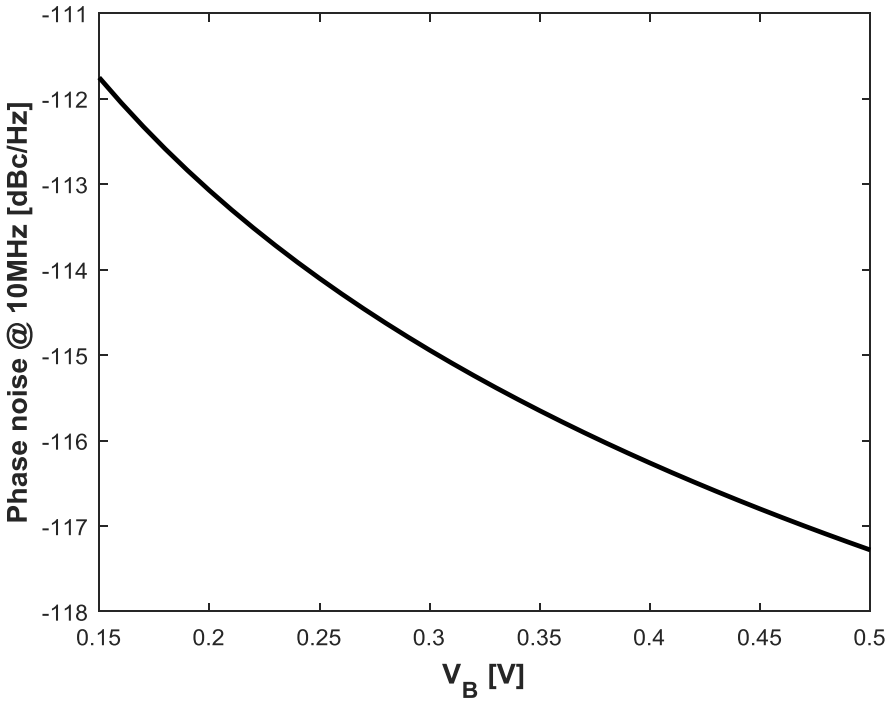


Figure 4.12 Phase noise at 10 MHz offset according to (4) when T, I_{bias}, γ_n, γ_p, v_T and f_{out} are 300°C, 3 mA, 2/3, 2/3, 26 mV and 2 GHz, respectively.

$$\alpha = \frac{\frac{V_{sw}}{I_{bias}}}{\frac{V_{sw}}{I_{bias}} + \frac{mv_T}{I_{bias}}} = \frac{V_{sw}}{V_{sw} + mv_T} \tag{32}$$

On the other hand, i_2, the noise generated by M_1, is highly degenerated by the source resistance M_1, and only a small fraction of i2 is delivered to the output, as described by the following equation.

$$i_{out,2} = (1-\alpha) i_2 \tag{33}$$

Similarly, the current noise from R_0 and M_2 can be calculated, as described the following equations

$$i_{out,3} = \beta i_3 \tag{34}$$

$$i_{out,4} = (1-\beta) i_4 \tag{35}$$

where β is the current division ratio at the source of M_2, which is defined as the following equation when M_2 is biased in a subthreshold region.

$$\beta = \frac{V_R}{V_R + mv_T} \tag{36}$$

Figure 4.11 shows equivalent noise sources in the detection circuit, $i_{1\text{-}4}(t)$. The output frequency noise can be calculated by multiplying the closed loop gain from the output current of the detection block by the output frequency. The noise contributions from C_{sw}, R_0, M_1 and M_2 can be found as follows:

$$L_{C_{sw}}(f) = \frac{4kT}{I_{bias}V_{sw}}\frac{f_{out}^2}{f^2} \tag{37}$$

$$L_{M_1}(f) = \left(\frac{1-\alpha}{\alpha}\right)^2 \frac{4kT\gamma_n g_{m1}}{I_{bias}^2}\frac{f_{out}^2}{f^2} \tag{38}$$

$$L_{R_0}(f) = \frac{\beta^2}{\alpha^2}\frac{4kT}{I_{bias}V_R}\frac{f_{out}^2}{f^2} \tag{39}$$

$$L_{M_2}(f) = \left(\frac{1-\beta}{\alpha}\right)^2 \frac{4kT\gamma_p g_{m1}}{I_{bias}^2}\frac{f_{out}^2}{f^2} \tag{40}$$

Note that the noise from M_1 and M_2 are relatively negligible compared with the noise from C_{sw} and R_0 because α and β are close to 1. By rewriting α and β in (37)-(40) using (32) and (36) and by summing all of the noise sources, the overall phase noise can be found as follows:

$$L(f) = \frac{4kT}{I_{bias}}\left(\frac{1}{V_{sw}}\left(1+\frac{\gamma_n mv_T}{V_{sw}}\right) + A_{noise}^2\frac{V_R+\gamma_p mv_T}{\left(V_R+mv_T\right)^2}\right)\frac{f_{out}^2}{f^2} \tag{41}$$

Detailed derivation on the phase noise is described in Appendix A. The discussion to this point shows that the output noise improves with a larger V_{sw}. A_{noise} is a function of V_{sw} as well, so increasing V_{sw} helps lower the noise not only from M_1 and C_{sw} but also from M_2 and R_0. The

smaller overdrive voltage of M_1 helps reduce the noise generated by M_1. Therefore, it is advantageous to maximize the transconductance of M_1 by increasing the width until M_1 operates in the subthreshold region. The latter part of (41) shows that increasing both V_R and $V_{ov,m2}$ helps reduce the output noise generated by M_1 and R_0. However, increasing V_R and $V_{ov,m2}$ limits the voltage tuning range of the VCO. As increasing V_R is almost two-fold more effective than increasing $V_{ov,m2}$, the size of M_2 should be again maximized until M_2 operates in the subthreshold region given a fixed voltage allocation of V_R and $V_{ov,m2}$ combined. Note that the overall phase noise has I_{bias} in the denominator, so the DCO noise can be reconfigured by tuning the bias current while keeping the bias conditions, V_{sw}, V_r, $V_{ov,m1}$ and $V_{mv,m2}$ constant. For instance, the FLL is configured in a low noise mode with a high current to prioritize noise performance. On the other hand, when power consumption is more important, the FLL is configured in a low current mode, sacrificing its noise performance.

In an attempt to find an optimal biasing condition on C_{sw}, R_0, M_1 and M_2, the conclusion thus far is to set M_1 and M_2 at subthreshold mode and maximize V_{sw} and V_R. Here, we will discuss a strategy in deciding the optimal ratio between V_{sw} and V_R. First, the voltage assigned to them is defined as V_B as follows.

$$V_B = V_{sw} + V_R = V_{DD} - V_{c,range} - 4v_T \tag{42}$$

where $V_{c,range}$ is the input voltage range of the VCO to generate the target frequency under the PVT variation. $4v_T$ is subtracted from V_{DD} as well to give sufficient V_{ds} to either M_1 or M_2. Then, (41) can be rewritten as the following by substituting V_R with V_B-V_{sw}.

$$L(f) = \frac{4kT}{I_{bias}}\left(\frac{1}{V_{sw}}\left(1+\frac{\gamma_n m v_T}{V_{sw}}\right)+\left(1+\frac{m v_T}{V_{sw}}\right)^2 \frac{V_B - V_{sw} + \gamma_p m v_T}{\left(V_B - V_{sw} + m v_T\right)^2}\right)\frac{f_{out}^2}{f^2} \tag{43}$$

The phase noise at 10 MHz offset is plotted in Figure 4.12 when T, I_{bias}, γ_n, γ_p, v_T, m and f_{out} are 300°C, 3 mA, 2/3, 2/3, 26 mV, 1.2 and 2 GHz, respectively. The optimal noise performance is achieved when V_R is almost equal to V_{sw}. The numerical solutions V_{sw}=0.271 and V_R=0.229 are found when V_B=0.5 after differentiating (34) and setting it equal to 0. Note that V_{sw} is weighted slightly more than V_R because A_{noise} affects both the noise from C_{sw} and V_R.

(43) can be simplified assuming equal V_R and V_{sw} to intuitively understand its theoretical limit in terms of its figure-of-merit (FoM).

$$\begin{aligned} L_{opt}(f) &\simeq \frac{4kT}{I_{bias}}\left(\frac{1}{V_{sw}}\left(1+\frac{\gamma_n m v_T}{V_{sw}}\right)+\frac{1}{V_R}\left(1+\frac{\gamma_p m v_T}{V_R}\right)\right)\frac{f_{out}^2}{f^2} \\ &= \frac{8kT}{I_{bias}V_{sw}}\left(1+\frac{\gamma_n m v_T}{V_{sw}}\right) \end{aligned} \tag{44}$$

Finally, the FoM of the proposed oscillator at its optimal biasing state can be found as the following.

$$\begin{aligned} FoM &= 10\log\frac{8kT}{I_{bias}V_{sw}}\left(1+\frac{\gamma_n m v_T}{V_{sw}}\right)\frac{f_{out}^2}{f^2}\times\frac{I_{bias}V_{DD}}{1mW}\times\frac{f^2}{f_{out}^2} \\ &= 10\log\frac{8kTV_{DD}}{10^{-3}V_{sw}}\left(1+\frac{\gamma_n m v_T}{V_{sw}}\right) \end{aligned} \tag{45}$$

The first observation regarding (45) is that the FoM of the proposed oscillator only depends on the voltage ratio of V_{DD} and V_{sw}, assuming $V_{SW} \gg \gamma_n v_T$. The theoretical FoM maximum is found when $V_{sw}=V_{DD}/2$, in which case $V_B=V_{DD}$, allowing zero voltage for $V_{c,range}$, M_1 and M_2. It is also assumed that $\gamma_n v_T/V_{sw} \ll 1$.

$$FoM_{\min} = 10\log\frac{8kTV_{DD}}{10^{-3}V_{DD}/2} = 10\log\frac{16kT}{10^{-3}} \approx -161.79 \tag{46}$$

As an example of a practical case, when V_{DD}=1, V_{sw}=V_R=0.25 and there is 10% additional power consumption in the VCO and non-overlapping clock generation, the FoM of the proposed

oscillator is -158.1 dBc/Hz. As a comparison, the theoretical FoM limit of a CMOS ring oscillator analyzed in [146] is determined as the following.

$$FoM_{\min,ring} = 10\log\frac{7.33kT}{10^{-3}} \approx -165.2 \quad (47)$$

The theoretical limit of the proposed oscillator is approximately 3.3 dB worse than that of a conventional ring oscillator. However, there are several other factors that need to be considered. 1) While adding transistors to give frequency tunability to a CMOS ring oscillator, the FoM typically gets worse. On the other hand, frequency tuning of the proposed oscillator can be achieved without FoM penalty. Therefore, the minimum FoM of a conventional ring oscillator is more over-estimated than that of the proposed oscillator. 2) The frequency tuning curve of the proposed oscillator is less sensitive to environmental change as it relies on an RC time constant rather than the transistor speed. 3) The proposed oscillator offers a highly linear frequency tuning curve, which is advantageous in the reduction of PLL loop bandwidth variation and two-point modulation [149]. 4) The proposed oscillator offers noise reconfiguration capability by programming its bias current. Therefore, the proposed oscillator is more efficient than a conventional ring oscillator in many applications.

4.5 Circuit Implementation

A schematic of the proposed circuit is shown in Figure 4.13. The gate voltages of M_1 and M_2 are generated using replica cells of the ones in the main branch. The amplifiers are designed to consume 500 nW so that the noise generated by those two amplifiers resides only in a very low frequency range and is filtered by the PLL loop. Low power voltage references are implemented using the 2-T structure proposed in [19]. R_0 and C_{SW} are used to tune the output frequency and the

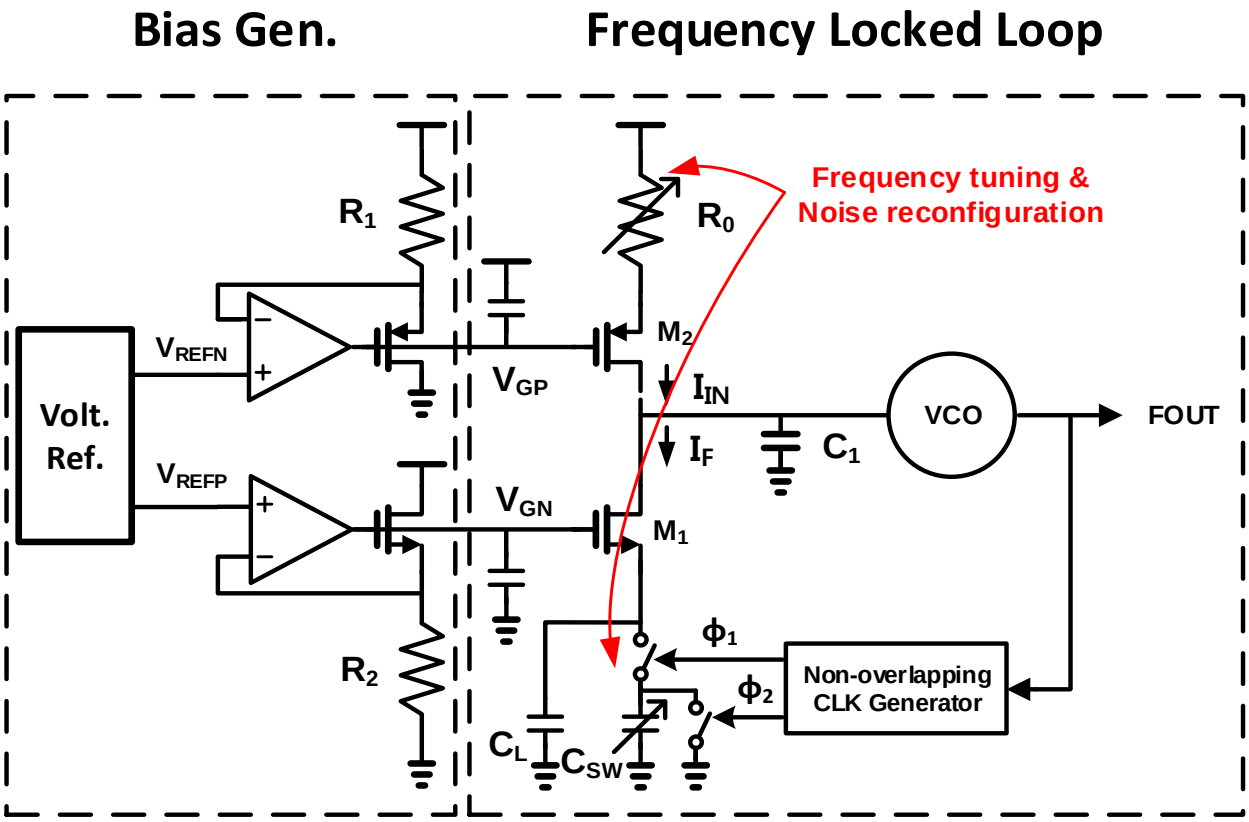


Figure 4.13 A block diagram of the proposed digital PLL.

noise. The size of M_1 and M_2 are tuned together with R_0 and C_{sw} so the voltages on R_0 and C_{sw} do not change depending on their values.

4.5.1 Multi-phase feedback

C_L is placed in parallel with C_{sw} to minimize the voltage ripple caused by the switching operation. When the switched capacitor is grounded, and only C_L is connected to the source of M_1, V_{sw} increases by the bias current, reducing the gate to the source voltage of M_1 as shown in Figure 4.14(a). Then, C_{SW} is connected to the source of M_1, causing an abrupt drop at the source voltage. The ripple magnitude is determined by the ratio between C_L and C_{SW}. If a small C_L is used, the voltage ripple becomes large, modulating V_{GS} of M_1 substantially. As M_1 provides a non-linear relationship between its V_{gs} and I_{ds}, such fluctuation can perturb the linearity of the DCO frequency

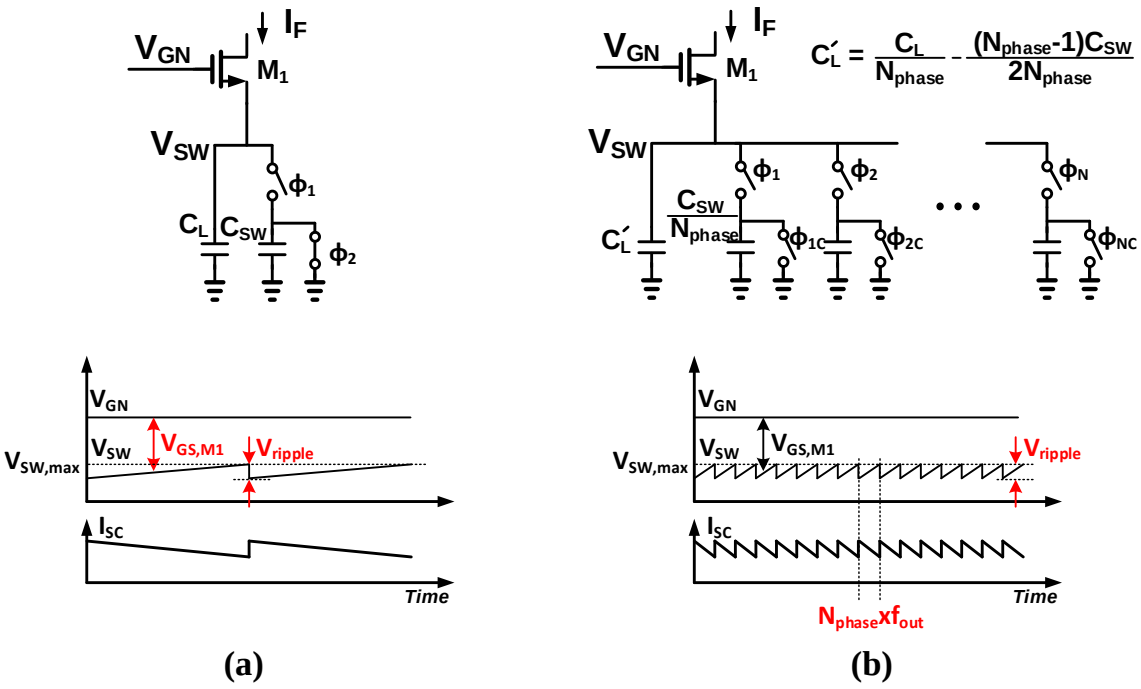


Figure 4.14 Voltage ripple caused by the switching operation (a) when a single phase is used (b) when multi-phases are used

tuning curve. Therefore, C_L must be at least 10x greater than C_{sw} to sufficiently lower the ripple magnitude. However, a large C_L incurs low second pole frequency in the FLL, degrading the stability and causing area penalty. In this work, we adopted multi-phase feedback from the VCO so that its effective switching frequency becomes N_{phase} times higher, where N_{phase} is the number of VCO phases as shown in Figure 4.14(b). Then, the total capacitance connected in parallel with the switching capacitance is reduced by the factor N_{phase}, and it helps to provide higher f_{BW} and phase margin. In addition, the multiphase feedback helps to reduce the area greatly. As the switching capacitance is reduced by the factor of N_{phase}, the total parallel capacitance can also be reduced by the same factor. Furthermore, nearly half of the non-switching capacitors are connected to the source of M_1, serving as parallel capacitors. Therefore, the size of the additional capacitance

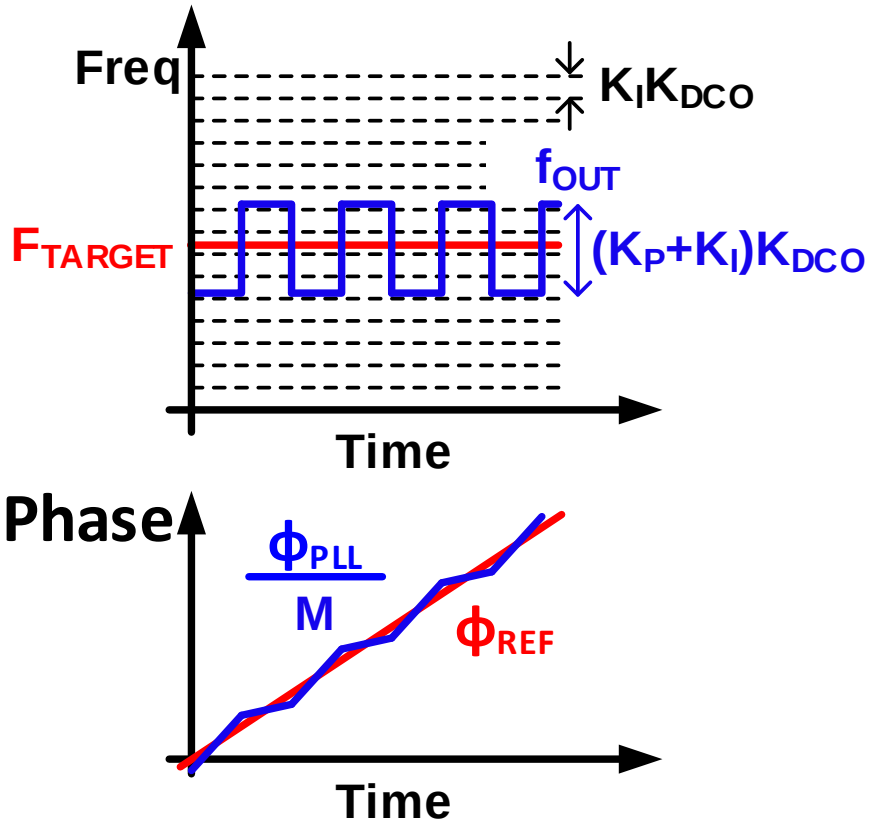


Figure 4.15 Behavior of a BBPFD-based digital PLL when DCO noise is not presented.

is $C_L/N_{phase}-(N_{phase}-1)C_{sw}/2N_{phase}$, which is approximately 5 pF, while the total switching capacitance is 7.5 pF. Compared with 75 pF, when single phase feedback is used, 93% of the area is saved.

4.6 Noise Detector

In this section, a noise detector circuit using the statistical behavior of the BBPFD output is demonstrated. A digital PLL using a BBPFD has a limit-cycle due to the non-linearity of the BBPFD. Assuming no DCO noise is present, the DCO control alternates between two numbers neighboring the target frequency at every reference cycle. The BBPFD output also alternates between 1 and 0, and the resulting feedback phase is shown in Figure 4.15. The VCO phase drawn in a blue color follows the reference phase. The peak difference between the feedback and

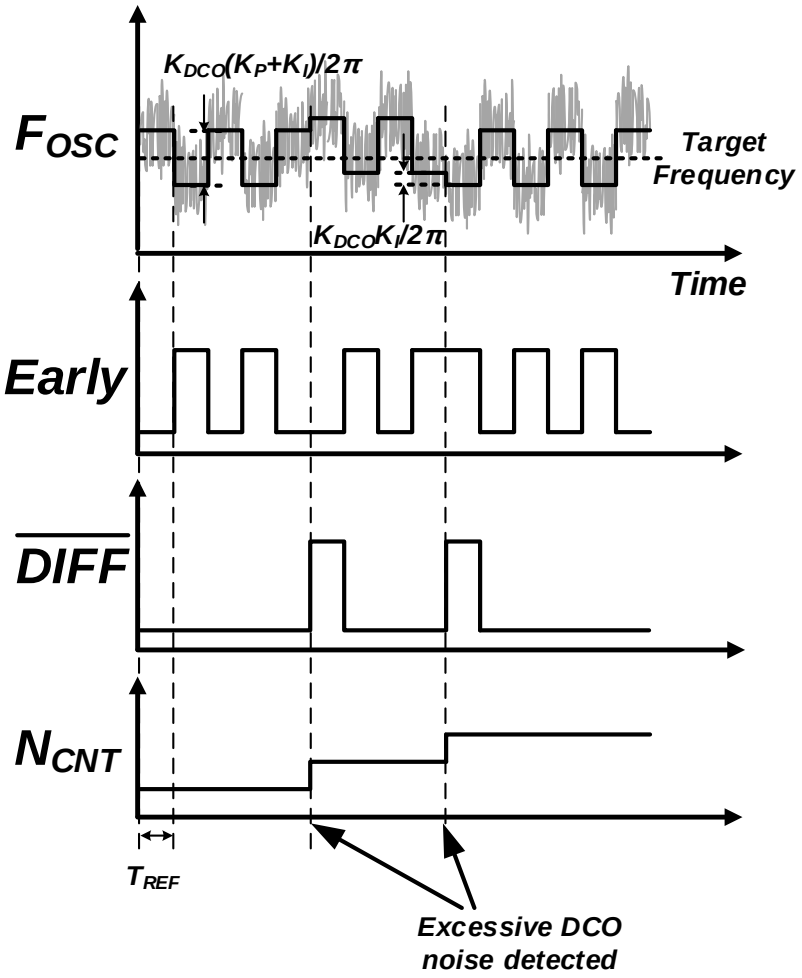


Figure 4.16 Transient waveforms (drawn from simulation results) of output frequency (f_{out}), PFD output (Early) and the noise detection result (DIFF).

reference phase is the magnitude of the limit cycle, Φ_{lmt}. It can be found as the following equation where K_{DCO} is the DCO gain, K_P is the proportional path gain, K_I is the integral path gain.

$$\Phi_{lmt} = \frac{K_{DCO}\left(K_P + K_I\right)T_{REF}}{2} \tag{48}$$

When DCO noise presents, it perturbs the DCO output phase, and its magnitude may exceed Φ_{lmt}. In such cases, BBPFD produces consecutive 1s or 0s. In Figure 4.16, Early is the output of the BBPFD. At times t_1 and t_2, BBPFD generates either consecutive 1s or 0s due to the excessive noise of the DCO.

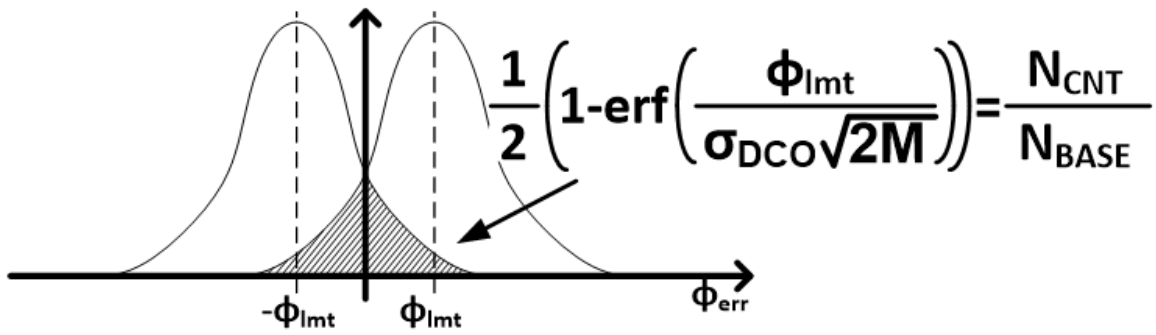


Figure 4.17 Histogram of the feedback phase.

The histogram of the feedback phase is shown in Figure 4.17. The DCO phase noise produces a Gaussian distribution in the feedback phase, and the limit cycle offsets the distribution by $\pm\Phi_{lmt}$. The shaded region represents the possibility that the DCO noise exceeds Φ_{lmt}, in which case the BBPFD produces either consecutive 1s or 0s. A schematic to detect such an event is shown in Figure 4.18. The BBPFD output is compared with its previous value, and when they are the same, the noise count is increased by 1. After N_{BASE} cycles of F_{REF}, the noise count N_{CNT} is delivered to the DCO control block. f_{out} is inversely proportional to the switching capacitance as shown in (3). Therefore, K_{DCO} can be accurately determined as a capacitance ratio between total switching capacitance, C_{SW} and unit capacitance, $f_{out}C_u/C_{sw}$, assuring robust operation of the noise detector.

As the DCO noise is adjusted using the proposed noise detector and the DCO gain is accurately controlled using a capacitor ratio, the PLL loop dynamics stay largely invariant to environmental changes. In this part, the PLL bandwidth and output jitter will be derived in terms of the DCO noise and other PLL configuration parameters. The unity gain frequency of the open loop transfer function of the PLL, f_u, can be found by equalizing the absolute value of (27) to 1 and it is

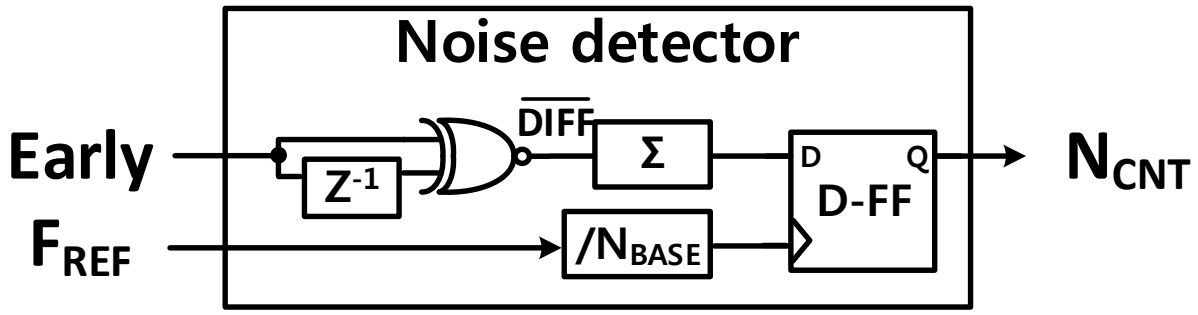


Figure 4.18 The proposed noise detection circuit.

$$f_u = \frac{1}{2\pi}\frac{T_{REF}K_{PD}K_{DCO}K_P}{2M} = \frac{1}{4\pi}\frac{T_{REF}K_{DCO}K_P}{M}\frac{G}{\sqrt{2\pi}\sigma_{PLL}}. \quad (49)$$

Assuming that the DCO noise is dominant at the output of the PLL and its flicker noise is negligible compared to the white noise, σ_{PLL} can be approximated as a function of σ_{DCO} and the PLL loop bandwidth as the following [158].

$$\sigma_{PLL} = \sigma_{DCO}\sqrt{\frac{f_{out}}{2\pi f_u}} = \sigma_{DCO}\sqrt{\frac{M}{2\pi f_u T_{REF}}}. \quad (50)$$

By combining (49) and (50), σ_{PLL} can be derived as

$$\sigma_{PLL} = \sigma_{DCO}^2\frac{2\sqrt{2\pi}M^2}{T_{REF}^2K_{DCO}K_PG}. \quad (51)$$

Note that σ_{PLL} is proportional to the square of the DCO noise because it exacerbates σ_{PLL} by reducing the phase detector gain as well as by its own power. Assuming an accurate DCO noise adjustment, σ_{DCO} can be derived from the equation shown in Figure 4.19.

$$\sigma_{DCO} = \frac{\Phi_{lmt}}{\sqrt{2M}\,erf^{-1}\left(1-\frac{2N_{CNT}}{N_{BASE}}\right)} \simeq \frac{K_{DCO}K_PT_{REF}}{2\sqrt{2M}\,erf^{-1}\left(1-\frac{2N_{CNT}}{N_{BASE}}\right)}. \quad (52)$$

Finally, f_u and σ_{PLL} can be expressed as the following equations which are independent to the environmental changes. Note that K_{DCO} is replaced to $(M/T_{REF})\times(C_u/C_{SW})$.

$$f_u = \frac{T_{REF}^3 K_{DCO}^2 K_P^2 G^2}{(4\pi)^2 M^3 \sigma_{DCO}^2} = \frac{T_{REF} G^2 \left(erf^{-1}\left(1 - \frac{2N_{CNT}}{N_{BASE}}\right)\right)^2}{2\pi^2 M^2} \quad (53)$$

$$\sigma_{PLL} = \frac{\sqrt{2\pi} M K_{DCO} K_P}{4\left(erf^{-1}\left(1 - \frac{2N_{CNT}}{N_{BASE}}\right)\right)^2 G} = \frac{\sqrt{2\pi} M^2 K_P \left(C_u / C_{SW}\right)}{4\left(erf^{-1}\left(1 - \frac{2N_{CNT}}{N_{BASE}}\right)\right)^2 T_{REF} G} \quad (54)$$

4.6.1 Overall Implementation

Figure 4.19 shows a block diagram of the proposed BBPFD-based digital PLL with PI control. A DCO Noise controller tunes R_0 and C_{SW} values while keeping their products constant at a value dependent on N_{CNT}/N_{BASE}, forming a noise self-adjustment loop. Note that I_{bias} is inversely proportional to R_0 as shown in (10) and (11), and the DCO noise is also inversely proportional to I_{bias} as shown in (41). DCO frequency tuning is achieved by controlling C_{sw}. The capacitance in an integral path consists of 6-bit coarse input, 10-bit fine input and 1-bit dithering input. The proportional path is designed with 5-bit control to maintain constant DCO gain while reconfiguring C_{sw}.

Figure 4.20 shows a transient waveform of the proposed PLL. Initially, an automatic frequency control (AFC) operates to find the switching capacitance that generates the target frequency. Then, the PLL loop is enabled to lock the output phase again using C_{con}. After phase lock is achieved, a binary noise search is enabled using the noise detection block. Overall phase locking is achieved within 10 μs, and the noise locking takes 5.2 ms with 50MHz reference clock.

4.7 Measurement Results

The proposed design is fabricated in a 28-nm FDSOI process. The overall area is 0.045 mm^2. The proposed PLL is tested with 50 MHz input frequency generated using a function

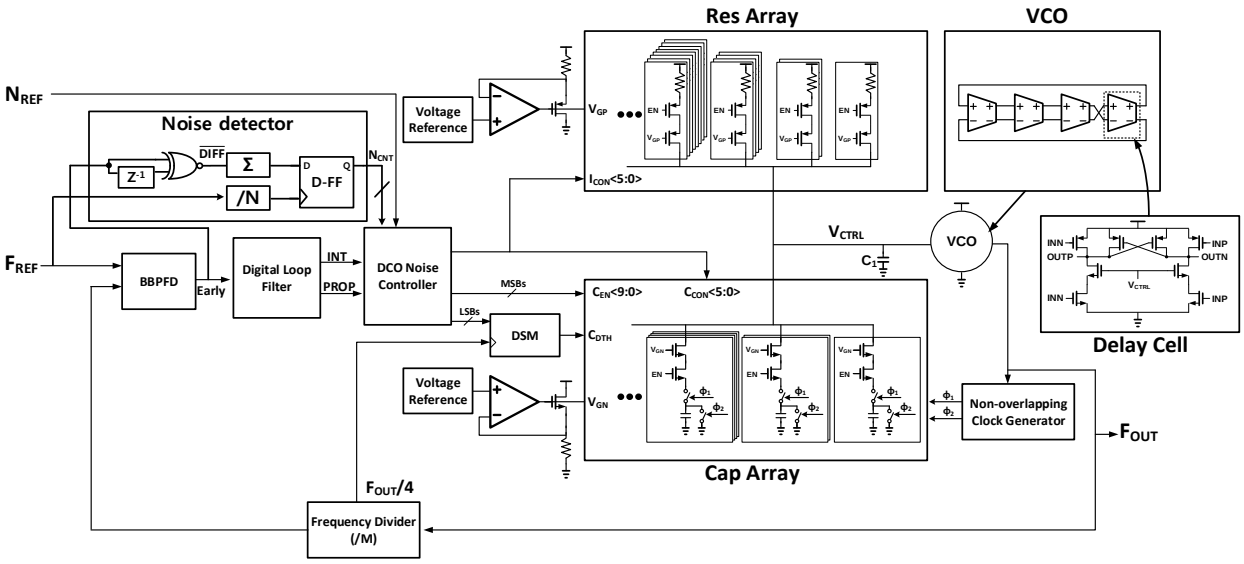


Figure 4.19 A detailed schematic of the proposed digital PLL.

generator (Keysight33600A), and its output noise is measured using a spectrum analyzer (Agilent N9030A). Frequency tuning curves of the proposed FLL is measured in Figure 4.21. It shows highly linear frequency tuning curve until the VCO tuning range is limited by the supply headroom. Figure 4.22 shows the power consumption of the PLL and the integrated phase noise. The integrated output phase noise is inversely proportional to the power consumption, as expected in (41). The integrated jitter can be configured from 2.5 to 15 ps while making a trade off with the power consumption from 1.7 to 5 mW. Figure 4.23 illustrates the function of the noise detection circuit depending on the configuration of the PLL. $K_{DCO} \times K_P$ is changed from 600kHz/LSB to 4MHz/LSB and $K_{DCO} \times K_I$ is adjusted in accordance with K_P keeping K_P/K_I as 128 assuring the PLL loop stability. The noise count shows a monotone relationship between the DCO noise amount and the noise count enabling the stable operation. The proposed noise detector assumes the Gaussian distribution of output noise. However, delta-sigma modulator (DSM) in the integral path generates quantization noise that does not follow a Gaussian distribution, and it can cause a discrepancy between the measurement and the theoretical calculation. This effect is more

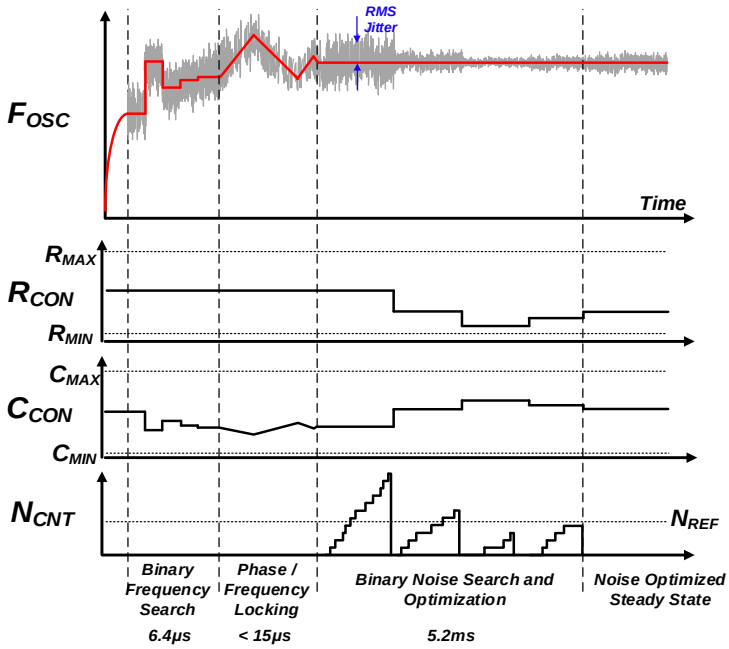


Figure 4.20 A transient waveform (drawn from simulation results) of the proposed PLL.

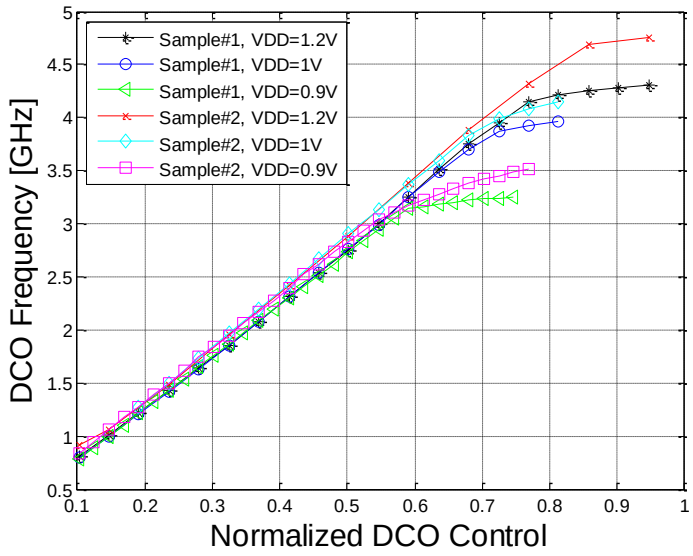


Figure 4.21 Measured DCO frequency tuning curve.

pronounced when the intrinsic DCO noise is small, i.e. when σ_{DCO}/Φ_{lmt} is small, making DSM quantization noise non-negligible as shown in Figure 4.23. The proposed PLL is tested with temperature sweep to verify the operation of noise self-adjustment. The DCO phase noise caused by device thermal noise is linear with temperature as shown in (41), whereas the PLL output jitter

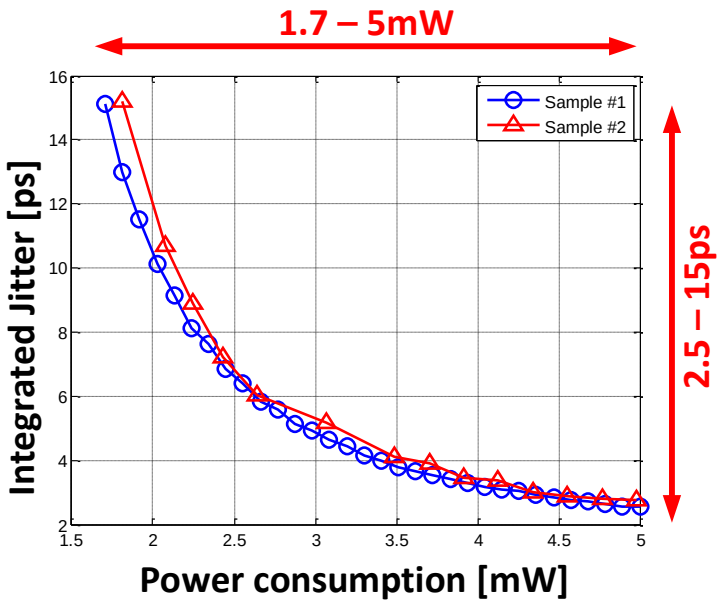


Figure 4.22 Measurement results of the integrated phase noise and the power consumption depending on the jitter configuration.

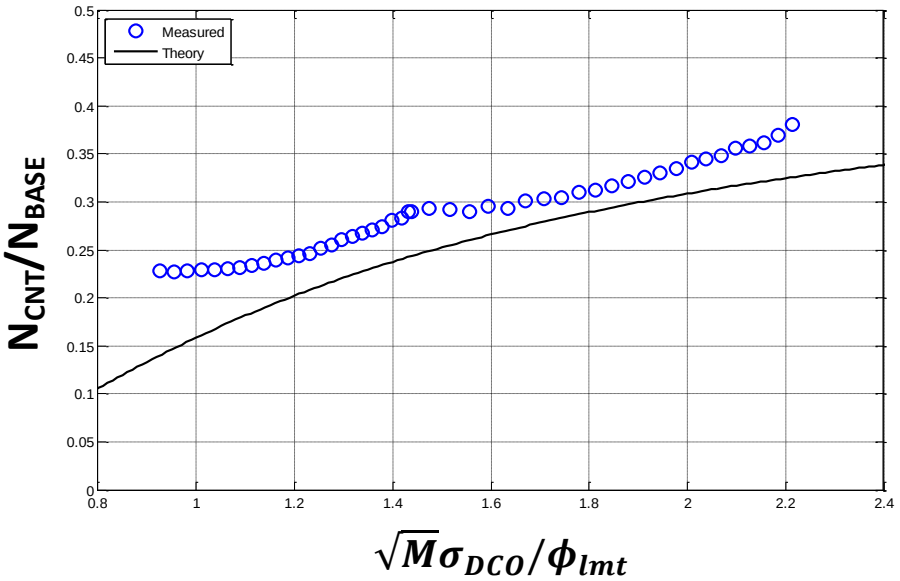


Figure 4.23 Measurement results of the noise detector output across varying DCO gain and noise.

is proportional to the square of the DCO jitter because of the reduced bandwidth (51). Therefore, the PLL jitter has a quadratic relationship with temperature as it can be observed in Figure 4.24.

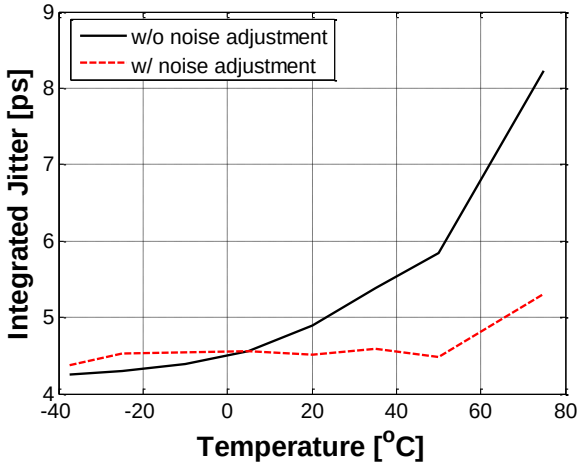


Figure 4.24 Measurement results of the integrated jitter depending on the temperature.

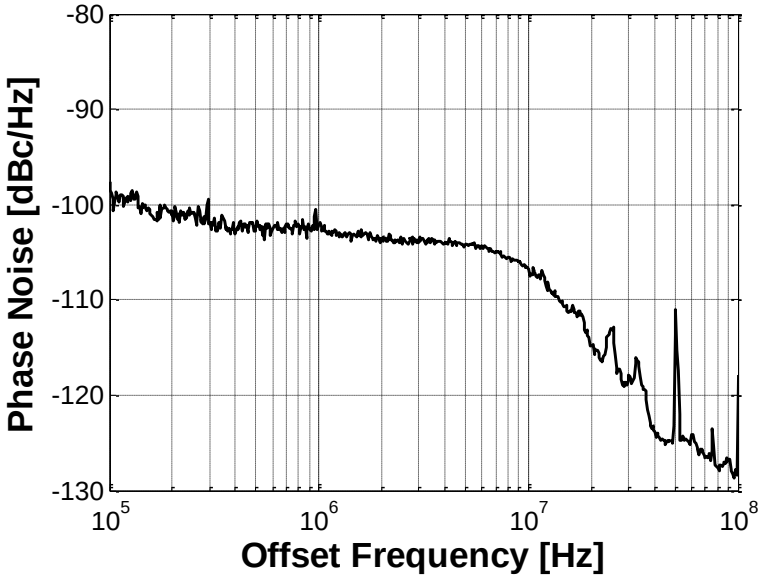


Figure 4.25 The phase noise measurement result when f_{out} is 2.4 GHz and the PLL is configured to the lowest noise mode.

When the noise adjustment is enabled, the output noise remains relatively constant to the temperature change.

Figure 4.25 shows the phase noise measurement results when the output frequency is 2.4 GHz and DCO is configured to a minimum noise state. The integrated phase noise is 2.522 ps while consuming 5 mW. A die photo of the layout is displayed in Figure 4.26. Table 4.1 compares

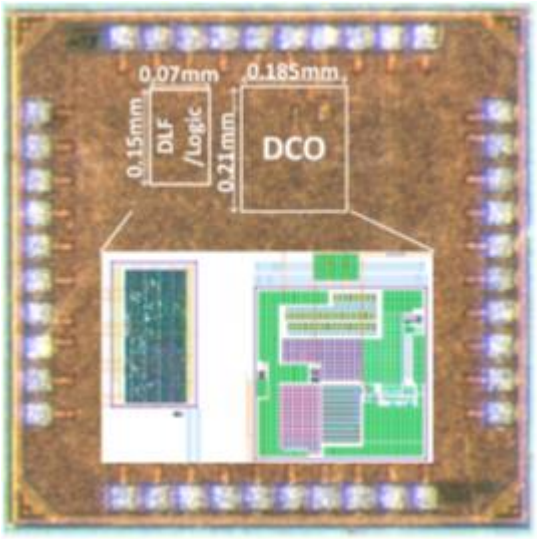


Figure 4.26 Die photo of the proposed design.

Table 4.1 Performance summary of the proposed design and comparison to prior arts of inductor-less designs.

	This work	[36]	[37]	[38]	[39]	[1]	[40]		[16]
Output Frequency (GHz)	0.8-3.2	3.2	2.4	1.6	0.2-3.8	0.2-3.2	0.8-1.8		2.4
Oscillator Type	Ring	Ring	Ring	Ring	Ring	Ring	Ring	MDLL	MDLL
Reference Frequency (MHz)	50	200	26	266	300	N/A	375	375	75
RMS Integrated Jitter (ps)	2.52 @ 2.4GHz	3.85	2.418	2.418	2.13*	3.1-14	3.2	0.4	0.7
Integration Range (MHz)	0.1-100	N/A	0.01-40	0.01-2	N/A*	0.01-100	0.01-100	0.01-100	0.01-40
Power Consumption (mW)	5 @ 2.4 GHz	2.915	6.4	2.7	1.98	0.7-3.4	0.9	0.6	0.43
Noise Reconfiguration	DCO Noise & Pwr	N/A	N/A	N/A	PLL Loop Bandwidth	N/A	N/A	N/A	N/A
Figure of Merit (dB)	-225.1 ~ -226.5	-224	-221.6	-226.7	-230.5	-224.8 ~ -218.6	-228.59	-248.7	-246.7
Area (mm^2)	0.049	0.0216	0.013	0.019	0.026	0.017	0.2	0.2	0.024
Technology	28nm SOI	40nm	40nm	65nm	65nm	22nm	130nm	130nm	28nm

the performance of the proposed PLL with previous works using ring oscillators. The proposed work provides a wide output frequency range of 0.8 to 3.2 GHz. Also, this work shows less than 3 ps integrated jitter while using a cost-effective 50 MHz reference. Overall, the proposed PLL shows competitive performance compared with the previous works while providing power and noise reconfiguration and noise self-adjustment capability.

4.8 Conclusions

In this chapter, a digital PLL using a nested FLL as a DCO is introduced. The proposed DCO provides accurate gain insensitive to the environmental changes as its period is locked to an R-C constant. Also, phase noise of the DCO can be controlled using a bias current, so it can be adaptively tuned according to the noise specification. Further, a noise detection and self-adjustment scheme is proposed to maintain constant noise performance under the environmental changes. The proposed work showed wide noise reconfigurability from 2.5 to 15ps while controlling its power consumption from 1.5 to 5mW.

CHAPTER 5

Miniaturized Logger for

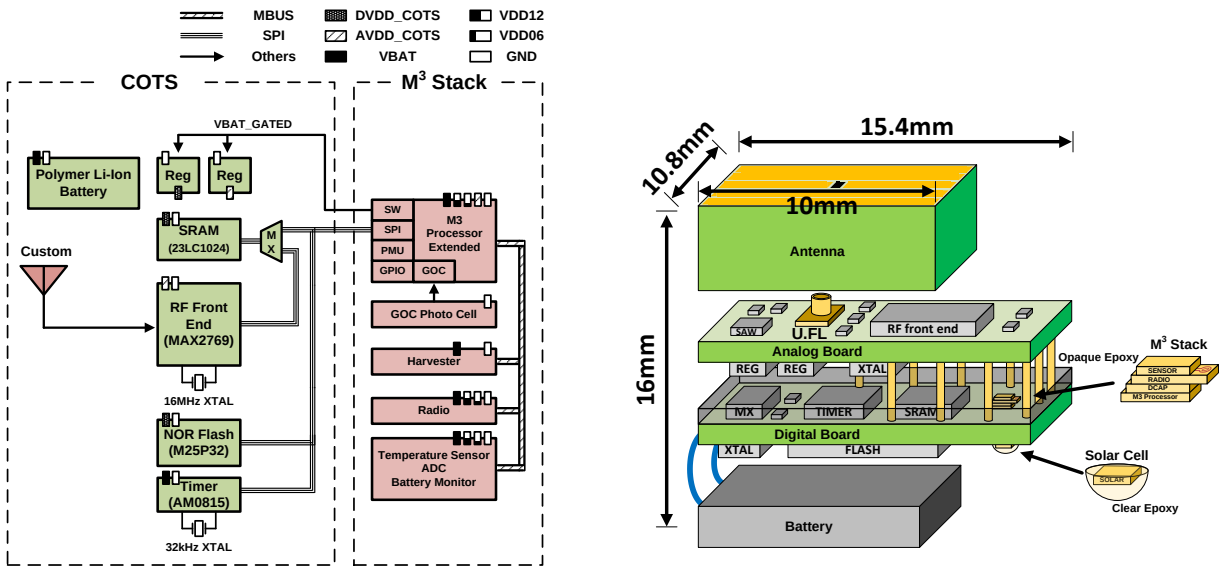
Global Navigation Satellite System

5.1 Introduction

A prototype design of a miniaturized global navigation satellite system (GNSS) is proposed in this chapter. An energy harvester, a power management unit and RF and optical transceivers are implemented to support energy-efficient, stand-alone operation. A sensor interface layer is also implemented to monitor environmental variables such as temperature and pressure.

5.2 Introduction

In this section, we introduce a prototype design of a GNSS logger implemented for position-tracking of an object. There is a growing demand for miniaturized, low power GPS receivers for use in child safety devices, drones, smart watches, smart grids, wearable devices and devices for tracking pets and vehicles. Many of these applications do not require a high rate or real-time position-tracking, so the power requirement is significantly reduced by heavily duty-cycling. The power of the GNSS signal is lower than the channel noise, and the small form factor makes it even smaller due to the small radiation efficiency. In this work, we developed a custom electrical antenna that achieved 20.66% radiation efficiency. In addition, we implemented an



(a) (b)

Figure 5.1 (a) Block diagram of the proposed GNSS logger and (b) conceptual graph of its assembly

autonomous system to sustain its operation with duty-cycling and energy harvesting by adopting the circuit techniques proposed in Chapter 2 of this dissertation.

A block diagram of the prototype design is shown in Figure 5.1. The system is managed by a Michigan Micro Mote (M^3) [3], which is a die-stacked system composed of an ARM Cortex-M0 processor layer, energy harvester, decoupling capacitor, global optical communication (GOC) receiver, sensor layer and RF transmitter. The processor layer includes 8 kB SRAM, which is programmed by using the GOC receiver. A power gating switch in the processor layer is used to turn off the external components. A gate-induced drain leakage (GIDL) reduction technique [159] is adopted to improve the on-off ratio of the switch. The off-leakage and on-resistance are measured as 0.4 nA and 4.1 Ω, respectively. A serial peripheral interface (SPI) and a set of general purpose input/output (GPIO) are used to control the external components. A PMU based on a

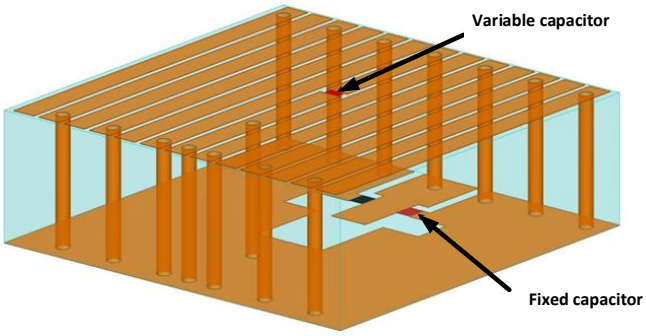


Figure 5.2 A CAD drawing of the printed antenna for the GNSS logger.

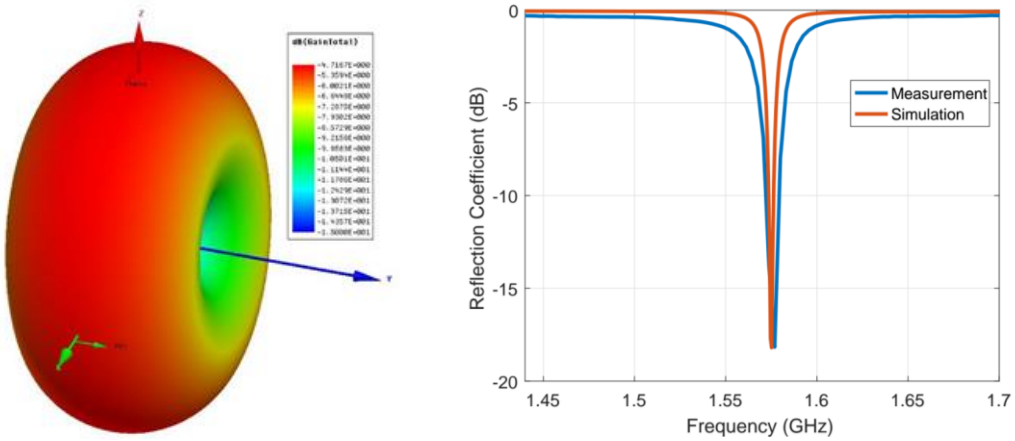


Figure 5.3 (a) The radiation pattern of the loop antenna (b) Simulation and measurement results of the reflection coefficient of the antenna.

successive-approximation switched-capacitor DC-DC converter (section VII, [108]) provides supply voltages to the M^3 stack layers. Its quiescent power and driving capability is programmable using the clock frequency so that the output driving strength is small and operates in low power mode during the sleep mode, while the output driving strength is high and operates in high mode during the active mode. The radio layer transmits the GPS data to the base station. The radio uses a monolithic inductor as an antenna to reduce the area requirement (section V-A, [160]) and provide a maximum bit rate of 40.7 kbps with 4.7 nJ/bit energy consumption. The sensor layer

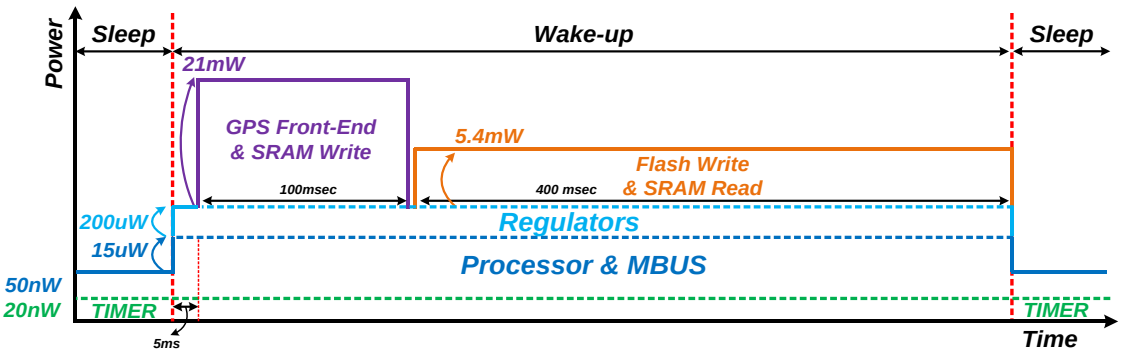
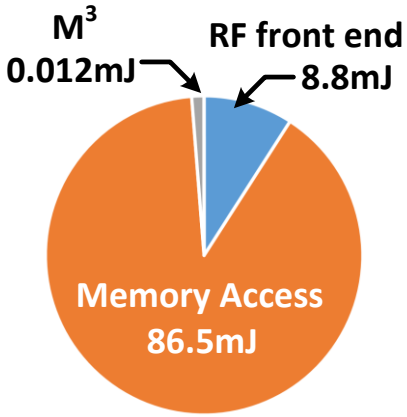


Figure 5.4 Timing diagram of the operation of the proposed GNSS logger

Item	Specification
Energy / fix	96.5 mJ
Fix interval (T_F)	5 Min
System life time	6.2 days
Battery Capacity (E_{BAT})	172.8 J
Standby Power (P_S)	100 nW
System size	12 x 15 x 20 mm



Total # of Fixes(N_{FIX}) = E_{BAT}/E_{tot} = 1791 Fixes

Figure 5.5 Breakdown of the energy consumption

measures the temperature and battery voltage of the system, which can potentially be used to further calibrate the RF front end and operation interval [2], [101], [161].

The electrically small antenna developed for the GNSS logger is connected to the analog board through a U.FL connection. A printed 3D loop geometry, depicted in Figure 5.2, is chosen for this application. The orange areas correspond to the metalized portions. A variable capacitor (top) and a fixed capacitor (bottom) are used for matching to 50 Ω. The antenna dimensions are 10×10×3.175 mm^3, and it is printed on Rogers RT/duroid® 5880. The copper sheet on the bottom side acts as a shield between the antenna and the rest of the system. In order to account for fabrication tolerances, a variable capacitor (cap trimmer) is used as one of the capacitors.

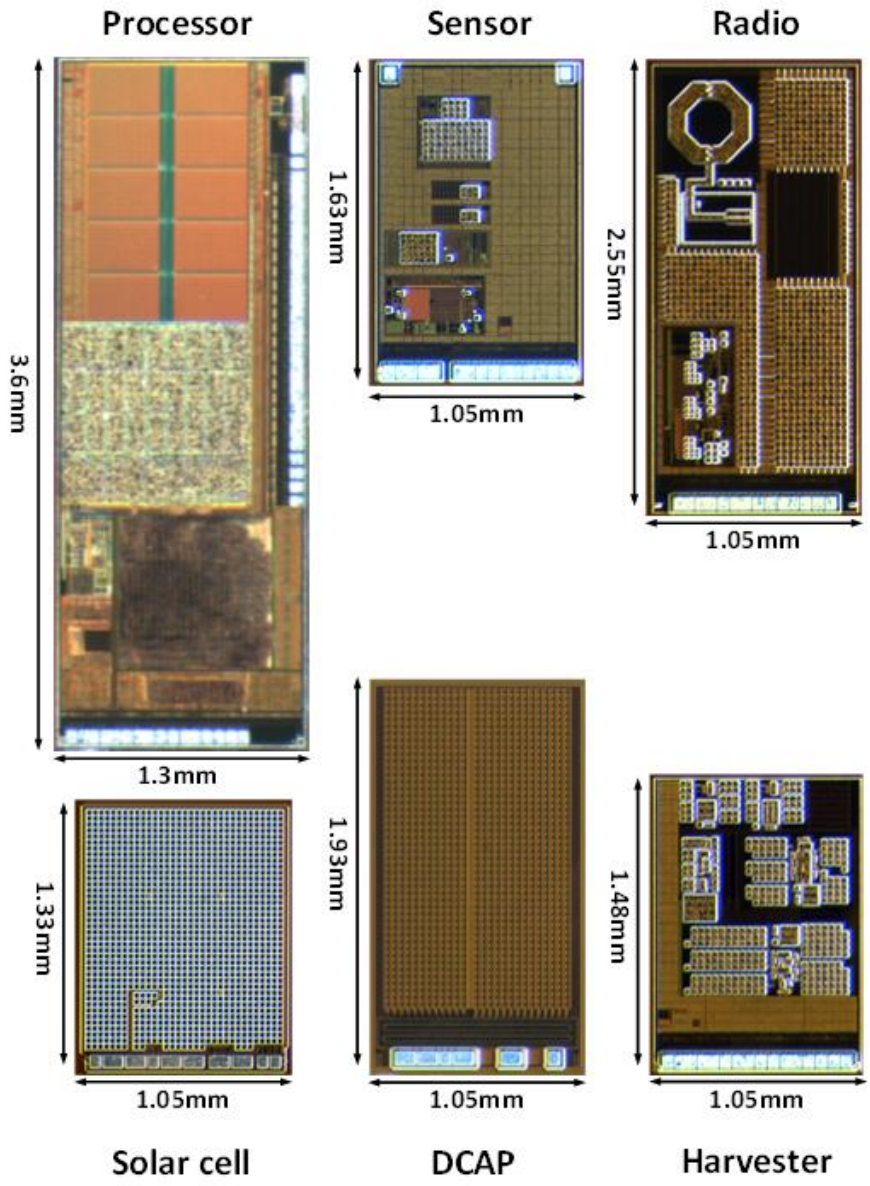


Figure 5.6 Die photos of M^3 system.

The antenna is simulated in ANSYS Electronics. Its radiation pattern is shown in Figure 5.3(a), and its simulated radiation efficiency is 20.66%. The reflection coefficient of the antenna, obtained through simulation and measurement, is plotted in Figure 5.4 (b), and it matches well at the frequency of interest (1.57542 GHz).

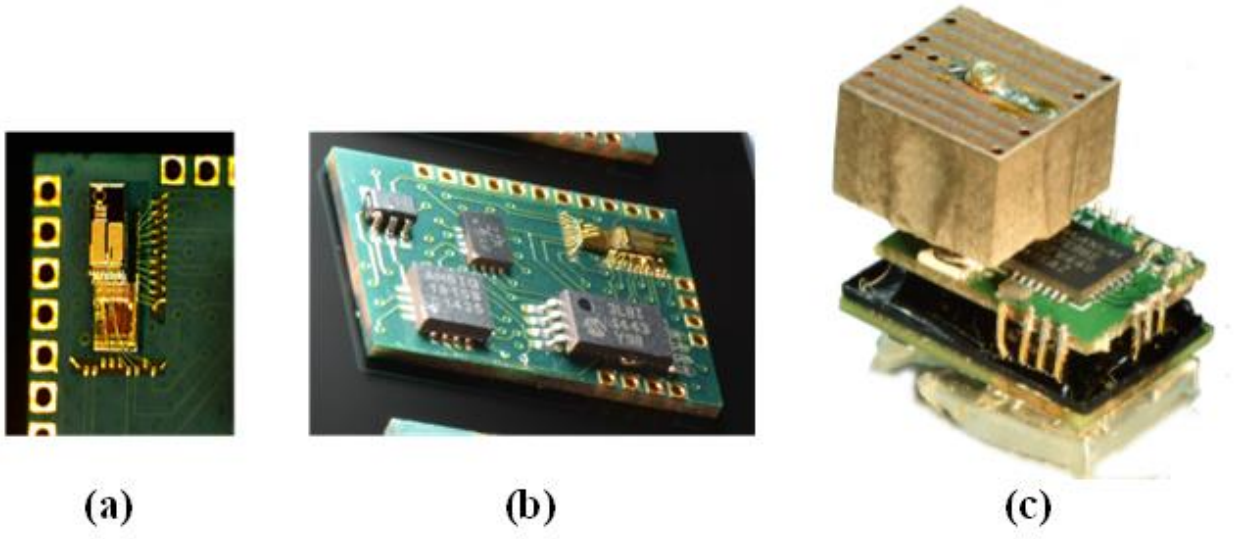


Figure 5.7 Photo graphs of the proposed system (a) On-PCB die stacking and wirebonding (b) board assembly (c) entire system

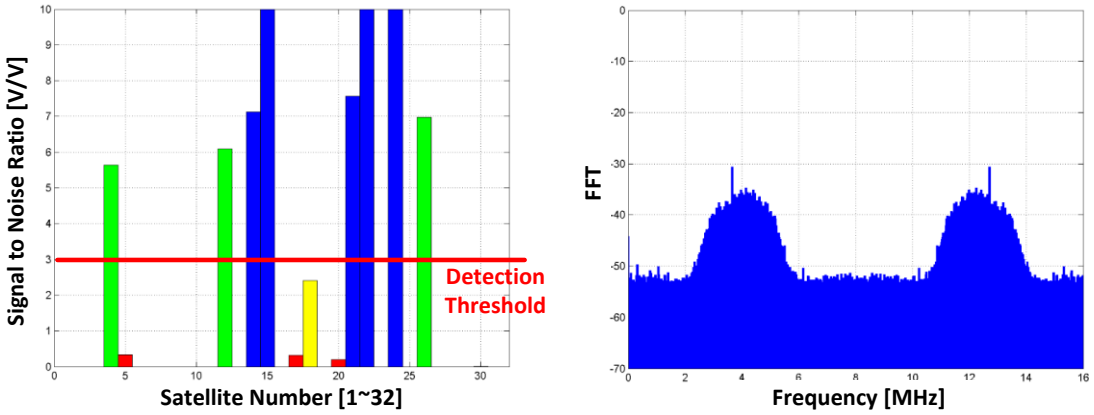


Figure 5.8 (a) Measured correlation results of the output of the GNSS logger (b) Fast Fourier transform of the IF signal

The RF front-end and IF stage of the GNSS receiver incorporates commercial products and a custom antenna. The MAX2769 RF front end chip is configured to use 4 MHz IF, and the quadrature data is produced at a rate of 16 MHz. The stream of data is stored in SRAM (23LC1024) and then transferred to a NOR flash (M25P32) together with the reception time produced by the

wake-up timer (AM0815). The correlation of the received data is processed in the base station after retrieving the data using the RF transmitter in the M^3-stack.

The system timing diagram is shown in Figure 5.4. The system is designed to have a programmable sleep time that can vary from a few minutes to multiple hours. After sleep, the system wakes up and initiates regulators, RF front-ends and SRAM within 5 ms. This time period is dominated by the startup of the 16 MHz crystal driven by the MAX2769. Then, the receiver is enabled to collect the data into the SRAM for 100 ms. The GPS data is transferred to a flash memory before the system goes back to sleep. The total energy consumption of the system is summarized in Figure 5.5. The system includes a 12 mAh polymer Li-ion battery, which can provide sufficient energy to collect 1,791 fixes without harvesting energy. The system can sustain its operation permanently with 12 klux light when the system operates at 10-min intervals.

Figure 5.6 shows the micrographs of the chips used to build the M^3 stack, and Figure 5.7 shows the digital board as well as the overall system. The size of the proposed system is $1.54\times1.08\times1.6$ cm^3. The digital board includes the M^3 stack, SRAM, flash and timer chips. The top side of the digital board is coated with black epoxy, which mechanically protects the M3 stack and blocks light. The bottom side is coated with clear epoxy to allow light to reach the PV cell. The antenna is connected to the analog board using a U.FL connector.

For testing, a GNSS signal is recorded for 30 minutes with a GNSS signal generator, LS01, and repeated using a horn antenna. The system is programmed to wake up every minute and acquire the received the GNSS signal. The measurement results of the GNSS logger after the correlation are shown in Figure 5.8. The system records IF GNSS signal quantized with 2-bit ADC for 100 ms. The correlation is performed in a base station after obtaining the data through radio communication. The system successfully acquired 8-10 satellites for each acquisition, which can

potentially enable ultra-low power miniaturized position tracking functions for child safety applications, drones, wearable devices and smart watches.

5.3 Conclusion

As a proto-type design, a 2.7cm^3 stand-alone GNSS logger is presented. The proposed logger has the capability to sustain its operation without energy harvesting for 5 days while acquiring GNSS data at five-minute intervals.

CHAPTER 6

Noise Improved Amplifier Using Parametric Amplification

6.1 Introduction

Miniaturized sensors are frequently used for *in situ* monitoring of bio-medical and environmental signals. In particular, neural recording sensor systems require miniaturization to limit brain tissue damage and accommodate tightly spaced electrodes. At the same time, neural potential sensor interface circuits must achieve aggressive input referred noise levels of <5 μVrms to monitor neural signals with sufficient accuracy. Given the small size and proximity to sensitive brain tissue, power consumption is also highly constrained to meet strict tissue heating limits.

Noise efficiency factor (NEF) is the typical metric to quantify the amplifier noise vs. power efficiency [42] with the goal of achieving low input referred noise while drawing low current. While some amplifiers [162] have approached the ideal NEF of 1 (i.e., the NEF of a single bipolar junction transistor), neural recording amplifiers tend to have much larger NEF (3-7) because of many other stringent specifications such as: high input impedance, low signal frequency, high common mode rejection ratio, and high power supply rejection ratio [163]. In this work, we plan to develop a new neural recording amplifier that achieves an NEF of 1.8 while meeting the other

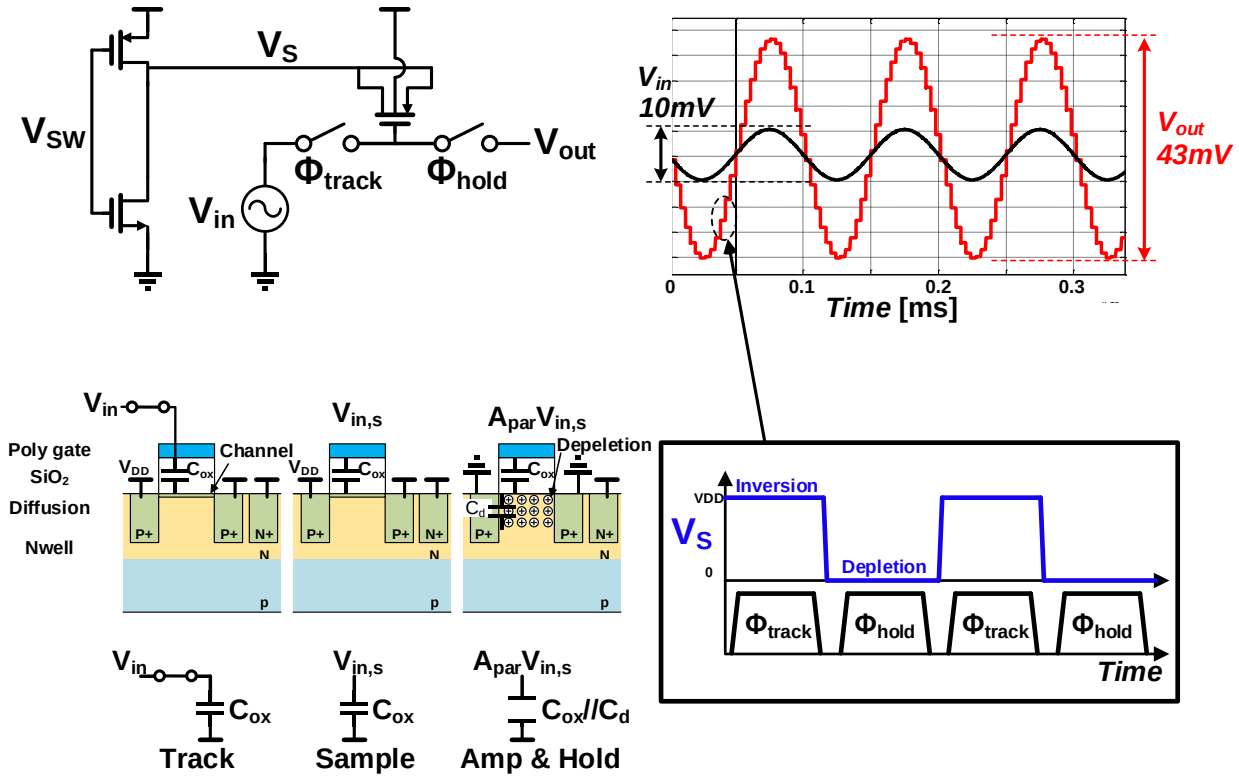


Figure 6.1 Schematic (top left), cross section view (bottom left), input and output voltages (right) of a PMOS discrete-time parametric amplifier (DC voltages are neglected)

listed specifications. We will use a pre-amplifier stage that performs parametric amplification based on MOS C-V characteristics; this is coupled with effective suppression of the sampling-induced kT/C noise by the electrode impedance. Power will be further limited with stepwise charging of the source voltage in the parametric amplifier.

6.2 Parametric Amplification

Parametric amplification via modulation of capacitance was introduced in [164], as shown in Figure 6.1. The DC gate voltage of the sampling capacitor sets the MOS capacitor in strong inversion during the track phase (V_s = VDD). After the input signal is sampled, the source voltage of the sampling p-type transistor is switched from VDD to GND, increasing the threshold voltage and setting the transistor in depletion mode. This reduces the gate capacitance, and with the total

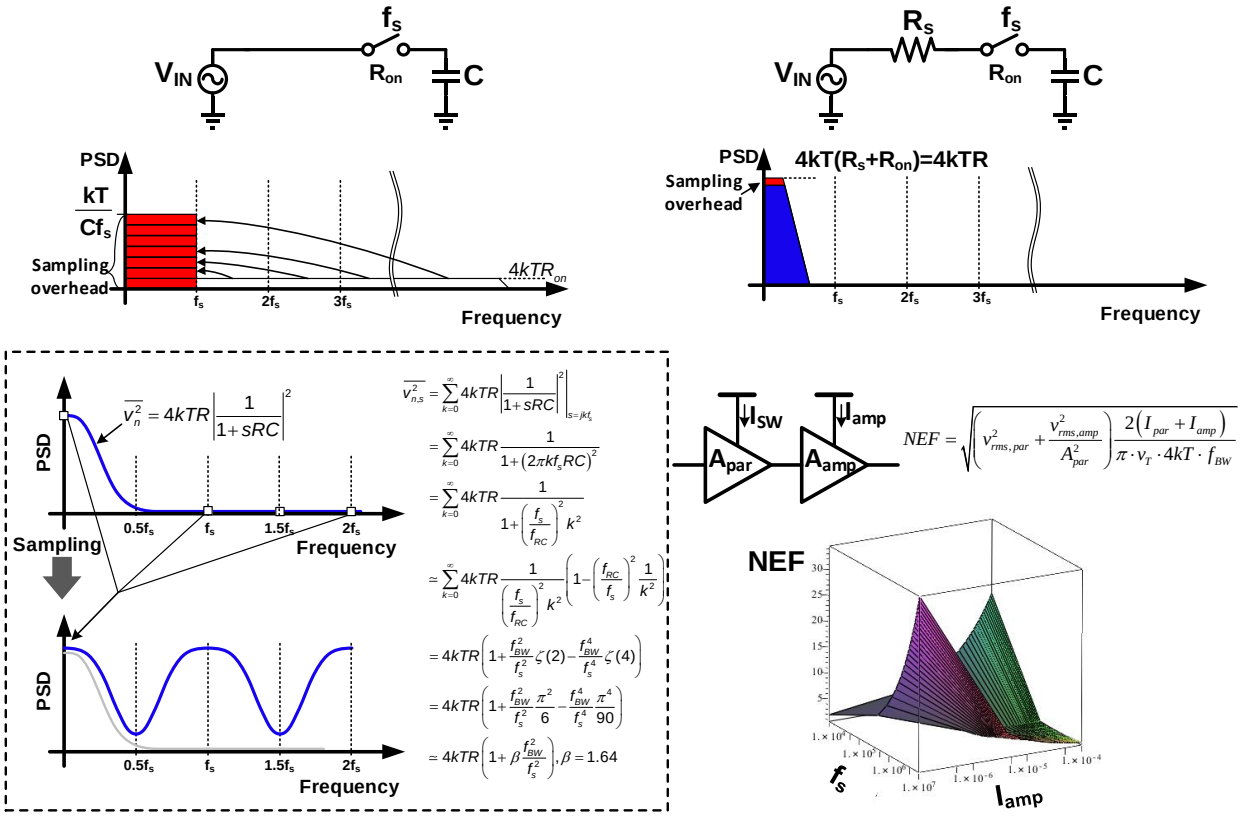


Figure 6.2 Sampling noise when the input bandwidth is larger than the sampling frequency (top left). Sampling noise when the input bandwidth is smaller than the sampling frequency due to a large source resistance (top right). Noise calculation after the sampling when the input bandwidth is smaller than the sampling frequency (bottom left). NEF calculation of an amplifier chain composed of a parametric and a conventional amplifier (bottom right).

charge on the capacitor unchanged, a "parametric" amplification of the input signal is achieved. However, sampling operation of the parametric amplifier incurs kT/C noise, making it difficult to achieve low input referred noise. When the input signal is sampled on the sampling capacitance C at rate f_s, the input referred noise floor becomes kT/Cf_s due to noise aliasing as shown in Figure 6.2 (top)

To address this issue, we first note that microelectrode-to-brain interfaces of neural recording probes typically exhibit large impedances (>100kΩ [163]), which set the input R-C

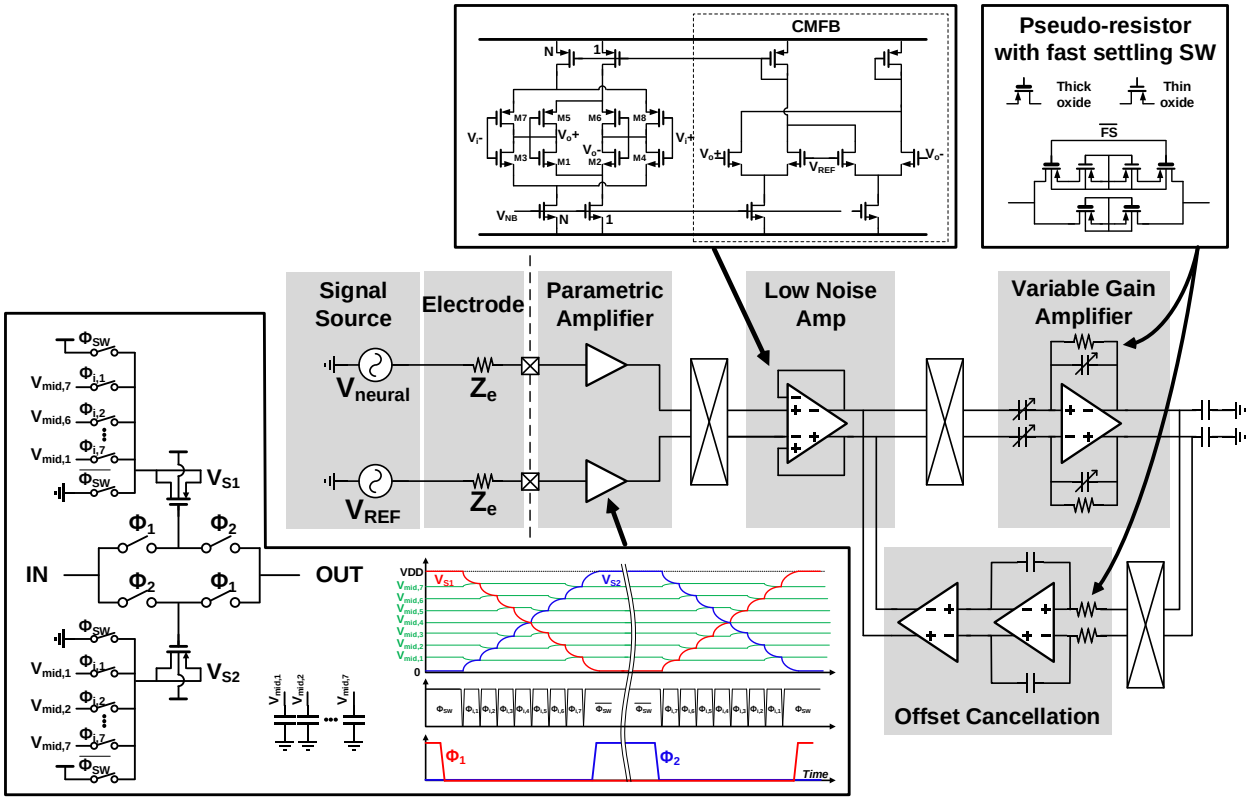


Figure 6.3 Schematic of the proposed instrumentation amplifier.

bandwidth to be far smaller than the sampling frequency, assuming a reasonable capacitor size of < 10pF (Figure 6.2). In this case, the additional noise generated by the sampling operation is $4kTR_{on}$ where R_{on} is the sampling switch on-resistance. A more detailed analysis is given in Figure 6.2 (bottom left) and shows that sampling noise becomes < 1% of resistor noise when f_s is 12.8× higher than the input R-C bandwidth. The NEF of the amplifier chain, consisting of a parametric and conventional amplifier can be further defined as follows:

$$NEF = \sqrt{\left(v_{rms,par}^2 + \frac{v_{rms,amp}^2}{A_{par}^2}\right)\frac{2\left(I_{par} + I_{amp}\right)}{\pi \cdot v_T \cdot 4kT \cdot f_{BW}}} \tag{55}$$

where $v_{rms,par}$, $v_{rms,amp}$, and A_{par} are the noise from parametric amplifier due to sampling, the following conventional (main) amplifier input referred noise, and the parametric amplifier gain, respectively. I_{par} and I_{amp} are switching currents of the parametric amplifier and the conventional

amplifier bias current, respectively. Note that input referred noise of the main amplifier is scaled by A_{par}. Increasing the sampling frequency can lower $v_{rms,par}$ by reducing noise aliasing at the expense of increased switching power for the MOS capacitor and $v_{rms,amp}$ reduces with larger I_{amp}, as expected. Therefore, the total amplifier chain NEF is a function of f_s and I_{amp} and is plotted in Figure 6.2 (bottom right) assuming a main amplifier NEF of 2. The north and south corners represent cases in which one of the amplifiers' current is large, such that the other amplifier dominates total noise. The optimum combination of f_s and I_{amp} exists through a line from west to east corner where noise and current levels of the parametric and main amplifiers are balanced.

6.3 Adiabatic Source Switching

In order to reduce NEF when using parametric amplification, it is critical that the source switching power at node V_s is kept small. In this work, we adopt an 8-phase soft-charging technique [165] to minimize the current overhead, as shown in Figure 6.3 (bottom). Instead of driving the source voltage directly to VDD or GND, the voltage is switched in small steps by charge sharing intermediate capacitors at each step. The intermediate voltages are uniformly self-defined after several cycles of transitions.

6.4 Proposed Neural Recording

Figure 6.3 shows the detailed schematic of the proposed amplifier. A variable gain amplifier (VGA), employs a conventional structure using capacitor ratio and is placed after the main amplifier. The low cutoff frequency of the amplifier chain is determined by the pseudo-resistor that forms a DC servo loop for the variable gain amplifier (VGA). A fast settling path is implemented using pseudo-resistors with a lower threshold voltage in order to reduce startup time while retaining a sufficiently large pseudo-resistance during normal operation. Note that this

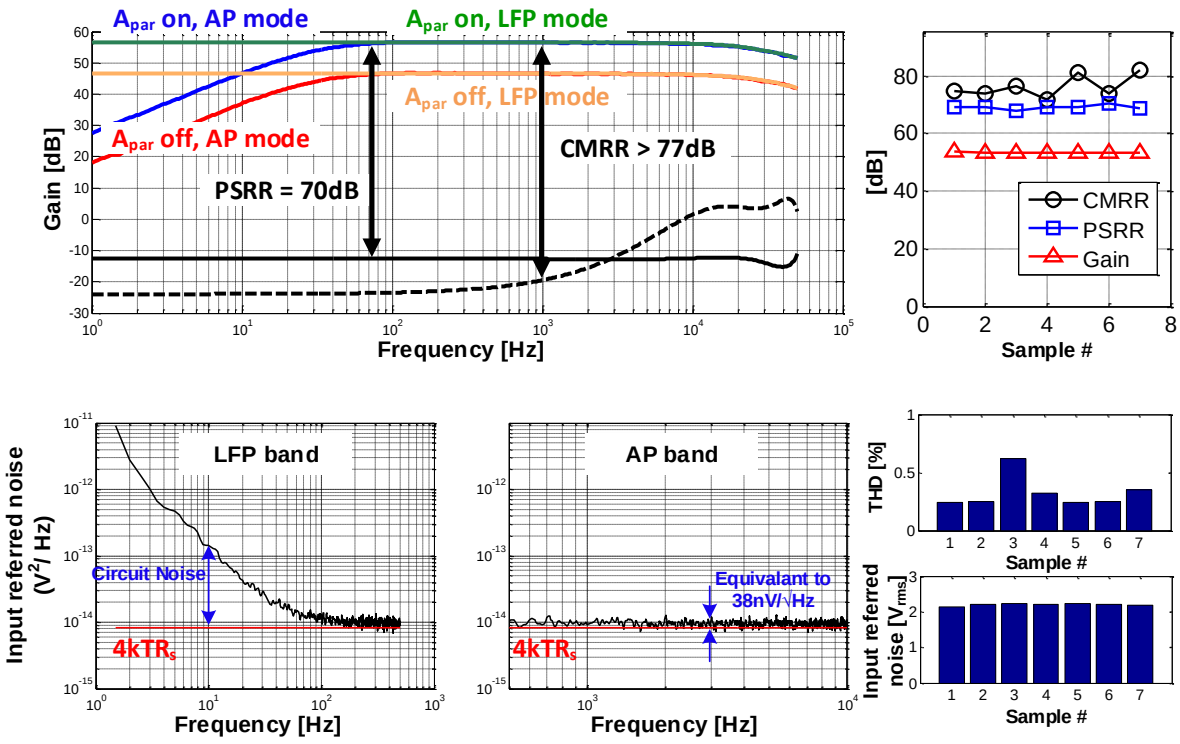


Figure 6.4 Measured transfer function, PSRR, CMRR, input referred noise and THD with 2mVpp input.

structure is not suitable for the low noise amplifier (LNA) and only as a third stage, variable gain amplifier due to its large input capacitance. As parametric amplifier gain depends on the capacitance ratio before and after switching the source voltage, a large LNA input capacitance can lower its gain. Instead, we adopt an LNA that achieves its gain of 4 using a g_m ratio as shown in Figure 6.3 (top). Device transconductance is proportional to the bias current when it operates in the subthreshold region. Therefore, LNA gain can be accurately controlled by using the current ratio.

6.5 Measurement Results

The proposed design is fabricated in 0.18µm CMOS technology with an area of 0.073mm^2. Figure 6.4 (top) shows the measured amplifier transfer function. The mid-band gain of the amplifier is improved by 3.37× by parametric amplification. The gain of the complete proposed amplifier is configurable from 30 to 60dB. The input referred noise is measured with 250kΩ source

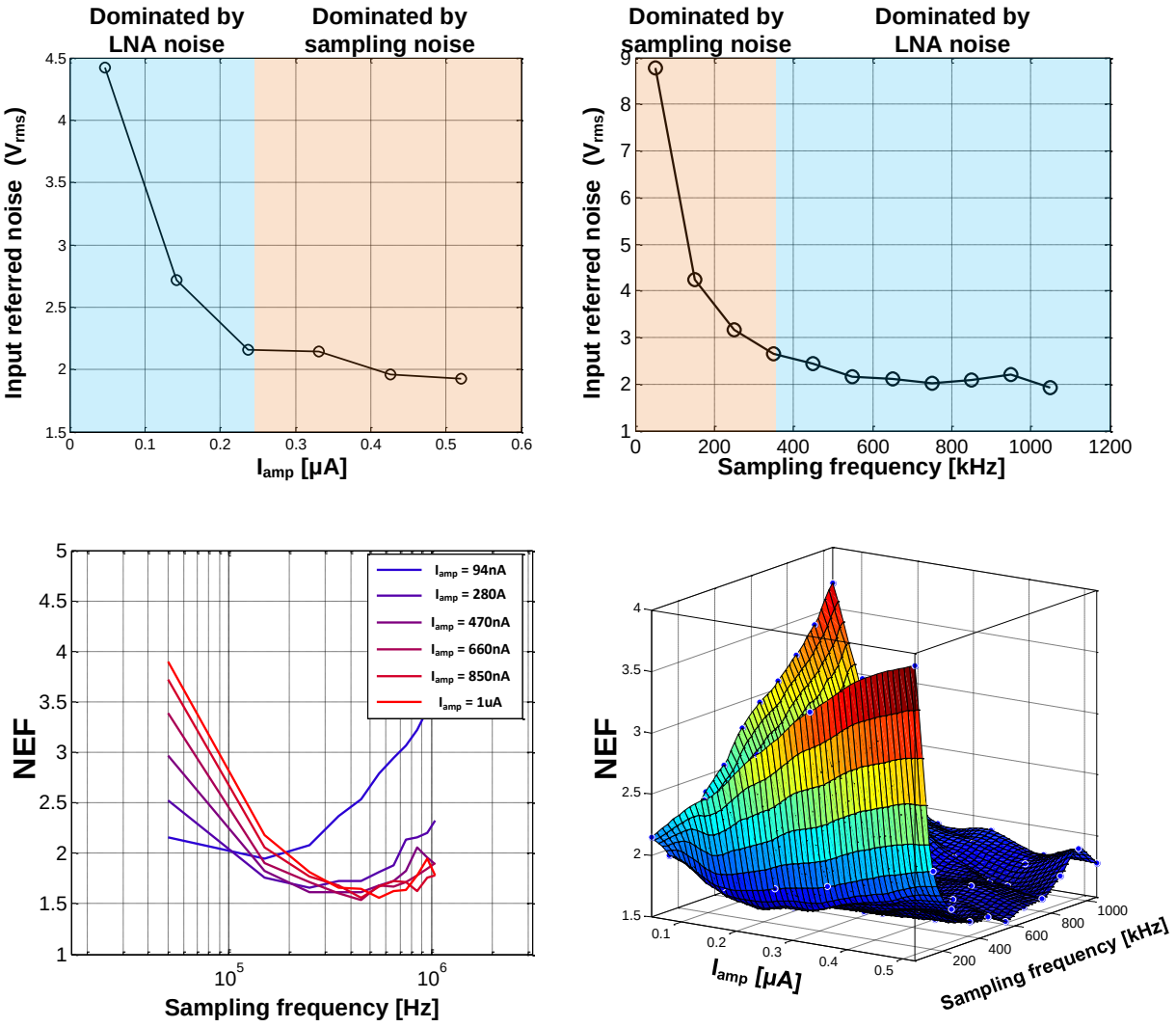


Figure 6.5 Measurement performance of the parametric amplifier + LNA. Input referred noise when f_s=550kHz (top left). Input referred noise when I_{amp}=470nA (top right). 2-D and 3-D plot of NEF as a function of I_{amp} and f_s (bottom).

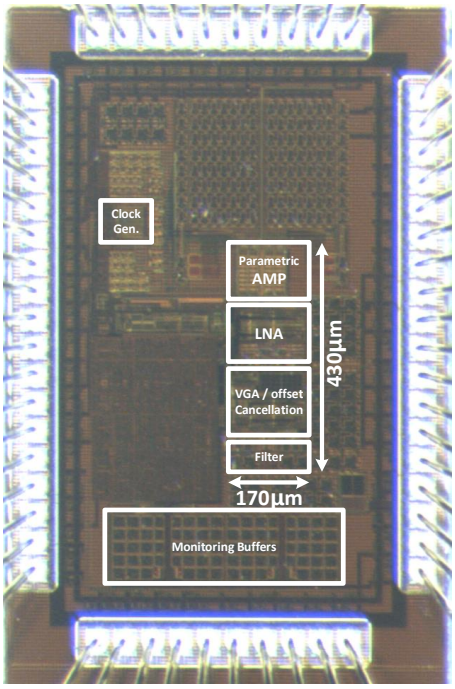


Figure 6.6 Die photograph of the proposed parametric amplifier based neural recording amplifier.

resistance and is shown in Figure 6.4. The input referred noise for the action potential (AP) frequency band (0.3-5kHz) is measured to be 2.1µVrms while consuming 2.4µW from 1.2V. The measured input referred noise for the local field potential (LFP) band (1-500Hz) is 3.5 µVrms. In addition, the performance metrics of 7 samples are plotted in Figure 6.4 (right). Neural recording front ends are often implemented as an array of a large number of channels, allowing for the non-overlapping clock generator, charge sharing capacitors, and reference current generators to be shared. In the calculation of power and area, the aforementioned building blocks are considered amortized as in a multi-channel recording system.

Figure 6.5 shows the measured noise characteristic of the proposed amplifier while varying LNA amplifier bias current and parametric amplifier sampling frequency. With a fixed sampling frequency of 450 kHz, total noise is dominated by the LNA when I_{amp} is small and the noise eventually saturates at larger I_{amp} when sampling noise starts to dominate (Figure 6.5, top left).

Table 6.1 Performance comparison with state-of-the-art instrumentation amplifiers for neural recording.

	This work		Ng, ISSCC2015	Muller, ISSCC2014	Chandrakumar, ISSCC2016	Chandrakumar, ISSCC2017	Lopez, ISSCC2013
Power (μW)	2.4		2.8	2.8	2	2.8	5.4
Input referred Noise (μV_{rms})	AP: 2.1 LFP: 3.5		4.13	1.3	AP: 7 LFP: 2	AP: 5.2 LFP: 1.8	3.2
Bandwidth (Hz)	1-5000		1-8200	1-500	1-5000	1-5000	300-6000
NEF	Parametric Amp + LNA	AP: 1.55 LFP: 2.68	2.93	4.76	AP: 4.9 LFP: 7	AP: 4.4 LFP: 7.4	2.83
	P-AMP + LNA + VGA + Offset AMP	AP: 1.8 LFP: 3.07					
Gain (dB)	30-60		57.8	-	-	-	30-74
Signal type	AP+LFP		AP+LFP	LFP	AP+LFP	AP+LFP	AP
Input common mode range (mV_{pp})	45		200	-	40	40	-
Input impedance (MΩ)	74		-	28	300	1600	-
PSRR (dB)	> 70		78	-	-	-	70
CMRR (dB)	> 70		> 80	-	-	-	60
THD	1% ($4mV_{pp}$)		-	-	-74 dB	-76 dB	1% ($9mV_{pp}$)
Size (mm^2)	0.071		0.042	0.025	0.071	0.069	0.088[1]
Technology	0.18μm		65nm	65nm	40nm	65nm	0.18μm

[1] Estimated

Similarly, output noise also decreases as the sampling frequency increases until it saturates to the noise level of the LNA (Figure 6.5, top right). Therefore, an optimal NEF is achieved when the noise sources are balanced with each other, as seen in Figure 6.5 (bottom left). Table 6.1 summarizes the performance of the proposed design. The combination of the parametric amplifier and the LNA achieves 1.55 NEF when integrating noise from 300 Hz to 5 kHz for spike detection while also achieving competitive common-mode rejection and power supply rejection ratios of > 70 dB. The NEF of the full proposed design is 1.8 in AP mode and 3.07 in LFP mode. Figure 6.6 provides a die photo of the design.

6.6 Conclusion

In this chapter, a power efficient analog front-end scheme using a parametric amplification is introduced. The noise aliasing induced by the sampling operation is avoided by using the inherent large source impedance of a microelectrode. The proposed scheme achieved the lowest NEF of 1.8 in the neural recording applications.

CHAPTER 7

Conclusions and Future Directions

7.1 Summary of Contributions

There are many benefits that can be obtained by implanting a millimeter scale computing platforms. First, it reduces the risk of human implantation drastically. The implantation can be simply done with a syringe rather than surgical operation. As the surface area decreases, long-term sustainability of the system improves drastically. Second, the application space for environmental monitoring sensor nodes, such as temperature, pressure and acceleration sensors expands much more widely as a result of the miniaturized system size.

The major challenges to realizing such a small system result from the limited battery capacity. Compared to Alkaline AA battery, the capacity shrunk by a factor of million. Therefore, the design circuit regime should be moved from milliwatt to nanowatt level. In addition, the die size needs to be small enough for the mm-scale integration while the use of off-chip components is highly limited.

In Chapter 3 of this dissertation, a wake-up timer that consumes 4.7nW and exhibits 13.8 ppm/℃ temperature coefficient was introduced. The ultra-low power consumption is highly advantageous in reducing the system sleep power because the wake-up timer is the key always on block that dominates the total sleep power consumption. In addition, the reported temperature

coefficient of 13.8 ppm/°C is the lowest among RC oscillators, and it drastically improves energy overhead for the synchronization with peers.

The 2.5ps_{rms} digital-PLL presented in Chapter 4 improves the system stability by reducing the variation of the loop bandwidth using a nested FLL. Furthermore, a noise detection scheme using the statistical behavior of BBPFD was proposed to maintain constant output noise performance under the change of environment such as temperature. Consequently, the power overhead is minimized with the given noise specification.

In Chapter 5, a 2.7cm^3 GNSS logger was proposed. It includes a die-stacked sensor platform composed of ARM cortex M0 processor, sensor, radio, solar cell, decoupling capacitor and harvester layers. The proposed system can acquire up to 1791 fixes using a miniaturized antenna with the radiation efficiency of 20.66%.

Finally, Chapter 6 of this dissertation covered a power efficient front-end scheme using parametric amplification. Sensor interface circuits, which interacts with pressure, humidity, acceleration and bio-medical signals are required to exhibit appropriate input referred noise so it can monitor the signals with sufficient accuracy. At the same time, the power consumption of the interface needs to be as low as possible due to the highly constrained power budget incurred by the system form factor. Therefore power efficiency of the front-end amplifiers is highly emphasized. This work proposes an analog-front-end scheme using a parametric amplification for neural recording applications. The proposed work showed input referred noise of 2.1 μV and 3.5 μV for action potential bandwidth and local field potential bandwidth, respectively.

7.2 Future Directions

The presented wake-up timer uses only a single pair of supply voltages without requiring any external references or trimmings, which makes it readily applicable to a sensor node system.

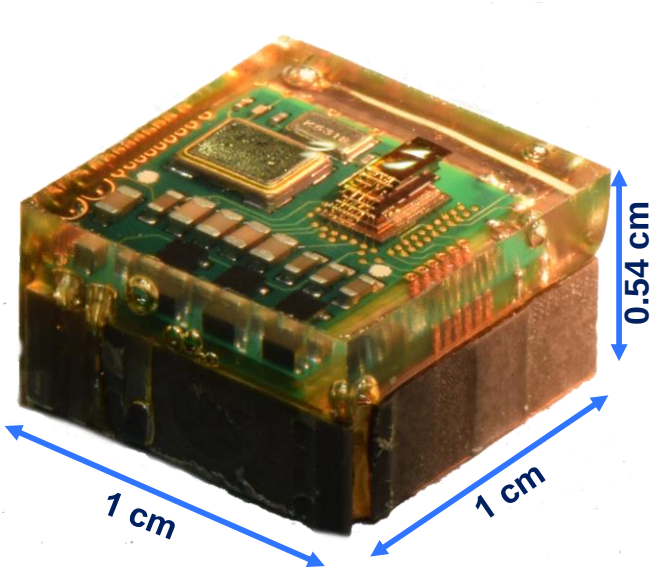


Figure 7.1 A GNSS receiver implemented by integrating all the building blocks in a die-stacked platform except for crystals and power regulators.

Therefore, implementation of a sensor node system that benefits from its ultra-low power consumption and accuracy can be the next step of this work.

The proposed noise detection scheme using statistical behavior of the BBPFD occupies small area and consumes negligible power consumption. However, it takes more than 5ms to construct a fine representation of the output noise distribution which can be an issue for applications requiring fast locking time. Instead, a noise detection scheme using a time-to-digital converter (TDC) can be studied as an attempt to improve the noise locking time. In addition, the presented FLL-based DCO has a highly linear frequency turning curve. This characteristic can be exploited to instantly lock the output frequency with a change of the frequency multiplication ratio.

The GNSS logger system presented in Chapter 5 adopted an off-the-shelf RF-front end and a flash memory. By integrating those circuits to the die-stacked sensor platform, the system size can be further miniaturized as shown in Figure 7.1.

Lastly, this dissertation presented a neural recording amplifier using parametric amplification. The sampling noise during the parametric amplification phase was avoided by exploiting the large impedance of the microelectrode. This concept needs to be verified using a practical microelectrode. Furthermore, a multichannel neural recording system using this parametric amplification can be implemented to validate the practicality of the circuit.

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