An Isolated High-Voltage High-Frequency Pulsed Power Converter for Plasma Generation

by

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ABSTRACT

This thesis reviews plasma technology, pulsed power technology, basic structures of pulsed power generator and semiconductor devices. Based on above, an isolated high voltage pulsed power converter with high repetitive frequency for low power level application such as ozone generation is proposed in this thesis. The hardware for proposed pulsed power converter is well set up. The output pulsed voltage can reach -12 kV with pulse frequency up to 15 kHz. The pulse interval is designed as 1.6 μs.

The proposed pulsed power converter system could be divided into two main parts, which are boost converter stage and a resonant stage. This thesis detailly introduces the structure and operating principles of the boost converter stage and the resonant stage. As for the boost converter stage, both analog control and digital control are applied to achieve the boost voltage function and power limiting function. As for the resonant stage, a pulse generating signal and spark protection function is achieved with a DSP control.

This thesis also detailly gives an analysis for parasitic parameters of the proposed pulsed power converter system. Parasitic capacitances of SiC MOSFETs will affect spike performance of the proposed pulsed power converter system. A mathematical model of describing a relationship between parasitic capacitances of SiC MOSFETs and the spike voltage of the proposed pulsed power converter is proposed in this thesis. A comparison test is conducted to prove the proposed analysis.

Chapter 1 Introduction

1.1 Review of plasma technology

What is plasma? Plasma is an ionized gas, one of the four fundamental states of matter, which was first discovered by chemist Irving Langmuir in the 1920s [1]. Like the other three fundamental states of matter, plasma could be collected by suppling enough energy to the matter.

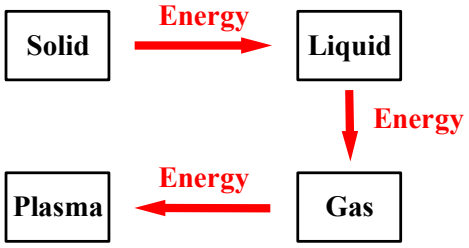

Figure 1. Generation of plasma

The plasma does not exist under normal condition on earth. But it does appear in our daily life. Neon signs and the lightings are all plasma phenomena [2].

The artificial plasma is usually generated by external electric field with neutral gas. The function block is illustrated as Fig. 2.

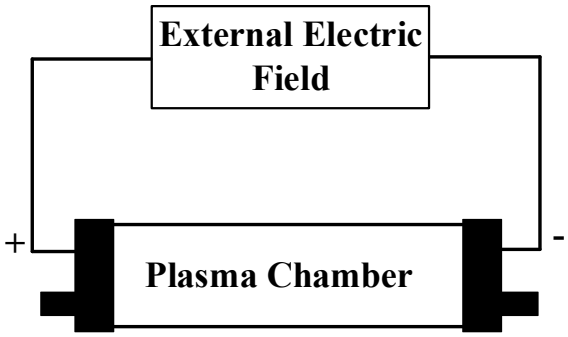

Figure 2. Artificial plasma generation by external electric field with neutral gas

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These chapters are part of my published work with title of "An Isolated High-Voltage High-Frequency Pulsed Power Converter for Non-Thermal Plasma Ozone Generation"

Due to the specification of high temperature, plasma arose attention in past a few decades. Plasma technology were widely used in different industrial fields. Gas treatment using plasma systems is detailly introduced in [3]. [4] lists plasma technology's effect on field of material surface treatment. Cymer Inc ever utilized plasma technology to create specific wavelength light for photolithography field [5]. The plasma technology is also used in broad areas such as water treatment, pollution treatment, biomedical treatment [6]- [8]. Besides above, ozone generation system also utilizes technology of plasma system.

1.2 Review of pulsed power technology

Pulsed power technology accumulates power over a relative long time and releases with a tiny interval to generate pulses. Usually the energy is stored in electrostatic field as capacitors and magnetic field as inductors. Depending on different load requirements, the output voltage and output current employ kinds of amplitudes, durations and pulse frequencies.

Utilizing specification of releasing enormous energy within tiny interval, pulsed power technology is widely used to generate plasma.

1.3 Review of structure of pulsed power converter

There are different types of pulsed power converter were produced.

The Basic Marx Generator is firstly proposed by E. Marx in 1925 which is earlier than discovery of plasma. The structure of Basic Marx Generator is illustrated as Fig. 3.

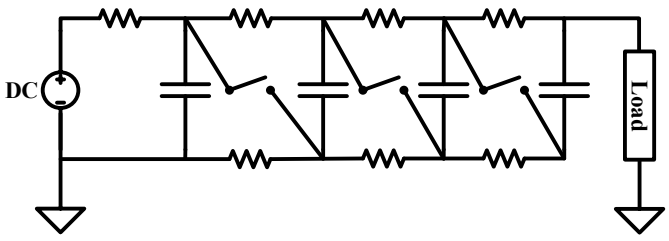


Figure 3. Structure of Basic Marx Generator

The electrostatic field as the capacitors are used to store energy. When the capacitors are all fully charged, the switch in the Fig. 3 will be closed. The terminal of load will form an enormous voltage. With increase of number of paralleled capacitor, the voltage across terminal will hit over 10 MV. The short coming of Marx Generator is relative long pulse duration.

With time goes on, the Marx Generator expands its topology as Solid-state Marx Generator, Inversion Generator, Stacked Blumlein Generator and PFN Marx Generator. [9]- [12] detailly introduce each topology respectively.

Different with Marx Generator using capacitors to store energy, Inductive Adder topology utilizes inductor to store energy. A transformer is used to combine several stages and form pulse power across the load. Detailed design and analysis of inductive adder topology is introduced in [13]. Fig. 4 gives a structure of Inductive Adder topology.

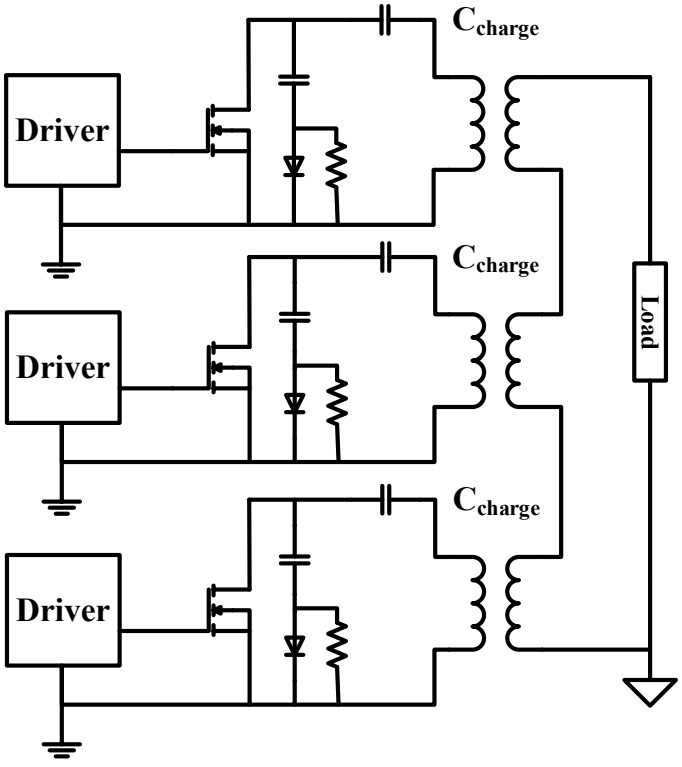


Figure 4. Structure of Inductive Adder topology

Apart from Marx Generator and Inductive Adder topology, Magnetic Pulse Compression technology is also often used to generate pulse power. Different with Marx Generator and Inductive Adder topology, magnetic pulse compression technology utilizes magnetic switch technology to compress the duration of pulse, which makes interval of pulse could be within nano-seconds level. [15]- [18] detailly introduce and analyze magnetic switch technology and Magnetic Pulse Compression technology. Fig. 5 shows structure of Magnetic Pulse Compression topology.

With development of plasma technology, pulsed power generators are taking much more important role than ever in industrial fields.

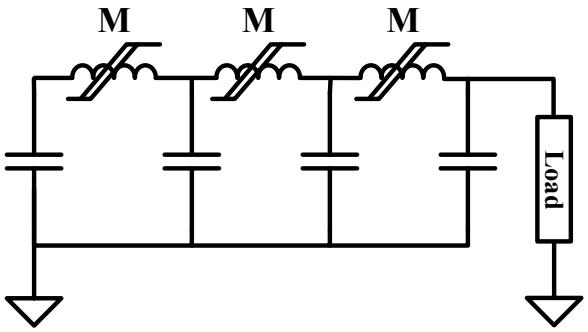


Figure 5. Structure of magnetic pulse compression

1.4 Review of semiconductor devices

All above mentioned topologies get involved with switch control. Semiconductor devices are widely used in power conversion and power control.

The basic concept of semiconductors is utilizing PN junction to achieve controlling power [18]. Structure of PN junction is showed in Fig. 6.

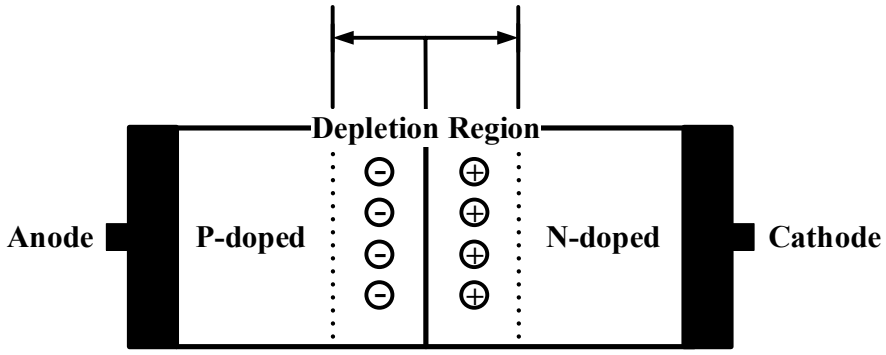


Figure 6. Structure of PN junction

Artificially increase the number of holes or electrons to silicon is called doping. Doped silicon material with more holes is called p-type material. Doped silicon material with more electrons is called n-type material. With doping action, connect p-type material and n-type material, a PN junction will form.

PN junction has specification of unilateral conductivity. The current could flow through PN junction only at the moment of PN junction's forward biased. Due to this specification, a lot of semiconductor devices were produced.

By control's capability difference, semiconductor devices could be roughly divided by uncontrolled semiconductor devices, half-controlled semiconductor devices and fully-controlled semiconductor devices.

The uncontrolled semiconductor devices generally refer to diodes. The diodes are constructed by a simple PN junction, which is introduced in 1900s [19]. Diodes could not be controlled to turn-on or turn-off. As long as PN junction is forward biased, current can flow through diode from anode terminal to cathode terminal. The diode will turn-off when PN junction is reverse biased.

Thyristors is most the common half-controlled semiconductor devices. The thyristors are combined from two transistors. It could be controlled to turn-on, letting current flow through.

However, it could not be controlled to turn-off manually. The tunnel would close only at the moment current flowing through thyristor drops to a threshold value.

Compared with uncontrolled semiconductor devices and half-controlled semiconductor devices, fully-controlled semiconductor devices have abundant different type devices and more complicated structure. Gate-turn-off Thyristors (GTO) are introduced in 1958, Power MOSFETs and insulted gate bipolar transistors (IGBT) are introduced in 1975 and 1985 respectively [20]. Fully-controlled semiconductor devices could be controlled to both turn-on and turn-off.

Power MOSFETs and IGBTs are mostly used in recent industrial fields. The Power MOSFETs are mainly subjected to handle high switching frequency projects and IGBTs are used for high voltage high power applications.

With occurrence of wide-bandgap material, SiC MOSFETs are also widely used for high voltage high power application recent years.

1.5 Proposed topology of pulsed power converter

Topologies mentioned above are mainly applied on high power level applications such as Electrothermal Chemical (ETC) guns [21]. An isolated high voltage pulsed power generator with high repetitive frequency for low power level application such as ozone generation is proposed in this thesis.

The proposed pulsed power generator could be roughly divided by two main parts. The first part is boost converter stage part. This part boosts voltage from low input voltage level to 500 volts. Besides, the boost circuit will sample input current to achieve power limiting function. The second part of whole system is resonant stage, which is the critical part of proposed pulsed power generator system. This part utilizes specification of resonant technology to form a pulse across the

chamber load. The resonant stage also has function of load spark protection, which is very important for plasma application.

The structure of proposed high voltage high frequency pulsed power generator for low power level application such as ozone generation is showed in Fig. 7.

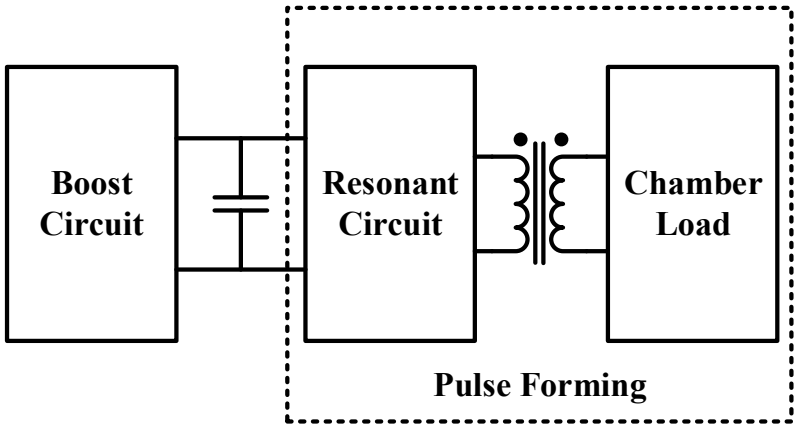


Figure 7. Proposed high voltage high frequency pulsed power generator for low power level application such as ozone generation

The proposed pulsed power generator is designed to form pulse with output reaching -12 kV. The duration of pulse is 1.6 us and frequency of pulse is 15 kHz. The input voltage of pulsed power converter is varying from 300 V to 380 V. The power rating is designed as 320 W.

The specification of proposed pulsed power converter is listed in Table I.

Table I Specification of proposed pulsed power converter

Input voltage	300 – 380 V
Output voltage	-12 kV
Rated power	320 W
Pulse frequency	15 kHz
Pulse duration	1.6 us

1.6 Organization of thesis

The rest of the thesis is organized as follows: Chapter 2 will detailly introduce boost stage's design which includes introduction of operation principle of boost stage and control mode, power limiting function on boost stage, functions implementation by either analog and digital methods and

hardware selection for boost stage circuit. Chapter 3 will review resonant circuit theory, detailly introduce and analyze operating principle of resonant stage. In this chapter, snubber design, driver circuit design and protection circuit design will be covered. Hardware selection of resonant stage will conclude this chapter. Chapter 4 will introduce parasitic capacitances of SiC MOSFETs and analyze impact of parasitic capacitance on proposed pulsed power generation. A mathematical model and simulation model will be generated in this chapter. Chapter 5 will cover hardware verification test of proposed pulsed power converter and comparison verification test for proposed theory of parasitic capacitances and spike voltage. Chapter 6 will conclude this thesis and list future work concerning about pulsed power converter project.

Chapter 2 Boost converter design with current limiting function

2.1 Introduction of boost converter

DC to DC converter is the circuit transferring direct current from a voltage level to another voltage level. Boost converter, as one type of DC to DC converter, is used to produce higher voltage at the load than the input voltage [22].

Due to the specification of stepping-up output voltage, boost converter is widely used in industrial fields. [23] and [24] introduce boost converter on fuel cell vehicle application and electric vehicle application. Besides, boost converter is also widely used for Power Factor Correction circuit to promote power factor performance of power supply.

The basic structure of boost converter is simple, combined with input inductor, diode, output capacitor and semiconductor switch device as Fig. 8.

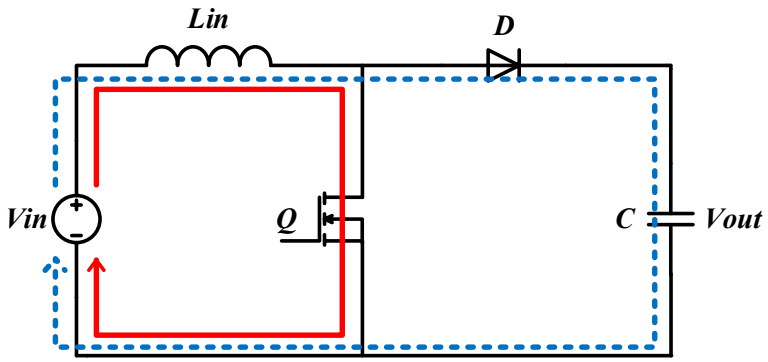


Figure 8. Structure of boost converter

The operating conditions of boost converter could be divided by two states, which are semiconductor switch on-state and semiconductor switch off-state.

As semiconductor switch is in on-state, equivalent circuit is illustrated in Fig. 9.

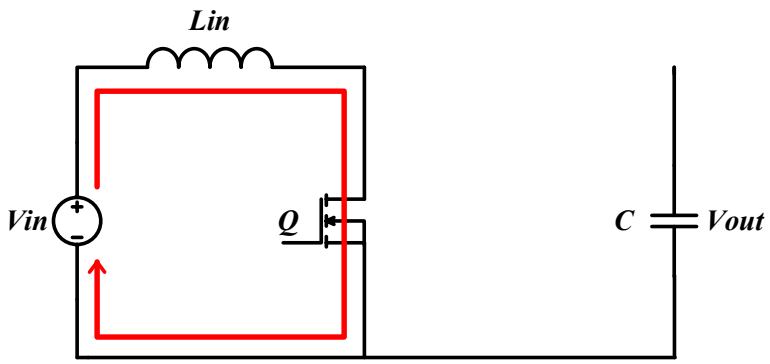


Figure 9. Equivalent circuit of boost converter as semiconductor switch is in on-state

DC power supply on input side begins to charge input inductor along red line highlighted in Fig. 9 during time interval T_{on}.

As semiconductor switch is in off-state, equivalent circuit is illustrated in Fig. 10.

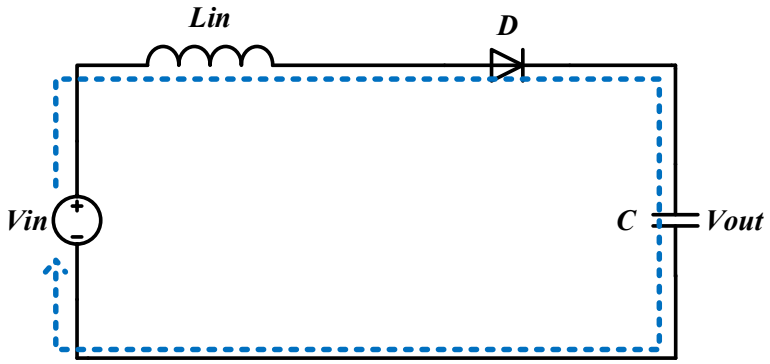


Figure 10. Equivalent circuit of boost converter as semiconductor switch is in off-state

During the time interval T_{off}, input inductor releases power, ever stored in T_{on}, to output capacitor. For such system, as it works in steady-state, energy stored in input inductor during T_{on} equals to energy released to output capacitor during T_{off}. We assume input voltage as V_{in} and output voltage on load as V_{out}.

Thus, we have:

$$Vin \cdot Ton = (Vout - Vin) \cdot Toff \quad (1)$$

Then we can get formula for output voltage with respect to input voltage and duty cycle α.

$$Vout = Vin \cdot \frac{(Ton + Toff)}{Toff} = Vin \cdot \frac{1}{1-\alpha} \quad (2)$$

Where

$$\alpha = \frac{Ton}{Ton + Toff}$$

2.2 Introduction of control mode of boost converter

For the most of power supplies, closed loop feedback system is introduced to provide with stable power under different load conditions [25]. There are two main methods for closed loop feedback controls, which are voltage mode control and current mode control.

The voltage mode control only feeds back the voltage on the output side to gate control system, which is straightforward for designing feedback loop but with slow response.

The current mode control feeds back both output voltage and inductor current to gate control system. A double loop, which are inner current loop and outer voltage loop, is used to achieve current mode control, which is complicated but with faster response performance.

[26] detailly introduces both voltage mode control and current mode control.

Compared with voltage mode control, current mode control gets advantages as:

- Current mode control could provide with faster response for converter. There is no delay issue as it happened in voltage mode control.
- Current mode control could sense either output voltage or input inductor current, which is necessary for limiting current application.

Current mode control could also be divided as:

- Peak current mode control
- Valley current mode control
- Average current mode control

- Sample-and-Hold current mode control

Among different current mode controls above, peak current mode control and average current mode control are more popular in designing boost converter [27].

One big advantage of current mode control, comparing with voltage mode control, is pulse by pulse current limiting function.

Current limiting function is critical in circuit protection. As for proposed pulsed power converter, the load is the chamber with blowing air flow. With variance of voltage across chamber, the characteristic of load would change a lot. Also, different circumstance temperatures and humidity would change characteristics of load, which requires current limiting function on boost converter stage to protect whole power system.

2.3 Boost converter design with analog control system

Boost converter in proposed pulsed power converter system is designed with:

- Input voltage: 300 V-380 V
- Output voltage: 500 V
- Switching frequency: 45 kHz
- Power rating: 320 W

The inductor of boost converter is used to store energy. The size of inductor is proportional to product of inductance and square value of ripple current flowing through the input inductor. Thus, in order to save size of inductor, one optimal way is to increase switching frequency of boost converter. However, with increase of switching frequency of boost converter, switching loss on MOSFETs of boost converter will increase either. Thus, this thesis made a trade of power density and efficiency, selecting 45 kHz as switching frequency for boost converter.

The boost converter's control system is implemented by analog chip UC2844. As contents mentioned above in section "Introduction of control mode of boost converter", to implement power limiting function, current mode PWM controller is necessary.

UC2844 can operate with Pulse-by-Pulse current limiting function under as high as 500 kHz for boost converter [28], which is a good candidate for proposed power system. Function diagram of UC2844 is showed in Fig. 11 [28].

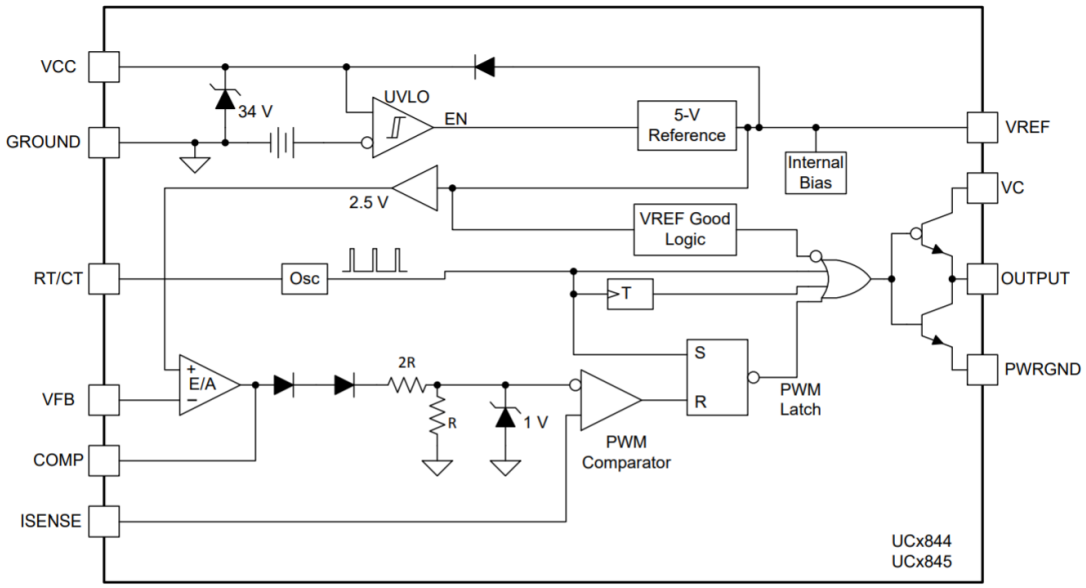


Figure 11. Function diagram of UC2844 [28]

Based on designing specification, switching frequency is set as 45 kHz. From datasheet of UC2844, oscillator frequency f_{osc} is set by resistor R_{RT} and capacitor C_{CT}.

$$fosc = \frac{1.72}{R_{RT} \times C_{CT}} \tag{3}$$

Switching frequency is one half of oscillator frequency, with function (3), setting R_{RT} as 5 kΩ, we can calculate C_{CT} is 3.8 nF.

A simulation model based on PSIM platform for UC2844 controlling proposed boost converter is set up and showed in Fig. 12.

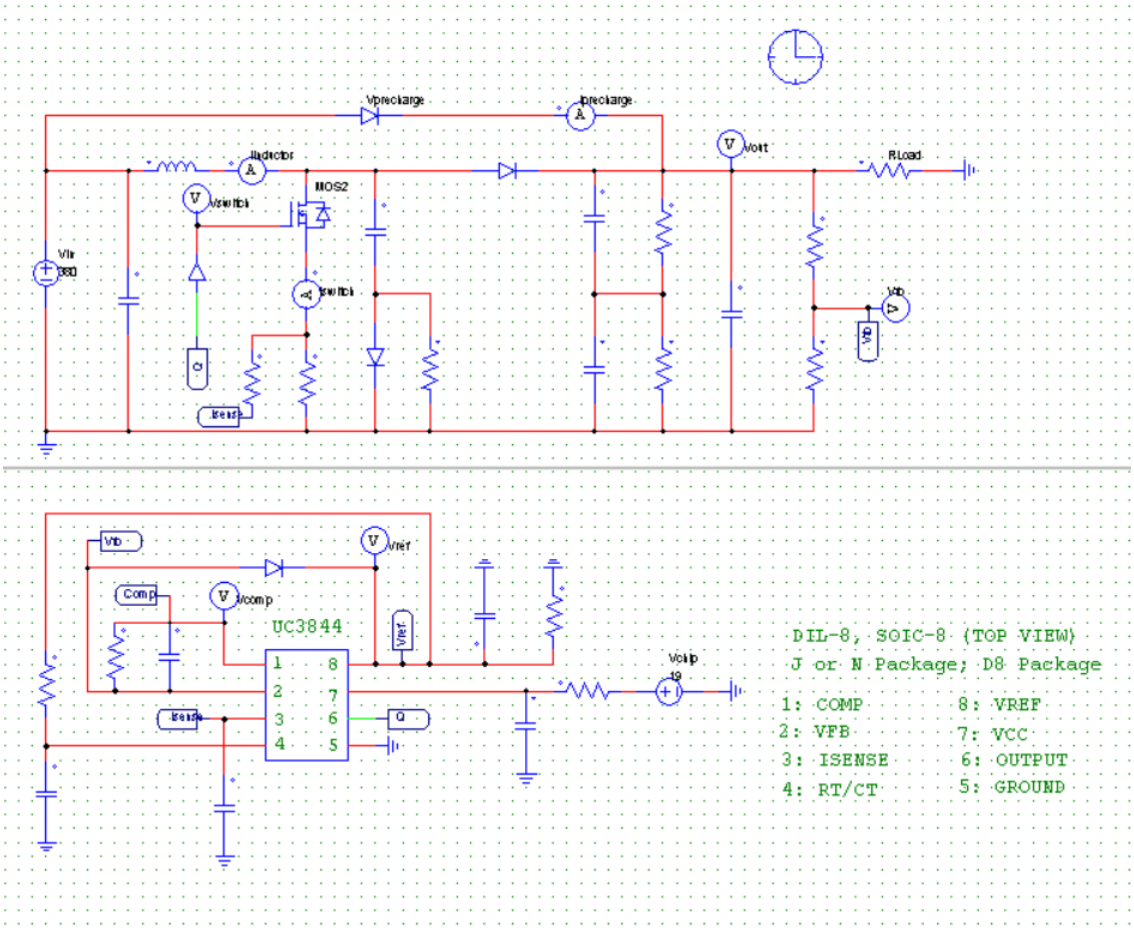


Figure 12. Boost converter controlled by UC2844

2.4 Boost converter design with digital control system

With same specification of designing boost converter. A digital control system is generated which is planning to be achieved by DSP TMS320F28335.

In order to achieve power limiting function with boost converter, inner current loop in design is critical. A digital control model is set up and simulated by PSIM showed in Fig. 13.

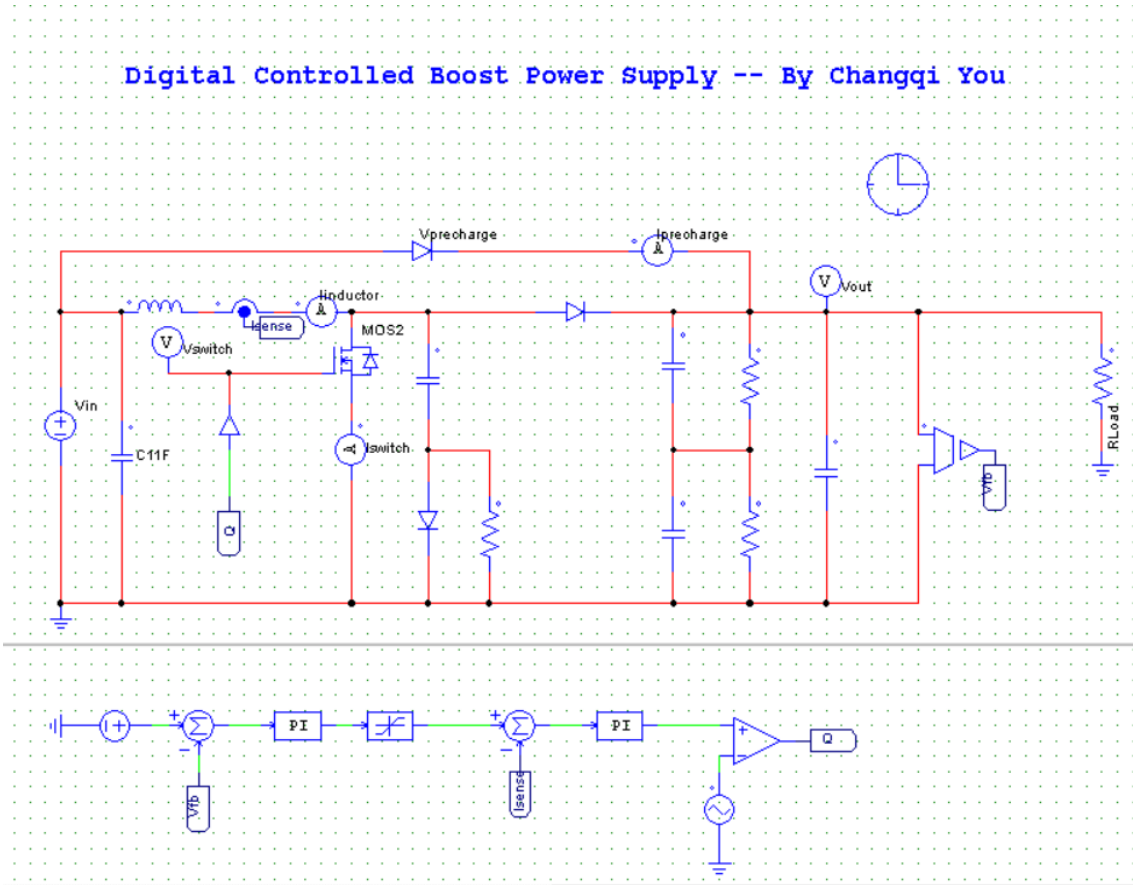


Figure 13 Boost converter with digital control system

An inner current loop and outer voltage loop is well placed in design as showed in Fig. 13. Feedback voltage comes from output load will be made a difference calculation with reference voltage. The difference will go through PI control, forming reference current for feedback input current.

Simulation result of output voltage and input inductor current is showed in Fig. 14.

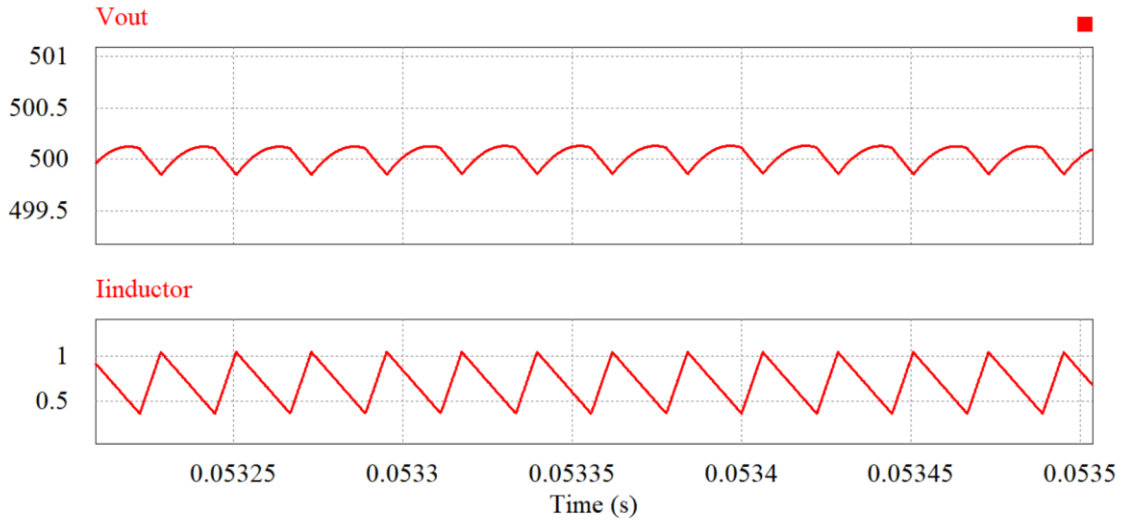


Figure 14. Simulation result of output voltage and input inductor current

Based on design, the maximum average current is set as 0.8 A. A simulation of variance of load is made to test current limiting function. The simulation result is showed in Fig. 15.

As showed in Fig. 15, at t=0.1 s. The load increase, which requires more power from boost converter. With current limiting function, boost converter will limit average input current as set value and pull-down output voltage to protect whole power system.

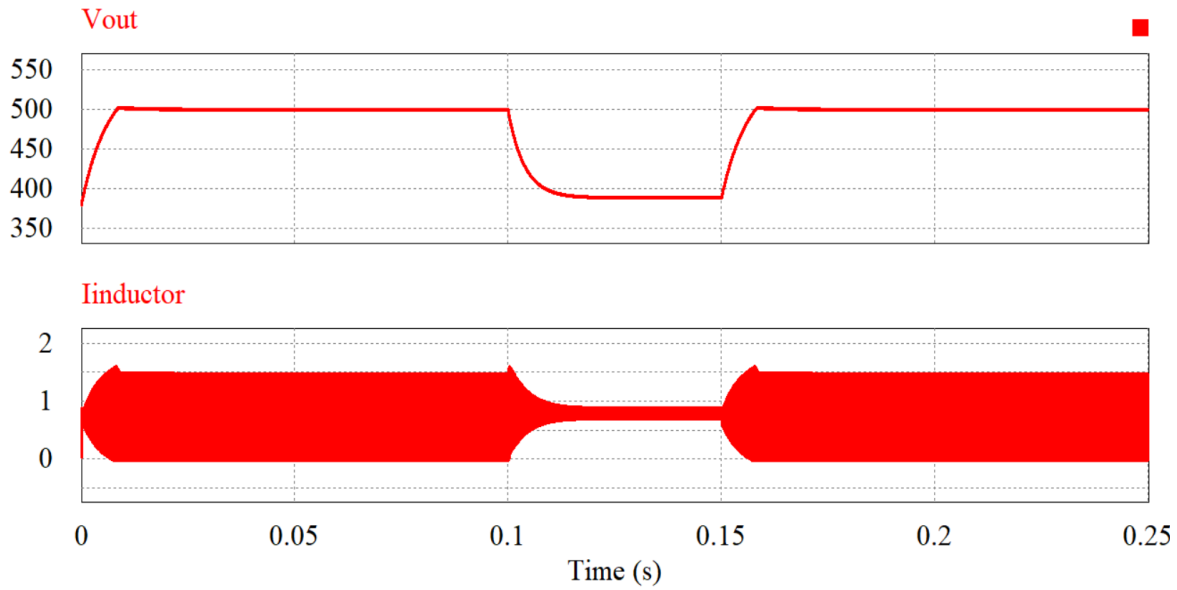


Figure 15. Simulation result for current limiting function

2.5 Power stage hardware selection of boost converter

There are three current modes for input inductor current of boost converter, which are:

- Continuous Conduction Mode (CCM)
- Discontinuous Conduction Mode (DCM)
- Critical Conduction Mode（CrCM）

Compared with discontinuous conduction mode and critical conduction mode, continuous conduction mode could provide with minimum peak current, which is good for preventing magnetic saturation for input inductor.

Assume input inductor current ripple as I_r, duty ratio as α, switching frequency as f, then:

$$Ir=\frac{Vin\cdot\alpha}{Lin\cdot f} \tag{4}$$

If let boost converter functions as critical conduction mode, then average input inductor current Iin is equals to:

$$Iin=\frac{Pout}{Vout\cdot(1-\alpha)}=\frac{1}{2}\times\frac{Vin\cdot\alpha}{Lin\cdot f} \tag{5}$$

With formula (4) and (5), we can get value of input inductor making boost converter functions under critical conduction mode as:

$$Lin=\frac{Vin\cdot Vout\cdot\alpha\cdot(1-\alpha)}{2\times f\cdot Pout} \tag{6}$$

Based on formula (6), we can get, as L_{in} equals to 1.6 mH, when V_{in} is 300 V and P_{out} is 250 W. As long as the value of L_{in} is selected larger than 1.6 mH under same condition, the boost converter will function under continuous conduction mode.

A simulation is made with different value for input inductor to observe different current conduction mode.

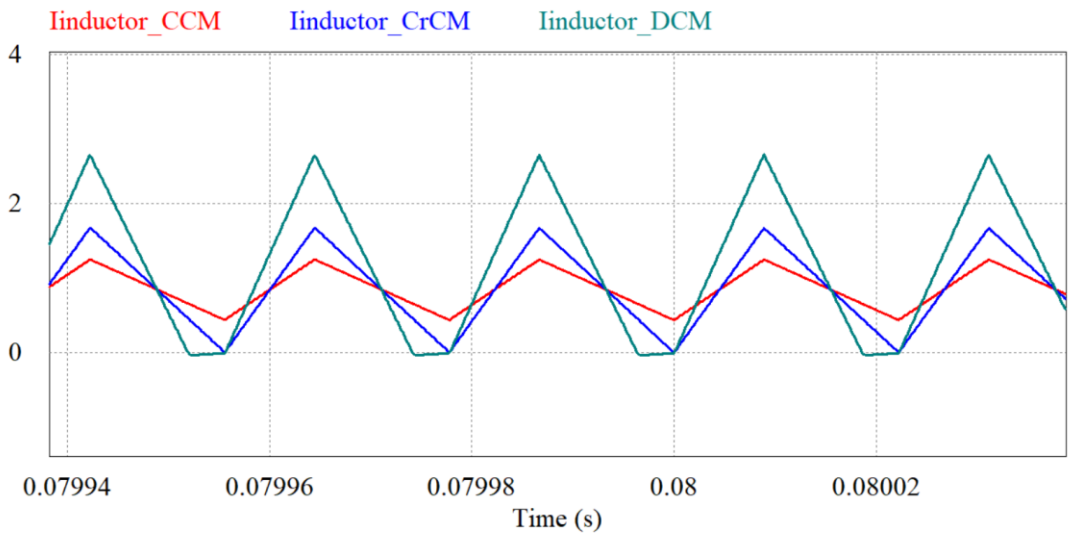


Figure 16. Simulation result for different current conduction mode

To maintain boost converter functions as continuous conduction mode, this thesis chooses input inductor as 3.3 mH. 1140-332K-RC from Bourns is selected.

IRFBF30 is selected as semiconductor switch device.

Two capacitors series connected is used for output capacitor, UCA2G220MHD from Nichicon is selected.

Chapter 3 Resonant stage design

3.1 Resonant circuit introduction

Resonant circuit, is also called as LC circuit. As the name says, it always contains at least one inductor and one capacitor in the circuit.

A resonant tank is showed in Fig. 17.

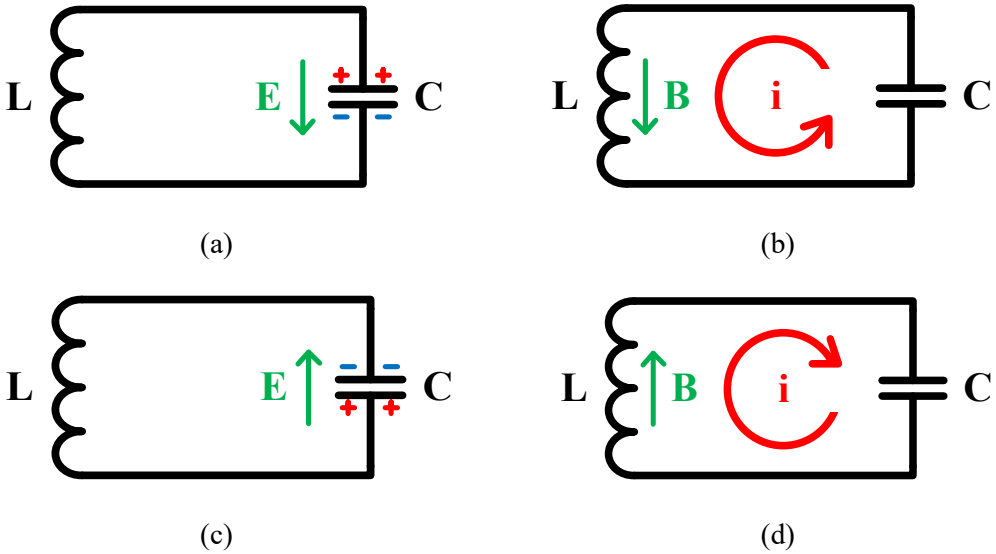


Figure 17 LC circuit analysis

(a) Capacitor store energy as electric field (b) Capacitor charges inductor, energy stored in inductor as magnetic field (c) Inductor charges capacitor, electric field reverse direction (d) Capacitor charges inductor, magnetic field reverse direction

As illustrated in Fig. 17, at first moment, capacitor has an initial voltage, which reflected as electric field. Then the capacitor and inductor will self-resonant and take care of storing energy one after another. The energy will be reflected as electric field and magnetic field by turns. The resonant tank will resonant at natural resonant frequency ω.

Where ω equals to:

$$\omega = \frac{1}{\sqrt{L \cdot C}} \tag{7}$$

3.2 Resonant stage design and analysis

The proposed pulsed power generator system consists of a resonant stage, which is critical to generate pulses. Fig. 18 shows structure of resonant stage of pulsed power generator system which is controlled by DSP.

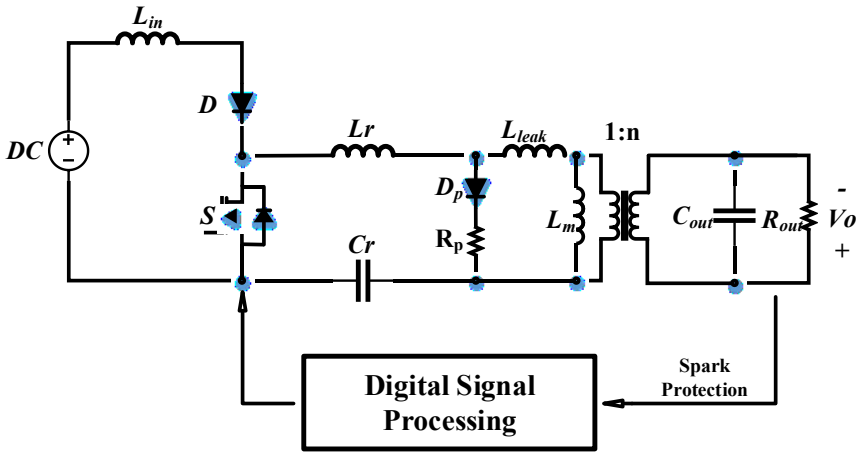
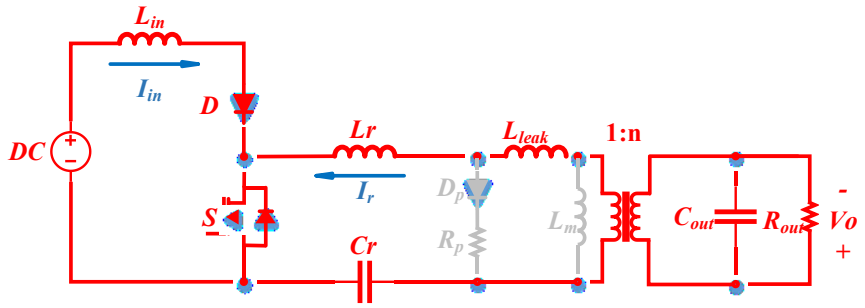


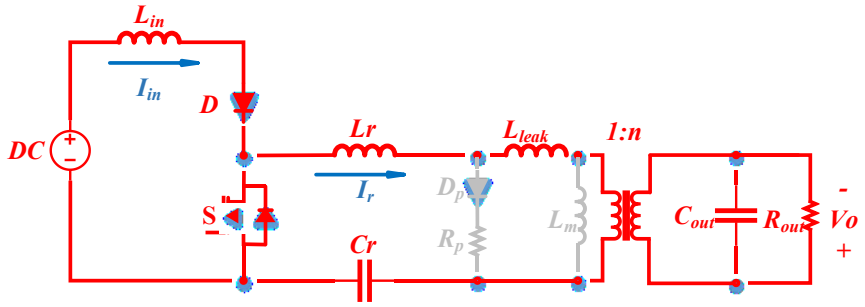
Figure 18. Structure of resonant stage of pulsed power generator system

The resonant stage is designed to convert DC to high frequency high voltage pulsed power. The pulse frequency range is 500 Hz to 15 kHz. The input DC voltage is 500 V and the output pulsed voltage is rated at -12 kV. Pulse duration is 1.6 μs.

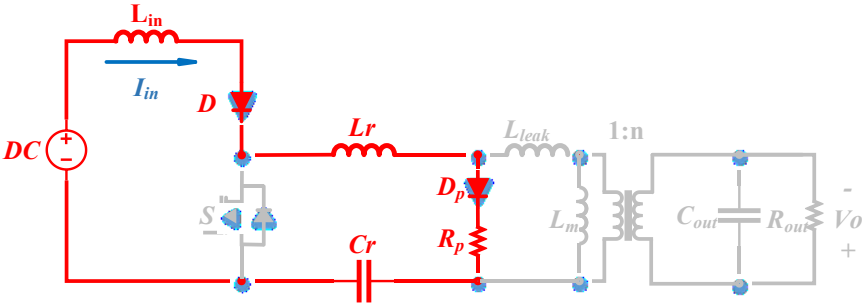
The operation of the resonant stage is composed of 4 modes as shown in Fig. 19 (a) to (d). Fig. 20 is the corresponding waveforms of the input current, resonant inductor current, resonant capacitor voltage and the output pulsed voltage.



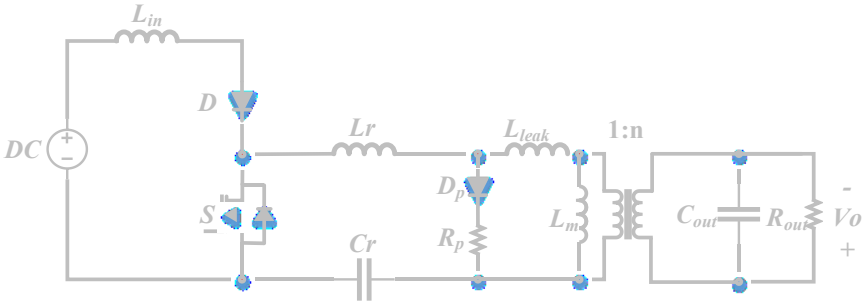
(a)



(b)



(c)



(d)

Figure 19. (a)-(d). Equivalent circuits for converter operating mode 1-4

Mode 1:

In Mode 1 ($t0$-$t1$), switch S is on. It should be noted that the resonant capacitor C_r has already been charged to its maximum value V_{cr_max} before S is on. At the moment when S is on, a resonant loop is formed which includes the resonant inductor L_r, transformer leakage inductance L_{leak}, resonant capacitor C_r, and the reflected capacitance from the load. The transformer magnetizing inductance L_m is large enough to be excluded from the resonance. The waveform of the inductor current through L_r is sinusoidal because of the resonance. The duration of Mode 1 is calculated in (8).

$$t_1\text{-}t_0=\pi\cdot\sqrt{(L_r+L_{leak})\left(\frac{C_r\cdot C_o\cdot n^2}{C_r+C_o\cdot n^2}\right)} \tag{8}$$

Mode 2:

In Mode 2 ($t1$-$t2$), the current through L_r is reversed and continues to flow through the body diode of the switch or the external anti-parallel diode. The resonant capacitor C_r finished discharging at the end of Mode 2.

The voltage equations for duration of mode1 and mode2 can be summarized as (9) to (11).

$$iL_r+\frac{VC_r}{R_o/n^2}=(-C_o\cdot n^2)\cdot\frac{dVtr}{dt} \tag{9}$$

$$VL_r+VL_{leak}=(L_r+L_{leak})\cdot\frac{diL_r}{dt} \tag{10}$$

$$iL_r=(-C_r)\cdot\frac{dVC_r}{dt} \tag{11}$$

Where V_{Lr}, V_{Lleak}, V_{Cr} and V_{tr} are the voltages across the resonant inductor, leakage inductor, resonant capacitor and the transformer primary winding. i_{Lr} is the resonant inductor current. With the maximum resonant capacitor voltage V_{Cr_max}, the resonant inductor current i_{Lr}, the transformer primary voltage V_{tr} and the output voltage V_o and can be approximately derived in (12) to (14) respectively.

$$\mathrm{iL_r} \approx \frac{\sqrt{C_o \cdot n^2 \cdot C_r \cdot (L_r + L_{leak}) \cdot (C_o \cdot n^2 + C_r)}}{L_r \cdot (C_o \cdot n^2 + C_r)} \cdot VC_{r\_max} \ sin\left(\frac{\pi}{t_1 - t_0} t\right) \tag{12}$$

$$Vtr \approx \frac{C_r}{C_o \cdot n^2 + C_r} \cdot VC_{r\_max} \cdot (cos(\frac{\pi}{t_1 - t_0} t) - 1) \tag{13}$$

$$Vo \approx n \cdot \frac{C_r}{C_o \cdot n^2 + C_r} \cdot VC_{r\_max} \cdot (cos(\frac{\pi}{t_1 - t_0} t) - 1) \tag{14}$$

Mode 3:

In Mode 3 ($t2$-$t3$), the voltage across the resonant capacitor C_r reaches its minimum value V_{Cr_min}. Switch S is off. The DC source charges the resonant capacitor along the input inductor L_{in} and resonant inductor L_r. The transformer primary winding is shunted by the fast recovery diode D_p and ballast resistor R_p.

The duration of Mode 3 is calculated in (15).

$$t_3 - t_2 = \sqrt{(L_{in} + L_r) C_r} \cdot (\pi - \varphi) \tag{15}$$

Where φ equals to:

$$\varphi = arccos\left(\frac{(V_{DC} - VC_{r\_min}) \cdot \frac{\sqrt{(L_{in} + L_r) C_r}}{L_{in} + L_r}}{\sqrt{(V_{DC} - VC_{r\_min})^2 \cdot \frac{C_r}{L_{in} + L_r} + \frac{{V_{DC}}^2 \cdot (t_2 - t_0)^2}{{L_{in}}^2}}}\right)$$

The voltage equations can be summarized as (16) to (20).

$$V_{DC} - VL_{in} - VL_r - VR_p - VC_r = 0 \tag{16}$$

$$VL_{in} = L_{in} \cdot \frac{diL_{in}}{dt} \tag{17}$$

$$VL_r = L_r \cdot \frac{\mathrm{d}iL_{in}}{\mathrm{d}t} \tag{18}$$

$$VR_p = R_p \cdot iL_{in} \tag{19}$$

$$iL_{in} = C_r \cdot d\frac{VC_r}{\mathrm{d}t} \tag{20}$$

Where V_{DC}, V_{Lin} and V_{Rp} are the voltages across the DC source, input inductor and the ballast resistor. i_{Lin} is the resonant inductor current. With the minimum resonant capacitor voltage V_{cr_min}, the input charging current i_{Lin} and the resonant capacitor voltage V_{cr} can be derived in (21) and (22) respectively.

$$\mathrm{iL_{in}} \approx (V_{DC} - VC_{r\_}min) \cdot \frac{\sqrt{(L_{in}+L_r)\cdot C_r}}{L_{in}+L_r} \cdot \sin\left(\frac{1}{\sqrt{(L_{in}+L_r)\cdot C_r}} \cdot t\right) + \left(\frac{V_{DC}\cdot(t_2-t_0)}{L_{in}}\right) \cdot \cos\left(\frac{1}{\sqrt{(L_{in}+L_r)\cdot C_r}} \cdot t\right) \tag{21}$$

$$\mathrm{Vcr} \approx (VC_{r\_}min - V_{DC}) \cdot cos\left(\frac{1}{\sqrt{(L_{in}+L_r)\cdot C_r}} \cdot t\right) + V_{DC} + \left(\frac{V_{DC}\cdot(t_2-t_0)}{L_{in}}\right) \cdot \frac{\sqrt{(L_{in}+L_r)\cdot C_r}}{C_r} \cdot sin\left(\frac{1}{\sqrt{(L_{in}+L_r)\cdot C_r}} \cdot t\right) \tag{22}$$

The maximum resonant capacitor voltage is obtained by equating the input charging current i_{Lin} to 0 as (23):

$$\mathrm{VC_{r\_}max} = V_{DC} + \sqrt{\frac{{V_{DC}}^2\cdot(t_2-t_0)^2}{{L_{in}}^2} \cdot \frac{L_{in}+L_r}{C_r} + (VC_{r\_}min - V_{DC})^2} \tag{23}$$

Where V_{cr_min} is:

$$\mathrm{VC_{r\_}min} = \sqrt[2]{VC_{r\_}max^2 - \frac{2\cdot Pout}{f\_operation}}$$

f_operation varies from 500 Hz to 15kHz.

Mode 4:

In Mode 4 ($t3$-$t4$), switch S is off, there is no current flowing in the circuit. The voltage on the resonant capacitor remains at its maximum value V_{cr_max}. The requirement for the resonant period can be written as follows in respect to the pulse frequency range from 500 Hz to 15 kHz. The

minimum repetitive interval, which is 67 μs, should be longer than one operation period from $t0$ to $t3$, as shown in (24)

$$t_3\text{-}t_0=2\pi\sqrt{(L_r+L_{leak})\left(\frac{C_o\cdot n^2\cdot C_r}{C_o\cdot n^2+C_r}\right)}+\sqrt{(L_{in}+L_r)\cdot C_r}\cdot(\pi\text{-}\varphi)<67\ \mu s \tag{24}$$

Where φ equals to:

$$\varphi=arccos\left(\frac{(V_{DC}\text{-}VC_{r\_}min)\cdot\frac{\sqrt{(L_{in}+L_r)C_r}}{L_{in}+L_r}}{\sqrt{(V_{DC}\text{-}VC_{r\_}min)^2\cdot\frac{C_r}{L_{in}+L_r}+\frac{V_{DC}{}^2\cdot(t_2\text{-}t_0)^2}{L_{in}{}^2}}}\right)$$

Fig. 20 is the corresponding waveforms of the input current, resonant inductor current, resonant capacitor voltage and the output pulsed voltage from mode 1 to mode 4.

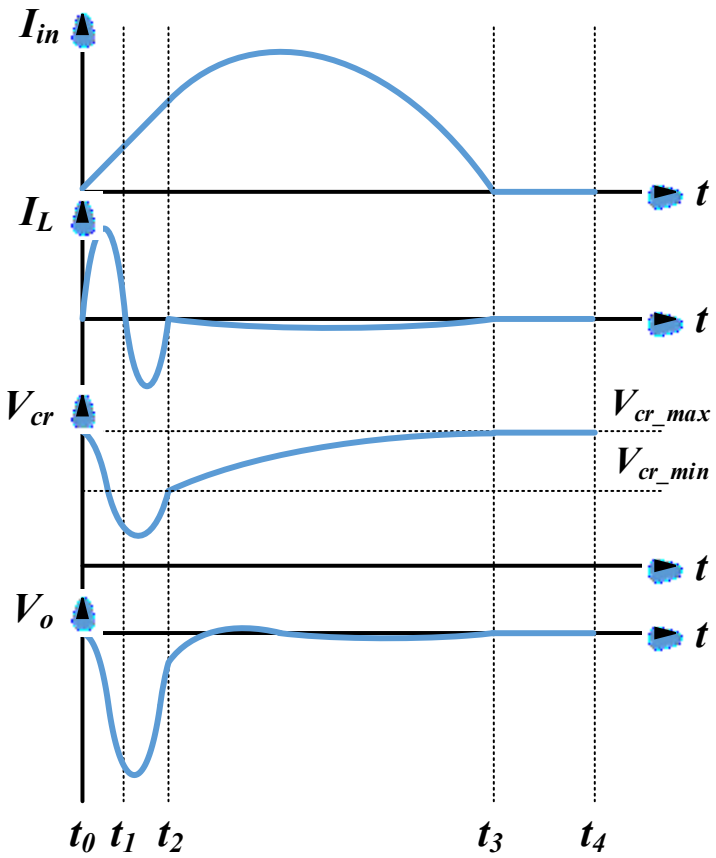


Figure 20. Principle operating waveforms.

3.3 Simulation of resonant stage

As showed in Fig. 21, a simulation model of resonant stage is set up.

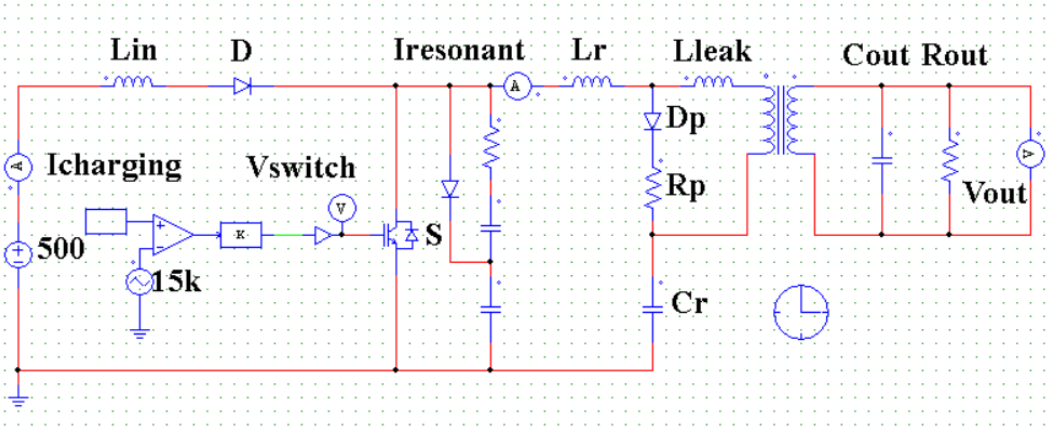


Figure 21. Simulation model of resonant stage

Simulation result of output pulse voltage, charging current, resonant current and switch voltage are showed in Fig. 22.

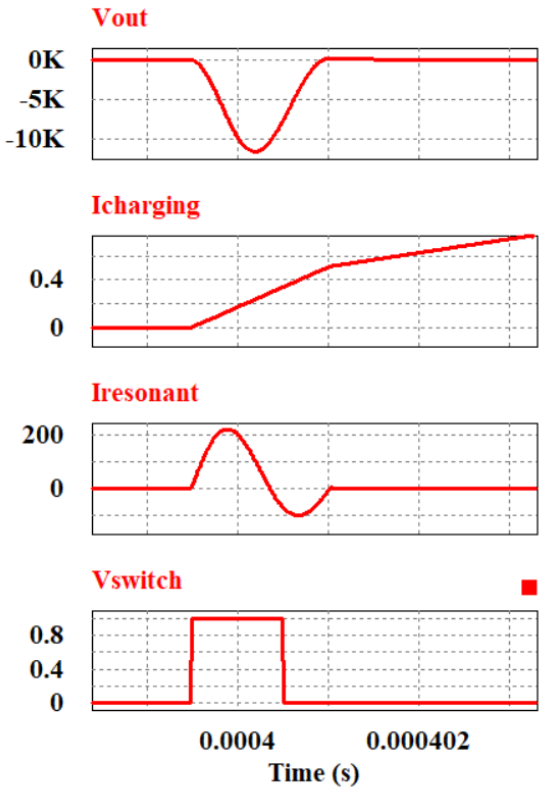


Figure 22. Simulation result of resonant stage

3.4 Protection circuit design

The load of proposed pulsed power generator system is a chamber with blowing air, which is not stable at some specific conditions. The spark will occur across chamber randomly. Thus, spark protection is necessary for power system.

When the spark occurs, the load gets short circuit. The equivalent capacitor and resistor of load will be bypassed. The voltage on resonant capacitor will reverse to a negative value. Based on this characteristic, a spark protection circuit is introduced.

Fig. 23 shows structure of spark protection circuit.

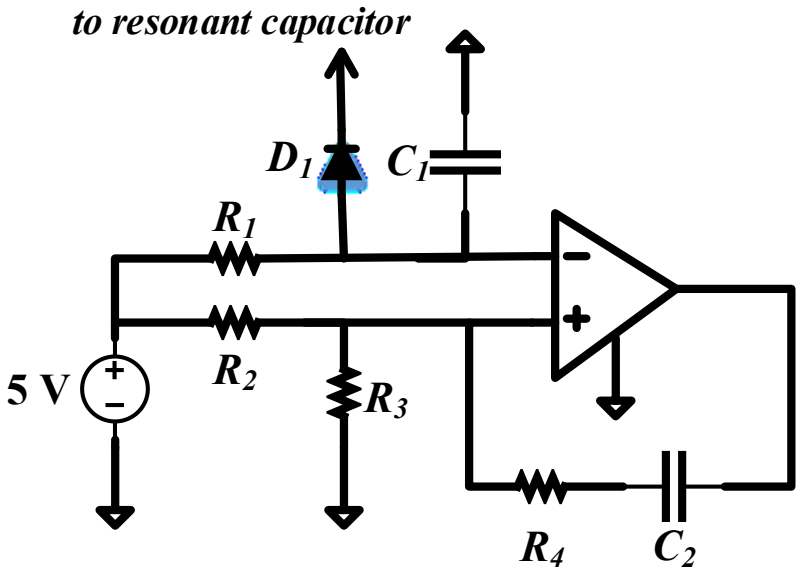


Figure 23. Structure of spark protection circuit

As illustrated in Fig. 23, an op-amp is utilized, functioning as a comparator, to achieve spark protection function. As a negative voltage occurs across resonant capacitor, energy stored in the capacitor C_1 of the protection circuit would be discharged. Thus, the voltage of the inverting terminal would decrease to 0 V, which is less than the voltage value of the noninverting terminal. The output of op-amp would be set to high. The protection circuit would be reset after spark. A simulation result in PSIM is showed in Fig. 24.

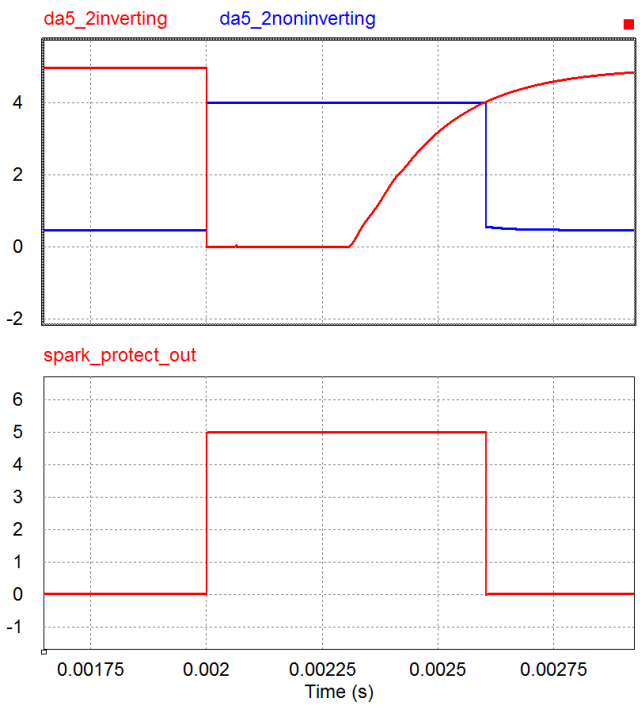


Figure 24. Simulation of spark protection circuit

As spark occurs, a pulse will be generated by spark protection circuit and be sent to DSP. The external interrupt of DSP will detect rising edge of input signal and stop ePWM function at once.

3.5 Power stage hardware selection of resonant stage

The transformer is the core part in this design for the sake of a stable and efficient operation. A ferrite toroidal core of 50 mm×30 mm×20 mm is selected. The primary has 6 turns. The number of turns for secondary winding is 108. The windings must be arranged in a way that the leakage inductance and stray capacitance are minimized in order to improve the high frequency response. the leakage inductance is 0.6 μH in this design. Progressive winding method has been used to reduce the stray capacitance. A transformer model developed in ANSYS/Maxwell, shown in Fig. 25, verifies the design. The total insulation thickness of fiber glass tape between the primary and secondary is 2.5 mm, with insulating ability up to 25 kV. The external surface is immersed with epoxy resin under vacuum environment.

The pulse duration is designed at 1.6 μs. Based on (19), resonant inductor's value is obtained by:

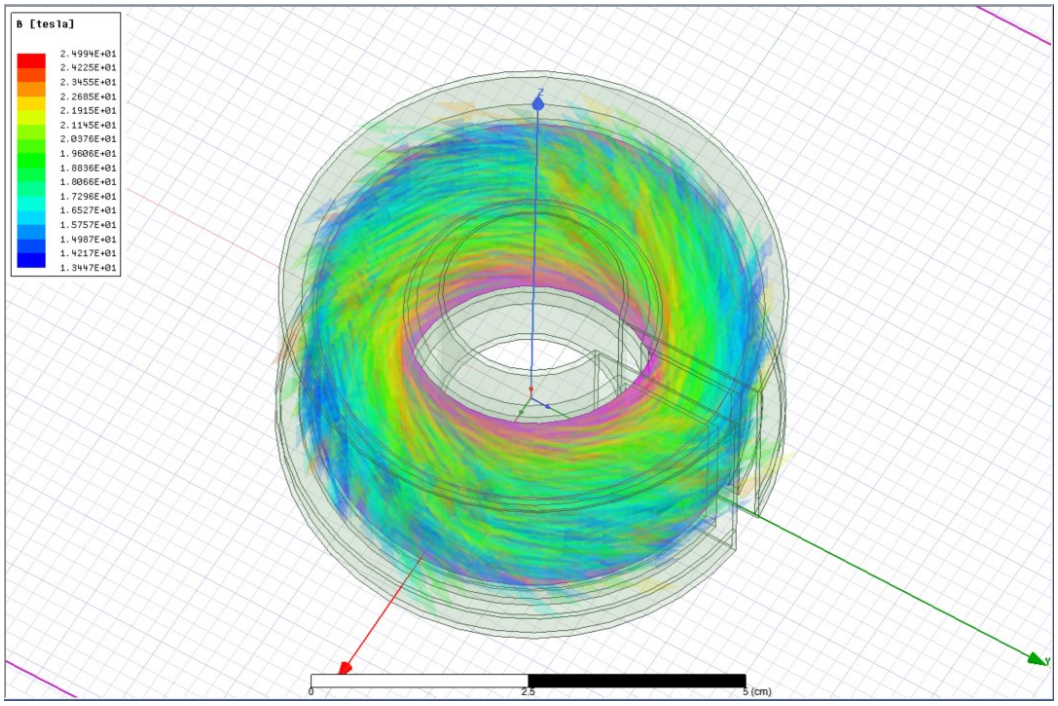


Figure 25. Transformer model in ANSYS/Maxwell

$$L_r = \frac{Pulse\ duration^2}{\left(\frac{C_r \cdot C_o \cdot n^2}{C_r + C_o \cdot n^2}\right) \cdot 4\pi^2} - L_{leak} = \frac{1.6\ \mu s^2}{\left(\frac{200\ nF \cdot 280\ pF \cdot 18^2}{200\ nF + 280\ pF \cdot 18^2}\right) \cdot 4\pi^2} - 0.6\ \mu H = 0.55\ \mu H \quad (25)$$

Both transformer and resonant inductor are customized.

AIRD-02-222K from Abracon LLC is selected as input charging inductor.

Two R76TN3100SE40K from KEMET parallel connected is selected as resonant capacitor.

Two SCT3040KL SiC MOSFETs from Rohm Semiconductor, parallel connected, is selected as semiconductor switch.

Chapter 4 Parasitic parameters of circuit analysis

4.1 Introduction of parasitic capacitances of SiC MOSFETs

Si-based MOSFETs (metal-oxide-semiconductor field-effect transistor) has been widely used for several years in a great number of fields. With applications varying, the requirements for MOSFETs have been much harsher, which leads the occurrence of wide-bandgap material based MOSFETs, such as SiC (silicon carbide) MOSFETs. Comparing with Si-based MOSFETs, SiC MOSFETs provide with higher voltage rating, making MOSFETs be an alternative for 1.2 kV application. Besides that, SiC MOSFETs own very high temperature handling capability and significantly reduced switching losses [29]- [31].

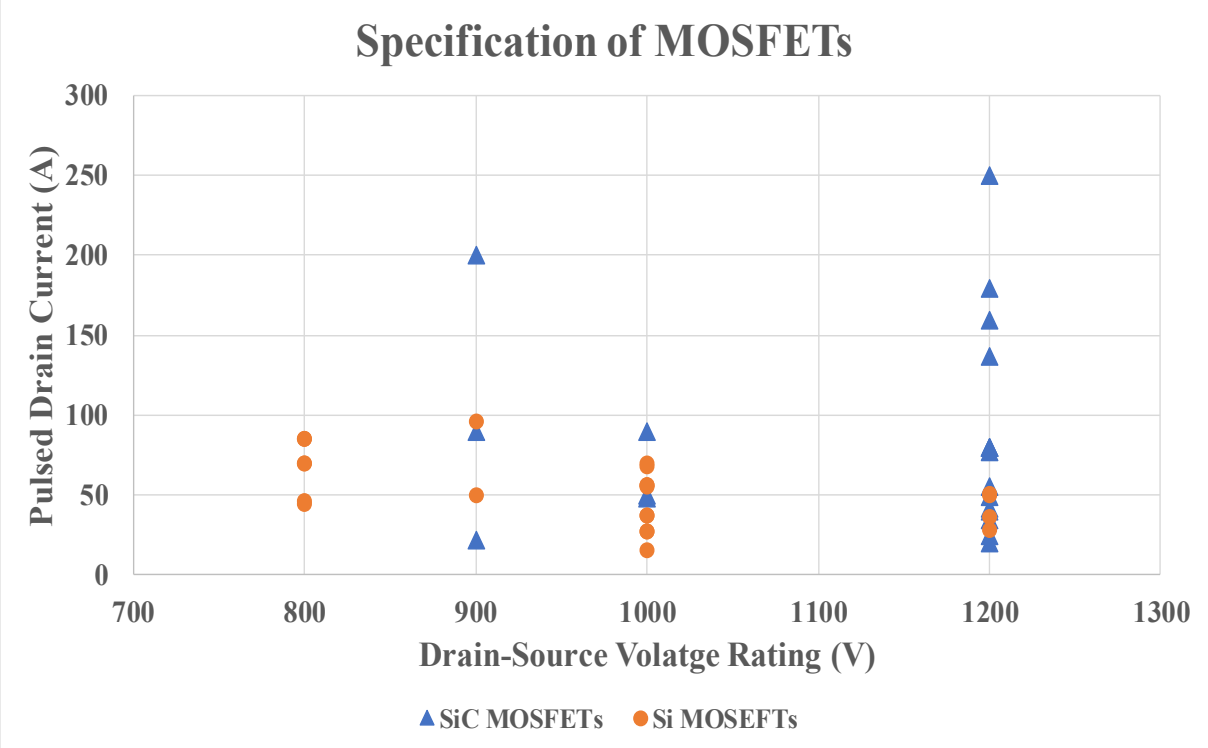


Figure 26. Comparison of SiC MOSFETs and Si-based MOSFETs on pulsed drain current

As for pulsed power converter system, compared with continuous drain current, non-repetitive pulsed drain current is more critical. Fig. 26 shows a comparison of SiC MOSFETs and Si-based MOSFETs' pulsed drain currents with drain-source voltage varying from 800 V to 1200 V.

As shown in Fig. 26, comparing with Si-based MOSFETs, SiC MOSFETs could work with higher pulsed drain current rating. Less parallel connected MOSFETs would leads less parasitic capacitances.

Parasitic capacitances of SiC MOSFETs could not be neglected during designing.

SiC MOSFETs' parasitic capacitances are divided as input parasitic capacitance, reverse transfer parasitic capacitance and output parasitic capacitance, expressed in (26)- (28) respectively [32].

$$Ciss=Cgs+Cgd \tag{26}$$

$$Crss=Cgd \tag{27}$$

$$Coss=Cgd+Cds \tag{28}$$

Structure of parasitic capacitance of SiC MOSFETs is showed in Fig. 27.

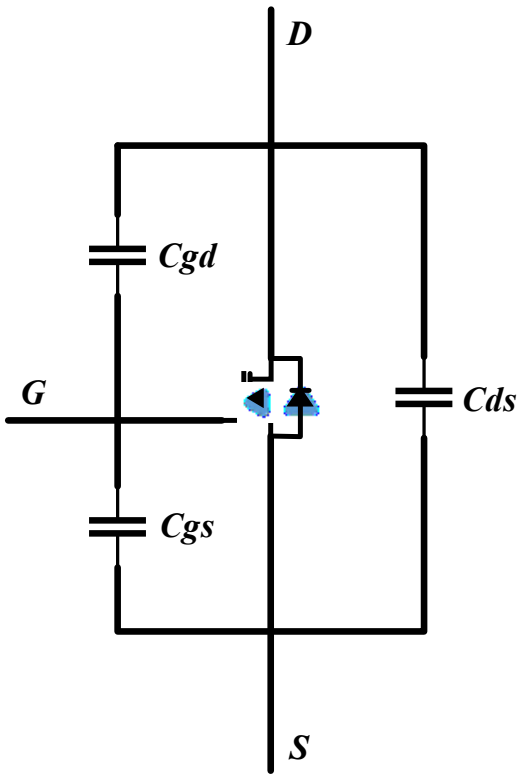


Figure 27. Structure of parasitic capacitance of SiC MOSFETs

A few researches have been addressed on studying role of parasitic capacitances of SiC MOSFETs on power electronics field.

A SiC case study for parasitic capacitance in power MOSFETs taking effect on turning-on switching speed has been detailed derived in [33]. [34]- [36] detailly introduced effect of parasitic capacitance of MOSFETs on designing and analysis power amplifier. The parasitic capacitance's effect on inverter system has been studied and analyzed in [37]- [38]. A study of utilizing parasitic capacitance of SiC MOSFETs to minimize switching losses has been detailed derived in [39].

However, there is few researches focusing on analyzing role of parasitic capacitance of SiC MOSFETs on pulsed power generator system.

For topology of isolated single-ended resonant converter proposed in chapter 3, parasitic capacitance of SiC MOSFETs taking effect on spike voltage performance will be detailly analyzed in next section.

4.2 Parasitic parameters analysis on proposed pulsed power converter

Pulsed power converter system is detailly introduced in chapter 3. There are four modes for pulsed power generator system's operation.

At beginning of mode 3, a spike voltage will occur on semiconductor switch *S*. This section will detailly analyze how the parasitic parameters of circuit, especially parasitic capacitances of SiC MOSFETs, affecting spike voltage across switch *S*, which is critical for semiconductor switch protection.

SiC MOSFETs model with parasitic capacitances on proposed pulsed power generator system is showed in Fig. 28.

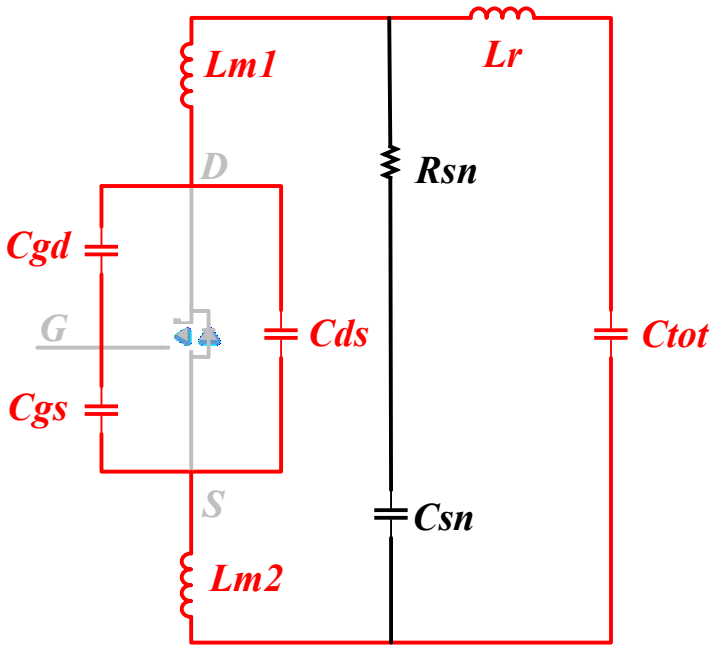


Figure 28. SiC MOSFETs model with parasitic capacitance on proposed pulsed power generator system

There is no resonant current forward through the anti-parallel body diode of SiC MOSFET at the beginning of mode 3. The switch S performs like an open circuit. With existence of parasitic capacitance C_{gs}, C_{gd} and C_{ds} of SiC MOSFETs, a new resonant tank occurs, including parasitic capacitance C_{gs}, C_{gd} and C_{ds} of SiC MOSFET, resonant inductor L_r, parasitic inductance of trace

on PCB L_{m1} and L_{m2}, resonant capacitor C_r and equivalent output capacitor C_o as highlighted in Fig. 28. The resonant tank will undamped self-resonant with a very high frequency, which will lead to very severe EMI problem. In order to eliminate undamped self-resonant, a RC snubber circuit across switch S is necessary for forcing resonant tank functioning at damped oscillation. Resistor and capacitor of snubber circuit is denoted as R_{sn} and C_{sn} respectively in Fig. 28.

Due to the parasitic capacitance C_{gd} is far less than parasitic capacitance C_{ds}, equivalent capacitance across SiC MOSFETs' drain and source is approximately equals to parasitic capacitance C_{ds} as showed in (29)

$$C_{d\text{-}s}=\frac{C_{gd}\cdot C_{gs}}{C_{gd}+C_{gs}}+C_{ds}\approx C_{ds} \tag{29}$$

A simulation showed in Fig. 29 is addressed for comparing with and without C_{gd} and C_{gs} on spike voltage analysis.

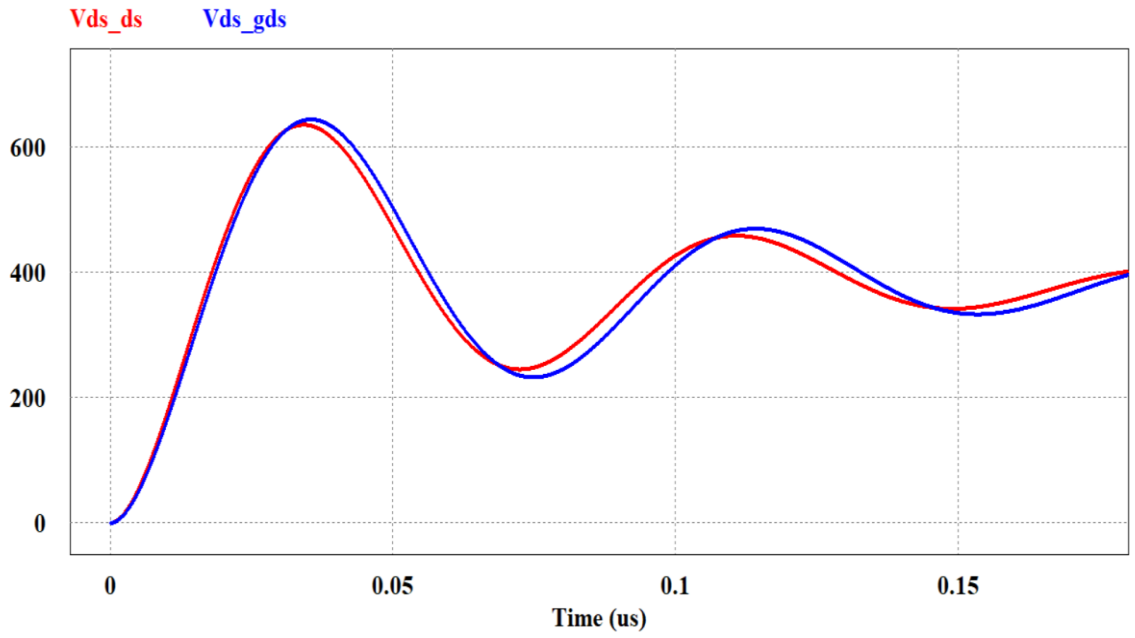


Figure 29 Comparison simulation of with and without Cgd and Cgs on spike voltage analysis

(Blue: with C_{gd} and C_{gs}, Red: without C_{gd} and C_{gs})

As showed in Fig. 29, two waveforms are almost same, which proves that parasitic capacitances C_{gs} and C_{gd} does not affect spike voltage on SiC MOSFETs much.

Compared with impedance of parasitic capacitance C_{ds}, impedance of parasitic inductance of trace on PCB L_{m1} and L_{m2} is far less.

A simulation showed in Fig. 30 is addressed for comparing with and without L_{m1} and L_{m2} on spike voltage analysis.

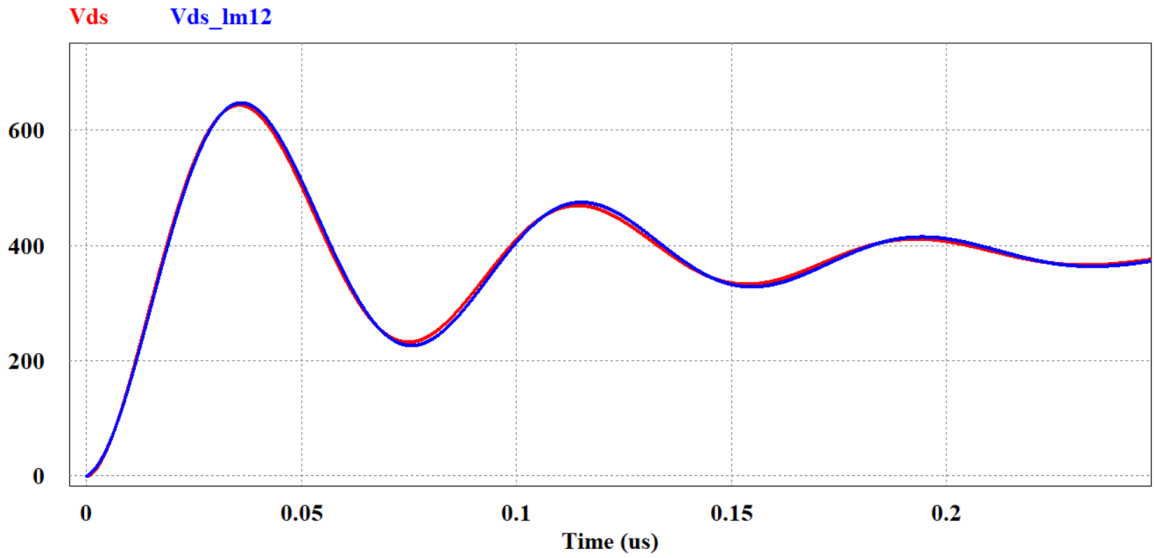


Figure 30 Comparison simulation of with and without Lm1 and Lm2 on spike voltage analysis

(Blue: with L_{m1} and L_{m2}, Red: without L_{m1} and L_{m2})

As showed in Fig. 30, two waveforms are almost same, which proves that parasitic inductances L_{m1} and L_{m2} does not affect spike voltage on SiC MOSFETs much.

Thus, this section neglects effects of parasitic capacitances C_{gd} and C_{gs}, parasitic inductances L_{m1} and L_{m2} on spike voltage analysis.

For simplifying the analyzing model, due the capacitance of C_{tot} is much larger than either parasitic capacitance C_{ds} of SiC MOSFETs or capacitance of snubber circuit C_{sn}, this section assumes C_{tot} as a voltage source with voltage as V_{Cr_min}.

Where C_{tot} equals to:

$$Ctot = \frac{C_r \cdot C_o \cdot n^2}{C_r + C_o \cdot n^2}$$

Then this section will equally combine branch of parasitic capacitance C_{ds} and branch of RC snubber circuit into a simple RC branch with parameters C_{eq} and R_{eq} for further analysis.

The impedance of those two branches including C_{ds}, C_{sn} and R_{sn} described above is equals to:

$$Z = \frac{\frac{1}{j\omega \cdot Cds} \times (\frac{1}{j\omega \cdot Csn} + Rsn)}{\frac{1}{j\omega \cdot Cds} + \frac{1}{j\omega \cdot Csn} + Rsn} \tag{30}$$

Where ω equals to:

$$\omega = \sqrt{(Cds + Csn) \cdot Lr}$$

By means of mathematical calculation, equation (30) can be equally transferred as (31):

$$\sqrt{\frac{1 + \omega^2 \cdot Csn^2 \cdot Rsn^2}{Rsn^2 \cdot \omega^4 \cdot Cds^2 \cdot Csn^2 + \omega^2 \cdot (Cds + Csn)^2}} \angle [\, arctan(-Rsn \cdot \omega \cdot Csn) + \pi - arctan(\frac{Cds + Csn}{\omega \cdot Csn \cdot Cds \cdot Rsn})] \tag{31}$$

Based on equation (31), we will get the value of C_{eq} and R_{eq} as:

$$Ceq = \sqrt{\frac{1 + \omega^2 \cdot Csn^2 \cdot Rsn^2}{Rsn^2 \cdot \omega^4 \cdot Cds^2 \cdot Csn^2 + \omega^2 \cdot (Cds + Csn)^2}} \cdot sin(\varphi)$$

$$Req = \sqrt{\frac{1 + \omega^2 \cdot Csn^2 \cdot Rsn^2}{Rsn^2 \cdot \omega^4 \cdot Cds^2 \cdot Csn^2 + \omega^2 \cdot (Cds + Csn)^2}} cos(\varphi)$$

Where φ equals to:

$$\varphi = arctan(-Rsn \cdot \omega \cdot Csn) + \pi - arctan(\frac{Cds + Csn}{\omega \cdot Csn \cdot Cds \cdot Rsn})$$

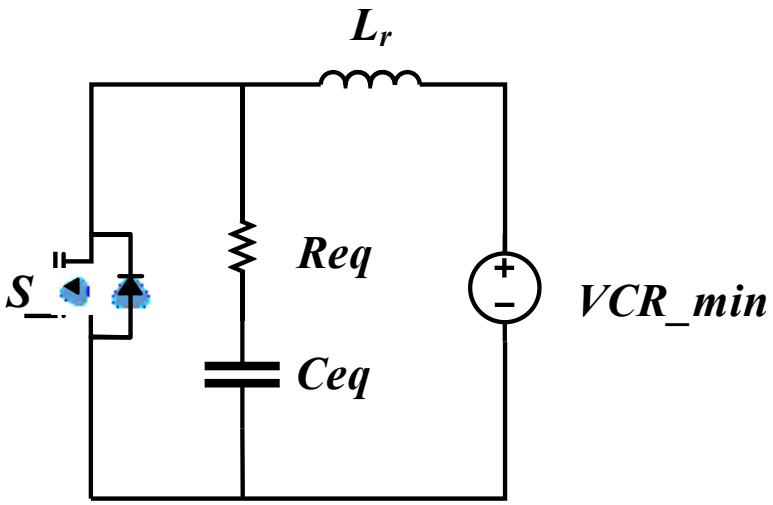


Figure 31. Equivalent circuit of parasitic capacitance model

With the value of C_{eq} and R_{eq}, we get the equivalent circuit of switch S on spike voltage analysis shown as Fig. 31.

The complex SiC MOSFETs switching model is transferred as a simple RLC resonant circuit as Fig. 31.

A second order matrix of RLC resonant circuit as (32) and (33) is conducted to gain the time-varying response of voltage across SiC MOSFETs switch S. The voltage across SiC MOSFETs switch S is set as output signal Y. The voltage V_{Cr_min} is set as input signal U_{in}. Denote voltage of C_{eq} as V_{Ceq}, current through resonant inductor as I_{Lr}.

$$\begin{bmatrix} \dot{VCeq} \\ \dot{ILr} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{Ceq} \\ -\frac{1}{Lr} & -\frac{Req}{Lr} \end{bmatrix} \cdot \begin{bmatrix} VCeq \\ ILr \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{Lr} \end{bmatrix} \cdot Uin \tag{32}$$

$$Y = [1 \quad Req] \cdot \begin{bmatrix} VCeq \\ ILr \end{bmatrix} \tag{33}$$

Using matrix above, the transfer function H(s) is:

$$H(s)=\frac{Y(s)}{Uin(s)}=\frac{\frac{Req}{Lr}\cdot s+\frac{1}{Lr\cdot Ceq}}{s^2+\frac{Req}{Lr}\cdot s+\frac{1}{Lr\cdot Ceq}} \tag{34}$$

Thus:

$$Y(s)=Uin(s)\cdot H(s) \tag{35}$$

Taking inverse Laplace transform to equation (35), we can get relationship of voltage across SiC MOSFETs switch S varying with time y(t).

The maximum value of spike voltage across switch S gained at the moment of $t=\pi\cdot\sqrt{Lr\cdot Ceq}$.

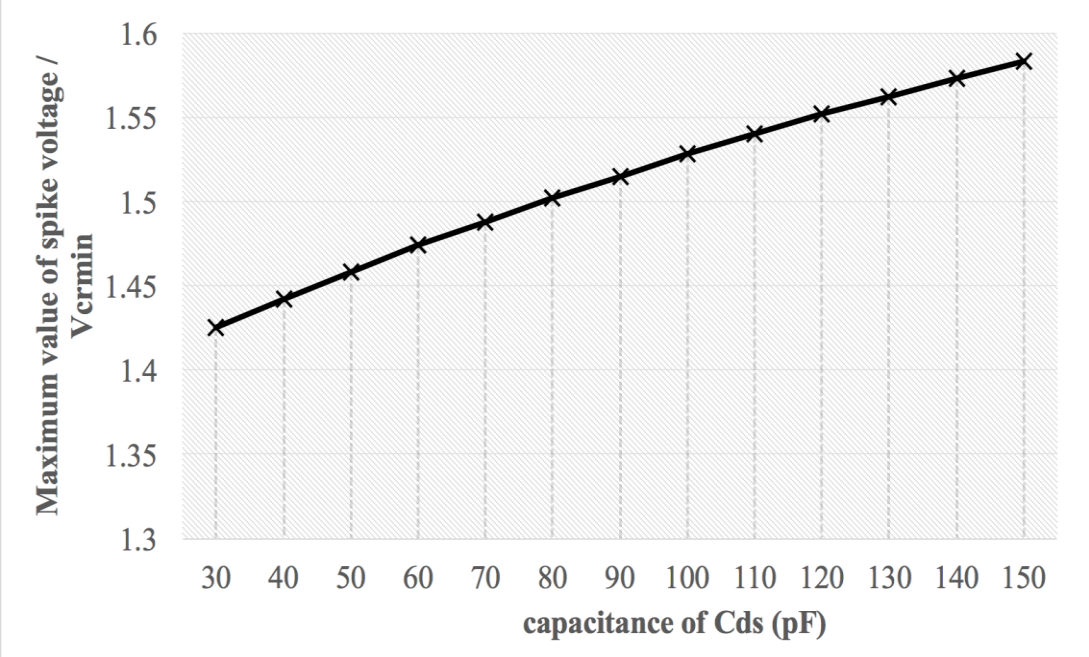


Figure 32. Relationship between Cds and maximum value of spike voltage across switch *S*

Using MATLAB, we gain the relationship between parasitic capacitance C_{ds} of SiC MOSFETs and maximum value of spike voltage across switch *S* as showed in Fig. 32. (assume R_{sn} is 56ohm, C_{sn} is 165pF)

With increase of parasitic capacitance C_{ds} of SiC MOSFETs, the spike voltage across switch *S* will increase.

4.3 Simulation verification for proposed mathematical model

In order to accurately simulate spike voltage across SiC MOSFETs for pulsed power converter system, we utilize Ansys Q3D, in Fig. 33, to simulate parasitic inductance of trace L_{m1} and L_{m2} on PCB. Fig. 34 shows 3D vision of SiC MOSFETs position on PCB.

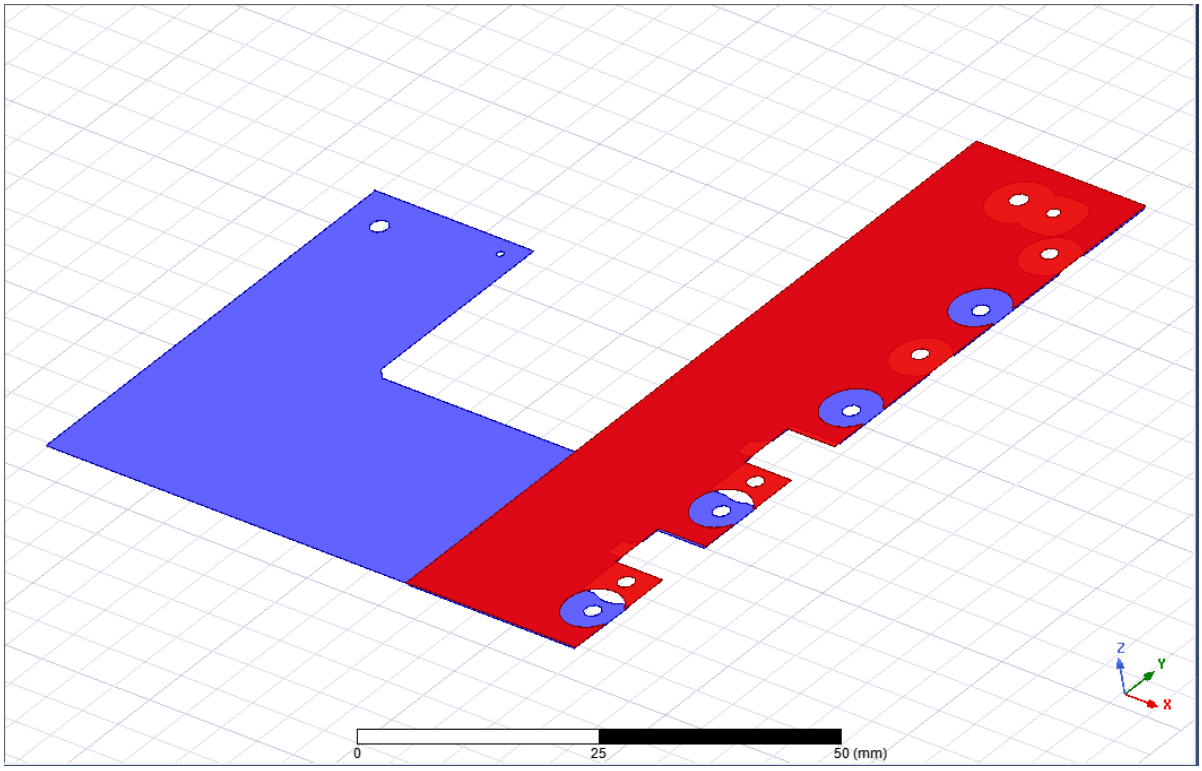


Figure 33. Simulation of parasitic inductance L_{m1} and L_{m2} of trace on PCB based on Ansys Q3D

ANSYS Q3D Extractor efficiently performs electromagnetic field simulations. Due to long and thick traces is applied to connect SiC MOSFETs to resonant circuit, this thesis set sources and sinks for both top layer (red) and bottom layer(blue) to simulate parasitic inductance L_{m1} and L_{m2} separately. The top layer is used to connect the drain terminal of the SiC MOSEFTs to inductor L_{in} and the bottom layer is used to connect the source terminal of the SiC MOSFETs to ground.

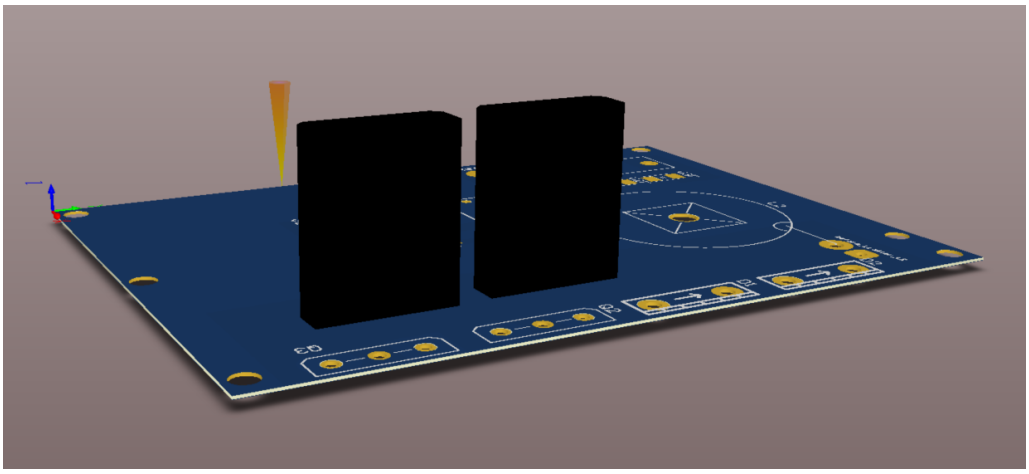


Figure 34. 3D vision of SiC MOSFETs position on PCB

After simulation by Ansys Q3D, we get value of parasitic inductances as L_{m1} is 14.7 nH and L_{m2} is 18.83nH.

With value of L_{m1} and L_{m2}, a simulation model for the spike voltage analysis has been developed in PSIM as showed in Fig. 35.

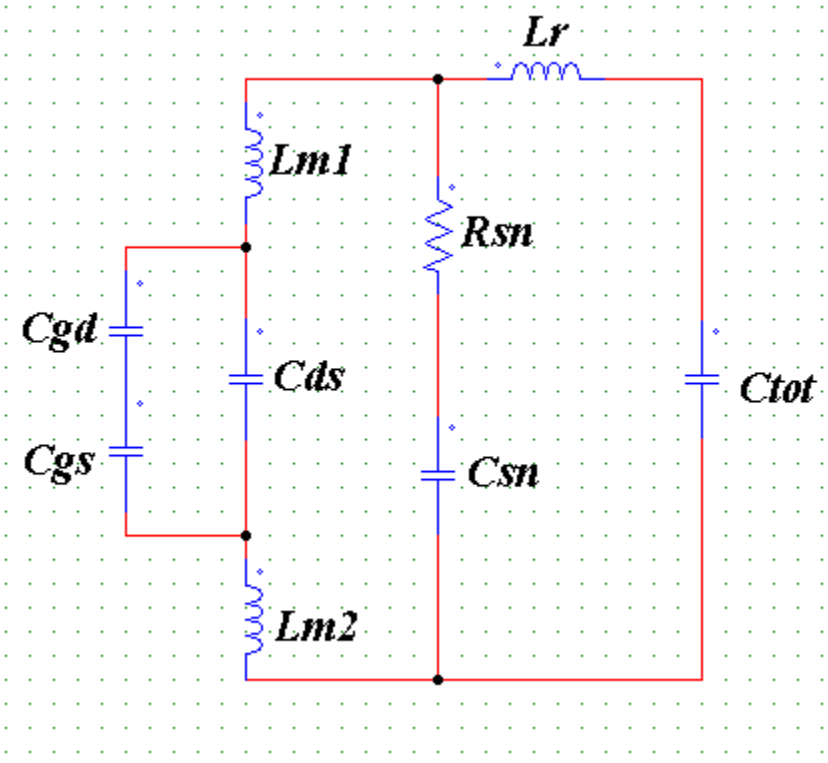


Figure 35. Simulation model for the spike voltage analysis on PSIM

Fig. 36 shows the simulation waveforms, with increase of parasitic capacitance C_{ds} of SiC MOSFETs, the spike voltage across switch *S* increases either, which verifies the analysis last section proposed.

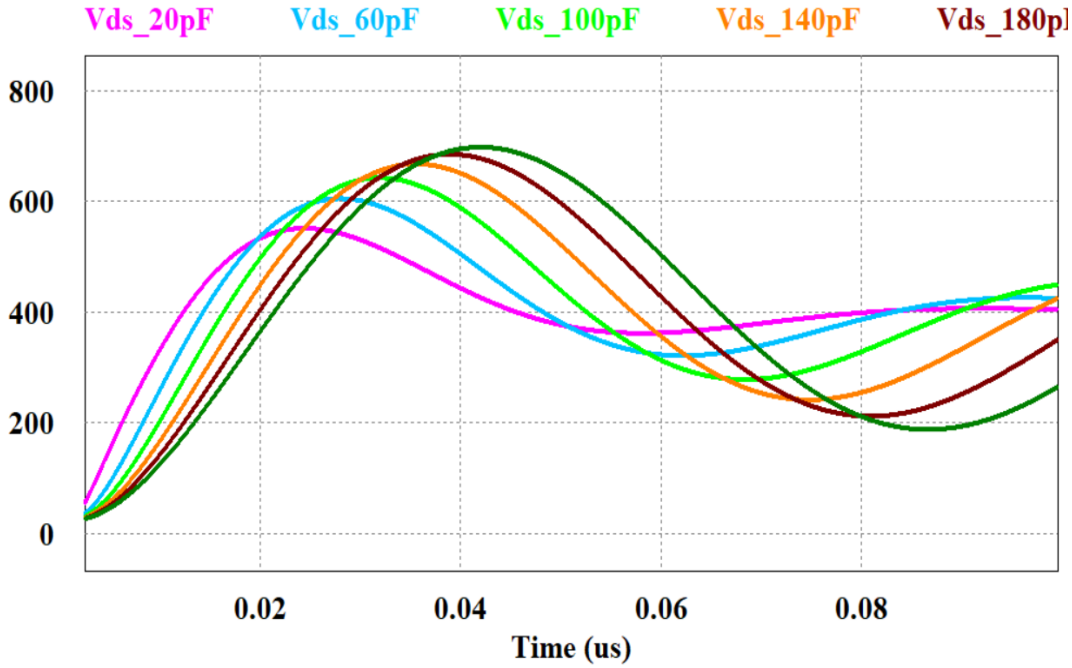


Figure 36. Simulation waveform of drain to source voltage on switch S with different value of parasitic capacitance Cds of SiC MOSFETs

Chapter 5 Hardware verification test

5.1 Hardware verification test of proposed pulsed power converter system

Fig. 37 is the hardware setup for pulsed power converter and spike voltage across SiC MOSFETs testing. Two SiC MOSFETs parallel connected, were used for switch *S* with current sharing purpose.

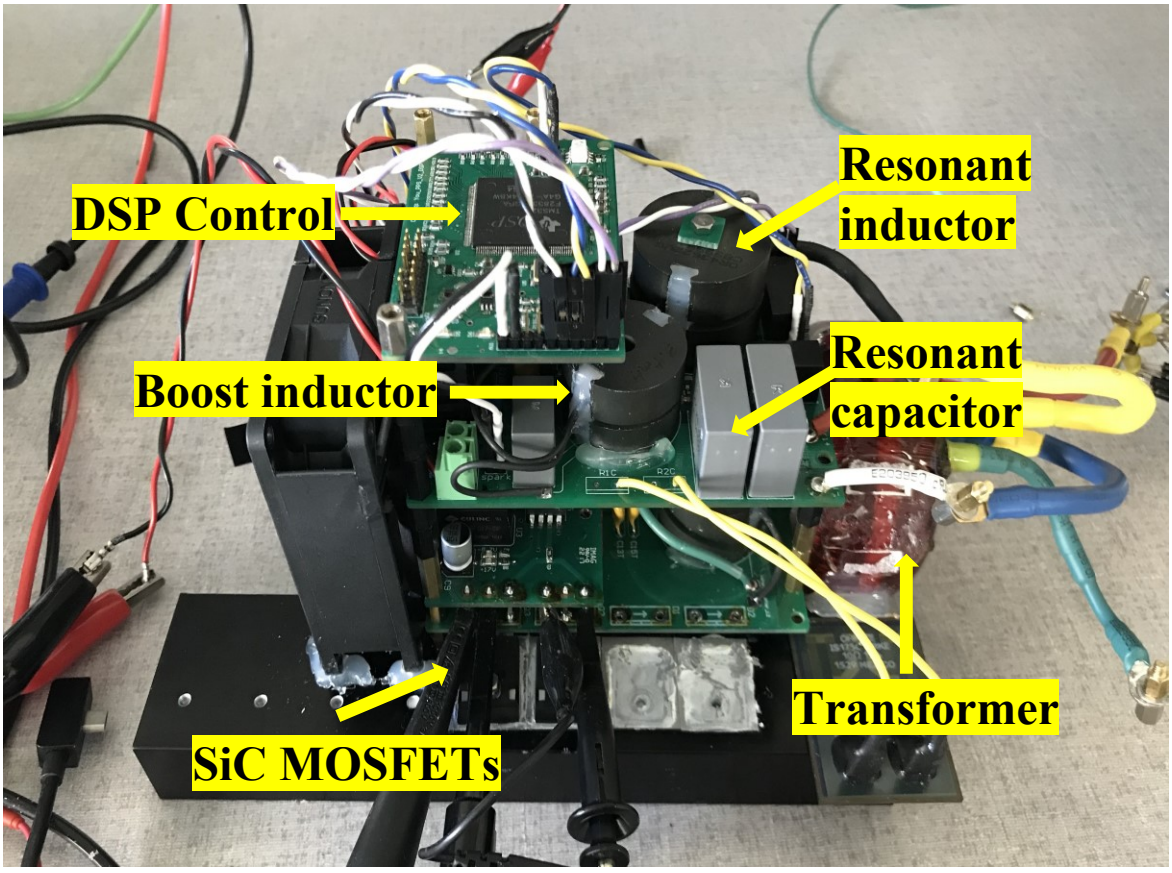
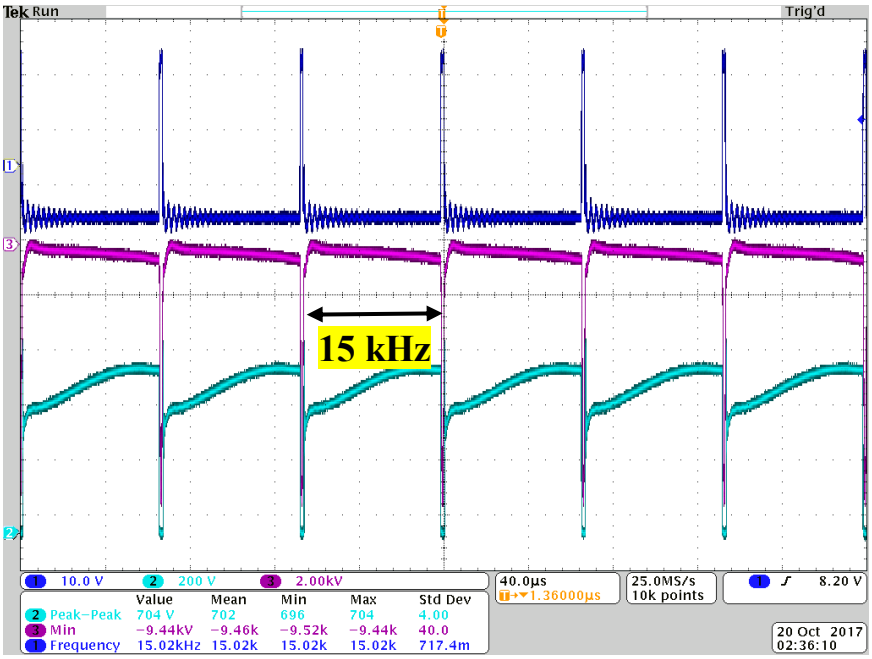
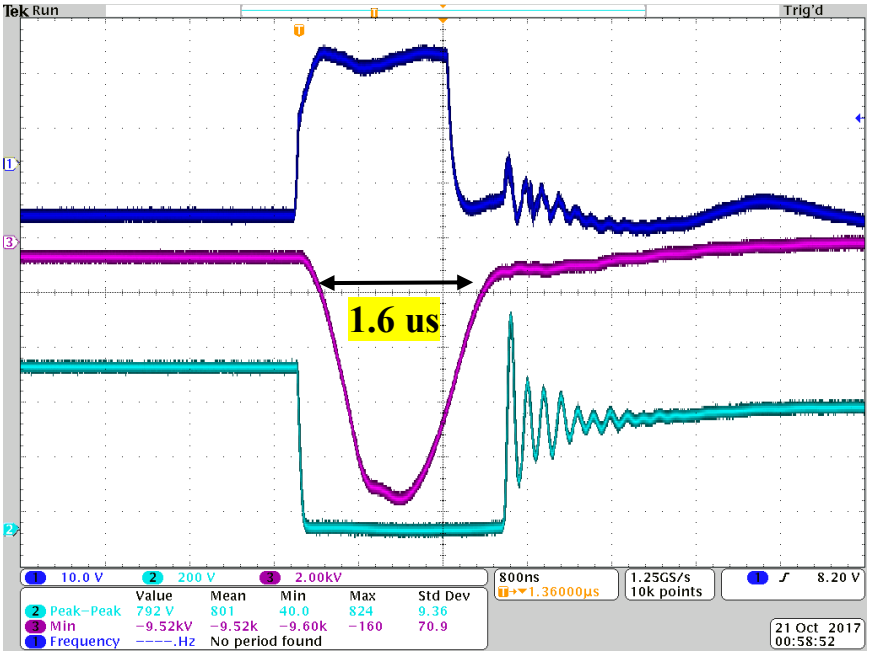


Figure 37. Hardware prototype of pulsed power generator system



(a)



(b)

Figure 38 . (a) Measured waveforms of gating signal, output pulsed voltage and the SiC MOSFETs drain-source voltage. (b) zoom-in view of testing waveforms

(Blue: Gate signal of SiC MOSFETs, Purple: Output voltage, Green: SiC MOSFETs drain-source voltage)

Fig. 38(a)(b) shows functionality testing waveforms.

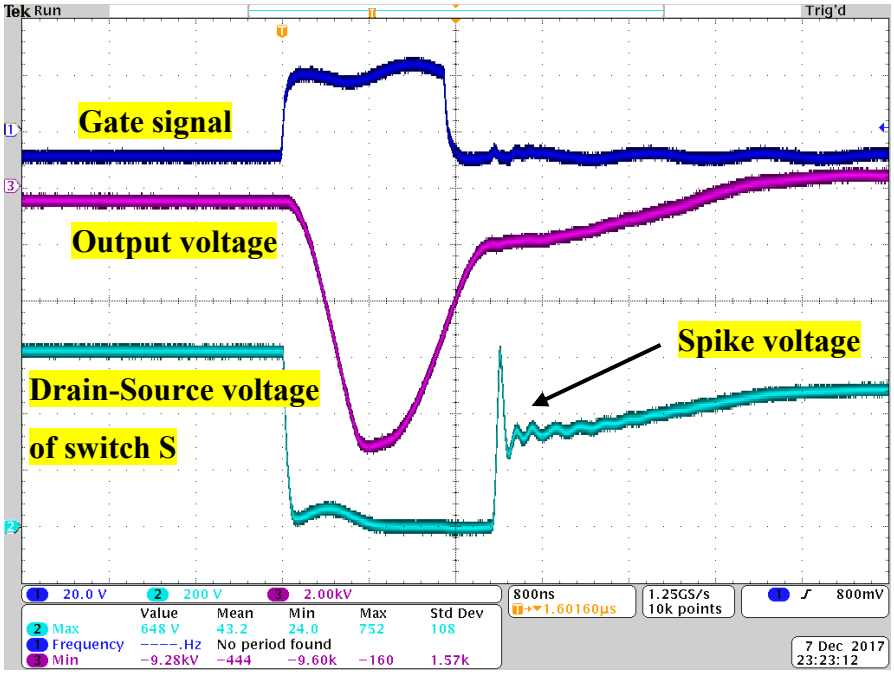
The blue waveform shows gate signal of switch *S* on resonant stage. The purple waveform shows pulsed output voltage across chamber load. The green waveform shows voltage across switch *S*. The pulse duration is 1.6 μs and a pulsed is occurred on MOSFETs drain-source voltage. The pulse frequency is 15 kHz as deigned. From the Fig. 38(b), the switch opens between half period of resonant and a full period of resonant. Duty cycle of switch *S* is only 2.4% controlled by DSP which requires fast turning-off specification of switch *S*. The output voltage does not hit as -12 kV because of generation of plasma varying load characteristic of chamber load. There is a spike voltage across SiC MOSFETs. A spike voltage and ringing could be observed on gate signal due to effects of parasitic parameters of circuits. Designing specifications of pulsed power converter system is well addressed.

5.2 Comparison verification test of parasitic capacitances of SiC MOSFETs' effect on spike voltage

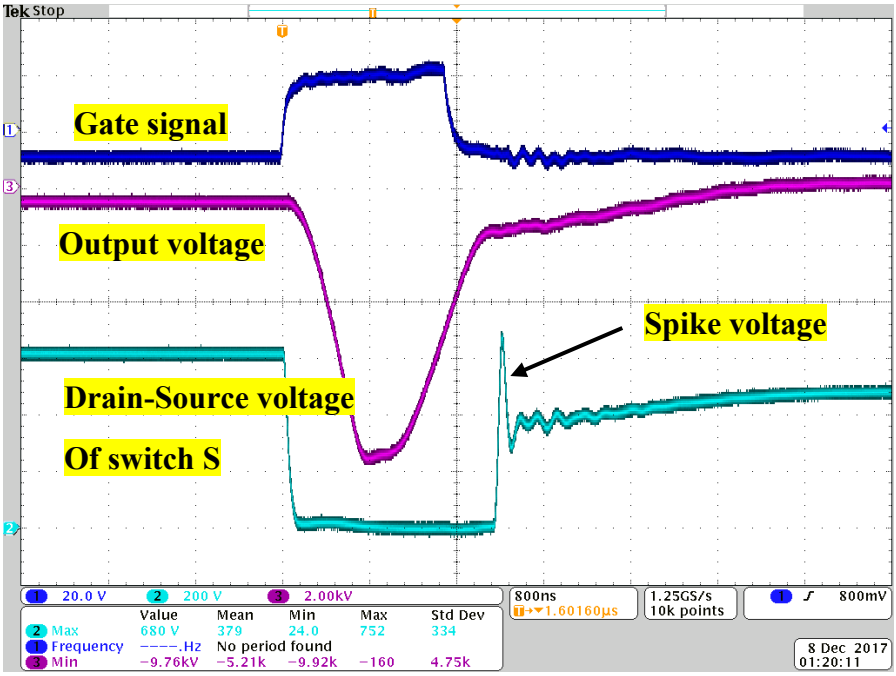
In order to specify the effect of parasitic capacitance C_{ds} of SiC MOSFETs on spike voltage of pulsed power converter, this thesis chooses two different SiC MOSFETs with same voltage rating to do comparison test. The information of two different SiC MOSFETs are listed at Table II.

Table II MOSFETs parameters

Name	Manufacture	Voltage rating	Cds @ Vds = 800 V
SCT2160KE	Rohm	1200 V	38 pF
SCT2080KE	Rohm	1200 V	59 pF



(a)



(b)

Figure 39 Comparison test within two different SiC MOSFETs with different values of parasitic capacitances

(a)SCT2160KE (b)SCT2080KE

Fig. 39(a)(b) shows test waveforms of two different SiC MOSFETs separately. There is a voltage

spike occurs on SiC MOSFETs as anti-parallel diodes of SiC MOSFETs stop conducting current. The spike voltage of SCT2160KE is 648 V. The spike voltage of SCT2080KE is 680V which is higher due to its higher parasitic capacitance C_{ds}. Fig. 40 gives the spike voltage performance comparison of two SiC MOSFETs with zoom-in view.

With existence of SiC MOSFETs' parasitic capacitance, spike voltage across semiconductor switch *S* occurs. Fig. 39 and Fig. 40 show the parasitic capacitance of SiC MOSFETs do affect spike voltage on switch *S*. With higher parasitic capacitance, the switch has higher possibility of suffering over voltage damage. For pulsed power converter application, as switch get short circuit damage, the converter self will suffer an over current issue. Thus, parasitic capacitance of SiC MOSFETs is a critical part as designing a pulsed power converter.

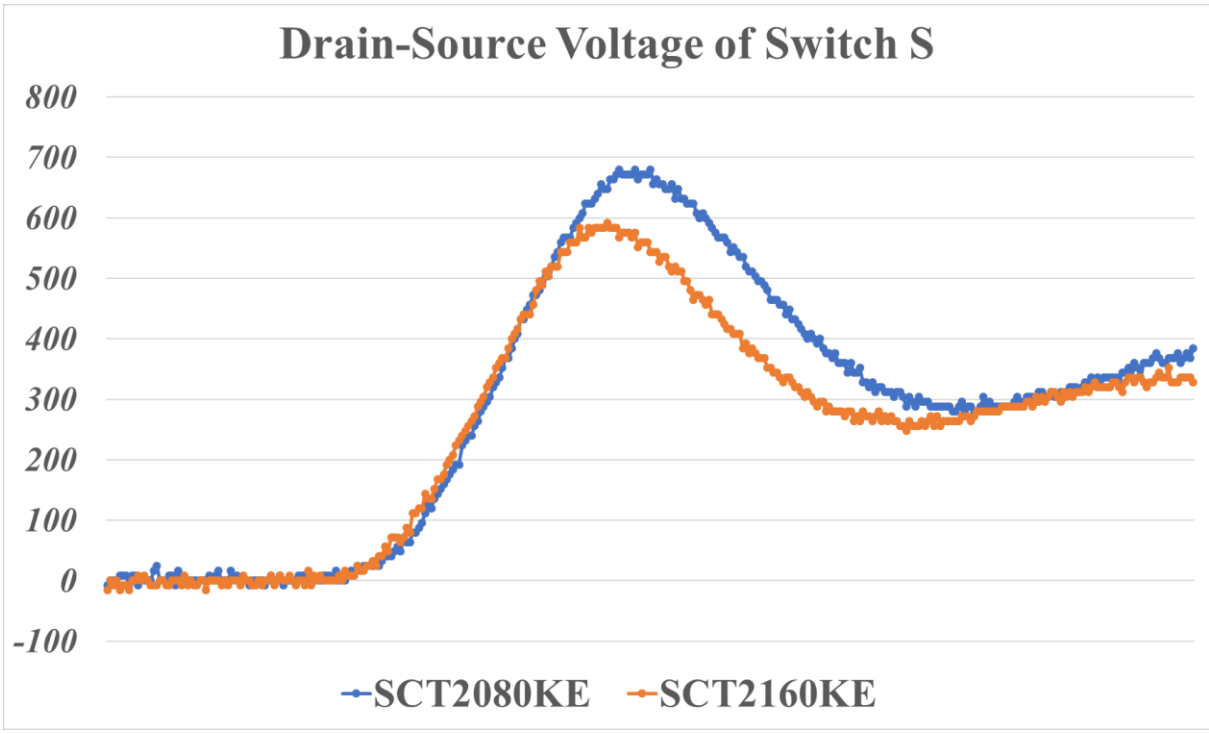


Figure 40. Comparison test within two different SiC MOSFETs with different values of parasitic capacitances zoom in view

Chapter 6 Conclusion and future work

6.1 Conclusion

Due to the specification of high temperature, plasma arose to attention in the past few decades. Plasma technology has been widely used in different industrial fields.

Plasma does not exist under normal condition on earth. The artificial plasma is usually generated by an external electric field with neutral gas.

With development of plasma technology, different types of plasma generators have been introduced in the past few decades. The Marx Generator, Inductive Adder topology and Magnetic Pulse Compression technology are always used for high power level application. This thesis has proposed a pulsed power generator system including a boost stage and resonant stage designed for low power high voltage high frequency applications.

This thesis detailly introduces and analyzes the operating principles of a boost converter. This thesis utilizes both analog and digital control systems to implement a boost voltage function and a current limiting function.

This thesis detailly introduces and analyzes the proposed resonant stage with four operation modes. The mathematical model of the resonant stage is detailly introduced and has been verified by software simulation and hardware verification.

SiC MOSFETs are good candidates for high voltage high frequency applications, the parasitic capacitances of SiC MOSFETs could not be neglected during circuit design. A mathematical model of parasitic capacitances of SiC MOSFETs' effect on spike voltage has been properly set

up in chapter 4. Simulations and a comparison test was conducted, proving the proposed mathematical model has been well addressed.

6.2 Future work

There is still some work left for this thesis as below:

- A double loop control for boost circuit should be conducted.
- Parasitic capacitances of SiC MOSFETs analysis with non-linear parasitic capacitances model is needed to be considered for more accurate analysis.
- A close loop control for resonant stage could be considered.

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