Investigation of the Performance of Photon Counting Arrays Based on Polycrystalline Silicon Thin-Film Transistors

by

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Abstract

Projection x-ray imaging is commonly employed to visualize internal human anatomy and used to produce diagnostic images. Modern projection imaging is typically performed using an active matrix, flat panel imager that is comprised of a converter layer overlying a pixelated array. The images are formed by converting x-ray photons into electrical signals, and then integrating those signals over a frame time – a method referred to as fluence integration.

Recently, imagers employing a second method for creating x-ray images – referred to as photon counting – have been developed and used to perform mammographic imaging (a form of projection imaging). Photon counting involves measuring the energy of each interacting x-ray photon and storing digital counts of the number of photons exceeding one or more energy thresholds. Because the imaging information is stored digitally, photon counting imagers are less susceptible to noise than fluence-integrating imagers – which improves image quality and/or decreases the amount of radiation required to acquire an image.

Current photon counting mammographic imagers are based on crystalline silicon and are limited in detection area. In order to produce an image, the array is moved in a scanning motion across the object of interest. A photon counting imager with larger detection area would benefit other projection imaging modalities – such as radiography (which produces, for example, chest x-ray images) or fluoroscopy (which is used for non-invasively inserting stents and other medical devices). However, techniques to increase detection area, such as tiling multiple arrays, result in increased imager complexity or cost. For this reason, our group has been exploring the possibility of creating photon counting arrays using a different semiconductor material, referred to as polycrystalline silicon (poly-Si). This material is fabricated using a thin-film process, which allows the economic manufacture of monolithic, large-area arrays and has favorable material properties for creating complex, high speed circuits.

Using poly-Si, a set of prototype arrays have been designed and fabricated. The design of the arrays consists of four components: an amplifier, a comparator, a clock generator, and a counter. Several circuit variations were created for each component, and circuit simulations were performed in order to determine energy resolution and count rate values for each variation of each component.

For the amplifier component, all circuit variations were determined to have an energy resolution of ~10% when presented with a 70 keV input x-ray photon (a typical photon energy level used in diagnostic imaging). This energy resolution value is

comparable to those reported for photon counting imagers fabricated using crystalline silicon. In addition, while count rate values for the amplifier component were roughly one order of magnitude too low for radiographic and fluoroscopic applications (which require count rates on the order of 1 million counts per second per square millimeter [cps/mm2]), a hypothetical amplifier circuit variation with count rate capabilities suitable for these applications (while preserving the same ~10% energy resolution) was designed. In addition, the count rate values for the various comparator, clock generator, and counter circuit variations ranged from 100 to 3000 kcps/mm2. Finally, due to improvements in the poly-Si fabrication process (driven largely by the display industry), future photon counting arrays employing this material can have pixel pitches as small as 250 um – a size approaching that suitable for radiographic and fluoroscopic imaging.

Chapter 1:

Introduction

Over 120 years after their discovery, X rays continue to play a variety of crucial roles in modern medicine, including visualization of human anatomy. Such visualization takes the form of projection (i.e., two-dimensional) imaging and volumetric (i.e., three-dimensional) imaging. Projection imaging can be divided into static imaging (involving the production of a single image, such as for radiography and mammography) and dynamic/fluoroscopic imaging (where a series of images is produced at video rates and visualized in real time).

Considerable innovation has been applied to the development of x-ray detector technologies used to perform projection imaging. For the purpose of this dissertation, some detectors can be considered to have an identifiable component (referred to as a *backplane*) that captures the image. For static imaging, backplanes initially took the form of glass plates (and, later, plastic sheets) coated with an emulsion such as silver halide. Exposure of the emulsion to X rays forms a latent image which, after chemical development, results in a viewable image on the "film". To increase the fraction of

incident X rays that interact with the detector (referred to as x-ray quantum efficiency), as well as to amplify the amount of signal generated per X ray (referred to as x-ray sensitivity), a layer of photoluminescent material (referred to as an intensifying screen) is positioned in front of and/or behind the film. Such screen-film systems remained a dominant, ubiquitous backplane technology for static imaging for many decades.

In early forms of dynamic imaging, physicians viewed images in real time by directly observing light output from a phosphor screen positioned in line with the x-ray source and placed between the physician and the patient. However, due to the relatively low light level of images produced by such screens, physicians needed to dark adapt before viewing. The development of x-ray image intensifiers (XRIIs) overcame this limitation by amplifying the image signal by several orders of magnitude. XRIIs are comprised of an input phosphor screen, a photocathode, a high-voltage tube, an output phosphor screen and a camera. The energies of incident X rays are first converted into light photons by the input screen, and then into electrons by the photocathode. Electrons emitted from the photocathode are then accelerated in the high-voltage tube and strike the output screen – producing a signal that is captured by the (typically CCD) camera. Compared to the signal produced by the input screen, the signal presented to the camera is amplified by a factor of ~1000 or more.[1] XRIIs allow a wide variety of interventional procedures to be performed safely and relatively easily – such as inserting ports for chemotherapy or stents for vascular procedures.

In the latter part of the 20th century, a new technology for static imaging called computed radiography (CR) was successfully introduced into the clinic. CR backplanes incorporate a photostimulable phosphor that converts the energy of incident X rays into trapped signal, resulting in the storage of a latent image.[2] That image is later "read out" by using a laser to stimulate the phosphor and release the stored energy in the form of light. That released light is converted to an electrical signal, then amplified, digitized and stored in a computer for subsequent processing, viewing and archiving.

In the late 1980s, active matrix flat panel imagers (AMFPIs) were conceived and their development began.[3-5] An AMFPI is made up of an x-ray converter material positioned over a backplane taking the form of a two-dimensional pixelated array fabricated on a glass substrate. For indirect-detection AMFPIs, the converter is a phosphor screen (such as thallium-activated cesium iodide, CsI:Tl) in which the energy of incident X rays is transformed into optical light. For direct-detection AMFPIs, the converter is a photoconductor (such as amorphous selenium, a-Se) in which x-ray energy is transformed into electron-hole pairs. Both types of detection result in imaging signal that is captured by, and stored in, the pixels of the array. Each AMFPI pixel is comprised of a storage capacitor that retains the signal, coupled to a single thin-film transistor (TFT) that functions as an addressing switch. (In indirect-detection AMFPIs, the storage capacitor takes the form of a photosensitive element, usually a PIN photodiode.) The gate nodes of all the TFTs in a given row of pixels are connected to a common wire referred to as a *gate line*. The source nodes of all the TFTs in a given column of pixels are connected to a common wire referred to as a *data line*. Peripheral electronics are

used to "read out" the image by sequentially activating one gate line at a time in order to transfer the signals stored in the pixels along that row onto the orthogonal data lines. The signals are conveyed by the data lines to pre-amplifiers located on the periphery of the array where they are magnified before being digitized and stored in a computer. AMFPIs are versatile devices and are used to perform static and dynamic/fluoroscopic imaging, as well as volumetric imaging.

The TFTs in AMFPI pixels (and photodiodes in indirect-detection AMFPIs) are fabricated using hydrogenated amorphous silicon (a-Si:H), a semiconductor material which allows the creation of large area, monolithic imaging arrays with dimensions commensurate with human anatomy – currently as large as ~43×43 cm^2. In addition, a-Si:H TFTs and photodiodes are highly resistant to the effects of radiation.[6, 7] These desirable characteristics (i.e., large area and radiation damage resistance), together with real-time, digital imaging capabilities as well as high image quality under many conditions, have allowed AMFPIs to increasingly replace film, XRIIs and CR. However, under conditions of low x-ray exposure per frame (such as is encountered in fluoroscopy), the signal-to-noise performance of AMFPIs suffers due to the relatively high electronic readout noise of the peripheral electronics compared to the imaging signal.[8]

Given that prospects for reducing electronic readout noise in AMFPIs are poor, a variety of methods for increasing signal are being investigated. One method is to

increase x-ray sensitivity by substituting a-Se with an alternative photoconductive material such as mercuric iodide (HgI_2), lead iodide (PbI_2) or lead oxide (PbO).[9-16]

Another method is to magnify the signal stored in the pixel before readout by introducing an amplifier circuit into each pixel – a concept referred to as active pixel. Active pixel detectors created using crystalline silicon (c-Si, a common semiconductor material) are currently employed in mammographic imaging (such as the GE Senographe Crystal) and for interventional radiology and cardiology (such as the Siemens Artis Q.zen). The high electron and hole mobilities of c-Si – on the order of 1000 $cm^2/V\text{-}s$ – allow the creation of highly-performing active pixel circuits. However, unlike a-Si:H, c-Si is not well-suited to the economic manufacture of monolithic, large-area arrays and is typically not radiation resistant. While active pixel arrays based on a-Si:H have been explored,[17, 18] the rather low electron and hole mobilities of a-Si:H (which are two and four orders of magnitude lower than those of c-Si, respectively) make it difficult to design highly-performing circuits.

In this context, a promising, alternative, thin-film semiconductor material is polycrystalline silicon (poly-Si). Like a-Si:H, poly-Si allows the creation of monolithic, large-area arrays, but exhibits much higher electron and hole mobilities – within an order of magnitude of that offered by c-Si. Poly-Si TFTs also demonstrate good radiation resistance.[19] Active pixel arrays created using this material are currently being explored by our group.[20-22]

Figure 1.1 shows the circuit diagram for a typical AMFPI pixel, as well as for two active pixel circuit designs created using poly-Si. In the figure, compared to the single-transistor AMFPI pixel circuit shown in Fig. 1.1a, the active pixel circuit shown in Fig. 1.1b has a one-stage amplifier with three transistors, and the active pixel circuit shown in Fig. 1.1c has a two-stage amplifier with five transistors. Early prototypes of these one- and two-stage pixel amplifiers provide nominal signal gains of ~10 and 20, respectively,[21] which offer the potential of greatly improving the signal-to-noise ratio.

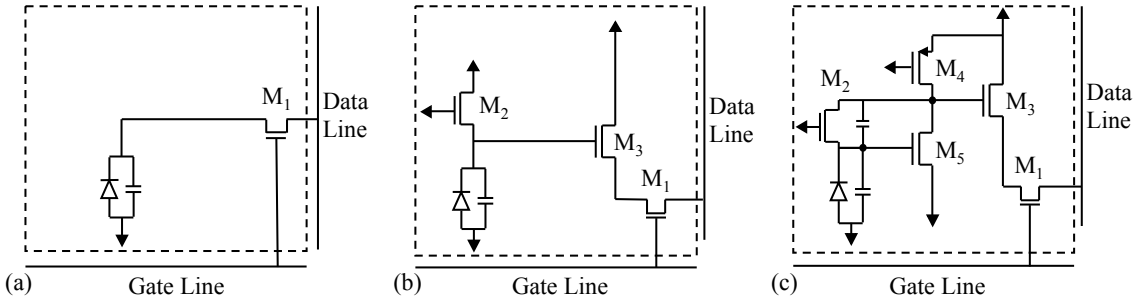


Figure 1.1. Circuit diagrams for (a) a typical AMFPI pixel, (b) an active pixel with a one-stage amplifier, and (c) an active pixel with a two-stage amplifier. In each diagram, the circuit elements labeled with "M" are transistors, the dotted box represents the pixel boundary, the empty-triangle-and-line symbol is a photodiode, and the black triangles indicate connections to externally supplied voltages.

For the x-ray detector technologies described above, images are formed by integrating the signal created by X rays interacting with the converter – a method of imaging that can be regarded as fluence integration. This fluence is typically generated by conventional x-ray sources which produce X rays with a spectrum of energies that are tailored to a given medical application through selection of suitable materials for the target and filter of the x-ray tube. However, fluence integration results in the loss of

spectral information which could be used to improve image quality. For example, since higher-energy X rays are more likely to penetrate denser objects than lower-energy X rays, the ability to selectively view images formed only from higher-energy X rays would allow improved visualization of higher-density anatomical features with less interference from lower-density objects. To some degree, such density separation can be achieved with fluence-integrating detectors and conventional x-ray sources by acquiring and subtracting two images: one taken at a low x-ray energy and one taken at a higher x-ray energy. However, this results in increased dose to the patient, increased time to acquire the images, and registration problems if the patient moves between acquisition of the two images.

In comparison to fluence-integrating detectors, photon counting detectors can perform density separation imaging using a single image acquisition. A photon counting detector measures the energy of each interacting X ray individually and records this information digitally. Because the imaging signal information is stored digitally within each pixel, photon counting detectors are not susceptible to electronic readout noise. In addition, photon counting detectors can potentially eliminate Swank noise (i.e., variation in the amount of converted signal for each interacting X ray).[23] For those reasons, photon counting detectors offer the prospect of improved image quality and, potentially, decreased radiation dose.

Photon counting detectors based on c-Si have been employed for mammographic imaging.[24, 25] Those devices take the form of a linear array of silicon strip detectors

coupled to readout electronics. To form an image, the array moves in a sweeping motion across the field of view during irradiation to form a 2D image –providing, for example, a 26×24 cm^2 image with an acquisition time on the order of 1 second.[24] The detector has a pitch of 50 μm and employs two energy thresholds [26] set to 10 keV (to remove background noise) and 18-22 keV (to separate low- and high-energy photons)[27]. Mammographic imaging using such photon counting detectors has been reported to reduce radiation dose by much as ~67%.[28]

Photon counting detectors in the form of 2D pixelated arrays based on c-Si are also being explored.[29-34] Reported prototype arrays have pixel pitches ranging from 55 up to 1000 μm,[35] and employ up to 8 energy thresholds.[29] Some prototypes have capabilities which enable neighboring pixels to combine information to more accurately resolve the energy of an X ray whose signal was spread across two or more pixels.[29] (Since this dissertation is concerned with large-area detectors, the specialized photon counting detector modules under development and use for fan-beam computed tomography [CT] are not discussed.)

However, these photon counting prototypes are limited in detection area due to their c-Si-based backplane arrays. This detection area can be increased by joining multiple arrays together (commonly referred to as tiling), but this increases detector complexity and complicates assembly. In addition, the areas where arrays are joined together may not be sensitive to X rays.

For these reasons, our group has been exploring the possibility of creating photon counting backplanes (referred to as photon counting arrays, PCAs) using poly-Si and an initial set of prototype PCAs named SPC1 have been created.[36] In contrast to the ~3 to 5 transistors used to create active pixel circuits, our initial prototype PCA pixels contain several hundred transistors. This increase in transistor count is necessary in order to create the various circuit components needed to perform photon counting. Although each pixel has a very high number of transistors, this does not affect the fill factor (i.e., the percentage of pixel area that is used to collect signal) since the photodiode (for indirect detection) or storage capacitor (for direct detection) would be manufactured out-of-plane (i.e., on top of the circuits).

The schematic diagram in Fig. 1.2 shows the four components of the SPC1 photon counting pixel circuits: an amplifier, a comparator, a clock generator and a counter – similar to how other photon counting circuits are generally organized. The input to the amplifier component is an electrical signal produced by an overlying x-ray converter, such as cadmium zinc telluride (CZT) – a material with signal properties that lend itself to photon counting. That signal is amplified (by the first component) and compared (by the second component) to a user-defined energy threshold. If the signal exceeds this threshold, the comparator component will generate an output pulse. That pulse activates the clock generator component, which produces clock signals suitable for incrementing the counter component. Following image capture, the information stored in the counter is read out to external electronics, one row of pixels at a time – parallel to the readout operation of AMFPIs or active pixel imagers.

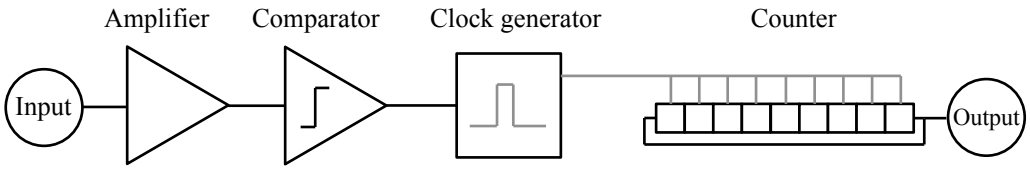


Figure 1.2. Schematic diagram of the four circuit components of a photon counting pixel.

The organization of the remainder of this dissertation is as follows. Chapter 2 presents a description of the SPC1 prototype arrays and their pixel circuit designs, along with a summary of the considerations behind those designs. While this dissertation is focused on a theoretical examination of the performance of the pixel circuits, the information presented in Chapter 2 is provided in the spirit of giving context for the simulation studies reported in Chapters 3 and 4. In addition, this information also serves as documentation to assist future empirical studies of the SPC1 arrays.

While the SPC1 prototype designs presented in Chapter 2 resulted from collaborative efforts between members of our group (including myself) and scientists at the Palo Alto Research Center, the latter chapters document my efforts to characterize the performance of those prototype designs. The results of those simulation efforts have been reported in first-author publications that have already been accepted (and presented in Chapter 3) or are under review (and presented in Chapter 4). The work has also been reported in 2 conference proceedings,[36, 37] 2 oral presentations, and 1 poster presentation.

Chapter 3 presents theoretical performance results for the pixel circuit designs of the four components of the SPC1 prototypes, as well as an estimate of the minimum achievable pixel pitch for future poly-Si-based photon counting arrays. The components are divided into analog (i.e., the amplifier) and digital (i.e., the comparator, clock generator, and counter) components. For the analog component, a circuit simulation framework was used to determine amplifier output response and energy resolution. For the digital components, a different simulation framework was used to determine robustness (employing a metric that predicts how reliably a given circuit will perform) and an estimate of count rate (employing a metric related to how quickly a circuit can resolve x-ray photons). Finally, potential improvements in the poly-Si manufacturing process that may lead to reduced pixel pitch are discussed. The work presented in Chapter 3 has been adapted from a peer-reviewed article.[38]

Chapter 4 presents a study performed to explore the count rate capabilities of the analog amplifier component. A circuit simulation framework capable of determining detailed count rate metrics for poly-Si-based amplifier circuits was developed and used to estimate the count rate of the pixel circuit designs of the amplifier component. In addition, using this framework, a hypothetical amplifier circuit with improved count rate was identified and its capabilities explored. The work presented in Chapter 4 has been adapted from a manuscript recently submitted for publication.[39]

Finally, the summary and conclusions for this dissertation are presented in Chapter 5.

Chapter 2:

Design and Development of Poly-Si Photon Counting Arrays

I. Introduction

The design of SPC1 prototype arrays was the result of a 14 month long collaborative effort involving myself and other members of our research group and two scientists at the Palo Alto Research Center (PARC). During that time, numerous material- and circuit-specific considerations were discussed and the final circuit designs of the SPC1 prototypes reflect many of those considerations. This chapter serves to document the history of the SPC1 prototypes in the spirit of providing a guide for future design efforts.

The fabrication of the SPC1 prototype arrays involved the use of low-temperature, polycrystalline silicon semiconductor material to create thin-film transistors (TFTs) for the pixel circuits. Low-temperature polycrystalline silicon is created by depositing a thin film of amorphous silicon (a-Si:H) on a quartz substrate followed by recrystallization of the a-Si:H using an excimer laser. The use of this form of polycrystalline silicon in the creation of photon counting arrays introduces a number of material-specific

characteristics that must be considered in circuit design. Compared to transistors fabricated using crystalline silicon (c-Si), TFTs created using polycrystalline silicon (poly-Si) cannot be manufactured as uniformly, resulting in variations in transistor properties and changes in circuit performance. In addition, poly-Si TFTs cannot be manufactured as small as c-Si transistors – leading to decreased circuit density and/or larger pixel pitch. While c-Si transistors currently have a minimum feature size (i.e., a value that describes the smallest structure that can be created) as small as 10 nm, the minimum feature size for poly-Si was in the range of 3-6 μm at the time that the SPC1 designs were under development. For the SPC1 prototypes, a minimum feature size of 6 μm was chosen so as to maximize fabrication yield.

In addition to these material-specific characteristics, circuit designs also have to account for process limitations imposed by the fabrication facility – which, for the SPC1 prototype arrays, was a poly-Si prototyping line at PARC. For example, the PARC prototyping line allows up to 4 metal layers for signal routing and bias voltages. Two of those layers are reserved for contacting the top and bottom of a photoconductive x-ray converter or a photodiode, leaving only 2 layers available for photon counting circuitry. Furthermore, the PARC line employs resistors created using doped a-Si:H. This material has an estimated sheet resistance of 10 MΩ/square – generally limiting resistance values to a range of 0.5 to 200 MΩ.

In order to design circuits that accounted for these characteristics and limitations, circuit simulations based on the Eldo SPICE circuit simulator (Mentor Graphics, OR)

employing version 2 of the RPI poly-Si TFT model [40] were used. To make the simulation results representative of the poly-Si semiconductor material produced by PARC, empirical measurements of individual poly-Si TFTs were performed and transistor parameters derived from those measurements were employed. (Those TFTs were previously fabricated by PARC in connection with active pixel array development – a related area of research in our lab.) Simulation frameworks were developed to determine photon counting performance metrics and simulation results were used to identify designs that were more tolerant to TFT variations, required fewer and/or smaller circuit elements, and met PARC process limitations.

II. Overview of the SPC1 designs

The SPC1 prototype arrays encompass 11 different array designs that share a number of common specifications – such as the pixel pitch, the method of signal routing, the method of signal input and the form of signal-chain architecture.

The pixel pitch of the arrays was set to 1 mm to ensure that there would be sufficient space within the pixel for the circuit elements (including ~200 TFTs) needed to create the photon counting circuits, as well as for wires that provided power and signal routing. In addition, using a common pitch allowed those wires to be organized in a nearly identical manner for each array design – greatly reducing the overall design effort, as well as making it possible for a single set of external data acquisition electronics to operate all of the arrays. Note that empirical evaluation of the prototypes is not a part of this dissertation.

Signal input considerations included selecting the type of x-ray converter material that the pixel circuits should be designed to accept input from. Ideally, a fast converter material should be employed – such as cadmium zinc telluride (CZT) – so as to maximize the count rate capabilities of the imaging system. However, as it was unknown at the time of the design of the prototypes whether it would be practical to deposit CZT on the arrays, a number of alternative approaches for signal input were developed. First, in order to allow the arrays to be tested with signal generated by x-ray radiation, some arrays were designed with a discrete a-Si:H photodiode in each pixel – which would require a scintillator such as cesium iodide (CsI:Tl) to first convert x-ray photons into optical photons. However, because a-Si:H photodiodes are inherently slow, the maximum count rate of those arrays would be limited by the photodiodes – even though the circuits of the SPC1 prototype arrays were designed to operate faster. In order to operate the SPC1 prototypes faster, all arrays include *test input pads* connected to each pixel. Those pads can be used to directly inject an electronically generated signal to a pixel circuit – thereby providing input pulses of any shape, magnitude, or rate.

Finally, the prototype arrays also employed a common signal-chain architecture consisting of 4 components: an amplifier, a comparator, a clock generator, and a counter. For each of those components, a number of circuit designs, called *variations*, were identified through simulation studies. The 11 unique prototype array designs consist of different combinations of these circuit variations. In the remaining sections of this

chapter, the circuit variations are described and the reason for including certain combinations of those variations in the prototypes is discussed.

III. Amplifier circuit design

The amplifier component is responsible for magnifying the input signal generated by the converter material. For the design of this component, the most important considerations were signal gain and bandwidth. The gain of the amplifier needs to be large enough to enable the next component (i.e., the comparator) to operate properly, while the bandwidth of the amplifier has implications for count rate and noise.

Assuming the comparator component required an input of ~1 V, the gain of the amplifier was designed to be on the order of 1000 – based on an estimated ~1 mV input corresponding to the amount of signal generated by a 70 keV x-ray photon interacting with a CsI:Tl converter and collected by a 100×100 μm^2 a-Si photodiode. (This corresponds to the size of the photodiode located in the same plane as the pixel circuits in several of the SPC1 array designs.) However, an empirical measurement performed by PARC on one of their earlier single-stage poly-Si amplifiers demonstrated a gain of only ~10 to 100. As a result, it was determined that multiple amplifier stages would be required to achieve a gain of 1000. For most of the prototypes, a 3-stage architecture, with each stage providing a gain of ~10, was chosen.

The second important consideration was amplifier bandwidth – defined as the operational frequency range of the circuit between a low-frequency 3 dB point and a

high-frequency 3 dB point. (A 3 dB point is the frequency value at which the gain of the amplifier is equal to $1/\sqrt{2}$ of the maximum gain.) For the prototypes, the main concern regarding bandwidth was noise. Specifically, flicker noise (or 1/f noise) was the only noise source considered since this type of noise is dominant at low frequencies. Flicker noise for a given transistor can be calculated using the following equation:[41, 42]

$$S_{V-flick} = \frac{k_f}{C_{ox}^2 WLf} . \qquad [2.1]$$

In the equation, k_f is a fabrication- and bias-dependent constant of the transistor, C_{ox} is the gate oxide capacitance (which depends on processing parameters and material properties, and was estimated to be 0.345 fF/μm^2 for the TFTs fabricated on the PARC line), W and L are the width and length, respectively, of the gate of the transistor and *f* is frequency (in Hertz). The integral of Eq. 2.1 over frequency yields an equation which shows that flicker noise is proportional to bandwidth. Thus, decreasing the bandwidth will decrease flicker noise. (While flicker noise can also be decreased by maximizing the W and L dimensions of the transistor, that has the undesirable effect of increasing gate capacitance – which generally reduces the efficiency of signal transfer through the circuit.) For the prototype arrays, a target bandwidth extending from ~50 to 100 kHz was chosen. The upper limit corresponds to the high-frequency 3 dB point empirically determined by PARC in the characterization of their single-stage poly-Si amplifier, while the lower limit was chosen somewhat arbitrarily – keeping in mind the effect of bandwidth on flicker noise.

With these design targets in mind (i.e., the number of stages and signal gain, as well as the frequency bandwidth), a total of three amplifier circuit variations were

created. The first two variations are three-stage designs, as shown in Figs. 2.1a and 2.1b. Comparing the two variations, the variation shown in Fig. 2.1a consists of two cutoff stages and one bandpass stage (forming a 1st order bandpass), while the variation shown in Fig. 2.1b consists of one cutoff stage and two bandpass stages (forming a 2nd order bandpass). Note that the cutoff stages are different for the two designs – also an arbitrary choice. Between each stage is an AC-coupling capacitor – which allows each stage to set its own DC bias. A value of 500 fF was chosen for this capacitor. Smaller capacitor values were found to attenuate the signal too much, and values larger than 500 fF did not provide significantly better AC-coupling performance.

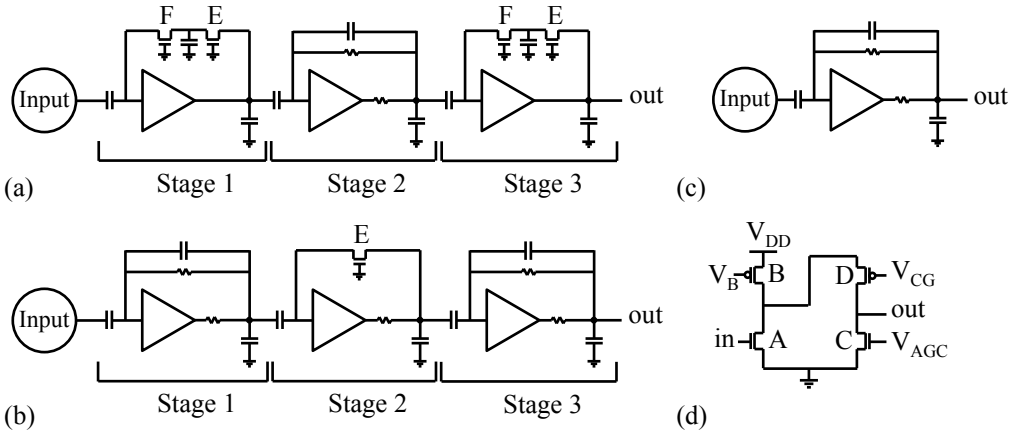


Figure 2.1. Circuit diagrams for the three amplifier circuit variations: (a) 3-stage, 1st order bandpass, (b) 3-stage, 2nd order bandpass, and (c) 1-stage, 1st order bandpass. In each diagram, the triangle is a folded cascode circuit, shown in (d) and the letters A-F denote transistors.

The third amplifier variation, shown in Fig. 2.1c, is a single-stage design consisting of the same bandpass stage used for the other variations – forming a 1st order bandpass. Due to its lower gain, this design is capable of accepting a larger input signal, while still producing an output response that is ~1 V. A larger input signal can be

produced by irradiating an array with higher energy X rays, or by directly injecting signal into the test input pads. The advantage of providing a larger input signal would be to overcome any potential noise that is present at the input of the amplifier (which would be amplified along with the input signal). Since, at the time the prototypes were created, it was unclear what the magnitude of the input noise would actually be, this single-stage design would allow empirical characterization of some prototype arrays even if the magnitude of this noise turned out to be large.

IV. Comparator circuit design

The comparator component produces an output pulse if the input signal provided by the amplifier component exceeds a user-defined threshold level. For this component, two circuit variations were created for the SPC1 prototypes – one based on a Schmitt trigger and another based on a differential pair circuit.

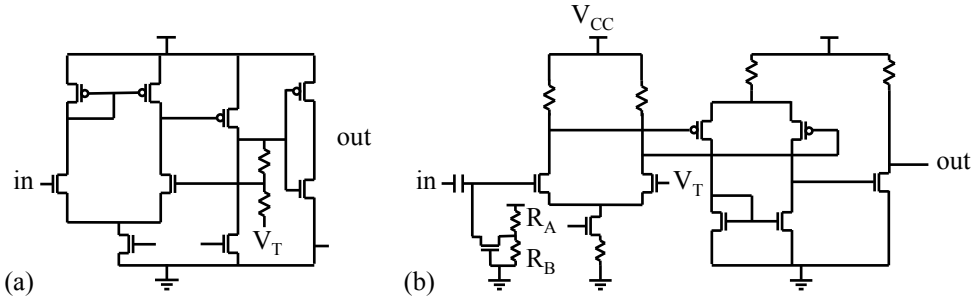


Figure 2.2. Circuit diagrams for the two comparator circuit variations: (a) the Schmitt trigger and (b) the differential pair circuit. The symbol V_T denotes where the threshold voltage should be applied. See text for details regarding the power rail V_{CC} and resistors R_A and R_B.

The comparator circuit shown in Fig. 2.2a is the Schmitt trigger variation. A key feature of a Schmitt trigger is *hysteresis* – a change in the behavior of a circuit due to something that happened in the past. Specifically, after an input signal exceeds the threshold voltage and the circuit produces an output pulse, the comparator will be unable to produce another output pulse until the input has fallen a certain amount below the threshold level. For the SPC1 prototypes, that amount was chosen to be ~500 mV. The advantage of having hysteresis in the comparator component is that noise in the input signal will not trigger multiple output pulses (assuming the noise is smaller than 500 mV).

However, the Schmitt trigger circuit variation presents a number of challenges. Most importantly, the DC bias level of the Schmitt trigger is directly tied to that of the amplifier – resulting in an unpredictable threshold level. Specifically, due to TFT variations, the DC level of the amplifier can vary from pixel to pixel – requiring, in principle, a different threshold level for every pixel.

A second challenge with the Schmitt trigger circuit is its power consumption profile. When idle, the Schmitt trigger draws very little current from the power rail, but, in order to generate an output pulse, the circuit requires a large amount of current in a very short period of time. This current "spike" can propagate through the power rails and affect the performance of other circuits. Digital components (such as the clock generator and counter) are less susceptible to such spikes, but analog components (such as the amplifier) are very sensitive to power rail spikes. In order to protect the analog

components, the prototype arrays employ two power rails – one for analog components and one for digital components. Since the comparator component converts the analog output of the amplifier into a digital output pulse, the comparator can be considered to be both analog and digital. Simulations of the Schmitt trigger circuit showed that energy resolution is greatly affected when the circuit is connected to the digital power rail. As a result, it was decided that this circuit should be connected to the analog power rail – at the cost of possibly affecting the performance of the amplifier component.

In order to overcome this power rail dilemma, the second variation of the comparator component based on a differential pair circuit (shown in Fig. 2.2b) was designed. This circuit splits the "comparing" function and the "output pulse generating" function into two sub-circuits – allowing the more sensitive comparing sub-circuit to be connected to the analog rail while the generating sub-circuit is connected to the digital rail. In addition, the input to the circuit includes an AC-coupling capacitor – which separates the DC bias level of this comparator circuit from that of the amplifier component. The resistors R_A and R_B (shown in Fig. 2.2b) ensure that the DC bias level at the input of this circuit is always 2 V (when the power rail, V_{CC}, is set to 8 V) – which allows the threshold level to be set uniformly for all pixels in an array. However, this circuit lacks hysteresis and may produce erratic output pulses – a problem that was not addressed in the SPC1 prototype designs.

V. Clock generator circuit design

The clock generator component is responsible for creating a pair of clock pulses suitable for operating the next component (i.e., the counter). Since the preceding component (i.e., the comparator) outputs a single pulse, one requirement of the clock generator is to split this signal into two non-overlapping clock pulses. In addition, the clock generator must guarantee a minimum pulse width for each clock pulse in order for the counter to operate properly – regardless of the width of the input pulse provided by the comparator. Due to the nature of the comparator, the width of the comparator output pulse can vary – depending on the energy of the x-ray photon or due to pulse pile-up when multiple pulses are spaced too closely in time and manifest themselves as a single pulse.

A circuit architecture commonly employed to create pulses with a fixed width is a monostable multivibrator (MSMV). The clock generator component of the prototype arrays is very similar to an MSMV, except it outputs 2 clock pulses (whereas an MSMV typically only outputs a single pulse). For the clock generator component, a total of 4 circuit variations, shown in Figs. 2.3a to 2.3c, were created for the SPC1 prototypes. Note that Fig. 2.3a represents two circuit variations that only differ by the transistor dimensions employed in the circuit.

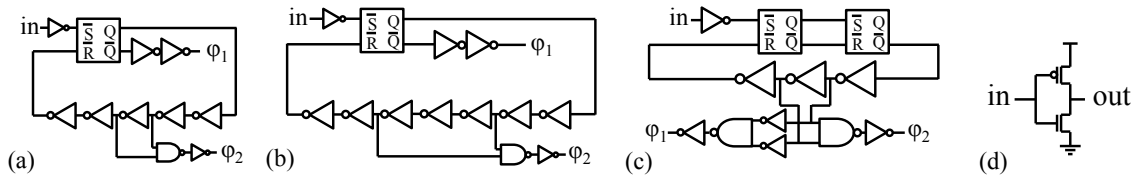


Figure 2.3. Circuit diagrams for the four clock generator circuit variations: (a) the 1SR-5inv design (with two configurations referred to as 1SR-5inv-long and 1SR-5inv-short), (b) the 1SR-7inv design, and (c) the 2SR-3inv design. In each diagram, the triangle-and-bubble symbol represents an inverter circuit, shown in (d), the combined plug-shape-and-bubble symbol represents a NAND gate, the rectangle represents an SR (i.e., set-reset) latch based on 2 NAND gates, and φ_1 and φ_2 denote the output clock pulses.

As seen in the figure, all circuit variations employ one or more set-reset (SR) latches. An SR latch outputs a digital "high" signal if the set input (labeled S-bar) is triggered, and will continue to output this signal until the reset input (labeled R-bar) is triggered – at which time, it changes to and continues to output a digital "low" signal. By connecting the output labeled Q (or, in the case of 2SR-3inv, Q-bar) to the reset input, the circuit will automatically reset itself after being triggered – resulting in a fixed-width output pulse. The width of the pulse can be adjusted by introducing delay elements between Q and R-bar. For the prototype arrays, these delay elements took the form of an inverter circuit (shown in Fig. 2.3d). Decreasing the W/L ratio of the transistors in that circuit, as well as increasing the number of inverters, increases the delay.

For the clock generator circuit variations involving a single SR latch (shown in Figs. 2.3a and 2.3b), the φ_1 clock pulse is generated by the output labeled Q-bar. Note that the two inverter circuits before the φ_1 label are intended as buffers, not delay elements. The φ_2 clock pulse is generated by attaching a NAND gate to the chain of delay-generating inverters. Note that the number of inverters straddled by the NAND

gate (and also the W/L ratio of those inverters) controls the width of the φ_2 pulse, and that the NAND gate must span an odd number of inverters.

For the remaining circuit variation shown in Fig. 2.3c, the φ_1 and φ_2 clock pulses are generated in a different manner – by tapping the 3-inverter chain. The φ_1 pulse is generated when S-bar is triggered, and the φ_2 pulse is generated when R-bar is triggered. Again, the inverter circuit before the φ_1 and φ_2 outputs are buffers.

The four clock generator circuit variations described above were created in the spirit of addressing a "flaw" discovered in the circuit behavior during the design process. For the single-SR-latch configuration, input pulses with a very specific spacing in time can cause the clock generator to produce clock pulses that are overlapping and/or do not have the required minimum pulse width. Either of these conditions would invalidate the value stored in the counter component, as explained in more detail in Sec. VI of this chapter. This problem, referred to as *racing*, was first discovered in the 1SR-5inv-long design, and the 1SR-5inv-short design was created to try to make the probability of encountering the problem less likely. Specifically, the "short" variant employs transistors with shorter gates, which decreases the amount of delay produced by the inverter chain. Due to this modification, racing will only occur if the input pulses are spaced closer together. For the 1SR-7inv design, even closer input pulse spacing is required for racing to occur. Unlike the "short" variant, the 1SR-7inv design does not rely on further shortening of the transistor gates. Due to minimum feature size limitations, the length of the gates could not be fabricated shorter than those specified for the "short" variant, and

thus the 1SR-7inv design employs carefully selected transistor dimensions for the inverters in order to "shape" the pulse as it propagates through the inverter chain in an attempt to suppress racing.

However, none of these three circuit variations are immune to racing. Due to the statistical nature of x-ray photon generation, the flux rate reported for a given imaging modality represents only an average rate (e.g., on the order of 10^6 to 10^7 counts per second per mm^2 for radiography [see Appendix 2.B])[43]. Thus, there is always the possibility of encountering input pulses spaced any arbitrary distance apart. The fourth variation, the 2SR-3inv design shown in Fig. 2.3c, circumvents the design flaw entirely by adding a second SR latch to the input of the circuit. This SR latch acts as an enable flag for the clock generator. When an input pulse arrives, this additional latch will produce an "enable" signal that allows the rest of the clock generator circuit to operate. If additional input pulses arrive while the enable signal is active, they are ignored. The enable signal will be deactivated after the circuit has finished generating the two clock pulses, at which time the circuit is ready for another input pulse.

VI. Counter circuit design

The counter is the final component in the signal chain and stores the number of counts detected by the pixel circuit. The number of counts is stored in a binary format in *bits*. For the prototype arrays, a 9-bit, maximum-length linear feedback shift register (LFSR) architecture was employed. The 9-bit length chosen for the prototype arrays was

arbitrary. A clinically useful imager would likely require more bits. A schematic diagram of the LFSR is shown in Fig. 2.4a.

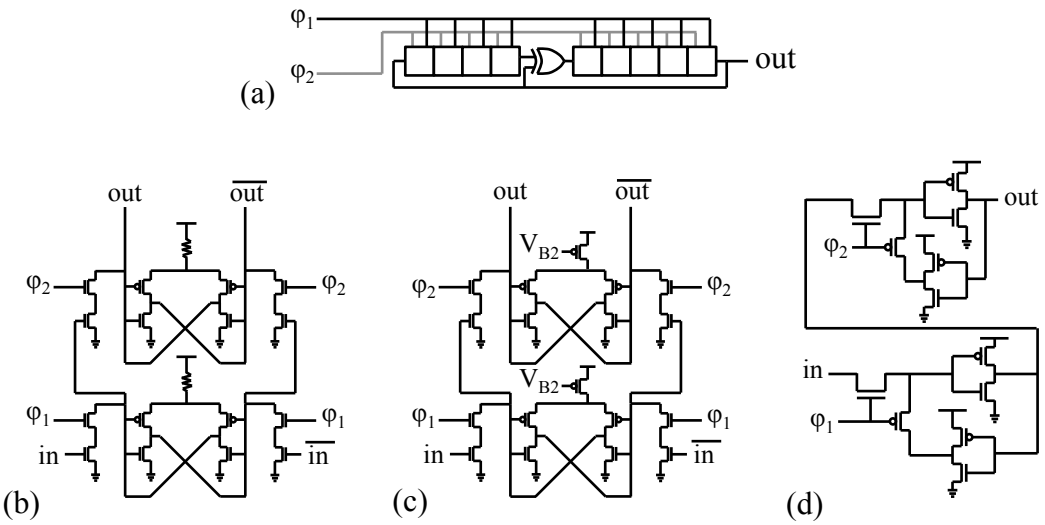


Figure 2.4. Schematic diagram of (a) the 9-bit, maximum-length LFSR, as well as circuit diagrams for one bit of each counter component circuit variation: (b) the resistor-biased differential pair, (c) the transistor-biased differential pair, and (d) the gated CMOS.

For the counter component, three circuit variations were created for the SPC1 prototypes. For a given circuit variation, the bits are identical and the circuit diagram for one bit of each variation is shown in Figs. 2.4b to 2.4d. Note that, for the circuit of a given bit, the "out" node is connected to the "in" node of the next bit – and the out node of the last bit is connected to the in node of the first bit. Similarly, where applicable, the "out-bar" node of one bit connects to the "in-bar" node of the next bit – and the out-bar node of the last bit is connected to the in-bar node of the first bit. All circuit variations have a maximum count of 511 (i.e., $2^9 - 1$) since the LFSR circuit has an invalid state when all bits are zero. This invalid state can occur randomly when the array is connected to power and turned on – but the probability that such an event occurs is expected to be

very low (approximately 1 in 512 for a 9-bit counter, assuming an equal probability of a bit powering up in either a high "1" or low "0" state). While methods for preventing this invalid state (such as introducing logic that would force a bit to a high state upon power up) were considered, no solutions were implemented in the prototype arrays.

The differential pair bit designs, one resistor-biased and one transistor-biased (shown in Figs. 2.4b and 2.4c, respectively), were the first two circuit variations created. Compared to the transistor-biased variation, the resistor-biased variation has the advantage of requiring one less wire, which simplifies wire routing. On the other hand, the transistor-biased variation allows for user-controlled fine-tuning of the bias – which may be necessary if TFT variations cause the bits to perform poorly.

During the design process, it was discovered that both differential-pair-based circuit designs are sensitive to TFT variations – specifically, variations in electron and hole mobility. The differential bits employ a self-reinforcing loop to store a value. In order to change the value in the bit, a large amount of current is required to overcome the self-reinforcing loop. If the transistors of the self-reinforcing loop have very high mobility or if the transistors responsible for changing the value of the bit have very low mobility, the current will not be sufficient to override the self-reinforcing loop and change the value.

To overcome this problem, the gated-CMOS design (shown in Fig. 2.4d) was introduced. This design employs a "shutoff" transistor that disables the self-reinforcing loop when changing a value – significantly decreasing the amount of current required.

For the readout of the values stored in the counter, two methods were considered. One method involves externally mimicking comparator output pulses and using those pulses to activate the clock generator component in order to generate clock pulses. This method allows for simpler readout – minimizing the requirements on the timing of the input pulses since the clock generator will "normalize" those inputs and create the correctly timed non-overlapping clock pulses. However, the readout speed would be limited by the speed of the clock generator circuit. The second method – and the one employed for the SPC1 prototypes – involves generating clock pulses externally and using those pulses to directly operate the counter component. Compared to the first method, this method allows readout to be performed as fast as the counter circuit can support, but requires two input wires instead of one. Furthermore, the second method requires the user to carefully construct the clock pulses (i.e., the pulses must be non-overlapping and have a minimum width).

During normal photon counting operation or readout, the pair of clock pulses are used to "increment" the LFSR. When φ_1 is high and φ_2 is low, the value present at the "in" node will be stored in the first "half" of the bit. When φ_1 subsequently changes to low and φ_2 changes to high, the value in the first half of the bit is moved to the second half of the bit. When both clock pulses are low, no values are being shifted. However,

when both clock pulses are high, the value stored in the counter is invalid since both halves of a bit would become conducting – essentially allowing the counter to "increment" itself without correlation to input photons being detected. This scenario will occur if the clock generator component "races" (see Sec. V of this chapter), or if the user inputs malformed clock pulses during readout.

Instead of storing progressive, incremental values (e.g., 1, then 2, then 3, etc.), an LFSR produces pseudo-random numbers. After storing 511 unique, random numbers, the counter begins to repeat the same sequence. This sequence can be computed analytically to generate a look-up table. To use an LFSR as a counter, an initial value must be read out prior to irradiation of the array. After irradiation, the counter is read out again, and the look-up table is used to determine the number of steps that have advanced. However, if more than 511 counts occur during irradiation, there is no way to detect that the LFSR has "looped back" to the beginning – e.g., a count of 1 is indistinguishable from a count of 512. For that reason, the number of bits in the counter must be carefully chosen to be greater than the anticipated number of x-ray interactions during the image frame. Note that each additional bit essentially doubles the maximum number of counts (e.g., from 511 to 1023 to 2047, etc.), but would only result in a small increase in circuit area.

VII. SPC1 prototype array design

The SPC1 prototype arrays have an 8×8 pixel configuration with a pixel pitch of 1 mm. The arrays were fabricated on quartz wafers that could accommodate up to 12 arrays of this size. Note that, since there were 11 unique prototype array designs, one

design was duplicated on each wafer. In addition, numerous test circuits and "helper" circuit elements were also fabricated on each wafer, as summarized in Appendix 2.A.

Table 2.1 shows the circuit variations chosen for each component of each array design. For some array designs, two versions were created – one with a photodiode and one without.

Table 2.1. Summary of the identifier codes (column 1) and circuit variations chosen for each component of the 11 prototype array designs. In the identifier codes, the letter "n" denotes the absence of a photodiode, the "s" denotes a sparse configuration and the "p" denotes a design with an extra probe pad connected to the input of the amplifier. See text for further details.

Array ID	Amplifier	Comparator	Clock-generator	Counter
Pxl2n	3stage-2BP	Schmitt	1SR-5inv-long	TFT-Diff
Pxl3	3stage-2BP	Schmitt	1SR-5inv-long	Res-Diff
Pxl4	3stage-2BP	Diff-pair	1SR-5inv-short	Res-Diff
Pxl5	3stage-2BP	Diff-pair	2SR-3inv	Gated-CMOS
Pxl5s	3stage-2BP	Diff-pair	2SR-3inv	Gated-CMOS
Pxl6	3stage-2BP	Diff-pair	1SR-7inv	Gated-CMOS
Pxl7	3stage-1BP	Diff-pair	2SR-3inv	Gated-CMOS
Pxl7n	3stage-1BP	Diff-pair	2SR-3inv	Gated-CMOS
Pxl8	1stage-1BP	Diff-pair	2SR-3inv	Res-Diff
Pxl8n	1stage-1BP	Diff-pair	2SR-3inv	Res-Diff
Pxl9p	3stage-1BP	Diff-pair	2SR-3inv	Gated-CMOS

The array design that is considered to be the most promising is Pxl5. Two copies of that design were fabricated per wafer. In addition, in order to obtain more detailed empirical measurements, a special version of this design (called Pxl5s) was created. Pxl5s has a pixel configuration similar to a checkerboard where, for a given pixel, neighboring pixels do not have circuits fabricated in them – and are referred to as "circuitless" pixels. Instead, test pads (i.e., metal surfaces designed to be contacted by a probe) are fabricated

inside the circuitless pixels. Those test pads are connected to the inputs and outputs of each component of neighboring, "normal" pixels, as well as intermediate points within select components (such as the output of the first and second stage of the amplifier). These pads allow monitoring of the signal as it propagates through each component of a pixel circuit. In addition, they also allow signal to be injected anywhere in the chain – which enables bypassing of components in case a particular component does not function as expected.

For the array designs incorporating the 1SR-5inv-long clock generator circuit (i.e., Pxl2n and Pxl3), the comparator component was required to be the Schmitt trigger. This design decision was made because the Schmitt trigger, due to hysteresis, outputs wider pulses than the differential pair circuit variation – resulting in pulses that are less likely to trigger the design flaw of the 1SR-5inv-long circuit (as discussed in Sec. V of this chapter). For the 1SR-5inv-short clock generator circuit, the comparator component was chosen to be the differential pair circuit variation – a decision based on the assumption that the "short" variant of the clock generator would be able to accommodate the narrower output pulses of the comparator.

VIII. Summary and discussion

The design process for the SPC1 prototype arrays took ~14 months to complete. During that time, several new simulation methodologies were developed to predict circuit behavior. The results from these simulations were used to identify problems with circuit designs and aided in developing solutions to those problems.

These simulation methodologies represent preliminary frameworks for determining photon counting performance based on poly-Si transistors. While the results of those simulations could be used to *compare* the relative performance between different circuit variations, the simulations are not detailed enough to determine values for metrics such as energy resolution and count rate. The remainder of this dissertation focuses on the subsequent development of these frameworks to include more considerations – such as introducing noise calculations for each transistor or incorporating more realistic incident x-ray spectra – in order to determine values for those metrics.

Finally, empirical characterization of these prototype arrays would provide invaluable information to complement the results determined through simulation. Such characterization will require new hardware and software tools to be developed – such as external peripheral electronics to operate the arrays and scripts to control function generators. Such tools are under development by our group, and empirical characterization of the SPC1 prototype arrays are planned.

Appendix 2.A *– SPC1 test circuits and helper circuit elements*

In order to facilitate empirical characterization of the prototype arrays, a number of test circuits and "helper" circuit elements were fabricated on the same wafers as the arrays. The test circuits are comprised of isolated circuits corresponding to the variations of the four pixel circuit components. These isolated circuits allow straightforward characterization of each variation of each component – without the confounding factors associated with being connected in series to other components.

Since transistors fabricated in close proximity on a wafer should have similar performance, the test circuits for a given component have been organized into "bundles" of variations for that component. This facilitates direct comparison of empirical measurements performed on the different variations of a given component. Figures 2A.1 through 2A.6 show the six bundles fabricated with the SPC1 arrays. Each bundle was duplicated ~100 times per wafer. Note that one of the clock generator circuit variations, 1SR-5inv-short, does not have a test circuit.

In addition to the test circuits, each prototype array is fabricated with a number of "helper" circuit elements that are also designed to aid empirical analysis. Specifically, each array is fabricated with two small sets of individual test transistors (and resistors) located near two corners of the array. Compared to using transistor parameters derived from test transistors located on the periphery of the wafer, parameters extracted from measurements performed on the helper circuit elements of a given array should more

closely match the properties of the transistors located in that array. For this reason, simulations employing parameters obtained from transistors located near an array should yield results that closely align with the empirical performance measured from that array. Moreover, the results of those simulations can be used to guide empirical measurements – for example, by predicting the appropriate values of bias voltage to apply to each component of the pixel circuits.

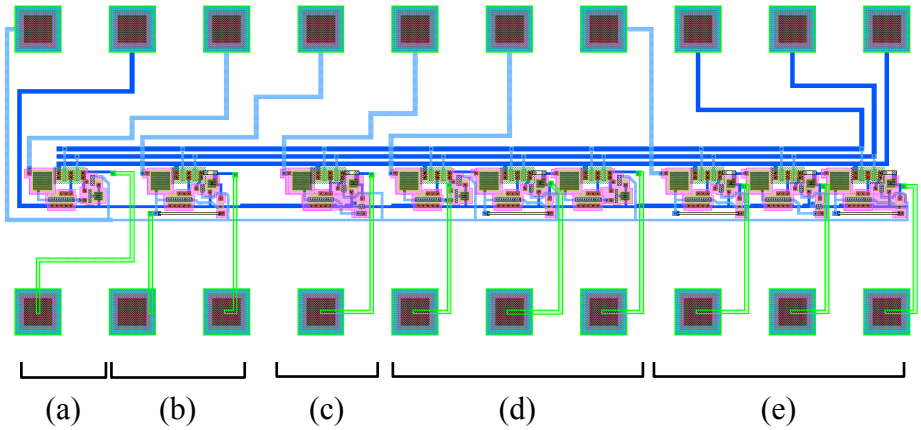


Figure 2A.1. Layout view of the amplifier test circuit bundle. From left to right, the circuits are: (a) a single cutoff stage [named 2T-amp], (b) a single bandpass stage [named 2R-amp], (c) another single cutoff stage [named 1T1R-amp], (d) a 3-stage, 1st order bandpass [named 3st-1bw-amp], and (e) a 3-stage, 2nd order bandpass [named 3st-2bw-amp].

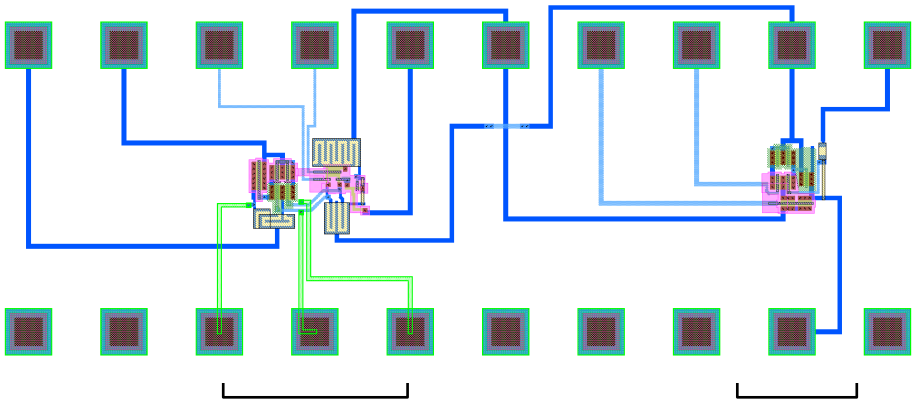


Figure 2A.2. Layout view of the comparator test circuit bundle. From left to right, the circuits are: (a) a differential-pair comparator [named diff-comp] and (b) a Schmitt-trigger comparator [named Schmitt-comp].

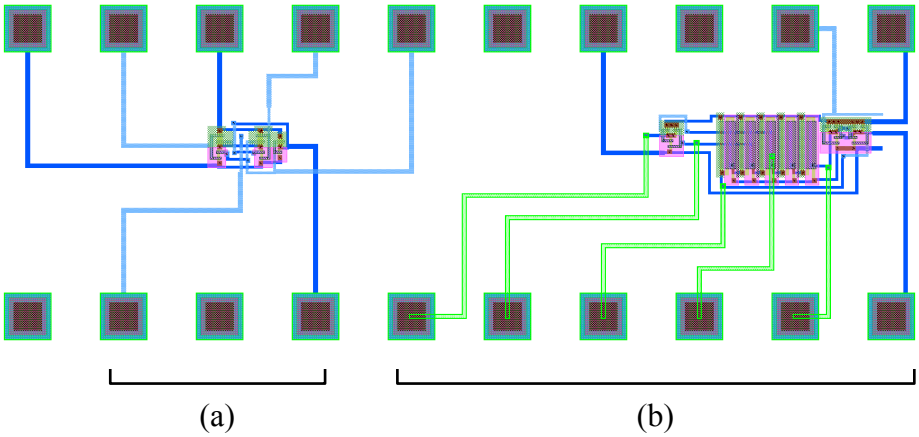


Figure 2A.3. Layout view of the first clock generator test circuit bundle. From left to right, the circuits are: (a) a tri-state buffer [named tri-buffer] and (b) a 1SR-5inv-long circuit [named 1SR-5inv-long].

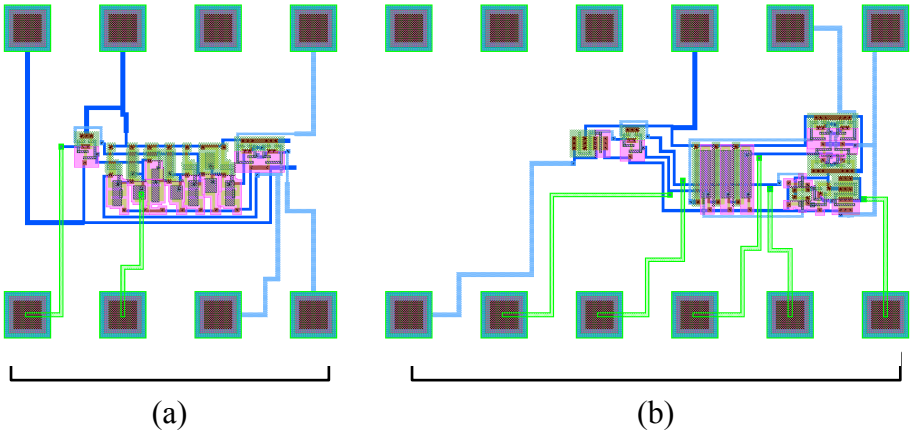


Figure 2A.4. Layout view of the second clock generator test circuit bundle. From left to right, the circuits are: (a) a 1SR-7inv circuit [named 1SR-7inv] and (b) a 2SR-3inv circuit [named 2SR-3inv].

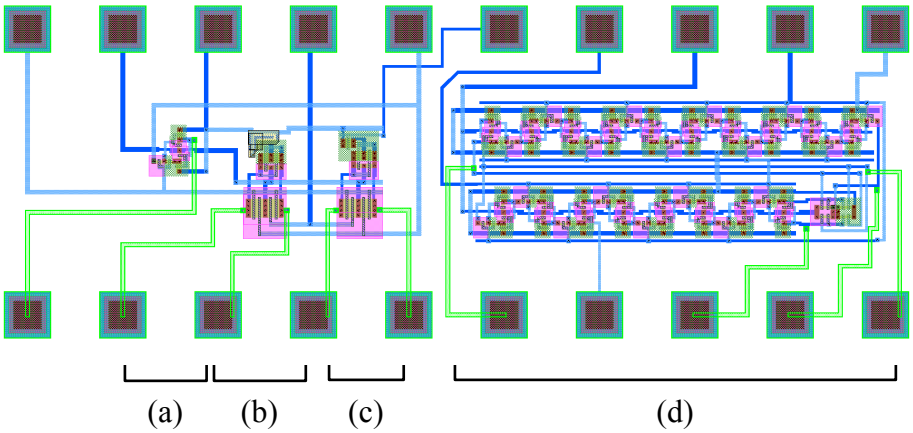


Figure 2A.5. Layout view of the first counter test circuit bundle. From left to right, the circuits are: (a) one bit of the gated CMOS design [named gated-cmos-bit], (b) one bit of the resistor-biased differential pair design [named diff-res-bit], (c) one bit of the transistor-biased differential pair design [named diff-tft-bit], and (d) a 9-bit LFSR based on gated CMOS bits [named gated-cmos-lfsr].

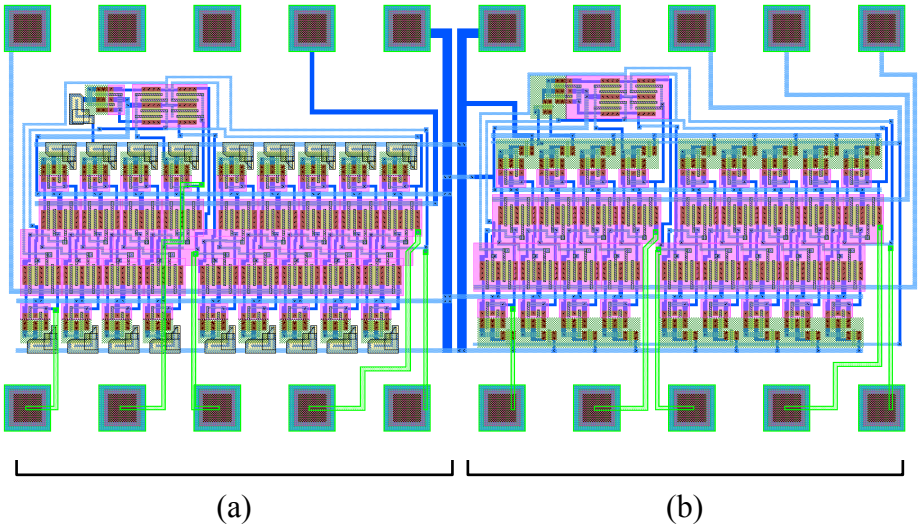


Figure 2A.6. Layout view of the second counter test circuit bundle. From left to right, the circuits are: (a) a 9-bit LFSR based on resistor-biased differential pair bits [named diff-res-lfsr] and (b) a 9-bit LFSR based on transistor-biased differential pair bits [named diff-tft-lfsr].

Appendix 2.B *– Conversion of radiographic exposure to counts/sec/mm^2*

The radiation dose for a chest PA ranges from 40 to 1230 μGy for exposure times ranging from 25 to 450 ms.[43] The median value of the dose was 180 μGy. Assuming this median dose, an exposure time of 100 ms, a conversion factor of 8.3 mR per 72.5 μGy,[44] and a fluence of 262410 x-rays/mm^2/mR,[14] the approximate event rate (in units of counts per second per mm^2, cps/mm^2) incident on a photon counting array for a radiographic image can be calculated as follows:

$$Rate = \frac{180\ \mu Gy \times \frac{8.3\ mR}{72.5\ \mu Gy} \times \frac{262410\ xrays/mm^2}{mR}}{100\ ms} = 12\ Mcps/mm^2 \qquad [2.B1]$$

Chapter 3:

Performance of In-Pixel Circuits for PCAs Based on Poly-Si TFTs

I. Introduction

This chapter describes the development of two simulation frameworks that provide insight into the signal and noise behavior of individual poly-Si TFTs within the photon counting circuits, as well as the impact of variations in TFT performance on overall photon counting performance – information that is not obtainable empirically from prototypes. Results from simulation of each variation of every SPC1 circuit component are reported. In addition, a mathematical model for estimating the pixel pitch of PCAs based on poly-Si is presented.

II. Methods

The four components of the SPC1 prototypes are shown in Fig. 3.1, along with the general shape of the signal input to or output by each component. Depending on the type of signal present at the input and output of the component, each component can be classified as analog or digital, with the comparator component regarded as both since it

has an analog input and a digital output. For this dissertation, the comparator component is considered to be solely in the digital domain.

Two simulation frameworks, an analog framework for simulation of analog components and a digital framework for simulation of digital components, were developed to estimate the performance of each circuit design. These frameworks, implemented using the Eldo SPICE circuit simulator software package (Mentor Graphics, OR), were used to examine intrinsic noise, robustness, and output count rate, and are described in the following sections.

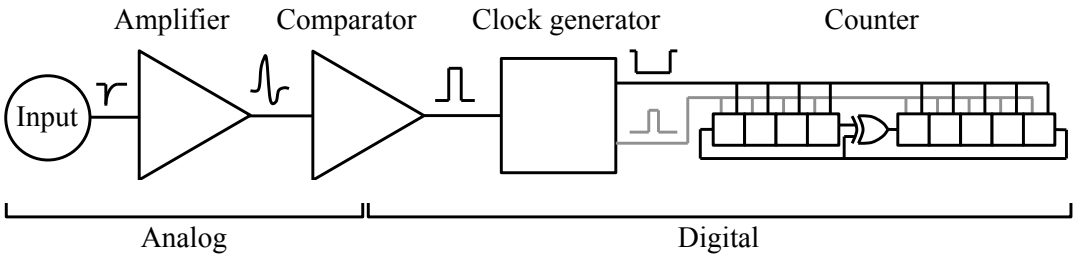


Figure 3.1. Diagram of the four main circuit components of the prototype photon counting pixels: an amplifier, a comparator, a clock generator, and a counter. The waveforms between components schematically illustrate the shape of the signals at that point in the design. The clock generator component has two outputs, denoted by black and grey lines.

In addition to simulating analog and digital performance, a study was conducted to estimate the impact of anticipated advances in processing technology on the pixel pitch of future hypothetical prototypes. To that end, an algorithm was developed to estimate the minimum possible pixel pitch of the current prototype designs as a function of minimum feature size and 3D spatial organization of the circuits.

IIa. Methods - Transistor parameters and noise characteristics

Both simulation frameworks employ version 2 of the RPI poly-Si TFT model [40] for modeling transistor behavior. In order to make the simulations representative of the low-temperature poly-Si material under consideration, transistor model parameter values, including mobility (μ_{00}) and threshold voltage (V_{t0}), were extracted from transfer and output characteristics measured from individual poly-Si TFTs. (Transfer and output characteristics were obtained by measuring channel current as a function of gate voltage and drain-source voltage, respectively.) A set of such parameter values obtained from a single transistor is called a "model card". The transfer and output characteristics obtained from different poly-Si TFTs are not as tightly uniform as those of c-Si transistors, largely due to variations in the dimensions of the crystal grains that are formed during laser-annealing of amorphous silicon to create poly-Si on quartz substrates,[45] as well as variations in unintended channel doping. In particular, such non-uniformity in signal characteristics can be considerable from substrate to substrate and, though more subdued, still non-negligible across a given substrate. In order to examine the effects of such non-uniformity, model cards derived from transistors across many different substrates were used in the digital framework to simulate variations caused by the fabrication process. By comparison, for the case of the analog framework, uniform transistor characteristics were assumed. This involved choosing one n-type transistor and one p-type transistor with favorable values for μ_{00} and V_{t0} as "standard" transistors. The model cards corresponding to these standard transistors were used in the analog framework to simulate the signal and noise performance of amplifier circuits.

TFT noise characteristics were also measured for use in the analog framework. These were obtained by measuring the variations in the channel currents of the standard transistors (sampled at ~4 Hz for 1 hour) for different combinations of drain, source, and gate bias values. At such low frequencies, these variations are mainly due to flicker noise. The channel current variations were then referred to the gate (as voltage variations), converted into a noise power spectral density (using a Fourier transform) and were fit using the following model equation for flicker noise:[41, 42]

$$S_V(f) = \frac{k_f}{C_{ox}^2 WLf} \ . \qquad [3.1]$$

In this equation, $S_V(f)$ is the noise power spectral density, referred to the gate; k_f is the process-dependent flicker noise constant of the transistor; C_{ox} is the gate oxide capacitance (set to 0.345 fF/μm^2 for the devices considered in this study – a value which was derived from processing parameters and material properties); W and L are the width and length, respectively, of the gates of the measured transistor; and f is frequency in Hz. Fits of Eq. 3.1 to the measured $S_V(f)$ spectra were used to determine k_f values. Since the standard model cards were used to simulate every transistor in the amplifier designs, and since each transistor is operated at different gate, drain, and source voltages, channel current for each standard transistor was measured at gate, drain, and source voltage values representative of the range of operating conditions for the amplifier designs. The averages of the k_f values obtained over these operating conditions (referred to as k_{fn} and k_{fp} for the n-type and p-type standard transistors, respectively) were used as parameters to model the noise characteristic of the transistors.

IIb. Methods - Amplifier performance simulations

The analog simulation framework was developed to investigate the amount of intrinsic noise in the amplifier component of the SPC1 arrays. Intrinsic noise refers to the noise generated by the transistors in the circuit – which can affect image quality. This noise was quantified in terms of the ratio of signal to noise (SNR).

In this study, the signal portion of the SNR was chosen to be the maximum change in the output voltage of the amplifier in response to an ~2.44 fC charge injection to an input capacitor – simulated in the frequency domain, from 0.1 Hz to 10 MHz. This injection of charge corresponds to a 70 keV photon interacting with a cadmium zinc telluride (CZT) detector with a work function (i.e., the average amount of energy required to produce an electron-hole pair) of 4.6 eV.[46] (Note that 70 keV happens to correspond to the mean energy of the IEC RQA9 dedicated chest x-ray spectrum.) The input capacitor was assumed to be 1×1 mm^2 with a 500 μm thick [47] dielectric (consisting of CZT) having a relative permittivity of 10. The gain of the amplifier can vary, as discussed below, but an output signal magnitude between 1.25 and 2 V (a range expected to be sufficient to allow good comparator performance) was desired.

The noise portion of SNR was taken to be the intrinsic noise of the amplifier, which was computed as follows. For a given transistor in the circuit design, Eq. 3.1 was used to determine S_V from 0.1 Hz to 10 MHz using the average k_f value derived from the appropriate standard transistor (i.e., k_{fp} or k_{fn}), as well as the W and L for that transistor.

(Note that outside of this frequency range, all transistors were found to have negligible effect on the intrinsic noise of the amplifier.) In order to account for the frequency-dependent gain applied to S_V, the frequency response of the output of the amplifier was determined by applying a small, 1 mV AC input at the gate of that transistor and performing a simulation in the frequency domain, again from 0.1 Hz to 10 MHz. From the simulation results, gain at each frequency was determined by dividing the AC output voltage magnitude of the amplifier by the AC input voltage magnitude. The S_V value at each frequency was weighted with the appropriate gain value, and this weighted S_V curve was integrated over the frequency range. The resulting "transistor noise value" (in units of volts) is the noise contribution of that transistor to the overall amplifier output. This procedure was repeated for every transistor in each amplifier design. The sum in quadrature of the noise values for all the transistors in a design represents the total intrinsic noise (also in units of volts) of that design.

Two amplifier designs were considered in this study. Both designs are 3-stage, folded cascode circuits. The circuit diagrams for the two designs (a 3-stage, 1^{st} order bandpass filter and a 3-stage, 2^{nd} order bandpass filter) are shown in Figs. 3.2a and 3.2b, respectively. The amplifier input was simulated using the circuit shown in Fig. 3.2c and consists of a current source providing the ~2.44 fC input to the capacitor formed by the CZT detector which is in parallel with a 100 MΩ resistor to ground. The circuit diagram for a single folded cascode circuit is shown in Fig. 3.2d. The voltage bias inputs V_{AGC}, V_B, and V_{CG} are used to control the gain and the cutoff frequencies of the amplifier.

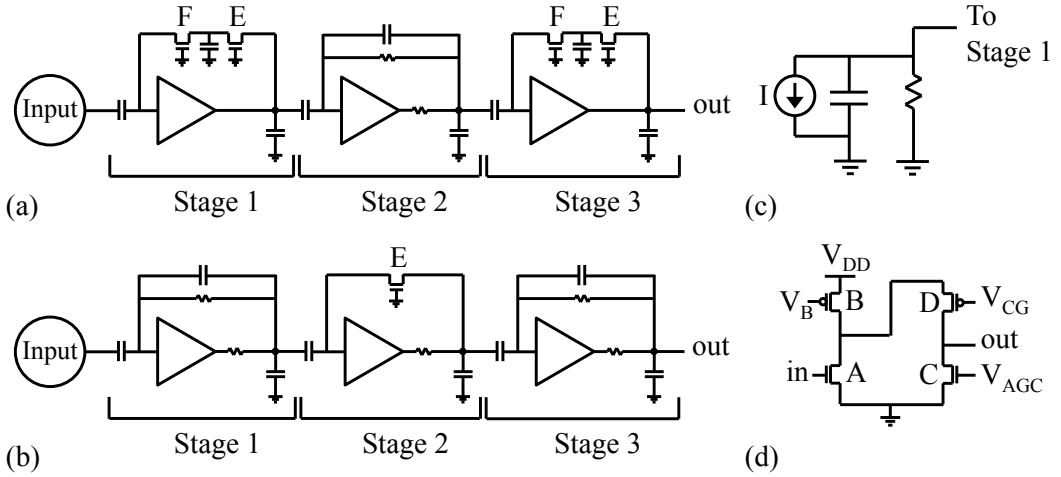


Figure 3.2. Circuit diagrams for the amplifier designs considered in this study: (a) a 3-stage, 1st order bandpass filter design, and (b) a 3-stage, 2nd order bandpass filter design. In these figures: the circles labeled "Input" represent the circuit shown in (c); the triangles are folded cascode circuits, the diagram of which is shown in (d); and the stages are labeled as Stage 1, Stage 2, and Stage 3. Transistors in the folded cascode circuit are labeled A through D, and transistors not related to the folded cascode circuit are labeled E and F.

To determine the most suitable set of voltage bias input values, the analog framework was used to simulate the circuit at various voltage levels for each bias value. V_{AGC} and V_B were varied from 0 to 6 V in 0.1 V steps and 0.25 V steps, respectively. V_{CG} has only a minor effect on gain or bandwidth and was fixed at 0.25 V. V_{DD}, the power rail for the circuit (a notation used for all circuits considered in the study), was fixed at 8 V. An SNR value was calculated for each combination of bias settings and the combination resulting in the highest SNR, while also providing the desired output voltage (i.e., between 1.25 and 2 V), was identified as the best combination. For a given amplifier design, once the best combination was determined, the equivalent input noise of that design (E_{noise}) in units of energy was calculated by dividing the input photon energy E_{in} (i.e., 70 keV) by the resulting SNR value. For each amplifier design, the energy

resolution (ΔE), in terms of the full width at half maximum (FWHM) and expressed as a percentage of the input photon energy, was determined as follows:

$$\Delta E = \frac{E_{noise} \times 2.35}{E_{in}} \times 100\% \,. \qquad [3.2]$$

IIc. Methods – Comparator+clock generator performance simulations

The digital simulation framework was developed to evaluate the performance of the various circuit designs of the digital components, taking into account the effects of non-uniformity in poly-Si TFT signal characteristics caused by the fabrication process (as discussed in Sec. IIa of this chapter). To investigate the effect of such non-uniformity, simulations were performed on circuits that had randomly chosen model cards assigned to every transistor. A circuit with model cards assigned in this way is referred to as a "variation." For each digital component, numerous variations were created for each design for the purpose of scoring and ranking the designs by their "robustness" – defined as the percentage of variations meeting certain select criteria (detailed in Secs. IIIc and IIId of this chapter). Circuits with higher scores are expected to exhibit superior ability to meet the criteria – thereby reflecting better tolerance to TFT non-uniformities.

The comparator and clock generator components were simulated together to take into account their interdependencies. The four combinations of comparator+clock generator components employed in the SPC1 prototype arrays are summarized in Table 3.1 and all those combinations were examined in the study. For each combination, a total of 200 variations were created. The circuit diagrams of the two comparator designs are shown in Fig. 3.3. In the figure, V_{B1} is a bias input and V_T is the threshold

voltage level. The circuit diagrams for the four clock generator designs are shown in Fig. 3.4, with the two configurations of the 5-inverter design (referred to as long-delay and short-delay in Table 3.1) represented by the circuit diagram in Fig. 3.4a.

Table 3.1. Combinations of comparator and clock generator designs examined in the study. Each design pair is employed in the corresponding SPC1 arrays (described in more detail in reference 36) indicated in the last column.

Design ID	Comparator design	Clock generator design	Used in SPC1 Array
5inv-long	Schmitt trigger	1 SR + 5-inverter (long-delay)	Pxl2, Pxl3
5inv-short	Differential pair	1 SR + 5-inverter (short-delay)	Pxl4
7inv	Differential pair	1 SR + 7-inverter	Pxl6
3inv-2SR	Differential pair	2 SR + 3-inverter	Pxl5, Pxl7, Pxl8, Pxl9

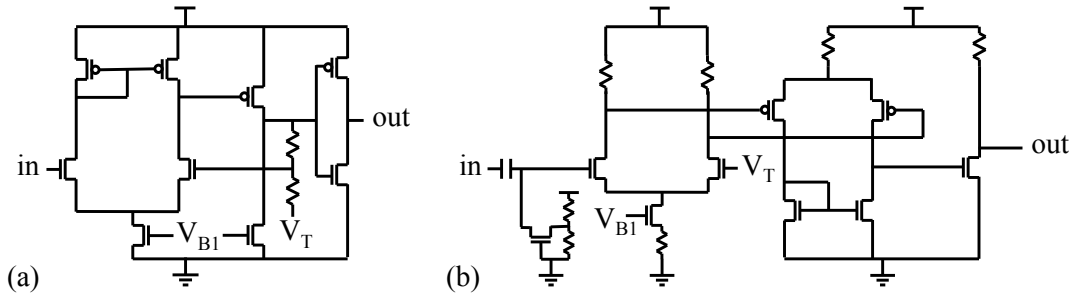


Figure 3.3. Circuit diagrams for the comparator designs considered in this study: (a) a Schmitt trigger design, and (b) a differential pair design. For both designs, two adjustable nodes, V_{B1} (bias) and V_T (threshold), are labeled.

For the simulation of the variations of these four combinations, the input consisted of a train of square input pulses parameterized by a variable, t_{min}. For each variation, a three-dimensional sweep of V_{B1} and V_T voltage levels, and t_{min} time values was simulated to investigate the performance of that variation over a wide range of operating conditions. The V_{B1} levels ranged from 0 to 6 V in 0.5 V steps; the V_T levels ranged from 3 to 5 V in 1 V steps; and t_{min} had values of 10, 32, 100, 316, 1000, 3162,

and 10000 ns – which, with 200 variations, resulted in a total of 54,600 simulations for each combination. For each of the 7 values of t_{min}, the width of each pulse and the time between pulses was assigned a random multiple of that value – resulting in 7 different input pulse trains.

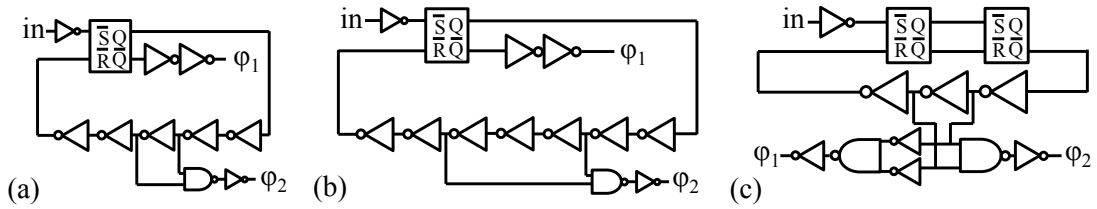


Figure 3.4. Circuit diagrams for the clock generator designs considered in this study: (a) a 1 SR + 5-inverter design (corresponding to two configurations: long-delay and short-delay), (b) a 1 SR + 7-inverter design, and (c) a 2 SR + 3-inverter design. In the diagram, the rectangles represent 2-NAND-gate-based SR (i.e., set-reset) latches; the combined triangle-and-bubble symbols represent inverter stages; and the combined plug-shape-and-bubble symbols represent NAND gates. The outputs of the clock generator are denoted as φ_1 and φ_2.

IId. Methods - Counter performance simulations

The counter architecture implemented in the SPC1 prototype arrays is a 9-bit, maximum-length linear feedback shift register (LFSR) operated by a two-phase clock. This LFSR is a pseudorandom counter with 511 unique states. A two-phase clock "cycle" is used to increment the counter by one step. After advancing 511 steps from a given starting point, the counter "loops" back to that starting value. Three different counter designs were implemented in the SPC1 prototype arrays and a schematic circuit diagram of one bit of each design is shown in Fig. 3.5.

The counter component was also evaluated with the digital framework. Similar to the comparator+clock generator simulations, 200 variations of each counter design were

simulated. Unlike the comparator+clock generator simulations which had 3 input variables, the counter simulations only had a single dependency: the two-phase clock. Thus, all variations of the counter component were evaluated by changing the timing of this clock.

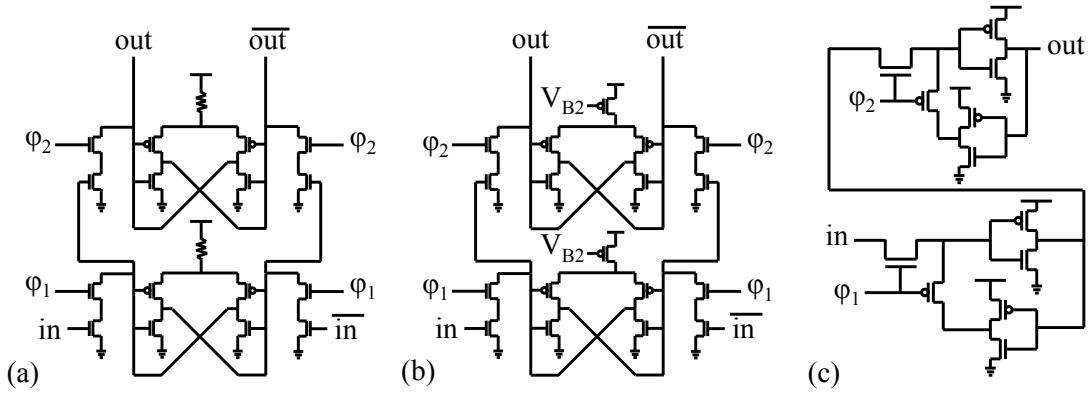


Figure 3.5. Circuit diagrams for one bit of each of the counter designs considered in this study: (a) a differential-pair with resistive load design (referred to as Differential-Res), (b) a differential-pair with transistor load design (referred to as Differential-TFT), and (c) a gated-CMOS design. The symbols φ_1 and φ_2 indicate inputs provided by the preceding clock generator component. The bias voltage V_{B2} was set to 4 V.

Each variation was simulated for a minimum of 511 clock cycles, corresponding to at least one full loop of the counter. Each two-phase clock cycle consisted of non-overlapping clock pulses on two different inputs, labeled as φ_1 and φ_2 in Fig. 3.5. For example, for a given clock cycle duration of 1000 ns (corresponding to a count rate of 1 MHz), φ_1 will be high for 375 ns, then it will be low for the remaining 625 ns; φ_2 will be low for the first 500 ns, then high for 375 ns, then low for the remaining 125 ns. Count rates of 0.1, 0.25, 0.5, 1, 2, and 3 MHz were simulated.

IIe. Methods – Minimum pixel pitch calculations

The SPC1 prototype arrays were designed and fabricated using a minimum feature size of 6 μm, which defines the smallest transistor gate dimension allowed in the

design. The fabrication process employed 4 metal layers, a-Si:H-based resistors, and a 100 nm thick SiO_2 gate dielectric that was also used to form capacitors. The pixels are arranged in a quad format with a group of 4 pixels sharing common wires (e.g., bias and power lines). To facilitate common wire routing to peripheral electronic pads, a 1 mm pixel pitch was employed for all SPC1 arrays, resulting in the layouts of the circuits of each design not fully utilizing the 1 mm^2 pixel area.

In order to estimate the minimum pitch achievable for a given SPC1 array design, an algorithm was developed to calculate the area occupied by circuit elements such as transistors, resistors, and capacitors in each component, as well as the area occupied by the common wires. In the algorithm, the occupied area for each transistor is estimated to be 9 times the gate area (defined as the product of W and L) of that transistor in order to account for source and drain contacts, as well as for spacing between other elements. Next, the area occupied by capacitors and resistors is multiplied by 2 and 3, respectively, to account for spacing between other elements. The larger factor of increase used for resistors compared to that used for capacitors is due to consideration of the oblong shape of resistors (which increases the perimeter of the element) as opposed to the more square-like layout of the capacitors employed in the designs. Finally, the area occupied by common wires (which is estimated to be 0.25 mm^2 for the SPC1 designs) was assumed to be dependent on the number of metal layers but independent of minimum feature size. The minimum pixel pitch is given by the square root of the total circuit area (corresponding to the sum of the areas of the transistors, capacitors, resistors, and common wires) computed by the algorithm.

Two pixel designs were considered – one with the largest component area (corresponding to Pxl3) and one with the smallest component area (corresponding to Pxl5). Microphotographs corresponding to each design are shown in Fig. 3.6. A decrease in pixel pitch was explored by employing three strategies: eliminating unoccupied pixel area, reducing the minimum feature size, and increasing the number of metal layers used in the fabrication process. Eliminating unoccupied pixel area involved excluding areas where no circuits were fabricated from the overall pixel pitch determination. Reducing minimum feature size, which is assumed to only affect the area occupied by transistors and resistors, involved shrinking that design rule from 6 μm down to 3 μm and then to 1 μm. However, instead of assuming a quadratic decrease in occupied area (which would be the consequence of reducing, for example, both the width and length of the transistors), a linear reduction was assumed to approximately account for non-shrinking elements, such as inter-layer contacts (i.e., vias), and source and drain contacts for the TFTs. Finally, 4 additional metal layers were introduced in the fabrication process to allow the area required for the common wires to be distributed over more planes.

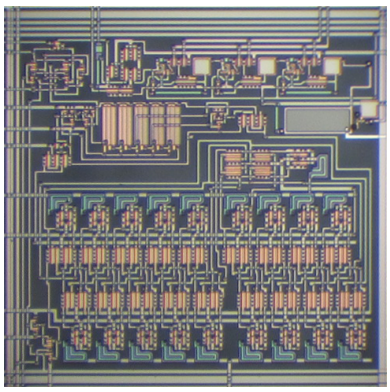
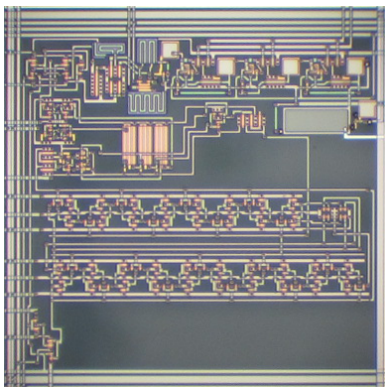
(a)  (b) 

Figure 3.6. Microphotographs of a single pixel from (a) the Pxl3 array with 229 transistors, 9 capacitors, and 26 resistors and (b) the Pxl5 array with 197 transistors, 11 capacitors, and 12 resistors.

III. Results

IIIa. Results - Transistor parameters and noise characteristics

Transfer and output characteristics were measured from approximately 320 individual poly-Si transistors sampled from 20 substrates. From that data set, a total of 16 transistors (8 n-type and 8 p-type) with threshold voltages approximately equally spaced between -0.3 and 1 V (for n-type) or 0 and -1 V (for p-type) were selected. Transfer characteristics from these transistors are plotted in Fig. 3.7, after normalization by the W-to-L ratio of each transistor.[42] The spread observed in the data illustrates the effect of process variations during fabrication (e.g., due to laser-annealing or doping).

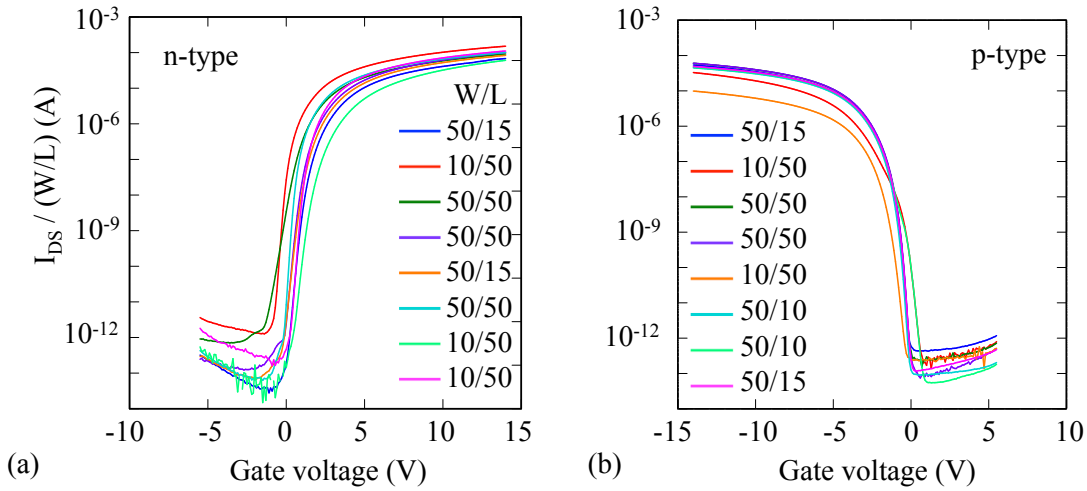


Figure 3.7. Normalized transfer characteristics measured from (a) 8 n-type and (b) 8 p-type poly-Si TFTs. The legend indicates the dimensions of W and L, in μm, for the individual transistors.

From the unnormalized transistor measurement results, a total of 16 model cards were created. For these cards, the minimum and maximum values of mobility and threshold voltage are summarized in Table 3.2 – along with the corresponding values for the standard n-type and p-type transistors. Separately, from noise power spectra obtained from channel current measurements, the average values for k_f in Eq. 3.1 for the n-type and p-type transistors, k_{fn} and k_{fp}, were determined to be 4.5×10^{-25} and 7.6×10^{-25} C^2/m^2, respectively.

Table 3.2. Minimum and maximum mobility (μ_{00}) and threshold voltage (V_{t0}) values for the 8 n-type and 8 p-type transistor model cards. The values for the standard transistor model cards are also shown.

Parameter	*n-type*			*p-type*		
	min	**standard**	**max**	**min**	**standard**	**max**
μ_{00} (cm^2/V-s)	89.2	134.5	178.6	46.5	78.1	78.4
V_{t0} (V)	-0.26	0.35	0.96	-0.80	-0.47	-0.19

IIIb. Results – Amplifier performance simulations

Figure 3.8 shows the simulation results for output signal, intrinsic noise, and SNR as a function of V_{AGC} and V_B for the two amplifier designs considered in the study. Figures 3.8a and 3.8d show that there are regions where amplifier output signal increases quickly, as illustrated by the sharp transition between the blue and the dark-red regions. Figures 3.8b and 3.8e show that intrinsic noise is highest when the corresponding output signal is highest. Finally, Figs. 3.8c and 3.8f indicate that the SNR is highest where output signal is only moderately high.

In Fig. 3.8, the "plus" and "cross" symbols superimposed upon the plots denote the best combination of V_{AGC} and V_B bias settings – i.e., the one that provides the highest SNR, while also providing the desired output signal (i.e., between 1.25 and 2 V). That best combination for the 3-stage, 1^{st} order bandpass design and the 3-stage, 2^{nd} order bandpass design is (V_{AGC}=2.3 V, V_B=2.00 V) and (V_{AGC}=3.9 V, V_B=1.75 V), respectively.

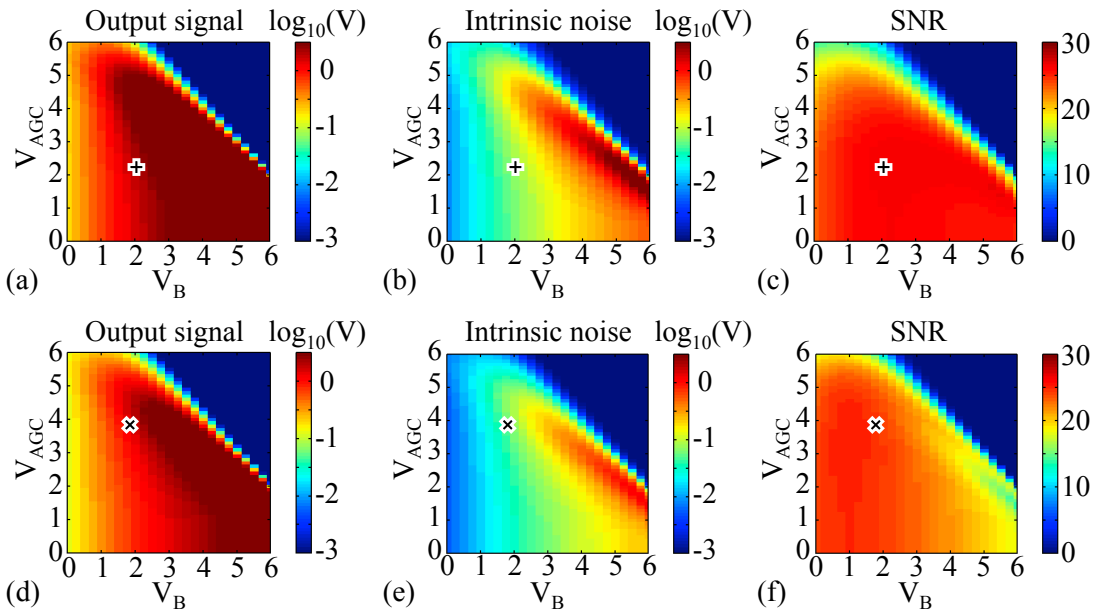


Figure 3.8. Results for (a) output signal, (b) intrinsic noise, and (c) SNR for the 3-stage, 1st order bandpass amplifier plotted as a function of V_{AGC} and V_B – with the best combination indicated by the superimposed "plus" symbol. (d), (e), and (f) show the corresponding signal, noise, and SNR results for the 3-stage, 2nd order bandpass amplifier – with the best combination indicated by the "cross" symbol. For each plot, the color bar to the right denotes the scale. Note that output signal and intrinsic noise are plotted on a logarithmic scale while SNR is plotted on a linear scale.

For each amplifier design at its best combination of bias settings, transistor noise values for each TFT (referred to the output of the amplifier) are given in Fig. 3.9. From the figure, for each stage of each design, transistors A and B are seen to contribute more noise than the other transistors. Furthermore, transistors in the earlier stages generally contribute greater noise than their counterparts in later stages – a consequence of the noise being magnified through the remainder of the amplifier chain.

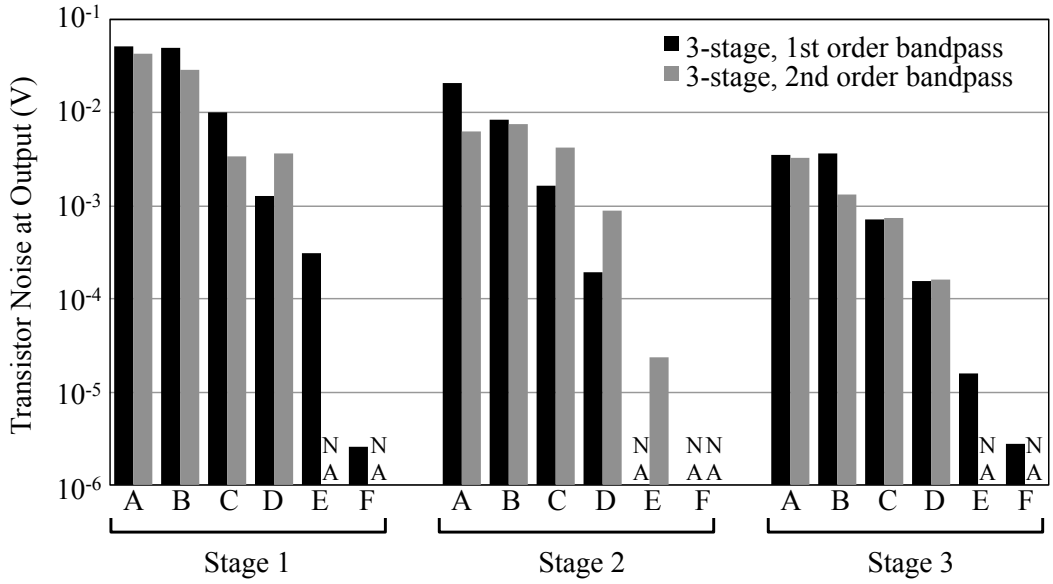


Figure 3.9. Noise values, referred to the output of the amplifier, for each transistor in the 3-stage, 1st order bandpass and 3-stage, 2nd order bandpass amplifier designs, indicated by the black and grey bars, respectively. The transistor results are grouped by stage. In each stage, the letters A through F correspond to the transistors appearing in Fig. 3.2. Finally, the use of the notation "NA" in place of a black or grey bar indicates the absence of that transistor in a given stage of a design.

Table 3.3 summarizes the simulation results for the two amplifier designs operated at their respective best combination of bias settings. For the 3-stage, 1st order bandpass design, the output signal was 1.99 V and the total intrinsic noise was 75.1 mV, which corresponds to an SNR of 26.5. For this design, the equivalent noise of the design in units of energy was 2.64 keV – resulting in an energy resolution of 8.9% FWHM at 70 keV. For the 3-stage, 2nd order bandpass design, the output signal was 1.29 V, and the intrinsic noise was 52.5 mV, which corresponds to an SNR of 24.6. For this design, the equivalent noise was 2.85 keV – resulting in an energy resolution of 9.6% FWHM at 70 keV. The energy resolution of the SPC1 amplifier designs is comparable to those reported for c-Si PCAs.[26, 48]

Table 3.3. Simulation results for output signal, total intrinsic noise, SNR, equivalent noise, and energy resolution corresponding to a 70 keV incident photon for each amplifier design using the best combination of V_{AGC} and V_B indicated in Fig. 3.8. Note that, for each design, the intrinsic noise values correspond to the sum in quadrature of the noise values of the individual transistors given in Fig. 3.9.

	3 stage, 1st order bandpass	3 stage, 2nd order bandpass
Output signal	1.99 V	1.29 V
Total intrinsic noise [rms]	75.1 mV	52.5 mV
SNR	26.5	24.6
E_{noise}	2.64 keV	2.85 keV
ΔE (FWHM)	8.9%	9.6%

IIIc. Results – Comparator+clock generator performance simulations

For the comparator+clock generator simulations, the waveforms of the input to the comparator ($comp_{in}$) and expected outputs from the clock generator (φ_1 and φ_2) are illustrated in Fig. 3.10. The figure also illustrates the four timing parameters used to characterize the timing behavior of each output pulse of a simulation: t_{phi1}, t_{phi2}, t_{edge1}, and t_{edge2}. t_{phi1} and t_{phi2} are defined as the time intervals during which φ_1 and φ_2 exceed 80% of V_{DD}, respectively. t_{edge1} is the time interval defined between φ_1 dropping below 20% of V_{DD} and φ_2 exceeding the same 20% threshold. t_{edge2} is the time interval defined between φ_2 dropping below 20% of V_{DD} and φ_1 exceeding the same 20% threshold.

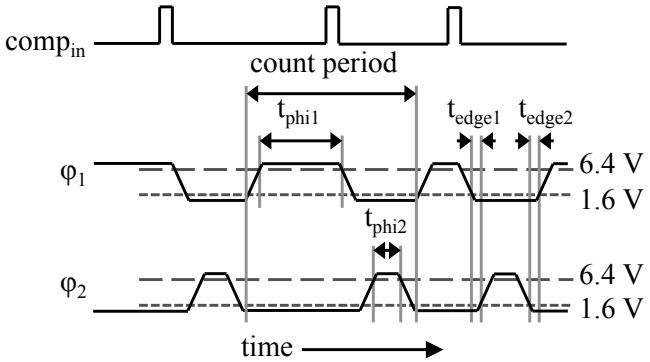


Figure 3.10. Illustrations of the waveforms input to the comparator component ($comp_{in}$) and output from the clock generator component (φ_1 and φ_2). Each pulse appearing in the $comp_{in}$ waveform corresponds to an event triggered by one X ray interacting with the detector. In the simulation, the input pulses swing between ground (0 V) and V_{DD} (8 V). The short-dashed and long-dashed horizontal lines represent 20% (1.6 V) and 80% (6.4 V) of V_{DD}, respectively, and are used to evaluate the φ_1 and φ_2 waveforms. Superimposed on the figure are labels for the timing parameters (t_{phi1}, t_{phi2}, t_{edge1}, and t_{edge2}) and count period used for evaluation of the variations.

In order to determine the performance of the four comparator+clock generator designs, the output from a simulation was required to meet the following four timing requirements: all t_{phi1} and t_{phi2} have values of 375 ns or greater, and all t_{edge1} and t_{edge2} have values of 125 ns or greater. (Note that this combination of timing requirements corresponds to a maximum input count rate to the subsequent counter component of 1 MHz.) For each pairing of one of the 200 variations and one of the 7 values of t_{min}, the 39 simulations performed for that pairing (corresponding to all combinations of V_{B1} and V_T values) were considered a "cohort". Each cohort was considered successful if it met two conditions: (i) at least one simulation of the cohort met the four timing requirements, and (ii) all of the simulations in the cohort that did not meet those requirements did so because neither φ_1 nor φ_2 ever exhibited a voltage between the 20% and 80% thresholds (an outcome referred to as a "no-swing"). Thus, even if only a single simulation in a cohort failed to meet the timing requirements, this was interpreted to mean that the cohort was not successful – since such behavior can result in unpredictable behavior of the

counter component. (On the other hand, a no-swing outcome would not have such an effect upon the counter. Of course, if every simulation in a cohort resulted in a no-swing outcome, then the cohort was considered to have failed since the counter would never be incremented.) The percentage of all 1400 cohorts for each design that were successful is defined as the robustness and is shown in Fig. 3.11a. The results indicate that the 5inv-long and the 3inv-2SR designs exhibited the lowest and highest robustness, respectively, while the 5inv-short and 7inv designs demonstrated nearly identical robustness.

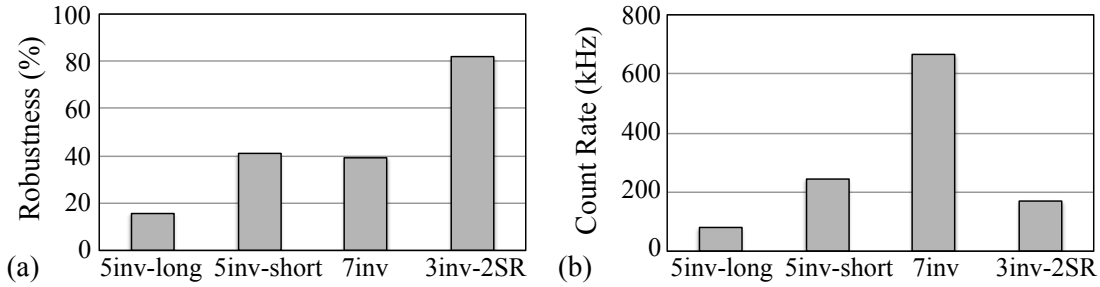


Figure 3.11. Simulation results for the four comparator and clock generator design combinations listed in Table 3.1: (a) robustness, and (b) maximum count rate obtained for each design. See text for further details.

For each simulation that passed all four timing requirements, a count rate was derived by taking the inverse of the shortest count period in the output of that simulation – defined as the time interval from the beginning of one φ_1 to the beginning of the next φ_1, as illustrated in Fig. 3.10. A maximum output count rate was established for each design based on the fastest variation of that design – resulting in rates of ~80, 250, 650, and 175 kHz for the 5inv-long, 5inv-short, 7inv, and 3inv-2SR designs, respectively, as illustrated in Fig. 3.11b.

As seen in Fig. 3.11, the first three designs (i.e., 5inv-long, 5inv-short, and 7inv) have much lower robustness compared to the 3inv-2SR design, and exhibit a wide range of maximum output count rates. This lower robustness can be largely attributed to the single SR-latch circuit architecture common to all three designs that, under certain combinations of t_{min} and model cards, can produce overlapping φ_1 and φ_2 pulses that result in violation of one or more of the four timing requirements. The wide range of maximum count rates can be attributed to the specific W-to-L ratios employed for the transistors in each of the three designs. For the 3inv-2SR design, the maximum count rate could be considerably increased (conceivably by an order of magnitude, or more) by modifying the W-to-L ratios in that design – without significantly affecting the favorably high robustness demonstrated in Fig. 3.11a since this design employs a circuit architecture (i.e., the dual SR-latch) which circumvents the possibility of generating overlapping pulses.

IIId. Results - Counter performance simulations

In the study, a counter variation was considered to be successful if it cycled through all 511 unique states before "looping" back to the starting state and repeating. For each counter design at each count rate, the number of successful variations divided by the total number of variations simulated (i.e., 200) is defined as the robustness.

Table 3.4 shows robustness as a function of count rate for the three counter designs. The Differential-Res and Differential-TFT designs are seen to demonstrate good robustness (i.e., above 90%) up to 1 MHz. Above 1 MHz, robustness for these designs

falls off sharply – a result of how the bits of the designs change their stored values. For both designs, a value is stored within the bit by means of a self-reinforcing feedback loop and, in order to change the value of a bit, a certain amount of time is needed in order to overcome this feedback loop and store a new value. The amount of time required to store a new value depends on the quality of the TFTs in the circuit, which is affected by TFT variations. For example, a counter bit comprised of low-mobility TFTs will require a longer time in order to store a new value – resulting in increasing likelihood for that counter to fail at higher count rates.

The gated-CMOS design, on the other hand, demonstrates good robustness across the entire range of simulated count rates. This design also employs a self-reinforcing feedback loop in order to store a value, but a gating transistor is used to disconnect the feedback loop when storing a new value – greatly decreasing the time needed to store a new value and thus making the design more tolerant of TFT variations at higher count rates.

Table 3.4. Robustness results from simulation of the three counter designs shown in Fig. 3.5 as a function of count rate.

Count rate (MHz)	**0.1**	**0.25**	**0.5**	**1**	**2**	**3**
Differential-Res	97%	97%	96.5%	92.5%	4%	0%
Differential-TFT	100%	100%	100%	99.5%	72.5%	33%
Gated-CMOS	100%	100%	100%	100%	100%	94%

IIIe. Results - Minimum pixel pitch calculations

In Fig. 3.12, the minimum pixel pitch and total circuit area of the components and common wires for the circuit designs of the Pxl3 and Pxl5 prototypes are shown as a function of conceivable, progressive improvement in the layout and fabrication of poly-Si PCAs. In the figure, the improvement labeled Im1 corresponds to the original design specifications of the prototypes (i.e., a minimum feature size of 6 μm and 4 metal layers), but with unoccupied pixel area excluded. Under these conditions, the circuit designs of Pxl3 and Pxl5 would have pixel pitches of ~835 and 672 μm, respectively. Im2 corresponds to a reduction in minimum feature size to 3 μm – resulting in pixel pitches of ~693 and 598 μm for Pxl3 and Pxl5. Im3 corresponds to a further reduction in minimum feature size to 1 μm – resulting in pixel pitches of ~578 and 544 μm for Pxl3 and Pxl5. From these results, it is apparent that decreasing minimum feature size provides diminishing benefit, and the area occupied by common wires becomes the dominant factor in determining minimum pixel pitch. Accordingly, increasing the number of metal layers from 4 to 8 (corresponding to Im4) reduces pixel pitch to ~290 and 243 μm for Pxl3 and Pxl5.

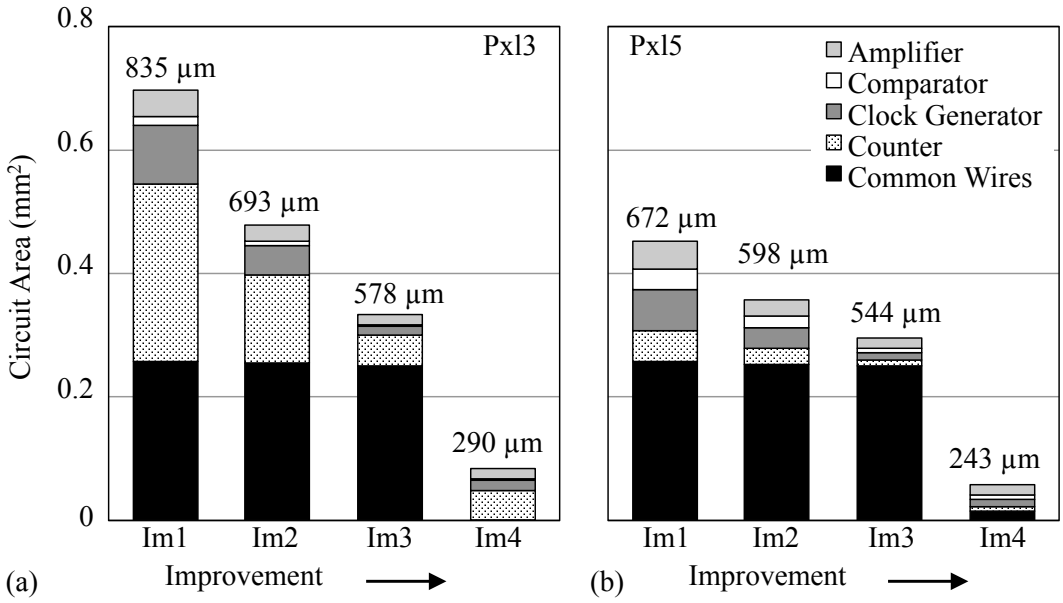


Figure 3.12. Bar graph illustrating the total circuit area for the circuit designs of the (a) Pxl3 and (b) Pxl5 prototypes as a function of progressive improvement in the layout and fabrication of these designs – as detailed in the main text. For each bar, the areas occupied by the amplifier, comparator, clock generator, and counter components, as well as the common wires, are indicated by different shadings. The number appearing above each bar is the pixel pitch corresponding to the total circuit area.

IV. Discussion

In this study, simulation modeling has been used to examine the potential performance of prototype PCAs based on large-area poly-Si TFT process technology. The frameworks employed in the study enable examination of the influence of individual transistors within photon counting circuits on circuit performance (a level of detail that is not normally accessible through empirical measurement) and provide insight into how the circuits can be improved. From the results of this study, a number of interesting observations can be made.

The analog simulation framework employed frequency-domain simulations (to determine signal and noise) in order to calculate SNR values for the amplifier designs.

A more precise, but also more computationally intensive, determination of SNR could be achieved by means of time-domain simulations for signal and noise, while also utilizing a more advanced poly-Si transistor noise model that scales the noise depending on the operating condition of each transistor (whereas the current study utilized averaged k_f values derived from a range of operating conditions).

For the digital simulation framework, the methodology adopted for this study helps to identify those designs that best cope with non-uniformities in poly-Si TFT signal characteristics from substrate to substrate – as well as help to minimize the number of pixels on a given substrate which do not meet specified criteria. While the present study was limited to an examination of component circuits corresponding to recently fabricated prototypes, the methodology can be used to guide development of new circuit designs that meet even more demanding criteria (e.g., higher output count rates for the comparator+clock generator) while maintaining a high degree of robustness.

In order for a PCA to be clinically practical for diagnostic imaging, the pixels would be required to handle input x-ray count rates (in units of mega-counts per second per mm^2) on the order of 1 to 50 Mcps/mm^2.[43] By comparison, PCAs based on c-Si have reported maximum count rate capabilities ranging from 1 to 600 Mcps/mm^2.[35] Given that the minimum pixel pitch predicted in this study is on the order of 250 μm, the expected input x-ray count rates for such a pixel size would be ~0.06 to 3.1 Mcps (i.e., one-sixteenth of the estimated rates per mm^2 cited above). In an array, since the maximum count rate capability per pixel is generally limited by that of the slowest component, it

was of interest in the current study to examine the maximum count rates (expressed in units of MHz) of individual components of the SPC1 PCA circuit. The count rates for the designs exhibiting the highest robustness were ~0.175 and 3 MHz for the comparator+clock generator (3inv-2SR) and counter (gated-CMOS) components, respectively. (The count rates of the amplifier designs were not evaluated in this study.) While these count rates compare favorably with the expected input x-ray count rates, the comparator+clock generator components would limit the maximum count rate for the overall pixel. However, given that the circuits evaluated in this chapter only represent initial poly-Si designs, it is strongly anticipated that higher rates can be achieved while maintaining high robustness.

Given the large number of circuit elements in a PCA design, pixel pitch can be minimized, to a degree, through judicious choice of circuit designs without detrimental effect on performance. For example, the Pxl5 design not only allows a smaller pixel pitch compared to Pxl3, its comparator+clock generator and counter components were identified as those with the highest robustness (and, in the case of the counter, the highest count rate as well). Further reduction in pixel pitch can be obtained through improvement in the poly-Si fabrication technology. The minimum pixel pitch estimates reported in this study were based on published and/or conceivable improvements in that technology. Of the 3 process-related improvements investigated, both an increase in the number of metal layers from 4 to 8 and a reduction in minimum feature size from 6 to 3 μm are readily achievable with current fabrication techniques – while employing a 1 μm minimum feature size is not commercially available at this time, but may be in the

future. Reduced pixel pitch can also be achieved by redesigning circuits (to better optimize their layouts or to decrease the number of transistors) or by reducing the number of common wires needed to operate the array (for example, through introduction of multiplexing).

The results of this initial study of the theoretical performance of the pixel circuit components used in the first prototype PCAs based on poly-Si TFTs are encouraging. We anticipate that such information, along with results obtained from empirical characterizations of the SPC1 PCAs, will form a starting point for future optimization of poly-Si based PCAs exhibiting higher robustness, increased count rate, and smaller pitch.

Chapter 4:

Count Rate Capabilities of In-Pixel Amplifiers for PCAs Based on Poly-Si TFTs

I. Introduction

In Chapter 3, while the count rates of the latter three pixel circuit components (i.e., the comparator, clock generator, and counter) were determined to be sufficient for radiographic and fluoroscopic procedures, the count rate of the amplifier component was not examined. The amplifier, however, is of definite interest since, as the first component in the signal chain, the degree to which its count rate performance can be maximized influences design decisions affecting subsequent pixel circuit components.

In the present study, the count rate capabilities of amplifiers suitable for PCA pixel circuits, based on poly-Si TFTs, are investigated. To this end, circuit simulation was used to estimate count rate for amplifier circuits in photon counting pixels and used to explore the effects of a wide range of circuit design variables on amplifier count rate.

II. Methods

IIa. Overview

Circuit simulations were performed to examine the count rate performance of the amplifier circuit designs incorporated in the pixels of the previously mentioned prototype poly-Si photon counting arrays.[36] In addition, hypothetical variations of those prototype amplifier designs that provide higher count rates, while maintaining or improving signal gain, linearity of signal response and energy resolution, were identified and investigated.

The simulations employed the Eldo SPICE circuit simulation software package (Mentor Graphics, OR). In the simulations, the transistors were modeled using version 2 of the RPI poly-Si TFT model [40] and, to make the results representative of the properties of low-temperature poly-Si, the model card parameters required for the TFT model were the same empirically-determined values used in Chapter 3.[38]

In the present study, each signal input to an amplifier circuit was assumed to be generated by an X ray depositing all of its energy in a direct detection x-ray converter in the form of a 500 μm thick cadmium zinc telluride (CZT) detector.[38] The energy distribution of these X rays was assumed to take one of three forms: 70 keV monoenergetic X rays, 1 to 200 keV monoenergetic X rays, and X rays corresponding to an RQA5 spectrum in IEC 1267. Each signal input to the amplifier circuit took the form of an *input pulse* with a height corresponding to an x-ray energy sampled from one of these distributions – resulting in the generation of an *amplifier output response*.

IIb. Determination of Energy Resolution

Energy resolution for a given amplifier circuit design was calculated from the ratio of the amplifier output response to the intrinsic noise associated with the TFTs present in that circuit. Following the methodology of Chapter 3, the noise contribution from each TFT was obtained through simulations (performed in the frequency domain) employing the following equation for the noise power spectral density associated with TFT flicker noise:

$$S_{v-flicker}(f) = \frac{k_f}{C_{ox}^2 WLf} . \qquad (V^2/Hz) \qquad [4.1]$$

In this equation, k_f is the flicker noise constant (empirically determined to be 4.5×10^{-25} and 7.6×10^{-25} C^2/m^2 for n-type and p-type TFTs, respectively), C_{ox} is the gate oxide capacitance (0.345 $fF/\mu m^2$), W and L are the width and length dimensions of the TFT gate, and *f* is frequency in Hz.[38]

The amplifier output response used in the calculation of energy resolution was the signal response of the amplifier circuit to an input pulse corresponding to a 70 keV X ray. Circuit simulations of signal response were performed in the temporal domain – as described in the next section.

IIc. Determination of Count Rate

In Chapter 3, the signal response of the amplifier was examined via circuit simulations performed in the frequency domain. However, detailed investigation of the count rate performance of amplifier circuit designs necessitates examination of signal response over time. For that reason, all simulations of signal response in this study were

performed in the temporal domain using the adaptive time step feature of the Eldo package. In order to quantify the count rate capabilities for a given amplifier circuit, trains of pulses were input to the circuit and detailed information generated by the simulations about the response of the circuit to that input was extracted and analyzed.

In the simulations performed to investigate count rate, the input pulses (each having a 20 ns rise time and a 80 ns fall time) had a pulse height distribution that corresponded to the RQA5 spectrum. A total of 10,000 pulses, randomly distributed in time, formed the input pulse train. In the simulations, the input flux for this pulse train (expressed in counts per second per pixel) was varied from 1 to 2000 kcps/pixel by varying the duration over which the 10,000 pulses were input to the amplifier circuit from 10 s to 5 ms.

For each amplifier circuit, simulations were also performed to determine the calibration curve for the amplifier output response as a function of incident x-ray energy. For each energy, a single input pulse corresponding to a 1 to 200 keV monoenergetic X ray was used. (Note that, while the RQA5 spectrum has a maximum energy of 72 keV, input pulses larger than 72 keV may be encountered during the simulations due to pulse pile-up.) The resulting calibration curve was used in the determination of several measures of count rate.

Once the simulations described above were performed, the count rate for a given amplifier circuit was determined by taking the ratio of the number of times the amplifier

output response exceeded a selected voltage level to the duration of the input pulse train (i.e., 5 ms to 10 s). Using the calibration curve, that voltage level was chosen to correspond to an energy threshold of 19.5 keV – so as to allow the entire RQA5 distribution (which has a minimum x-ray energy of ~20 keV) to contribute to the count rate.

From the values of count rate obtained from the simulations, three specific measures of count rate were determined for each amplifier circuit design. The first was CR_{max} (maximum count rate), which is the highest count rate determined by the simulation. The other two measures are referred to as CR_{10} and CR_{30} and correspond to the rates obtained when 10% and 30% of the input flux fail to be counted due to dead time loss. (Dead time refers to the time period after one or more input pulses when the amplifier circuit observes the next input pulse as part of the last detected pulse due to pulse pile-up.)[49]

III. Results

IIIa. Amplifier Designs

The names and technical descriptions of the amplifier circuit designs examined in this study are summarized in Table 4.1 and the circuit diagrams for those designs, all of which employ a 3-stage architecture, are illustrated in Fig. 4.1.

Table 4.1: Design name, circuit description and pixel pitch for each of the amplifier circuit designs examined in this study.

Design Name	Circuit Description	Pixel Pitch
SPC1-amp1	3-stage, 1st order bandpass	1 mm
SPC1-amp2	3-stage, 2nd order bandpass	1 mm
New-amp-a	3-stage, 3rd order bandpass	1 mm
New-amp-b	3-stage, 3rd order bandpass	0.25 mm

Designs SPC1-amp1 and SPC1-amp2 are 1st order and 2nd order bandpass circuit designs that correspond to the prototype amplifier designs [36] and are illustrated in Figs. 4.1a and 4.1b, respectively. Design New-amp-a is a hypothetical, 3rd order bandpass variation of the first two circuit designs and is illustrated in Fig. 4.1c. These three designs were assumed to be incorporated in a pixel with a pitch of 1 mm – i.e., the same as that of the prototype arrays.[36] Design New-amp-b also corresponds to the circuit diagram in Fig. 4.1c, but was assumed to be implemented at a pixel pitch of 0.25 mm.

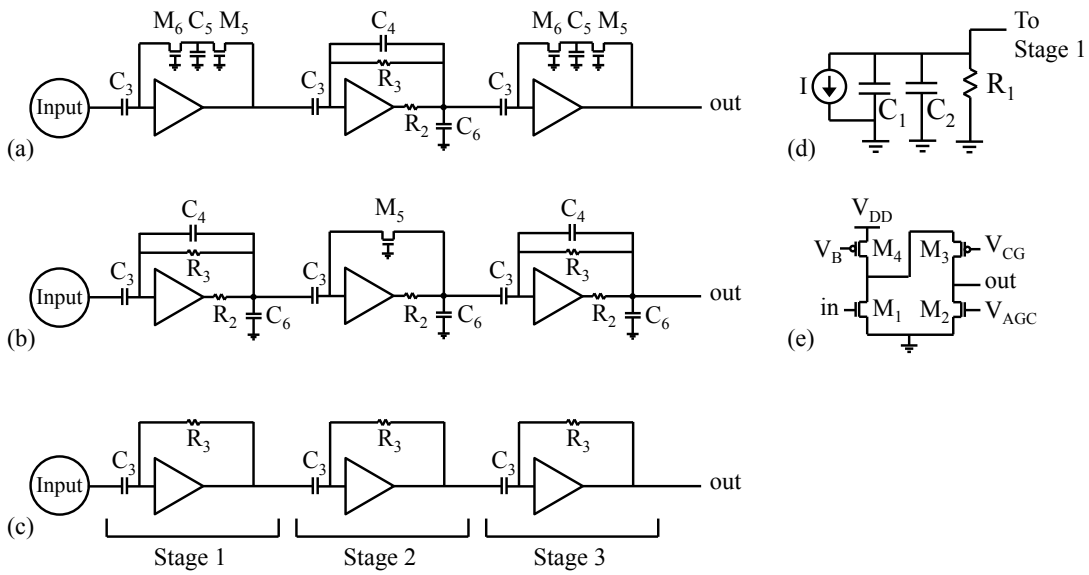


Figure 4.1. Circuit diagrams for the amplifier circuit designs described in Table 4.1: (a) SPC1-amp1, (b) SPC1-amp2, and (c) New-amp-a and New-amp-b. In these diagrams, transistors are labeled M_1 to M_6, capacitors are labeled C_1 to C_6, and resistors are labeled R_1 to R_3. Other circuits depicted in the figure include: (d) the circuit corresponding to the circle symbol at the input to each amplifier; and (e) a folded cascode circuit corresponding to the triangle symbols in each of the designs. Note that C_1 is the capacitance of the CZT detector, C_2 is a parasitic capacitance, V_{AGC}, V_B and V_{CG} are bias voltages, and V_{DD} is a power rail (which is set to 8 V in the study).

The transistor dimensions, resistance values and capacitance values corresponding to the various TFTs, resistors and capacitors appearing in the circuit diagrams of Fig. 4.1 are given in Table 4.2. In the case of SPC1-amp1 and SPC1-amp2, these values are the nominal specifications used in the design and layout of those prototype amplifier designs. The values of parasitic capacitance C_2 appearing in the table are estimates based on the area of overlap between the CZT detector and underlying metal wires in the pixel circuit, as well as the dielectric constant and assumed thickness of the passivation layer that separates the detector and wires. In the case of New-amp-a and New-amp-b, the values appearing in the table for these hypothetical amplifier designs were determined as described in the next section.

Table 4.2. Transistor width/length dimensions, as well as the resistance and capacitance of the other circuit elements, for the various amplifier circuit designs examined in this study. The symbols for the circuit elements listed in the table correspond to those appearing in Fig. 4.1. Note that the design specifications for New-amp-a and New-amp-b are identical, except for the value of the input detector capacitance C_1.

	SPC1-amp1	SPC1-amp2	New-amp-a	New-amp-b
Transistor dimensions (μm/μm)				
M_1	50/10	50/10	50/5	50/5
M_2	10/10	10/10	10/10	10/10
M_3	20/10	20/10	20/10	20/10
M_4	20/10	20/10	20/10	20/10
M_5	10/10	6/6	-	-
M_6	10/10	-	-	-
Resistor values (MΩ)				
R_1	200	200	10	10
R_2	10	10	-	-
R_3	200	200	15	15
Capacitor values (fF)				
C_1	195	195	195	12
C_2	100	100	100	100
C_3	500	500	500	500
C_4	100	100	-	-
C_5	100	-	-	-
C_6	10	10	-	-

IIIb. Simulation Results for Performance Metrics

For SPC1-amp1 and SPC1-amp2, simulations were performed to examine the following *performance metrics* of those circuits: (i) the magnitude of the amplifier output response generated by an input pulse corresponding to a 70 keV X ray; (ii) the degree of non-linearity of the amplifier output response over the input signal range of interest in this study (i.e., from 20 to 100 keV); (iii) the energy resolution; and (iv) the *settling time* of that circuit in response to an input pulse corresponding to a 70 keV X ray. Non-linearity was calculated following the convention described in reference 50 and

energy resolution was determined using the methodology described in Sec. IIb of this chapter. In addition, settling time is defined as the time required after an input pulse for the amplifier output response to essentially return to its baseline condition – i.e., return to and stay within 1% of its peak – as illustrated in Fig. 4.2. Shorter settling times are generally associated with higher count rates since they allow the amplifier circuit to resolve more input pulses.

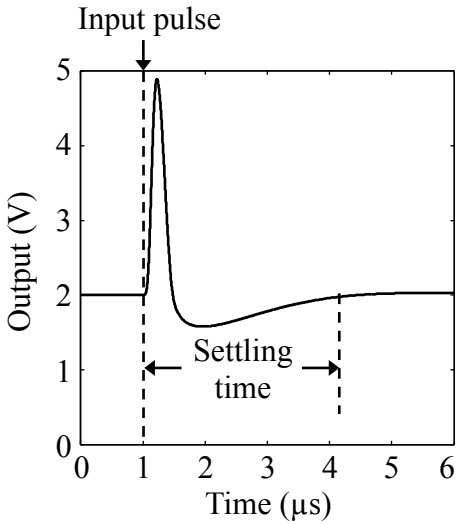


Figure 4.2. Schematic illustration of the concept of settling time. The solid curve represents the amplifier output response to an input pulse corresponding to an interacting X ray. Note that the dashed vertical line on the left corresponds to the introduction of an input pulse. See main text for further details.

For a given amplifier circuit design, performance metrics (i) through (iv) and, ultimately, count rate, are strongly affected by the values of the bias voltages applied to each amplifier stage. The values of these voltages (V_{AGC}, V_B and V_{CG}, shown in Fig. 4.1e) are collectively referred to as the *operating conditions* of the circuit. In the study, these voltage values were systematically varied so as to identify the *optimal* operating conditions – defined as that set of values which minimized settling time as well as satisfied a pair of criteria related to performance metrics (i) and (ii). For the first

criterion, in order to ensure that the amplifier output response is sufficiently large so as to be well above the noise floor of the subsequent component in the pixel circuit (i.e., the comparator), a minimum response of 1.25 V was required – consistent with a similar criterion used in Chapter 3.[38] For the second criterion, the deviation of the amplifier output response from linear behavior was required to be no larger than 10%.

In the simulations performed to identify the optimal operating conditions for SPC1-amp1 and SPC1-amp2, V_{AGC} was varied from 0 to 6 V in 0.1 V steps, V_B was varied from 0 to 6 V in 0.25 V steps, and V_{CG} was varied from 0 to 8 V in 0.5 V steps. The resulting values of optimal operating conditions, along with the corresponding values of performance metrics, are shown in Table 4.3. For both prototype amplifier designs, the resulting value for amplifier output response is well above the required minimum of 1.25 V while the degree of non-linearity is slightly below the upper limit of 10%. Interestingly, while SPC1-amp1 is seen to exhibit better energy resolution, SPC1-amp2 demonstrates better settling time.

Table 4.3. Summary of the values for the optimal operating conditions (columns 2 to 4) identified for each amplifier circuit design examined in this study – along with the values of the corresponding performance metrics (columns 5 to 8).

	V_{AGC}	V_B	V_{CG}	Amplifier Output Response	Non-Linearity	Energy Resolution	Settling Time
SPC1-amp1	2.0 V	5.75 V	4.5 V	2.7 V	7.51%	6.78%	143 μs
SPC1-amp2	2.1 V	3.50 V	1.0 V	2.8 V	9.23%	14.9%	53.3 μs
New-amp-a	2.7 V	2.75 V	3.5 V	2.9 V	5.34%	5.88%	5.56 μs
New-amp-b	3.4 V	1.50 V	3.0 V	2.9 V	8.11%	2.76%	3.11 μs

In the spirit of exploring the degree to which reductions in settling time could be achieved compared to those reported above for SPC1-amp1 and SPC1-amp2, a variety of

alternative amplifier circuit designs were explored. Starting from those prototype amplifier designs (and maintaining a pixel pitch of 1 mm), this exploration involved modification of the transistor dimensions, of the resistance and capacitance of the circuit elements, and of the configuration of the feedback loop. For each variation of design examined, the optimal operating conditions were determined using the same methodology employed for SPC1-amp1 and SPC1-amp2.

A promising design identified in this exploration (referred to as New-amp-a) is the circuit shown in Fig. 4.1c – the circuit element values for which are given in Table 4.2. New-amp-a differs from the prototype amplifier designs by virtue of a change in dimension for transistor M_1, the removal of resistor R_2 and capacitor C_6, and a change in the configuration of the feedback loop. Specifically, the new feedback loop is comprised solely of a resistor (R_3) with significantly lower resistance values than the R_3 resistors employed in the prototype designs.

The values of the optimal operating conditions, along with the corresponding values of performance metrics, for New-amp-a are shown in Table 4.3. Results are also shown for the same circuit implemented at a pixel pitch of 0.25 mm – corresponding to an estimate of the minimum pitch that the poly-Si circuits in the prototype arrays could potentially be reduced to.[38] The circuit element values for this design, referred to as New-amp-b, are given in Table 4.2.

In Table 4.3, the optimal values for V_{AGC}, V_B and V_{CG} for hypothetical amplifier designs New-amp-a and New-amp-b are all well within the range of values examined in the simulations – as is also the case for the prototype amplifier designs SPC1-amp1 and SPC1-amp2. Compared to the prototype designs, the amplifier output response of the hypothetical designs is seen to be very similar and the degree of non-linearity is seen to be generally better. Furthermore, New-amp-a and New-amp-b exhibit significantly better energy resolution and shorter settling times than SPC1-amp1 and SPC1-amp2 – largely due to the new feedback loop. For example, the improvement in energy resolution is partially a result of the decreased frequency bandwidth exhibited by the hypothetical designs which (as expected from Eq. [4.1]) causes a reduction in flicker noise. Note that, compared to New-amp-a, New-amp-b has a smaller C_1 capacitance that results in a larger signal at the input of the amplifier for the same input pulse, further improving the energy resolution of that design. Finally, the improved settling time of the hypothetical designs reflects more rapid dissipation of amplifier output response after an input pulse is applied.

The operating conditions shown in Table 4.3 were also used to obtain the results reported in the next section.

IIIc. Simulation Results Related to Count Rate

Count rates obtained from the simulations of the prototype amplifier designs and hypothetical amplifier designs are shown in Fig. 4.3 as a function of input flux. When input flux is low, each of the amplifier circuits is able resolve every input pulse – as seen from the close overlap of the count rate curves with the dashed line representing ideal

behavior. As input flux increases, SPC1-amp1 and SPC1-amp2 are seen to deviate from the dashed line (due to dead time loss) at considerably lower input fluxes than New-amp-a and New-amp-b – an expected outcome given the improvement in settling time reported for the hypothetical designs in Table 4.3.

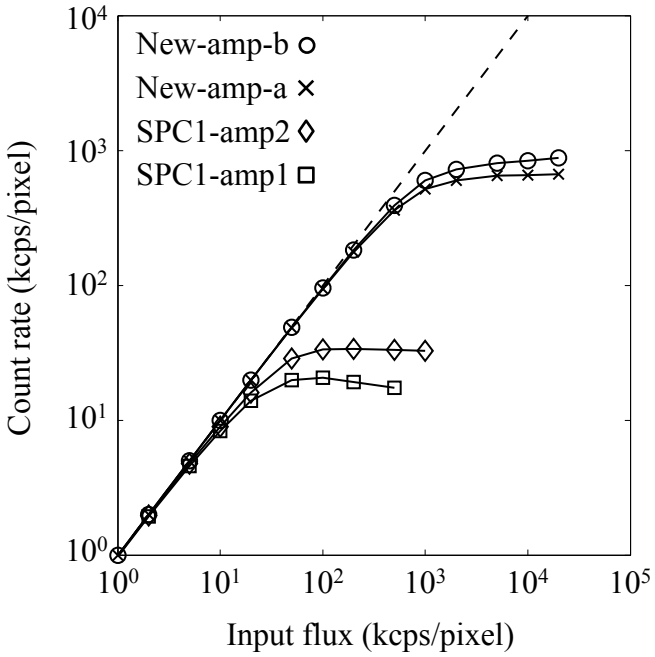


Figure 4.3. Count rate as a function of input flux for the four amplifier circuit designs. For each design, results are plotted up to that value of input flux beyond which less than 2% of the flux is resolved. The solid lines are drawn to guide the eye while the dashed line corresponds to the ideal of a 1-to-1 correlation between count rate and input flux.

Table 4.4. Results for the three measures of count rate (CR_{max}, CR_{30} and CR_{10}) for each amplifier circuit design. See text for further details.

	CR_{max} (kcps/pixel)	CR_{30} (kcps/pixel)	CR_{10} (kcps/pixel)
SPC1-amp1	20.7	13.9	5.03
SPC1-amp2	33.9	21.6	8.36
New-amp-a	666	381	154
New-amp-b	882	491	210

A summary of results obtained for maximum count rate, as well as for count rates with 30% and 10% dead time loss (CR_{max}, CR_{30} and CR_{10}, respectively), is shown in Table 4.4. For each of the four amplifier circuit designs, the values reported for CR_{max} are ~1.5 to 2 times higher than that for CR_{30}, and the values reported for CR_{30} are ~2 to 2.5 times higher than that for CR_{10}. As expected, for a given measure of count rate, the count rate values for the four designs are roughly correlated with the settling times reported in Table 4.3 – a correlation which validates the selection of minimum settling time in the determination of optimal operating conditions. In addition, for all three measures of count rate, New-amp-a and New-amp-b exhibit much higher values than SPC1-amp1 and SPC1-amp2 by a factor of ~20 to 30 – a result that can be largely attributed to the new feedback loop. Furthermore, New-amp-b exhibits higher count rates than New-amp-a due to its smaller input capacitance C_1 – which allows for the selection of optimal operating conditions with a faster, more favorable settling time.

The simulation methodology described in Sec. IIc of this chapter was also used to determine *energy response profiles* for each design – providing a means to visualize how accurately a given amplifier circuit design reproduces the input energy distribution. Energy response profiles were determined for two input energy distributions – the RQA5 spectrum and 70 keV monoenergetic X rays. For a given input energy distribution, the energy response profiles were obtained through simulations in which the energy threshold applied to the amplifier output response was increased in 1 keV steps from 19.5 up to 199.5 keV. For a given threshold, the number of times the amplifier output

response exceeded that threshold was tallied. A histogram of the differences of the tallies for consecutive thresholds formed the energy response profile.

The resulting energy response profiles for each of the four amplifier circuit designs are shown in Figs. 4.4 and 4.5. In each figure, results are shown for four input fluxes: 1, 10, 100 and 1000 kcps/pixel. Figure 4.4 corresponds to results obtained with the RQA5 spectrum. For SPC1-amp1 (which had a CR_{10} value of 5.03 kcps/pixel), when the input flux is 1 kcps/pixel, the energy response profile largely overlaps with the input energy distribution – demonstrating good fidelity. However, as input flux increases, the energy response profiles increasingly deviate from the input energy distribution – reflecting the progressive inability of the SPC1-amp1 circuit to unambiguously resolve, or correctly identify the energy of, input pulses that are more closely spaced in time. The same pattern of behavior is exhibited by each of the other amplifier circuit designs – with significant deviations from the input energy distribution becoming apparent at progressively higher input fluxes for SPC1-amp2, followed by New-amp-a and then New-amp-b. Note that the area under the curve for the input energy distribution is 10,000 counts – corresponding to the number of pulses used in the simulation. By comparison, for all amplifier circuit designs, while the area under the curve for the energy response profile is ~10,000 counts at lower input fluxes, the area decreases at higher input flux values – approaching a lower limit of 1 count due to progressively greater degrees of dead time loss.

Figure 4.5 corresponds to results obtained with 70 keV monoenergetic X rays. While the figure exhibits behaviors similar to those observed in Fig. 4.4, it more clearly illustrates how the energy response profiles change as a function of input flux. For all designs, as input flux increases, the number of counts below or above 70 keV increases due to pulse pile-up (at least until the input flux is so high that dead time losses result in only a small fraction of pulses being resolved). Interestingly, compared to New-amp-a and New-amp-b, SPC1-amp1 and SPC1-amp2 more strongly shift the monoenergetic, 70 keV input energy towards lower energies. This is a result of the prototype amplifier designs providing an amplifier output response that more severely undershoots compared to that provided by the hypothetical amplifier designs. An example of undershoot appears in Fig. 4.2 where the amplifier output response falls below the initial baseline value – affecting subsequent pulses that start during the undershoot.

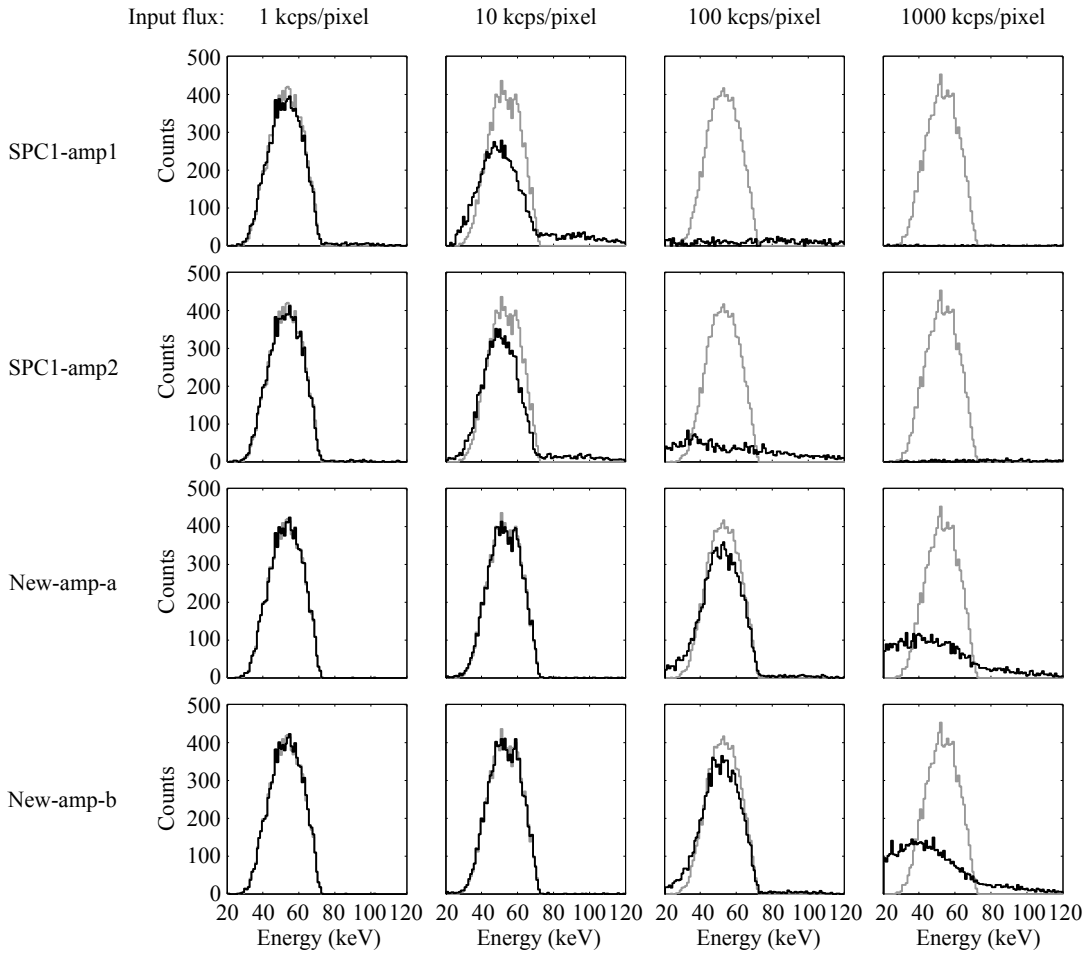


Figure 4.4. Energy response profiles for the four amplifier circuit designs. For each design, results are shown for input flux values ranging from 1 to 1000 kcps/pixel. For a given design and flux, the grey and black lines in a graph represent the input energy distribution (corresponding to the RQA5 spectrum) and the resulting energy response profile, respectively. Note that counts are plotted for a bin size of 1 keV. See main text for further details.

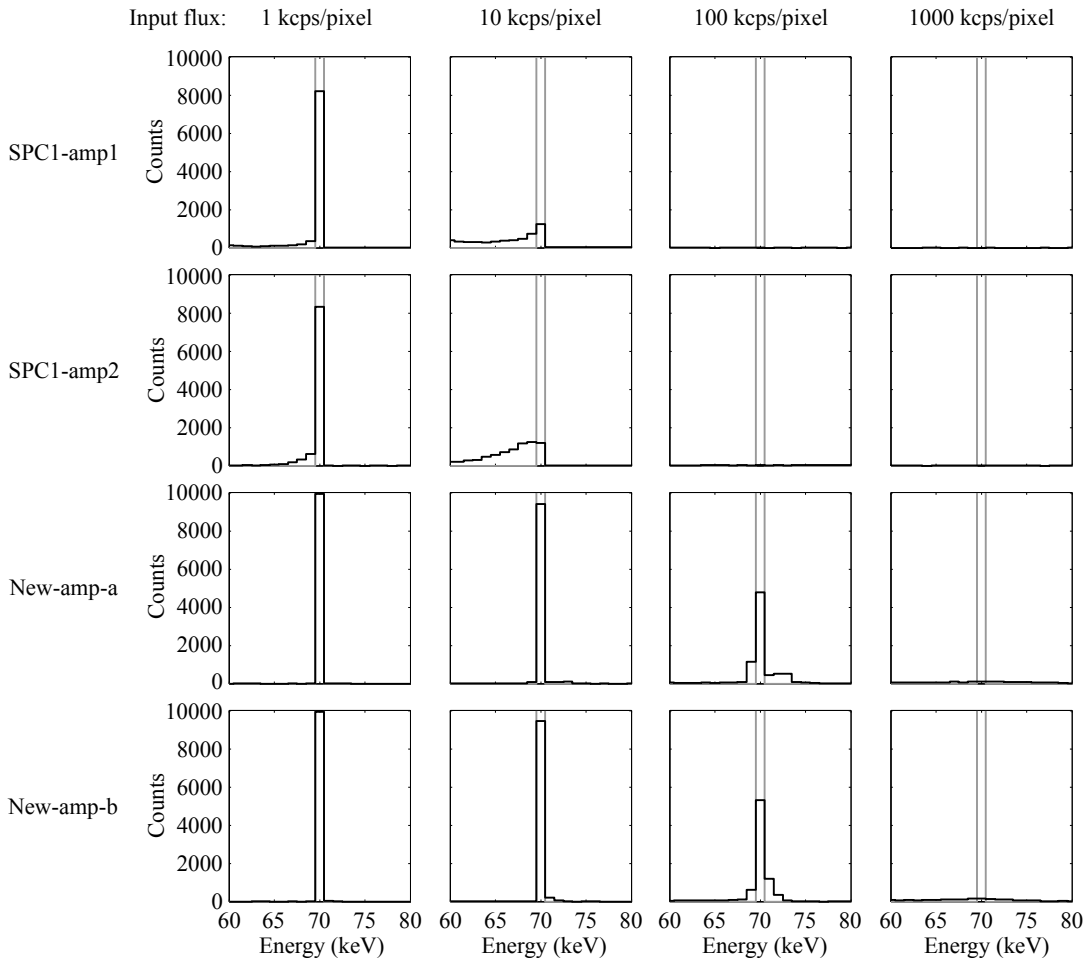


Figure 4.5. Energy response profiles for the four amplifier circuit designs – following the same conventions used in Fig. 4.4 – but where the input energy distribution corresponds to 70 keV monoenergetic X rays.

IV. Discussion

Circuit simulations have been employed to investigate the potential performance of amplifier circuit designs based on thin-film, poly-Si transistors for use in large-area, monolithic photon counting arrays. The simulations enabled detailed examination of energy resolution and count rate for existing prototype amplifier designs (SPC1-amp1 and SPC1-amp2), as well as for a pair of hypothetical amplifier designs (New-amp-a and New-amp-b) offering a number of advantages.

Compared to SPC1-amp1 and SPC1-amp2, the number and size of circuit elements (i.e., resistors, capacitors and transistors) in New-amp-a have been reduced – representing a simplification that could potentially improve reliability of this crucial analog component. (While these changes also reduce the area required for the amplifier circuit by 10% to 20%, this reduction represents only on the order of 1% to 5% of the total pixel area and therefore would be of limited assistance in reducing pixel pitch.)

A second advantage is that the significant increase in count rate capability offered by New-amp-a (which is over an order of magnitude greater than that of the prototype amplifier designs) approaches the rates associated with radiographic and fluoroscopic imaging applications. For example, the CR_{10} value for New-amp-a (which was implemented at a pixel pitch of 1 mm) is within an order of magnitude of the range of count rates associated with radiography and fluoroscopy (1 to 50 Mcps/mm^2). Moreover, New-amp-b (which corresponds to implementation of the amplifier circuit design of New-amp-a at a pitch of 0.25 mm) not only provides further significant improvement in the count rate per pixel, but also corresponds to a CR_{10} value of 3.4 Mcps/mm^2 – a highly encouraging result.

Further improvement of amplifier performance may be possible. In particular, while the hypothetical amplifier designs examined in this study were limited to the same folded cascode architecture as the prototype amplifier designs, exploration of alternative amplifier architectures may lead to further improvements in count rate. For example,

while the three stages for a given design were identical (i.e., employed circuits with identical transistor dimensions), expanding the exploration of designs to account for different transistor dimensions for each stage may lead to new circuit designs exhibiting even higher count rates. A second example would be employing a mix of amplifier architectures beyond the folded cascode for each stage to achieve higher count rates.

A simplifying assumption used in this study – that the input energy distributions presented to the amplifier circuits were given by the incident x-ray energy spectra – was chosen so as to result in simpler and easier to interpret energy response profiles such as those shown in Figs. 4.4 and 4.5. While not accounting for more realistic absorbed energy distributions is believed to have had relatively little effect upon the count rate results, extending the study to do so (as well as to account for effects such as detector shot noise) would produce more realistic energy response profiles – allowing, for example, the degree to which the amplifier reproduces interesting features of the absorbed energy distribution, such as k-edges, to be studied as a function of input flux.

In the examination of energy resolution, the simulation of noise was performed in the frequency domain – based on a framework developed in Chapter 3.[38] As a result, while the flicker noise contribution from transistors in the circuits was accounted for, the contribution from transistor thermal noise (which will become a dominant noise source at sufficiently high frequencies) was not. However, the designs of the amplifier circuits examined in the study (combined with the operational conditions of those circuits) are

such that the contribution of thermal noise is relatively minor – as demonstrated through analytical calculations presented in Appendix 4.A.

In summary, the simulation methodology employed in this study provides a powerful means for identifying new amplifier designs that offer improved performance. The encouraging results obtained from simulations of the hypothetical amplifier designs reported in this chapter support the hypothesis that poly-Si -based, large-area photon counting arrays that exhibit clinically useful count rates are feasible. Use of simulation techniques to further improve the energy resolution and count rate of the amplifier component, as well as to characterize and improve the other components (i.e., comparator, clock generator, and counter) of photon counting pixels for large-area arrays is planned.

Appendix 4.A *– Estimates of the relative contribution of TFT thermal noise based on analytic calculations*

The frequency domain circuit simulations performed in this study, which facilitate relatively straight-forward computation of TFT flicker noise, account for the complexity of the shape of the response of the circuit in frequency space. Estimates of the relative importance of the TFT thermal noise contribution were obtained from the analytic calculations described below.

The power spectral density for the flicker noise contribution of a transistor, in units of V^2/Hz, is:

$$S_{v-flicker}(f) = \frac{k_f}{C_{ox}^2 WLf} . \qquad [4.A1]$$

This equation was introduced as Eq. 4.1 in Chapter 4 (along with a description of its parameters) and is repeated here for convenience. The corresponding equation for the power spectral density for flicker noise expressed in units of A^2/Hz is:

$$S_{i-flicker}(f) = \frac{k_f g_m^2}{C_{ox}^2 WLf} . \qquad [4.A2]$$

The power spectral density for the thermal noise contribution of a transistor,[50] in units of A^2/Hz, is:

$$S_{i-thermal} = \frac{8}{3} k_B T g_m \qquad [4.A3]$$

In Eqs. 4.A2 and 4.A3, g_m is the transconductance of the TFT (which varies for each TFT in a design as a function of operating conditions), k_B is the Boltzmann constant (1.38×10^{-23} J/K) and T is temperature (298 K).

Integration of Eqs. 4.A1 through 4.A3 was used to provide estimates of noise for each TFT in each of the amplifier circuit designs. For a given TFT in a given design, the integration limits were determined through frequency domain simulations – yielding the pair of frequencies at which the gain of that TFT is $1/\sqrt{3}$ of its maximum value, known as the 3 dB points, and referred to in this study as f_{lo} and f_{hi}. (Those simulations also provide the value of g_m for the TFT.) With these values, taking the integral of Eq. 4.A1 provides an expression for an estimate of the flicker noise in units of volts:

$$\sigma_{v-flicker} = \sqrt{\frac{k_f}{C_{ox}^2 WL} ln\left(\frac{f_{hi}}{f_{lo}}\right)}\,, \qquad [4.A4]$$

taking the integral of Eq. 4.A2 provides an expression for an estimate of the flicker noise in units of amps:

$$\sigma_{i-flicker} = \sqrt{\frac{k_f}{C_{ox}^2 WL} ln\left(\frac{f_{hi}}{f_{lo}}\right) g_m^2} \qquad [4.A5]$$

and taking the integral of Eq. 4.A3 provides an expression for an estimate of the thermal noise in units of amps:

$$\sigma_{i-thermal} = \sqrt{\frac{8}{3} k_B T g_m (f_{hi} - f_{lo})}\,. \qquad [4.A6]$$

Each of the four amplifier circuit designs examined in the study has three folded cascode stages and each stage consisting of four TFTs: M_1, M_2, M_3 and M_4, as shown in Fig. 4.1. (When present in a circuit, the M_5 and M_6 TFTs did not contribute significantly to the noise.)[38] Due to the effect that the gain of each subsequent cascading stage has on noise from the previous stage(s), the noise associated with the first stage was found to be, by far, the dominant contributor of noise – rendering the noise contribution of the second and third stage negligible. For each of the analytical noise Eqs. 4.A4 through 4.A6, the noise for the first stage of a given design is given by the quadratic sum of that noise component for the four TFTs:

$$\sigma_{v-flicker}^{Stage\ 1} = \sqrt{\left(\sigma_{v-flicker}^{M1}\right)^2 + \left(\sigma_{v-flicker}^{M2}\right)^2 + \left(\sigma_{v-flicker}^{M3}\right)^2 + \left(\sigma_{v-flicker}^{M4}\right)^2}, \quad [4.A7]$$

$$\sigma_{i-flicker}^{Stage\ 1} = \sqrt{\left(\sigma_{i-flicker}^{M1}\right)^2 + \left(\sigma_{i-flicker}^{M2}\right)^2 + \left(\sigma_{i-flicker}^{M3}\right)^2 + \left(\sigma_{i-flicker}^{M4}\right)^2}, \quad [4.A8]$$

and

$$\sigma_{i-thermal}^{Stage\ 1} = \sqrt{(\sigma_{i-thermal}^{M1})^2 + (\sigma_{i-thermal}^{M2})^2 + (\sigma_{i-thermal}^{M3})^2 + (\sigma_{i-thermal}^{M4})^2}. \quad [4.A9]$$

Finally, the combined flicker and thermal noise for the first stage of a given design is:

$$\sigma_{i-combined}^{Stage\ 1} = \sqrt{\left(\sigma_{i-flicker}^{Stage\ 1}\right)^2 + \left(\sigma_{i-thermal}^{Stage\ 1}\right)^2}. \quad [4.A10]$$

Calculations carried out using these equations indicate the following. Across the four amplifier circuit designs, the magnitude of the flicker noise component obtained analytically from Eq. 4.A7 was consistently found to be ~67% to 70% of the corresponding flicker noise for the first stage obtained from the circuit simulations – illustrating the degree to which the analytical approach captures the full extent of the simulated flicker noise.

With regards to thermal noise, across the four amplifier designs, the magnitude of that noise obtained analytically from Eq. 4.A9 was found to be approximately $1/7^{th}$ (for New-amp-b) to $1/20^{th}$ (for SPC1-amp1) that of the flicker noise obtained analytically from Eq. 4.A8. As a result, the combination of thermal and flicker noise (from Eq. 4.A10) is only 0.1% to 1.1% larger than the flicker noise alone (from Eq. 4.A8) – demonstrating the relatively minor contribution of thermal noise.

Chapter 5:

Summary and Conclusion

This dissertation explored the feasibility of creating monolithic, large-area photon counting arrays using polycrystalline silicon TFTs through circuit simulations involving a number of simulation frameworks. The frameworks incorporated transistor parameters extracted from empirical measurements of individual poly-Si TFTs to make the simulation results representative of that semiconductor material. In the research, early versions of such frameworks were developed to guide the design of a set of poly-Si PCA prototypes named SPC1, then later extended to allow theoretical characterization of the various amplifier, comparator, clock generator, and counter circuit components of the SPC1 pixels.

For the amplifier component, exploration of the performance of the two amplifier circuit variations employed in the SPC1 prototypes involved the development and use of two simulation frameworks: an *energy-resolution framework* for examining output signal and energy resolution, and a *count-rate framework* for investigating count rate properties.

The energy-resolution framework presented in Chapter 3 was used to examine the output signal and energy resolution of the amplifier circuits in response to 70 keV x-ray photons. Using this framework, both circuit variations were found to provide sufficient output signal to allow the next component (i.e., the comparator) to operate properly. In addition, the energy resolution of both variations was found to be comparable to energy resolution capabilities reported for existing c-Si-based photon counting detectors.[†] The framework was also used to determine the noise contribution of each individual transistor in a given design. Such information can be used to identify which transistors make the largest noise contribution and should, therefore, be optimized in order to reduce overall noise and improve energy resolution.

The count-rate framework presented in Chapter 4, which was used to examine count rate properties for the amplifier circuits, assumed an RQA5 x-ray energy distribution. The count rates of the two amplifier circuit variations were found to be roughly two orders of magnitude lower than typical flux rates for radiographic or fluoroscopic (R/F) imaging – two forms of projection imaging where a large-area photon counting imager would be of potential interest. Using both the energy-resolution framework and the count-rate framework, a new amplifier circuit design was identified that provides output signal and energy resolution similar to those of the SPC1 circuit variations, while exhibiting a significantly higher count rate capability that is consistent with R/F flux rates.

[†] Note that those reported values were derived from characterization of an entire pixel, whereas the study performed in this dissertation only characterized the amplifier component of the signal chain.

For the remaining three components of the SPC1 prototypes (i.e., the comparator, clock generator and counter), a *robustness simulation framework* was developed to examine count rate properties as a function of robustness – a metric defined to measure how tolerant a circuit design is to variations in transistor properties. The comparator and clock generator components were evaluated together since those two components are highly dependent on each other. This resulted in four pairs of circuit variations for the comparator and clock generator components, and three circuit variations for the counter component. The robustness for a given circuit variation was determined after simulating 200 design variants and tallying the number of "successful" variants, as described in Chapter 3.

For the combined comparator and clock generator components, the pair of circuit variations with the highest robustness was found to exhibit a modest count rate (about one order of magnitude lower than R/F flux rates). However, it is expected that the count rate for that combination could be increased by at least an order of magnitude if more optimal transistor sizes were employed. For the counter component, all three circuit variations exhibited very high robustness as well as count rates sufficient for R/F. In particular, the circuit variation with the highest robustness also exhibited the highest count rate.

In this dissertation, simulations of circuit behavior were performed either in the temporal domain or the frequency domain. Specifically, simulations of count rate

(employing the count-rate framework and the robustness framework) were performed in the temporal domain, since count rate is inherently a time-dependent metric. On the other hand, simulations of noise (employing the energy-resolution framework) could be performed in either the frequency or temporal domain. For the amplifier energy resolution studies, the noise simulations were performed in the frequency domain. Frequency domain simulations offer the advantage of being less computationally intensive – which results in more rapid feedback and faster design iterations. In addition, to further accelerate the simulations, the amplifier energy resolution study only accounted for the noise contribution due to flicker noise generated by transistors – since that noise source was found to be the dominant source for the SPC1 circuits.

However, circuit simulations performed in the frequency domain do not predict real-world performance as accurately as temporal domain simulations, for a variety of reasons. For example, since frequency domain simulations only model small-signal behavior (which assumes a small, ~1 mV input stimulus and that all circuit elements behave linearly), they do not account for the non-linearity that occurs when signal becomes large (as is the case for the amplifier circuit when the output signal is on the order of 1 V). For this reason, a method to simulate poly-Si circuits in the temporal domain has been recently developed by our group and used to characterize the noise of active pixel circuits.[22] That methodology accounts for the flicker noise generated by transistors, as well as thermal noise generated by both transistors and resistors. Future simulations of poly-Si photon counting circuits could employ this methodology to produce more accurate estimates of noise and energy resolution. However, employing

this temporal-domain methodology in the energy-resolution framework would be challenging for a number of reasons, including that the computation time would increase by at least an order of magnitude.

Another way to improve the simulations would be to extend the existing frameworks to study the performance of components not investigated in this dissertation. For example, the robustness framework (which was used to investigate the comparator, clock generator and counter components) could be extended to facilitate examination of the robustness of the amplifier component. Furthermore, the count-rate framework (which was only used to investigate the amplifier component) could be extended to facilitate examination of the count rate performance of the entire pixel circuit. Specifically, this could be accomplished by progressively adding more components (i.e., the comparator, then the clock generator, and finally the counter) to the signal chain and determining the count rate – eventually resulting in a value of count rate for the entire pixel circuit.

In addition to improving the simulations, future development of photon counting circuits should include empirical measurements of prototype arrays and test circuits (such as those for SPC1) in order to calibrate the simulations and validate the circuit models. Such measurements require peripheral data acquisition electronics capable of operating those prototypes – a capability under development by our group. Furthermore, to empirically test the improvements predicted by simulations, new prototype arrays and test circuits (incorporating, for example, the hypothetical amplifier design reported in

Chapter 4) will need to be fabricated. However, while such empirical measurements will be valuable, circuit simulations should continue to be employed in order to derive important information that complements the measurements. For example, the robustness framework simulates 200 design variants in order to determine a robustness value for a given design – an important metric that should be determined before each new set of prototype arrays and test circuits are fabricated. Furthermore, simulations employing the energy-resolution framework can determine the noise contribution of each individual transistor in a circuit – a level of detail that empirical measurements would not be able to easily provide.

While this dissertation has focused primarily on improving photon counting pixels by modifying circuit design, the performance of such pixels is also heavily influenced by manufacturing considerations. On-going improvements in the poly-Si fabrication process (largely driven by the display industry) should make possible physical improvements, such as higher circuit density and/or finer pixel pitch, that will favorably impact performance. For example, the analytical algorithm developed in Chapter 3 to estimate the minimum pixel pitch achievable for future poly-Si photon counting arrays predicts that the 1 mm pitch of the SPC1 prototype arrays could be reduced to 250 μm – assuming a decrease in poly-Si minimum feature size from 6 μm to 1 μm and an increase in the number of metal layers allowed in the fabrication of poly-Si circuits from 4 to 8. As the display industry continues to invest in and refine poly-Si device fabrication, such processing improvements appear increasingly likely, and have the potential to reduce pixel pitch below those predicted in this dissertation. In the future, a combination of such

processing improvements and different circuit designs that occupy smaller pixel area while offering similar (or better) performance may allow photon counting arrays based on poly-Si TFTs to achieve pixel pitches as fine as 100 to 200 μm (the current range of pixel pitches employed for radiography and fluoroscopy).

In conclusion, given the encouraging results obtained by the theoretical studies performed in this dissertation, along with expected advances in poly-Si processing, the creation of large-area, monolithic photon counting arrays based on poly-Si TFTs appears increasingly feasible. Through judicious circuit design guided by empirical measurements of prototypes and additional simulation studies, it is anticipated that poly-Si-based photon counting imagers of a size commensurate with human anatomy and capable of resolving clinically-relevant x-ray flux rates can be created and employed – offering prospects for improving image quality while also potentially reducing radiation dose to the patient.

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