Bidirectional Neural Interface Circuits with On-Chip Stimulation Artifact Reduction Schemes

by

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To my parents, Elżbieta and Ernest

To God and mankind

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I find it ironic that doctoral studies are a time of great personal struggle, self-imposed solitude, and reliance on one's own motivation, yet they truly are an embodiment of the proverb "it takes a village ..." It is thus my duty to acknowledge and thank everyone in this proverbial village.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABSTRACT

Bidirectional neural interfaces are tools designed to "communicate" with the brain via recording and modulation of neuronal activity. The bidirectional interface systems have been adopted for many applications. Neuroscientists employ them to map neuronal circuits through precise stimulation and recording. Medical doctors deploy them as adaptable medical devices which control therapeutic stimulation parameters based on monitoring real-time neural activity. Brain-machine-interface (BMI) researchers use neural interfaces to bypass the nervous system and directly control neuroprosthetics or brain-computer-interface (BCI) spellers.

In bidirectional interfaces, the implantable transducers as well as the corresponding electronic circuits and systems face several challenges. A high channel count, low power consumption, and reduced system size are desirable for potential chronic deployment and wider applicability. Moreover, a neural interface designed for robust closed-loop operation requires the mitigation of stimulation artifacts which corrupt the recorded signals. This dissertation introduces several techniques targeting low power consumption, small size, and reduction of stimulation artifacts. These techniques are implemented for extracellular electrophysiological recording and two stimulation modalities: direct current stimulation for closed-loop control of seizure detection/quench and optical stimulation for optogenetic studies. While the two modalities differ in their mechanisms, hardware implementation, and applications, they share many crucial system-level challenges.

The first method aims at solving the critical issue of stimulation artifacts saturating the preamplifier in the recording front-end. To prevent saturation, a novel mixed-signal stimulation artifact cancellation circuit is devised to subtract the artifact before amplification and maintain the standard input range of a power-hungry preamplifier. Additional novel techniques have been also implemented to lower the noise and power consumption. A common average referencing (CAR) front-end circuit eliminates the cross-channel common mode noise by averaging and subtracting it in analog domain. A range-adapting SAR ADC saves additional power by eliminating unnecessary conversion cycles when the input signal is small. Measurements of an integrated circuit (IC) prototype demonstrate the attenuation of stimulation artifacts by up to 42 dB and cross-channel noise suppression by up to 39.8 dB. The power consumption per channel is maintained at 330 nW, while the area per channel is only 0.17 mm^2.

The second system implements a compact headstage for closed-loop optogenetic stimulation and electrophysiological recording. This design targets a miniaturized form factor, high channel count, and high-precision stimulation control suitable for rodent in-vivo optogenetic studies. Monolithically integrated optoelectrodes (which include 12 μLEDs for optical stimulation and 12 electrical recording sites) are combined with an off-the-shelf recording IC and a custom-designed high-precision LED driver. 32 recording and 12 stimulation channels can be individually accessed and controlled on a small headstage with dimensions of 2.16 x 2.38 x 0.35 cm and mass of 1.9 g.

A third system prototype improves the optogenetic headstage prototype by furthering system integration and improving power efficiency facilitating wireless operation. The custom application-specific integrated circuit (ASIC) combines recording and stimulation channels with a power management unit, allowing the system to be powered by an ultra-light Li-ion battery.

Additionally, the μLED drivers include a high-resolution arbitrary waveform generation mode for shaping of μLED current pulses to preemptively reduce artifacts. A prototype IC occupies 7.66 mm^2, consumes 3.04 mW under typical operating conditions, and the optical pulse shaping scheme can attenuate stimulation artifacts by up to 3x with a Gaussian-rise pulse rise time under 1 ms.

CHAPTER 1

Introduction

1.1 Background and Motivation

Over the past century, there have been tremendous advances in our understanding of animal and human brain function. One of the greatest accelerators of this research is the rapid development of technology that measures, analyzes, and interacts with the brain and the nervous system. Moreover, neural interfacing technology not only helps satisfy the scientific curiosity, but also provides powerful clinical tools for treating widespread neurological disorders and for control of prosthetic limbs in amputees. The concept of implanting electronic microchips into a brain to correct or alter its function not long ago would have been considered a science-fiction fantasy; now it has an entire dedicated research field and industry. Commercial electronic medical devices such as Medtronics' Activa® Neurostimulator for deep brain stimulation or NeuroPace's RNS® device for epilepsy treatment have already been implanted into patients to help them cope with life-debilitating disorders.

Neural interfacing technology is concerned with two major tasks: recording from neurons and controlling, or stimulating, neurons. Neural recording is a necessary tool for most neuroscientific research as it provides concrete validation for theories ranging from synapse-level activity to large-scale biological neural circuits and networks. Neural stimulation, or neuromodulation, is used in medical devices where an artificial activation of neurons can treat or alleviate symptoms of neurological disorders. These two tasks can also be used in conjunction to

provide an even more powerful set of tools. Localized stimulation can trigger or alter a neural circuit that is simultaneously being recorded for a study. Conversely, neural recordings can help control a neuromodulation system by giving real-time feedback and automatically adjusting stimulation parameters. The direct and on-line combination of recording and stimulation is commonly referred to as closed-loop neuromodulation and has gained increasing popularity.

1.2 Current State-of-the-Art Neural Interfacing Systems

Engineers and scientists have been building and utilizing neural interfaces for almost a century. One of the earliest accounts of neural recording was provided by Hans Berger's discovery of electroencephalography (EEG) in 1924 [1]. Further on, the adoption of silicon-based integrated circuit technology allowed significant size reduction and improved reliability of neural interface devices. In the late 1960s, the introduction of the silicon probe enabled neuroscientists to reliably record action potentials (AP) at a micro-scale distance from the neurons [2]. The introduction of miniature low-cost neural recording amplifier ICs in early 2000s allowed the design of compact and low-power recording systems [3].

As simple unidirectional system design blocks are gaining maturity, further advancements often rely on effectively combining recording and stimulation. True integrated bidirectional neural interfaces which combine recording and stimulation circuitry within the same package (shared PCB or chip die space) have now been reported for over a decade [4]. Majority of these systems utilize electrical recording and electrical stimulation modalities. Bidirectional systems without closed-loop algorithm implementations have been built from commercial-off-the-shelf (COTS) devices [5] or custom application-specific integrated circuits (ASICs) [6], [7], [16]–[18], [8]–[15]. Further integration of bidirectional interfaces with DSP-based closed-loop algorithms has been shown with COTS devices [19]–[27] and custom ASICs [28], [29], [38], [30]–[37].

Bidirectional neural interfaces also incorporate alternative recording or stimulation modalities. In this dissertation, we will additionally focus on interfaces for optogenetics studies. In optogenetics, artificial light sources generate visible light that stimulates genetically-engineered light-sensitive neurons [39]. When combined with high resolution electrical recording, this creates a powerful tool that utilizes the advantages of the two techniques. At University of Michigan, a novel probe has been developed which monolithically integrates electrical recording sites with micro-light-emitting-diodes (μLEDs) onto a single implantable shank for multi-channel optogenetic studies [40]. Several miniaturized LED- and LD- (laser-diode) based interface system publications have also appeared in recent years. In [41]–[43], optical probes are combined with wirelessly-controlled LED/LD driver electronic backends, while [44]–[48] also added recording capability. Due to the technique's novelty, there is considerable room for improvement in terms of system size, power consumption, and number of channels, which are all focus of the proposed systems in Chapter 4 and Chapter 5.

A fundamental challenge of a bidirectional interface (especially in closed-loop operation) is the concurrent recording of high-fidelity neural signal and stimulation [49]. When a system is recording a neural response to a stimulus, unwanted stimulation artifacts directly couple onto recording channels. By corrupting the recorded signal, these artifacts negatively impact data processing and proper functionality of closed-loop algorithms which rely on detecting features from the recorded signals. Despite the substantial research accomplished to prevent or mitigate the effects of stimulation artifacts, there is no consensus on the most robust technique that does not sacrifice basic system constraints. Current state-of-the-art artifact cancelation or mitigation techniques can be subdivided into analog front-end techniques which prevent channel saturation and digital back-end algorithms which subtract artifacts if they are within the input range. The

former include quick-recovery amplifiers with a reset control input [6], [10], [15], [17]–[19], [23], [29], [35], [38], signal-blanking systems which disconnect input during stimulation [20], [24], [36], [50], or symmetrically-implanted electrodes for common mode artifact rejection [28]. The digital back-end techniques include filtering and template subtraction algorithms [26], [32], [51]–[58]. This work introduces two novel artifact cancellation and prevention schemes for low-power IC integration: a mixed-signal cancellation approach for electrical stimulation in Chapter 3, and an optical stimulus pulse-shaping approach for optical stimulation in Chapter 5.

1.3 Outline

The rest of the thesis is organized as follows. Chapter 2 provides basic neuroscience and neurotechnology background. Chapter 3 describes a bidirectional electrical neural interface IC architecture with stimulation artifact rejection circuit and additional noise and power reduction schemes. Chapter 4 introduces a new opto-electrophysiology system that combines the Michigan optoelectrode with custom and off-the-shelf application-specific integrated circuits (ASICs) yielding a highest-channel-count miniature headstage. Chapter 5 introduces a new custom ASIC which combines LED driving and electrical recording capabilities with a power management unit (PMU) and a new optical-artifact preventive technique based on optical pulse shaping. Finally, contributions and future research directions are discussed in Chapter 6.

CHAPTER 2

Neuroscience and Neurotechnology Background

2.1 Introduction to Neuroscience[1]

While weighing only 1.5 kg, the brain is an immensely complex computing machine which controls most human functions, behaviors, and thought processes. The basic unit of the brain is a neuron cell (shown in Figure 2-1) which performs computations inside of its center, or *soma*, based on the electrochemical inputs to the cell at the *dendrites*. The neuron carries a signal through the physical space in an elongated part, called the *axon*, and delivers the output to other neurons through micro-scale connections called *synapses*. The signaling modality of the neuron is a spike or *action potential* (AP) in the cellular membrane voltage potential. An AP is formed by the fluctuating ionic concentrations inside and outside of the cell caused by electrochemical forces. The movement of these ions is governed by ion channels or *gates* embedded in neural walls which react to changes in potential. A change in membrane potential activates neighboring gates that in themselves increase its surrounding potential. This creates a "chain reaction" of activated gates and changing potentials that travels down the neuron as an action potential. It is this process that can be triggered or inhibited through therapeutic neuromodulation techniques. The APs can be externally and artificially triggered through depolarization, or by significantly changing cell

[1] Information in Section Chapter 2 is excerpted from a textbook "Principles of Neural Science" by E. Kandel, T. Jessel, and J. Schwartz. [124]

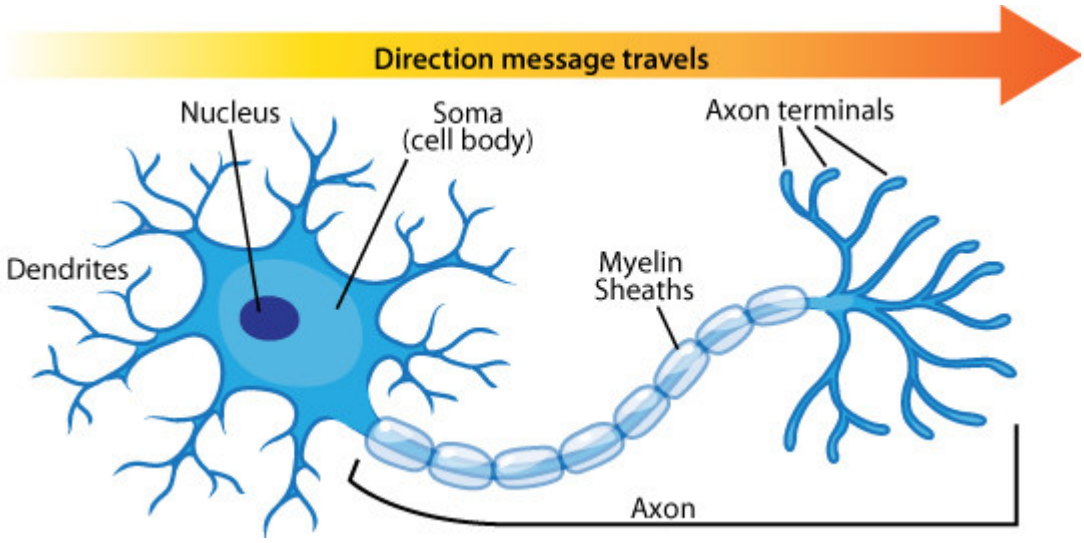


Figure 2-1. Simplified neuron diagram. (Source: https://askabiologist.asu.edu/neuron-anatomy)

potential, either with current or voltage stimulation, or through modification of ion channels to react to other stimuli such as light (optogenetics).

While the discovery of neuron cell activity is still one of the major breakthroughs of modern science, the mapping of high-level neuronal circuits has become an even greater challenge. After all, there are over 80 billion nerve cells in an average human brain with over 1000 connections (synapses) per each neuron [59]. Neuron cells communicate with one another through APs and create larger neural circuits which control specific functions, all the way from basic motor skills to forming memories and abstract concepts. Moreover, many common neurological disorders arise from malfunctions of these circuits. A reduced level of dopamine neurotransmitters which are responsible for connections between neurons is generally considered as the cause of Parkinson's Disease (PD). Excessive synchronization of neuron firings is often correlated with epileptic seizures. Active monitoring of these circuits and targeted external modulation through electronic hardware has already been introduced in clinical fields with a relatively high degree of success

[60], [61]. The potential for impact is high: PD in 2015 has affected about 6.2 million people globally, while epilepsy has affected more than 39 million [62].

We must not forget that the nervous system is not just constrained to the brain, but it covers almost every part of the human body. The spinal cord provides an information highway between the brain and major organs and limbs, as well as it performs some low-level control. The nervous system extends to most organs, controlling their functionality, either consciously, such as in muscles, or subconsciously, such as in the digestive system. This subset of the nervous system is called the peripheral nervous system (PNS). There is substantial research in mapping and understanding of PNS, as it is also often easier to access than the brain itself.

2.2 Neuromodulation and Closed-loop Control

2.2.1 Neuromodulation

As defined in [63], neuromodulation is any technology that interfaces with and affects the nervous system. Processes related to neuromodulation include stimulation, inhibition, modification, or regulation in the central or peripheral nervous systems. While most of the technological advances in neuromodulation began taking place in latter half of the 20th century, one of the earliest accounts of "neuromodulation therapy" dates to 15 AD. According to a reported story, a freed slave of Roman Emperor Tiberius was suffering from chronic pain until he had accidentally stepped on an electric torpedo fish and experienced an electric shock; afterwards, he claimed that the pain has substantially decreased. Unfortunately, it took almost 2 millennia for our society to grasp the underlying mechanism of this unlikely cure.

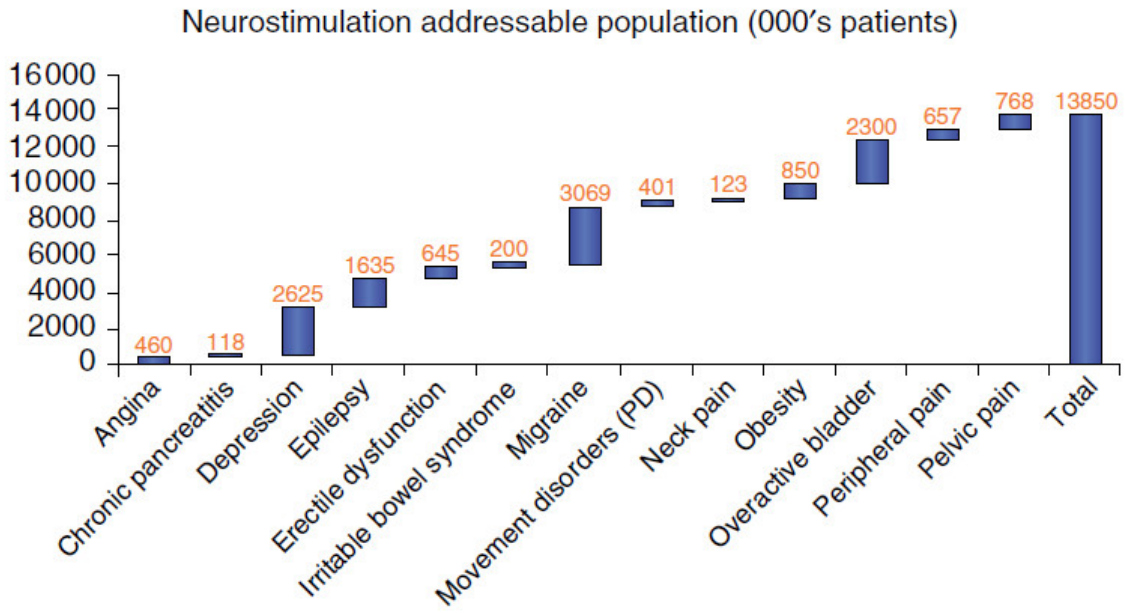


Figure 2-2. Disorders and estimated population in USA affected by disorders which can be treated by neurostimulation. [63]

Neuromodulation is most often associated with therapeutic devices, and quite understandably, most research focuses on such applications. Neuromodulation devices are being introduced or are already utilized for a wide range of neurological disorders, ranging from epilepsy and PD to obesity and erectile dysfunction (see Figure 2-2). A two-year study of a responsive neurostimulation system (NeuroPace) observed an average seizure reduction of 50% in 191 epilepsy patients [61]. Likewise, Deep Brain Stimulation (DBS), a popular neurostimulation technique for treatment of various neurological diseases, has improved the quality of life for many patients worldwide [64]. An estimated 14 million people in United States alone may benefit from neurostimulation devices. However, neuromodulation may also be used for other purposes. It is already a common basic science tool allowing triggering of neuronal circuits under test, often through electrical or optogenetic means [65]. Neural interface has also become the talk of the start-

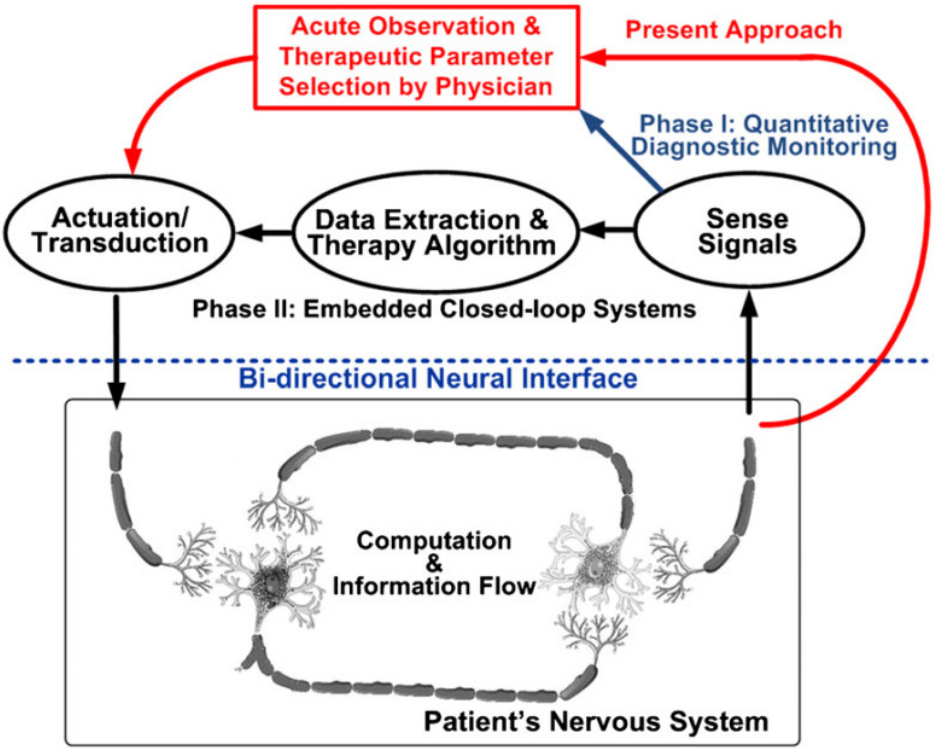


Figure 2-3. Diagram comparing open-loop (in red) and closed-loop (in black) neuromodulation approach. [28]

up world as entrepreneurs, scientists, and engineers have recently founded companies aiming at improving and enhancing the human brain functions through implantable hardware [66], [67].

2.2.2 Closed-loop Modulation

The process of implanting and controlling neuromodulation devices is most often an open-loop task. The surgeon inserts the stimulating device into the tissue and fine-tunes the parameters of stimulation to provide the desired effect. A patient who undergoes such treatment has to report back to the clinic on a regular basis to change the stimulation settings in order to adapt to his or her changing symptoms. The only feedback in this system – as shown in red in Figure 2-3 – is the physician making an acute observation and selecting proper stimulation parameters. An obvious way to improve the procedure is to introduce an automated control of the neuromodulation device – this would minimize patients' need for medical supervision and hospital visits. In an automated

system, a closed-loop neural interface controls current stimulation to a brain region by monitoring the recorded neural signal from the neighboring neural tissue and adjusting stimulation parameters in a feedback fashion (as shown in black in Figure 2-3). Closed-loop operation may not only alleviate the problems of more established experimental techniques but also enable new experiment techniques in basic science [68], [69]. Quick and precise feedback can be used to guide perturbations of neural systems, generating and confirming circuit-based models of underlying neuronal networks. In chronic applications such as neuroprosthetics control, closed-loop feedback can adapt stimulation to changing neural dynamics caused by brain's neuroplasticity, relieving the need for periodic manual parameter updates. This philosophy has been shown in studies [70], [71] and has been carefully introduced to a number of neuromodulation devices such as [28] and [61].

2.3 Neural Interface Modalities

In this section, different neural recording and stimulation techniques will be reviewed, with extra emphasis on the ones implemented in this work. First subsection describes the different neural recording modalities and analyze the signal properties of electrical neural recording. The second subsection overviews various neural stimulation modalities, in particular, electrical stimulation and optogenetic stimulation.

2.3.1 Neural Recording

Neural recording can be categorized into 4 general modalities, as shown in Figure 2-4 [72]. (1) Electrical recording probes measure changes in voltage around (or inside) neuronal cells. (2) In optical recording, a microscope is used to detect light emission from neural activity chemical indicators (such as fluorescent indicators). (3) Magnetic resonance imaging (MRI) can detect neural activity through measuring magnetic changes of various agents inside the brain. (4) In molecular recording devices, a record of neural activity is stored in a biomolecular polymer.

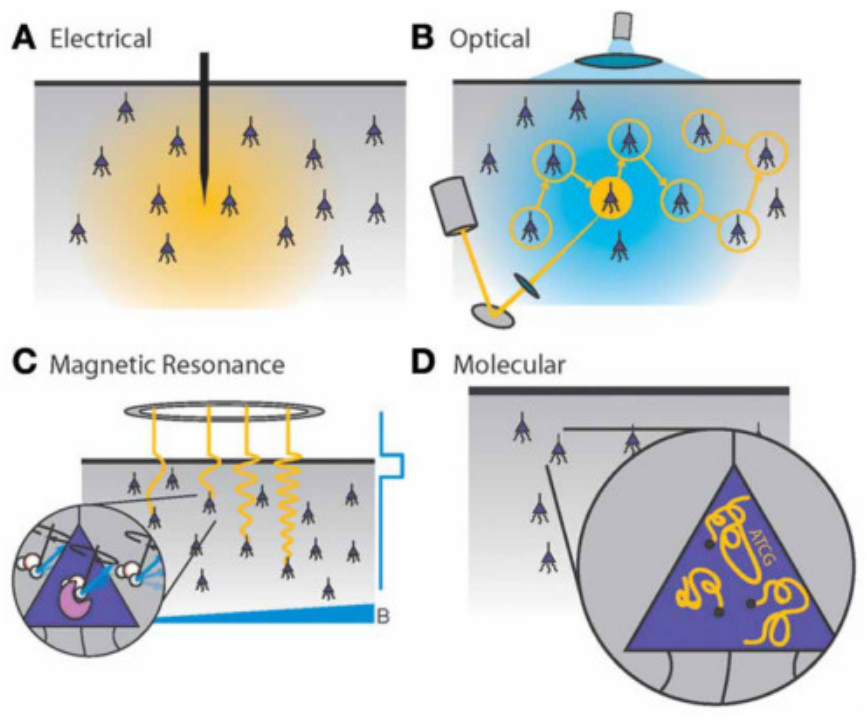


Figure 2-4. Four major neural signal recording modalities: (A) electrical recording, (B) optical recording, (C) MRI recording, and (D) molecular recording. [72]

Each modality has its advantages and disadvantages, and can be differentiated by 3 major quantitative parameters: the number of neurons monitored, the spatial resolution, and temporal resolution. Multi-electrode arrays can record > 1000 neurons with single neuron resolution and sub-millisecond temporal resolution. Optical recording can currently monitor ~100,000 neurons at a 1s temporal resolution. MRI is able to non-invasively scan the entire brain at 1s scale but does not have a single neuron spatial resolution. In following chapters, only electrical recording is considered in the proposed devices as it is most widespread and easily implantable with microfabrication technologies, and we will thus refer to it as simply "recording."

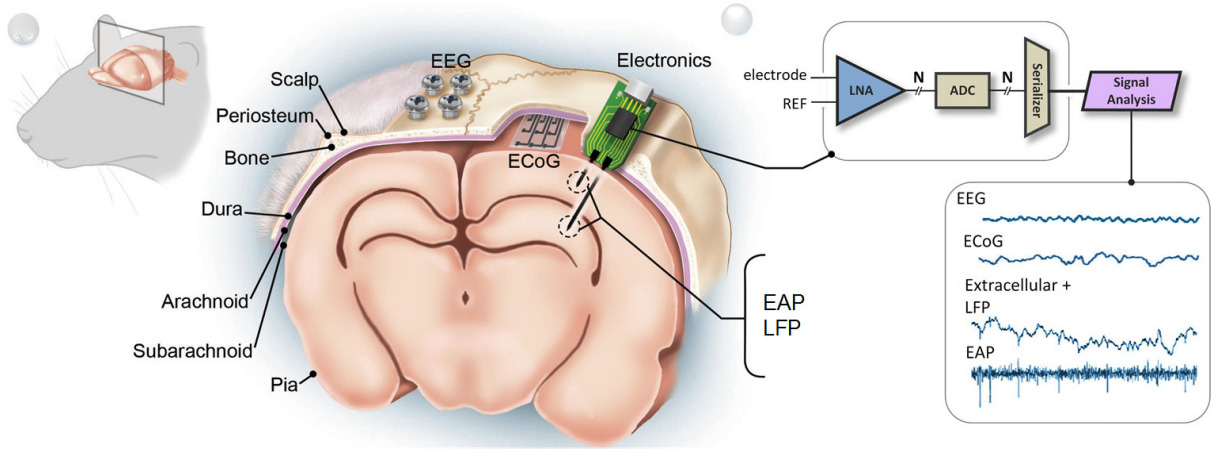


Figure 2-5. Illustration of various electrophysiological neural recording technologies implanted in a mouse brain. Adapted from [125].

Table 2-1 Electrophysiological Neural Signal Modalities (adapted from [92])

Signal Type	EEG	ECoG	LFP	AP
Bandwidth	0.5-50Hz	1-500Hz	1-500Hz	250Hz-10kHz
Amplitude	1-50µ	1-500µ	10µ-5mV	10µ-1mV
Spacing	3cm	0.2-10mm	0.1-1mm	0.1-1mm
Invasive	No	Craniotomy, no neural damage	Craniotomy, neural damage	Craniotomy, neural damage
Area Coverage	Whole Brain	~ cm2, whole brain	~ mm2	~ mm2
Stability	Decades	Decades	Years	Months

We can further classify electrical recording in terms of recording site location and signal characteristics. Figure 2-5 illustrates the placement of the various electrophysiological recording technologies in a mouse brain cross-section. Electroencephalogram (EEG) signals contain information from a large cortical area and are sensed through non-invasive electrodes placed on a scalp. Unfortunately, due to distance between the neural signal sources and the scalp as well as the large attenuation inside the bone skull, the signal is level is very low (below 50 µV) and high temporal and spatial resolution is lost. Most EEG systems cover the entire brain and can theoretically (using dry electrode setup) maintain its signal fidelity over a very long time.

Electrocorticography (ECoG) retains more temporal and spatial content, as well as higher signal amplitude. It can be recorder from large electrodes (but smaller than EEG electrodes) implanted at the surface of the brain, but underneath the skull. This modality is popular for many human-use biomedical devices since the neural tissue is not directly damaged during the implantation process. It also provides good area coverage when using large grid arrays and may provide stable recording for many years. Intracortical implants are the most invasive technology because they are inserted directly into the neural tissue, displacing a portion of neural tissue in the process. However, they do provide the most precise neural information and are the only well-proven technique of capturing single-neuron information. Intracortical electrodes detect 2 kinds of signals, local field potentials (LFPs) and extracellular action potentials (EAPs). EAPs give a direct insight into neural activity and are therefore the most important modality for basic science research. Spikes require large recording bandwidth (up to 10kHz) and dynamic range (up to 1mV). LFPs are slow local potential fluctuations which form as a result of aggregate neural activity. They can be recorded with the same intracortical probes but capture a larger area of neural activity, albeit at lower time and spatial resolution.

Systems implemented in this thesis will focus on ECoG, LFP, and EAP recordings. In Chapter 3, the bidirectional interface implements ECoG recording channels since they are commonly used in epilepsy and Parkinson's suppression devices. The optogenetics systems described in Chapter 4 and Chapter 5 are designed as basic science research tools and implement intracortical LFP and EAP recording front-ends.

2.3.2 Neural Stimulation

Like neural recording, neural stimulation can be implemented through a variety of techniques and modalities. In this thesis, we will focus on two stimulation techniques: electrical

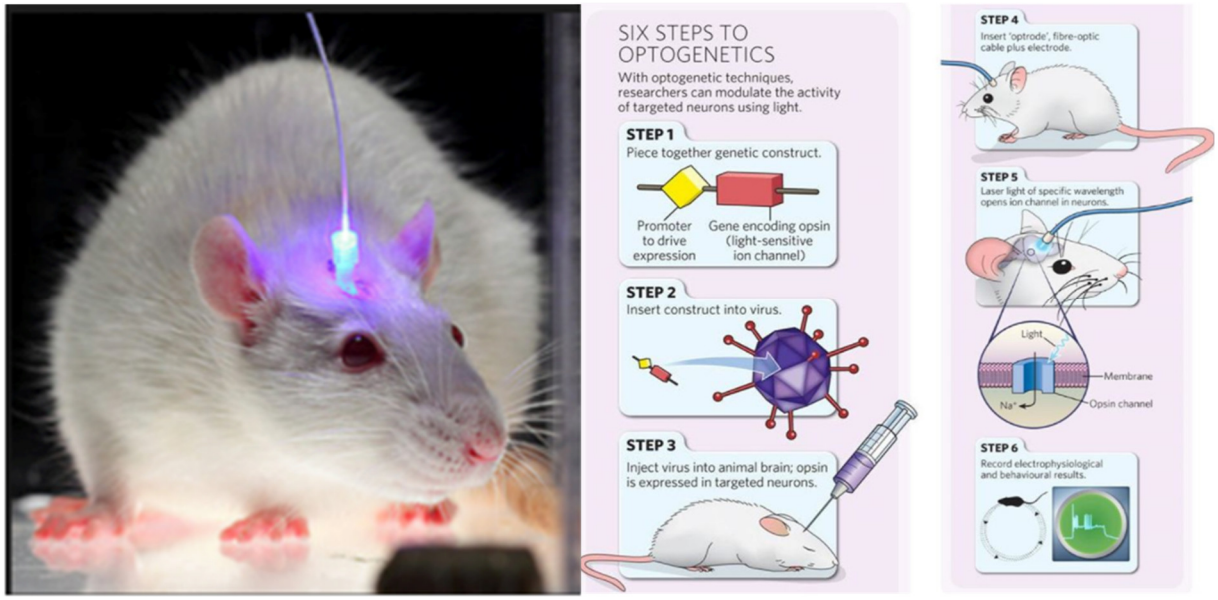


Figure 2-6. Pictorial explanation of the optogenetics technique. [126]

and optical stimulation. The two methods are popular in the neuroscientific community as they demonstrate high spatial and temporal resolution.

Electrical stimulation provides the most direct method for activating neurons inside neural tissue [73]. An electrical stimulator injects current into the tissue, creating an electric field gradient between the stimulating site and the ground. If the voltage potential around a neuron increases above a certain threshold, the neuron will depolarize and it will fire an action potential.

Optical stimulation of neurons is accomplished through a tool called optogenetics. Optogenetics has become a popular and powerful tool for neuroscience research since its introduction in 2005 [39]. The technique utilizes advances in genetic engineering and optics to provide superior resolution and specificity. Shown in Figure 2-6, it involves genetically modifying specific types of neurons to express light-sensitive ion channels, called opsins, on their membranes. The light-sensitive ion channels then provide means to selectively excite or silence neurons with light at specific wavelengths. Neural activity can thus be precisely modulated by controlling the light output from the sources in neurons' vicinity. Optical stimulation offers several

advantages over electrical stimulation: cell type specificity, multi-modality, and greatly reduced stimulation artifact. Only the neurons of the specific types that express opsins can be stimulated with light. Cells can be either activated or silenced by light of specific wavelength based on the type of opsin expressed. Finally, light stimulation produces little or no artifact in the recorded signal since it does not directly inject current into the tissue. These advantages combined make optical stimulation an exceptional choice for stimulation in neuroscience experiments.

CHAPTER 3

Bidirectional Neural Interface IC with Active Stimulation Artifact Rejection

3.1 Introduction

Continuous brain monitoring during stimulation presents a challenge due to large artifacts which appear alongside the neural signal. These artifacts distort useful information in the recorded signal and can disrupt closed-loop system operation. Many published works have attempted to mitigate this problem in a variety of ways, especially in pure electrical stimulation and recording systems where these artifacts are substantially larger than the recorded signal itself. In this chapter, we will present a novel neural interface circuit architecture and an IC prototype incorporating signal conditioning front-end features to reduce aforementioned artifacts without a substantial sacrifice in system performance [74]. The mixed-signal adaptive approach removes the artifacts at the front-end of the recording channels in order to prevent preamplifier saturation. The chapter will also introduce additional system features to increase signal fidelity and lower the power consumption. A noise removal technique called Common Average Referencing (CAR), implemented at the front-end, removes cross-channel common-mode noise and improves channel SNR. In addition, a new Range-Adapting (RA) SAR ADC architecture provides a more power efficient digitization of the neural signal.

The chapter is subdivided in the following format: Section 3.2 discusses the prior art of artifact prevention and removal and provides the theoretical background for the proposed

stimulation artifact cancellation algorithm. Section 3.3 analyzes the sources of common mode noise and introduces the CAR algorithm. Section 3.4 describes the circuit implementation of the new architectural elements as well as the new RA SAR ADC. Sections 3.5 and 3.6 show recording channel characterization and *in-vivo* measurements respectively. Finally, conclusions are drawn in Section 3.7.

3.2 Theory of Stimulation Artifact Cancellation

3.2.1 Artifact Coupling

Proper operation of a closed-loop neural interface microsystem requires simultaneous recording and stimulation. In practice, continuous monitoring during stimulation presents a challenge due to large saturating artifacts appearing with the signal. Stimulation artifacts inherently form at the recording interface during concurrent sensing and stimulation. Figure 3-1 (a) depicts simultaneous stimulation and recording and shows the corrupted recorded signal. We expect a stimulation-injected current to travel to a nearby neuron to affect its state by either triggering or inhibiting its spiking activity, while the recording probe monitors the neuron's activity throughout this process. Unfortunately, due to proximity of the recording and stimulation probes, a fraction of the stimulation current bypasses the neural tissue and directly couples onto the recording probe. Because the direct path is short and the stimulus current is usually larger than the neural extracellular ionic currents, the resulting stimulation artifact dominates the recorded signal. This leads to two problems. First, the large artifact current can saturate the sensitive preamplifier, causing signal loss and lowering the biomarker detection rate. An increased dynamic range might mitigate this problem but at the cost of high power consumption. Second, even if the artifacts do not saturate the amplifier, they might be mistaken for the biomarkers themselves, as it is shown in Figure 3-1 (b), leading to a high false biomarker detection rate.

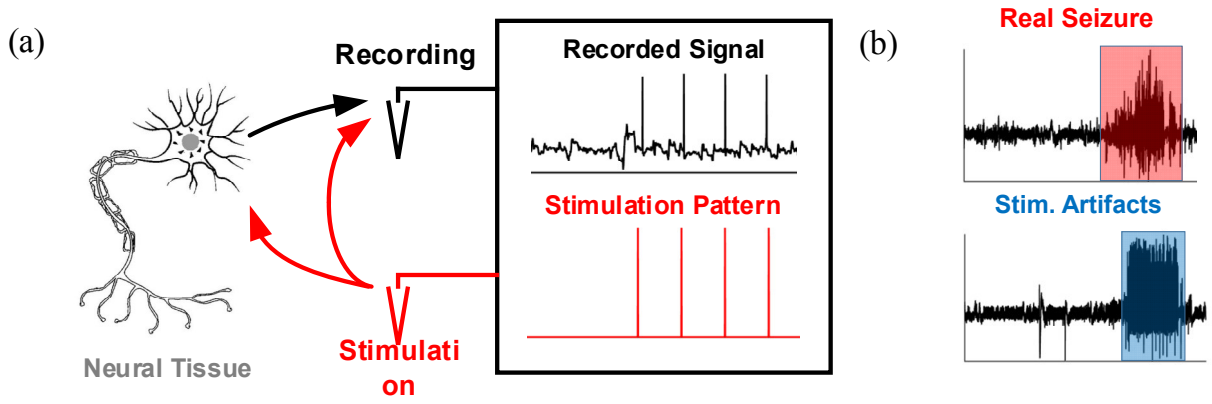


Figure 3-1. (a) Diagram showing formation and addition of stimulation artifacts in the recorded signal, and (b) comparison of similar characteristics of a seizure and stimulation artifact signal.

3.2.2 Prior Art

Many closed-loop systems that suffer from large artifacts do implement some sort of artifact cancellation. This can be done in various ways, and it usually depends on the application and system constraints. Let us first assume a number of constraints before we continue with analysis. The ultimate system that we would like to implement is wireless, therefore we want to minimize power consumption and area. The location of the artifact removal module within the system will have significant impact on these parameters.

As shown in Figure 3-2, we can generalize the placement into 3 different types. In a), the artifact removal takes place at the very back-end of the system. It can be implemented in software and computed at the processor level, or in a dedicated DSP engine that handles the computational load before being fed into a closed-loop controller. This approach has been used in [51]–[53], [55], [56], [58]. The advantages of this approach are complete reconfigurability and access to virtually limitless resources. However, due to our assumption of the large dynamic range consumed by the artifact, the entire analog-front-end (AFE) in the wireless module has to consume more power to accommodate an extra 30dB of dynamic range [75]. Second, the transceiver will need to accommodate higher bandwidth (BW) and thus also consume more power. In the second approach,

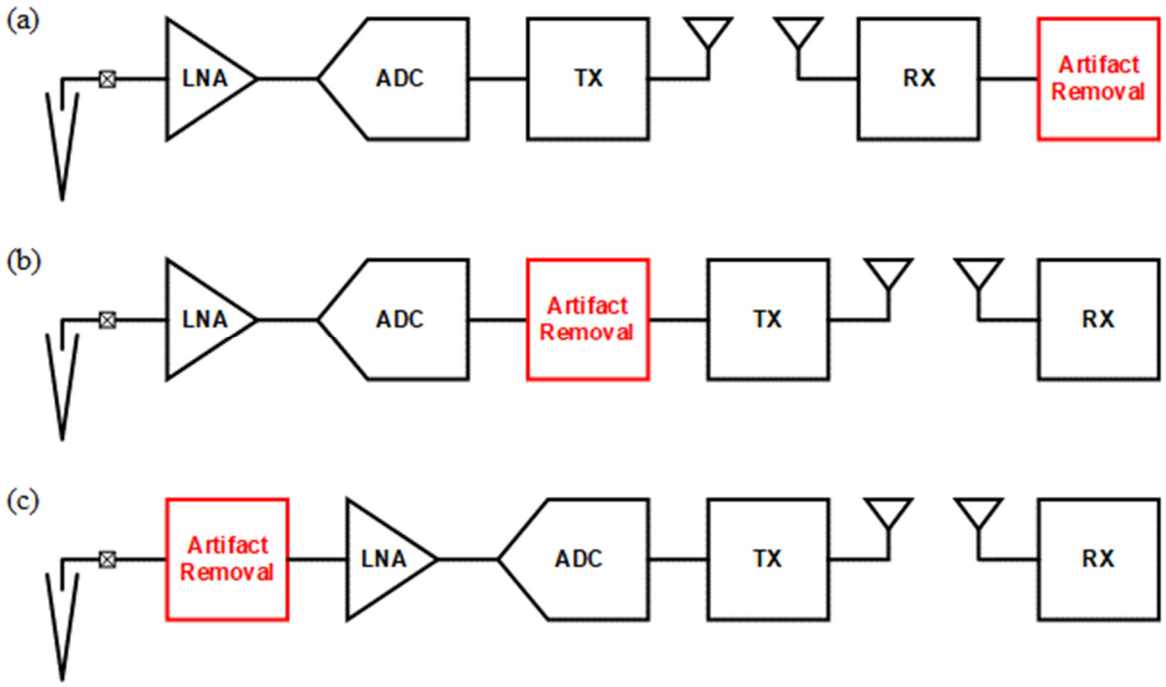


Figure 3-2. System-level approaches to artifact removal.

published in [32], the artifact removal algorithm is placed directly after the analog-to-digital converter (ADC). In this approach, the wireless module does not have to consume extra BW to accommodate the artifacts. In fact, this approach will also allow a full implementation of the closed-loop algorithm module within the node. Unfortunately, the power-hungry front-end module still needs to properly digitize the full signal with artifacts. This leaves us with the option of placing artifact removal before the initial amplification, as shown in Figure 3-2 (c). A proper implementation in the analog domain can greatly relax the constraints of the analog front-end amplification and analog-to-digital conversion.

Previous approaches to front-end artifact cancellation include signal blanking and symmetric sensing. In signal blanking, the input to the recording amplifier is simply turned off during stimulation [76], as shown in Figure 3-3 (a). While this prevents the amplifier from saturating and temporarily losing its input voltage bias, any signal appearing during the off-period is lost. In symmetric sensing (Figure 3-3 (b)), the recording and stimulation electrodes are placed

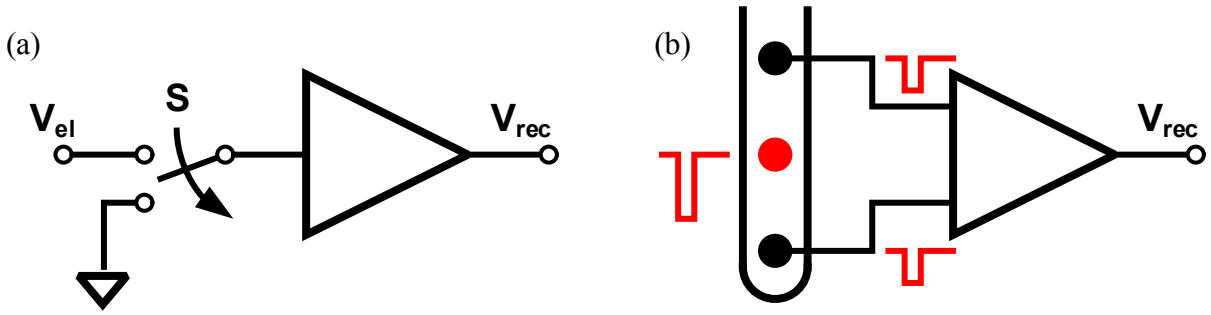


Figure 3-3. Previous front-end artifact rejection methods: (a) signal blanking and (b) symmetric sensing.

in a particular configuration to differentially cancel the artifact [77]. Here, the stimulation site is placed equidistantly between two differential recording sites so that the artifact equally couples onto each recording channel is rejected by the differential amplifier. While the neural signal is preserved in this scheme, it requires an inflexible electrode configuration that possibly hinders the effectiveness of the stimulation. Instead, we propose a universal architecture for artifact cancellation, which can be used in a wide variety of applications while preserving the recorded neural signal and avoiding the shortcomings of previous works.

3.2.3 Artifact Cancellation Algorithm

Our approach to artifact cancellation circuit stems from the similarity in coupling between stimulating and recording probes of a closed-loop stimulation microsystem to the near-end crosstalk (NEXT) problem in wireline communication systems. In NEXT, a strong transmitter output couples to the input of the sensitive receiver amplifier and corrupts the received signal, increasing the system's bit-error rate [78][79]. However, by utilizing the direct correlation between the transmitted signal and the observed artifact, a number of filtering techniques have been developed to cancel the artifacts. One such technique, called *adaptive noise cancellation*, learns the filtered crosstalk noise response of the channel and subtracts it from the recorded signal [80].

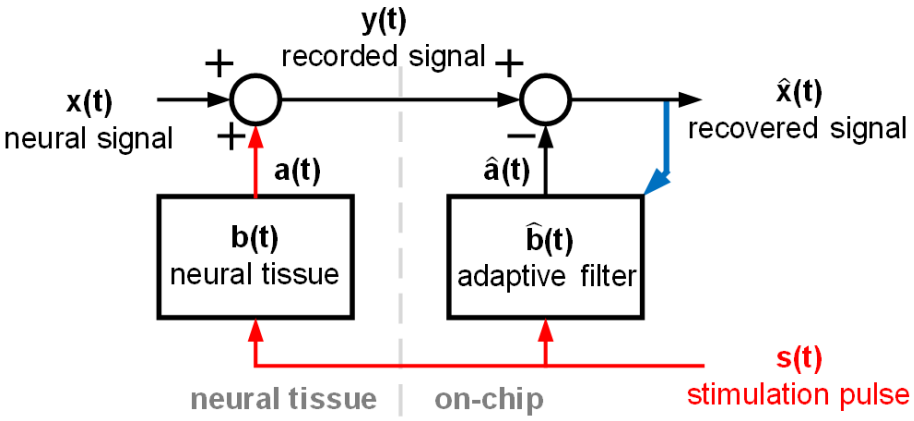


Figure 3-4. System diagram of stimulation artifact addition and cancellation through adaptive filtering. The recorded signal, $y(t)$, is the corrupted neural signal picked up at the tissue-circuit interface, while the recovered signal, $\hat{x}(t)$, is the on-chip recovered neural signal.

Due to its simplicity and general applicability, we apply a similar approach to cancel neural stimulation artifacts in an implantable neural interface [81].

Analysis of the algorithm begins with the simplification of neural tissue response to a linear, time-invariant (LTI) filter. The recorded signal, y(t), can be expressed as a linear sum of the neural signal x(t) and the artifact, a(t), as shown in Figure 3-4. Furthermore, the artifact a(t) can be expressed as a stimulation signal s(t) filtered by the neural tissue response b(t):

$$\begin{aligned} y(t) &= x(t) + a(t) \\ &= x(t) + b(t) * s(t). \end{aligned} \tag{3-1}$$

Adaptive noise cancellation artificially recreates the response of the neural tissue in order to subtract it from the corrupted signal. To perform this task, an adaptive filter, $\hat{b}(t)$ (in Figure 3-4), learns the impulse response of the neural tissue. When stimulation s(t) is fed through this filter, its output recreates the artifact $\hat{a}(t)$ and this recreated artifact is subtracted from the recorded signal to cancel the real artifact as shown in following equation:

$$\begin{aligned} \hat{x}(t) &= x(t) + a(t) - \hat{a}(t) \\ &= x(t) + b(t) * s(t) - \hat{b}(t) * s(t). \end{aligned} \tag{3-2}$$

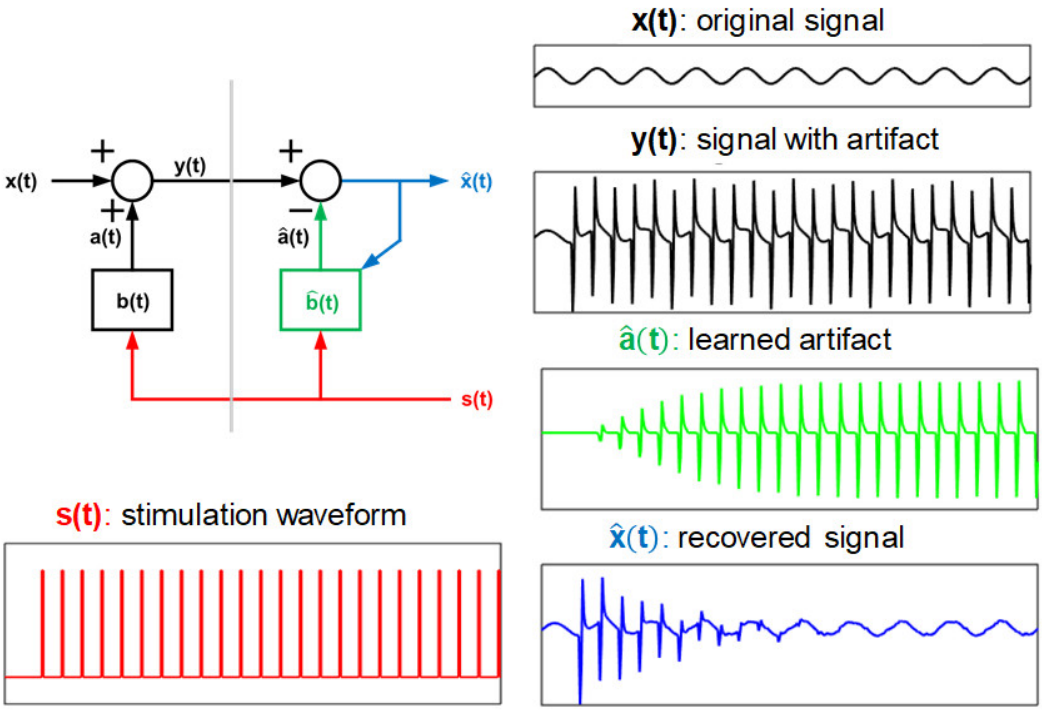


Figure 3-5. Simulation of the stimulation artifact cancellation algorithm with artificial neural data showing the system learning the response of the tissue.

By inspection of the equation above, when the fully-trained filter $\hat{b}(t)$ approximates the neural response $b(t)$, the stimulation term $s(t)$ is cancelled, and the recovered output signal $\hat{x}(t)$ approximately equals the original neural signal $x(t)$.[2]

A key block in adaptive noise cancellation is the learning algorithm of the adaptive filter. The Least Mean Squares (LMS) learning algorithm, first presented by Widrow, et al. and extensively used in telecommunications, is simple and reliable [82]. In LMS, the adaptive filter coefficients are updated every cycle to better approximate the desired response. The update quantity is derived by applying the steepest gradient descent approach to minimize power of the

[2] It is important to note that while the actual non-artifact neural response is also correlated to the stimulation signal, it is much delayed and not LTI; if the filter length is kept short enough, the real neural signal is not cancelled. The neural signal will thus be omitted in further explanation.

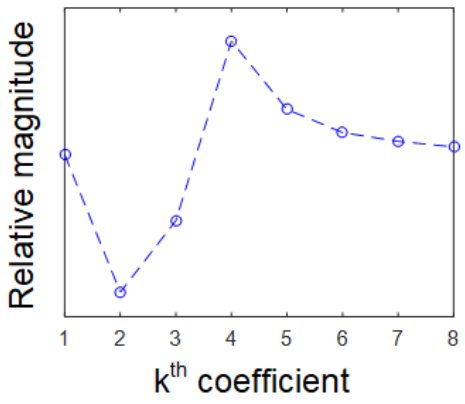


Figure 3-6. The final impulse response of the adaptive filter after training resembles the artifact waveform.

noise error, $\hat{x}(t)$. As shown in [81], the online LMS algorithm predicts the coefficient update, needing only the value of the recovered output signal $\hat{x}(t)$ from the previous cycle and the stimulation input s(t) as shown:

$$\hat{b}(t+1) = \hat{b}(t) + \mu s(t)\hat{x}^*(t). \quad 3\text{-}3$$

The adaptation constant μ is an adjustable knob for the user to trade adaptation speed for accuracy. A simplified version, called sign-sign LMS, eases the hardware requirements by performing computation on a sign-bit signal representation, resulting in the following update equation [83]:

$$\hat{b}(t+1) = \hat{b}(t) + \mu\left(s(t) \times \text{sign}\left(\hat{x}(t)\right)\right). \quad 3\text{-}4$$

To show the effectiveness of the scheme, the algorithm is simulated with pre-recorded neural data, as shown in Figure 3-5. We artificially corrupt a known signal (here, a sinusoidal wave for clarity) with pre-recorded artifact waveforms, added at predetermined times that are correlated to the stimulation waveform. As the algorithm runs for a few stimulation cycles, the filter output begins to resemble the added artifacts. In fact, the plotted impulse response of the adaptive filter at the end of simulation in Figure 3-6 resembles a single added artifact, since the filtered artifact waveform is simply a pulse train convolved with a single 8 sample long artifact-shaped sequence. Furthermore, the recovered signal shows a decrease in correlated cross talk noise without

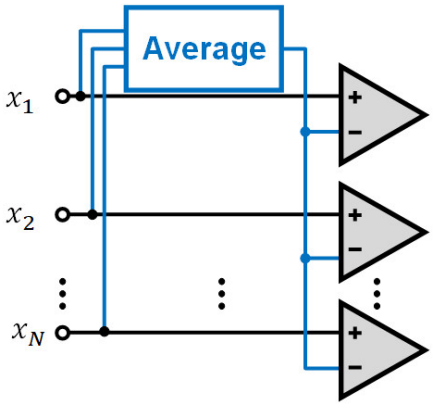


Figure 3-7 Top-level diagram of common average referencing (CAR) algorithm.

significant distortion of the original uncorrelated signal.

The selection of the adaptive filter length was guided by maximizing the subtraction of artifact without removing the desired evoked neural potential. An analysis of typical electrocorticograph (ECoG) and local field potential (LFP) signals showed a 2 ms period between the stimulation pulse and earliest neural response, and during this time period the artifact can be safely removed. Because the filter is sampled at the ADC frequency of 4 kHz, an 8-tap filter is sufficient to attenuate most artifacts while preserving the non-artifact neural response.

3.3 Common Mode Noise Rejection

As studied in [84], various environmental noise sources such as power lines and fluorescent lights capacitively couple onto the electrodes, the electrode wires, and the preamplifier inputs, potentially causing large amplitude common-mode noise. This noise can be cancelled through differential recording, where noise in two neighboring channels is rejected as common mode signal. Inconveniently, differential recording requires the user to double the number of electrodes and may also remove important signals shared between the channels. As a compromise, a large single reference electrode is often used to subtract the reference noise from multiple channels without introducing localized neural signals. Unfortunately, because of the impedance mismatch

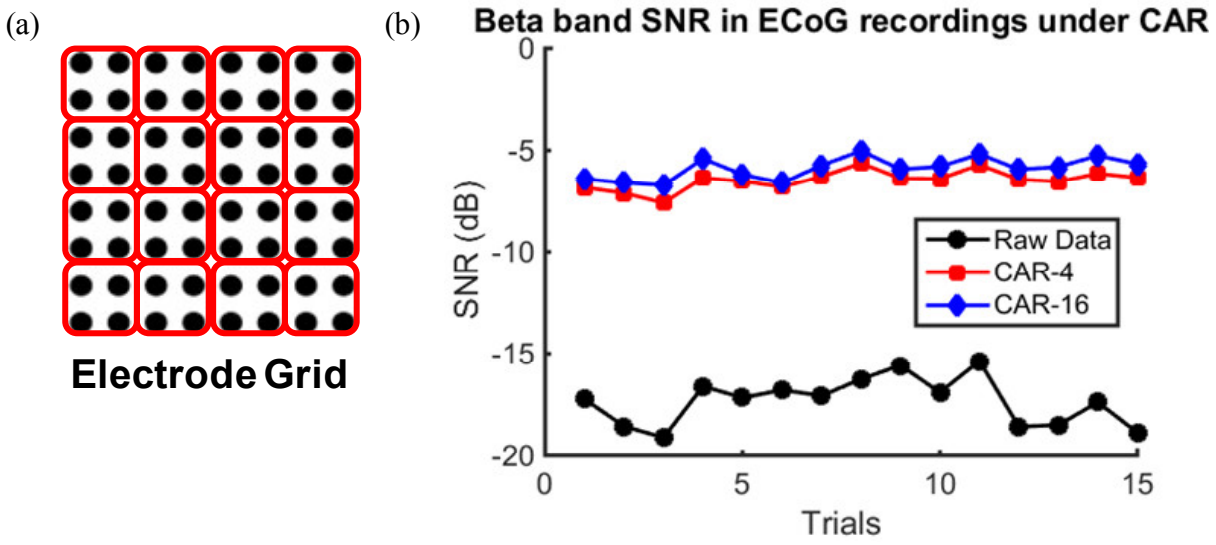


Figure 3-8. (a) CAR-4 4-channel groupings mapped onto an ECoG electrode grid, and (b) comparison in SNR of ECoG recordings between raw data, active CAR-4, and active CAR-16 algorithms.

between the recording and reference electrodes, line noise couples differently to the positive and negative inputs.

Instead of relying on a single electrode to provide an accurate reference signal, we can create a new reference signal from the existing channels. [85] creates this new reference signal in a software post-processing scheme called Common Average Referencing (CAR). CAR has become a common step in signal conditioning in neuroscientific literature [86][87]. As shown in Figure 3-6, the new reference signal is computed by averaging neighboring channels and subtracting this average from every channel. If used properly, the average holds most of the common mode noise and little of neural signal, thus providing a clean, stable reference signal.

While it has been previously implemented as a software post-processing step, we implement CAR at the recording front-end. By cancelling the noise before final amplification and digitization, the dynamic range constraints of the analog circuitry can be greatly relaxed. Challenges include unintended signal cancelation if the CM signal itself is of importance – this can be alleviated by

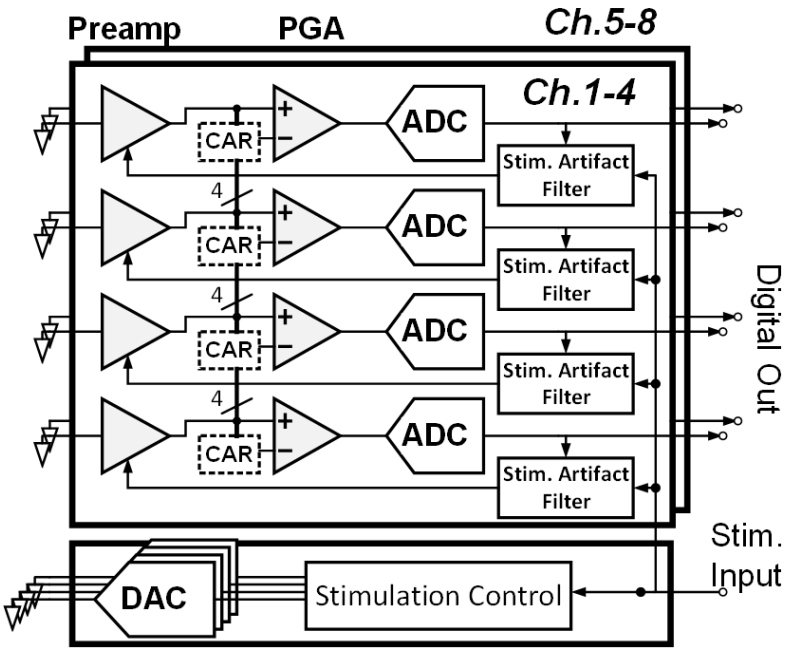


Figure 3-9. Top-level system architecture.

averaging enough channels so that the average contains a minimal amount of localized neural signal. Analysis of experimental neural data (Figure 3-8) shows that even a 4-channel CAR (CAR-4) can substantially improve SNR, while the use of 16-channel CAR (CAR-16) only slightly further increases SNR. This relatively small number of needed channels allows us to minimize the circuit area for CAR as described in section IV.B. The common average reference can also be contaminated by a single very strong, or perhaps broken, channel. For this reason, the user should be able to eliminate that channel from the average calculation so that the noise does not bleed into other channels.

3.4 Circuit Implementation

The proposed system architecture, shown in Figure 3-9, consists of 8 recording channels and 4 stimulation channels. Each recording channel consists of a preamplifier with a gain of 100, a programmable gain amplifier (PGA) with gain ranging from 1 to 10, and an ADC. The bandwidth of the preamplifiers is deliberately limited to a range of 1Hz to 2kHz to pass electrocorticograph

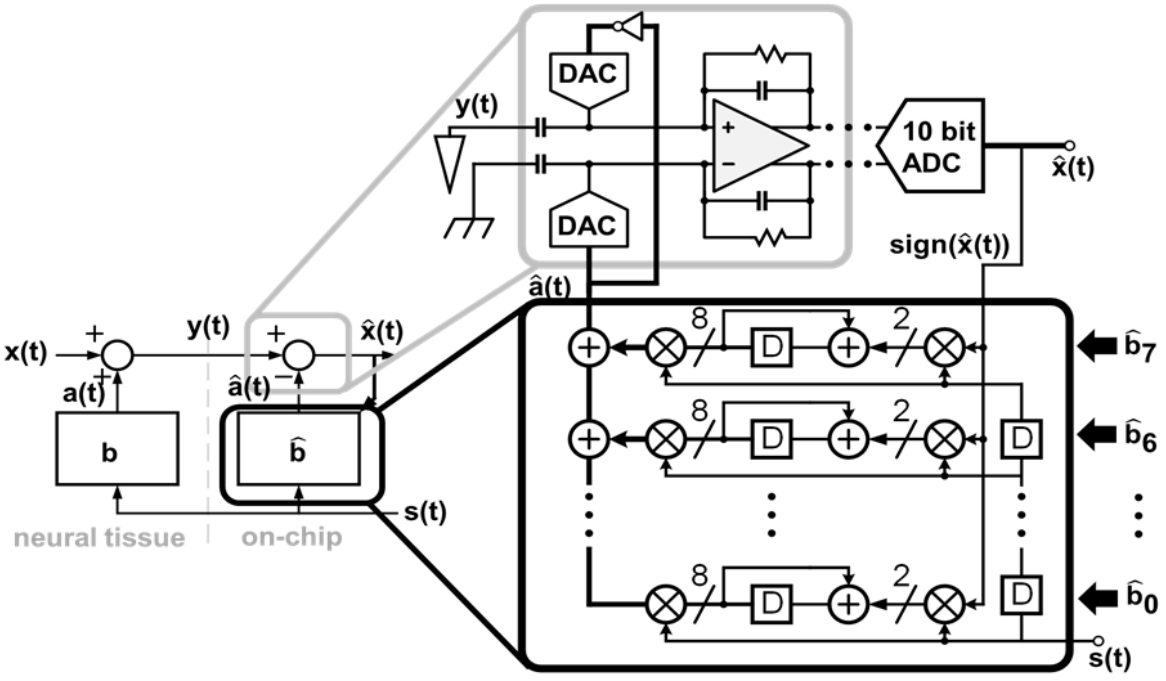


Figure 3-10. Schematic of stimulation artifact cancellation circuit. Analog subtraction is framed in gray while the adaptive filter is framed in black.

(ECoG) and local field potiental (LFP) signals, which are most commonly used for neuromodulation control. The sampling rate of the ADC is set at 4 kS/s to properly sample the neural signals without aliasing. The resolution of the ADC is set to 10 bits to maintain the channel input-referred noise below 5 μV_{rms} (i.e. below the biological noise limit) while providing the ADC differential input dynamic range of 1V. The recording channels are split into two groups of 4 channels. In each group, every channel can be referenced to an average formed from any combination of these channels. The CAR circuit is placed after the preamplifier and before the PGA to remove the noise before final amplification and digitization. A stimulation artifact cancellation filter is implemented for every individual channel, as we cannot expect a similar coupled stimulation artifact for each channel. The stimulation data input is fed into the stimulation control block and also to the bank of stimulation artifact cancellation filters. Lastly, the stimulation channels themselves consist of current DACs and digital timing and control circuitry. The current

DAC resolution of 7 bits and dynamic range up to 8 mA are enough for most neuromodulation applications.

3.4.1 Stimulation Artifact Cancellation Circuit

The stimulation artifact cancellation scheme is implemented with the mixed-signal circuit shown in Figure 3-10. First, the single-bit stimulation input s(t) is fed through the digital adaptive filter. The filter output, or the digitally recreated artifact $\hat{a}(t)$, is converted into a differential analog signal using two digital-to-analog converters (DACs). This analog artifact replica is then subtracted from the corrupted neural signal at the preamplifier input to prevent signal saturation in the channel. Finally, the sign of digitized recovered signal, $\hat{x}(t)$, (from the 10-bit ADC) and single-bit stimulation signal, s(t), are fed to the adaptive filter to train its coefficients.

A pair of capacitive digital-to-analog converters (DACs) converts $\hat{a}(t)$ into a differential analog signal. The DAC's 8-bit resolution is chosen to reduce artifacts by up to 42 dB. From data analysis, this is sufficient to prevent channel saturation in most situations. While an increase in resolution would only result in a marginal increase in power consumption (less than 1nW per channel for every additional bit), the area of the DAC would increase exponentially with extra resolution, since the LSB capacitor size is limited by mismatch. The 8-bit DAC resolution allows us to keep the area of the DAC below 12% of the complete channel layout area. A further advantage is that the capacitive DAC architecture offers the ability to scale the DAC LSB size, which corresponds to the μ step size of the learning algorithm in equation 3-4, by adjusting the capacitive DAC reference voltage.

A standard 8-tap LMS digital adaptive filter nominally requires 16 multipliers and 15 adders to perform necessary computations, significantly contributing to the system power consumption

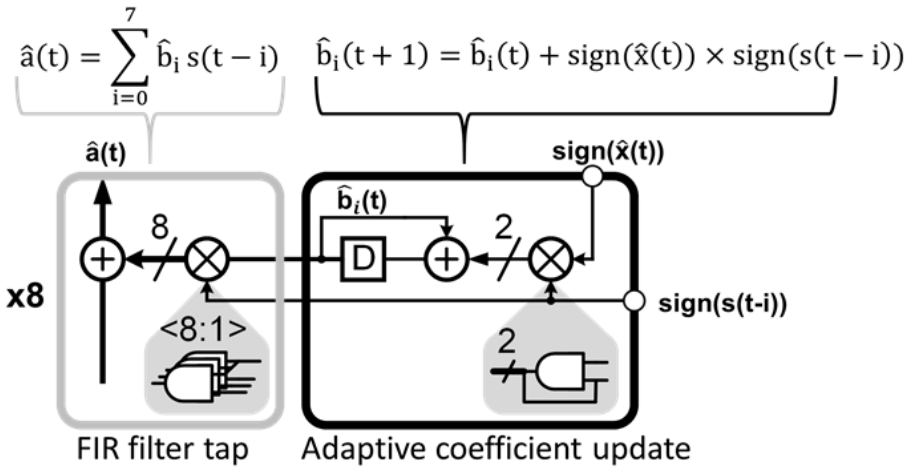


Figure 3-11. Schematic of a single filter tap implementing LMS update and filter multiply and accumulate.

and area. To minimize this overhead, we propose a simplified parallel architecture that eliminates computation elements by utilizing the sign-sign LMS algorithm in equation 3-4 that takes advantage of the simplified single-bit inputs.

First, the adaptive filter coefficients are updated by the following matrix combination:

$$\begin{bmatrix} \widehat{b_0}(t+1) \\ \widehat{b_1}(t+1) \\ \vdots \\ \widehat{b_7}(t+1) \end{bmatrix} = \begin{bmatrix} \widehat{b_0}(t) \\ \widehat{b_1}(t) \\ \vdots \\ \widehat{b_7}(t) \end{bmatrix} + \mathrm{sign}\big(\hat{x}(t)\big) \begin{bmatrix} s(t) \\ s(t-1) \\ \vdots \\ s(t-7) \end{bmatrix}. \qquad 3\text{-}5$$

The sign of the error (or recovered) signal $\hat{x}(t)$ is represented by the MSB of the recorded signal, and it is taken directly from the ADC output. The single-bit stimulation input, which represents a stimulation pulse with 1 and a lack of stimulation with 0, is fed from the stimulation circuit and is appropriately delayed by a shift register for each of the 8 taps. The 8 coefficient updates in equation (6) are then computed in parallel. Figure 3-11 shows the hardware implementation of a single filter tap and coefficient update. On the right of Figure 3-11, the single-bit $s(t-i)$ input is multiplied by the sign of $\hat{x}(t)$. This multiplication, performed only with a single AND gate and a direct node

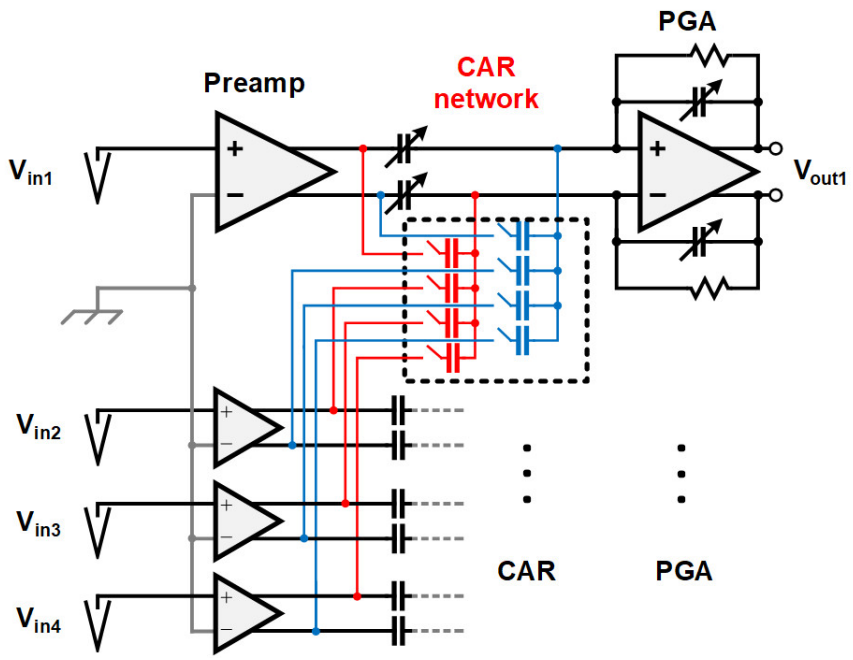


Figure 3-12. CAR circuit implementation: the averaging CAR network is implemented for each channel in the group as shown for channel 1.

connection, yields a 2-bit number representing -1, 0, or +1. This product is then added to the 8-bit $\widehat{b_1}(t)$ coefficient, computed and stored in the previous cycle, creating a new updated coefficient $\widehat{b_1}(t+1)$.

Next, the $\hat{b}(t)$ coefficients are fed to the FIR filter to compute the artifact replica using the following FIR filter matrix multiplication:

$$\hat{a}(t) = [\widehat{b_0}(t) \quad \widehat{b_1}(t) \quad \cdots \quad \widehat{b_7}(t)] \begin{bmatrix} s(t) \\ s(t-1) \\ \vdots \\ s(t-7) \end{bmatrix}. \qquad 3\text{-}6$$

The computation above is implemented with 8 multipliers and 7 adders. Similarly to the coefficient update described above, the multiplication and addition is performed in parallel for each tap, using a total of 8 multipliers and 7 adders. However, the single tap FIR filter multiplication is implemented with only 8 AND gates, as shown in Figure 3-11 on the left, since it uses a single-bit

stimulation signal $s(t-i)$ as the second operand. Finally, the seven 8-bit ripple-carry adders sum the multiplier outputs to create $\hat{a}(t)$.

In summary, the full adaptive filter uses only 15 ripple-carry adders and no full multipliers. Because the filter runs at the very low ADC sampling frequency (4 kHz), the gates are minimum-sized to further reduce power consumption. Since most logic gates are active only when non-zero bits appear in the stimulation waveform, the average power consumption at conventional stimulation rates is below 11nW and is almost negligible in comparison with the power consumption of the rest of the system.

3.4.2 Common Average Referencing (CAR) Circuit

CAR is implemented at the input of the second stage amplification to relax the dynamic range of the PGA. The circuit implementation is shown in Figure 3-12. Preamplifier outputs from 4 neighboring channels are fed into a capacitive averaging network, one per channel. An advantage of this approach is that it is passive and does not add to the total power consumption. Moreover, the switchable capacitor array allows full reconfigurability in case undesirable channels should be disconnected. The additional capacitors increase the area of the recording channel by less than 3% if number of references is kept at 4 (sufficiency of this number of references is shown in section 3.3). Furthermore, these capacitors can be placed above the active circuitry to further save area. The averaged output is fed into the input of the PGA with opposing polarity alongside the original preamplifier connection to effectively subtract the CAR signal. To maintain the proper functioning of the averaging when changing the number of reference channels, input and feedback capacitors are connected or disconnected to maintain constant gain. Also, the output impedance of the preamplifiers must be low enough so that the changing preamplifier output load due to switching capacitors does not significantly affect the bandwidth.

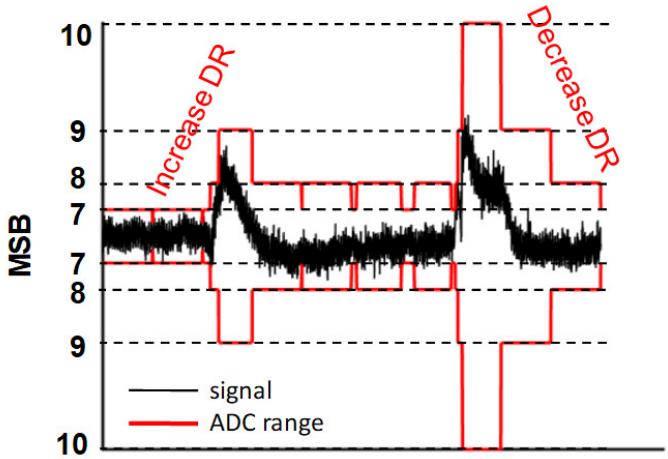


Figure 3-13. Example of Range-Adapting (RA) SAR ADC range (MSB) following the shape of a neural signal.

3.4.3 Range Adapting (RA) SAR ADC

To further lower the average power consumption of recording channels, we also propose a new adaptive ranging technique for SAR ADCs. Typical recording channels must have a high dynamic range to process large signal amplitudes due to artifacts or periods of high neural activity. However, because high-amplitude activity in neural signals is relatively sparse, this high dynamic range is often underutilized. By adapting the dynamic range of the ADC to the signal, we can minimize the effective number of bits evaluated by the SAR algorithm and save power. Such system can be also applied to other types of sparse signals where the activity is low for majority of the time.

3.4.3.1 Range-Adapting Algorithm

The range-adapting algorithm adjusts the ADCs dynamic range (DR) in two ways, as seen in Figure 3-13. DR is automatically increased when a sample is detected to be out of range. DR can also be decreased between sampling cycles with an off-chip controller. Such a controller, for example, can predict periods of low activity and reduce the range accordingly. In our simple implementation, a timer is set to decrease the dynamic range by a single bit every 200 milliseconds.

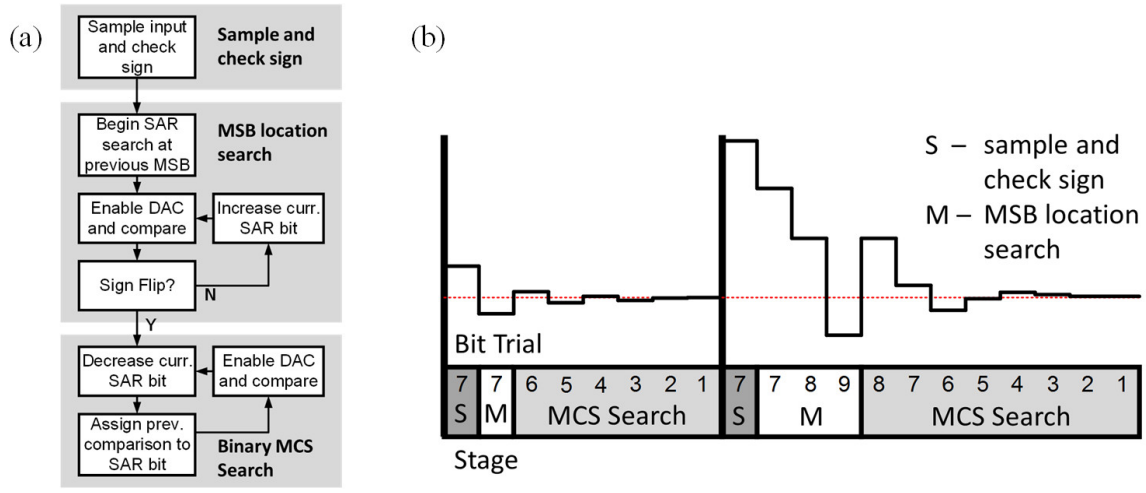


Figure 3-14. (a) Range-Adapting (RA) SAR algorithm logic flowchart and (b) comparator input voltage during RA SAR A-to-D conversions for in-range and out-of-range samples respectively. The conversion phases and bit cycles are also shown.

Any algorithm which would adjust the range to fit the approximate envelope of the signal may be considered desirable; however, such algorithm should not alter the ADC's range at every sample since every range calculation requires extra logic power and it can dominate ADC power consumption.

3.4.3.2 Range Adapting SAR Switching Scheme

The range adapting algorithm is easily implemented in a SAR ADC with a modified capacitor DAC switching scheme by taking advantage of a specific application-adapted binary search, similar to [88]. Our scheme is divided into 3 phases outlined in Figure 3-14 (a), namely: (1) sample and sign check phase, (2) MSB range search, and (3) binary LSB search. Figure 3-14 (b) shows two conversion examples for an in-range and out-of-range samples by tracking the comparator input voltage. First, stage (1) finds the sign of the sampled voltage. The sign determines which direction the capacitive DAC changes the comparator input voltage for each SAR bit. Only in stage (2), does the algorithm search for the location of MSB. The search algorithm makes its initial guess based on the previous sample MSB location which is stored in between samples (bit

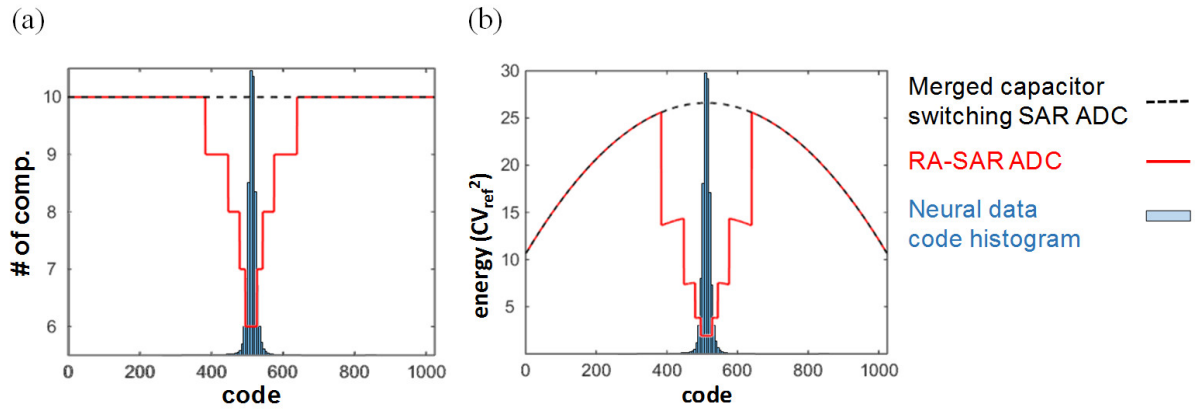


Figure 3-15. Simulated minimum (a) number of comparisons and (b) capacitive DAC switching energy for 10 bit RA SAR ADC as compared to a merged capacitor switching SAR ADC. Overlaid neural data code histogram show most data falls within the most efficient code range.

7 for both cases in the example). The DAC assigns the previously found sign bit to the current MSB location, and the comparator checks if the polarity has changed. If it does not change, the algorithm performs additional trials by increasing the MSB location, switching in the appropriate capacitors in the DAC, and observing the comparator result. When the comparator output finally changes, or when the maximum MSB is reached, the algorithm keeps the found MSB and moves on to stage (3). At this time, operating in stage (3) the ADC performs the traditional binary search from the current MSB to determine the remaining bits. In our scheme, the merged capacitor switching (MCS) scheme is used to minimize capacitor switching and power consumption [89].

3.4.3.3 ADC Power Consumption

Figure 3-15 demonstrates the possible power reduction in a RA SAR ADC. Figure 3-15 (a) plots the minimum number of comparisons in the case of correct initial range guess for every code in the 10-bit ADC. Note that the minimum initial guess is kept at the 6th bit because neural signals rarely maintain lower amplitudes. The biggest power reduction when compared to a traditional

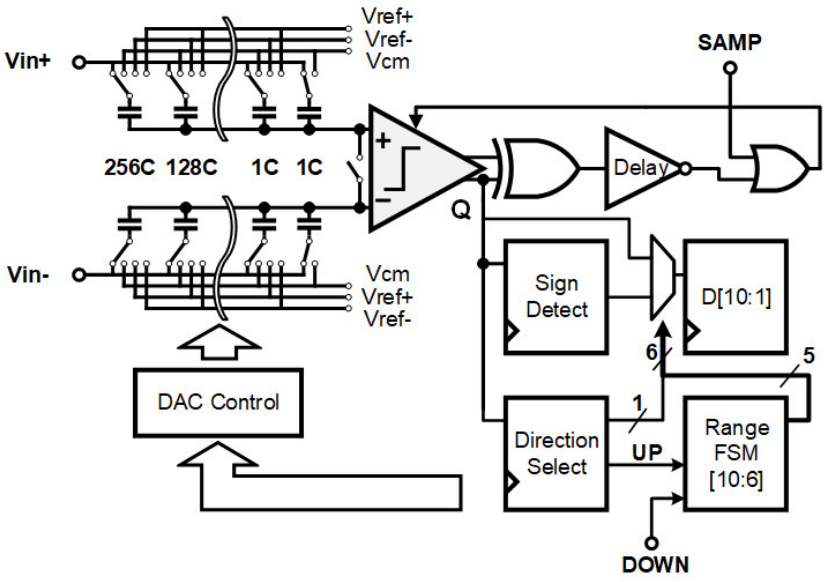


Figure 3-16. RA SAR ADC architecture schematic.

MSC SAR ADC scheme is observed for small input signals. This is due to the reduced number of significant bits checked by the RA algorithm.

A code histogram of previously recorded neural data is overlaid to show that a great majority of the signal does fall in the power-saving range. In fact, simulations showed a 25% reduction in the average number of comparisons. In Figure 3-15 (b), the capacitive DAC switching energy per code is plotted for the MCS and RA switching schemes. Similarly, the greatest power savings are found in the middle codes. A 72% reduction in average DAC power consumption is observed.

3.4.3.4 ADC Circuit Implementation

The SAR ADC is implemented in differential fashion and employs bottom-plate input sampling to reduce parasitic error (Figure 3-16). The ADC also uses an asynchronous architecture. At the beginning of every sample, the sampling clock triggers a self-timing delay loop that first clocks the comparator. When the comparator makes the decision, it activates the SAR logic and

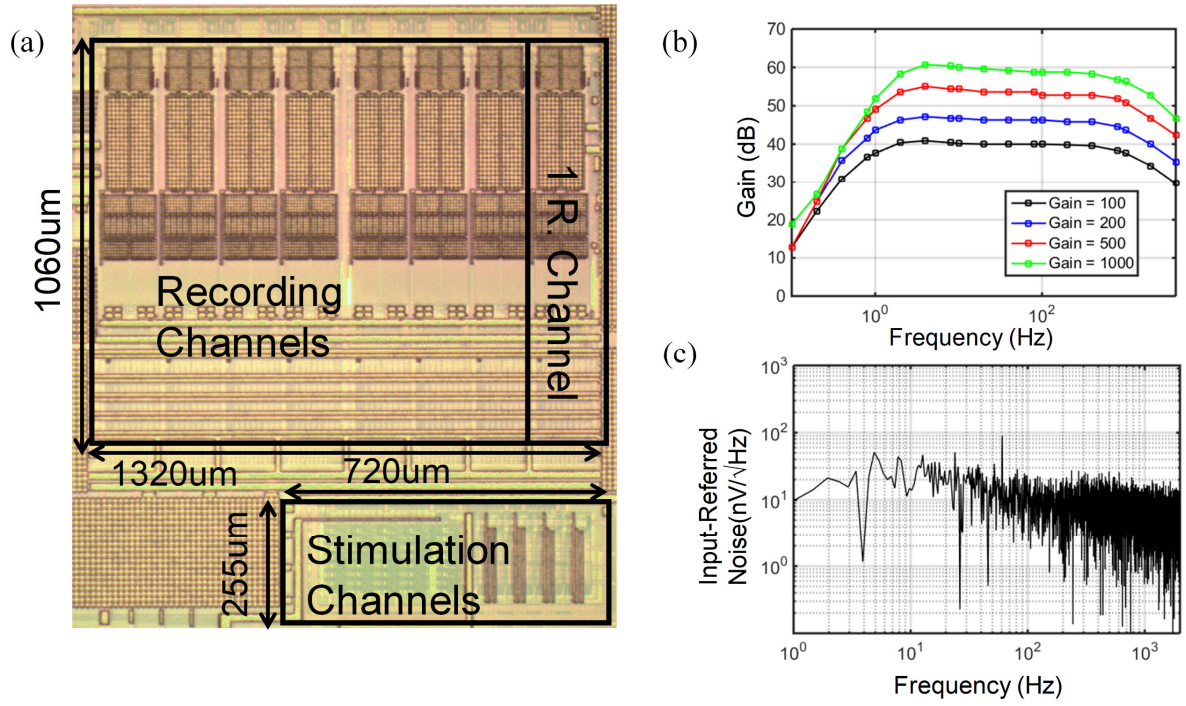


Figure 3-17. (a) Chip microphotograph, (b) Recording channel frequency response for 4 gain settings measured at ADC output and (c) input-referred noise of the full recording channel.

sends a signal through an inverter-based delay line to give time for settling of the capacitive DAC and to re-trigger the comparator for the next bit conversion cycle.

The SAR logic executes the range-adapting algorithm. The stages of the algorithm are controlled by the "direction select" flip-flop and logic. In stage (1), the comparator output Q is stored onto the "sign detect" flip-flop. After that, the "direction select" state tells the SAR logic to assign the sign bit to the current MSB location stored in a finite state machine (range FSM). The range FSM is a 5-bit one-hot counter that saves the MSB location in-between ADC samples and it increases or decreases its value as required by the RA algorithm. A mux, controlled by the range FSM and the "direction select" flip-flop, selects the SAR flip-flops that will be assigned the sign bit. As the logic detects the comparator polarity change at the end of stage (2), the "direction select" flip-flop changes its state and begins the MCS search of stage (3), finds the remaining bits, and stores them into the 10-bit SAR flip-flops. In between the samples, the range FSM can be

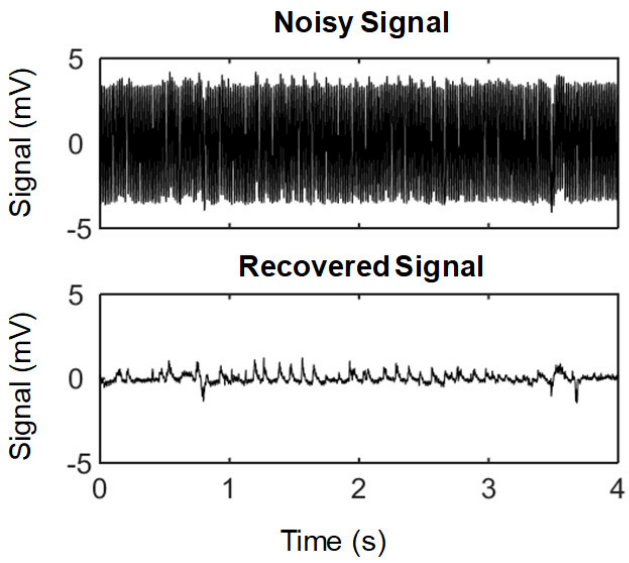


Figure 3-18. Full channel recording before and after activating the 4 channel CAR circuit, showing the common mode (60 Hz) noise reduction in *in-vitro* recording.

externally triggered by the DOWN control input to decrease the initial MSB location to be used in the next sample conversion.

3.5 Measurements

3.5.1 System Performance

The prototype is fabricated in 0.18 µm CMOS. Figure 3-17 (a) shows the chip microphotograph. The total area of the recording circuit is 1.4 mm^2 or 0.17mm^2 per channel, while the area of the stimulation circuit is 0.18mm^2. Figure 3-17 (a) shows the measured frequency response of the recording channel for 4 gain settings: 100, 200, 500, and 1000. Each of the gain settings maintains a bandwidth of 1Hz-2kHz. Figure 3-17 (b) shows the input-referred noise of the full recording channel at the ADC output with a shorted input. The total measured input-referred noise is 3.05 μV_{rms} between 1Hz and 2kHz. The measured power consumption per recording channel is 0.33 µW.

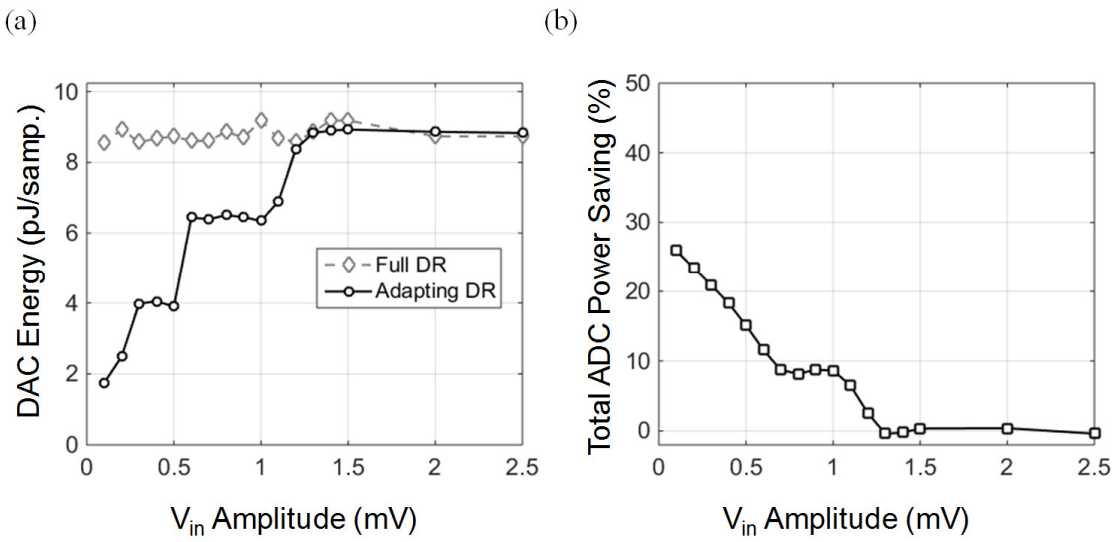


Figure 3-19. ADC measurements showing (a) capacitive DAC energy consumption per sample for enabled/disabled adapting DR algorithm for amplitude-swept sinusoid input and (b) the ADC total power savings.

3.5.2 CAR Circuit Measurements

An in-vitro experiment with a 4-channel recording was conducted to test the functionality of the CAR circuit. The 4 channel waveforms were constructed from a synchronized 60 Hz noise signal. A prerecorded neural signal was then added to one of the channels. The top plot in Figure 3-18 shows the channel with merged 60 Hz noise and the prerecorded signal. When CAR is switched on for the 4-channel group, as shown in bottom of Figure 3-18 the averaged reference reduces the recorded 60 Hz power by -36 dB, effectively increasing the recording channel SNR by the same amount.

3.5.3 ADC Measurements

The average power consumption of the ADC is 89 nW when measured at 4kS/s for a full-range sinusoid input. To test the functionality of the range-adapting algorithm, the channel input signal amplitude is swept while monitoring the power consumption of the full ADC and DAC. Figure 3-19 shows a significantly reduced DAC energy consumption for low amplitude inputs (by

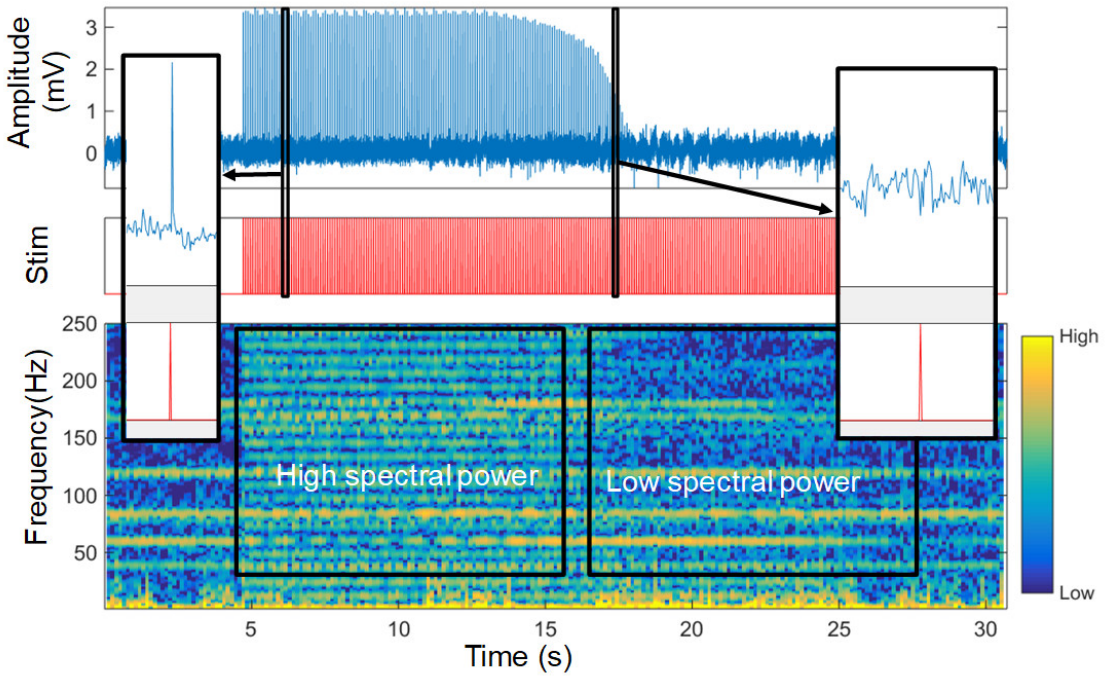


Figure 3-20. *In-vivo* experiment results showing stimulation artifact cancellation learning process for 12 Hz 600 μA biphasic stimulation. Top plot shows the raw time-domain plot of the recording output, middle plot shows the stimulation timing, and the bottom plot shows the recorded output spectrogram.

more than a factor of 4). The shape of the plot is similar to the predicted DAC energy consumption from Figure 3-15. This amounts to total ADC power consumption saving of more than 25% for low-amplitude inputs.

3.6 *In-vivo* Measurements

A series of *in-vivo* tests were performed to test the system functionality in a real application. Recordings were taken during the stimulation of a rat hippocampus as the rat was under chemically-induced seizures[3]. Seizures were induced following the injection of 4-aminopyradine unilaterally into the CA3 region of the hippocampus. The stimulation was then applied to the

[3] The *in-vivo* experiments were performed at the Netoff Epilepsy and Neuroengineering Lab at University of Minnesota under the approval from the Institutional Animal Care and Use Committee.

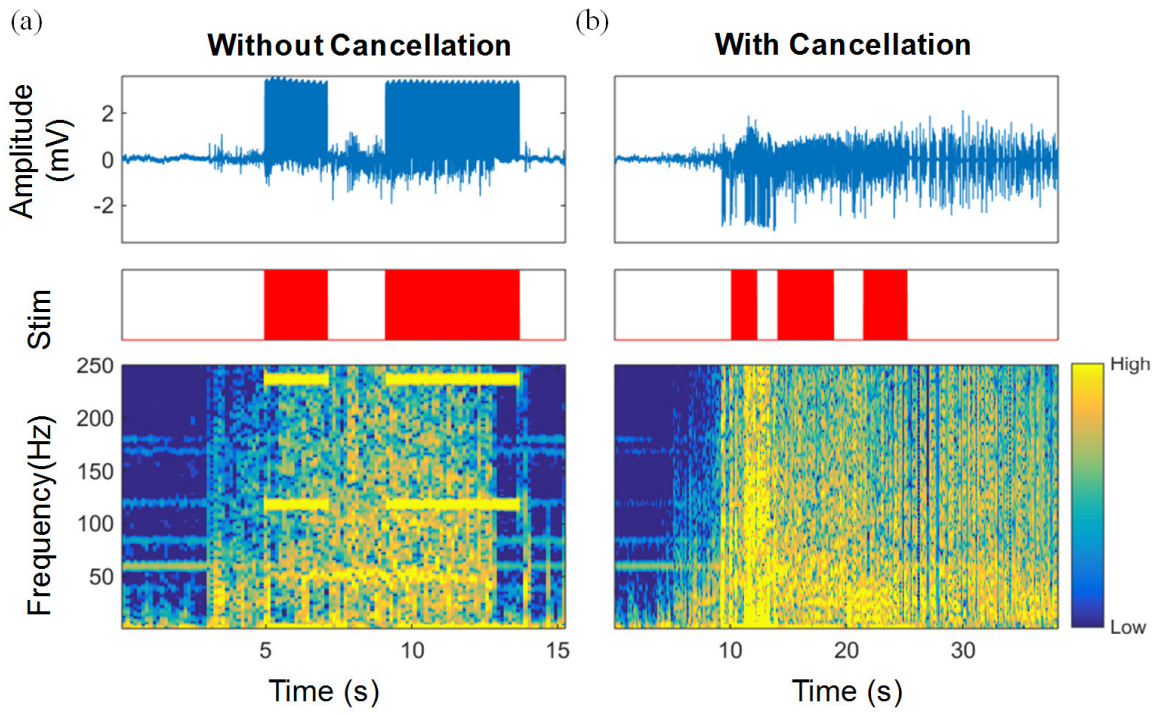


Figure 3-21. Neural recordings of 120 Hz 600 µA biphasic stimulation during seizure activity (a) without activate artifact cancellation and (b) with active artifact cancellation.

ventral hippocampal commissure (VHC) which bilaterally innervates the CA3 regions where the seizures are induced. A recording electrode was placed in the CA1 region of the hippocampus, close to the injection region. In this setup, the recording electrode has a clear recording of the seizure activity and the proximity of the recording and stimulation electrodes results in large stimulation artifacts that test the artifact removal algorithm.

In initial experiments, recordings were taken when stimulating the tissue as the artifact cancelling algorithm trained the filter weights. In Figure 3-20 a 12 Hz 600uA biphasic pulse stimulation train is applied and the response is recorded in time and time-frequency domain. As the stimulation begins in the 5th second, large artifacts clearly dominate the recorded waveform. Because the artifacts are being clipped at the start of stimulation, the reduction of artifacts is not apparent until the 15th second as the filter weights become large enough to successfully reduce the recorded artifacts. When the filter weights approach their steady-state values, the artifacts are

Table 3-1. Performance Summary and Comparison with Other Recent Works

	[90]	[91]	[92]	**This Work**
Technology	0.18 μm	0.13 μm	65 nm	0.18 μm
Area (per recording ch.) (mm^2)	~0.42	~0.625	0.025	0.17
Rec. Power (μW/ch.)	7.35	4.2	2.3	0.33
BW (Hz)	~0.5-7k	0-320	1-0.5k	1-2k
IR Noise (μV_{rms})	5.23	2	1.32	3.05
Stimulation Artifact Cancellation	No	No	No	Yes
CAR	No	No	No	Yes

reduced to the below-noise level. In a latter experiment, shown in Figure 3-21, we stimulated the brain with and without cancellation as the seizures where episodically occurring. The non-cancelled artifacts from the 120 Hz stimulation clearly dominate the seizure activity both in time and frequency domain. After the cancellation filter is turned on, the artifacts disappear below the visible seizure signal, clearly showing the improved signal quality as the seizure signal becomes unobstructed by the artifact peaks. Across trials, artifacts are suppressed on average by at least 24dB; however, this number could be even higher if not for the high biological noise masking the suppressed artifacts. Note that the full learning process needs to be performed only once after implantation, as the neural tissue response does not change significantly during chronic use of stimulation[4].

3.7 Conclusions

We present a new bi-directional neural interface circuit for closed-loop stimulation. The microsystem introduces novel architectural features to combat environmental noise such as stimulation artifacts and cross-channel common mode noise, allowing overall proper closed-loop control. The circuit also includes a new Range Adapting (RA) SAR ADC to reduce power

[4] When the filter coefficients reach a steady state, the adapting algorithm can be turned off to maintain their constant value. It can also be periodically turned on to adapt coefficients to a slowly changing neural tissue response.

consumption. The system was fully characterized and verified *in vivo*. Table 3-1 summarizes and compares few key specifications with previously published works highlighting the state-of-the-art performance. Our work maintains a relatively low area and low noise in comparison with the published ECoG recording ICs in [90]–[92]. However, at lower power consumption, the system implements new functionality which enables the use in a wider variety of applications.

CHAPTER 4[5]

Miniature Headstage for High Resolution Closed-Loop Optogenetics

4.1 Introduction

As we mention in Section 2.3.2, optical stimulation has become a popular neuromodulation technique in the neuroscience community. Compact bidirectional neural interfaces can be applied for optogenetic systems, where neural activities are optically modulated and electrically monitored. Researchers have developed a variety of such interfaces ranging from multi-functional optical fibers [93] to transparent shanks in Utah-probe-like arrays [94]. Recent publications have attempted to integrate small light sources and recording electrodes onto small microfabricated probe shanks [40], [95]. [40] has monolithically integrated several neuron-size (~10 μm) light-emitting-diodes (μLED) precisely positioned in the vicinity of recording sites within photolithographical resolution (< 1 μm), enabling high-spatial-resolution optical stimulation and electrical recording for local circuit analysis [40].

In addition to the physical implantable probe arrays, a custom electronic system is required to interface the transducers with a host controller for closed-loop optogenetic studies. The light sources need to be driven by precise current sources with real-time control of amplitude, timing and shape. Simultaneously, neural recording front-ends should be able to amplify, digitize, and transmit the recorded signals to the host with high fidelity.

[5] Some of the material in this chapter is co-written by Kanghwan Kim.

To date, the commercial systems such as Plexon's PlexBright or Blackrock's CerePlex's offer optogenetic stimulation capabilities, but in a large form factor and with limited channel counts. A few publications have attempted to scale down the size of system by integrating active circuitry on a headstage. In [41], a 2 channel stimulator chip was designed for a wireless fiber-based optogenetic stimulation system, while in [42] and [43], commercial off-the-shelf (COTS) components are integrated on miniature printed circuit boards (PCBs) to perform the same function. While these systems achieve significant size reductions, they suffer from low stimulation channel count and no recording capability. [96] proposes to increase the stimulation channel count by placing 18 μLEDs on a CMOS-fabricated probe shank with a fully-integrated electronic back-end. In [44], a μLED-coupled waveguide microneedle array probe is integrated with a wireless LED driver ASIC, but a separate commercial recording system is used to interface with the recording sites over long wire leads, preventing the system's use in behavioral studies. [45] includes an on-board a COTS amplifier chip for neural recording in addition to the LED drivers. However, the system's capabilities are reduced by a bulky single-channel light source. Systems in [46], [47], [97] add full wireless capability to the bidirectional headstage concept; however, the use of COTS components and probes, and the limitations of wireless transceivers hinder high channel count integration. In [48], a custom 6-recording-channel and 4-stimulation-channel probe-back-end chip is used to provide high-precision control for a hybrid LED/recording site electrode. This probe and system, however, are not verified *in vivo*.

While the aforementioned systems have made big strides in miniaturization and improvement of bidirectional opto-electrophysiology, there is still an unmet need for a high-resolution, high-channel-count system with real-time stimulation control and a compact form factor allowing behavioral studies in rodents. To achieve this goal, we present a new optogenetics

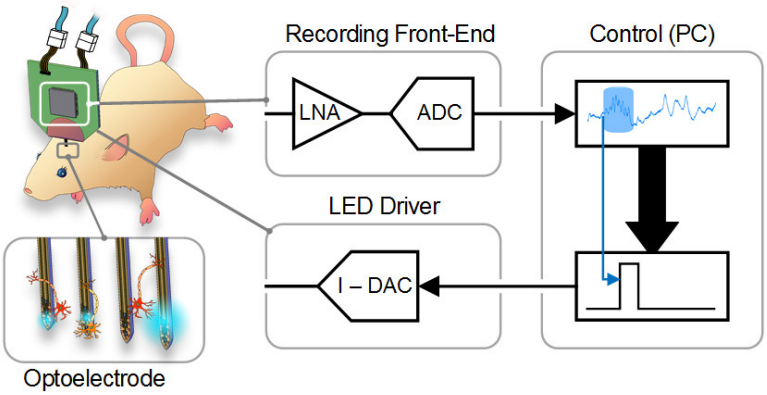


Figure 4-1. Schematic diagram of the opto-electrophysiology system in closed-loop configuration.

headstage suitable for our high density µLED optoelectrodes ([40], [98]) which integrates custom ASICs on a small light-weight printed circuit board (PCB) [99]. This headstage enhances the performance as compared with the current state-of-the-art works by: (1) scaling the number of stimulation and recording channels by a factor of 2, (2) providing more precise real-time optical stimulation control within a 1 µA LED current (or approximately 42.4 nW output radiant flux), and (3) reducing the system mass below 2 g for freely-moving *in vivo* mouse experiments. Figure 4-1 shows the conceptual drawing of the proposed headstage, the peripheral interface modules and the µLED optoelectrode configuration. The remaining contents of the chapter offers an in-depth description of the system implementation, benchtop tests, and *in vivo* validation experiments. Section 464.2 describes the system architecture and the host controller. Section 4.3 explains the headstage hardware design including custom integrated circuits for optical stimulation. Section 4.4 provides the results of benchtop system characterization. In section 4.5, *in vivo* experimental results are shown. Section 4.6 provides a discussion and a path for complete closed-loop system implementation. Finally, concluding remarks are made in section 4.7.

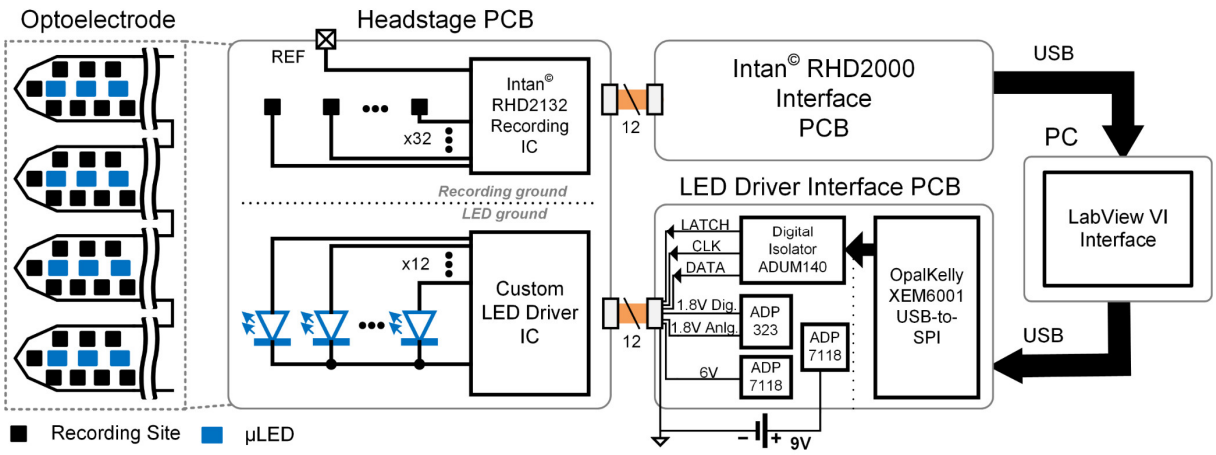


Figure 4-2. System circuit diagram showing the connections between the headstage PCB with integrated optoelectrode and recording and LED driver ICs, interface boards providing power and communication for the recording and LED driver ICs, and the PC-based LabView VI Interface.

4.2 System Architecture

The complete hardware system consists of four main modules as shown in Figure 4-2: (1) the headstage PCB, (2) LED driver interface board, (3) Intan® RHD2000 USB interface, and (4) the host PC.

4.2.1 Headstage

The headstage is composed of a small form factor PCB integrated with the optoelectrode and interfacing ASICs. The optoelectrode contains 12 µLEDs and 32 recording sites in a 4-shank configuration [40], [98]. Each µLED is driven by separate anode connection and shares a common cathode (or the µLED ground). The recording reference node is routed off-board to a headstage fixture and an animal reference electrode.

The µLEDs are driven by a custom ASIC for channel-specific current driving with precise timing and amplitude control. The recording is performed by an off-the-shelf digital electrophysiology interface chip (RHD2132) from Intan Technologies. The two ICs are assembled and placed near the optoelectrode to minimize the distance from the stimulation and recording

Figure 4-3. LabVIEW-based user interface for individual µLED control. In the inset, the channel 1 µLED located on top of the leftmost shank is configured to pulse at 1Hz frequency with 50% duty cycle and 10µA current amplitude.

sites. The short distance between the µLEDs and the driver chip reduces the parasitic capacitance and inductance, thus minimizing the rise time and overshoot of the input current pulse. Likewise, the short recording channel traces reduce parasitic capacitances and interference in the recording circuit. The stimulation and recording grounds are separated on the headstage and throughout the entire system. This eliminates any possible high frequency noise in the recording channels coupled from the µLED current return path. The headstage is connected to the peripheral control modules via two cables, each carrying digital control signals and power and ground to the ASICs. Thin, flexible 12-wire cables with compact, lightweight connectors are used to minimize the tethering force to the animal's head during experiments.

4.2.2 Peripheral Components

The µLED driver IC is powered and controlled through a custom driver interface module. System power is provided by a 9 V battery. Analog Devices ADP323 voltage regulator is used to provide 1.8 V, supplying the power to both analog and digital control circuits in the driver IC, while the ADP7118 voltage regulator provides the 6 V supply to the µLED current output nodes. An OpalKelly XEM6001 FPGA module converts the USB packets from the PC into an SPI-based protocol to communicate with the chip. Analog Devices ADuM140 digital isolator is used to

transform the digital signals into a separate power and ground domain, isolating the stimulation system ground on the headstage PCB from the PC ground.

The recording chip is powered and controlled through an Intan® RHD2000 USB interface board. The board uses an OpalKelly XEM6010 FPGA for control and data acquisition between the Intan® RHD2132 recording IC and the PC.

A custom LabVIEW graphical user interface (GUI) is developed for easy and precise control of the μLEDs, as shown in Figure 4-3. Each μLED can be individually programmed and controlled to generate a pulse train of current at a given frequency and duty cycle. The μLED can be also configured to respond in real-time by onscreen button clicks or external triggers.

4.3 Headstage Hardware Design

4.3.1 μLED Optoelectrode

The optoelectrode is designed for high-spatial-resolution optical stimulation and electrical recording from a small brain tissue volume with a high neuron density, such as the hippocampus. We monolithically integrated neuron-sized μLEDs (10 μm by 16 μm) and electrodes on the tips of fine silicon shanks in the typical 'Michigan Probe' configuration [40], [98]. GaN-on-Silicon wafers with epitaxially grown InGaN multi-quantum-wells (MQWs) are used to form the mesa structure of μLEDs.

The dimensions of the optoelectrode and the layout of μLEDs and the recoding sites are shown in Figure 4-4. The optoelectrode has four 5-mm long, 40-μm thick, and 70-μm wide silicon shanks. Shanks are 250 μm apart from one another, providing sufficient coverage of hippocampus

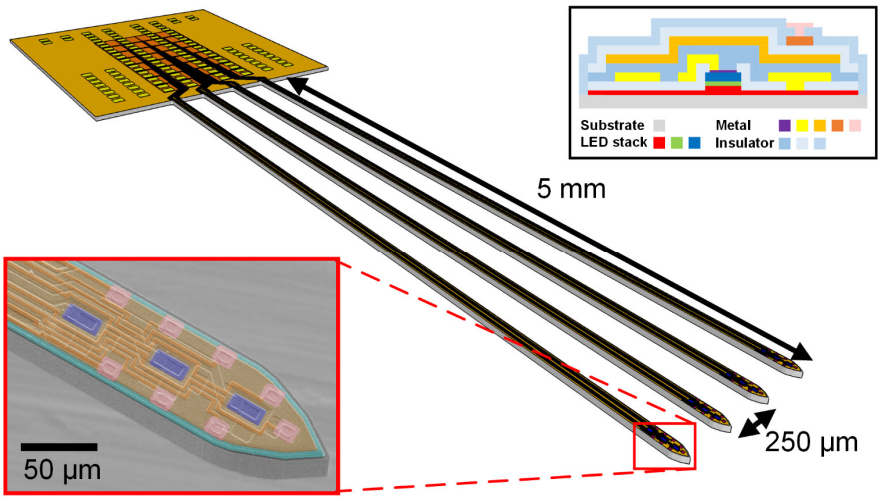


Figure 4-4. Schematic diagram of the µLED optoelectrode. The insets show (bottom left) SEM image of the tip of a shank of the fabricated optoelectrode with coloring for visualization and (top right) the cross-section of the optoelectrode.

by a single insertion. Each shank contains three blue (λ_{peak} = 460 nm) InGaN MQW µLEDs vertically spaced by 60 µm and eight iridium electrodes vertically spaced by 20 µm.

As shown in the cross-sectional schematic diagram (Figure 4-4, top right inset), there are multiple metal layers integrated on the optoelectrode. The interconnection lines (interconnects) for the µLEDs are shielded by a dedicated EMI shielding ground layer. The µLEDs are connected in a common cathode configuration, so that each µLEDs can be individually controlled by the respective current source while the grounds are shared. The EMI shielding layer provides an additional ground plane for the electric field generated from the µLED cathode interconnection layer to minimize any possible electric field-induced interference.

Micromachining techniques that are used for fabrication of the Michigan Probes are slightly modified and utilized for µLED optoelectrode fabrication. The µLED mesa structures and the interconnects are defined on GaN-on-Si wafers (NovaGaN). The EMI-shielding metal layer is deposited and patterned, following a blanket ALD deposition of Al_2O_3 and PECVD SiO_2 on the

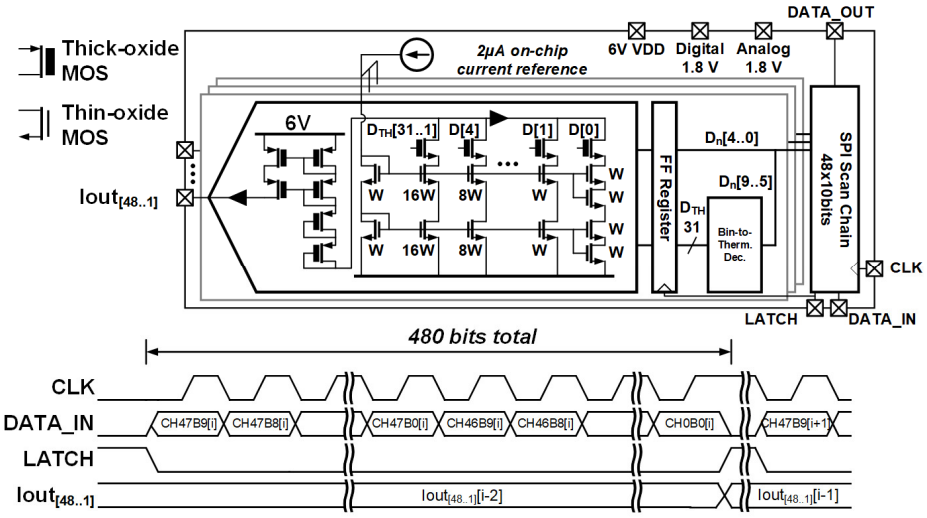


Figure 4-5. LED driver ASIC schematic and input/output signal timing diagram.

μLED mesa structures for passivation. After forming the recording electrode arrays and the interconnection layers, a two-step plasma dicing technique is used to define the outer boundary of the optoelectrodes and then release the devices using DRIE processes.

4.3.2 LED Driver ASIC

We have designed a custom ASIC to drive current to the μLEDs on the optoelectrode. The full circuit schematic is shown in Figure 4-5. The chip consists of 48 current digital-to-analog converters (DACs) controlled by an SPI-based serial input, with only 12 current DACs connected to the 12 μLEDs in the present optoelectrode configuration. The DACs drive the μLEDs with up to 1.023 mA current at a 10-bit resolution. The 1 μA current steps provide fine control of emitted optical power while the large output range allows a high optical power option for neural activation in a large tissue volume.

The output currents are simultaneously updated at the rate of 11.72 kHz by feeding 48 10-bit values into an input register which controls the output current level for each DAC channel. The serialized digital input, DATA_IN, is clocked in through the CLK pin and then latched into a

decoder at the LATCH signal's positive edge (shown in Figure 4-5, bottom). For every channel, the 10 bit code is split into two halves for the upper thermometer-coded DAC and the lower binary-coded DAC. All final bits are buffered through a register clocked by the LATCH signal to prevent transient logic glitches at the cost of increasing output latency by one LATCH cycle.

Decoded and buffered bits are then fed into an NMOS current steering DAC. The digital signals turn on or off the cascoded current sources controlled by thick-oxide NMOS transistor switches. To lower the effective area, the transistor sizing is referenced to 2 μA. The LSB corresponding to a 1 μA current source employs stacked transistors to multiply the effective length by 2, thereby resulting in half its reference current. The code, at which the thermometer/binary DAC split occurs, and the absolute transistor sizing was selected to minimize the chance of non-monotonic output behavior and increase the overall yield. The reference current is generated by an on-chip β-multiplying-style current source.

Since the μLEDs require a voltage compliance well above the allowable supply voltage of the used technology (3.3 V for 0.18 μm), we use a level-shifting current mirror in order to translate the output voltage while maintaining the same current. The mirror is implemented through a pair of cascoded PMOS transistors which mirror the current coming from the DAC and feed it into output pads. The supply voltage of 6 V was selected to maintain high linearity by keeping the current mirror in the saturation regime while driving the μLED up to 5 V. Since the high-voltage option of the technology was not used, the output stage has been carefully designed to minimize the effect of large voltage drops across the transistor gates and channels. The thick-oxide transistors are used with a long channel, and additional diode-connected transistors are placed between the current mirror and the DAC. Thanks to exponential I-V characteristics of μLEDs, the output transistors do not experience a large voltage drop when driving high currents, extending the

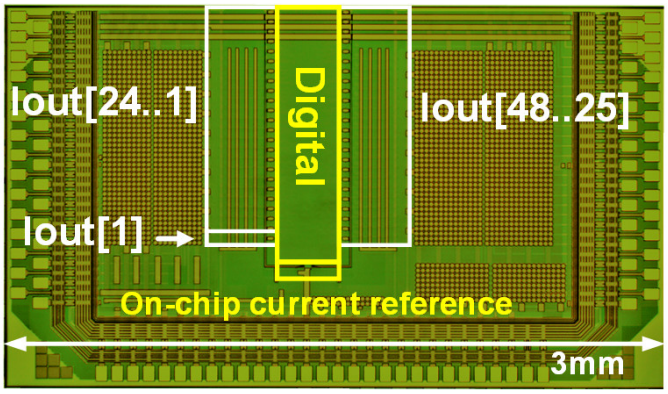


Figure 4-6. Chip microphotograph of µLED Driver ASIC chip.

lifetime of the circuit. The additional advantage of the long channel design is the increased output impedance which increases the linearity of the current mirror.

The chip is implemented in 0.18 µm CMOS technology. A chip microphotograph is shown in Figure 4-6. Full chip dimensions of 3 mm x 1.5 mm include the active circuitry as well as the power-decoupling capacitors and the wirebonding pads. The active area of the circuit only consumes 1.3 mm^2 or 0.272 mm^2 per channel.

4.3.3 Headstage Assembly

All the fabricated components including an optoelectrode, an LED driver ASIC, and an Intan recording chip (RHD2132) have been assembled on a 4-metal-layer PCB to form a headstage, as shown in Figure 4-7. The two inner layers of the PCB are dedicated as the ground planes for the recording and the stimulation systems. Two ASICs are attached on the opposite sides of the PCB on top of their respective ground planes.

A polyimide-based flexible cable, similar to that of microflex interconnection [100], is used to provide the electrical connection between the optoelectrode and the PCB. The cable fabricated with a simple two-mask process provides a connection density higher than that acquired from the conventional wire bonding processes. This gives the design freedom by allowing the bonding pads

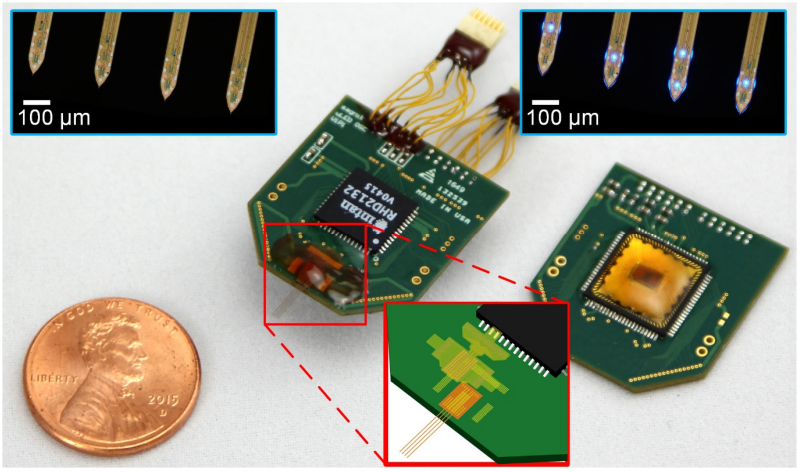


Figure 4-7. Photographs of the assembled headstages. Insets show(top) micropho- tographies of the tips of the optoelectrodes, and (bottom) the schematic diagram of the polyimide-based flexible cable interposer. The light leakage from the sides of the optoelectrode shank, shown in the top right inset, is an artifact due to the combination of poor light coupling efficiency in the air and high optical output power.

to be placed anywhere on the PCB area. The flexible cable also allows reusability of the headstage because the optoelectrode can be easily dissembled and replaced if needed.

Two ASIC chips and passive components are first reflow-soldered onto the PCB. After that, two 12-pin miniature connectors (Omnetics PZN-12-DD) are attached to the headstage via 2-cm long 36-AWG flexible wires to decouple the tethering force of the long cables connecting the headstage and the interface control module. The optoelectrode is then attached to the PCB using a flexible polyimide cable as an interposer. After bonding the interposer with the optoelectrode using a ball bonder (K&S 4524D), the optoelectrode-PCB interface is secured with a silicone encapsulant (Dow Corning Sylgard® 184), followed by applying a thin layer of biocompatible epoxy (Epoxy Technology Epo-tek® 353 NDT) for protection.

The dimensions of the assembled headstage are 2.16 cm × 2.38 cm × 0.35 cm. The total mass, including the connectors, is 1.9 g. Since it is generally recognized that the mass of a headstage should not exceed 10% of the weight of an animal for awake and behaving experiments,

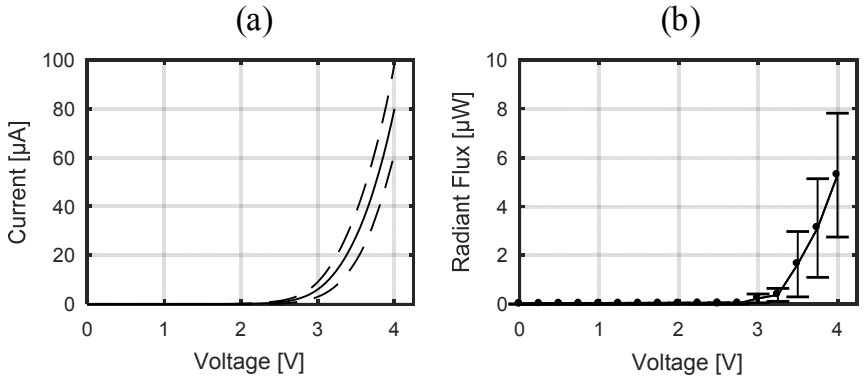


Figure 4-8. The opto-electrical characteristics of μLEDs (n = 7) on the fabri- cated μLED optoelectrode: (a) I vs. V curves and (b) output radiant optical flux vs. V curves. Dotted lines and the error bars represent one standard deviations from the mean.

the low mass as well as the small dimensions of the assembled headstage make it suitable for experiments with awake rodents [101].

4.4 System Characterization

The optical stimulation capability of the headstage was characterized on benchtop first. The μLED optoelectrode and the LED driver IC are separately characterized to ensure proper operation of each component. The performance of the combined components was then characterized to ensure the performance of the assembled headstage.

4.4.1 μLED Characterization

The electrical and the optical properties of the fabricated μLED optoelectrode were characterized. The μLED optoelectrode was attached onto a PCB with no active components using the same assembly procedure as in the actual headstage. Electrical connections to the μLEDs were provided with an Omnetics connector.

Figure 4-8 (a) shows the I-V characteristics of μLEDs (n = 7), measured using a sourcemeter (Keithely 2400). The μLEDs have an approximate turn-on voltage of 2 V, and a forward current

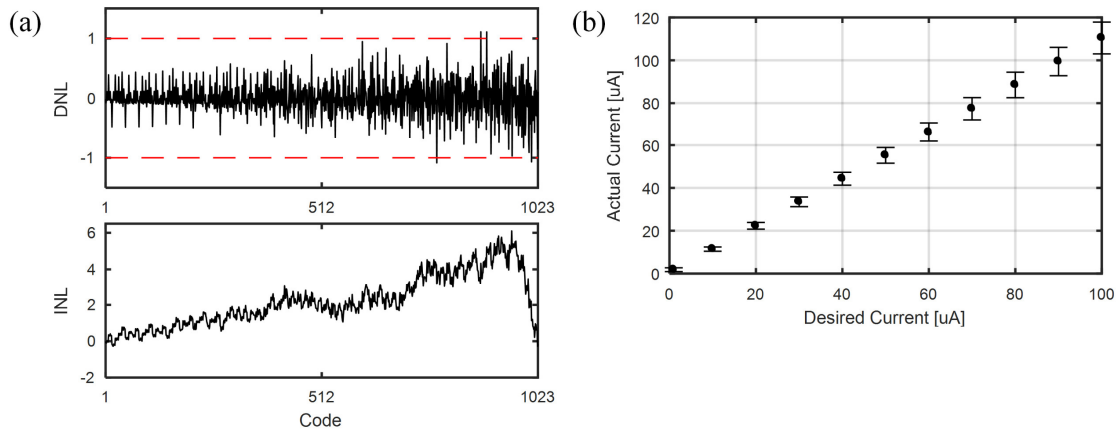


Figure 4-9. DC output current measurements of the fabricated LED driver chip showing (a) differential and integral non-linearity plots, and (b) mean current measurements across 19 dies. Error bars represent one standard deviation from the mean.

of approximately 100 µA at 4 V. Figure 4-8(b) shows the output radiant optical flux (Φ_e) as a function of µLED voltage, measured using a voltage source (Agilent E3631A), an integrating sphere (Ocean Optics FOIS-1), and a calibrated spectrometer (Ocean Optics Flame VIS-NIR). The output radiant flux of each µLED was then calculated by integrating the measured spectral flux from λ = 400 nm to 600 nm. The radiant flux from the µLEDs at 4 V bias was measured as 5.3 µW, equivalent to irradiance of 33.1 mW/mm^2 at the surface of the µLED, which is more than sufficient to excite neurons expressing channelrhodopsin-2 (ChR2) with a threshold irradiance of 1 mW/mm^2 [102]. Since we have previously shown that heat dissipation from a 10 x 16 µm µLED at the tip of a 5-mm long, 70 µm wide, and 30 µm thick silicon shank during pulsed stimulation induces the temperature increase of the brain tissue less than 1 ºC [98], additional thermal characterization of the assembled headstage was not conducted.

4.4.2 LED Driver Characterization

The LED driver chip was characterized on a dedicated test PCB while the output currents were monitored using an NI-DAQ interface card. Total of 19 chips were measured.

First, nonlinearity was measured to evaluate the precision of current control. Figure 4-9(a) shows the differential and integral nonlinearity (DNL and INL) plots from a DAC channel. The average maximum DNL and INL across 19 chips are 1.33 and 6.12, respectively. Since the high DNL values appear mostly at higher codes, the linearity of the DAC is maintained high at lower currents where precision is more necessary. The increase in INL is due to the reduction of output impedance at high μLED currents. The mean and standard deviation of output current is shown in Figure 4-9 (b). The measured mean output current accuracy from the nominal value is 12.3%, while the average standard deviation is 6.7%. The deviations however do not require additional calibration of the ASIC since the μLED optical output power response should be calibrated after the assembly.

The quiescent power consumption of the fabricated chip (excluding I/O power) is approximately 218 μW. Single channel power consumption is a function of the channel current and can be expressed by

$$P_{ch} = 2\gamma I_{ch} V_{supply}$$

where I_{ch} is the desired output current, V_{supply} is the output transistor supply voltage (in our current design, V_{supply} = 6 V), and γ is a non-ideality factor that should be close to 1. The chip consumes 1.7 mW when driving all 12 μLEDs with a square- pulse current with an amplitude of 100 μA, frequency of 1 Hz, and duty cycle of 10%.

Finally, the stability of current over time was characterized by monitoring the current generated from a channel for an extended period. The chip was programmed to generate a square pulse of 4 Hz with a 50% duty ratio at 100 μA and the amplitude of the generated current was

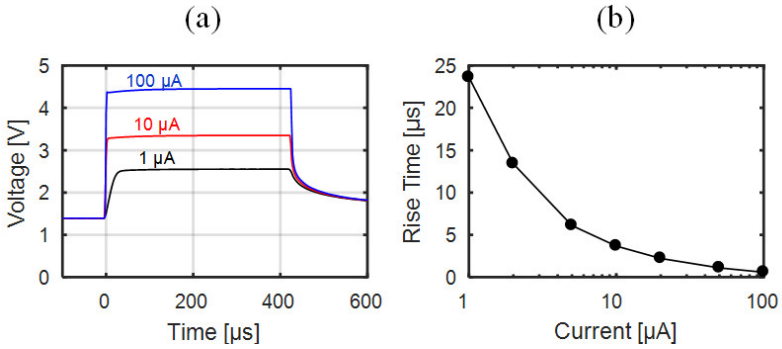


Figure 4-10. (a) µLED anode voltage transient response to 3 current pulses of varying amplitudes and (b) plot of changing µLED anode voltage rise timewith increasing driving current pulse amplitude.

measured. The current from the channel varies less than 1% over one million cycles, which is equivalent to 70-hour long continuous operation.

4.4.3 Integrated System Measurements

The transient voltage response of µLEDs to different current level pulses was measured to observe the effect of parasitic capacitance and inductance in the interconnection lines A wire trace on the headstage PCB connecting the on-chip LED driver to the µLED under test was probed and the signal was buffered by a high-speed low-input-capacitance unity-gain amplifier (Analog Devices AD825) and captured by an oscilloscope. Figure 4-10 (a) shows the measured anode voltage response for 3 current pulses with different magnitudes (1, 10, and 100 µA) while Figure 4-10 (b) plots the voltage rise times measured for currents between 1 and 100 µA. Low current pulses exhibit longer rise times due to slower charging of the µLED channel's parasitic shunt capacitance. The rise times, however, are significantly shorter than the biological response (whose detection is sufficient with 20 kHz sampling frequency of the recording chip) and therefore does not affect the *in vivo* experiment.

The optical response of the µLEDs on the optoelectrode was characterized using the LED driver ICas the current source to show the effectiveness of LED constant-current control. An

integrating sphere and a spectrometer were used to collect spectral response ($\Phi_{e,\lambda}$) and the integrated radiant flux (Φ_e) of each μLED at different current levels provided by the LED driver. The average Φ_e vs. I curve (Figure 4-11 (a)) shows a near-linear current-to-radiant flux response with a slope of approximately 68.5 nW/μA in 0 - 100 μA range.

The normalized average spectral radiant flux values from the μLEDs as a function of current are shown in Figure 4-11 (b). They are superimposed with the plot of the normalized spectral response of channelrhodopsin-2 (ChR2), the most widely used opsin. It can be seen from the graphs that the spectrum of the μLED emission is optimal for activation of ChR2 regardless of the forward current level. The measured peak and the width of the spectrum were approximately 460 nm and 40 nm (FWHM), respectively.

Finally, the profile of the optical power distribution inside the brain tissue was simulated. We built a model of a μLED structure embedded inside brain tissue and performed a ray tracing simulation using Zemax Optic Studio. The refractive index and the absorption coefficient of the μLED structure's SiO_2 passivation layers were measured using an ellipsometer (Woollam M-2000) and used in the model. The values for the refractive indices, the absorption coefficients and the scattering coefficients of the tissue and the other μLED materials were obtained from the literature [103]–[105]. The emission from the μLED was assumed to be monochromatic (λ = 460 nm) for simplicity. The result of simulated irradiance distribution at 100 μA is shown in Figure 4-12. A semi-lambertial irradiance profile was obtained in front of the μLED with a few scattered bright and dark spots due to scattering inside the tissue (Henyey-Greenstein Model). The boundary of the volume where irradiance is greater than 1 mW/mm^2, known as the threshold irradiance of channelrhodopsin-2, is shown that it is no larger than 20 μm away from the surface of the μLED. The result suggests that the volume of the brain illuminated by the μLED can be strictly confined

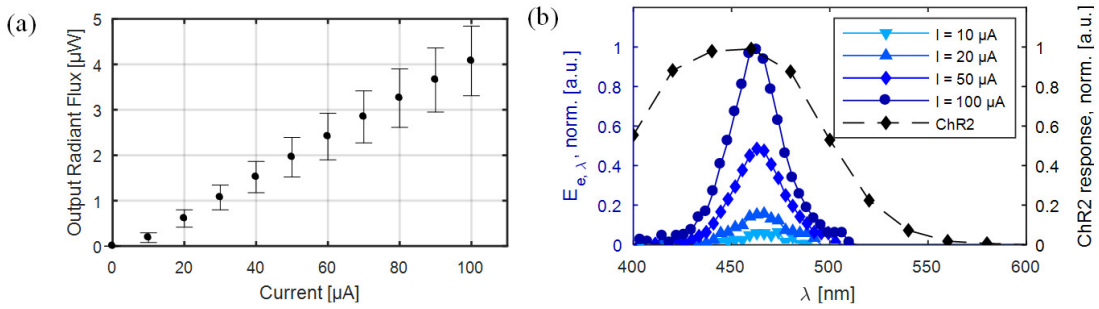


Figure 4-11. The optical characteristics of the μLEDs on the fabricated μLED optoelectrode showing (a) average Φe vs. I curve (n = 7) and (b) the normalized spectral radiant flux of the μLED at different forward current (with the spectral response of ChR2).

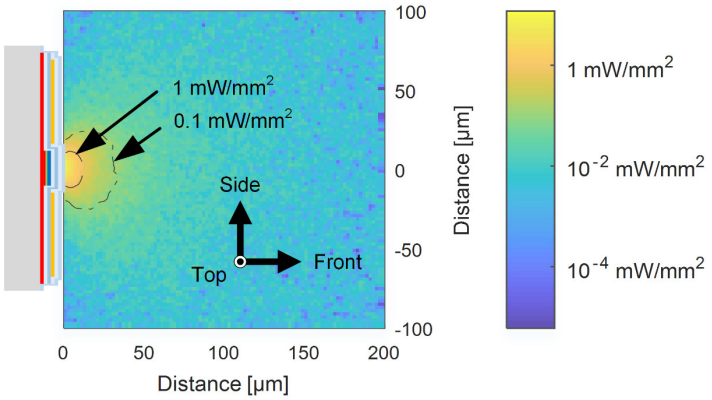


Figure 4-12. Irradiance distribution inside the brain tissue by μLED illumination, on the axial cross-sectional plane with the origin located at the center of the μLED surface. The thickness of the LED, metal, and dielectric layers are not drawn to scale.

to a small volume near the μLED surface by the precise control of optical power, confirming previous *in vivo* results obtained using the μLED with the same dimensions and configuration [40].

Key specifications and measurements of the optoelectrode, the LED driver IC, as well as those of the entire system, are summarized in Table 4-1.

4.5 *In Vivo* Validation

In vivo experiments were conducted to validate the complete system's capability of simultaneous high-resolution optical stimulation and electrical recording. The animal experiments were conducted at the Buzsaki lab at New York University and strictly followed the protocols

Table 4-1. System specifications and performance summary

Parameter	Value
µLED Optoelectrode	
µLED size/wavelength	10 x 16 µm / 460 nm ± 40 nm
µLED output radiant flux	5.3 µW @ 100 µA
Rec. electrode impedance	< 1 MΩ @ 1 kHz (Typ.)
LED Driver IC	
Current range (resolution)	0 to 1023 µA (10 bits)
LED current update rate	11.72 kHz
Power consumption	(12 ch. @ 100 µA, 10% duty) = 1.7 mW
Active Area	1.3 mm^2 (0.272 mm^2 per channel)
Headstage	
# of rec./stim. channels	32/12
Dimensions	2.16 cm x 2.38 cm x 0.35 cm
Mass	1.9 g
Volume of stimulation	2660 μm^3 @ 100 µA

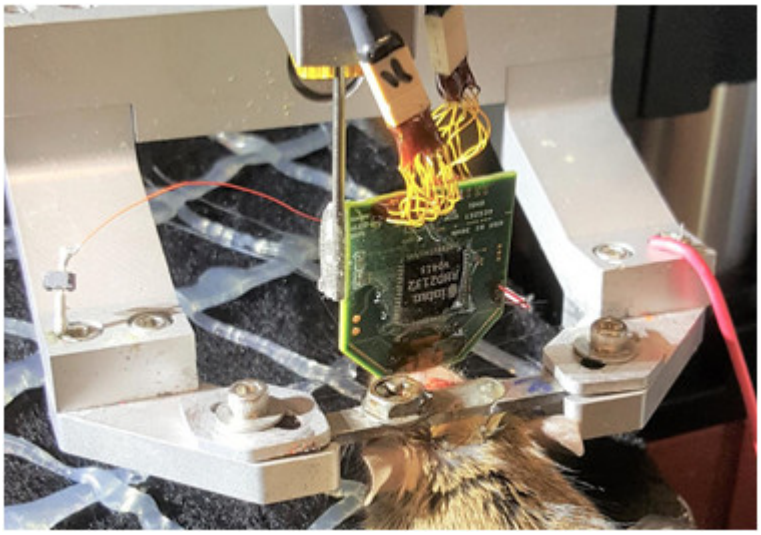


Figure 4-13. *In vivo* measurement setup of the headstage. The optoelectrode is implanted into an anesthetized mouse.

approved by the Institutional Animal Care and Use Committee of New York University. A 12-week-old male mouse expressing ChR2 (F1 generation of homozygous CaMKII-Cre crossed with homozygous Ai32 mice, whose expression of ChR2 is restricted to pyramidal neurons) was prepared and anesthetized for acute recordings. The headstage was attached to a stereotaxic frame with a micromanipulator for precise positioning. The setup for the *in vivo* experiment is shown in Figure 4-13.

Measurements were taken from the CA1 region of mouse hippocampus. Localization of the

recorded volume was obtained by stereotaxic targeting of known coordinates with help of the micromanipulator. The accurate position of the optoelectrode tips was confirmed by observation of the ripple-patterned oscillations in local field potentials, which is one of the characteristics of the electrophysiological recordings from the hippocampus. After each experimental session, a template matching algorithm was used on the raw recorded data for semi-automated spike sorting followed by manual curation and reclustering of noisy units. All the spike sorting tasks were performed using KlustaKwik.

4.5.1 Validation of Optical Induction of Neuronal Activities

In the first experiment, a single μLED was turned on and the resulting neural responses from the illuminated volume were recorded using nearby electrodes. Current pulses with varying on-time current were generated using the LED driver ASIC. Pulses with forward current of 0, 2, 4, 6, 8, and 10 μA were generated, and the duration of each pulse was 500 ms. Total of 20 pulses with each current level were generated.

Figure 4-14 (a) and (b) show the raw signals recorded from one of the electrodes around the μLED during stimulation with pulses with 10 μA on-time current and 0 μA (pulse repeat setting was on with zero current setting), respectively. It is clear that the activity of one of the nearby neurons, whose recorded action potentials are indicated by green, is notably increased during the μLED on-time with forward current of 10 μA. The waveform of the filtered action potentials during stimulation on- and off-times remained unchanged (Figure 4-14 (c)). We also observed an increase of the neuronal response to the increased light intensity. The peristimulus time histogram as a function of the on-time current (Figure 4-14 (d)) shows that the activity of the neuron was notably increased with a forward current greater than 4 μA. This observation is made possible by the high current resolution of the LED driver.

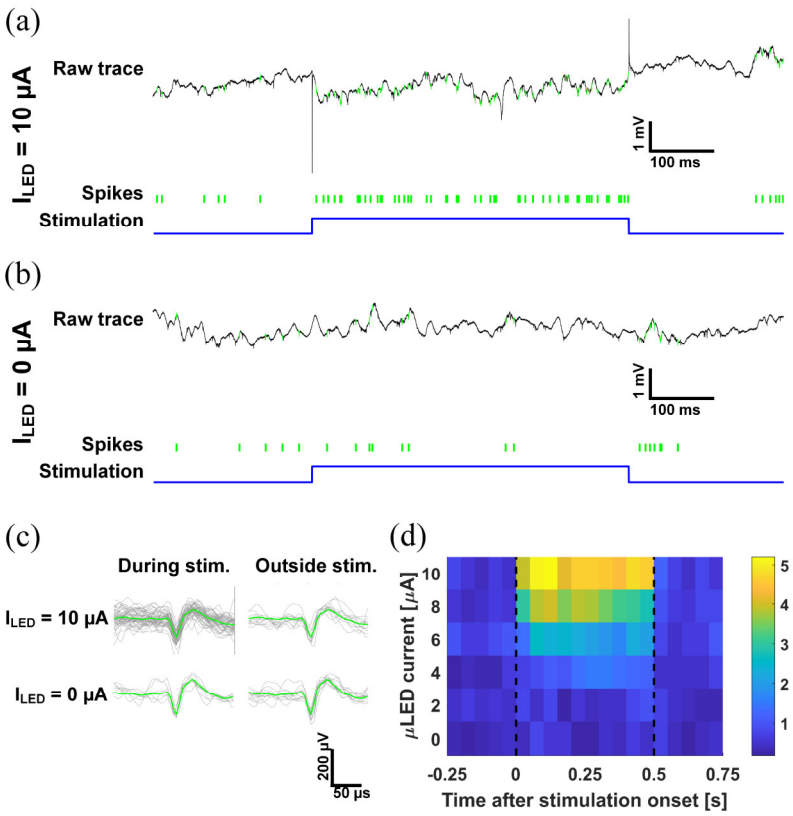


Figure 4-14. *In vivo* measurements validating the light-induced neuronal activity: raw signals recorded from an electrode as well as the raster plots of spikes from an optically excited neuron during a pulsed stimulation with (a) 10 µA and (b) 0 µA forward currents, (c) waveform of the action potential during the off- and the on-time of the pulse, and (d) peristimulus time histograms of the neuron at different on-time forward currents.

4.5.2 Validation of Selective Local Stimulation Capability

In the second experiment, two µLEDs on the two adjacent shanks were separately turned on. Changes in the activities of the neuronal population near the illuminated region were recorded from the both shanks and the approximate location of the recorded cells were calculated using triangulation.

Raster plots of spikes from two optically excited neurons are shown in Figure 4-15 (a). Cell 1 (indicated with a red triangle, Figure 4-15 (b)) and cell 2 (indicated with a green triangle, Figure 4-15 (b)) were activated with stimulation using a µLED on shank 1 (LED 1) and with stimulation using a µLED on shank 2 (LED 2), respectively. Stimulation with the µLED on one shank did not

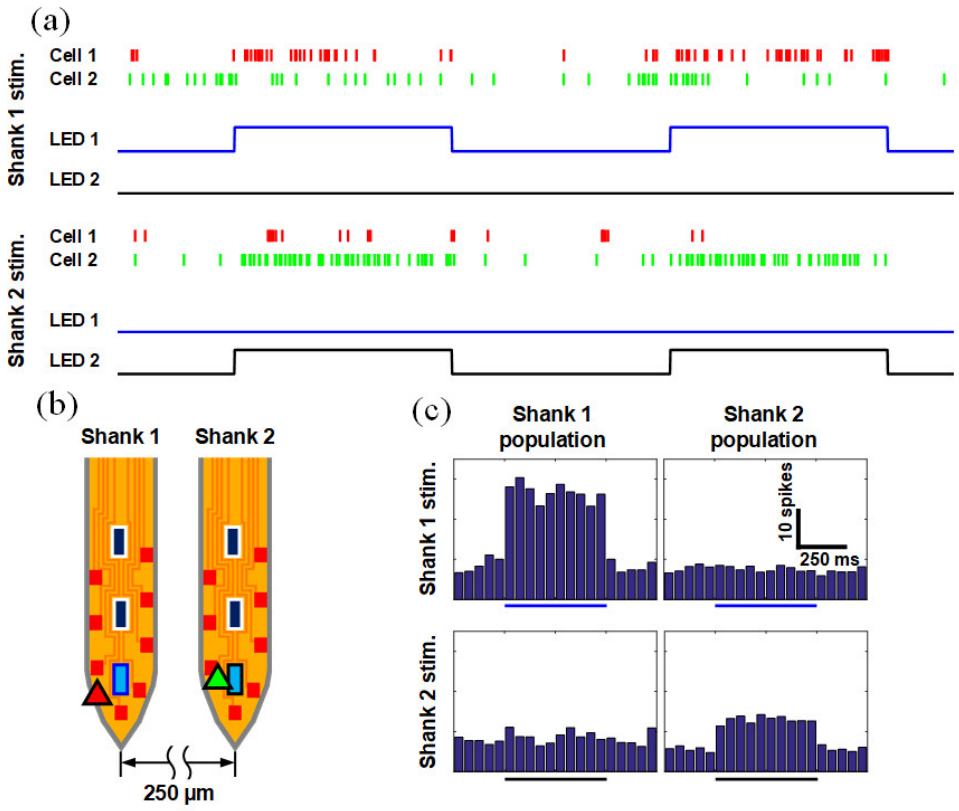


Figure 4-15. In vivo measurements validating selective location neural stimulation: (a) raster plots of spikes from two optically excited neurons responding to different µLEDs, (b) estimated locations of the neurons and the µLEDs, and (c) peristimulus time histograms of the neurons around shanks with the respective µLEDs.

activate the cell close to the other shank. The peristimulus time histograms of the neuronal populations around shank 1 and shank 2 during stimulation with µLED 1 and µLED 2 are shown in Figure 4-15(c). The local confinement of the µLED stimulation within a small region surrounding the shank was clearly validated with the change in the activities of the population.

4.6 Discussion

Our system is compared to previously published opto-electrophysiology systems in Table 4-2. The miniature headstage achieves the highest total channel count integration and the highest spatial and LED power resolution within a small form factor and low mass. While the current

Table 4-2. Comparison with Other Opto-Electrophysiology Headstage Systems

	Lee [95]	Kim [94]	Zhao [48]	Nag [45]	Gagnon-Turcotte [47]	**This Work**
# stim. ch.	4	4	6	1/64[6]	1	**12**
# rec .ch	Comm. Sys.[1]	Comm. Sys.[3]	4	16	8	**32**
Stim. res.	N/A[2]	1-bit (PWM only)[4]	8-bit	1-bit (PWM only)	1-bit (PWM only)[7]	**10-bit**
Headstage Mass	-	-	-	4 g	4.7 g[8]	**1.9 g**
Connection	Wired	Wired[5]	Wired	Wired[5]	Wireless	**Wired**

[1]32-channel recording performed with Intan Technologies RHD2132 system.
[2]Voltage-control; resolution not reported .
[3]1-channel recording performed with Plexon Omniplex system.
[4]Uncalibrated power through wireless link.
[5]Wireless capability only for stimulation.
[6]64-channel option for LED surface array only.
[7]Current set initially by hardware components.
[8]Including battery.

capabilities are enabled in part by a low-tether-force wired connection, we plan to introduce wireless capability in future work.

The bidirectional neural interface can readily be used for closed-loop optogenetic experiments with an appropriate algorithm for adaptive control of the stimulation parameters. However, a few improvements can be made on the hardware components of the system to enable the system's seamless operation for closed-loop experiments.

4.6.1 Reduction of Communication Latency

One of the bottlenecks to the ideal closed-loop operation of the system is the long round trip delay in the signal path inside the loop due to the high communication latency between the PC and the interface module. This is mainly due to the slow and inconsistent communication between the PC and the interface PCBs provided by a USB 2.0 connection [106]. It can potentially take up to a few tens of milliseconds for a stimulation command sent from the PC to initiate the desired optical stimuli. While the delay could possibly be insignificant for certain types of experiments, it is suboptimal for the experiments that require the stimulus to be precisely synchronized with fast and stochastic signals such as spiking activity of a specific neuron. Therefore, it would be desirable

to reduce the communication latency between the PC and the interface PCB to as low as several hundreds of microseconds.

The communication latency can be significantly reduced by replacing the existing communication links with ones with a higher bandwidth and a shorter latency. One of the potential candidate is PCI Express, which provides a high data rate of 8 Gb/s with a delay of less than a millisecond [107]. The system could be further modified to utilize a single interface board with the help of the high duplex data bandwidth.

4.6.2 Reduction of Stimulation Artifact

Another possible improvement to the system can be made by decreasing the magnitude of the stimulation artifact affecting the recorded electrophysiological signals. The artifact, which shows up at the onset and the offset of the optical stimulation, has relatively short duration ($\tau < 50$ μs) yet high magnitude (500 μV < Vpp < 5 mV). Although it can easily be removed either online with template matching or offline with spike sorting, the artifact can impact the system operation by affecting the quality of the recorded signals and adding extra computational burden.

It is understood that both the electromagnetic interference (EMI) [98] and photovoltaic effect [2] contribute to the stimulation artifact. Whereas the EMI cannot be significantly reduced due to the innate non-ideality of the ground and shielding planes originating from the resistance along the long and narrow shanks of the optoelectrode, the photovoltaic effect can be further reduced by engineering the silicon substrates. SPICE circuit simulation results suggest that the magnitude of the stimulation artifact can be reduced to as low as 50 μV after reducing the photopotential.

4.7 Conclusion

We present a new system architecture for high-precision and high-channel count optical stimulation and electrical recording by integrating an optoelectrode with interfacing ASICs on a single headstage. The system can simultaneously stimulate 12 μLEDs with a spatial resolution as low as 60 μm and record from 32 recording sites with a spatial resolution as low as 20 μm. The constant-current LED driver ASIC can drive up to 48 μLEDs with a 0 to 1.024 mA current range at 10-bit precision and 11.72 kHz update rate. The integrated headstage has a small form factor and a low mass of 1.9 g, enabling its use in behavioral *in vivo* rodent experiments.

CHAPTER 5

Opto-Electrophysiology Neural Interface IC with Artifact-Preventing Optical Pulse Shaping

5.1 Introduction

Despite achieving a higher channel count, higher density, and greater control of optical stimulation, the integrated interface presented in the previous chapter leaves many challenges unmet.

First, the system requires a wired connection to the host system, hindering long-range behavioral experiments where the subject (i.e. a rodent) may move several meters in multiple directions. The removal of the tether will enable scientists to use the system in new settings, freeing the animal subjects to do wide-area behavioral tasks, and minimizing the likelihood of the headstage torque affecting the animal's movements and decision making. While several wireless opto-electrophysiology headstages have been recently published, they suffer from the limited capabilities of the hardware components. Headstages published in [47] and [97] weigh 4.9 g and 5.5 g, respectively, making them both too heavy for mouse experiments. In these works, we notice that batteries often consume a large fraction of the mass budget. A reduction of power consumption would reduce the need for large battery while an alternative energy source could potentially allow the removal of battery altogether. An increased count of recording and stimulation channels is also desirable to cover a larger volume of brain tissue and increase the spatial resolution. While the

maximum recording channel count has been steadily increasing, the number of optical stimulation channels has mostly remained low due to the physical size of the light sources and delivery channels (fiber or waveguides). The use of monolithically integrated μLED probes promises a significant size reduction and improved spatial resolution. Further reduction in size (and power) is achievable through integrating electronics onto single custom ASICs. Such systems have been published in [48], [108]–[112], yet their levels of integration still leave much room for improvement.

The second challenge, unique to the bidirectional nature of the interface, is the formation of optical stimulation artifacts. Despite the many on-probe, on-chip, and off-chip solutions that have been introduced for electrical stimulation artifacts (see Chapter 3), their optical stimulation counterparts have been mostly left unaddressed. This could be attributed in part to the relatively recent introduction of the technique as well as the diversity of hardware and artifact coupling mechanisms. As optogenetics is being adapted to closed-loop systems and clinical neuromodulation, the ability to remove artifacts with low latency will become more important to the system's functionality. Although several filter-based techniques for electrical stimulation artifact removal can be used to eliminate optical artifacts in a similar fashion, an approach which considers the properties of the optical stimulation may yield similar results with considerably less resources.

In this paper we describe an opto-electrophysiology interfacing integrated circuit designed for a system that tackles the following challenges: system size, power consumption, channel count, and stimulation artifacts. With these in mind, we present three novel features and circuits: (1) integration of recording and μLED driver channels with a power management unit to minimize the area footprint, (2) a fully-integrated inductor-less step-voltage regulator for efficient wide-current-

range μLED drivability, and (3) an μLED driver circuit which suppresses the formation artifacts by precise current pulse shaping. The rest of this chapter is organized as follows: Section 5.2 explains the formation of optical stimulation artifacts and the method for their reduction. Section 5.3 describes the system architecture and the defining requirements. Section 5.4 describes the implementation of crucial circuit blocks. Sections 5.5 and 5.6 present the benchtop and *in vivo* measurements respectively. Lastly, Section 5.7 provides the conclusions.

5.2 Optical Artifact Analysis and Prevention

As explained in Chapter 3, the dominant artifact component in electrical stimulation is derived from the electric field formed in the tissue between the stimulation current source and sink. The electric field is detected as a potential difference between the recording channel electrode and the reference electrode. The tissue thus becomes not just a source of the neural signal itself but also the medium for simulation-recording crosstalk. In optical stimulation and electrical recording, intuitively this cannot be the case since the different modalities should not interfere with one another besides through neuromodulation itself. Nevertheless, these artifacts do appear and in fact have been described in several publications. For reader's convenience, the artifact measurements from these papers are included in Figure 5-1. In Figure 5-1 (a) Cardin et al. in [113] observe that the direct exposure of metal electrodes to a fiber-guided laser beam causes large electrical artifacts. By steering the fiber output away from the surface of the electrode, the authors are able to significantly reduce the artifact magnitude. Kampasi et al. in [114] observe artifacts in recordings from an integrated laser waveguide probe with recording sites (Figure 5-1 (b)). Here, the authors deduce in this publication as well as in [115] that the major source of artifact is in fact the capacitive coupling between the LD driver and the recording channel traces on the backend PCB platform. Finally, our own experiments described in the previous chapter (as well as in [99]) have shown

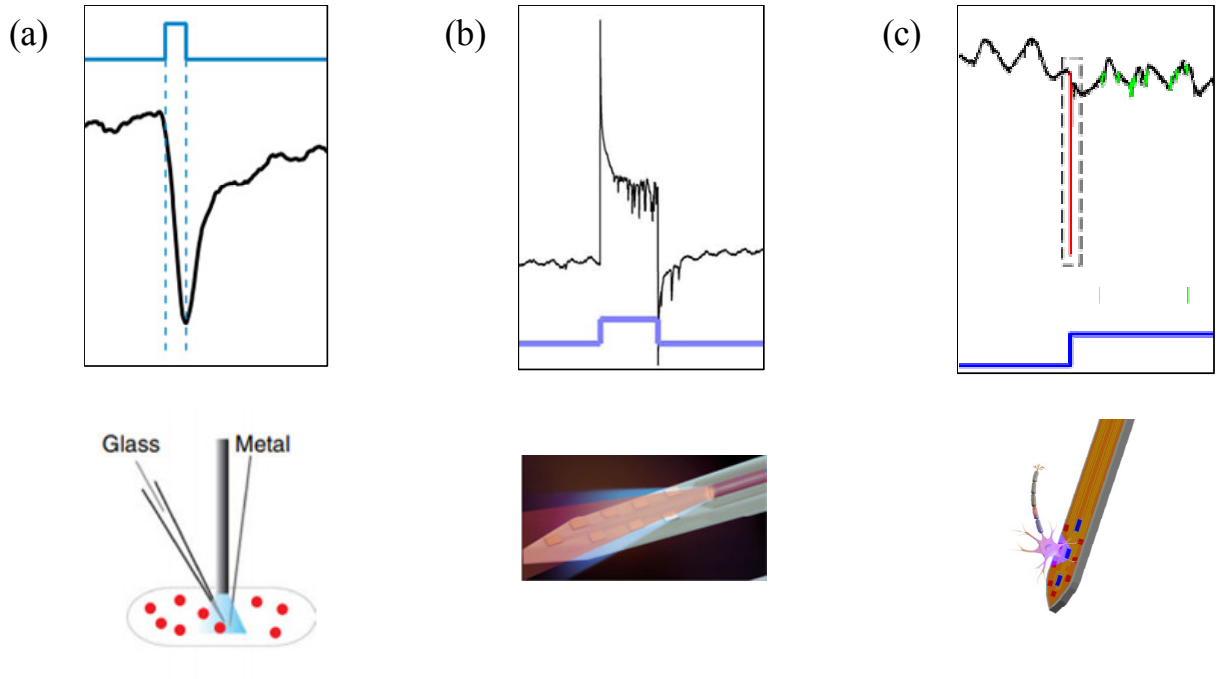


Figure 5-1. (a) Stimulation artifact forms when a fiber-guided laser light hits the surface of a metal wire electrode inside the neural tissue [113], (b) stimulation artifact observed on an integrated laser waveguide probe with recording electrodes in [114], and (c) stimulation artifacts observed on an integrated μLED probe with recording electrodes [99].

large but short artifacts during activation and deactivation of on-shank integrated μLEDs. In the following subsection, we explore how the artifacts form on an optoelectrode.

5.2.1 Artifact Formation

A proper discussion of artifact formation inside the μLED optoelectrodes should begin with the description of the optoelectrode structure itself. The probe's simplified single shank cross-section is shown in Figure 5-2. The structure sits on a floating un-doped substrate which provides the mechanical support for the probe. The substrate is left floating as it is not used for any signal routing. Next, the μLED stack sits on top of the substrate. Its anode connections are separately routed on the bottom metal layer while the common cathode connection is also routed on the same layer. The second metal layer is connected to the recording ground and it is used a shielding layer

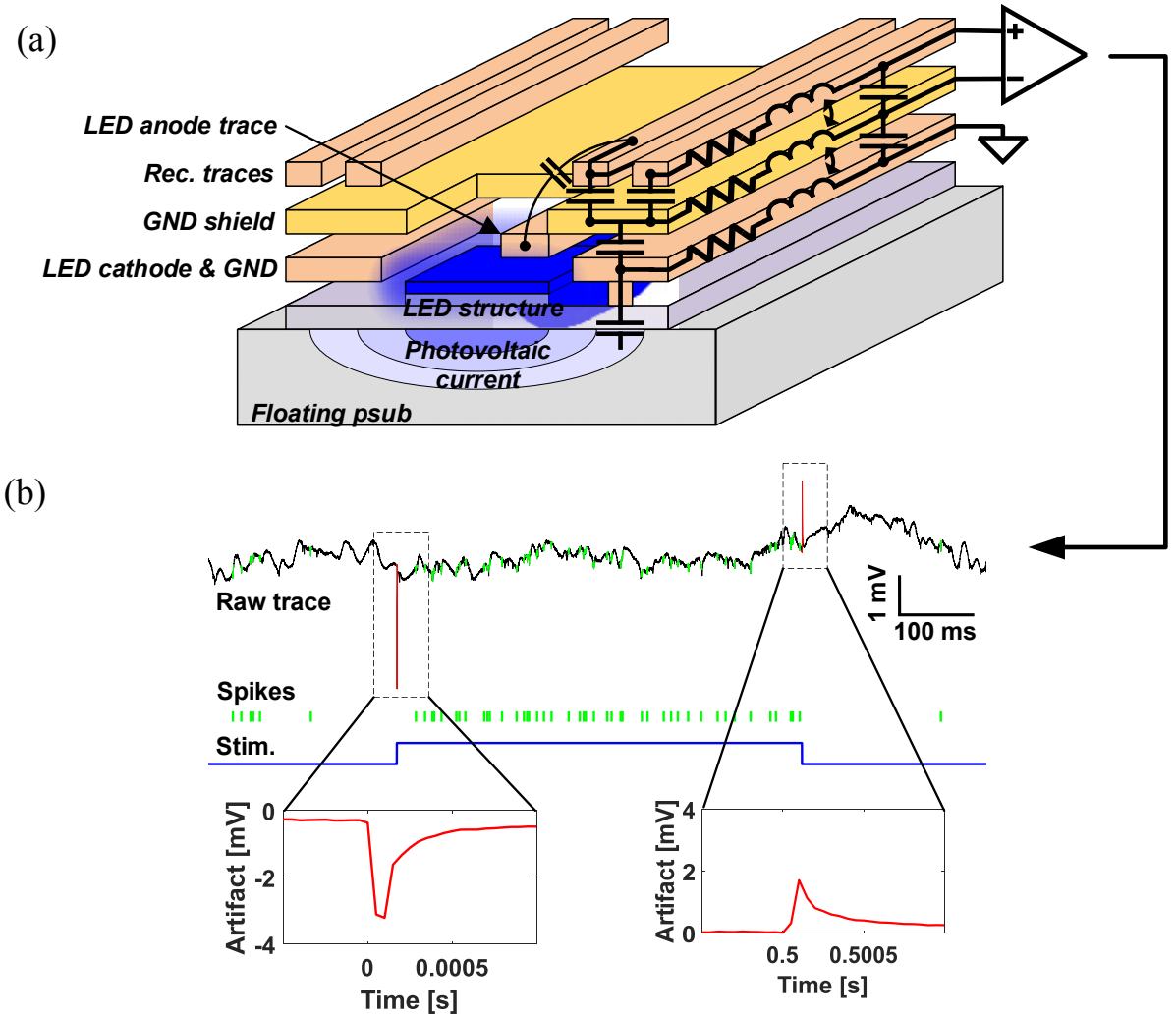


Figure 5-2. (a) Simplified µLED optoelectrode cross-sectional diagram highlighting the artifact coupling mechanisms and (b) recording snippet from a 2-layer optoelectrode showing artifacts (in red) at stimulation activation and deactivation.

between the stimulation and recording traces. The top metal layer is then used for routing of the recording channels.

Preliminary analysis has shown the dominating effects of two artifact coupling mechanisms: capacitive coupling between the stimulation traces and the photovoltaic effect occurring at the substrate. In the first mechanism, also described in [98], the parasitic capacitance between the stimulation and recording traces transmits the high frequency components of sharp µLED-driving current pulses into the recording channels. Despite the shielding between the

recording and stimulation traces, the finite resistivity of the metal weakens the ground at the shank tip and does not completely eliminate the coupling. In the latter mechanism, the photons emitted from the μLED generate electron-hole pairs in the substrate which are then similarly capacitively coupled onto the recording traces. This photovoltaic effect in silicon microelectrodes has been previously described in [116] and [117]. Figure 5-2 (b) shows the appearance of artifacts (in red) in the optoelectrode recordings during stimulation activation and deactivation. The artifacts have a narrow pulse width on the order of 100s of microseconds. The amplitudes of ~1.5 mV do not saturate the front-end but are much greater than the recorded action potentials and require intensive post-processing for removal.

A series of simulations was performed for further analysis. While it is difficult to simulate a transient response of the photovoltaic effect, the capacitive coupling mechanism can be easily analyzed by a circuit model. To do so, COMSOL was employed to extract a lumped SPICE circuit of a single optoelectrode shank structure model. It includes parasitic components such as shunt coupling capacitors, mutual inductance, and trace resistance similar to ones shown in Figure 5-2 (a). The model was then imported into the Cadence schematic simulator and an AC simulation was performed to analyze the frequency spectrum of the coupling signals. In the simulation, a sinusoid current input of amplitude 1 μA was injected into the trace leading to the middle μLED (Figure 5-3). Since the μLEDs are inherently non-linear while the AC simulation *is* linear, we applied the sinusoid small signal current at different bias points. The outputs of the recording traces were connected to an ideal buffer with an input capacitance of 4 pF. The buffered output voltages (in dB) are shown in Figure 5-3 for two bias points: 0 μA when the μLED is fully off and 100 μA when the μLED is operating in the higher input current range. A few observations can be made from the simulation results. The plots clearly show an increase in magnitude corresponding to an

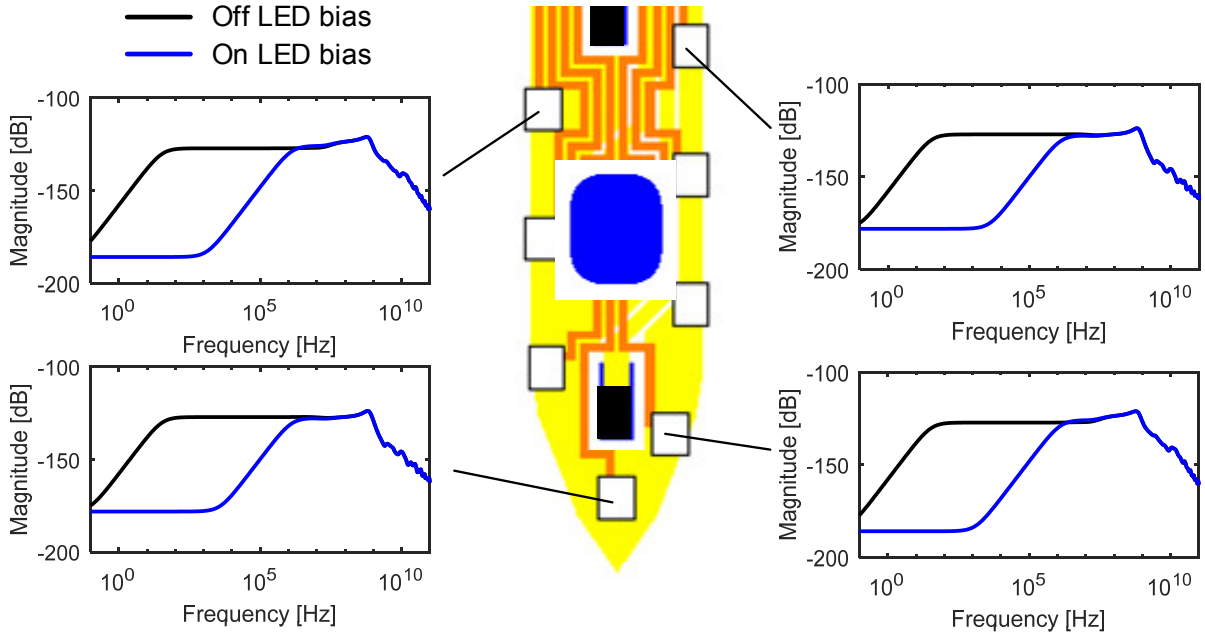


Figure 5-3. SPICE simulation results of on-probe EMI coupling between the µLED and recording channels. A current sinusoid of 1 µA was injected into the middle µLED channel and its frequency was swept from 0.1 Hz to 100 GHz. This was performed at two bias points: 0 µA (off µLED) and 100 µA (on µLED).

increase in frequency, pointing to the capacitive coupling between the stimulation and recording channels. In addition, the recording channels are also more prone to artifacts in the 1 Hz to 100 kHz range at lower bias currents than they are at higher bias currents. This can be intuitively explained by considering the larger effective resistance of the diode at lower currents, forcing a larger fraction of the current to flow through the parasitic shunt capacitors. At higher bias currents, the effective resistance is lower, and the shunt current begins to dominate at much higher frequencies.

5.2.2 Artifact Prevention

Given the system constraints of a µLED-integrated optoelectrode, there are a few ways the stimulation artifact can be reduced. The first and most direct approach is improving the structure of the optoelectrode. Extra metal layers may be used to shield the recording traces from the µLED

traces and the substrate, as reported in [98]. In this work, the original 1-metal-layer design was improved by adding a second metal layer to separate the stimulation and recording traces. Significant artifact reduction was observed, yet it was not eliminated. Adding additional shielding layers may improve the performance even more. A 3-metal-layer version of the probe, shown in Figure 5-2 (a) is used in experiments in section 5.6. Nevertheless, the variations of the fabricated electrodes and physical constraints of shielding layers limit the performance gains of more complex structures.

Another approach to minimizing the artifacts can be borrowed from the recording-based artifact removal algorithms and circuits discussed in Chapter 3. Front-end artifact cancellation techniques work relatively well for short, single channel stimulation scenarios, yet require increasing complexity with longer artifact responses and increasing number of channels. The increasing size and power consumption of the filters may prohibit the approach in low-power wireless headstage systems.

In this work, we explore a third strategy, which is based on precisely controlling the μLED current input. Insight into *how* to control the current can be gained from the SPICE simulations shown in the previous section. Most optogenetic studies use rectangular pulses to drive the light sources. This approach can be implemented with a simple driving circuit. However, rectangular pulses contain many high frequency components which, shown in Figure 5-3, couple stronger to the recording channels than low frequencies. The intuitive approach to reduce the higher frequencies is the smoothing of the input current pulse shape. [118] and [40] use current-mode and voltage-mode sine wave inputs, respectively, to drive the light sources while preventing large artifacts. Unfortunately, the constantly changing current complicates the analysis of the neuromodulation since it is difficult to measure at what exact optical power the neurons experience

optical stimulation. A compromise can be reached by attaching smooth rising and falling edges to flat rectangular pulses. If the rise and fall times are shorter than the desired temporal resolution in the experiment, a resulting pulse shape will still function as a constant power output pulse. For example, a 1-2 ms photocurrent response time for the ChR2 opsin is cited in both [102] and [119], thus pulses with shorter rise times should evoke similar responses. An arbitrary rise-time pulse can be simply implemented by adjusting the slope of the rectangular pulse, essentially forming a trapezoidal-shaped pulse. This pulse is defined as follows:

$$y = 0, \qquad t \leq 0$$

$$y = \frac{At}{T_{rise}}, \qquad 0 < t \leq T_{rise}$$

$$y = A, \qquad T_{rise} < t \leq T_{rise} + T_{pulse}$$

$$y = A - \frac{A\left(t - T_{rise} - T_{pulse}\right)}{T_{rise}}, \qquad T_{rise} + T_{pulse} < t \leq 2T_{rise} + T_{pulse}$$

$$y = 0, \qquad 2T_{rise} + T_{pulse} < t$$

where T_{rise} is the rise and fall time between 0 and current amplitude A, A is the peak current, and T_{pulse} is the pulse width (excluding the transition time). Plots of the trapezoidal pulses with varying T_{rise} are shown in Figure 5-4 (a). A smoothened frequency spectrum plot shows a significant reduction in high frequency components as T_{rise} is increased, which will lower the coupled artifact.

Further high frequency content reduction can be achieved by using the rounded pulses which eliminate sharp inflection points. We chose two candidates: a “sine-rise” pulse and a “Gaussian-rise” pulse. The sine-rise pulse is defined as follows:

$$y = 0, \qquad t \leq 0$$

$$y = \frac{A[-\cos(\omega t) + 1]}{2}, \qquad 0 < t \leq \frac{\pi}{\omega}$$

$$y = A, \qquad \frac{\pi}{\omega} < t \leq \frac{\pi}{\omega} + T_{pulse}$$

$$y = \frac{A\left[\cos\left(\omega\left(t - \frac{\pi}{\omega} - T_{pulse}\right)\right) + 1\right]}{2}, \qquad \frac{\pi}{\omega} + T_{pulse} < t \leq \frac{2\pi}{\omega} + T_{pulse}$$

$$y = 0, \qquad \frac{2\pi}{\omega} + T_{pulse} < t$$

where ω is the equivalent frequency of the sine-wave transition period, A is the pulse peak amplitude, and T_{pulse} is the pulse width. The Gaussian-rise function is defined as:

$$y = 0, \qquad t \leq 0$$

$$y = Ae^{-\frac{(t-T_{rise})^2}{2\sigma^2}}, \qquad 0 < t < T_{rise}$$

$$y = A, \qquad T_{rise} < t < T_{rise} + T_{pulse}$$

$$y = Ae^{-\frac{\left(t-T_{rise}-T_{pulse}\right)^2}{2\sigma^2}}, \qquad T_{rise} + T_{pulse} < t < 2T_{rise} + T_{pulse}$$

$$y = 0, \qquad 2T_{rise} + T_{pulse} < t$$

where T_{rise} is the rise and fall time of the pulse, σ defines the sharpness of the rise curve, and T_{pulse} is the pulse width. Both pulses with varying parameters and their frequency spectrums are plotted in Figure 5-4 (b)-(c). For comparison, the three pulse shapes with similar rise time parameters are overlaid with a rectangular pulse of the same pulse width in Figure 5-4 (d). The frequency spectrum plot shows that the sine-rise and Gaussian-rise pulses have lower high frequency content than rectangular and trapezoidal pulse shapes.

To obtain the final clues about artifact coupling, the 4 pulse shapes - trapezoidal, sine-rise, Gaussian-rise, and rectangular current pulses - were applied to the μLED channel in SPICE

simulations and the artifact was observed in a single recording channel (Figure 5-5). The parameters for the 3 non-square pulses were chosen for similar rise time, while the rise time of the rectangular pulse equals to the simulation's sampling time which is 6.5 μs. The maximum amplitude of all pulse shapes was set to 100 μA. The voltage artifact waveforms show varying peak amplitudes: 1869 nV for a square pulse, 93 nV for a trapezoidal pulse, 43 nV for a sine-rise pulse, and 5 nV for a Gaussian-rise pulse. As predicted, the square pulse artifact has the highest amplitude due to high frequency components. The explanation for the low Gaussian-rise waveform artifact could lie in its slow initial rise. As shown in Figure 5-4, there is a wider spectral coupling at low bias currents due to the exponential nature of the μLED's I-V characteristic. Thus, the lower spectral content at the beginning of the Gaussian-rise curve prevents the formation of a large artifact at the bottom of the pulse.

The results of this analysis point to pulse shaping as a viable technique for reduced-artifact stimulation. The integration of this technique will require a precise μLED current control in software and hardware. Thus, the remaining challenge is the design of a system and circuit architecture that implements a μLED-driving high-resolution current-mode digital-to-analog converter while maintaining low power consumption and miniaturized form factor of the wireless headstage.

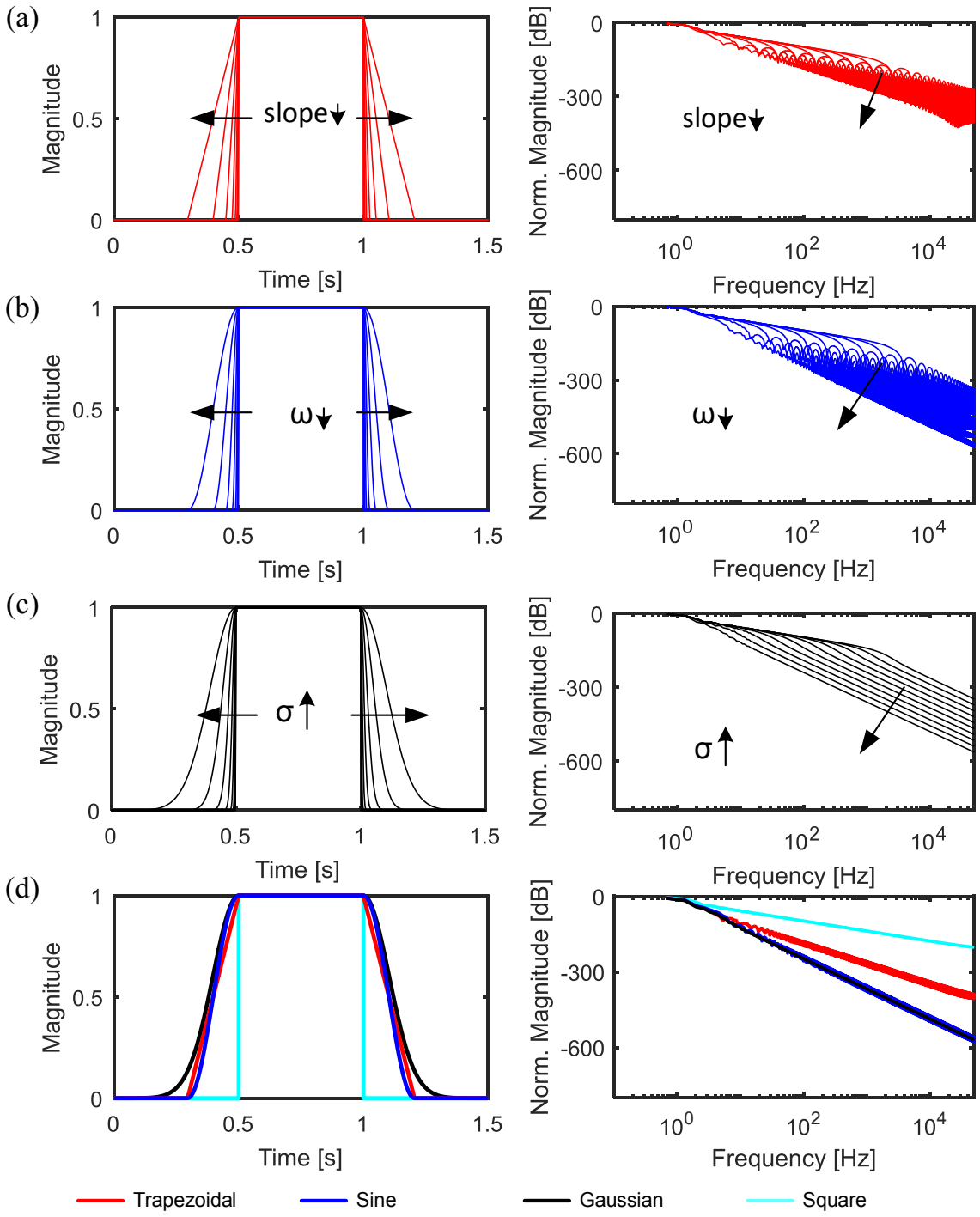


Figure 5-4. Time-domain and frequency spectrum plots of (a) trapezoidal pulse with varying slope, (b) sine-rise pulse with varying transition frequencies, (c) Gaussian-rise pulse with varying σ parameters, and (d) comparison of 3 pulse types with similar rise times to a rectangular pulse.

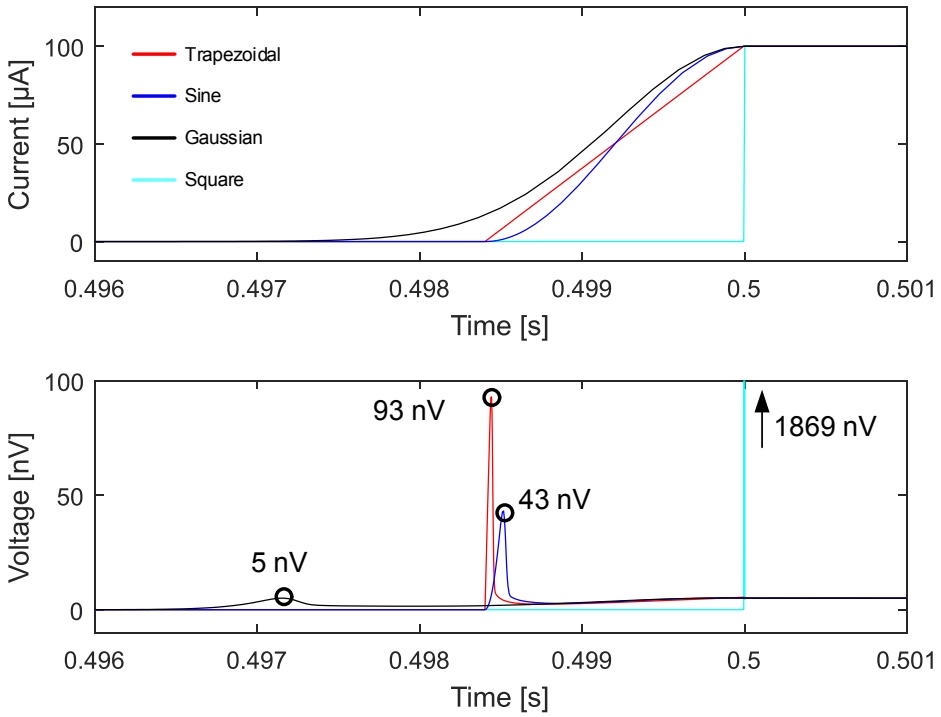


Figure 5-5. Time-domain simulation of LED current pulse-related artifact. Plot on top shows the input current and bottom plot shows the artifact simulated on a same-shank recording channel with annotated peak voltages.

5.3 System Architecture

The interface IC prototype is designed to be an integral part of a complete wireless headstage system shown in Figure 5-6. The chip combines recording front-ends and stimulation μLED drivers connecting to the optoelectrode described in Chapter 4. The digitized recording outputs and stimulation inputs are sent to and received from a separate wireless transceiver and controller IC. The interface chip also incorporates a power management unit which redistributes the power from an ultra-light-weight Li Polymer battery to both the interface and transceiver ICs. Additionally, the headstage must include a low-power crystal oscillator to provide a stable clock reference, and an antenna which, combined with a proper transceiver design, will enable fully

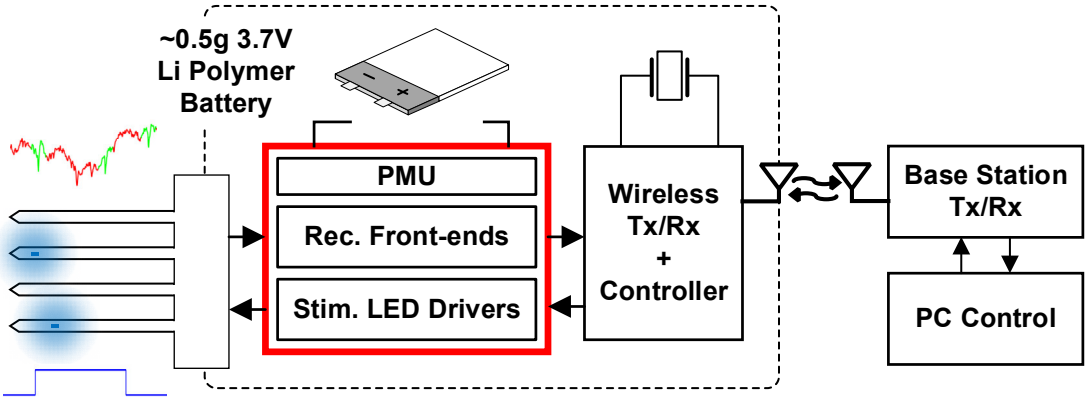


Figure 5-6. Proposed wireless opto-electrophysiology system with interface IC outlined in red.

duplex communication. Finally, a base station transceiver and a PC-based host provide the remote control of the headstage.

The interface IC architecture is shown in Figure 5-7. Recording module consists of two groups of 16 recording channels (32 channels total). Each group contains 16 separate signal inputs and single-ended low noise amplifiers, while sharing the rest of the signal conditioning, digitizing, and biasing blocks to save area. The low-noise amplifiers provide a gain of 100 and a bandwidth of 1 Hz – 15 kHz, providing a wideband recordings capability for LFPs and APs. The outputs of the individual low noise amplifiers are fed into an analog multiplexer which cycles through every channel and subtracts a shared amplified signal reference. Time-division multiplexed signal is then additionally amplified by a programmable-gain amplifier and fed into a 10-bit SAR ADC. The digital outputs of the two ADCs, one per 16 channel group, are fed into a shared SPI interface which serializes the data into a 3-wire communication link. The SPI interface also provides the control of the recording front-end circuit biasing blocks.

The 12 LED drivers address the unique challenges of μLED optogenetics stimulation. The drivers provide constant-current pulses, ranging from 0-1mA at 10-bit resolution (LSB = 1μA) and with a minimum rise-time of <50 μs necessary to observe quick neuronal reactions. The

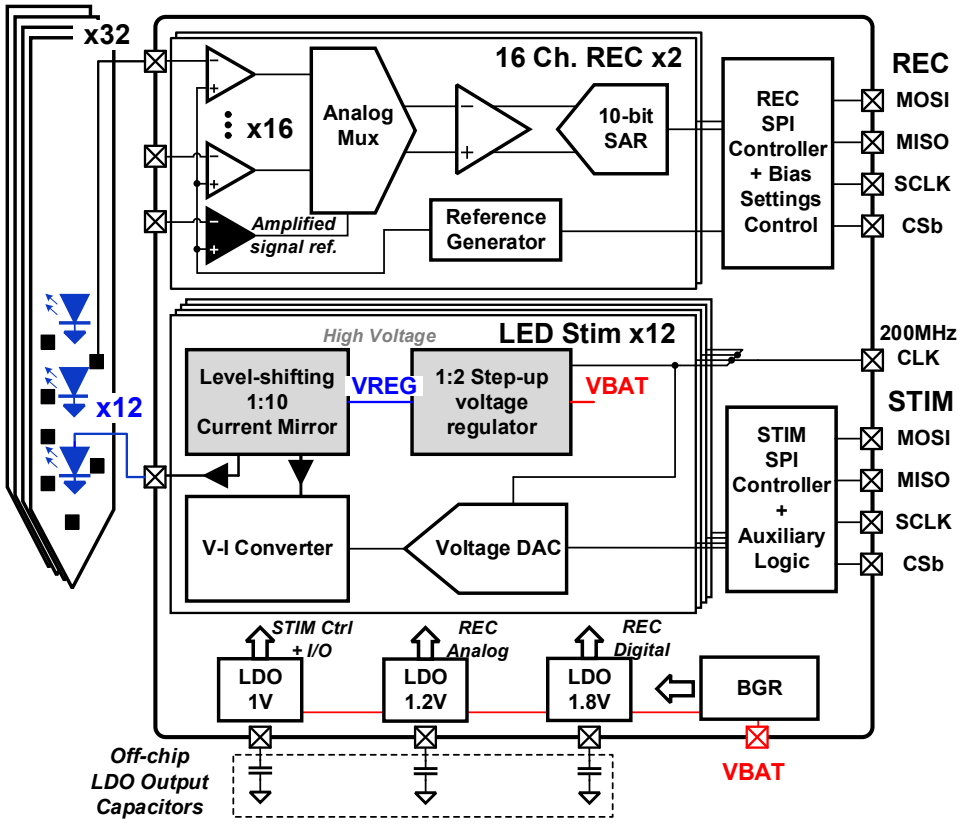


Figure 5-7. Proposed chip architecture block diagram. Blocks in grey utilize thick-oxide transistors for high voltage operation.

architecture is subdivided into a high-precision current-pulse-shaping circuit and a step-up voltage regulator providing the high supply voltage and current necessary to drive µLEDs. The voltage digital-to-analog converter (VDAC) and the voltage-to-current (V-I) converter generate a current pulse which is multiplied and upconverted to a higher output voltage. The split between low-voltage pulse generation circuitry and high-output-voltage regulator and current-mirror allows the integration in a low-voltage 0.18µm CMOS process. A 200 MHz clock is supplied externally to the step-up voltage regulator and the VDAC, and it is shared between all the channels. An additional SPI interface allows the user to program and reconfigure each LED driver channel.

The integrated low-dropout (LDO) linear voltage regulators provide 3 voltage-domain power supplies to the recording and LED-driving control circuitry. A 1.2 V supply is used for the

analog portion of the recording circuit, a 1.8 V supply is used for the digital portion of the recording circuit, and a 1 V supply is used to power the stimulation channel waveform generation circuits as well as the chip's I/O buffers. A separate 1 V regulator is included to supply power to the external wireless transceiver IC. All the regulators share a common bandgap-reference circuit and require off-chip output capacitors. The process mismatch effects of the bandgap-reference circuit can be calibrated through external digital control pins.

5.4 Circuit Implementation

This section covers the implementation of the stimulation channel circuitry. We first describe the implementation of the LED driver that generates current pulses to drive the μLEDs. Second, we describe the integrated step-up voltage regulator which provides the high voltage power to the the LED driver.

5.4.1 LED Driver with current pulse modulation

The LED driver is, in essence, a digital-to-analog converter that provides constant-current pulses to the μLEDs (which are characterized in Chapter 4). The driver also includes high-precision arbitrary waveform generation functionality to create smooth pulses for artifact reduction as described in section 5.2.2. Due to the inherent converter trade-off between additional resolution and higher power consumption, we devise a two-mode operation which allows the user to choose either a more power efficient constant-current mode or a less efficient high-resolution mode. We call the first mode the *pulse-width modulation (PWM) mode*. In *PWM mode*, a predefined current is set by the digital input and is directly switched on and off at the output to create rectangular current pulses. The second mode, or *pulse-shaping (PS) mode*, constantly converts the digital input to a current output waveform, allowing the user to update the output current with high temporal precision as well as with increased amplitude precision.

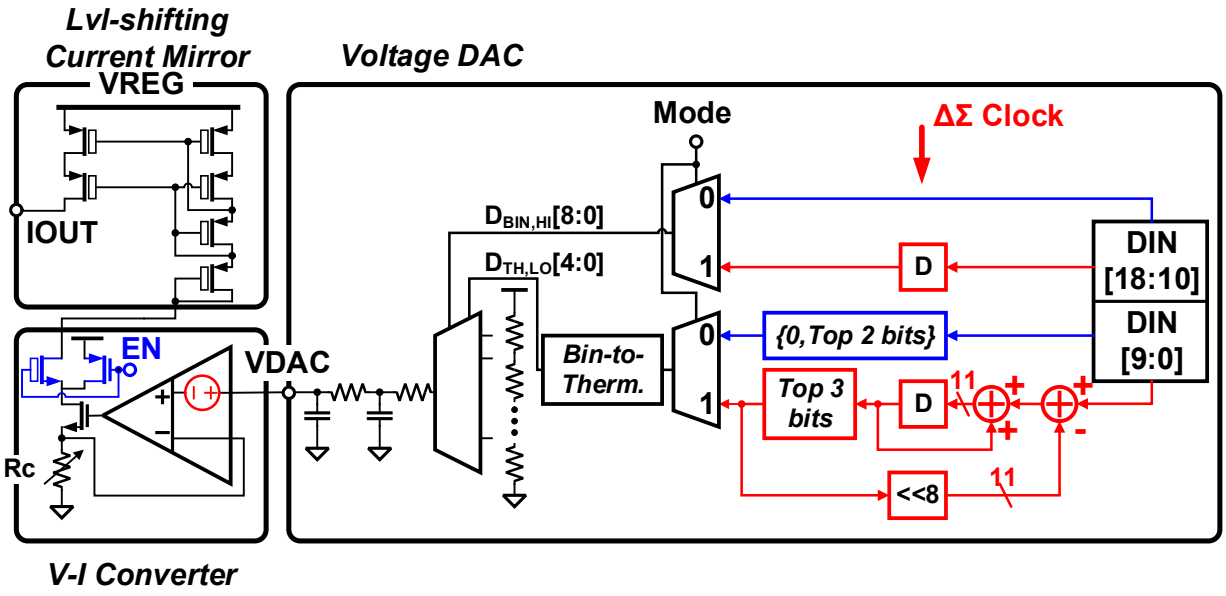


Figure 5-8. Circuit schematics of voltage DAC, V-I converter, and the level-shifting current mirror. Regular *PWM mode* DAC settings are shown in blue, while *PS mode* DAC settings are shown in red.

The driver architecture (shown in Figure 5-8) is designed to implement the dual functionality while taking advantage of the power-resolution trade-off. It is divided into 3 modules: a voltage DAC, a V-I converter, and a level-shifting current mirror. The voltage DAC converts the digital input into a specific voltage level proportional to the desired output current. As we describe later, the resolution of the voltage DAC can be increased through the oversampling and noise-shaping of its digital input. This operation facilitates the *PS mode*. Following the voltage DAC, the V-I converter linearly converts the output of the voltage DAC to a scaled version of the output current. The scaled current is then mirrored, multiplied by 10, and shifted to the high voltage domain through the level-shifting current mirror. The connection between the V-I converter and the level-shifting can be switched on and off, creating a fast-rising rectangular pulse. This facilitates the *PWM mode*.

Let us analyze the circuit modules in greater detail, beginning with the voltage DAC. The general digital-to-analog conversion is performed by a multiplexer that selects the desired voltage

level from a nominal 10-bit resistor ladder that lends to the DAC's high linearity. The user can change the resolution of the voltage DAC by toggling the mode selector switch (Mode). In *PWM mode* (Mode = 0), the digital SPI input is directly connected to the multiplexer. In *PS mode* (Mode = 1), the 2 least significant bits and additional 8 lower bits are routed to a 1st-order ΔΣ modulator which dithers the DAC output. The ΔΣ modulator is clocked by a divided external 200 MHz reference, shared between all the channels. The digital input is then fed into the multiplexer which controls the resistor ladder output. While its nominal output range is 0-100 mV, an extra most significant bit is added to increase the range to 0-200 mV to accommodate the offset calibration of the V-I converter (explained later in this section). The multiplexer is split into a binary 9b MSB multiplexer and smaller "2.5b" thermometer-coded LSB "sub-multiplexers". The use of a 2.5b thermometer-coded sub-multiplexer ensures that switching between two neighboring values requires switching of only a single bit. This greatly increases the linearity during the fast bit dithering present in the *PS mode* by ensuring equal charge slewing when dithering any neighboring bits. The ladder itself is implemented with high resistance un-salicised poly-silicon resistors, ensuring low static power consumption while minimizing area. The high frequency switching noise in the output voltage is filtered with a 2-pole passive RC filter.

Overall, this circuit effectively adds extra bits of resolution with little area overhead. Additionally, the 1st-order ΔΣ modulator can also be instantaneously engaged or disengaged to provide more power savings. As shown in Figure 5-9, a pulse-shaped train requires the high precision mode to be activated only at pulse transitions. During the rest of the period, the modulator can be deactivated, thus minimizing the dynamic power consumed by the digital logic. In the example in Figure 5-9, the *PS mode* is activated only 15% of every period, yielding a total LED driver power saving of 25%.

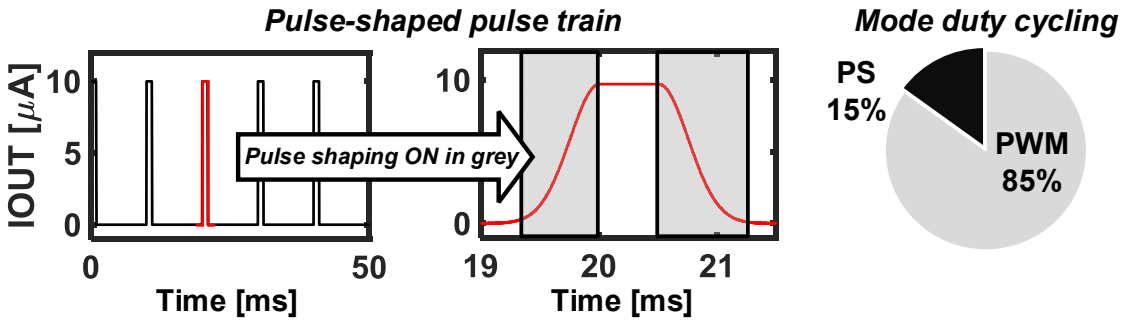


Figure 5-9. Pulse-shaped pulse train current output showing the switching between PS and PWM modes. Duty-cyling between the modes in the shown example can lead to 25% reduction in power consumption.

The output of the voltage DAC is connected to a V-I converter which uses an amplifier to maintain a current through the resistor **Rc** proportional to the input voltage (Figure 5-8 and Figure 5-10). As previously mentioned, the output current of the V-I converter can be selectively disengaged to create sharp pulses in *PWM mode*. The output current is redirected from the output current mirror to a low voltage supply using the "enable" switch. During this switching operation, the amplifier's output voltage does not change – the amplifier thus does not need a large slew rate and a high bandwidth to create sharp square waves, alleviating its power consumption requirements.

The amplifier, shown in Figure 5-10, utilizes a two-stage OTA architecture combining a recycling folded cascode stage and a common source stage. The recycling folded cascode structure delivers enhanced performance under a low voltage supply [121], [122], while the common-source output stage provides a wide output swing. The output stage drives the gate of **Mcs** which generates the appropriate current in its channel. To enhance linearity, the body of **Mcs** is connected to its source. Since **Mcs** must provide a very wide current range (0 – 10 μA) it transitions between saturation and cutoff regimes, severely varying the closed-loop bandwidth of the V-I converter.

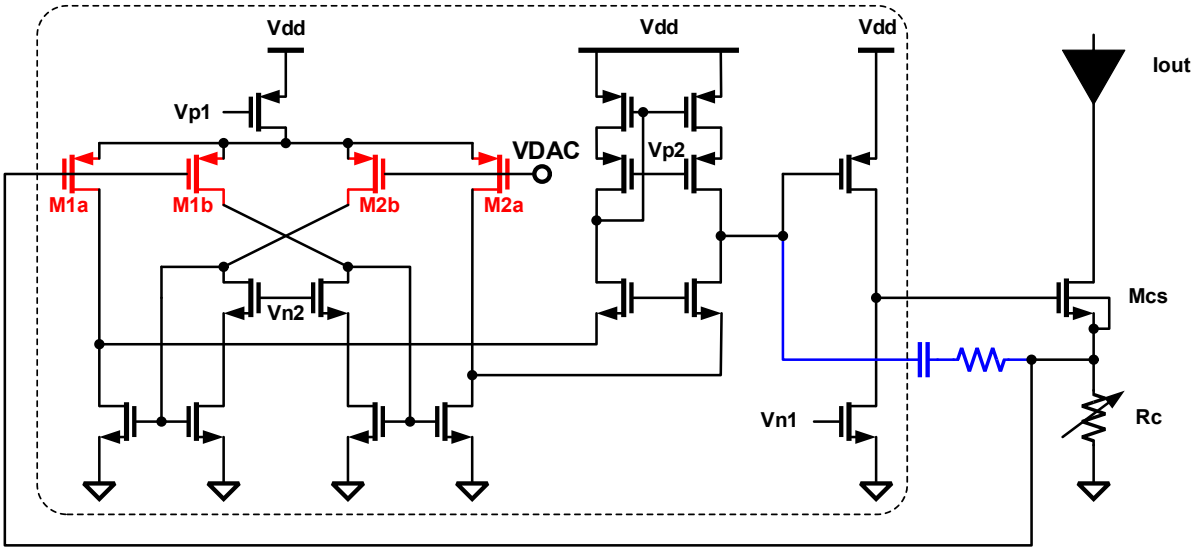


Figure 5-10. Circuit schematic of the V-I converter amplifier (inside the dotted line) and the V-I convert transistor and resistor. Transistors in red are not symmetrical to introduce offset. Miller compensation capacitor and resistor is highlighted in blue.

The Miller compensation capacitor (and zero-eliminating resistor) is thus placed between the first and 3rd stage output to stabilize the amplifier while equalizing bandwidth over its operating regime. When **Mcs** is in saturation, the higher gain of the last two stages will increase the Miller capacitance, limiting the dominant pole and provide a wide phase margin. When **Mcs** is in the cutoff region, the Miller capacitance is reduced due to reduced gain of the **Mcs** stage, thus increasing the frequency of the dominant pole and maintaining the amplifier's bandwidth. However, since the low-frequency gain is reduced, the stability of the amplifier is maintained.

The V-I converter may suffer inaccuracies from two sources of mismatch: the amplifier offset, and the absolute resistor accuracy. A positive amplifier offset may severely impact the performance since it would introduce a steady quiescent current through **Mcs** even if the voltage DAC output is 0 V. To mitigate this problem, a mismatch is intentionally introduced to the input transistors **M1a**, **M1b**, **M2b**, and **M2a** to provide an inherent negative offset which is easy to

calibrate by increasing the voltage DAC output. The resistor can be calibrated through the switchable parallel resistor branches that can change the total resistance across **Rc**.

Finally, the output of the V-I converter is fed into a high-voltage current mirror, providing a transition from the 1 V domain to the high-voltage domain necessary to drive the LEDs. Like the circuit described in Chapter 4, the current mirror uses long-channel cascoded thick-oxide PMOS transistors to prevent oxide breakdown beyond the maximum supply voltage in the technology and provide high output impedance to maintain high output current linearity. The current mirror nominally operates at 6.7 V supply voltage and can provide linear output current at output voltages up to 5.5 V.

5.4.2 Fully-Integrated Step-up Voltage Regulator

The need for a step-up voltage regulator arises from the need to convert the 3.7 V battery supply voltage to 6.7 V supply for level-shifting current mirror. The voltage regulator needs to maintain good efficiency over a large current range (1 μA – 1 mA). Simultaneously, it is desirable to eliminate any off-chip components including capacitors and large inductors since a high LED driver channel count would prohibitively scale the area needed to accommodate them.

The voltage regulator circuit is shown in Figure 5-11 (a). It consists of two 2-phase (or effectively 4-phase) switched-capacitor voltage doublers controlled by a dynamic-voltage-comparator-based regulator providing an effective pulse density modulation (PDM) control. The effective 4 phases reduce the overall ripple size. The regulator monitors the output voltage through a 1/10 resistor divider. The total resistance of the series divider is 2 MΩ which minimizes the static current flow. The output of the divider is fed into a dynamic zero-on-reset comparator which creates a clock signal when the divided voltage drops below VREF (set to 670 mV). The dynamic comparator is clocked by the 200 MHz clock reference shared with the ΔΣ modulator. Its design

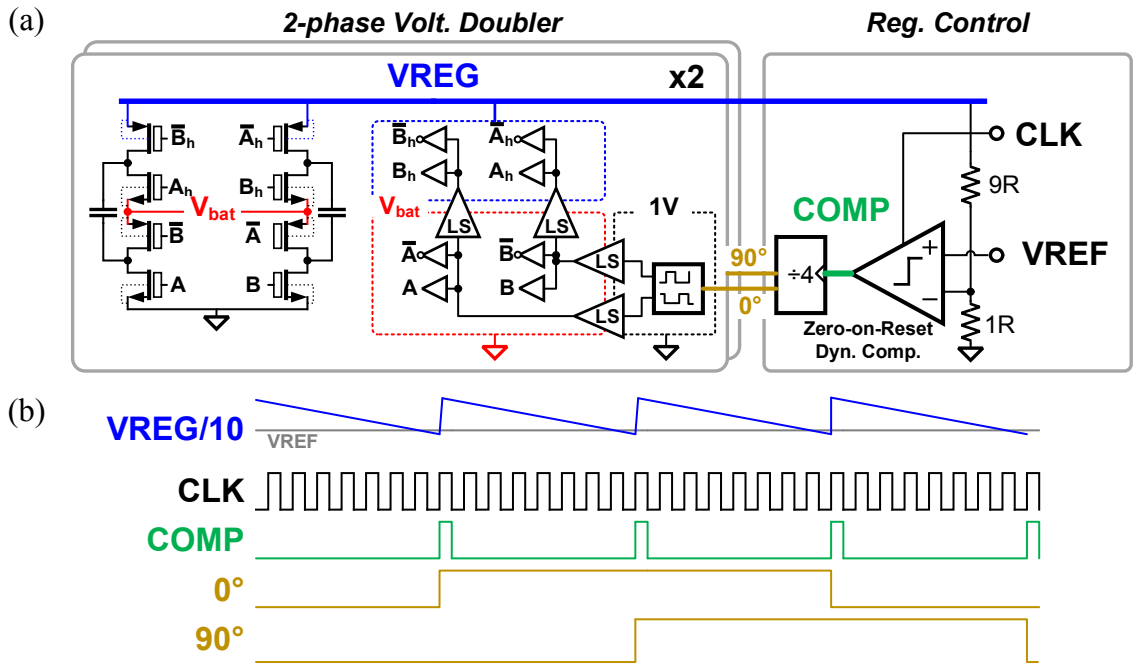


Figure 5-11. (a) integrated step-up voltage regulator circuit schematic and (b) control signal timing diagram.

is optimized for efficiency (using minimum-sized input stage transistors) since accuracy is not essential in its operation. The output of the comparator is fed into the clock input of a counter which provides 2 phases for the 2 voltage doublers (as shown in Figure 5-11 (b)). Each phase drives a non-overlapping clock generator which provides non-overlapping phases for the switch drivers. The clock phases are level-shifted first to the 0 – 3.7 V battery voltage domain, second to the upconverted voltage domain 3.7 V – 6.7 V. The second set of level shifters use additional capacitor-boosting to ensure proper functionality even during start-up [123]. Inverter-based switch drivers control the 1:2 capacitor ladder. The switch and capacitor sizes are set to provide full range current to the µLED driver while minimizing switching power consumption and output voltage ripple. The circuit uses on-chip thick-oxide MOS and MIM capacitors which are placed directly on top of driver circuitry. A full metal layer gap and additional ground shielding above sensitive analog circuitry minimizes the coupling of switching noise.

5.5 Benchtop Measurements

The chip prototype is fabricated in 0.18 µm CMOS and occupies 7.66 mm^2 including the surrounding pad rings and decoupling (Figure 5-12).

The recording circuit occupies 0.012 mm^2/ch. Figure 5-13 shows the measured input referred noise spectrum and the analog gain of the channel as a function of frequency. The integrated input referred noise between 1 Hz and 15.6 kHz is 5.7 μV_{rms}. The channel maintains a flat gain of 50 dB between 1 Hz and 15.6 kHz.

The LED driver circuit occupies 0.089 mm^2/ch. Linearity of the LED driving DAC was analyzed by measuring voltage generated by the current across a 4.7 kΩ resistor. Figure 5-14 (a) shows 10-bit DNL and INL plots generated in the *PWM mode*. The maximum DNL and INL values are 0.403 and 1.37 respectively. Additionally, the fidelity of the high-resolution *PS mode* was tested by generating a 10 Hz full-scale sinusoidal current across a 4.7 kΩ resistor and measuring the resulting voltage. The output spectrum in Figure 5-14 shows a peak at 10 Hz with 42 dB SNDR. Harmonics stemming from driver non-linearities are the major source of this effective resolution loss.

The recording circuit measured power consumption per channel is 23.6 µW/ch. The LED driver consumes 31 µW of quiescent power at 3.7 V battery supply. The efficiency of the LED driver was measured across the narrow Li Poly battery output voltage variations (3.6 – 3.8 V) and it is shown in Figure 5-15 (a). It achieves a peak efficiency of 50% at 1 mA output current. The total power consumption of the IC including the PMU is 3.04 mW when stimulating one µLED at 100 µA and 10% duty cycle. This translates to about 3 h of operation if the chip is to be powered by an ultra-light-weight 10 mAh 0.5 g Li-ion battery (this does not include the wireless module power consumption). Figure 5-15 (b) shows the power consumption distribution of the full

interface IC while maintaining the previously stated operating condition. Due to the inherently inefficient architecture of the LDO linear voltage regulators, they account for over 50% of power consumption. This can be mitigated in the future designs by employing more efficient switching regulators.

In the final benchtop test, actual μLEDs are driven by the on-chip μLED drivers. The evaluation board including the interface IC is connected to an optoelectrode with μLEDs via a ~1.5-foot breakout cable. The voltage at the μLED input was buffered by an AD825 op-amp connected in unity-gain feedback and then recorded with an oscilloscope. The 4 major pulse shapes– square, trapezoidal, sine-rise, and Gaussian-rise pulses – of varying amplitude were generated and monitored. The voltage was then converted into current via I-V curve interpolation and the currents are shown in Figure 5-16. A small ripple noise found at the pulse peaks is the 60 Hz line voltage noise from the measuring equipment amplified by the voltage-to-current interpolation.

Table 5-1 compares the chip and system parameters of the fabricated IC with previously published optogenetic systems incorporating optogenetic-specific ASICs. The fabricated IC demonstrates the highest-level integration and the first incorporation of arbitrary waveform generation for optical pulse shaping into the LED driver. These features allow the proposed integrated headstage to achieve state-of-the-art power consumption, form factor, and recorded signal fidelity.

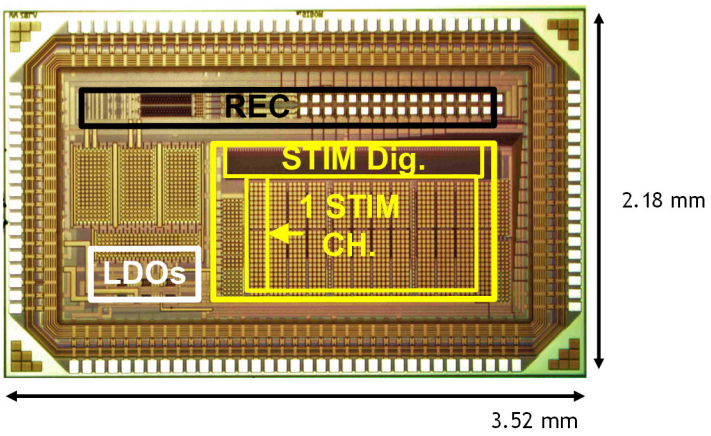


Figure 5-12. Die photo.

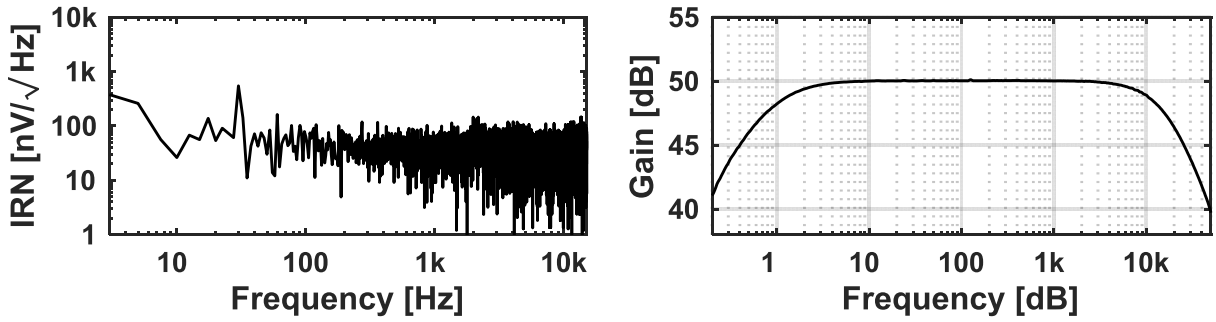
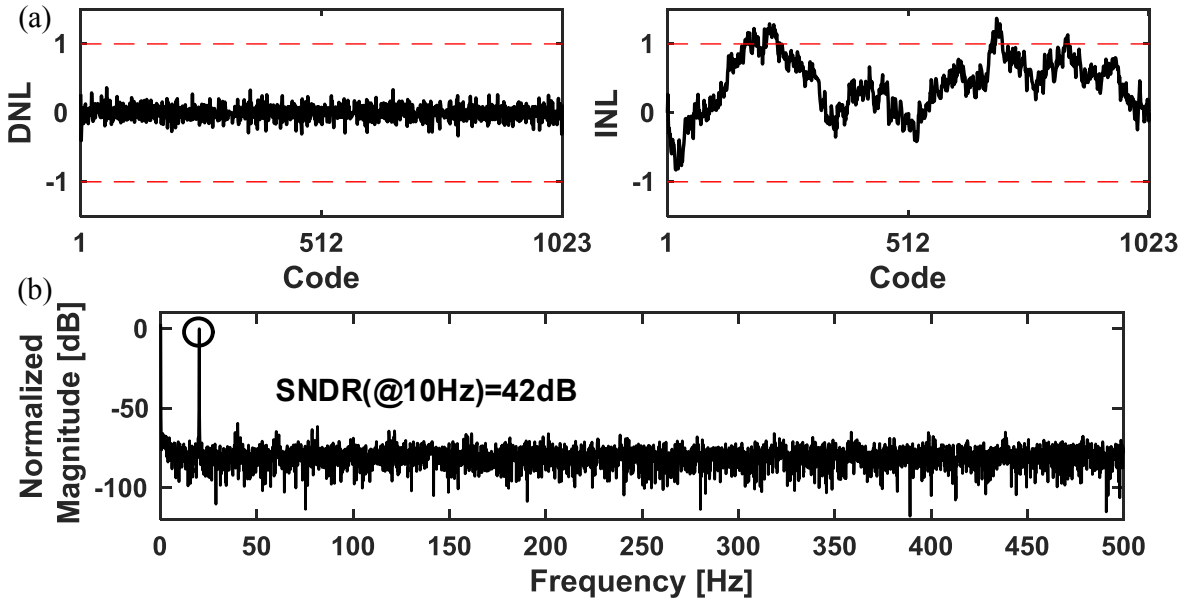


Figure 5-13. Measured recording circuit input referred noise and gain output frequency spectrum.



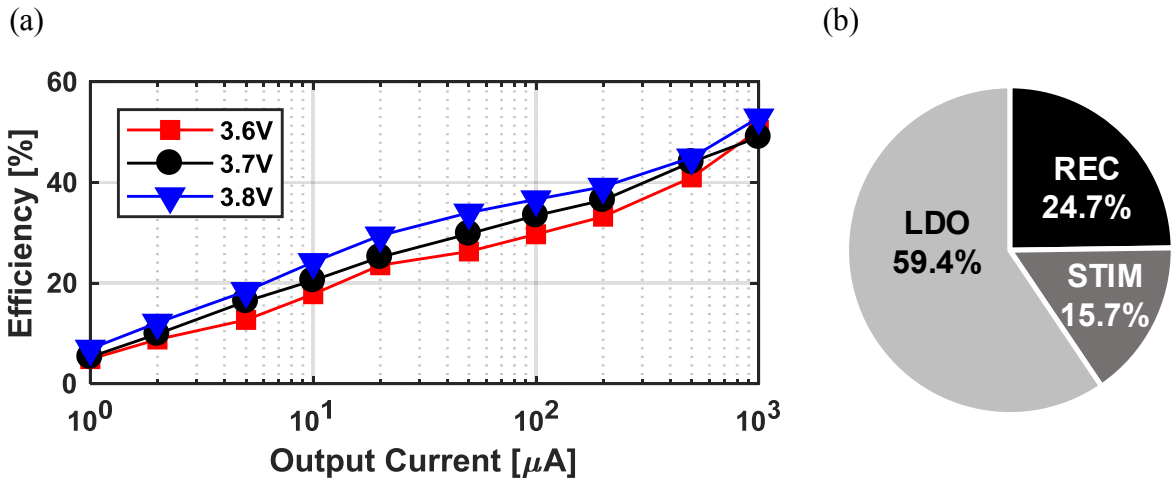


Figure 5-15. (a) LED driver total efficiency measured across a range of output currents and input voltages; (b) power consumption distribution of the interface IC when driving one μLED device at 100 μA and 10% duty cycle.

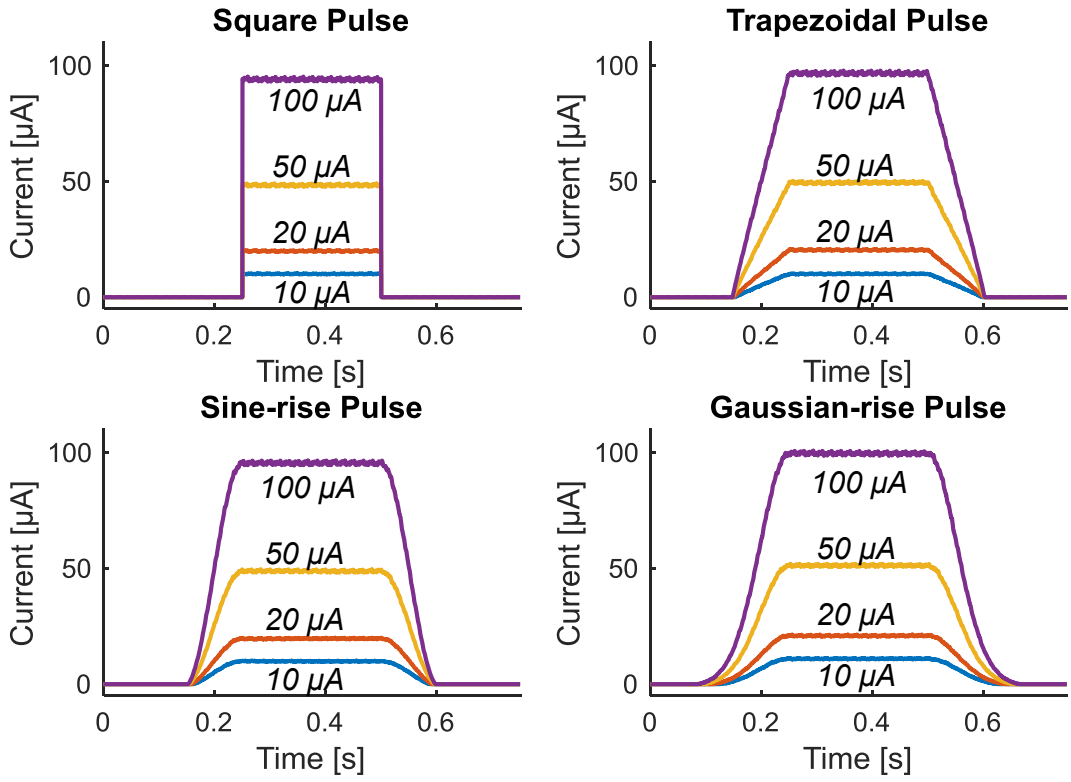


Figure 5-16. Current pulse shapes driven across the μLEDs with the LED driver operating in *PS mode.*

Table 5-1. Optogenetic-specific ASIC system comparison table.

	Technology			# rec. # stim.	Power Source	Stim. Range Stim. Res.	Stim Control	Rec. BW	Rec. Res
	Rec.	Stim.	PMU						
Paralikar 2011 [108]	N/A	0.8 µm	0.8 µm	-/2	RF 3.8 V bat.	0 – 51 mA 10-bit	PWM, ampl.	N/A	N/A
Zhao 2015 [48]	0.35 µm		N/A	4/6	N/A	0-1 mA 8-bit	PWM, ampl.	500 Hz (1 kS/s)	10-bit
Mendrela 2017 [117]	COTS	0.18 µm	COTS	32/12	9 V bat.	0 – 1mA 10-bit	PWM, ampl.	7.5 kHz (30 kS/s)	16-bit
Chen 2017 [110]	0.18 µm		N/A	1/1	N/A	0 – 330 mA 8-bit	PWM, Ampl.	5 kHz	N/A
Gagnon-Turcotte [111]	0.13 µm		N/A	10/4	3.7 V bat.	HW Preset	PWM, Res. Set	7 kHz (20.8 kS/s)	14-bit
Jia [112]	N/A	0.35 µm		-/16	RF	0 – 10 mA 2-bit	PWM Ampl.	N/A	N/A
This Work	0.18 µm			32/12	3.7 V bat.	0 – 1 mA 10 bit	Arb. Wave	15 kHz (32 kS/s)	10-bit

5.6 *In Vivo* Measurements

The system was further validated in a series of *in vivo* experiments. The experimental setup is shown in Figure 5-17. The chip (packaged in a CPGA-120 package) was placed in a socket on a custom evaluation board. The evaluation board utilizes two Opal Kelly FPGA boards to control both recording and stimulation SPI buses as well as to communicate with the PC. The analog outputs of the chip are connected to a passive µLED probe headstage via separate shielded cables.

Two male mice (30 g, 14 weeks old) were used in this study. The animal procedures were approved by the Institutional Animal Care and Use Committee of the University of Michigan (IACUC; protocol number: PRO-7275). The surgery was performed by Dr. Mihály Vöröslakos. The mice were kept on a regular 12 h–12 h light–dark cycle and housed in pairs before surgery. No prior experimentation had been performed on these animals. Atropine (0.05 mg/kg, s.c.) was administered after isoflurane anesthesia induction to reduce saliva production. Stages of anesthesia were maintained by confirming the lack of nociceptive reflex. Skin of the head was shaved and a 1 mm diameter craniotomy was performed 1.75 mm posterior from bregma and 2 mm lateral of the

midline. The dura was removed over the dorsal CA1 region of the hippocampus and the mice were injected with AAV5, CaMKII promoter driven ChR2 (AAV5-CaMKIIa-hChR2(H134R)-EYFP), resulting in expression of ChR2 in pyramidal neurons. After the surgery, the craniotomy was sealed with Kwik-Sil (World Precision Instruments) until the day of recording. On the day of recording, the mice were anesthetized with isoflurane, the craniotomy was cleaned and the optoelectrode was lowered to the CA1 region of the hippocampus.

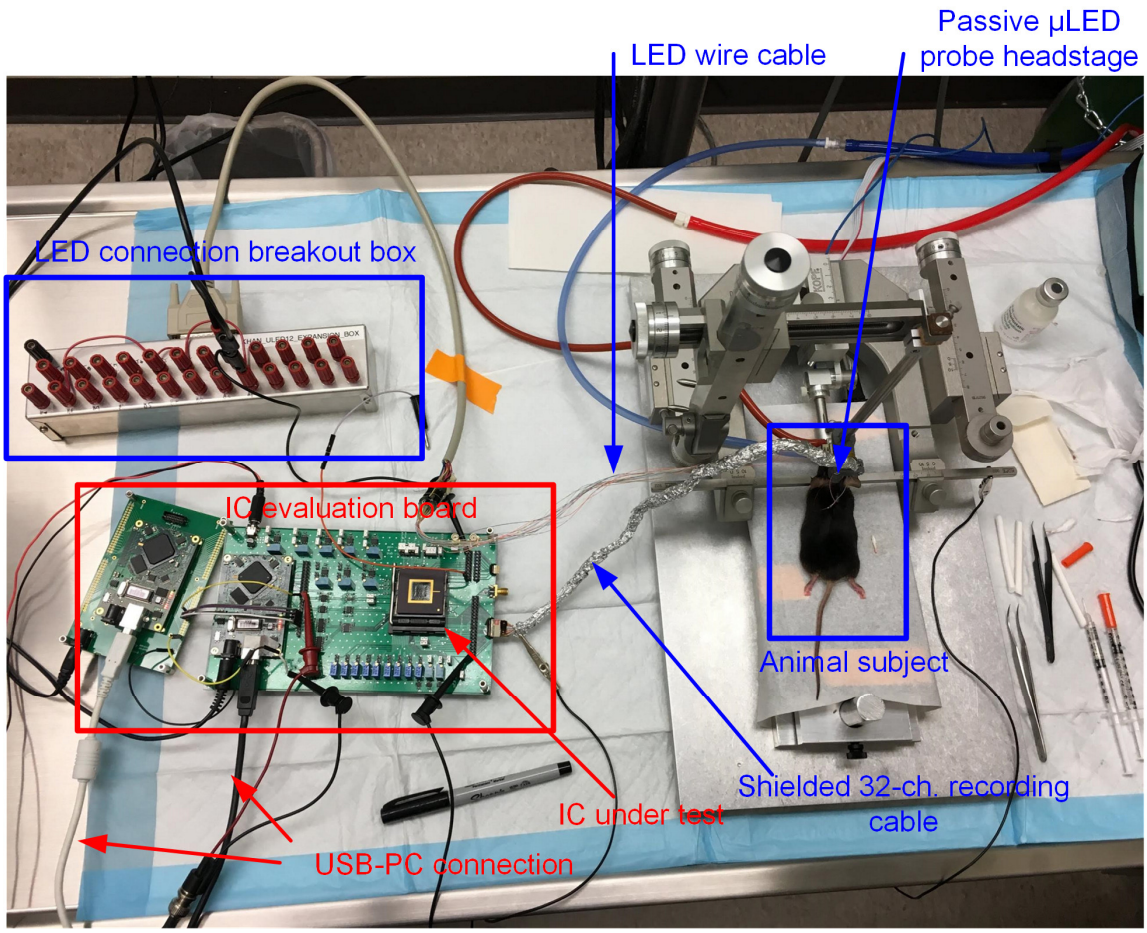


Figure 5-17. *In vivo* test setup.

In Figure 5-18, the system's operation is validated by driving the bottom µLED on shank 3 with a rectangular pulse with an amplitude of 100 µA and 250 ms pulse width. While some form of artifact is present in all recorded 32 channels, the recording sites on shank experience the largest

artifact as expected. We also observe high LFP activity in shank 3 corresponding to the stimulation. In Figure 5-18 (b), an enlarged waveform from the shank-3 channel-6 recording site is shown. The fidelity of the recording allows spike detection and sorting as shown in the spike raster plot below.

To accurately analyze the effect of pulse shaping, we devise an experiment where a single μLED is stimulated with a preprogrammed current waveform consisting of 31 different pulse shapes (with a peak amplitude of 100 μA and duration of 250 ms) where each pulse shape window is 750 ms long. The complete waveform consists of 1 square wave, 10 trapezoidal pulses of varying rise times, 10 sine-rise pulses of varying ω parameters, and 10 Gaussian-rise pulses of varying σ parameters (see pulse definitions and parameters in section 5.2.2). A graphical analysis of the recorded artifacts is shown in Figure 5-19. Raw data from a selected channel on the stimulated shank (shank-3 channel-4 shown in Figure 5-19 (a)) is divided into 0.75 s windows, one window per single stimulation pulse. The windows are then sorted, detrended, and averaged for every pulse type. In Figure 5-19 (b), a full averaged pulse waveform is shown. We observe that the artifacts appear both at the beginning and at the end of the pulse. They consist of two major components: a sharp spike-like high-frequency artifact and a slow-decaying low frequency artifact. While we do not observe a substantial change in the low frequency artifact with varying pulse shapes, we disregard it in this analysis since it can be easily filtered out with a high-pass filter. The dependence of the high-frequency artifact on the pulse shape is shown in Figure 5-19 (c)-(f). In Figure 5-19 (c)-(e), the trapezoidal, sine-rise, and Gaussian-rise pulses and the corresponding averaged artifacts are plotted. A rectangular pulse artifact is also shown in cyan for comparison. The transient artifacts not only have different peak amplitudes for different pulses and parameters, but also distinct shapes for corresponding pulse types. Gaussian-rise pulses result in the smoothest artifact curves and lowest peak amplitudes, not unlike in simulations in section 5.2.2. However,

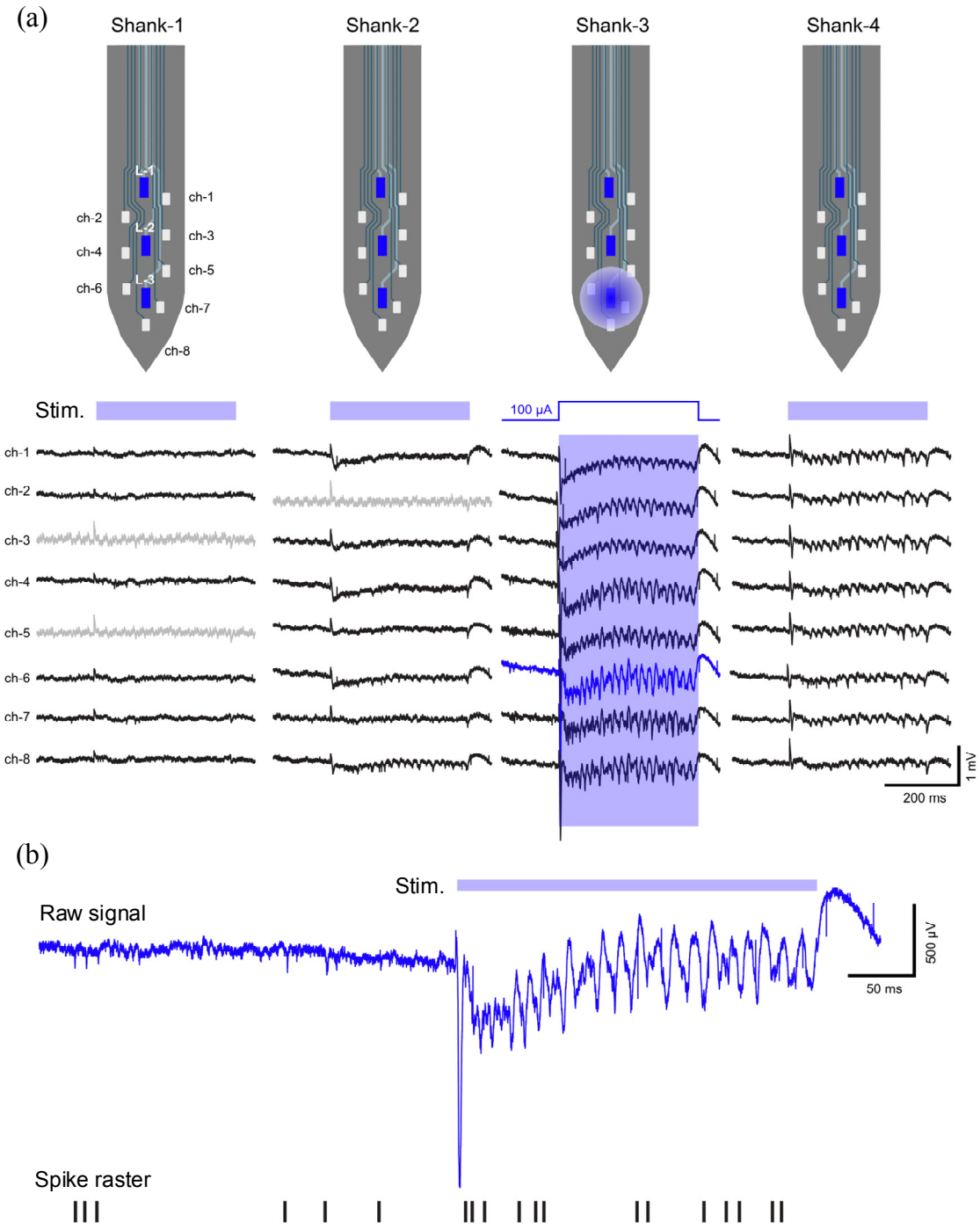


Figure 5-18. (a) Wideband (1-3000 Hz) spiking activity recorded on a four-shank µLED probe from CA1 pyramidal layer of the hippocampus of an anesthetized mouse expressing ChR2 in pyramidal cells. Light-induced artifacts are visible on all channels during rectangular 100 µA-driven light pulses. Note the most prominent artifacts appear on shank-3 (shank-3, LED-3 was used). Stimulation induced local field potential change and spiking. Grey channels connect to broken recording sites (Z_{el} > 10 MΩ). (b) High-pass filtered signal of the blue highlighted channel. Rasters at the bottom show multi-unit activity which is altered by light stimulation.

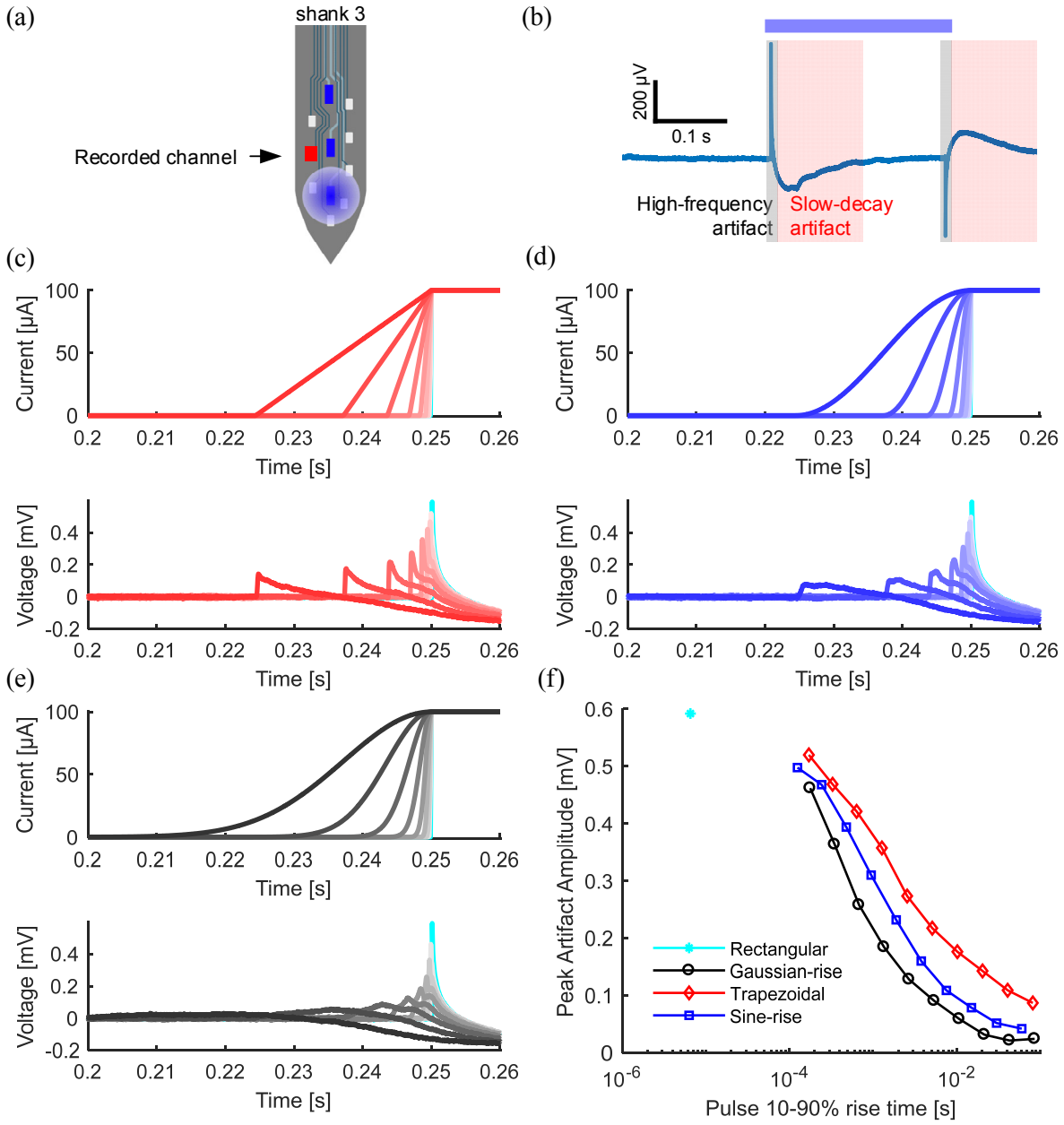


Figure 5-19. (a) artifact analysis stimulation is performed on bottom µLED on shank 3 while recordings are taken from the ch-4 on shank 3. (b) i*n vivo* recordings are averaged over each corresponding pulse-shaped stimulation period (peaking at 100 µA). Artifacts appear both at light activation and deactivation. Averaged artifact waveform shows a high-frequency component and pulse-shape-independent slow-decay component. (c)-(e) show the trapezoidal, sine-rise, and Gaussian-rise current pulse shapes and the mean high-frequency artifacts, respectively. Rectangular pulse artifact is shown in cyan for comparison. Peak artifact amplitudes versus pulse rise time are shown for different pulse shapes in (f).

the absolute magnitudes of the artifacts are much greater *in vivo*, pointing to inadequate simulation models. We also observe that the artifact peaks occur at the start of each pulse, which is most likely related to the higher μLED impedances at low bias currents (sub-1 μA). Figure 5-19 (e) provides a direct comparison of the artifact peak amplitudes as a function of current pulse rise time (defined as time between the 10% of maximum amplitude to 90% of maximum amplitude). The Gaussian-rise pulses consistently show lower peak amplitudes, proving that it is a good candidate for a stimulation pulse shape. When compared to a standard rectangular pulse, a Gaussian-rise pulse with a 1 ms rise time shows almost a x3 reduction in artifact amplitude.

Before we conclude the effectiveness of the pulse shaping scheme, we must also prove the optogenetic efficacy of the optical pulses. To do so, a repeated 31-pulse waveform (100 μA amplitude) is applied to a μLED (shank-1 LED-1) and a waveform is recorded from a site neighboring a light sensitive spiking neuron (shank-3 channel-5). The location of the active sites is shown in Figure 5-20 (a). The peristimulus time histogram in Figure 5-20 (b) shows strong modulation in firing rate due to the rectangular pulse stimulation. The mean spike waveforms and the autocorrelation histogram show appropriate neural firing characteristics during stimulation. In Figure 5-20 (c), the mean spiking rates for all tested waveforms are shown as a function of rise time. No substantial change in spiking rate is observed in the pulse-shaped waveforms as compared to rectangular pulses. PSTH plots in Figure 5-20 (d) additionally verify that there are no systematic changes in spiking response due to different pulse shapes.

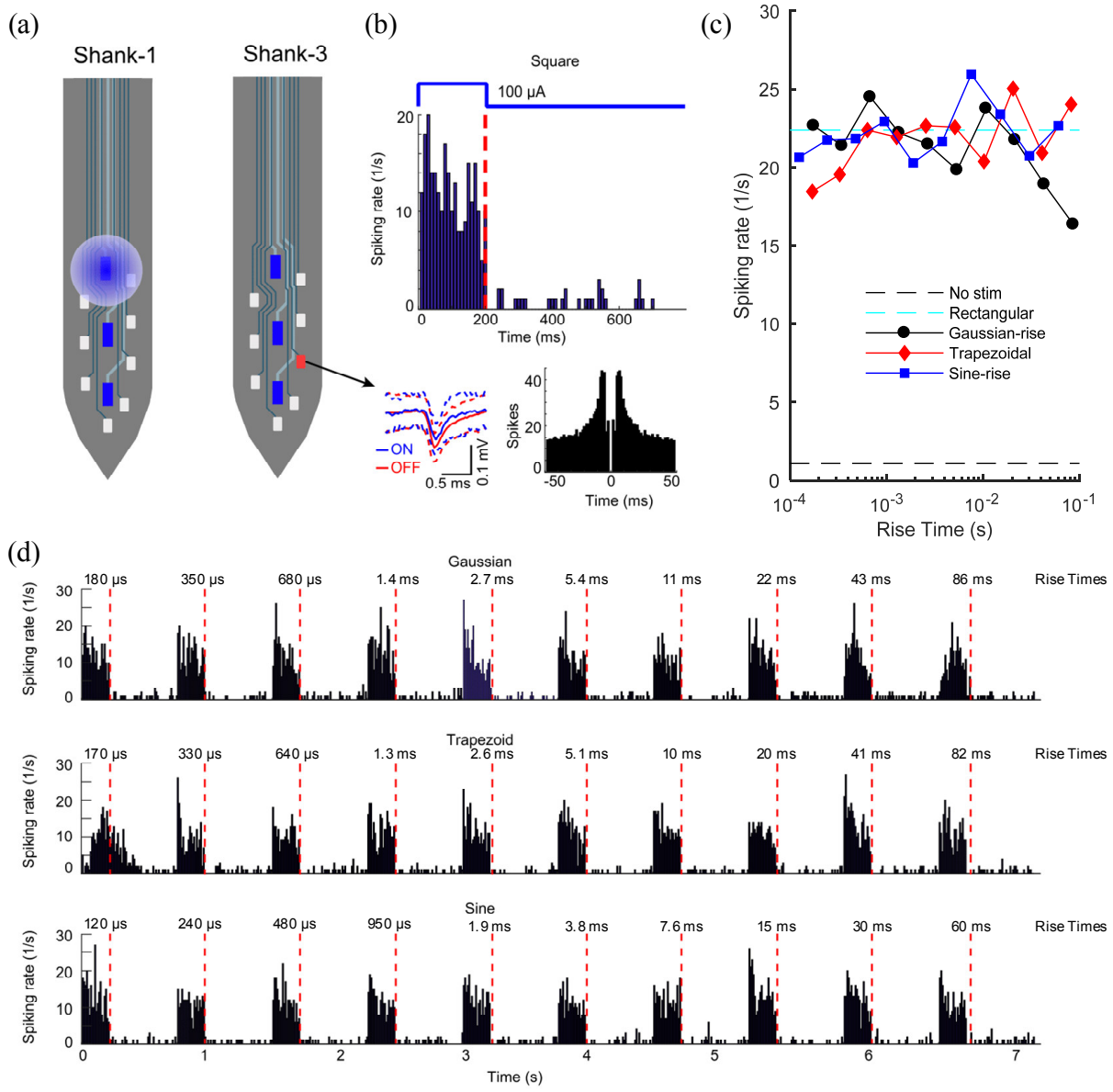


Figure 5-20. (a) Shank schematic shows the location of stimulation (shank-1 LED-1) and the recording site where the modulated neuron was recorded (shank-3 channel-5). The light sensitive neuron on shank-3 is probably driven by another neuron close to shank-1, which we did not record from (the recorded neuron is 500 µm from the µLED). (b) Peristimulus time histogram (PSTH) shows strong firing rate modulation due to 100 µA 200 ms rectangular pulse stimulation. Bottom inset shows identical spike waveforms during stimulation (100 µA, 460 nm) and control periods (blue and red, respectively). Autocorrelation histogram is shown for the same neuron during light stimulation. (c) Mean spiking rate altered by light stimulation does not depend on the applied pulse shape nor its rise time (n = 56 trials). (d) Full PSTHs at different pulse shapes. Red lines mark the falling edge of each pulse.

5.7 Conclusion

In this chapter, we present the design and verification of an opto-electrophysiology neural interface IC for a wireless headstage with an on-chip artifact reduction scheme. To reduce the headstage form factor, the IC features the highest level of integration to date by combining 12 μLED driver channels, 32 wideband neural recording channels, and a power management unit that minimizes the number of passive components. This reduction is aided by the full integration of inductor-less step-up voltage regulators which allow efficient (up to 50%) but wide-current-range high voltage driving of the μLED. The system also introduces a new on-chip artifact reduction scheme through the means of pulse shaping. By changing the transition shape and rise time of the nominally rectangular pulses, the amplitude of the transient artifact can be decreased. A high-resolution DAC-based LED driver architecture offers precision control of μLED current waveforms while maintaining efficient operation.

A prototype, fabricated in 0.18 μm CMOS technology, occupies 7.66 mm^2. The power-conscious system level design achieves a power consumption of 3.04 mW under typical operating conditions. The optical pulse shaping scheme was proven *in vivo* and shows up to x3 artifact reduction using a Gaussian-rise instead of a rectangular pulse, while maintaining the total rise time under < 1 ms.

CHAPTER 6

Contributions and Future Work

6.1 Contributions

The main contribution of this dissertation can be distilled to a set of novel architectural solutions that enable efficient high-fidelity bidirectional neural interfaces. The engineering problem that these systems attempt to address is how to efficiently reduce noise and artifacts in neural recordings while simultaneously performing stimulation. We subdivide these attempts into three distinct chapters, where each chapter presents either a solution tailored to a particular interface type, or a solution to a different facet of the overarching problem. Chapter 3 introduces an integrated circuit for simultaneous electrical recording and electrical stimulation which cancels the large artifacts associated with this interface before they saturate the recording channels. Chapters 4 and 5 describe the design of a neural interface for electrical recording and optogenetic stimulation. Chapter 4 focuses on the miniaturization of the headstage through the integration of ASIC-based electronics and microfabricated optoelectrodes while Chapter 5 increases the level of system integration for the eventual addition of a wireless modules and introduces an artifact-reducing optical stimulation architecture. All the solutions presented in these chapters are designed under the constraint of minimizing power consumption.

A more detailed list of contributions and achievements is shown below:

(Chapter 3) Bidirectional neural interface IC with active stimulation artifact rejection

- A front-end-based active stimulation artifact cancellation technique is developed for neural recording by employing a mixed-signal adaptive noise-cancelling filter, achieving up to 42 dB of measured artifact attenuation.
- A reconfigurable common-average referencing (CAR) scheme is implemented in analog domain to reduce cross-channel common-mode noise and relax dynamic range specifications. Up to 39.8 dB cross-channel noise suppression is measured.
- An energy-efficient SAR ADC switching scheme, called range-adapting (RA), adaptively adjusts its dynamic input range to the amplitude of the recorded neural activity.
- The 8-recording-channel and 4-stimulation-channel system prototype is fabricated in 0.18 μm CMOS, occupying 0.17 mm^2 per channel and consuming 330 nW per channel. The fabricated IC is characterized and tested *in vivo* in an epileptic rat model.

(Chapter 4) Miniature Headstage for High Resolution Closed-Loop Optogenetics

- We successfully integrate the highest number of electrical recording (32) and optogenetic stimulation channels (12) to date in a single headstage system using microfabricated optoelectrodes and multi-channel recording and stimulation ASICs.
- A custom LED-driving ASIC is designed and fabricated enabling high amplitude precision (1 μA current or 68.5 nW radiant flux) and temporal resolution (update rate < 10 kHz) of optical output power.
- Single animal *in vivo* experiments validate the headstage's capability to precisely modulate single neuronal activity and independently modulate activities of separated neuronal populations near neighboring optoelectrode shanks.

Chapter (5) Opto-Electrophysiology Neural Interface IC with Artifact-Preventing Optical Pulse Shaping

- We achieve the highest level of integration for an opto-electrophysiology system combining 32 recording, 12 μLED driver channels, and a power management unit to minimize the area footprint.
- A novel fully-integrated inductor-less step-voltage regulator circuit upconverts a low Li Poly battery voltage (3.7 V) to the high μLED input voltage. The full μLED driver channel achieves up to 50% efficiency over 0 – 1 mA current range and consumes 31 μW quiescent power, while occupying only 0.089 mm^2/ch.
- High-precision LED driver circuit efficiently generates pulse-shaped μLED current waveform that reduce stimulation artifacts in recordings. This scheme is validated *in vivo* and has shown effective stimulation and artifact reduction.
- The prototype IC is fabricated in 0.18 μm CMOS, occupies 7.66 mm^2, and consumes 3.04 mW under typical operating conditions.

6.2 Future Research Directions

Since the field of neural interfacing is still in its infancy, it is ripe with topics that needs to be tackled. While the biggest tasks ahead most likely lie in the realms of neuroscience and microfabrication, there are many challenges on the electronic and system side as well. Let us use the thesis content as the starting points of this discussion.

The proof-of-concept prototype in Chapter 3 can be further expanded by adding more recording and stimulation channels to match the needs of next generation microelectrode arrays. The artifact adaption scheme should then consider not just a single source of stimulation but

multiple stimulation channels simultaneously. Further DSP circuit optimization will be required to increase the sampling rate for AP recording – the filter will require longer response times, and thus a higher number of taps. The use of analog signal processing might alleviate the amount of additional resources. However, the usefulness of this approach will be greatly reduced if its additional resources surpass those of brute-force methods such as the increase of input dynamic range. At the time of writing of this thesis, several such solutions are gaining popularity. By increasing the dynamic range, the artifact processing can be pushed to a generic processing engine in the back-end, greatly increasing its reconfigurability and usefulness.

The opto-electrophysiology systems introduced in Chapter 4 and 5 make several strides towards achieving the goal of miniaturization, yet there is still a long way before fully utilizing our current technological capabilities. The first task that needs to be done is the completion of the wireless system proposed in Chapter 5. The integration of the optoelectrode, the neural interface IC, the wireless transceiver IC, a crystal oscillator, a duplex antenna, and other required passive components needs to be done on a small, lightweight platform. The platform may range from a thin printed circuit board, to a flexible PCB, or even a custom-made PI cable. The form factor of the platform will affect its implantation procedure as well as the range of behaviors the experimental subject will be able to perform. Extensive testing needs to be performed to assess the system's reliability and its wireless range.

The performance of the optogenetic neural interface IC can be improved in several ways. The power consumption can be reduced by substituting the LDO linear regulators with switching regulators which perform large voltage downconversions more efficiently. The extra die space on the chip may be used to integrate the capacitors in order to eliminate the regulators' off-chip components. By lowering the power consumption of the circuit, we can also employ energy

harvesting techniques to power the headstage wirelessly, eliminating the bulky battery which can consume more than 50% of the system mass. Furthermore, complete integration of a wireless module with the interface circuitry on a single die will enable even greater reduction of the form factor. It will require a reimplementation of circuitry in smaller technology nodes (necessary for an efficient wireless transceiver), as well as the integration of a clock recovery circuit from the wireless telemetry and an on-chip antenna.

There are still many unanswered questions about the dependence of artifacts on the structure and the materials used in optoelectrodes. Better models for optical artifact coupling should be developed to allow a design of more optimal pulse shapes for even greater artifact reductions. While the SPICE models give us some insight into the trends of capacitive coupling artifacts, they do not yet explain the formation of low-frequency slow-decaying artifact. A more effective photovoltaic effect simulation may shed light into the possible cause of the low-frequency artifact.

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