Charge-Domain Analog/Mixed-Signal Circuits and Applications

by

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CHAPTER 1.

INTRODUCTION

The goal of technology has been and always will be to make its products available to more people. Fundamentally this is because technologies are designed to add value to people's lives and to trigger a demand. Equally importantly, there is a whole industry that depends on cultivating and then sating those demands. Incessantly, technology has striven to deliver more devices into the hands of happy customers, and this trend continues with the Internet of Things (IoT). Projected to infuse the world with tens of billions of new devices in next several years, the IoT is the latest and the largest mega-trend in the world of technology.

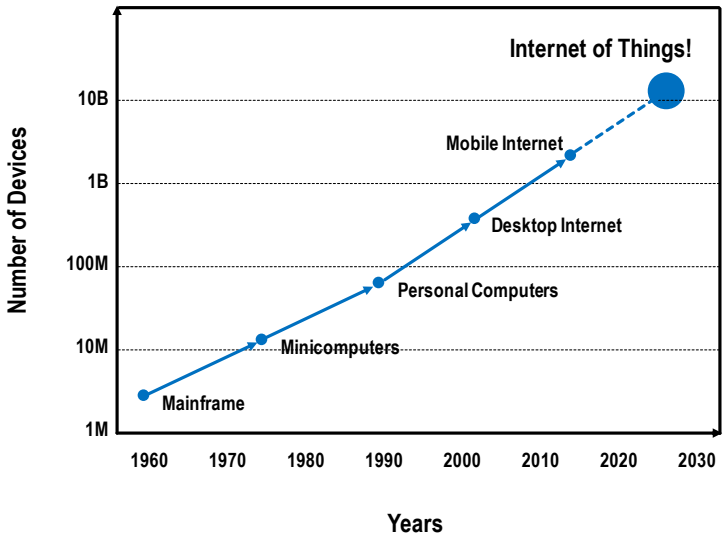


Figure 1. Main drivers in the trend of technological evolution. IoT is projected to add tens of billions of devices during the next decade.

The IoT offers tangible value by compacting sensors and artificial intelligence to a miniaturized form factor and coupling them with connectivity so that technology become available

in every area of our lives. Embracing this technology will enable us to continuously assimilate vital information about ourselves and our surroundings and manipulate it to a degree not previously possible. With the foundation of a strong communicational and computational infrastructure, we now possess the capacity to sustain such a mass-deployed network of simple but intelligent things. The IoT is here to prompt real change.

With the maturation of supporting technologies such as cloud computing, smart mobile handsets, hi-fi sensors, and wireless data connectivity, the time for the IoT is ripe. These technologies allow information to be gathered and processed on a mass scale. Furthermore, with more advanced key technologies for the IoT being realized (e.g., low-power connectivity/computing, neural network-based intelligence, high-density solid-state battery, and wireless sensor nodes), the IoT will soon be able to provide substantial improvements in our lives.

We, as circuit designers, stand at the forefront of delivering the promises of the IoT. The capability and success of IoT devices are highly dependent on how well we can design circuits, the core components of such intelligent devices, with respect to viability, cost-effectiveness, and resource-efficiency. This is a new challenge for circuit designers in that there has been little discussion of the resource budgets of these nearly invisible and ubiquitous devices as they represent a distinct diversion from the traditional trajectory of mainstream industry as epitomized by Moore's law.

Although Dr. Moore may not have expected his observation to be interpreted this way, traditionally the law has been used to drive the industry to make use of surplus transistors per dollar to integrate more features, performance, and functions into a circuit product. All of this was supposed to be accomplished while maintaining the price point. Often the primary goal has been to push the performance limit to beat competitors, and aided by the underlying physics of scaling,

the industry was simply set toward maximizing performance through a scaling speed race. Evidently, the word “scaling” in the semiconductor world has been synonymous with better performance in the past decades.

This approach worked well because the dominant market of semiconductors has been in computation, which involves CPUs and memories that scaled very well in terms of both cost and performance as technology improved. Also, the resources available for these computer elements have been generous so that the industry could focus on this singular drive for better performance. However, recently, scaling is finally slowing down to a level where devices are getting neither cheaper nor faster due to physical barriers. Thus, the economics of making faster or more powerful computers is becoming less and less attractive. Currently, the industry is striving to determine what to do with its honed economics of surplus transistor per dollar or diminished dollar per transistor besides just pursuing more Moore.

As we near the saturation of the 30-year drive of Moore’s law in computers, the semiconductor industry is turning to the IoT and its associated non-traditional applications that have different measures of value. This new development has been coined “More Than Moore” and is focused on scaling the industry beyond the paradigm of Moore’s law of computers and exploring new areas of future exponential growth. Married with the concept of the IoT, “More than Moore” promises to add value in extremely different and more diversified ways than simply making computer boxes run incrementally faster, as had been the focus in the past.

The philosophy behind the IoT that brings the industry to a new level is, in my opinion, that not all useful things require powerful performance. Oftentimes, it is preferred that IoT devices perform small load of interesting tasks in an extremely harsh environment. This type of situation usually arises when devices are interfacing with the natural world. In the natural world, events

happen in terms of seconds, minutes or hours instead of pico-seconds, a timeframe more common in the artificial world of computation. Therefore, such a task requires much less bandwidth. However, because IoT devices need to be deployed in unconventional spaces to access the large volume of untapped information, the resources to be spared per device can be extremely small.

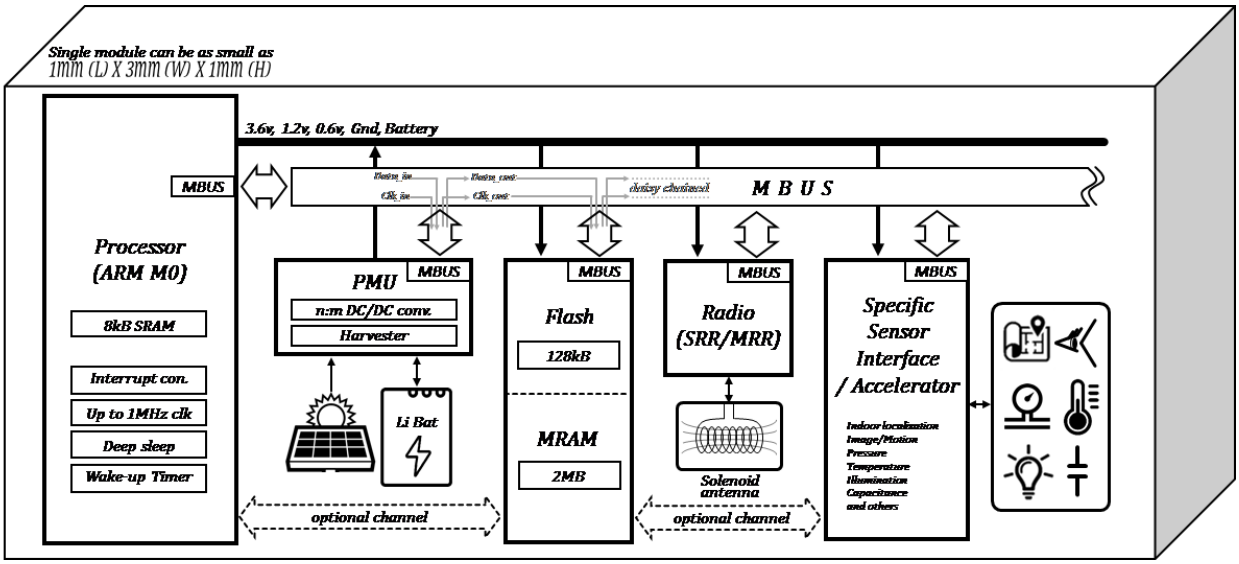


Figure 2. Example low-power IoT sensor node. The node compacts all of sensor, readout, intelligence, power management, and communication all into a small form-factor to allow for mass dissemination

Building slow-operating, low-performance circuits for this purpose may seem like an easy chore given today's capability. However, the limitations of the resources, e.g., battery power and fabrication cost, force circuit designers to consider unconventional trade-offs. Recent circuit developments for IoT devices have focused on making the systems that consume low enough levels of power such that operation can be sustained with the small footprint battery, sacrificing area and speed. The efforts have been successful in that the first wave of commercial circuits for IoT devices has been produced. But to make further improvements in this area, I predict (and assert) that we must focus on circuit techniques that maximize energy efficiency as well as the

efficiency of silicon area usage, a concept sometimes neglected. To date, only few circuit techniques have been discussed as ways to enhance these resource efficiencies.

To fulfill the dream of tens of billions of newly added IoT devices, the economics of deploying small, less powerful but ubiquitous sensors/computers must be grounded in reality to generate sufficient revenue. To trigger an exponential adaptation of such devices, the next milestone to be met is to develop IoT products at a cost that makes mass deployment possible. To achieve this goal, I believe increasing the area efficiency in circuit design will become increasingly important.

To better illuminate the importance of resource efficiency with a focus on design, let's consider the design of an ADC, one of the most representative building blocks in sensors and communication-intense circuits. During the past ten years, there has been a rise in the number of IoT-purposed low-power ADCs in academic domains, as shown in Figure 3 (red dots). The data is from a survey [1] of published ADCs at the International Solid-State Circuit Conference and VLSI Symposium from 1997 to 2017.

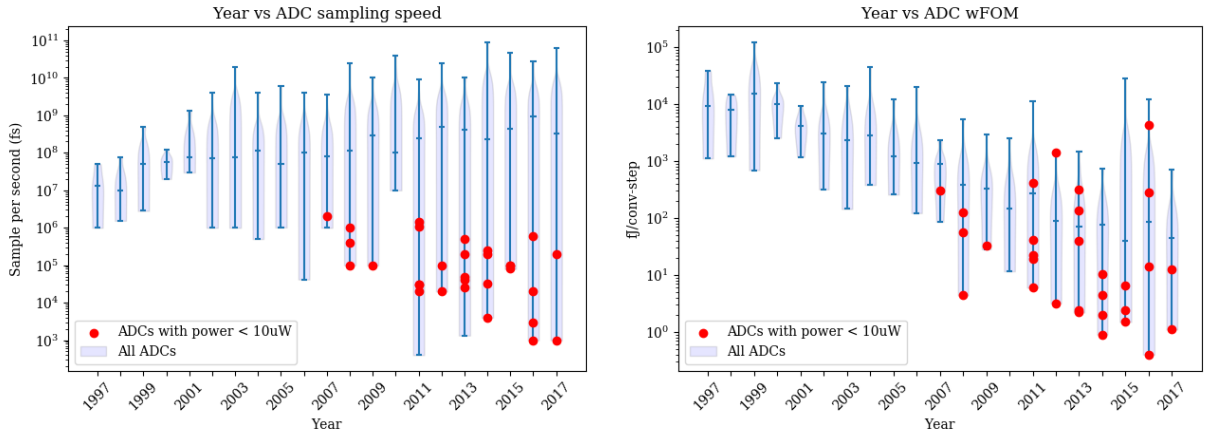


Figure 3. Trend of low-power ADCs in sampling speed and Walden's FOM

This trend began around 2007, with an increasing number of reports of designs constrained to consume less than ten micro-watts and to run at very low speeds (below or around 1 MS/s) [2][3][4][5][6][7][8]. Many of these designs were energy efficient, as indicated by their excellent Walden's FOM (wFOM), and indeed these ADCs set a new record wFOM almost every year.

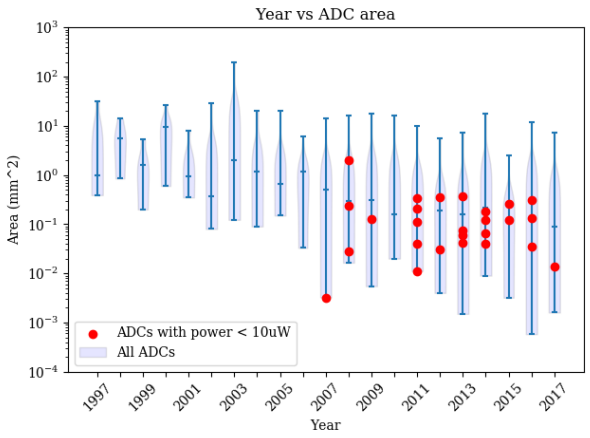


Figure 4. Trend of low-power ADCs in area

Although improving the energy efficiency is a significant accomplishment as far as the success of the IoT is concerned, the size of these ADCs did not decrease despite the sacrifice in speed, as shown in Figure 4. This means that less powerful low-power IoT circuits have become more energy-efficient in recent years but not cheaper, a quality that I believe is paramount to the mass marketing of such devices. Yet as a general consensus, for many analog/mixed-signal designs, the silicon area is deemed a parameter of a particular circuit, not a serious constraint or a measure of how successful the design is. This mindset is due to the fact that analog/mixed-signal designs are often considered already-small-enough peripherals alongside gigantic digital circuits that dominate the size, e.g., in CPUs and APs. It is natural to think in this situation that scaling of size is an issue for digital circuits rather than analog/mixed-signal circuits. Furthermore, there have not been many circuit techniques available to help reduce analog/mixed-signal circuit size.

For the IoT, however, as the core functionality has shifted from computation to sensor interface and communication, analog/mixed-signal circuits have become a more prominent component on the chip. Thus, the area occupied by analog/mixed-signal circuits should start to matter in this case.

Because previously the area of analog/mixed-signal circuits was of little concern, there has not been a good figure of merit by which to evaluate the area efficiency of an ADC design. Thus, I propose a new figure of merit, which I call the information-rate density (IRD) with physical meanings intended:

$$Information - rate\ density = \frac{conv-steps \cdot f_s}{Area} \qquad \textit{Equation 1}$$

As the process scaling is now truly coming to an end, the silicon area is becoming a more expensive resource. In future designs of ADCs, achieving the maximum conversion rate per a given area will become an important metric for the success of analog-intense circuit systems in terms of cost effectiveness. By using IRD, I aim to capture the future evolution in circuit design with a quantifiable metric related to area and speed that has a physical basis.

The IRD includes the sampling rate ($f_s=1/T_{conv}$) and the effective conversion step (conv-steps=2^{ENOB}) in the numerator and the area as the denominator. This equation describes the rate at which an ADC is capable of putting out total valid quantization, which I dubbed the 'information-rate,' given a certain area. For example, imagine two ADCs with the same performance and power but with different sizes (e.g., one is 10x larger than the other). Nowadays, given the success of interleaved ADCs [9][10][11][12][13], extra silicon area can almost readily be converted to higher speed by pursuing parallelism such that the larger design can be said to be ten times inferior to the smaller design. This concept is captured in the IRD since the design with the larger area will have

an IRD that is only one-tenth that of the smaller design. For the same end-functionality, a larger design wastes potential speed enhancement per area, leading to increased manufacturing cost.

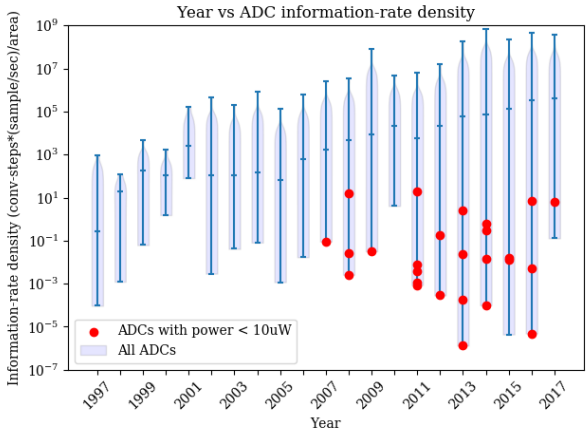


Figure 5. Trend of low-power ADCs in information-rate density

Indeed, as can be seen in Figure 5, the IRDs of low-power ADCs have been very poor. This observation is true because they essentially use the same circuit techniques as the other ADCs, but they apply aggressive voltage scaling to boost the energy efficiency. When voltage scaling is utilized as a method to trade off speed for energy efficiency, the linear change in voltage (and therefore energy efficiency) results in a quadratic or exponential reduction in speed. That is why their IRDs are so low. The dashed trend lines in Figure 6 illustrate that trade-off.

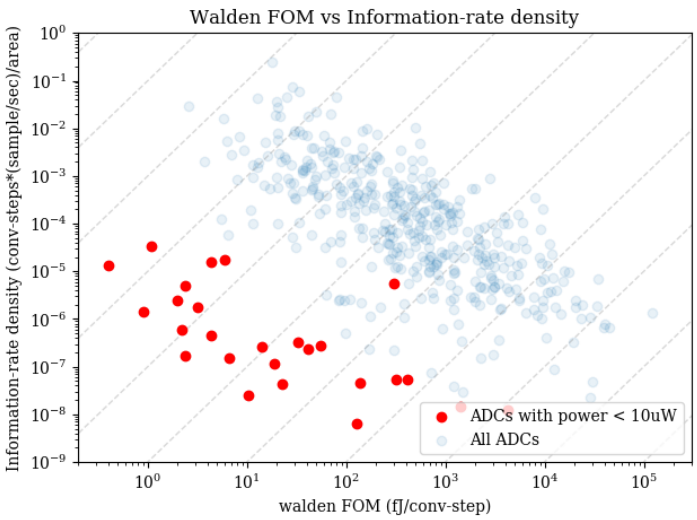


Figure 6. ADC evaluation plane of information-rate density and Walden's FOM. Upper left is towards ideal

As seen in Figure 6, the low-power ADCs follow a different trend than other ADCs: their wFOMs are state-of-the-art, but their IRDs are orders of magnitude lower than those of other ADCs. Process scaling has worked in favor of the trend that brought the normal ADCs to the upper-left corner of the plot, whereas a similar trend is observed in low-power ADCs but with a severe offset to the lower-left.

My goal in circuit design was to overcome this trend toward low IRD for low-power ADCs and increase their IRD to levels comparable to that of the other ADCs [14][15] in the upper-left region of the plot. At the same time, I sought to maximize the energy efficiency, so the overall design becomes resource efficient. With these goals in mind, I investigated charge-domain circuit techniques as a possible solution to the IoT problem, benchmarking their successes in high-speed serial links [16] and in high-speed ADCs [17].

Charge-domain circuit techniques are attractive due to their inherent focus on charge as an energy-centric mode of operation, which has the potential to achieve a level of energy efficiency that is higher than that obtained by using a conventional current or voltage mode of operation.

Also, this approach provides interesting features that cannot be achieved with a conventional domain of design.

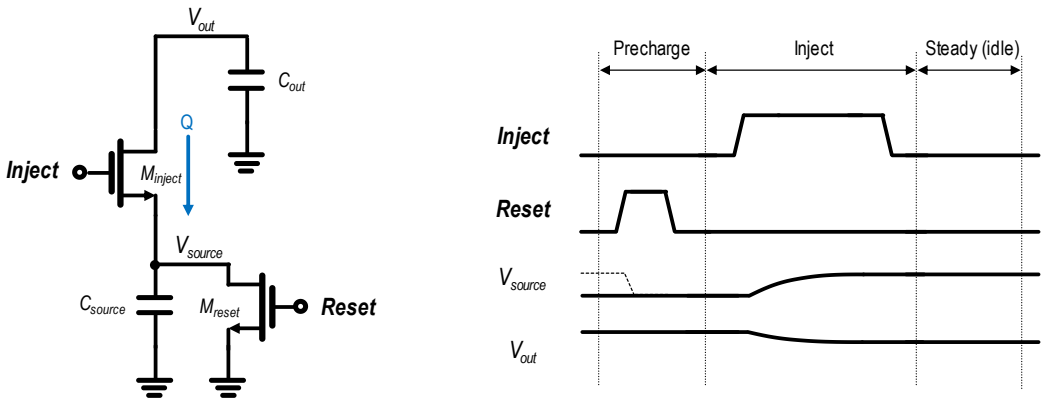
Throughout the next chapters, I introduce the charge-injection technique that was developed and analyzed in an effort to improve the energy efficiency and IRD of ADCs [14] and describe its unique properties (Chapter 2). Next, I explain its adaptation into an analog-circuit-intense low-power image sensor for IoT application with focus on improving the energy efficiency (Chapter 3) as well as a pre-amplifier for enhancing comparator performance while being energy efficient (Chapter 4). Then I conclude my dissertation (Chapter 5).

CHAPTER 2.

CHARGE-INJECTION TECHNIQUE

CHARGE-INJECTION CELL

I first introduced the charge-injection cell technique [14], to enable a charge-domain way of designing a digital-to-analog converters (DAC) and analog-to-digital converts (ADC). It is a circuit that can create fixed amount of charge (or voltage difference) per operation and the method's aim is to exploit dynamicity of charge-based circuits in the operation of DACs. The prevalent method of operating the DAC today is based on capacitor-array based structure which is far from being dynamic in operation. Although being robust, the simple way of its operation is hindering the design to go any further from what was originally described of its potential years before. With exploring dynamicity, charge-injection cell technique births many useful features in DACs and ADCs that other methods were not capable of.



(a) (b)

Figure 7. (a) the most basic charge-injection cell (b) operating waveform. For simplicity of understanding, drawing only shows pull-down version of the charge-injection cell.

Charge-injection cell, in its most strip-down form is shown in Figure 7. The purpose of the cell is to deliver the same amount of charge every time it runs, such that it can become a reliable charge/voltage reference generator. Toward this goal, the circuit is designed to conduct current on to the output capacitor in a controlled manner so that the amount of charge output is always kept at fixed value given that the execution is done the same way every time. The way that it works is similar to how dynamic logic circuits would work, having a discrete pre-charge state followed by an operating state to then a steady state, with a distinguishing difference being that this circuit is designed to achieve analog precision rather than to make a digital decision.

A single transfer of the charge-injection cell starts from resetting the bottom capacitor, C_{source}, to ground. During reset, transistor M_{inject} is put into turn-off state to shut-off any charge to conduct between V_{source} and V_{out}. Also, V_{out} on C_{out} is initialized to a reasonably high voltage to give headroom for transistor M_{inject}. The circuit then enters the injection phase. During injection phase, the Reset signal goes down to turn off M_{reset}, and the Inject signal transitions from zero (turn-off for M_{inject}) to a logic-high state. The logic high voltage needs to be precisely controlled to achieve analog precision of the overall operation. Now, the M_{inject} transistor enters saturation region of operation and start to conduct charge through V_{source} and V_{out}. The current quickly puts charge on to C_{source} which makes the voltage of V_{source} to rise, consequently pushes the M_{inject} transistor deep into sub-threshold region of operation. By this time, the current through M_{inject} decays exponentially to several decades smaller value so voltages on V_{source} and V_{out} are relatively slow-changing. The inject signal is then de-asserted at a deterministic time to end the injection state and then the circuit enters idle state waiting for the next transfer cycle to begin. The voltage change from start to end of this operation on V_{source} (and V_{out}) reflects how much charge has been

delivered to C_{out}, and is a quantity majorly decided by the interplay of logic high voltage on Inject signal, conductance of M_{inject}, C_{source} and the time given for the injection operation.

Considering that M_{inject} and C_{source} are circuit elements that are fixed at design time, the presence of time and voltage as a controlling factor for the charge-injection cell provides ex post facto way of tuning the amount of charge injection. Furthermore, the size of C_{out} determines the conversion gain at which the transferred charge translates to voltage, so the circuit reserves yet another axis of freedom to control its behavior.

Jitter Rejection Property

However, time becomes a weaker determinant as the circuit is left on for a long time which put M_{inject} into deep sub-threshold. This makes the charge flow into C_{out} diminish as the operation goes on. One interesting property of the charge-injection circuit is found here that the jitter on the clock that synthesizes the Inject signal will have correspondingly smaller impact over the circuit as turn-on duration extends longer. The amount of extra charge transferred due to the jitter-influenced timing of Inject signal is only proportional to the current that M_{inject} conducts at the end of transfer. Furthermore, the relevant jitter here is the period jitter that impacts the conduction of M_{inject} through varying the pulse width of Inject signal. Because period jitter is mostly a result of white noise sources in the clock generation circuit with no integration involved, overall magnitude of period jitter is relatively small compared to integral or absolute jitter. Overall, the circuit only puts out small extra amount noise charge.

The exponentially decaying profile of the transfer current, hence reduced sensitivity to jitter gives opportunity for the clock generation energy to scale down steeply as well. As the transfer operation is given longer time that its transfer current is diminished, the accuracy on the clock edge timing is much more relaxed, allowing the clock generation energy to scale down together. As a

general knowledge, an oscillator designed in above-threshold-voltage regime outputs jitter that is in square root relation to the period of the oscillator clock. This means that with slower clock, the circuit easily gains quadratic SNR improvement due to increasing ratio of oscillator frequency to jitter. Significant gain in overall system energy efficiency and jitter tolerance can be reaped by this mechanism. For applications absent of a clean powerful clocking source, slowing down the transfer operation is an effective and viable design choice that will lead to both improved jitter immunity and energy efficiency.

On the contrary, as the same logic projects that jitter tends to contribute more noise charge out of the charge-injection cell as it is run with a faster clock. Yet, it is still valid that an injection cell having a decaying transfer current profile would always outperform an injection cell having a flat-line profile. Also, since period jitter is usually a fraction of the integral jitter, e.g. $1/10^{th}$, a circuit element that is sensitive to integral jitter would most likely be the limiting factor of jitter related performance. As widely known, for systems such as ADCs that must accurately control sampling time instance, integral jitter plays bigger role in defining the performance limit than period jitter, therefore depending on the design target, the contribution of charge-injection cell noise from period jitter can be made inconsequential over other sources of noise.

Noise Characteristics from Reuse

One other powerful method to fight jitter is conjoined to the charge-injection cell's inherent reset which stems the concept of reusability in charge injection cell. In fact, this reusability is the heart of the charge-injection technique. After a transfer operation, the cell is put to a reset state preparing for the next transfer cycle while resetting the internal capacitor. This means that the cell is naturally designed to be reused to transfer another instance of charge to an output capacitor to create bigger voltage change. If multiple charge-injections activations of a single cell are spread

over time rather than being concentrated to a single activation, the design can benefit from noise averaging as each instances of period jitter will be uncorrelated. In fact, this operation allows all independent high-bandwidth sources of noise, including period jitter and thermal noise, to have an impact diminished by square-root-of-N, whereas N is the number of total injections. So, the designer can incorporate this aspect of the circuit into the design to combat jitter and even other white noise sources. Also, because creating a bigger voltage swing on the output only necessitates multiple charge-injection cell activations not specific to how many cells are implemented in the design, re-use feature of the charge-injection cell can also be used towards reducing the physical size of the system.

Resetting and re-using the charge injection cell is also beneficial in reducing the impact of flicker noise. In creation of a certain reference voltage through using a continuous time circuit, the flicker noise modulates the conduction of the device and appears on the output. Flicker noise is tricky to get rid of for it changes very slowly thus cannot be low-pass filtered. However, it could be high-pass filtered. It has been well understood through studies on RTS noise behavior in cyclo-stationary current sources [18] and dynamic comparators that when the device is repeatedly turned on/off in their operation, the traps states in/under the gate oxide, which is the source of RTS noise, are brute-forcedly reset. The point of turning the device repeatedly on/off is to not allow the device to cumulate the trap states that they end up entirely randomly occupied/emptied over time, greatly deviating from the ideal value.

When the circuit is reset, it reduces channel carrier concentration under the oxide so that the traps also tend to empty out. When it turns back on, only the traps that are within a certain energy level are able to react quick enough to probabilistically capture a carrier before the next turn-off happens. Only those traps contribute noise which is a significant reduction from original

status without cycled reset. The trapping and de-trapping of oxide traps in CMOS is governed by a Poisson process that has mean-time to capture/emit as modeled by the following equations (NMOS case) [19].

$$\tau_c = \frac{1}{\sigma_n \cdot V_{th} \cdot n} \qquad \textit{Equation 2}$$

$$\tau_e = \frac{exp[\frac{E_F - E_T}{kT}]}{\sigma_n \cdot V_{th} \cdot n} \qquad \textit{Equation 3}$$

The equations suggest that since mean-time to emit could become very short when the device is off ($E_F << E_T$) that it indeed is resetting the trap states in the oxide. Eliminating cumulation of trapped states with using this reset, the resultant noise does not show up as 1/f noise but rather a modulated tone in a higher frequency coupled to the periodicity of the reset. Or a flat-then-rolloff profile, effectively showing the high-pass filtration of the operation. Applying the idea to the charge-injection cell, as the cell is being reset per every transfer and each transfer only takes place during finite time duration, the contribution of flicker turns into an uncorrelated noise that is much suppressed from its original amount.

Noise Sources and Analysis

Then what about thermal noise? There are several sources of thermal noise that can affect the amount of output charge. The contribution of the noise sources can be written as follows.

$$Q_{n,out}{}^2 = Q_{n,reset}{}^2 + Q_{n,inject}{}^2 + Q_{n,channel}{}^2 + Q_{n,gate,S}{}^2 + Q_{n,gate,D}{}^2 + Q_{n,other}{}^2 \qquad \textit{Equation 4}$$

Q_n denotes the noise charge. Mostly they are the kTC charge noise from the reset operation through M_{reset} on C_{source}, the thermal noise contribution from conduction of M_{inject} that defines the

final voltage of V_{source} at the end of the transfer, the random amount of channel charge injected out of the drain of M_{inject} at the time it is turning off, and the thermal fluctuation of the signal at the gate coupled to V_{source} then therefore modulating the current output of M_{inject}. Some of these elements are a straight forward in their analysis, but some of them are non-linear and time-variant. To study the contribution of these noise sources to acquire intuition for design, some simplifications were committed.

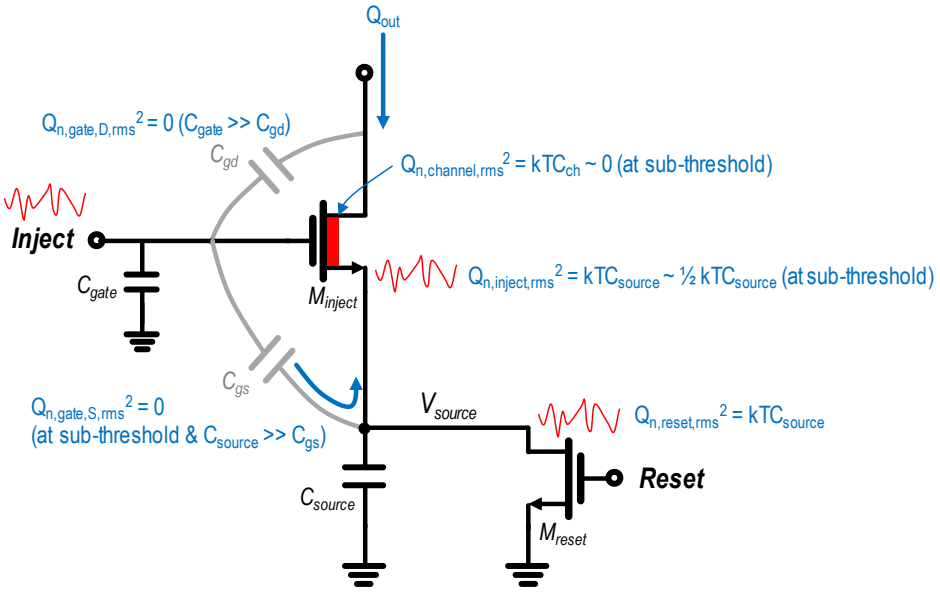


Figure 8. Thermal noise sources in charge-injection cell

The output charge of charge-injection cell is (ideally) exactly the amount of charge C_{source} has gained. In simplistic point, what defines Q_{out} is the initial and the final voltage on C_{source} and the capacitance value as formulated in below equation.

$$Q_{out}(t) = C_{source} \cdot \left(V_{source}(t) - V_{source}(0^{-})\right) \qquad \textit{Equation 5}$$

In Q_{out}, the two terms that contribute noise are simply $V_{source}(0^{-})$ and $V_{source}(t)$. The two terms are dominantly affected by the thermal noise from M_{reset} during reset and the thermal noise

of M_{inject} during injection. The thermal noise of M_{reset} can be easily analyzed that $Q_{n,reset}^2 = kTC_{source}$ assuming no other capacitance are seen at V_{source} node. But trickily, $V_{source}(0^-)$ and $V_{source}(t)$ become uncorrelated during the transfer process if t is sufficiently long that the latter term does not duplicate the contents of the first term.

The process of transferring charge in the charge-injection cell is in fact very similar to the process of soft-reset commonly found in image sensor literatures. The technique is usually applied to a 3T APS structure that must control its reset noise to achieve higher performance. Relying on these prior studies [20], a mechanism of how $V_{source}(t)$ and $V_{source}(0^-)$ loses correlation in progression of time is illuminated and also the final form of the noise contribution is found. Applying the analysis to the charge-injection cell, assuming the transfer has already taken place long-enough at $t=0^-$ to drive M_{inject} into sub-threshold region and considering shot-noise, following can be formulated.

$$< V_{source}(t)^2 > = \frac{mkT}{2C_{source}} \cdot \left(1 - \frac{1}{\left(1+\frac{qI_{inject}(0)t}{mkTC_{source}}\right)^2} \right) + < V_{source}(0^-)^2 > \cdot \frac{1}{\left(1+\frac{qI_{inject}(0)t}{mkTC_{source}}\right)^2} \qquad \textit{Equation 6}$$

As t approaches infinity, the form is further simplified to the following, whereas $m = 1 + C_{dep}/C_{ox}$ of a MOSFET that is slightly higher than 1 and I_{DC} is the current at which M_{inject} started conducting.

$$< V_{source}(t)^2 > = \frac{mkT}{2C_{source}} \cdot \left(1 - \left(\frac{mkTC_{source}}{qI_{inject}(0)t}\right)^2 \right) + < V_{source}(0^-)^2 > \cdot \left(\frac{mkTC_{source}}{qI_{inject}(0)t}\right)^2 \qquad \textit{Equation 7}$$

As $<V_{source}(t)^2>$ term includes $<V_{source}(0)^2>$ as initial condition, the multiplied term diminishes to zero as t approaches infinity. The final form is shown below.

$$\lim_{t\to\infty} c(t) = \lim_{t\to\infty} \left(\frac{mkTC_{source}}{qI_{inject}(0)t}\right)^2 = 0 \qquad \textit{Equation 8}$$

$$< V_{source}(\infty)^2 > = \frac{mkT}{2C_{source}} \qquad \textit{Equation 9}$$

I call C(t) as a compression term which stems out because of the decay of current through M_{inject} as V_{source} rises in time. Intuitive way of understanding the compression term is to picture two charge-injection cells with slightly different start voltage of V_{source} during charge-injection. Cell that has a higher starting voltage on V_{source}, because the V_{GS} across M_{inject} would be smaller, will conduct less current. The ratio of the reduced current to the normal case is more drastic if the current conduction become a stronger function of V_{GS}, as in sub-threshold CMOS device or BJT. Under steep (exponential) decay of current through M_{inject} with reducing V_{GS} for the case of charge-injection cell, therefore, the voltages that started out higher and conduct smaller current gets caught up by the normal case. After sufficient time, the voltage difference of the two cases at V_{source} become very close and compressed. The compression term C(t), as a function of time, indicates how much this compression progressed.

Above equations outlines the behavior of noise during sub-threshold part of the operation. It suggests that whatever small-signal noise is on V_{source} at $t=0^-$, the eventual noise on V_{source} after a sufficiently long time will become half of the kT/C noise on C_{source}. It agrees with the common sense that when one strips out one degree of freedom in conduction direction to which the electrons can flow in 1-D resistor, the noise contribution is effectively halved. This phenomenon is known to be present in devices with diffusion-based conduction where a potential barrier is present that can blockade certain direction of conduction, i.e. diode or bipolar devices or sub-threshold CMOS.

The noise behavior in above-threshold is dictated by the drift behavior of channel carriers which is only weakly associated with potential barrier that it does not limit the degree of freedom in electron conduction. What this means is that during the transfer of charge in charge-injection cell in above-threshold regime, $<V_{source}(t)^2>$ will exhibit the whole of kT/C noise power. And as the device enters sub-threshold region, this noise amount will become subject to compression then therefore decays to zero whereas a new half kT/C through sub-threshold operation will take over as time progresses.

Without compression, meaning if the current source is used in place of charge-injection cell, the noise charge contribution should be square-root proportional to the total transferred amount of charge which is the characteristics of shot noise. In this case, the noise can infinitely grow as one increases the amount of charge being injected out. However, the charge-injection cell operation is capable of outputting noise charge far less than current source limited by shot-noise. What compression does, in this sense, is that it is providing a strong negative feedback mechanism that factors down the shot-noise process to a thermal limit. If by chance a shot-noise was present in M_{inject} conducting more charge, the conduction immediately feeds back to V_{source} and raises the voltage. This in turn causes exponentially less current flow of M_{inject} to enact compression, and hence the cell operation is regulated by constructing a strong negative feedback. As a result, the shot-noise contribution does not integrate on C_{out} to an infinite value, but it is suppressed to a kTC_{source} noise by the work of this feedback on V_{source} with C_{source}.

The phenomenon can readily be observed through simulation using transient-noise analysis with Berkeley Design Automation (now Mentor). In simulation, a test circuit comprised of arbitrarily sized M_{inject} plus 300 fF for C_{out} and 11 fF for C_{source} is run for 100 iterations with ideal voltage sources for control. The result confirms with our projection of noise power that the

variance of the charge output from the charge-injection cell is at $2 \cdot kTC_{source}$ (kTC_{source} from reset + kTC_{source} from M_{inject} in above-threshold) and as time progresses, it asymptotically approaches $1.5 \cdot kTC_{source}$ (kTC_{source} still from reset + $0.5 \cdot kTC_{source}$ from M_{inject} in sub-threshold) as the conduction device is put into deeper into sub-threshold. The required time from the state to transition from $2 \cdot kTC_{source}$ noise state to $1.5 \cdot kTC_{source}$ noise state is related to the rate-of-decay of the compression term. This implies that if the circuit has smaller C_{source} and the initial current flowing through M_{inject} is larger, the transition point will come earlier, leading to the conclusion that having larger M_{inject} and smaller C_{source} is beneficial in quickly bringing the noise down to $1.5 \cdot kTC_{source}$. However, there are other aspects to the selection of those sizes which makes the design become subject to trade-off.

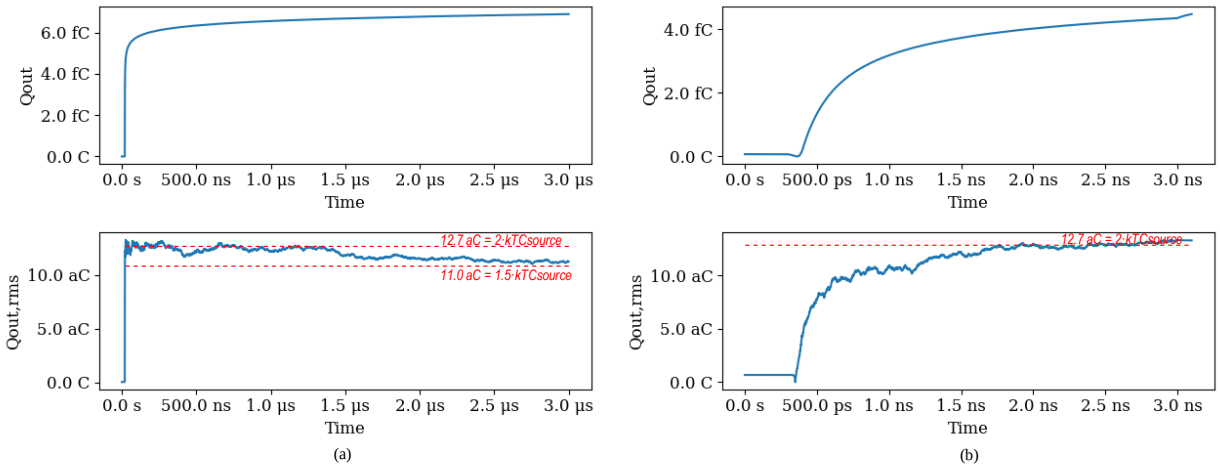


Figure 9. Signal charge and noise charge comparison in simulation. (a)[upper] Time versus charge output [lower] Time versus standard deviation of charge output (from 100 noise seed iterations) (b) zoom in on the time scale of (a)

Assuming C_{source} output fixed amount of charge mapped to a constant voltage difference from $V_{source}(0-)$ and $V_{source}(final)$, denoted V_{delta}, the SNR of a fast single transfer event can be written as follows.

$$SNR_{fast\ single\ transfer} = \frac{V_{delta} \cdot C_{source}}{\sqrt{2kTC_{source}}} = V_{delta} \cdot \sqrt{\frac{C_{source}}{2kT}} \qquad \textit{Equation 10}$$

As V_{delta} (approximately V_{DD}-V_{th} = ~hundreds of mV) is typically significantly larger than thermal noise (~1mV) on a small (~10fF) capacitor, the SNR of a single transfer is in the range of 50~60dB. Now comparing the result to a static current source,

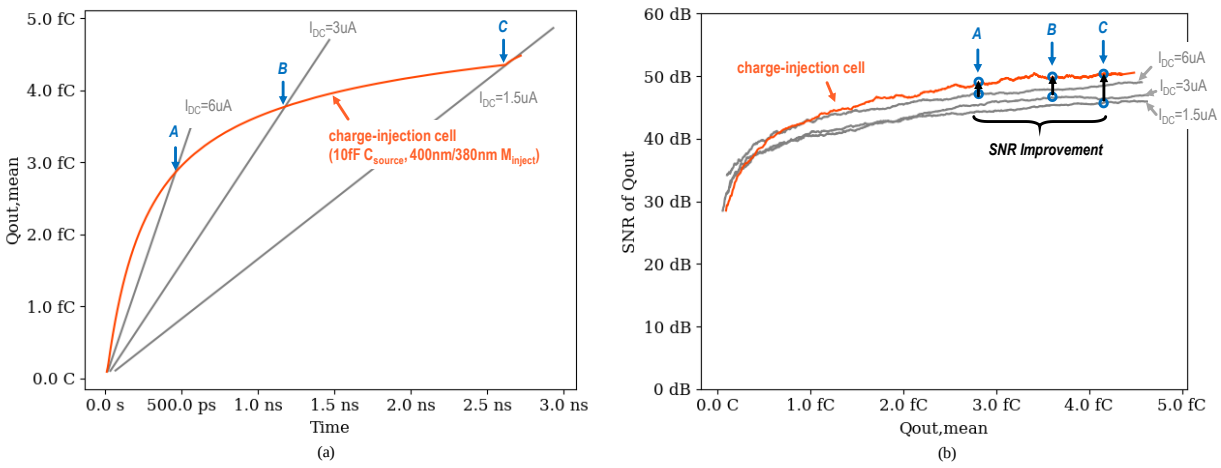


Figure 10. (a) charge transfer characteristics (Q_{out} vs time) of charge-injection cell compared to simple current sources with different DC currents (1.5uA,3uA,6uA) (b) The SNR of charge transfer and current sources at different Q_{out} value

The charge-injection cell can be used multiple times (=N) to acquire higher signal output, so the SNR can be easily improved by factor of square-root of N. And to improve SNR even further, enlarging C_{source} will make the circuit more accurate by the square root of its size increase. If the design requirement requires better noise performance yet the voltage range is flexible, one can leverage the fact that the noise is determined by C_{source} but V_{delta} has room to grow to improve the SNR. But if a higher voltage is not readily available, one can apply a voltage extension (boost) technique through modulating the bottom node of C_{source} as shown in Figure 11. By using the technique, the signal output of the charge-injection can be at least doubled with the noise charge maintained at similar level. Combined, the overall achievable SNR of the inject operation can be

formulated as follows, where N is the number of transfer operation and k_{boost} is the gain factor from the boost technique.

$$SNR_{multiple\ transfer\ with\ boost} = k_{boost} \cdot V_{delta} \cdot \sqrt{\frac{N \cdot C_{source}}{2kT}} \qquad \textit{Equation 11}$$

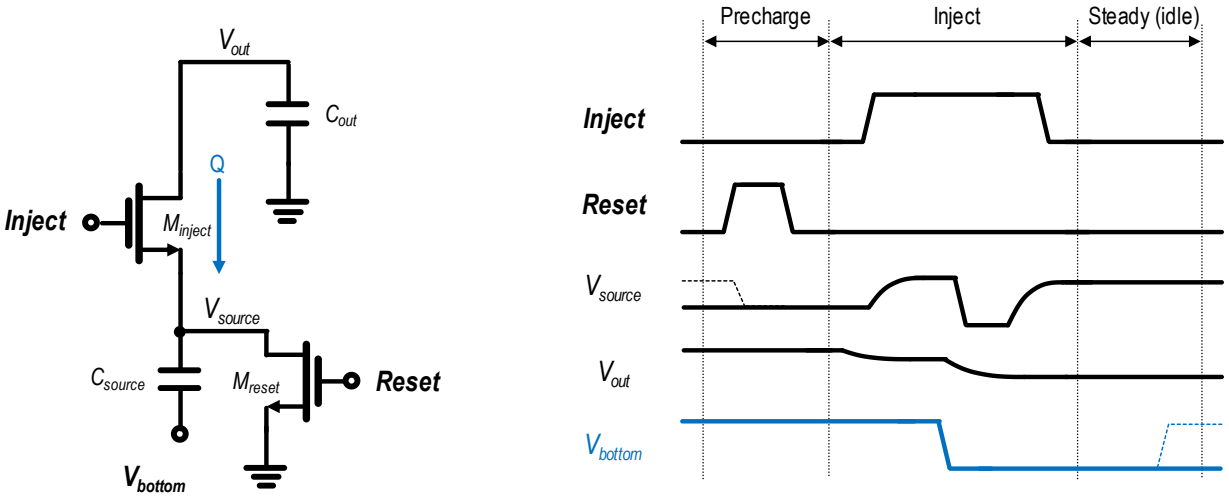


Figure 11. (a) Modified charge-injection cell with bottom of C_{source} controlled by signal, V_{bottom}. (b)Operation timing of the modified cell. The V_{delta} can significantly be increased.

A small drawback of the boost technique is that now the system could see yet another thermal noise source at V_{bottom}, where a transistor must be present for selectively passing logic-high and logic-low level. This noise will modulate the conduction of M_{inject} resulting in noise charge, however, as the current through M_{inject} diminishes as it enters sub-threshold, the magnitude of modulation becomes extremely small to inflict only minuscule noise charge.

This filtering process is what diminishes other contributors of noise in $Q_{n,out}$ and is worth taking a closer look. Assuming an inverter is driving the V_{bottom} node and the parasitic capacitance is in the order of fF, the bandwidth of the thermal noise given at V_{bottom} should be in the order of

GHz. Yet the network conformed by M_{inject} and C_{source}, because M_{inject} is to enter sub-threshold after sufficient time, has the bandwidth in the lower MHz range (or even lower in deep sub-threshold). This means the fast-changing noise coupling into V_{source} is rejected out by the speed of M_{inject}, hence does not result noise charge.

A similar mechanism holds for thermal noise that enters V_{source} through C_{gs} of M_{inject}. The Inject signal is also driven by an inverter, therefore is not free of thermal noise fluctuation. When that fluctuation gets coupled into V_{source}, a similar filtering as above takes place to mitigate the impact. The size of the cap, C_{gs}, can also be controlled to be a small quantity compared to C_{source} to reduce the effect. It may be important to size M_{inject} with smallest possible width to suppress this noise along with meeting other specifications, i.e. output impedance or leakage.

One other source of noise, which is the randomness of channel charge that gets injected out of M_{inject} to C_{out}. Because our assumption of the charge-injection operation is that V_{out} is maintained sufficiently high to sustain M_{inject} in saturation. What this implies is that the electrons that form the channel of M_{inject} is entirely attracted to V_{out} because of its high potential, that all electrons flow out to the drain direction. The question then is how much noise charge was originally stored at the channel by kTC, instead of by what unknown (noisy) ratio will channel electrons split into either the source and the drain. The noise charge stored at the channel is simply kTC_{gate}, assuming the device is in strong inversion that the channel charge constitutes mostly of minority carriers at the channel and not the space charge in the depletion region.

If the charge-injection operation is halted while M_{inject} is in above-threshold and in saturation, the noise charge amount of kTC_{gate} will appear at C_{out}. However, if the operation has taken place for long time that M_{inject} is in sub-threshold region, the impact reduces greatly. In sub-threshold region, the charge stored at C_{gate} is mostly comprised of the space charge in the depletion

layer beneath the oxide layer. The space charge, during turning-off of the device, attracts majority carrier to neutralize itself from mostly the body terminal of the device and neither from the source or the drain. This means that the charge flow in turning-off a sub-threshold region operating device is nearly zero when seen from source/drain. Almost no noise charge will be output to C_{out} when M_{inject} is in sub-threshold for this reason.

Lastly, the C_{gd} of M_{inject} provides a coupling path between V_{out} and the Inject signal, passing the thermal noise on the Inject through to V_{out}. The noise transfer characteristic will be all-pass, however, the division factor of this noise can be designed to be quite high (e.g. with C_{gd} ~ few fF and C_{out} ~few hundred fF) that its overall effect is negligible.

Mismatch and Calibration

As discussed to this point, operating the charge-injection cell for long enough time for M_{inject} to reach sub-threshold region of operation helps reject unwanted involvement of several noise sources in the design. The same holds to fend off the impact of mismatch as well.

The main source of mismatch in charge-injection cell is the M_{inject} transistor. Two factors involved as sources of mismatch in M_{inject} transistor are; 1) variations that can impact the final value of the V_{source}, that is the V_{th} variation of the device, and 2) variations that impact the course of V_{source} transition, that is the mobility variation of the device. Typically, people simplify the variation model of a MOSFET as being entirely flattened to the V_{th} change, however, for our use case as in charge-injection cell, the aspect of mobility should be separated to study the operation more accurately.

As discussed in the previous section, the charge that is injected out is determined by V_{delta}. The path difference during the large-signal transition on V_{source} is compressed to a small value if the charge-injection cell is operated for sufficiently long time. What this means is that the mobility

variation of the MOSFET is compressed out of the picture whereas only the V_{th} variation remains as the most significant variation source that impacts the charge injected out of the cell.

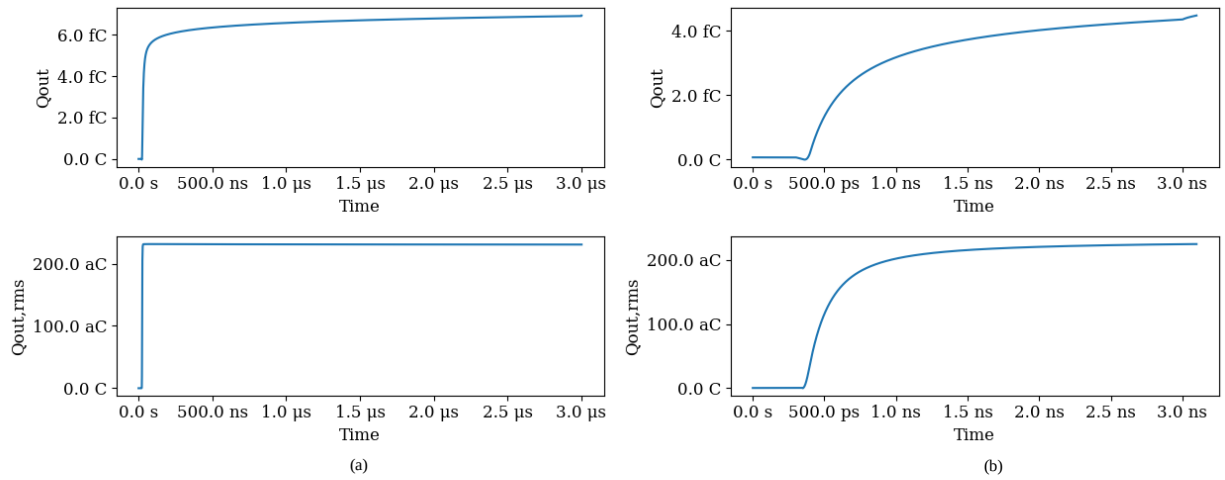


Figure 12. Mismatch on $Q_{out,}$ simulation comparison. (a)[upper] Time versus charge output [lower] Time versus standard deviation of charge output (from 100 monte-carlo iterations) (b) zoom in on the time scale of (a)

Although the same charge-injection cell can be reused multiple times with perfect matching between each inject operations, the absolute size of the charge injection is subject to process variation. This variation can be as high as few $\%_{rms}$ of the typical amount of charge transferred, therefore it calls for calibration if it were to be used for high-precision systems. The ratio of the variation can greatly differ by different selection of V_{delta} and also the $\Delta V_{th,rms}$ of M_{inject}, but a representative number for V_{delta} is ~600 mV (V_{DD}-V_{th}) whereas $\Delta V_{th,rms}$ ~30mV (for 400nm/380nm, thick oxide device) which results in 5 $\%_{rms}$ variation in injected charge amount..

Each of the determining factors of the charge-injection cell can be trimmed to yield calibrated charge output, however in terms of feasibility and efficiency, only two methods are favorable.

First method is to change the logic-high voltage of the Inject signal to a specific analog value so to control the V_{source}(final). Because M_{inject} device's threshold voltage is the most

dominant factor that alters the charge-injection amount, this method is the most straight forward and effective way to cancel out the global process and temperature variations of the threshold voltage. Also, it is relatively easy to build a replica circuit to acquire an analog voltage that tracks the process and temperature change of V_{th}. However, the method typically necessitates a voltage buffer to apply the tracked logic-high level into the charge-injection cells, so it is less disturbed with injection operation. In many cases, the design cost of having it can outweigh the benefit. And designing it to a very fine resolution quickly grows the noise/power budget of the buffer and the replica.

The second method is to apply a tunable capacitor-array at the place of C_{out}. C_{out} is assumed to be a high-density on-chip lumped capacitor so partially converting it into a monotonic capacitor-array (also not strongly constrained by matching) only incurs slight overhead to the overall size. With using capacitance to trim the different gain of the charge-injection cell, fine resolution of calibration can be reached. For example, if original C_{out} is around ~300 fF, a multitude of small capacitance of ~300 aF (varactor scheme preferred) can be added to enable 10b-equivalent calibration capability. To cover the local variation of a single charge-injection cell, the full depth of calibration needs to cover ±3~6σ, which is typically around ±10~20 % of normal charge transfer amount.

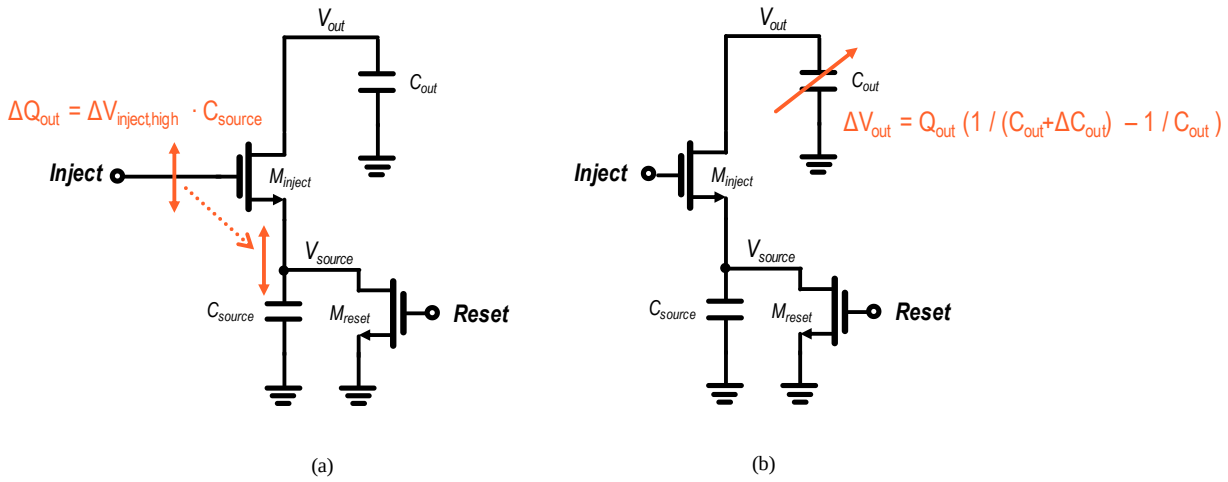


Figure 13. (a) calibration through modifying $V_{inject,high}$ (b) calibration through modifying C_{out}

Output Impedance and Cascoded Charge-Injection Cell

One final characteristics of concern is the consistency against varying V_{out}. If the charge-injection cell outputs vastly different amount of charge for different V_{out}, it is not usable as a reliable reference voltage. Assuming the gate voltage of M_{inject} can be precisely controlled, one can devise a direct comparison between charge-injection cell and a simple static current source to highlight the difference between their consistency performance.

For this simulation experiment, same size transistors were given, which is 400 nm width and 380 nm of length. Each are operating as a charge-injection cell and a static current source for fixed duration of time (3 ns) to output charge to their respective V_{out} node. With sweeping V_{out}'s initial potential where the operation starts from, I measured how much charge has been output during the operation time. The gate voltage of the current source is fixed to an arbitrary value that yielded similar amount of charge as the charge-injection cell. The result is shown in Figure 14.

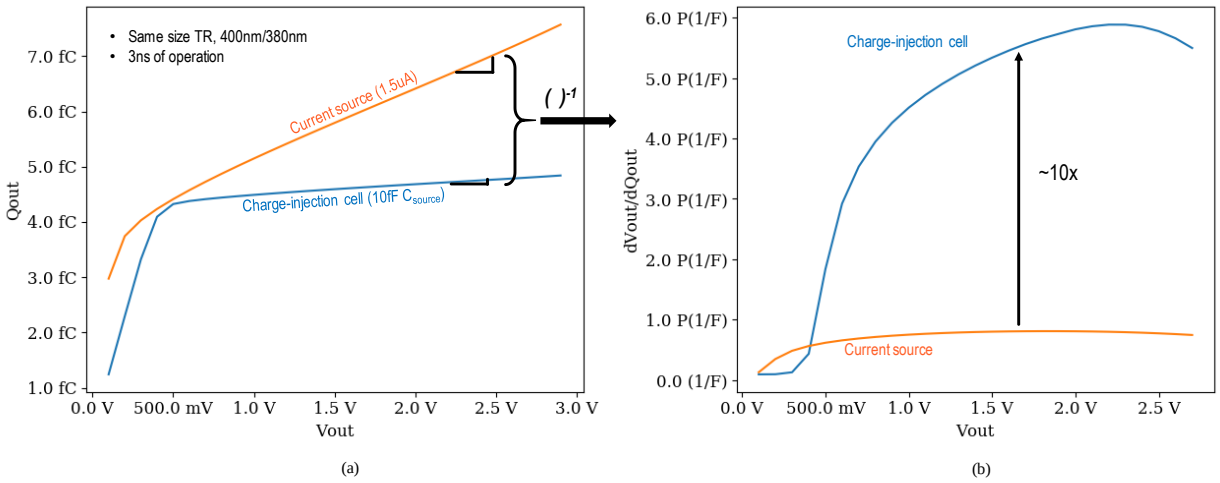


Figure 14. Comparison of static-current source and charge injection cell with same-sized transistor device. (a) Comparison of Q_{out} by sweeping V_{out} for static current source and charge-injection cell (b) charge-domain equivalent of output impedance mapped to different V_{out}

From the figure, it is evident that both circuits exhibit a saturation behavior. That is, past a certain voltage in V_{out}, the amount of charge that is being output goes into a region where it stays relatively flat. However, a distinction should be made between the two circuits in respect to how well the circuits conform to saturation. By reading the numbers, the charge-injection cell outperforms a simple current source easily by 10 times with respect to equivalent output impedance.

The reason for such improvement on the charge-injection cell is again related to the negative feedback on V_{source} node that helps regulate the current output. The mechanism of "having more current through M_{inject} that leads to faster voltage rise on V_{source}, and then feeding the voltage back that produces much lesser current through M_{inject}" plays significant factor in regulating the output charge. Starting from having different current through M_{inject} at the beginning of the operation due to different V_{out}, negative feedback quickly compresses the current through M_{inject} to a significantly smaller variance. So, what really modulates the Q_{out} is the integral of the difference in current through M_{inject} over time that it took until the negative feedback compress the

current to a negligible variance. This identifies the source of the variance that limit the output impedance of the cell as the above-threshold part of the operation. Also what needs a second mention is that once the compression has taken place, meaning the M_{inject} is in sub-threshold region of operation, the output current through M_{inject} experiences drastically improved output impedance. So, beyond this point, M_{inject} does not get influenced much with what voltage is set for V_{out} as can be interpreted from Figure 15.

In contrast, a static current source has limitation of having low output impedance at above-threshold region of operation. The trade-off for using it in sub-threshold is that the current output is strongly affected by mismatch. However, charge-injection cell traverse from above-threshold (high-speed) to sub-threshold region (high-accuracy) of operation, and benefits from both worlds to output consistent charge while being fast.

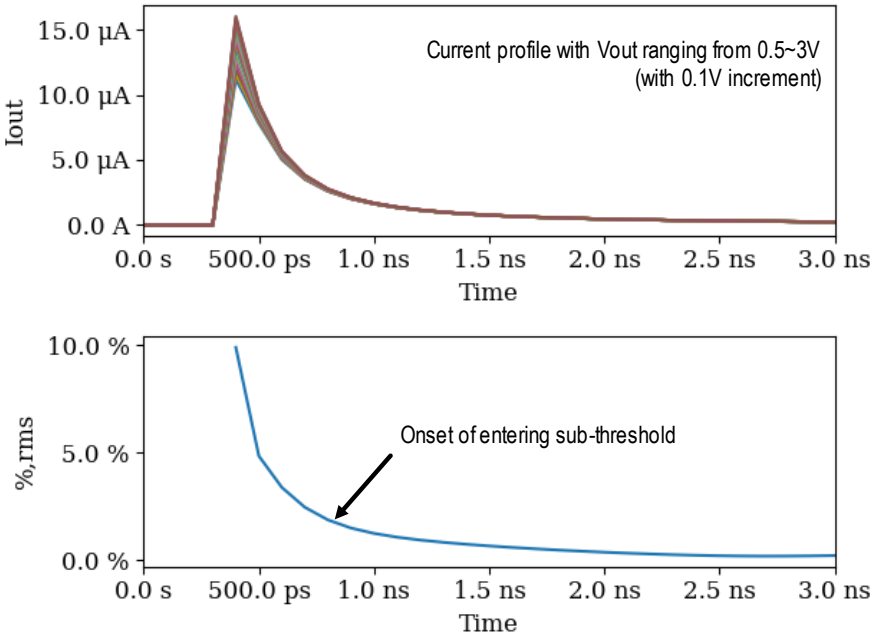


Figure 15. Variation in current due to different V_{out} diminishes as the device is operated for a longer time. (top) output current through M_{inject} over time with different V_{out} (0.5~3V) represented as different traces (bottom) standard deviation of output currents at each time point normalized to their means

Expanding from this fact, it could be derived that the more the charge-injection cell operates in sub-threshold region, the more accurate it will become. By operating the charge-injection cell longer, an improved charge-domain equivalent output impedance could be acquired. This is backed by simulation result in Figure 16.

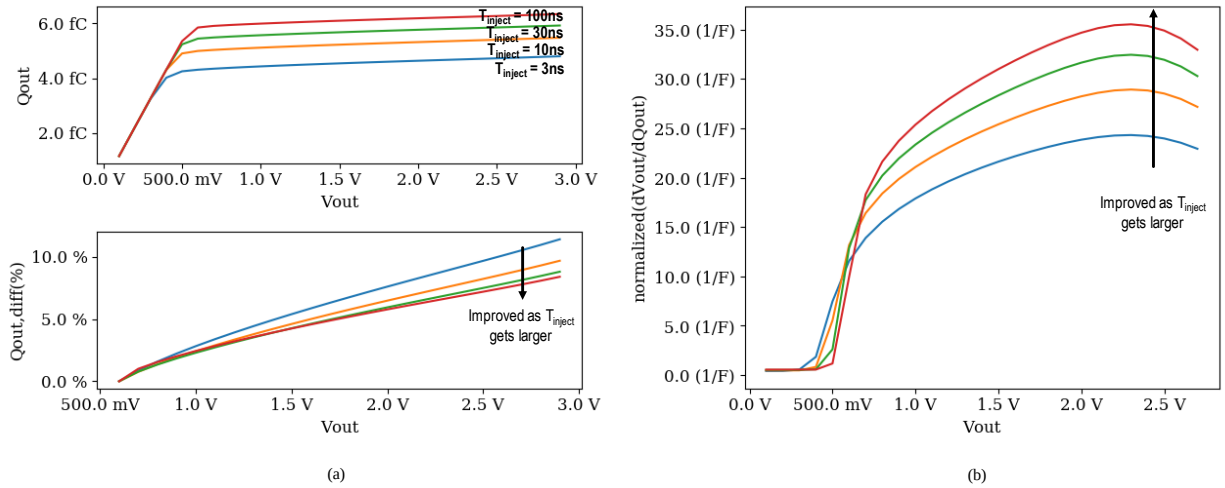


Figure 16. T_{inject} effect on the consistency of the charge-injection cell (a, upper) Q_{out} vs. V_{out} (a, lower) difference in Q_{out} with sweeping V_{out}, normalized to its own Q_{out} at V_{out}=500mV (b) Calculated charge-domain equivalent of output impedance, normalized to its own Q_{out} at V_{out}=500mV

As another significant factor affecting the consistency, the rate of feedback (or compression) is reliant on the size of C_{source} by which constructs the feedback gain for the behavior. With smaller C_{source}, the sensitivity on V_{source} increases with respect to current therefore the charge-injection cell achieves compressed state much faster with smaller C_{source}. For running the charge-injection cell for a fixed time, the consistency of the charge-injection cell improves with smaller smaller C_{source}. This is because the cell spends more time in compressed state where V_{out} is not in effect. The effect can be observed through simulation result captured in the following figure.

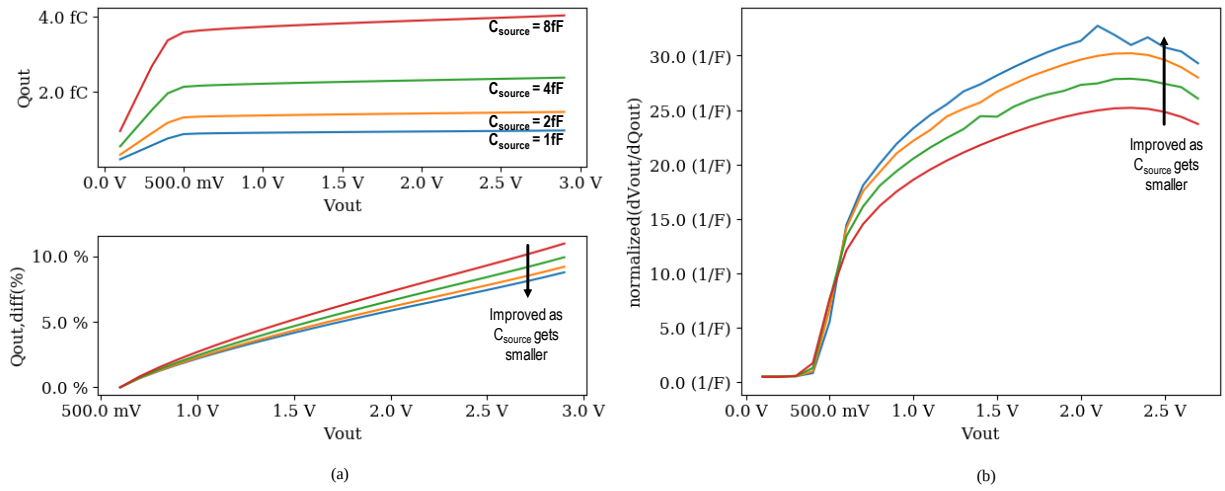


Figure 17. C_{source}'s size effect on the consistency of the charge-injection cell (a, upper) Q_{out} vs. V_{out} (a, lower) difference in Q_{out} with sweeping V_{out}, normalized to its own Q_{out} at V_{out}=500mV (b) Calculated charge-domain equivalent of output impedance, normalized to its own Q_{out} at V_{out}=500mV

The initial variation in the output current, as can be seen in Figure 15, is due to the lack of output impedance of M_{inject} in above-threshold region of operation. Since this variation is the main constriction in improving the consistency of the charge-injection cell, it is important to address it to achieve higher accuracy. To our advantage, the output impedance of M_{inject} transistor in above-threshold region, which is the cause of this variance, will respond to conventional design methods. Typically, increasing the length of the device will be the first choice in improving the output impedance, however, it comes with the disadvantage of slowing down the transfer operation that will make the time for it to enter the compressed-current state to be elongated. What this entails is that the amount of improvement could be diminished or even worsened if the operation time is constrained to be very short. In deep-submicron domain of design, increasing the length to be somewhat longer than minimum feature size may be more effective even accounting what has been lost due to slower speed, but the gain could diminish past a certain length. As seen in Figure 18, the consistency improves drastically as one increases the length of M_{inject} to be longer than the minimum length, however, the gain diminishes at the length of 4~8 um that their $\%_{rms}$ deviation

of Q_{out} is almost at par to each other. Also, if the energy to operate the charge-injection cell is taken into the account, the cost of increasing the length become even more prohibitive.

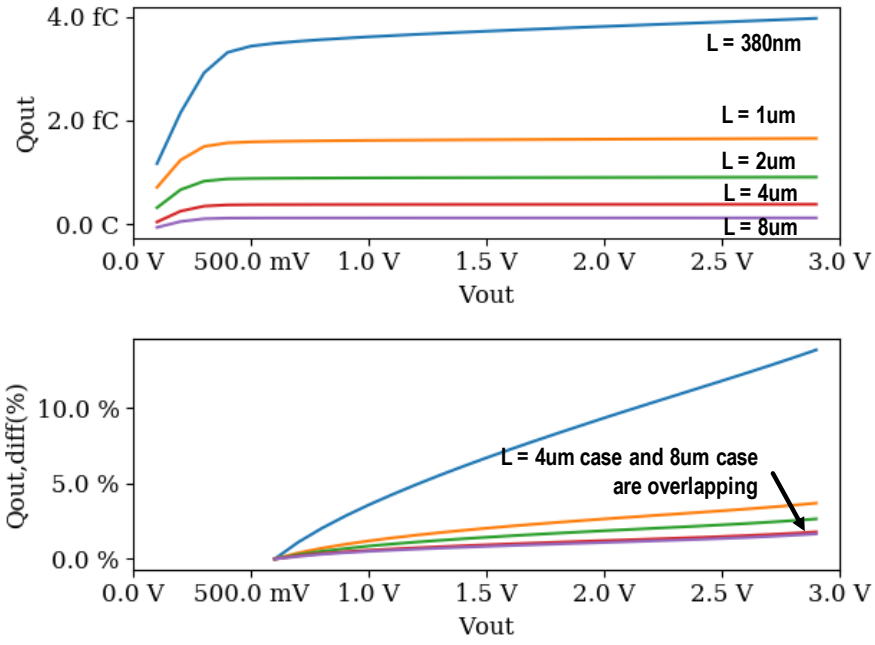


Figure 18. Length effect on the consistency of the charge-injection cell (upper) Q_{out} vs. V_{out} (lower) difference in Q_{out} with sweeping V_{out}, normalized to its own Q_{out} at V_{out}=500mV

A second conventional approach useful for improving the consistency of the charge-injection cell is to apply a cascode transistor to M_{inject}. Cascoding effectively shields the M_{inject} transistor from V_{out} while it is working in the above-threshold region. The outcome is that the output current of M_{inject} become much more stable with regards to varying V_{out}. However, the benefit for having a cascode, overall, is not as drastic as in static current sources. The introduction of parasitic node, $V_{cascode}$, results in some loss from expected improvement (by $g_m r_o$) of cascoding.

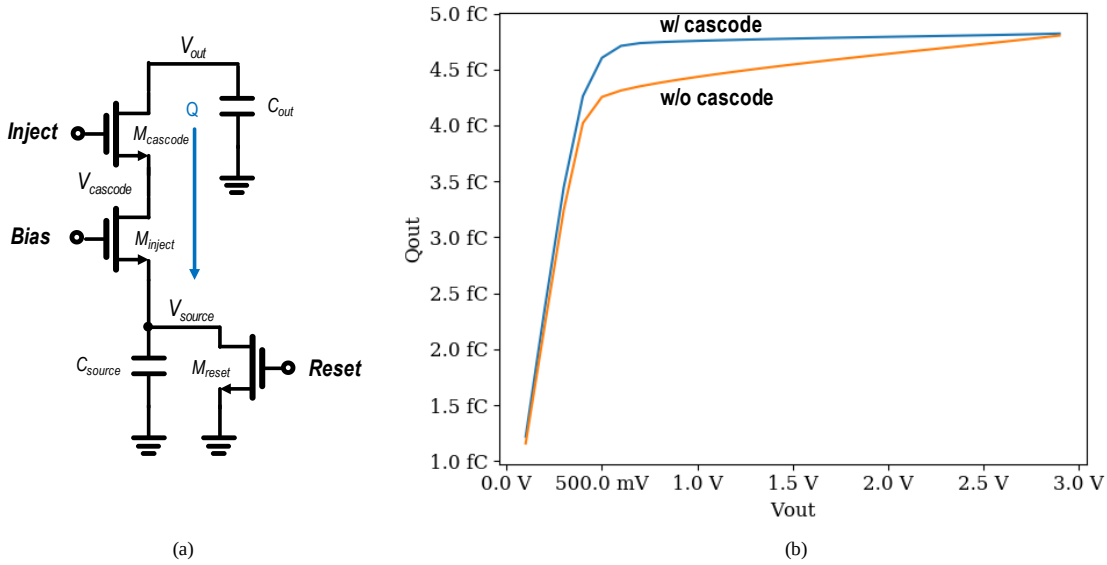


Figure 19. (a) Charge-injection cell with cascode transistor (b) comparison of consistency with and without cascode device from Q_{out} vs V_{out}.

The degradation is in two-folds. First, in the compressed-current state of operation, what dictates the output charge is the M_{inject} transistor. But the drain voltage that it sees is now a more volatile $V_{cascode}$ (capacitance should be minimized to benefit from cascoding) not the more stable V_{out} (large capacitance). Because $M_{cascode}$ transistor, although it is also in sub-threshold, is injecting charge out to V_{out}, the voltage on $V_{cascode}$ changes more so than V_{out}. This affects M_{inject} in that it sees larger deviation at its drain than in non-cascoding case, so it results in more variation of output current when the cell is in compressed-current state (Figure 20, lower right, tail of the graph). But since the impact of variation in the compressed-current state is already very small compared to above-threshold region operation that this effect does not overtake the benefit of cascoding entirely.

The second is that, because $V_{cascode}$ has to start from the reset voltage and then rise to sufficiently high level to put M_{inject} into saturation, the cell has a duration of time where it makes M_{inject} operate in linear region. In linear region, the output impedance is greatly reduced that the output current become more subjective to V_{out} difference. The result is that the suppression of

current variation does not measure up to the ideal cascode gain, however, the overall suppression is still more than non-cascoding case (Figure 16, lower right, head of the graph). With these short comings, having the cascode transistor still is able to provide ~7x resiliency against V_{out} from the non-cascoding case.

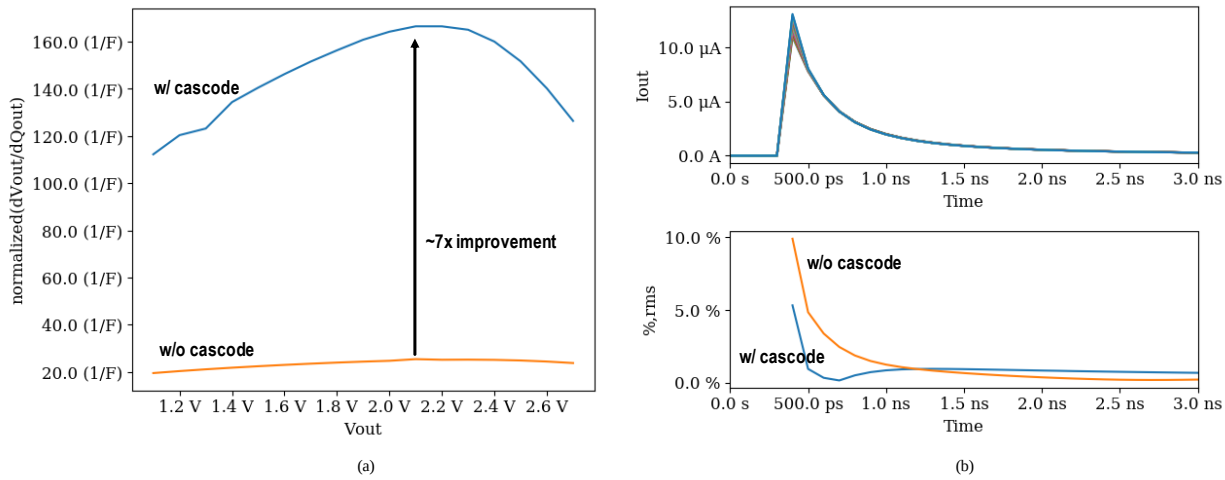


Figure 20. Comparison of cascoding and non-cascoding charge-injection cells (a) charge-domain equivalent output impedance (b) output current profile in span of time

In this sub-chapter, I have studied the concept and the characteristics of the charge-injection cell in terms of jitter rejection, noise, mismatch and output impedance. The improvement stemming from its dynamic operation, traversing from above-threshold to sub-threshold, compared to a static current source has been discussed. In the next sub-chapter, I will look into how this charge-injection cells can be integrated together to form a digital-to-analog converter (DAC) and then to be incorporated into a SAR ADC while providing unique benefit over the conventional capacitor-based DACs and SAR ADCs.

CHARGE-INJECTION DAC AND SAR ADC

The most prevalent structure for synthesizing a reference voltage of our time for data-converter purpose is the capacitor-array and many techniques were investigated to expand its capacity [21][22][23][24]. Through using a capacitor as both the source of charge and the converter of charge to voltage, the capacitor-array structure has successfully delivered feasible solutions to many circuit applications honing its simplicity and robustness. However, there are applications where capacitor-array structures have not been so well-performing, e.g. image sensors, for many reasons including their prohibitive area penalty for increased bit depth and costly inclusion of well-matched capacitors to the process. The base of the capacitor-array structure that births these difficulties, in my observation, is that they resort to an integral and inseparable method of controlling the flow of charge and converting it into voltage.

This inseparable mapping of sourcing charge and converting to voltage in capacitor-arrays, impose limitations in exploiting trade-off. It leads to a case where to optimize one aspect of the circuit, e.g. bit-depth, speed; the other aspects must settle with suboptimal, e.g. area, noise. However, with charge-injection cell technique, creation of charge and its conversion into voltage are an explicitly separated process controlled by distinctly separated elements so the design is more flexible therefore become extricated from this entanglement. However, it does not mean that the charge-injection cell designs are free from trade-off itself, but it means that it certainly provides merits to the designers with more degrees of freedom to utilize. The outcome is that designers can explore fundamentally different trade-offs to create novel and useful features for applications where half-century old capacitor-array DAC structure have not been a good fit.

Throughout this sub-chapter, I draw comparison between capacitor-array structure and charge-injection cell structure of their merits as a DAC (or SAR ADC incorporating it) to better

differentiate what the charge-injection cell structure can achieve. To begin the comparison, the most basic structure for both are shown in the following figure.

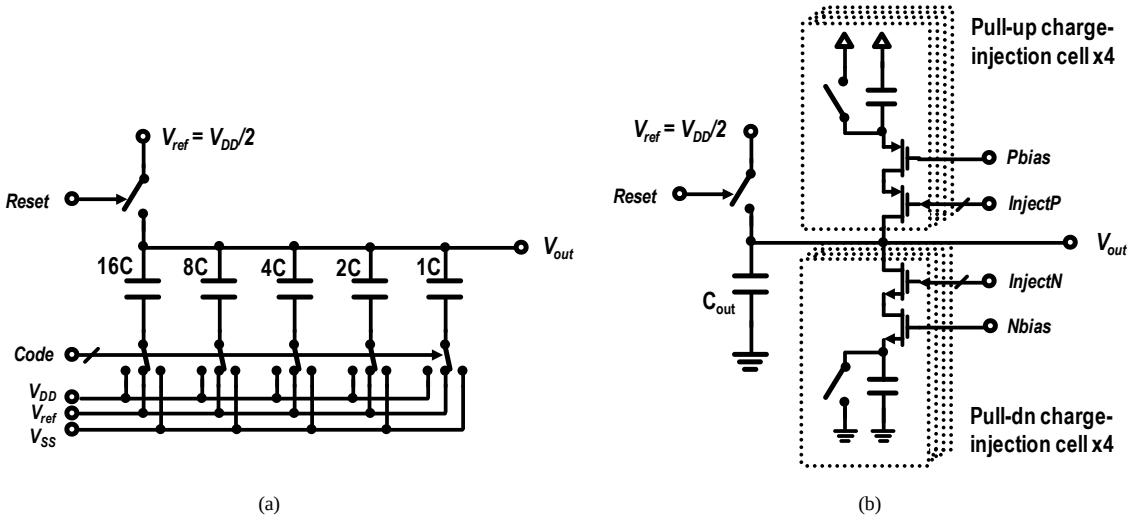


Figure 21. Simplest 5b DAC of
(a) capacitor-array structure (b) charge-injection cell structure

Figure 21 shows two 5-bit DAC example comprised in capacitor-array style and charge-injection style. Both structures have a signal range that is centered at half-V_{DD} and cover either up or down. If the reference voltage is perfect, the capacitors in capacitor-array are much closer at being an ideal charge source than charge-injection cells. It is inherently immune to clock jitter and also has no dependence on V_{out}. It also does not accumulate noise on to the output capacitor like charge-injection cells. Though it may be puzzling, the charge-injection cells are indeed inferior to simple capacitors in these aspects. However, there are ways to leverage unique features of charge-injection cells to break equal or even to outperform capacitor-array structures.

One of the most useful difference of charge-injection structure is that all charge-injection elements can be re-used. It means that for designing a DAC for a given bit depth, the number of elements required can be chosen arbitrarily small in charge-injection cell structure. It is unlike the capacitor-array where the number of unit elements incorporated has to match with the number of

quantization steps. The principle reason why capacitor-array must be designed in such a way is that it cannot decouple the source of charge to the destination where it converts to voltage. Once a capacitor is used to output certain amount of charge, the state of which that capacitor is in also changes due to the operation, e.g., the voltage at the bottom of the capacitor as drawn in Figure 21 (a). There exists no way that one can revert this voltage back to the original state without rolling back the output voltage to the prior state also. This inseparable coupling of charge sourcing and charge-to-voltage conversion renders the structure not suitable to be re-used to produce the same amount of charge output repeatedly.

However, charge-injection cell is devised to decouple charge-sourcing operation to voltage-generation. The cell can reset after its operation that its state return to the condition as before the operation while its output is isolated. This is the key differentiator in enabling the re-use in charge-injection cell structure. The output voltage accumulates change; however, it is necessary to design it to sustain many number of repeated operation without impacting the repeatability of the charge-injection cell operation.

Improvement in Information-Rate Density (IRD)

With leveraging the re-use feature, charge-injection cell structure has the benefit of occupying smaller space on silicon. The cost of it is that the operation of unit charge-injection cells need to spread out over in time, taking a penalty on speed. Although the maximum operable speed of a single charge-injection DAC is reduced from adopting re-use, one should account for the overall benefit of having smaller area that can be leveraged to exploit higher degree of parallelism, to fairly evaluate its usefulness.

Typically, SAR ADCs that uses these DACs resort to interleaving, a type of parallelism, to achieve very high-speed overall A/D conversion. When parallelism is utilized, it prompts

application space where a charge-injection cell structure could be more benefiting than capacitor-array structure. To emphasize this aspect, I resort to information-rate density analysis using model simulation.

The simulation experiment is conducted to apply this figure-of-merit (IRD) to study the differences between capacitor-array based structure and the charge-injection structure. Based on a model of the two structures, the experiment yields the result illustrated in Figure 22 through Figure 24. To derive the model, following factors are considered.

- Assumed for both structures that the DAC size is decided by mismatch limit
- Each comparator time increases by 10% from original per bit increase for both
- Comparator and logic size increases 20% per bit increase for both
- [Cap DAC] To increase one bit of resolution with same INL performance, the size of unit capacitor is increased to twice the original size
- [Cap DAC] DAC settling time, in capacitor-array structure, increases 10% per bit increase
- [Ci DAC] To increase one bit of resolution, the size is double for ci cell when cell count increases by 2x
- [Ci DAC] Injection takes 10% longer time due to RC delay per doubling number of ci cells
- [Ci DAC] C_{out} area for charge-injection cell structure doubles per bit increase

The mark up factors (penalty on area and speed per resolution increase) are decided by matching the result to the author's 6b ADC (charge-injection structure) in [1] and other high-speed ADCs (capacitor-array structure), then extrapolating to other cases to the best discretion of the author. The details of the modeling are shown below. (n is the bit-depth of an ADC, and 2^p [$=N_{inj}$] is the number of charge-injection cells in the ADC. N_{trans} is the total number of toggles on the Inject signal to meet given resolution.) Although the absolute values from the modeling may not capture the reality in absolute scale, but it offers intuition into how the two structures differ in

relative scale. Note that ci cell is assumed to be far larger than the unit capacitor size for capacitor-array.

$$Area_{cap-array}(n) = 2^{n-1} \cdot {K_{a_{cap}}}^{n} \cdot a_{cap,0} + {K_{a_{dec}}}^{n} \cdot a_{dec,0} \qquad \textit{Equation 12}$$

$$T_{conv,cap-array}(n) = (n-1) \cdot {K_{t_{cap}}}^{n} \cdot t_{cap} + n \cdot {K_{t_{dec}}}^{n} \cdot t_{dec} \qquad \textit{Equation 13}$$

$$Area_{inj}(n,p) = 2^{p} \cdot {K_{a_{inj}}}^{p} \cdot a_{inj,0} + {K_{a_{cout}}}^{n} \cdot a_{cout,0} + {K_{a_{dec}}}^{n} \cdot a_{dec,0} \qquad \textit{Equation 14}$$

$$T_{conv,inj}(n,p) = \sum_{i=0}^{n-2} \begin{cases} 1 & if\ 2^{i} < 2^{p} \\ 2^{i-p} & if\ 2^{i} \geq 2^{p} \end{cases} \cdot {K_{t_{inj}}}^{p} \cdot t_{inj} + n \cdot {K_{t_{dec}}}^{n} \cdot t_{dec} \qquad \textit{Equation 15}$$

$$N_{inj} = 2^{p},\ N_{trans} = \sum_{i=0}^{n-2} \begin{cases} 1 & if\ 2^{i} < 2^{p} \\ 2^{i-p} & if\ 2^{i} \geq 2^{p} \end{cases} \qquad \textit{Equation 16}$$

Table 1. Selection of mark-up factors used for modeling charge-injection cell-based ADC against capacitor array-based ADC

$K_{a,cap}$	$K_{a,inj}$	$K_{a,cout}$	$K_{a,dec}$	$K_{t,cap}$	$K_{t,inj}$	$K_{t,dec}$
2.0	2	2.0	1.2	1.1	1.1	1.1
$a_{cap,0}$	$a_{inj,0}$	$a_{cout,0}$	$a_{dec,0}$	t_{cap}	t_{inj}	t_{dec}
0.08	0.5	1.0	10.0	1.0	0.5	1.0

Figure 22 illustrates the resulting information-rate density comparison of the two structures. It shows that for above 6b, there exists a re-use scheme where the charge-injection cell structure wins over the capacitor-array structure in terms of information-rate density. Also, for each of the lines representing different bit-depth, there is an optimum on the number of charge-injection cells to incorporate in the ADC. The convex shape of each trace in Figure 22 (a) is a result of interplay of two factors. The tendency of increase in the left side of the curves is due to the exponential increase in total number of inject activity required to create the right number of

quantization steps. The exponential increase in activity renders the speed of the overall conversion to be very slow if re-use is brought to the extreme. Also, the tendency of decrease at the right side of the curves is due to exponential increase in N_{inj} that comes to occupy significant area in the converter. As both conversion time and area of the converter are at the denominator of information-rate density, having either of them grow can significantly weaken the figure of merit. Yet leveraging re-use in charge-injection structure to the right amount, opens up opportunity to find a balance between the two to give an optimal information-rate density.

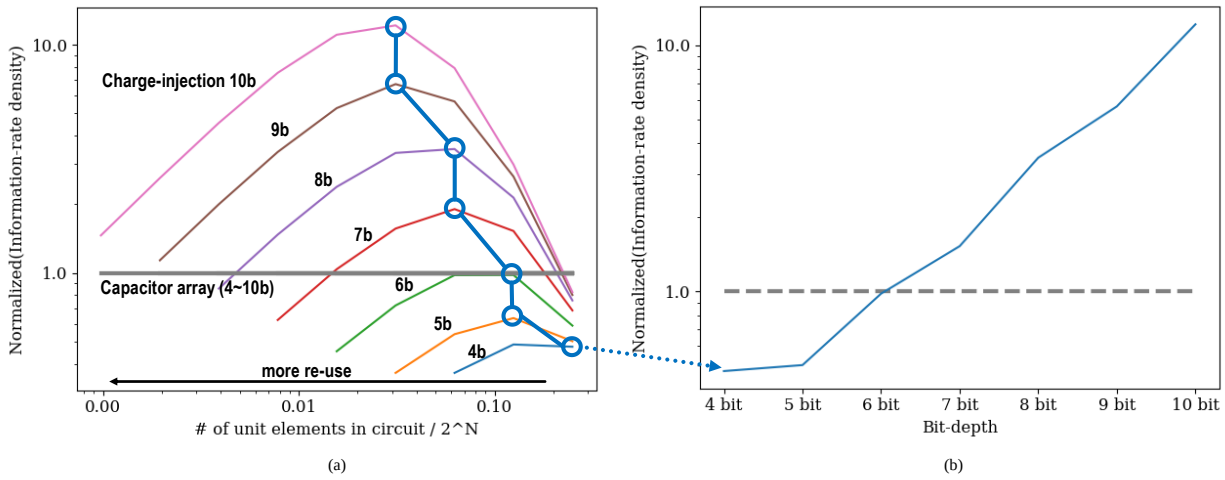


Figure 22. (a) Information rate density (normalized to capacitor-array structure) vs. number of unit charge-injection cells incorporated in the ADC (normalized to total number of conversion step) (b) (near-)optimum information rate density at different bit-depth

From Figure 22 (b), I also find that the optimal information-rate density has the tendency to increase along with the bit-depth. This positive relationship, between bit-depth and the optimal information-rate density, is due to the fact that the number of transfer operations in charge-injection structure do not initially grow exponentially with using re-use, whereas the size of the array reduces exponentially with re-use (Figure 23). In high resolution case, like 10b, re-use can easily half the overall ADC area since the DAC elements are the most area consuming part in the ADC. The efficacy is further fortified by the fact that the N_{trans}, which is the main constraint on

speed, hover at more-or-less the same value. It is because the overhead for re-use that halves the overall size is only a single extra toggle on the Inject signal. However, in lower resolution than 6b, the reduction of size does not come as drastically as high-resolution cases because the area is dominated by other parts than the DAC elements. And also, the size of the ci cell ($\boldsymbol{a_{inj,0}}$) is originally larger than the capacitor unit cell ($\boldsymbol{a_{cap,0}}$) that if unless sufficient degree of re-use is utilized, the overall size of the ADC will turn out larger for charge-injection cell structure, making its information-rate density poorer.

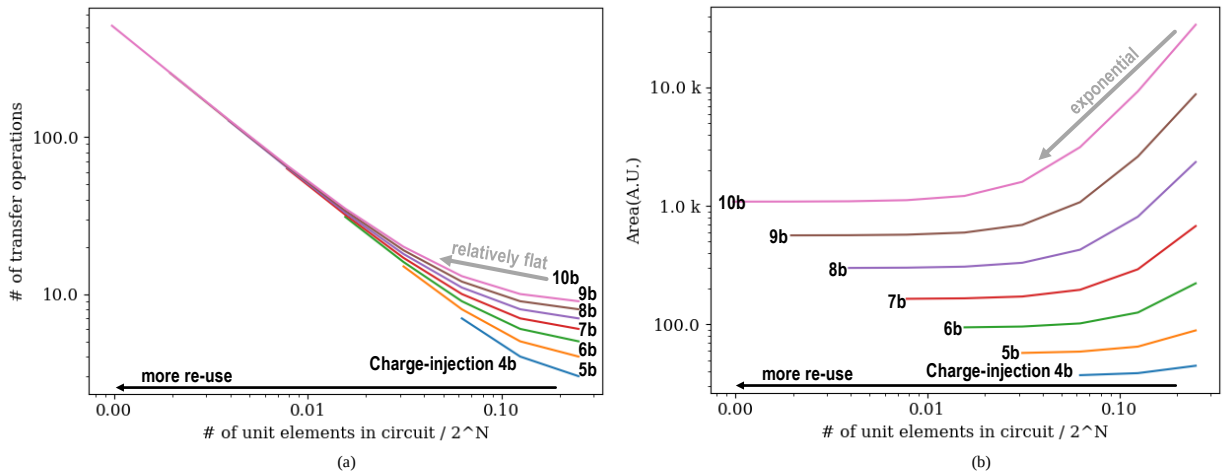


Figure 23. N_{trans} and area from charge-injection structure vs. degree of re-use at different bit-depths

To agree with what has been estimated, Figure 24 shows that the optimum information-rate density per different bit resolution in charge-injection structure is indeed more strongly affected by the reduction of area rather than speed. As bit-depth increases, the area of the charge-injection structure and the capacitor-array structure split up to more than an order-of-magnitude difference in the figure, whereas the difference in conversion time remain small. From this study, I can conclude that moving to charge-injection structure is better than capacitor-array structure in achieving higher area-efficiency thus is more advantageous in acquiring higher speed per valuable

silicon area. As the trend in semiconductor is now progressing towards an era without process scaling, this method could contribute an economic way of designing analog-intense IC products.

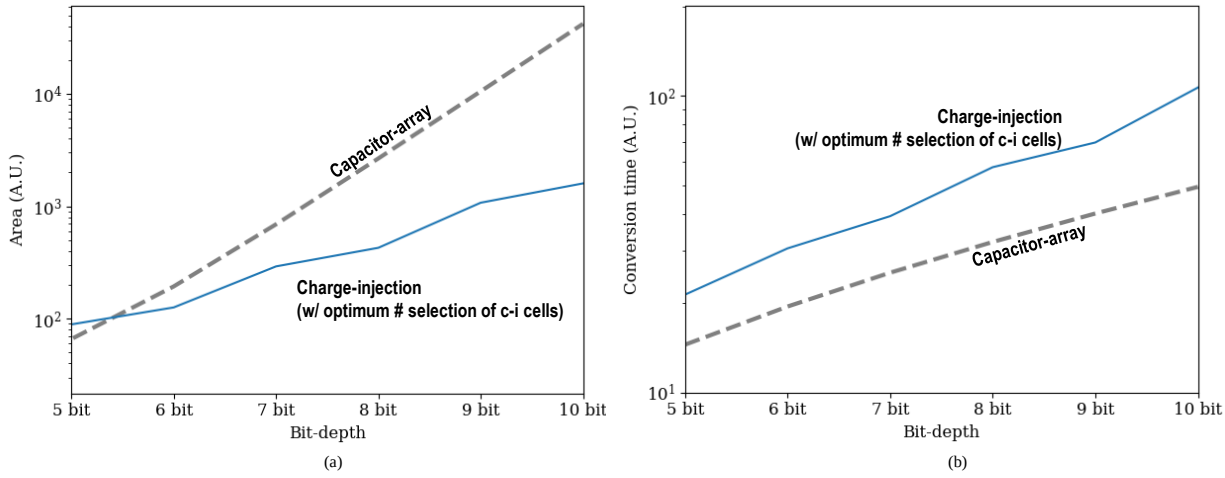


Figure 24. Charge-injectionl and capacitor-array structure comparison. (a) area vs. bit-depth and (b) conversion time vs bit-depth. Area is the dominant factor that drives excellent information-rate density in charge-injection structure

Improvement in Linearity

Until here, I have shown the economic side (area cost) of the charge-injection cell-based DACs. Yet charge-injection cell-based DACs have another benefit in fighting against device mismatch that leads to improving INL and DNL performance.

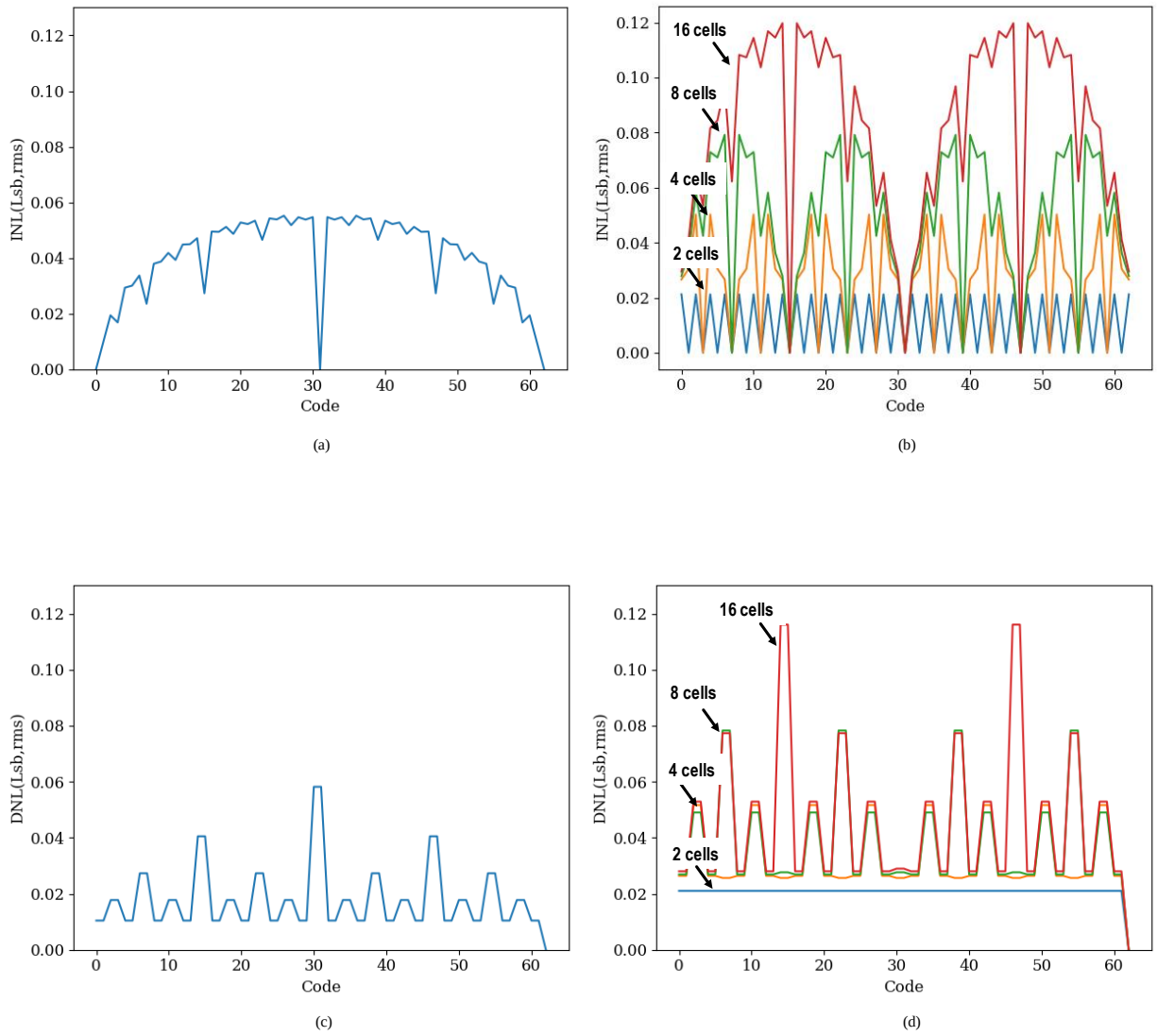


Figure 25. (a) INL of capacitor-array structure (b) INL of charge-injection structure with different degree of re-use (c) DNL of capacitor-array structure (d) DNL of charge-injection structure with different degree of re-use
For comparison, rms mismatch of unitcell in capacitor-array is assumed to be 1% of its nominal value and for charge-injection cell, 3% is assumed

As can be seen in Figure 25, with assuming certain mismatch for the unit cells of both the capacitor-array structure and the charge-injection structure, there exists a level of re-use that results in equivalent (or even better) INL and DNL performance. Note that the charge-injection cell has more per cell mismatch than unit capacitor in capacitor-array based structure. One important disclaimer here is that without calibrating the charge-injection structure, it may suffer from varying

DAC range chip-to-chip. But assuming perfect calibration, there is a definite improvement over capacitor-array structure that the amount of maximum mismatch cumulation is reduced with more re-use. At high bit-depths, a higher degree of re-use could be selected to effectively suppress INL/DNL.

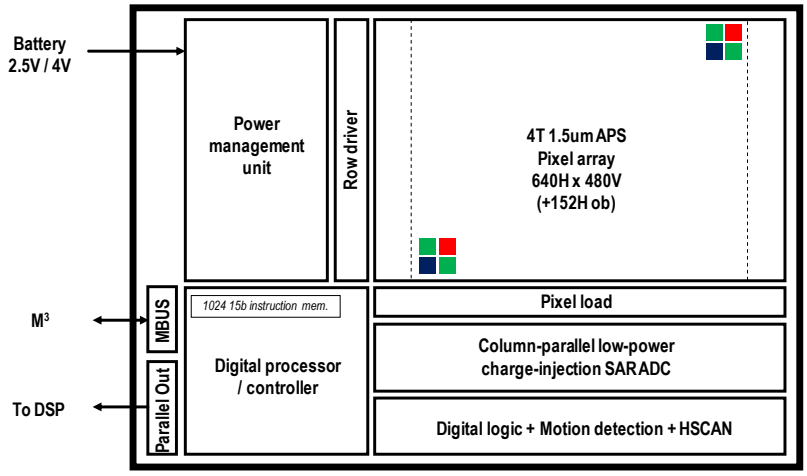
At an extreme, if only one charge-injection cell is to be used in the design, the amount of charge output per different bit decision is going to be in perfect integer-numbered ratio. With having lesser elements in the design, I leverage the fact that the mismatch manifests itself in a less damaging way (i.e. DAC/ADC gain error) than non-linearity/distortion. With this interesting side of charge-injection structure, I can fundamentally break the trade-off in designing high-accuracy circuit that typically involve rise in complexity. Bringing the notion to the extreme, one can shoot to design a 10b ADC with equivalent complexity that of a 1b ADC, i.e. with only a single charge-injection cell. There are other complicating factors, such as sampling switch with boot-strapping or low-noise comparators, but it is certainly true that the design complexity can be holistically brought down with using the charge-injection cell-based structure.

In this chapter, I have discussed the characteristics of charge-injection technique and charge-injection DAC/ADCs, seen in several different perspectives. In the next chapter, I will introduce an image sensor design where the charge-injection technique was applied to enhance its energy efficiency.

CHAPTER 3.

LOW-POWER IMAGE SENSOR USING CHARGE-INJECTION SAR ADC

Internet of things (IoT) is gaining more and more traction in recent years. Billions of sensors will be deployed in various forms of IoT devices, and among them, image information is one of the most interesting and useful data to be gathered in mass deployment. It is crucial that the sensors are designed to consume only minuscule power to last sufficiently long on a limited battery. To achieve this, an extremely low-power but capable image sensor design is in demand.



Power domain	Value
VDDA	1.4V
VDDP	1.7V
VDDUB	3.4V
VDDH	
VSS	0V
VSSN	-3.4V
VDDTGRGH	2.3V
VSSTGL	-2.5V
VSSRGL	-1.8V
VSSRGD	-0.6V

Figure 26. Overall structure of the low-power image sensor

To sate these demands, I designed the low-power image-sensor depicted in Figure 26. The sensor is built with column-parallel array of energy-efficient and low-noise capacitor-array assisted charge-injection SAR ADCs (c-ciSAR), and expansion from [14]. And it is coupled with a high quality 4T APS array of VGA size, that is sufficiently small to enable low-power operation but is reasonably large to acquire good spatial resolution in the image. The sensor also contains a

complete power management unit for it to generate all the required voltage domains internal to the chip such that only source of power is from a single 2.5V battery. And it features a fully programmable digital processor/controller to readily flex the sensor behavior to support operation in non-constant environments.

Typical use case for these sensors is not to continuously stream data, as it would diminish the battery very quickly, but to operate in full capacity only when there is interesting change in the scenery. Therefore, it is crucial that the sensor is, within itself, capable of monitoring the scene while it is only operating in part to conserve energy [25]. However, the placement of such function in the pixel [26], requires sacrifice in image quality. So, we looked to incorporate it digitally as part of the ADC. Also, to be sufficiently low-power in the monitoring mode, the circuits designed to operate at slow-speed (<10fps,max) and maximize the energy-efficiency.

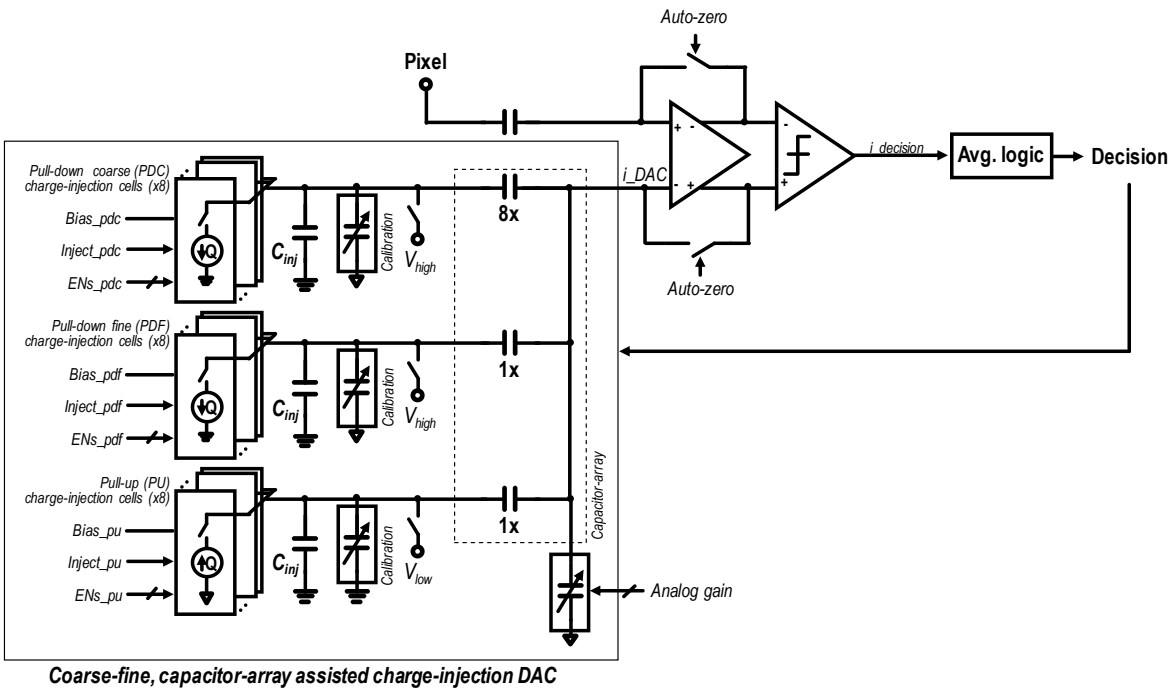


Figure 27. Block diagram of the low-power capacitor-array assisted charge-injection SAR ADC.

In the proposed energy-efficient SAR ADC, the charge-injection technique [14] is incorporated into a hybrid structure with the capacitive DAC as shown in Figure 27. The DAC is effectively divided into three paths, whereas per each path, eight charge-injection cells are implemented along with an output charge-to-voltage conversion capacitor (C_{inj}), a pre-charge switch, and a calibration capacitor bank. Each path has one of the either pull-down or pull-up direction set to its charge-injection cells and they are enabled accordingly to generate falling or rising change to their outputs. The changes in each path eventually merge to a single DAC output via connections through the capacitive DAC.

The separation of paths per their direction helped to better the linearity of charge-injection cells for their voltage headroom to operate in saturation significantly increased. And one of the three paths, which is a coarse pull-down path (PDC), is designed to have higher gain (8x) over the

others in the capacitive DAC to save the number of charge-inject operations required for the A/D conversion. One other benefit stemming from the separation is that the signal division ratio via the low-gain (1x) paths is high that swing range on their internal output on C_{inj} is also made high. This is good in terms of enlarging the LSB injection of the charge-injection cell, therefore, maximizing the SNR of the operation.

The subsequent comparator block has a static-current consuming pre-amplifier in the front to relax the comparator design. Using the pre-amp and the comparator, voltage generated by the DAC is compared with the pixel voltage and performs SAR operation. Auto-zeroing is performed before entering the SAR operation using the pre-amp, which is useful in reducing the reset-level SAR range and to decouple the DC level between the pixel and the ADC.

CASCODED CHARGE-INJECTION CELL WITH DUMMY PATH

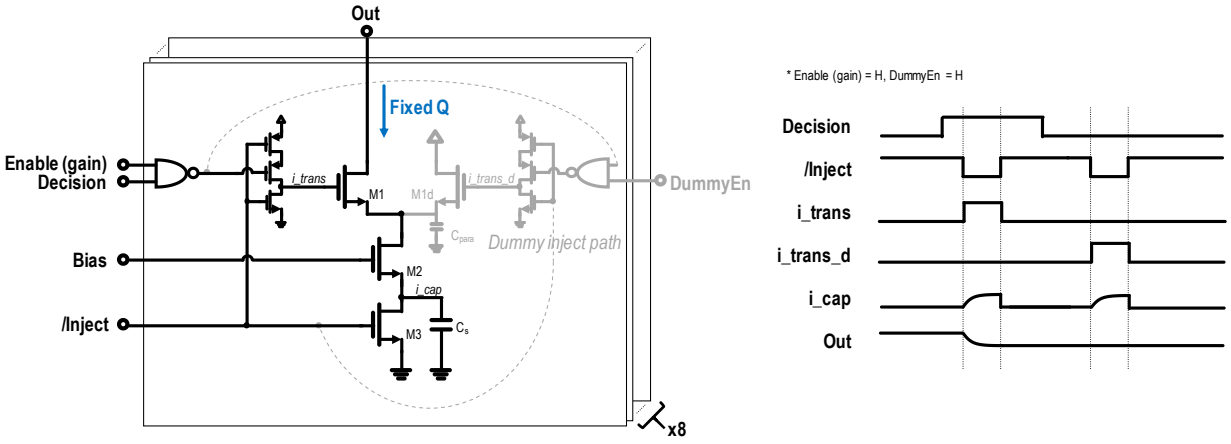


Figure 28. Charge-injection cell used for the proposed SAR ADC

Figure 28 depicts the charge-injection cell design for the proposed SAR ADC. The cell is designed to output fixed amount of charge when Inject signal is pulsed for pre-determined duration of time. During the operation, the majority of output charge comes from C_s. M2 with adjustable analog bias voltage connected to its gate is inserted in the charge conduction path. Its purpose is

to limit the maximum voltage on i_cap node during injection to control how much charge is sourced out for C_s, under the relation, Q=CV. M1 controls the on/off of the conduction path taking SAR decision direction and gain control word as supplementing inputs to an Inject signal. Also, C_{para} also contributes to the output charge, however, because its control voltage (VDD) may not be well regulated in this digital-intense circuit, the size of C_{para} was minimized to reduce its impact.

The cell also includes a dummy conduction path through M1d. To guarantee uniform operation among columns, as there is array of ADCs, the globally routed signals including powers should be well cared for to not add any modulation that would affect the whole array. For this reason, we inserted dummy conduction path that turns on whenever the conduction through the main path is absent, equalizing the operation. With dummy operation, the charge-injection process per column become independent of the local bit decisions that the global signals, i.e. power, is not modulated by any particular column operation. This greatly relaxes the speed/power requirement of the power management unit that supplies the VDD (or bias voltages).

The charge-injection cell is designed entirely of high-voltage transistors to control the stand-by power for low-power operation. It is also critical that high-voltage transistors are used for some parts of the circuit to dial down the impact of leakage current. For example, the cumulation of leakage current into the floating output capacitor (C_{inj}) through long ADC conversion time incurs voltage change leading to direct degradation of signal quality, therefore high-voltage devices must be used for part of charge-injection cell and calibration capacitors that are in contact with those floating nodes.

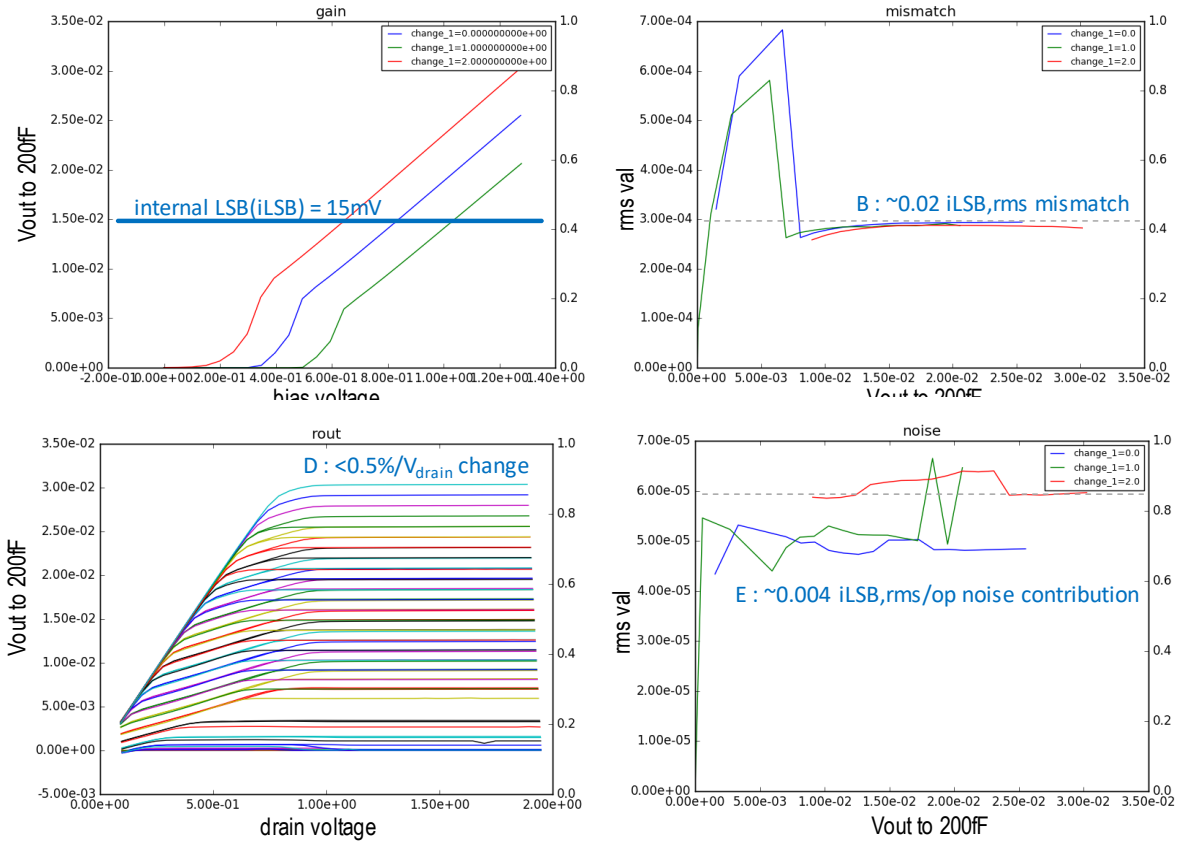


Figure 29. Performance measure of single pull-down charge-injection cell (upper-left) Charge output (measured in voltrage) to 200fF cap per sweeping bias voltage (upper-right) monte-carlo (m=100) result. X=internal LSB, Y=$\sigma_{v,mismatch}$ (lower-left) Drain voltage effect on charge output (measured in voltage). Multiple traces for different bias voltage (lower-right) Transient noise simulation (m=100) result. X=internal LSB, Y=$\sigma_{v,noise}$

Figure 29 shows the various performance measures of a single charge-injection cell of this design. As the upper-left figure shows, the target internal LSB (on C_{inj}) is around 15 mV whereas corner cases including PVT variations were also able to support the value. Note that at the lower-left corner of the plot, the line is kinky when biased below a certain voltage. This is related to the simulation setup that the cell does not reset completely within the simulated time as weakly conducting M2 interferes with the reset of C_{para}.

Plot on the lower-left shows the linearity performance of the cell. As the drain voltage (voltage on C_{inj}) falls (for pull-down case) from its initial value, it is crucial that the cell exhibits

sufficient output impedance that the amount of charge being output remains sufficiently constant against change in drain voltage. This is directly related to the successful >10b accuracy. To this purpose, designing the cell to have M1 and M2 to be in cascode configuration helped greatly to enhance the output impedance of the cell at the cost of slight reduction of voltage headroom. Initializing the output capacitor to the highest available voltage (or lowest for pull-up cell) in the sensor extends the linear range of the cell to accommodate the required signal swing.

The plot on the upper-right shows the mismatch performance of the charge-injection cell. The mismatch value (in unit of output voltage change) remains flat as the i_LSB size is increased (=bias voltage increase) since mismatch is dominated by the V_{th} variation of M2, which set the output charge amount. Because V_{th} variation is a static parameter unrelated to the bias voltage, mismatch voltage due to V_{th} also remains constant although the i_LSB size changes. Given the same circuit design, it is therefore desirable to operate the charge-injection cell at higher bias voltage to markdown the impact of mismatch relative to its output size. A similar observation can be found in the noise performance shown on the lower-right plot. Because the dominant noise from the kTC noise of C_s which is isolated from the biasing condition of the cell, bias voltage has negligible effect on it.

ADC ROW CONVERSION SEQUENCE

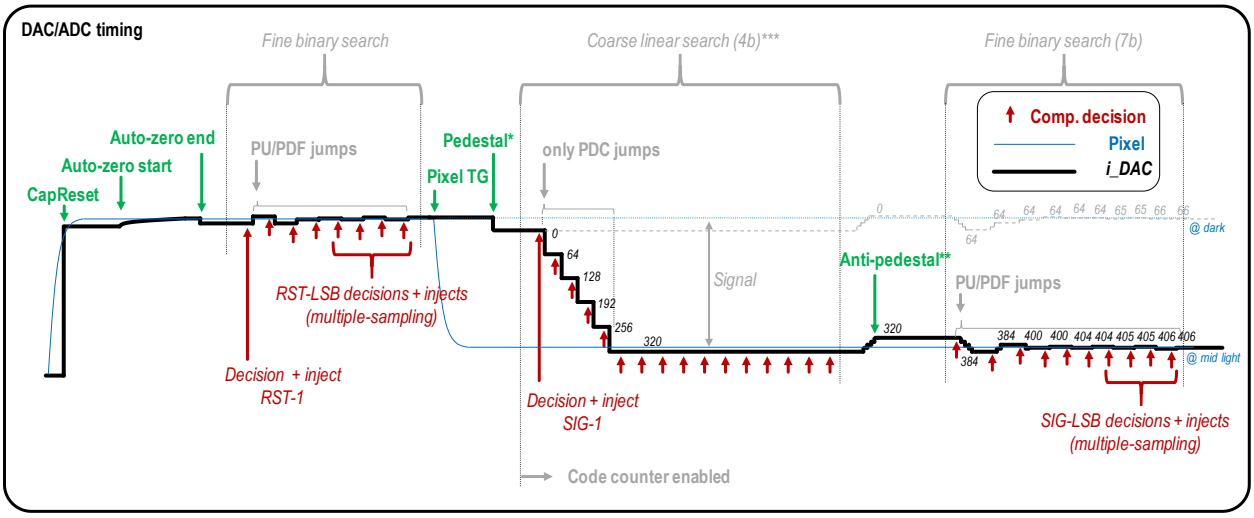


Figure 30. Illustrative waveform of pixel signal and the DAC output over ADC operation

With using the proposed ADC structure, we go through the conversion sequence illustrated in Figure 30 to construct the ADC code. First, with using the auto-zero switch on the pre-amplifier and switch on C_{inj}, the ADC is reset. And since exiting from the reset state may cause unaccounted alteration on the reset value, a small binary (or sub-radix) search is performed with using pull-down/pull-up cells in the low gain (1x). The two operations (autozero & reset value search) constitute dual correlated double sampling (dual-CDS), both done in analog domain. The decision result from reset value search is not saved as the intended CDS is done in the analog domain saved in the form of DAC output voltage, simplifying the CDS operation. After doing the first binary search (i.e. reset ADC), the pixel transfer gate is enabled for the signal to flow out to the pixel output and the ADC waits for it to stabilize. During this time, the DAC executes a pedestal operation. Pedestal operation is done to initially bring the DAC away from dark level before signal-level conversion to avoid triggering coarse linear search around the dark signal value. The reason is that the coarse linear search involves activation of the high-gain (8x) path which is relatively

high in terms of noise impact. Allowing the high-gain path activation to be involved in the dark-level conversion, the sensor noise performance can be degraded significantly. Once the pedestal level is applied, the ADC enters into a coarse-linear search.

The deployment of coarse linear search before going into the fine binary search, is important in several aspects. First, if binary search were to be used, it requires extra coarse pull-up operations to be implemented. This incurs extra circuit overhead and it is not sufficiently leveraging the fact that the signal in image sensor always tends to go down. Therefore, by applying coarse linear search, it saves on those unnecessary up operations and associated circuits. Also, the elimination of the extra up circuitry optimizes the required swing range of the pull-up and pull-down paths (internal) as an extra divisor in the capacitor divider is spared. Secondly, the coarse linear search allows the pre-amplifier to respond regularly and incrementally to small changing voltage, which means a slower pre-amplifier is sufficient to respond to the voltage changes. Also, making comparator decisions along every small step guarantees that although there is an error in the decision, the impact of the error will be contained within reasonable redundancy range of the subsequent binary conversion step. Also, albeit the increased number of decisions from deploying linear search instead of binary search, the loss of time is still minimized because smaller delta in DAC voltage limits the transition of pre-amplifier, therefore it can move on to the next decision step quicker.

After the coarse decision, an anti-pedestal is inserted before the beginning of the binary conversion to center the DAC voltage at the middle of the coarse linear search step. Doing this maximize overlap between the linear search and the fine binary search that the redundancy range is maximally utilized. The binary search begins from the step size which gives 1b overlap region with the coarse search. During this operation, only the lower gain (1x) pull-down and pull-up paths

are activated and the decisions are counted with a digital logic on +1/0 counting basis (not +1/-1). So, the output code of dark signal naturally contains an offset value of ~66 code in the example above.

The last operations of the binary search are for multiple sampling. To achieve multiple sampling, two different approaches are implemented; 1) repeat the LSB decision cycle for MS1 times and/or 2) fire the comparator decisions MS2 times within a cycle and perform majority voting. When the noise level is comparable to the LSB size, using the first approach is both effective and energy efficient. The sensor can incorporate a one of or both approaches to lower the input referred noise of the ADC. However, MS2 necessitates either increased current conduction on the pixel bias and the pre-amplifier or increased comparator decision interval to have observable noise-lowering effect. If the currents are small or the comparator decision interval is too short, the noise from the pre-amplifier and the pixel changes too slow that they are not sufficiently uncorrelated at each comparator activations to benefit any noise averaging.

In each LSB decisions, one of either low-gain (1x) pull-up or pull-down cell is activated first then a decision is made and then the other cell is activated based on the decision and another decision is made. So, a single LSB operation is actually comprised of two comparator decisions and DAC activations. If both pull-up or pull-down cells are activated to apply a single decision result, it is effectively an LSB-1 operation (+1/-1) which results code-of-two difference not an LSB decision. To apply code-of-one difference, we separate the DAC activations into two cycles each enabling only one of the pull-up (0/-1) or pull-downs (+1/0) and make the comparator decisions. The order of execution is not important.

C-CIDAC NOISE CONTRIBUTION

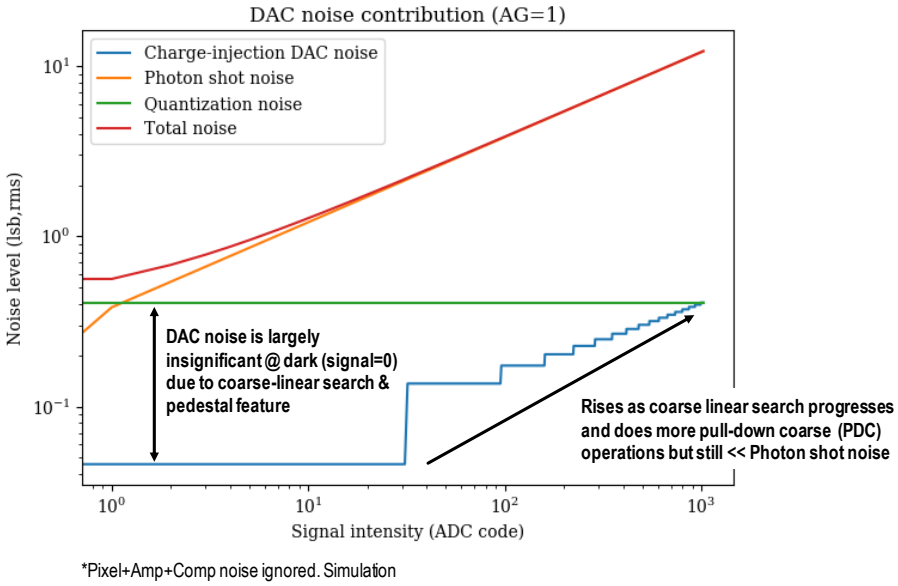


Figure 31. Increasing noise contribution of DAC at larger codes and its relative magnitude compared to photon shot noise and quantization noise contribution

As mentioned previously, an interesting noise property of the proposed ADC is present due to coarse linear search. The coarse linear search makes the ADC to arrive at smaller signal values with less activations from the DAC. Distinctly from binary search, the number of charge-injection activations for different codes are not constant. This is important because in the proposed DAC structure, every charge-injection activity directly adds cumulated noise at its output (as in accumulator, random walk) and involving lesser activity translates to less noise contribution from the DAC at that value. The issue of added noise from DAC activity could be observably high when the fact that high-gain (8x) path impacts stronger to the resultant noise due to smaller division involved in the design of the path is considered. By avoiding high-gain (8x) path from activating in the noise-critical code, i.e. dark level in image sensors, helps to reduce the overall contribution of the DAC noise. The notion is simulated, and the result is shown in Figure 31.

The simulation sweeps the input code and assumes uncorrelated noise addition per each DAC activations to estimate the noise contribution at the swept code. As can be told from the plot, the noise contribution from the DAC at low code is in fact very small thanks to the inactivity of the coarse high-gain (8x) path and also the significant division factor for the low-gain (1x) paths. But as the code increases, its contribution tends to increase and finally come close to the quantization noise, signifying the increased contribution of noise from the high-gain (8x) path activations with progressing linear search. The heightened DAC noise at higher code is, however, tolerable for the case of image sensors because when the captured scene is lit, the photon shot noise dominates the SNR which has the tendency to increase as the code rises. This means that the DAC noise at higher code can hide far underneath the photon shot noise, unaffecting the sensor SNR. The only codes of concern to the ADC, thanks to the linear search operation, is around the dark level codes. At dark level, only low-gain path (low noise) activations are involved in the AD conversion, hence greatly alleviates the energy budget of charge-injection cell design. As a result, the overall sensor is both DAC noise tolerant and energy efficient.

ENERGY EFFICIENCY IMPROVEMENT USING HIGH-GAIN CAPACITIVE SUMMATION PATH

Though noisy as it may be, the high-gain (x8) path is useful in increasing the energy efficiency of the DAC operation. Operating the ADC in 10b with only the low-gain (x1) paths would require more than 1024 activations of charge-injection cells, which consumes too much energy. Also, it renders the ADC undistinguishably energy-inefficient compared to single-slope ADC which has proportional activations of its elements to conversion-steps. Assuming the ADC does full-scale binary operation with only low-gain paths, the ADC would require ~1136 activations of charge-injection cells.

Table 2. Energy consumption of each parts in the ADC based on simulation

* Not accurate to measurement. Values based on simulation. Not optimized

	100us 1H-time	*Power domain (V)*	*# (avg) ops in 1H*	*Total charge (pC)*	*Total energy (pJ)*	*% energy*
ADC	Amplifier	1.4		10	14	26.8%
	Comp. +driver	1.4	30	4.7	6.58	12.6%
	Charge injection	1.4	384	5.76	8.06	15.5%
	Leakage of LGC	1.2		2	2.4	4.61%
ADC sub-total (pJ)					*31.04*	*59.5%*
Pixel	Pixelbias	1.7		10	17	32.6%
CTRL /HSCAN	Others	1.2		3.39	4.07	7.89%
Total Energy (pJ)					***52.11***	***100%***

However, with introducing the high-gain (8x) path and applying coarse linear search, the number of charge-injection cell activations is reduced to 384 times (with assuming the signal to be at mid-level) with dummy transfer overhead. The number goes down to 202 activations if dummy transfer overhead is not counted. Through using this technique, the energy consumption of the DAC can scale. With higher gain on the high-gain path, the energy consumption can further be reduced. Also, leveraging the fully programmable controller and the flexibility of the proposed DAC, selection of different allocation of bits for coarse linear search and the fine binary search (=larger coarse step) can be explored and the number of activations then can be lowered to 146, further enhancing the energy-efficiency

NOISE REDUCTION USING MULTIPLE SAMPLING

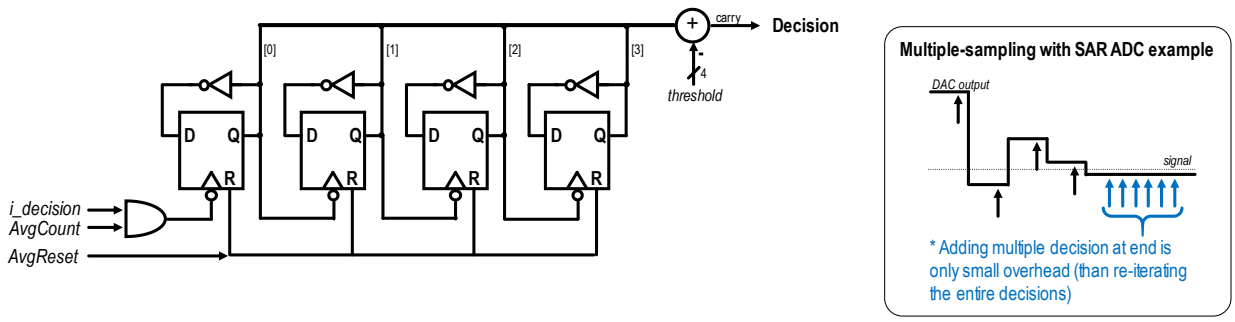


Figure 32. Average circuit enables multiple sampling within one decision cycle

One of the distinct merit of using SAR ADCs in image sensors compared to industry-wide dominant single-slope ADC is that its ease in leveraging multiple sampling. Multiple sampling is useful in lowering the noise contribution of the circuit. In single-slope ADCs, multiple sampling has to involve the entire conversion to be repeated from beginning, therefore, there is an extremely low limit on how much of multiple sampling can be realistically achieved. However, in SAR ADCs, to reap the effect of multiple sampling, it only needs to repeat LSB operations. This means that the multiple sampling count can easily be increased with only sacrificing relatively short duration of time at the end of the conversion cycles that minimizes its impact on speed.

The procedure and the circuits for multiple sampling is shown in Figure 32. The averaging circuit is inserted after the comparator to count the positive decisions and then to compare the sum with a programmable threshold value. This operation constitutes a majority voting. The 4b counter design effectively allows up to 7 times of multiple sampling (MS2) to be done per one decision cycle.

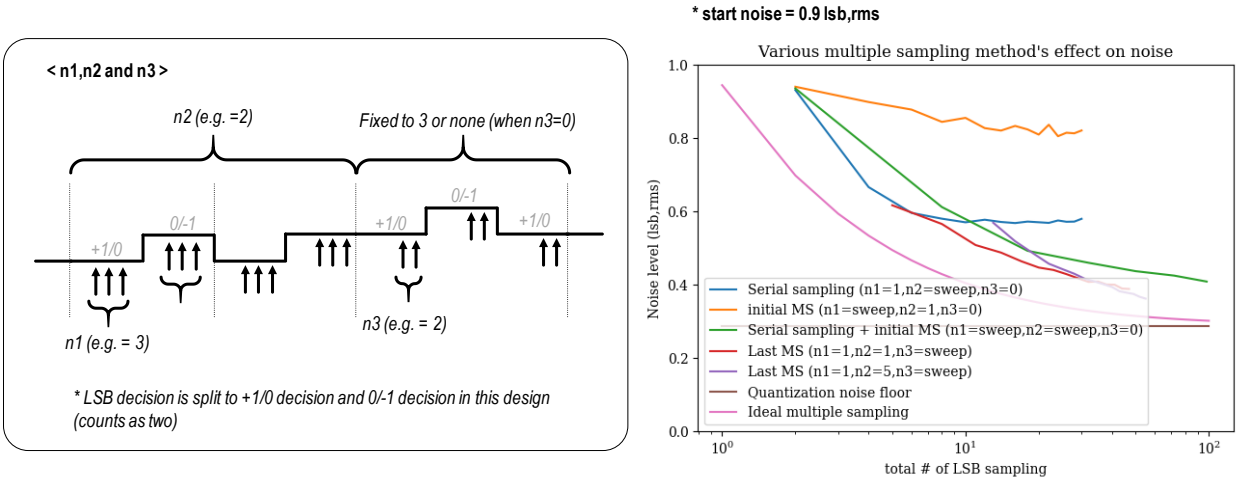


Figure 33. Different implementation of multiple sampling and their efficacy. Simulation result (right) is based on a model that assumes uncorrelated noise at every sampling instances

Yet the efficacy of multiple sampling can vary vastly by how MS1 and MS2 are combined. With different allocation of MS1 and MS2, the resulting noise can be quite different. Figure 33 shows different strategies and their respective noise output with sweeping total number of sampling. As pink line on the right plot shows an ideal noise reduction profile for given the same noise (=$1/\sqrt{N}$), other lines are found to its right which implies they are inferior. This shift can be explained to the first order by the fat that double decisions are involved within the proposed LSB operation and it renders the multiple sampling inefficient by $1/\sqrt{2}$ as default.

The blue and the red line of the plot are closest to the ideal noise reduction curve, therefore can be said as the most effective among the choices. The blue line is in fact not incorporating any MS2. It instead just executes LSB decisions for several more times (MS1), yet it is shown to be effective to bring the noise down to a certain lower limit. The effect can be explained by imagining white noise that is much greater than an LSB size. Although the noise is much larger than the LSB size, statistically it is likely that the DAC level has settled to a point where the probability of making an up decision or down decision has become close to 50/50 after multiple trials of LSB

decisions. For decisions past this point, the DAC is likely to alternate around that level by one code, which means it has depreciate the size of the noise that spans multiple LSBs around it. This behavior implies filtering and therefore, just repeating the LSB decisions has an effect to reduce the noise.

Yet the lowest noise that blue line can achieve is bound to certain limit. To go further down in noise, we must resort to strategy demonstrated as red or purple line which involves MS2. Both approaches involve MS2 on the last three MS1 iterations, where three is chosen to supply sufficient redundancy range. The plot shows that to go down further below the limit on the blue strategy, we must resort to explicitly doing multiple comparator sampling per decision cycle (MS2). The blue line strategy (MS1) is more effective and energy-efficient when the noise is comparable or larger than an LSB. And red strategy (MS1+MS2) achieves the best noise. The sensor can be programmed either ways.

CALIBRATION CAPACITOR BANK AND CALIBRATION OPERATION

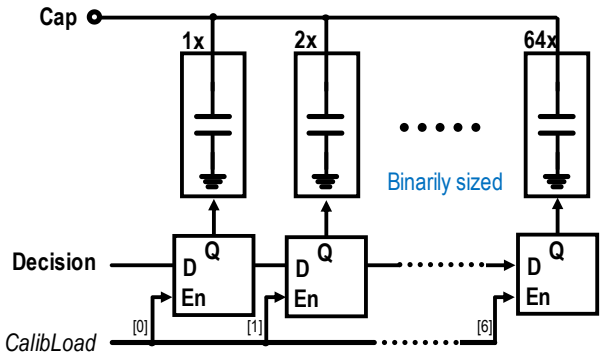


Figure 34. Calibration capacitor bank

The charge-injection DAC structure offers many performance boosts, yet it comes with one disadvantage compared to single-slope ADC in that it requires per-ADC and per-path calibration to combat mismatch. Single-slope is tolerant to per-column mismatch for it is typically

referenced by a single ramp signal generator that is global to all the column ADCs. However, the charge-injection cells in our proposed ADC are all separate devices that is victim to their respective mismatches.

To fight mismatch, calibration capacitor banks are installed per path that will trim the output capacitor (C_{inj}) to adjust the charge-to-voltage conversion ratio to be equal among all columns. This function is implemented as shown in Figure 34.

Necessitating a calibration capacitor array at C_{inj} may defeat the purpose of using charge-injection cell-based DAC structure that is originally supposed to reduce area. Yet the matching requirement of these capacitors for calibration is much relaxed than capacitors that construct typical 10b capacitor DACs that its size can still be compact. The calibration capacitor bank is designed to be 7b but because they do not need strict matching properties, each bit capacitors are binarily sized. This is tolerable for this design as they only need to be monotonic.

The size of the array, 7b, is determined from the desired INL performance of the image sensor and the mismatch characteristics of the charge-injection cell. As a rule of thumb, any form of static error that manifests in column or row basis (not pixel basis) in the image should be 1/10 of the noise (TN = temporal noise) that dithers it. Therefore, the gain error of the ADC, which is the relevant column basis performance in this case, should be lesser than 1/10 of the photon shot noise. Calculation yields that the required error should be lesser than 0.5 % so we designed the resolution of the calibration capacitor bank as to be around 0.25 % with margin. Yet a single charge-injection cell exhibits ~2 $\%_{rms}$ mismatch that with incorporating eight cells per path, the anticipated mismatch per group is ~0.7 $\%_{rms}$. Taking ±6σ as our design criteria, the range that the calibration capacitor bank should cover becomes ~± 5%=10 $\%_{min\text{-}max}$ range. Expecting some extra

amount of deterministic column-to-column error, we have implemented ~30 $\%_{min\text{-}max}$ range of tunability for calibration capacitor, thus is designed at 7b.

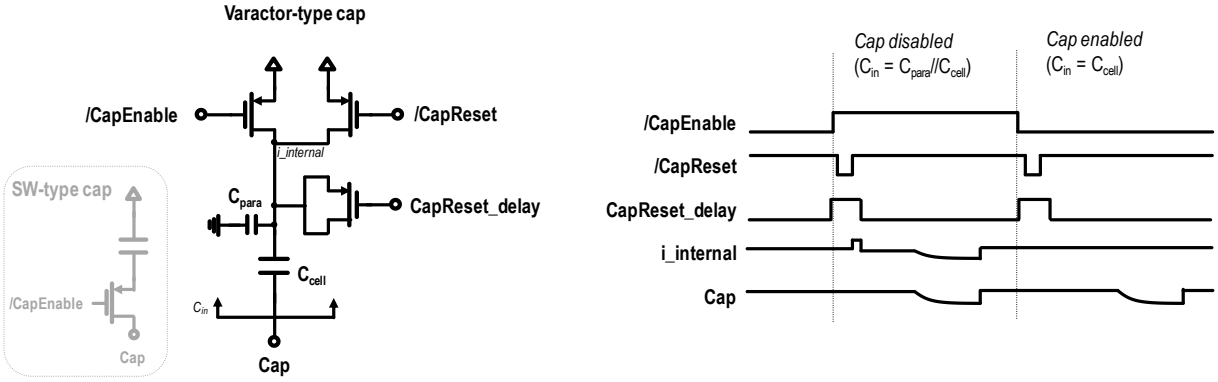


Figure 35. PMOS varactor-type capacitor for calibration capacitor bank and AG cap used for pull-down paths.

In making the capacitor bank, simple switch-and-capacitor design was insufficient in achieving the resolution of 0.25 % from 200 fF (= 0.5 fF), thus I had to resort to a varactor-type capacitor as shown in Figure 35. Normal approaches to tunable capacitor involves a switch that can either conduct or isolate the node from extra capacitance. However, this technique was inadequate for controlling such small delta capacitance whereas the gate capacitance and the s/d capacitance alone exceeded the required 0.5fF limit. Also, the capacitance of this type is non-linear and changes with applied voltage, therefore is not suitable to achieve 10b operation. Varactor-type capacitors has off-capacitance that could be fairly larger than the conventional type, but it is capable of generating small delta capacitance. As shown in the figure, when the capacitor is on, it sees the entirety of the C_{out} whereas when it is off, it sees a serial connection of C_{out} and C_{para}. If C_{para} is designed to be comparably large, the delta capacitance of this cell can become small. Also the capacitance is constant with applied voltage, making it suitable for 10b.

However, one drawback of this design is that the switches controlling the on/off may leak current if the voltage on the internal node (i_internal) were to rise beyond VDD (for PMOS case).

Although the voltages on the output node of the charge-injection cell go only one direction that with right configuration of polarity will avoid such event, but there is still coupling from activities of other paths that may put the internal node (i_internal) to a value that prompts leakage. Also, even the coupling of the gate signal (CapReset) that releases the reset of the floating internal node (i_internal) may put the voltage temporarily above VDD.

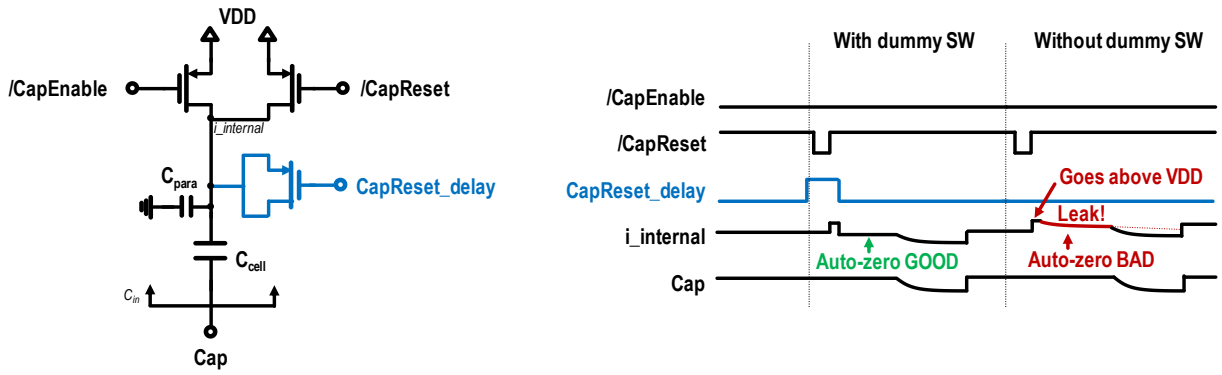


Figure 36. Avoiding leakage due to i_internal coupling higher than VDD

To avoid this effect, we have inserted a dummy transistor to cancel the rise of voltage with using a complementary signal that falls at the end of reset and then applying auto-zeroing. The falling complementary signal is useful to pull the i_internal node sufficiently down to not to be affected by leakage. If it weren't the case, not having a perfect auto-zeroing or correlated double sampling (CDS) risks generating column fixed-pattern noise (CFPN) that streaks the captured image in vertical direction. With adding the dummy transistor to prevent rising of i_internal, it helped to reduce CFPN down by more than 2x (from 0.1 LSB_{rms} to 0.04 LSB_{rms} in measurement).

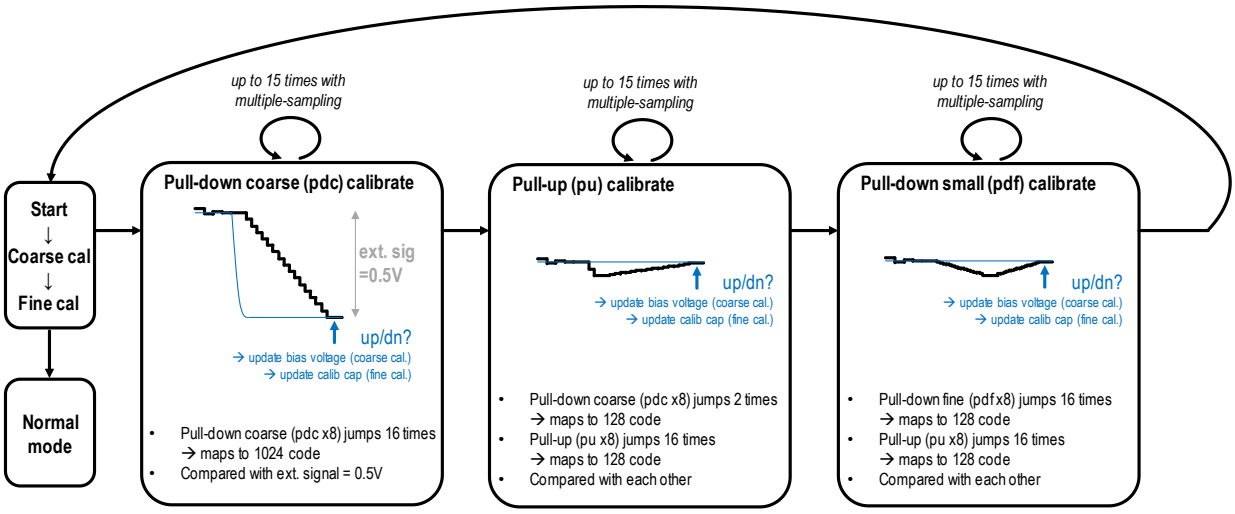


Figure 37. Calibration sequences

With introducing the calibration capacitor bank to each column ADCs, the ADCs can be calibrated finely to adjust for its local mismatch. However, since PVT variation may introduce a larger breadth of fixed variation which may not be within the fine calibration range, a wider range calibration method is also needed. Hence the sensor integrates two calibration methods and performs them to cancel out the two different sources of variation. Dubbed fine calibration and coarse calibration, the procedure for each is carried out the same way, except that the fine calibration applies to the column-parallel calibration capacitor bank whereas the coarse calibration applies to the global charge-injection cell bias voltages.

The first path to calibrate is the pull-down coarse path (PDC). With using a known voltage generated within the PMU, the columns compare fixed amount of PDC jumps to determine whether the path's gain is higher or lower than desired. The information is tethered to the controller for the coarse calibration and then all column values are summed to be used to adjust the global bias. In fine calibration, the decision information is applied directly to the column calibration capacitor bank where latches are to hold them. The sequence continues to low-gain (1x) pull-up path (PU) calibration and then the pull-down path (PDF), where the calibrated output of the

previous paths is used as reference to tune the next one. Due to this sequential operation, the calibration error from the previous stage may roll over to the later stages. To work around this issue, it is important to design the circuit to make the most accurate adjustment to the PDC path. This may involve incorporate as many charge-injection operations as possible to reduce the effect of noise. In practice, the averaging circuit is activated to perform averaging of calibration decisions to further lower the noise contribution from the pre-amplifier and comparator.

PER-COLUMN SAR LOGIC CIRCUIT

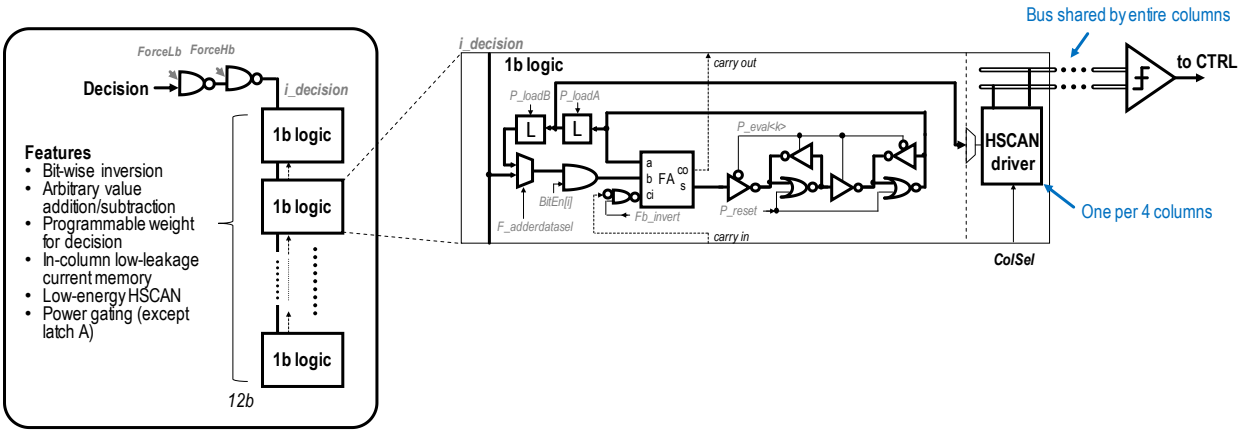


Figure 38. SAR logic circuit of the proposed ADC

The per-column SAR logic of the proposed ADC is shown in Figure 38. The block is comprised of multiple 1b logic cells that has the capacity to perform the list of functions denoted in the figure; 1) inversion, 2) absolute value, 3) arbitrary addition/subtraction, 4) storage, and 5) power gating. It also features a horizontal scan (HSCAN) driver that is static but is small swing to reduce energy consumption for data transfer.

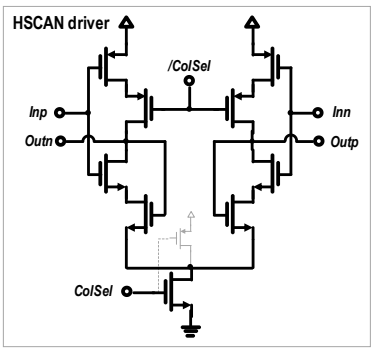


Figure 39. Static small-swing HSCAN driver

The driver has a diode connection for the pull-down part of the circuit that effectively limits the swing on the output node. Also, it is designed to be put into low-leakage mode when disabled to reduce the stand-by power.

MOTION DETECTION MODE

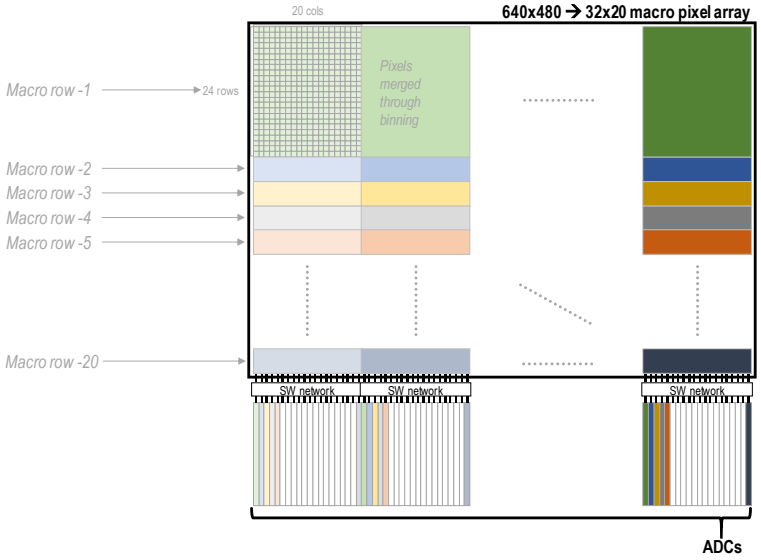


Figure 40. Sub-sampling of the pixel array for motion-detection (MD) mode and the macro-pixel mapping to column ADCs

As mentioned in the beginning of the chapter, the proposed image sensor contains a feature to monitor the scenery until interesting change has happened to invoke full capacity operation. During this monitoring state (MD mode), the pixels are grouped together to form a low spatial

resolution array (32x20) of macro-pixels (MD pixels). The number of MD pixels is selected to be less than the total number of ADCs so that values readout from each macro-pixel can be stored inside the pre-existing column memory to enable frame-to-frame comparison without incurring much hardware overhead. The stored frame value is retained until next frame comes then is used to see if change in value is greater than certain threshold. The controller aggregates the number of pixels that have exceeded this threshold to determine it is worth taking a full-capacity frame by applying another threshold. With using this feature, the sensor can run at low-demanding MD mode for most of its working time and only seldom trigger to take high-precision frame in extended interval.

As means to achieve MD functionality without needing extra hardware, a n-way side-step mapping of motion pixels to the ADCs is proposed, as shown in Figure 41. The MD pixels are subsampled every nth-column and ith-row. For row r, an MD pixel at coordinate (r • i, c • n), where c = {0, 1, …}, is re-routed sideways to column (c • n + r) for data retention and in-column MD computation. As readout progresses vertically across subsampled MD rows, the mapped ADCs shift horizontally, and all MD pixels are mapped to column ADC. Both the storage of the MD pixel values and the differencing of values between MD frames reuse existing hardware of the c-ciSAR, thereby incurring minimal area overhead. The subsample stride (n, i) and resulting MD frame size (h, v) are configurable with the constraint that h • v < k, where k is the total number of full active-array columns (640 for VGA). Skipped pixels can be enabled and binned together to minimize blind spots using three methods: floating diffusion (FD) binning on 2 shared Gr-Gb pixels, source-follower (SF) binning across horizontal/vertical direction, and digital binning in the column logic. For our evaluation case, n = 20 and i = 24, resulting in an MD frame resolution of 20x32 pixels.

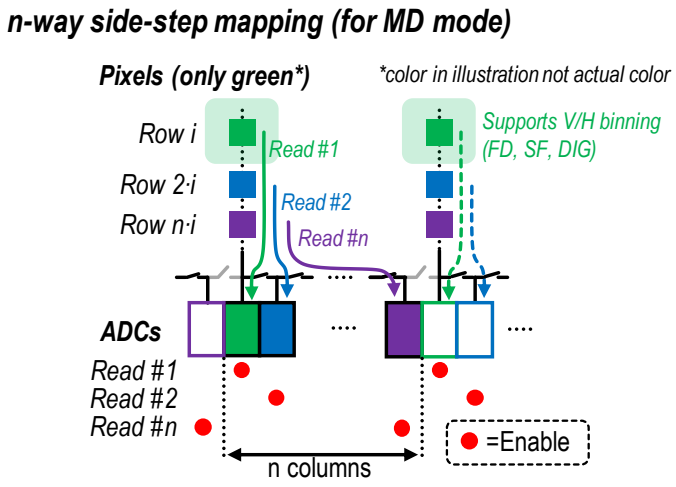


Figure 41. n-way side-step mapping for MD mode operation

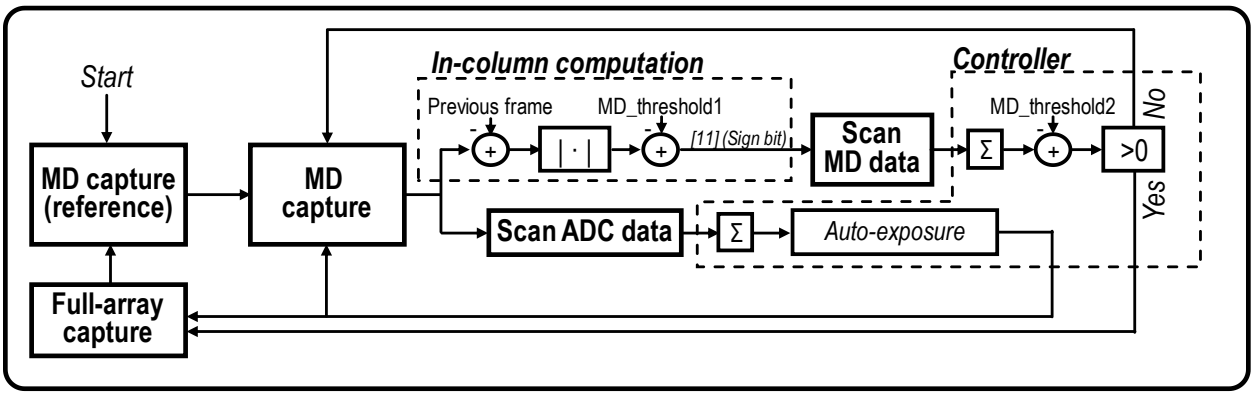


Figure 42. Algorithm for in-column motion evaluation.

Figure 42 shows the MD mode procedure. Using the unit operations of the SAR logic circuit that is part of the ADC, we store the MD pixels in-column and detect those with significant changes in their code. First, when a new MD frame is captured, its code is reconstructed from SAR decisions within the column. When the entire MD frame has been readout, the computation is performed to the whole frame. While the current frame code is stored into a separate column memory (Latch A), it is also being subtracted from the previous frame that was stored in the column memory (Latch B) in the logic. This operation yields the difference between the previous frame value and the current frame value. An absolute value function is then applied to the

difference by referring to the sign bit of the difference and then inverting it only when the sign bit is High, denoting negative value. Next, the pre-set threshold value is broadcasted from the controller to the entire array and then subtracted, giving a flag (inverse of the sign bit) that denotes whether the absolute difference has exceeded the broadcasted threshold value (MD_threshold1).

The controller gathers and accumulates the MD flags (sign-bit of difference result) along with the frame values to determine whether to proceed to full capture and to adjust exposure value. The full-array capture is only triggered when there were sufficient number of pixels (MD_threshold2) that had significant change in their values. Adjusting this threshold value can adjust the sensor's sensitivity to motion.

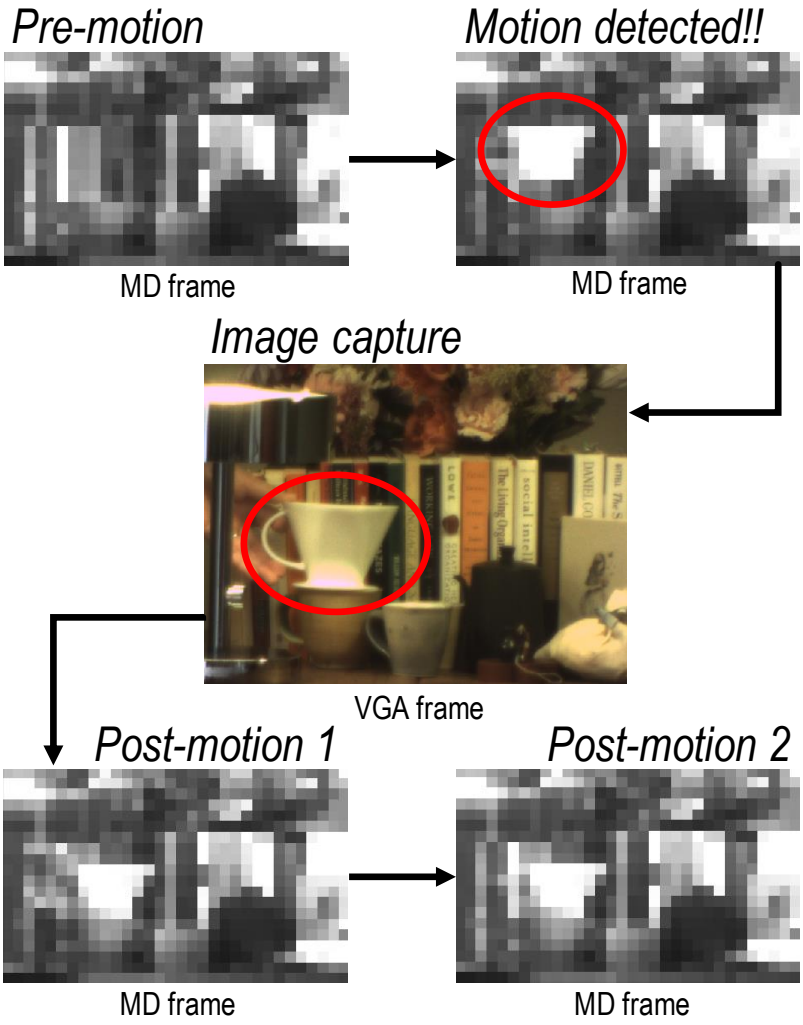


Figure 43. MD mode triggering full image capture when motion is detected

Figure 43 shows captured image result from the sensor in MD mode. In presence of a significant motion (red circle) the sensor successfully triggers the full-array capture to provide highly detailed image to tell what was newly introduced or was taken out of the scene.

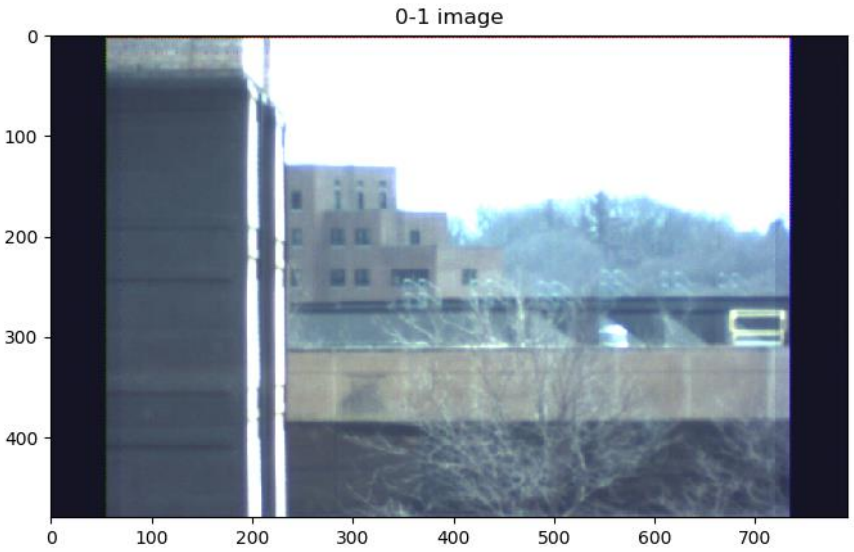
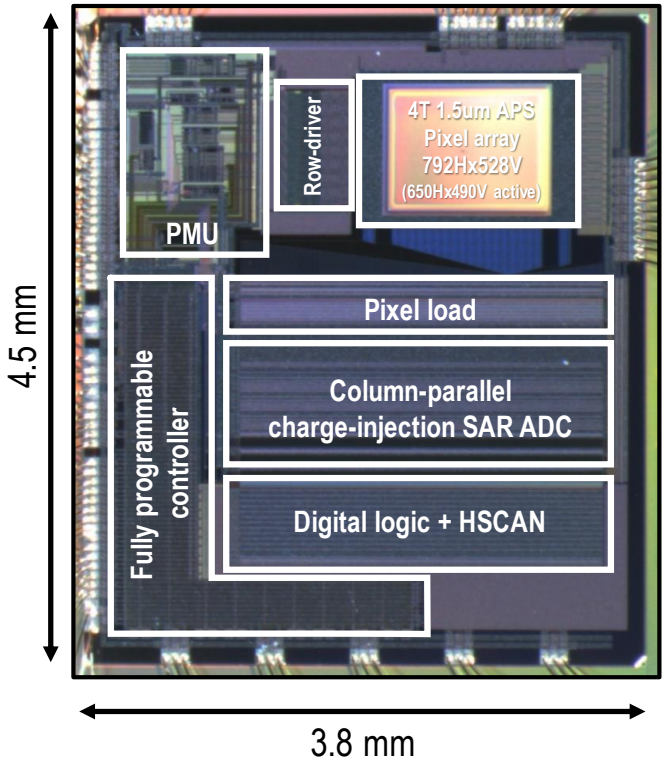
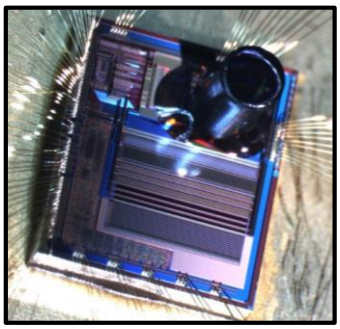


Figure 44. Sample image from the proposed imager in full-array mode





Technology	TPSCo CIS 65nm 1P3M
Die Size	3800 um (H) x 4500 um (V)
Pixel pitch	1.5um
APS array	792H x 528V (Active : 650H x 490V > VGA)
# of ADC ch.	792
ADC pitch	3.1 um

Figure 45. Chip photo along with sensor level specifications

Figure 44 shows a sample image taken with the proposed imager in full-array mode. The quality of the image (i.e., resolution) is limited by the optics and the sensor itself does not exhibit any noticeable artifacts, such as sunspots, blooming, CFPN or horizontal band noise. Color is reproduced with using OpenCV's de-mosaic function. Figure 45 show the chip photo of the proposed imager. The sensor is intended to operate with miniature optics (i.e., GRIN lens) and an example integration with GRIN lens is shown in the same figure (right). The proposed ADC is made at a different pitch than the pixels to fit high-voltage transistors inside the column. The full performance out from the proposed imager is comparable to the industry grade image sensors but consumes significantly less power.

Table 3 provides a comparison with other recent works with MD capability or SAR ADCs. The energy efficiency of the complete sensor is 37.9 *uV·nJ* (ADC FoM). However, this number is dominated by the fully programmable controller (for flexible testing purposes); a simple hardwired state machine could be used in a more lightweight implementation. Excluding the controller energy consumption and evaluating only the readout energy (pixel, ADC and stream-out), E/frame/pix is 63.6 *pJ*, and the ADC FoM is 14.4 *uV·nJ*. The E/frame/pix in MD mode is 230.5 times smaller than that of a single-slope sensor [25]. Also, the sensor can operate with its on-chip PMU, which generates all internal voltages from a single external 2.5V battery, enabling integration into an IoT sensor. The die area is 17.1 mm^2.

In this chapter, I have discussed the application of charge-injection technique to boost energy-efficiency of image sensors. In the next chapter, I will introduce another charge-domain technique applied on a pre-amplifier for comparator that was useful in improving its energy efficiency.

Table 3. Comparison table for the proposed imager

		This work			***Kumagai ISSCC 2018***		***Kim ISSCC 2013***	***Ji VLSI 2016***
Technology		65 nm CIS			90 nm CIS + 40 nm		130 nm	180nm
Pixel structure		4T 1.5 um			4T 1.5 um		3T 6.4 um	3T
Full array resolution		792 x 528 = 418.1 K (Active=VGA)			2560 x 1536 = 3.93 M		128 x 128 = 16.3 K	320 x 240 = 76.8 K
MD mode support (& MD resolution)		O (32 x 20 = 640)			O (16 x 5 = 80)		O (48 x 16 = 778)	X
Readout circuit	*ADC type*	Capacitor-array assisted charge-injection SAR ADC			Single-slope ADC		Single-slope ADC	SAR ADC
	Resolution	10 b			10 b		8 b	10 b
	Full signal range	500 mV			435 mV		-	-
	ADC noise [uVrms]	*Condition*	*Meas.*	*Q. adj*4*	*Cond.*	*Meas / Q. adj*	-	450 (w/ pixel noise)
		no MS, AG*1=7.7 dB	**226***3	211	AG=18 dB	100.4 / 98		
		MS=(4,1)*2, AG=7.7dB	180	161				
		MS=(1,5), AG=7.7 dB, I_{amp}↑	136	108				
		MS=(2,15), AG=7.7 dB, I_{amp}↑	106	68				
Full capture mode	*Dynamic range*	64.3 dB			67 dB		38.5 dB	-
	Max frame-rate	5.6 fps			60 fps		19 fps	130 fps
	@ dark condition, no MS, PMU off	*Readout only (ADC + pixel)*	*Sensor (w/ controller)*		*Sensor*		*Sensor*	*Readout only (ADC + pixel)*
	Energy / frame [uJ]	**26.6**	70.1		1583		1.5	16.9
	Energy / frame / pix [pJ]	**63.6**	167.5		400		610	220
	*ADC FoM [uV·nJ]*5*	**14.4**	37.9		40.1		-	99 (w/ pixel noise)
MD mode	*Res. & max. frame-rate*	10 b, 170 fps			8 b, 10 fps		3 levels, 30 fps	-
	Energy / frame [uJ]	**0.26**	1.7		110		0.036	-
	Energy / frame / pix [pJ]	**400**	2650		1375000		46.3	-
	*ADC FoM [uV·nJ]*5*	**90.4**	598.9 (x1)		138050 (x230.5)		-	-

*1 AG = Analog Gain
*2 Multiple-sampling (MS) notation : MS=(MS1, MS2)
*3 This number is used for the rest of the table
*4 Quantization noise adjust : sqrt(ADCnoise^2-2/12·LSB^2)
*5 ADC FoM : ADCnoise [uV] * (Energy / frame / total pix) [nJ]

CHAPTER 4.
ENERGY EFFICIENT CHARGE-DOMAIN PRE-AMPLIFIER WITH < 1 DISCRETE TIME EQUIVALENT NEF

Extremely low-power circuits are in high demand for IoT applications, such as health monitoring and activity detection. This trend is driving research in highly energy efficient circuits and calls for re-examination of basic building blocks to increase energy efficiency. Comparators are a critical building block in analog design and are frequently used in ADCs, where they often dictate performance. However, most research has focused on their speed or noise characteristics rather than energy efficiency. Comparators often use a low-noise continuous (pre-)amplifier to boost performance, but this typically limits overall energy efficiency since the pre-amplifier has a limited noise-efficiency factor (NEF) in CMOS (>2). Also, deploying a continuous-time pre-amplifier with a discrete time comparator risks wasting energy due to their inherent difference in operation principle (continuous vs. discrete). Recently, two new discrete time comparator approaches were proposed with time-domain amplification using edge propagation through inverter delay chain(s) [5][27], demonstrating renewed interest in energy efficient comparator design.

This paper presents a simple and energy efficient discrete time pre-amplifier (Q-ccAmp) that uses charge-domain operation and achieves gain via ratioed capacitances. Since the proposed pre-amplifier interfaces in voltage mode in discrete time, it easily integrates with existing comparators. When combined with a traditional comparator structure, comparator noise improves by 3.9× (992 to 252 uV_{rms}) while incurring only 10.1 *fJ/op* energy overhead (measured). The pre-

amplifier achieves an energy-noise^2 product (ENP) of 0.59 $fJ{\cdot}mV^2$ with 0.93 discrete time equivalent NEF (eq. NEF).

Conventional gm-based techniques for improving NEF, such as multi-chopper [28] or current re-use [29], are commonly used in continuous-time amplifiers to extract gm multiple times from the given current. However, those techniques require complex circuits to perform gm aggregation, and they do not integrate well with discrete time operation. Charge domain-based analog circuits, including amplification, have been proposed [14][30] but have not offered eq. NEF improvements. Charge domain operation uses finite amounts of charge and therefore has the advantage of being inherently discrete time and compatible with common discrete time comparators. The proposed pre-amplifier transfers charge (modulated by the input voltage) from a large capacitor to a small capacitor, thereby achieving input-to-output voltage gain. This operation poses a unique trade-off for improving NEF: energy is determined by capacitance voltage swing while noise is determined by kT/C and gain, which is only weakly coupled to voltage swing. Exploiting these trade-offs allows us to achieve a sub-1 eq. NEF (0.93).

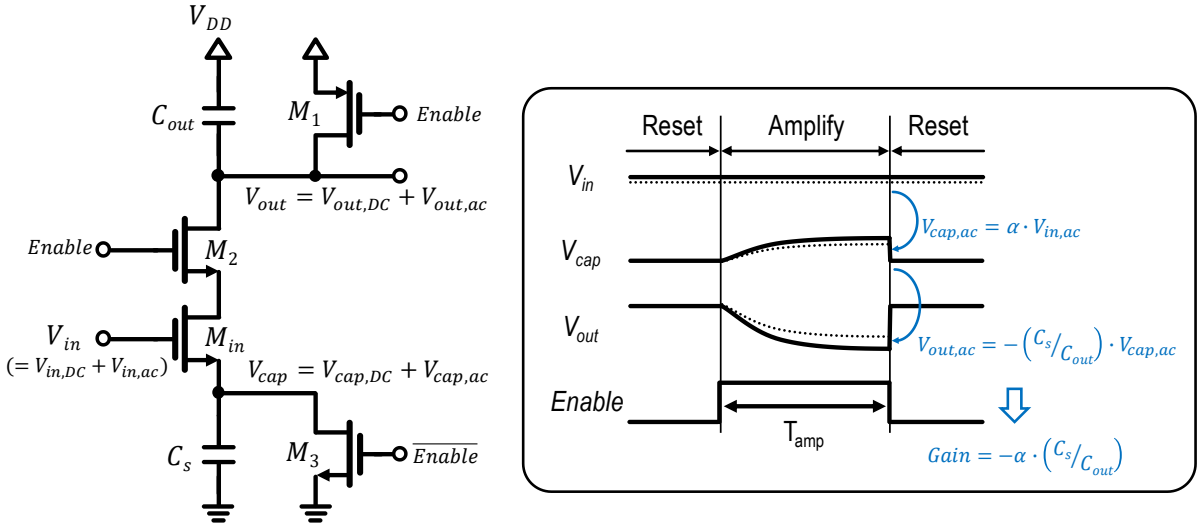


Figure 46. Proposed charge-domain capacitor ratio based pre-amplifier (Q-ccAmp) and its operating sequence. Gain between V_{in} and V_{cap} ($\equiv \alpha$) and the ratio between C_s and C_{out} determines the amplifier gain

Figure 46 shows the structure of the proposed pre-amplifier, consisting of four transistors: M_{in} is the input transistor, M_1 and M_3 provide reset functionality, and M_2 isolates conduction between V_{out} and V_{cap}. During the reset phase, C_{out} and C_s are pre-charged by M_1 and M_3 to V_{DD} and GND, respectively, while M_2 prevents conduction through the amplifier. The amplification phase is then initiated when the Enable signal pulses high, disabling the reset transistors and closing M_2. As charge is carried through M_{in} and M_2, the voltage on V_{cap} rises, while M_{in} slowly enters the sub-threshold region of operation with exponentially diminishing current flow. After sufficient time, V_{cap} rises to a voltage that reflects V_{in}, and carries a DC level and a small AC signal. Due to exponentially decaying current through M_{in} and hence a slowing transition on V_{cap}, the signal is only partially applied on V_{cap} by the factor of α (<1). The signal charge generated by $V_{cap,ac}$ on C_s transfers to C_{out} to form a voltage where the ratio of C_s and C_{out} determines the voltage gain. The circuit returns to the reset state once the cycle of discrete amplification completes. On a large scale, the amplification time (T_{amp}) affects amplifier gain and noise performance. However, these parameters are tolerant to small noise (jitter) in T_{amp} due to the decaying value of M_{in} current at the end of T_{amp}.

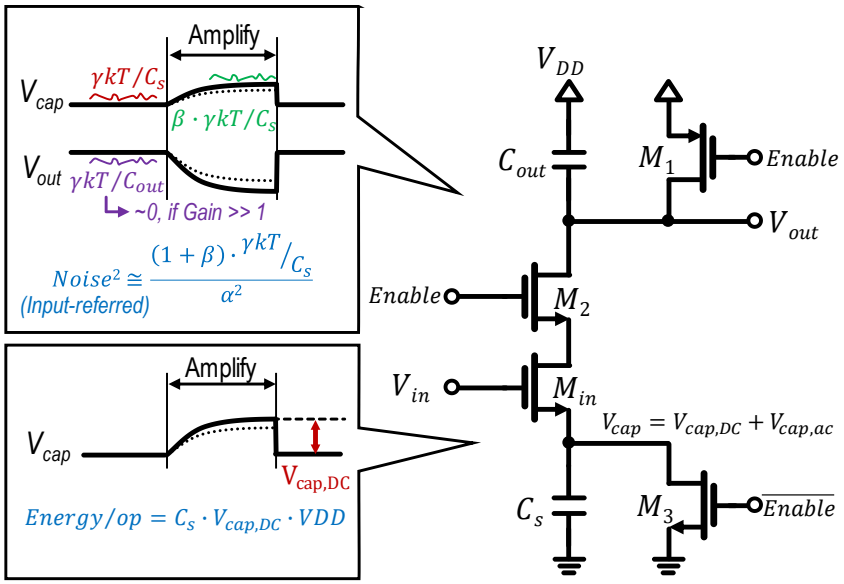


Figure 47. Noise and energy of the proposed Q-ccAmp

At the end of the amplification cycle, the noise appearing at the output contains four significant factors (Figure 47): 1) thermal noise incurred during reset of C_{out} by M_1, 2) thermal noise incurred during reset of C_s by M_3, 3) thermal noise on V_{cap} at the end of amplification from M_{in}, and 4) flicker noise sampled on V_{cap} from M_{in}. However, the impact of these noise sources on final input referred noise is attenuated due to several factors. First, assuming the gain of the amplifier is much larger than 1, the reset noise of C_{out} quickly diminishes as its input-referred contribution is divided by the amplifier gain. Also, the flicker noise from M_{in} is mitigated by the periodic reset of the amplifier, which resets the trapped states within M_{in}, effectively suppressing the below $f_s = (T_{amp}+T_{reset})^{-1}$ portion of the flicker noise energy. Finally, the thermal noise from M_{in} at the end of the amplification cycle is subject to a soft-reset operation, which halves its contribution if provided sufficient time. Assuming flicker noise and reset noise of C_{out} are small, the amplifier input-referred noise can be written as

$$Noise^2 \cong \frac{(1+\beta)\cdot {}^{\gamma kT}/_{C_s}}{\alpha^2}$$

Equation 17

where α is the gain from V_{in} to V_{cap} (≤1) and β is the soft-reset factor (≤1). Energy per amplifier operation, on the other hand, is determined by the amount of charge conducted through V_{out} and V_{cap} and can be formulated simply by the voltage swing on capacitor C_s.

$$Energy/op = C_s \cdot V_{cap,DC} \cdot V_{DD}$$

Equation 18

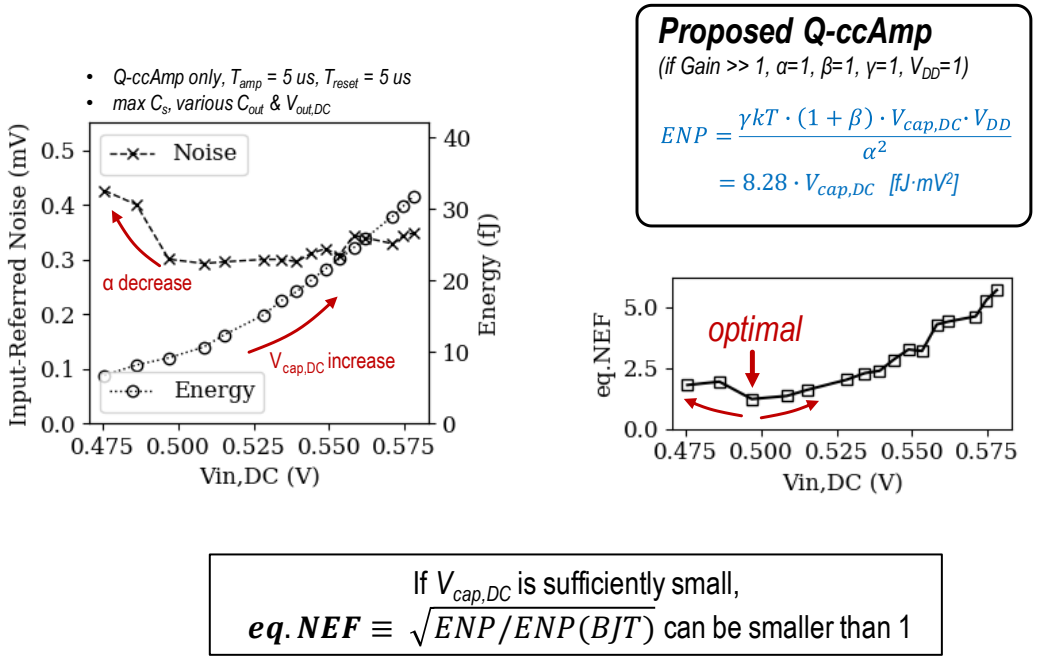


Figure 48. By controlling $V_{cap,DC}$, the discrete-time equivalent NEF (eq. NEF) can theoretically be made smaller than 1. Measurement confirms eq. NEF improvement and optimal point is identified

We use ENP as a cross-design measure of energy efficiency. For a continuous-time ideal BJT amplifier, an ENP of 0.68•V_{DD} $fJ{\cdot}mV^2$ is formulated by normalizing the continuous-time amplifier operation to 2πτ of settling time per discrete time operation as follows.

$$Noise^2(BJT) = BW \cdot \frac{\pi}{2} \cdot \frac{4kT \cdot U_T}{I_c}$$ *Equation 19*

$$Energy/op(BJT) = I_c \cdot VDD \cdot 2\pi\tau = I_c \cdot VDD \cdot \frac{1}{BW}$$ *Equation 20*

$$ENP(BJT) = \frac{\pi}{2} \cdot 4kT \cdot U_T \cdot VDD \approx 0.68 \cdot VDD$$ *Equation 21*

From this, an eq. NEF for the pre-amplifier is found by taking the ratio of the two ENPs then taking the square-root (Figure 48). Note that term $V_{cap,DC}$ appears in the expression for Energy/op, and hence also in ENP and eq. NEF, as shown in below.

$$eq.\ NEF\ (proposed) = \sqrt{\frac{ENP(proposed)}{ENP(BJT)}} = \sqrt{\frac{\gamma \cdot (1+\beta) \cdot V_{cap,DC}}{\alpha^2 \cdot 2\pi \cdot U_T}}$$ *Equation 22*

As a result, we can achieve eq. NEF < 1 for the proposed amplifier if $V_{cap,DC}$ is sufficiently lowered. However, a number of other amplifier parameters are correlated to $V_{cap,DC}$, including α and β. In particular, as $V_{cap,DC}$ reduces, M_{in} operates more extensively in the subthreshold regime, increasing the settling time of V_{cap} and reducing α under a fixed T_{amp}. This creates a trade-off where eq. NEF reaches a minimum at an optimal $V_{cap,DC}$. Finally, the capacitance C_s does not directly affect the eq. NEF since its noise and energy effects cancel out, however, it has an indirect impact through modulating the settling speed, thus affecting α.

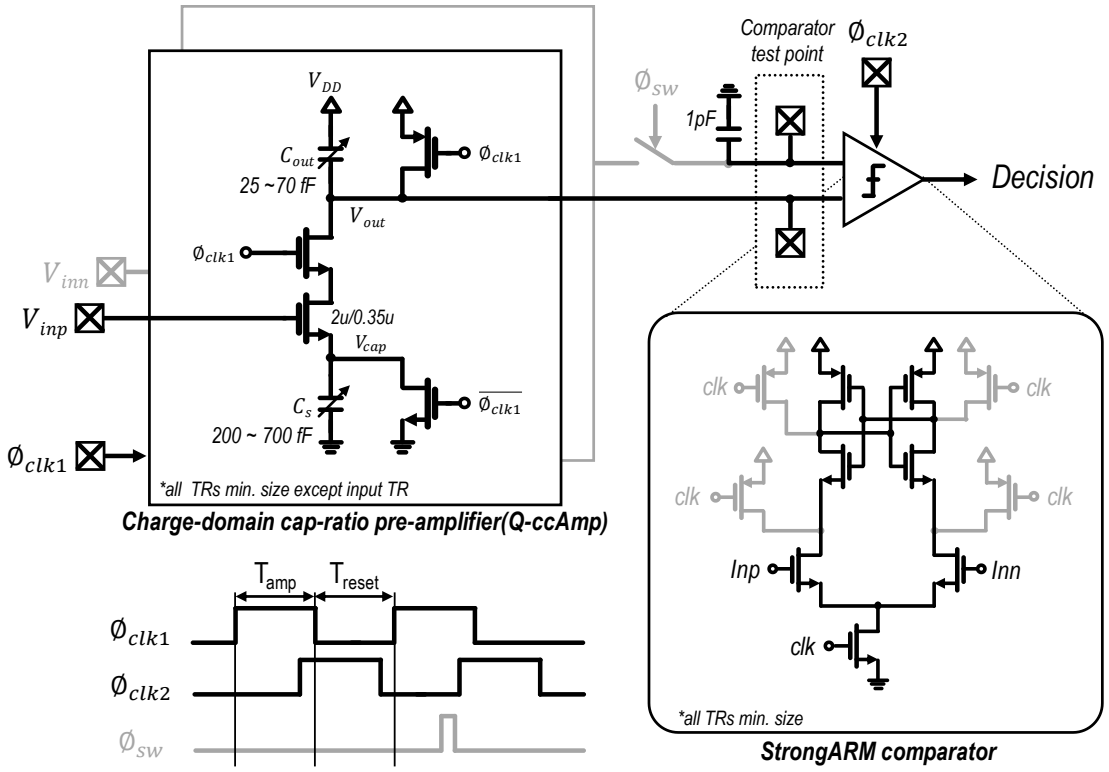


Figure 49. Test circuit configuration of proposed Q-ccAmp. Conventional StrongARM comparator is attached after Q-ccAmp to examine input-referred noise improvement

Figure 49 shows the test circuit for the Q-ccAmp. The structure contains a simple StrongARM comparator as a reference design, which is characterized with and without the pre-amplifier. The capacitors in Q-ccAmp (C_s, C_{out}) are MoM type and can be tuned from 200 to 700 *fF* and 25 to 70 *fF*, respectively, to study amplifier behavior (i.e., noise, energy, gain) across capacitor sizes. The test structure also contains a second instance of Q-ccAmp that can be activated at a decimated rate to generate a replica bias on a large capacitor (1 *pF*) for the differential comparator.

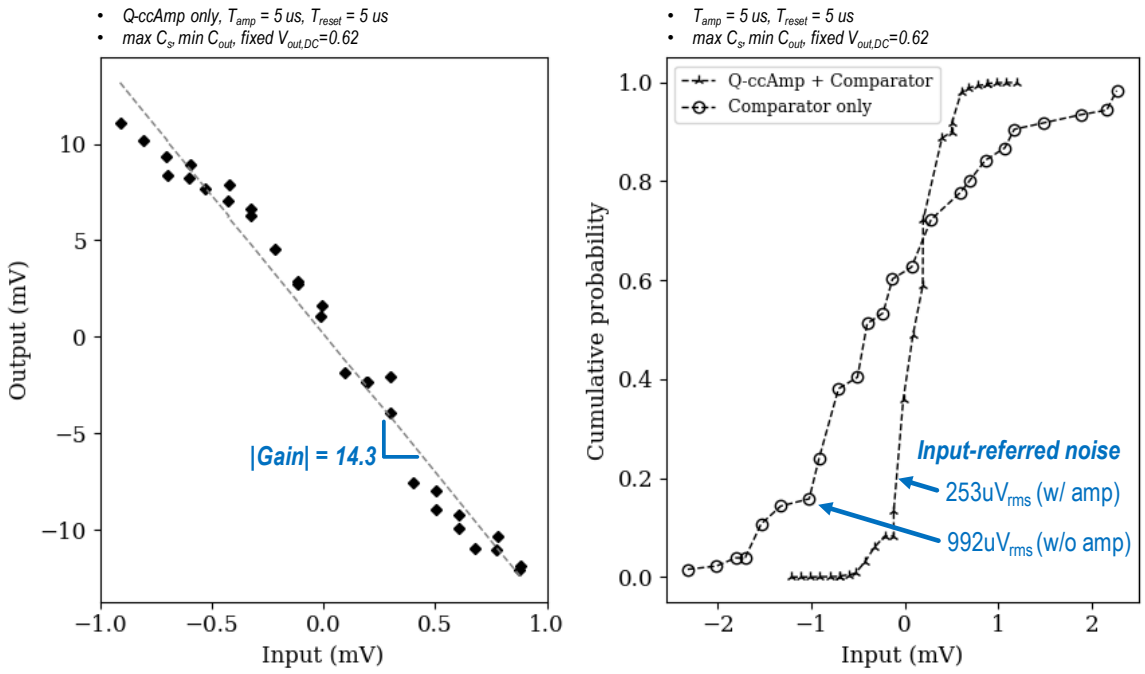


Figure 50. Measured gain of Q-ccAmp and input referred noise comparison w/ and w/o Q-ccAmp. Input-referred noise is measured by observing the probability of finding logic-high decision at given input voltage (from >10k decisions)

As shown in Figure 50, the Q-ccAmp is capable of providing a voltage gain of 14.3 when run with highest C_s setting at 100 *kHz*, and the input-referred noise of the combined comparator (Q-ccAmp + StrongARM comparator) is improved by 3.9× (992 uV_{rms} vs. 253 uV_{rms}) compared with the StrongARM comparator alone. With increasing C_s, the amplifier gain increases (Figure 51); however, the value starts to saturate at higher C_s values due to diminishing α. The gain also tends to drop with increasing frequency due to signal loss from insufficient settling on V_{cap}, which lowers α and impacts input-referred noise negatively. The best eq. NEF design point for Q-ccAmp uses large C_s and a sufficiently slow operating speed to allow for maximum signal transfer from V_{in} to V_{cap}.

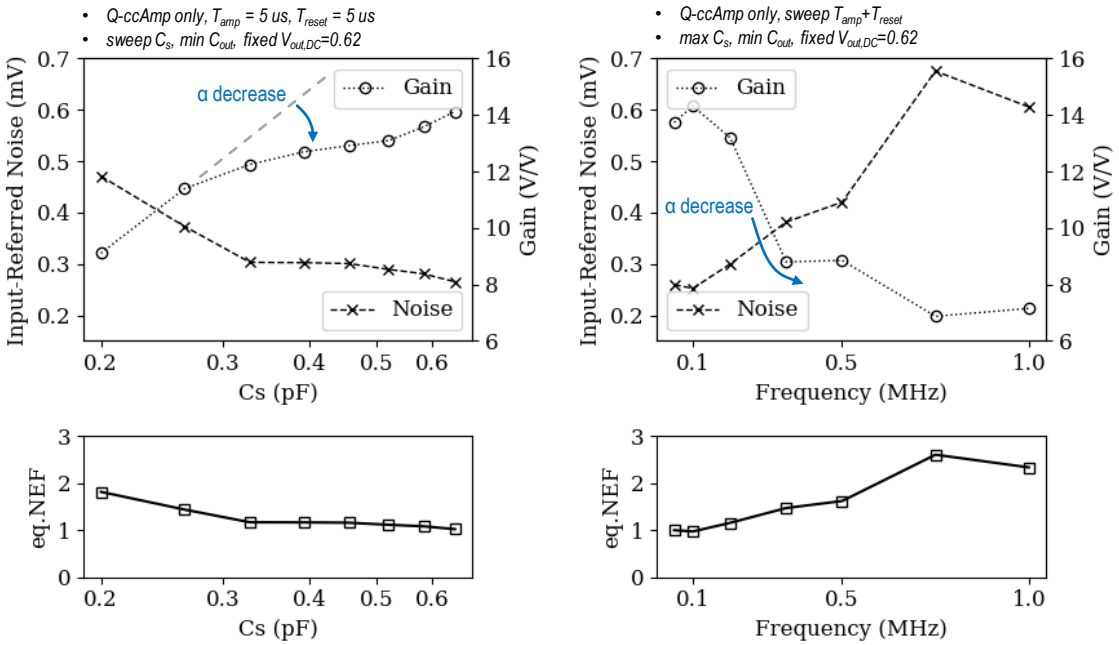


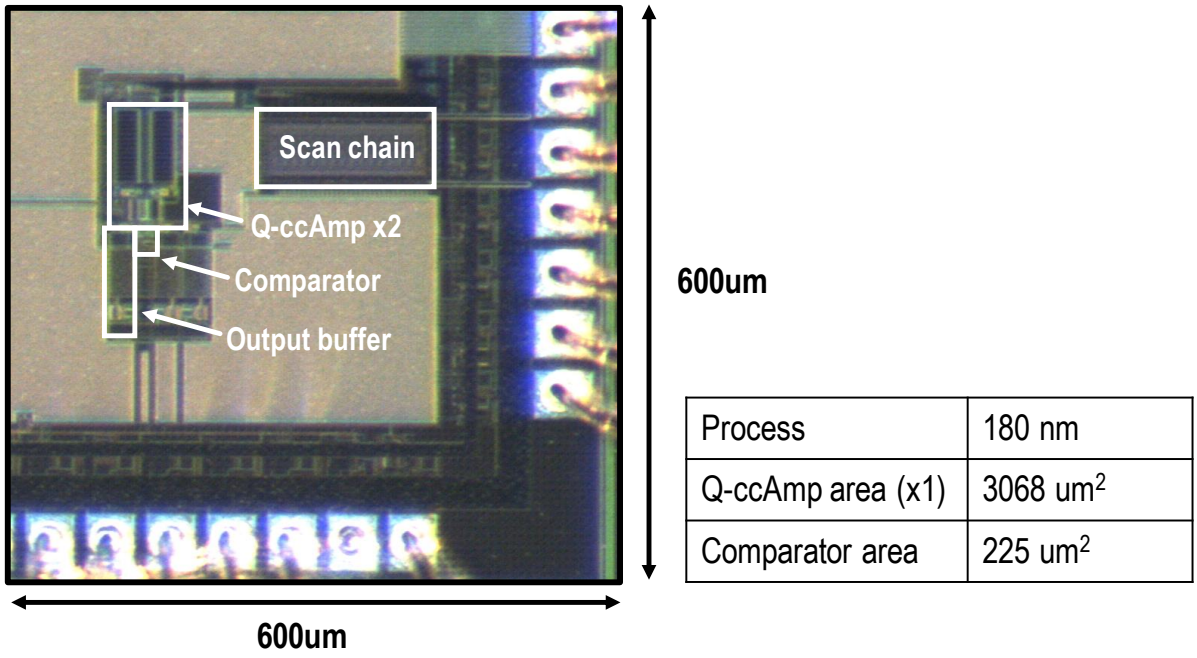
Figure 51. Measurement of gain, input-referred noise, and resultant eq. NEF over C_s and sampling frequency, $f_s=(T_{amp}+T_{reset})^{-1}$

Table 4 compares this work to other recent and well-known comparators. When tested in conjunction with a relatively high noise StrongARM comparator, the Q-ccAmp reduces the combined eq. NEF from 6.32 to 1.98 (3.19× improvement) with only 33.5% energy increase (measured without replica path). The combined comparator eq. NEF can be further improved by allocating more energy to the Q-ccAmp via larger C_s or by porting to a more advanced technology to reduce comparator energy. The proposed amplifier eq. NEF is the best among those listed in the table and could also be combined with the other listed works as a pre-amplifier to further improve their performance. Figure 52 shows the chip photograph. A single instance of Q-ccAmp requires 3068 um^2 of area in 180nm CMOS.

Table 4. Comparison of Q-ccAmp to other recent and well-known comparators

	This work			**Shim 2017 JSSC [1]**	**Lee 2011 JSSC [2]**	**Miyahara 2008 JSSC**
Process	180nm			40nm	180nm	90nm
Type	Q-ccAmp	Q-ccAmp + comparator	Comparator	Edge pursuit comparator	Time domain comparator	Pre-amp + comparator
Supply [V]	1.0			0.9	0.6	1.0
Frequency	100 KHz			300 KHz	1.2 MHz	1 GHz
Preamp gain [V/V]	-14.3		-	-	-	-
Energy/op [fJ]	**10.1**	40.2	30.1	10000*4	130	20
Input noise [uV_{rms}]	**242***1	252*2	992*3	15	65	660
ENP [$fJ \cdot mV^2$]	**0.59**	2.55	29.6	2.25	0.55	8.71
eq. NEF	**0.93**	1.94	6.60	1.92	1.16	3.58

*1 Comparator noise adjust : sqrt(TotalNoise^2-(1/Gain)^2·CompNoise^2)
*2 TotalNoise *3 CompNoise
*4 Read from plot



Process	180 nm
Q-ccAmp area (x1)	3068 um^2
Comparator area	225 um^2

Figure 52. Chip photograph of Q-ccAmp prototype

CHAPTER 5.
CONCLUSION AND FUTURE WORK

In this dissertation, novel charge-domain circuit techniques were introduced, and their unique properties were outlined. The techniques are based on a circuit referred to as a charge-injection cell, which was developed to create a repeatable and accurate amount of charge output. The charge-injection cell was applied to different analog/mixed-signal circuits to enhance their resource efficiency, and the mechanism by which they were improved was discussed.

Since the charge-injection cell was originally developed for the purpose of building a DAC, the dissertation first identified its value as an accurate charge/voltage source. The jitter-rejecting property of the charge-injection cell was discussed related to the diminishing conduction profile of its inject operation, and an important feature of reuse was stated from understanding its reset operation. Then, the charge-injection was studied from the perspective of noise, mismatch, and output impedance, and the relevant design points for optimizing each aspect were outlined.

The dissertation then discusses how the charge-injection cell can be put together to form an ADC. A simple exemplary design was studied through a model to understand its size, speed, and mismatch properties relative to capacitor array-based design. Based on the model analysis of its size and speed at varying degrees of reuse and bit-depth, an optimal design point was identified. The model predicts that the charge-injection cell-based ADCs can outperform capacitor array-based designs with respect to IRD by more than 10× at 10b. The projected IRD distinguishes the charge-injection cell-based design from the conventional capacitor array-based structure and certifies its potential to yield a highly resource-efficient ADC design.

Expanding on charge-injection cell-based ADCs, an energy-efficient image sensor design was discussed. In this design, the charge-injection cell is merged with a capacitor array structure to enhance the energy-efficiency of the SAR ADC operation. The sensor also packs other energy/area-saving features, such as motion detection mode, with n-way side-step mapping. Owing to the flexibility of charge-injection cell-based ADCs, the sensor also features multiple sampling functions to lower its readout noise from 226 to 106 uV_{rms}, again confirming the benefits of using a charge-domain circuit technique. The designed sensor and the column-parallel ADCs exhibit excellent energy efficiency, touting 14.4 uV·nJ ADC FoM (ADC+pixel only) and 37.9 uV·nJ when including the fully-programmable controller. The motion detection mode can be run with 1.7 uJ/frame while preserving 10b accuracy.

As a spin-off from the charge-injection cell structure, an energy-efficient charge-domain pre-amplifier was also developed. The pre-amplifier structure is almost identical to the charge-injection cell but with a different capacitor ratio at the top and bottom of the cell to achieve voltage gain. As it inherits the same noise performance as the charge-injection cell, and the energy consumption is semi-orthogonally defined by the swing on the capacitor nodes, it was projected that an optimum noise-efficiency factor could be found by lowering the swing of the circuit until declining voltage gain bounds it to a certain lower limit. The circuit was implemented in 180-nm CMOS, and it exhibits 0.93 discrete-time equivalent NEF, which is the best reported in its domain, again confirming the highly energy-efficient aspect of charge-domain circuit techniques.

Combining the two works, a hybrid two-step SAR ADC that has both high area-efficiency and energy-efficiency can be proposed, as shown in Figure 53.

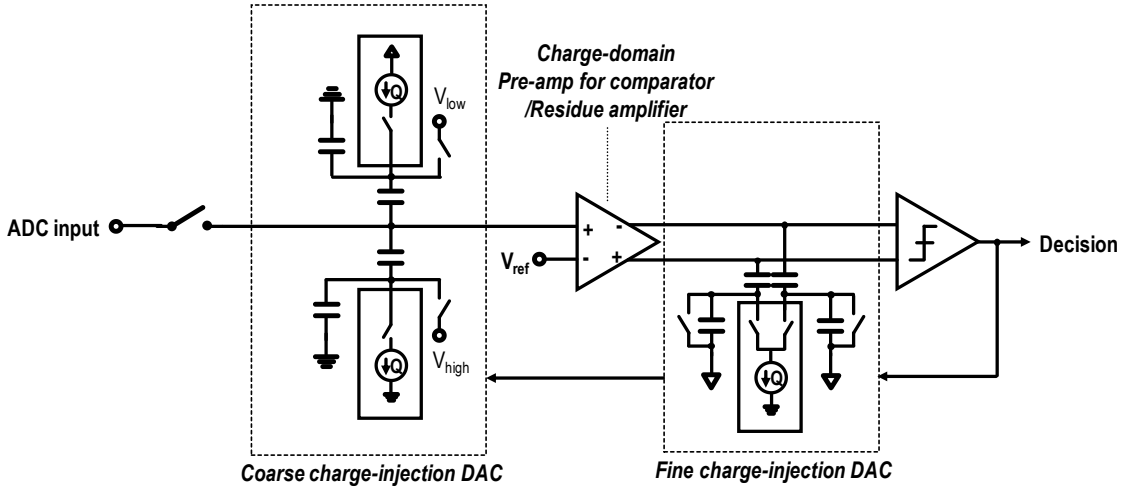


Figure 53. A hybrid two-step SAR ADC with using charge-domain comparator as residue amplifier

By heavily exploiting the reuse functionality of charge-injection cell-based ADCs, the DAC part of the ADC could be made extremely small, including as few as one charge-injection cell per each path, which would also be beneficial to reducing the energy overhead of the ADC along with area. The coarse-fine structure and the residue amplification will provide an extra divisor to the energy overhead, reducing the operational energy of the DAC to an insignificant value. The comparator operation will be highly energy efficient with the use of a charge-domain pre-amplifier. Altogether, the ADC will achieve both aspects of resource-efficiency, benefiting from the unique operating principles of charge-domain circuit techniques.

Bibliography

[1] B. Murmann, "ADC Performance Survey 1997-2017." [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

[2] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. A. M. Klumperink, and B. Nauta, "A 10-bit Charge-Redistribution ADC Consuming 1.9 uW at 1 MS/s," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1007–1015, May 2010.

[3] S. Jeong *et al.*, "A 120nW 8b sub-ranging SAR ADC with signal-dependent charge recycling for biomedical applications," in *2015 Symposium on VLSI Circuits (VLSI Circuits)*, 2015, pp. C60–C61.

[4] S. Jeong *et al.*, "21.6 A 12nW always-on acoustic sensing and object recognition microsystem using frequency-domain feature extraction and SVM classification," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, 2017, pp. 362–363.

[5] M. Shim *et al.*, "An oscillator collapse-based comparator with application in a 74.1dB SNDR, 20KS/s 15b SAR ADC," in *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, 2016, pp. 1–2.

[6] Y. Chae and G. Han, "A Low Power Sigma-Delta Modulator Using Class-C Inverter," in *2007 IEEE Symposium on VLSI Circuits*, 2007, pp. 240–241.

[7] H. Y. Tai, Y. S. Hu, H. W. Chen, and H. S. Chen, "11.2 A 0.85fJ/conversion-step 10b 200kS/s subranging SAR ADC in 40nm CMOS," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 196–197.

[8] F. M. Yaul and A. P. Chandrakasan, "11.3 A 10b 0.6nW SAR ADC with data-dependent energy savings using LSB-first successive approximation," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 198–199.

[9] K. Doris, E. Janssen, C. Nani, A. Zanikopoulos, and G. van der Weide, "A 480 mW 2.6 GS/s 10b Time-Interleaved ADC With 48.5 dB SNDR up to Nyquist in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2821–2833, Dec. 2011.

[10] N. L. Dortz *et al.*, "22.5 A 1.62GS/s time-interleaved SAR ADC with digital background mismatch calibration achieving interleaving spurs below 70dBFS," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 386–388.

[11] H. K. Hong *et al.*, "An 8.6 ENOB 900MS/s time-interleaved 2b/cycle SAR ADC with a 1b/cycle reconfiguration for resolution enhancement," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 470–471.

[12] B. Razavi, "Design Considerations for Interleaved ADCs," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1806–1817, Aug. 2013.

[13] S. L. Tual, P. N. Singh, C. Curis, and P. Dautriche, "22.3 A 20GHz-BW 6b 10GS/s 32mW time-interleaved SAR ADC with Master T&H in 28nm UTBB FDSOI technology," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 382–383.

[14] K. D. Choo, J. Bell, and M. P. Flynn, "27.3 Area-efficient 1GS/s 6b SAR ADC with charge-injection-cell-based DAC," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 460–461.

[15] C. C. Liu, "27.4 A 0.35mW 12b 100MS/s SAR-assisted digital slope ADC in 28nm CMOS," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 462–463.

[16] J. W. Jung and B. Razavi, "A 25 Gb/s 5.8 mW CMOS Equalizer," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 515–526, Feb. 2015.

[17] S. H. W. Chiang, H. Sun, and B. Razavi, "A 10-Bit 800-MHz 19-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 935–949, Apr. 2014.

[18] A. P. van der Wel, E. A. M. Klumperink, L. K. J. Vandamme, and B. Nauta, "Modeling random telegraph noise under switched bias conditions using cyclostationary RTS noise," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1378–1384, May 2003.

[19] Z. Celik-Butler and N. V. Amarasinghe, "Chapter 9. Random Telegraph Signals in Deep Submicron Metal-Oxide-Semiconductor Field-Effect Transistors," in *Noise and Fluctuations Control in Electronic Devices*, American Scientific Publishers, 2002, pp. 187–200.

[20] N. Teranishi, "Analysis of Subthreshold Current Reset Noise in Image Sensors," *Sensors*, vol. 16, no. 5, May 2016.

[21] C.-C. Liu, Y.-T. Huang, G.-Y. Huang, S.-J. Chang, C.-M. Huang, and C.-H. Huang, "A 6-bit 220-MS/s time-interleaving SAR ADC in 0.18-um digital CMOS process," in *2009 International Symposium on VLSI Design, Automation and Test*, 2009, pp. 215–218.

[22] P. Harpe, "A 0.0013mm2 10b 10MS/s SAR ADC with a 0.0048mm2 42dB-rejection passive FIR filter," in *2018 IEEE Custom Integrated Circuits Conference (CICC)*, 2018, pp. 1–4.

[23] C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.

[24] Y. Yoon and N. Sun, “A 6-bit 0.81mW 700-MS/s SAR ADC with sparkle-code correction, resolution enhancement, and background window width calibration,” in *2018 IEEE Custom Integrated Circuits Conference (CICC)*, 2018, pp. 1–4.

[25] O. Kumagai *et al.*, “A 1/4-inch 3.9Mpixel low-power event-driven back-illuminated stacked CMOS image sensor,” in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 86–88.

[26] G. Kim *et al.*, “A millimeter-scale wireless imaging system with continuous motion detection and energy harvesting,” in *2014 Symposium on VLSI Circuits Digest of Technical Papers*, 2014, pp. 1–2.

[27] S. Lee, S. Park, H. Park, and J. Sim, “A 21 fJ/Conversion-Step 100 kS/s 10-bit ADC With a Low-Noise Time-Domain Comparator for Low-Power Sensor Interface,” *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 651–659, Mar. 2011.

[28] Y.-P. Chen, D. Blaauw, and D. Sylvester, “A 266nW multi-chopper amplifier with 1.38 noise efficiency factor for neural signal recording,” in *2014 Symposium on VLSI Circuits Digest of Technical Papers*, 2014, pp. 1–2.

[29] D. Han, Y. Zheng, R. Rajkumar, G. Dawe, and M. Je, “A 0.45V 100-channel neural-recording IC with sub-uW/channel consumption in 0.18 nm CMOS,” in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 290–291.

[30] K. Kotani, T. Shibata, and T. Ohmi, “CMOS charge-transfer preamplifier for offset-fluctuation cancellation in low-power A/D converters,” *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 762–769, May 1998.

[31] C. H. Chan, Y. Zhu, S. W. Sin, U. Seng-Pan, and R. P. Martins, “26.5 A 5.5mW 6b 5GS/S 4x-lnterleaved 3b/cycle SAR ADC in 65nm CMOS,” in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, 2015, pp. 1–3.

[32] L. Kull *et al.*, “A 3.1mW 8b 1.2GS/s single-channel asynchronous SAR ADC with alternate comparators for enhanced speed in 32nm digital SOI CMOS,” in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 468–469.

[33] C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, “A 0.92mW 10-bit 50-MS/s SAR ADC in 0.13 um CMOS process,” in *2009 Symposium on VLSI Circuits*, 2009, pp. 236–237.

[34] X. Gao, E. A. M. Klumperink, M. Bohsali, and B. Nauta, “A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is Not Multiplied by N-square,” *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3253–3263, Dec. 2009.

[35] Z. Z. Chen *et al.*, “14.9 Sub-sampling all-digital fractional-N frequency synthesizer with -111dBc/Hz in-band phase noise and an FOM of -242dB,” in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, 2015, pp. 1–3.

[36] X. Gao, E. A. M. Klumperink, G. Socci, M. Bohsali, and B. Nauta, "Spur Reduction Techniques for Phase-Locked Loops Exploiting A Sub-Sampling Phase Detector," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1809–1821, Sep. 2010.

[37] T. Siriburanon *et al.*, "A 60-GHz sub-sampling frequency synthesizer using sub-harmonic injection-locked quadrature oscillators," in *2014 IEEE Radio Frequency Integrated Circuits Symposium*, 2014, pp. 105–108.

[38] X. Gao, E. A. M. Klumperink, G. Socci, M. Bohsali, and B. Nauta, "Spur-reduction techniques for PLLs using sub-sampling phase detection," in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2010, pp. 474–475.

[39] V. Szortyka, Q. Shi, K. Raczkowski, B. Parvais, M. Kuijk, and P. Wambacq, "21.4 A 42mW 230fs-jitter sub-sampling 60GHz PLL in 40nm CMOS," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 366–367.

[40] X. Gao, E. A. M. Klumperink, M. Bohsali, and B. Nauta, "A 2.2GHz 7.6mW sub-sampling PLL with 126dBc/Hz in-band phase noise and 0.15psrms jitter in 0.18 nm CMOS," in *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, 2009, pp. 392-393,393a.

[41] A. T. Narayanan *et al.*, "A Fractional-N Sub-Sampling PLL using a Pipelined Phase-Interpolator With an FoM of -250 #xa0;dB," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1630–1640, Jul. 2016.

[42] T. Siriburanon *et al.*, "A 2.2 GHz -242 dB-FOM 4.2 mW ADC-PLL Using Digital Sub-Sampling Architecture," *IEEE J. Solid-State Circuits*, vol. 51, no. 6, pp. 1385–1397, Jun. 2016.

[43] X. Gao *et al.*, "9.6 A 2.7-to-4.3GHz, 0.16psrms-jitter, 246.8dB-FOM, digital fractional-N sampling PLL in 28nm CMOS," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 174–175.

[44] X. Gao, E. Klumperink, and B. Nauta, "Sub-sampling PLL techniques," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, 2015, pp. 1–8.

[45] P. Harpe, H. Gao, R. van Dommele, E. Cantatore, and A. van Roermund, "21.2 A 3nW signal-acquisition IC integrating an amplifier with 2.1 NEF and a 1.5fJ/conv-step ADC," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, 2015, pp. 1–3.

[46] L. Shen, N. Lu, and N. Sun, "A 1V 0.25uW inverter-stacking amplifier with 1.07 noise efficiency factor," in *2017 Symposium on VLSI Circuits*, 2017, pp. C140–C141.

[47] J. W. Jung and B. Razavi, "2.4 A 25Gb/s 5.8mW CMOS equalizer," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 44–45.

[48] H. Wei, P. Zhang, B. D. Sahoo, and B. Razavi, “An 8 Bit 4 GS/s 120 mW CMOS ADC,” *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1751–1761, Aug. 2014.

[49] C. C. Liu *et al.*, “A 10b 100MS/s 1.13mW SAR ADC with binary-scaled error compensation,” in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2010, pp. 386–387.

[50] J. A. Fredenburg and M. P. Flynn, “A 90-MS/s 11-MHz-Bandwidth 62-dB SNDR Noise-Shaping SAR ADC,” *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2898–2904, Dec. 2012.

[51] B. Razavi, “A Tale of Two ADCs: Pipelined Versus SAR,” *IEEE Solid-State Circuits Mag.*, vol. 7, no. 3, pp. 38–46, Summer 2015.

[52] J. H. Park, S. Aoyama, T. Watanabe, K. Isobe, and S. Kawahito, “A High-Speed Low-Noise CMOS Image Sensor With 13-b Column-Parallel Single-Ended Cyclic ADCs,” *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2414–2422, Nov. 2009.

[53] T. Watabe *et al.*, “A 33Mpixel 120fps CMOS image sensor using 12b column-parallel pipelined cyclic ADCs,” in *2012 IEEE International Solid-State Circuits Conference*, 2012, pp. 388–390.

[54] P. J. A. Harpe *et al.*, “A 26 uW 8 bit 10 MS/s Asynchronous SAR ADC for Low Energy Radios,” *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, Jul. 2011.

[55] C. C. Lee and M. P. Flynn, “A SAR-Assisted Two-Stage Pipeline ADC,” *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 859–869, Apr. 2011.

[56] P. Harpe, E. Cantatore, and A. v Roermund, “A 2.2/2.7fJ/conversion-step 10/12b 40kS/s SAR ADC with Data-Driven Noise Reduction,” in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 270–271.

[57] J. h Kim *et al.*, “A 14b extended counting ADC implemented in a 24Mpixel APS-C CMOS image sensor,” in *2012 IEEE International Solid-State Circuits Conference*, 2012, pp. 390–392.

[58] S. Lim, J. Lee, D. Kim, and G. Han, “A High-Speed CMOS Image Sensor With Column-Parallel Two-Step Single-Slope ADCs,” *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 393–398, Mar. 2009.

[59] Y. Chae *et al.*, “A 2.1 M Pixels, 120 Frame/s CMOS Image Sensor With Column-Parallel Delta Sigma ADC Architecture,” *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 236–247, Jan. 2011.

[60] S. Lim *et al.*, “A 240-frames/s 2.1-Mpixel CMOS Image Sensor With Column-Shared Cyclic ADCs,” *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2073–2083, Sep. 2011.

[61] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.

[62] G. Kim *et al.*, "A 467nW CMOS visual motion sensor with temporal averaging and pixel aggregation," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 480–481.

[63] S. Ji, J. Pu, B. C. Lim, and M. Horowitz, "A 220pJ/pixel/frame CMOS image sensor with partial settling readout architecture," in *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, 2016, pp. 1–2.

[64] M. Shim *et al.*, "Edge pursuit comparator with application in a 74.1dB SNDR, 20KS/s 15b SAR ADC," in *2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2018, pp. 295–296.

[65] M. Shim *et al.*, "Edge-Pursuit Comparator: An Energy-Scalable Oscillator Collapse-Based Comparator With Application in a 74.1 dB SNDR and 20 kS/s 15 b SAR ADC," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1077–1090, Apr. 2017.

[66] M. Shim *et al.*, "Edge pursuit comparator with application in a 74.1dB SNDR, 20KS/s 15b SAR ADC," in *2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2018, pp. 295–296.

[67] M. S. J. Steyaert and W. M. C. Sansen, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," *IEEE J. Solid-State Circuits*, vol. 22, no. 6, pp. 1163–1168, Dec. 1987.

[68] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *2008 IEEE Asian Solid-State Circuits Conference*, 2008, pp. 269–272.

[69] C. Lin, C. Wong, C. Hsu, Y. Wei, and T. Lee, "A 200-MS/s Phase-Detector-Based Comparator With 400-$\mu\textV_\mathrmrms$Noise," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 63, no. 9, pp. 813–817, Sep. 2016.

[70] S. Iguchi, T. Sakurai, and M. Takamiya, "5.7 A 39.25MHz 278dB-FOM 19µW LDO-free stacked-amplifier crystal oscillator (SAXO) operating at I/O voltage," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 100–101.

[71] F. M. Yaul and A. P. Chandrakasan, "A sub-µW 36nV/√Hz chopper amplifier for sensors using a noise-efficient inverter-based 0.2V-supply input stage," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 94–95.

[72] C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "A 92dB dynamic range sub-µVrms-noise 0.8µW/ch neural-recording ADC array with predictive digital autoranging," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 470–472.

[73] S. Hsieh and C. Hsieh, “A 0.44fJ/conversion-step 11b 600KS/s SAR ADC with semi-resting DAC,” in *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, 2016, pp. 1–2.

[74] J. Deguchi *et al.*, “A 187.5μVrms-read-noise 51mW 1.4Mpixel CMOS image sensor with PMOSCAP column CDS and 10b self-differential offset-cancelled pipeline SAR-ADC,” in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 494–495.

[75] M. Sakakibara *et al.*, “A back-illuminated global-shutter CMOS image sensor with pixel-parallel 14b subthreshold ADC,” in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 80–82.

[76] A. Suzuki *et al.*, “6.1 A 1/1.7-inch 20Mpixel Back-illuminated stacked CMOS image sensor for new imaging applications,” in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, 2015, pp. 1–3.

[77] O. Kumagai *et al.*, “A 1/4-inch 3.9Mpixel low-power event-driven back-illuminated stacked CMOS image sensor,” in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 86–88.

[78] S. Sukegawa *et al.*, “A 1/4-inch 8Mpixel back-illuminated stacked CMOS image sensor,” in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 484–485.

[79] T. Takahashi *et al.*, “A Stacked CMOS Image Sensor With Array-Parallel ADC Architecture,” *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1061–1070, Apr. 2018.

[80] Y. Oike and A. E. Gamal, “CMOS Image Sensor With Per-Column ΣΔ ADC and Programmable Compressed Sensing,” *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 318–328, Jan. 2013.