

ADVANCED FUNCTIONAL MATERIALS

Supporting Information

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Exploiting In Situ Redox and Diffusion of Molybdenum to
Enable Thin-Film Circuitry for Low-Cost Wireless Energy
Harvesting

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Exploiting In Situ Redox and Diffusion of Molybdenum to Enable Thin-Film Circuitry for Low-Cost Wireless Energy Harvesting*Youngbae Son and Rebecca L. Peterson****Section S1. XPS analysis methods**

The XPS curves were analyzed using CasaXPS software version 2.3.17PR1.1. The curve energies were calibrated using the C 1s peak at 284.5 eV as a reference, to account for charge compensation. O 1s, Zn 2p_{3/2}, Sn 3d_{5/2}, and Mo 3d peaks were then analyzed by fitting the measured data using Gaussian–Lorentzian curves with FWHM less than two, and a linear background. For the O 1s core level, measured curves were deconvoluted into three Gaussian–Lorentzian curves. The positions of the three deconvoluted peaks correspond to oxygen atoms in the fully oxidized surroundings (M–O), those in oxygen deficient regions (V_O), and those in H₂O and –OH groups (M–OH). These are located at 530.1 ± 0.1 eV, 531.1 ± 0.1 eV, and 532.1 ± 0.2 eV, respectively.^[1–4] Peaks for loosely bound oxygen (M–OH) around 532 eV were only observed at the surface (etch time = 0 s) and thus are not shown in Figure 2a. Next, Zn 2p_{3/2} and Sn 3d_{5/2} peaks were fitted using Gaussian-Lorentzian curves, centered at 1021.8 ± 0.2 eV and 486.2 ± 0.2 eV, respectively. Lastly, Mo 3d doublet core levels were also analyzed using six Gaussian-Lorentzian curves with the following constraints: (a) the 3d_{5/2} to 3d_{3/2} ratio is 3:2 and (b) the peaks which correspond to different oxidation state of Mo are located within the region listed in a table below.^[5–7]

Binding energy (eV)							
Mo ⁶⁺		Mo ⁵⁺		Mo ⁴⁺		Mo ⁰	
Mo 3d _{5/2}	Mo 3d _{3/2}	Mo 3d _{5/2}	Mo 3d _{3/2}	Mo 3d _{5/2}	Mo 3d _{3/2}	Mo 3d _{5/2}	Mo 3d _{3/2}
231.9 ± 0.2	234.8 ± 0.1	230.4 ± 0.4	233.4 ± 0.3	228.5 ± 0.2	231.5 ± 0.1	227.0 ± 0.1	230.3 ± 0.1

After the core-level spectra analysis, the area under each XPS peak was calculated by integration to estimate atomic compositions of Zn, Sn, M-O, V_O, M-OH, Mo⁶⁺, Mo⁵⁺, Mo⁴⁺, and Mo⁰. The conversion from area to atomic concentration was done using relative sensitivity factors taken from CasaXPS_kratos.lib, available online at <http://www.casaxps.com/kratos/>.

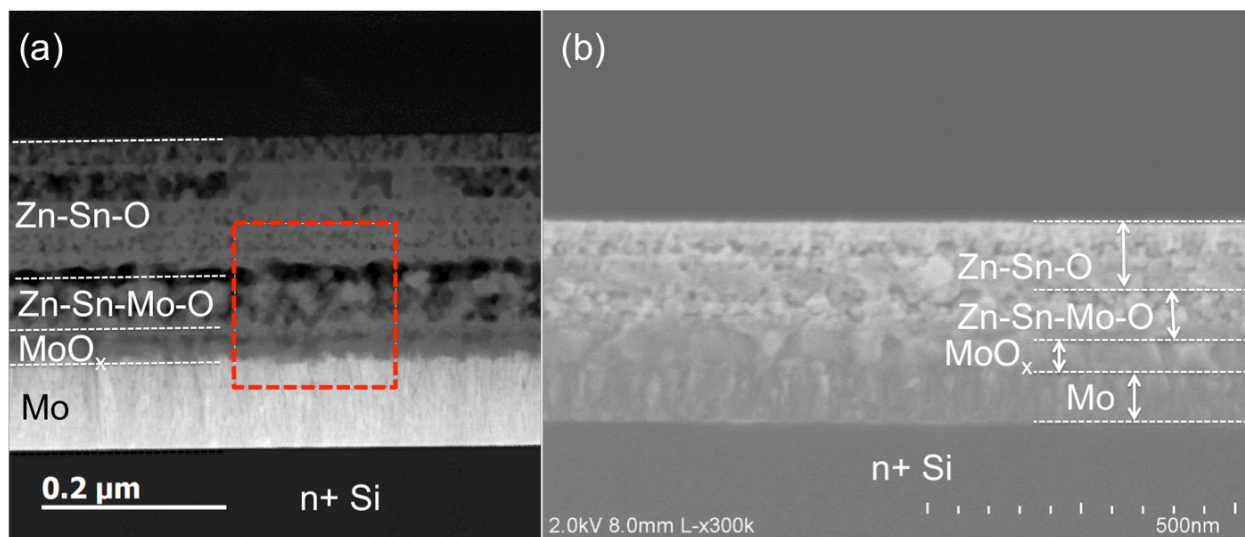


Figure S1. (a) Cross-sectional dark-field STEM image and (b) SEM image of Mo/a-Zn-Sn-O junction shown in Figure 2. The region where STEM image and EDS mapping shown in Figure 2c were carried is marked with red dashed line in (a). While the sample in (a) was prepared by the standard lift-out process using a focus ion beam system, the sample in (b) was prepared by scribing the substrate. In (b), SEM was measured using an Hitachi SU8000 In-line FE-SEM at an acceleration voltage of 2 kV. From both images, morphological differences in between layers are shown, where MoO_x layer exhibits smooth morphology compared to Zn-Sn-Mo-O layer. Both of the images reveal that Zn-Sn-Mo-O layer and Zn-Sn-O layer together have thickness of ~180 nm, which corresponds to depletion region thickness in Figure 1b.

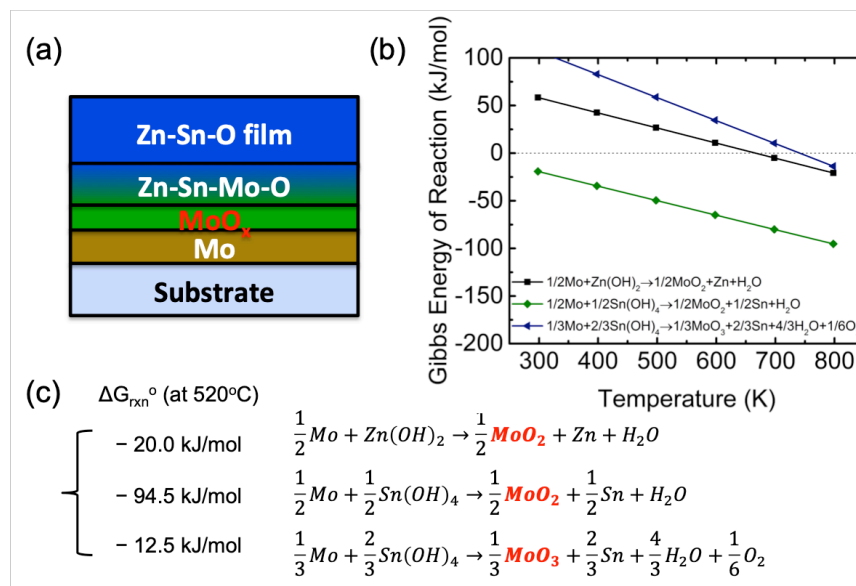


Figure S2. (a) Illustration of layers formed as a result of Zn-Sn-O solution process on top of Mo metal, highlighting MoO_x. (b) Standard Gibbs free energies (ΔG_{rxn}°) for various Mo oxidation routes during Zn-Sn-O deposition, including formation of MoO₃. Each reaction was normalized to one oxygen atom to allow comparison of ΔG_{rxn}° values, which are shown as a function of temperature in (b). (c) ΔG_{rxn}° values calculated at the annealing temperature for our solution process, 520 °C (793 K), which is required for high quality Zn-Sn-O film formation. The negative values of these ΔG_{rxn}° indicate that thermodynamics favor the formation of a MoO_x layer with various oxidation states (both MoO₂ and MoO₃).

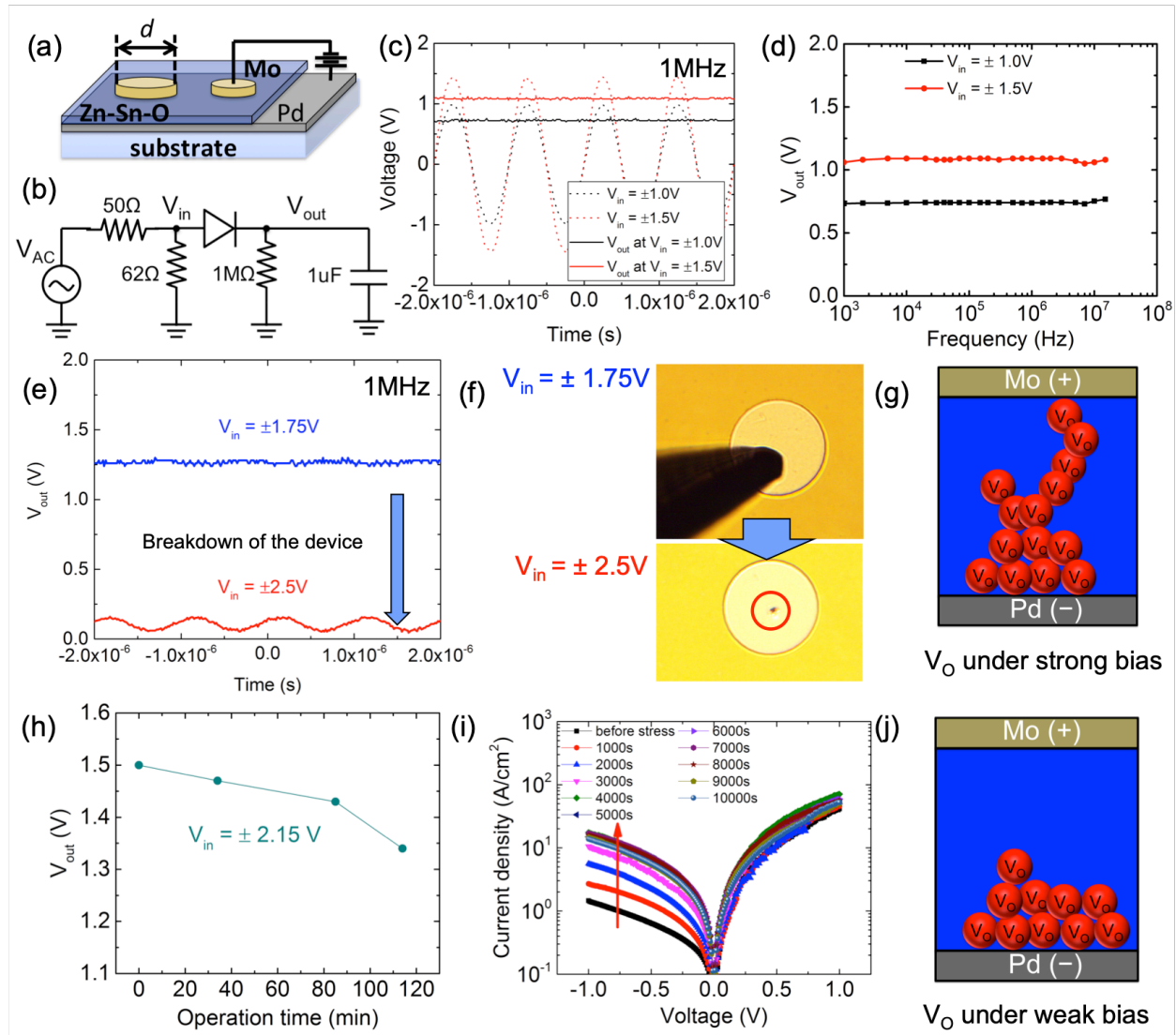


Figure S3. (a) Schematic of Pd:*a*-Zn-Sn-O diode structure. The devices described in this figure have $d = 100 \mu\text{m}$, the same size as Mo V-TFD. (b) Half-wave rectifier measurement setup, identical to Mo V-TFD shown in Figure 4a inset. (c) 1 MHz AC peak-to-peak input voltage (V_{in}) of 2.0 V and 3.0 V and corresponding DC output voltage (V_{out}). (d) Frequency response of V_{out} from 1 kHz to 15 MHz, showing no cut-off. (e) V_{out} measured for higher V_{in} of 3.5 V and 5.0 V and (f) microscope images of the diode showing pinhole defect (a point shown in red circle) when $V_{in} = 5.0$ V, caused by breakdown. Based on our observation of set-and-reset behavior after breakdown (often observed in memristors), the breakdown mechanism was concluded to be conductive filament formation by oxygen vacancy (V_O) migration within *a*-Zn-Sn-O, shown in (g). (h) The decrease of V_{out} over time. This is due to bias stress, which causes an increase in leakage current, as shown in (i). In (i), the diode was repeatedly tested after applying -2 V across the diode for 1000 s. The increase in leakage current is attributed to tunneling by oxygen vacancies (V_O) accumulating near the Schottky interface, as illustrated in (j).

Section S2. The effect of Zn-Sn-Mo-O layer on V-TFD on-current

Temperature varying J - V measurements were also performed for on-current at temperatures from 100 to 340 K. The measured on-current follow straight lines when plotted as $\ln J$ vs. $\ln V$. Such a power relationship between the on-current and voltage, $J \propto V^m$, indicates space-charge-limited current (SCLC) conduction mechanism. When the material is trap-free, the J - V relationship due to SCLC is $J = 9\varepsilon_s\varepsilon_o\mu_oV^2/8d^3$, known as Child's law.^[8] When a material has an exponential distribution of traps below the conduction band, the J - V relationship is modified to $J = \frac{qN_c\mu_o}{2} \left(\frac{2\varepsilon_s\varepsilon_o}{qg_{tc}kT_t} \right)^l \frac{V^{l+1}}{d^{2l+1}} f(l)$, where $f(l) = \left(\frac{1}{2} \right)^{l-1} \left(\frac{l}{l+1} \right)^l \left(\frac{2l+1}{l+1} \right)^{l+1}$ and $l=kT_t/kT$. More information about this charge transport mechanism can be found in the literature.^[9-12] Using this equation, the measured on-current from 100 K to 340 K was fitted using $\mu_o = 0.5$ - $1.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, $N_c = 6 \times 10^{16} \text{ cm}^{-3}$, $\varepsilon_s = 15$, $g_{tc} = 6.6 \times 10^{19} \text{ cm}^{-3}\text{eV}^{-1}$, $kT_t = 0.040 \text{ eV}$, $d = 80 \text{ nm}$. The measured data and the calculation shows good alignment across wide temperature range, as shown in Figure S4. Thus, we attribute the on-current of our V-TFD to SCLC with an exponential distribution of traps.

The SCLC mechanism is widely used to explain charge transport in materials with low free carrier density.^[13-18] The dominance of this mechanism as opposed to general Schottky emission indicates that the Zn-Sn-Mo-O layer, due to its lower conductivity, leads to bulk transport when the V-TFD is in the on-state. Within our Zn-Sn-Mo-O layer, Mo is doped into the Zn-Sn-O layer as shown in Figure 2a. Previously, Mo diffusion into ZnO and SnO₂ layers has been reported.^[19-21] Those studies report that Mo was easily incorporated into ZnO and SnO₂ layers due to the smaller ionic radius of Mo⁶⁺ compared to those of Zn²⁺ and Sn⁴⁺, but in all cases, excess Mo doping (> 2 at.%) led to conductivity loss in the ZnO and SnO₂ films. Such a reduction in conductivity can lead to SCLC-based conduction.

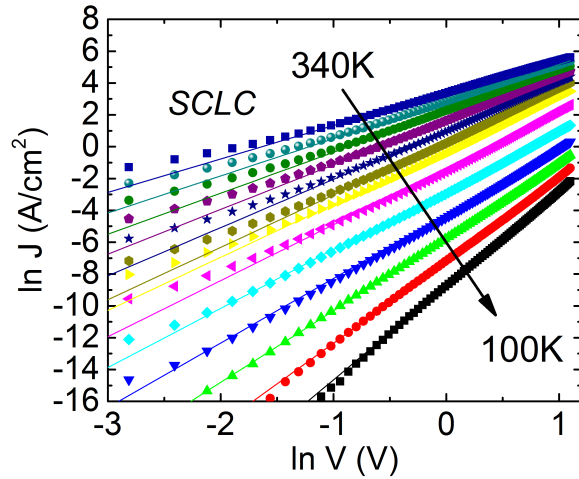


Figure S4. In addition to the temperature-dependent off-current shown in Figure 3b, the on-current was also analyzed with temperature-varying electrical measurements. The symbols refer to measured data, and the solid lines refer to the calculated results based on the SCLC model with exponential tail states.

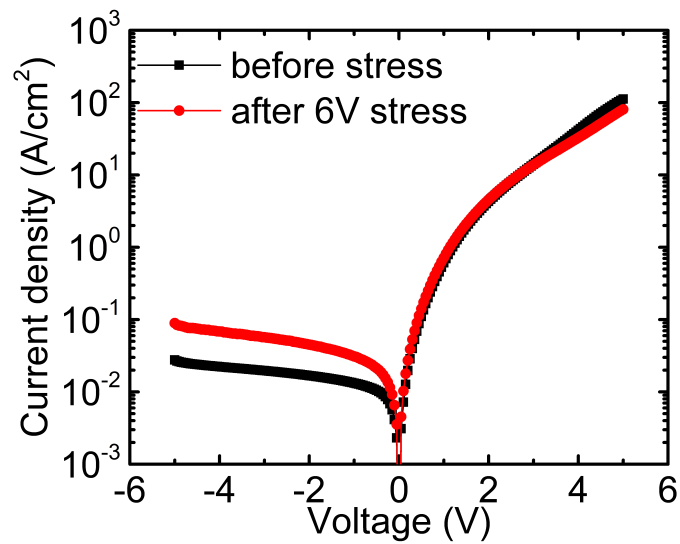


Figure S5. J - V measurements obtained from a Mo vertical thin-film diode before and after it was exposed to -6 V bias stress for 60,000 s, shown in Figure 3c. The change in J - V due to the stress is marginal.

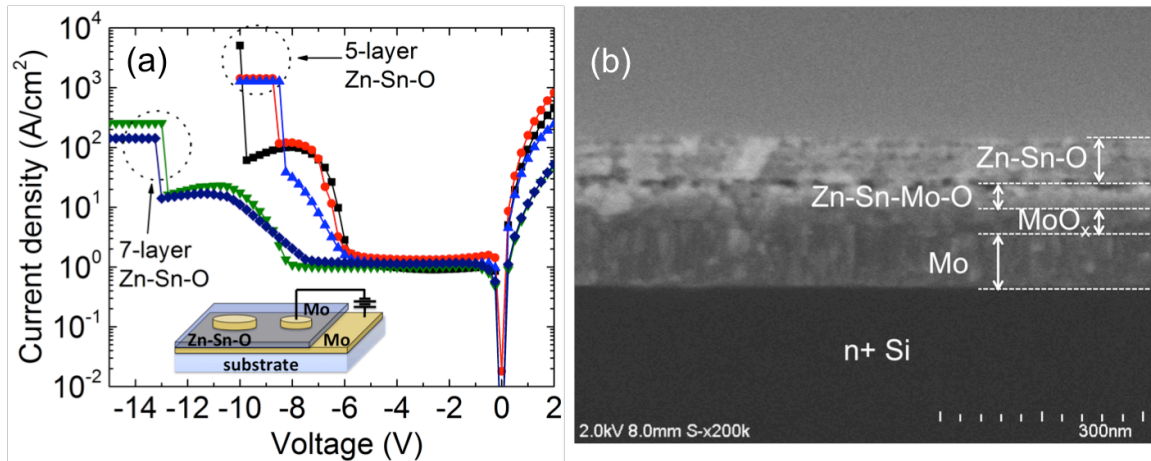


Figure S6. For integration of the V-TFD and TFT described in Figure 5 and 6, we deposited five layers of Zn-Sn-O instead of the seven layers used for the devices described in Figure 1 to 4. Thus, J - V characteristics and BV of the five-layer devices were measured to confirm that the Mo: a -Zn-Sn-O diode behavior was not significantly affected by the reduction in the number of layers. (a) BV of 5-layer V-TFD is slightly lower (> 8 V) than that of 7-layer V-TFD (> 10 V), but this BV range is still sufficient to harvest energy from commercial readers with 200 mW of output power. (b) Cross-sectional SEM image obtained from a five layer Zn-Sn-O layer on top of Mo. It shows similar features to the seven-layer case, with distinguishable MoO_x and Zn-Sn-Mo-O layers. The combined film thickness of Zn-Sn-Mo-O and Zn-Sn-O is ~ 150 nm. This thickness was used as L_{TFD} in Equation (4) to calculate the cut-off frequency shown in Figure 5d.

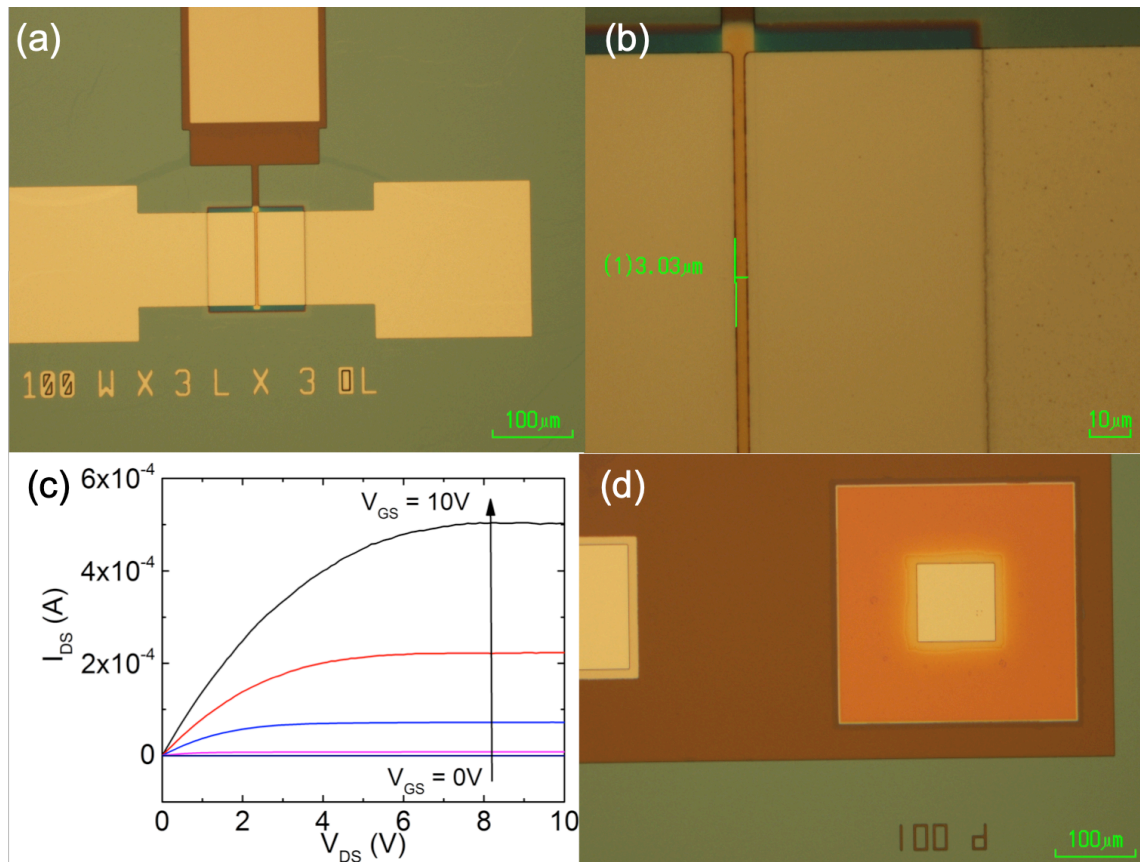


Figure S7. (a) Microscope image of a fabricated bottom-gate top-contact TFT. The device has dimensions of 100 μm width (W), 3 μm channel length (L), and 6 μm overlap length for source and drain (OL). The size of the Zn-Sn-O island is 100 μm×100 μm. (b) Zoomed-in image of the TFT measured in (c), showing $L = 3$ μm. (c) Output characteristics of the TFT. The transfer characteristics of the same TFT is shown in Figure 5b. (d) Microscope image of a vertical TFD fabricated on the same substrate. The size of the top electrode is 100 μm×100 μm. For comparison, an image of a full-wave rectifier is shown in the inset of Figure 6a.

Section S3. Evaluation of the maximum operating frequency

The maximum operating frequency (f_m) of a diode and a TFT can be evaluated by:^[22,23]

$$f_{m,diode} = \frac{1}{2\pi r_s C_b}, \text{ and } f_{m,TFT} = \frac{g_m}{2\pi(C_{gs}+C_{gd})} = \frac{\mu(V_{gs}-V_t)}{2\pi L(L+OL)}. \quad (S1)$$

Here r_s and C_b are the diode series resistance and capacitance at zero bias, g_m is the transconductance at a given V_{gs} . $C_{gs}+C_{gd}$ refers to the total gate capacitance, including overlap capacitance, and L and OL refer to the channel length and overlap length. Both of these equations can only evaluate operating frequency in a limited fashion, as they are based on small-signal analysis. As shown in Figure 4b, the sinusoidal input voltage to be harvested by a rectifier can range up to 10 V peak-to-peak. The values of r_s , C_b , and g_m change dramatically with voltage. However the above equations assume constant values for these parameters, so that the equations are simplifications of the true switching behavior.

Another method commonly used to calculate operation frequency of a diode and a TFT is based on carrier transit time (f_t), which considers the time that it takes for an electron with velocity v to transit from one electrode to the other, i.e. to traverse the carrier transit length, L . This frequency is given by Equation (3). In this equation, V_{in} is the maximum input voltage applied to the rectifier, and V_{out} is the DC output voltage. $V_{in} - V_{out}$ is thus the voltage applied to the rectifier to drive the drift of an electron. It is worth noting that the actual maximum frequency can be lower than the calculated value of f_t if the electron mobility is not accurately specified. In TFTs, a minimum gate voltage (i.e. the threshold voltage) is required in order to accumulate charge before electron transport occurs with the given mobility $5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. This voltage, V_T , for our TFT was calculated to be ~ 3 V, as shown in Figure 5b, but this parameter is not included in Equation (3). In case of V-TFDs, we showed in Figure 2 that our V-TFD consists of two different films, namely Zn-Sn-Mo-O and Zn-Sn-O. The carrier mobility within the Zn-Sn-Mo-O layer is expected to be lower than the value of $5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ used for Zn-Sn-O, based on the following evidence: (a) as noted earlier, the on-current of Mo V-TFDs was dominated by SCLC (Figure S4), a transport mechanism for low-mobility materials,^[9-11,17] and (b) the value of Richardson constant (A^*) extracted by fitting leakage current with Schottky emission (Figure 3b) was very low, $0.74 \text{ Acm}^{-2}\text{K}^{-2}$, compared to that obtained from Pd V-TFD,^[12] $44 \text{ Acm}^{-2}\text{K}^{-2}$. These values indicate that the Zn-Sn-Mo-O layer likely has a low electron mobility, compared to a -Zn-Sn-O.

A potentially more accurate way to calculate the operating frequency of V-TFD and TFT is based on large-signal analysis, as performed by Steudel, *et al.*^[24] and used by others.^[25-27] In

large signal analysis, the maximum frequency of a rectifier is determined by the speed at which the charge consumed by DC output load (R_L) during one AC cycle with frequency f_c becomes equal to the charge stored on the load capacitance (C_L) via current flowing through the rectifier during the fraction of the cycle when the charging diode is in forward bias. In other words,

$$\frac{V_{out}}{R_L} \frac{1}{f_c} = \int_{t_1}^{t_2} I_{rectifier} dt, \quad (S2)$$

where $R_L C_L \gg \frac{1}{f}$ and $C_L \gg C_{rectifier}$.

The derivation of maximum operating frequency from Equation (S2) requires I - V equations for the V-TFD and diode-connected TFT, as explained in the literature.^[24] Here, we fit the measured on-current of each device shown in Figure 5c to the equations below in order to calculate f_c for that device. The measured on-current of V-TFD and that of diode-connected TFTs were each fitted to the following equations:

$$I_{TFD} = A \frac{9\epsilon_0\epsilon_r\mu_{TFD}V_{forward}^2}{8L^3}, \quad (S3)$$

representing the SCLC behavior of the V-TFD with a 0 V transition voltage, and

$$I_{TFT} = \frac{\mu_{TFT}C_{ox}W}{2L} (V_{forward})^2, \quad (S4)$$

representing the saturation current of a diode-connected TFT with $V_T = 0$ V. The fitting results are shown as dotted lines in Figure 5c. The fits use $\mu_{TFD} = 0.15 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and $\mu_{TFT} = 0.015 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. The low mobility values compared to the Hall mobility are attributed to the presence of the Zn-Sn-Mo-O layer and absence of the threshold voltage in the equations, respectively. The resulting equations for $f_{c,TFD}$ and $f_{c,TFT}$ are given in Equation (4) and (5) and are plotted in Figure 5d.

The advantage of the large-signal model compared to the model based on carrier transit time is that we can use an effective mobility based upon on-current measurements, without needing to assume a bulk mobility from Hall measurements. Nonetheless, the large-signal calculation method still has some limitations. First, it neglects the effect of reverse current, which can discharge the load during the cycle time when the diode is off. Second, it assumes that the quasi-static J - V curve applies at high frequencies. This might not hold true when frequency-dependent charge transport such as hopping^[28] comes into play. Third, the effect of device capacitance is neglected in the derivation. Despite these limitations, we think that this method is the most accurate way to estimate the maximum frequency of operation for our full-wave rectifiers.

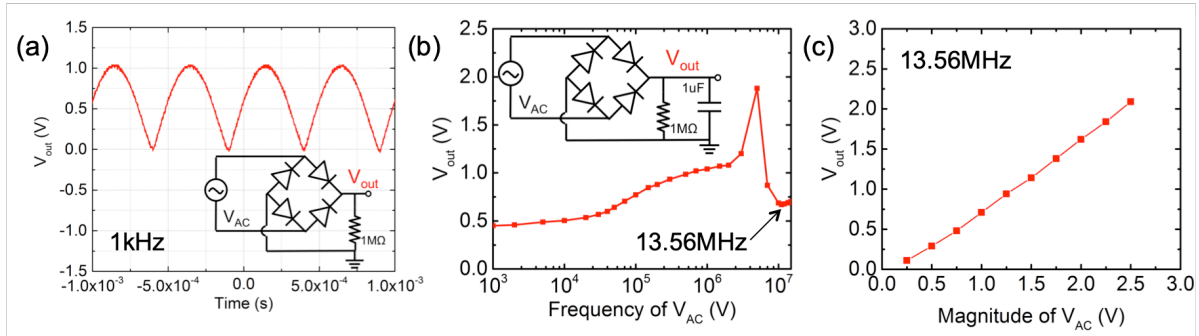


Figure S8. Full-wave rectifier (FWR) measurements in wired configurations (a)-(c). The input AC voltage was supplied by an HP 33120A function generator. Voltage measurement was done using a Tektronix MSO2024b oscilloscope. To ensure that V_{AC} floats from the ground of the load, an isolation transformer was used to power the function generator and isolate its ground from the ground of the oscilloscope. (a) In order to confirm operation of full-wave rectifier, a 1 M Ω load resistor was attached without a smoothing capacitor. For a peak-to-peak 3 V 1 kHz AC signal (V_{AC}), the voltage at the output node (V_{out}) has a period of 5×10^{-4} s, indicating rectification of a full cycle. (b) The frequency response of a FWR measured by sweeping the frequency of the function generator from 1 kHz to 15 MHz, while measuring DC V_{out} across the load. To obtain the DC output voltage, a smoothing capacitor of 1 μ F was used, as shown in the inset. We notice that V_{out} peaks at 7 MHz, which is attributed to resonance effects from parasitic inductances within the printed circuit board (PCB). (c) For a 13.56 MHz AC signal, the magnitude of input voltage (V_{AC}) is compared with the measured DC V_{out} .

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