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Exploiting In Situ Redox and Diffusion of Molybdenum to Enable Thin-Film Circuitry for Low-Cost Wireless Energy Harvesting

*Youngbae Son and Rebecca L. Peterson**

Direct additive fabrication of thin-film electronics using a high-mobility, wide-bandgap amorphous oxide semiconductor (AOS) can pave the way for integration of efficient power circuits with digital electronics. For power rectifiers, vertical thin-film diodes (V-TFDs) offer superior efficiency and higher frequency operation compared to lateral thin-film transistors (TFTs). However, the AOS V-TFDs reported so far require additional fabrication steps and generally suffer from low voltage handling capability. Here, these challenges are overcome by exploiting in situ reactions of molybdenum (Mo) during the solution-process deposition of amorphous zinc tin oxide film. The oxidation of Mo forms the rectifying contact of the V-TFD, while the simultaneous diffusion of Mo increases the diode's voltage range of operation. The resulting V-TFDs are demonstrated in a full-wave rectifier for wireless energy harvesting from a commercial radio-frequency identification reader. Finally, by using the same Mo film for V-TFD rectifying contacts and TFT gate electrodes, this process allows simultaneous fabrication of both devices without any additional steps. The integration of TFTs alongside V-TFDs opens a new fabrication route for future low-cost and large-area thin-film circuitry with embedded power management.

1. Introduction

Additive fabrication of thin-film electronics offers critical solutions for the "More than Moore" era. Thanks to compatibility with flexible substrates and large-area uniformity, additive fabrication of large-area electronics (LAE) has achieved commercial success in the display market. The use of LAE is now expanding to provide enhanced functionality to medical, wireless, sensing, and flexible systems.[1,2] To enable autonomous operation, wireless energy harvesting by thin-film components is often desired, for example in radio-frequency identification (RFID) tags. In parallel to these LAE efforts, the ongoing drive toward miniaturization of electronics demands functionality diversification via heterogeneous integration. Although silicon (Si) complementary metal oxide semiconductor (CMOS) integrated circuits (ICs) offer better electrical performance than thin-film circuits, the maximum operation voltage of sub-22 nm node Si CMOS is typically less than 1 V.[3] Therefore integration with electrical components that require higher input voltages requires board-level solutions or use of high voltage (HV) Si CMOS processes with larger gate lengths. To bridge this gap, higher voltage thin-film electronics can be directly and additively fabricated on sub-22 nm node CMOS.[4,5]

In both of these sectors, thin-film circuits are needed to provide power harvesting and management. For example, wireless powering of either LAE or miniaturized CMOS ICs requires alternating current-to-direct current (AC–DC) conversion, while assembly of sub-blocks for diverse functionality requires DC–DC power conversion to provide various operating voltages. Such power management circuitry requires power rectifiers and switches that operate at high efficiency over a wide range of voltages. To meet this need, numerous thin-film materials have been investigated for use in power devices. Some work has been done on thin-film transistors (TFTs) for input/output bridging or HV, low-current switching,[4,6–8] but most efforts have focused on rectifiers for energy harvesters in RFID tag applications. The materials investigated so far for power rectifiers include amorphous oxide semiconductors (AOS),[9,10] organic semiconductors,[11,12] or combined material architectures.[13] Although research on organics[14,15] is ongoing, AOS have a higher charge carrier mobility,[16] which is crucial to operate power devices at high frequency (HF) and efficiency.[17] Due to the advantageous material properties of AOS, both lateral TFTs[9] and vertical thin-film diodes (V-TFDs)[10] have been demonstrated for use in RFID energy harvesters. V-TFDs show superior performance[10,18] because their lower turn-on voltage, larger conduction area, and shorter device length enable a lower voltage drop and higher operating frequency.

However, the AOS V-TFDs demonstrated to date face two major challenges. First, the devices cannot withstand high operating voltages, limiting their use as power devices. Applying a moderate voltage vertically across a thin film leads to high electric field within the film that can create ion migration and cause premature breakdown.[19,20] Although the dynamics of ion migration can be utilized in resistive memory (RRAM)

Y. Son, Prof. R. L. Peterson
Department of Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, MI 48109-2122, USA
E-mail: blpeters@umich.edu

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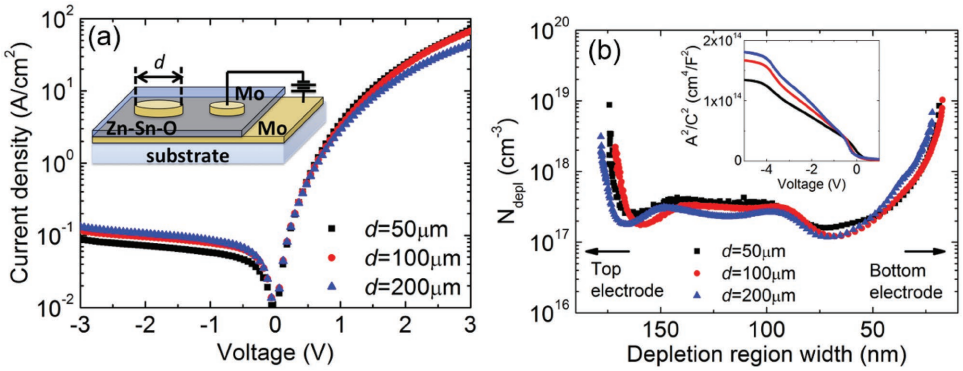

Figure 1. a) Typical *J–V* characteristics obtained from Mo:*a*-Zn-Sn-O diodes with various sizes. The inset shows a schematic of the V-TFDs, where *d* is the diameter of the top electrode. b) Depletion concentration (N_{depl}) profile for various size diodes. The corresponding *C–V* measurements are shown in the inset. *C–V* characteristics were measured at 1 MHz, across a DC sweep from +1 to −5 V, with 50 mV of AC voltage, in parallel *RC* model. Full depletion is achieved at −5 V, which corresponds to a film thickness of 180 nm.

applications,[21,22] this mechanism should be avoided in diodes that are intended to handle HVs with long-term stability. However, the effect of ion migration within AOS on V-TFD performance has not been characterized yet. Moreover, a way to prevent this mechanism is needed to enable wider application of V-TFDs. A second challenge for AOS V-TFDs is fabrication complexity. Previously reported methods to form rectifying contacts to AOS require deposition and patterning of a new, high-work-function Schottky metal, often followed by sophisticated oxidation steps in order to reduce oxygen vacancy defects near Schottky interfaces.[23–25] These additional process steps make V-TFD incompatible with TFT fabrication. This has led to the frequent use of diode-connected TFTs in rectifiers (by shorting the TFT gate and drain to form a two-terminal device). However, the large on-resistance of these devices causes poor rectifier performance.[9,26]

In this study, we demonstrate a novel method to overcome these challenges by using a dual-purpose solution process. We harness the chemical evolution of our ink, which can be controlled by the material underneath, to simultaneously enable the growth of rectifying junctions as well as of high-quality AOS channel layers. Our solution process not only solves the fabrication complexity issue of V-TFDs and TFTs, but it also forms a distinct layer at the Schottky barrier that prevents ion migration and enhances the voltage handling capability of V-TFDs. As a result, using a single fabrication process, we are able to integrate high-voltage diode rectifiers—which can operate at a much higher frequency than TFT rectifiers—alongside TFTs, which can be used for future digital circuitry. Solution processing is an attractive, low-cost, and large-area deposition method, as its in-air deposition capability eliminates the need for expensive vacuum-deposition tools.[1] It also offers inexpensive patterning via printing techniques for future additive fabrication.[27–29] Among various AOS candidates, we use amorphous zinc tin oxide (*a*-Zn-Sn-O) due to its earth-abundant and non-toxic elemental composition. We have previously demonstrated a solution process for environment-friendly, in-air deposition of *a*-Zn-Sn-O film with consistently high quality obtained across a wide humidity range for future large-scale manufacturing.[30] Our process temperature, 520 °C, allows non-destructive, additive fabrication on standard CMOS, and low-cost substrates like glass.[31,32] When our ink is deposited on a gate dielectric, it creates a high quality *a*-Zn-Sn-O film that can be used as a TFT channel layer.[30] When deposited on top of an Mo metallic layer, reduction–oxidation (redox) reactions and atomic diffusion of Mo occur in situ during *a*-Zn-Sn-O film coating and annealing. The redox mechanism enables formation of different interfacial layers with distinct properties in areas with different underlying patterns. This allows simultaneous fabrication of V-TFDs and TFTs by selective patterning of the underlying materials. In addition, atomic diffusion at the bottom Schottky interface greatly enhances the voltage handling capability of V-TFD. The resulting HV and HF operation of V-TFDs enables wireless energy harvesting from a commercial HF RFID reader. Here, we specifically choose Mo as it is one of the most commonly used metal electrodes for AOS TFTs due to its high-quality ohmic contact properties with various AOS.[33–37] Thus, our exploitation of Mo interaction with *a*-Zn-Sn-O may be widely adapted to other AOS.

2. In Situ Molybdenum Oxidation to Form Rectifying Contact

Prior to integrating V-TFDs with TFTs, V-TFDs using Mo and Zn-Sn-O were fabricated separately to analyze their performance and material composition. **Figure 1** shows the electrical characterization results. *J–V* measurements of V-TFDs, shown in Figure 1a, reveal rectifying behavior with the Schottky junction formed at the bottom of the AOS layer. Figure 1b shows the depletion concentration (N_{depl}) depth profile obtained from *C–V* measurements. *C–V* characteristics are shown in the inset as A^2/C^2 versus *V*, where *A* stands for the device area. The inset shows that diode capacitance decreases with reverse bias, which indicates expansion of the depletion region through the thin film. It reaches a constant minimum capacitance at a reverse bias of −5 to −4 V, which corresponds to full depletion. N_{depl} is calculated using $\frac{A^2}{C^2}=\left(\frac{2}{q\varepsilon_s\varepsilon_o N_{depl}}\right)(V_{bi}-V)$, where q is electronic charge, ε_s is the dielectric constant, ε_o is the permittivity in free space, and V_{bi} is the built-in potential.[38] The corresponding

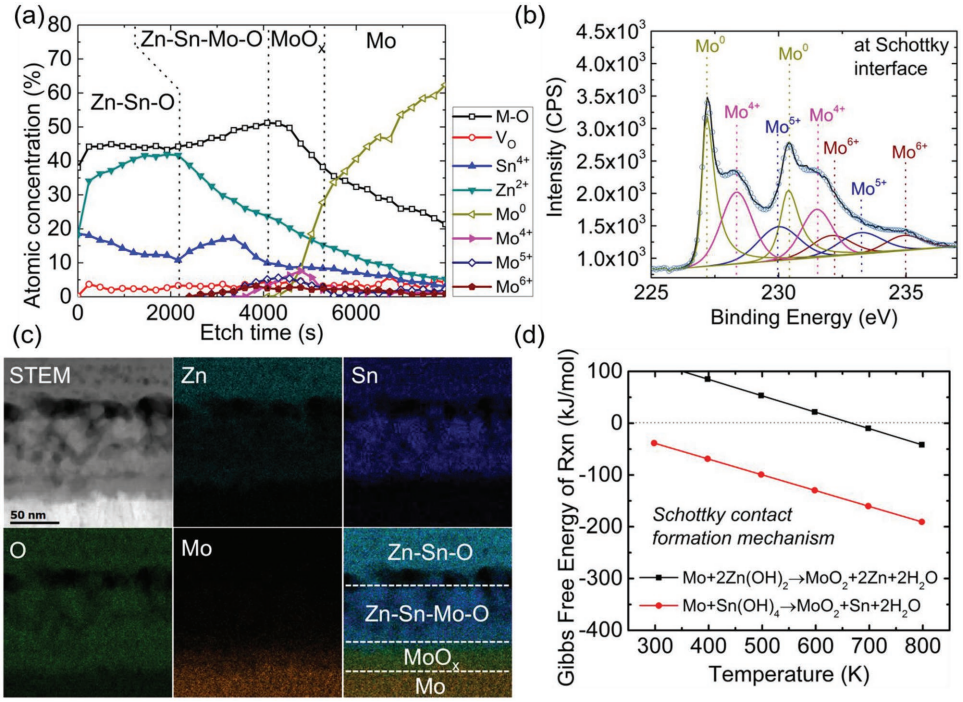

Figure 2. a) XPS depth profile of bottom Mo/*a*-Zn-Sn-O deposited on Si substrate. In between the Mo and *a*-Zn-Sn-O, layers of MoO_x and Zn-Sn-Mo-O appear. b) XPS Mo 3d core level analysis of the MoO_x layer, which corresponds to an etch time of 4800 s in (a). Hollow circles indicate the summation of the de-convoluted peaks, which overlaps with the measured curve. Details of XPS core-level analysis methods are described in Section S1 in the Supporting Information. c) Cross-sectional STEM dark-field image and EDS elemental mapping of Zn (cyan), Sn (blue), O (green), and Mo (orange) elements obtained near Mo/*a*-Zn-Sn-O junction. A STEM image of the entire film stack is shown in Figure S1 in the Supporting Information. Two additional interfacial layers (i.e., MoO_x and Zn-Sn-Mo-O) appear between metallic Mo and Zn-Sn-O, which accords with the XPS depth profile shown in (a). d) Standard Gibbs free energy of Mo oxidation during solution process of Zn-Sn-O, showing negative values at the film anneal temperature (793 K).

depletion width (w) is calculated from $C = \varepsilon_s \varepsilon_o \frac{A}{w}$. Using ε_s of 19, reported earlier for *a*-Zn-Sn-O,[24] we confirm that the depletion region expands vertically throughout the thin film; the depletion region width at full depletion is around 180 nm.

In order to explain the formation of a rectifying junction at the bottom Mo, extensive material characterization was performed as shown in **Figure 2**. X-ray photoelectron spectroscopy (XPS) depth profile was taken at the bottom Mo/*a*-Zn-Sn-O junction. Figure 2a reveals that two additional layers are formed as a result of *a*-Zn-Sn-O deposition on Mo. First, on top of the metallic Mo layer lies an Mo suboxide layer. In this region, Mo 3d core level analysis shows that Mo co-exists in the Mo^{6+}, Mo^{5+}, Mo^{4+}, and Mo^0 oxidation states (Figure 2b). The Mo oxidation states transition from Mo^0 to Mo^{4+} to Mo^{5+} to Mo^{6+} as we move from bottom Mo metal to top Zn-Sn-O. A similar transition of Mo oxidation state has been reported for thermally oxidized Mo and for MoO_3 grown on Mo substrates, where Mo^{6+} was interpreted as fully oxidized MoO_3, Mo^{5+} as MoO_3 with oxygen vacancies, and Mo^{4+} as metallic MoO_2.[39] Second, on top of this suboxide layer is a Zn-Sn-O layer with a noticeable amount of Mo incorporated into it (≈4 at.%) and with Sn-rich composition (Zn:Sn ratio of ≈5:3 compared to a ratio of ≈3:1 in the upper *a*-Zn-Sn-O layer). We hereafter refer to these layers as MoO_x and Zn-Sn-Mo-O, respectively. The spatial distribution of the Mo^{6+}, Mo^{5+}, and Mo^{4+} oxidation states indicates that the MoO_x and Zn-Sn-Mo-O layers are formed due to oxidation and diffusion of bottom Mo during the *a*-Zn-Sn-O deposition and annealing process.

In order to confirm the formation of these distinctive layers, scanning transmission electron microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDS) studies were carried out. Figure 2c shows two distinctive regions between Mo and *a*-Zn-Sn-O, with a ≈50 nm thick MoO_x layer and a ≈80 nm thick Sn-rich, Mo-doped Zn-Sn-Mo-O layer. While Mo itself is low-work-function metal, Φ_{Mo} = 4.4–5.0 eV,[40] and is often used to form ohmic contacts to AOS,[34] its oxidized counterpart has a high-work function, Φ_{MoOx} = 4.7–6.8 eV, the value of which depends on oxygen composition.[39,41] Therefore, we conclude that the thick, high-work-function MoO_x layer, which is generated at the bottom electrode as a result of our solution process, functions as a rectifying junction. The rectifying nature of the bottom contact is furthermore confirmed by the *C*–*V* measurements shown in Figure 1b, which show a deposition thickness of 180 nm. Cross-sectional STEM and scanning electron microscope (SEM) images likewise show that the thickness of the Zn-Sn-Mo-O layer and Zn-Sn-O layer combined is 180 nm (Figure S1, Supporting Information). Thus, the MoO_x layer functions as a rectifying contact and enables complete depletion of the Zn-Sn-Mo-O and Zn-Sn-O layers in reverse bias. This is in contrast to the ohmic top electrode that consists of metallic Mo deposited by sputtering.

The underlying mechanism of MoO_x layer formation can be explained by calculating the standard Gibbs free energy of reactions (ΔG_{rxn}^{o}) that occur during our solution process. When the ink is deposited on glass or alumina, the zinc and

tin acetates in the solution first thermally decompose into hydroxides ($Zn(OH)_2$ and $Sn(OH)_4$), and later go through a dehydroxylation process to form a uniform *a*-Zn-Sn-O film[30]:

$$x\mathrm{Zn(OH)_2} + (1-x)\mathrm{Sn(OH)_4} \rightarrow \mathrm{Zn_xSn_{1-x}O_{2-x}} + (2-x)\mathrm{H_2O}. \quad (1)$$

However, during this process the intermediate $Zn(OH)_2$ and $Sn(OH)_4$ species can interact with the bottom Mo layer to form MoO_2:

$$2\mathrm{Zn(OH)_2} + \mathrm{Sn(OH)_4} + 2\mathrm{Mo} \rightarrow 2\mathrm{MoO_2} + 2\mathrm{Zn} + \mathrm{Sn} + 4\mathrm{H_2O}. \quad (2)$$

The $\Delta G_{rxn}°$ values calculated for MoO_2 formation with Zn and Sn hydroxides are shown in Figure 2d as a function of temperature. Both values are negative at the Zn-Sn-O anneal temperature of 520 °C (793 K). Negative values of $\Delta G_{rxn}°$ indicate that $Zn(OH)_2$ and $Sn(OH)_4$ near Mo should spontaneously form MoO_2 during thin-film annealing. Similarly, Zn and Sn hydroxide can react with Mo to form MoO_3. The calculated $\Delta G_{rxn}°$ for these reactions are also negative at 793 K, as shown in Figure S2 in the Supporting Information. The multiple oxidation states of Mo observed near the interface in our films indicate that both the MoO_2 and MoO_3 reactions occur during our solution process.

3. In Situ Molybdenum Diffusion to Enhance Voltage Handling Capability

After material characterization, we evaluated the V-TFD device performance for power rectifiers (**Figure 3**). When a diode rectifies an AC voltage, most of the input voltage is applied as reverse bias across the diode, since the diode has higher impedance when it is in the off-state compared to the on-state. Therefore, the diode breakdown voltage (BV) and reverse-bias-stress endurance are important parameters for rectifier applications, which determine its voltage handling capability and lifetime.[42] The previously reported AOS V-TFDs have faced challenges in this regard, due to low BV and severe degradation when in reverse bias. The physical origin of these weaknesses have been attributed to field-induced oxygen vacancy (V_O) migration within AOS, as set-and-reset behavior was observed after breakdown in AOS V-TFDs.[19,20] These weaknesses, which we also previously observed in solution-processed Pd:*a*-Zn-Sn-O diodes,[19] significantly limit their use in rectifier applications: the rectifier degrades within short period of time (tens of minutes) and breaks down at low input AC voltage (peak-to-peak voltage of 5 V), as illustrated in Figure S3 in the Supporting Information. These challenges must be overcome for power rectifiers.

The Mo:*a*-Zn-Sn-O diodes presented here (which will be referred as Mo V-TFD for simplicity) offer a new way to address

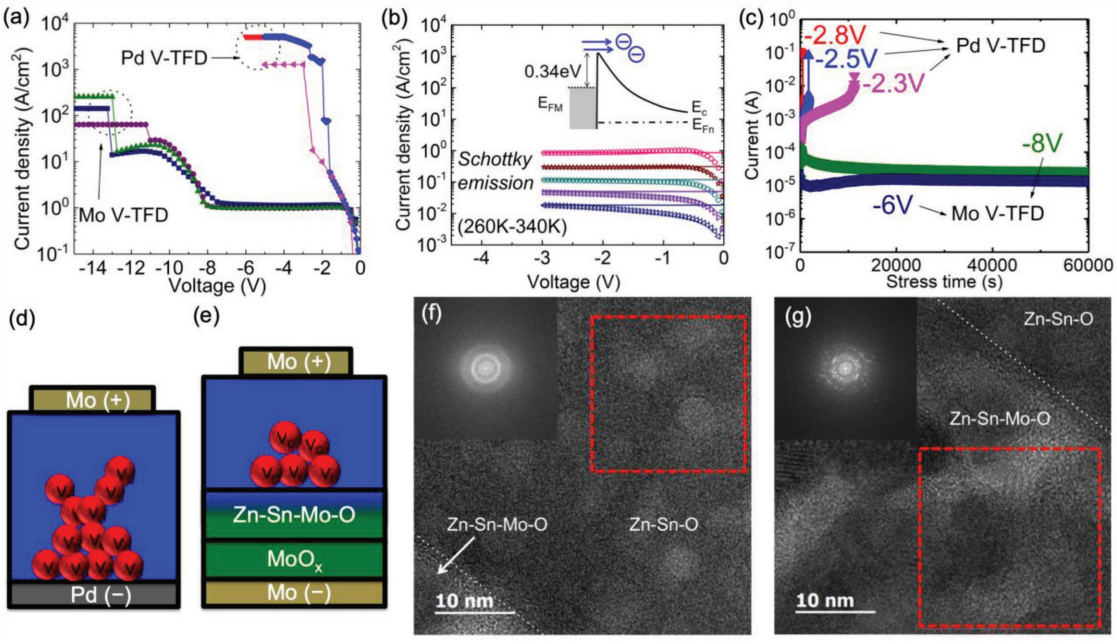

Figure 3. a) BV > 10 V measured on Mo V-TFDs with various electrode sizes (diameter of 30, 50, and 100 µm). BV measured on Pd V-TFDs with the same sizes are also shown for comparison. b) Temperature-varying reverse *J*–*V* measurements (symbols) of Mo V-TFDs. The bias-independent reverse current obeys Schottky emission over a potential barrier of 0.34 eV without image force lowering (solid lines). The charge transport analysis on forward current is shown in Figure S4 in the Supporting Information. c) Reverse bias stress in Mo V-TFD and Pd V-TFD. Unlike the Pd V-TFD, which was tested at <3 V magnitude, the Mo V-TFD were tested at a higher reverse voltages, 6 and 8 V, and still did not show any increase in leakage current. After the stress test, the Mo V-TFD still maintained its rectifying behavior as shown in Figure S5 in the Supporting Information. (b) and (c) are from 100 µm-diameter diodes. d) In Pd V-TFD, oxygen vacancy defects (V_O in red circles) accumulate near the Pd layer, which causes an increase in leakage current and premature breakdown, as shown in (c). e) In the Mo V-TFD, the Zn-Sn-Mo-O layer prevents V_O defects from accumulating near the MoO_x Schottky layer, preventing an increase in leakage current and resulting in a higher BV, as shown in (c). (f) and (g) show HRTEM images near Zn-Sn-O/Zn-Sn-Mo-O interface. The interface is marked with a white dotted line. The regions for FFT analysis are marked with red dashed lines and the corresponding FFT patterns are shown in the insets. Zn-Sn-O shows an amorphous morphology in (f), while g) Zn-Sn-Mo-O is polycrystalline.

these challenges. For oxygen vacancy migration to degrade and cause breakdown of AOS V-TFD, V_O defects must first accumulate adjacent to the Schottky interface and then form a conductive filament (CF) in order to short the bottom and top electrodes, as has often been observed in memristors.[43,44] In our Mo/*a*-Zn-Sn-O junctions, the layer adjacent to the MoO_x Schottky contact is the Zn-Sn-Mo-O film that was formed via in situ diffusion as shown in Figure 2. Therefore, the reverse bias behavior of Mo V-TFD is determined by the dynamics of V_O migration within the Zn-Sn-Mo-O layer. As shown in Figure 3a, the Mo V-TFD has a high BV of over 10 V, and exhibits a constant leakage current prior to breakdown. The leakage current of Mo V-TFD was analyzed with temperature-varying *J*–*V* measurements (Figure 3b). The temperature variance and bias independence indicates that current flow is via Schottky emission without image force lowering, obeying $J_r = A^* T^2 \exp\left(\frac{-\Phi_b}{kT}\right)$, with A^* as 0.74 A cm^{-2} K^{-2} and Φ_b of 0.34 eV. Thermionic emission leads to a constant leakage current, independent of reverse bias. Φ_b is the potential barrier formed at the MoO_x/Zn-Sn-Mo-O interface; the larger the value of Φ_b, the lower the leakage current, J_r. In the future, it may be possible to minimize leakage by increasing Φ_b through additional oxidation of Mo via O_2 plasma or O_2 annealing.[41,45] In addition to a constant leakage current, Mo V-TFDs show negligible degradation during reverse bias, even when relatively HVs of 6 or 8 V were applied for up to 60 000 s (Figure 3c).

The high BV and excellent bias-stress endurance of Mo V-TFD distinguish it from our previously reported Pd V-TFD, as shown in Figure 3a,c. We note that the same *a*-Zn-Sn-O and top Mo deposition methods were used for both the Pd and Mo V-TFDs, and the resulting *a*-Zn-Sn-O thicknesses are identical (≈110 nm) in these devices. As shown in Figure 3d, the poor stress endurance and low BV of the Pd V-TFD is due to oxygen vacancy (V_O) migration within *a*-Zn-Sn-O, causing trap-assisted tunneling near the Schottky contact and CF formation through the bulk. In contrast with the Pd case where *a*-Zn-Sn-O layer forms a junction with a Pd Schottky contact (confirmed with XPS depth profile[24]), for Mo V-TFD, a Zn-Sn-Mo-O layer forms in between the Schottky junction and Zn-Sn-O. Thus, the voltage handling capability of Mo V-TFDs is dominated by V_O dynamics within Zn-Sn-Mo-O. As both BV and bias stress endurance are better for Mo V-TFD, we conclude that V_O cannot easily migrate and accumulate within the Zn-Sn-Mo-O layer (Figure 3e). Our experimental data suggest a physical origin for the different oxygen vacancy behavior observed within Zn-Sn-Mo-O. First, the Zn-Sn-Mo-O layer has an Sn-rich composition with Mo incorporated by diffusion, as shown in Figure 2a,c. The different metal cation stoichiometry of Zn-Sn-Mo-O compared to *a*-Zn-Sn-O may lead to high activation energies for V_O formation and migration, caused by the change in oxygen ion hopping distance or in potential barriers within the ionically bonded structure. This approach—modifying activation energies for V_O formation and its migration with the help of impurity doping—is often used to tune forming behavior in memristive devices.[46] Second, in addition to the effect of chemical composition, the different crystallinity of the film may affect V_O migration and CF forming behavior. It has been previously reported that annealing amorphous indium gallium zinc oxide (*a*-IGZO) with diffused copper can generate crystalline clusters which results in prevention of CF-forming behavior.[22] In order to characterize the crystallinity of the films, high-resolution transmission electron microscopy (HRTEM) imaging was performed with the microscope operated in conventional TEM mode on the same sample shown in Figure 2. The HRTEM images and fast Fourier transform (FFT) diffraction patterns obtained for the Zn-Sn-O and Zn-Sn-Mo-O layers are shown in Figure 3f,g, respectively. While the Zn-Sn-O layer possesses an amorphous structure as expected, the Zn-Sn-Mo-O layer possesses a polycrystalline structure. Third, as indicated by analysis of forward *J*–*V* curves in Section S2 in the Supporting Information, the Zn-Sn-Mo-O layer functions as a low-doped region, reducing the maximum electric field at the Schottky interface under reverse bias. All of these mechanisms prevent or reduce field-induced accumulation of V_O defects at the Schottky interface, as illustrated in Figure 3e. As a result, in the Mo V-TFDs, we obtain a reduced leakage current, compared to the Pd V-TFDs, and avoid premature breakdown by CF formation. To further optimize Mo V-TFD diode performance, in the future work can be done to quantify the diffusion kinetics occurring in situ during solution-processed film deposition and annealing, in order to more precisely control the thickness and stoichiometry of the MoO_x and Zn-Sn-Mo-O layers.

For AC rectifiers, the BV of the diode should be larger than twice the desired DC output voltage. As the DC voltage required to drive logic circuits can be as high as 5 V, a BV of >10 V is desired. Commercial proximity HF RFID readers, which often generate output power of 200 mW with a 50 Ω source, can deliver AC peak-to-peak voltages up to ≈8.9 V to the diode $\left(P_{source} = \frac{1}{8} \times \frac{V_{pp}^2}{50\,\Omega}\right)$. Thanks to the strong reverse bias characteristics of our Mo V-TFD, shown in Figure 3, our diode can stably rectify AC voltages within this range. To confirm the rectifier behavior of the fabricated V-TFD at HF and voltage ranges, we characterized the diode in a half-wave rectifier circuit, shown in **Figure 4**. Figure 4a inset shows the measurement setup for observing AC-to-DC conversion. In order to obtain a stable DC output voltage, the load capacitance, C_L, should minimally discharge through the load resistor, R_L, during one AC cycle (period $T = 1/f$), i.e., $R_L C_L \gg 1/f$. In addition, the ratio between C_L and the diode capacitance, C_D, defines the amplitude of the small-signal AC voltage: C_L needs to be very large compared to C_D, $C_L \gg C_D$.[14,47] Therefore, a 1 µF load capacitor and 1 MΩ load resistor were used, which gives $R_L C_L = 1$ s and satisfies $C_L \gg C_D$, where C_D for the $d = 100$ µm diode measured here is approximately 25 pF when measured at 1 MHz at zero bias. In this configuration, the V-TFD rectifies the supplied AC voltage to DC (Figure 4a). AC peak-to-peak voltages as high as 10 V could be rectified to a DC output as high as 3 V (Figure 4b). As shown in Figure 4b, the diode does not show any cut-off behavior up to 15 MHz, indicating its usefulness for HF RFID tags operating at 13.56 MHz.

4. Co-fabrication of Wireless Energy Harvesters Alongside TFT Switches

The commercialization of AOS TFTs in display backplane applications has been enabled by their superior switching

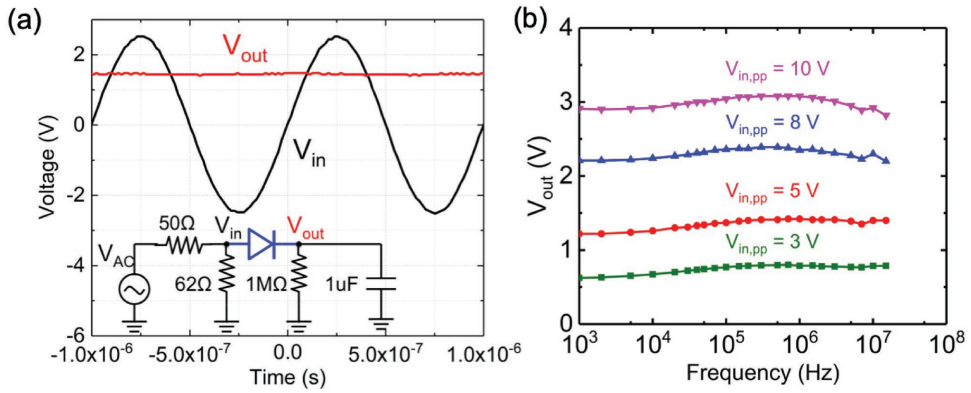

Figure 4. a) The measurement configuration of the diode in a half-wave rectifier circuit is shown in the inset. An AC input voltage (V_{AC}) was generated by a function generator, operated in 50 Ω mode and used in parallel with a 62 Ω input resistor. In (a), V_{in} (in black) indicates the 1 MHz, 5 V sinusoidal peak-to-peak voltage across the 62 Ω input resistor, measured using an oscilloscope. V_{out} (in red) shows the DC output voltage measured across the load. b) The frequency response of the output voltage measured up to 15 MHz, which is the maximum frequency of the function generator, is shown for different V_{in} peak-to-peak values. Because the diode has BV > 10 V, the rectifier can rectify up to peak-to-peak voltage of 10 V. The devices tested here have diameter of 100 µm.

performance in metal–insulator–semiconductor field-effect transistors (MISFETs). MISFETs can be diode connected to perform rectifying functions, but their performance is significantly worse than that of a V-TFD made using the same active semiconductor layer.[17] To confirm that Mo V-TFDs can be used to enhance rectifier performance of thin-film electronics, we next demonstrated the simultaneous fabrication of Mo V-TFDs and MISFETs on the same substrate (**Figure 5**). In future thin-film circuits, TFTs can be used for digital logic and analog amplification, while V-TFDs integrated on the same die can be used for efficient and HF AC–DC rectification. The fabrication process flow is illustrated in Figure 5a. A key feature of our process is that the Zn-Sn-O ink goes through different chemical evolution during annealing based on the material underneath. On top of Al_2O_3 gate dielectric, it forms a high-quality AOS channel layer for TFTs, while on top of exposed bottom Mo layers, it forms MoO_x and Zn-Sn-Mo-O layers for high-voltage V-TFDs. The former reaction involves dehydroxylation processes [Equation (1)], while the latter involves Mo diffusion and oxidation [Equation (2)]. For this sample, we deposited five spin-coated layers of Zn-Sn-O instead of seven, as were shown in Figures 1–4. We chose five spin-coated layers for Zn-Sn-O because we previously reported high-quality TFT performances with five-layer Zn-Sn-O,[30] and V-TFDs made with five layers shows higher on-current while maintaining good BV for use in energy harvesters for our 200 mW RFID reader, as shown in Figure S6 in the Supporting Information. Figure 5b shows transfer curves of fabricated TFTs, with enhancement-mode operation. For simple logic circuits, enhancement mode is more desirable than depletion mode, as it does not require level shifting.[48]

To justify the need for V-TFDs in rectifier applications, we compare the performance of V-TFDs with TFTs used in diode configuration, i.e., with gate and drain shorted. When enhancement-mode TFTs are used in the diode configuration, the positive turn-on voltage significantly limits the on-current. In addition, diode-connected TFTs have a fundamental geometric weakness compared to V-TFDs, due to the long transit length (the channel length) and narrow conduction area (the cross-sectional area of the thin film). These limits have been previously reported for vacuum-deposited AOS.[9,10,17,18,26,48] Despite attempts to minimize lateral resistance by increasing channel width,[49] and decreasing channel length[50,51] or overlap length,[52] the on-current of diode-connected TFTs is still low, compared to V-TFDs. In addition, to obtain short TFT lengths, high-resolution photolithography is required, which can be prohibitive.

To illustrate these points, a V-TFD and a TFT in a diode configuration were measured and compared. Both devices were located on the same sample and co-fabricated, and both had a size of 100 µm × 100 µm. For the TFT, the top contact area is included in the area calculation. Microscope images of these devices are shown in Figure S7 in the Supporting Information. Due to the V-TFD's lower turn-on voltage, larger conduction area (size of electrode), and shorter carrier transit length (film thickness) compared to the lateral TFT, the on-current of the V-TFD was more than five orders of magnitude higher than the diode-connected TFT, as shown in Figure 5c. A high on-current is important, as it not only reduces the voltage drop and increases the overall efficiency of a rectifier, but also increases rectifier operating frequency.

The theoretical operating frequency limits of the V-TFD and TFT were calculated for comparison. These were estimated using two approaches: the transit time of carriers (f_t) and the on-current of the rectifier (f_c). f_t considers the time that it takes for the fastest electron (with velocity v) to transit from one electrode to the other, i.e., to travel the distance L. This frequency can be expressed as:

$$f_t = \frac{v}{2\pi L} = \mu \frac{V_{in} - V_{out}}{2\pi L^2} \quad (3)$$

where $V_{in} - V_{out}$ is the maximum forward voltage applied across the rectifier and μ is the effective carrier mobility. f_c is the frequency at which the charge dissipated through the load (R_L) becomes comparable to the charge stored on the load capacitance (C_L) by the diode on-current. The maximum operating frequency for V-TFD ($f_{c,TFD}$) and diode-connected TFT ($f_{c,TFT}$) are expressed as[47]:

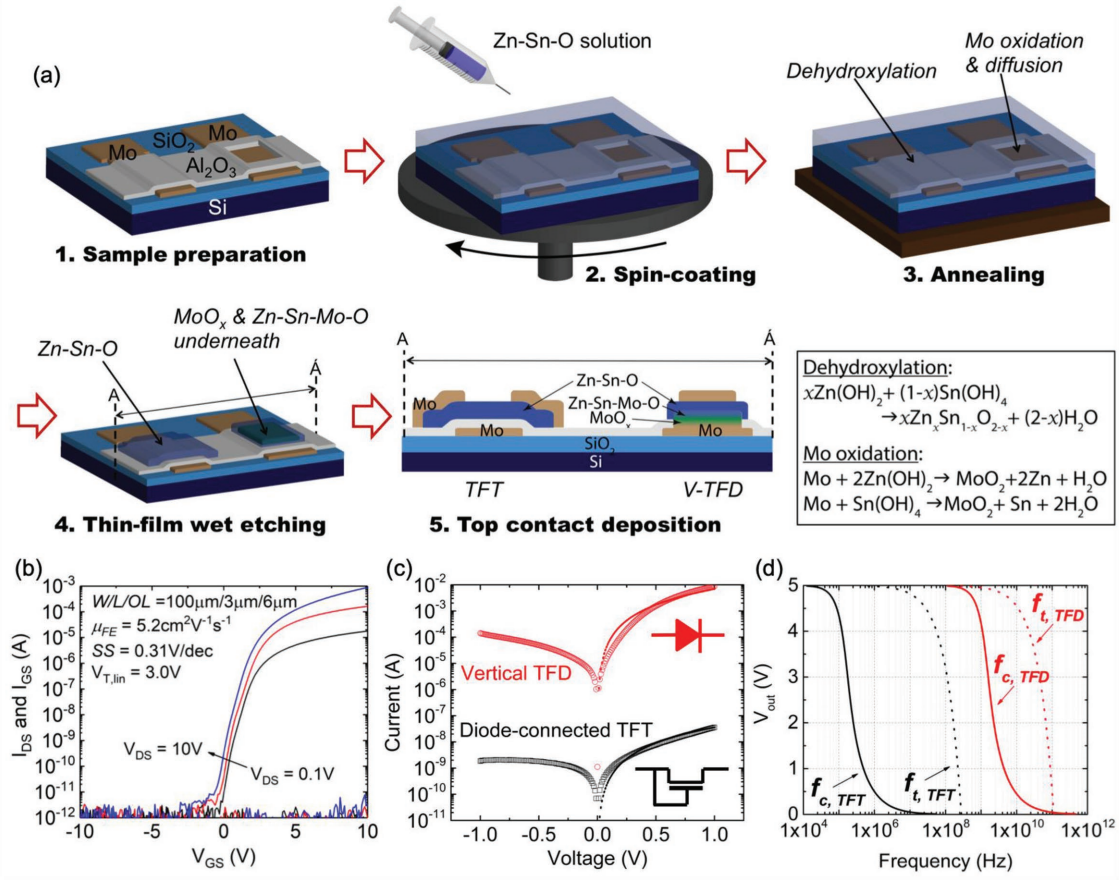

Figure 5. a) Simplified schematic of simultaneous fabrication of V-TFD and TFT on a single substrate. Thin films with different chemical composition are grown via different chemical evolution during solution deposition of Zn-Sn-O. Specifically, Zn-Sn-O is grown via dehydroxylation on top of Al_2O_3, while Mo oxidation and diffusion occur on top of bottom Mo, creating MoO_x and Zn-Sn-Mo-O layers in specific regions. A 2D cross-sectional view (A ↔ Á) of completed devices is shown in Step 5. b) Transfer curves obtained from a TFT with device dimensions of 100 μm in width, 3 μm in channel length, and 6 μm in overlap length, which leads to 100 μm × 100 μm in overall size, including source and drain contacts. Output curves are shown in Figure S7c in the Supporting Information. c) Comparison of *I*–*V* curves obtained from TFT in (b) with its gate and drain connected, and from V-TFD with 100 μm × 100 μm size. Hollow circles and squares are measured data and dotted lines are from the on-current model used to calculate $f_{c,TFT}$ and $f_{c,TFD}$ in (d). d) Maximum operating frequencies, calculated based on transit time (f_t) and measured on-current (f_c).

$$f_{c,\mathrm{TFD}} = \frac{9\mu_{\mathrm{TFD}}}{16\pi L_{\mathrm{TFD}}^2 V_{\mathrm{out}}}\left\{\left(V_{\mathrm{in}}^2 + 2V_{\mathrm{out}}^2\right)\cos^{-1}\left(\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}\right) - 3V_{\mathrm{out}}\sqrt{V_{\mathrm{in}}^2 - V_{\mathrm{out}}^2}\right\} \quad (4)$$

$$f_{c,\mathrm{TFT}} = \frac{\mu_{\mathrm{TFT}}}{4\pi L_{\mathrm{TFT}}^2 V_{\mathrm{out}}}\left\{\left(V_{\mathrm{in}}^2 + 2V_{\mathrm{out}}^2\right)\cos^{-1}\left(\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}\right) - 3V_{\mathrm{out}}\sqrt{V_{in}^2 - V_{\mathrm{out}}^2}\right\} \quad (5)$$

As seen in Equations (3)–(5), a shorter transit length, *L*, and a higher effective mobility, μ, lead to a higher rectifier operating frequency. Using a fixed V_{in} of 5 V, $f_{t,TFD}$, $f_{t,TFT}$, $f_{c,TFD}$, and $f_{c,TFT}$ were calculated and are shown in Figure 5d. For calculation of Equation (3), a Hall mobility of 5 $cm^2V^{-1}s^{-1}$, extracted from an identical five-layer *a*-Zn-Sn-O film was used.[30] For calculation of Equations (4) and (5), μ_{TFT} and μ_{TFD} were extracted from the experimental *I*–*V* curves shown Figure 5c, following the well-established method for f_c calculations.[14,15,17,47] An extended discussion of the frequency calculations can be found in Section S3 in the Supporting Information. It is clear that V-TFDs have a higher operating frequency than TFTs connected in the diode configuration. The maximum frequency of the V-TFD under V_{in} of 5 V and V_{out} of 3 V (i.e., the magenta line in Figure 4b) may be as high as 1.6 GHz. This estimate agrees with the previous demonstration of gigahertz-range operation of AOS V-TFDs made with *a*-IGZO.[10,18] The high operating frequency of the V-TFD is primarily due to the higher effective μ due to the lack of a turn-on voltage and the shorter *L* due to the vertical structure. For the TFT, *L* corresponds to the channel length (L_{TFT} = 3 μm), while for V-TFD, it is the film thickness (L_{TFD} = 150 nm).

Lastly, the wireless energy harvesting capability of solution-processed V-TFDs was tested, using a full-wave rectifier with four 100 μm × 100 μm V-TFDs fabricated on the same sample (**Figure 6**). To validate its applicability for wireless energy harvesting, a commercial 13.56 MHz RFID tag reader (DLP-RFID1, DLP Design) and antenna (DLP-RFID-ANT, DLP Design) were used. The reader has an output power of 200 mW and a read range of 10 cm (Protocol: ISO 15 693 and ISO 18 000–3). The full-wave rectifiers (FWRs) were wire-bonded to a printed circuit board (PCB) on which the load components and SubMiniature version A (SMA) connectors were soldered.

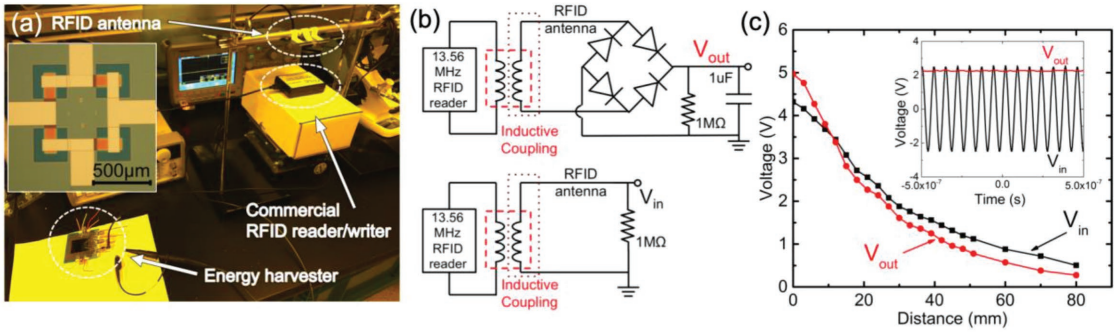

Figure 6. a) Wireless energy harvesting experimental setup. A commercial HF (13.56 MHz) RFID antenna and reader with 200 mW output power were placed in parallel. The power from the reader was wirelessly harvested using the antenna, while the distance between them was varied. The antenna was attached via SMA connection to an FWR wire-bonded onto a PCB with surface-mount loads. The DC output voltage of the FWR was measured with an oscilloscope. The inset shows a microscope image of an FWR with four 100 μm × 100 μm V-TFDs. b) Circuit diagrams showing the wireless energy harvesting measurement setup (top). To compare the measured V_{out} with V_{in}, V_{in} was measured as the voltage across a 1 MΩ resistor attached to the antenna, without the rectifier included (bottom). The maximum peak-to-peak V_{in} obtained at a distance of 0 mm was ≈8.7 V, which gives $P_{out} = V_{rms}^2/50\ \Omega \approx 190$ mW, close to the maximum output power of the reader. c) The magnitude of V_{in} and V_{out} as a function of separation distance. V_{out} exceeds over V_{in} when the distance is <10 mm, which is attributed to resonance due to mutual inductance. The inset shows V_{in} and V_{out} measured over time with the antenna and reader separated by a distance of 21 mm.

As shown in Figure 6a, the PCB was connected to the antenna to assess the energy harvested via inductive coupling from a commercial RFID reader.

The circuit diagrams of the wireless test setup for both input and output voltages are shown in Figure 6b. The AC voltage (V_{in}) delivered to the antenna via inductive coupling was measured using 1 MΩ load resistor (Figure 6b, bottom). As shown in Figure 6c, the maximum peak-to-peak V_{in} coupled from the reader to the antenna at 0 mm of distance was ≈8.7 V, which gives the output power of the reader to be $V_{rms}^2/50\ \Omega \approx 190$ mW. For DC output voltage (V_{out}) measurement, a 1 μF load capacitor and 1 MΩ load resistor attached to PCB via surface mount were connected to full-wave rectifier, as shown in Figure 6b (top). The result, shown in Figure 6c (inset), measured with an oscilloscope, is excellent AC–DC conversion using the V-TFD FWR for wireless energy harvesting. As shown in Figure 6c, reasonable output voltages are measured across the load as a function of distance, with V_{out}/V_{in} exceeding 80% at <40 mm of distance. At 0 mm, V_{out} as high as ≈5 V is obtained, which demonstrates that V-TFDs rectifiers can be used to power thin-film logic circuitry.[53] In order to obtain a higher V_{out} at larger distance, a voltage multiplier configuration can be implemented.[11] A comprehensive assessment of the FWR behavior at various input voltage and frequencies, obtained by additional measurements V_{out} and V_{in} in a wired configuration, is shown in Figure S8 in the Supporting Information.

5. Conclusion

In conclusion, we have developed a facile solution process that enables integration of high-voltage V-TFDs during the fabrication of Zn-Sn-O TFTs. We achieve this by exploiting in situ redox and diffusion of bottom Mo electrodes that occurs during ink-based deposition and annealing of Zn-Sn-O. The chemical interaction of the bottom Mo during AOS deposition not only forms a rectifying junction for V-TFDs, but also increases its voltage handling capability for rectifier applications by forming a low-doped Zn-Sn-Mo-O intermediate layer. After characterizing the effect of Mo oxidation and diffusion, which leads to formation of a rectifying junction and improvement in bias-stress endurance, V-TFDs were co-fabricated with TFTs on the same sample, without any additional fabrication steps. Both of the devices were characterized and compared for power rectifying applications. The performance of V-TFD diodes is far superior to that of diode-connected TFTs of the same size when operated at the same voltage, due to the larger on-current and shorter device length of V-TFDs: V-TFDs fabricated here show on-current at least five orders of magnitude higher than TFT, with the estimated maximum operating frequency being three orders of magnitude higher. To experimentally confirm the usefulness of the Mo V-TFD as a power rectifier thanks to its enhanced voltage handling capability, wireless energy harvesting using a full-wave rectifier was demonstrated with a commercial RFID reader. Despite the advantages of V-TFDs over diode-connected TFTs for rectifiers, three-terminal TFTs have unique functionality that cannot be replaced by V-TFDs. For example, TFTs are required for digital logic circuits, analog amplification, and pulse-width modulation in DC–DC conversion. TFTs fabricated in this work show enhancement-mode operation, and can be fabricated alongside V-TFD rectifiers to enhance the performance of thin-film electronics.

To our knowledge, this is the first report of simultaneous formation of different materials via chemical evolution of ink in order to fabricate different active circuit elements with a single solution process. Previously, Schottky diodes with AOS, including vacuum-deposited AOS, have only been reported using noble, high-work-function metals for rectifying contacts.[18,23–25] Such metals are disadvantageous as they are often incompatible with TFTs due to poor ohmic contact formation, they may require additional surface treatments to reduce oxygen vacancies near the Schottky interface,[23–25] and AOS V-TFDs fabricated with such metals often show vulnerability to bias stress.[19,20] In this work, we report for the first time a novel way to make a rectifying contact starting with low-work-function Mo, a metal widely used for AOS TFTs, by utilizing in situ

formation of the Schottky contact during Mo interaction with our Zn-Sn-O solution ink. The Mo oxidation and diffusion that occur during solution process, demonstrated here, can be widely exploited not only to enhance bias stress endurance of the films, but also to create novel fabrication routes for thin-film circuitry for future LAE or heterogeneous integration. For wider implementation of thin-film circuitry, the development of fully solution-processed electronics is highly desirable.[56,57] To realize our MoO_x-based V-TFD with a fully solution-processed approach, solution-processed MoO_x can be used for the bottom Schottky contact,[58,59] while the top ohmic contact could be replaced with solution-processed indium tin oxide (ITO) or indium zinc oxide (IZO).[56,57] In this scenario, because solution-processed Mo has not been developed, a low-work-function bottom gate metal for TFTs can be achieved by developing an area-selective, in situ reduction process, in which a solution-processed MoO_x layer could be converted into a metallic Mo gate metal during subsequent gate insulator deposition and annealing.

6. Experimental Section

Preparation of Precursor Solutions and Film Formation: The *a*-Zn-Sn-O layer was deposited by spin-coating a 0.5 M metal acetate precursor solution. Zinc acetate dihydrate (99.999%, $Zn(CH_3COO)_2{\cdot}2H_2O$, CAS number 5970-45-6, Sigma–Aldrich), and tin (II) acetate ($Sn(CH_3COO)_2$, CAS number 638-39-1, Sigma–Adrich) were dissolved in 2-methoxyethanol (99.8%, $CH_3OCH_2CH_2OH$, CAS number 109-86-4, Sigma–Aldrich) and ethanolamine (≥99.5%, $NH_2CH_2CH_2OH$, CAS number 141-43-5, Sigma–Aldrich), with a Zn:Sn ratio of 7:3. The solution was stirred for 12 h and filtered through a 0.22-µm syringe filter during dispensing, followed by spin-coating at 3000 rpm for 30 s. Each spun layer was pre-annealed at 520 °C for one minute at controlled humidity and temperature. After spin-coating the final layer, the samples were post-annealed at 520 °C for 1 h. Previously, this process was used to deposit smooth, amorphous zinc tin oxide semiconductor layers and fabricate TFTs[30,54] and Schottky diodes.[24,55]

Vertical Thin-Film Diode Fabrication: First, heavily doped *n*-type Si (n^{++}-Si (Sb), 0.01-0.02 Ω·cm, <100>) was used as a substrate, which was solvent-cleaned and dried. 100-nm Mo was sputtered to form the bottom electrode (Kurt J. Lesker Lab 18). After solvent cleaning, seven layers of Zn-Sn-O were deposited using the solution process described above. To expose the bottom Mo electrode, the deposited Zn-Sn-O layer at the edge of the sample was wet etched using dilute HCl and HNO_3 solution. After another solvent cleaning, a top electrode of 100-nm Mo was sputtered to form an ohmic contact to *a*-Zn-Sn-O,[34] and patterned with lift-off. Electrical characterization was done using an HP4156A semiconductor parameter analyzer and an HP 4284A Precision LCR meter. Temperature-dependent current–voltage measurements were taken using an HP4156A semiconductor parameter analyzer with a Lakeshore Cryotronics TTPX cryogenic probe station. For AC–DC measurements on a half-wave rectifier, an HP 33120A function generator was used with a Tektronix MSO2024b oscilloscope.

Co-fabrication of Thin-Film Diode and Transistor: Bottom-Schottky-contact V-TFDs were co-fabricated with bottom-gate, top-contact TFTs. Heavily doped *n*-type Si with 100-nm thermally grown SiO_2 was used as the substrate. On top of a cleaned substrate, 60-nm Mo was sputtered to form the gate electrode for TFT and bottom electrode for V-TFD (Kurt J. Lesker Lab 18). Then, bottom Mo was patterned using a reactive ion etching (LAM 9400). Next, a 55-nm Al_2O_3 gate dielectric was deposited using atomic layer deposition at 250 °C (Oxford OpAL ALD). The Al_2O_3 thickness was confirmed using spectroscopic reflectometry. To make an opening for bottom gate metal for TFT and to grow V-TFD, the Al_2O_3 layer was patterned by wet etch, using dilute NH_4OH. After solvent cleaning, five layers of Zn-Sn-O solution were deposited using the process described above. Next, the solution-processed Zn-Sn-O layer was patterned by wet etch, using dilute HCl and HNO_3 solution. This etch process enables device isolation and exposes the bottom gate electrode for TFT measurements. Top electrodes of 100-nm Mo were then sputtered to form ohmic contact for both TFTs and TFDs (Kurt J. Lesker Lab 18), and were patterned via lift-off. The fabrication steps are identical to those required for bottom-gate top-contact TFTs.

Material Characterization: XPS was measured using Kratos Axis Ultra XPS. A monochromatic Al X-ray source (8 mA and 14 kV) was used with a 110 µm aperture, pass energy of 20 eV, and step size of 0.1 eV. The Kratos charge neutralizer system was used. For depth profiling, argon ion sputtering was used with energy of 5 kV and ion source extractor current of approximately 90 µA, which resulted in a sputtering rate of 2–3 $nm{\cdot}min^{-1}$. XPS measurements were performed between 240 s sputtering intervals. For TEM measurements, an in situ FIB lift-out cross-sectional specimen was studied by using a JEOL JEM-3100R05 analytical electron microscope (AEM) attached with double Cs-correctors operated at 300 keV. Element mapping was conducted using X-ray signals with the microscope performed in STEM mode. High-angle annular dark-field images were taken for defining mapping regions.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

additive fabrication, amorphous oxide semiconductors, large-area electronics, solution process, thin-film circuitry

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