Vertical Self-Defined Thermoelectric Legs for Use in Thin-Film Micro Thermo Electric Generators (µTEG)

by

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Dedication

To my parents.

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Abstract

Micro thermoelectric generators (μTEGs) are solid-state devices that directly convert thermal power into electrical power through the Seebeck effect, a solid-state transduction mechanism. Through this effect, μTEGs can harvest power from temperature gradients available in their operating environment. They are capable of providing a robust and long-term power solution for remote sensing and internet of things (IoT) applications where there exists high servicing costs, harsh environments, or the need for long-term device operation.

In particular, thin-film based μTEGs are desirable due to ease of process integration, high throughput, material quality, and reproducibility. However, thickness constraints inherent to thin-film processes limit their potential usage. In conventional TEGs, the thickness of the thermoelectric film itself determines the separation distance between the hot and cold terminals. A very thin thermoelectric film thus creates a thermal short. This reduces the temperature difference across the device, limiting power output.

The focus of this dissertation is to remove this thermal limitation in thin-film generators. This is accomplished through a new μTEG design that decouples the height of the thermoelectric elements from the film thickness. Central to the implementation of the proposed design is the creation of thermoelectric (TE) films deposited over the sidewalls of high-aspect vertical columns. In this way, the height of the columns, and not the thickness of the TE film, sets the separation distance between the hot and cold ends of the thermocouples.

In this thesis, performance of this new μTEG design is analyzed. Bi_2Te_3 and Sb_2Te_3 thermoelectric films compatible with the proposed design are developed and integrated into functional μTEGs. The impact of column material, thermocouple height, and fill factor on μTEG performance are also presented.

The thermoelectric films used in this design are industry standard Bi_2Te_3 and Sb_2Te_3. The crystal structure of these films grown on vertical surfaces was found to differ significantly from that grown on standard planar substrates. Potential causes for this difference and impact on μTEG performance are investigated. Additionally, factors that impact Bi_2Te_3 and Sb_2Te_3 film growth are studied. These factors include surface topology, substrate material, deposition temperature, and the presence of a seed layer.

Key components required for the successful fabrication of μTEGs utilizing high-aspect column designs were developed. These include the creation of thermally insulating high-aspect columns, contact formation between N & P thermoelectric elements, and die attachment.

The fabricated μTEGs have thermocouple heights of 20 μm using 2 μm thick films and a fill factor of 17.5%. The measured power output of the fabricated generators is 4-5 $\mu W/K^2/cm^2$. These μTEGs use thermoelectric films grown over sidewall surfaces. The power factors of the sidewall films were 0.85 and 1.36 mW/K^2m for the N and P type films, respectively. Sidewall film performance was poorer in comparison to N and P type thermoelectric films grown under similar conditions on planar surfaces. These planar films had power factors of 3.63 and 1.30 mW/K^2m for the N and P type materials.

Chapter 1 Introduction

Thermoelectric generators (TEGs) are solid-state heat engines that convert thermal energy directly into electrical energy. They operate using the Seebeck effect, where an input temperature difference across two terminals of a conductor generates an electrical potential across the same terminals.

The first generators utilizing the Seebeck effects were known as thermopiles. These consisted of two dissimilar metals exhibiting opposing polarities in their potential response. To increase voltage output, multiple of these pairs were connected in series. One such example, the Markus thermopile, was invented in 1864. It consisted of an alloy of copper, zinc and nickel for the "negative" metal and an antimony, zinc, and bismuth blend for the "positive". With one end heated by fire and the other cooled in water, it was capable of an output of 55 mV [1].

Despite their long history, these TEGs were never widely adopted. They were briefly used in the 1920s to power radios in remote areas. However, rural electrification soon rendered them obsolete. One cause is their low conversion efficiencies. Compared with steam turbines capable of achieving 35% efficiency, TEGs typically come in under 5% [2]. While multistage systems were theorized to be capable of up to 20% [2], they are still outmatched by steam turbines for use in central power generation.

Despite their low efficiencies, TEGs have found use in niche applications where maintenance free, long-term operation is desired. TEGs require no moving parts due to their solid-state

transduction mechanism, giving them superb reliability .. For the last four decades [3], Voyager 2 has been continuously powered by a TEG heated using the radioactive decay of plutonium. The Soviet Union used TEGs to power remote light houses [4]. TEGs were even used in nuclear powered pacemakers [5].

In recent years, there have been renewed interest in utilizing TEGs for localized power generation from waste heat sources. Efforts to reclaim energy from oil flares [6], car exhausts [7], and in-home heating systems using TEGs are underway.

In the micro-electronics domain, the development of wireless sensor networks has created new opportunities for micro-scale power generation. It is in these applications where micro-scale thermoelectric generators (μTEGs) may finally achieve widespread use.

1.1 Micro-Thermoelectric Generators and Coolers

Micro-Thermoelectric Generators

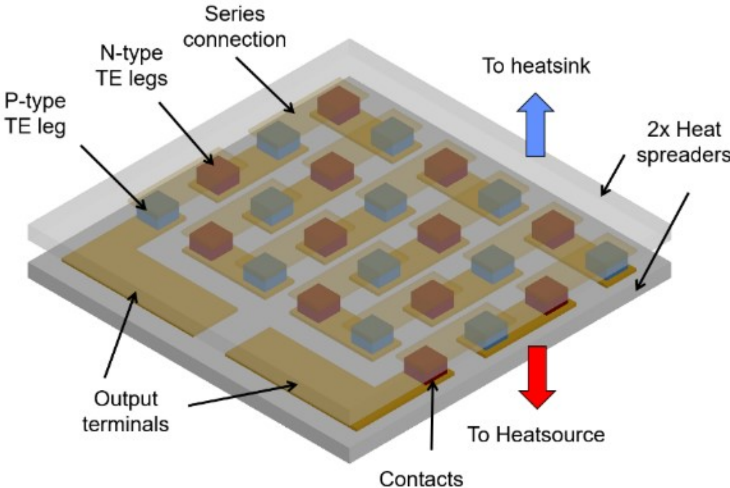


Figure 1-1: Diagram of a Standard Micro-Thermoelectric Generator

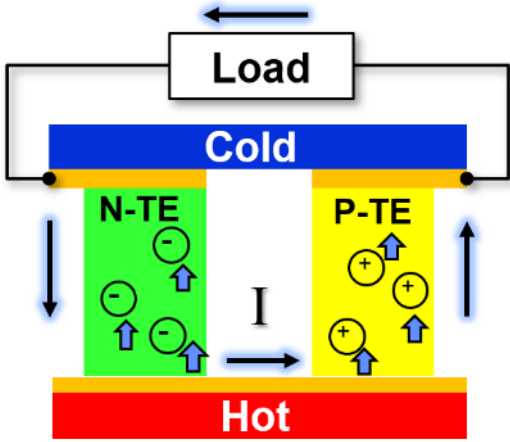


Figure 1-2: Carrier and current flow through a single thermoelectric leg-pair.

The core structure of a µTEG is composed of multiple N-type and P-type thermoelectric (TE) elements connected in series to improve voltage output. These elements are typically referred to as thermoelectric "legs". Unlike standard thermocouples, these N & P "legs" are not typically connected directly together to avoid diode formation. Instead, interconnects, typically composed of Au or Cu link the multiple N & P elements together [Fig. 1-1]. Alternating N-type and P-type TE legs allows power generation from both the hot-to-cold and the cold-to-hot thermal gradient introduced by the series connection. The TE material can be formed through a variety of methods, including evaporation [8], sputtering [9], screen-printing [10], electrodeposition [11], or attachment of bulk materials [12]. Due to its high thermal conductivity and ease of process integration, a silicon substrate is typically used as the heat spreader in µTEGs. For larger TEGs,

aluminum nitride [13],[14] is typically the heat spreader of choice, due to its higher thermal conductivity of 285 W/mK compared to silicon, at 100 W/mK.

The power output of a thermoelectric generator is proportional to the square of the temperature difference across the device. Thus, TEG performance is typically given in units of μW/K^2. Power density, the standard figure of merit (FoM) for μTEGs is given in units of μW/K^2/cm^2. However, this figure does not account for the thermal resistance of the device, which limits power output in real world situations. As the voltage output of the thermoelectric legs is proportional to the temperature difference across it, any thermal resistances in line with the legs function as a temperature divider and reduce output. This can include packaging, heatsink, thermal interfaces.

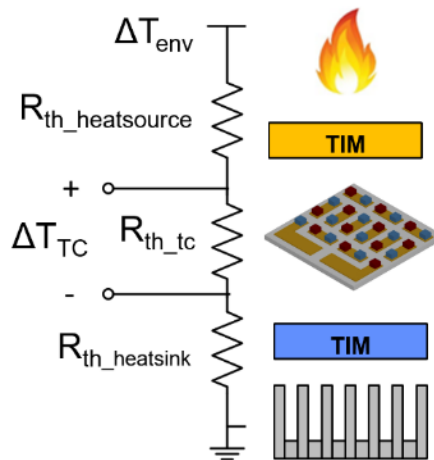


Figure 1-3: Basic heat path present in the TEG system

A low performance, high thermal resistance device can thus outperform a high FoM, low thermal resistance device given a large external thermal resistance. An example of one such demanding application would be powering a watch. Seiko's μTEGs used in their Thermic lines of watches anticipated an external thermal resistance on the order of 500 K/W [12]. Under such conditions their μTEGs could output roughly 1 μW with a given FoM of 5.6 μW/K^2/cm^2. Given the same conditions, the power output for Stanford's 1.5 K/W device would be less than .01 μW, despite their high device FoM of 120 μW/K^2/cm^2 [15].

Micro-Thermoelectric Coolers

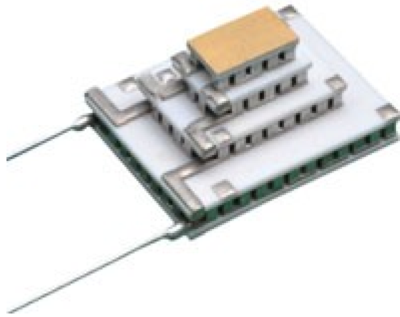


Figure 1-4: Stacked Thermoelectric Cooler from Marlow [78]

Micro-Thermoelectric coolers (μTECs) operate using the Peltier effect, a thermoelectric phenomenon related to the Seebeck effect where an applied current generates heat flow. They are arranged similarly to μTEGs, with multiple TE legs connected in series. The performance metric for TECs is known as the co-efficient of performance (COP), defined as the amount of heat pumped per unit of energy input. Like μTEGs, high thermal resistance across the device is desired, as low thermal resistance allows passive heat flow opposing the direction of the heat pump. This reduces efficiency and the maximum achievable temperature gradient across the device. For applications requiring low temperatures, μTECs are typically stacked (Fig. 1-4), with each proceeding stage larger than the preceding to compensate for excess heat generated through joule heating by the preceding stage.

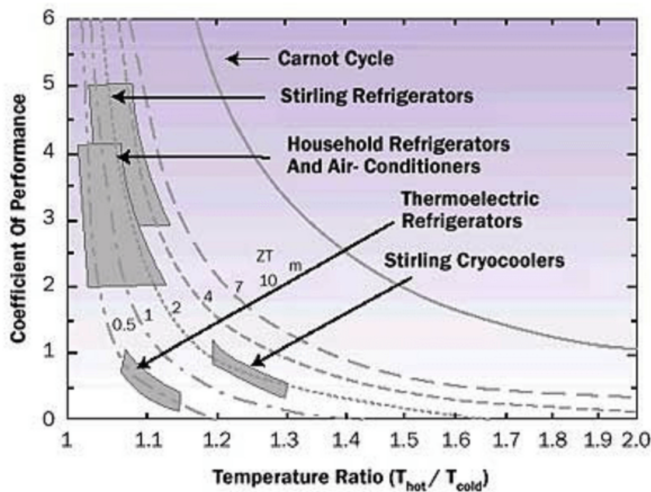


Figure 1-5: Coefficient of Performance (COP) of thermoelectric, compressor-based and Stirling refrigerators. [79]

While less than half [16] as efficient compared to conventional compressor-based refrigeration systems (Fig. 1-3), μTECs have the same advantages as μTEGs, namely size, simplicity, and robustness. Thus, they are often used in small-scale applications where reliable spot cooling is needed. They are commercially used to cool laser diodes, IR detectors, and small consumer

coolers. Currently, they are also being investigated for cooling hotspots in stacked semiconductors [17].

1.2 Emerging μTEG Applications

The low power demands of modern day micro-electronics and micro-sensors allow such devices to be powered solely through μTEGs. Potential applications of these sensor systems powered by μTEGs include wireless sensor networks for structural health monitoring, wearable electronics, and general internet of things devices.

The requirements of these μTEG differ from those of macro-scale TEGs intended for industrial power generation. Unlike space missions that can tolerate high per-unit costs, these applications require cost effective generators. Without dedicated heating systems, they must utilize much smaller pre-existing heat sources in their operating environment. Examples of such sources include utility pipes, solar heating, waste heat from exhaust systems and even the human body. Small form factors are also required to match the small size of their intended systems.

Given these requirements, μTEGs fabricated through micro-electromechanical systems (MEMS) processing techniques have come to the forefront of research. Using MEMS-based fabrication methods, small, compact μTEGs can be mass produced in a cost-effective manner.

1.3 Goals and Motivation

Due to advantages in production volume, cost and material usage, most commercial μTEGs [18],[13] use thin film techniques to deposit the thermoelectric material. However, the thickness limitation of thin film methods also limits the separation of hot and cold junction of the μTEG. This creates a low resistance thermal path across the active region of the μTEG, reducing the

temperature difference seen by the thermoelectric and thus performance. This effect is especially significant in emerging applications that require small form factors, as heatsink performance scales linearly with system size (Fig. 1-4). μTEGs with low thermal resistances are simply incompatible with such applications as the majority of power is lost from the heatsink and thermal interfaces.

Alternative TE deposition methods to create taller thermoelectric elements have been explored. However, these methods have their own associated drawbacks. Thick film deposition, such as electroplating [11] and screen-printing [10] allows for high thermal resistance but sacrifices material quality. Lateral designs sacrifice fill factor [19],[20] and suffer from substrate conduction [21]. Micro hot-pressed μTEGs, such as the one developed by Fujistsu, allow both thermal resistance and material quality at the cost of lower efficiency due to the thermal conduction of the mold [22].

The overall goal of this work is to allow practical thin-film based, micro-TEGs in form factors required for emerging energy harvesting applications. This is accomplished by increasing thermal resistance, giving greater compatibility in heatsink selection compared to traditional thin film designs.

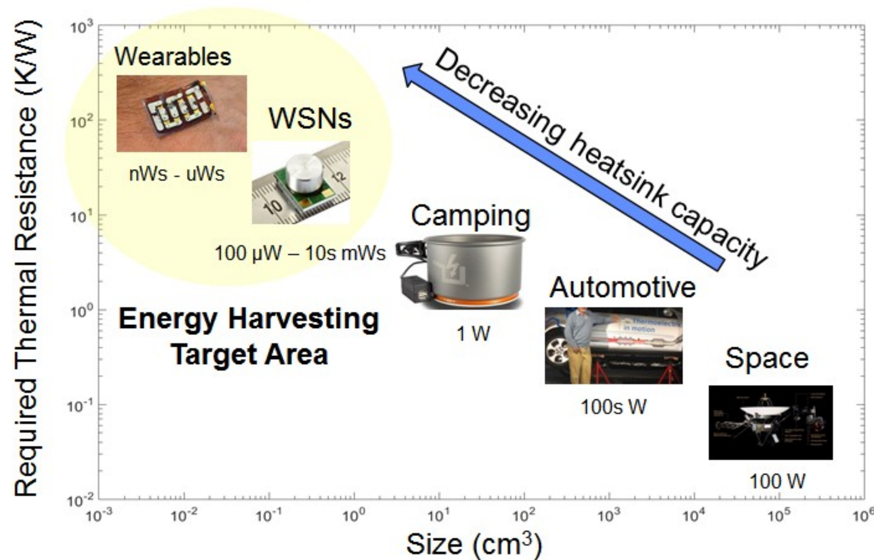


Figure 1-6. System size vs. Thermal required resistance

1.4 Thesis Contributions

This dissertation seeks to establish a new µTEG design that allows greater thermal resistance with thin-film thermoelectrics while maintaining the high fill factor of vertically oriented µTEGs. Thermal resistance is increased through improvement in thermocouple design, rather advancements in the properties of the thermoelectric materials used. In this design, the length of the thin-film based thermoelectric elements is increased using a novel thermocouple structure where the thin-films are deposited onto the sidewalls of dense, high-aspect scaffolds. Thereby, the length of the thermoelectric element and its thermal resistance is decoupled from the thickness of the thermoelectric film.

Detailed in this thesis is the technology required to make µTEGs utilizing this high-aspect thermocouple structure. Central to this design is the characterization and optimization of co-evaporated Bi_2Te_3 and Sb_2Te_3 films grown on vertical surfaces. Fabrication of functional µTEGs utilizing the novel thermocouple structure and the associated sidewall thin-films is achieved.

Thesis Contributions:

1. **Characterization of Bi_2Te_3 and Sb_2Te_3 thin films deposited over vertical surfaces**
    - **a.** Characterization of thermoelectric film growth over vertical scaffolds. The impact of the physical structure of the scaffold on film growth is evaluated. These scaffold variables include sidewall angle, scaffold pitch, height, and thermal conductivity. Differences in crystal morphology, composition, and electrical resistivity compared to films grown on planar surfaces are analyzed.
    - **b.** Optimization of vertical thermoelectric films with respect to thermoelectric properties. The effect of surface topology, substrate material, deposition temperature, material flux ratios, and the presence of a seed layer are investigated.
    - **c.** Investigation in to the limits of the deposition technique and their causes. This includes maximum height of the vertical surfaces due to thermal considerations, changes in crystal quality with increasing film thickness and shadowing effects caused by co-evaporation at different angles.
2. **Analysis of micro-thermoelectric generator designs under thermal constraints.**
    - **a.** Development of a Matlab model to calculate the performance of vertical thin-film μTEGs. Analysis on the effect of substrate material, thermocouple height, and fill factor on μTEG performance are presented and compared with the performance of traditional vertical μTEGs.
    - **b.** Analysis of μTEG optimizations given limited heatsink efficiency. Factors analyzed include including packaging considerations, thermal conduction through the scaffold and bond ring conduction.
3. **Fabrication of μTEGs with the vertical, high-aspect thermocouples**

a. High-aspect scaffold patterning and material selection. Thermally and electrically isolating scaffolds compatible with the growth of Bi_2Te_3 and Sb_2Te_3 thin films are reported. Scaffolds can be patterned over 20-μm tall with a 35-μm pitch.

b. Creation of electrical connections between successive Bi_2Te_3 and Sb_2Te_3 elements.

c. Development of other supporting fabrication technologies required for the successful integration high-aspect thermocouples into a μTEG. These technologies include patterning of Bi_2Te_3 and Sb_2Te_3 through shadow masks, formation of thermal contacts to Bi_2Te_3 and Sb_2Te_3 thermocouples, and die attachment.

1.5 Outline

This dissertation is organized into 9 chapters. Chapter 1 serves as an introduction to thermoelectric generators and the core goals of this work. Chapter 2 provides technical background on the thermoelectric phenomena and thermoelectric materials in general. The thermoelectric materials used in this work, Bi_2Te_3 and Sb_2Te_3 are introduced here. Chapter 3 provides analysis of μTEG performance, including common bottle necks and major sources of loss. This chapter provides additional rational on the necessity of the longer TE legs presented in this work. A limited review of published μTEGs is also included. Chapter 4 presents the design and analysis of the proposed high-aspect thermocouple structure. Benefits and drawbacks compared to convention μTEGs designs are discussed. Chapter 5 discusses the characterization of N-type Bi_2Te_3 and P-type Sb_2Te_3 thermoelectric films produced for this work. These films were produced using thermal co-evaporation. Optimal deposition conditions for depositions on planar

substrates is given. Analysis on the impact of substrate, temperature, deposition rate on film performance are also presented. In contrast to Chapter 5, Chapter 6 focuses on Bi_2Te_3 and Sb_2Te_3 based thermocouples deposited over vertical surfaces. Differences in the optimal deposition conditions for the planar vs vertical films are given. Potential causes for the performance discrepancy between planar and vertical films are also presented along with potential solutions. The impact of poorer film performance on the viability of the proposed μTEG design is also given. Chapters 7 and 8 focus on the integration of the developed sidewall thermoelectric films into a high-aspect μTEG. Chapter 7 targets the major fabrication steps involved in fabrication and provides the rationale behind the selected method of implementation. Fabrication based challenges that affect μTEG performance are also analyzed. Chapter 8 provides the complete fabrication steps of μTEGs utilizing both oxide and polyimide based scaffold on which vertical thermoelectric films are deposited. Encountered fabrication challenges, solutions, and potential improvements are given. Test results of the fabricated generators are also presented. Chapter 9 concludes the work. It summarizes the work accomplished and gives paths for further development of the high-aspect μTEGs presented in this thesis.

Chapter 2 Background on Thermoelectrics

This chapter provides background information on thermoelectric phenomenon, materials, and factors impacting their performance. The figures of merit (FoM) used for evaluating thermoelectric material performance are explained. An overview of select thermoelectric materials is also provided. In particular, the crystal structure and properties of bismuth telluride and antimony telluride are given. Bi_2Te_3 and Sb_2Te_3 are the N and P type thermoelectric materials used in this thesis.

2.1 Thermoelectric Phenomenon

The thermoelectric effect refers to three inter-related steady-state thermoelectric phenomenon: The Seebeck, Peltier, and Thomson effects. Together, they generalize the transduction mechanisms between steady-state temperature differences and the movement of electrons. Transient effects, such as pyroelectricity, function by a different mechanism and are not addressed here.

The Seebeck effect

When a steady-state temperature gradient is applied across a conductor, an electromotive force is generated across the element proportional to the magnitude of the temperature difference between the cold and hot ends. This proportionality constant is known as the Seebeck coefficient. Its value is defined as the difference between the electrical potential at the cold and hots ends divided by the difference between the temperature at the cold and hot ends (2.1).

$$\boldsymbol{\alpha_s = -\frac{V_H - V_c}{T_H - T_c}} \qquad \textbf{(2.1)}$$

Above, α_s is the Seebeck Co-efficient, V_H and V_C are voltages at the hot and cold ends, respectively. T_H and T_C are the temperatures at the hot and cold ends, respectively.

The magnitude of the Seebeck coefficient is typically lower than 20 µV/K for metals, and above 100s µV/K for thermoelectric materials of interest.

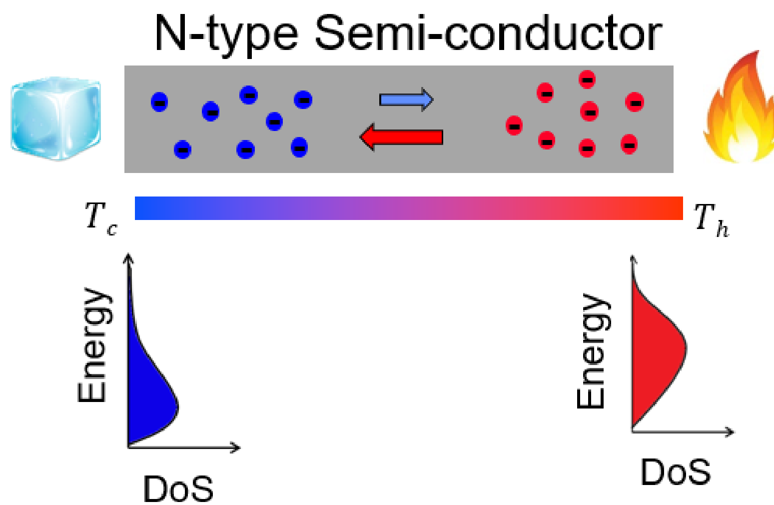


Figure 2-1: (Top) Electron movement in a thermoelectric material. (Bottom) Electron energy distributions at the cold and hot electron junctions.

This effect is caused by the diffusion current of hot and cold charge carriers within the conductor. Consider a bar of an N-type semiconductor, with one side heated and the other cooled. Electrons at the hot end are excited, preferentially occupying higher energy states compared to the cold side. This uneven electron distribution gives rise to diffusion currents, with hot carriers diffusing to the cold side and cold carriers diffusing to the hot side.

$$V_S = \alpha_s(T_H - T_C) \qquad \textbf{(2.2)}$$

Due to the energy dependent nature of electron collisions, and faster diffusion of hot carriers, the diffusion currents are unequal. This means typically the cold side will see a buildup of excess charge carriers under steady state conditions, generating an electrical field and potential difference across the hot and cold end. Thus, P-type materials typically exhibit positive Seebeck coefficients while N-type materials have negative values. The voltage generated is given by equation (2.2) above, which is a simple rearrangement of the terms in equation (2.1). This voltage does not depend on the temperature distribution across the material, only the temperature difference between the two ends.

This effect is considered a solid-state heat engine with the electrons as the working fluid. Thus, power generated by this effect is limited by Carnot efficiency given by equation (2.3) below.

$$\eta_c = \frac{T_H - T_C}{T_H} \quad (2.3)$$

Where η_c if the Carnot efficiency limit, T_H and T_C are the temperatures of the hot and cold reservoirs.

Peltier effect

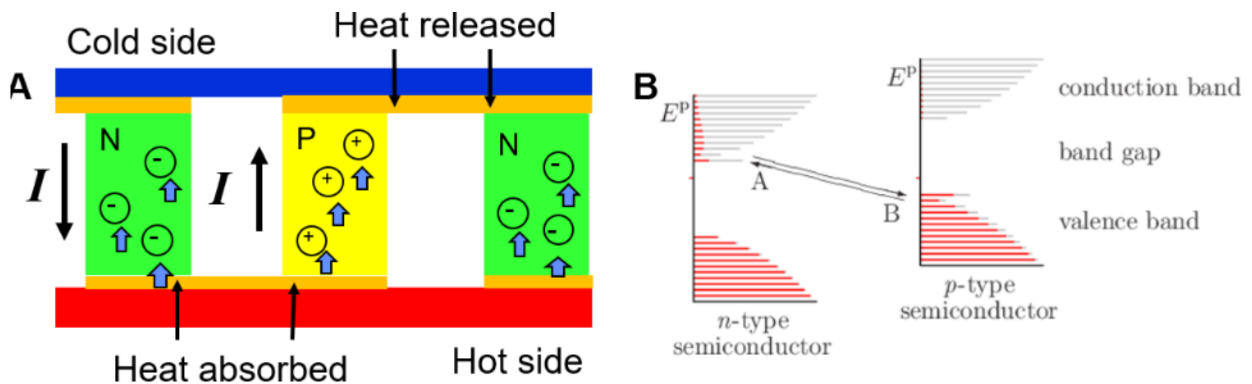


Figure 2-2: (A) Diagram of carrier movement in a thermoelectric device. (B) Electron movement between the N & P type semiconductor.

The Peltier effect can be thought of as the converse of the Seebeck effect. Whereas the Seebeck effect creates current in response to heat flow, the Peltier effect generates heat flow in response to an applied electrical current. This effect is caused by the movement of charge carriers between the valence band of a p-type material and the conduction band of an n-type material. As the two bands reside at different energy levels, thermal energy is transferred during this process. In TEGs, the Peltier causes heat flow from the hot to cold end, causing a self-cooling of the device and reducing power output.

The Peltier coefficient is the Seebeck coefficient multiplied by the temperature at the junction, given by equation (2.4) below. The rate of thermal energy change, Q, at the junction is given by equation (2.5) where Π_A and Π_B are the Peltier coefficients of the two materials and I is the applied current.

$$\boldsymbol{\Pi = \mathrm{T}\alpha_s} \tag{2.4}$$

$$\boldsymbol{Q = (\Pi_A - \Pi_B)I} \tag{2.5}$$

These equations hold true except in the case of strong magnetic fields or for magnetic materials.

Thomson effect

The Thomson effect manifests as a heat flow proportional to the magnitude of the temperature gradient across a conductor. It has the smallest magnitude of the three thermoelectric effects and is typically ignored in design considerations for thermoelectric devices. Its existence was first noted by Lord Thompson in the mid-19th century when he tried to resolve discrepancies between the measured and theoretical Seebeck voltages in a reversible thermodynamic system. The Thompson effect arises due to the temperature dependent nature of the Seebeck coefficient. As a temperature gradient exists along the length of a conductor heated at one end, the Seebeck

coefficient also varies across the conductor. This essentially causes a continuous version of the Peltier effect, carrying heat across the conductor. The Thomson coefficient is given by the temperature multiplied by the first derivative of the Seebeck coefficient with respect to temperature, shown by equation (2.6) below.

$$\mathbf{K} = \mathbf{T}\frac{d(\alpha_s)}{dT} \tag{2.6}$$

$$\dot{q} = -\mathbf{K}J * \nabla\mathbf{T} \tag{2.7}$$

Above, K is the Thomson coefficient, T is the temperature, and α_s is the Seebeck coefficient. Heat flow density, denoted by $\dot{q}$, is given by equation (2.7), where K is the Thomson coefficient, J is the current density, and ∇T is the gradient of the temperature.

Nernst–Ettingshausen effect

The application of a magnetic field perpendicular to the temperature gradient causes a potential to arise perpendicular to both the magnetic field and temperature gradient. This effect is due to the Lorentz force acting on carriers moving due to the Seebeck effect. This effect is typically not used in thermoelectric generators.

2.2 Thermoelectric Materials

Material Figure of Merits

The *power factor* of a thermoelectric material is proportional to its electrical power output for a given temperature difference. It is defined as the square of the Seebeck coefficient (α_s) of a material the over its electrical resistivity (ρ). It is analogous to the equation $P = V^2/R$ used to calculate electrical power.

$$\textbf{Power Factor} = \frac{\alpha_s^{\,2}}{\rho} \tag{2.8}$$

The figure of merit for Thermoelectric materials, known as *Z,* is the power factor of the material multiplied by the multiplied by the thermal resistivity (κ). For thermoelectric generators, efficiency increases with increasing thermal resistance. Additionally, larger thermal resistances also allow a greater temperature difference (ΔT) to be maintained across the device, increasing power generation.

$$Z = \frac{\alpha_s^{\,2}\kappa}{\rho} \tag{2.9}$$

To account for greater efficiencies and power generation at higher temperatures, the dimensionless figure of merit *ZT* is frequently used, which is simply *Z* multiplied by the optimal operating temperature.

Seebeck Coefficient

In metals, the Seebeck coefficient is related to the Fermi energy level and is given by [1].

$$\alpha_s = \frac{\pi^2 k^2}{3e} T \left(\frac{\mathrm{d}(\ln \sigma)}{\mathrm{d}E}\right) \tag{2.10}$$

Where k is the Boltzmann constant, σ is the conductivity, T is the temperature and e is electron charge. The Seebeck coefficient, α_s is also referred to as *thermopower*.

In semiconductors, the Seebeck coefficient is proportional to the difference between the average electron energy level and the lowest electron energy level, i.e. $E_c - E_f$ in N-type materials [23]. As E_f increases with carrier concentration, reducing the carrier concentration increases the

Seebeck coefficient. As with metals, the Seebeck coefficient is temperature dependent increasing with temperature up to a maximum. Past this maximum, the Seebeck coefficient decreases due to generation of minority charge carriers which exhibit a Seebeck coefficient of an opposing sign to the majority carriers. While not as numerous, the minority carriers exhibit a greater relative effect due to increased Seebeck coefficients at lower carrier concentrations [24].

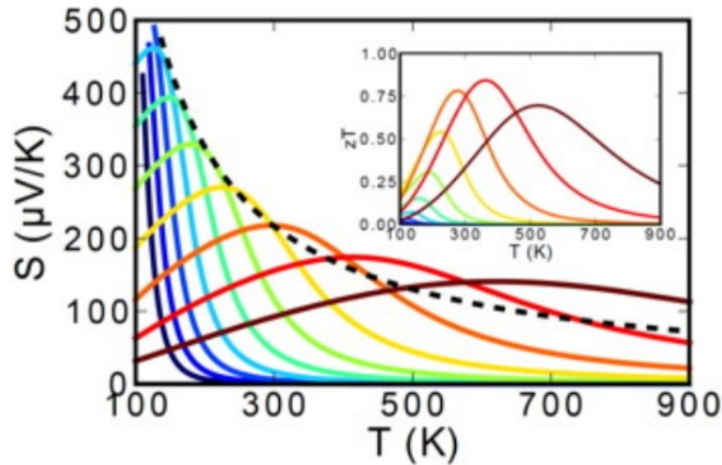


Figure 2-3: The Seebeck Coefficient as a function of temperature and doping level. Doping levels vary from lightly doped (dark blue) to heavily doped (brown) [24].

For semiconductors, the Seebeck coefficient can be approximated by the equation below (37).

$$\alpha_s = -\frac{k}{e}\left[\left(\frac{5}{2}+s\right)+\ln\frac{2(2\pi m^* kT)^{1.5}}{h^3 n}\right] \tag{2.11}$$

Where s is a scattering parameter, m^* is the effective carrier mass, h is Planck's constant and n is the carrier concentration. The scattering parameter, s, is affected by energy dependent scattering mechanisms as hot and cold carriers see different effective resistances due to differences in the electron collision rate.

Other than hot and cold carrier diffusion, phonon drag is another mechanism by which carriers can be driven by thermal gradients. Collisions during the movement of phonons from the hot to

cold ends of the conductor transfers momentum to electrons. However, this effect is only significant at about 1/5 of the Debye temperature. For reference, the Debye temperature for Bi_2Te_3, a common thermoelectric material, is 164.9 K [26]. Thus, phonon drag is not typically considered in room temperature thermoelectric devices.

Electrical Conductivity

The second component of power factor is electrical resistivity. This value is determined by two factors, the carrier concentration, n, and carrier mobility, denoted by u_n for electrons.

$$\rho = \frac{1}{q u_n n} \tag{2.12}$$

While an increasing carrier concentration is beneficial for ZT by reducing electrical resistivity, it reduces the magnitude of the Seebeck effect. Thus, there is an optimal carrier concentration for maximum ZT of a thermoelectric semiconductor. This value is typically between 10^{19} and 10^{21} /cm^3 [27].

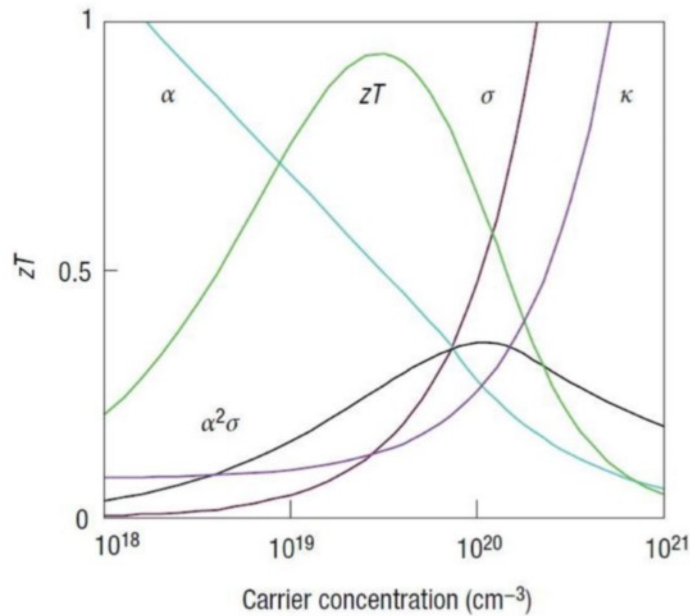


Figure 2-4: Thermoelectric Properties as a function of carrier concentration [27]

Carrier mobility is affected by crystal quality. For bulk materials and those grown by epitaxy, crystal quality is typically not a concern. However, for deposition methods that result in high defect densities or small grain sizes, losses in carrier mobility can noticeably affect thermoelectric performance. These deposition methods include common MEMS techniques such as sputtering, evaporation, electrodeposition or screen printing.

Thermal Conductivity

Heat flow in a material is caused by both lattice vibrations (phonons) and electron movement. The total thermal resistivity of a material is a composite of these two factors.

$$\frac{1}{\kappa} = \frac{1}{\kappa_{phonon}} + \frac{1}{\kappa_{electron}} \tag{2.13}$$

The thermal conductance due electrons cannot be reduced without affecting the electrical conductance and Seebeck coefficient of the material. Phonon conduction, however, can be tuned relatively independently from the electrical conductance and Seebeck. From figure 2-4, we can see that thermal resistivity, κ, does not change significantly below doping concentrations of $10^{19}/cm^3$. In this region, thermal conductivity is dominated by lattice vibrations. Thus, any reduction in the thermal conductivity of a thermoelectric material in this region should lead to a relatively linear increase in Z.

The thermal conductance due to phonons is given by below [28], where *C* is the phonon heat capacity per unit volume, *v* is the phonon velocity, and *l* is the phonon mean free path (MFP).

$$\kappa_{phonon} = Cvl \tag{2.14}$$

The MFP represents the average distance traveled by a phonon between momentum scattering collisions. The lower the MFP, the more thermally resistive the material.

2.3 Thermoelectric Materials

Thermoelectric materials are materials that exhibit high ZT values allowing them to be used for TEGs and TECs. Until the late 1990s, Bi_2Te_3 exhibited one of the highest FoM among such materials. In recent years, research into new thermoelectric materials have yielded significant advances in performance, surpassing Bi_2Te_3 (Fig. 2-5).

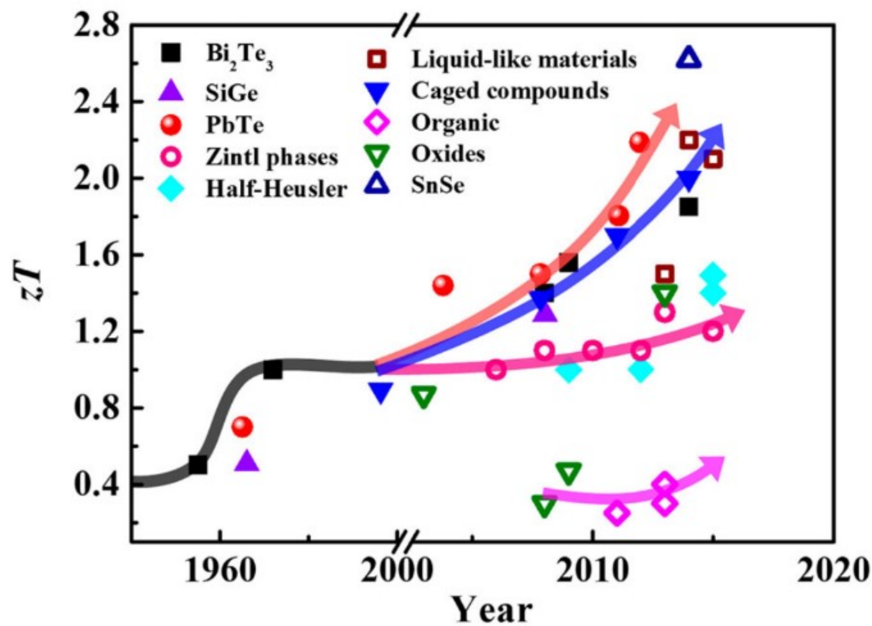


Figure 2-5: Maximum ZT values of thermoelectric materials by year [29].

However, despite advances in material performance, current high performance μTEGs still utilize Bi_2Te_3 and, to a lesser extent, Sb_2Te_3 as their thermoelectric materials. This is due to the superior room temperature performance of these materials in addition to integration difficulties of the new exotic materials into practical μTEG designs. In addition, as subsequent chapters show, significant μTEG performance improvements can still be achieved with Bi_2Te_3 based generators through design improvements. (make sure the table is not split across two pages)

Table 2-1: Reported High-Performance µTEGs

Author	N-Material	P-Material	Power Output ($\mu W/K^2/cm^2$)
Kouma[22]	Bi_2Te_3	Sb_2Te_3	18.3
Kishi[12]	Bi_2Te_3	Sb_2Te_3	5.6
Roth[11]	Bi_2Te_3	Cu	1.6
Böttner[18]	Bi_2Te_3	BiSbTe	2.4
Dunham[15]	Bi_2Te_3	Sb_2Te_3	120

Chalcogenides

Chalcogenides are materials containing at least one element from group 16 of the periodic table, with the exclusion of oxygen. The chalcogenides used in thermoelectric applications are predominantly semiconductors. They have good intrinsic thermal resistivities and thermopowers. Chalcogenides of note are N-Bi_2Te_3 and P-Sb_2Te_3, two industry stand materials exhibiting excellent room temperature performance. For high temperature applications, PbTe is widely used due to its temperature stability and high ZT. P-PbTe has been reported with a ZT of over 1.4 at 400°C [23]. A drawback of chalcogenide usage is the rarity of the elements used in the materials, especially Te and Se.

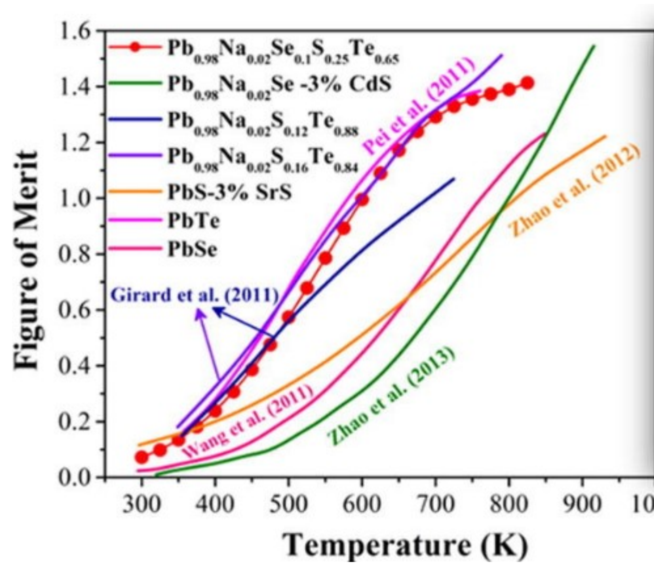


Figure 2-6: Reported ZT of various Pb based chalcogenides [59]

Bismuth telluride and Antimony Telluride

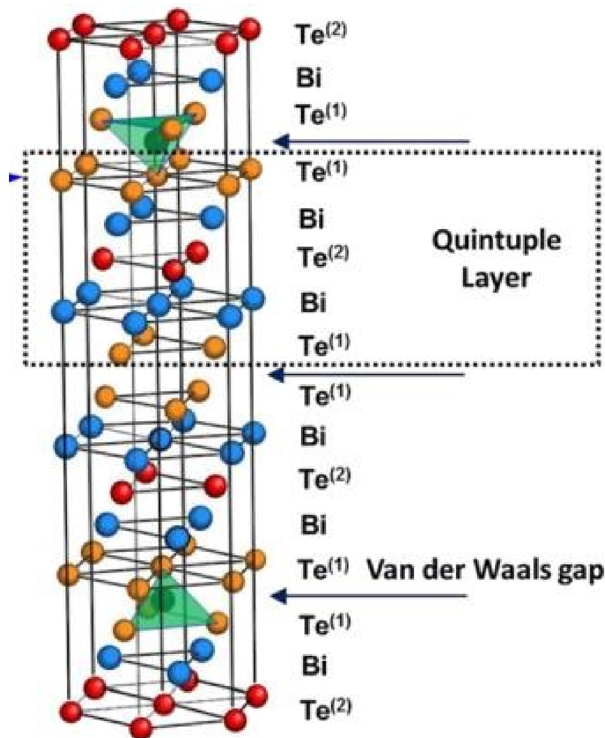


Figure 2-7: Structure of a Bi_2Te_3 unit cell.

Bismuth telluride (Bi_2Te_3) and antimony telluride (Sb_2Te_3) can have ZT values above 1 at room temperature. These two materials are widely used in room temperature TEGs and TECs.

Bi_2Te_3 has a rhombohedral crystal structure, composed of multiple layers of Bi and Te. While bonding between Bi and Te layers is strong, bonds between the successive Te layer is weak, being only held together through the Van der Waals force. This makes the material brittle and easy to cleave in the a-b plane.

The highly anisotropic crystal structure results in different thermoelectric properties across the a-b plane and the C-axis. For Bi_2Te_3, the in-plane [a-b plane] figure of merit Z is twice that of cross-plane performance, with a reported value of 2.9x10^-3 /K [54]. For Sb_2Te_3, the cross-plane performance is superior to in-plane, with a Z of 1.6 x 10^-3 /K cross-plane compared with .65x10^-3 /K in-plane [54].

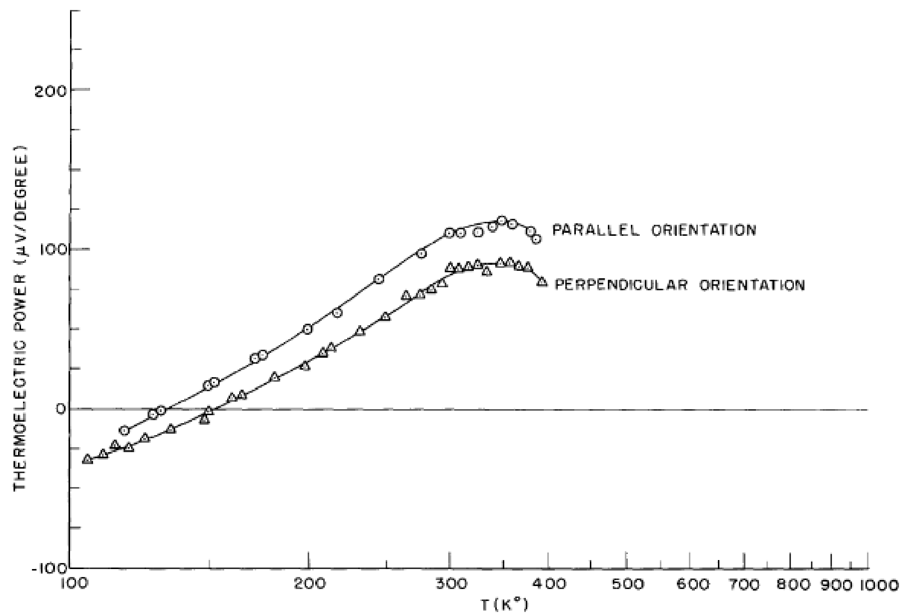


Figure 2-8: Seebeck (Thermopower) values of in-plane and cross-plane Bi_2Te_3 [49]

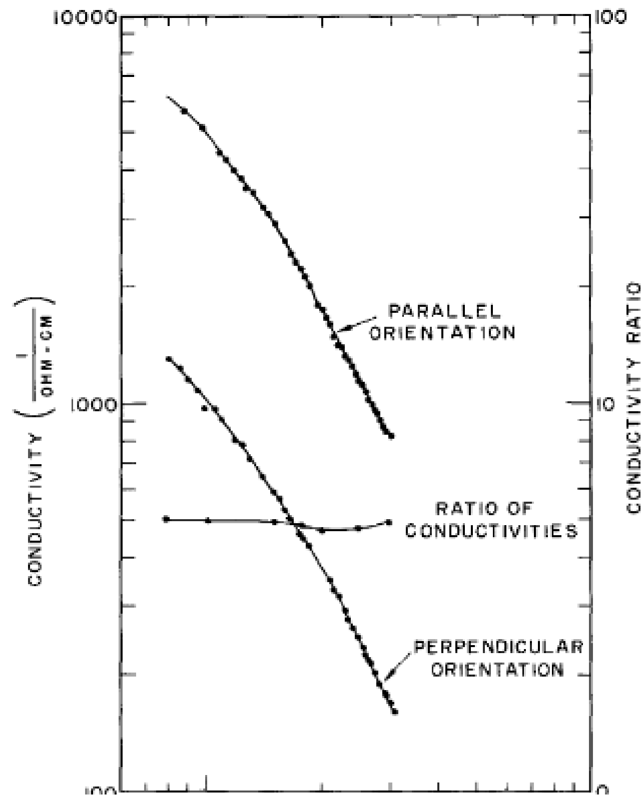


Figure 2-9: Conductivity of in-plane and cross-plane Bi_2Te_3 [49]

TAGS

TAGS materials are composed of materials with the elements Te/Sb/Ge/Ag. $AgSbTe_3$ itself is a good high temperature p-type thermoelectric material. It was found that alloying this material with GeTe increased thermopower, with optimal ratios in the 75 – 90% range [56]. TAGS is currently used in radioisotope TEGs for space applications by NASA and was used in the generator powering the Curiosity Mars rover.

Traditional Semiconductors

Silicon and SiGe are standard substrates used in the semiconductor industry. Due to their widespread use, they are readily available and well understood. They are capable of high temperature operation and exhibit moderate ZT values (< .5) at high (>600°C) temperatures.

However, the high thermal conductivity of the materials, a plus in the semiconductor industry, limits their use in room temperature thermoelectric applications. This is due to the difficulty of forming a temperature gradient across a highly conductive material. However, lowering the dimensionality of these materials have been shown to significantly increase thermal resistance [33].

2.4 Nanostructured Materials

One way to increase the ZT of thermoelectric materials is reduce the mean free path of phonons (MFP). As the MFP of phonons is considerably larger than that of electrons, this has the potential to improve thermal resistance without affecting the electrical properties of the material.

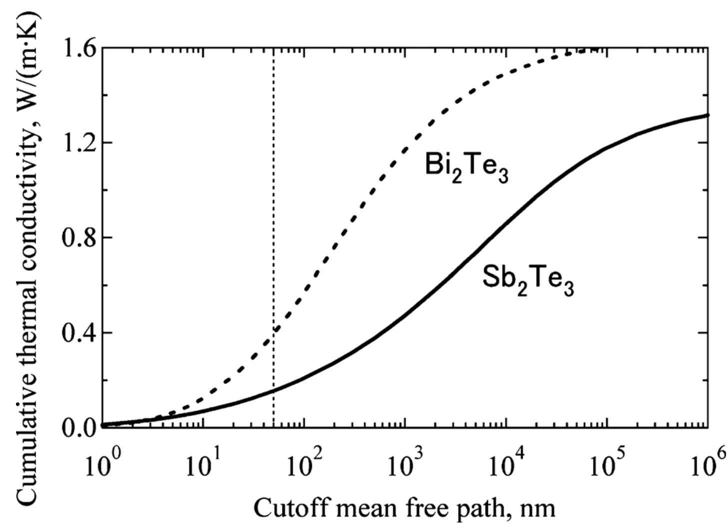


Figure 2-10: Thermal conductivity in Bi_2Te_3 and Sb_2Te_3 as a function of phonon mean free path [30]

Methods of doing this include creating porous materials [30] or through the use of superlattices [31], composed of alternating layers of different thermoelectric materials. Isoelectronic substitution, the replacements of elements with other elements with similar electron configuration, can reduce phonon transport without affecting electron movement. Inclusion of

defects, such as SiC into $Bi_{.5}Sb_{1.5}Te_3$ [61] have also been shown to improve thermoelectric properties.

Quantum Confinement

Other methods include reducing the dimensionality of materials, such as Si nanowires [32]. Lower dimensions improve thermal resistances [33] and quantum confinement effects can improve power factor [34].

Chapter 3 Micro-Thermoelectric Generators

This chapter provides insight into the design of micro-thermoelectric generators, and potential bottlenecks. The importance of high-thermal resistance in generators and its impact on power output is highlighted. Reported methods to achieve this resistance in µTEGs are also detailed, as well as the tradeoffs involved. A review of the performance of published µTEGs is also presented.

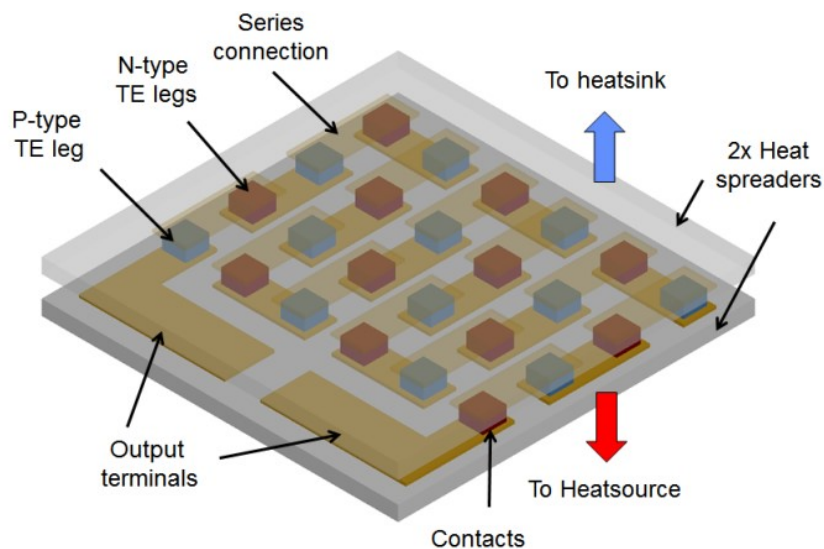


Figure 3-1: Standard Micro-Thermoelectric Generator

A µTEG has three main components: the thermoelectric elements, or “legs”, the electrical connections between the TE legs, and heat spreaders at the hot and cold ends of the device [Fig. 3-1]. The TE legs are typically connected in series to increase the output voltage in low temperature applications. The legs are composed of both N & P-type TE material to allow power

generation from both the hot-to-cold and cold-to-hot temperature gradients introduced by the series connection. The TE material itself can be formed through a variety of methods, including evaporation [8], sputtering [9], screen-printing [10], electrodeposition [11], or bonding of bulk materials [12]. Due to its high thermal conductivity, the silicon substrate is typically used as the heat spreaders in µTEGs, though AlN [13],[14] can also be used.

3.1 Ideal Generator Power Output

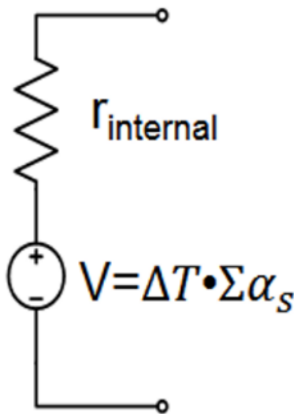


Figure 3-2: Simplified TEG electrical model

An ideal TEG can be modeled as a temperature-controlled voltage source in-line with the electrical resistance of the generator (Fig. 3-2). Voltage output is equal to the combined Seebeck coefficients of all thermoelectric elements connected in series multiplied by the temperature difference seen by the elements. The internal electrical resistance is simply the sum of the resistance of each individual thermoelectric leg, given a series connection. The total power generated is thus given by:

$$P = \frac{V^2}{r} = \frac{N\Delta T^2\left(\alpha_p - \alpha_N\right)^2}{r} \tag{3.1}$$

Where N is the number of thermoelectric leg-pairs, ΔT is the temperature across the thermoelectric legs, α_p and α_N are the Seebeck coefficients of the P and N type legs. Due to the quadratic dependence on the temperature difference, the TEG device figure of merit is typically given in units of µW/cm^2/K^2.

The internal resistance, r, can be expressed in terms of the number of thermoelectric legs, the resistivity of the thermoelectric, and the geometry of the thermoelectric leg. Assuming the geometry of the N and P legs are identical, this resistance is given by:

$$r_{internal} = \frac{N(\rho_N + \rho_P)}{2}\left(\frac{L_{leg}}{A_{leg}}\right) \tag{3.2}$$

Where N is the number of thermoelectric legs connected in series, and ρ_N and ρ_P are the resistivities of the N and P type TE material. $A_{leg,}$ denotes the area of the thermoelectric leg, this area is defined as the cross-sectional area of the thermoelectric leg perpendicular to current and heat flow. L_{leg}, or leg length, refers to the length of the thermoelectric element parallel to current and heat flow. For a µTEG with a vertical configuration, this "length" is the height of the leg perpendicular from the substrate. While from an electrical standpoint it is advantageous to make the leg height L_{leg} as short as possible, shorter legs cause greater thermal losses, as detailed in section 3.2.

Whether the TE leg-pairs are connected in series or parallel does not affect the power output of the device. If all leg-pairs were to be connected in parallel rather than in series, the reduction in voltage output would be compensated by the decrease in the electrical resistance of the TE legs, as all N legs / P legs would be connected in a single block. However, voltage conversion loses can have an impact on the power ultimately available in the µTEG system**.** To keep losses at a minimum, it is important to maintain voltage above the startup requirements of the converter. This necessitates a high density of thermoelectric legs connected in series for low-temperature applications.

Table 3-1: Required start up voltages for reported low voltage charge pumps [35]

Reference	Startup mechanism	Converter Topology	Ext. Parts	Startup Voltage	Input Voltage	Output Voltage	% Efficiency	Output Ripple	Area (mm^2)	Process
[3]	Charge pump	LCP (N=3)	None	270 mV	450 mV	1.40 V	58 %*	15 mV	0.42	130-nm
[6]	Charge pump with V_{TH} tuning	Inductor based	Cap.	95 mV	100 mV	0.90 V	72 %*	N/A	0.17	65-nm
[7]	Forward body biased charge pump	LCP, inductor	N/A	180 mV	180 mV	0.74 V	N/A	N/A	0.29	65-nm
[8]	N/A	ECP (N=3)	None	150 mV	150 mV	0.85 V	30 % (sim.)	N/A	N/A	65-nm
This work	Charge pump (I_L= 0.1 μA)	LCP (N=3)	None	125 mV	125 mV	0.35 V	65 (est.) / 62 % (sim.)	1.2 mV (I_L= 0.1 μA)	0.1	130-nm
		LCP (N=7)	None	125 mV	125 mV	0.61 V	59 (est.) / 51 % (sim.)		0.15	130-nm

* End-to-end converter efficiency

If the electrical resistivity of the P and N type materials are equal, and the Seebeck coefficients are of equal magnitude, but opposing signs, power output of a TEG can be simplified to:

$$P = \left[\frac{\alpha_s{}^2}{\rho}\right] \Delta T^2 \frac{NA_{leg}}{L_{leg}} \quad (3.3)$$

Here, the first set of terms is the *power factor* of the thermoelectric material. N•A_{leg}, represents the *effective area* of the thermoelectric film. Divided by the device area, this given us the *fill factor* of a TEG, a measure of area efficiency for a TEG design.

$$\text{Fill Factor} = \frac{Effective\ Area}{Device\ Area} \quad (3.4)$$

Efficiency is given by the ratio of electrical power output divided by the thermal energy input at the hot end of the TEG. This can be written in terms of the TE figure of merit Z [1]:

$$\boldsymbol{\eta} = \left[\frac{T_H - T_C}{T_H}\right]\frac{\sqrt{1 + ZT_A - 1}}{\sqrt{1 + ZT_A} + T_C/T_H} \tag{3.5}$$

Where η is the efficiency, T_H, T_C, and T_A are the hot, cold, and average temperatures seen by the thermoelectric. Z is the thermoelectric figure of merit.

As TEGs are heat engines, they are limited by the Carnot efficiency, given by the first set of terms in the equation. This means that for a room temperature TEG with a hot side 10 K above ambient, efficiency is capped at 3%, even using a hypothetical perfect material with an infinite figure of merit. For many scavenging applications, this low efficiency is not a concern, as the heat source is assumed to be very large compared to the magnitude of the heat losses through the body of the µTEG.

3.2 Source of Loss

Given the same thermoelectric materials, fabricated µTEGs show greatly reduced power output compared to the ideal case. Losses in a non-ideal µTEGs system can reduce output to less to 10% of the theoretical values.

Thermal Losses

A major source of loss in a µTEG system is unwanted thermal pathways which reduce the effective ΔT across the thermoelectric legs. These resistances can be either in series or parallel to the thermoelectric legs. The series resistances act as a temperature divider, lowering ΔT. Examples of such resistances include: the heat sink, the substrate, µTEG packaging, and thermal interfaces. Resistances parallel to the thermoelectric legs further increase this temperature divider effects by lowering the effect thermal resistance of the TE legs themselves (Fig. 3-3). These resistances include air convection and bond rings.

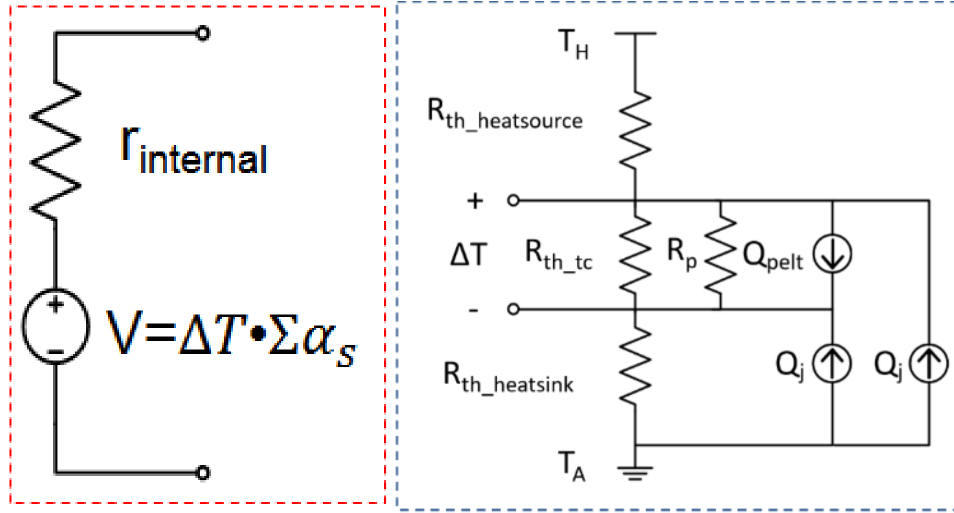


Figure 3-3: (Left) Electrical model and (Right) thermal model for a μTEG.

In the figure above, Q_{pelt} is the heat flow due to Peltier cooling and Q_j represents heat generated from joule heating. R_{th_tc} is the thermal resistance of the TE legs, R_p represents the sum total of all thermal resistance in series with the TE legs, and $R_{th_heatsink}$ and $R_{th_heatsource}$ are the thermal resistance to the heatsink and heatsource, respectively. T_H and T_A are the temperature of the heat source and the thermal ground.

Temperature across the thermoelectric legs can be written as:

$$\Delta T = (T_H - T_A)\frac{R_{th_tc}//R_p}{R_{th_tc} + R_{th_{heatsink}} + R_{th_heatsource}} \tag{3.6}$$

$$P_{actual} = P_{potential}\left(\frac{R_{th_tc}//R_p}{R_{th_tc} + R_{th_{heatsink}} + R_{th_heatsource}}\right)^2 \tag{3.7}$$

Here $T_H - T_A$ represent the total temperature difference available in the environment. As ΔT is only a fraction of that value, potential μTEG power output is thus reduced. An example of this temperature drop can be seen from a testing set up reported by Stanford [15], where the

temperature measured across the active thermoelectric material was less than 5K compared to a total temperature difference of ~19 K.

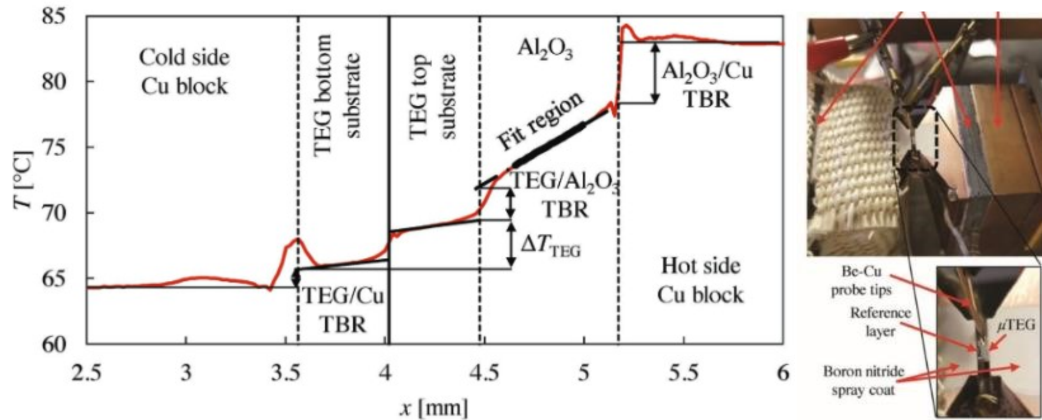


Figure 3-4: Temperature profile across a μTEG testing system [15]. Total temperature range from 64 °C on the cold end to 83 °C on the hot end. Only about 5°C is dropped across the thermoelectric material. Additionally, the cooling set up, (right) is extremely large in comparison to the actual μTEG.

During operation, TEGs also undergo self-cooling due to the Peltier effect pumping heat with the thermal gradient, further contributing to the reducing of ΔT. Additionally, joule heating within in the device can also decrease ΔT. However, for room temperature devices operating with low efficiencies, this impact is typically small.

Electrical Resistance

Another source of loss is the contact resistance of the thermoelectric legs to the routing metal. In an ideal TEG, the electrical resistance of the device is solely determined by the resistivity of the thermoelectric material and the TE leg geometry. Typically, the electrical resistivity of TE material is low to maximize the figure of merit, Z. However, without an accompanying low contact resistivity, the contacts represent a major portion of the total device resistance.

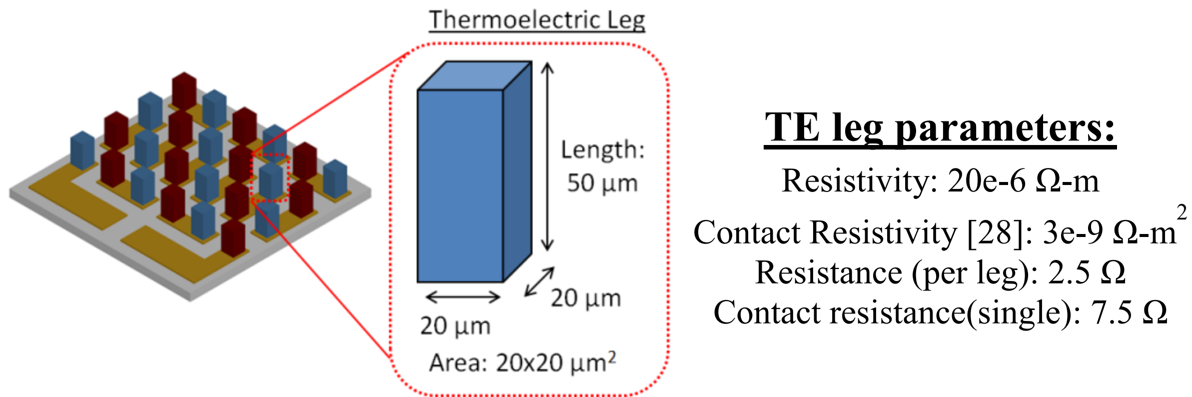


Figure 3-5: Example Dimensions of a TE Leg and Resistances

For example, take a TEG leg with a height of 50-µm. Assuming Bi_2Te_3 as the TE material with a resistivity of 20 uΩ-m and a contact resistance of 3e-9 Ω-m^2[28], contact resistance accounts for 75% of the total resistance of the structure. This reduces the potential output of the TEG to 25% of its theoretical value. In thin-film based µTEGs with short TE leg heights, this loss is proportionally greater due to the low resistance of shorter legs. Additionally, for very short legs, the metal routing between successive TE legs can also represent a major source of additional electrical resistance.

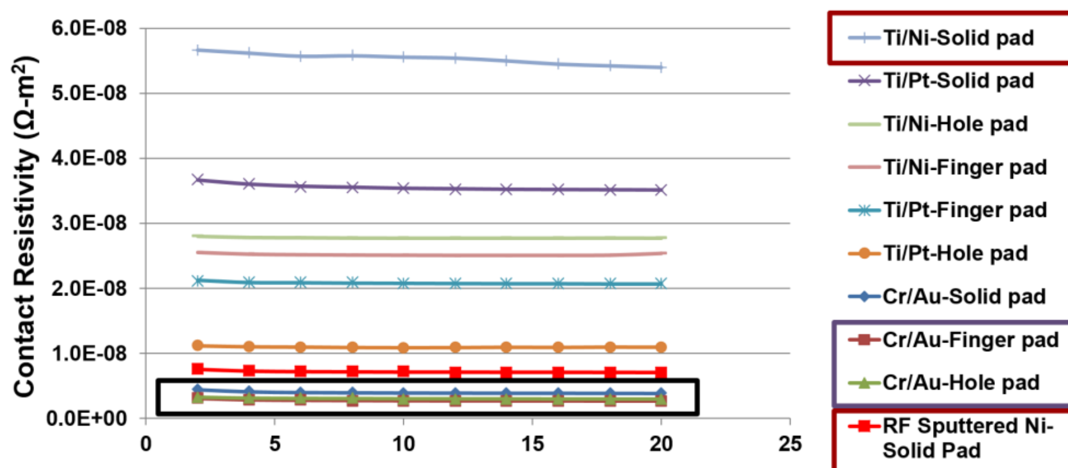


Figure 3-6: Contact resistance of Bi_2Te_3 to various metals [28]

3.3 Optimal µTEG Leg Dimensions

The thermal resistance of the TE legs of an ideal TEG is determined by the geometry of the leg itself along with the thermal resistivity of the thermoelectric material, κ.

$$R_{th_tc} = \kappa \frac{L_{leg}}{NA_{leg}} \qquad \mathbf{3.8}$$

For greater ΔTs across a TEG, it is desirable to have tall thermoelectric legs with a small effective area. However, this is the opposite of the desired configuration for low electrical resistance, as shown in equation 3.3. The power-ΔT relationship is quadratic, but the power-electrical resistance relationship is linear. This implies an optimal thermal and electrical resistance exists, and thus an optimal leg geometry exists to maximize power generation. For vertical µTEGs, this occurs when the thermal resistance across the TE legs equals the total resistance of all other thermal resistances in series with the TE legs, shown in equation 3.9 below.

$$\frac{1}{R_{th_tc}} + \frac{1}{R_p} = \frac{1}{R_{th_tc} + R_{heatsink+}R_{heatsource}} \qquad \mathbf{(3.9)}$$

This resistance can be achieved by modifying either the height of the TE legs, L_{leg}, or the effective area, NA_{leg}. From a manufacturing standpoint, modifying L_{leg} rather than NA_{leg}. Is desirable as reducing NA_{leg} decreases the power density of the device. For wafer-based MEMS devices, reducing effective area also increases the cost/watt of the device, as costs are proportional to device area. Thus, NA_{leg} should be maximized while scaling L_{leg} to achieve maximum power generation.

3.4 The Need for Longer Thermocouples (TE legs)

In a typically µTEG system, the air – heat sink junction typically has the highest thermal resistivity. This is due to the poor thermal conduction of air compared with solids. Therefore, the optimal height of the TE legs is mostly determined by the heatsink resistivity.

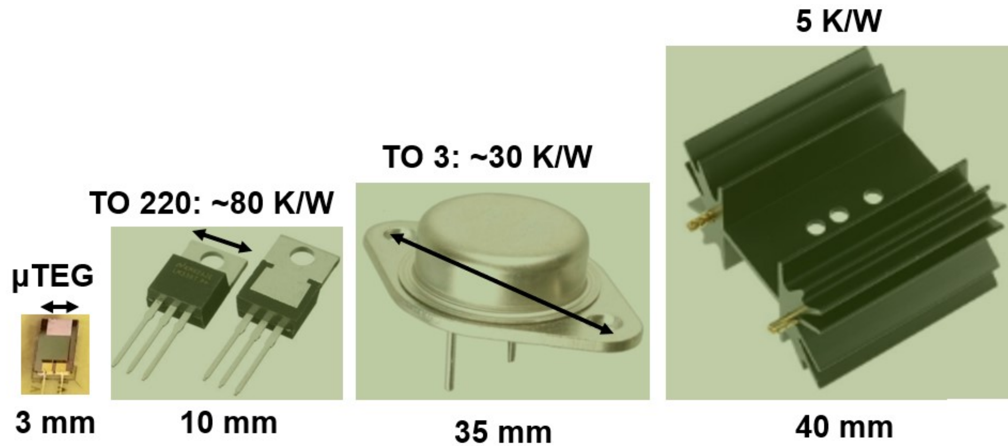


Figure 3-7: Heatsink-Air junction resistances of select Heatsinks

Typical heatsinks used in electronics packaging have thermal resistances of 5 K/W and above. For an ideal Bi_2Te_3 based µTEG with a 20% fill factor, the optimal thermocouple leg height is over 25-µm tall.

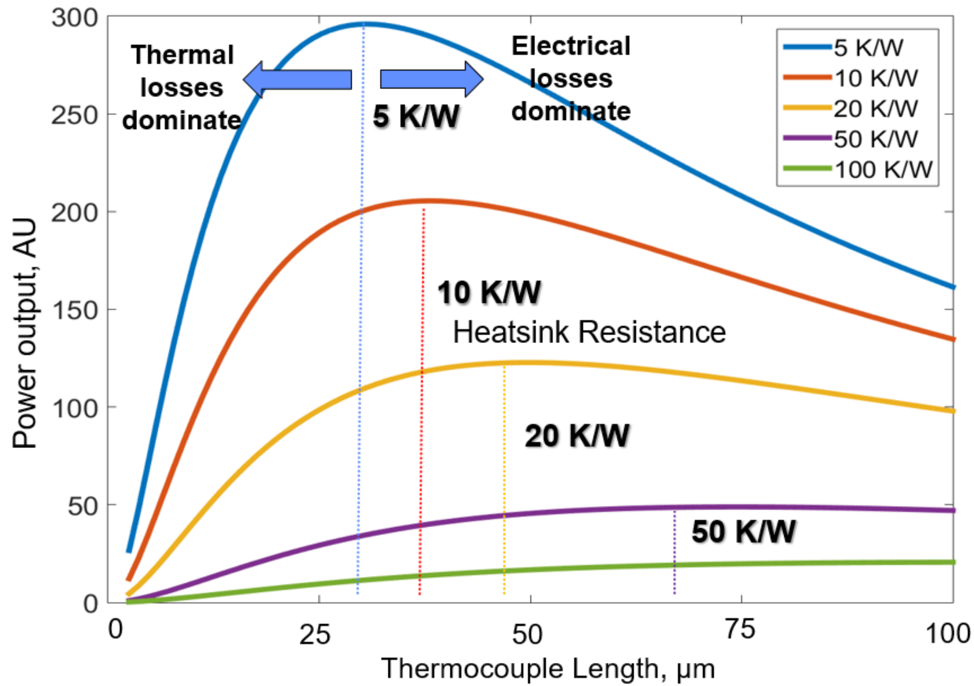


Figure 3-8: Power output of a µTEG as a function of TE leg length (height) and heat sink resistance. µTEG is Bi_2Te_3 based with a 20% fill factor.

As heat sink size shrinks, the height requirement for the thermoelectric legs further increases. For a heatsink resistance of 20 K/W, the optimal TE leg height is almost 50-µm. This poses difficulties for thin film designs, due to thickness limitations of the deposition technique. This issue is especially evident for body heat harvesting, where thermal resistances of over 200 K/W [12] can be necessary.

3.5 High-thermal resistance designs

Two approaches can be taken in order to achieve the necessary thermal resistances. The first approach is through design. By switching from a vertical to lateral configuration, long thermoelectric legs over 100s of microns long can be created. In this way, µTEGs with high thermal resistance can be created independent from film thickness limitations. However, this approach causes a critical reduction in the fill factor of the device, with a corresponding loss in

power output (Fig 3-11). The second approach is through alternative deposition methods. Keeping a standard vertical μTEG configuration (Fig. 3-9), long thermoelectric legs are created by abandoning thin-film depositions methods in favor of thick film-methods capable of creating the necessary thermocouple length. These methods include electrodeposition, screen printing, even bonding of bulk TE materials onto the substrates.

Lateral Designs

In a lateral μTEG, the heat flow runs parallel to the substrate surface, rather than perpendicular for vertical designs. This approach switches the geometric constraints of the thin-film thermoelectric legs from length limited to area limited. Here, length and area used the same definitions as in equation 3.2. While removing the length limitation allows high thermal resistances, a constraint on area lowers the fill factor of the device. Practically, this greatly increases the electrical resistance of the device. Additionally, unlike vertical designs, lengthening the TE legs on a lateral μTEG uses up more area, reducing the leg density.

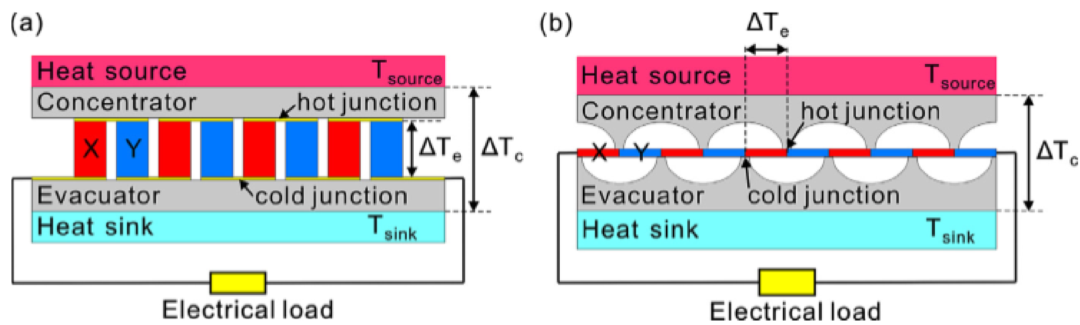


Figure 3-9: (Left) Vertical TEG configuration. (Right) Fabricated lateral TEG from [20]

In lateral designs, thermal conduction through the substrate is also a concern. While this substrate can be removed underneath the thermoelectric, this process creates additional process complexity. For packaging purposes, the lateral configuration also complicates heatsink

attachment as there is no large, flat surface readily available. For these stated reason, lateral μTEGs designs are typically far outperformed by their vertical brethren (Fig. 3-11).

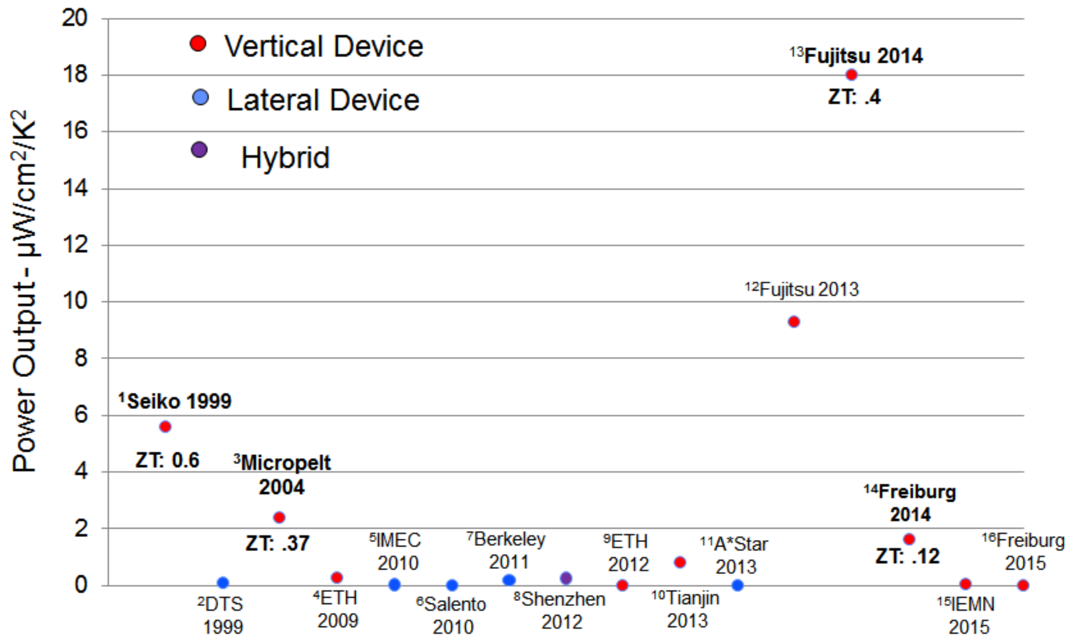


Figure 3-10: Reported Performance of Select Micro-Thermoelectric Generators

To improve the output of lateral devices, researchers [14],[36] have arrayed multiple lateral structures together to increase power density. While power output is improved, these hybrid arrayed designs still have trouble reaching the fill factor of true vertical designs, and thus power output still lags behind vertical devices (Fig. 3-11). Arrayed designs also incur a large increase in fabrication complexity and expense.

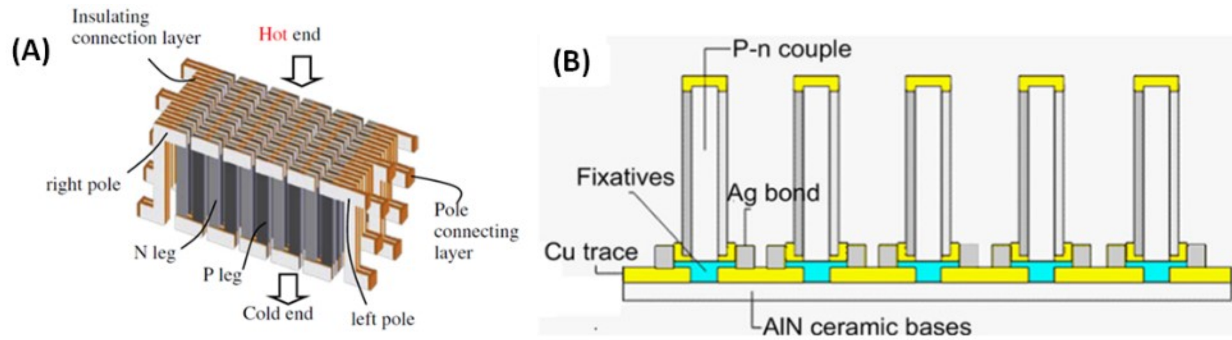


Figure 3-11: µTEGs composed of an array of lateral designs from (A) Shenzhen [36] and (B) Tianjin [14]

Alternative Deposition Methods

Another way to reach to necessary TE leg lengths is to forgo the use of thin-film altogether. Alternate thermoelectric film deposition techniques exist that allow thicker films, such as screen-printing [37],[10] and electrodeposition [11]. While these techniques allow high fill factor and sufficient thickness for good thermal impedance, they are often limited by the material quality. TE material deposited through electrodeposition [11] have power factors up to four times lower than material through thin film evaporation [8], while reported screen printed films [10],[38] have power factors lower by an order of magnitude. Furthermore, while cheap, screen-printing limits TE leg density, hindering their application in low temperature scavengers due to their low voltage output [8].

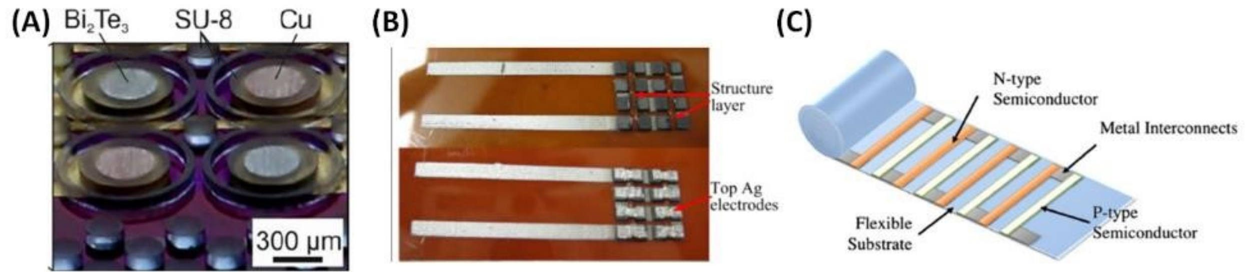


Figure 3-12: µTEGs utilizing thick film processes (A) Electroplated µTEG from Frieburg[12] and screen printed µTEGs from (B) Southampton[77] and (C) Berkeley [10]

Another developed thick-film method was micro-hot pressing. Hot pressing is a standard process for the creation of high-quality bulk TEs where Bi_2Te3 powder is placed into molds and heated

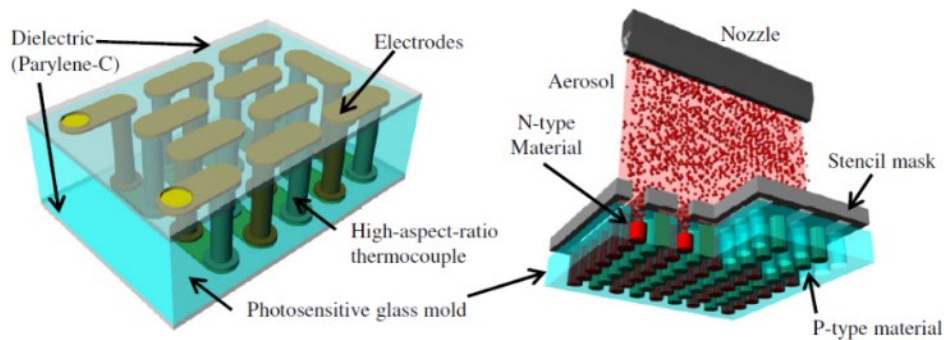


Figure 3-13: Deposition of TE material via Aerosol Spray and Hot Pressing [39]

under pressure to form a solid block. This method was successfully miniaturized by Tsuboi and Kouma[22][39]. The resulting device has achieved an impressive µTEG FoM to date of 18.3 $\mu W/K^2/cm^2$. However, the inclusion of the glass mold into the final design introduces a significant heat path, reducing the proportion of thermal energy passing the thermoelectric itself, and thus lowering power output and efficiency.

Bulk thermoelectric materials can also be directly integrated onto micro-fabricated µTEGs via bonding. Seiko's [12] µTEG for wrist watches is one notable example**.** The use of bulk allows superior material properties [10] compared to thin films and well as thermal resistance in excess

of 300 K/W [12]. However, this method is expensive compared to traditional MEMS process techniques and thus may not meet the cost requirements of many WSN and IoT applications.

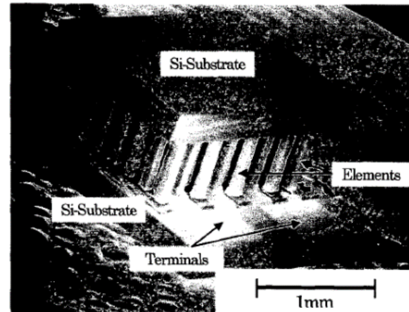


Figure 3-14: Bulk material based μTEG for wrist watches. Kishi [12]

3.6 Reported μTEGs

A comparison of μTEGs reported in literature is listed below. Of note, the majority of reported μTEGs use Bi_2Te_3 and Sb_2Te_3, and vertical orientations typically outperform lateral configurations. As thermal resistance is not often reported, it is difficult to compare such device performance in systems with limited heatsinks.

Table 3-2: Reported µTEGs in Literature. Chapter Specific reference at listed in section 3.10.

#	Author	N-TE	P-TE	Deposition/Type	Orientation	ΔT	Power	Size	FOM	Leg length
						K		mm^2	$\mu W/K^2/cm^2$	um
[21]	Francioso	Bi_2Te_3	Sb_2Te_3	Sputtered	Lateral	40	32 nw	2100	9.5 E-7	2000
[18]	Böttner	Bi_2Te_3	Bi_2Te_3	Sputtered	Vertical	5	670 nw	1.12	2.4	20
[36]	Fan	Bi_2Te_3	BiSbTe	Sputtered	Stacked Vertical	60	20 µW	-	-	640 (est)
[40]	Stark	Bi_2Te_3	Sb_2Te_3	Sputtered	Stacked Lateral	40	97 µW	68	0.089	2800 (est)
[20]	Yuan	PolySi	PolySi	LPCVD	Lateral	23	7 µW	30	0.045	70
[19]	Su	PolySi	PolySi	-	Lateral/Angled	25	420 nW	-	0.027	10 (est)
[41]	Li	SiGe	SiGe	Nanowire	Vertical	70	.47 µW	25	3.80E-04	1.1
[42]	Yu	PolySi	PolySi	LPCVD	Lateral	52	15 µW	9	0.252	50 (est)
[43]	Glatz	Si	Si	Electrodeposition	Vertical	20.4	-	-	0.25	120
[11]	Roth	Bi_2Te_3	Cu	Electrodeposition	Vertical	39	2338 µW	1(est)	1.63	80 - 135
[14]	Wang	BiSeTe	BiSbTe	Electrodeposition	Stacked Lateral	20	78 µW	25	0.78	3600
[12]	M.Kishi	Bi_2Te_3	BiSbTe	Bulk	Vertical	-	22.5 µW	4	5.6	600
[9]	Ghadfouri	Bi_2Te_3	Sb_2Te_3	Bulk	Lateral	11	.8 µW	8	6.60E-03	2000
[38]	AChen	Bi_2Te_3	Sb_2Te_3	Printed	Stacked Lateral	20	10.5 µW	-	0.187	5000
[10]	Cao	Bi_2Te_3	Bi_2Te_3	Printed	Vertical	20	2.62E-02	400 (est)	1.64E-05	500
[39]	N Kouma	Bi_2Te_3	BiSbTe	Hot Press	Vertical	30	720 µW	9	9.3	300

3.7 Commercial Devices

Over the last decade, numerous µTEGs have been commercially available. Notable among these include those produced by Micropelt, Nextreme/Laird, and RMT Ltd. All these devices utilized Bi_2Te_3 based-thermoelectric materials. However, each device used different deposition methods for their thermoelectric film. Micropelt's generators used a thick, sputtered TE film of Bi_2Te_3 packaged using a silicon substrate.

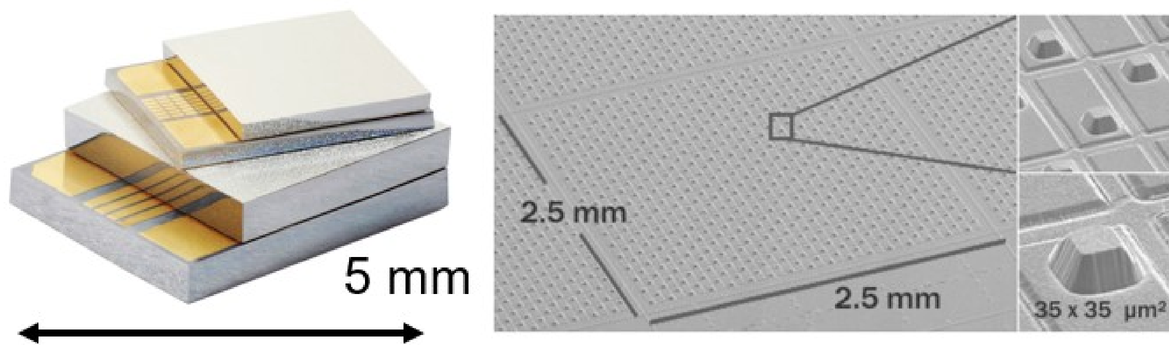


Figure 3-15: Micropelt MPG Series µTEG. (Right) Close up of TE legs.

Nextreme, and later Laird, used thin-film based TE. Package thermal resistivity for these devices was reduced by using an aluminum nitride heat spreader rather than a silicon one.

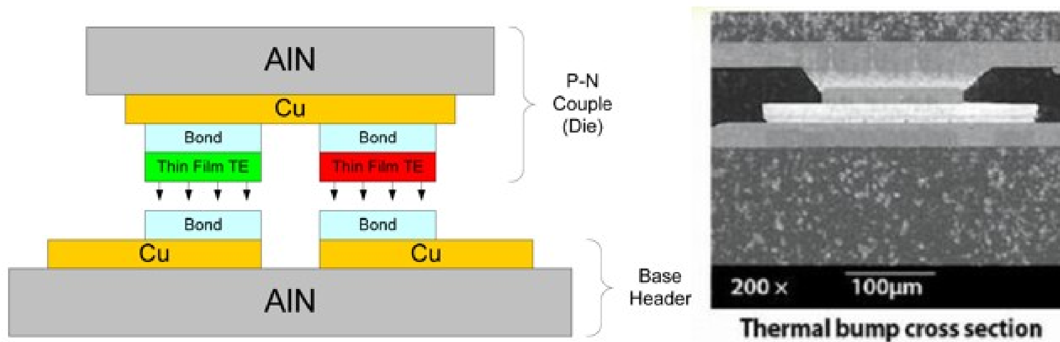


Figure 3-16: Thin Film µTEG from Nextreme

RMT Ltd. bonded convention bulk Bi_2Te_3 onto miniature ceramic substrates and patterned the TE material into legs through dicing.

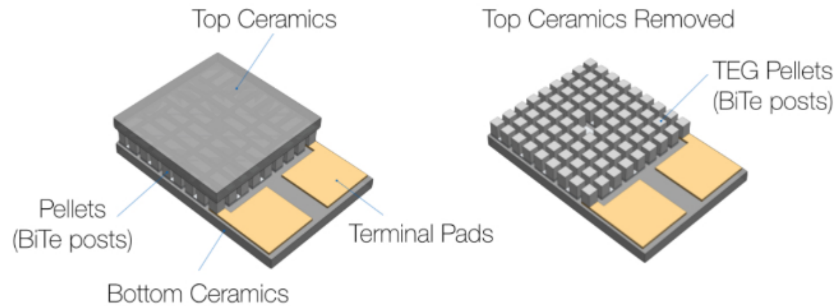


Figure 3-17: µTEGs from RMT Ltd.

Performance of these µTEGs, derived from their datasheets, is provided below. Unfortunately, these product lines are defunct as of this writing, and the thermal characteristics of these devices cannot be easily attained. A TEG from Marlow, TG12-2.5-01LS is provided below for comparison. This TEG is a macro-scale device created from bulk Bi_2Te_3 and Sb_2Te_3.

Table 3-3. Derived µTEG performance of Commercial µTEGs. The Marlow TG12 is a standard, bulk Peltier cooler.

Device	Electrical Resistance (Ω)	Matched load Voltage (mV/K)	Matched load Current (mA/K)	Figure of Merit (µW/K^2/cm^2)	Size
Micropelt MPG-D655	210 Ω	40	.38 mA/K	95	6.9 mm^2
Laird eTEG PG37	10 Ω	12	1.2 mA/K	221	6.5 mm^2
RMT 1MD-03-024	3.1 Ω	2.3	52 mA/K	24	12.6 mm^2
Marlow TG12-2.5-01LS	8.75 Ω	16	1.8 mA/K	12.5	900mm^2

3.8 Conclusion

The power output of a μTEG is determined by primarily four factors: the performance of the thermoelectric material itself, the contact resistance between thermoelectric material, the thermal resistance of the thermoelectric legs, and the device fill factor. Of these four factors, only the first is unaffected by the μTEG design. Thus, the power output of a μTEG can be increased by optimizing the latter three factors independent of material performance. Current thin-film based generators have difficulty meeting thermal resistances required for optimal generator output. This is due to limitations on thermoelectric leg length imposed by the deposition method. Lateral μTEG designs remove this resistance limitation at the cost of significant reductions in fill factor. In the ideal case, neither fill factor nor thermal resistance should be sacrificed. What is desired is a thin-film μTEG design that removes the leg length constraint while maintaining fill factor.

Chapter 4 High-Aspect Vertical Thermocouples for use in µTEGs

This chapter presents a novel, thin-film µTEG design that allows for high thermal impedance capabilities without sacrificing fill factor. Benefits and drawbacks of this design, and estimated performance improvements over traditional designs are presented.

4.1 Improving Micro-Thermoelectric Generator Performance

While there have been advancements in µTEGs output in recent years, current levels of performance are still markedly below material limits for even standard thermoelectric materials such as Bi_2Te_3 and Sb_2Te_3. A hypothetical µTEG using the optimal design geometry of Freibrug's [11] electroplated generator and a moderate film ZT of .4 [8] has the potential to achieve a power output of well over 100 $\mu W/K^2/cm^2$ with thermal resistances over 30 K/W. (Fig. 4-1). This level of performance is something current devices fall well short of. (Table 4-1)

Table 4-1: Comparison of reported Vertical Thermoelectric generators.

	Rth	Size	FoM (uW/K2/cm2)	Avg. Film ZT
Fujitsu[22]	17.1	9 mm^2	9.3	.4
Seiko[12]	~600	4 mm^2	5.6	.6
Freiburg[11]	.59	1 mm^2	1.63	.12

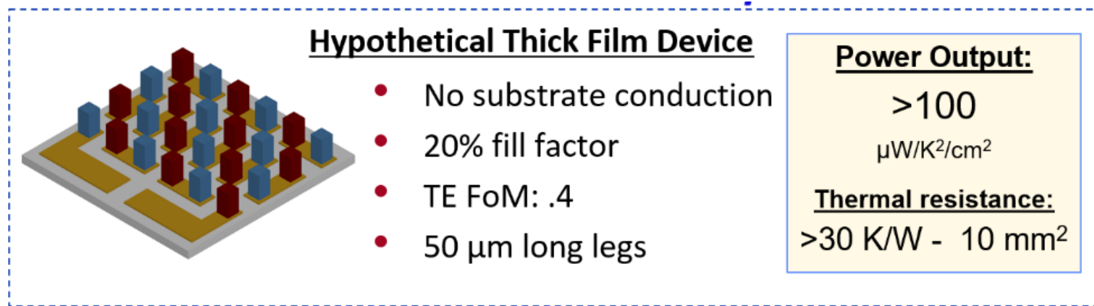


Figure 4-1: Estimated performance of a thick film μTEG

Thus, the current generation of μTEGs are not so much limited by the performance of their thermoelectric material, but rather by their design. To achieve the optimal design dimensions, research has been focused on improving the material properties of thick TE films that can achieve the optimal leg geometry. However, an alternate improvement path lies with removing the geometric limitations of thin films. We believe it is possible to achieve the large fill factors and long TE legs possible with thermoelectric thick films by depositing thin films over tall, vertical surfaces. This would allow good separation and thus thermal isolation between hot and cold junction, while maintaining the good material properties and manufacturing advantages of thin films.

4.2 High-Aspect Vertical Thermocouples

This thesis presents a new, thin-film μTEG design that allows for the high thermal impedance capabilities by way of increased thermoelectric element length. In the proposed μTEG design, thin film thermoelectric material is conformally deposited over dense, high-aspect scaffolds (Fig. 4-2), forming our TE legs. Fill factor is maintained due to the high density of the scaffolding, which increase the area available for film deposition. As the TE leg height is determined by the

height of the scaffold rather than the thickness of the film, the structure allows thermocouple lengths of over 25-µm using films as thin as 1-µm.

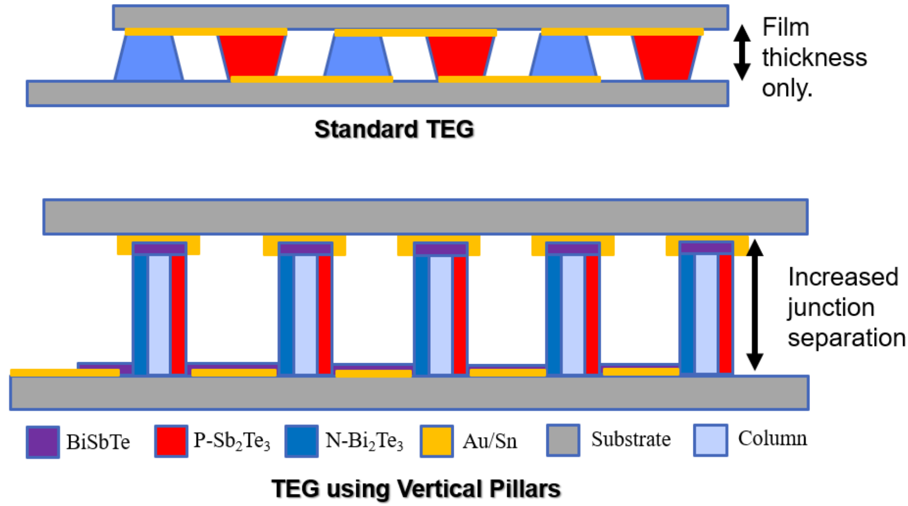


Figure 4-2: µTEG Design using high aspect scaffold. Vertical (A) and Lateral (B) µTEG designs provided for comparison.

The key elements required for successful fabrication of the device are: creation of high-aspect, thermally insulating vertical pillars compatible with film growth, vertical film deposition over the sidewall surface, formation of electrical connection between successive N and P elements, and die bonding. These elements will be discussed at length in the proceeding chapters.

4.3 Modeling

In order to efficiently model the impact of various design choices on µTEG performance, a model of the µTEG was created based on heat flow across the µTEGs. The heat absorbed at the cold end of a thermoelectric leg can be approximated by:

$$\mathbf{Q_C = \alpha I T_C - R_{leg}(T_H - T_C) - \frac{1}{2} r I^2} \quad \mathbf{(4.1)}$$

Where T_H and T_C are the temperature are of hot and cold ends of the thermoelectric leg, R_{leg} is the thermal resistance across the hot to cold ends of the thermoelectric, I is the current, and r is the electrical resistance of the leg itself, its contact, and the connection to other TE legs. Correspondingly, the heat released at the hot end is given by:

$$\mathbf{Q_H = \alpha I T_H - R_{leg}(T_H - T_C) + \frac{1}{2} r I^2} \quad \textbf{(4.2)}$$

In the above set of equations, the first group of terms represent the heat flow due to the Peltier effect. The second is thermal conduction through the thermoelectric and the third is the contribution from to joule heating. The thermal resistance, R_{leg}, is composed of the thermal paths through the TE materials, its scaffolding, potential bond rings/package leakage and air convection. The current, I, is generated by the Seebeck effect and is given by:

$$\boldsymbol{I = \alpha_s (T_H - T_C)/r} \quad \textbf{(4.3)}$$

As there is no closed form solution to the above equations, the system was solved numerically in Matlab. To verify the Matlab model, an FEM simulation of two TE leg-pairs was created in COMSOL. COMSOL was not used to simulate the full µTEG due to memory constraints. Thermal resistance, electrical resistance, current and voltage were within 10% of each other.

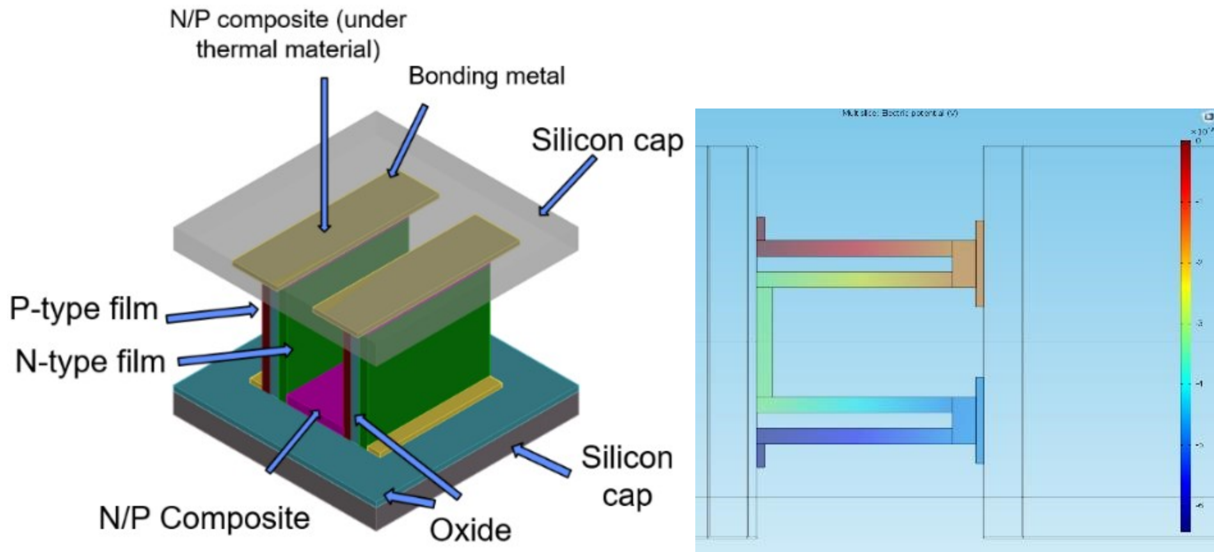


Figure 4-3: TE leg pairs in COMSOL (Right) Voltage output.

Table 4-2: Film parameters used for Comparison

Parameters	Length	Film thickness	Seebeck µV/K	Resistivity	Thermal Resistivity	Contact Resistivity[28]
N-Bi_2Te_3	25 µm	2 µm	-250	20 µΩ-cm	1.3 W/mK	2 nΩ-m^2
P-Sb_2Te_3	25 µm	2 µm	150	30 µΩ-cm	1.3 W/mK	2 nΩ-m^2

Table 4-3: Comparison of Matlab and COMSOL models

Parameter	Matlab	COMSOL
Thermal Resistance	**61.6 K/W**	**69.7 K/W**
Elec. Resistance	**20.8 Ω**	**22.9 Ω**
Hot Junction Temperature	**302.4 K**	**302.7 K**
Cold Junction Temperature	**295.4 K**	**294.5 K**
Voltage (OC)	**5.88 mV**	**6.30 mV**
Voltage (matched load)	**2.79 mV**	**3.09 mV**
Current	**0.133 mA**	**0.135 mA**
Power	**0.37 µW**	**0.42 µW**

Model Parameters

To more accurately model µTEG performance, the power factors used in the model were taken from measurement of Bi_2Te_3 and Sb_2Te_3 films created in our evaporator system. Details of the evaporation process are provided later in Chapter 5. A thermal resistivity of 1.5 W/mK[44] was assumed for both Bi_2Te_3 and Sb_2Te_3 films. Contact resistivity for Bi_2Te_3 to Au was previously measured at 3E-9 Ω-m^2. This same value was assumed for Sb_2Te_3.

Table 4-4: Thermoelectric Properties of Bi_2Te_3 and Sb_2Te_3 used for modeling

Film	Resistivity µΩ-m	Seebeck µV/K	Power Factor mW/K^{2}m	Thermal Resistivity. W/mK	ZT	Contact Resistance Ω-m^2
Bi_2Te_3	12.38	-212	3.63	1.5[44]	.72	3E-9[28]
Sb_2Te_3	20.6	166	1.33	1.5	.26	3E-9

In the model, the top and bottom substrates are composed of 500-µm of Si with a 1-µm oxide layer facing the thermocouple. The topside thermal contact is formed with 2 microns of an Au-Sn eutectic. The routing metal at the bottom of the structure is formed through 500 nm of Au. The composite (purple) film is assumed to be twice the thickness of the N and P type films combined and have properties that are an average of the N and P films.

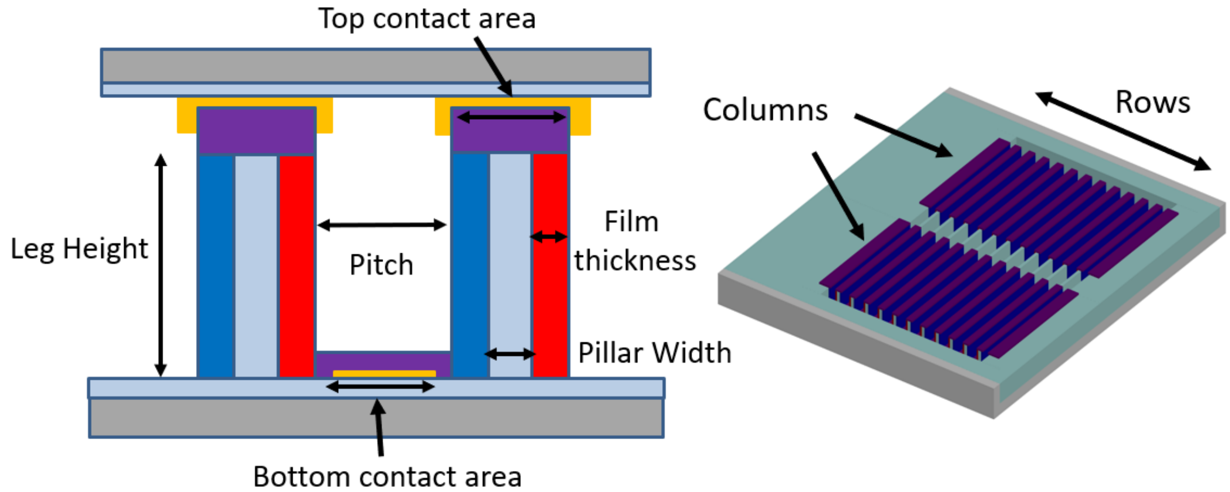


Figure 4-4: Geometric Parameters considered in µTEG design.

Modeled Output

The performance of a 3x3 mm^2 µTEG with oxide pillars with the following parameters is given below. A 1 K/W thermal resistance was assumed to exist between the device and the heat source.

Table 4-5: Geometric µTEG parameters

Parameter	N Film Thick.	P Film Thick.	Pitch	Leg Height	Pillar width	Columns
Value	2 µm	2 µm	25 µm	20 µm	2 µm	2

Table 4-6: Modeled µTEG performance.

ΔT (Total)	ΔT (Across TE legs)	Total Leg Resistance	Package Resistance	Elec. Res.	Voltage	Power	Figure of Merit	Size
10 K	6.42 K	4.7 K/W	2.5 K/W	141 Ω	103 mV/K	760 µW	**86 µW/K^2/cm^2**	3x3 mm

Using moderate films with an average ZT of .49, the vertical thermocouple design is capable of a figure of merit of 86 µW/K^2/cm^2 and a thermal resistance of 6.4 K/W. This level of power output is close to that of an idealized given in Fig. 4-1, though the thermal resistance is lower. This

figure of merit is far greater than the 18.3 μW/K^2/cm^2 reported by Tsuboi [22]. The potential power output is not as high as the traditional thin-film 135 μW/K^2/cm^2 reported by Dunham[15] of 135 μW/K^2/cm^2 , but the high-aspect design has a thermal resistance 4 times higher at 6.4 K/W vs 1.5 K/W[15] for the traditional thin-film device. The impact of this higher thermal resistance can be seen when the modeled μTEGs attached to imperfect heatsinks. Though the traditional thin-film μTEGs with a 1.5 K/W thermal resistance has a figure of merit almost twice and high as the 4.7 K/W μTEG, at an external heatsink resistance of 5 K/W, the relative performance is switched, with the 4.7 K/W device outperforming the 1.5 K/W by almost a factor of 2. This is due to the lower temperature difference across the traditional thin-film device in the presence of external thermal resistances. This factor is not accounted for in the μTEGs figure of merit.

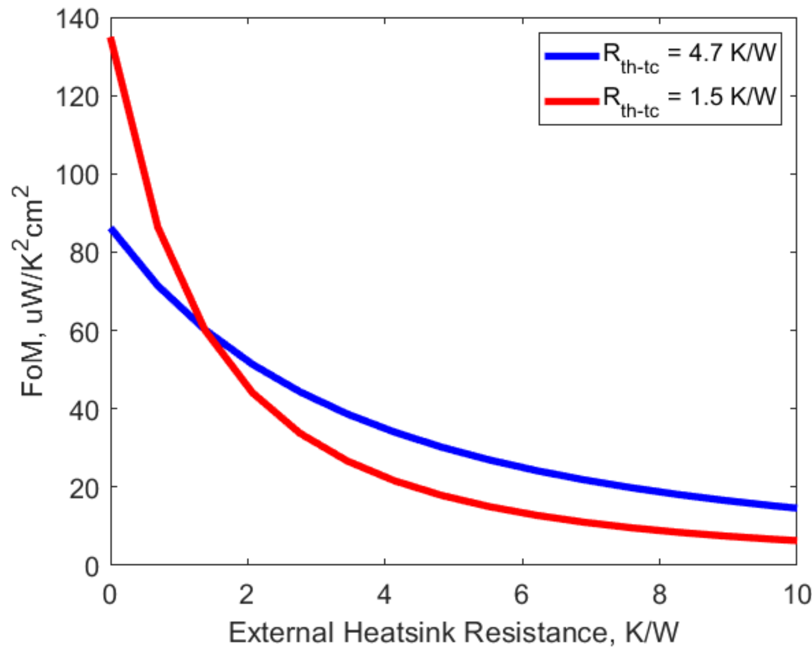


Figure 4-5: Power output of two μTEG as a function of external heatsink resistance. $R_{th\text{-}tc}$ refers to the thermal resistance of the thermocouples only. A 2.5 K/W packaging resistance is used for the 4.7 K/W device while a 0.5 K/W packaging resistance is used for the 1.5 K/W device.

Optimal Leg Height and Film Thickness

The design parameters of a µTEG must be optimized to the target heatsink. As given by equation 3.8, the correct ratio of TE leg height to fill factor must be maintained to achieve optimal µTEG performance. In our design, TE leg height is controlled by the height of the oxide scaffold while fill factor is proportional to the film thickness. For a pitch of 20-µm, fill factor is simply the sum of the N & P sidewall film thickness multiplied by 5.

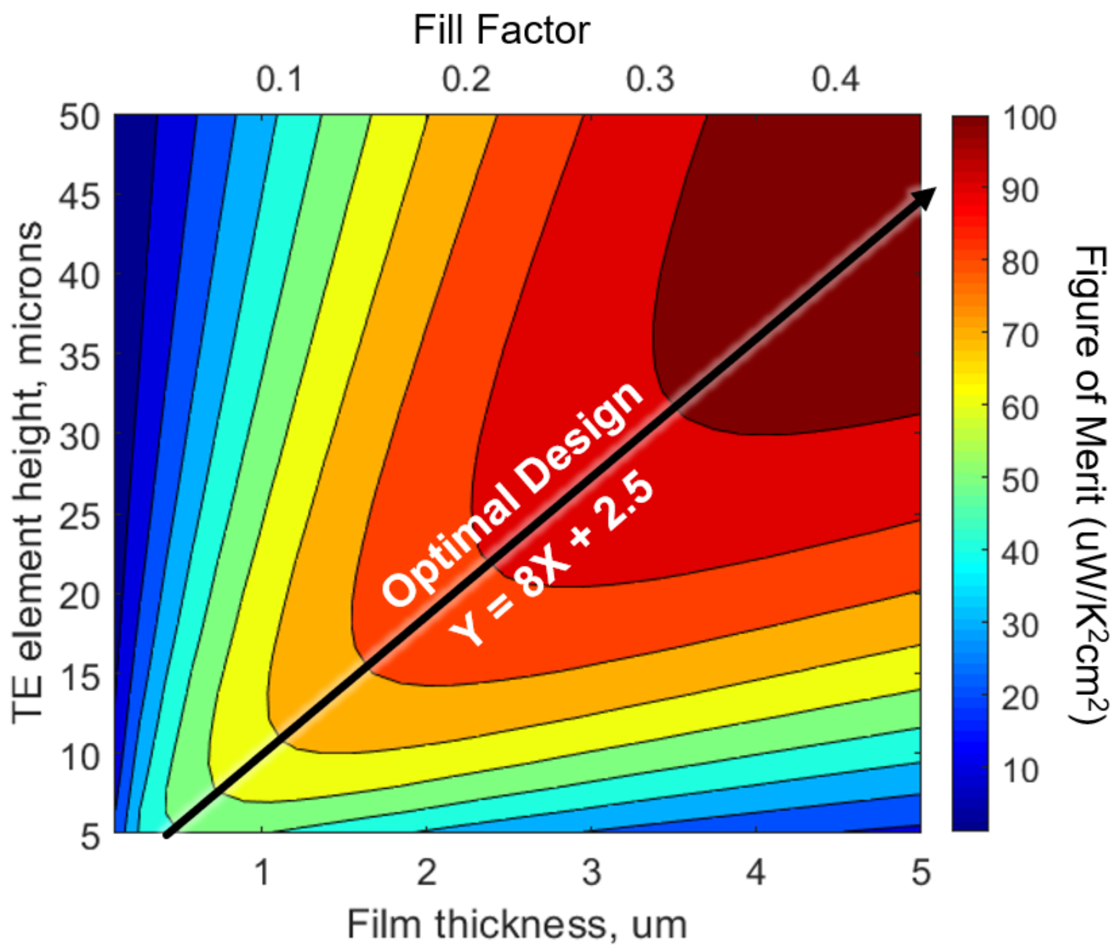


Figure 4-6: TEG FoM as a function of Fill factor and TE leg height. Temperature is measured directly across the two ends of the µTEG device. On the X-axis is the average thickness of the N and P type films on the sidewalls. On the Y-axis is the leg height of the thermocouples.

From the graph, we can clearly see the optimal ratio of film thickness to TE leg height. Along this line, electrical and thermal losses are matched, giving the optimal performance for a given TE material. For any point along this line, performance decreases moving left due to the increase in electrical resistance. Performance decreases moving down due to decreased ΔT from low thermal resistances

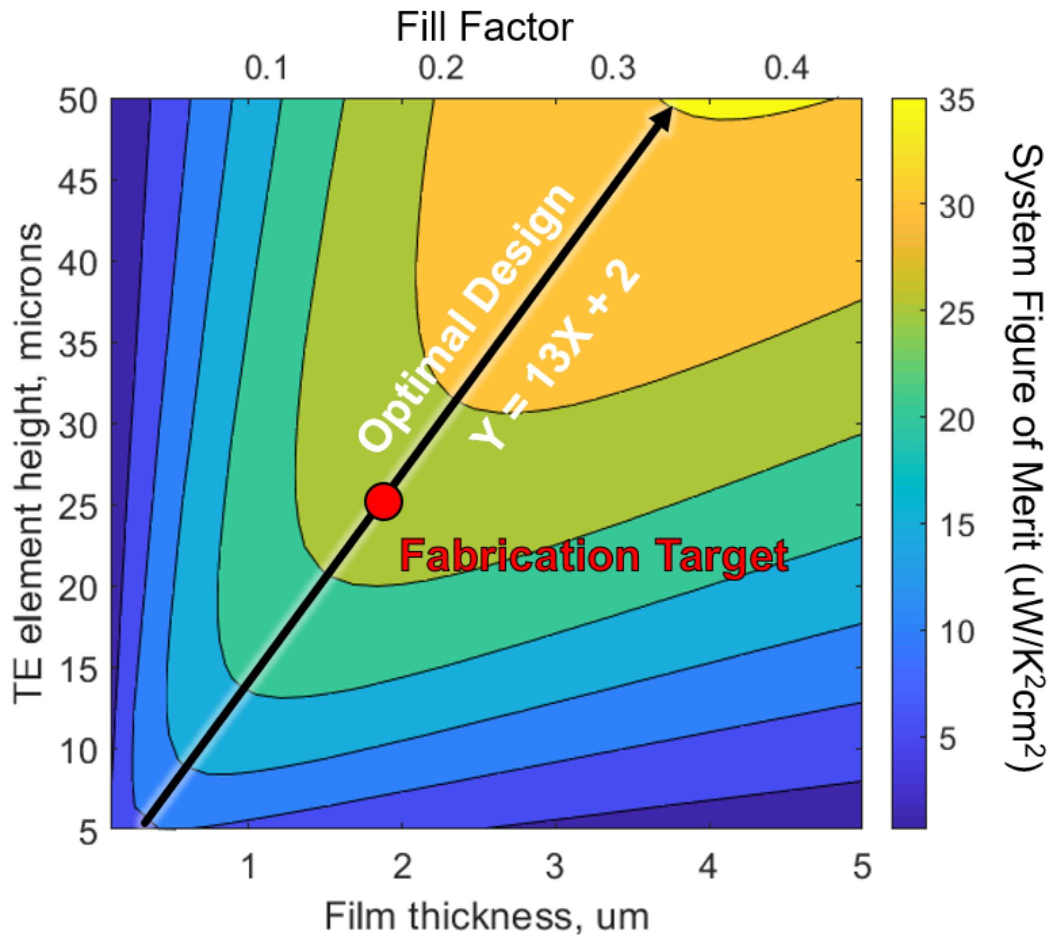


Figure 4-7: TEG System FoM with a 5 K/W heatsink attached. Note the colormap scale is different from the previous figure (4-6).

When attached to a 5 K/W heatsink, the slope of the optimal design line increases from L_{leg} = 8(Film Thickness) to L_{leg} = 13(Film Thickness). This is expected due to the increased thermal resistance requirements given the external thermal load. Additionally, a large drop in the power output is seen, as expected from Figure 4-5. This is due to the decreased ΔT across the device,

which cannot be fully compensated for with longer TE legs without affecting the electrical resistance of the generator.

The fabrication target of this project is for a film thicknesses of 2 microns, corresponding leg height of 25-µm. This target is denoted by a red dot in Figure 4-7. Two microns was chosen as the film thickness due to limitations in the deposition systems caused by the life span of the monitor crystals. Additional film deposition beyond two microns was not expected to significantly increase in generator performance. This is due to the buildup of the composite material over the pillars during deposition (Fig. 4-8). This composite material does not contribute to the power generation of the device. The excess thermal resistance of this composite increases linearly with sidewall film thickness.

4.4 Comparison with Traditional Thin Film Designs

A performance comparison between the High-Aspect Vertical µTEG design and a traditional design is given below. The thickness of the film used for the high-aspect design was 2-µm, and the film thickness for the traditional design was set to 10-µm. Even assuming perfect heatsink efficiency, the high-aspect design outperforms the traditional design with a figure of merit of 86 $\mu W/K^2/cm^2$ compared to 56 $\mu W/K^2/cm^2$.

Table 4-7: Performance Comparison Between High-Aspect and Traditional µTEG designs. Film parameters used are given in Table 8.

Thermo-couple Design	Film thickness	Fill Factor	ΔT (Total)	ΔT (Across TE legs)	Total Leg Res.	Total Device Resistance	Figure of Merit
High-Aspect	2 µm	0.2	10 K	6.42 K	4.7 K/W	7.2 K/W	**86 $\mu W/K^2/cm^2$**
Traditional	10 µm	0.2	10 K	5.16 K	1.4 K/W	2.6 K/W	**56 $\mu W/K^2/cm^2$**

The superior performance of the High-Aspect design can be attributed to the higher ΔT across its thermocouple. Thermal resistance simply due to the silicon substrate and Au contacts is enough to decrease the ΔT by almost half in the traditional design. When connected to a 5 K/W heatsink, the High-Aspect µTEG outperforms the traditional design by a factor of 5.

Table 4-8: Performance Comparison Between High-Aspect and Traditional µTEG designs assuming a 5 K/W heatsink.

Thermo-couple Design	Film thickness	Fill Factor	ΔT (Total)	ΔT (Across TE legs)	Total Leg Res.	Total System Resistance	Figure of Merit (
High-Aspect	2 µm	0.2	10 K	3.46 K	4.7 K/W	12.2 K/W	**25 $\mu W/K^2/cm^2$**
Traditional	10 µm	0.2	10 K	1.59 K	1.4 K/W	7.6 K/W	**5 $\mu W/K^2/cm^2$**

Contacts and Interconnects

As shown in section 3.2, the contact resistance for a 50-um tall TE leg can be 3 times greater than resistance of the leg material itself. Additionally, as there are two set of contacts per leg (Fig. 4-8 B) in the traditional design, the effect is doubled. With short TE legs (<10 µm), interconnect resistance can also contribute significantly [15] to electrical resistance. These presence of these two additional resistances decreases device performance for a traditional µTEG by a factor of 10.

Table 4-9: Performance of a Tradition µTEG with and without contact and interconnect resistance.

Thermo-couple Design	Contact Resistivity (Ω-m^2)	Resistance (Ω)	Film thickness	Average Film ZT	Figure of Merit (
Traditional	2E-9	260	10 µm	0.49	**56 $\mu W/K^2/cm^2$**
Traditional	0	20	10 µm	0.49	**603 $\mu W/K^2/cm^2$**

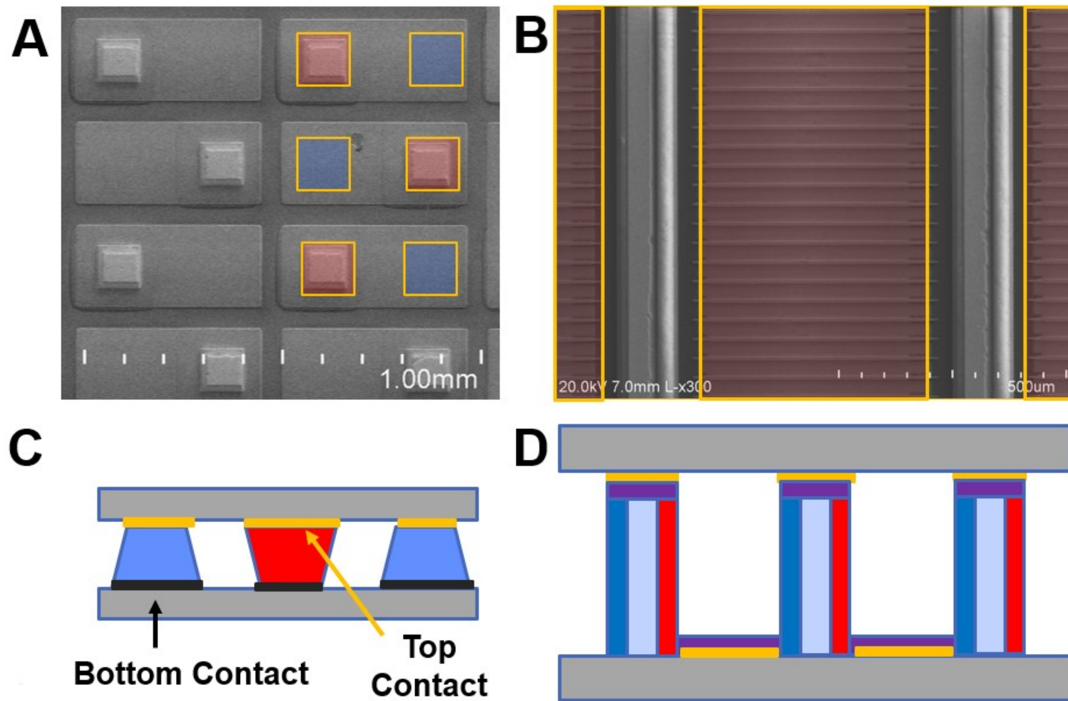


Figure 4-8: (A/C) Top/side views of area available for contact formation on a traditional μTEG. Two discrete sets on contact on the top and bottom must be formed. (B/D) Area available for contact formation with a high-aspect TC design. Only one set of contacts need to be formed.

Unlike traditional designs that require four separate contacts per TE leg-pair (fig. 4-8), the High-Aspect design is intrinsically connected through a composite BiSbTe film formed between the N-Bi_2Te_3 & P-Sb_2Te_3 films. Reducing the electrical resistance of this connection is key to fabricating high performance μTEGs with the high-aspect thermocouple design. For modeling, as this "contact" area encompasses this resistance of this junction is estimated using a contact resistance half of the area available. Further detail of this connection is provided in chapter 6.

One anticipated issue with the High-Aspect design is that the available contact area above the scaffold is small, creating a current bottleneck due to the small contact area. This contact area is proportional to the sum of the film thickness and the oxide scaffold width. For oxide based scaffolds, increasing the scaffold thickness does not improve overall μTEG performance as the

reduction in contact resistance is offset by the increase in thermal conduction from the wider scaffold. However, polyimide based scaffold may present a solution to this issue. Polyimide has a much lower thermal lower thermal conductivity of 0.2 W/mK compared to 1.3 W/mK of SiO_2. This allows patterning of scaffolds up to 5-um wide with a net increase in device performance.

Table 4-10: Performance of a High-Aspect µTEG with and without contact and interconnect resistance.

Thermo-couple Design	Contact Resistivity (Ω-m^2)	Resistance (Ω)	Film thickness	Average Film ZT	Figure of Merit
High-Aspect	3E-9	140	2 µm	0.49	**86 µW/K^2/cm^2**
High-Aspect	0	61	2 µm	0.49	**190 µW/K^2/cm^2**

In both traditional and high-aspect designs, the majority of the electrical resistance is due to the contacts and interconnects. However, the contact resistance for high aspect designs composes a much smaller fraction of the overall device resistance. This is due to the layout of the design, where all available planar surface in thermocouple chain can serve as a contact region to reduce contact resistance.

4.5 Composite BiSbTe Material

Due to the deposition process, the composite BiSbTe that forms over the top and bottom surface of the thermoelectric material can be very thick. Due to the configuration of the µTEG, this TE material does not contribute to the power generation of the device but rather, hinders as it is a source of additional thermal resistance. Under the standard deposition angle of 30° to the normal of the wafer, this TE material is twice as thick as the combined thicknesses of the sidewall films. If this composite material can be kept below 1-µm in height, µTEG performance would be improved by increasing film thickness without increasing TE leg height.

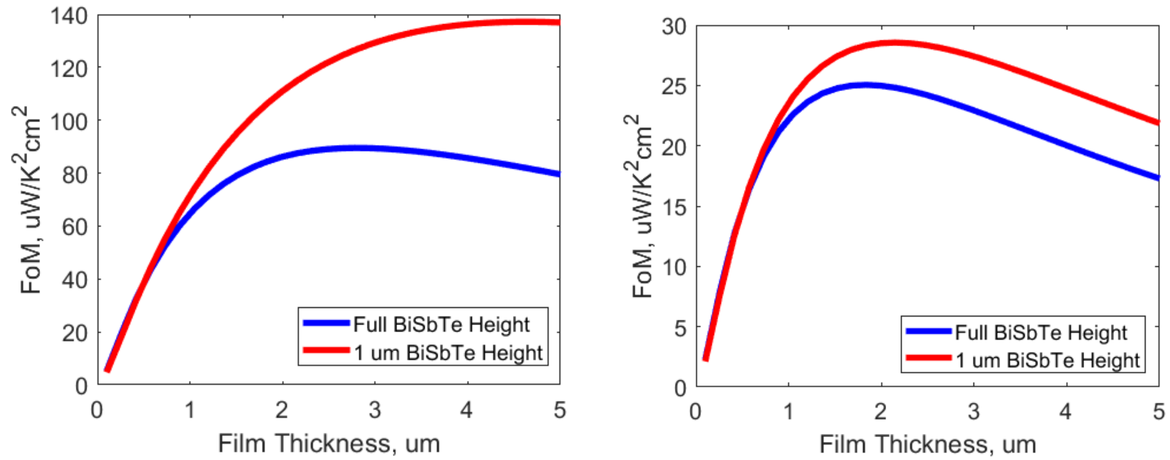


Figure 4-9: The effect of the composite BiSbTe material on µTEG power output (Left) and µTEG system output with a 5 K/W heatsink (Right).

4.6 Other Design Considerations and Effects

Film Matching

While typical µTEGs include both N and P type TE materials to increase power generation, this does not always hold true in cases where one film has a significantly higher power factor than the other. In such a case, it may be desirable to used metal as a stand in for the other TE material.

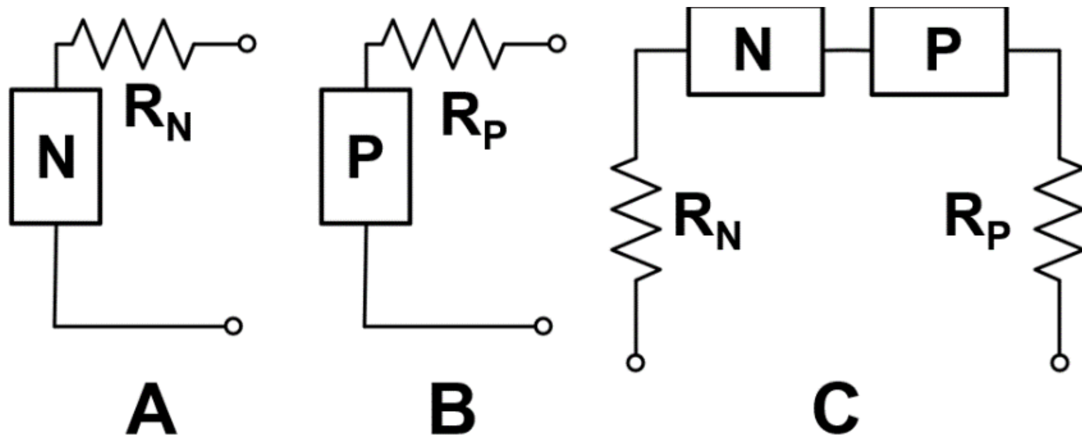


Figure 4-10: Example Generators A, B, and C

Consider two thermoelectric generators, A and B. Generator A is composed of a single N-type and generator B is composed of a single P-type element. The combined power output of the two generators is given by:

$$\boldsymbol{P} = \left[\frac{\boldsymbol{\alpha_N}^2}{\boldsymbol{r_N}}\right]\boldsymbol{\Delta T^2} + \left[\frac{\boldsymbol{\alpha_P}^2}{\boldsymbol{r_P}}\right]\boldsymbol{\Delta T^2} \quad \textbf{(4.4)}$$

Where $\boldsymbol{r_N}$ and $\boldsymbol{r_P}$ are the resistances of the N-type and P-type generator. If the N-type and P-type elements are connected together in series, power output of the combined generator, denoted generator C, now becomes:

$$\boldsymbol{P} = \frac{(\boldsymbol{\alpha_N} + \boldsymbol{\alpha_P})^2}{\boldsymbol{r_N} + \boldsymbol{r_P}}\boldsymbol{\Delta T^2} \quad \textbf{(4.5)}$$

If $\alpha_N = \alpha_P$ and $r_N = r_P$, equation 4.4 and 4.5 have the same value. However, if the power factor of the N-type film is much greater than the power factor of the P-type film, generator A can produce a greater power output than that of the combined generator, C. In this case, the power produced by the N-type film, but lost through the P-film resistance, r_P, is greater than the power generated by the P-type generator. This occurs when:

$$\left[\frac{\boldsymbol{\alpha_N}^2}{\boldsymbol{r_N}}\right] > \frac{(\boldsymbol{\alpha_N} + \boldsymbol{\alpha_P})^2}{\boldsymbol{r_N} + \boldsymbol{r_P}} \quad \textbf{(4.6)}$$

However, this case only considers a single TE element. In practice, room-temperature μTEGs must connect multiple elements together in series. Due to the layout, the routing from hot-to-cold and cold-to-hot sides require paths to be formed from a P-type or neutral material. While metal has a good electrical conductivity, it has a very high thermal conductivity as well, making the usage of a low performance P-type material more desirable.

Peltier Effect

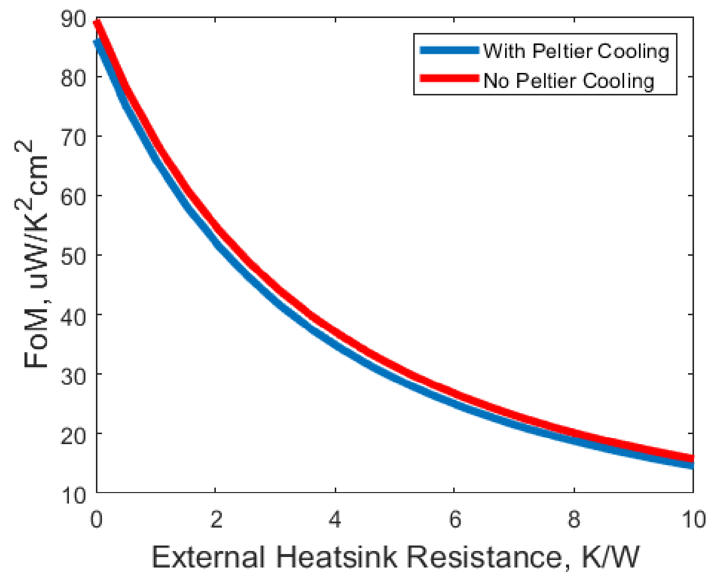


Figure 4-11: μTEG power output. Normal output in blue, output without accounting for the Peltier effect in red.

In a μTEG, the Peltier effect pumps heat along the established temperature gradient, reducing the ΔT across the device. This causes a small, but consistent drop in power output of roughly 3-4%. This can be measured as an effective decrease in the thermal resistance across the active thermoelectric elements.

Thermal Considerations

As explored in chapter 3, thermal resistances in the TEG system decrease the power output. The only beneficial thermal resistance that increases performance is that across the thermoelectric elements. This section investigates the magnitude of common source of thermal resistances.

Scaffold Conduction

In the high-aspect TC design, the scaffold on which the TE film is deposited contributes to unwanted thermal conduction through the junction. Too thick of a scaffold eliminates the thermal

advantages of the design. For a µTEG with 2-µm thick TE films and an oxide scaffold, the figure of merit decreases roughly linearly from 86 $\mu W/K^2/cm^2$ at a thickness of 2-µm to 52 $\mu W/K^2/cm^2$ at a scaffold thickness 20-µm. At 20-µm, the power output is roughly equal to a traditional µTEG design using 10-µm thick films.

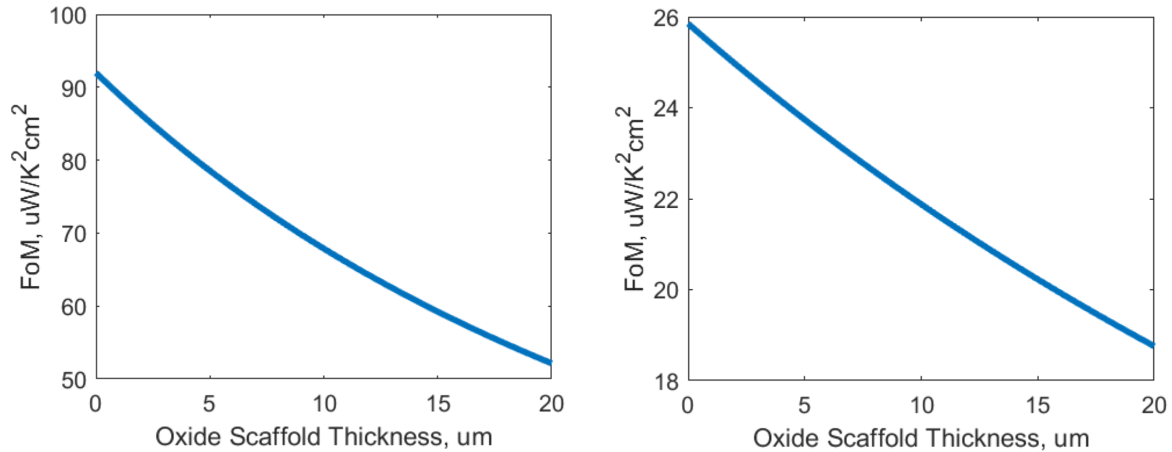


Figure 4-12: FoM vs. Scaffold Thickness for (Left) TEG only (Right) TEG system with a 5 K/W heatsink

Bond Ring

A bond ring is often required to increase the mechanical robustness of a µTEG. Depending on the thickness required for packaging, the thermal conductance of this ring can be quite substantial. For a 3x3 mm µTEG with an 80-um thick oxide bond ring on the periphery, this conductance equates roughly to the amount as the 2-um oxide scaffold.

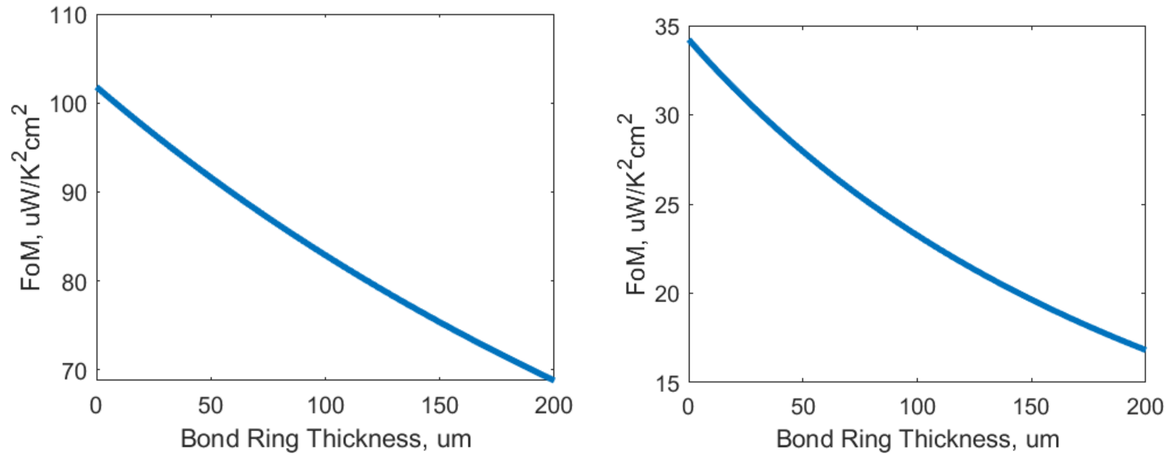


Figure 4-13: FoM vs. Bond Ring Thickness for (Left) TEG only (Right) TEG system with a 5 K/W heatsink.

Si Thinning

While Si has a very high thermal conductivity of over 120 W/mK[45] at room temperature, it is also much thicker than the TE junction. Thinning this silicon can increase the FoM of the µTEG. In a µTEG system with a external heatsink of 5 K/W, thinning of the silicon wafer down from 500 to 100-µm can improve the power output by over 15%, from 25 µW/K^2/cm^2 to 29 µW/K^2/cm^2.

Table 4-11: Affect of Substrate thinning on µTEG FoM

Si Thickness	Heatsink (K/W)	ΔT (Total)	ΔT (Across TE legs)	Package Resistance	Total System Resistance	Figure of Merit
500 µm	0 (Perfect)	10 K	6.42 K	2.5 K/W	7.2 K/W	**86 µW/K^2/cm^2**
100 µm	0 (Perfect	10 K	7.36 K	1.6 K/W	6.3 K/W	**113 µW/K^2/cm^2**
500 µm	5	10 K	3.46 K	2.5 K/W	12.2 K/W	**25 µW/K^2/cm^2**
100 µm	5	10 K	3.71 K	1.6 K/W	11.3 K/W	**29 µW/K^2/cm^2**

4.7 Conclusion

The High-Aspect thin-film µTEG design can produce µTEGs with much greater thermal resistances than traditional vertical µTEGs designs while maintaining fill factor. This gives the High-Aspect design an edge in performance under realistic conditions where the external thermal load is >3K/W. This performance advantage increases as the external thermal resistance increases. The greater tolerance for external thermal resistances increases the compatibility of the High-Aspect µTEG design with applications where: the heatsink is limited, or high-quality thermal contacts cannot be made to the µTEG, due to size or cost constraints. An area of concern regarding this design is the contact resistance at the junction between the N & P type films. Due to the ambiguous nature of these contacts, the resistance across them cannot be easily estimated, and thus must be experimentally determined.

Chapter 5 Thermal Co-Evaporation of Bi_2Te_3/Sb_2Te_3

The most important component in a thermoelectric generator is not-so-arguably the thermoelectric material itself. Poor thermoelectric material performance can cancel out the advantages gained through better µTEG designs. Thus, efforts to develop high quality, thermoelectric thin-films compatible with the proposed high-aspect structure is central to the viability of the design. This chapter details efforts to deposit Bi_2Te_3 and Sb_2Te_3 films on standard planar substrates composed of polycrystalline silicon in addition to thermally insulating silicon oxide and polyimide. These two materials are later used as the scaffold material in our µTEGs in chapter 8. The effect of deposition conditions such as flux ratio and deposition temperature on the resulting thermoelectric films are evaluated. Later in chapter 6, details on thermoelectric film deposition over vertical surfaces are provided. Additionally, differences between films grown on planar and vertical surfaces are discussed.

Table 5-1: Reported Performance of Co-evaported Bi_2Te_3 and Sb_2Te_3

	Bi_2Te_3			Sb_2Te_3		
	Seebeck (µV/K)	Resistivity (µΩ-m)	Power Factor (mW/K^{2}m)	Seebeck (µV/K)	Resistivity (µΩ-m)	Power Factor (mW/K^{2}m)
Goncalves[8]	-248	12.6	4.9	188	12.6	2.8
Ghadfouri[28]	-250	20	3.1	195	18.9	2.03
Zou[63][64]	-228	13	4.0	171	10.4	2.8
Huang[62]	-208	18.8	2.3	160	12.9	2.0

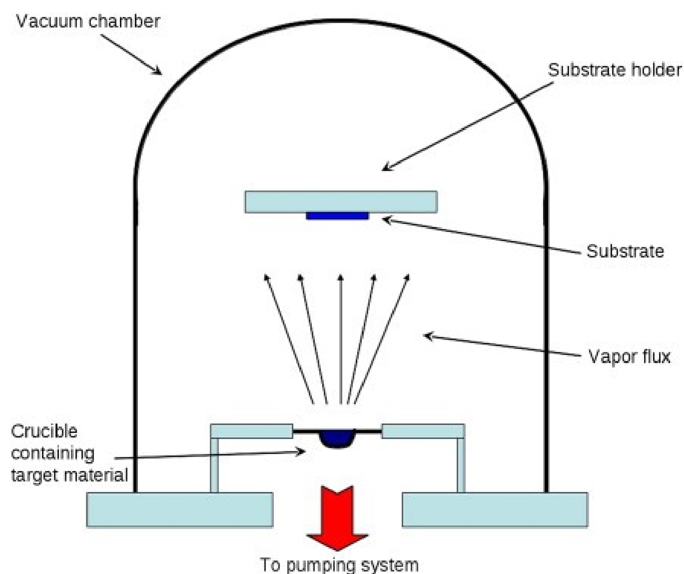


Figure 5-1: Diagram of a Thermal Evaporation System

The films produced for this work were solely deposited via thermal co-evaporation. This method is attractive from a manufacturing standpoint due to its relative simplicity in both process control [22] and equipment requirements. Furthermore, co-evaporation been shown to produce quality Bi_2Te_3 and Sb_2Te_3 films with power factors over 4 and 2 mW/K^{2}m, respectively (Table 5-1).

In the co-evaporation process, target materials are placed into crucibles and heated to achieve the desired vapor pressure and deposition rate through joule heating. This rate is monitored using a quartz microbalance crystal mounted above the crucible. As material deposits on the crystal, its resonance frequency decreases. This frequency shift can be converted to a deposition rate given the density of the deposited material. Dome rotation is usually required for uniformity in system with multiple sources as the placement of sources is not centered. Unlike e-beam evaporators, thermal evaporators can deposit thermally insulating materials, such as tellurium, with a high degree of control. Co-evaporation is required for Bi_2Te_3 and Sb_2Te_3 as the different vapor pressures of the materials would cause changes in the stoichiometry of the evaporated material from the target material if Bi_2Te_3 or $Sb_2Te_3$was used as the starting source.

Table 5-2: Vapor pressures of Bi, Sb, and Te [28].

Material	Melting point (K)	T (K) @ vapor pressure 750 (Torr)	T (K) @ vapor pressure 75 (Torr)	T (K) @ vapor pressure 7.5 (Torr)
Bi	544.7	1835	1538	1325
Sb	903.8	1858	1491	1219
Te	722.7	1266	1042	888

Under vacuum, the vapor flux from the source impinge on a substrate mounted facing toward the target. High vacuum is typically desired to reduce reactive species and contaminates. As a side effect, the evaporated material has a large mean free path resulting in line-of-sight deposition. With a large throw distance from source to substrate, the material flux is collimated near the substrate surface. This allows resolution patterning through shadow masking, even when the shadow mask is offset from the wafer surface.

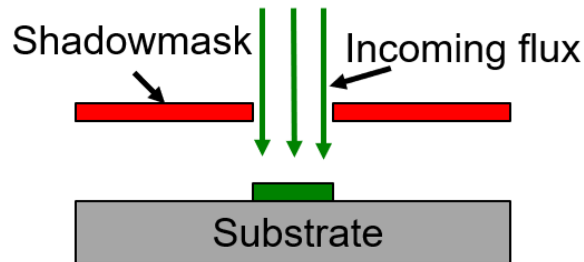


Figure 5-2: Shadow mask patterning with a collimated material flux.

This is advantageous for the process integration of Bi_2Te_3 and Sb_2Te_3 films, which can be sensitive to common clean room solvents including acetone and n-methyl-2-pyrrolidone (NMP).

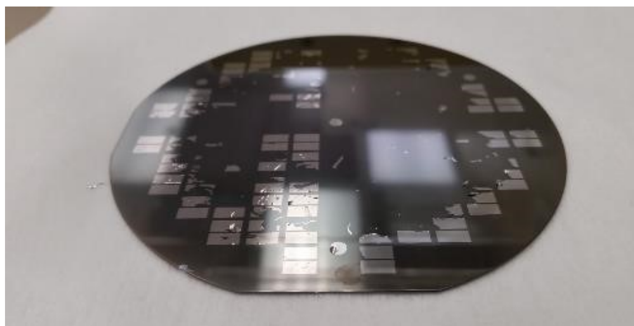


Figure 5-3: Delamination of Sb_2Te_3 after exposure to Acetone for 10 min.

Dome rotation is usually required for uniformity in systems with multiple sources as the placement of sources is not centered.

5.1 Deposition System

Bi_2Te_3 and Sb_2Te_2 deposition was performed using a Lab 18 series PVD system from Kurt J. Lesker. The system contains 6 separate sources, each with their own individual power supply for concurrent deposition up to 6 individual materials. Each source has its own crystal microbalance rate monitors. Depositions were conducted at a chamber pressure below 2E-6 torr. Due to concerns about changes in tooling factor, source crucibles were kept above half full for all runs. Bi_2Te_3 and Sb_2Te_3 thickness were limited by the life of the monitor crystals to 5-µm and below. Crystal shutters were able to extend this thickness but caused large variations in deposition rate and thus were not used. Typical depositions maintained accuracy within ± .2 Å/s with semi-annual updates of the tooling factor. Non-uniformity was less than 10% across the wafer with dome rotation. No shaper was used. Substrate heating was provided by two IR lamps facing the backside of the wafer holder.

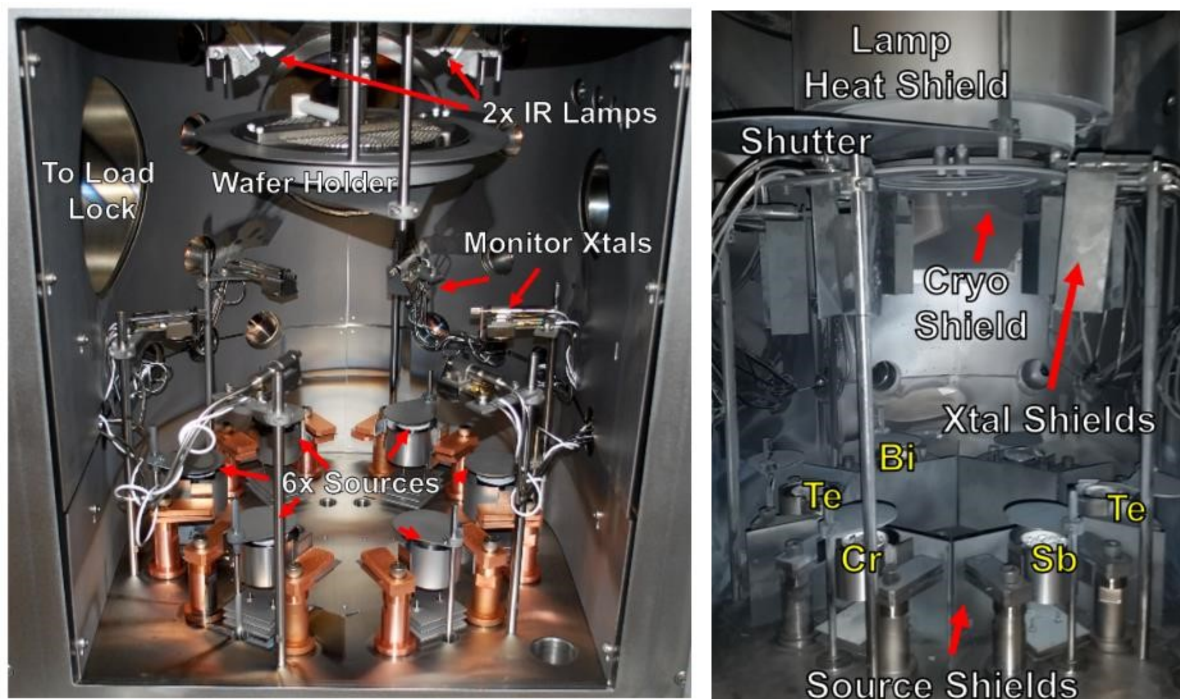


Figure 5-4. (Left) A. Evaporation chamber without shields. (Right) B. Evaporation chamber with shields installed.

Tall shields surrounding the monitor crystals were installed to prevent cross-talk between the evaporation of different sources. A heat shield surrounding the IR heater was present to prevent unwanted heating of the chamber walls. During deposition, Bi, Sb, and Te deposit on the chamber walls; heating of these walls would cause re-evaporation of these materials from the chamber walls to the wafer.

Temperature was measured through a thermocouple mounted within the heatshield, 1 cm above the platen. The offset of the nominal to actual temperature on the wafer surface measured to be roughly 13% using temperature dots. Thus, for a nominal temperature of 290 °C set, the actual temperature on the wafer surface is 254 – 260 °C. Unless noted otherwise, temperatures reported in this work are an estimate of the actual temperatures on the wafer surface.

Table 5-3: Set vs. Measured Temperature

Set Temperature	Actual Temp.
140 °C	<116 °C
155 °C	127 – 131 °C
250 °C	< 232 °C
275 °C	232 – 241 °C
285 °C	232 – 241 °C
295 °C	254 – 260 °C

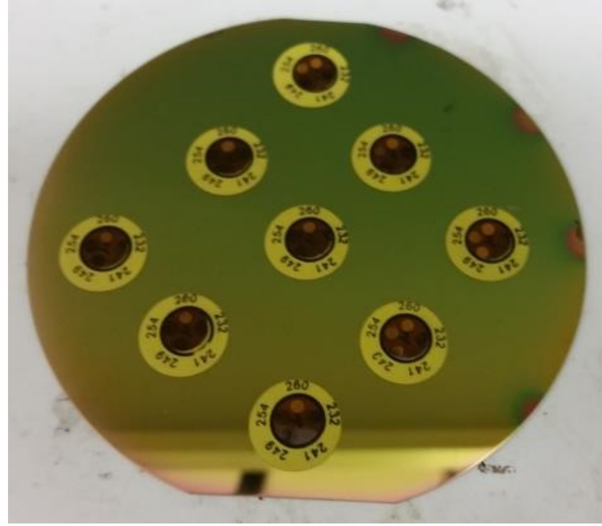


Figure 5-5: Non-reversible temperature monitors.

5.2 Evaporation Process

At the start of the evaporation process, sources were heated and kept at a steady temperature for a long 10 minute soak to help control the initial evaporation rate. A shutter delay phase followed to allow the PID controller to reach the target deposition rates before actual material deposition. To improve the crystallinity of the resulting films, the substrate was heated during deposition to 230 – 270°C. During standard depositions, the deposition rate was set to 1Å/s for Bi and Sb, and 3 Å/s for Te. These tellurium rich depositions were found to yield superior power factors in the resulting thermoelectric films. During deposition, excess tellurium re-evaporates, leaving behind stoichiometric film. After deposition, the sample was cooled to 50 °C at a rate of 10°C/min before retrieval. Immediate retrieval of the hot substrate would expose the film to temperature shock, potentially causing delamination.

Reproducibility

Run to run variation on the material properties of the produced films was low, especially if the films were deposited consecutively. However, if the films were spaced apart, larger variations occurred.

Table 5-4: Comparison of two consecutively deposited Bi_2Te_3 films

Run #	Material	Substrate	Temp. °C	Seebeck (µV/K)	Resistivity (µΩ-m)	Power Factor (mW/K^{2}m)
185	**Bi_2Te_3**	**Poly-Si**	**275**	**-251**	**30.2**	**2.09**
186	**Bi_2Te_3**	**Poly-Si**	**275**	**-248**	**28.9**	**2.13**
Difference				**1.1%**	**4.3%**	**1.8%**

Table 5-5: Comparison of two deposited Bi_2Te_3 films space by 2 other depositions

Run #	Material	Substrate	Temp. °C	Seebeck (µV/K)	Resistivity (µΩ-m)	Power Factor (mW/K^{2}m)
187	**Bi_2Te_3**	**Poly-Si**	**260**	**-266**	**18.1**	**3.91**
190	**Bi_2Te_3**	**Poly-Si**	**260**	**-241**	**16.01**	**3.62**
Difference				**9.3%**	**11%**	**7.4%**

Film Thickness Limitations

The thickness of deposited Bi_2Te_3 and Sb_2Te_3 were limited by the life of the monitoring crystals. Crystal life was limited to 4-µm of tellurium. Under the standard deposition ratio of 1:3 Bi:Te and a sticking ratio of .7 for Bi, this limited the thickness of the deposited to just over 2-µm. For planar films, this crystal limitation could be circumvented through the use of multiple sources. However, for later vertical films, this was not possible. Thus, all vertical films remained below 2.5-µm thick for Bi_2Te_3 and Sb_2Te_3. This limited the fill factor of the fabricated µTEGs to 20% given a 25-µm pillar pitch. This fill factor can be further improved through the reduction of the pillar pitch.

Film Adhesion

For un-patterned blanket films, film adhesion was another concern due to the elevated deposition temperatures. The large mismatch in the co-efficient of thermal expansion (CTE) between Bi_2Te_3/Sb_2Te_3 and common substrates causes large mechanical stresses during cool down. The in-axis CTE of Bi_2Te_3 and Sb_2Te_3 are used as deposited films showed a strong C-oriented growth. To improve film adhesion, a 10 nm layer of chrome was added to blanket film depositions.

Table 5-6: Linear thermal expansion coefficients at room temperature

Polyimide	Oxide	Si		Bi_2Te_3[65]	Sb_2Te_3[65]
~20 ppm/K*	1 ppm/K	2.6 ppm/K	CTE (//)	18 ppm/K	32 ppm/K
			CTE (⊥)	10 ppm/K	18 ppm/K

*Kapton, 100 HN

Experimental thickness limits for Bi_2Te_3 and Sb_2Te_3 for different substrates are given below.

Table 5-7: Thickness limitations of Blanket TE films with a 10 nm Cr adhesion layer

Substrate	Bi_2Te_3 (T = 260 °C)	Sb_2Te_3 (T = 250 °C)	Sb_2Te_3 (T = 230 °C)
Poly-silicon	2 μm	< 1.5 μm	>1.5 μm
Polyimide	4 μm	> 1 μm	-
Silicon Oxide	2 μm	< 1 μm	1.5 μm

However, this thickness limitation was not found for patterned films with feature sizes < 500 μm. Thus, film adhesion is not a significant concern in the design or fabrication of High-Aspect μTEGs.

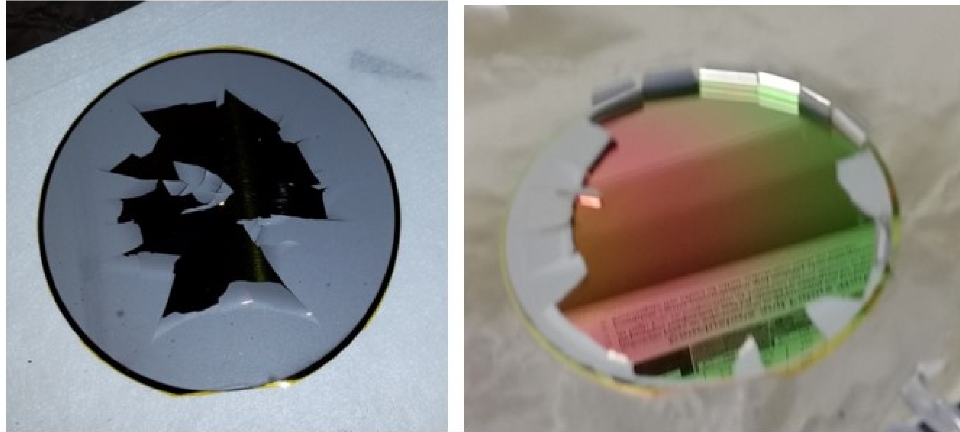


Figure 5-6: (Left) Delamination of 5 µm Bi_2Te_3 on Polyimide. (Right) Extreme delamination of 1.5 µm Sb_2Te_3 on polysilicon

5.3 Thermoelectric Film Characterization

Measurement

Sheet resistance was measured using a commercial Miller FPP-5000 4-point probe. Film thickness was measured using a Dektak surface profilometer.

The Seebeck coefficient was measured with a custom measurement set up consisting of a heater, and two thermocouples and voltage probes. Thermocouples and probes were attached together using thermal epoxy. Secure connection to the film was ensured using clamps. Thermal grease at the point of contact to the TE film was used to improve the accuracy of the temperature reading. However, long term measurements were not possible as the thermal grease would seep into the films, affecting their properties. The entire set up was placed into a small oven to reduce the effect of air flow.

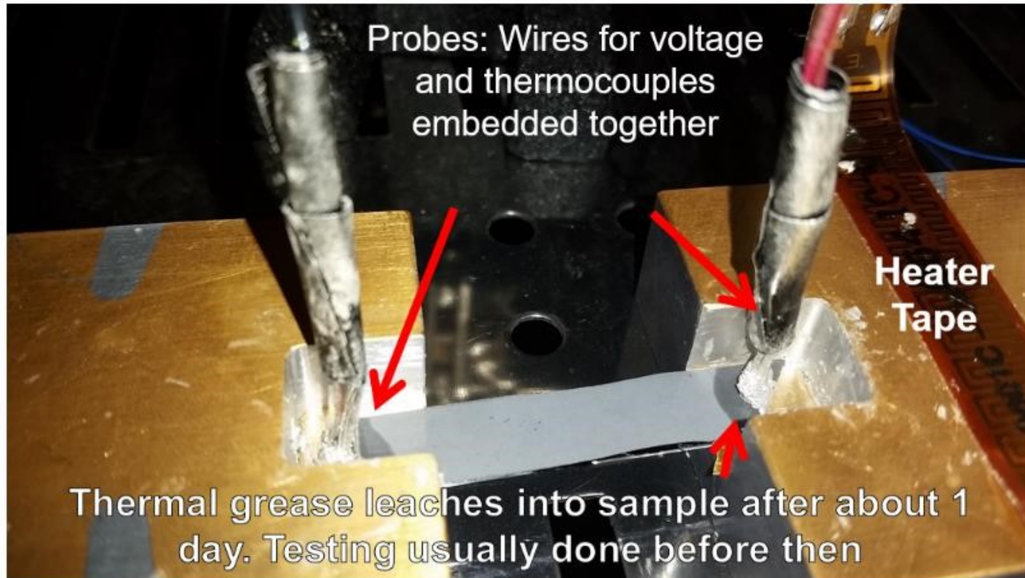


Figure 5-7: Experimental setup for Seebeck Measurement.

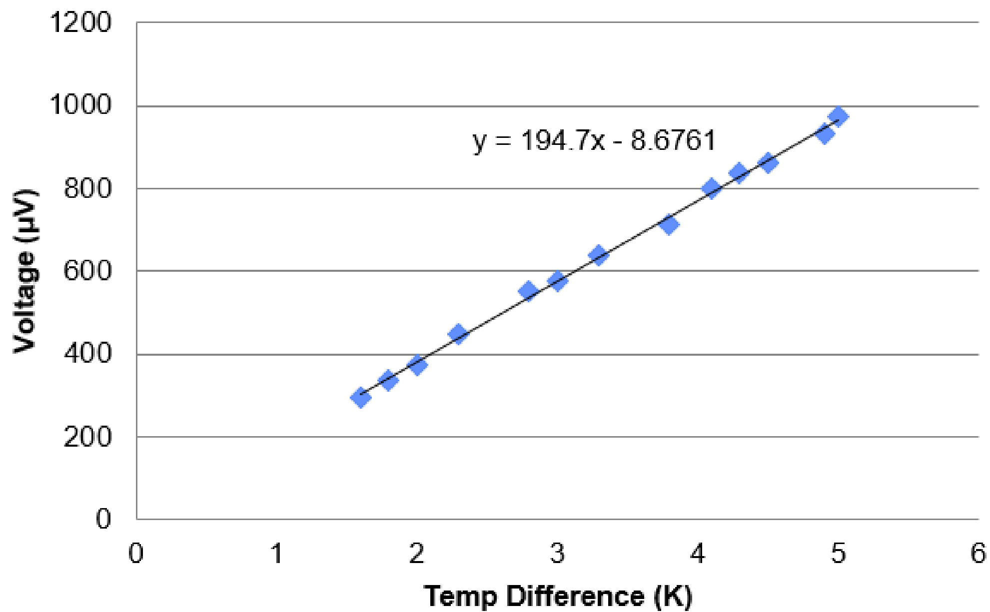


Figure 5-8: Typical measurement of a film sample. The slope of the V/T curve is taken as the Seebeck value while the offset is ignored.

The thermocouples used in the system were calibrated using boiling water and an ice bath for the 100 °C and 0 °C reference. The accuracy of the test system was evaluated by comparing the measured Seebeck values of bismuth and nickel to the published values. The Seebeck values

measured by our system were found to be 6 – 20% lower (Table 5-8) than the published values. However, as Ni and Bismuth were deposited through thin film methods over an oxidized Si substrate, the actual Seebeck values of the samples may differ from published bulk values.

Table 5-8: Measured Seebeck Values of Ni and Bi

	Measured Seebeck	Published Seebeck[66]	Difference
Nickel	-14.9	-18.5	-19.4%
Bismuth	-72.1	-77	-6.3%

Measurements were also checked for consistency against the measurements [28] taken by a previous student of the group using a similar set up and found to match. These previous measurements were previously verified using a 4-point probe test set up under vacuum and temperature controlled using a cryostat.

However, Seebeck measurement at an external company did not agree with the measured values. Seebeck values measured externally were consistently 25% lower than those measured using the above set up. However, as there was a consistent percentage difference in the values, relative values of the Seebeck agreed and should be useful for comparison purposes.

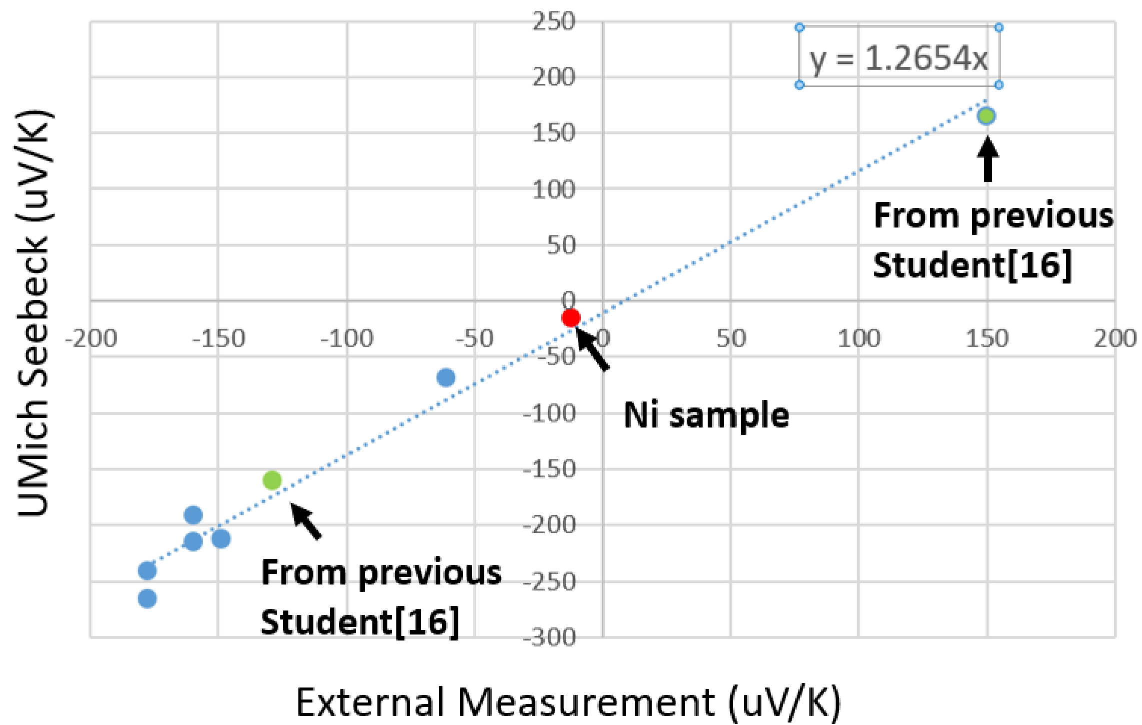


Figure 5-9: Comparison of Seebeck values measured at Michigan (Y-axis) and at an external company (X-axis).

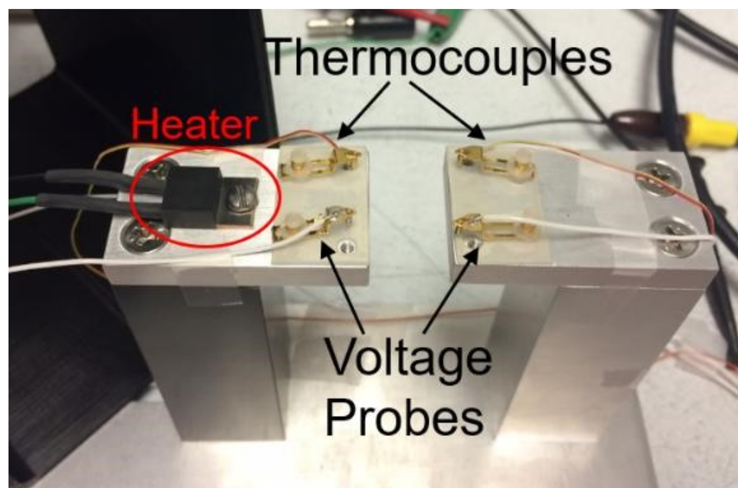


Figure 5-10: Measurement setup at external company.

Thermal Properties

Due to difficulties measuring the thermal properties on thin films, and the low variation expected, thermal conductivity of the films was not measured. For the purposes of modeling and

ZT calculations, the resistivity of the deposited Bi_2Te_3 and Sb_2Te_3 films were assumed to be 1.5 W/mK [44].

5.4 Crystal Morphology

Bi_2Te_3 film growth was characterized by an initial layer of crystal grains isotropic in shape (Fig. 5-6 A). Despite its appearance, this initial crystal layer is highly C-oriented (Fig. 5-14). Over this initial layer, Bi_2Te_3 crystals grew in a columnar fashion (Fig. 5-6 B). This columnar growth is speculated to be caused by preferential crystal growth along the C-axis of the Bi_2Te_3 crystal, where multiple Van-der-Waals gaps exists as opposed to the A-B axis. The presence of this initial "seed" layer was thought to be impacted by the lattice mismatch of the Bi_2Te_3 crystals to the polysilicon substrate. However, later depositions on amorphous substrates including polyimide and oxide showed no changes in the crystal morphology of this initial layer.

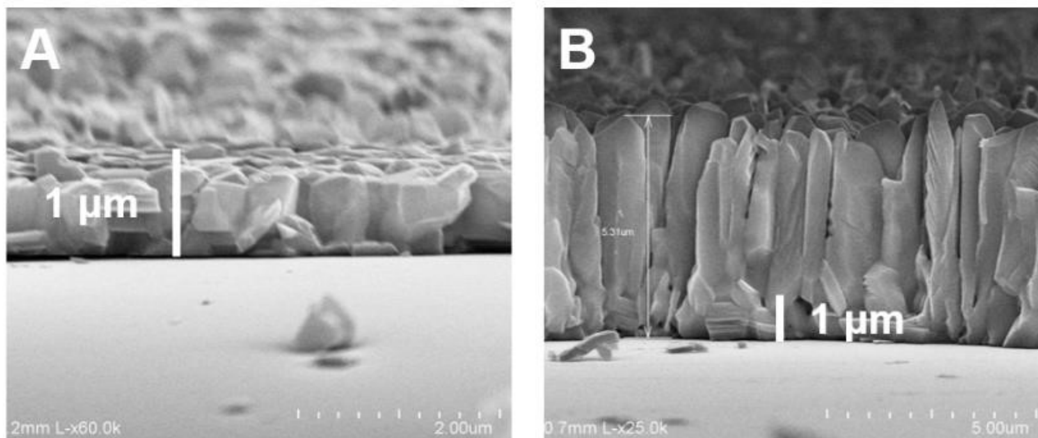


Figure 5-11: Side view of Bi_2Te_3 (Left) Initial film growth (Right) Columnar film growth over initial layer. Polyimide substrates.

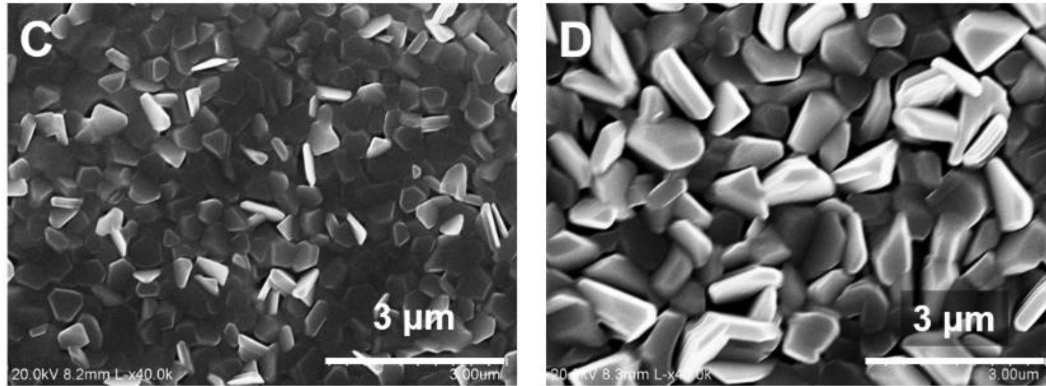


Figure 5-12: Top down view of Bi_2Te_3 (Left) Initial film growth (Right) Columnar film growth over initial layer.

The initial "seed" layer had different thermoelectric properties compared to the later film growth. The electrical resistivity and the Seebeck of this seed layer are larger than that of subsequent film growth. Due the lower Seebeck of the columnar crystal film growth, the power factor of the thicker film is over 16% lower than the power factor of the thin film which only contains the "seed" layer.

Table 5-9: Change in film properties of thick and thin films

Substrate	Type	Thickness	Temp. °C	Bi/Te Ratio	Resistivity μΩ-m	Seebeck	Power Factor mW/K^2m
Polyimide	Bi_2Te_3	0.9 μm	260	39.6/60.4	25.0	-264	2.78
Polyimide	Bi_2Te_3	5.3 μm	260	40.1/59.9	19.3	-212	2.32

The thickness of this initial layer, as well as the grain size of the columnar crystals, increases with the deposition temperature. However, using this method does not yield a large increase in film performance as film resistivity increases for Bi_2Te_3 depositions above 260°C. This negates the decrease in resistivity from going from the seed to bulk crystal structures.

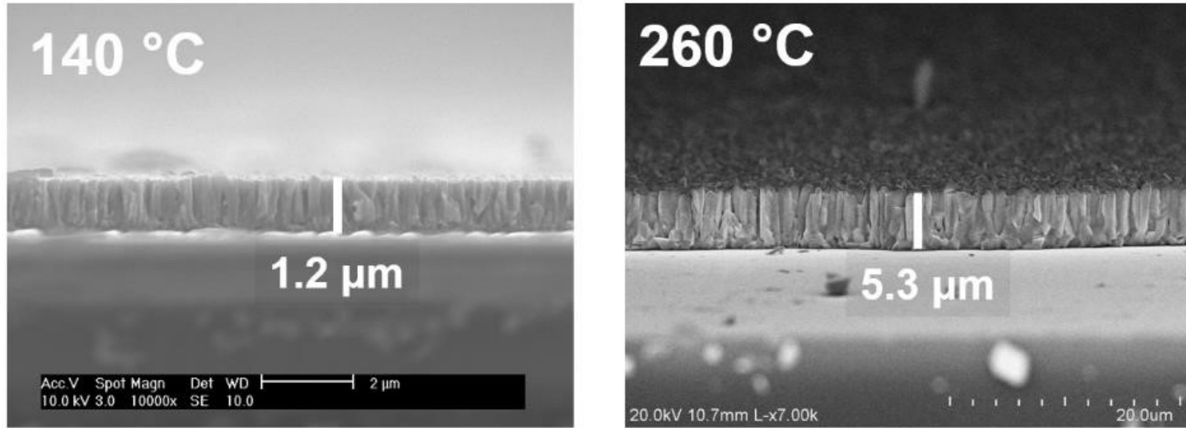


Figure 5-13: Film deposited at (Left) 150°C and (Right) 260°C. Grain size for Bi_2Te_3 films deposited at 260°C film is approximately 5x larger than at 140 °C.

This increase in grain size was previously documented in [28] for Sb_2Te_3.

Orientation

As the in-plane (A/B-axis) properties of Bi_2Te_3[54] and Sb_2Te_3[46] are superior to cross-plane (C-axis), it is desirable to grow such films in the C-orientation from the substrate in the High-aspect thermocouple design. Fortunate, initial Bi_2Te_3 nucleation sites are C-oriented [47], and above 240 °C, all Bi_2Te_3 films were found to be highly C-oriented [Fig. 5-9] as measured through XRD. Films below 240 °C were not measured. Figure 5-9 below shows the XRD peaks of Bi_2Te_3 deposited at 250 °C. The strongest peak returns were for the C-oriented planes of (0 0 6), (0 0 9), and (0 0 15). For comparison, the XRD peaks of powdered Bi_2Te_3 is provided immediately below. The crystal orientation of the powdered sample is assumed to be completely randomized.

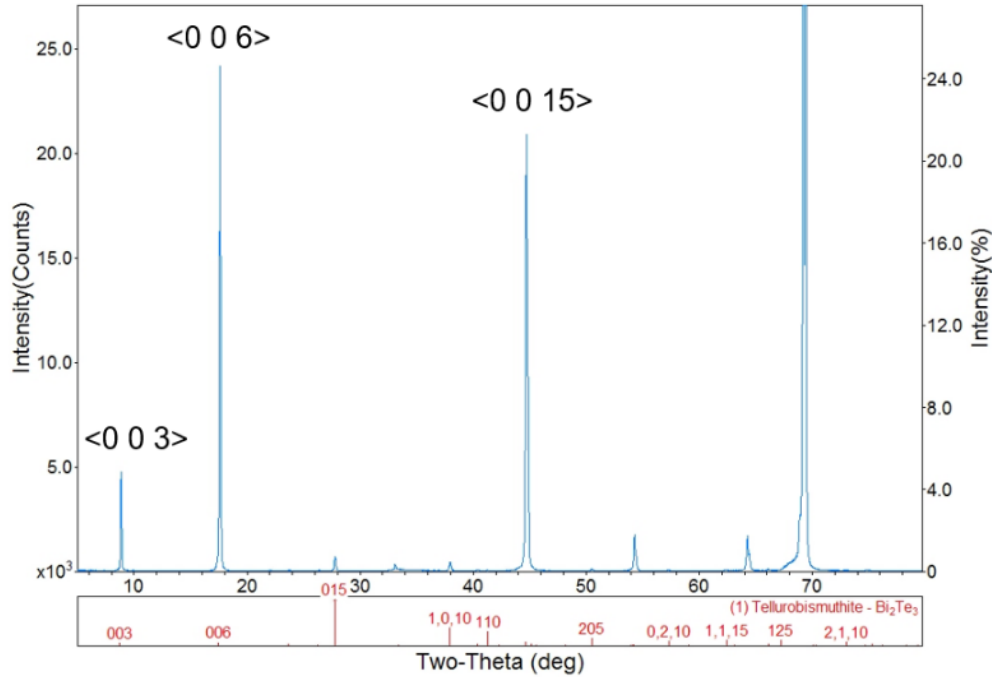


Figure 5-14: XRD of 1 µm of Bi_2Te_3 deposited at 250 C on Poly-Silicon. The peak at 68° is due to the silicon substrate. Reference XRD peaks of (isotropic) Bi_2Te_3 powder are shown below. The typical FWHM for Bi_2Te_3 films deposited above 240°C was 0.15°.

Sb_2Te_3 films also showed a preference for C-oriented growth. However, this was not as strong as seen in Bi_2Te_3. The greatest XRD returns were from the (1 0 10) and (0 1 5) plane, indicated greater isotropy. However, the majority of the film is still believed to be C-oriented as the relative returns of the C-oriented (0 0 3) and (0 0 6) planes are large, compared to the small peaks from the powder reference.

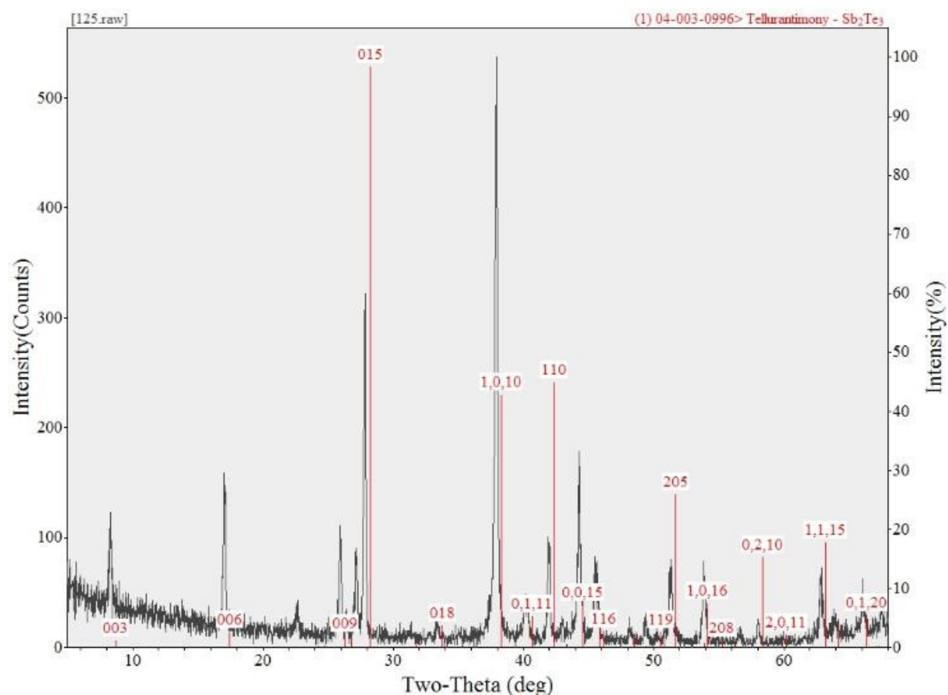


Figure 5-15: XRD of 1 µm of Sb_2Te_3 deposited at 230 C on oxide. Red lines represent the XRD peaks from Sb_2Te_3 powder, assumed to be randomly oriented. The typical FWHM for Sb_2Te_3 films deposited above 240°C was 0.2°.

Substrate Effect

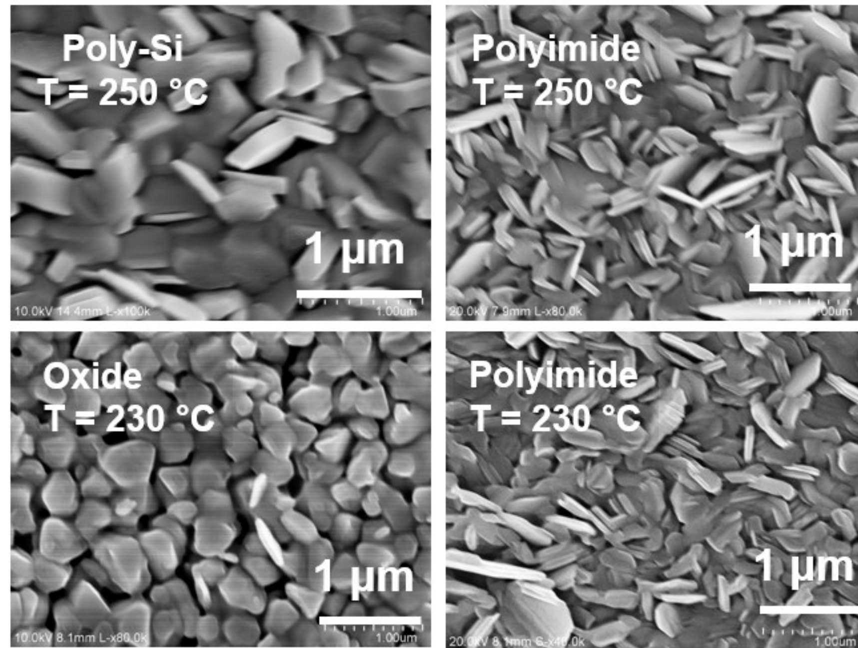


Figure 5-16: Impact of substrate on Sb_2Te_3 film morphology. Sb_2Te_3 was deposited on oxide at a lower temperature due to stress issues.

The crystal structure of Sb_2Te_3 films were found to be affected by the substrate despite similar film compositions. However, this difference in crystal structure did not have a significant impact on the material properties of the film.

Table 5-10: Sb_2Te_3 power factor on different substrates

Substrate	Deposition Temperature	Sb:Te ratio	Resistivity µΩ-m	Seebeck µV/K	Power Factor mW/K^2m
Poly-Silicon	250 °C	41:59	31.14	165	0.87
Polyimide	250 °C	42:58	33.8	176	0.91
Polyimide	230 °C	41:59	38.2	201	1.05
Oxide	230 °C	38:62	38.1	199	1.04

For Bi_2Te_3, no difference in film morphology was seen across different substrates. The Seebeck coefficient remained constant for films deposited on poly-Si and polyimide at 270 °C. However,

a large difference in the electrical conductivity of the films was seen. Likewise, a difference in the conductivity of Bi_2Te_3 deposited on poly-Si and oxide at 250 °C was seen, though the power factor was unchanged due to opposing changes in the Seebeck coefficient.

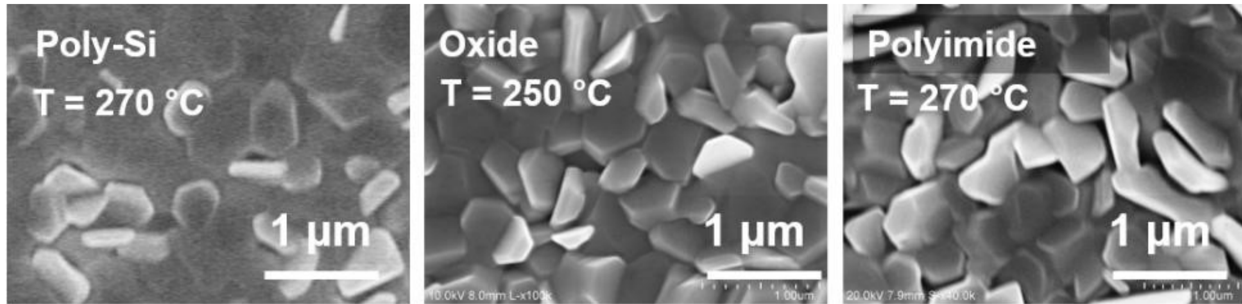


Figure 5-17: Impact of substrate on Bi_2Te_3 morphology. Bi_2Te_3 was deposited on oxide at a lower temperature to lower stress.

Table 5-11: Bi_2Te_3 power factor on different substrates

Substrate	Deposition Temperature	Bi:Te ratio	Resistivity µΩ-m	Seebeck µV/K	Power Factor mW/K^2m
Poly-Si	270 °C	39:61	18.05	-266	3.92
Polyimide	270 °C	40:60	24.9	-264	2.80
Poly-Si	250 °C	38:62	9.36	-183	3.57
Oxide	250 °C	40:60	12.2	-212	3.63

Amorphous to crystalline transition

Bi_2Te_3 depositions show a transition from an amorphous film to a crystalline film at roughly 100°C. Sb_2Te_3, while not tested, is expected to have a similar transition point [48].

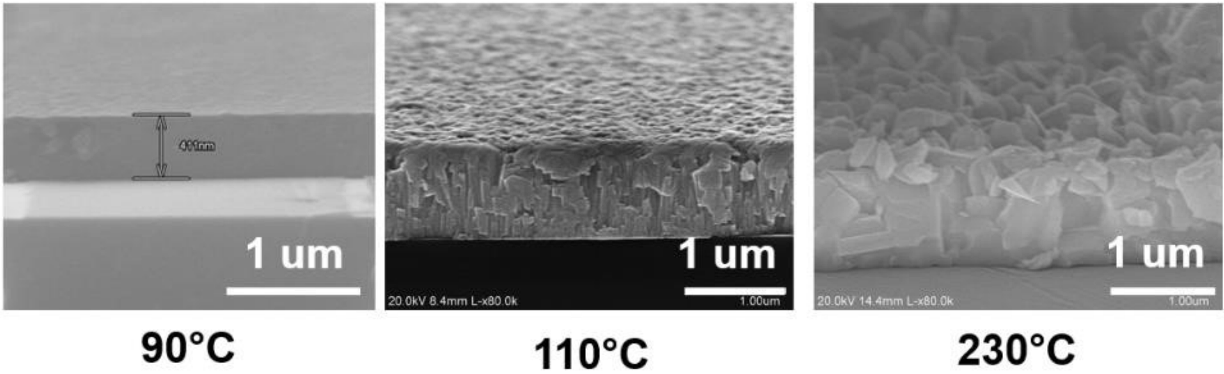


Figure 5-18: Bi_2Te_3 deposited at 90°C, 110°C, and 230°C. There is an amorphous to crystalline transition in the material between 90°C, 110°C.Film Optimization

5.5 Film Optimization

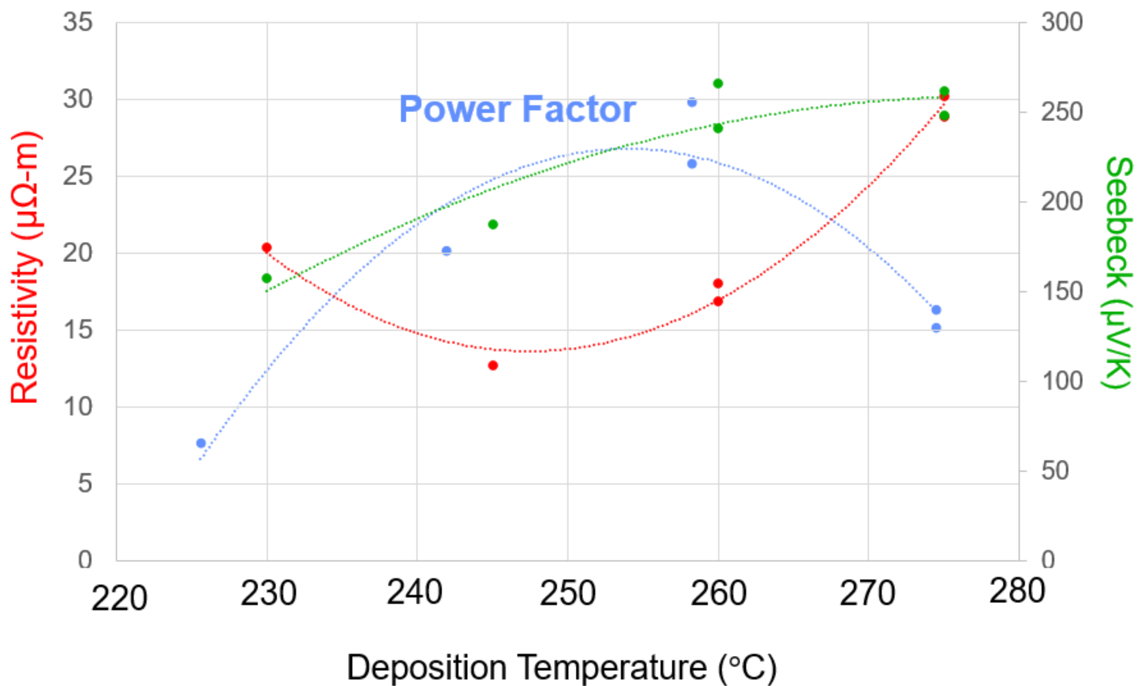


Figure 5-19: Power factor (In Blue) of Bi_2Te_3 deposited on polysilicon as a function of temperature.

Bi_2Te_3 and Sb_2Te_3 films have an optimal temperature range for deposition. While the magnitude of the Seebeck coefficient increased with the deposition temperature up to the tool limit of 300 °C, the resistivity of the film had a minimum within the 230 – 270°C range for Bi_2Te_3. Power

factor is thus maximized for film depositions around this low resistivity region. It is believed that this change in resistance is due to a decrease in the carrier concentration with increasing deposition temperature. Lower temperature depositions may allow greater defect densities which contribute to the carrier concentration. These defects could be located inside the crystal themselves, or at the grain boundaries. As grain size increases with temperature [28], lower deposition temperatures would increase surface area of the boundaries and thus the defect density. However, at too low of a temperature, the decrease in carrier mobility would offset the effect of increased carrier concentrations.

Carrier concentration and mobility were measured through a commercial hall measurement system. Electron mobility in Bi_2Te_3 was found to be stable around 200 cm^2/V-s with changes in resistivity due to changes in carrier concentration. An Sb_2Te_3 film deposited on polysilicon was found to have high mobilities but very low carrier concentrations.

Table 5-12: Film properties measured by Hall Effect. Resistivity is compared to that measured by 4-point probe.

Sample	Temp.°C	Substrate	CC (cm-3)	Mobility (cm^2/V-s)	Res. (Hall) (μΩ-m)	Res(4 point) (μΩ-m)
Bi_2Te_3	270	Poly-Si	-1.48E+19	223.6	18.8	18.1
Bi_2Te_3	270	Poly-Si	-1.49E+19	224.6	18.6	16
Bi_2Te_3	250	Oxide	-2.82E+19	206.8	10.7	12.38
Bi_2Te_3	120	Oxide	-4.35E+20	23.88	16.2	-
Sb_2Te_3	250	Poly-Si	3.460E+18	580.6	31.1	31.14
Sb_2Te_3	120	Poly-Si	3.84E+19	24.2	47.6	-

Film Composition

For Bi_2Te_3, films with the correct stoichiometric ratio of 2:3 Bi:Te produced the highest power factors. These films are also the most reproducible due to the tellurium rich deposition process, where excess tellurium is re-evaporated, leaving stoichiometric Bi_2Te_3 behind. However, for

Sb_2Te_3, films with considerable deviation from the stoichiometric 2:3 Sb:Te ratio were found to yield superior power factors. However, due to the large run-to-run variation associated with off stoichiometry deposition, this path was not pursued.

Table 5-13: Comparison of Sb_2Te_3 deposited on oxide.

Temp.°C	Seebeck (µV/K)	Resisitivty (µΩ-m)	Power Factor (mW/K^{2}m)	Sb:Te ratio
230	166	20.6	1.33	**42:58**
230	186	24.1	1.43	**28:72**
230	195	10.7	2.03	**26:74**

Material Source

Antimony telluride depositions were carried out with Sb sourced from both Kurt J. Lesker and Alfa Aesar. Sb_2Te_3 deposited using Sb supplied by Alfa Aesar produced films with superior power factors than films produced by Kurt J. Lesker. It is currently unknown what causes this difference.

Table 5-14: Comparison of Sb_2Te_3 films produces with different Sb suppliers

Sb Supplier	Substrate	Temp.°C	Seebeck (µV/K)	Resisitivty (µΩ-m)	Power Factor	At. Frac. Sb/Te
Alfa Aesar	Oxide	230	166 µV/K	20.6 µΩ-m	1.33	42/58
Kurt J. Lesker	Oxide	230	199 µV/K	38.1 µΩ-m	1.04	38/42

Best Achieved Thermoelectric Thin Films

Deposition conductions for the best reproducible thermoelectric films are detailed below.

Table 5-15: Best Achieved Power Factors for TE Depositions

Film	Substrate	Temp.° C	Rate Bi/Sb:Te	Resistivity (μΩ-m)	Seebeck (μV/K)	Power Factor (mW/K^{2}m)	Bi/Te Ratio
Bi_2Te_3	Poly-Si	260	1:3 Å/s	16.01	-241	3.62	39.8/60.2
Bi_2Te_3	Oxide	245	1:3 Å/s	12.38	-212	3.63	39.5/60.5
Bi_2Te_3	Polyimide	260	1:3 Å/s	24.9	-264	2.79	39.7/60.3
Sb_2Te_3	Poly-Si	240	1:3 Å/s	31.14	165	.86	41:59
Sb_2Te_3	Oxide	220	1:3 Å/s	20.6	166	1.33	39.3:60.7
Sb_2Te_3	Polyimide	245	1:3 Å/s	33.8	176	.916	39.7/60.3

Substrates were composed of silicon with either a 1-μm thick LPCVD poly-silicon layer, 2-μm thick thermal oxide layer, or a 25-μm thick polyimide layer.

5.6 Conclusion

Bi_2Te_3 and Sb_2Te_3 films with power factors of 3.63 and 1.33 mW/K^{2}m have been reliably produced on the insulating substrates required for our μTEG design. The estimated ZTs of these films are 0.72 for Bi_2Te_3 and 0.26 for Sb_2Te_3 assuming a thermal resistivity of 1.5 W/mK [44]. The figure of merit for the produced Bi_2Te_3 film compares favorably with the ZT values of 0.6, 0.12, and 0.4 used in μTEGS from Seiko [12], Freiburg [11] and Fujitsu [22] given in table 4-1. The properties of Sb_2Te_3, however, was lackluster. Depositing Sb_2Te_3 films rich in Te was found to increase the ZT from .26 to .39 (Table 5-16). However, these non-stoichiometric depositions were hard to reproduce and thus not pursued. Even given the poor Sb_2Te_3 film properties, the produced thermoelectric films allow a μTEG figure of merit of 86 μW/K2/cm2 using the high-aspect thermocouple design (Fig. 5-17). Additionally, the optimal temperature for film

deposition was found to be >230° C. As standard photoresists do not survive these temperatures, lift off cannot be used to pattern the film in our μTEGs.

Chapter 6 Vertical Thermocouple Formation

The optimal deposition conditions for co-evaporated Bi_2Te_3 and Sb_2Te_3 on planar substrates were found in chapter 5. Presented in this chapter is the modification of the planar deposition method to produce uniform thermoelectric films on the sidewall surfaces. This sidewall deposition process is what enables our High-Aspect μTEG design to be fabricated, and thus, central to this thesis. A method to pattern these films into separate N & P thermoelectric legs is presented in addition to a process to electrically link the thermoelectric legs in series. The contact resistance of this link is also analyzed. It was found that Bi_2Te_3 and Sb_2Te_3 deposited over vertical surfaces show inferior thermoelectric properties compared to planar films. Methods to reduce this discrepancy, its anticipated impact on μTEG performance, as well as potential causes and solution.

6.1 Deposition Overview

Depositing thin films over tall vertical surfaces poses several challenges. First, film patterning is a concern as high aspect structures interfere with photoresist patterning. Spun photoresists are physically blocked by the presence of the scaffolds, leading to pooling and poor step coverage. Spray on resist patterning methods can achieve good step coverage. However, difficulties with the exposure of the photoresist over vertical surfaces remain.

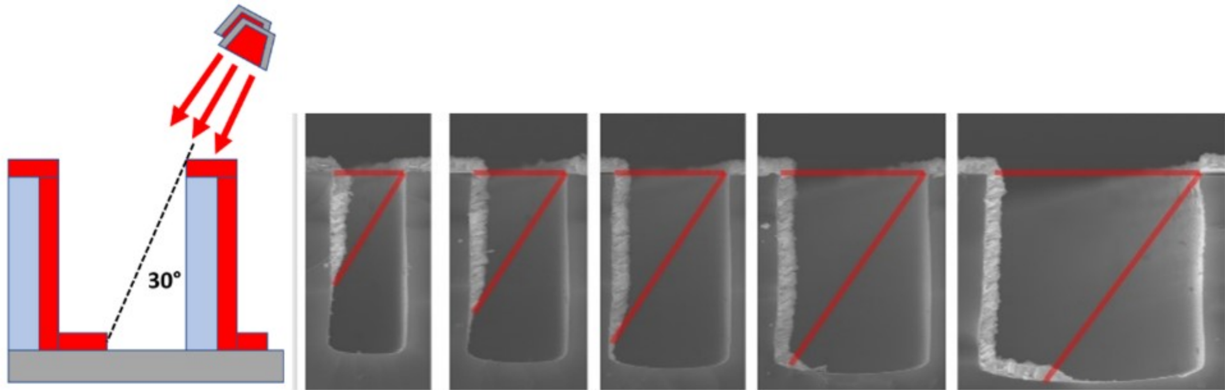


Figure 6-1: (A) Single sided evaporation of TE material and (B) chamber set up.

Fortunately, these two issues can both be solved by the angling of the material source with respect to the wafer (Fig. 6-2, above) to form a thermoelectric leg without additional patterning. The self-shadowing effect of the columns themselves are used to pattern each individual thermocouple. To form the N-type thermoelectric leg, Bi and Te sources were placed 30° from the wafer normal facing right (Fig. 3). Due to the line-of-sight nature of evaporation, the columns block film deposition on the left facing sidewall surface, forming an N-type thermoelectric leg on the right sidewall. At the 30° angle, the thickness of the sidewall film is roughly equal to the thickness of film deposited on the planar surfaces on top of the column and in the valley between columns. To compensate for non-uniformity due to a lack of substrate rotation during deposition, Bi_2Te_3 was formed under Te rich conditions. Excess elemental tellurium re-evaporates from the surface faster than it deposits, leaving stoichiometric Bi_2Te_3 behind in a Bi limited system.

To form the P-type thermocouple, Sb and Te sources were placed facing left. Thus, after deposition, a N & P leg pair is created on each column (Fig. 6-3). This deposition method allows the creation of a Bi_2Te_3 and Sb_2Te_3 leg-pair on each scaffold with minimal patterning required. At the adjoining planar surfaces, a Bi_xSb_yTe composite forms. This composite material serves as the basis for electrical contact between the legs. This approach also allows most of the surface

area of the wafer to serve as the contacts, improving contact resistance. In addition, the patterning of all electrically active elements on a single wafer allows for relaxed bonding requirements for the top cap. As electrical connection to the cap is not needed, the resulting device does not require 100% bond yield of each TE leg pair to the top cap for current routing. Due to the self-patterned nature of deposition, the leg density is determined by the scaffold density. With sufficiency dense scaffolds, TE leg pair densities upwards of 100-leg pairs/mm^2 can be achieved, enhancing voltage output.

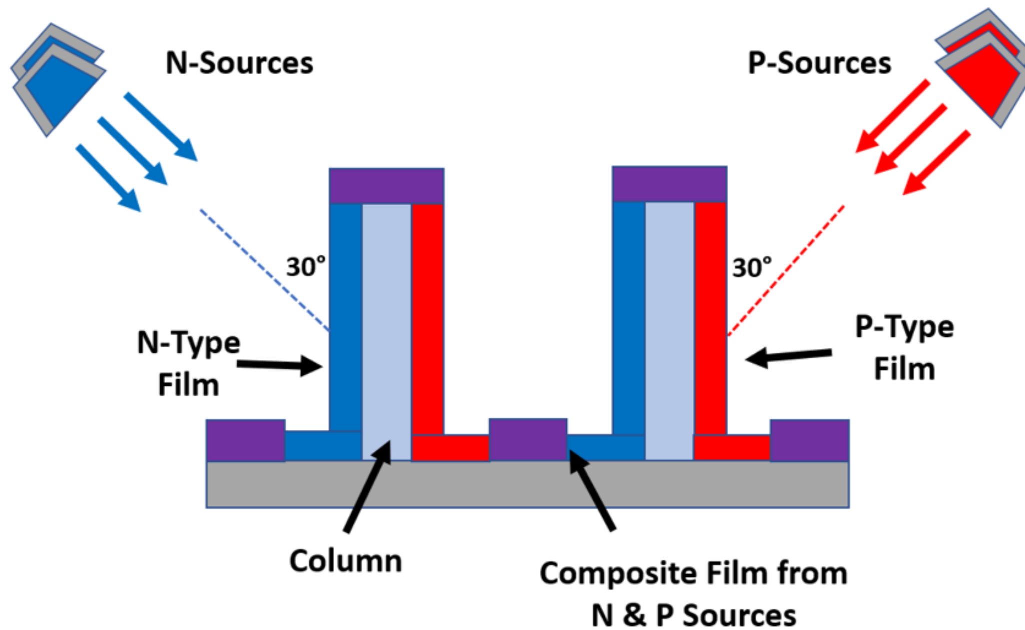


Figure 6-2: Double sided deposited of two different TE materials

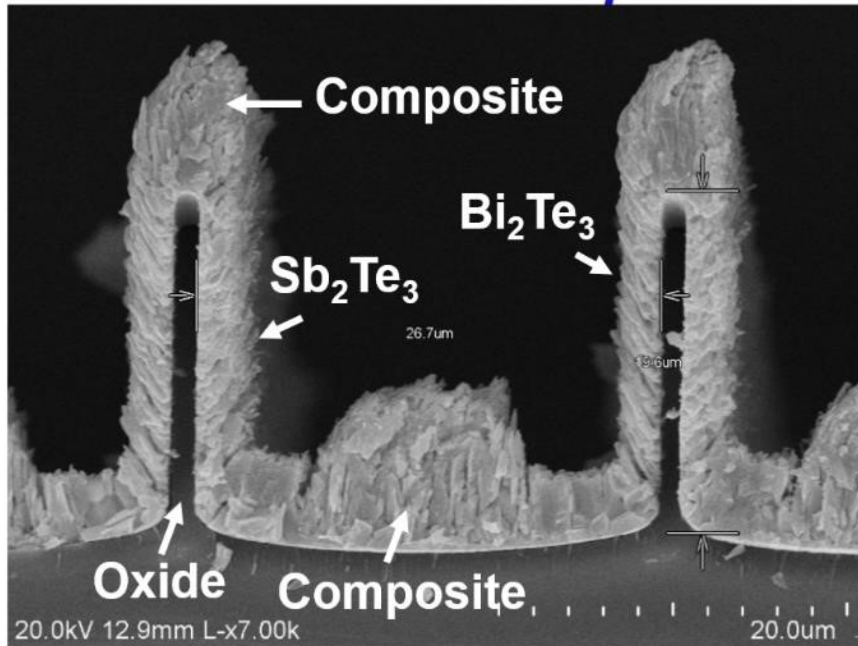


Figure 6-3: Cross-section of deposited vertical thermocouples.

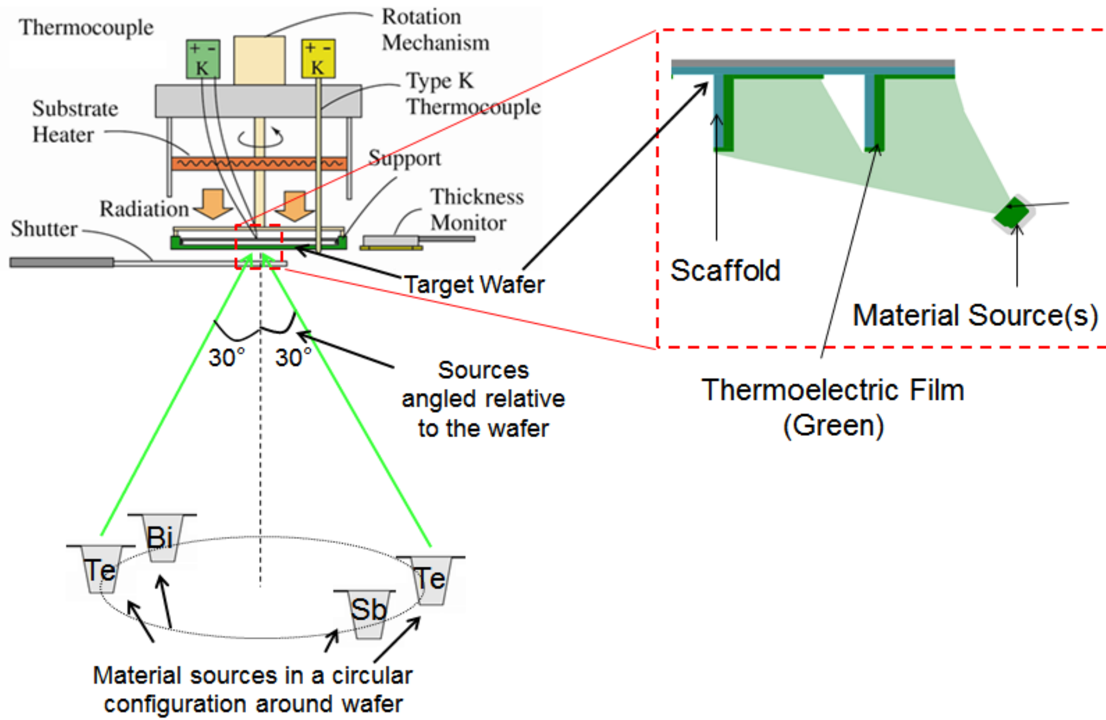


Figure 6-4: Chamber configuration during sidewall deposition of Bi_2Te_3 and Sb_2Te_3

6.2 Contact Resistance

Concurrent Bi_2Te_3 and Sb_2Te_3 Deposition

During most depositions, evaporation of the N-type and P-type film were carried out simultaneously. This method allowed a lower resistance for the device structure compared to serial deposition of the films. To measure the contact resistance, a contact chain of N- $Bi_2Te_3$and P-Sb_2Te_3 thermoelectric legs was created. The resistance of the structure was then measured through 4-point probe. The resistances of the $Bi_2Te_3$and Sb_2Te_3 film was assumed to be identical to those found previously for planar films, detailed in table 5-11. Planar Bi_2Te_3 films located on process control modules could not be measured as the difference in the deposition rate altered the film properties of the vertically deposited films compared to the planar films.

The N & P legs were electrically linked solely by the composite BiSbTe film. The resistance of the structure was found to be 4 times higher than expected using the average resistivities of the P & N type film. The average contact resistance was estimated at 4.2E-8 Ω-m^2, significantly higher than the 3E-9 Ω-m^2 resistivity found for Bi_2Te_3 to Au contacts. Thus, Au was later added underneath the thermoelectric film to reduce the resistance of the junction during device fabrication, as detailed in chapter 8.

It is unknown what the relative contract resistance values of the Bi_2Te_3 – BiSbTe junction and the BiSbTe – Sb_2Te_3 junction are. BiSbTe is typically P-type, so it is possible the Bi_2Te_3 – BiSbTe junction disproportionately affect total contact resistance. Additionally, measurements on control devices consisting solely of BiSbTe film as shown in chapter 8.1 and 8.2 imply the BiSbTe film itself, and not the junction between films, is the cause of the increased resistance.

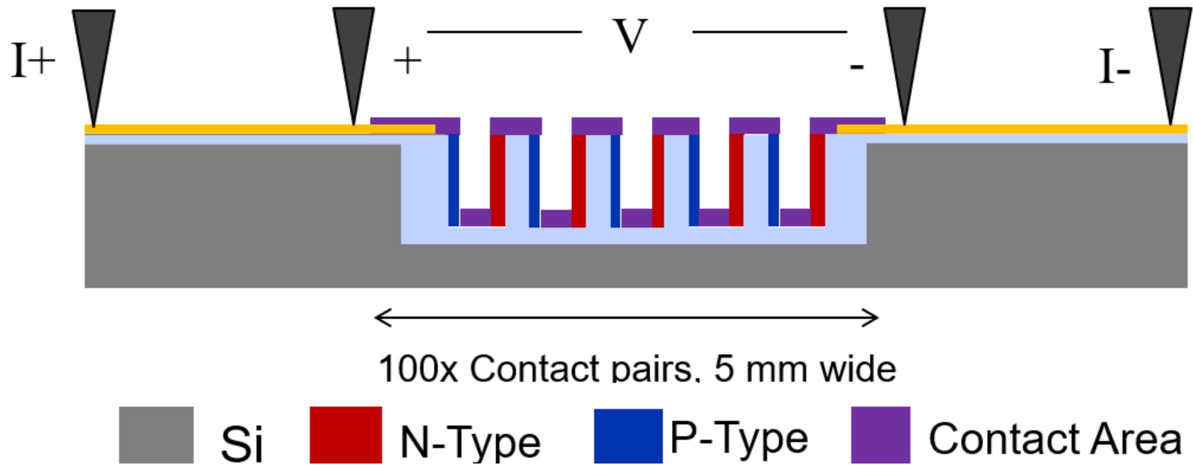


Figure 6-5: N-Bi_2Te_3, BiSbTe, P-Sb_2Te_3 contact chain and measurement. Films were deposited concurrently.

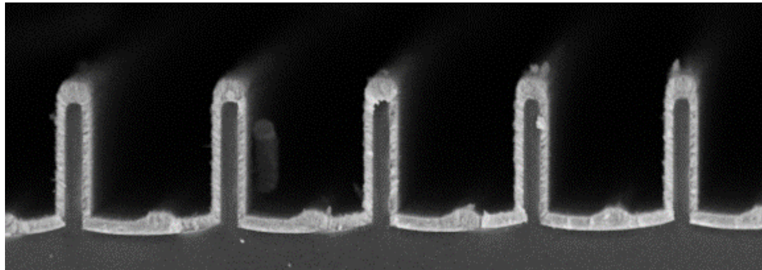


Figure 6-6: Cross section of a N-Bi_2Te_3, BiSbTe, P-Sb_2Te_3 contact chain. Films were deposited concurrently.

Serial Bi_2Te_3 and Sb_2Te_3 deposition

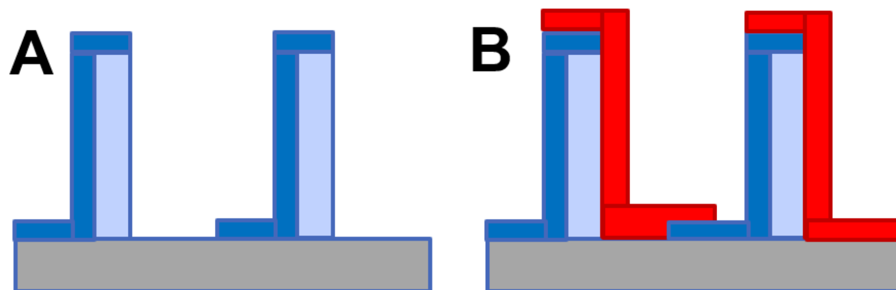


Figure 6-7: Serial deposition (A) deposition of N-Bi_2Te_3, and (B) deposition of P-Sb_2Te_3 afterwards.

Deposition of the N-Bi_2Te_3 and P-Sb_2Te_3 thermoelectric material can occur serially or at the same time. The advantage of serial deposition is the ability to optimize the deposition conditions

of each film seperately. Te re-evaporation from the substrate does not have to be considered, leading to better films. The drawback of serial deposition is a much greater contact resistance between the N and P legs in the area where they overlap. While the contact of N-Bi_2Te_3 and P-Sb_2Te_3 does not form a P-N diode, the junction resistance is still high. This junction resistance was measured through cross-bridge Kelvin structures. The films for these structures were patterned through shadowmask.

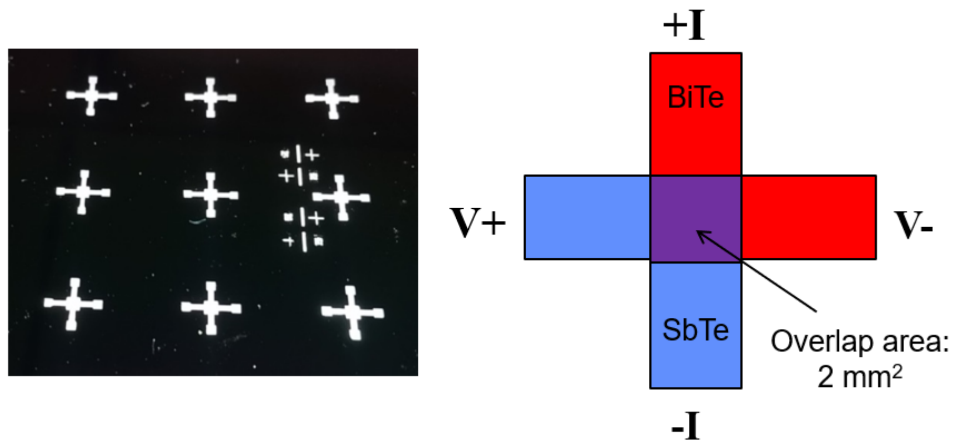


Figure 6-8: Cross bridge Kelvin Structures for measurement of contact resistivity.

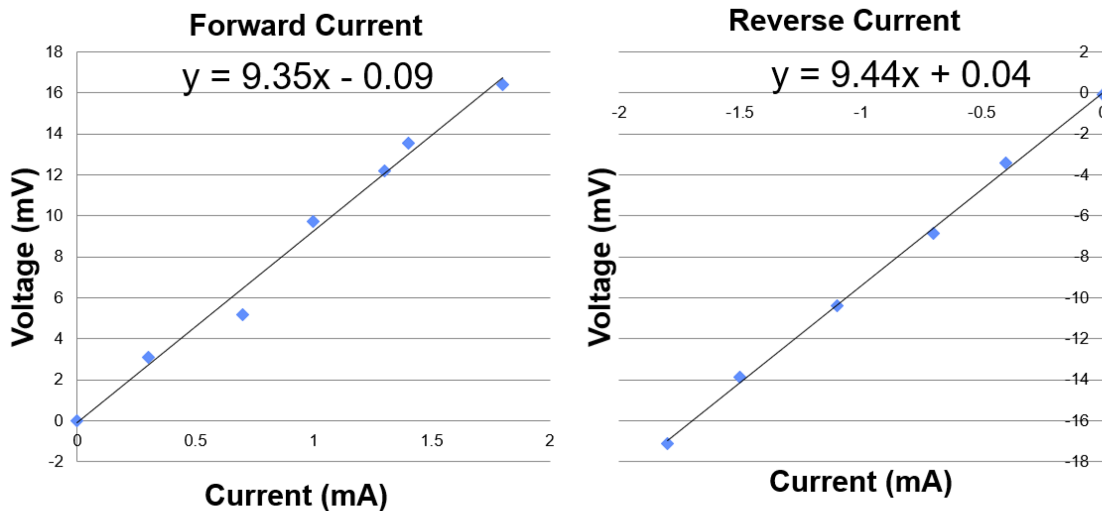


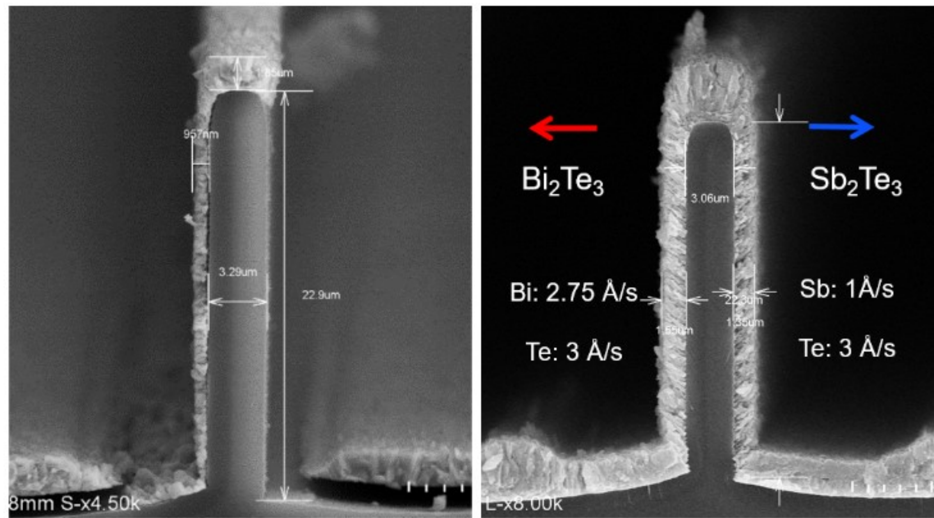
Figure 6-9: IV curves across the Bi_2Te_3 – Sb_2Te_3 junction.

Cross bridge Kelvin structures were formed on a standard silicon wafer with 1.4-μm of thermal oxide on top. Contact resistivity was measured to be 18.7E-6 Ω-m^2 for stoichiometric Bi_2Te_3 and Sb_2Te_3 deposited at 260°C and 230°C, respectively. To reduce the contact resistance, it may be possible to add an intermediate Au layer between the two TE film depositions. However, patterning of this film layer is difficult given the narrow width of the scaffolds. Additionally, Au must be kept away from the sidewall of the scaffolds to prevent degredation of thermocouple performance.

When the N & P legs are deposited seperately, the resulting junction is highly resistive at 10^{-5} Ω-m^2 as measured by cross-bridge kelvin structures. However, when both films are deposited simultaneously, the connecting material is ohmic and has an upper limit of 10^{-8} Ω-m^2. For comparison, Bi_2Te_3 to Au were previously measured by our group to have a resistivity of 3E^{-9} Ω-m^2 [28].

6.3 Film Uniformity

Getting consistent film stoichiometry along the length sidewall is difficult due to the different dispersal patterns of tellurium, which is more isotropic, and bismuth, which is more anisotropic. Furthermore, as the Bi and Te sources must be exposed to only one face of the scaffold, full dome rotation could not be used to improve uniformity. The solution implemented was to angle the Bi directly orthogonal to the vertical surface of the scaffold. This, combined a with a large, 1 meter throw distance, allowed for conformal coating of bismuth across the wafer. Te was placed at 30°C offset from the surface and did not form a uniform coating. However, as the deposition process is tellurium rich, the excess tellurium evaporated, leaving uniform, stoichiometric film behind. This effect was less noticeable for Sb and Te.



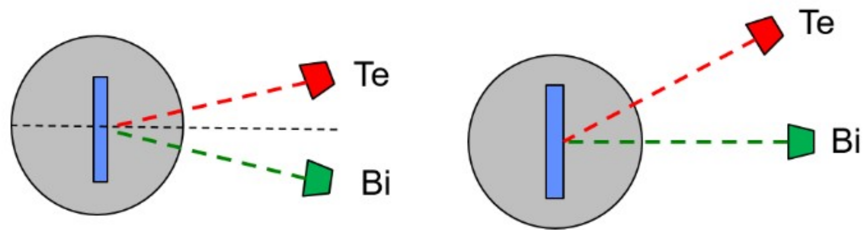


Figure 6-10: Film growth on vertical surfaces with (A) scaffold normal between sources and (B) scaffold normal centered on the Bi source.

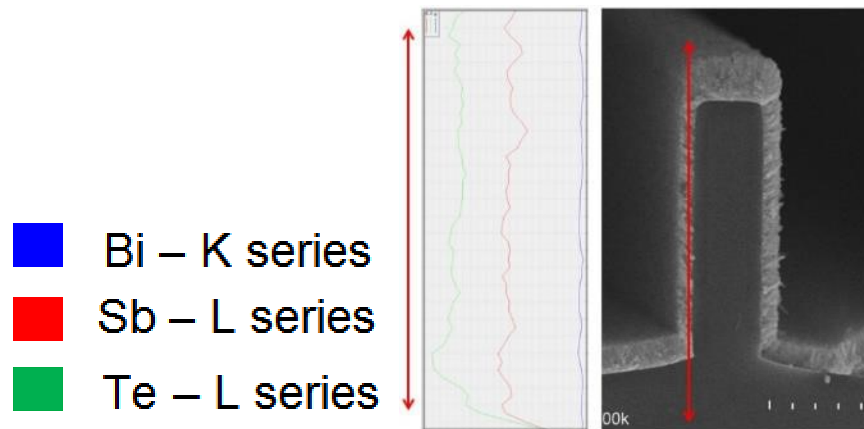


Figure 6-11: Film stiochiometry along the vertical scaffold surfacem measured via XRD.

6.4 Deposition Ratios

Compared to planar films where a simple 1: 3 Å/s Bi:Te deposition rate provided the necessary Bi, vertical films required increased Bi deposition rates of 2 – 2.75 Å/s depending on the deposition temperature. Sb_2Te_3 films required an increase in the Sb deposition rate from 1 to 1.5 Å/s. Tellurium re-evaporation from the substrate is theorized as one of the possible reasons for the need to increase Bi and Sb deposition rates to produce stoichiometric films.

Table 6-1: Bi_2Te_3 Film Composition

Film	Substrate	Temperature (°C)	Bi Dep. Rate (Å/s)	Te Dep rate (Å/s)	Bi:Te ratio
Planar	Oxide	250	1.0	3.0	40/60
Planar	Oxide	230	1.0	3.0	40/60
Sidewall	Oxide	230	1.0	3.0	19/81
Sidewall	Oxide	275	2.75	3.0	42/58
Sidewall	Oxide	265	2.2	3.0	41/59
Sidewall	Oxide	250	2.0	3.0	43/57
Sidewall	Oxide	110	3.0	3.0	41/59

Table 6-2: Sb_2Te_3 Film Composition

Film	Substrate	Temperature (°C)	Sb Dep. Rate (Å/s)	Te Dep rate (Å/s)	Bi:Te ratio
Planar	Oxide	230	1.0	3.0	40/60
Sidewall	Oxide	250	1.5	3.0	39:61
Sidewall	Oxide	230	1.5	3.0	41:59

6.5 Vertical Film Morphology

A significant change in film morphology was found transitioning from planar to sidewall films. Sidewall films showed angled grain structures, forming narrow rod-like columns reminiscent of the catalyzed vapor-liquid-solid growth of nanowires [76]. These columns are angled with a 30° away from the surface at a deposition temperature 260° C (Fig. 8B). This angle has been found to be temperature dependent but unrelated to the angle of the sources. Under standard deposition conditions, sidewall films also exhibit voids between successive crystal grains (Fig. 6-12), unlike planar films which are dense and void free. (Fig. 6-13). This difference in morphology is thought to be the root cause of the difference between planar and vertical TE film performance.

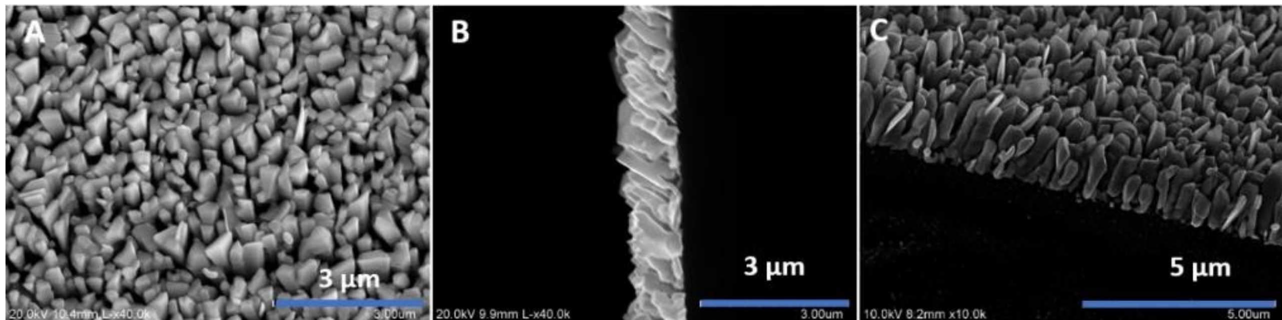


Figure 6-12: Planar Film Growth of Bi_2Te_3. (A)Front, and (B)(C) Side views.

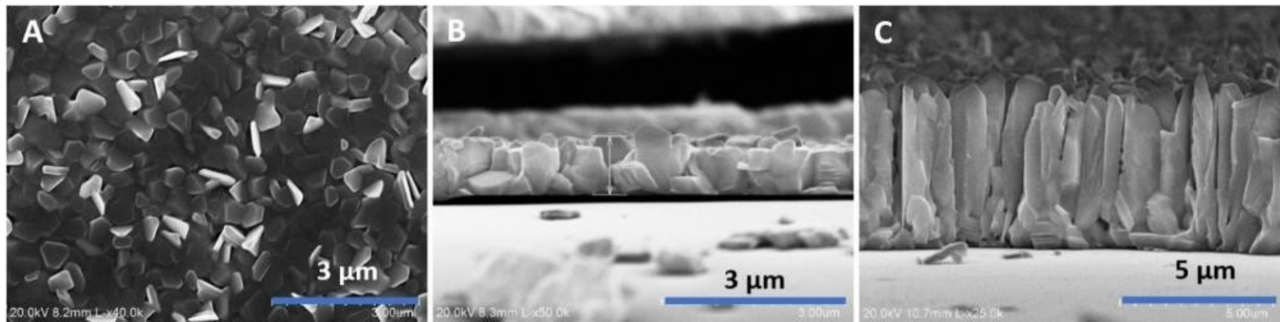


Figure 6-13 : Planar Film Growth of Bi_2Te_3. (A)Top, and side views of (B) thin and (C) thick film depositions.

At a deposition temperature of 250°C, films on planar substrates exhibit an initial 1-µm "seed" layer (Fig. 6-14) before columnar growth, as previous discussed in Chapter 5.4. However, vertical film depositions at the same temperature show a much thinner seed layer, at only 200 nm. This seed layer never fully merges together, like in the planar case. Over this "seed" layer, the columnar crystal growth exists, but shows a strong direction preference at about 45° from the vertical. This angle is believed to be in line with the C-axis of the Bi_2Te_3 crystal. The angle of this growth decreases with increasing deposition temperature, unlike planar film growth, where the orientation of the columns is always perpendicular to the substrate. The cause of this angled growth is currently uncertain, though factors impacting this angle are investigated in section 6.9.

The sparse growth of these columns is reminiscent of vapor-liquid-solid growth of nanowires, where the growth is primarily vertical direction and not lateral. However, unlike VLS growth, there is no evidence of liquid present at the tips of the columns and the deposition temperature is far below the 580°C melting point of Bi_2Te_3. Thus, it is theorized that bismuth telluride preferentially grows along the C-axis where the Van der Waal gaps exists. This implies that the key to creating a dense, uniform sidewall film lies in the creation of a dense, C-oriented seed layer. Sidewall Sb_2Te_3 films displays similar growth characteristics to sidewall Bi_2Te_3 films.

However, grain structures in sidewall Sb_2Te_3 films are typically wider than Bi_2Te_3 and show less gaps.

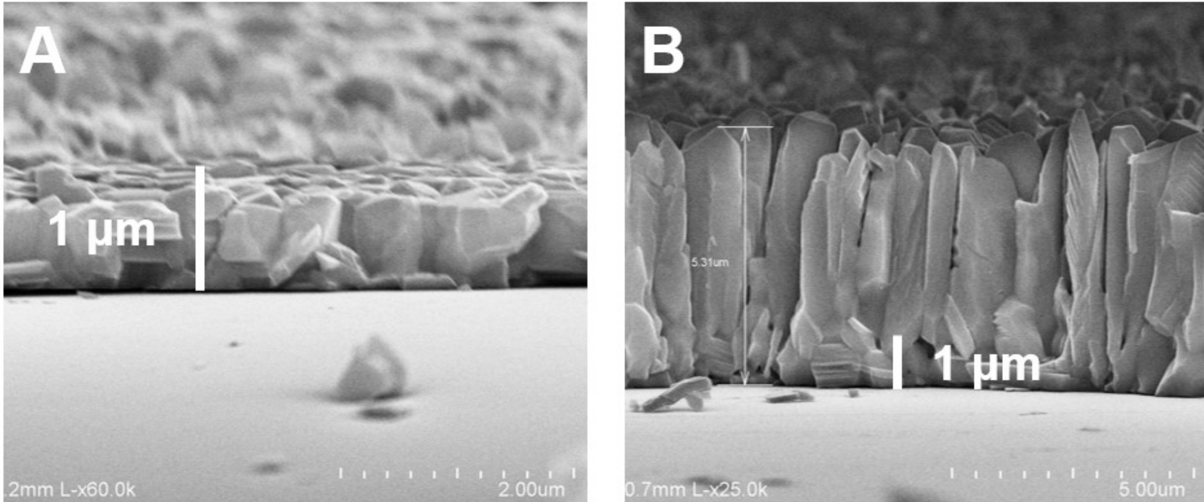


Figure 6-14: (Left) Initial "seed" Bi_2Te_3 crystal growth and (Right) Vertical, columnar Bi_2Te_3 crystal growth over the "seed" layer.

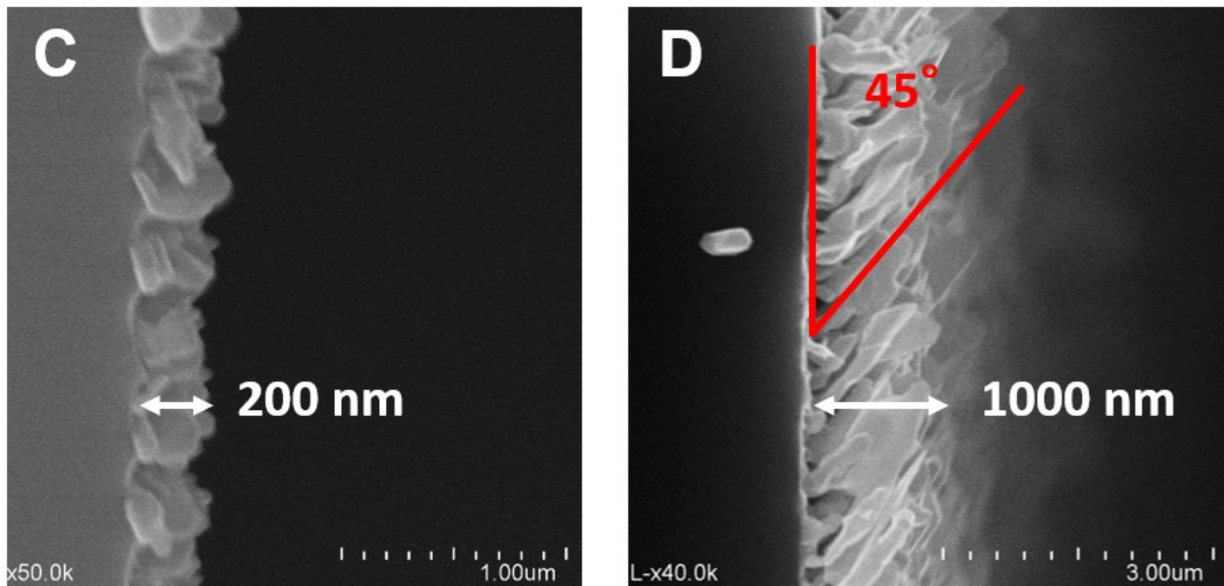


Figure 6-15: (Left) Initial "seed" Bi_2Te_3 crystal growth on a vertical substrate (Right) Angled, columnar Bi_2Te_3 crystal growth over the "seed" layer.

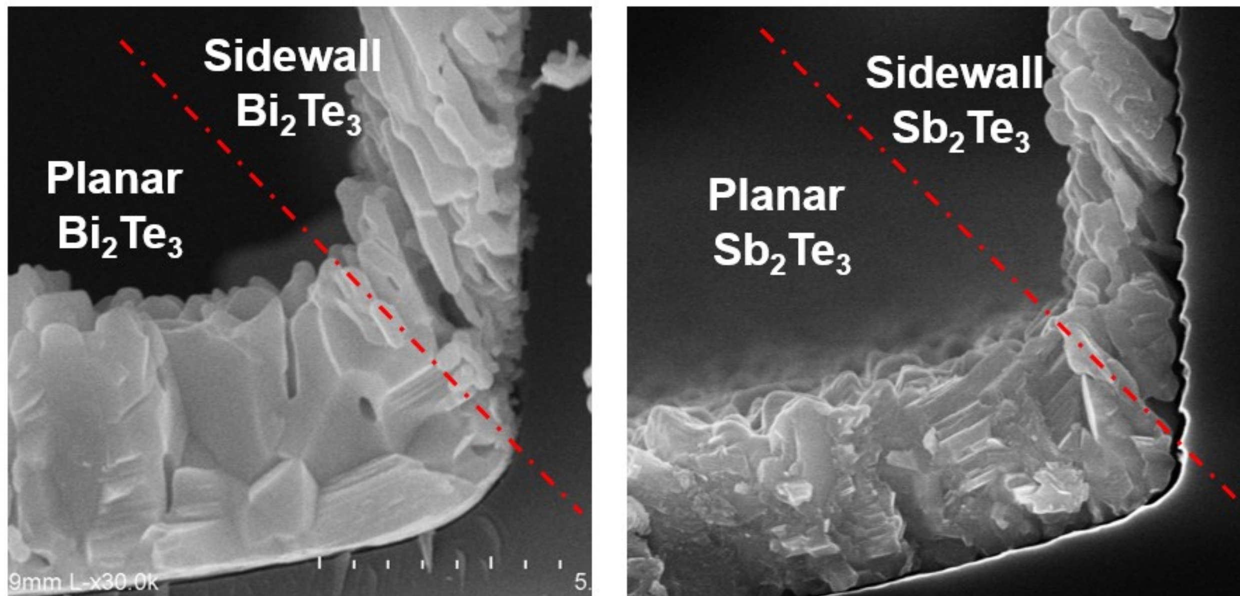


Figure 6-16: Transition of Bi_2Te_3 and Sb_2Te_3 from planar to vertical film morphologies on an oxide substrate. The transition in crystal structure occurs immediately once the substrate orientation changes.

Film Orientation and Quality

The crystal orientation of sidewall films was measured through X-ray diffraction (XRD). The measurements were conducted with the beam facing orthogonal to the surface of the sidewall. XRD showed film growth on vertical substrates are not c-oriented with respect to the substrate normal, compared with the heavily C-oriented films (Fig. 5-10) associated with planar film depositions. Bi_2Te_3 in particular shows lower peaks from C-oriented planes (0 0 3), (0 0 6) compared to reference Bi_2Te_3 powder. It is theorized that the direction of the grain structure represents the C-axis of the Bi_2Te_3 crystal structure and thus accounts for the near isotropic XRD returns. The average full-width-half-max of the Bi_2Te_3 and Sb_2Te_3 sidewall peaks were < .2°. on par with .17° and .19° of planar Bi_2Te_3 and Sb_2Te_3 films.

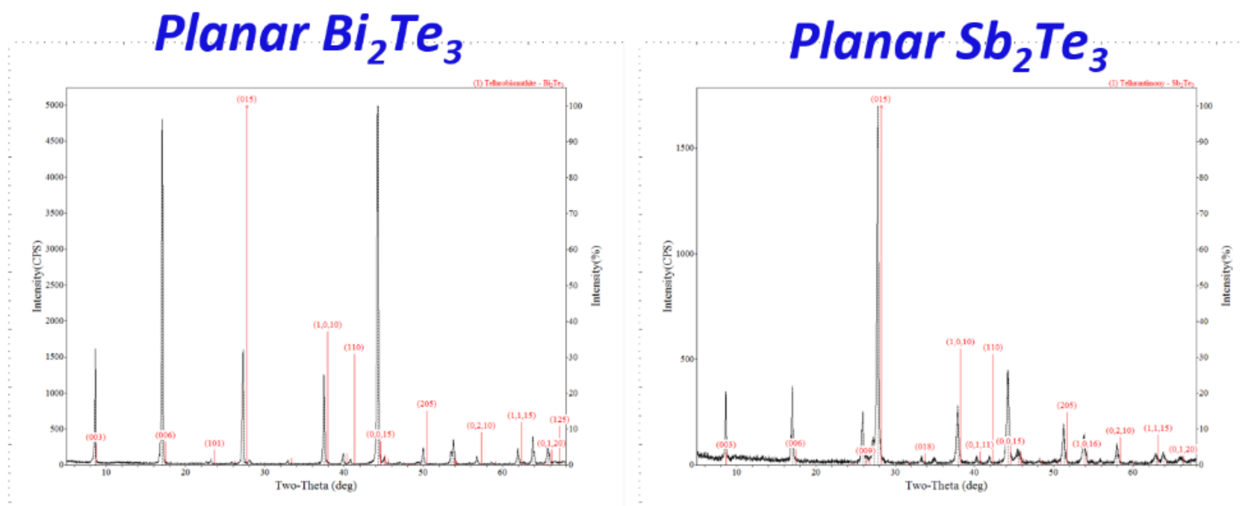


Figure 6-17: XRD of Bi_2Te_3 and Sb_2Te_3 deposited on planar oxide surfaces. Red lines represent the XRD returns of powdered Bi_2Te_3 and Sb_2Te_3.

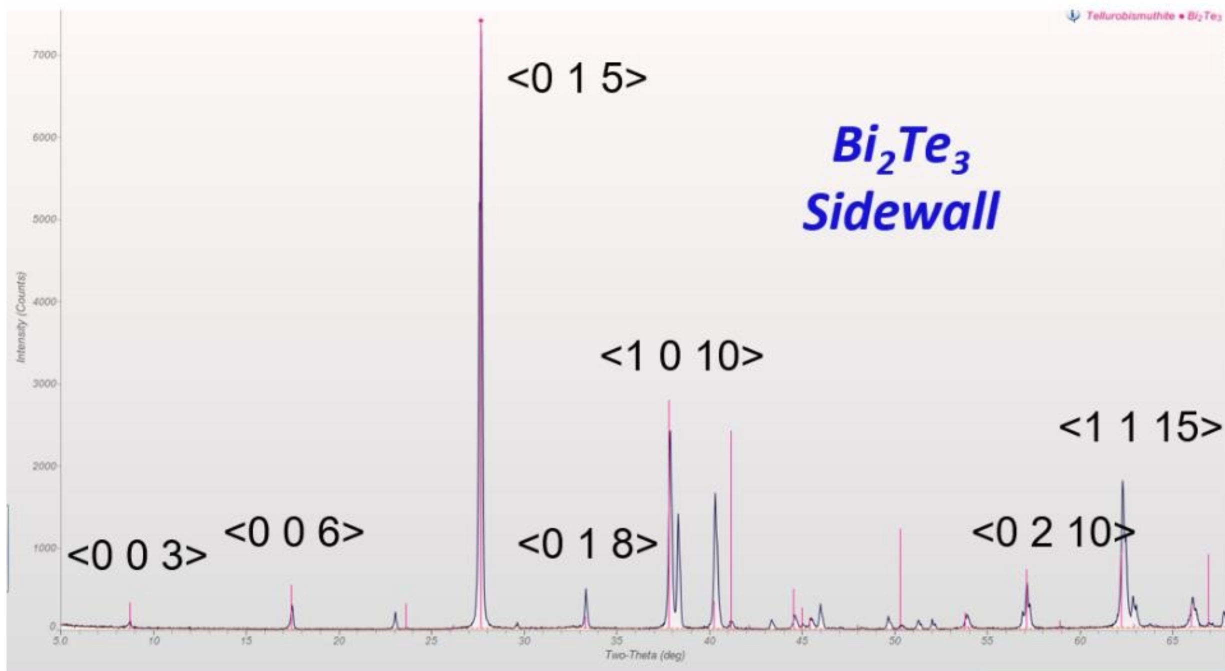


Figure 6-18: XRD of Sidewall Bi_2Te_3 deposited at 250°C on oxide. Crystal planes for major peaks are labeled. Red lines represent the XRD returns of powdered Bi_2Te_3.

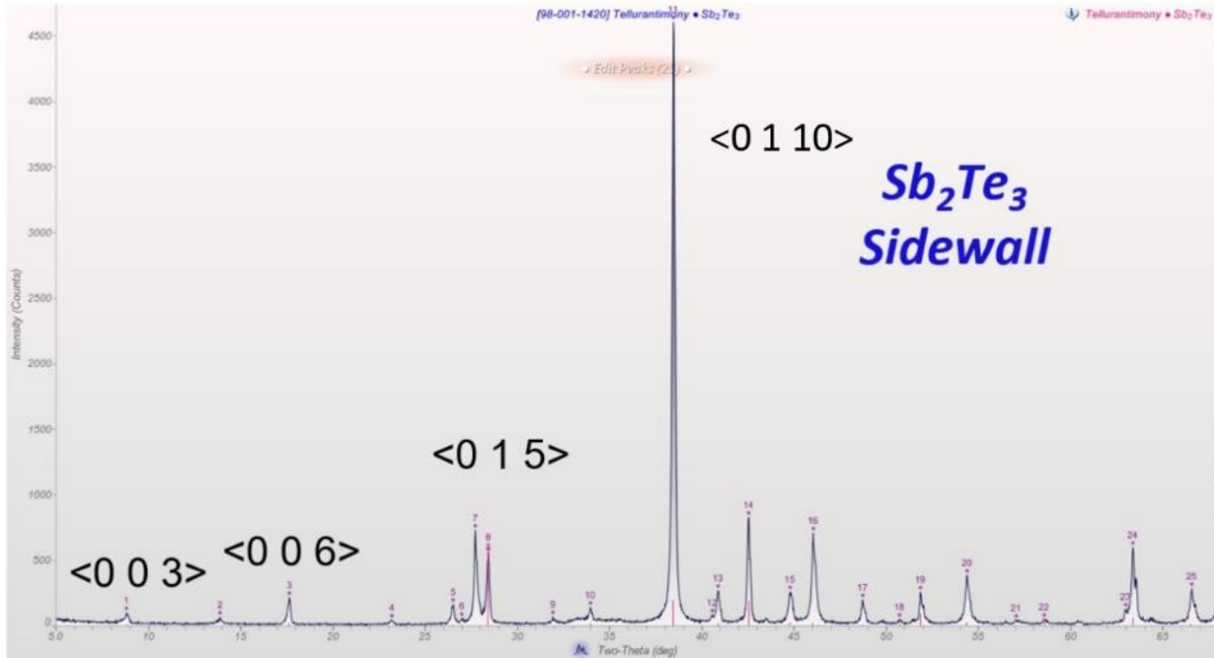


Figure 6-19: XRD of Sidewall Sb_2Te_3 deposited at 250°C on oxide. Crystal planes for major peaks are labeled. Red lines represent the XRD returns of powdered Sb_2Te_3.

6.6 Film Measurement

Measurement of the vertical thermoelectric properties of the sidewall film was difficult due to issues with temperature measurement across a small, 25-µm gap. Thus, only select sidewall films were measured. A test structure consisting of 1 mm of glass anodically bonded to 500-µm Si wafers on both sides was devised to increase the temperature drop across the thermoelectric material. Si on both sides of the glass served as heat spreaders and temperature probes. Surface mount thermocouple were glued to both ends of the silicon for temperature measured. The sidewall surface of the structure was created by multiple passes with a dicing blade to remove material.

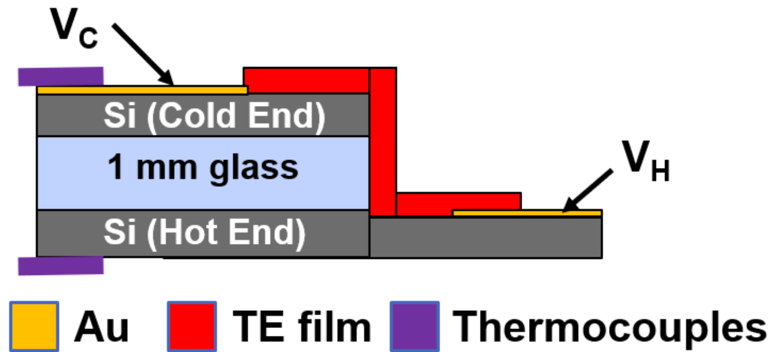


Figure 6-20: Test structure for the measurement of sidewall films in the vertical direction.

Resistivities for Bi_2Te_3 films deposited using this method were extremely high, on the order of 100s of uΩ-m.

Table 6-3: Film resistivities for TE films deposited on a diced glass surface.

Substrate	Film	Temp (°C)	Res. (uΩ-m)	Dep. Frac. (Å/s)	Composition Bi/Sb : Te	Seebeck
Si/Glass/Si	Bi_2Te_3	250	100 – 200	2 : 3	42 : 58	-
Si/Glass/Si	Bi_2Te_3	250	100 – 200	2 : 3	40 : 60	-
Si/Glass/Si	Bi_2Te_3	275	200 - 300	1.5 : 3	40 : 60	-
Si/Glass/Si	Sb_2Te_3	250	20	1 : 3	30 : 70	165

This was due to the extremely large roughness of the diced glass surface. The topology of the surface created large discontinuities in Bi_2Te_3 film which increased resistance. Unlike Bi_2Te_3 grown on planar surfaces, films on vertical surfaces were unable to “fill in” these gaps to reduce electrical resistance. Sb_2Te_3, however, did not have this issue and formed films with comparable properties to planar films. However, this level of performance could not be reproduced with stoichiometric Sb_2Te_3 films on oxide.

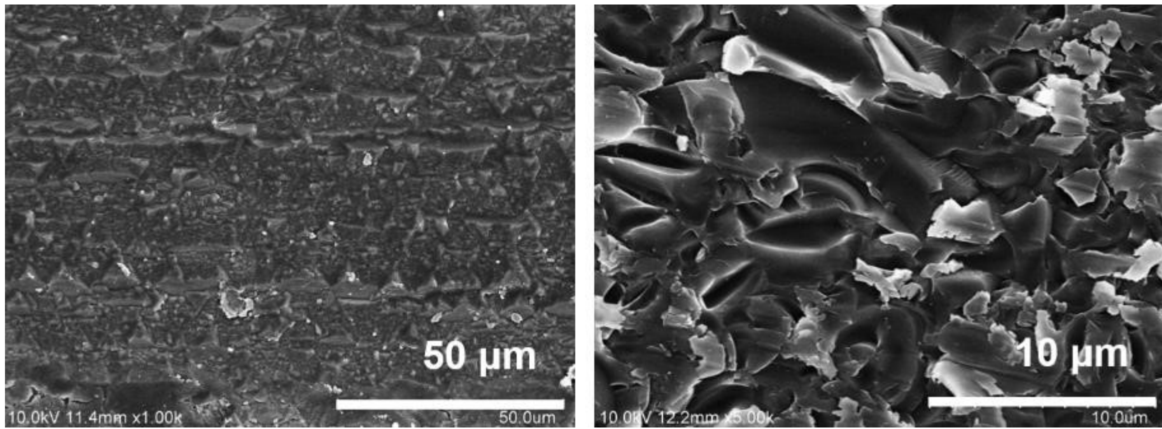


Figure 6-21: SEM of the surface of a glass surface dicing using a 30 µm grit diamond blade and a spindle speed of 24K RPM.

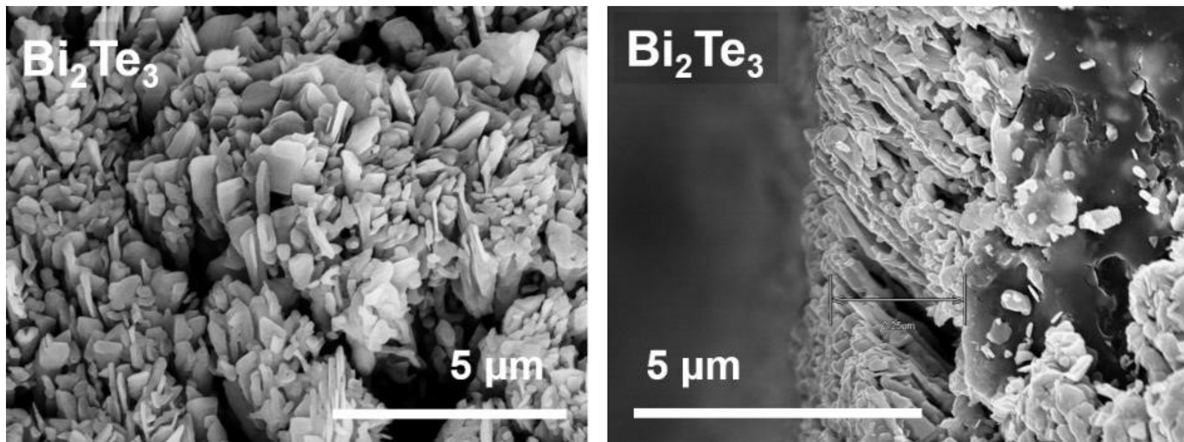


Figure 6-22: SEM of (Left) Front and (Right) Sideview of Bi_2Te_3 deposited on diced glass

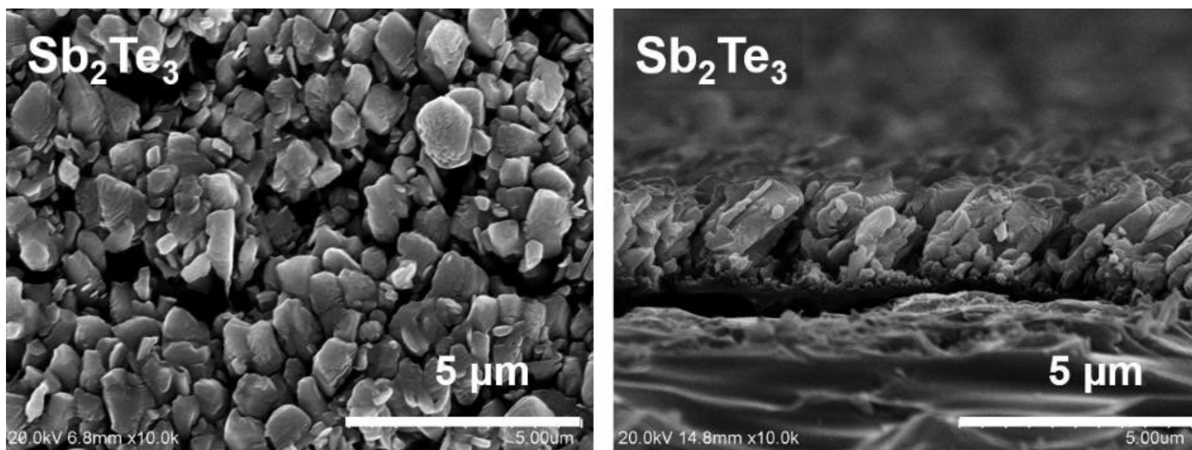


Figure 6-23: SEM of (Left) Front and (Right) Sideview of Bi_2Te_3 deposited on diced glass.

The lateral properties of the vertical film were easier to measure. A test structure composed of two closely spaced pillars was created. The first pillar acts as a "blocker" to prevent unwanted film deposition on the bottom surfaces of the substrate. Combined with a shadow mask, the structure is capable of creating a long strip of TE film solely on the sidewalls of the pillar. The Seebeck and electrical resistance of this film can then be easily measured.

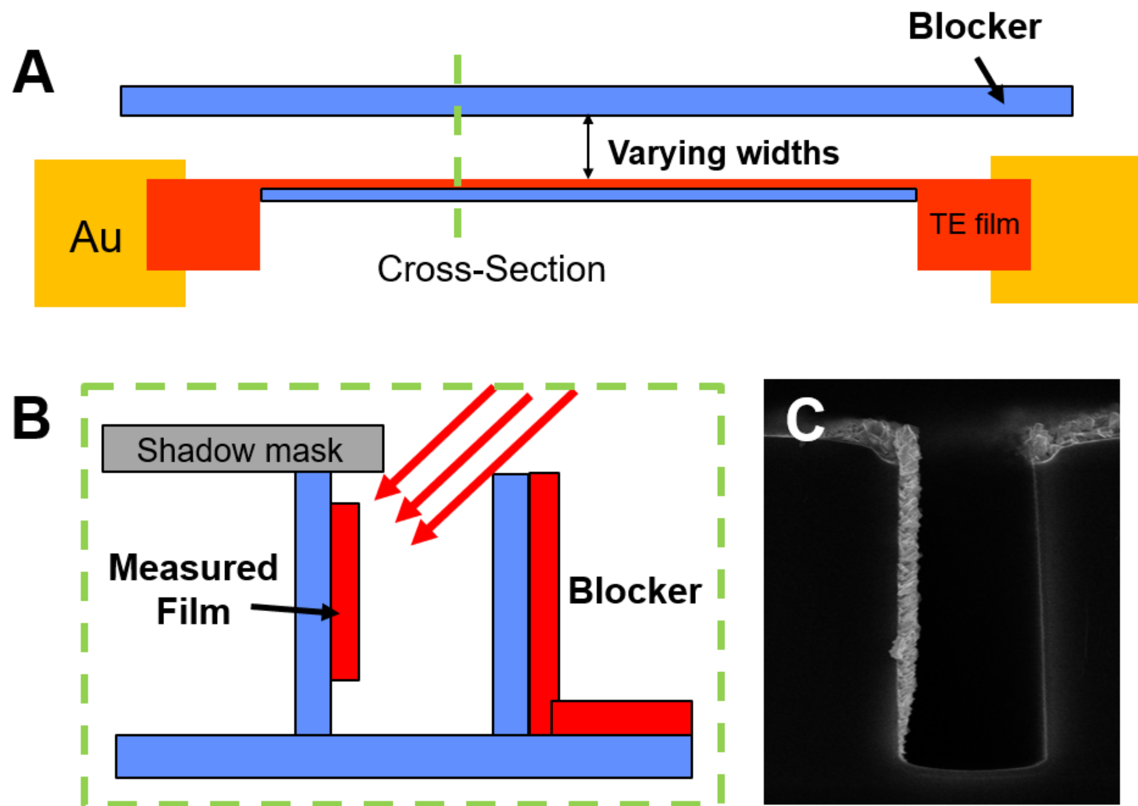


Figure 6-24: Test structure of measurement of lateral film properties.

6.7 Vertical Film Performance

Table 6-4: Best measured power factors of Planar and Sidewall Films

Film	Type	Substrate	Dep. Temp. (°C)	Seebeck (μV/K)	Resistivity (μΩ-m)	Power Factor (mW/K^2m)	ZT (Est)
Bi_2Te_3	Sidewall	Oxide	240	-160*	30*	0.85	**0.16**
Bi_2Te_3	Planar	Oxide	245	-212	12.38	3.63	0.68
Sb_2Te_3	Sidewall	Oxide	240	120*	30*	0.5	**0.10**
Sb_2Te_3	Sidewall	Diced Glass	250	165	20	1.36	**0.26**
Sb_2Te_3	Planar	Oxide	220	166	20.6	1.3	0.24

*Lateral properties measured

The power factors of the best achieved vertical films are markedly worse than that of planar films. Part of the reason is believed to be due to the voids present on the vertical films, increasing film resistivity. Additionally, the orientation of the films is not optimal, which would cause a reduction in the Seebeck coefficient as cross-plane Bi_2Te_3 and Sb_2Te_3 power factors are worse than in-plane Bi_2Te_3 and Sb_2Te_3 power factors. However, even given the subpar sidewall film performance, the High-aspect μTEG design was still expected to produce a FoM of 30 $\mu W/K^2/cm^2$ (Fig. 6-25).

Additionally, voids in the Bi_2Te_3 and Sb_2Te_3 films are likely to increase the thermal resistivity of the film, partially compensating for the decrease in power factor. This potential effect was not considered in table 6-4 or figure 6-26.

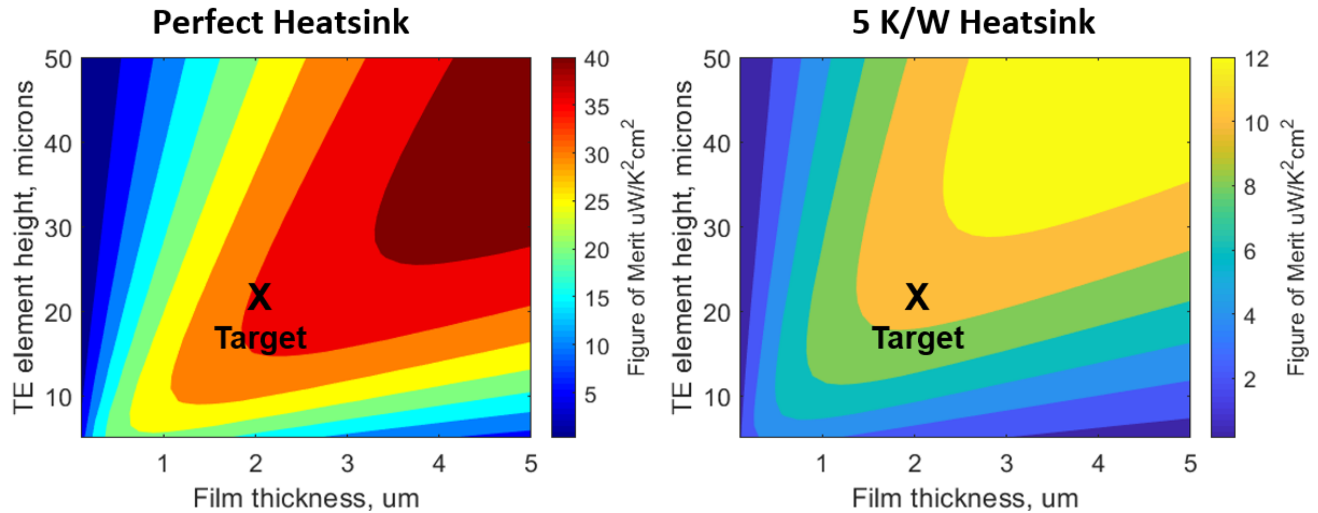


Figure 6-25: Revised performance estimated with achieved Vertical TE films.

6.8 Vertical Film Improvement

The two main causes responsible for the decrease in sidewall film performance were thought to be: angled growth, which caused non-optimal orientation of the films, and discontinuities in the film, which increased electrical resistance. Attempts to resolve these two issues are detailed in this section.

Temperature Effects

A potential cause of this growth phenomena was thought to be due to lower temperature existing on the scaffold compared to the bottom surface of the substrate. To test this theory, Bi_2Te_3 and Sb_2Te_3 films were deposited on a partially oxidized pillar at 230°C. This pillar was 5-µm wide with 500 nm of thermal oxide grown on each side. The 5-µm silicon backbone provides a good thermal contact to the bulk of the wafer, reducing the temperature difference from the planar surface to the sidewall surface. The addition of this silicon backbone was not found to affect the film morphology, ruling out temperature differences from the vertical to planar surface as the cause of the angled grain growth.

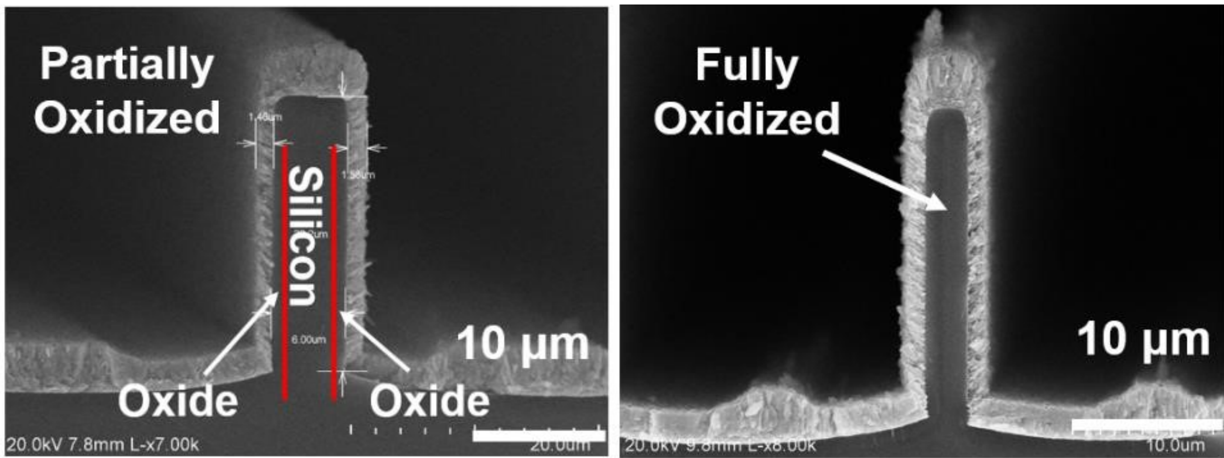


Figure 6-26: Deposition of thermoelectric films on a (Left) partially and (Right) fully oxidized scaffold

Similar to planar Bi_2Te_3 films, the grain size of the initial "seed" layer was found to increase with deposition temperature. However, compared to planar films, the grain size is dramatically reduced for a given temperature on vertical surfaces. At 220°C, grain sizes were roughly 100 nm in diameter for sidewall films compared with 700 nm for planar films.

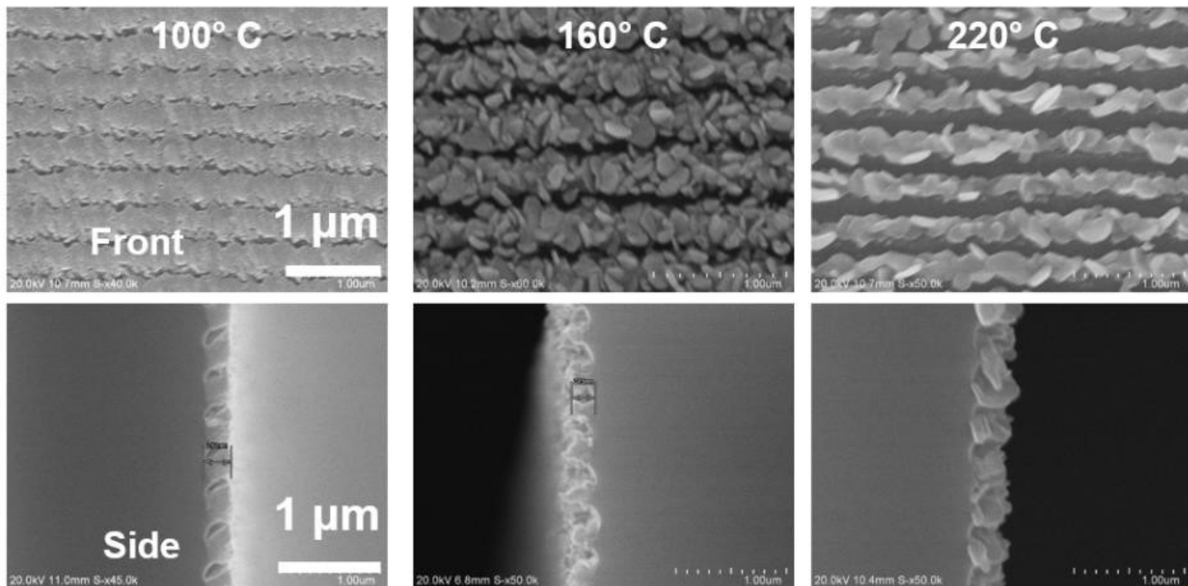


Figure 6-27: Temperature affects on seed layer

Due to the small grain sizes, the "seed" layer never fully merges before columnar type film growth starts, leading to voids in the thermoelectric film. The mechanism determining the size of this initial seed layer is believed to be related to the mobility of the initial Bi and Te atoms impinging on the substrate surface. At higher mobilities – determined by substrate temperature – atoms could move farther between nucleation sites without crystallizing. This causes a reduction in the nucleation site density, but also allows the growth of larger grains. Why temperature affects the thickness of this initial seed layer and why the grain sizes varies from planar to vertical surfaces require further investigation.

Nucleation Site Density

A potential solution to the discontinuous grain structures was to increase the nucleation site density for the initial film through the use of a separate seed layer. This was thought to lead to greater columnar grain density, eliminating the voids and reducing film resistance.

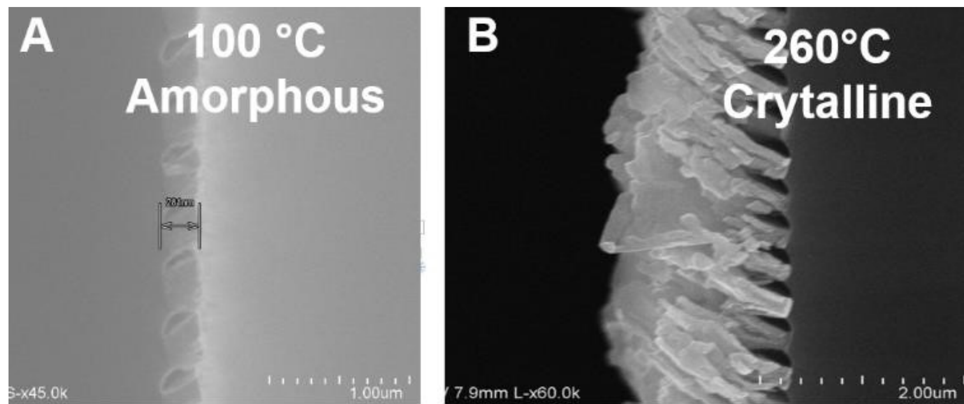


Figure 6-28: (A) Amorphous Bi_2Te_3 seed layer. (B) High temperature Bi_2Te_3 deposition over the seed layer.

Seed layers investigated include a 100 nm thick metal Bi layer and a 300 nm amorphous Bi_2Te_3 layer deposited with low substrate temperatures. However, it was found that high temperature deposition over this seed layer consumed both these seed layers, creating even greater voids

between the columnar grains. The consumption of this seed layer and subsequent creation of voids where films existed implies the diffusion lengths of Bi and Te are greater than 100 nm at 260°C. Furthermore, amorphous Bi_2Te_3 is not temperature stable.

Substrate Material and Topology

The substrate material was not found to significantly impact Bi_2Te_3 film morphology. Notably, the width of the Bi_2Te_3 columnar grains did not vary. However, scalloping from DRIE on single crystalline silicon (SCS) surfaces reduced the density of the Bi_2Te_3 grains. On this sidewall, Bi_2Te_3 grains grew preferentially along the bottom of the scallops, as the bottom surface is angled towards the Bi and Te sources. This causes the grains to grow with a regular period determined by the period of the scallops. This effect persists on oxidized silicon if the scallops remain.

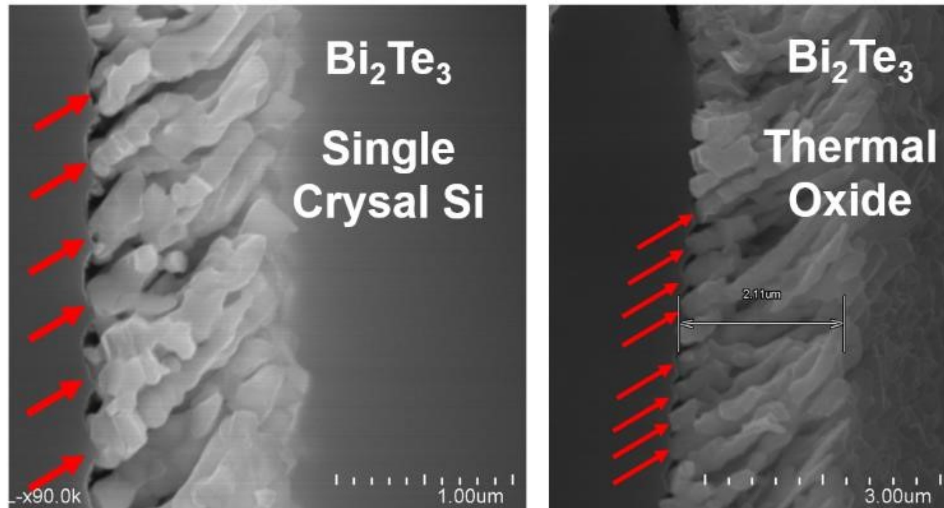


Figure 6-29: Preferential growth of Bi_2Te_3 on the bottom surface of the scallops.

An extreme example of this period can be seen on high temperature Bi_2Te_3 deposited on a low temperature, amorphous Bi_2Te_3 seed layer, as was the case in (fig. 6-27 B). There, the regularity of the resulting Bi_2Te_3 nano-rods becomes immediately apparent.

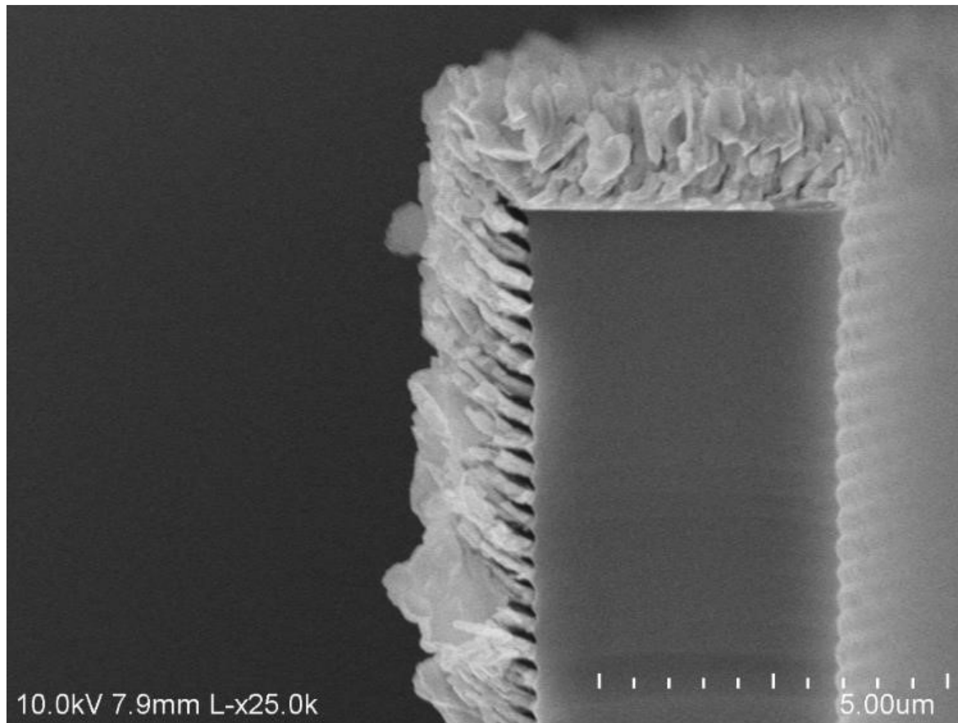


Figure 6-30: Regular growth of Bi_2Te_3 rods on oxidized Silicon.

It was also found that this columnar growth was independent of the substrate for Bi_2Te_3. Depositions on single crystal silicon, polyimide, fused silica, and oxide substrates yielded the same crystal structure. However, differences were seen for Sb_2Te_3 grown over the same substrates.

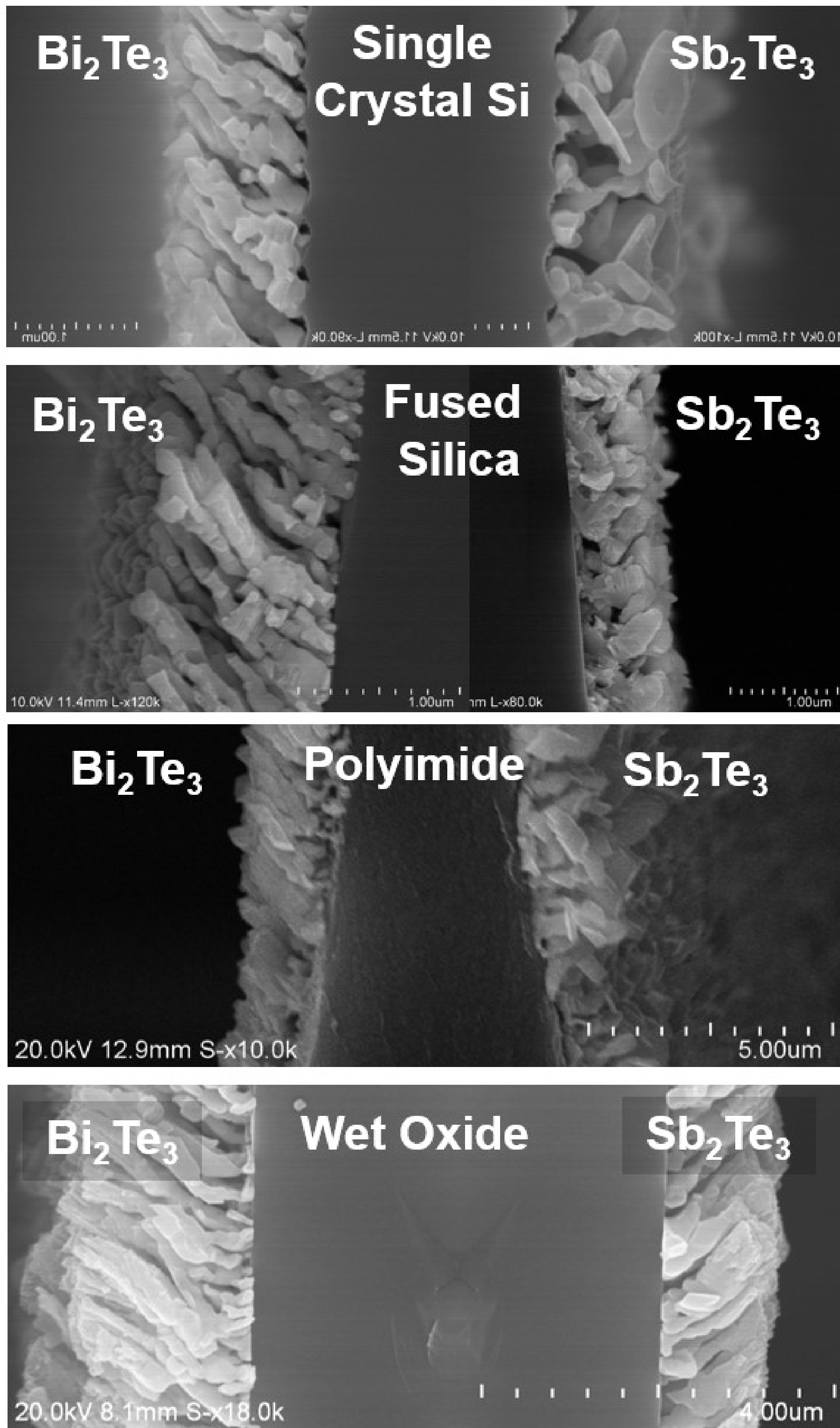


Figure 6-31: Sidewall film growth on different substrates at 260 °C.

Non-Stoichiometric Bi_2Te_3

Bi rich Bi_2Te_3 did not have the same discontinuity issues as stoichiometric Bi_2Te_3 growth on sidewall surfaces, creating a dense and continuous film surface.

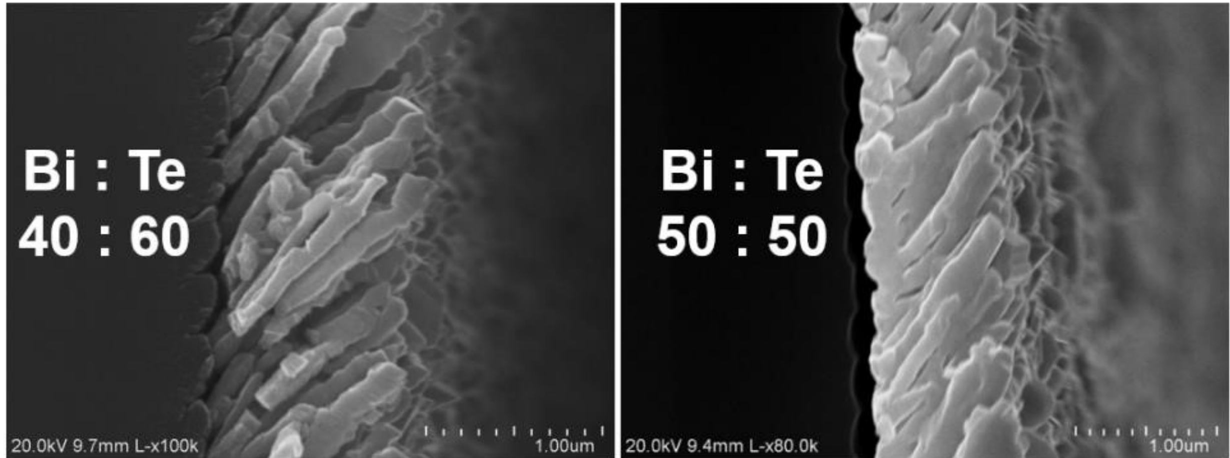


Figure 6-32: Stochiometric and Bi rich Bi_2Te_3 films deposited on oxide.

However, a film composition of 1:1 Bi:Te was needed to produce the void free film. At such a film composition, planar, Bi rich Bi_2Te_3 has a far inferior power factor compared to stochiometric Bi_2Te_3. It is believed that vertical, Bi-rich films would exhibit the same performance degradation. Thus, this method was not pursued. However, results given in Table 6-4 suggests that depositing Te rich Sb_2Te_3 is a viable way to improve the performance of the P-type thermoelectric leg in our generator. This would require further improvements in the run to run variation of off-stoichiometric Sb_2Te_3.

Table 6-5: Power Factor of Stoichiometric and Bi-rich Bi_2Te_3

Orientation	Temperature (°C)	Bi:Te ratio	Resistivity (µΩ-m)	Seebeck (µV/K)	Power Factor (mW/K^{2}m)
Planar	250	40/60	25	-264	2.78
Planar	250	49/51	10.8	-68	0.91
				% Difference	-67%

Dual Temperature Films and Backfilling

To reduce the voids on sidewall films, a low temperature amorphous film was deposited over a high temperature Bi_2Te_3 film. It was hoped that this amorphous layer would backfill the voids present in the high temperature film. Crystal quality would then be recovered through a high temperature anneal.

This process was first tested on planar surfaces where film properties could be easily measured. For planar films, this low temperature crystalline layer had relatively low Seebeck value of -125 μV/K but increased carrier concentration compared to high temperature films. Given the results, a thin, 0.3-μm layer of low temperature film over high temperature sidewall film was not expected to significantly degrade the Seebeck coefficient of the composite film.

This two temperature deposition process was utilized for the 2nd round of μTEGs with oxide scaffolds. It resulted in a significant decrease of almost 50% in the resistance of the device compared to 1st round oxide μTEGs, which utilized a single, high temperature film. The results of this are further detailed in Chapter 8.3.

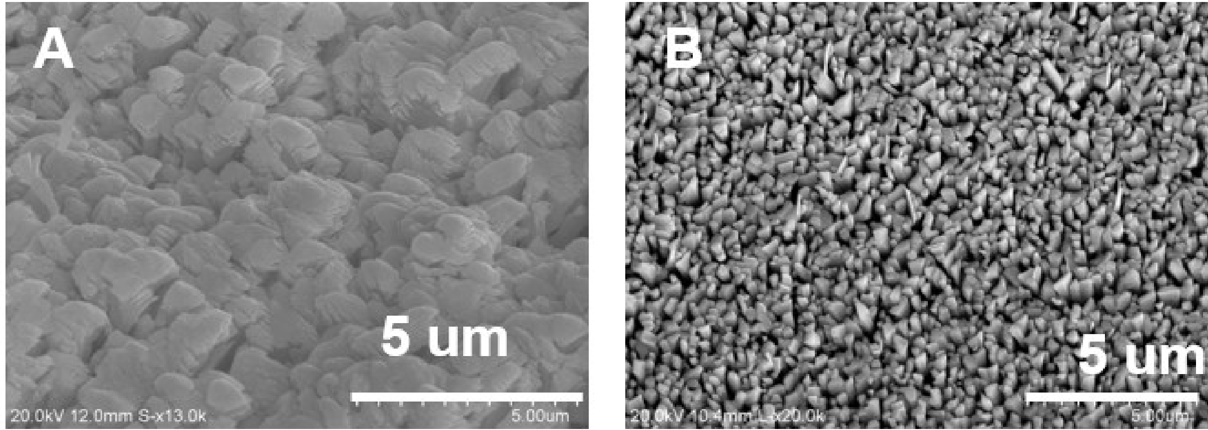


Figure 6-33: (A) Backfilled 280 C films with .5 µm of 100 C film. (B) 280 C Bi_2Te_3 film on vertical surface. Deposition parameters and the composition of the two films are given below in table 6-6.

Table 6-6: Deposition and composition of two temperature film in Fig. 6-34.

Film	Temperature (°C)	Bi Dep. Rate	Te Dep. Rate	Bi:Te ratio
1st layer	250	2 Å/s	3 Å/s	43.3/56.7
2nd layer	250	2 Å/s	3 Å/s	38.8/61.2

6.9 Angled Growth

The non-perpendicular growth angle of Bi_2Te_3 and Sb_2Te_3 grains indicate that the C-axis of the crystals are not orthogonal to the vertical surface. This means that the film properties of the thermoelectric films are a combination of the in-plane and cross-plane properties. As in-plane properties of Bi_2Te_3 and Sb_2Te_3 are significantly superior [49],[46] to cross-plane properties, potential solutions to this issue were investigated.

Temperature

Originally, the cause of the angled growth was though simple due to the angle of the Bi and Te sources relative to the substrate surface. However, this growth angle was found to be temperature

dependent, indicating another cause. Higher temperatures caused an increase in the angle of the film growth relative to the perpendicular of the sidewall surface. This growth is always pointed away from the bottom substrate surface. At a deposition temperature of 260°C, Bi_2Te_3 crystals grow 30 degrees away from the wafer vertical. At 90°C, crystals are arranged at 60 degrees. Additionally, the initial "seed" layer appears to be at 90 degrees, (Fig 6-15 C/D, Fig. 6-32) matching the expected C-oriented nucleation sites [47]

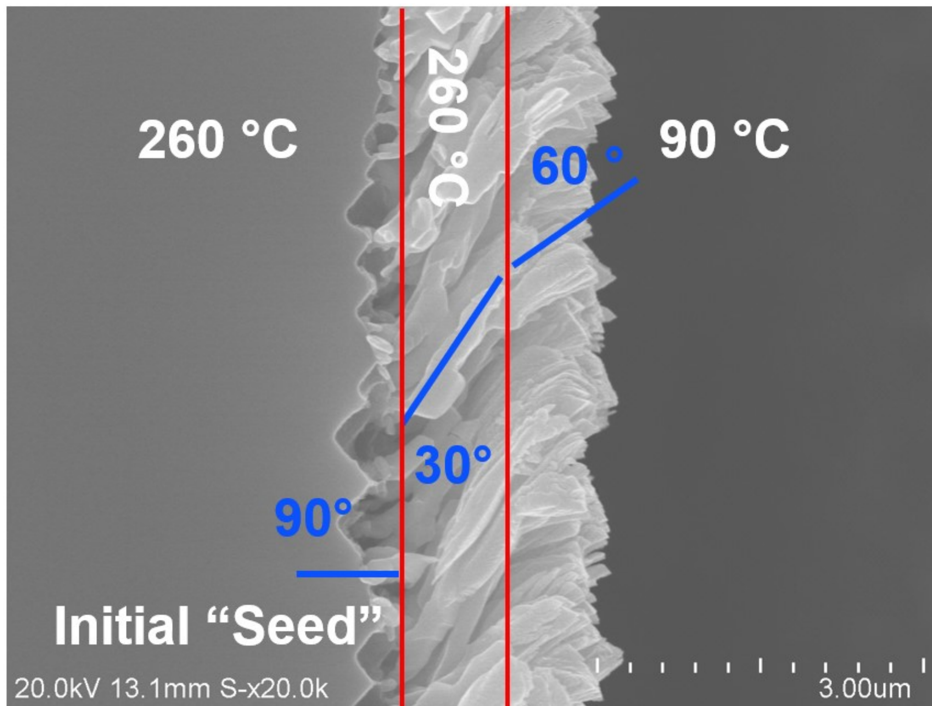


Figure 6-34: Growth angle of Bi_2Te_3 crystals at 260°C and 90 °C. The initial "seed" layer roughly 300 nm thick is oriented at 90° compared to the "bulk" 260°C deposition at 30° and the 90°C deposition at 60°C.

Given this information, low temperature film deposition can provide a path towards improved sidewall film performance. Bi_2Te_3 and Sb_2Te_3 films deposited below 120°C do not show the discontinuities of high temperature films (Fig. 6-37). Additionally, they exhibit a much less severe growth angle. While low temperature depositions have lower intrinsic film properties, it may be possible to recover film performance through annealing.

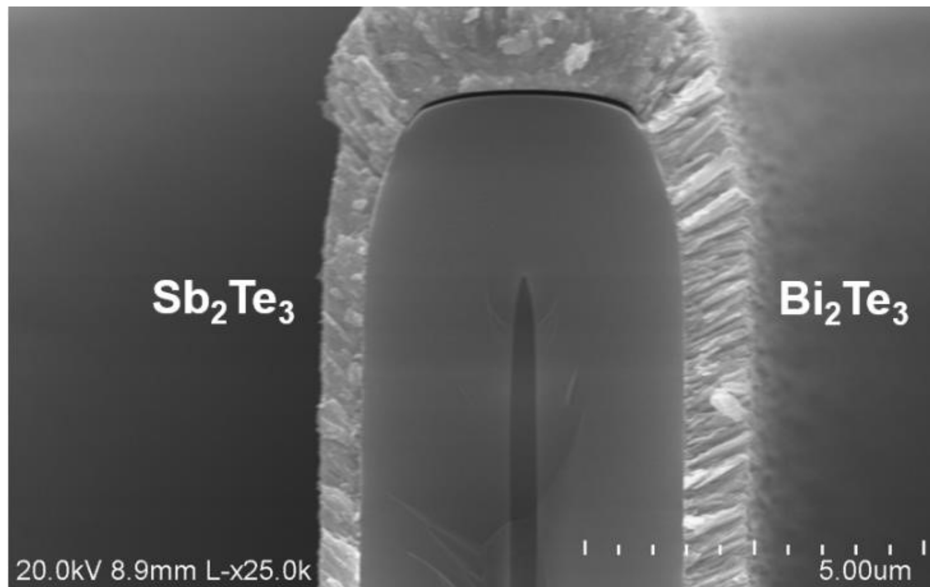


Figure 6-35: Bi_2Te_3 and Sb_2Te_3 deposited at 120°C over oxide

Tellurium Re-evaporation

Given the temperature dependent effects and the initial perpendicular growth layer, it was suspected that tellurium re-evaporation from the bottom substrate surface, as well as along the sidewalls, was causing the angled growth. Tellurium re-evaporation occurs in this process due to the extremely rich Te deposition conditions. Significant amounts of this Te re-deposits from the bottom surface onto the sidewalls, as evidenced by the need for an increased Bi deposition rate going from planar to vertical films. To test this theory, Bi_2Te_3 and Sb_2Te_3 were deposited oxide pillars with a narrow and a wide pitch. The closely spaced pillars prevented film deposition on the bottom surface and resulting in a growth angle of 60 ° from the vertical. The widely spaced pillars allowed significant film deposition on the bottom surfaces and resulted in a more acute angle from the vertical, at 30°C. This agrees with the theory that tellurium re-evaporation is a contributing factor to the growth angle deviation.

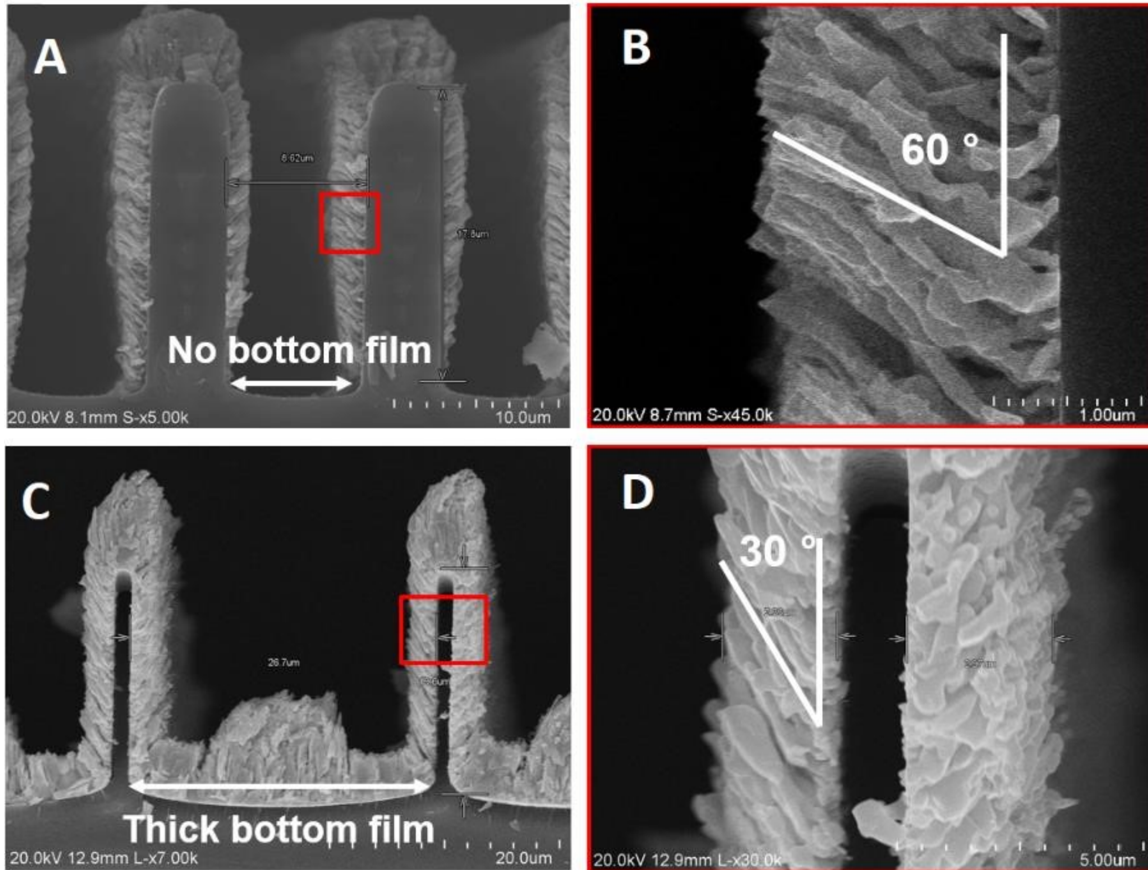


Figure 6-36: Bi_2Te_3 deposition at 260°C on oxide. (Top) 60° angled growth with no bottom film deposited due to the narrow spacing of the pillars. (Bottom) 30 °C angled growth with widely spaced pillars and film deposition on the bottom surface.

These results also indicate that the film properties measured with the test structure given in 6.6 may be further off from the actual performance of the films. The test structure is only capable of measuring lateral film properties. Given the vertical directionality of the films, lateral and vertical properties may differ. Furthermore, due to the close spacing of the Seebeck test structure, the angle of film growth also differs from the films integrated into μTEGs.

6.10 Conclusion

The power factors of co-evaporated Bi_2Te_3 deposited over vertical surfaces are significantly lower than that of planar films. Vertical Sb_2Te_3 however, demonstrates similar power factors to

its planar counterpart if an off stoichiometric deposition method is used. Even with the decreased film performance, the High-Aspect μTEG design is still expected to produce generators with high figure of merits above 30 $\mu W/cm^2/K^2$. However, the large performance discrepancy between vertical and planar TE films developed here indicate large gains in the performance of the High-Aspect μTEG design can be achieved through continued film research. Additionally, decreasing the pitch of the scaffolds improves film angle and may correspond to increases in film performance. This has the added benefit of increasing the fill factor of the designed generators. The High-Aspect μTEGs presented here do not utilize this approach as the pitch of the scaffolds is currently limited by the bond alignment tolerance. Another promising approach is the creation alternating layers of high temperature and low temperature films, as a kind of temperature based "superlattice". The incorporation of a low temperature amorphous film layer over a high temperature one has been shown to significantly decrease the resistance of the resulting μTEG.

Chapter 7 Characterization of Key Steps for μTEG Fabrication

This chapter provides an overview of the major fabrication steps necessary for the integration of the high-aspect, vertical thermocouples structure into a μTEG device. Detailed below are fabrication steps needed for the creation of high-aspect pillars, patterning of Bi_2Te_3 and Sb_2Te_3 films, die attachment, and fabrication considerations. Fabrication details and challenges specific to a given generator design detailed separately in Chapter 8. One of the major fabrication challenges is the prevention of damage to the Bi_2Te_3 and Sb_2Te_3 film after deposition. These films are sensitive to oxidation and common clean room solvents. A solvent free shadow masking process was developed to overcome this difficulty and detailed here.

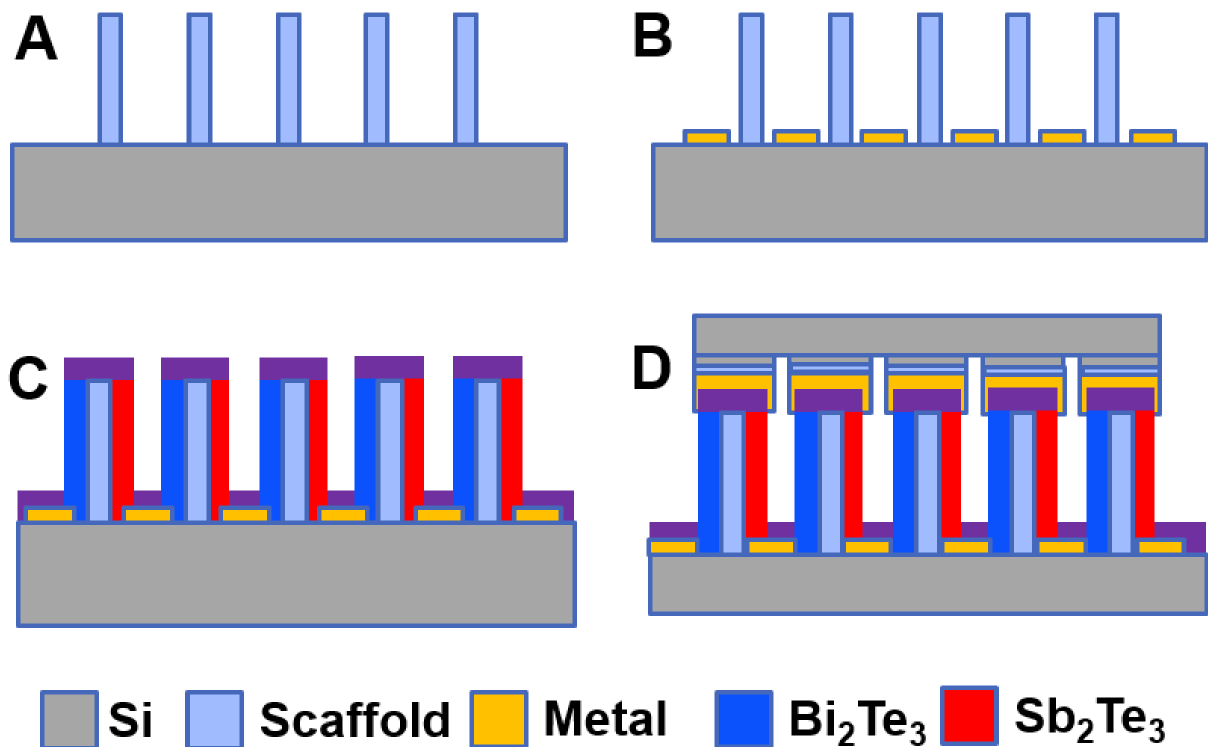


Figure 7-1: Generalized process steps for High Aspect µTEG fabrication.

The basic fabrication steps for the High Aspect µTEG are: (A) formation of dense, high aspect scaffolds, (B) deposition of Au onto the bottom surfaces to reduce contact resistance, (C) deposition of Bi_2Te_3 and Sb_2Te_3 onto the sidewalls of the scaffolds, and (D) bond metal patterning and die attachment.

7.1 High-Aspect Scaffolds

The requirements for the scaffolds are: they must be least 25-µm tall, thermally resistive, electrically isolating. Most importantly, they must be compatible with Bi_2Te_3 and Sb_2Te_3 film growth. As any heat path through the scaffold lowers the power output and efficiency of the µTEG, it is desirable to keep the scaffolds as narrow as possible. For Bi_2Te_3 and Sb_2Te_3 films 2-µm thick, scaffold widths below 2-µm for oxide and 6-µm for polyimide keeps the thermal conduction of the scaffold to below 20% of that of the thermoelectric. The two materials chosen

for this scaffold were oxide and polyimide. As detailed in Chapter 5.5 N-Bi_2Te_3 and P-Sb_2Te_3 thermoelectric films with power factors over 2.8 and .9 mW/K^2m were successfully grown over these substrates [Table 5-11].

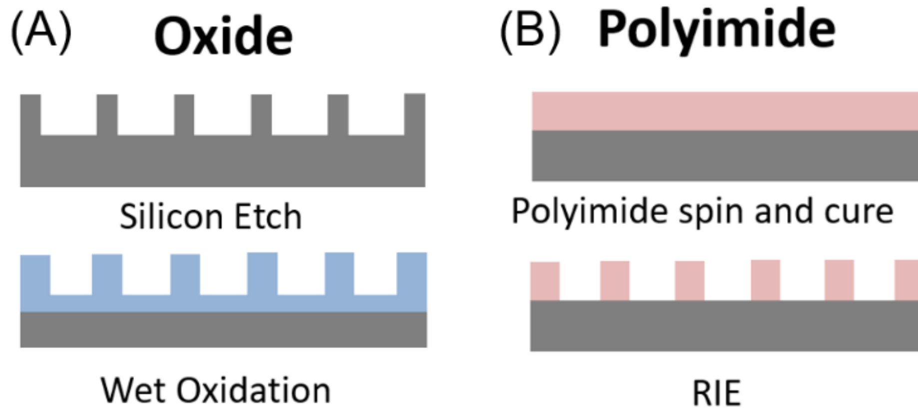


Figure 7-2: Abbreviated steps for scaffold creation.

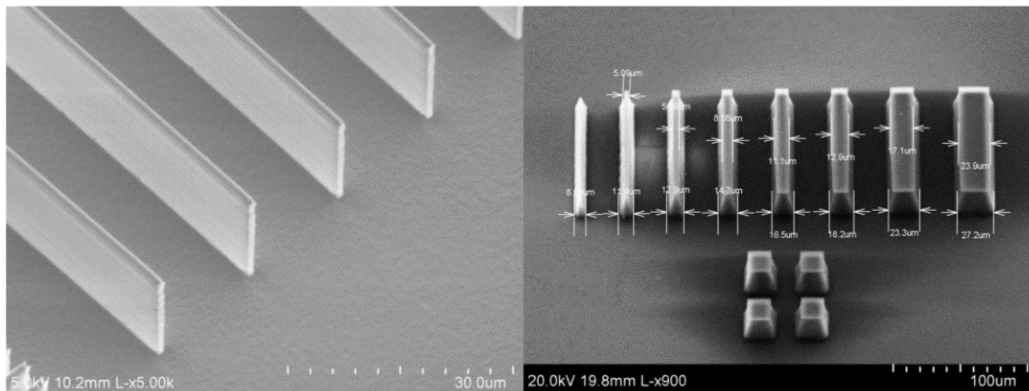


Figure 7-3 (A)Oxide scaffolding (B) Polyimide Scaffolding

Oxide Scaffolds

To create oxide scaffolding, silicon pillars are first etched via DRIE (Fig. 7-1) then partially oxidized through wet oxidation. To create smooth sidewalls surfaces free of scalloping, this oxide is then stripped, and the remaining silicon is oxidized again. Repetition of the oxidation

and strip steps also allows a greater initial thickness of the silicon pillars, which improved thickness uniformity of the resulting oxide scaffold. This was due to lithography limitations, where thinner, 2 – 3 µm drawn features were difficult to pattern with the selected photoresist, SPR 220, 3.0. However, the oxidation process introduces a layer of insulating oxide below the scaffolds that degrade performance.

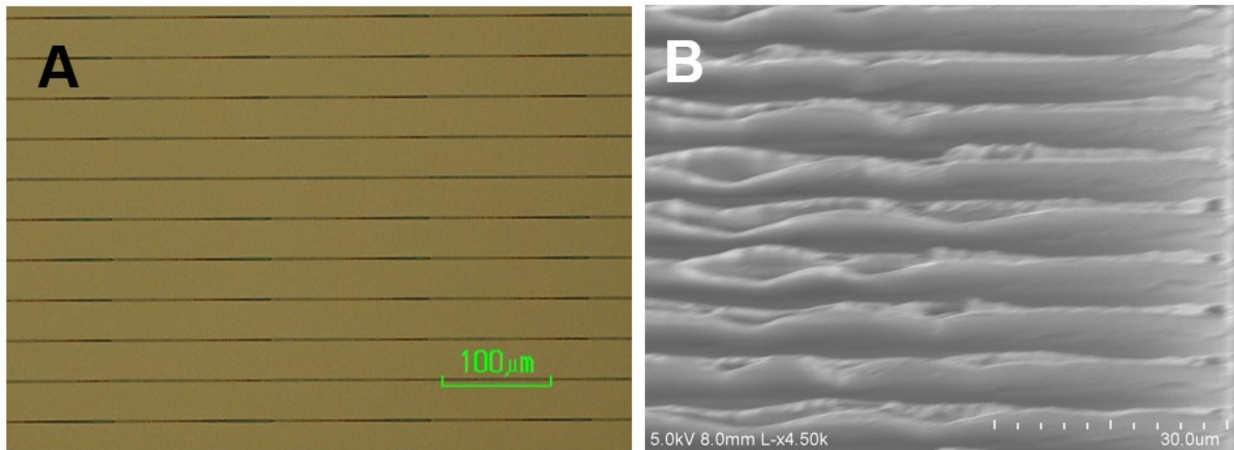


Figure 7-4: (A) Patterned photoresist mask for DRIE of Si pillars. Inconsistent spacing due to resolution limits from the mask are visible. (B) Oxidation of poorly defined Si pillars.

Polyimide Scaffolds

In comparison to oxide, polyimide allows wider scaffolds due to its lower thermal conductivity of 0.2 W/m•K compared to the 1.3 W/m•K of oxide. The wider scaffolding allows a larger contact area above the pillar for the connection of the N & P films at the cost of lower TE leg density. Due to the current unique composite BiSbTe junction forming our contacts, this increase in contact area did not reduce the electrical resistance of fabricated devices. Details are given later in chapter 8.

The spin-on polyimide used for our process is HD 4110 from HD Microsystem. HD 4410 is a negative-tone polyimide precursor capable of thickness up to 20-µm in a single coat. While HD

4410 is photo patternable, the desired aspect ratio of 5-µm wide and 25-µm tall (after cure) could not be achieved through photopatterning.

Table 7-1: Minimum feature size of HD 4410 vs. Exposure time for 50 thick (before cure) coats.

Exposure Time	15 sec.	25 sec.	60 sec.	120 sec.	180 sec.
I-line dose mJ/cm^2	150	250	600	1200	1800
H-line dose mJ/cm^2	300	500	1200	2400	3600
Result	No polyimide remains after dev.	Very shallow patterns	Rough edges, shallow pattern	15 µm min. feature size	15 µm min. feature size

Thus, an anisotropic RIE etch capable was developed for patterning. After spinning, the polyimide is cured at 400°C in a nitrogen environment for one hour. The cured polyimide is patterned through RIE using a gas mixture of 80% O_2 with 20% CF_4. This recipe was based on a reported recipe by Turban [68] where oxygen and fluorine were the main two reactive species. A 1000 Å thick evaporated Al layer is used as the masking material. The addition of the fluorine source both increases the etch speed and reduces pitting (Fig. 22).

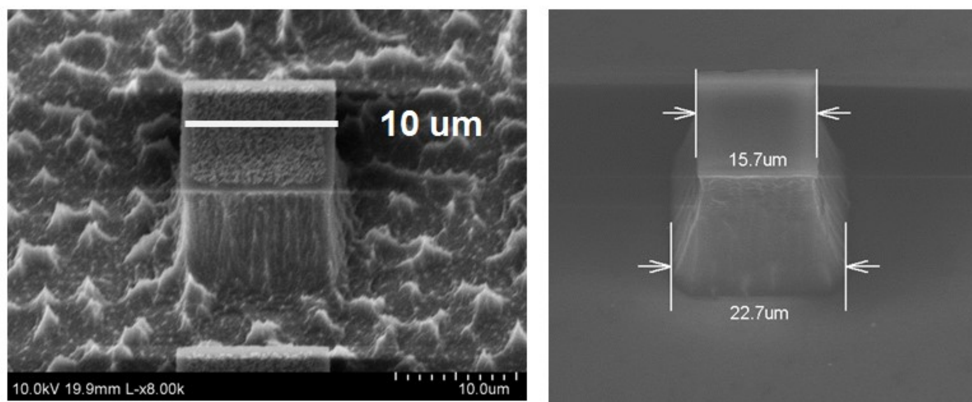


Figure 7-5 (A) O_2 only RIE of polyimide (B) Polyimide RIE with O_2 and CF_4

Table 7-2: Polyimide RIE Parameters

	$O_2 + CF_4$	O_2 Only
Etch rate	**0.59 µm/min**	**0.25 µm/min**
Composition	80/20 O_2/CF_4	O_2 only
Power	200 W	200 W
Mask	Al	Al
Al Selectivity	> 300:1	> 300:1
Oxide etch rate	0.1 µm/min	0.1 µm/min
Open Area	60 cm^2	60 cm^2

The developed etch was carried out in a LAM 9400, a transformer coupled plasma etching tool, the LAM 9400. The etch had a tapered sidewall angle of 75° with a concave feature directly below the surface. This feature was caused by the undercut of the Al hard mask used for patterning. For a 20-µm polyimide etch, a drawn feature of 6-µm had a width of 3-µm at the top increasing to 8-µm at the base.

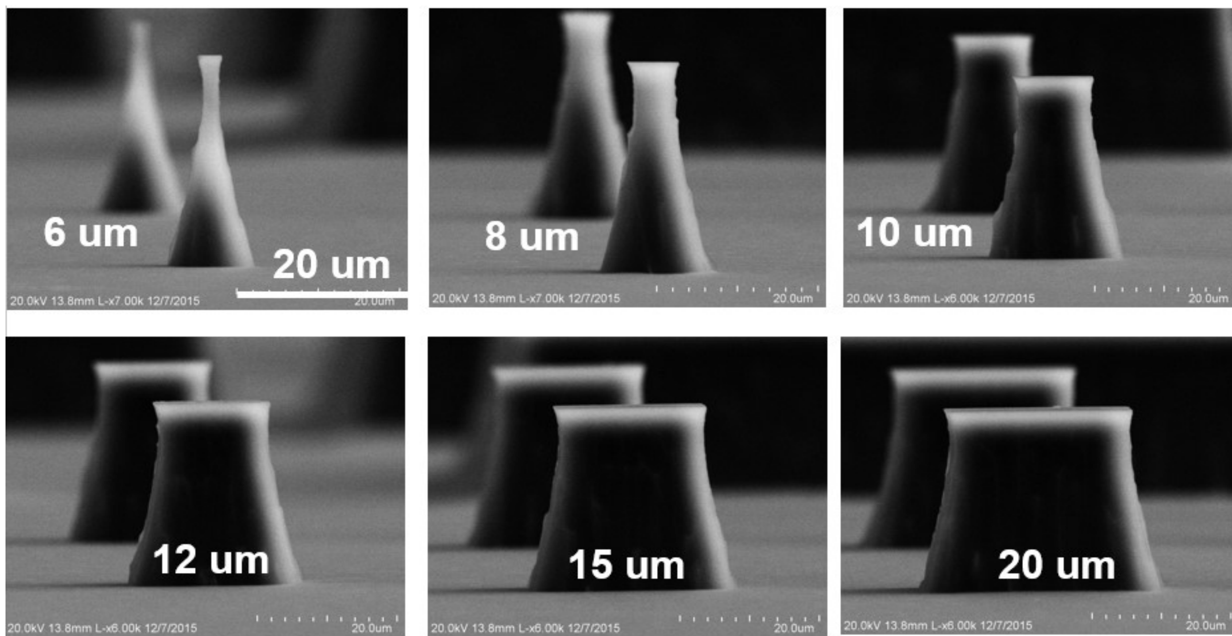


Figure 7-6: Side profile of developed polyimide dry etch. Widths given are drawn dimensions.

The concave feature caused shadowing during TE film deposition, leading to a discontinuity in the TE film. This gap was eliminated through the use of a 10 minute, isotropic oxygen plasma etch after the removal of the Al hard mask.

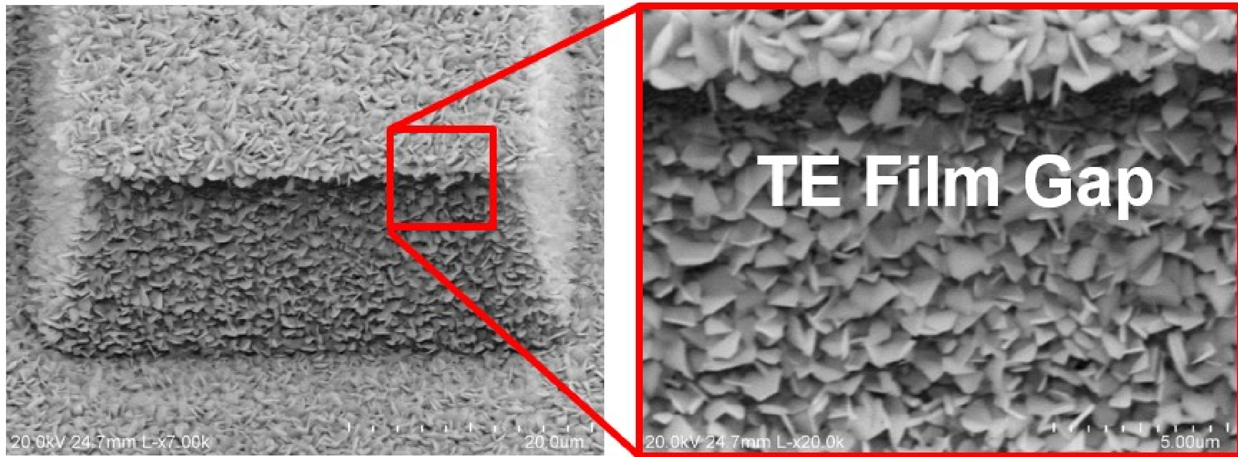


Figure 7-7: TE Film gap due to concave polyimide etch profile.

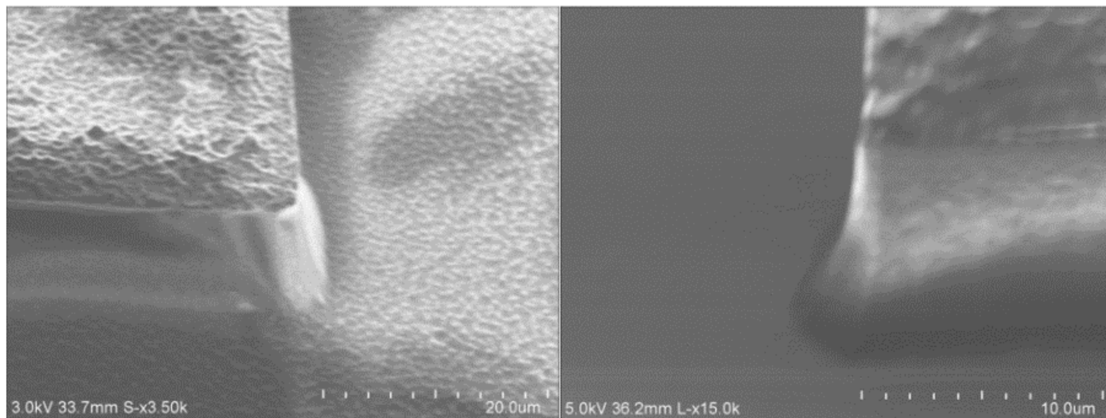


Figure 7-8 (A) Polyimide profile after RIE but before smoothing and (B) polyimide profile after smoothing.

7.2 Metal Patterning

Au deposition in the valleys between the pillars is desired to reduce the electrical resistance of the Bi_2Te_3-BiSbTe-Sb_2Te_3 connection. This connection represents a significant part of the electrical resistance of the entire device. With 25-µm tall pillars space 25-µm apart, 1/3 of the

total electrical resistance of the device is located at this junction. To reduce this resistance, Au is deposited in this area before TE deposition.

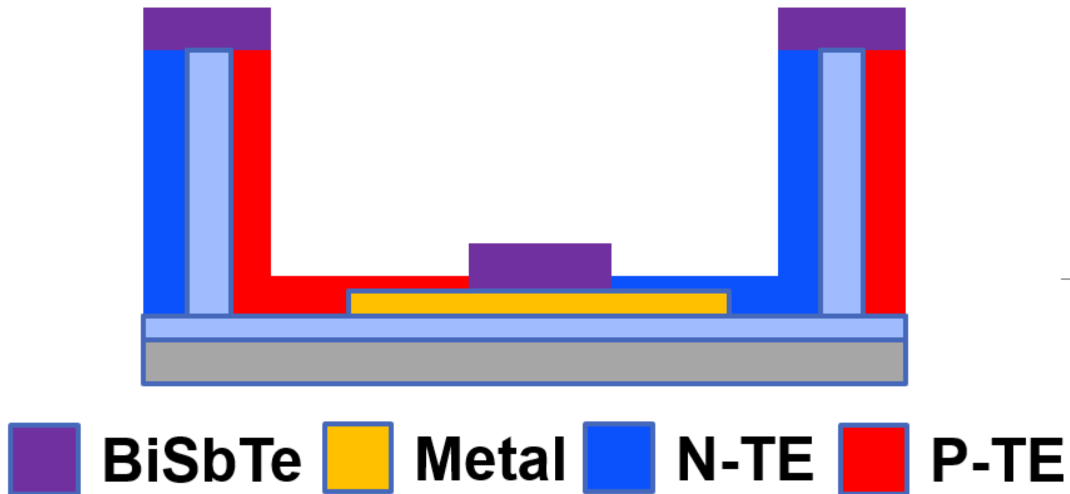


Figure 7-9: Diagram of Bi_2Te_3-BiSbTe-Sb_2Te_3 connection between pillars

In the High-Aspect μTEG, a single Au patterning step is used to create both the routing. For polyimide based generators, Au was simply deposited before polyimide was spun-on to the wafer and patterned. However, for oxide based generators, scaffold creation was a subtractive step, necessitating Au deposition and patterning after scaffold creation. This posed a challenge for as photoresist patterning in between the valleys of the scaffold was difficult due to the severe topology.

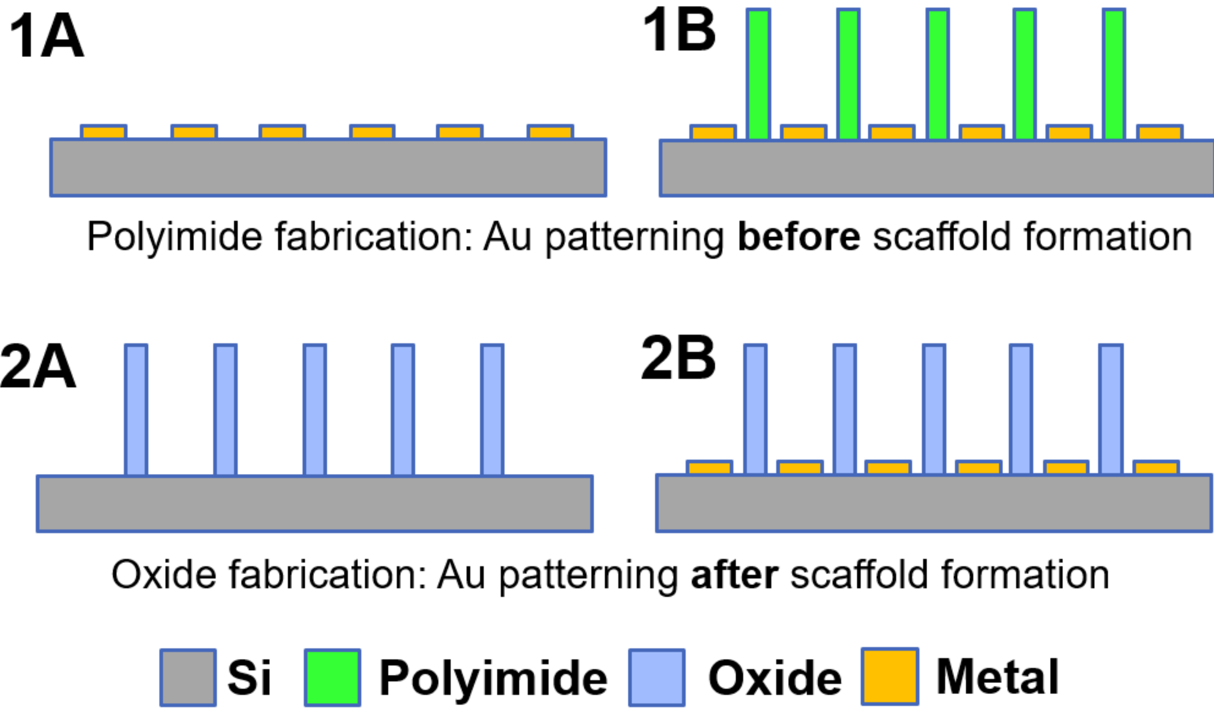


Figure 7-10: (A) Metal deposition in polyimide generators. (B) Metal deposition in oxide generators.

Due to excessive thickness, photoresist around the scaffolds could not be removed without multiple exposure and development cycles. With multiple cycles, the thin photoresist at the center of the valley would frequently be removed. This was caused by the diffraction of light effectively enlarging the clear areas on the mask.

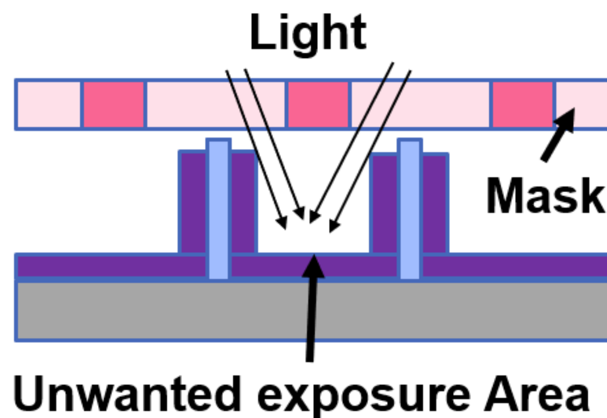


Figure 7-11: Space between mask and bottom surface of the wafer allows light through

The height of the scaffold created a significant gap between the mask and the bottom surface of the wafer, preventing close contact to eliminate this issue. The presence of Au on the sidewalls of the pillars prevented wet etching of any Au deposited there. This effectively shorted the subsequent thermoelectric films deposited on the pillars.

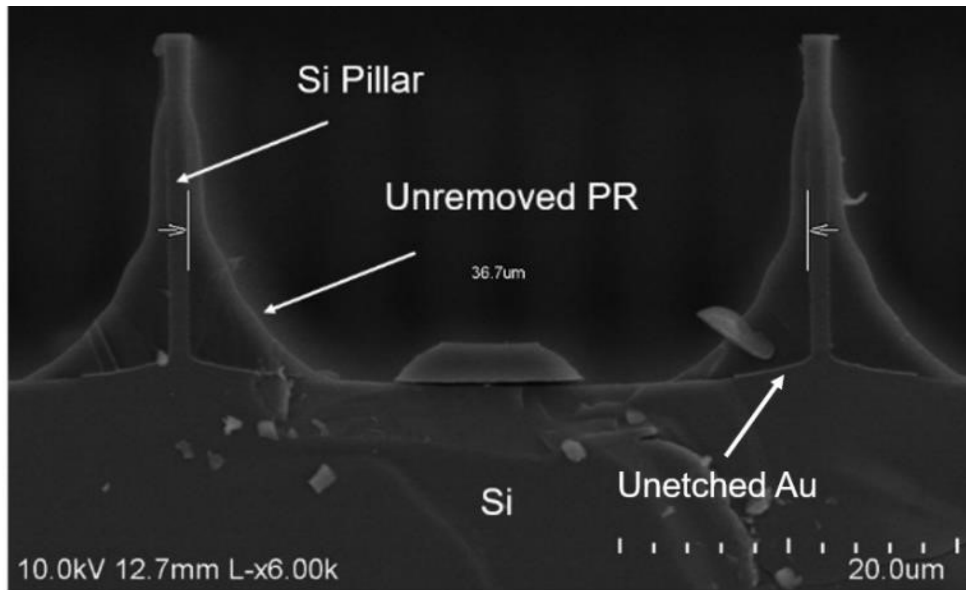


Figure 7-12: Photoresist patterning over high aspect oxide features.

To overcome this issue, latter Au patterning for oxide based μTEGs were accomplished using a shadow mask.

7.3 Shadow Masked Film Deposition

Patterning of co-evaporated Bi_2Te_3 and Sb_2Te_3 is difficult. The presence of tellurium in the film poses contamination issues for non-dedicated plasma etching systems. The high substrate temperature during deposition required for film quality is incompatible with most resists used in lift off techniques. Wet etching is possible using aqua regia [28],[69], or HNO_3[70] based chemistries but has large undercuts. Unique to our thermocouple geometry, photoresist step coverage was an additional concern. Due to the sensitivity of our deposited films to common

clean room solvents such as acetone (Fig. 5-3) and N-methyl-2-pyrrolidone (NMP), it was decided to forgo wet processing altogether and pattern Bi_2Te_3 strictly through shadow masks.

Minimum feature size, a common concern for shadow masks, was not an issue as the self-patterned nature of the deposition process meant that the shadow mask did not need to define individual thermocouples. Shadow masks were created from etched silicon wafers. Due to the angled nature of deposition, thick masks would block incoming material. Thus, a two-step DRIE process was used to created thinner masks (Fig. 7-12). First, the desired features were etched on a silicon substrate 75-µm deep. The wafer was then flipped and mounted feature side down onto a carrier wafer using Santovac, a viscous pump fluid that does not outgas. The mounting process was conducted under vacuum to avoid potential air pockets, which would expand during DRIE and cause mounting failure. After mounting the wafer is then etched from the backside to the desired thickness.

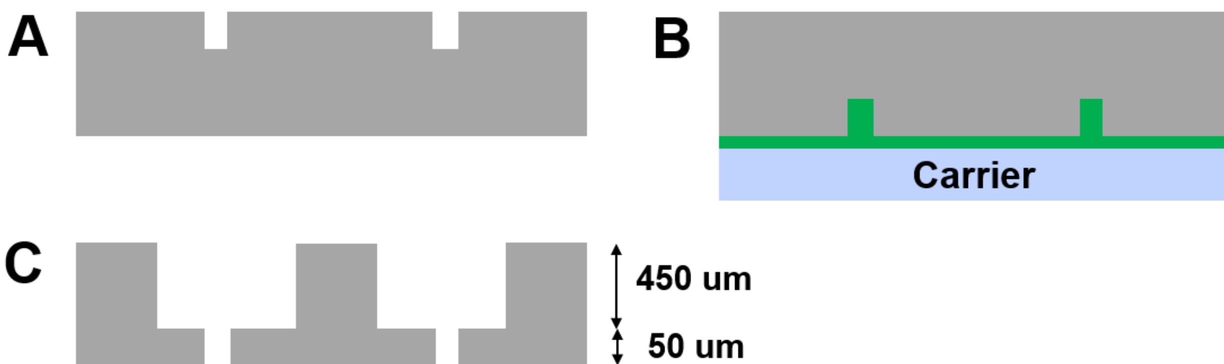


Figure 7-13: Two step DRIE process for shadow mask creation. (A) Front side DRIE of desired features. (B) Mount to carrier wafer for backside DRIE. (C) Backside thinning DRIE and removal from carrier. Thick Si is left for mechanical support.

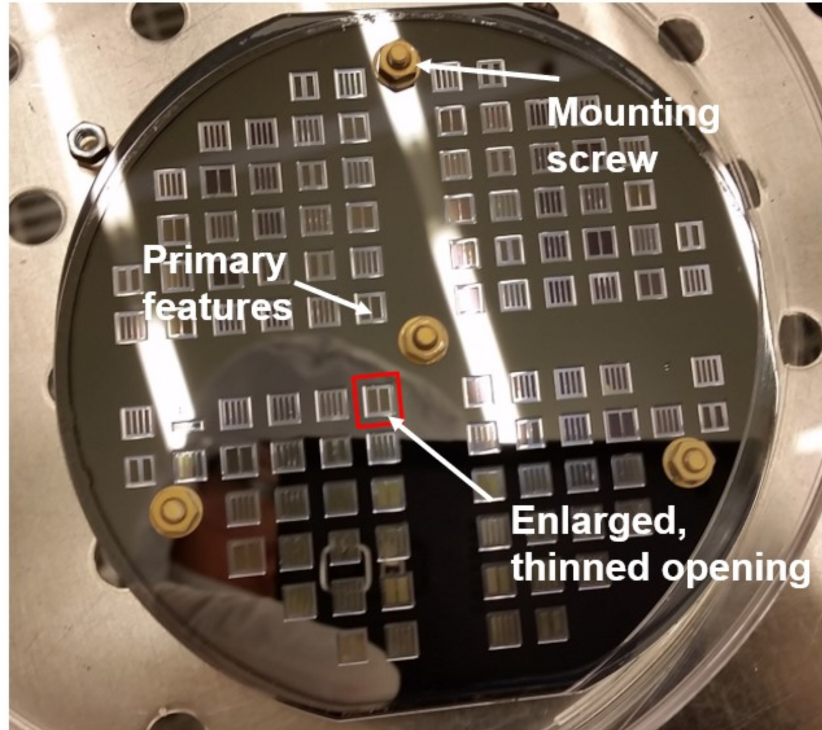


Figure 7-14: Fabricated shadow masked with mounting screws.

Shadow mask attachment was accomplished through the use of mounting holes 3.05 mm in diameter etched on the shadow mask and the receiving wafer. Stainless steel screws in diameter 3.0 mm were then used to affix the wafers together along with hex nuts and washers.

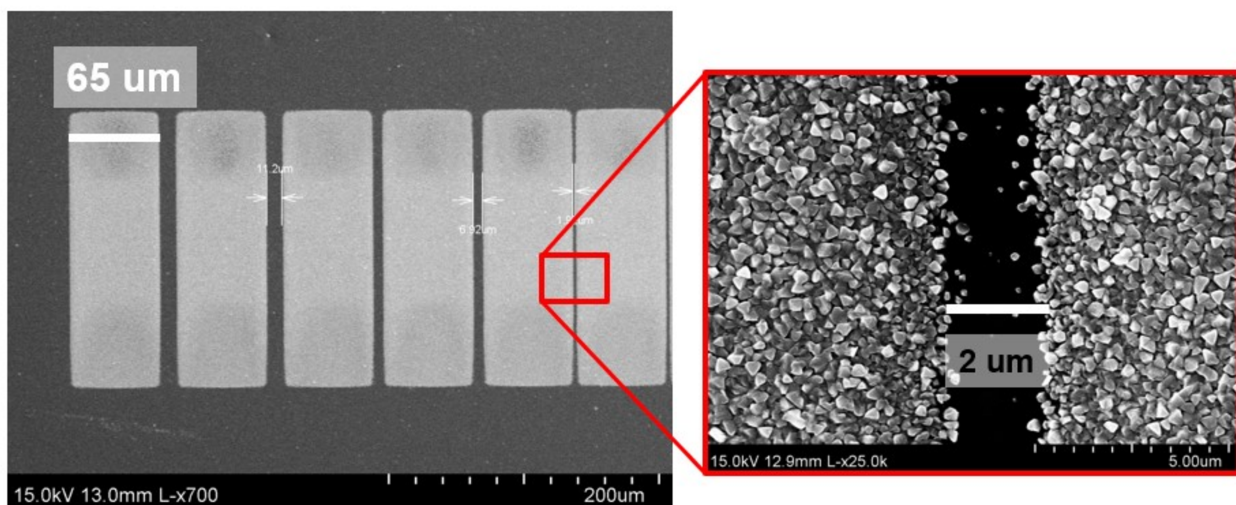


Figure 7-15: Bi_2Te_3 patterned through shadow masks.

Alignment was done by hand under an optical microscope. Misalignment typically was less than 5-µm before deposition. After deposition with a heated substrate, misalignment would increase by an additional 5-µm, to 10-µm in total. Unheated depositions did not see an increase in misalignment during the deposition process.

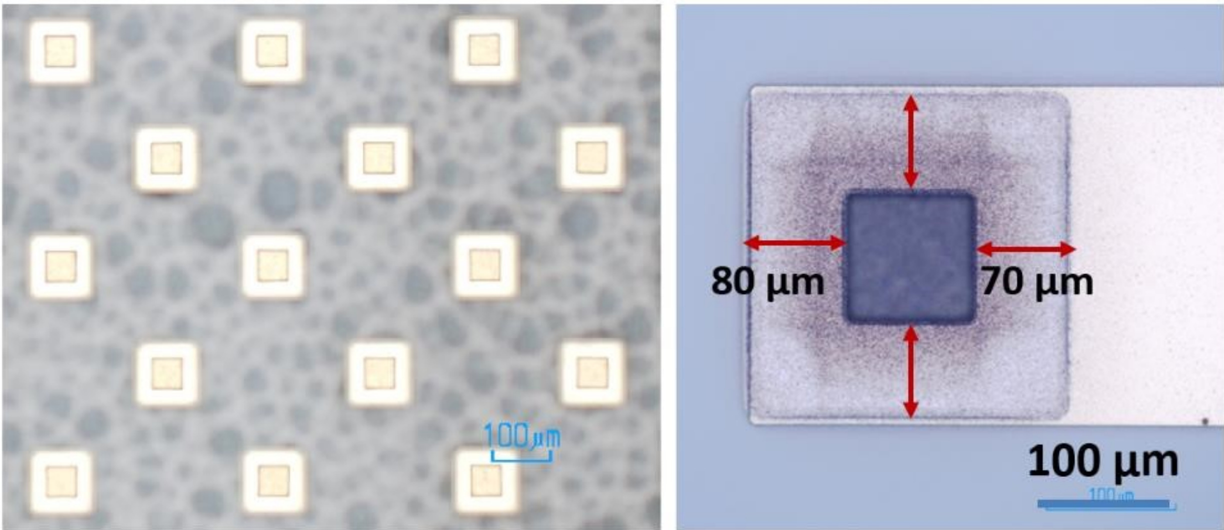


Figure 7-16: (Left) Aligned shadow mask opening with polyimide (yellow) squares. (Right) TE deposition at 250°C through an aligned shadow mask.

7.4 Die Attachment

The complete µTEG requires the attachment of a topside heat spreader. In typical µTEG designs, N and P-type thermoelectric legs are fabricated on separate wafers [15],[12],[1] and bonded together. This method means that the bond metal stack also serves as the electrical connection between the wafers. This restricts the bond metal choices to those that form low resistance contacts to the underlying TE films, or the use of thick diffusion barriers. Au and Ni (Fig. 3-6) were measured to have the lowest contact resistivity to Bi_2Te_3 at 3E-09 and 4E-09 Ω-m^2, respectively. Additionally, if all TE elements are connected in series, this process requires 100% bond yield of the individual TE legs.

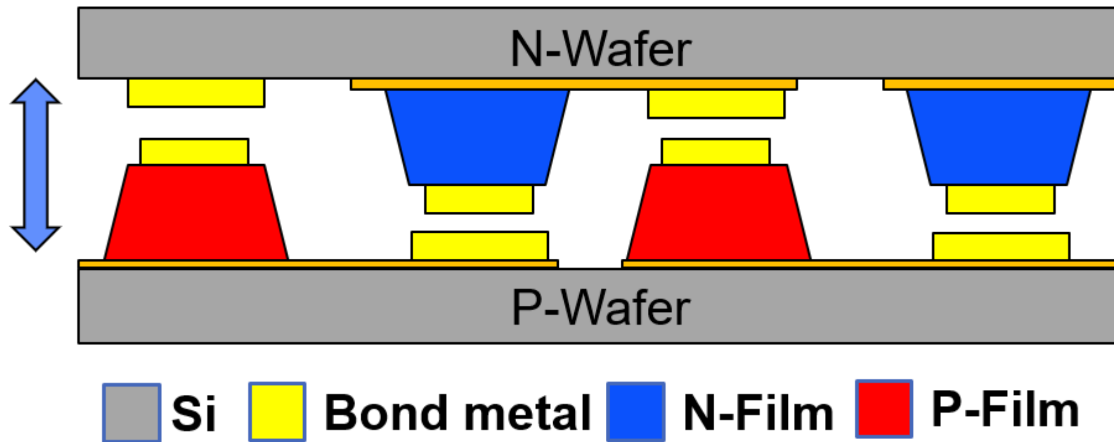


Figure 7-17: Bonding of a µTEG with separate N-type and P-type material wafers. Electrical connection is routing through the bond metal.

In contrast, for the presented high-aspect µTEG design, electrical connection is complete on a single wafer. Thus, the primary purpose of die attachment is only to form the thermal connections of the µTEG device. While Au is used as the bonding metal, no decrease in device resistance was seen after bonding due to oxidation of the films during bonding in atmosphere. In fact, device resistance increased due to oxidation of the Bi_2Te_3 and Sb_2Te_3 at the elevated bonding temperatures.

Two bonding processes were considered. A more traditional approach, pictured above, used eutectic bonding for attachment to the top Si cap. This method allows the formation of soft, deformable metal during the bonding process. Au-Sn eutectic was chosen due to its high thermal conductivity of 57 W/mK and low eutectic temperature of 278° C [74]. When aligned and pressed against the TE pillars, the 4-µm thick Au/Sn stack conforms to the shape of the TE pillars, establishing good thermal contact without unwanted wetting of additional surfaces.

A 100-µm thick bond ring offset from the active thermoelectric legs was fabricated for secure attachment. For silicon oxide, this bond ring was composed of closely space oxide pillars, rather than a solid oxide mass to reduce thermal conduction through the ring.

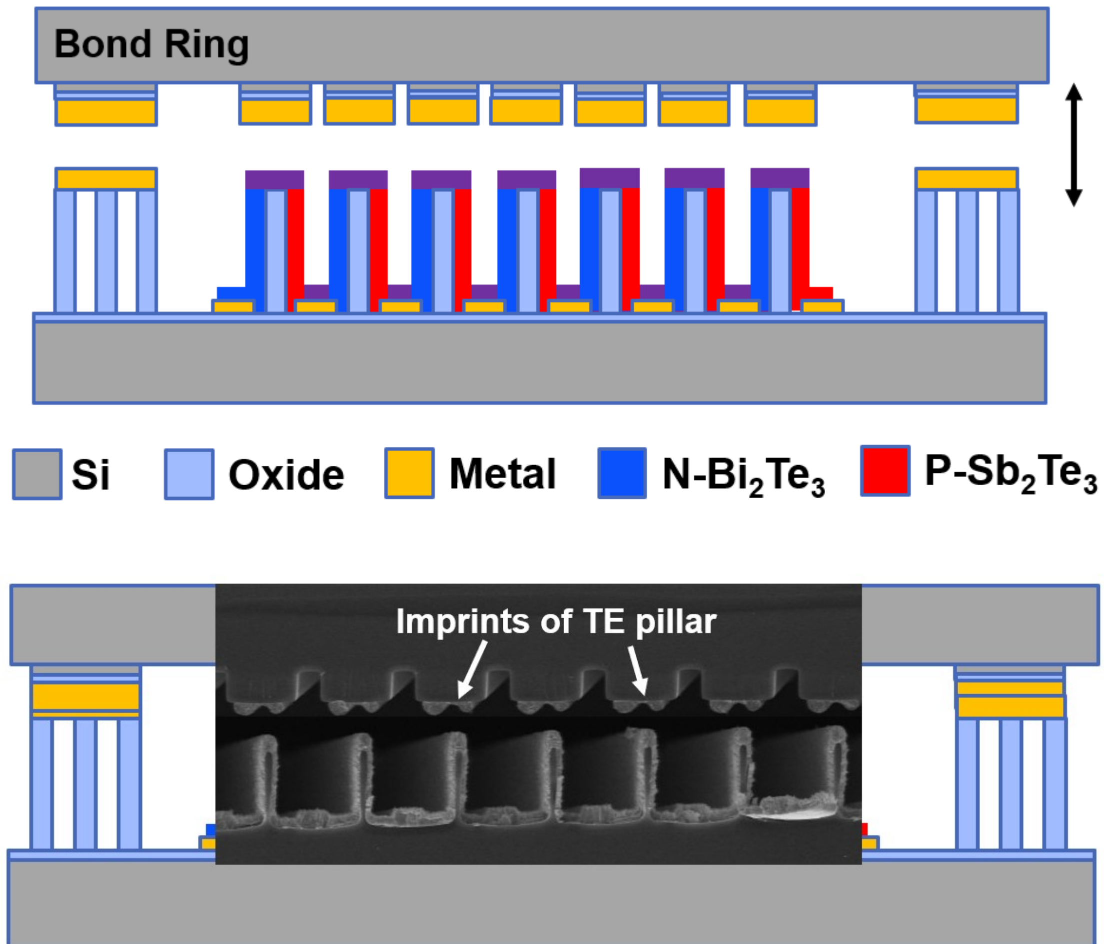


Figure 7-18: (Top) Diagram of µTEG pre-bond. (Bottom) Composite SEM of µTEGs legs bonded to a top cap and later separated. Imprints of pillar on the top side Au/Sn eutectic are clearly visible.

Bonding was conducted on a flip chip bonder from Finetech. During bonding, the assembly was heated to 300°C, slightly above the Au-Sn eutectic temperature, and held for 5 minutes under 4 N of pressure. Due to tool limitations, the bonding process was conducted in atmosphere. To

compensate, forming gas, a standard method of oxide removal, was blown across the bond area throughout the entirety of the bonding process.

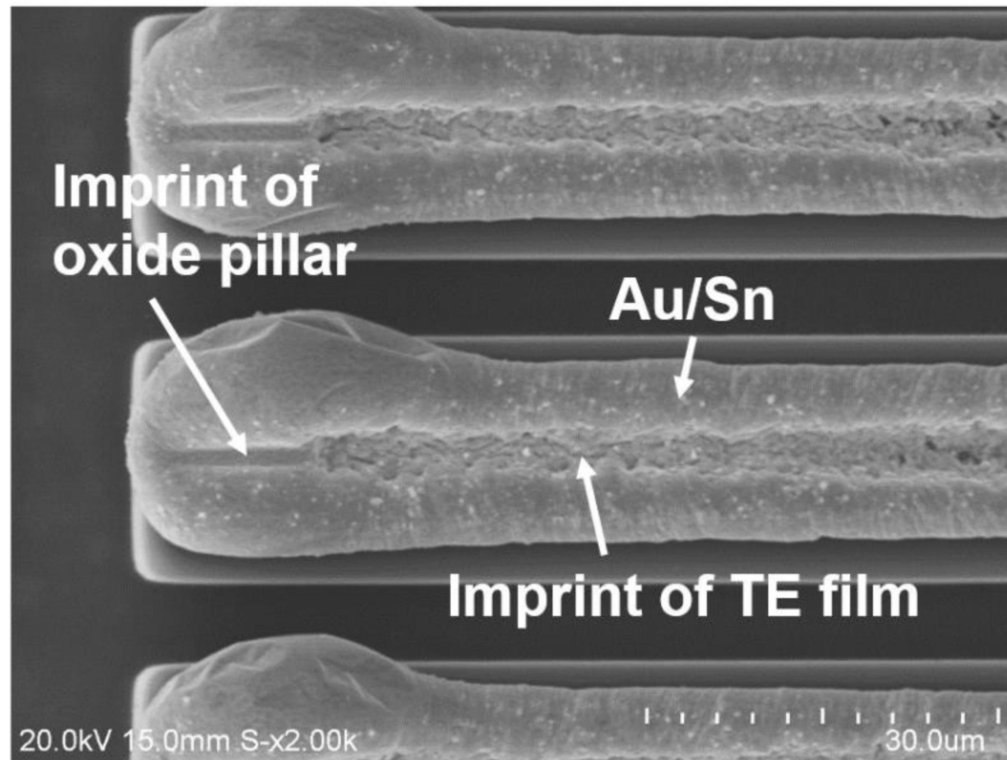


Figure 7-19: Imprint of TE pillars onto the Au/Sn eutectic.

Solder Oxidation

Bonding in atmosphere results is an oxide passivation layer covering the device. This passivation can prevent bonds from forming. Due to a lack of an effective enclosure for the bonding tool, forming gas did not entirely resolve the issue. Scrubbing [37], an industry standard of oxide removal and heating through mechanical motion could not be used due to the brittleness of the TE films. To resolve this issue, Au/Sn bond sites were created as small, individual squares. When pressed during bonding, fresh, unoxidized material squeezes out on the periphery of the squares, allowing a bond to form.

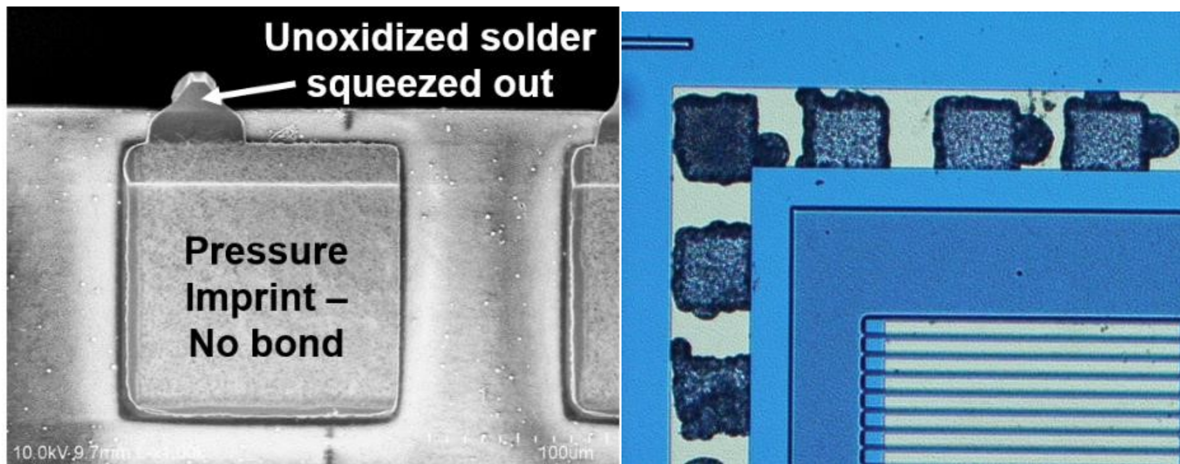


Figure 7-20: (Left) Oxidation layer prevents effective bonding. Pressure is applied to the bottom half of the bond pad. Solder escapes from the top half. (Right) Pressure is applied across the entire bond bad, creating a good bond around the periphery of the square due to unoxidized metal escaping from the edges.

Standoffs

When bonding to polyimide pillars, the softness of the polyimide caused it to deform when the bond pressure exceeded 3N. Deformation of the polyimide would lead to cracking of the brittle thermoelectric film over it, reducing electrical connectivity. Lower forces caused a large wedge error to appear during bonding. To better control the bond force, two fabrication changes were implemented. First, the height of the bond ring was set to at least 1.5-µm greater than the height of the TE film stack. Second, tall Si pillars were etched into the cap die. These pillars mechanically stop the compression of the polyimide beyond a set point and allow uniform pressure distribution across the entire die, reducing the wedge error problem.

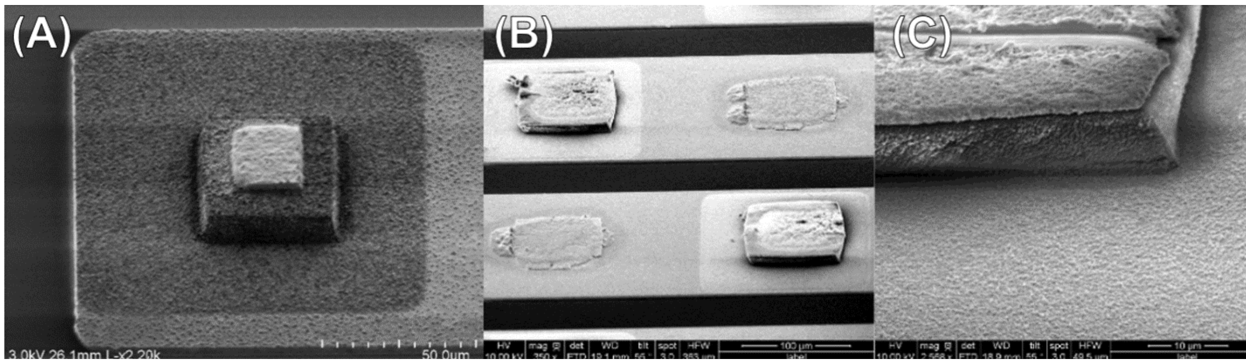


Figure 7-21: An-Sn on Bi_2Te_3 over polyimide (A) before and (B) (C) after bonding. Under 10 N of force, polyimide after bond shows severe deformation.

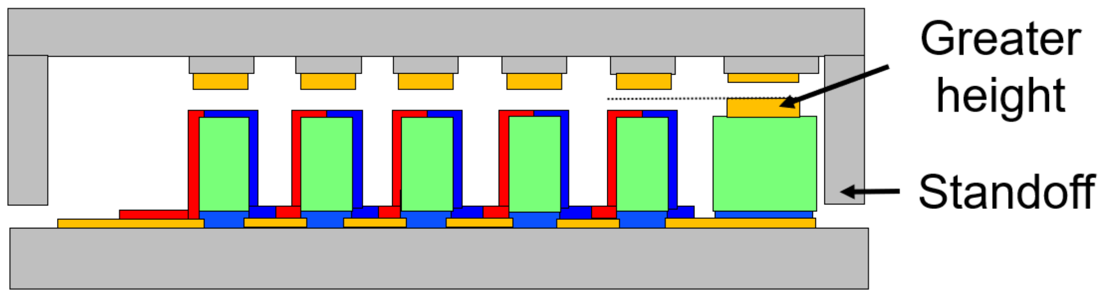


Figure 7-22: Standoff to control bond height

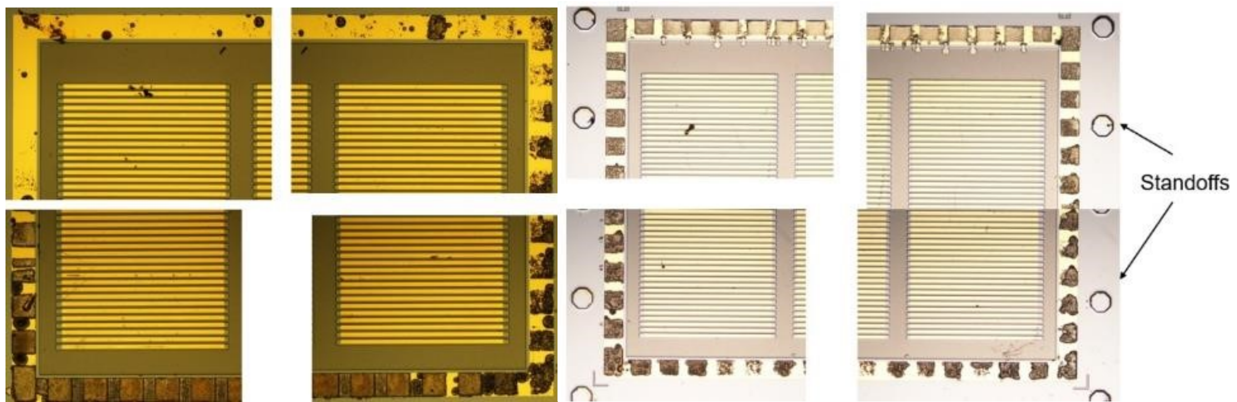


Figure 7-23: (Left) Wedge issue during bonding – only half of the die shows evidence of bonding. (Right) Use of stand offs improves bond uniformity.

Epoxy Attachment

In addition to eutectic bonding, die attachment with thermally conductive epoxy was also attempted. In this process, 8329TCM epoxy from MG chemicals was screen printed over the of the top cap and pressed down using 10N of force. This process was attractive due to its simplicity and lack of need for alignment. However, the thickness of the epoxy could not be well controlled due to its high viscosity. This created a significant extra layer of epoxy material above the TE pillars and below the silicon cap. The presence of this extraneous epoxy, in addition to its filling of the space between the pillars, degraded the thermal characteristics of the µTEG and thus, epoxy bonding was not pursued further for die attachment.

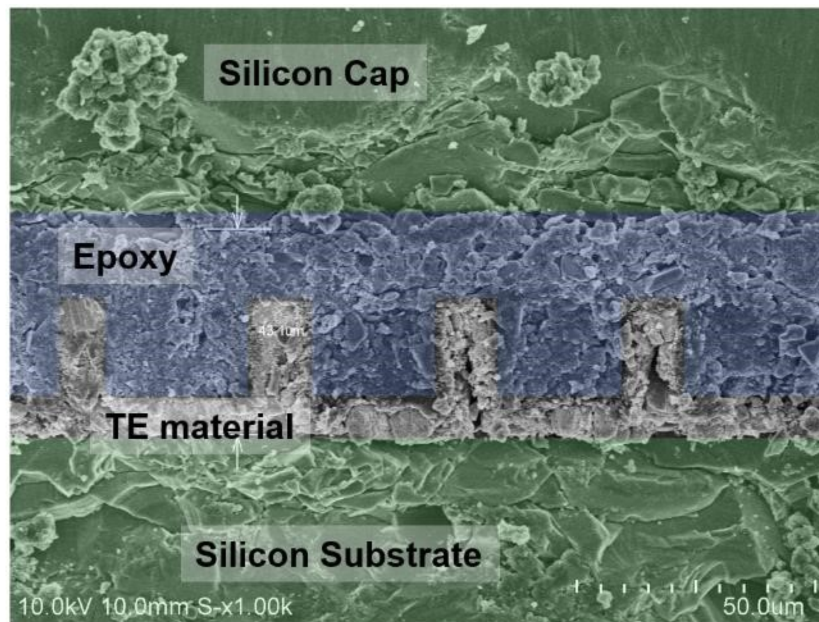


Figure 7-24: Cross-section of an epoxy bonded µTEG. The top and bottom silicon substrates are highlighted in green and the epoxy fill is highlighted in blue. In the uncolored portion of the image are thermoelectric legs of the µTEG.

Film Oxidation

During bonding, oxidation of Bi_2Te_3 and Sb_2Te_3 was encountered. In atmosphere, Bi_2Te_3 oxidizes into Bi_2O_3 and TeO_2. Formation of this oxide occurs at temperatures as low as 320 K

and increases steadily with temperature until of 650 K where a four-fold increase in the oxidation rate[71] exists. Furthermore, migration of Au into Bi_2Te_3 can increase this rate[72] The high surface to volume ratio of the deposited TE films, in addition to atmospheric bonding, made the fabricated µTEGs highly susceptible to oxidation. To measure the effect of this fabrication, test devices were fabricated without metal contact to the TE thermocouples to rule out the effect of metal diffusion into the TE as a possible cause. For measurement purposes, two Au pads were present and connected to the TE leg-pairs with a contact area of 1 mm^2 each.

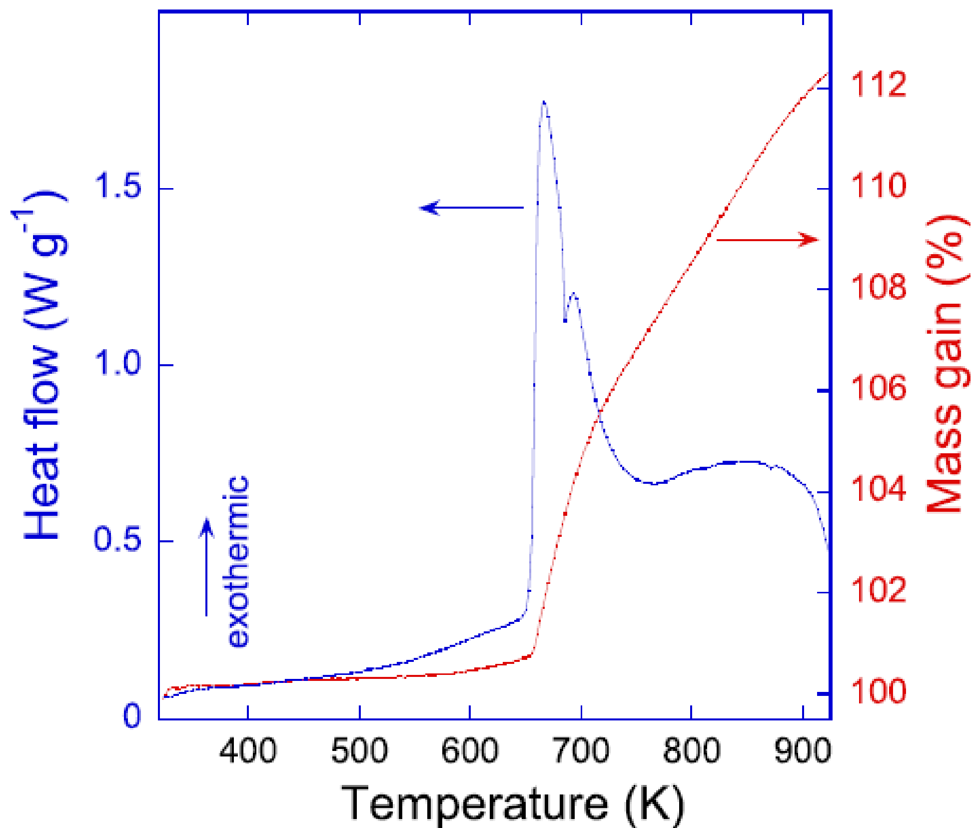


Figure 7-25: Relative oxidation rate of Bi_2Te_3 powder in atmosphere as measured by calorimeter [71].

For a device with an initial electrical resistance of 400 Ω, heating in atmosphere at the Au-Sn eutectic temperature of 280° C for 4 minutes increase resistance by over 50%, to 610 Ω. With forming gas, an increase of only 25% from 400 to 500 Ω is observed. No significant increase in

resistance was seen for temperatures at 200°C, while the increase for 240°C was less than 10% after 6 minutes. Given these results, bonding of Bi_2Te_3 based μTEGs should be carried out in vacuum or at temperatures below 240°C.

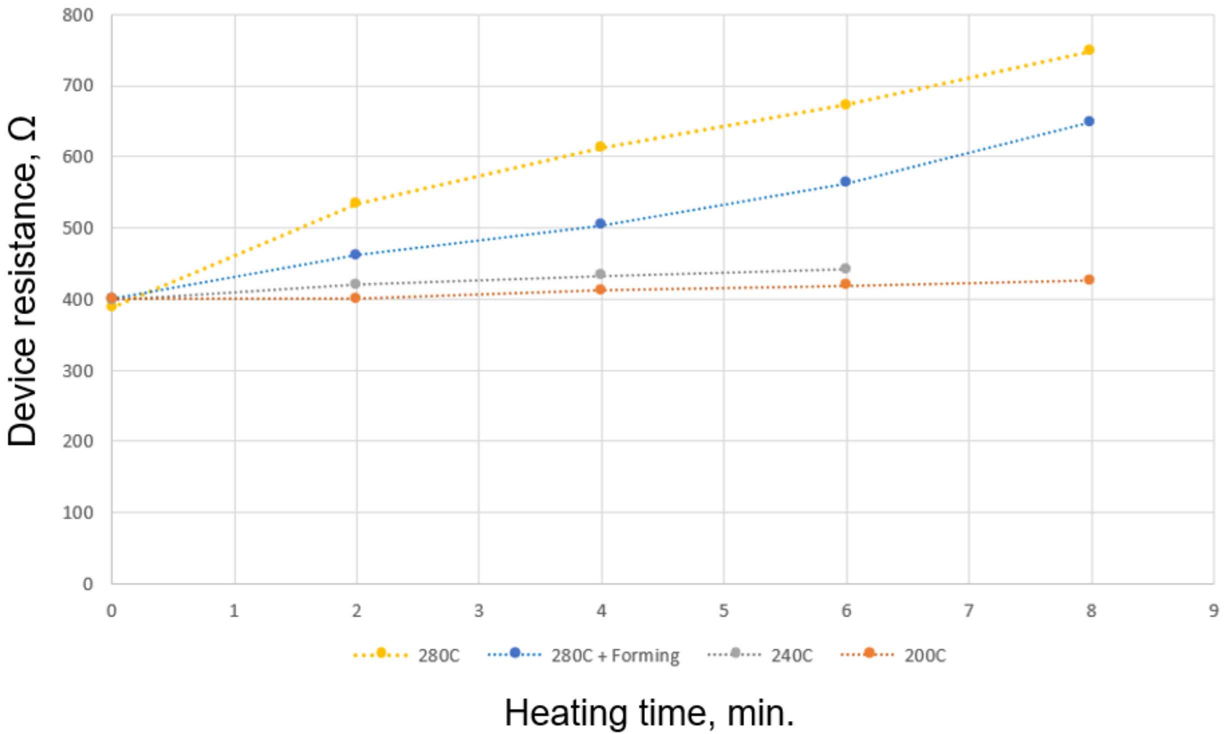


Figure 7-26: Increase in μTEG device resistance after heating in atmosphere

Oxidation was also seen during O_2 plasma cleaning of the film at lower temperatures. Using a standard photoresist stripping recipe at 150°C, O_2 plasma cleaning at 800 W almost doubled device resistance after 3.5 minutes. Initial resistance of the test device was 1.38 KΩ. After a 120 second plasma clean under the conditions given above, this resistance increased to 1.70 KΩ. Further exposure to oxygen plasma increased resistance to 2.11 KΩ after 210 seconds.

7.5 Conclusion

In this chapter, the major fabrication steps required to integrate the presented High-Aspect thermocouple design into functional thermoelectric generators were presented. The sacffolds themselves were created from both from oxidized silicon and polyimide patterned through dry etching. Polyimide scaffolds were shown to require additional support structures during bonding due to its deformation cracking the thermoelectric films deposited over it. The patterning of Bi_2Te_3 and Sb_2Te_3 films over high aspect structures was achieved using shadow masks. Shadow mask patterning with silicon hard masks is compatible with both severe substrate topologies and high deposition temperatures. Shadow masking has the additional benefit of being a dry process. This avoids exposure of the delicate Bi_2Te_3 and Sb_2Te_3 films to damaging solvents. During bonding, film oxidation was identified as a major concern due to the high surface to volume ratio of these thin thermoelectric films. This oxidation can be resolved by bonding in a vacuum environment or keeping bond temperatures below 240°C. An In-Au system, with a eutectic temperature of 156°C would be low enough to avoid the major effects of oxidation.

Chapter 8 μTEG Device Integration

This chapter details integration of the developed high-aspect thermocouple structures into functional thin-film μTEGs. Two types of μTEGs are present; one utilizing polyimide scaffolds and one utilizing oxide scaffolds. Detailed fabrication steps and challenges encountered with process integration are provided. Initial measurement of the performance of the fabricated μTEGs are also presented.

8.1 Proof of Concept

A proof of concept μTEG was fabricated on a polyimide substrate. This design did not incorporate Au into the metal junctions.

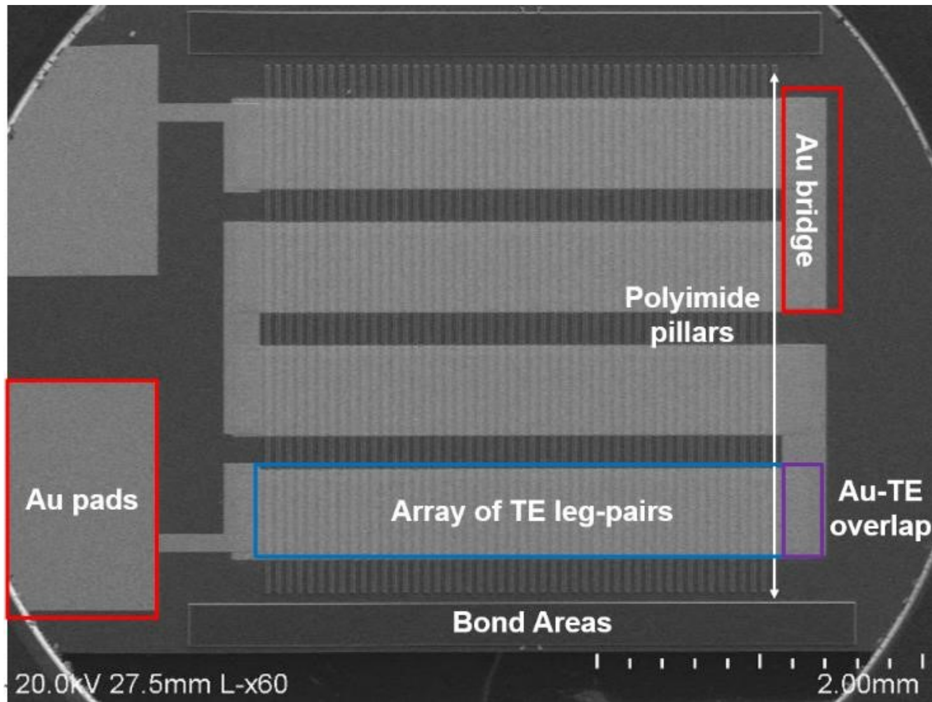


Figure 8-1: SEM of µTEG proof-of-concept device.

Attachment to a topside heatsink was achieved using thermally conductive epoxy method described in Chapter 7-4. The presence of large amounts of epoxy with low thermal conductivity of 1.3 W/mK hampered device performance.

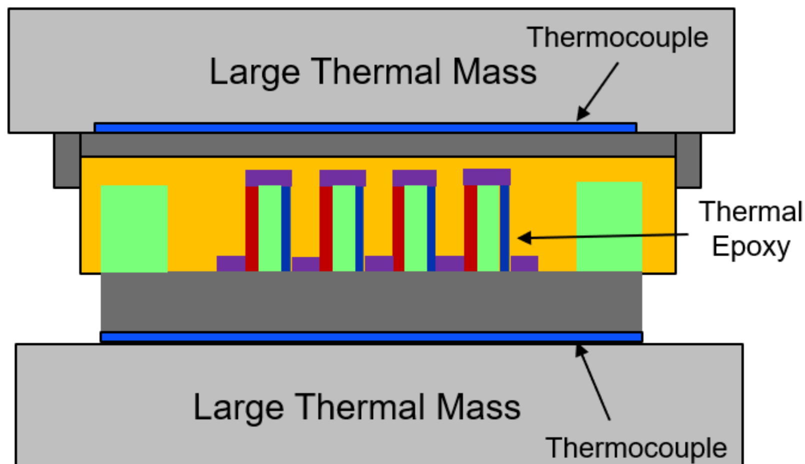


Figure 8-2: Diagram of proof-of-concept TEG and testing set up

Temperatures were measured using a FLIR camera on the topside of the device and a surface mounted thermocouple below the bottom substrate. The topside heatsink was passively cooled in air. Due to the small size of the topside heatsink, only a small temperature gradient could be maintained across the device.

Table 8-1: Voltage output of Proof-of-Concept Device

Sample #	Description	T_{Hot} - T_{Cold}	Measured Voltage	Resistance
C1	No TE deposited	58 – 56 °C	Noise	N/A
C2	TE film, no scaffolds	58 – 56 °C	.067 mV	1424 Ω
S1	2/30 µm pitch	58 – 56 °C	1.32 mV	1024 Ω
S2	3/30 µm pitch	56 – 54 °C	1.15 mV	1040 Ω
S3	2/25 µm pitch	56 – 54 °C	2.66 mV	-

Of note is that the electrical resistance for the measured control die (C2) with no scaffold present has a higher electrical resistance than films deposited on devices with the polyimide scaffolds. This is despite the fact that the polyimide scaffold doubles the effect length of the film, and the dual Bi_2Te_3 and Sb_2Te_3 deposition on a single surface means that this composite BiSbTe on C2 is twice as thick as the films in S1 – S3. The resistivity of the BiSbTe composite layer is thus likely over 4 times higher than the average resistivity of the Bi_2Te_3 and Sb_2Te_3 films. This means that the resistance across the Bi_2Te_3 – BiSbTe – Sb_2Te_3 interface may be dominated by the resistance of the BiSbTe film itself, and not the contact resistance between the different films, as previously though.

8.2 Polyimide μTEGs

Fabrication

The final fabrication process for High-Aspect μTEGs using polyimide scaffolds is given below. Starting with an initial Si wafer with 500 nm of thermal oxide, a 10/500 nm thick Cr/Au metal is deposited through evaporation and patterning using lift off (A). This metal layer serves as the metal bridge between successive TE leg-pair arrays (Fig. 8-1) and provides a way to reduce the electrical resistance of the BiSbTe composite layer between the polyimide pillars. After Au deposition, mounting holes for shadow mask alignment are created using a through wafer DRIE etch. After DRIE, blanket low-stress oxynitride is deposited over the wafer (B).

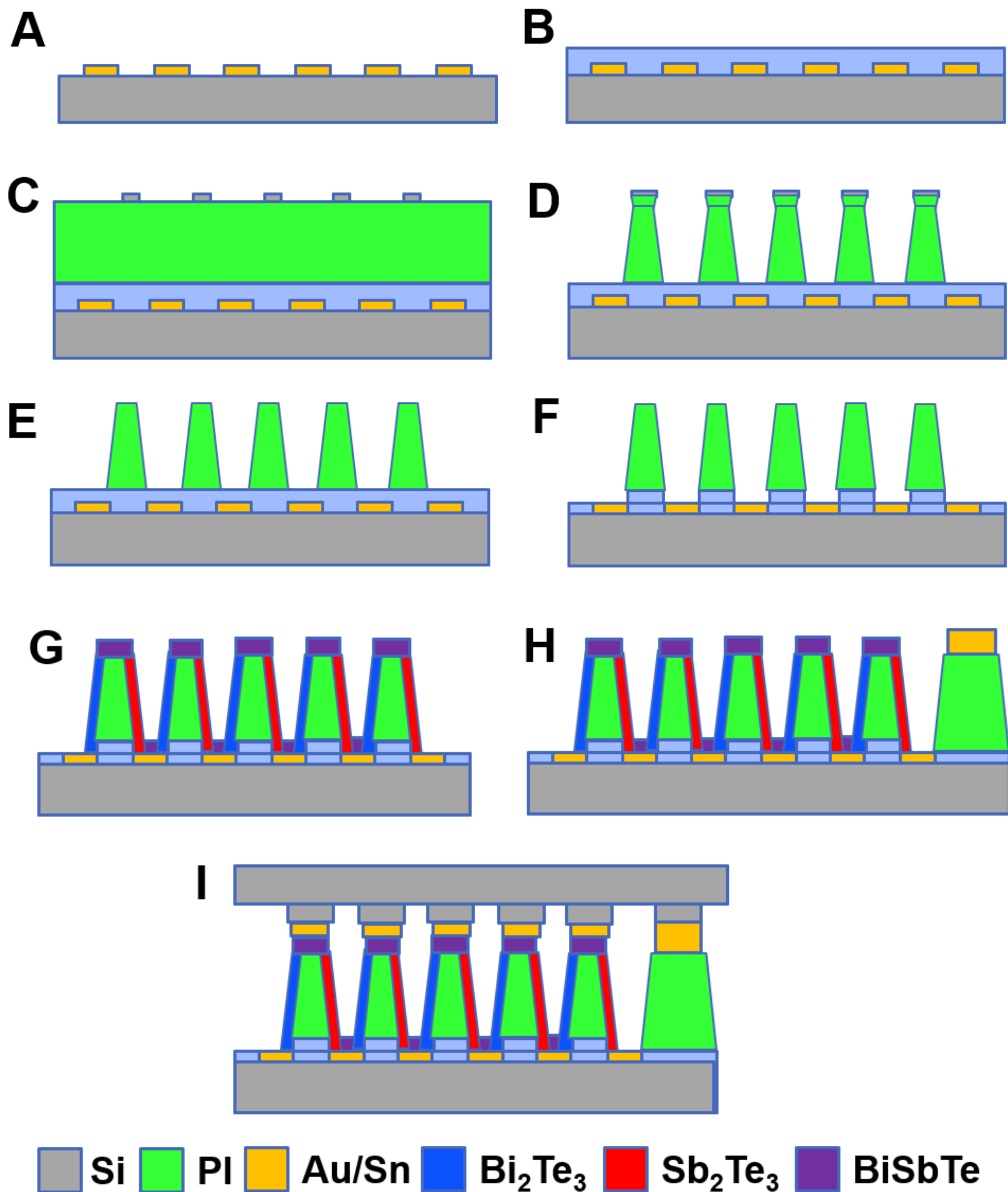


Figure 8-3: Fabrication steps of a µTEG using polyimide scaffolds

The oxynitride passivates the Au layer during the polyimide dry etch, eliminating tool contamination from the exposed Au. A thick 2-um layer of the oxynitride was required due to the

long polyimide etching and smoothing process. (C)A 50-μm thick coat of HD 4110 polyimide precursor is spun over the entire wafer and then fully cured at 400°C for 60 minutes in an inert environment. During the curing process, the thickness of the spin-on-polyimide decreased from 50 to 20 μm. To prevent stress related issues during curing, a 30 minute hold at 200°C is used before full cure at 400 °C. Additionally, the ramp rate from 200°C to 400°C was set to a slow 5°C/min. After cure, a 100 nm layer of Al is deposited over the polyimide to serve as the hard mask for polyimide RIE (C). This Al layer is patterned through wet etching. The anisotropic RIE process given in table 7-2 leaves a reentrant profile near the top of polyimide. To remove this profile, the Al hard mask is first stripped, the underlying polyimide is subjected to a 10 minute isotropic O_2 + CF_4 etch with no applied RF bias (E). Afterwards, the protective oxynitride layer is selectively removed(F) to expose clean Au for deposition of the thermoelectric films (G). The thermoelectric films are deposited using parameters given below in table 8-2 through a shadow mask.

Table 8-2: TE film parameters for deposition on vertical polyimide surfaces

Film	Temperature	Bi/Sb Dep. Rate	Te Dep. Rate	Set Thickness (kÅ)	Measured thickness
Bi_2Te_3	250 °C	Bi: 2 Å/s	3 Å/s	Bi/Te :12/18	1.95 μm
Sb_2Te_3		Sb: 1 Å/s	3 Å/s	Sb/Te : 6/18	1.75 μm

A thick bond metal composed of 2-μm of Sn and 3-μm of Au was deposited over the polyimide bond ring on the periphery of the device(H). The thickness of this bonding material (yellow)was set to be 1.5-μm greater than the thickness of the composite BiSbTe (purple) film to ensure good contact and pressure distribution during bonding. Recesses are then etched on the cap wafer to prevent shorting of the bond material. The cap was then passivated through a wet oxidation step. A metal stack identical to the bond metal in step (H) was then deposited over the cap wafer.

Using an identical stack in this process allows the cap and device wafer to share the same deposition run, saving material costs. Finally, the cap and device wafer are bonded together using a Fine-tech flip chip bonder at 300°C. The pressure used for the bonding process was 4 MPa, accounting for both the polyimide bond ring and the thermocouples.

The Au/Sn eutectic does not wet the BiSbTe material during bonding and thus the only bond regions formed are along the bond ring.

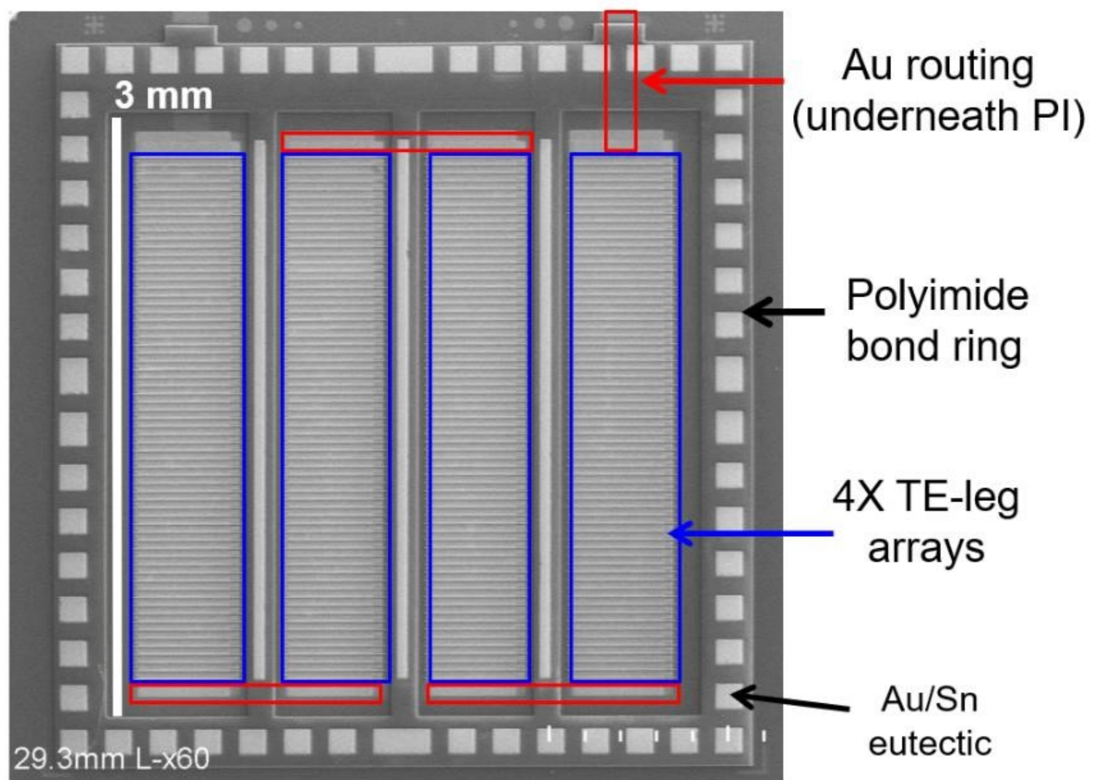


Figure 8-4: SEM of Fabricated μTEG with polyimide scaffolds

Measurement

To measure the voltage output of the fabricated μTEGs, the μTEGs were sandwiched between two copper blocks. These copper blocks were then attached to larger Al masses using thermal grease. The large Al blocks provide a large thermal mass for better temperature stability.

Thermal grease was not used between the TEG and the copper blocks as the tackiness of the grease would frequently detach the cap from the device die, preventing further measurement. This was an issue due to the low yield of the polyimide fabrication process. The temperature was measured using an FLIR infrared camera calibrated for copper. The voltage output of the fabricated polyimide devices was measured to be relatively low. A typical value of 6 mV/K was achieved for µTEGs consisting of 2 TE-leg arrays, corresponding to a Seebeck per-TE leg of only 38 µV/K, far below the expected Seebeck of 120 – 160 µV/K (Table 8-3). With a measured device resistance of 602 Ω, the TEG figure of merit is only 0.6 $\mu W/cm^2/K^2$, compared with the expected FoM of 8 $\mu W/cm^2/K^2$.

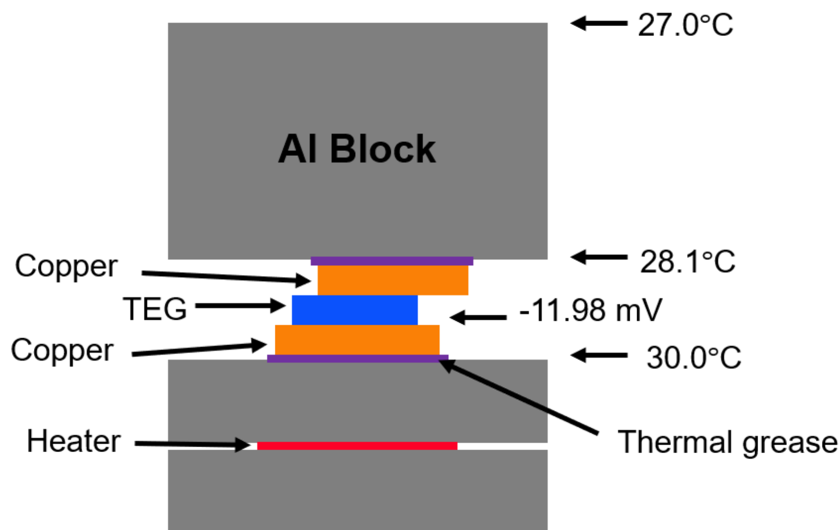


Figure 8-5: Polyimide µTEG Measurement set up.

Table 8-3: Measured vs. expected values of a Polyimide µTEG.

	Measured	Expected
Resistance	602 Ω	280 Ω
Voltage	6.3 µV/K	22 µV/K
Thermal Res.	-	11.2 K/W

A major reason for the voltage discrepancy above was believed to be cause by the inaccurate measurement of the temperature across the μTEG. The fixed focal plane of the FLIR could only measure the temperature of the aluminum block, and not the temperature at the surfaces of the μTEG. The temperature measured is believed to be an overestimate of the actual temperature across the device. The two major unknown thermal resistances that contribute to this temperature difference was that of the Al-thermal grease-Cu junction and the copper-TEG junction, which did not contain thermal grease. The increase in resistance of the device was attributed to its oxidation during bonding, detailed in Chapter 7.4, and fabrication defects detailed below.

Challenges

The initial fabrication runs of the polyimide process yielded μTEGs with extremely high electrical resistances, roughly 5 – 10x greater than the expected value. Additionally, the control dies, which had no no pillars present, had resistance over twice of what was expected given an assumed resistivity value of 30 μΩ-m. This assumed value is the average resistivity of the Bi_2Te_3 and Sb_2Te_3 films. This higher resistance matches the results from the proof-of-concept μTEG device. This provided further evidence that the BiSbTe film was exceptionally resistive.

Table 8-4: Pre-bond polyimide μTEG resistances.

Die Type	Measured (Ω)	Expected(Ω)
Control (no pillars)	345	150
F (1)	1630	320
F (2)	3260	320
F (3)	1910	320
F (4)	3890	320
H (1)	2080	280
H (2)	1820	280

The larger increase in the resistance of the non-control μTEGs was found to be caused by the undercut of the oxynitride present below the polyimide pillars (Fig. 8-6). This undercut occurred during the PI dry etching processes. Over etching of the polyimide was required due to variation in the polyimide height due to the slow spin speed and high film thickness. The sloped sidewalls of the PI during etching causes ion channeling effects, preferentially etching the passivation at the base of the polyimide. The isotropic etch, with poor selectivity to SiON, then enlarges this opening and undercuts below the base of the polyimide. The resulting gap is hard to fill by the TE deposition process, leading to a resistance chokepoint at the bottom of the polyimide.

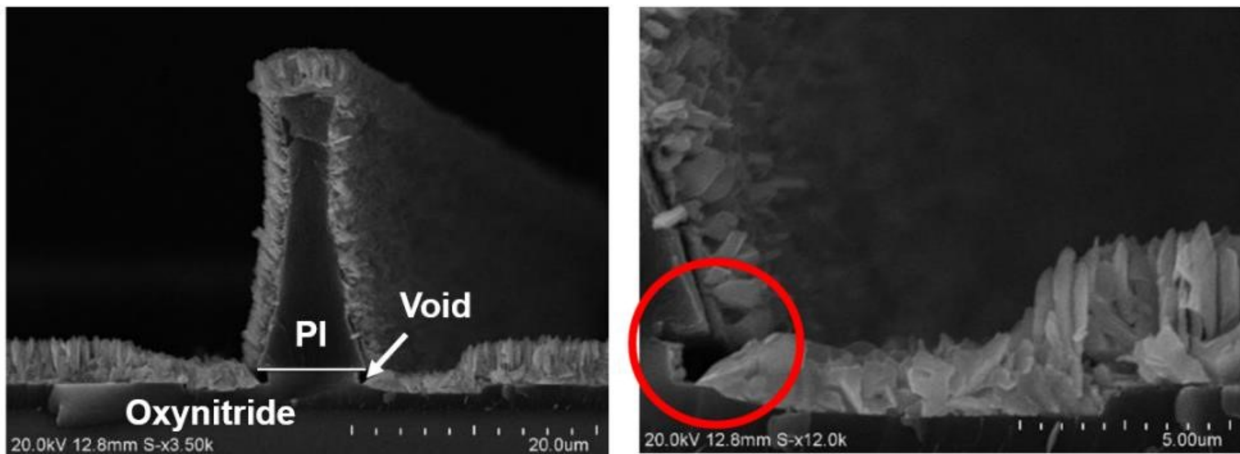


Figure 8-6: Undercut of oxynitride below polyimide pillars.

This thin connection between the film also rendered the μTEGs extremely sensitive to oxidation during bonding, and the already high electrical resistance increased significantly post bond.

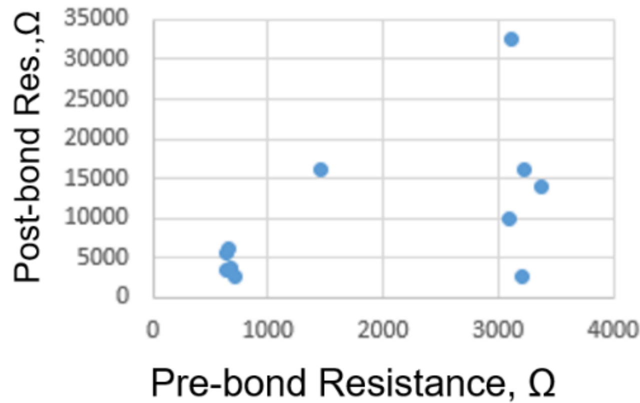


Figure 8-7. Resistance of polyimide µTEGs, before and after bonding.

Better control of the polyimide etch process and thinner polyimide resolved this issue. Thinner polyimide could be spun at faster speeds, improving film uniformity near the edges of the wafer and reducing edge bead. With a more uniform film, over etching of the polyimide was no longer necessary, and a timed stop of the etch on the oxide surface was easier to obtain. Polyimide generators fabricated using this process did not show the undercut present in the taller device.

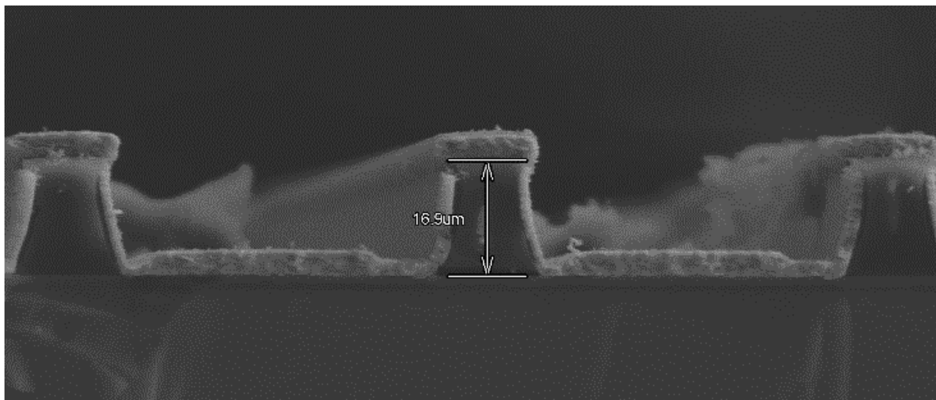


Figure 8-8: Thinner polyimide scaffolds with no oxide undercut

Additionally, the did not exhibit the extremely large increase in electrical resistance after bonding. However, due to oxidation and the high bond temperature of 305° C, resistance still increased by a factor of 2 during the bonding process.

Table 8-5: Increase in device resistance during bonding

Die	PI Spacing	Res. before bonding	Res. After Bonding	Bond temperature
A	35 µm	961 Ω	-	
C	25 µm	683 Ω	1.22 KΩ	305 °C
D	25 µm	756 Ω	-	
E	30 µm	558 Ω	1.07 KΩ	305 °C

8.3 Oxide Based Generators

In addition to polyimide scaffold, µTEGs were also fabricated using oxide scaffolds. The advantages of oxide are greater scaffold height, and thus greater µTEG thermal resistance, and higher scaffold density for increased fill factor. The drawback is reduced area on top, initially this was thought to make contact formation harder, but was later overcome with a soft bonding metal.

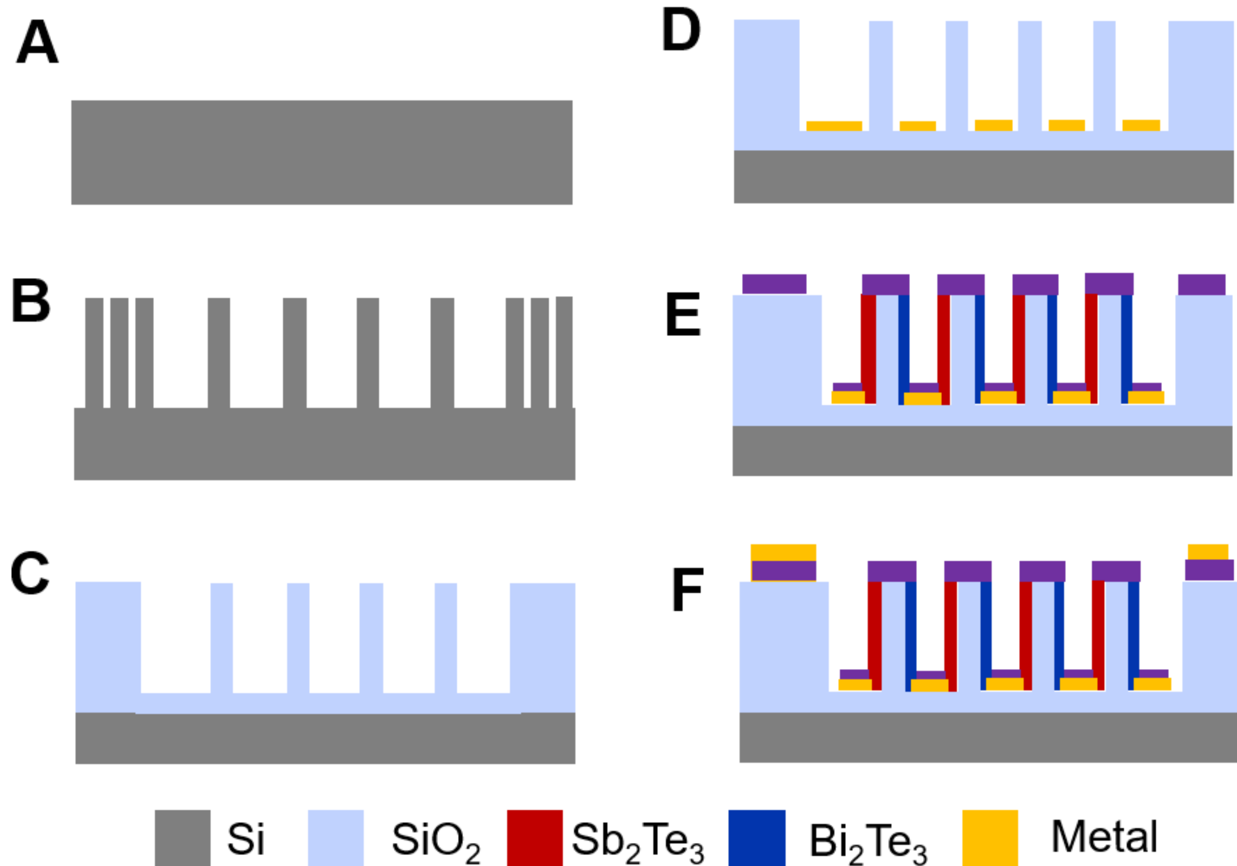


Figure 8-9: Fabrication process for µTEGs with oxide scaffolds

Fabrication processes was similar to the polyimide µTEG fabrication. Starting with (A) bare silicon wafer, mounting holes for shadow mask attachment are etched. Afterwards, narrow silicon pillars 3-µm wide and 25-µm tall are created on the wafer surface through silicon DRIE (B). Afterwards the structure is wet oxidized, consuming 1-µm of silicon from each side of the pillar, leaving 1-µm remaining. The oxide from this initial oxidation is then stripped in 1:10 HF, smoothing the sidewall surface of the pillars. The remaining silicon pillar is then fully oxidized, creating narrow oxide pillars 2-µm wide (C). The bond ring is similarly formed from silicon pillars, but with greatly decreased pitch for structural robustness. If the initial Si pillars are space closely enough, a solid block of oxide can be formed after the first oxidation step [75]. However, to reduce thermal conductivity, pillars were spaced farther apart, at 1:3 intervals.

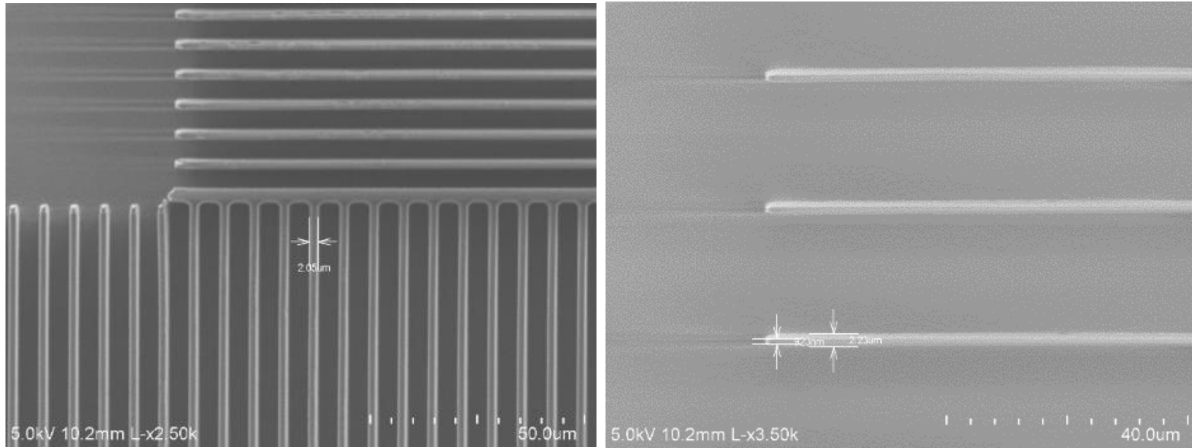


Figure 8-10: (Left) Close up of bond ring composed of tightly packed oxide pillars. (Right) Oxide scaffold for TE deposition.

(D) 10/500 nm Cr/Au is then deposited between the high-aspect oxide pillars through shadow mask. Manual attachment of the shadow masks using screw fixtures detailed in Chapter 7.3 . The alignment accuracy of this process is less than 3-µm for unheated deposition processes. Unlike the polyimide process, TE film is deposited over the bond rings as well as the scaffolds. The additional thickness of the bond rings from the TE film deposition reduces the thickness requires of the follow Au/Sn eutectic layer (E). The TE film over the bond ring also increases the surface area available for bonding of each individual pillar. Due to the angled nature of deposition and the closed space pillars of the bond ring, the TE materials only coats a small portion of the vertical surface of the bond ring pillars, reducing its effect on the thermal conductivity of the bond ring.

Figure 8-11: Au deposited between SiO_2 pillars with shadow mask. Thinner Au exists on the top and bottom of the drawn feature due to the angle of deposition and the 25 µm offset of the shadow mask from the wafer surface.

Afterwards, the wafer is bonded to a cap using Au-Sn eutectic bonding at 300° C. The lowered bonding temperatures reduced the increased in resistance but rendered the dies more fragile.

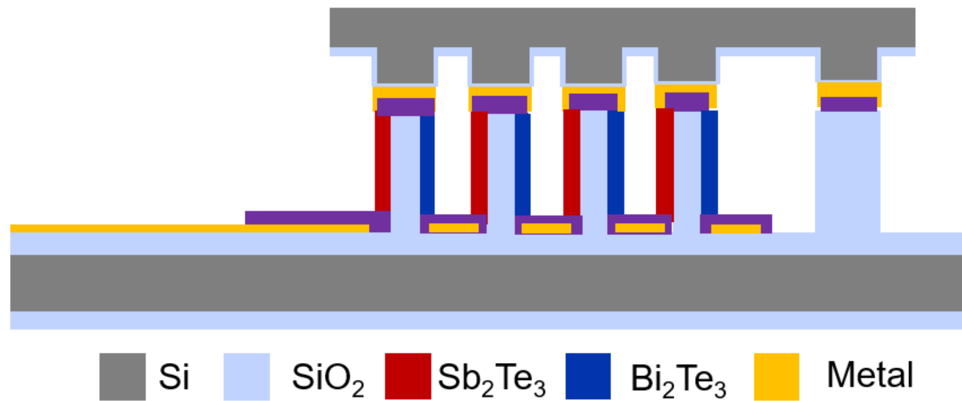


Figure 8-12: Diagram of bonded µTEG with oxide scaffolds

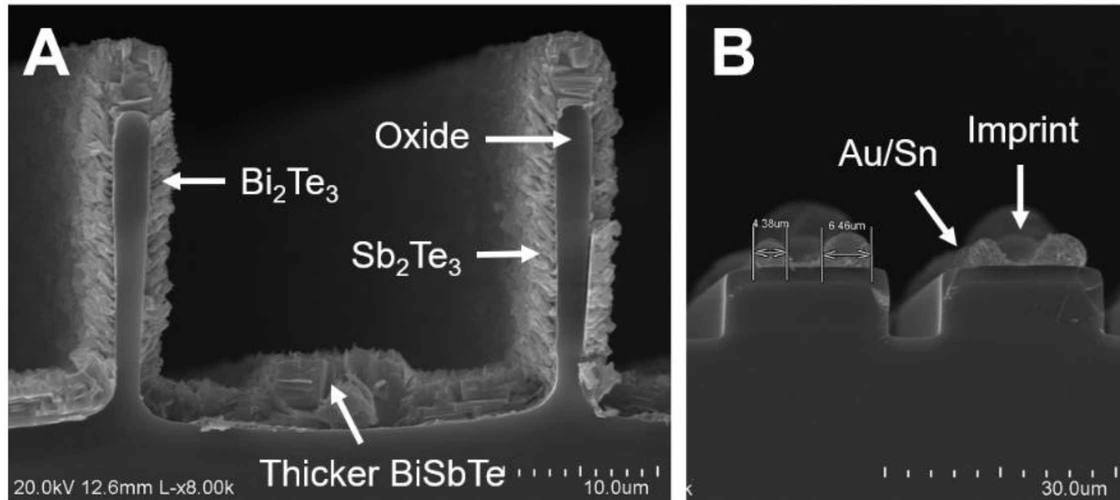


Figure 8-13: Fabricated oxide µTEG. Devices were previously bonded and broken apart. (A) Device die. (B) Cap die. Imprint of the TE-pillars can be clearly seen on the Au/Sn eutectic.

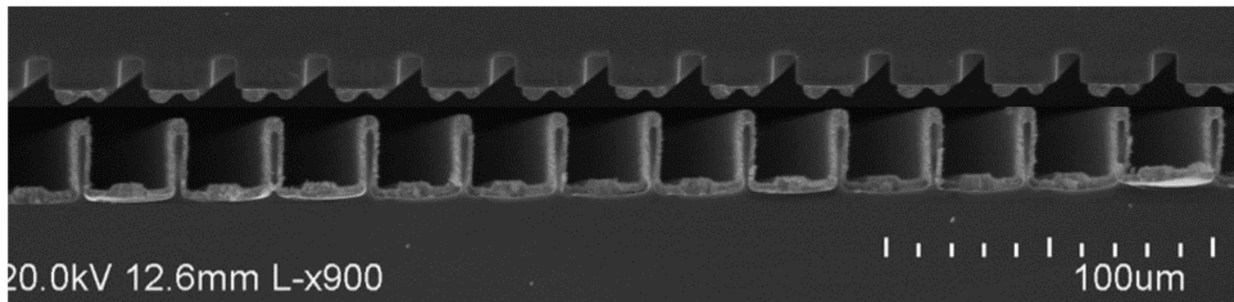


Figure 8-14: Composite SEM of a TE-leg pair array. Pictured is a Type "B" device.

Dual Temperature Films

For the oxide generators, the thermoelectric film was deposited under two different temperature conditions. For the first batch of devices, a single deposition temperature of 260° was used. This is denoted as Film #1 in Table 8-6 below. The second batch of devices used two different deposition temperatures, as previously discussed in Chapter 6.8. In addition to a standard 2-um thick 260°C deposition, a second TE film deposition at 100°C was deposited to "fill in" the voids of the high temperature film and increase electrical conductance. Chamber vacuum was not broken between the deposition of the high and low temperature films.

Table 8-6: TE Film deposition parameters on Oxide generators

	Film	Temp.	Bi/Sb Dep. Rate	Te Dep. Rate	Set Thickness (kÅ)	Measured thickness	Composition
Film #1	Bi_2Te_3	260 °C	2.4 Å/s	3 Å/s	Bi/Te 24/30	2.4 µm	38/62
	Sb_2Te_3		1.5 Å/s	3 Å/s	Sb/Te 15/30	2.15 µm	39/61
Film #2, 1st layer	Bi_2Te_3	260 °C	2.4 Å/s	3 Å/s	Bi/Te 21.6/27	1.94 µm	-
	Sb_2Te_3	260°C	1.5 Å/s	3 Å/s	Sb/Te 15/30	1.9 µm (est)	-
Film #2, 2nd layer	Bi_2Te_3	90 °C	3 Å/s	3 Å/s	3/3	-	-
	Sb_2Te_3	90 °C	1.6 Å/s	3 Å/s	1.6/3	-	-

Devices with TE films deposited using the two-temperature process showed significantly reduced electrical resistances compared with devices with standard TE films. This decrease was seen for both µTEG designs, A and B. Design A consisted of 4 TE-leg arrays. Each array contained 108 thermoelectric leg-pairs connected in series. The width of each leg-pair was 735-µm. Design B consisted of 2-TE leg arrays with 80 leg-pairs each. The width of each leg pair was double that of design A, at 1470-µm.

The average device resistance for "A" devices utilizing film #1 was 3200 Ω while device utilizing film #2 showed a 43% decrease in resistance with an average device resistance of 1810 Ω. The resistance for "B" devices were similar lower using film #2, at 339Ω, compared with 664 Ω for film #1. This is a decrease of 49% in electrical resistance.

Design A contains 2.7 time more thermocouples than design B with half the width. Thus a 5.4x increase in resistance is expected from device A to B if the resistance of the device was dominated by the thermocouple structure. This was observed in film #1, where the resistance of A devices was 4.8 times greater than B devices. For film #2, device A had a resistance 5.3 times greater than device B, almost exactly in line with expectations.

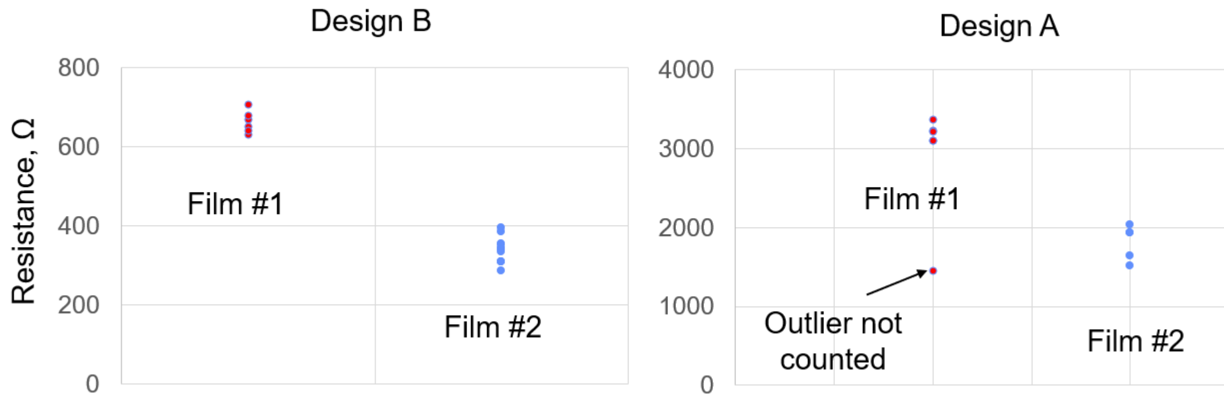


Figure 8-15: Decrease in device resistance using TE films with two deposition temperatures.

Fill Factor and Height

The fill factor of the fabricated “A” design is 17.5% and the fill factor of the “B” design is 12.5%. The height of the oxide pillar used in the design is 20-µm, corresponding to the effective thermoelectric leg length. These parameters are close to the fabrication target of 20% fill factor and 25-µm leg length. The leg length can be easily increased to 25-µm through deeper DRIE of the initial silicon pillars later oxidized to the oxide scaffolds. Fill factor can be increased by reducing the pitch of the scaffolds, with no changes required to the film deposition process. Currently, the minimum pitch of the scaffolds is limited by the 10-µm alignment tolerance of the Fine-tech flip chip bonder.

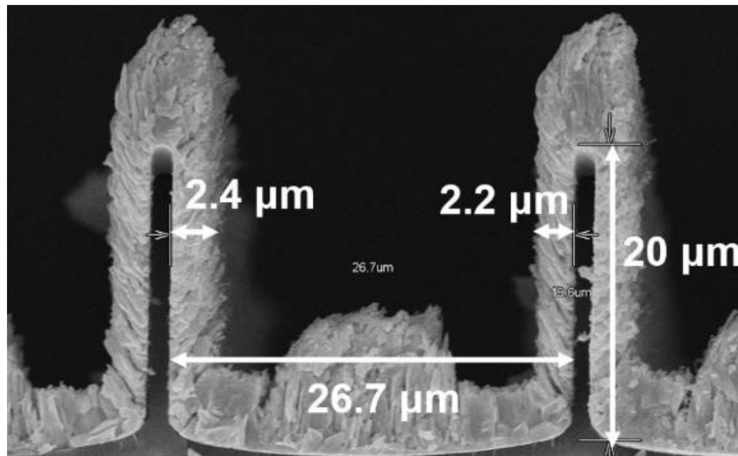


Figure 8-16: Dimensions of design "A".

Oxidation

Most devices showed a marked increase in resistance under standard bonding conditions of 5 minutes at 300°C. As noted in chapter 7.4, this increase in resistance was thought to be caused by oxidation of the thermoelectric film. The minimum bonding temperature was limited by the Au-Sn eutectic temperature of 280°C, above the point where significant increases in resistance occur (Fig. 7-25). In practice, set temperatures below 300°C resulted in poor bond quality; these dies did not typically survive handling. Hold times below 180 sec. at 300°C also resulting in poor bond quality. No correlation with the post-bond resistance was seen with the bonding force, up to 5N for a standard 3x3 die.

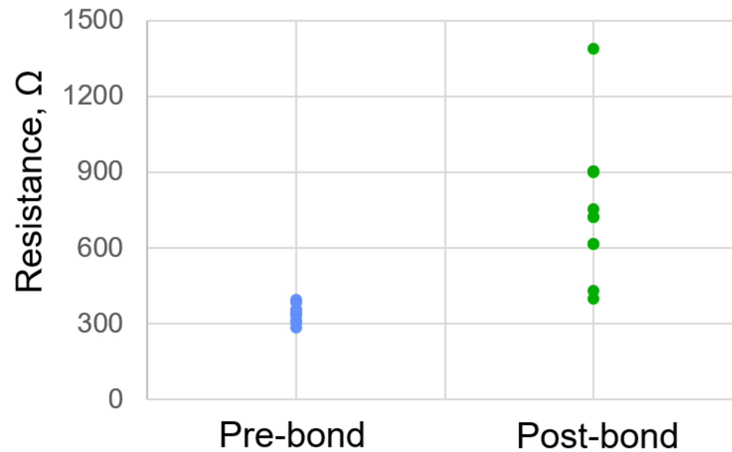


Figure 8-17: µTEG resistance before and after bonding. Forming gas was enabled for all bonds. However, due to technical difficulties, gas may have not been flowing.

Fabrication Considerations

To reduce bonding temperatures, an Au/In eutectic was considered as an alternate bonding material. Au/In has a eutectic temperature of 156°C, comfortable below the 240°C limit (Fig.7-25) where oxidation significantly effects device resistance. Ultimately, Au/In was not used due to concerns about shorting of the bond pads (Fig. 8-17). The +/- 10-µm anticipated alignment tolerance during die bonding required bond pads over 20-µm wide opposing the TE pillars (Fig. 8-12). During bonding, there was concern that these pads could short to each other. While this was rarely seen during Sn/Au bonding, the ductile nature of In could lead to greater shorting occurrences. Interestingly, the spread of Au/Sn solder was well controlled over areas contacting the TE film directly, with problems only occurring where the bare oxide pillar contacted the Au/Sn eutectic. With better bond alignment and removal of eutectic metal from the ends of the oxide pillars, using an Au/In eutectic may be able to resolve the TE oxidation issues, even when bonding in atmosphere.

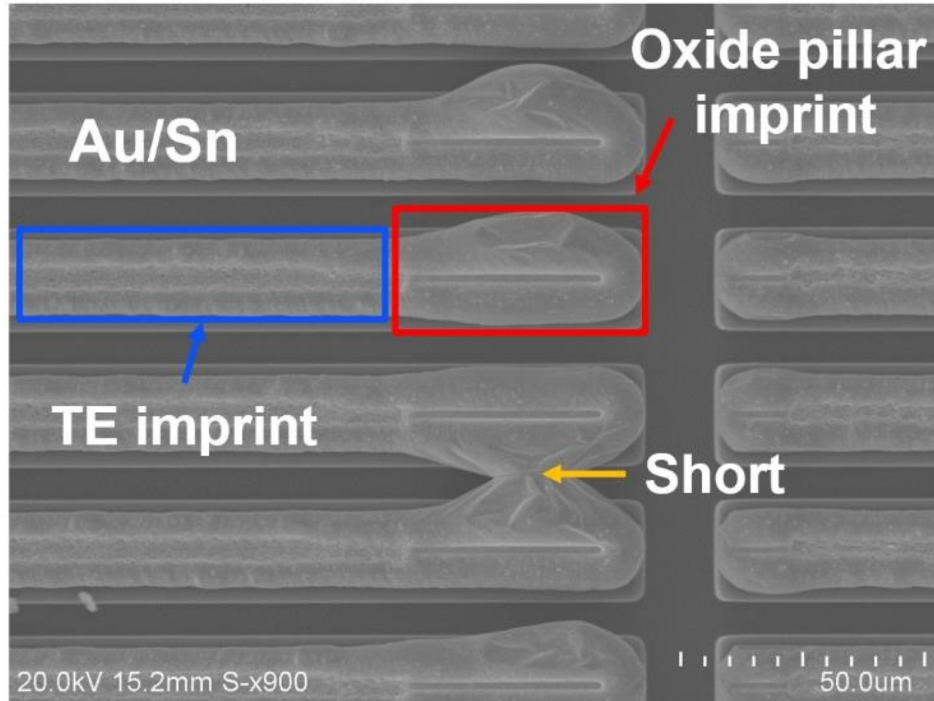


Figure 8-18: Shorting of closely spaced between bond pads opposing the TE pillars.

8.4 Measurement

Measurement on oxide μTEGs was conducted in a similar manner to polyimide μTEG testing. The key difference is the application of thermal grease to the top and bottom surfaces of the μTEG and the removal of the copper blocks. Instead, indents in the Al block were cut out to allow the FLIR camera to measure temperatures closer to the TEG. While the application of thermal grease gives a better thermal contact improving temperature measurement accuracy, the weakness of the bonding with the 300°C bonding process combined with the tackiness of the grease renders the measurement process destructive. Additionally, design “A” had an 80 micron wide bond ring compared to design “B” with 200 microns. This thinner bond ring made handling of the “A” design difficult and this design would frequently break during measurement set up.

Due to the height of the soldered wire lead to the μTEG devices, a 500-μm thick thermal pad was placed between the top side of the μTEG and the Al block. This thermal pad is malleable and

believed to compress to half its original thickness during testing. This pad is the 4237 series from Arctic with a stated thermal conductivity of 6 W/mK. This pad is expected to add a thermal resistance of 2.7-5.4 K/W to the system.

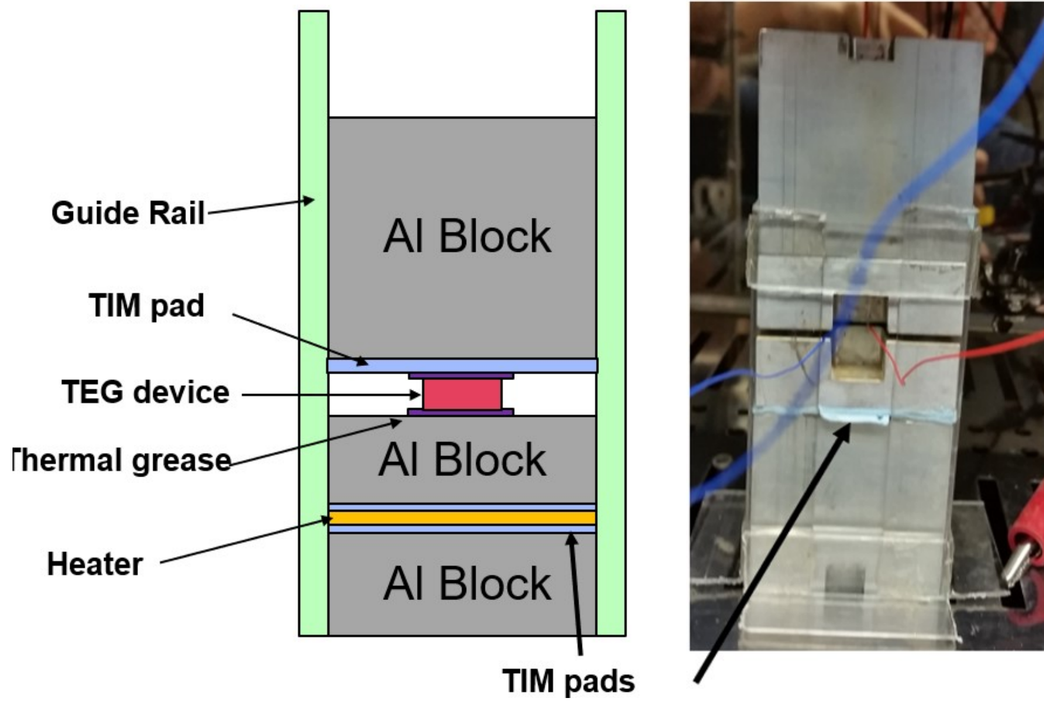


Figure 8-19: Measurement set up

Figure 8-20: Measurement of temperature through an infrared camera

A load test of a µTEG was conducted by connecting the device to a variable resistance and measuring the power output is given below. The tested device had a TE area of 3 x 3 mm. During testing, the heater was set to a 13 watt power output and the temperature was allowed to stabilize. The temperature difference across the junction was measured at .7° C. The tested device had an initial electrical resistance of 605 Ω. During testing however, this resistance increased to 660 Ω. As expected, the power output peaks with a matched external load close to the internal resistance of the device, at 700 Ω. At this point, power output is approximately 0.18 µW, corresponding to a device figure of merit of 4.08 $\mu W/cm^2/K^2$.

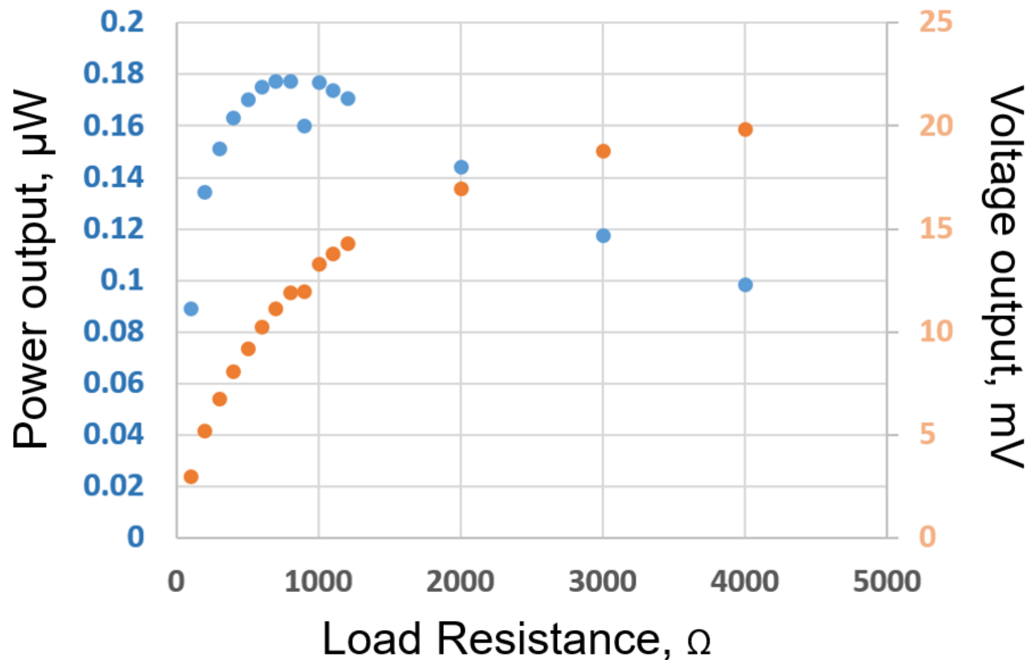


Figure 8-21: Measured power output as a function of load resistance

The expected figure-of-merit for the best measured µTEGs are given below in Table 8-7. The values are lower than the expected values from Figure 6-4, which account for the lower power factor of sidewall films. The discrepancy in output voltage is partially attributed to the thermal resistance of the thermal pad used during testing, along with the thermal grease used at the

interfaces. Furthermore, the accuracy of the temperature measurement taken with the FLIR camera has not been verified, and it is possible large error bars exists in both directions.

Table 8-7: Measured voltage output of fabricated μTEGs.

	Measured Res.	Expected Res.	Measured Voltage	Expected Voltage	Figure of Merit ($\mu W/K^2/cm^2$)
Polyimide TEG	602 Ω	280 Ω	6.3 μV/K	22 μV/K	0.86
Oxide B, Film #1	691 Ω	152 Ω	26 μV/K	45 μV/K	4.9
Oxide B, Film #2	600 Ω	152 Ω	23 μV/K	45 μV/K	4.4

The resistances of the fabricated devices are also much higher than expected. Half of this increase in resistance can be attributed to oxidation of the thin TE films during bonding. This oxidation can be resolved by bonding in a vacuum environment, or switching to lower temperature bonding materials, such as Au/In eutectic. The second half of the resistance increase is suspected to be caused by either the BiSbTe material itself, given the high resistance of blanket BiSbTe films (Table 8-1, 8-5), or the Bi_2Te_3-BiSbTe-Sb_2Te_3 junction. This connection is eliminated between pillars with the addition of Au. However, it still exists over the top surface of the pillars. This material over the top surface is not affected by bonding to Au/Sn, as a presumed oxide layer over the BiSbTe prevents wetting of the surface. This oxide can potentially be removed through bonding in a sealed environment with forming gas. Alternatively, Au deposition over the top surface of the pillars can directly bridge (Fig.8-20) the Bi_2Te_3 and Sb_2Te_3 films. This approach would require further significant process development due to the difficulty of patterning over high aspect structures.

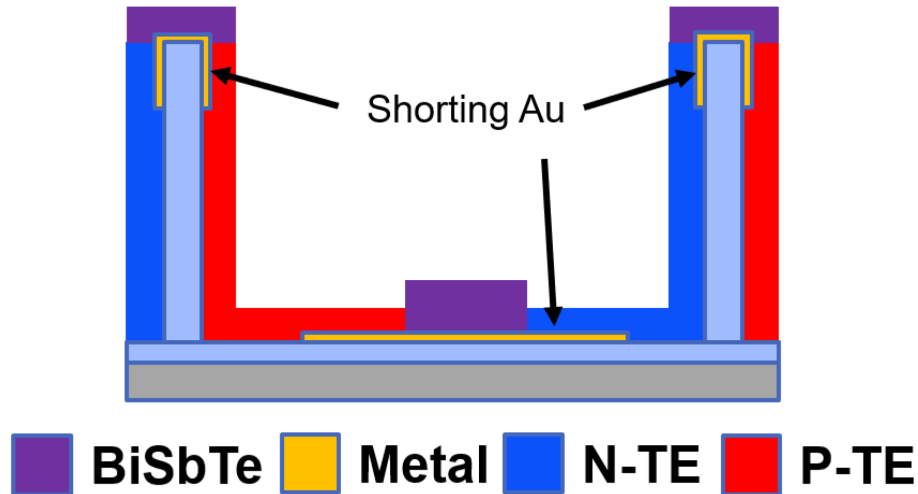


Figure 8-22: Addition of Au to decrease contact resistance over oxide pillars

8.5 Conclusion

In this chapter, successful integration of the High-Aspect thermocouple structure into functional micro-thermoelectric generators was presented. Fabrication processes for μTEGs utilizing oxide and polyimide scaffolds were presented. The fabricated oxide μTEGs had thermoelectric leg lengths of 20-μm and fill factors of 17.5%. These values are slightly lower than target values but can be increased through process changes.

Film oxidation and the BiSbTe composite were identified as significant sources of electrical resistance in the thin-film μTEG design. The oxidation issue can be resolved by bonding in a vacuum environment. This would half the electrical resistance of the fabricated generators and double power output. The resistivity of the composite BiSbTe material is estimated to be 4 times that of the sidewall films, at 120 μΩ-m compared with 30 μΩ-m for sidewall Bi_2Te_3. This high resistivity is in-line with the BiSbTe resistivities reported by Ghafouri [28] of similar co-evaporated BiSbTe films. There, it was believed that the cause of the higher resistances was due

to the much smaller grain sizes of co-evaporated BiSbTe compared with Bi_2Te_3 and Sb_2Te_3, causing much lower carrier mobilities.

Table 8-8: Reported properties of co-evaporated BiSbTe [28]

T_{sub}	FR (Bi:Sb:Te)	ρ (μΩ-m)	α_s (μV/K)	α_s^2/ρ (mW/K^{2}m)	At% (Bi:Sb:Te)	Average Roughness (nm)
160	0.5:1.5:3	162	85	0.045	10.4:27.8:61.8	21.1
200	0.5:1.5:3	169	113	0.075	7.4:28.9:63.7	45.2
240	0.5:1.5:3	161.7	75	0.038	8.2:30.6:61.2	89.6

The power output of the produced generators was measured to be lower than expected, producing a moderate output of 4.1 μW/K^2/cm^2. This output is less than that of the μTEGs reported by Kishi [12] of 5.6 μW/K^2/cm^2 and Kouma [22] of 18.3 μW/K^2/cm^2. The aforementioned μTEGs used bulk thermoelectric films with ZTs of 0.4 – 0.6. The fabricated μTEGs exhibited superior performance compared to most thin-film based μTEGs (Table 8-9) with the notable exception of that reported by Dunham [15] of 135 μW/K^2/cm^2. This generator used a traditional thin-film architecture with low thermal resistance. The total thermal resistance of Dunham's μTEG[15] was reported at low 1.5 K/W with a thermocouple resistance of 0.92 K/W.

Table 8-9: Performance of Thin-film μTEGs

Ref #.	Author	N-Film	P-Film	Dep. Method	FoM (uW/K^2/cm^2)
[15]	Francioso	Bi_2Te_3	Sb_2Te_3	Sputtering	9.5 E-7
[9]	Böttner	Bi_2Te_3	Bi_2Te_3	Sputtering	2.4
[4]	Stark	Bi_2Te_3	Sb_2Te_3	Sputtering	0.089
[16]	Yuan	PolySi	PolySi	LPCVD	0.045
[17]	Yu	PolySi	PolySi	LPCVD	0.252
[15]	Dunham	Bi_2Te_3	Sb_2Te_3	Sputtering	135
	This Work	Bi_2Te_3	Sb_2Te_3	Evaporation	**4.08**

As the design and fabrication process for the presented μTEG structure is new, significant performance improvements can be realized without improving the underlying thermoelectric materials themselves. Through improvements in the design and fabrication processes, the performance of these μTEGs can be improved from 4 to 28 μW/K^2/cm^2 (Table 8-10). The simplest of these improvements would be to bond under vacuum to remove film oxidation. This would reduce the electrical resistance of the finished devices to the pre-bond resistances of 300 Ω, yielding an FoM improvement from 4.9 to 12 μW/K^2/cm^2. Without oxidation of the TE film, Au can be placed over the top of the thermocouple structures to further reduce electrical resistance. Finally, the pitch of the columns can be decreased from the current 25-35 microns to 15 microns, increasing the fill factor and voltage output, bringing the expected FoM to 28 μW/K^2/cm^2.

Table 8-10: Impact of design and fabrication improvements on High-Aspect μTEG performance

	FoM (μW/K^2/cm^2)	Electrical Resistance	Voltage Output
Current Result	4.9	691 Ω	26 μV/K
Vacuum Bonding	12	300 Ω	26 μV/K
Topside Contacts	17	200 Ω	26 μV/K
Decrease Pillar Pitch	28	330 Ω	43 μV/K

At this level of performance, the High-Aspect design becomes competitive with the high FoM but low thermal resistance μTEGs, such as the kind reported by Dunham [15]. While these traditional thin-film generators have a very high initial FoM, the power output of these devices drops considerably given realistic [15] external thermal resistances of 5 – 10 K/W. At an external resistance of 4.6 K/W, the power output of a 1.5 K/W device drops to just 10% of its original value (Fig. 8-22). Above this thermal load of 4.6 K/W, the improved High-Aspect μTEG is

expected to performance better as its higher thermocouple resistance of 5 K/W makes it more resistant to the effects of a high thermal load. This is despite its low initial FoM of 28 μW/K^2/cm^2. If the sidewall Bi_2Te_3 and Sb_2Te_3 films can be improved to match that of the best co-evaporated planar films reported in literature, this cross-over point can be reduced to an external load of just 0.9 K/W.

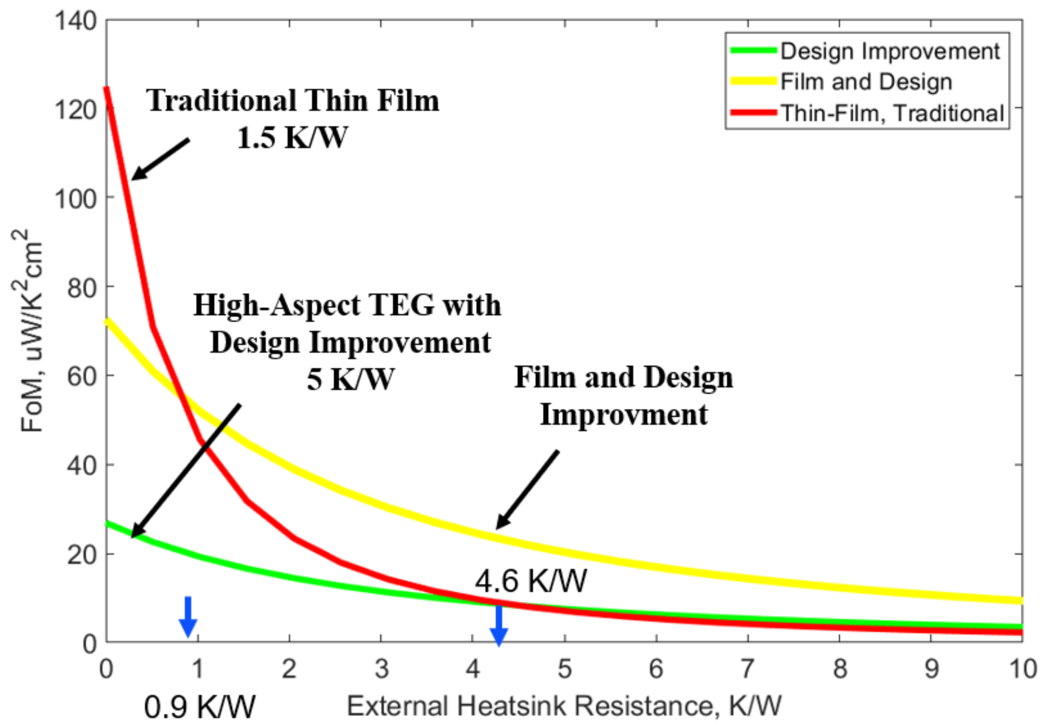


Figure 8-23: Power output of a traditional, low thermal resistance thin-film μTEG compared with potential power output of the High-Aspect design presented in this work.

This example illustrates the importance of building μTEGs with high thermocouple thermal resistance and the drawback of tradition thin-film based μTEGs. The work presented in this thesis allows thin-film μTEGs to overcome this resistance limitation and presents a path to superior μTEG performance under real world conditions. Through further design optimization, it is believed that the performance of μTEGs based on the presented high-aspect scaffold structure

can surpass traditional thin-film designs, even given the poorer properties of the sidewall thermoelectric materials.

Chapter 9 Conclusion and Future Work

The presented work provides a pathway to high performance thin-film μTEGs through device design. While much of the existing work in thermoelectrics focuses on the materials themselves, this thesis presents analysis on the design and integration challenges of thin-film thermoelectric generators. The principal drawback of thin-film based μTEGs, their low thermal resistance, is addressed through the novel High-Aspect thermocouple structure presented. Analysis on this new design indicate superior performance compared with convention thin-film generators, especially given realistic external thermal loads.

The challenges of thin-film integration into this new design is explored. While the configuration of the High-Aspect thermocouple structure currently does not support high ZT films, potential causes and solutions for this phenomenon are presented. Even given the poor performance of current integrated TE films, the presented design is expected to allow μTEGs with power outputs in excess of 30 $\mu W/cm^2/K^2$ with thermal resistance above 6 K/W. Specific contributions of this work are:

- Development of a novel thin-film μTEG thermocouple structure that decouples the film thickness from the thermocouple length while maintaining at least a 17.5% fill factor.
- Modeling and analysis of this new structure, including optimal design parameters given a specific external thermal load. Evaluation of the new structure as compared to tradition vertical μTEGs.

- Characterization of co-evaporated Bi_2Te_3 and Sb_2Te_3 films deposited on oxide, polysilicon, and polyimide substrates.
- Characterization of Bi_2Te_3 and Sb_2Te_3 deposited on vertical surfaces. Analysis of different factors impacting the sidewall film growth including deposition temperature, substrate topology and roughness, and film composition.
- Proposed methods to improve the performance of Bi_2Te_3 and Sb_2Te_3 deposited over vertical surface, including alternating high and low temperature depositions temperature and reduced scaffold spacing.
- Fabrication of new test structures to isolate the thermoelectric properties of vertical films.
- Integration of Bi_2Te_3 and Sb_2Te_3 sidewall films into the modeled thermocouple structure using angled deposition and self-shadowing.
- Analysis of the electrical contact between Bi_2Te_3 and Sb_2Te_3 sidewall films formed by the in-situ deposited BiSbTe film composite.
- Presentation of shadow masks as a clean, solvent free method to pattern Bi_2Te_3 and Sb_2Te_3 films.
- Identification of oxidation at elevated temperatures above 240°C as a major area of concern for thin Bi_2Te_3 and Sb_2Te_3 films.
- Integration of the presented High-Aspect thermocouple structures into functional μTEGs.

The best measured μTEGs had a power output of 4.9 $\mu W/cm^2/K^2$. This performance is above most thin-film based designs. These designs are highlighted in figure 9-1 in blue and purple for lateral and stacked designs, respectively. However, the achieved power output is below generators using bulk thermoelectric films, such as those reported by Kishi [12] with 5.6 $\mu W/cm^2/K^2$ and Kouma [22] with 9.3 $\mu W/cm^2/K^2$. However, there is significant room for

improvement in the high-aspect thermocouple design. By eliminating the identified oxidation issue by bonding under vacuum, device performance can be doubled (Fig. 9-1) to 9.8 μW/cm^2/K^2. Further gains can be realized through decreasing the pitch of the columns from the 35-μm of the tested devices to 15-μm, increasing thermocouple density. A pitch of 15-μm is above the minimum pitch spacing of 10-μm (Fig. 9-2) given a 20-μm tall scaffold. This increase in thermocouple density can double the output of the μTEG from 9.8 to almost 20 μW/cm^2/K^2, at a slight cost of lowering the thermal resistance of the device from 8.7 to 6.6 K/W. Finally, reduction of the contact resistance between the N and P legs through the incorporation metal over the BiSbTe junction can further reduce device resistance, bringing expected device performance to 28 μW/cm^2/K^2.

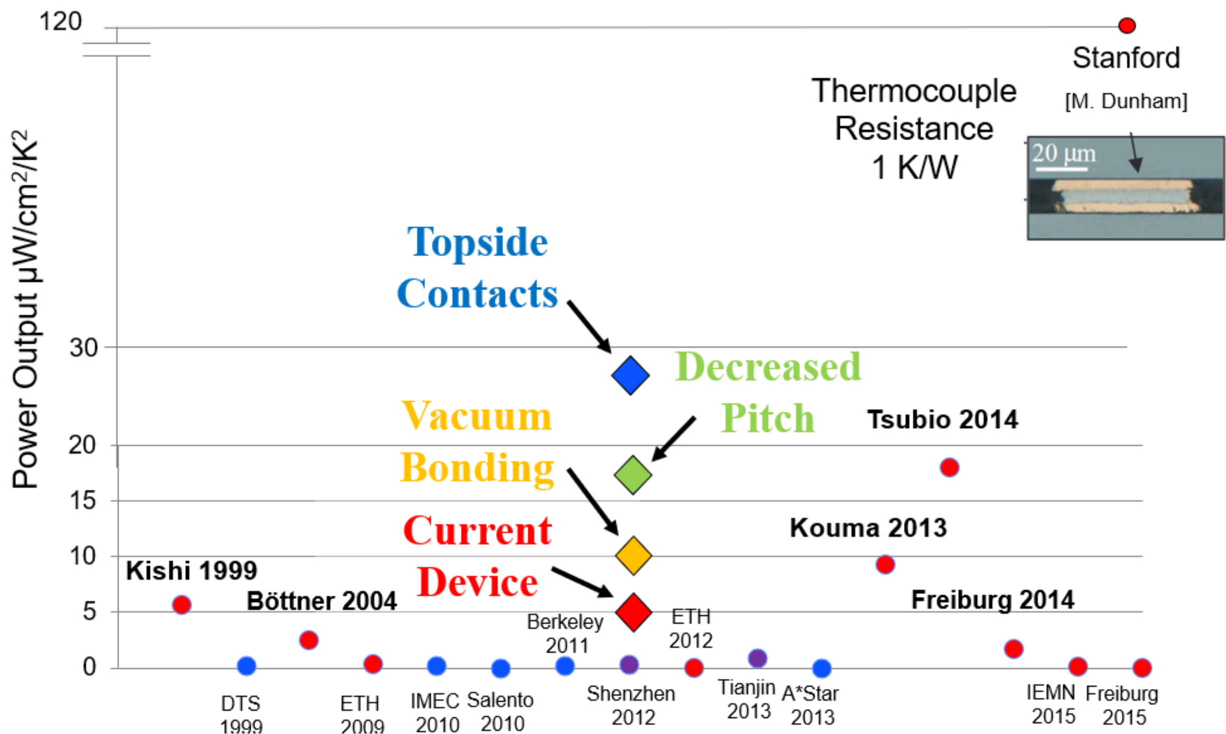


Figure 9-1: Current and potential device performance

Thus, through design changes alone, and without further material development, the performance of our generators can be improved from 4.9 to 28 μW/cm^2/K^2. At this point, the performance of our generator design becomes competitive with the traditional thin film designs such as the 120 μW/cm^2/K^2 reported by Dunham [15]. This is due to the greater thermocouple resistance of the high aspect devices. As seen in figure 8-22, the larger thermocouple resistance of these devices makes them less susceptible to the thermal impedances of the μTEG system. For realistic heatsink junction resistances of >5 K/W, the improved high aspect design with an initial FoM of 28 μW/cm^2/K^2 but a thermocouple resistance of 4.7 K/W will outperform a traditional thin-film design with a higher FoM of 120 but a lower thermocouple resistance of 1 K/W (Fig. 8-22).

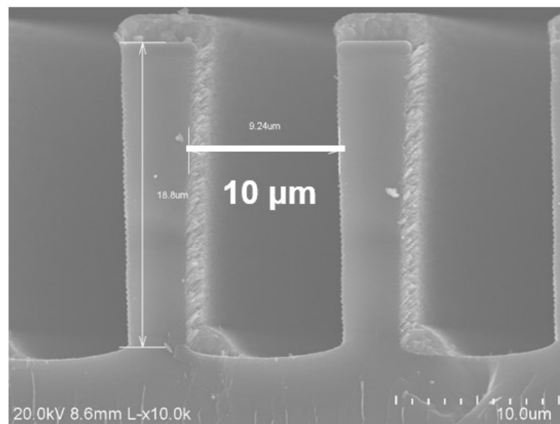


Figure 9-2: 10-µm pillar spacing limit. Below this limit, the contact resistance of the thermoelectric film at bottom of the trench reduces device performance due to smaller areas.

Future Work

Beyond the steps mentioned in the previous section, further investigation into the underlying mechanisms responsible for the sidewall Bi_2Te_3 and Sb_2Te_3 grain growth is necessary to improve the quality of the thermoelectric films used in the presented structures. Possible experiments include varying substrate angles and growing vertical films on epitaxially deposited seed layers

or seed layers deposited previously in the planar configuration. Additionally, amorphous film deposition followed by annealing should be investigated as a potential method to improve the film properties. If the performance of the vertical thermoelectric films can be improved enough to match the properties of films deposited on planar surfaces, the performance of the presented μTEG can be improved to 72 $\mu W/cm^2/K^2$, making the device outperform the μTEG with the highest reported FoM by more than a factor of two given an external thermal resistance of 4.6 K/W (Fig. 8-22).

Methods to reduce the resistance of the Bi_2Te_3 and Sb_2Te_3 connection should be investigated. These methods include traditional Au contacts between the two films or ion implantation directly into the BiSbTe junction. The formation of Au contacts over the top of the pillar structures require further development of high-aspect patterning techniques while ion implantation would require high energies in excess of 10 MeV to reach the entirety of the junction.

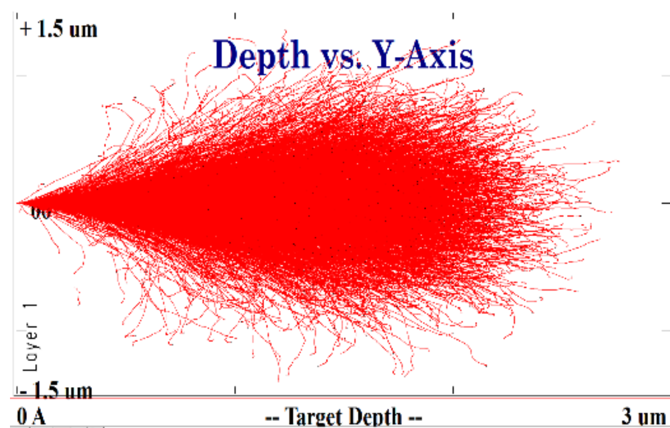


Figure 9-3: Penetration depth of Au ions into Bi_2Te_3 at 10 MeV. Simulated using SRIM.

On the design side, the limits on the density of the scaffold should be explored. Changing the angle of the Bi and Te source with respect to the sidewall surface can create extremely dense thermoelectric leg-pairs (Fig. 9-2).

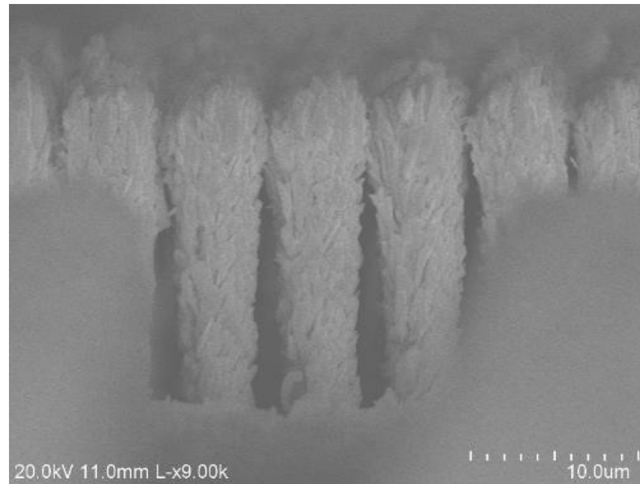


Figure 9-4: Dense thermoelectric legs

Such a device could exhibit extreme packing densities and fill factors. Additionally, the sidewall surface of such devices could be utilized for contacts rather than the planar surface of the presented generators, further increasing area efficiency (Fig. 9-2). Such a device may require unaligned bonding methods to avoid alignment tolerance limitations. This method may be a refinement of the thermal epoxy cap attachment process in Chapter 7.4.

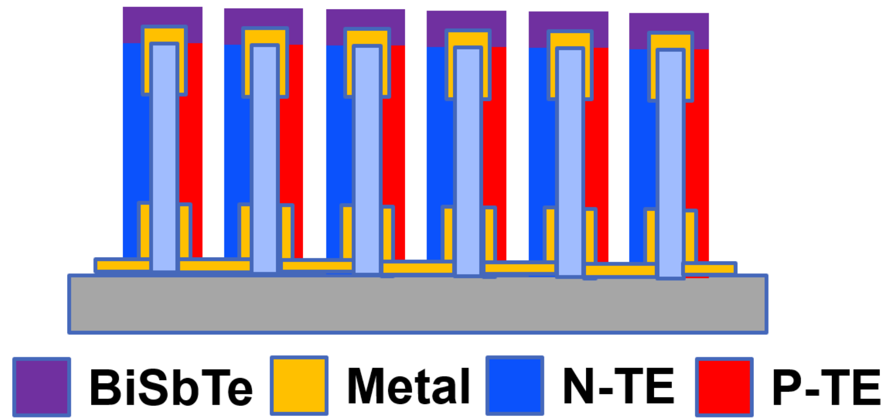


Figure 9-5: Ultra-dense Vertical thermoelectric generator.

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