Solution-Processed Amorphous Oxide Semiconductors for Thin-Film Power Management Circuitry

by

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To my parents and my beautiful wife

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Abstract

Thin-film electronics has opened up new applications not achievable by wafer-based electronics. Following commercial success in displays and solar cells, the future industry sectors for thin film devices are limitless, and include novel wearable electronics and medical devices. Such new applications enabled by human-size electronics have been widely investigated, but their potential use in power-management circuitry has been seldom addressed. The key strengths of thin-film electronics are that they can be deposited on various substrates at a large-area scale, and they can be additively deposited on existing device layers without degrading them. These advantageous features can be used to overcome the current barriers facing silicon (Si) electronics in power-management applications. Namely, thin film electronics can be used to directly deposit circuits including power harvesters on RFID tags to reduce the current tag cost based on Si IC. Furthermore, they can be directly heterointegrated with Si chips to enhance their voltage handling capability. Finally, thin film electronics can be deposited onto solar cell arrays to improve efficiency by managing partial shading conditions.

Among thin-film materials, we explore the scope of solution-derived amorphous oxide semiconductor (AOS) due to its high carrier mobility, wide band-gap, and in-air deposition capability. In this thesis, we push the boundaries of AOS by (i) developing an air-stable, ink-based deposition process for high-performance amorphous zinc-tin-oxide semiconductor. We choose a deposition process based on metal-organic decomposition, such that the film properties are independent of relative humidity in the deposition ambient, enabling future large-area roll-to-roll processing. (ii) Second, by exploiting *in situ* chemical evolution, namely reduction and

oxidation, at the interface of zinc-tin-oxide and various metal electrodes (primarily Pd, Mo, and Ag), we intentionally manipulate the electrode contact properties to form high-quality ohmic contacts and Schottky barriers. We explain the results based on competing thermodynamic processes and interlayer diffusion. (iii) Third, we combine these techniques to fabricate novel devices, namely vertically-conducting thin-film diodes and Schottky-gated TFTs, and we investigate the impact of the contact formation process on the resulting device physics using temperature-dependent current-voltage measurements. (iv) Finally, we demonstrate the use of these devices in several novel thin-film power electronics applications. These circuits include thin-film RFID energy harvesters, thin-film heterointegrated 3D-IC on Si chip for voltage bridging, and thin-film bypass diodes for future integration on solar cells to improve efficiency under partial shading conditions.

Chapter 1 Introduction

1.1 The opportunities of thin-film power electronics

Today, 40% of the worldwide energy consumption is in the form of electric energy where the generated electric energy undergoes several transformations before it is consumed. These transformations can be efficiently processed by power electronics through means of electronic switching devices, called power devices. These power devices play a key role in electric power conversion, which occurs widely in the generation, storage, and distribution cycle of electric energy. Historically power devices have been based on silicon (Si) technology, which has achieved numerous device innovations (including structural revolution from planar to trench structures in MOSFETs, and the introduction of IGBTs). These Si devices have successfully dominated the power device market, especially in the low and medium power range, but today, their performance has reached the theoretical limit.

Increasing demand for higher-performance power devices has led to the search for new materials that overcome the limit of Si. To date, extensive research and development has been undertaken to explore for new materials such as silicon carbide (SiC), gallium nitride (GaN), and gallium oxide (Ga_2O_3). These materials have been targeted due to their superior material properties including high carrier mobility and wide bandgap, that enable power devices to accomplish high-power and high-frequency applications. While these materials have superior performance-wise dominance over other materials in the power device area, they pose major fabrication challenges. First, they are not amenable to mass production and require multi-billion dollar fabrication facilities, imposing a barrier to low-cost fabrication. Second, they are not

scalable over large area and are not capable of hetero-integration (i.e., deposition on different materials). Although these conditions might be manageable when fabricating discrete power devices or isolated power management ICs to be integrated with other components separately, these characteristics can severely limit their application to low-cost and large-area electronics. Large-area electronics is promising for the future semiconductor industry and thus the need for materials compatible with large-area compatible and capable of additive-integration remains [1].

Large-area electronics (LAE) is generally defined as integrated device arrays or circuitries with a size exceeding tens of centimeters. The initial work on LAE has centered on displays and photovoltaics, as these are fundamentally area-intensive applications. However, over the last two decades, the scope of applications envisioned for LAE has expanded dramatically [1]. To name a few examples, LAE includes stretchable electronic skins, electronic textiles, flexible RFID tags, flexible solar cells and displays, x-ray imagers, which can be implemented over numerous niche applications, such as medical, wireless, sensing, flexible, and ultrathin applications. Despite the long-standing attraction of flexible human-size electronics, no industrial commercially successful technology has evolved to date. One of the main reasons for this delay is likely the difficulty in achieving an independent power management scheme for LAE. LAE, as all other electronic systems, requires electric power that needs to be harvested, stored, and distributed properly. For example, for a fully isolated e-skin, not only should the pressure sensor/actuator array be established on a stretchable substrate, but it should also be integrated with power harvester, battery, and power management circuitry to operate on its own. While there is on-going research toward flexible solar cells, piezoelectric materials, and thin-film batteries for power harvesting and storage in future LAE, power management schemes have been

rarely investigated. Thus, there is not yet an agreed-upon approach to integrate power management circuitry with functional devices in LAE.

LAE imposes serious restrictions on material selection, which makes single crystalline materials mentioned above (and therefore, high-quality power devices) difficult to use. LAE is achieved by depositing and patterning electronic devices over large area, while limiting overall fabrication cost. These two requirements raise the need for different type of materials: materials that have large-area deposition capability, low-cost deposition methods, easy access to hetero-integrations, and strong durability to mechanical flexibility. While c-Si, SiC, GaN, and Ga_2O_3 are strong candidates for high-performance power devices, their crystallinity prevent their use in LAE application. To integrate these high-quality power devices on LAE, there may be two approaches. One is to grow these crystalline materials via thin-film deposition on low-cost substrates, but the strain effects coming from lattice mismatch limit film growth. Their crystallization requires high temperature, preventing additive-integration capability. Mechanical bending of these films also has detrimental effects to their crystallinity and electrical properties, leaving them vulnerable to mechanical flexibility, which is of critical importance in LAE. The other approach is to make devices on the substrate of these materials, but high-quality substrates for SiC, GaN, and Ga_2O_3 themselves are currently prohibitively expensive, and making devices on isolated wafers require additional dicing/packaging/attachment process for hetero-integration. For these reasons, numerous publications on LAE have attached Si CMOS power management ICs for demonstration instead, as Si CMOS is currently mass-produced. In the same manner, however, these ICs are not strictly flexible-compatible and integrating numerous IC on flexible substrates [2] requires an additional pick-and-place process and packaging steps, which can be costly.

Developing new types of semiconductor materials that are capable of both large-area deposition and additive integration, and using them for power managing applications can be a game changer in the future of LAE. Such materials are usually referred as "thin-film" materials, as the materials are grown in thin-film on heterogeneous substrates, rather than being grown as bulk wafers. Their ability to be deposited on various substrates on a large area scale can pave the way for novel power electronics for new LAE applications. First, future autonomous LAE requires the subsystems of LAE in thin layers (e.g., solar panel layer, pressure sensor array layer, display layer, and etc.), to be piled up and integrated in a layer-by-layer configuration [3]. In this scenario, each thin layer will need its own power conversion scheme (i.e., AC-DC and DC-AC conversion for power transfer between layers, and DC-DC power converter for voltage stabilization), which requires thin-film power electronic components, rather than bulky packaged ICs. Second, thin-film power electronics can also be widely exploited in future RFID tags. Currently based on Si technology, the fabrication cost of RFID tag is dominated by the costs of separate packaging of Si IC and its attachment on RFID antenna [1]. To reduce the cost of RFID, instead of using a packaged Si IC, one can deposit thin-film circuitry directly on a tag with the antenna, at a large-area scale for mass production. Such an innovation would have a critical impact on the future RFID market. Third, thin-film electronics can be used to continue the increase of device density of Si CMOS, which has stagnated in the recent years due to the challenges in further device scaling in Si-based technology [4]. Instead of two-dimensional scaling, the additive integration capability of thin-film electronics provides a new method to increase device density by three-dimensional device layer stacking [5]. Depositing thin-film electronics on low-voltage, miniaturized Si CMOS wafers can be especially beneficial when thin-film electronics can be used for high-voltage efficient power management [6]. Lastly, solar

cell arrays also may benefit from hetero-integration of thin-film devices in terms of power management. Recently, extensive research has been done on flexible solar cell arrays [7]. Being flexible, these novel photovoltaic arrays are exposed to partial shading conditions. Integrating one bypass diode per one solar cell can prevent partial shading issues and effectively manage power harvested from the solar cells [8]. This integration may be easily achieved by large-area, additive integration of thin-film diodes on top of the solar cell array.

1.2 Amorphous oxide semiconductor for thin-film power electronics

Due to the strict material specifications for LAE, materials that do not require high crystallinity, namely polycrystalline, amorphous, or organic semiconductors come into play for thin-film electronics. However, for polycrystalline thin-film materials, the mechanical stability, film smoothness, and spatial uniformity of composition are frequently less than what is desired for high-performance LAE, and the films require expensive crystallization and doping processes. These challenges can be mitigated by amorphous semiconductors, but most covalent semiconductors in amorphous phase exhibit extremely poor electrical properties (e.g. amorphous hydrogenated silicon shows μ_e of < 1 $cm^2V^{-1}s^{-1}$ compared to > 80 $cm^2V^{-1}s^{-1}$ for polycrystalline silicon [9]) due to lattice disorder present in this covalently-bonded material. Organic semiconductors are being widely explored for LAE, but their electrical properties are often even worse than amorphous Si and show extreme environmental instability.

An attractive choice to overcome the weaknesses of these materials is to use amorphous oxide semiconductors (AOSs). While AOSs are structurally amorphous, they still offer good electrical properties. Beginning with Hosono's work in 2004, investigations of AOS, such as amorphous indium gallium zinc oxide (a-IGZO) and amorphous zinc tin oxide (a-ZTO), have

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gained momentum [10]–[12]. The superior electrical properties of these AOS compared to other candidates for LAE comes from their unique conduction band dispersion. Their conduction band minimum is composed of spherical ns-orbitals of metal cations, the overlap of which is minimally affected by lattice disorder (Figure 1.1(a)). Given this property, oxides in the amorphous phase often exhibit electron mobility comparable to that of single crystalline oxides (μ_e of 10 – 30 $cm^2V^{-1}s^{-1}$ [13]), and have superior charge carrier mobility compared to a-Si and organic semiconductors [10]. The high mobility allows devices to operate at higher efficiency and frequency (Figure 1.1(b)).

Such high carrier mobility comes along with other important features for LAE, such as large area processibility, substrate agnosticism, mechanical flexibility, film smoothness, and composition uniformity, thanks to disordered crystal structure in AOS. Due to these benefits, AOS has successfully dominated commercial LAE markets such as active-matrix display backplanes [14]. Moreover, its exploitation for other novel LAE applications such as x-ray imagers [15] and RFID tags [16], [17] are being actively pursued. Among these benefits of AOS, substrate agnosticism is of specific interest because it enables novel heterogeneous integration. Heterogeneous integration most commonly refers to the intimate placement and connection of components made using different materials and processes on top of a single substrate to provide enhanced functionality. Due to the fact that the top film properties are weakly dependent on the substrate underneath, AOS can allow additive integration of thin-film electronics on existing devices. The existing devices underneath are not limited to novel LAE devices; they can extend to conventional devices such as back-end-of-line silicon CMOS, for further functionality diversification. Due to these reasons, hetero-integration of thin-film circuitries based on AOS

TFTs on top of active elements made of different materials, have been reported previously, including on GaN high-electron-mobility transistor (HEMT) [18] and Si CMOS [19].
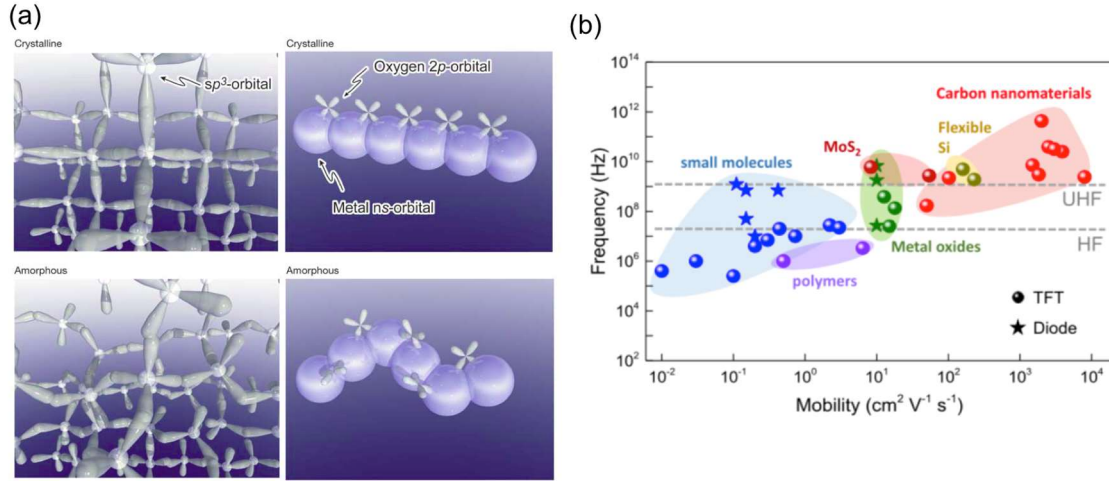
Figure 1.1 High carrier mobilities obtained from amorphous oxide semiconductor (a) Schematic orbital drawings for the carrier transport paths in crystalline and amorphous semiconductors. The left two figures are drawn for a covalent semiconductor, Si, and the right two figures are drawn for metal oxide semiconductors, reprinted with permission from ref. [10]. (b) A comparison of rectifiers made with various materials, from ref. [20]. The proportionality between material mobility and operation frequency of rectifier is noticeable, where metal oxides show promising mobilities.

Despite the promises of AOS, for certain devices, such as photovoltaics, pressure sensors, or LEDs, a-Si and organic semiconductors may be better choices. Even so, when it comes to choosing the best power device material among LAE-compatible materials, AOS remains the strongest candidate. To evaluate a potential strength of new material for power device application, the figure-of-merit used as general rule-of-thumb is Baliga's figure-of-merit (BFOM), which is the product of electron mobility (μ_e), the dielectric constant (ε_r) and the cube of critical electric field (E_c^3). μ_e is closely related to the conduction loss of the power device, and E_c indicates voltage handling capability of a material, as E_c is defined as the maximum electric field that the material can withstand without breaking down. The E_c of a material is generally higher for wider band gap (E_g) materials. This fact drives the extensive investigations, mentioned previously, into SiC, GaN, and Ga_2O_3, all of which have wide E_g. (Table 1.1) Not only is the

electron mobility the largest for AOS among the other candidates for LAE such as a-Si and organic semiconductors, but the bandgap of AOS is also high (~3.0 eV), making the material semi-transparent. Given these properties, exploring AOS as a material candidate for power devices for future LAE is of significant academic and industrial importance.

Table 1.1 Comparison of relevant semiconductor properties, from ref. [13], [14], [21]–[25]							
Material properties	**c-Si**	**a-Si:H**	**ZnO**	**GaN**	**Ga$_2$O$_3$**	**4H-SiC**	**AOS**
Bandgap (eV)	1.12	1.7-1.9	3.3	3.4	4.6	3.3	~3.0
Relative dielectric constant	11.8	11.8	8.75	10.6	10.2	9.7	11.5-13.8
Electron mobility (cm^{2}V^{-1}s^{-1})	1400	<1	226	5300	100-300	1000	10-30

1.3 The motivation for vertical thin film device

Due to these advantages of high carrier mobility and wide bandgap, AOS has already been widely commercialized for high resolution and large area display backplanes, including in the iPad Pro, OLED TV, and MS Surface Pro 4 [14]. However, most of the investigations so far were centered on thin-film transistors (TFTs) for the switching element of display backplanes [13], [26]. The basic TFT operation is similar to that of a conventional MOSFET, where a conductive channel is formed at the surface of the semiconductor at the interface with a gate insulator by application of a voltage to a gate electrode. TFTs are so named since the semiconductor layer deposited on the substrate is usually much thinner than one micrometer. Figure 1.2 shows the typical device configurations for TFTs [27]. Common among these configurations is that the current conduction through channel layer occurs laterally through a narrow cross-sectional area and across the long channel length.
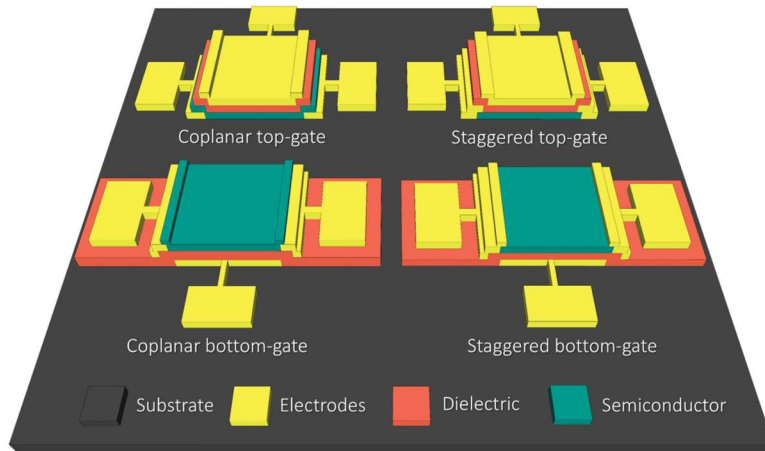
Figure 1.2 Typical device configurations for lateral TFTs, reprinted with permission from ref. [28]. When these TFTs are switched on, the on current flows through the thin semiconductor (the green layer) laterally. Therefore, the current conduction in lateral TFTs occurs through a long (typically in μm) and thin (typically in tens of nm) channel layer.

However, this lateral structure has critical limitations in terms of conduction loss and operation frequency. For efficient power handling, the device needs to support a large amount of current with little resistance when it is in the on-state. This minimizes the Joule loss coming from conduction. For a given material, these conditions can be met structurally when the current conduction length is short, and the area through which the conduction occurs is wide. However for lateral structures, this becomes difficult to achieve as thin film thickness dramatically narrows the area for current flow. A further limitation is that achieving a short conduction length is constrained by the resolution of the patterning/alignment process. Equally important to addressing conduction loss is achieving high operation frequency. The operation frequency of a device is often attributed to the carrier transit time, which is the time it takes for the carrier to transport from one metal electrode to the other. A shorter transit time is desirable for higher device operation frequency, and this can be achieved by high mobility or short conduction length. Since mobility is largely determined by material selection, a shorter conduction length can reduce this transit time and increase the device operation frequency. However once again, obtaining a short conduction length in lateral structures is limited by the resolution of photolithography.

To summarize, lateral thin-film devices pose challenges to achieving large area and short length of conduction, both of which are important features for low loss and high frequency operation. We should note here that several attempts have been made to mitigate these limitations of lateral structures in AOS TFTs so far. First, in order to increase the area of conduction, inter-digitated source and drain electrodes have been used to increase the effective width [29]. Second, high-resolution photolithography [30], self-alignment approaches [31], and vertical deposition of the channel [32] have been used to shorten the conduction length. However, inter-digitated source and drain or vertical deposition of the active layer requires thin metal electrodes with poor current-handling capability, and high-resolution photolithography or self-alignment approaches increase fabrication complexity and cost. Moreover, the current conduction area in all of these approaches is still limited by film thickness.

The device design window to achieve large conduction area and short conduction length can be expanded dramatically by using a vertical device structure. In vertical structures, the conduction length is determined by the thin film thickness. As film thickness can be easily controlled at the nanometer scale, short conduction lengths that are difficult to achieve for lateral devices, become easily achievable in vertical structures. In terms of conduction area, the area for current flow in vertical structure is limited only by the area of the electrodes, not the film thickness. As spatial composition uniformity is one of the well-known strengths of AOS, a large area for high current flow is expected to be easily achievable once a vertical structure is obtained. Additionally, in the vertical configuration, the two high current-carrying electrodes can be located on opposite sides of the wafer, which enables the use of thick metal electrodes and avoids transport of current through thin metal fingers. Given these characteristics, vertical thin-film device structures can enhance operation frequency and reduce conduction losses with the

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help of short conduction length and large conduction area. Therefore, in order to push the current limit of lateral AOS devices for future power devices to be implemented in large-area electronics, investigation should be made of vertical AOS device structures.

1.4 The motivation for in-air fabrication of thin film

Aside from the geometric improvements that can be achieved by a vertical structure, a novel deposition technique can lead to a dramatic reduction in LAE fabrication cost. Of particular interest for low-cost LAE are solution-based processes for AOS. These processes enable AOS to be deposited in air instead of in vacuum as in conventional vacuum deposition techniques. Once fully commercialized, these processes are expected to be a game-changer in the LAE semiconductor industry, as it eliminates the need for expensive equipment costs typical of vacuum deposition, thus dramatically lowering economic barriers to utilizing AOS for LAE. In addition, solution processibility opens up new possibilities for inexpensive patterning, such as ink-jet printing techniques, which can significantly decrease material costs by reducing material waste and avoiding additional patterning steps [33], [34]. Ink-jet patterning for AOS TFT is currently being investigated by multiple groups with promising results [34]–[36]. Lastly, in-air deposition capability with solution process may enable roll-to-roll processes, which would achieve deposition areas larger than what is achievable by vacuum techniques.

One of the major obstacles for solution-processed AOS is consistently achieving high-quality films over a wide range of process conditions. Conventional vacuum deposition is performed in a controlled environment and thus exhibits a high level of control and consistency in film stoichiometry and quality. In contrast, solution deposition of AOS is typically done in air, with thermal annealing used to drive chemical structure evolution. In this process, the

thermodynamics and kinetics of film formation can be greatly influenced by the ambient environment. Importantly, the choice of annealing temperature and humidity in air during deposition have been shown to affect the electrical and chemical characteristics of solution-deposited films [37]–[41]. Therefore, the advantageous capability of AOS deposition in air has also been its weakness, due to challenges in achieving uniform film properties. To achieve the full benefit of AOS deposition in air, these challenges must be overcome.

1.5 Thesis objectives

The main goal of this thesis is to push the boundaries of solution-processed AOS further and develop novel applications for AOS in thin-film power electronics. We first develop a solution process method to resolve the present limit of in-air deposition of AOS. Then, we analyze the undergoing chemical evolution during our process for process optimization. So far, the majority of literature on AOS were based on conventional TFTs with a metal-insulator-semiconductor structure. Developing other structures such as vertical thin-film diode (V-TFD) or Schottky-gated TFTs can further enhance the capabilities of AOS-based thin-film electronics, but this requires a high-quality Schottky contact. Therefore, we develop Schottky contacts using our in-air deposition method. We first start by developing Schottky contacts with a bottom metal electrode, thereby making bottom-Schottky V-TFDs. To understand the resulting contact properties, we analyze the interface chemistries between various bottom electrodes and AOS that occur during the solution process. Using the resulting metal-semiconductor junctions, we characterize bottom Schottky V-TFDs with high-voltage and high-frequency operation. We demonstrate its application in wireless energy harvester for future monolithic integration of RFID tags. Next, in order to enhance further the quality of the Schottky-contact, we develop a

new Schottky contact using a top metal electrode. This leads to the highest device performance of AOS V-TFD and Schottky-gated TFT reported to-date. Using these devices, we demonstrate their application in 3D monolithic integration of power electronic on top of low-voltage, miniaturized Si CMOS ICs. This paves the way for future functionality diversification in electronic devices for More-than-Moore. Lastly, the application of V-TFD on large-area solar cell array for integration of individual bypass diodes is demonstrated via simulation. This opens new opportunity for large-area power management by thin-film electronics.

1.6 Thesis overview

In Chapter 2, we develop a solution-based, in-air deposition process of AOS that is stable over ambient conditions. After establishing a solution process method that can induce air-stable reactions, we investigate the effect of annealing conditions on film properties. Thermodynamics during film formation play a crucial role. With optimized annealing conditions, we experimentally confirm that our solution process can deposit high quality thin-film in air across a wide process window. In Chapter 3, we use this process to fabricate AOS V-TFD using bottom Schottky contacts. We find that chemical evolution of the film during solution process causes interactions with the bottom metal upon annealing, which needs to be exploited to obtain the desired contact properties. Utilizing these interface chemistries, we fabricate two V-TFDs with bottom Schottky contacts, using palladium and molybdenum. In Chapter 4, to determine the source of the non-ideal switching behaviors from these V-TFDs, we analyze their charge transport mechanisms. This analysis combined with the material characterization in Chapter 3 suggests that due to multiple reactions and interdiffusion at the interface of the bottom electrode and semiconductor, obtaining excellent switching characteristics using V-TFD with a bottom

Schottky contact structure may be challenging using solution process. In Chapter 5, we show that for a power rectifier, a Pd V-TFD exhibits severely low voltage handling capability and instability. After analyzing the source of these weaknesses, we find that Mo V-TFD, on the other hand, has greatly improved power rectifier features. These strengths are experimentally confirmed by demonstrating wireless energy harvesting using commercial RFID reader and antenna coupled to a full-wave rectifier made with Mo V-TFDs. In Chapter 6, we explore a new V-TFD structure to further enhance its switching performance. Based on our conclusion that obtaining high-quality, bottom-Schottky contacts is difficult using our in-air process, we develop high-quality top-Schottky and bottom-ohmic contacts. These contacts allow us to make V-TFDs and Schottky-gated TFTs with excellent switching performance. Thanks to the performance improvements, these devices are used to demonstrate applications of thin-film power electronics on Si CMOS IC or on solar cell arrays. The thesis concludes with Chapter 7, which summarizes the major contributions and findings of this work. Several recommendations for future research are suggested at the end of the thesis.

Chapter 2 Air-stable fabrication of high quality thin-film

2.1. Introduction

Amorphous oxide semiconductors (AOS) have superior charge carrier mobility compared to amorphous silicon and organic semiconductors [10], are transparent to visible light, and can be deposited on various substrates on a large-area scale. They can also be deposited using a variety of methods, including solution-based processes. Solution processes are of particular interest, because of their potential for in-air deposition and inexpensive deposition/patterning techniques [33], [34]. In general, a solution process includes the following steps: (1) solution/ink preparation that involves dissolving precursors in solvents, (2) ink deposition onto the desired surface and/or locations, (3) film formation that involves evaporating a solvent and inducing a chemical reaction/physical transformation [42], [43]. Each of these steps has a significant influence on the resulting film quality. Thus, the proper material and deposition method should be chosen carefully.

Among the material candidates for AOS, we investigate amorphous zinc tin oxide (*a*-Zn-Sn-O or *a*-ZTO). *a*-ZTO is an attractive AOS compared to other strong candidates, namely *a*-IGZO and *a*-IZO, because *a*-ZTO has an indium-free composition. Indium is relatively scarce and has become expensive due to increasing demand for indium tin oxide as a transparent conductor [44]. Unlike indium, both zinc and tin are earth-abundant. For indium-containing AOS, indium is an important element that enables good electrical conduction. Thanks to the large and spherical 5s orbital of indium, a conduction band dispersion is achieved between

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neighboring metal ions. In case of ZTO, the 5s orbital of tin contributes to this dispersion mechanism [45] and replaces the need for indium, without sacrificing electrical performance. In addition to having an indium-free composition, a-ZTO can be readily formed with an amorphous morpohology, which is critical for large-area compatibility. ZTO maintains its amorphous phase up to 650°C [46] thanks to the high co-solubility between ZnO and SnO_2 [47], which is enabled by similar ionic radii of Sn^{4+} (0.071 nm) and Zn^{2+} (0.074 nm). These features have led to considerable interest in a-ZTO, which has been targeted as a promising ternary amorphous oxide semiconductor for large area electronics, and thus is our choice of material.

After a target material is selected, the ink must be chosen for solution processing. The choice of precursors and solvents that make up the ink determine its chemical evolution during deposition, and it affects important features of the solution process. The entire solution process should be environmentally-friendly and provide a wide process window in terms of ambient environment conditions. Conventional hydrolysis-based sol-gel processes, however, mostly use precursors that can generate harmful byproducts and it has been shown that their film properties can change dramatically depending on the ambient humidity during deposition. Specifically, many conventional hydrolysis-based sol-gel solution processes use nitrate [48], [49], chloride, or sulfide precursors [41], which can create toxic byproducts. More importantly, the resulting metal oxide films showed significant change in film conductivity [49], electron mobility [49], film thickness [41], and even crystallinity [38] when the air humidity during deposition was changed. This constitutes a major limitation for LAE. Thus, a solution processes that can overcome this limitation is needed. Compared to these hydrolysis-based sol-gel processes, metal-organic decomposition (MOD) is known to be less sensitive to water during deposition [40]. The MOD process takes place when acetate precursors are used, and does not generate toxic byproducts. In

the case of *a*-ZTO, various solution preparation methods have been developed using various precursors such as chlorides [50]–[52], acetates [53], [54], and nitrates [55], as well as various organic solvents [55]. However, the advantages of using acetate precursors has not yet been experimentally demonstrated. Thus, we investigate acetate precursors for our *a*-ZTO ink. Given the MOD route, it is expected that using these acetate precursors will achieve more consistent film properties over a wide humidity range during deposition. A further expected benefit is that unlike nitrate-, chloride-, or sulfide- compounds, acetate-based inks do not create harmful byproducts upon annealing, making their use more feasible for large-area, in-air deposition.

For deposition, we choose a multi-layer spin-coating method (Figure 2.1 (a)). Spin-coating is one of the solution deposition techniques that are currently available, including spin-coating, inkjet printing, spray-coating, dip-coating, screen printing, blade coating and gravure printing [42], [56]. Spin-coating remains the easiest way to deposit film over wide area with uniform thickness. Multi-layer spin-coating deposition is used to increase film thickness [33] and reduce pores and defects [57]. Typically multi-layer films are annealed briefly after coating each layer and annealed again after deposition of the final layer, typically for a longer time. We refer to these steps as pre-annealing and post-annealing, respectively.
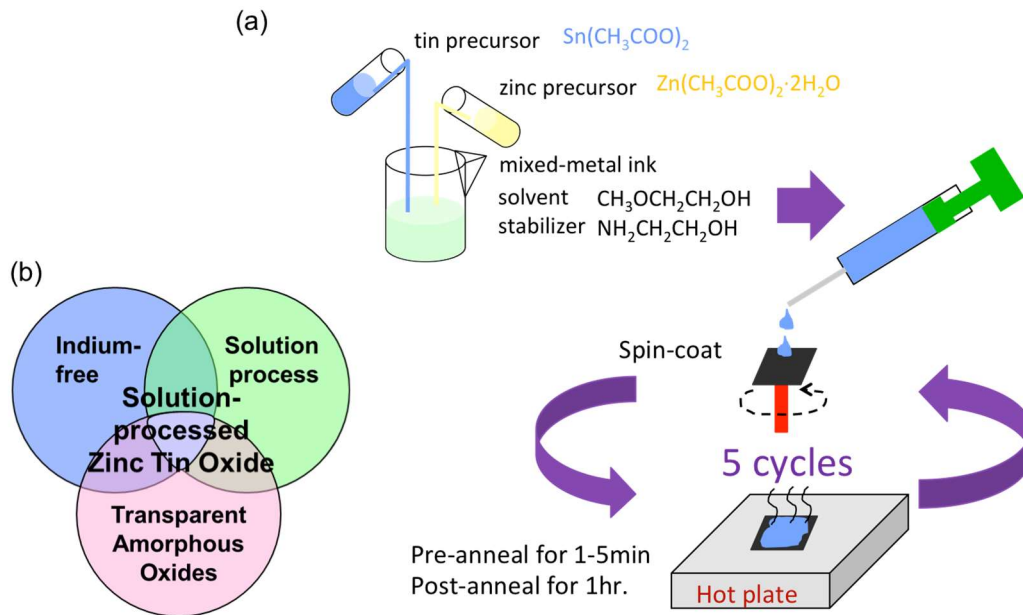
Figure 2.1 (a) Schematic of multiple layer spin-coating with pre-annealing and post-annealing for our solution process and (b) solution processed *a*-ZTO for our material choice of AOS.

Based on these considerations, we choose a multi-layer spin-coated *a*-ZTO film for our target solution-processed AOS thin film (Figure 2.1 (b)). Our main interest here is to confirm that by using acetate precursors, a high quality thin film can be fabricated over a wide range of ambient humidity levels, so that a truly low-cost and large-area-compatible deposition method can be realized in the near future. At the beginning of this chapter, we establish the thermodynamic understanding of chemical evolution occurring during our solution process by studying *a*-ZTO films annealed in different temperatures. This understanding will inform our explanation of an interface engineering technique at metal-semiconductor junctions, described in Chapter 3. We will then characterize the chemical composition and thickness of our *a*-ZTO films via means of XPS, FTIR, EDS, SEM, and Dektak. Along with Hall measurements on bulk films, thin-film transistors will be fabricated and measured for our *a*-ZTO films to fully characterize their electrical properties. Correlations between material and electrical properties will be

established. Most importantly, we deposit our thin films over wide range of humidity with the help of our customized glovebox, and characterize their TFT performance. This is done to experimentally confirm the wide process window over humidity levels during acetate-based *a*-ZTO deposition.

2.2. Experimental Section

2.2.1 Sample fabrication

The *a*-ZTO layer was deposited by spin-coating a 0.5 M metal acetate precursor solution. Zinc acetate dihydrate (99.999%, $Zn(CH_3COO)_2 \cdot 2H_2O$, CAS number 5970-45-6, Sigma-Aldrich), and tin (II) acetate ($Sn(CH_3COO)_2$, CAS number 638-39-1, Sigma-Adrich) were dissolved in 2-methoxyethanol (99.8%, $CH_3OCH_2CH_2OH$, CAS number 109-86-4, Sigma-Aldrich) and 0.5 M ethanolamine ($\geq$99.5%, $NH_2CH_2CH_2OH$, CAS number 141-43-5, Sigma-Aldrich), with a zinc to tin ratio of 7:3. The solution was stirred for 12 hours and filtered through a 0.22-μm syringe filter during dispensing, followed by spin-coating at 3000 rpm for 30 seconds. During spin-coating, the ambient relative humidity (RH) and temperature were controlled at approximately 35% and 21°C. Five layers were spin-coated onto the samples. Each spun layer was pre-annealed at either 250°C for five minutes or 520°C for one minute at controlled humidity and temperature. After spin-coating the final layer, the samples were post-annealed at 520°C for one hour. The annealing environment was fixed at approximately 13% RH and 45°C.

To precisely control the temperature and humidity of ambient air during spin-coating and annealing, we use a custom glovebox (LCBT-201, LC Technology Solutions, Inc., Salisbury, MA). As shown in Figure 2.2, the glovebox has automated air temperature and humidity control.

Air temperature is controlled using a water chiller (ThermoFlex TF25-T1, Thermo Fisher Scientific, Waltham, MA) connected to a 2 kW heat exchanger/fan along with a separate heater and recirculating fan. By setting the water chiller to a temperature below the desired set point, the heat exchanger can cool the internal air against the heat load provided by the hot plates and heater inside the glovebox. RH is controlled via injection of dry air (Zero grade compressed dry air, Cryogenic Gases, Pittsfield, MI) balanced with operation of an ultrasonic humidifier containing deionized water. Both RH and air temperature are measured using *in situ* sensors and are controlled using a custom-built control box. In addition, we use a secondary enclosure, internal to the glovebox, to protect samples on hot plates from drafts due to the heating and cooling fans. The secondary enclosure also has the effect of creating a hotter and drier environment for pre- and post-annealing, due to the operation of hotplates inside the enclosure. In addition to the permanently-installed sensors that are linked to the controller, we use portable temperature and RH sensors to verify and log the spinning and annealing environmental conditions.
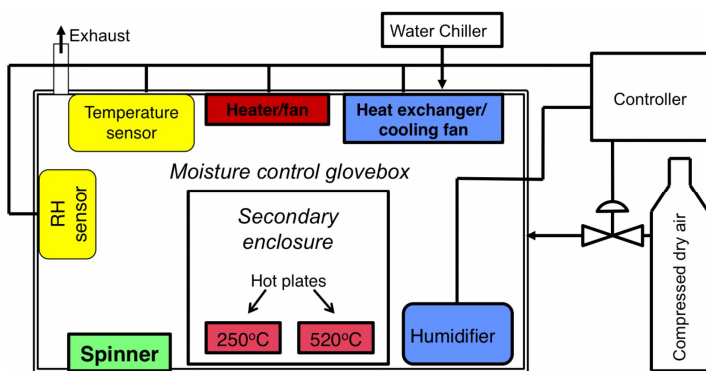
Figure 2.2 Schematic of the custom glovebox. The controller senses the internal temperature and provides automated PID control to achieve the desired set point using a heater/recirculating fan and/or a cooling fan connected to a 2 kW heat exchanger supplied by an external water chiller. Likewise, the internal RH is sensed and controlled using a humidifier and/or dry air flow. The secondary enclosure contains hot plates for annealing. Reproduced from Ref. [58] with permission from The Royal Society of Chemistry.

For comparison of different pre-annealing temperatures, Corning Eagle XG glass was used as a substrate, cleaned with acetone and isopropanol. For samples made for chemical

composition analysis such as XPS, FTIR, and EDS, *a*-ZTO thin film deposition was performed, as described above, on clean glass. For TFT fabrication, a bottom-gate, top-contact structure was used. On top of a clean glass substrate, 100-nm Mo was sputtered using a Kurt J. Lesker Lab 18 tool to form the gate electrode. A 55-nm Al_2O_3 gate dielectric was deposited using atomic layer deposition (Oxford OpAL ALD) at 250°C. The Al_2O_3 thickness was confirmed using spectroscopic reflectometry (Nanometrics Nanospec 6100). After *a*-ZTO deposition, the ZTO layer was patterned by wet etch using a hydrochloric acid and nitric acid solution to isolate each transistor. Source and drain electrodes of 100-nm Mo were then sputtered to enable good ohmic contact to *a*-ZTO [59], and were patterned with lift-off.

For comparison of different ambient humidity, heavily-doped *n*-type Si (n^{++}-Si (Sb), 0.01-0.02 Ω·cm, <100>) with 100-nm thermally grown SiO_2 was used as the substrate. Then, the *a*-ZTO deposition and TFT process was followed to produce bottom-gate top-contact transistors, including the deposition of molybdenum gate metal and alumina gate insulator, as explained above. The glovebox controller was used to vary ambient humidity during *a*-ZTO deposition and annealing.

2.2.2 Chemical composition analysis and electrical measurements

XPS was measured using Kratos Axis Ultra XPS. A monochromatic Al x-ray source (8 mA and 14 kV) was used with a spot size of 300×700 μm^2, pass energy of 20 eV, and step size of 0.1 eV. The Kratos charge neutralizer system was used for all analyses. For depth profiling, argon ion sputtering was used with energy of 5 kV and an ion source extractor current of approximately 90 μA, which results in an estimated sputtering rate of 2-3 nm/min. XPS measurements were performed between 240-sec sputtering intervals. To confirm that we

sputtered all the way down to the glass substrate, we continued sputtering until the Si 2p peak was observed at least five times in a row. The XPS curves were analyzed using CasaXPS software. The curve energies were calibrated using the C 1s peak at 284.5 eV as a reference, to account for charge compensation. Measured O 1s curves were deconvoluted into three Gaussian–Lorentzian curves using a linear background. The positions of the three deconvoluted peaks correspond to oxygen atoms in the fully oxidized surroundings (M-O), those in oxygen deficient regions (V_O), and those in H_2O and -OH groups (M-OH). These are located at 530.1 ± 0.1 eV, 531.1 ± 0.1 eV, and 532.1 ± 0.2 eV, respectively [40], [60]–[62]: Zn $2p_{3/2}$ and Sn $3d_{5/2}$ peaks were fitted using Gaussian-Lorentzian curves with a linear background, centered at 1021.8 ± 0.2 eV and 486.2 ± 0.2 eV, respectively. Finally, the areas under each XPS peak were calculated by integration to estimate atomic compositions of Zn, Sn, M-O, V_O, and M-OH. The conversion from area to atomic concentration was done using relative sensitivity factors developed for the Kratos XPS. XPS relative sensitivity factors are taken from CasaXPS_kratos.lib, available online at http://www.casaxps.com/kratos/

FTIR was measured using an Agilent uFTIR Microscope (Cary 620) and Analytical Bench (Cary 670). Film thickness measurements were done using a Dektak 6M surface profilometer. Energy-dispersive spectroscopy (EDS) was done using an Hitachi SU8000 In-line FE-SEM.

Current-voltage (*I-V*) characteristics of TFTs were measured using an HP4156A semiconductor parameter analyzer. Room temperature measurements were performed in ambient air, in the dark. Temperature-dependent *I-V* measurements were taken in the dark, in vacuum, from 77 K to 300 K using a Lakeshore Cryotronics TTPX cryogenic probe station. Multiple devices were measured on each sample. The *I-V* data shown here are representative of typical

device performance. Hall effect and van der Pauw measurements were conducted using an HL5500PC Hall measurement system at room temperature in air, with additional van der Pauw measurements made using an HP4156A semiconductor parameter analyzer with high resolution source measure units. The measurements were performed on un-gated samples made on glass substrates with sputtered molybdenum corner contacts.

2.3. Achieving a wide process window for in-air deposition

2.3.1 Chemical evolution during solution process

The choices of metal precursors and organic solvents guide the chemical reactions that induce metal oxide bond formation. Our main goal is to explore chemical reactions that are consistent in ambient air. The use of chlorides, nitrates, and alkoxides as metal precursors usually results in sol-gel [37], [38], [60], [40] or combustion synthesis [39], [63], [55]. These processes are quite sensitive to the ambient environment, as sol-gel processes typically follow hydrolysis and condensation, and combustion requires complex redox reactions. In contrast, carboxylate precursors, which includes the acetates used here, are known to follow a MOD route [64]–[66] involving direct thermal decomposition of organic precursors to form the target metal oxide. Despite its potential for more in-air stable deposition of thin film, the MOD process for AOS has been studied in a limited fashion. *Kim et al.* [66] performed thermal gravimetric analysis and differential scanning calorimetry (TGA-DSC) alongside FTIR in order to observe decomposition and dehydroxylation occurring in the formation of *a*-IGZO from zinc acetate, gallium nitrate and indium nitrate ink. *Jeong et al.* [53] performed TGA-DSC on an acetate-based ZTO solution identical to that used here. They observed significant weight loss below

250°C followed by heat flow from 300 to 500°C, similar to that seen by *Kim et al.* [66], indicating similar decomposition and dehydroxylation mechanisms. However the exact formation mechanisms and intermediates for each process are still not fully understood.

In order to verify the effect of each mechanism on film properties, we performed XPS analysis on two different *a*-ZTO films. One sample consisted of a multi-layer *a*-ZTO film that was annealed at 250°C for five minutes for each layer. Based on TGA-DSC [53], 250°C anneals should evaporate the solvent and thermally decompose the precursors, without dehydroxylation. The other sample consisted of a multi-layer *a*-ZTO film that was annealed at 520°C for one minute for each layer, and after final layer deposition, annealed at 520°C for one hour. The annealing temperature of 520°C is chosen to facilitate complete dehydroxylation after decomposition, without crystallizing the film [53]. XPS was performed after sputtering for 1800 sec to interrogate the bulk film, and the O 1s and C 1s peaks were analyzed. The C 1s region is devoid of peaks for both samples (Figure 2.3(a)), illustrating that pre-annealing at 250°C is sufficient to reduce carbon to below the XPS detection limit of approximately 0.1 at%. In contrast, the O 1s spectra are notably different for 250°C vs. 520°C processes (Figure 2.3(b)). After 250°C pre-annealing, a significant amount of oxygen remains in the form of hydroxides (M-OH). Annealing at 520°C facilitates conversion of these hydroxides into metal-oxygen bonds (M-O). Therefore, we conclude that 250°C anneals cause the removal of carbon-containing compounds and formation of hydroxides (i.e, Zn-OH and Sn-OH), while 520°C anneals promote metal-oxygen bond formation (i.e., Zn-O and Sn-O). These reaction steps correspond with the TG-DSC results from *Jeong et al.* [53] and the decomposition/dehydroxylation mechanisms suggested by *Kim et al.* [66]. Therefore, we deduce the following mechanisms for our solution process:

$$Decomposition: Zn(CH_3COO)_2 \cdot 2H_2O + Sn(CH_3COO)_2 + \tfrac{9}{2}O_2 \rightarrow Zn(OH)_2 + Sn(OH)_4 +$$

$$2CH_3COOH + 4CO_2 + H_2O \tag{2.1}$$

$$Dehydroxylation: xZn(OH)_2 + (1-x)Sn(OH)_4 \rightarrow Zn_xSn_{1-x}O_{2-x} + (2-x)H_2O \tag{2.2}$$
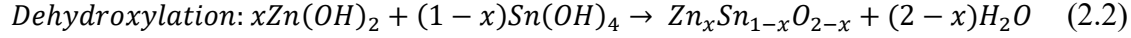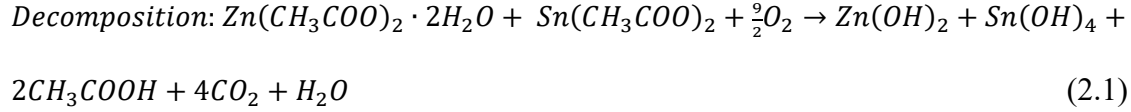
The exact products and intermediate stages of decomposition summarized by Equation (2.1) are not yet known. However, our XPS data of Figure 2 support the formation of zinc and tin hydroxides at temperatures below or at 250°C, and subsequent dehydroxylation (Equation (2.2)) at a temperature between 250°C and 520°C, resulting in ionically-bonded metal oxide thin films.

The spontaneity of a given reaction can be quantitatively described by its standard Gibbs free energy ($\Delta G_{rxn}{}^o$). Since the standard molar enthalpies of formation ($\Delta H_f{}^o$) of ZTO will vary according to its stoichiometry, we calculate $\Delta G_{rxn}{}^o$ for the dehydroxylation of zinc and tin hydroxides, $Zn(OH)_2$, $Sn(OH)_2$, and $Sn(OH)_4$, into their oxide counterparts, ZnO, SnO, and SnO_2, using reference values of $\Delta H_f{}^o$ and standard molar Gibbs free energy of formation ($\Delta G_f{}^o$) [67], [68]. The dehydroxylation reactions and corresponding $\Delta G_{rxn}{}^o$ values with respect to temperature are shown in Figure 2.3(c). The Gibbs free energy of dehydroxylation is strongly dependent on temperature, indicating the need for a relatively high annealing temperature for effective metal-oxygen bond formation.
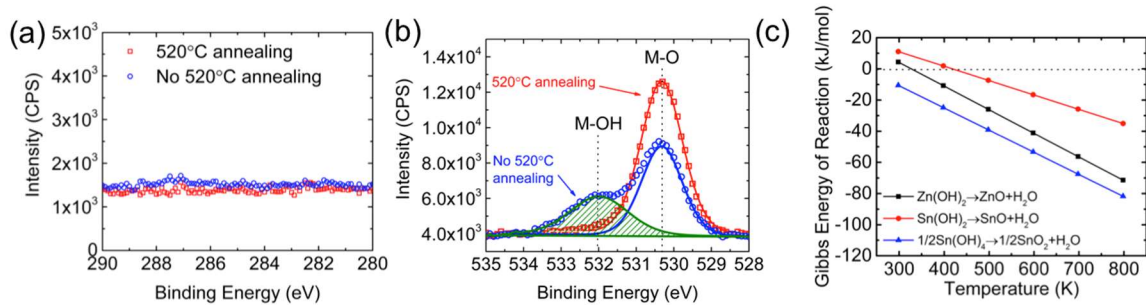
Figure 2.3 Dehydroxylation in our solution process. XPS analysis on (a) C 1s peaks and (b) O 1s peaks for samples pre-annealed at 250°C (open blue circles) and pre- and post-annealed at 520°C (open red squares). Solid lines indicate the deconvoluted curves obtained by fitting the experimental data (symbols). The green hatched area shows the contribution of metal hydroxides (M-OH) in films annealed at 250°C. (c) Chemical equations and corresponding standard Gibbs free energy for dehydroxylation reactions, $\Delta G_{rxn}{}^o$, of $Zn(OH)_2$, $Sn(OH)_2$, and $Sn(OH)_4$. The reaction

equations are normalized by the number of oxygen atoms in the metal oxide, so that ΔG_{rxn}^o represents the free energy per oxygen atom in the metal oxide. Reproduced from Ref. [58] with permission from The Royal Society of Chemistry.

2.3.2 Electrical properties of *a*-ZTO thin films

As shown in the previous section, we can see that temperature affects the spontaneity of MOD processes and therefore the annealing temperature will alter the chemical composition of the thin film dramatically. For multi-layer spin-coating, there exists two annealing steps: pre-annealing and post annealing. There have been several studies on the effect of post-annealing temperature on metal oxide film properties, coupled with extensive efforts to achieve low temperature solution processes for compatibility with flexible substrates [37], [40], [39], [69], [54], [70], [71]. However, the effects of pre-annealing temperature rarely have been investigated [50]. Pre-annealing often is performed at a lower temperature than post-annealing with the intention of evaporating the solvent without inducing metal-oxide bond formation [50], [57], [72], [73], but its impact on film properties has not been well-established. Since there is no thermal-budget benefit for choosing the pre-annealing temperature to be lower than the post-annealing temperature, the choice of pre-annealing temperature should be driven by a clear understanding of its effect on film properties.

According to the thermodynamic calculations and XPS results of Section 2.3.1, a post-annealing temperature of 520°C is sufficient to fully convert metal hydroxides into stoichiometric metal oxide [54]. Thus, with a fixed post-annealing temperature of 520°C, we change pre-annealing temperature to examine the effect of the pre-annealing step on film properties. To do so, we fabricate two films, one using pre-annealing at 250°C for five minutes (hereafter referred to as LT sample, for low-temperature) and the other using pre-annealing at

520°C for one minute (hereafter referred to as HT sample, for high-temperature). After depositing five layers, both samples were post-annealed at 520°C for one hour.

Hall measurements were obtained for the two ZTO films deposited on glass. The Hall mobility (μ_H) of ZTO film deposited with HT TFT annealing conditions was 5.53 cm^{2}V^{-1}s^{-1} and the free electron concentration was 4.6×10^{16} cm^{-3}. The LT films, in contrast, had a sheet resistance $10^7 \times$ greater than that of the HT films and a very low Hall voltage, below the measurement limit of our equipment: The measured sheet resistance, R_{sh}, of the LT sample was 1.32×10^{13} Ω/□ (measured with an applied voltage of 30 V), while that of HT sample was seven orders of magnitude smaller, 2.14×10^6 Ω/□ The high sheet resistance observed in LT films is attributed to charges present at the surface of ZTO (possibly due to oxygen absorption) that form a depletion region within ZTO film. Surface depletion has been observed previously in metal oxide films [74], [75]. When the film is thin and is not gated, this depletion region may extend across the majority of the ZTO film, making it highly resistive. To investigate whether surface depletion is affecting our sheet resistance results, we made LT samples with different thickness by spin-coating five-layer, ten-layer, and twenty-layer films, and performed van der Pauw measurements on these samples. The thickness of these films were measured to be ~180 nm, ~360 nm, and ~790 nm, respectively, using DekTak profilometry. While their XPS depth profiles revealed almost identical chemical composition (Figure 2.4 (a)), the R_{sh} of the five-layer LT sample was one hundred times higher than that of twenty-layer LT sample (Table S1 in Figure 2.4), which cannot be explained by the four-fold difference in film thickness. Therefore, this result shows that low conductivity of LT sample is due to the dominance of surface depletion, happening due to ambient.
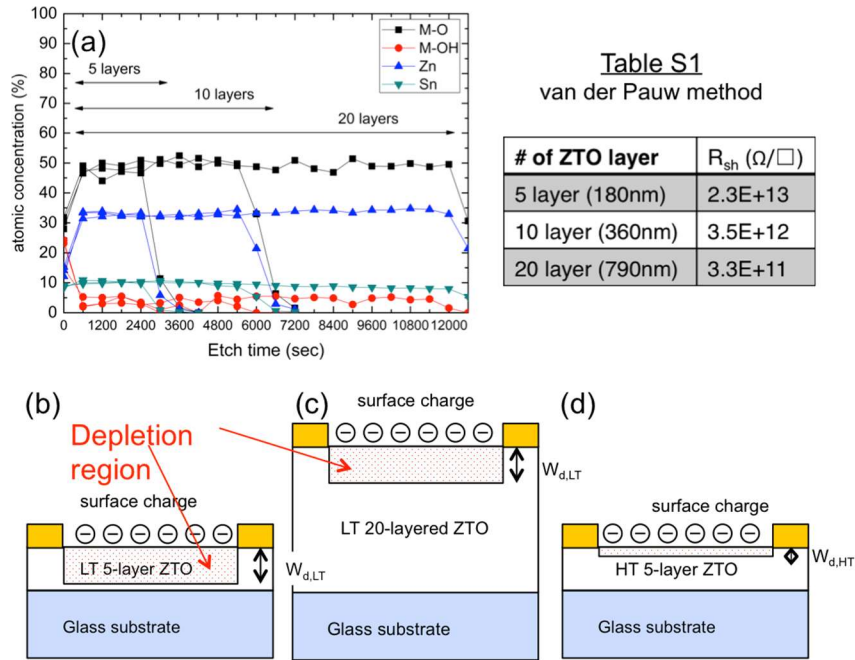
Figure 2.4 The effect of surface depletion in LT samples (a) XPS depth profile of LT samples with different numbers of spin-coated layers (5, 10, and 20 layers). V_O is excluded for clarity. **Table S1** shows film sheet resistance measured using the van der Pauw method with sputtered molybdenum for ohmic contact. (b), (c) and (d) show schematics of depletion region width (W_d) for ZTO thin films with (b) five layers deposited under LT conditions, (c) twenty layers deposited under LT conditions, and (d) five layers deposited under HT conditions. Reproduced from Ref. [58] with permission from The Royal Society of Chemistry.

2.3.3 Electrical properties of *a*-ZTO thin film transistors

Hall measurements on un-gated (and un-passivated) thin films suffer from surface depletion, which prevents assessment of electrical properties of the non-depleted film. Rather, the main interest in AOS as n-type semiconductor layer is due to its charge transport properties when electrons are accumulated, and this requires the film to be gated. Moreover, as introduced in Chapter 1, most of the devices made out of AOS use a lateral TFT structure. Thus, measuring and characterizing TFTs made out of our *a*-ZTO will provide better understanding of its charge transport properties as well as enable its fair comparison with other reported AOSs. With this background, bottom-gate top-contact TFTs are fabricated with the same conditions as the LT and

HT samples above (Figure 2.5 (a)). These devices will be hereafter be referred to as LT TFT and HT TFT, respectively.

Performance of TFTs is often evaluated by field-effect (FE) mobility using an analytical expression based on the following gradual-channel approximation:

$$I_{DS} = \frac{W}{L} \mu_{FE} C_{ox} \left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2} \right], \tag{2.3}$$

where C_{ox} is gate capacitance, μ_{FE} is FE mobility, and V_{th} is a pseudo-constant called threshold voltage. μ_{FE} often refers to linear mobility (μ_{lin}), which is retrieved as $\mu_{FE}(V_{GS}) = g_m(V_{GS}) \frac{L}{W C_{ox} V_{DS}}$. This comes from the fact that at very low V_{DS} (i.e., in linear region), Equation (2.3) reduces to $I_{DS} \approx \frac{W}{L} \mu_{FE} C_{ox}[(V_{GS} - V_{th})V_{DS}]$.

Equation (2.3) is derived from calculating the drift current of the mobile charge collected at the channel layer due to the capacitance dependence on the gate voltage, V_{GS}. In other words, the charge accumulated at the active channel layer at given point x, $Q_{acc}(x)$, can be expressed as follows (neglecting the body effect):

$$Q_{acc}(x) = C_{ox}(V_{GS} - V_{th} - V_{CS}(x)), \tag{2.4}$$

where V_{CS} is the channel voltage. If the on-current at point x, $I_{DS}(x)$, can be characterized by the drift of these accumulated charges, then $I_{DS}(x) = W Q_{acc}(x)v(x)$, where $v(x)$ is the drift velocity. For a constant band mobility, μ_o, the drift velocity, $v(x) = \mu_o E_x(x)$, where $\int_0^L I_{DS}(x)dx = W \int_0^L Q_{acc}(x)v(x)dx$. Thus, for continuous current throughout the channel, this expression reduces to

$$I_{DS} = \frac{W\mu_o}{L} \int_0^L Q_{acc}(x)E_x(x)dx. \tag{2.5}$$

This becomes

$$I_{DS} = \frac{W\mu_o}{L} \int_0^{V_{DS}} C_{ox}(V_{GS} - V_{th} - V_{CS}(x))dV_{CS}, \qquad (2.6)$$

which, following integration, leads to Equation (2.3).

Transfer curves were measured on LT TFTs and HT TFTs and their field-effect mobilities were calculated according to Equation (2.3). Our solution-processed a-ZTO TFT showed significant improvement with higher pre-annealing temperature (Figure 2.5 (b)). The subthreshold swing (SS) is also calculated as the minimum value of $\partial V_{GS}/\partial log_{10} I_{DS}$ in the subthreshold region [76]. As Table 2.1 shows, μ_{FE} for HT TFTs compared to LT TFTs showed an approximately eight-fold increase from 0.75 cm^{2}V^{-1}s^{-1} to 5.91 cm^{2}V^{-1}s^{-1} and the SS was decreased from 1.37 V/decade to 0.44 V/decade. As a result, while the two devices show similar off-current, which is dominated by gate leakage current, the on-current and on/off current ratio increased dramatically, by a factor of approximately 70. We note the similarity of the Hall and TFT mobility values for HT films. Higher V_T observed in LT TFTs might also be correlated with the surface depletion that occurs in the LT films.
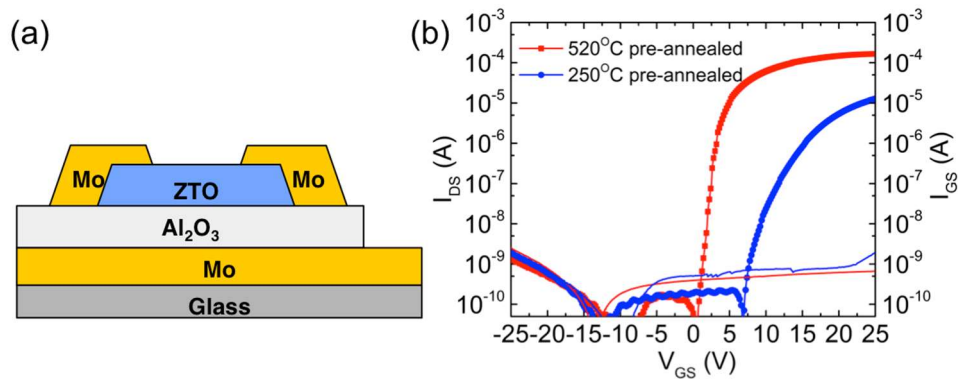
Figure 2.5 (a) Device schematic of bottom-gate top contact TFT structure. (b) Representative transfer characteristics of TFTs made using different pre-annealing conditions, with W/L = 500 μm/50 μm and V_{DS} = 1 V. The solid lines with symbols indicate drain current (I_{DS}) while thin solid lines without symbols show gate leakage current (I_{GS}). Reproduced from Ref. [58] with permission from The Royal Society of Chemistry.

Although electron mobilities were measured at room temperature, a more thorough analysis of AOS charge transport properties requires temperature-varying electrical measurements. Equation (2.3) is derived under the assumption that all of the charges at channel layer accumulated by V_{GS} consist of free mobile carriers that travel via band-like transport, characterized by a band mobility, μ_o. In other words, the FE mobility experimentally extracted from $\mu_{FE} = \frac{\delta I_{\mathrm{DS}}}{\delta V_{\mathrm{GS}}} \cdot \frac{L}{W C_{ox} V_{\mathrm{DS}}}$ assumes that the entire charge induced as $C_{ox} \delta V_{\mathrm{GS}}$ contributes to δI_{DS}. However, this assumption does not hold for materials that have deep-level trap states. For such materials, a significant amount of the charge accumulated by V_{GS} (i.e., Q_{acc} in Equation (2.4)), becomes trapped due to these states, and therefore cannot contribute to I_{DS}, as was assumed in Equation (2.5). If Equation (2.4) and Equation (2.5) were valid, μ_{FE} extracted from Equation (2.3) would be μ_o as was shown in Equation (2.6) which would then exhibit a decrease at higher temperature due to increased phonon scattering. In contrary, the FE mobility extracted from AOS TFTs often shows an increase at higher temperatures. This thermal activation behavior of μ_{FE} observed for AOS TFTs has been explained by various models, which include the trap-limited conduction (TLC) and percolation models. Here, we study the TLC model that was introduced by *Nathan et al.* [77]–[80], which is also referred to as multiple trap-and-release (MTR) by other authors [81] (Figure 2.6). This model explains the discrepancy between μ_{FE} and μ_o with the change of free mobile charge (Q_{free}) and trapped charge (Q_{trap}) with respect to E_F, leading to $\mu_{FE} = \mu_o \frac{Q_{free}}{Q_{free} + Q_{trap}}$.
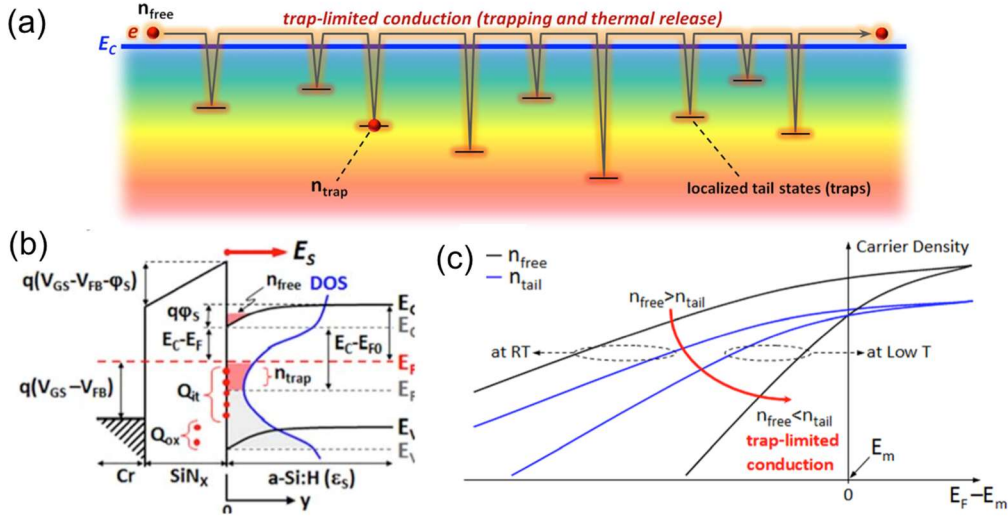
Figure 2.6 (a) Illustration of trap-limited conduction from ref. [80], (b) schematic of the accumulated charge (both n_{free} and n_{trap}) induced by V_{GS} from ref. [79], and (c) schematic of n_{free} and n_{trap} with respect to E_F for different temperatures from ref. [78].

Amorphous oxide semiconductor is generally known to have exponential tail states beneath the conduction band minimum (CBM) due to its amorphous nature. This is different from conventional semiconductors, which have shallow donor states that become fully ionized at room temperature (RT). The density of states (DOS) of such tail states can be expressed as

$$g_{tail}(E) = g_{tc} \exp\left[\frac{E-E_C}{kT_t}\right], \tag{2.7}$$

where E_C is energy level of conduction band minimum, g_{tc} is tail state density when $E=E_C$, and kT_t is the characteristic energy of tail state. Although these tail states of AOS are relatively shallow compared to other amorphous semiconductors such as a-Si, they can still act as deep-level trap states that do not fully de-trap electrons at low temperature. This is expressed as the characteristic energy of tail state, kT_t in Equation (2.7), being higher than the lattice thermal energy, kT. In such situation, the rise of Fermi level due to higher V_{GS} not only increases Q_{free} but also Q_{trap}. Therefore, while the accumulated charge due to V_{GS} in Equation (2.4) is equivalent to

Q_{free} + Q_{trap}, the charge that contributes to I_{DS} in Equation (2.5) is Q_{free}, excluding Q_{trap}. This leads to the invalidity of Equation (2.6).

When E_F is within the distribution of the tail states, the density of electrons trapped within the tail states (n_{trap}) can be calculated under the assumption that it can be approximated as electrons trapped below E_F, i.e.,

$$n_{trap}(E_F) = \int_{E_{F0}}^{E_F} g_{tail}(E)f(E) \ dE. \tag{2.8}$$

In order to solve this analytically, we define $u \equiv \exp\left[\frac{E-E_F}{kT_t}\right]$. Then, $n_{trap}(E_F) =$

$$\int_{E_{F0}}^{E_F} \frac{g_{tail}(E)}{1+\exp[\frac{E-E_F}{kT_t}]} \ dE = g_{tc}kT_t\exp[\frac{E_F-E_C}{kT_t}]g(u), \text{ where } g(u) \equiv \int_0^{\exp[\frac{E_C-E_F}{kT}]} \frac{1}{1+u^{T_t/T}} \ du.$$

Depending on the comparison between kT_t and kT, the solution of the above equation results differently. When $kT_t > kT$, $g(u) \approx \frac{\pi(T/T_t)}{\sin(\pi T/T_t)}$ and when $kT_t \gg kT$, $g(u) \approx 1$, which leads to

$$n_{trap}(E_F) \approx g_{tc}kT_t\exp[\frac{E_F-E_C}{kT_t}]. \tag{2.9}$$

When $kT_t < kT$, $g(u) \approx \frac{1}{2}\exp\left(-\frac{E_F-E_C}{kT_t}\right)\left\{\frac{2\ln(\exp\left(\frac{E_C-E_F}{kT_t}\right)+1)}{\exp\left(\frac{E_C-E_F}{kT_t}\right)}\right\}^{T_t/T}$ and when $kT_t \ll kT$, $g(u) \approx$

$\frac{1}{2}\exp\left(-\frac{E_F-E_C}{kT_t}\right)\exp\left(\frac{E_F-E_C}{kT}\right)$, which leads to

$$n_{trap}(E_F) \approx \frac{1}{2}g_{tc}kT_t(\frac{2(E_c-E_F)}{kT_t})^{kT_t/kT}\exp[\frac{E_F-E_C}{kT_t}] . \tag{2.10}$$

On the other hand, the density of free electrons, n_{free}, for given E_F can be calculated with Boltzmann approximation ($kT \ll (E_c-E_F)$):

$$n_{free}(E_F) = \int_{E_C}^{\infty} D_C(E)f(E) \; dE = N_C \exp\left[\frac{E_F - E_C}{kT}\right],$$ (2.11)

where N_c is the effective density of states. From 2D-Poisson's equation and Gauss law, we have

$$\frac{Q_{acc}}{\varepsilon_s} = \frac{C_{ox}(V_{GS} - V_{th})}{\varepsilon_s} = \sqrt{\frac{2q}{\varepsilon_s}\int_{E_{F0}}^{E_F}\{n_{free}(E_F') + n_{trap}(E_F')\} \; dE_F'}\;,$$ which gives the relationship

between E_F and V_{GS} by substitution using Equation (2.9) and Equation (2.11) [80]:

$$E_F - E_C \approx kT_t ln\left(\frac{C_{ox}^2(V_{GS} - V_T)^2}{2\varepsilon_s g_{tc}(kT_t)^2}\right).$$ (2.12)

Therefore, the FE mobility with respect to bias can be derived from plugging in Equation

(2.9), (2.11), and (2.12) in $\mu_{FE} = \mu_o \frac{n_{free}}{n_{free} + n_{trap}}$:

$$\mu_{FE} = \mu_o \left(\frac{N_C}{g_{tc}kT_t}\right)\left(\frac{C_{ox}^2}{2\varepsilon_s g_{tc}(kT_t)^2}\right)^{(l-1)}(V_{GS} - V_T)^{2(l-1)},$$ (2.13)

where $l = kT_t/kT$. This MTR model requires kT_t being larger than kT such that the thermal energy

alone cannot excite all the electrons in tail states above the CBM. This condition was taken into

account by using Equation (2.9) in the above derivations. In this case, the increase of kT leads to

the increase of the exponent l in Equation (2.13) and eventually leads to the increase of μ_{FE}. We

previously reported similar MTR behavior of our a-ZTO TFTs with different Zn:Sn ratios [54].

In conclusion, the exponential tail states occurring within AOS lead to thermal activation

behavior of FE mobility in AOS TFTs. We should note here that in addition to the multiple-trap-

and-release (MTR) [81], [82] model, which we have just explained, other models of AOS charge

transport have also been proposed including percolation [26], [83], and variable-range hopping

[52], [84]. Therefore, the exact charge transport mechanism(s) in AOS are still under

investigation. However, all of these models include the widely-reported phenomenon that the

extracted mobility of AOS is thermally activated, leading to the increase of TFT drain current with respect to temperature:

$$I_{DS} = I_0 \, exp(-E_A/k_BT), \tag{2.14}$$

where I_0 is a constant, E_A is an activation energy, k_B is the Boltzmann constant and T is the temperature [77], [85]. This thermal activation originates from trap states based on MTR model, and from a non-uniform conduction band (CB) as postulated in the percolation model.

Temperature-dependent current-voltage characteristics have been measured for both HT and LT TFTs. Our TFTs indeed follow Equation (2.14). Activation energies (E_A) were calculated as a function of V_{GS} by linearly fitting $ln \, (I_{DS}(V_{GS}))$ vs. $1/k_BT$ curves (Figure 2.7 (a)). The rate of change in E_A with respect to V_{GS} in the subthreshold region indicates how efficiently the quasi-Fermi level of a channel shifts with respect to the external gate bias [86], [87]. Low $|\partial E_A/\partial V_{GS}|$ values are often attributed to traps present either in the channel (N_t) or at the interface (D_{it}). In Figure 2.7 (a), $|\partial E_A/\partial V_{GS}|$ for the LT TFT, 22.9 meV/V, is significantly lower than that of the HT TFT, 106 meV/V, indicating that for our MOD process, higher annealing temperatures are effective at reducing trap state densities.

In addition, at high V_{GS} the E_A value for the HT TFT converges to a smaller value (~25 meV) compared to the LT TFT (~60 meV). The existence of trap states in the channel (i.e., N_t) can significantly reduce the effective electron mobility and increase its activation energy, $E_{A,\mu}$. Explaining Equation (2.14) by a temperature-activated change of effective mobility leads to:

$$\mu_{FE} = \mu_0 \, exp(-E_{A,\mu}/k_BT). \tag{2.15}$$

Once again, the MTR model incorporates the effect of trap states by describing the thermally-activated field-effect mobility shown in Equation (2.13) [85], [81], [88], [80]. Here, for comparison of different charge transport in LT and HT TFTs, we use Equation (2.15). Figure 2.7 (b) shows μ_{lin} with respect to inverse temperature for a HT and LT TFT. The μ_{FE} values follow Equation (2.15). Values for μ_0 and $E_{A,\mu}$ were extracted and are shown in Table 1. The HT TFT has a significantly larger μ_0 (14.0 cm^{2}V^{-1}s^{-1}) and smaller $E_{A,\mu}$ (24.7 meV) than the LT TFT (5.3 cm^{2}V^{-1}s^{-1}, 59.6 meV). (Because they are extracted in the on-state, well above threshold, the $E_{A,\mu}$ values are nearly the same as the E_A values extracted from I_{DS} at high V_{GS}.) According to the MTR (or TLC) model, the higher $E_{A,\mu}$ of the LT TFT indicates that its ZTO film contains a higher concentration of traps in the bulk than the HT TFT film. This is corroborated by the higher *SS* values observed for LT TFT compared to HT TFT, given that $SS=log_e10\times k_BT/q[1+q(tN_t+D_{it})/C_{ox}]$, where q is the elementary electric charge and t the channel thickness. Assuming that D_{it} is negligible compared to bulk traps, the N_t value extracted for the HT TFT is 4.16×10^{17} cm^{-3}eV^{-1}, much smaller than that for the LT TFT, 1.25×10^{18} cm^{-3}eV^{-1}. Therefore, it is reasonable to conclude that the large density of trap states in the near CB region of the LT TFT ZTO film leads to its poorer electrical performance compared to the HT TFT device.
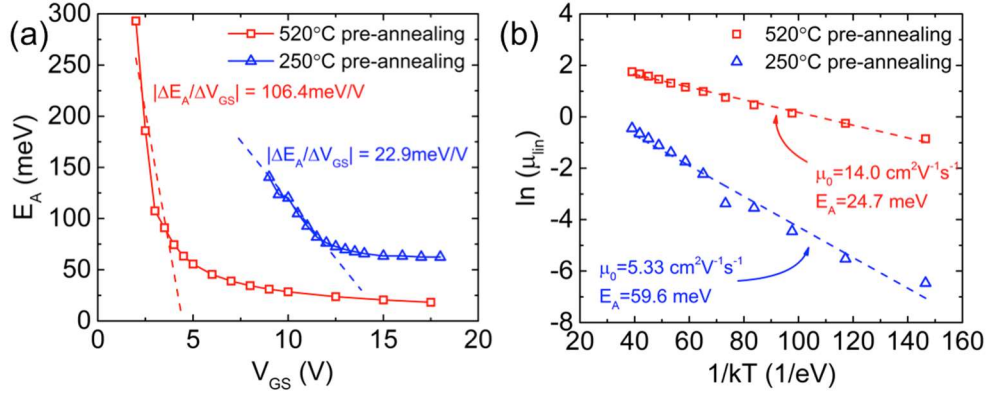
Figure 2.7 (a) Variations of activation energy (E_A) of the I_{DS} extracted from temperature-varying transfer curves for both devices. (b) Arrhenius plot of extracted linear mobility showing thermal activation behaviour. μ_{lin} is extracted from the above-threshold region (V_{GS} 3-8 V for HT TFT, and 12-17 V for LT TFT). In both (a) and (b), red squares refer to HT TFT and blue triangles refer to LT TFT. The dotted lines show linear fits to extract $\partial E_A/\partial V_{GS}$, and μ_0 and $E_{A,\mu}$, respectively. Reproduced from Ref. [58] with permission from The Royal Society of Chemistry.

Table 2.1 ZTO TFT performance comparison						
Pre-annealing conditions	Transfer characteristics			Temperature-dependent measurements		
	μ_{lin} (cm^{2}V^{-1}s^{-1})	On/off ratio	SS (V/decade)	$\|\partial E_A/\partial V_{GS}\|$ (meV/V)	μ_0 (cm^{2}V^{-1}s^{-1})	$E_{A,\mu}$ (meV)
LT TFT	0.75	2.79×10^4	1.37	22.9	5.3	59.6
HT TFT	5.91	1.97×10^6	0.44	106.4	14.0	24.7

2.3.4 Chemical composition of *a*-ZTO thin films

Chemical composition analysis. Previous studies of AOS have shown that changes in metal cation composition [89], [63], [90] and oxygen components [91]–[95] can affect the density of states and charge transport properties which ultimately affect device performance. In order to understand the origin of the trap states, N_t, and their relationship with pre-annealing conditions, we performed various measurements to study the chemical composition of the LT and HT ZTO films.

For these experiments, we deposited ZTO films on clean glass substrates using the LT and HT process conditions described above for TFTs. XPS depth profiles were performed until the Si 2p peak appeared repeatedly, indicating that we had reached the glass substrate. The

atomic concentration of oxygen components in LT and HT films are shown in Figure 2.8 (a) and

(b), respectively, based on analysis of the O 1s peaks. The top layers of the LT and HT ZTO

films (i.e., the first 2000 sec of sputtering) exhibit similar amounts of V_O and M-OH. As

sputtering proceeds deeper into the film (i.e., 3120-4320 sec of sputtering), V_O and M-OH

concentrations decrease in the HT sample. In contrast, in the LT sample the V_O and M-OH

concentrations remain uniform with respect to depth. For bottom-gate TFTs, in which

accumulation occurs at the bottom of the semiconductor film, XPS depth profile measurements

are critical to obtain accurate information about the chemical composition in the channel region.
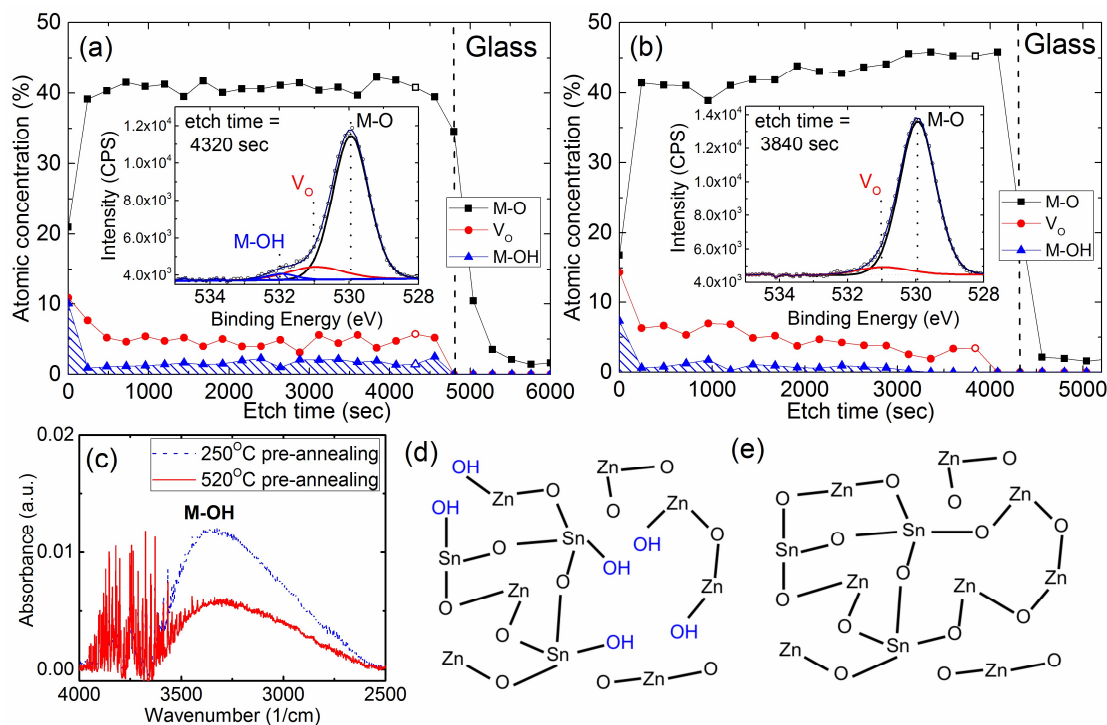
Figure 2.8 Atomic concentrations of oxygen components M-O, V_O, and M-OH obtained from XPS depth profiles of (a) LT and (b) HT samples. The insets show representative XPS data near the substrate, corresponding to the open symbols at ~4300 sec (a) and ~3850 sec (b). Vertical dashed lines indicate the location of glass substrate interface, as identified by appearance of the Si 2p peak. (c) FTIR measurement of LT and HT samples. Schematic illustrations of atomic structure of (d) LT samples and (e) HT samples. Reproduced from Ref. [58] with permission from The Royal Society of Chemistry.

In order to confirm the XPS results, we performed FTIR. The absorbance of OH-group stretching vibrations [96], [97] corresponds to a broad peak at wavenumbers of 3000-3500 cm^{-1}. As shown in Figure 2.8 (c), the absorbance in this region was more than twice as high for the LT sample compared to the HT sample. Absorbance is proportional to both concentration and sample thickness [98]. Surface profilometry measurements show that the LT and HT films have similar thickness of 160±10 nm and 140±10 nm, respectively. This minor thickness difference of ~14% was also observed as a ~11% difference in XPS sputtering time (4800 sec for LT sample and 4320 sec for HT sample). This small thickness variation cannot account for the large increase in absorbance of the LT sample compared to the HT sample. This difference must be due predominantly to a higher M-OH concentration occurring in films pre-annealed at low temperature. It is notable that the high M-OH concentration observed earlier after only a 250°C pre-anneal (Figure 2.3 (b)) is not fully eliminated even after a 1-hr 520°C post-anneal (inset Figure 2.8(a)). Thus we conclude that a sufficiently high pre-anneal temperature is critical to completing the dehydroxylation process.

As mentioned earlier, electron transport in amorphous oxide semiconductors occurs via empty *ns* states with short inter-cation distances [10]. A short inter-cation distance can be achieved in M-O-M, but not with M-OH, as one valence electron of oxygen is bonded with hydrogen instead of with a metal ion (Figure 2.8 (d) and (e)). For this reason, AOS films containing M-OH often exhibit poor electrical performance [96], [99]. In our TFTs, the channel/gate insulator interface occurs at the bottom of the AOS film, as shown in Figure 2.5 (a). From the XPS results shown in Figure 2.8 (b), the bottom of the HT AOS film shows no M-OH component, while the LT film shows a substantial M-OH contribution throughout the film. The dramatic enhancement of the HT TFT performance compared to that of the LT TFT is thus

partially attributable to the significant decrease in M-OH, especially at the bottom of the film near the gate dielectric.

For *a*-ZTO, the Zn:Sn ratio of the film has been shown to exert a critical influence on the film properties [53], [54], [89], [90], [95], [62]. Despite the fact that the same ink was used for both LT and HT samples, the films exhibit different metal cation stoichiometry. Figure 2.9 illustrates the Zn and Sn compositional depth profile obtained from Zn 2p$_{3/2}$ and Sn 3d$_{5/2}$ XPS peaks. EDS traces are shown in the insets. The Zn:Sn ratios obtained from XPS and EDS reveal that the LT sample has a higher Zn:Sn ratio (3.0±0.2 from XPS and 2.8±0.2 from EDS) compared to the HT sample (2.2±0.2 from XPS and 1.9±0.2 from EDS).
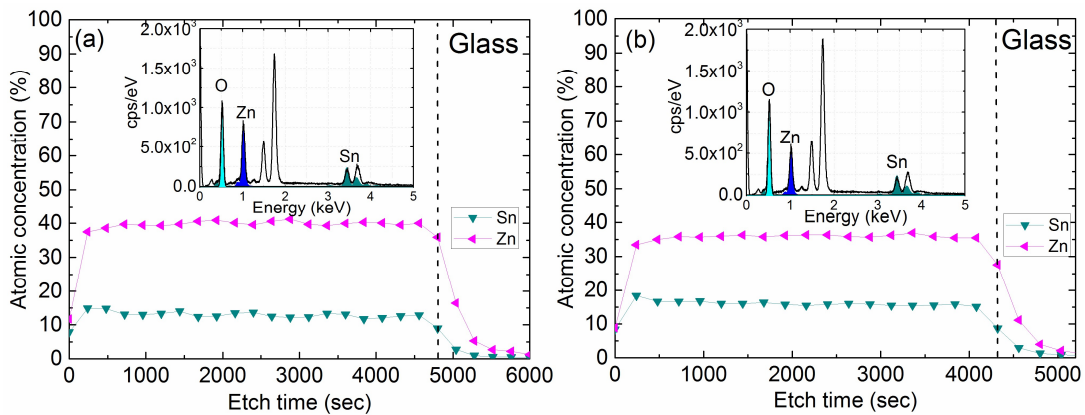
Figure 2.9 Atomic concentrations of Zn and Sn obtained from Zn 2p$_{3/2}$ and Sn 3d$_{5/2}$ XPS depth profiles in (a) LT and (b) HT samples. The vertical dashed lines show the location of the glass substrate, as detected by the appearance of Si 2p peaks. The inset figures show EDS traces for the same samples. The large peaks at ~1.5 and ~1.7 keV are due to aluminium from the chuck and silicon from glass, respectively. Reproduced from Ref. [58] with permission from The Royal Society of Chemistry.

The Zn:Sn ratios extracted from XPS and EDS of the LT sample are significantly higher than that of the prepared solution (Zn/Sn=2.3): the LT sample has enhanced zinc incorporation. In oxide alloys, larger spherical *ns* orbitals, such as those associated with 5s Sn^{4+} or In^{3+} compared to 4s Zn^{2+}, are postulated to have a higher degree of orbital overlap and increased conduction-band dispersion. This phenomena has been used to explain the trend that *a*-ZTO with

high Sn content has higher conductivity [90], [95] and higher TFT field-effect mobility [53], [62], [89]. Thus poor performance of LT TFT compared to HT TFT may also be due to the greater zinc incorporation during the LT process. The Zn:Sn ratio is reasonably uniform with depth in both samples despite the non-uniformity of oxygen components with respect to depth observed in the HT sample (Figure 2.8 (b)). For both samples, the Zn:Sn ratio obtained at the un-passivated surface (i.e., at etch time = 0 sec) is significantly different from that obtained in the bulk. This illustrates that the metal stoichiometry, as well as the magnitude of the oxygen components, cannot be accurately measured using surface XPS on unpassivated zinc tin oxide [60], [51]. Rather, depth-profile XPS measurements are needed to assess bulk film properties [62], [100], [101].

The exact mechanism by which a change in pre-annealing temperature leads to differences in film stoichiometry is difficult to conclude at this point and requires further study. However, we propose the following mechanisms. As shown in Figure 2.3 (c), the dehydroxylation process (Equation (2.2)) happens more rigorously when the annealing temperature is higher. As the HT sample was pre-annealed at 520°C, rigorous dehydroxylation can lead to effective removal of M-OH defects. On the other hand as mentioned in Section 2.3.1, the 250°C pre-anneal used for LT samples induces decomposition (Equation (2.1)) but only partial dehydroxylation (Equation (2.2)). The post-anneal of the five-layer film at 520°C promotes dehydroxylation but may be inefficient at removing M-OH defects that are already incorporated deep in the LT film. This may explain the observed differences in M-OH and M-O content in the LT and HT films.

We also observed experimentally that HT samples have less Zn than the LT films and the HT film is slightly thinner than the LT films, indicating that more rigorous Zn loss may occur

during 520°C pre-annealing. To explain these differences, we note that zinc acetate dihydrate, the zinc precursor in our solution, shows [102] excess weight loss when annealed at 150-280°C in air with a slow heating rate of 2°C min^{-1}. This excess weight loss may be due to the formation of volatile organic byproducts containing Zn or sublimation of zinc acetate species. Little weight loss was observed above 280°C under slow heating conditions [102]. In our HT solution-process, rapid heating during the 1-min 520°C pre-anneals may induce a similar loss of Zn, leaving less $Zn(OH)_2$ to go through dehydroxylation. In contrast, 5-min pre-annealing at 250°C, used for LT films, can enhance the decomposition process, causing less Zn loss.

In conclusion, we have done thorough material and electrical characterization of our amorphous zinc tin oxide film. We show that the choice of a high pre-annealing temperature, equal to that used for post-annealing, can significantly enhance thin-film transistor (TFT) performance. Films pre-annealed at higher temperatures exhibit an increase in field-effect mobility from 0.75 cm^{2}V^{-1}s^{-1} to 5.91 cm^{2}V^{-1}s^{-1} and a decrease in subthreshold voltage swing from 1.37 V/decade to 0.44 V/decade. Based on chemical composition measurement, the improved film properties are attributed to a decrease in Zn-to-Sn ratio and to elimination of hydroxide defects by more effective dehydroxylation. These mechanisms are confirmed by XPS, Fourier transform infrared spectroscopy (FTIR), and energy-dispersive spectroscopy (EDS).

2.3.5 TFT fabrication over a wide humidity range

One of the major obstacles for solution-processed AOS is repeatedly achieving high-quality films over a wide range of process conditions. Conventional vacuum deposition is performed in a controlled environment and thus exhibits a high level of control and repeatability in film stoichiometry and quality. In contrast, solution deposition of AOS is typically done in air,

with thermal annealing used to drive chemical structure evolution. The thermodynamics and kinetics of film formation can be greatly influenced by the ambient environment. Especially, the lack of control over ambient humidity can impact the repeatability of device fabrication. Recently it was shown by *Plassmeyer et al.* [41] that changing relative humidity (RH) from 20% to 90% during a solution process involving hydrolyzed reactions led to a significant difference in film properties, including film thickness. *Kim et al.* and *Park et al.* observed that when nitrate precursors are used for In_2O_3 [48], IZO and IGZO [49], a higher conductivity is obtained under wet conditions. *Deepa et al.* [38] observed a change in crystallinity of sol-gel-derived tungsten oxide films by changing process RH from 55% to 75%. Such vulnerability can be problematic as the relative humidity in most research laboratories and manufacturing facilities is difficult to control without specialized, expensive equipment. Therefore, developing a solution process method that is insensitive to the ambient humidity can enable a wider process window to facilitate excellent device uniformity and repeatability.

As mentioned in Section 2.1, MOD processes are often considered insensitive to water [64] and this is the reason why acetate precursors are chosen for our *a*-ZTO films. As shown in Section 2.3.2 and 2.3.3, *a*-ZTO films that were pre-annealed and post-annealed at 520°C showed excellent electrical properties both as bulk films and in TFT devices (HT film and HT TFTs). In this section, we proceed to investigate the effect of RH on the electronic properties of *a*-ZTO films formed using high temperature pre-annealing during MOD solution processing. This is done with the help of customized glovebox that has capability of real-time monitoring, controlling, and stabilizing of ambient temperature and humidity. The schematic of glovebox was shown in Figure 2.2. We fixed the air temperature of the glovebox (the spin-coating environment) at 20°C which led to an air temperature of 40-45°C inside the secondary enclosure

(the annealing environment), due to heat generated from the hot plates. We varied the RH in the spin-coating environment from 10% to 83%. The corresponding RH of the annealing environment is 5% to 40%, respectively, as shown in Figure 2.10 (a). It is lower than the RH of the spin-coating environment due to the higher air temperature inside the secondary enclosure.

Using the HT TFT 520°C pre- and post-annealing procedure, we deposited 5-layer ZTO films under nine different RH conditions, and used these films to make bottom-gate, top-contact TFTs. Typical transfer characteristics are shown in Figure 2.10 (b) and extracted values of μ_{lin}, SS, and hysteresis are plotted versus process conditions in Figure 2.10 (c). Hysteresis, ΔV_C, is defined as the difference in the gate voltage at which $I_{DS} = 100$ nA for forward and reverse voltage sweeps. Despite the dramatic variation in RH of the spin-coating environment from 10% to 83%, the extracted transistor parameters are remarkably similar among different samples: μ_{lin} is 3.76-5.62 cm^{2}V^{-1}s^{-1}, SS are 0.23-0.39 V/decade, and ΔV_C is 0.39-0.76 V. Given that different transistors on the same sample show slight variations in properties (dotted circles in Figure 2.10 (c)), the differences between samples prepared at different RH are not significant. We observe in Figure 2.10 (b) that the threshold voltage (V_T) tends to shift toward more positive voltages for ZTO films made at higher RH. Since all films have similar μ_{lin} and SS, indicating similar bulk ZTO film properties, the observed shift in V_T is likely to be due to creation of defects in the gate dielectric (Al$_2$O$_3$) or at its channel interface that occurs when the dielectric is exposed to high humidity prior to ZTO deposition.
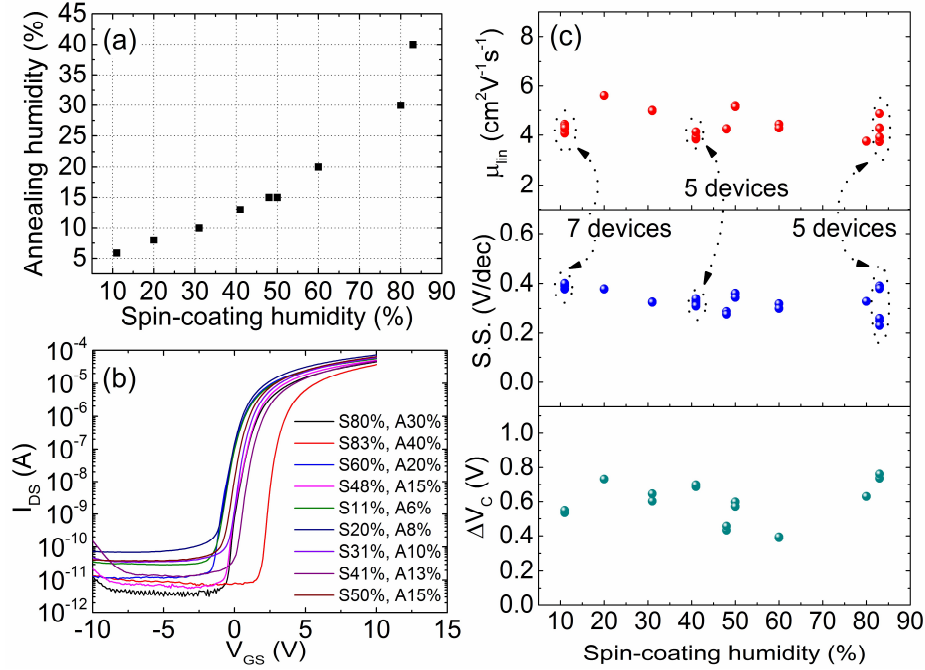
Figure 2.10 TFTs fabricated under various relative humidity in air (a) Relative humidity measured in the glovebox during spin-coating and in the secondary enclosure during annealing. (b) Representative transfer characteristics of TFTs fabricated under different environments with V_{DS} = 1 V and W/L = 500 μm/50 μm. "S" and "A" represent RH in the spin-coating and annealing environments, respectively. (c) Values of μ_{lin}, SS, and hysteresis shown with respect to spin-coating humidity. The device-to-device variations in μ_{lin} and SS are shown for three samples (dotted circles and arrows). The magnitude of device-to-device variation is similar to that of sample-to-sample variation. All of the devices summarized in (c) have W/L dimensions of 500 μm/40 μm or 500 μm/50 μm, and do not have any back channel passivation. Reproduced from Ref. [58] with permission from The Royal Society of Chemistry.

Un-passivated bottom-gate AOS TFTs exposed to high RH or wet conditions often exhibit back channel conduction due to chemisorption of H_2O on the exposed back channel surface, leading to high SS [103], [104]. For TFTs with ZTO deposited at the highest RH (83% for spin-coating and 40% for annealing), we observed a high SS of ~1 V/decade immediately following fabrication, as shown in Figure 2.11. However, after 16 days of storage in a vacuum-sealed bag (Weston Pro-2300 Vacuum Sealer), the SS decreased to ~0.4 V/decade, similar to that of other samples. From these results, it seems that while a high RH process may induce chemisorption of moisture at the ZTO and/or gate dielectric surface, it does not affect bulk ZTO film properties. When the MOD route is used with sufficiently high pre- and post-anneal

temperature, the chemical reactions during spin-coating and annealing were not significantly affected by ambient humidity. The insensitivity to RH for MOD solution-processed films observed here is in sharp contrast to the strong RH-dependence of hydrolysis-based sol-gel processes [38], [40], [41]. Therefore, by using non-hydrolysed MOD routes, we can achieve uniform film quality under a wide range of relative humidity conditions. However we note that the custom glovebox and secondary enclosure used here, along with the compressed dry air purity level and use of DI water for humidification may also facilitate the highly repeatable results observed here. More work is needed to determine the impact of these process design choices on film properties. Nonetheless, we have demonstrated here that MOD solution-process routes are a promising way to realize large-area deposition of metal oxide films in air under a broad range of relative humidity conditions.
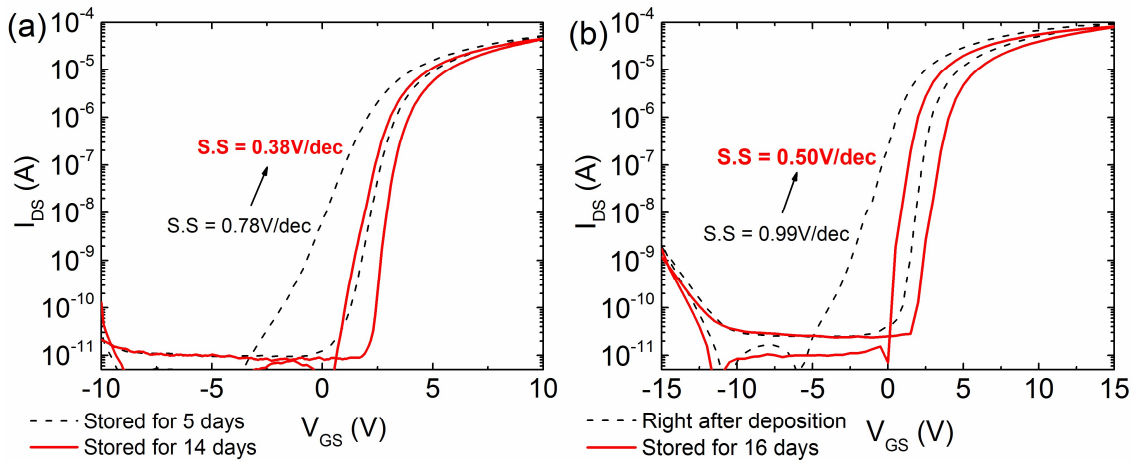
Figure 2.11 The effect of vacuum-packing on TFT transfer curves. Transfer curves for two different TFTs on the same sample are shown in (a) and (b). On this sample, the a-ZTO film was deposited at high humidity (S=83%). The TFT measurements were taken on various days following fabrication, with the dashed lines indicating the earlier measurements and the red lines indicating later measurements. When the samples were not being measured, they were stored in a vacuum pack, possibly inducing desorption of moisture from the back channel surface of the TFT. Both devices exhibit a significant reduction of SS and hysteresis upon aging, possibly due to the desorption of water. The *I-V* measurements taken after storing 14 and 16 days (the red curves) show notable increase in μ_{lin}, and decreases in SS and ΔV_C. The aged devices made at high RH thus have similar performance to devices made at lower RH. Reproduced from Ref. [58] with permission from The Royal Society of Chemistry.

2.4. Conclusions

Solution processing of ternary oxides composed of earthly-abundant metals is an attractive deposition method for AOS due to its in-air deposition capability. Despite its promising features, solution processing of AOS based on conventional sol-gel methods has shown that the film quality is highly sensitive to the ambient humidity during deposition, leading to narrow process window and low yield. Thus, a process that enables fabrication of high quality AOSs over a wide humidity range during solution process is urgently needed in order to achieve truly low-cost and large-area deposition with higher yield.

In this chapter, we have reported a humidity-insensitive solution process to realize future large-area, in-air deposition of metal oxide-based thin film electronics. By using high-temperature pre- and post-anneals of multi-layer spin-coated inks based on acetate-precursors, we induce complete metal-organic decomposition and dehydroxylation (MOD) and are thus able to form high-quality amorphous oxide semiconductor films under a variety of ambient humidity conditions. In addition, unlike nitrate- or chloride-compounds, acetate-based inks do not create harmful byproducts upon annealing, making their use attractive for large-area deposition.

We performed chemical composition analysis and electrical measurements to determine the impact of pre-annealing conditions on multi-layer film *a*-ZTO properties. Pre-annealing each layer at 520°C for one minute followed by 520°C post-annealing of the multi-layer stack produces tin-rich films with robust metal-oxide (M-O) bond formation via dehydroxylation, enabling good TFT performance. While 520°C might be too high of a temperature for flexible substrates, we note that with this process temperature, our devices can be fabricated on other rigid substrates, on both glass and Si substrate, which proves easy hetero-integration of solution-processed AOS. In contrast, pre-annealing at 250°C for five minutes yields zinc-rich films with

many hydroxide (M-OH) defects and poor TFT performance. These differences were explained by the thermodynamics of decomposition and dehydroxylation. We conclude that for MOD processes, there is no advantage to using a low pre-annealing temperature. Rather, for solution processes that use MOD routes, the pre-anneal temperature can be set equal to the post-anneal temperature to enhance semiconductor quality and TFT device performance.
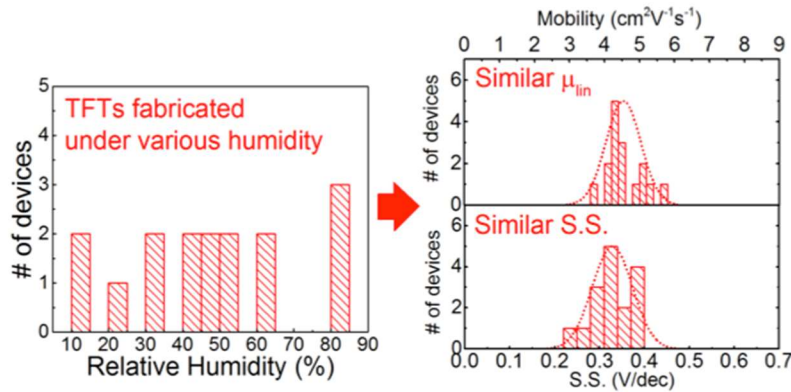
Figure 2.12 The distribution plots of TFT parameters from devices fabricated with a wide range of ambient relative humidity during solution processing. The devices all exhibit similar device characteristics, regardless of the RH during deposition. Reproduced from Ref. [58] with permission from The Royal Society of Chemistry.

In addition, we have designed a custom glovebox that controls the ambient air temperature and humidity during solution deposition and annealing. Using this glovebox, we show that a-ZTO TFTs fabricated in a variety of humidity conditions (RH from 10% to 83%) exhibit very similar device behavior. The MOD route investigated here is insensitive to ambient humidity, making solution processing of amorphous oxide films in air attractive for reliable device fabrication in manufacturing settings.

Chapter 3 Vertical thin-film diode (V-TFD) using bottom Schottky contact

3.1 Introduction

In Chapter 2, we established an in-air deposition process for a-ZTO thin films, which provides consistent film properties over wide range of ambient humidity during film processing. So far, thin-film transistors (TFTs) have been the device of major interest for LAE, especially for display backplanes, where AOS are undoubtedly the leading channel material due to its high electron mobility. Our a-ZTO TFT fabricated in air showed promising device performance: across a wide range of humidity from 10% to 83%, a uniform μ_{lin} of 3.76-5.62 cm^{2}V^{-1}s^{-1} and SS of 0.23-0.39 V/decade were achieved. Building upon this air-stable thin-film deposition process, the next goal is to achieve vertical devices with these thin films for applications in power devices, as explained in Chapter 1. Therefore, the main purpose of this chapter will be to utilize this air-stable and high-quality solution processed film in order to achieve vertical thin-film diodes (i.e., V-TFDs).

Power rectifiers are just as important as power switches, and are widely used in AC-DC conversion. In order to create a unipolar rectifier using AOS materials, which are usually n-type semiconductors, there exist the following three choices: i) a TFT in diode-configuration by connecting drain and gate; ii) a lateral Schottky diode by depositing two top contacts, where one is Schottky and the other is ohmic; and iii) a vertical Schottky diode with bottom and top contacts, where one contact is Schottky and the other is ohmic. The first two options suffer from a lateral structure, which severely limits power rectifier performance. A better choice would be

vertical Schottky diodes, which are expected to provide higher device operation speed, lower forward voltage drop, and higher on-current compared to lateral devices [105], all of which are desirable for power devices.

Given the advantages of V-TFDs, vertical Schottky diodes have been fabricated with vacuum-deposited *a*-IGZO and investigated by other groups recently. These diodes have shown remarkable results as rectifiers that can replace their TFT counterparts. In 2013, *Chasin et al.* reported GHz operation of vertical *a*-IGZO Schottky diodes [106], and demonstrated its usage for wireless energy harvesting for RFID tags in 2014 [106]. In 2015, *Zhang et al.* deposited vertical *a*-IGZO Schottky diodes on a flexible substrate while maintaining a high operation frequency in the GHz range [107]. This high operation speed is achieved via a vertical thin-film structure enabling short carrier transit length, and has remarkable performance compared to TFTs [108]–[110]. An equally important strength of Schottky diodes is their high on-current. When a TFT is used as a rectifier, its gate and drain are shorted. Then, TFT operates in saturation mode and its on current increases by only the square of the voltage. However, a Schottky diode usually has an on-current that increases exponentially by the voltage, leading to lower forward voltage drops and low on-resistance compared to a TFT [20]. Moreover, as mentioned in Chapter 1, vertical current flow of thin film diode structurally enables larger on-current thanks to its wide conduction area, compared to lateral current flow through a "thin"-film transistor.
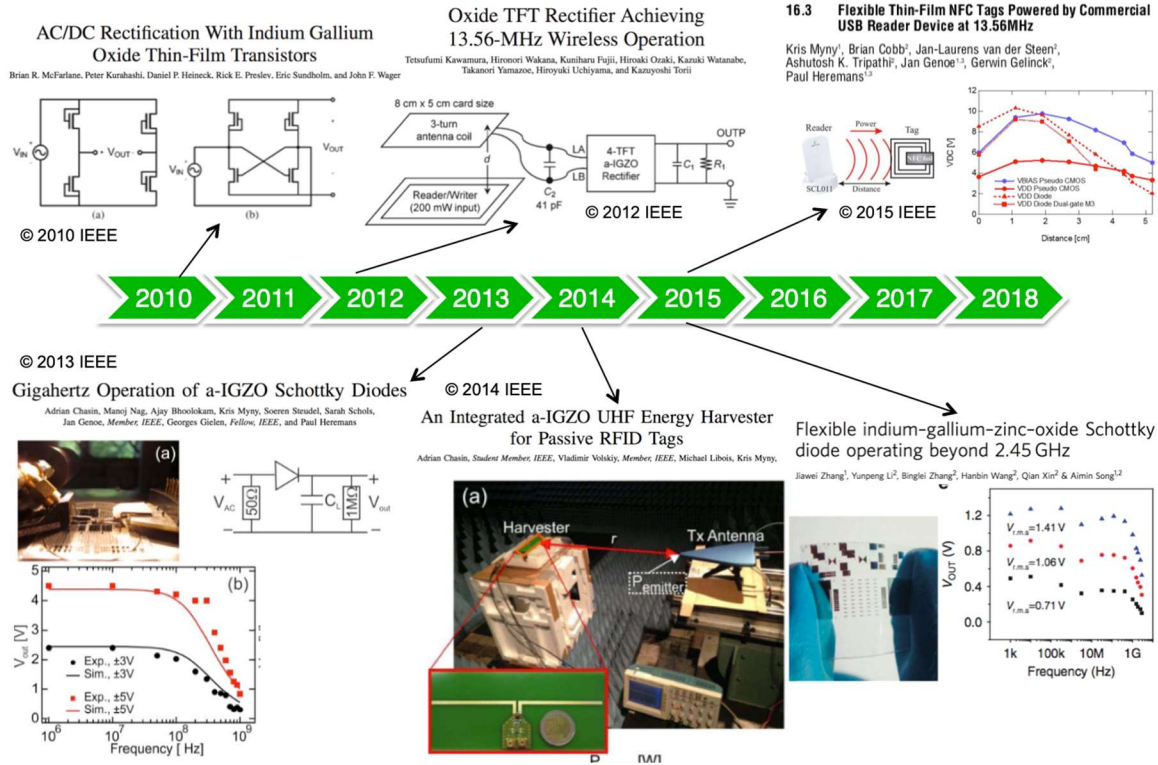
Figure 3.1 The recent progress of AOS as a high frequency AC rectifier. The top row shows the instances of TFTs used as rectifiers whereas the bottom row shows vertical Schottky diodes. The figures are taken from ref. [16], [107]–[109], [111], [112].

The main challenge of fabricating vertical Schottky diodes arises from the need to make a high quality Schottky interface. For an effective rectifying junction to form at the metal-(n-type) semiconductor interface, an abrupt junction with a smooth interface between a high work function metal and clean semiconductor is needed. However in reality, an abrupt clean heterojunction is not energetically favorable and an interfacial layer, interface defects, and semiconductor defects near the interface form naturally due to various interface interactions such as inter-diffusion and alloy mixing. Important and unique interfacial reactions occur with oxide semiconductors at their metal junctions, due to redox mechanisms. *Brillson et al.* and *Martin et al.* have done extensive research on metal-semiconductor junctions for oxide semiconductors, especially with ZnO [113], [114]. They have found that in addition to alloy formation, redox

mechanisms can occur at the Schottky interface, and both of these mechanisms can form Zn vacancies and O vacancies near the Schottky interface. These defects are well-known known in ZnO and can lead to dramatic degradation of Schottky diode performance via means of either Fermi-level pinning or trap-assisted tunneling. Due to these defects, the use of metals with high work functions such as palladium, platinum, and gold, have shown poor ZnO Schottky diode performance.

One common approach to forming Schottky barriers with oxide semiconductors has been the use of oxidized noble metals. Various processes have been used, including direct deposition of oxidized metals (e.g. Ag_xO, PdO_x, PtO_x, IrO_x) [115], [114], [116], [117] or oxygen plasma or anneal treatments on the metal [118], [119] or semiconductor surface [120], [121] prior to the formation of the junction. The presence of the oxidized metal is hypothesized to reduce oxygen vacancies at the Schottky interface [114], [115] or reduce surface electron accumulation to improve rectifying performance [122], [123]. Using this approach, Schottky contact formation with vacuum-deposited oxide semiconductors has been examined by other groups. However, solution-processed AOS Schottky diodes have been rarely reported, due to their complex interface chemistry with the bottom metal during deposition. As explained in Section 2.3.1, our solution-processed *a*-ZTO is formed via thermal decomposition and dehydroxylation (Equation (2.1) and Equation (2.2)), which occur during deposition. When the same deposition process is performed on top of a bottom Schottky metal, in addition to *a*-ZTO chemical evolution there occur interfacial reactions with the Schottky metal. Thus the interactions with metal electrodes are more complex for solution-processed films than for vacuum-deposited ones. The complex thermodynamics at the metal-semiconductor junction for solution-processed AOS should be carefully examined and understood in order to achieve vertical Schottky diodes.

In order to apply solution processed AOS to vertical thin-film devices for power rectifiers, we present a novel method to tune the metal-semiconductor interface properties and form high-quality Schottky contacts to our solution-processed *a*-ZTO. We show that a bottom metal layer can react with our solution *in situ* during chemical evolution and this reaction must be considered to create the desired interface property, either ohmic or Schottky. We present two different mechanisms to establish a rectifying contact between the bottom metal and the solution processed AOS. The first involves depositing and oxidized noble metal with high work function, making use of *in situ* reduction. We experimentally demonstrate this with palladium that is oxidized with oxygen plasma. The second involves depositing a reactive metal that will later oxidize during solution process and form an oxidized metal with high work function *in situ*. We demonstrate this using molybdenum as our bottom metal. We used x-ray photoelectron spectroscopy (XPS) depth profiling and cross-section scanning electron microscopy (SEM) to understand the interface chemistry of the bottom metals and our solution process. The spontaneity of these *in situ* oxidation and reduction mechanisms is evaluated by calculating Gibbs free energy of these reactions. We believe this approach can be extended to other metals and oxide semiconductors to predict their interface chemistry and the resulting electrical properties of the interfaces. Current-voltage (*I-V*) measurements and capacitance-voltage (*C-V*) measurements are taken to confirm the diode behavior.

3.2 Experimental section

3.2.1 Device fabrication

For PdO$_x$:ZTO diodes, 5-nm titanium (Ti) and 30-nm Pd were deposited onto two clean Corning Eagle XG glass substrates using an SJ-26 e-beam evaporator. On one sample, Pd was exposed to oxygen plasma (YES-CV200RFS with RF discharge of 800 W for 10 mins at 60°C with oxygen flow rate at 35 sccm). After bottom metal deposition, five layers of zinc tin oxide were deposited by spin-coating an acetate-based ink with 7:3 [Zn]:[Sn] metal ratio, with 2-methoxyethanol as the solvent. Each layer was annealed for one minute at 520°C. After deposition of the final layer, the sample was annealed at 520°C for one hour. The thickness of the resulting ZTO film was measured to be approximately 130 nm using a DekTak 6M surface profilometer. The peripheral region of ZTO was wet etched using a mixture of hydrochloric acid, nitric acid, and deionized water with a volume ratio of 1:10:90, in order to expose the bottom electrode for electrical measurements. To form the top ohmic contact, 100-nm molybdenum (Mo) was sputtered at 600 W for 230 sec (K. J. Lesker Lab 18) and patterned via liftoff. Sputtered Mo is known to form a good top ohmic contact to solution-processed ZTO [59].

For the Mo:ZTO diodes, 100-nm molybdenum (Mo) was sputtered on clean heavily-doped silicon substrate (n^{++}-Si (Sb), 0.01-0.02 Ω·cm), at 600 W for 230 sec (K. J. Lesker Lab 18). After bottom metal deposition, seven layers of zinc tin oxide layer were deposited using an identical solution process to that explained above. The peripheral region of ZTO was wet etched using the same etchant described above to expose the bottom electrode for electrical measurements. To form the top ohmic contact, 100-nm molybdenum (Mo) was sputtered at 600 W for 230 sec (K. J. Lesker Lab 18) and patterned via liftoff.

3.2.2 Measurement method

XPS measurement was carried out using Kratos Axis Ultra XPS. The measurements were performed in spectrum mode using monochromatic Al x-ray source (8 mA and 14 kV), and pass energy of 20 eV. The Kratos charge neutralizer system was used for all analyses. For depth profiling, argon ion sputtering was used with energy of 5 kV and current of 60 μA. The raster size was fixed to $2{\times}2$ mm^2, and the spot size used was $300{\times}700$ μm^2 for the Pd:ZTO junction while a 110 μm aperture was used for the Mo:ZTO junction. The sputtering time per cycle was 3 min and the expected sputtering rate is 2-3 nm/min for our materials under the given conditions.

The XPS curves were analyzed using CasaXPS software version 2.3.17PR1.1. The curve energies were calibrated using the C 1s peak at 284.5 eV as a reference, to account for charge compensation. O 1s, Zn $2p_{3/2}$, Sn $3d_{5/2}$, Pd $3d_{5/2}$, Si 2p, and Mo 3d peaks were then analyzed by fitting a measured data using Gaussian–Lorentzian curves with FWHM less than two, and a linear background. For the O 1s core level, the measured curves were deconvoluted into three Gaussian–Lorentzian curves. The positions of the three deconvoluted peaks correspond to oxygen atoms in the fully oxidized surroundings (M-O), those in oxygen deficient regions (V_O), and those in H$_2$O and -OH groups (M-OH). These are located at 530.1 ± 0.1 eV, 531.1 ± 0.1 eV, and 532.1 ± 0.2 eV, respectively [40], [60]–[62]. Oxygen atoms adjacent to oxygen vacancies donate some of their electron density toward metal atoms that are not fully coordinated and thus compensate for the loss of the adjacent oxygen [61]. In XPS measurements this causes the O 1s peak to shift from the M-O peak at 530 eV toward higher binding energy, near 531 eV. Thus, the peak near 531 eV indicates the presence of oxygen vacancy defects (V_O). Peaks corresponding to

loosely bound oxygen (M-OH) around 532 eV were only observed at the surface (etch time = 0

sec) and thus are not shown in depth profile plots. Finally, for O 1s analysis near the Pd:ZTO

junction, the broad peaks near 532 eV overlap with the Pd $3p_{3/2}$ peaks, and thus were attributed

to Pd instead of M-OH.

Next, Zn $2p_{3/2}$ and Sn $3d_{5/2}$ peaks were fit using Gaussian-Lorentzian curves centered at

1021.8 ± 0.2 eV and 486.2 ± 0.2 eV, respectively. Lastly, Mo 3d doublet core levels were

analyzed using six Gaussian-Lorentzian curves with the following constraints: (a) the $3d_{5/2}$ to

$3d_{3/2}$ ratio is 3:2 and (b) the peaks that correspond to different oxidation states of Mo are located

within the ranges given in Table 3.1 [124]–[126].

Table 3.1 Binding energy for Mo 3d core-level analysis (eV)							
Mo^{6+}		Mo^{5+}		Mo^{4+}		Mo^0	
Mo $3d_{5/2}$	Mo $3d_{3/2}$	Mo $3d_{5/2}$	Mo $3d_{3/2}$	Mo $3d_{5/2}$	Mo $3d_{3/2}$	Mo $3d_{5/2}$	Mo $3d_{3/2}$
231.9 ± 0.2	234.8 ± 0.1	230.4 ± 0.4	233.4 ± 0.3	228.5 ± 0.2	231.5 ± 0.1	227.0 ± 0.1	230.3 ± 0.1

After the core-level spectra analysis, the areas under each XPS peaks were calculated by

integration to estimate atomic compositions of Zn, Sn, M-O, V_O, M-OH, Mo^{6+}, Mo^{5+}, Mo^{4+}, and

Mo^0. The conversion from area to atomic concentration was done using relative sensitivity

factors taken from CasaXPS_kratos.lib, available online at http://www.casaxps.com/kratos/.

The electrical performance of the diodes was measured using an HP4156A

semiconductor parameter analyzer. All current-voltage measurements were taken in continuous

sweep mode with medium integration time. Capacitance-voltage (*C-V*) characteristics were taken

using an HP 4284A precision LCR meter. The measurements were performed at room

temperature in ambient air and in the dark.

3.3 Rectifying junction formation with bottom metal

3.3.1 Oxidation of Pd to obtain rectifying PdO$_x$:ZTO junction

Prior to ZTO layer deposition, we cleaned the Pd surfaces of the two samples, one with and one without prior oxygen plasma treatment, using organic solvents and carried out XPS measurements to verify that a PdO$_x$ layer is formed by our oxygen plasma treatment. The result is shown in Figure 3.2 (a). The coexistence of Pd and PdO is observed in the sample treated with oxygen plasma. Compared to thermal oxidation, Pd oxidized by oxygen plasma is known to exist in various oxidation states [127]. The thickness of the PdO$_x$ layer from DekTak 6M surface profilometry was thicker (~60 nm) compared to bare Pd (~30 nm) due to volumetric expansion during oxidation. Then, deposition of the ZTO layer and top Mo electrode were performed to fabricate vertical two-terminal devices. Using the fabricated devices, current density vs. voltage curves were measured and are plotted in Figure 3.2 (b). Devices without surface treatment show no rectifying behavior, whereas devices with the surface treatment showed on/off ratios of around 500 at ±1 V and on-current density of > 10^3 A·cm^{-2} at +1 V.
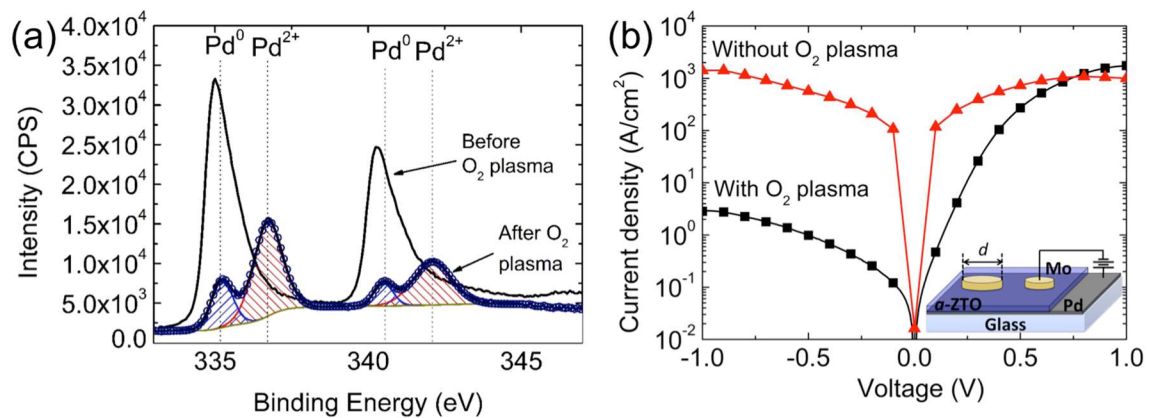
Figure 3.2 The effect of oxygen plasma on bottom Pd electrode (a) Pd 3d core-level spectra of XPS measurements from films that were not exposed to oxygen plasma (upper curve) and that were exposed to oxygen plasma (lower

To obtain a high quality Schottky contact, control of the interface chemistry is critical because both interface states and semiconductor density of states near the interface directly affect contact properties. For ZnO deposited using conventional vacuum techniques, it has been found that metals such as Au, Pd and Pt can react to form oxides as well as eutectics with Zn and can produce defects associated with oxygen vacancies and zinc vacancies [113], [128]. In order to reduce oxygen vacancies at the interface, minimize trap-assisted tunneling, and thus realize high quality Schottky contacts to ZnO, these high work function metals [115] have been used in conjunction with oxygen plasma treatment of the ZnO surface before Schottky metal deposition [129]. In addition, oxidized Pd has been used to form a Schottky contact to IGZO, another amorphous oxide semiconductor [118], [130]. Thus, we hypothesize that oxygen plasma treatment of the bottom Pd, by forming a PdO_x layer at the surface, may reduce oxygen-deficiency-related defects near the Pd/ZTO interface and thus improve the rectifying contact to solution-processed ZTO. In contrast, the Schottky contact for the device without oxygen plasma is nearly ohmic (Figure 3.2 (b)), similar to what has been reported by others [129]. We surmise that the ZTO layer deposited without oxygen plasma treatment of Pd has a significant number of defects that cause defect-assisted tunneling to be the dominant charge transport mechanism between Pd and ZTO.

To investigate the formation of PdO_x:ZTO rectifying contacts, we performed XPS depth profiles (Figure 3.3) on samples with Pd and five layers of ZTO deposited on heavily-doped silicon substrate (n^{++}-Si (Sb), 0.01-0.02 Ω·cm), using the process described above. As before,

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one sample was treated with oxygen plasma while the other was not. Analysis of the O 1s core level of the ZTO layer prepared without Pd oxygen plasma treatment showed an interface region with significant amounts of bonded oxygen atoms (M–O) and oxygen atoms near oxygen-deficiencies (V_O) (Figure 3.3 (a)). Measurement of ZTO prepared with Pd-oxygen plasma treatment showed a comparatively small V_O concentration at the same location (Figure 3.3 (b)). Thus, the oxygen plasma treatment, combined with ZTO deposition and annealing, reduces the concentration of oxygen vacancies within the ZTO layer close to the Schottky barrier interface.
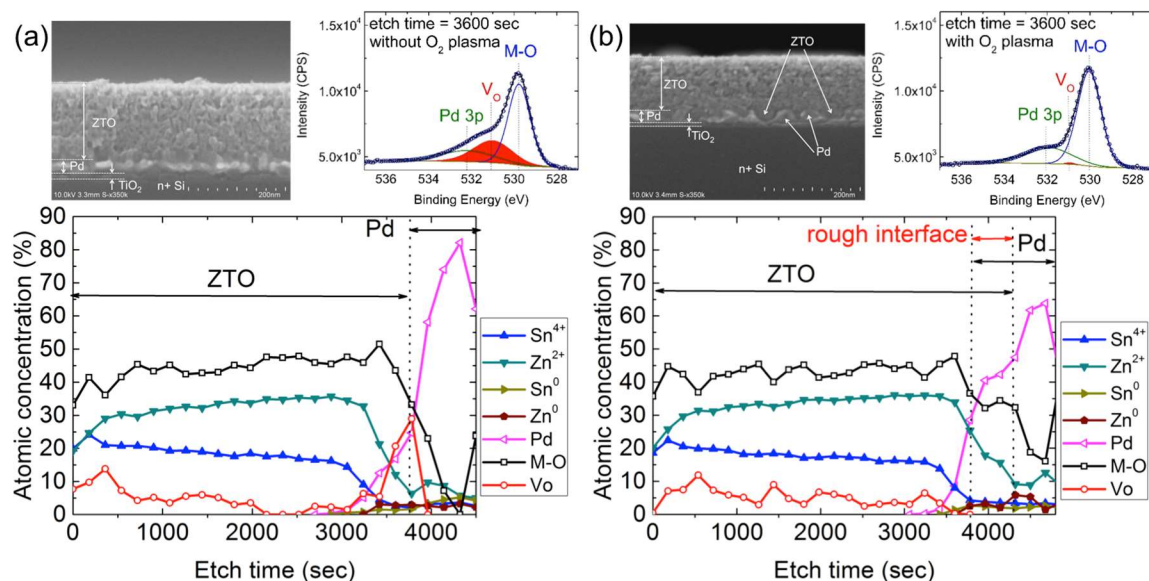
Figure 3.3 XPS depth profiles and cross-sectional SEM of ZTO/Pd deposited on Si substrate (a) without and (b) with oxygen plasma treatment of the Pd layer. Peaks for loosely bound oxygen around 532 eV were only observed at the surface (etch time = 0 sec) and are not shown above. Within the ZTO film region, fitting of the O 1s data did not require the 532 eV peak be included: the concentration of –OH is negligible in the bulk of the ZTO layer. For both samples, at the interface between the Pd/Ti and Si, the M–O curve was centered near 530 eV, possibly indicating that Ti was oxidized to TiO_2. The high atomic concentration of oxygen is most likely due to the fact that the Ti core-level was not measured, i.e. the Ti atomic concentration is not included. The O 1s and Pd $3p_{3/2}$ core-levels at the ZTO/Pd interfaces at an etch time of 3600 sec are shown in the insets. In the inset, symbols (circles) indicate the summation of the three de-convoluted peaks. The summation overlaps with the measured curve. Reprinted with permission from [101]. Copyright 2016 American Chemical Society.

It is important to note that oxygen plasma treatment before ZTO deposition converted Pd into PdO_x and thus the observed oxidation state changed from Pd^0 to a combination of Pd^0 and

Pd^{2+} (Figure 3.2 (a)). However after ZTO deposition, the Pd 3d peak appears only at the Pd^0 position, as shown in Figure 3.4 (a), indicating that the ZTO process has reduced the PdO_x layer back to metallic Pd. The thickness of Pd after the ZTO wet etch was measured to be around 30 nm which is similar to the thickness of the bare Pd before oxidation. Therefore, we can conclude that reduction of PdO_x layer provided an oxygen-rich environment during the formation of ZTO, and thus reduced the concentration of oxygen vacancies near the PdO_x:ZTO interface. This reaction takes place *in situ* during the deposition of ZTO. The driving force of this interface chemistry will be explained later in Section 3.3.5.

Cross-sectional SEM images of the same sample (Figure 3.3 (b) inset) show that the interface between PdO_x and ZTO was rough. This observation is in accordance with our XPS depth profile measurements of the same sample. As shown in Figure 3.3 (b), between the ZTO layer and Pd layer there was a region of approximately 10 to 20 nm thickness where Pd^0 and ZTO co-exist. (Since Pd was not in the Pd^{2+} state, as shown in Figure 3.4 (a), we know that Pd is not doped into ZTO, but rather the two materials form a mixed, rough interface.) We suspect that this roughness is due to rapid reduction of PdO_x during the ZTO solution process. In contrast, a cross-sectional SEM image of the ZTO/Pd sample without oxygen plasma treatment showed a relatively smooth interface between the Pd and ZTO layer, which corresponds to the smooth transition of Pd and ZTO observed in the XPS depth profile, Figure 3.3 (a). So, the *in situ* Schottky barrier formation process has the advantage of providing a good rectifying contact, but it simultaneously roughens the metal-semiconductor interface due to oxygen transfer during redox.
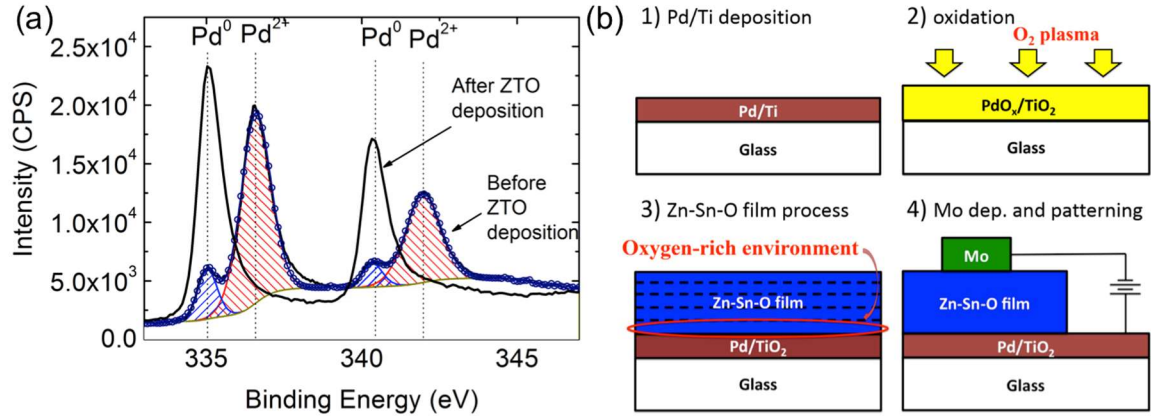
Figure 3.4 (a) Pd 3d core-level spectra on oxidized Pd before and after ZTO deposition. PdO$_x$ created by oxygen plasma treatment of Pd has been reduced to Pd^0 during ZTO deposition and annealing. The data shown for after ZTO deposition corresponds to the XPS measurement of Figure 3.3 (b) at etch time of 4680 sec. (b) The fabrication process for Mo/ZTO/Pd diodes with oxygen plasma treatment. The reduction of PdO$_x$ during the ZTO process provides an oxygen-rich environment near the Schottky interface. Reprinted with permission from [101]. Copyright 2016 American Chemical Society.

3.3.2 Rectifying behavior of PdO$_x$:ZTO diode

The forward-bias *J-V* curves for different top electrode areas were fit to a circuit model of an ideal diode with a series resistance, R_s, using the following equation:

$$J = J_S \left\{ \exp\left[\frac{q(V - J \cdot A \cdot R_S)}{n k_B T} \right] - 1 \right\}. \tag{3.1}$$

Here J_s is the saturation current density, *V* is the externally applied voltage, *T* is the temperature (assumed to be 300 K), k_B is Boltzmann's constant, *A* is the area of the Mo electrode (which corresponds to $(d/2)^2 \pi$ in the bottom inset of Figure 3.2 (b)), *q* is the electronic charge, and *n* is the ideality factor. The measured data are shown in Figure 3.5 (a). The forward current near 1 V increases as the area of the device increases, but it does not increase linearly with area. This indicates that the series resistance has two components: one that scales with area, and one that does not scale. The non-scaling (constant) component may be due to parasitic resistance from the probe, measurement setup, and so on. This is indicated by R_c in the inset of Figure 3.5

(a). We extracted a value for R_c of 19.65 Ω from the measured data. The forward J-V curves of the diodes are then corrected to exclude the voltage applied to R_c. The corrected J-V curves are shown in the top inset of Figure 3.5 (a) and exhibit good agreement across a wide range of device sizes.

In a high forward bias region of the corrected J-V curves, the current is still limited by series resistance. Under strong forward bias, the depletion region width is negligible and nearly the entire semiconductor layer is an ohmic drift region that contributes to the total series resistance, i.e. $R_{s,total} = R_c + R_{on,sp}/A$. Using Equation (3.1) and a contact resistance value, R_c, of 19.65 Ω, we extracted values of $R_{on,sp}$ for each device. The values, listed in Table 3.2, are similar for all devices. Since $R_{on,sp}$ corresponds to the resistance of the non-depleted portion of the ZTO layer, we use its value to calculate the free charge concentration (n_{free}) in our ZTO layer using the following equation,

$$\rho_{ZTO} = \frac{R_{on,sp}}{t_{ZTO}} = \frac{1}{q n_{free} \mu_e}, \tag{3.2}$$

where, t_{ZTO} and ρ_{ZTO} are the ZTO thickness and resistivity, and μ_e is the electron mobility. We take μ_e to be 5 cm^{2}V^{-1}s^{-1} from the Hall measurements in Section 2.3.2 and t_{ZTO} to be 130 nm based on film thickness measurements. Using these values, the free electron concentrations of the diodes were found to range from 2.54×10^{16} to 1.13×10^{17} cm^{-3} (Table 3.2).
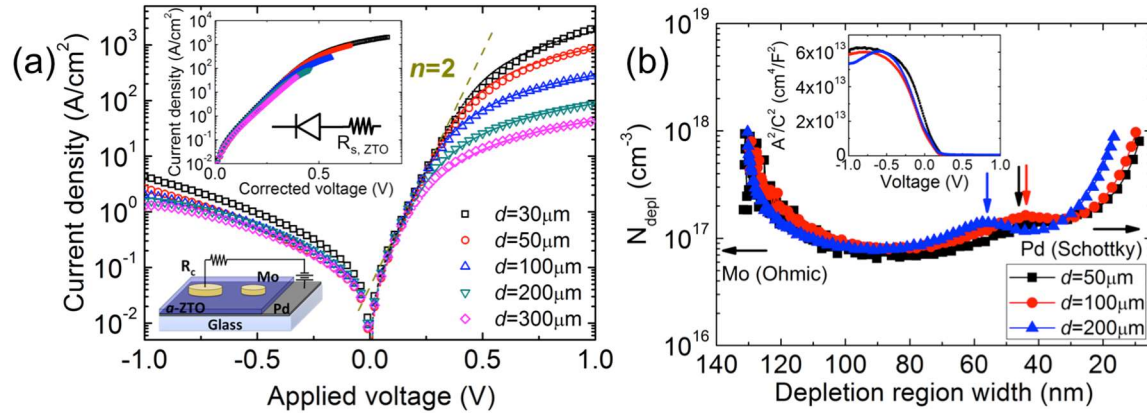
Figure 3.5 *J–V* and *C-V* characteristics of PdO$_x$:ZTO diode (a) *J–V* characteristics of diodes with various top electrode diameters. The solid line in forward bias shows the curve fits to the total series resistance, $R_{s,total}$. The inset shows the corrected *J-V* curves in which the voltage across the contact resistance, R_c, is subtracted from the applied voltage. The corrected *J-V* curves show good agreement between diodes with different electrode areas. (b) Depth profile of depletion charge density (N_{depl}) from *C-V* analysis. The small upward kink in N_{depl} is indicated by the arrows. N_{depl} values greater than 10^{18}cm^{-3} are omitted for clarity. The inset shows A^2/C^2 vs. voltage. Reprinted with permission from [101]. Copyright 2016 American Chemical Society.

Table 3.2 Electrical characteristics of circular PdO$_x$:ZTO Schottky diodes.					
Diameter	30 μm	50 μm	100 μm	200 μm	300 μm
$\Phi_{B,\,IV}$ (eV)	0.47	0.39	0.39	0.47	0.39
n (see note a)	1.94	1.82	1.87	2.02	2.14
$R_{on,sp}$ (Ω×cm^2)	1.44×10^{-4}	1.81×10^{-4}	4.32×10^{-4}	6.41×10^{-4}	1.65×10^{-4}
n_{free} (cm^{-3})	1.13×10^{17}	8.99×10^{16}	3.76×10^{16}	2.54×10^{16}	9.83×10^{16}

^{a}Values of *n* were extracted from the forward bias region, for 0.1 to 0.3 V.
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According to the thermionic emission (TE) model, the saturation current density, J_s, is given by

$$J_S = A^* \times T^2 exp\left(-\frac{q\Phi_{B,IV}}{k_B T}\right),\tag{3.3}$$

where $\Phi_{B,IV}$ is the effective Schottky barrier height, and A^* is the effective Richardson constant. Taking A^* to be 41 A·cm^{-2}·K^{-2} from the value found for *a*-IGZO [131], $\Phi_{B,IV}$ values were extracted from measured values of J_S and Equation 3.3. The results are shown in Table 3.2. The $\Phi_{B,IV}$ values of 0.39 to 0.47 eV are relatively low compared to the difference between the known

work function of Pd (5.22 - 5.6 eV) [132] and the electron affinity of ZTO (4.35 - 4.6 eV) [133], [134]. The ideality factors, *n*, were extracted from Equation (3.1) to be around 1.9 (see Table 3.2). The thermionic emission model was only used for forward bias because it cannot explain the observed sharp increase in reverse current with reverse bias voltage. The extraction of ideality factors significantly greater than one indicate that additional transport mechanisms should be considered [135]. More accurate charge transport analysis of the PdO$_x$:ZTO diode will be conducted in the next chapter.

Capacitance-voltage (*C-V*) characteristics were measured at 1 MHz. Complex impedance was fit to a parallel *RC* model. The A^2/C^2 $vs. V$ data are plotted in the Figure 3.5 (b) inset. Different electrode areas show similar capacitance densities. The minimum constant capacitance in reverse bias corresponds to full depletion, and the large increase in capacitance in the weak forward bias regime indicates reduction of the depletion region width. The capacitance of an abrupt Schottky junction follows Equation (3.4):

$$\frac{A^2}{C^2} = \left(\frac{2}{q\varepsilon_{ZTO}\varepsilon_o N_{depl}}\right)\left(V_{bi} - \frac{k_B T}{q} - V\right), \tag{3.4}$$

where ε_{ZTO} is the relative permittivity of ZTO, ε_o is the permittivity in free space, and V_{bi} is the built-in potential. V_{bi} values of approximately 0.24 V were found for all three devices. From the capacitance equation, $C = \varepsilon_{ZTO}\varepsilon_o A/w$, and assuming the full depletion width to be $w=t_{ZTO}$=130 nm, ε_{ZTO} was calculated to be approximately 19, which is close to the value of 18 used for *a*-IGZO [118]. Using these values, we calculated and plotted the ZTO depletion charge concentration, N_{depl}, as a function of the depletion width, *w*. The result is shown in Figure 3.5 (b). The measured N_{depl} is in the order of 10^{17} cm^{-3}, slightly higher but similar to the values of n_{free} in Table 3.2, which were extracted from *J-V* measurements.

3.3.3 *In situ* oxidation of Mo to obtain rectifying Mo:ZTO junction

For an n-type semiconductor like *a*-ZTO to form Schottky contact, it needs to form a junction with high work function metal, with minimum defects. For this reason, high work function metals such as Pd, Pt, and Au seem reasonable choice to make a Schottky contact. However, as we showed in the previous sections, depositing *a*-ZTO on Pd creates significant amount of V_O defects at the interface and does not give a rectifying contact. To resolve this, an additional oxidation step was required on Pd prior to *a*-ZTO deposition, in order to reduce oxygen deficiencies and obtain a Schottky contact. What we observed with our solution processed *a*-ZTO and Pd is in agreement with other vacuum-deposited metal oxides [114], [115], [118], [136], where noble metals had to be oxidized (e.g. PdO_x, PtO_x, IrO_x) to ensure a high quality Schottky diode. In all of these cases, *in situ* reduction of the bottom metal occurs. These metals tend to donate oxygen to neighboring oxide semiconductors as they are noble and non-reactive.

While choosing these oxidized noble metals might provide a solution to obtain Schottky contacts on AOS, it is a less favorable option from a fabrication viewpoint. V-TFD and TFT are both required for future thin-film ICs as the former provides better rectifier performance while the latter is inevitably required for logic. For TFT fabrication ohmic contacts are necessary as shown in Chapter 2. The challenge for V-TFD is that if we choose high work function metal for Schottky contact, it adds another deposition and patterning cycle for the Schottky metal. In addition, the oxidation step for these noble metals adds additional fabrication steps and complexity in order to obtain good Schottky diodes. The increased fabrication steps lead to an increase in overall fabrication cost, undesirable for low-cost and large-area electronics.

These processes can be avoided if *in situ* reactions of a bottom metal takes place, such that an ohmic contact metal can be turned into a high work function metal and achieve rectifying contacts. Therefore, in the following sections, we will describe a method to fabricate novel Schottky contacts using a low work function metal. To achieve this, our approach is to start from a low-work function metal that is widely used for TFT fabrication, which is also reactive instead of being noble. This reactivity leads to the bottom metal oxidizing during *a*-ZTO deposition, which results in *in situ* formation of a high work function oxidized metal. When the same metal is deposited on top of *a*-ZTO, this oxidation reaction does not take place because it is done after *a*-ZTO film formation and at room temperature. Molybdenum is one of the commonly used metal for AOS TFT fabrication [137], [59], [138]–[140] due to its low work function (4.4–5.0 eV [141]), and it can form a high-quality ohmic contact when sputtering on top of our *a*-ZTO [59]. In addition, Mo has a high oxidation energy and is therefore reactive. Thus, we investigate the *in situ* reaction of sputtered molybdenum with our solution process in the following sections.

In contrast with bare molybdenum, its oxidized counterpart, i.e., molybdenum suboxide, has a significantly higher work function (4.7–6.8 eV [126], [142]–[145]). Thus, if a Mo bottom electrode oxidizes *in situ*, it may form a rectifying contact as a result of the solution process. While *in situ* reduction of noble metals have been widely explored to obtain rectifying contacts to oxide semiconductors, the opposite mechanism, namely *in situ* oxidation of reactive metals has not been reported yet, to the best of our knowledge. Thus, here we seek to form a molybdenum suboxide layer at a bottom Mo:ZTO junction in order to establish a deeper understanding of the interface chemistry between metal and oxide semiconductors required for Schottky contacts.

We first deposit ZTO on top of solvent-cleaned bottom Mo, and then perform XPS depth profile and cross-sectional SEM image. The results are shown in Figure 3.6 (a) and (b). Both the XPS depth profile and SEM image reveal the existence of an additional MoO_x layer grown on top of bottom Mo. By analyzing the Mo 3d peaks from XPS measurement, the oxidation states of Mo indicate the formation of a MoO_x layer. Compared to metallic Mo^0 which is observed at the bottom, Mo near the Mo:ZTO junction shows various oxidations states of Mo^{6+}, Mo^{5+}, and Mo^{4+}. We note a transition in oxidation states from $Mo^{6+} \rightarrow Mo^{5+} \rightarrow Mo^{4+} \rightarrow Mo^0$ as we move from the boundary with ZTO toward the bottom Mo metal. A similar transition of Mo oxidation states has been reported for both thermally oxidized Mo and MoO_3 grown on Mo substrate, where Mo^{6+} was interpreted as Mo in fully oxidized MoO_3, Mo^{5+} as MoO_3 with oxygen vacancies, and Mo^{4+} as metallic MoO_2 [124]. The oxidation states of Mo analyzed from XPS depth profile data shows a spatial distribution indicating that a MoO_x layer with considerable thickness was formed due to the oxidation of bottom molybdenum during the *a*-ZTO solution process. The SEM cross-sectional image also shows distinct morphological changes, where a smooth MoO_x layer grown on top of polycrystalline Mo is observed. By comparing the sputtering time of XPS and the SEM image, we estimate the thickness of the MoO_x layer to be around 50 nm.
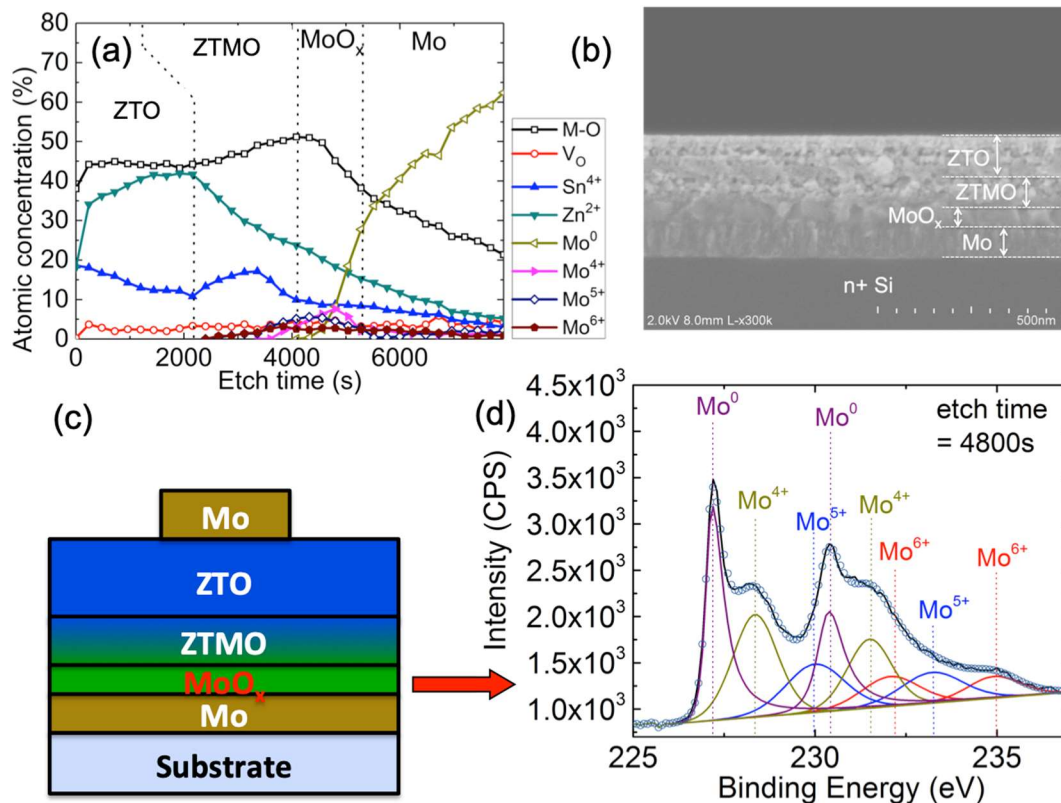
Figure 3.6 Material characterization of Mo:ZTO interface (a) XPS depth profiles and (b) cross-sectional SEM of ZTO/Mo deposited on Si substrate Peaks for loosely bound oxygen around 532 eV were only observed at the surface (etch time = 0 sec) and are not shown above just as PdO$_x$:ZTO case. Unlike PdO$_x$:ZTO junction, near the interface two additional interfacial layers appear, both as chemical composition change in (a) and as morphological change in (b). These distinctive layers are namely molybdenum oxide layer and Mo-doped ZTO layer. (c) shows a schematic of these layers. (d) Mo 3d core-level analysis of MoO$_x$ layer at ZTO/Mo interface (i.e., at an etch time of 4800 sec in (a)). Symbols (circles) indicate the summation of the three de-convoluted peaks, which overlaps with the measured curve. Reprinted with permission from [146].

Also from XPS depth profile we notice that between the ZTO and MoO$_x$ layers there exists another layer with a distinct chemical composition. In this region, the Mo mainly exists as Mo^{6+} and the Zn:Sn ratio is significantly decreased compared to that of the ZTO layer. The thickness of this region is around 50 nm. Thus, molybdenum not only oxidizes but also diffuses into the ZTO layer. From the cross-sectional SEM image, we note that on top of the smooth MoO$_x$ layer, there are two different layers, in which the top layer has a smooth morphology and the bottom layer has a comparatively rough morphology. Therefore, we can conclude that due to Mo diffusion, a Mo-doped ZTO film of 80-nm thickness is formed. Hereafter, this Mo-doped

ZTO layer will be referred as the ZTMO layer. In conclusion, the structure of Mo:ZTO junction appears to be composed of the following four layers, ZTO:ZTMO:MoO$_x$:Mo. Thanks to the high work function expected for MoO$_x$, we propose that the Schottky junction is formed between the ZTMO and MoO$_x$ layers. The rectifying behavior of the junction will be examined via electrical measurements in the next section.

3.3.4 Rectifying behavior of Mo:ZTO diode

After the deposition of the ZTO layer, a top ohmic Mo electrode of 100 nm in thickness was deposited via sputtering. Mo sputtered on top of ZTO forms a good ohmic contact, and a contact resistance as low as 8.3 Ω-cm has been extracted using the transmission line method [59]. After patterning of top Mo through liftoff, the *J-V* characteristics of thin-film diodes have been measured. Current density vs. voltage traces are plotted in Figure 3.7 (a). Rectifying behavior was observed where an on/off ratio of $> 10^2$ is achieved at ± 3 V. The on-current density is $\sim 10^2$ A·cm^{-2} at +3 V, which is slightly less than 10^3 A·cm^{-2} obtained at +1 V for PdO$_x$:ZTO diode. While the high on-current of the PdO$_x$:ZTO diode was achieved by an exponential increase of current due to forward bias, following Equation (3.1), the on-current of Mo:ZTO diode could not be fitted using Equation (3.1). An explanation of this deviation with the help of an accurate charge transport model for the Mo:ZTO diode will be established in the next chapter. Despite its lower on current, we note that on/off ratio of Mo:ZTO diodes is similar to that of the PdO$_x$:ZTO diode due to its lower off-current. One important observation is that the reverse leakage current of Mo:ZTO is observed to be relatively independent of reverse bias, indicating its usefulness for high voltage applications. The difference in reverse current behavior as well as

the difference in forward current behavior observed from these diodes will be explained via charge transport analysis in the next chapter.

Capacitance-voltage (*C-V*) characteristics were measured at 1 MHz. Identical to PdO$_x$:ZTO diodes, the complex impedance was fit to a parallel *RC* model. The A^2/C^2 $vs.V$ data are plotted in the Figure 3.7 (b) inset. Different electrode areas show similar capacitance densities. The minimum constant capacitance in reverse bias corresponds to full depletion, and the large increase in capacitance in the weak forward bias regime indicates reduction of the depletion region width. From the obtained *C-V* measurement, the depletion concentration depth profile can be obtained using Equation (3.4) which is repeated below:

$$\frac{A^2}{C^2} = \left(\frac{2}{q\varepsilon_{ZTO}\varepsilon_o N_{depl}}\right)\left(V_{bi} - \frac{k_B T}{q} - V\right), \tag{3.4}$$

where ε_{ZTO} is the relative permittivity of ZTO, ε_o is the permittivity in free space, and V_{bi} is the built-in potential. V_{bi} values of approximately 0.3 V were found for all three devices. Using ε_{ZTO} of 19 extracted from the PdO$_x$:ZTO diode in Section 3.3.2 along with the capacitance equation, $C = \varepsilon_{ZTO}\varepsilon_o A/w$, the full depletion width was extracted to be $w=t_{ZTO+ZTMO}=180$ nm, equivalent to the thickness measured by DekTak. N_{depl}, as a function of the depletion width, w, is shown in Figure 3.7. The measured N_{depl} is in the order of $>10^{17}$ cm^{-3}.
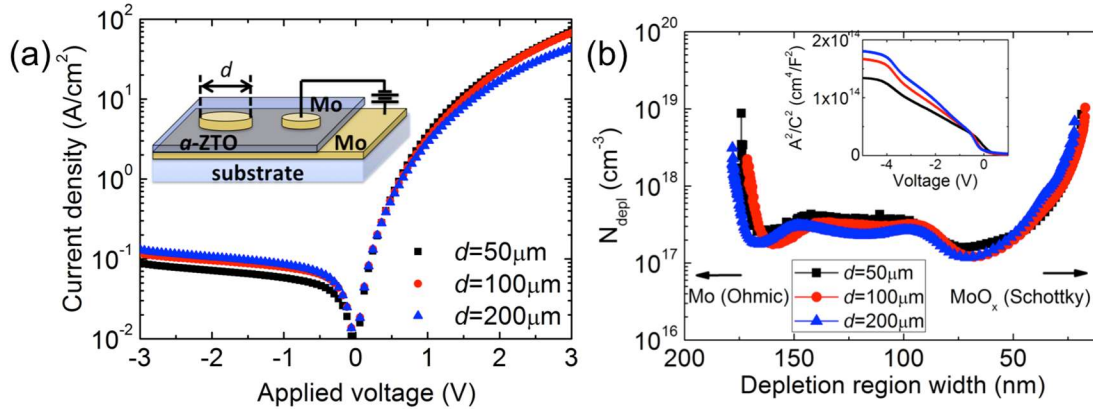
Figure 3.7 *J–V* and *C-V* characteristics of Mo:ZTO diode (a) *J–V* characteristics of Mo:ZTO diodes with various top electrode diameters, *d*. The *J-V* curves show good agreement between diodes with different electrode areas. (b) Depth profile of depletion charge density (N_{depl}) from *C-V* analysis. N_{depl} values greater than 10^{19} cm^{-3} are omitted for clarity. The inset shows A^2/C^2 vs. voltage. Reprinted with permission from [146].

3.3.5 The origin of *in situ* redox mechanism and diffusion

So far, we have observed that between the bottom metal and solution-processed AOS, various interface chemistries occur during solution deposition and annealing. These chemistries include oxidation, reduction, and diffusion. These reactions caused significant changes in contact properties, as confirmed by electrical measurements. The obtained *I-V* characteristics revealed that *a*-ZTO makes a semi-ohmic contact to bottom Pd but forms a Schottky contact to bottom Mo. This result can be predicted only if interfacial reactions are considered, because theoretically an n-type semiconductor should form an ohmic contact with a low work function metal, Mo, and a Schottky contact with a high work function metal, Pd (Φ_{Pd} of 5.22-5.6 eV [132], Φ_{Mo} of 4.4-5.0 eV [141], and χ_{ZTO} of 4.35-4.6 eV [133], [134]).

The property of metal-semiconductor contacts is undoubtedly a critical element in all semiconductor devices and technology, as it can dramatically change the overall device performance. Therefore, in order to design optimal contacts for future solution-processed AOS devices, a methodology to anticipate the interface chemistries for different metal contacts and

AOS should be developed. In this regard, we study the origin of these interface reactions, namely redox and diffusion, so that our observations of PdO_x:ZTO and Mo:ZTO junctions can be extended to predict the behavior of other junctions that have not been tested yet. To achieve this, we next focus on explaining the mechanisms that drive the reactions observed with PdO_x and Mo. We will first explain our solution process case and then later extend this understanding to the vacuum-deposited case.

In Chapter 2, we showed that using acetate precursors for solution processed ZTO enables good film quality that is consistent over a wide humidity range during deposition. The chemical evolutions that take place during this deposition, namely decomposition and dehydroxylation, were also explained. The Gibbs free energy of these reactions calculated versus temperature indicated that in order to obtain solution processed ZTO with excellent electrical properties, the spin-coated solution needs to be annealed up to at least 520°C in order to fully induce dehydroxylation and remove hydroxyl defects. This was experimentally confirmed by performing XPS depth profiles on ZTO films annealed at different temperature. Therefore, annealing ZTO solution at 520°C is inevitable in getting air-stable, high-quality ZTO film. In this case, our ZTO was deposited and annealed on top of stable oxides (SiO_2 and Al_2O_3) that do not interact with ZTO, and thus a uniform ZTO film could be grown without significant interfacial chemical reactions.

The situation is different when we make V-TFD using our *a*-ZTO process. For V-TFDs, our ZTO solution must be dispensed on top of bottom anodes instead of a dielectric films, and later be annealed at 520°C. This requires the bottom metal electrode and ZTO solution to be annealed together on the substrate (Figure 3.8). As we apply thermal energy during the solution annealing step, the system tends to find more energetically favorable states. Therefore,

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depending on the reactivity of the bottom metal, it might interact with our solution process of ZTO during annealing. In some cases it is thermodynamically favorable for the metal to react with the AOS to form a metal oxide (as in the case of Mo→MoO$_x$). In other cases, the metal-AOS interface is stable and any metal oxide present at the interface will reduce back to elemental metal (as in the case of PdO$_x$→Pd). Here, we explain these different reactions based on thermodynamics.
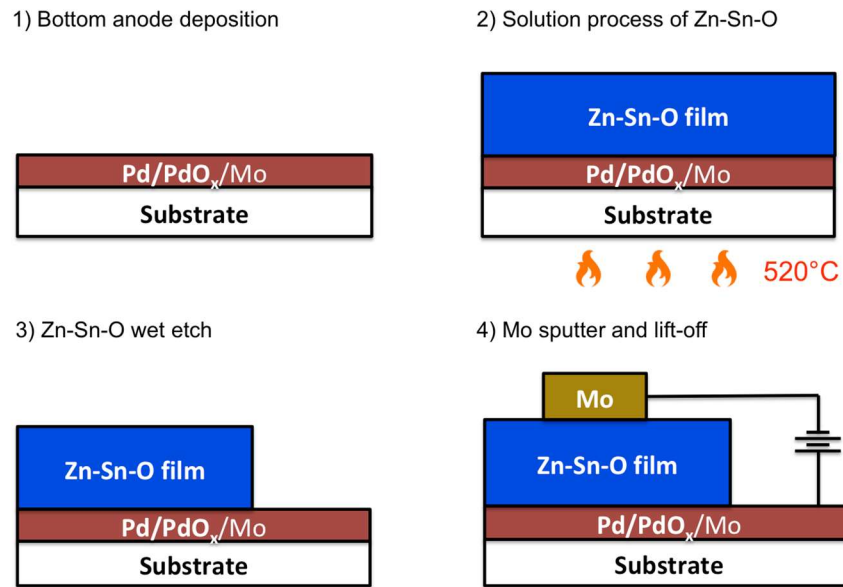
Figure 3.8 The schematic of ZTO deposition on metal electrode using solution process. On bottom metal, our acetate-based ink is dispensed, spin-coated, and annealed, following the procedure in Figure 2.2 (a).

Based on thermodynamic analysis, the spontaneity of a given chemical reaction is quantitatively determined by standard Gibb's free energy (ΔG_{rxn}^o). For any given reaction, ΔG_{rxn}^o needs to be negative for the reaction to be spontaneous, and the more negative, the more spontaneous. The value of ΔG_{rxn}^o can change significantly with respect to temperature, as the energetically favorable state of a system changes with temperature. Therefore, in order to quantify the spontaneity of possible reactions that may occur during solution process, the ΔG_{rxn}^o

at our annealing temperature, 520 °C (793 K), should be calculated. We already showed in Section 2.3.1 that upon annealing, our ZTO solution generates hydroxide intermediates (i.e., $Zn(OH)_2$ and $Sn(OH)_4$) via thermal decomposition, Equation (2.1). Therefore in order to calculate the thermodynamically-favorable chemical reactions between our ZTO solution and bottom metal, we choose $Zn(OH)_2$ and $Sn(OH)_4$ along with PdO and Mo as the possible reactants. The ΔG_{rxn}^{o} of redox between these reactants are calculated in order to explain *in situ* reactions of bottom metals occurring during solution process. The results are shown in Figure 3.7 where the ΔG_{rxn}^{o} of the following reactions were calculated separately: redox of PdO with $Zn(OH)_2$ and $Sn(OH)_4$ (Figure 3.7 (a)), and redox of Mo with $Zn(OH)_2$ and $Sn(OH)_4$ (Figure 3.7 (b)). These calculations reveal that by interacting with the hydroxides, PdO reduction and Mo oxidation will occur spontaneously at our post-annealing temperature of 520 °C (793 K). For comparison, we note here that SiO_2 and Al_2O_3 have very large negative standard molar enthalpies of formation ($\Delta_f H^{o}$ of SiO_2 is -910.7 kJ/mol, and that of Al_2O_3 is -1675.7 kJ/mol) and therefore the glass substrate or alumina layer used for bottom-gate TFTs in Chapter 2 do not interact with the ZTO layer.
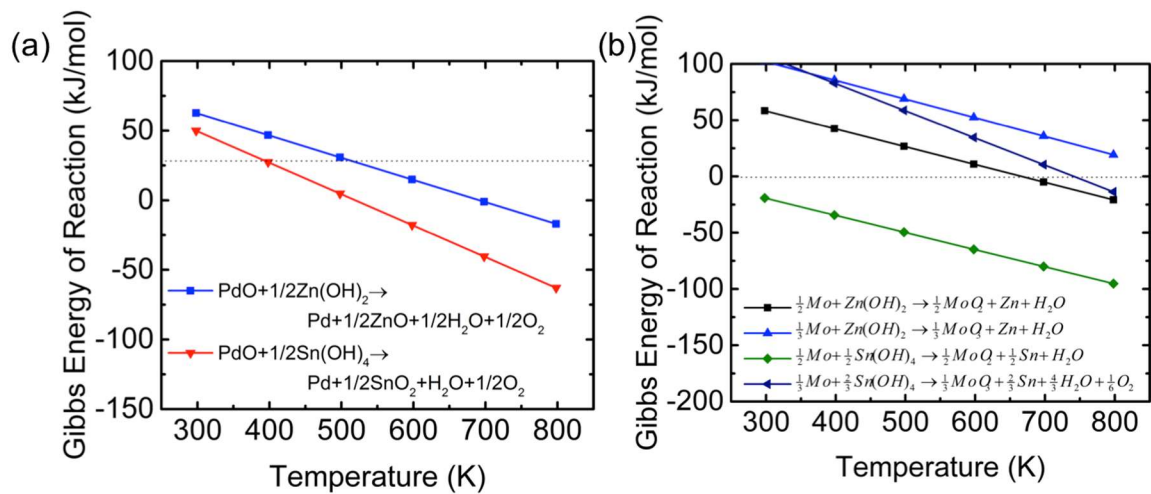
Figure 3.9 Gibbs free energy of reaction calculated for (a) reduction of PdO during dehydroxylation of $Zn(OH)_2$ and $Sn(OH)_4$ and (b) oxidation of Mo during dehydroxylation of $Zn(OH)_2$ and $Sn(OH)_4$.

In case of the bottom Mo layer, we observed that the metal not only oxidizes but also diffuses into ZTO (Figure 3.10 (a)). According to its oxidation states, it appears that the diffused Mo substitutes for Zn and Sn in ZTO. On the other hand, Pd did not exhibit diffusion even though the process condition was identical to that of Mo. We propose that one of the key factors driving diffusion is the ionic radius of the bottom metal. The ionic radii of metal ions in an oxide have been shown to be an important factor in determining how well the metal ions can mix. For ZTO, the high co-solubility of ZnO and SnO_2, which enables a amorphous morphology that is stable up to $> 600°C$, is achieved due to the similar ionic radius of Zn^{2+} (0.083 nm) and Sn^{4+} (0.071 nm). Mo in its ionized state, i.e., Mo^{6+}, has an ionic radius of 0.062 nm, which is only slightly smaller than that of Zn^{2+} and Sn^{4+}. It was reported by others [147]–[149] that due to its small but similar size, Mo^{6+} can effectively substitute for both Zn^{2+} and Sn^{4+} within their oxides. In contrast, the ionic radius of Pd in PdO is 0.100 nm, which is significantly larger than that of Zn^{2+} and Sn^{4+} (Figure 3.10 (b)). The large ionic size of Pd^{2+} likely prevents its diffusion into ZTO, thus enabling the abrupt junction observed at the Pd:ZTO interface. By comparing the ionic radii of Mo^{6+}, Pd^{2+}, Zn^{2+} and Sn^{4+}, we suggest that diffusion and incorporation of the bottom metal atoms into the AOS layer can dominate when the metal ionic radius is small/similar to that of the host metal ions in AOS. Therefore, in addition to evaluating the ΔG_{rxn}^{o} to predict possible redox mechanisms, the ionic radii of metal ions become an important criterion to determine the likelihood of diffusion during solution process.
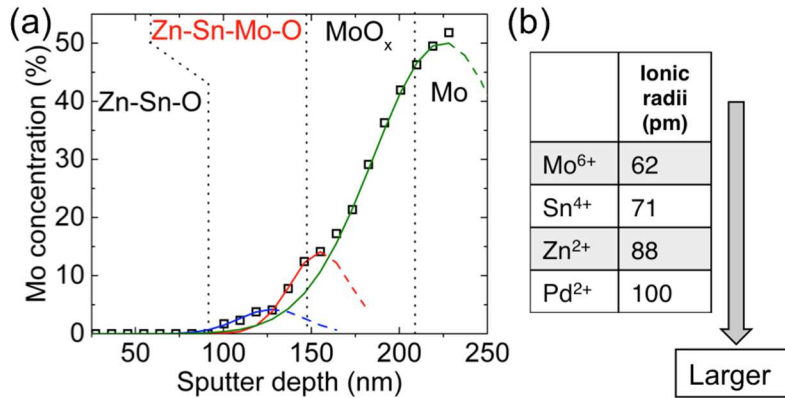
Figure 3.10 Mo diffusion into ZTO during ZTO deposition (a) Mo atomic concentration over depth, obtained from Figure 3.6 (a). The obtained Mo distribution is a result of a very complicated scenario, in which simultaneous inter-diffusion of four elements (Mo, Zn, Sn, and O) occurs during layer-by-layer solution dispensing and annealing. Due to the multilayer structure, the diffusivities of each element can dynamically vary over time and space. (b) Comparison of ionic radii of various metal cations, where smaller ionic size of Mo^{6+} can ease its diffusion into Zn-Sn-O, compared to Pd^{2+}.

The methodology we established here to explain thermodynamically favorable states and diffusion mechanisms can be further applied to understand and tune the metallic interfaces of other oxides, especially when high-temperature processing is required. Although this study was done with solution-processed oxides, the same methods can be used with vacuum-deposited oxides, guided by the same kinetics and thermodynamics. The only difference in vacuum-deposited oxides is that the electrode interacts with the complete oxide, instead of hydroxide intermediates, used here to model the chemical evolution of our solution process. Therefore for vacuum deposition case, the oxidation energy of complete metal oxides can be compared directly to estimate redox mechanism [150]. In Figure 3.11, we provide a schematic that illustrates ionic radii and oxidation energy of various metal oxides.
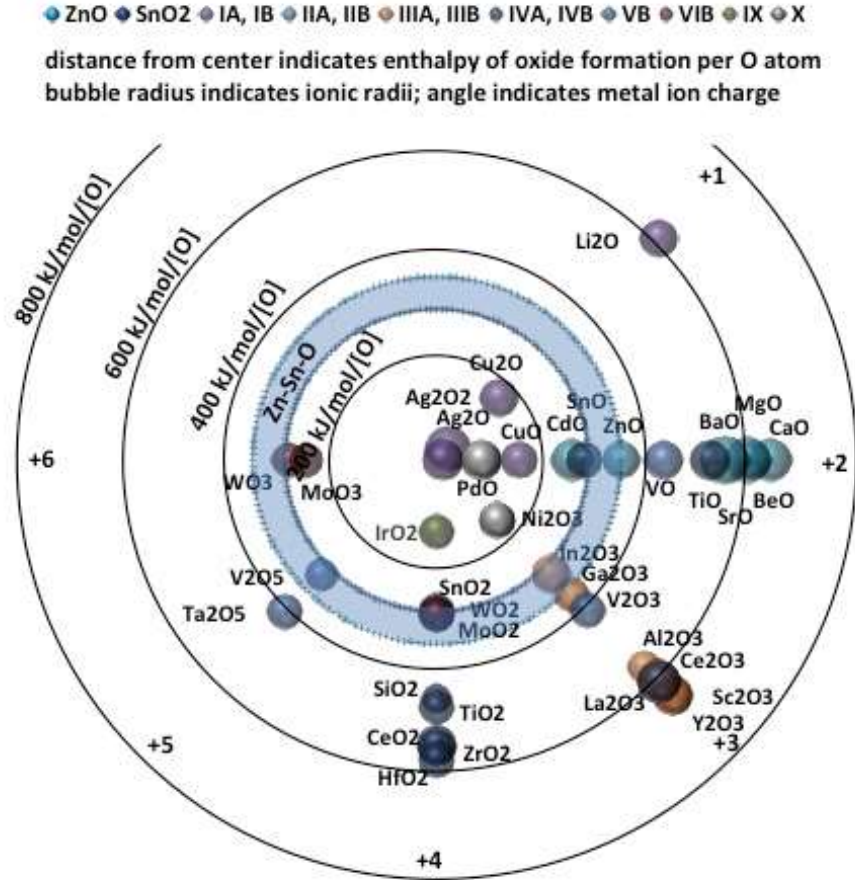
Figure 3.11 Schematic of ionic radii (illustrated by the size of the bubble) and oxidation energy per oxygen atom (illustrated by the distance from the origin) for different metal ions. For metallic junctions of vacuum-deposited oxides, this plot can be used to estimate possible redox and diffusion mechanism.

3.4 Conclusion

In this chapter, we have shown that when solution processing and thermal annealing of a metal oxide semiconductor is performed on top of a metal electrode, redox reactions and diffusion need to be considered to control the contact properties, in addition to work function alignment. This requires consideration of the Gibb's free energy of possible redox mechanisms and comparison of cation ionic radii. Based on these understandings, the interfacial chemical

reactions can be intentionally designed to tune the interface properties for a variety of metal / oxide semiconductor junctions and thus optimize their device performance.

We also present a novel way of forming a high-quality Schottky interface between a bottom metal electrode and solution-deposited ZTO. We experimentally demonstrate this by using two metals (i.e., Pd and Mo), which undergo different mechanisms to form a Schottky interface. The solution process requires thermal annealing to form an oxide semiconductor film from metal precursors. During this process, *in situ* chemical modification of the bottom metal-semiconductor interface occurs. When preceded by oxidation of palladium using oxygen plasma, this *in situ* process reduces palladium and forms a rectifying contact to solution-deposited ZTO. Oxygen plasma treatment on palladium before ZTO-deposition, was necessary to reduce oxygen-deficiencies near the interface. On the other hand, molybdenum, without the need of oxidation step, oxidizes *in situ* during solution process to form a rectifying contact.

We used XPS and SEM measurements to show that plasma oxidation of Pd indeed created an oxygen-rich PdO_x layer, and that it was then reduced back to metallic Pd during ZTO processing. The presence of an oxygen-rich interface during ZTO film formation reduced oxygen vacancy-related defects near the metal-semiconductor interface, improving the Schottky contact. In contrast, our XPS and SEM measurements on Mo:ZTO junction revealed that Mo, without oxygen plasma treatment, oxidized during ZTO deposition, and created ~50 nm of MoO_x layer that functions as a high work function, rectifying contact. This was also confirmed by observing the vertical distribution of Mo with various oxidation states. In addition to forming a rectifying contact, Mo also diffused into ZTO, creating a Mo-doped ZTO (or ZTMO) region ~80 nm thick. The effect of this ZTMO layer on the electrical performance of the Mo:ZTO diode will be explained in the following chapters. Using thermodynamic and kinetic analysis to determine the

Gibbs free energy and assess the ionic radii of the metal cations, we were able to postulate the redox mechanisms at the interface and the formation of an interfacial layer via diffusion.

To the best of our knowledge, this is the first demonstration of vertical Schottky-only diodes using solution-processed AOS. For both PdO_x:ZTO diodes and Mo:ZTO diodes, a rectification ratio greater than 10^2 was achieved. The vertical architecture enables high current-carrying capability: for a circular top electrode diameter of 50 μm (i.e., device area of $<2\times10^{-5}$ cm^2), the PdO_x:ZTO diode can flow an on-current of ~18 mA at +1 V and the Mo:ZTO diode can flow ~2 mA at +3 V. While the PdO_x:ZTO diode show a higher on-current than the Mo:ZTO diode, the off-current is also much higher and increases with bias, leading to high leakage in off state. The other critical weaknesses of PdO_x:ZTO diode, which limits its practical use in power rectifiers, can be overcome by Mo:ZTO diode. This will be characterized in the following chapters.

Chapter 4 Charge transport analysis of bottom-Schottky V-TFD

4.1 Introduction

In Chapter 3, we established rectifying contact formation mechanism in between bottom metal and a-ZTO film deposited in air. Using the reduction of PdO_x or oxidation of Mo, we showed that the vertical diodes can be made via solution process. The I-V and C-V measurements taken on these diodes confirmed their rectifying behavior. Despite the rectifying behaviors, they still exhibit non-ideal diode curves, which limit them from higher performance. First, both of these diodes show low on/off ratio, $>10^2$, and especially PdO_x:ZTO diode shows a reverse current that increases with respect to reverse bias. Second, despite the high on-currents compared to lateral devices, the on-current of Mo:ZTO diode does not follow an ideal diode equation (Equation (4.1)); on-current does not increase exponentially with respect to the voltage. PdO_x:ZTO diode does follow this equation, but the ideality factor obtained is ~1.9, which is much higher than an ideal case of one. Therefore, further analysis should be made so as to address the origin of these non-ideal behaviors.

For the purpose of addressing the origin, the charge transport mechanisms will be analyzed with the help of temperature-dependent electrical measurements. Although the temperature-varying studies of vacuum-deposited AOS Schottky diodes have been performed by several groups [118], [151]–[154], their analyses were conducted in a limited fashion: i) They were only performed for a-IGZO Schottky diodes, but not a-ZTO, ii) the charge transport analysis were obtained only for forward current, but not the reverse current, and iii) the forward

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current analyses were limited to temperatures above 120 K, as below this temperature, the deviation from general Schottky theories has been observed which was not explained. In order to overcome these limitations, we perform temperature-varying measurement to analyze charge transport mechanisms in our a-ZTO vertical Schottky diodes, both PdO$_x$:ZTO and Mo:ZTO diodes. Here we conduct on-current analysis down to 80 K, which revealed that for AOS diodes, the bulk of AOS film can dominate overall charge transport instead of the Schottky interface, leading to deviation from general Schottky theories. This dominance of bulk is closely related to subgap states in AOS. Among various subgap states, the localized tail states below the conduction band in AOS [10] are closely related to its electrical performance [155], [156]. Much work has been done on analyzing the effect of tail states on AOS TFT device performance, including temperature-dependent current measurements [50], [85], capacitance measurements [157], [158], photo-current measurements [159], and other optical measurements [160]. In contrast, there has been no such study done for AOS Schottky diodes, which is one of the motivations of this work. Also for the first time, the reverse currents of the two diodes will be analyzed in order to address the origin of their high reverse currents. As will be shown, the reverse current is determined not only by the potential barrier at Schottky interface, but also by deep-level defects within AOS near the interface.

4.2 Theoretical background

4.2.1 Charge transport theories across Schottky contact

The Schottky diode equation generally follows the form,

$$J = J_s \left\{ \exp\left[\frac{q(V - J \cdot A \cdot R_S)}{n\text{k}T}\right] - 1 \right\},$$
(4.1)

where J_s is the saturation current density, V is the externally applied voltage, T is the temperature, k is Boltzmann's constant, A is the area of the device, q is the electronic charge, and n is the ideality factor. R_s is a series resistance to the ideal diode.

The various current transport theories over the Schottky barrier are present that lead to the derivation of Equation (4.1). Unlike pn junction where the diffusion of minority carriers is the main current transport in forward bias, the current through the Schottky barrier is dominated by the transport of majority carriers, and their transport processes determine the derivation of Equation (4.1). For n-type semiconductor, these include (i) thermal emission of electrons from semiconductor to metal over the potential barrier, (ii) the diffusion of electrons through the depletion region, and (iii) quantum mechanical tunneling of electrons from semiconductor to metal through the potential barrier. (i) is called thermionic emission theory, (ii) is called diffusion theory, and (iii) is called field emission theory. Although the combination of these three different theories lead to the derivation of what are called thermionic field emission theory and thermionic emission diffusion theory, here we distinguish the former three mechanisms for understanding their assumptions and derivations.
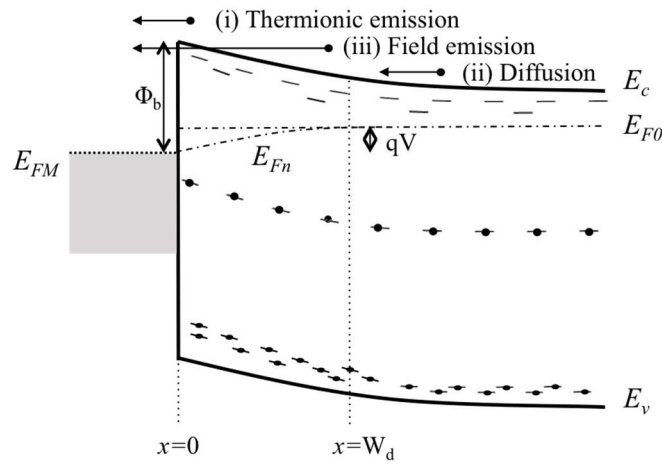
Figure 4.1 An illustration of three basic charge transport mechanisms in forward biased Schottky contact: (i) Thermionic emission, (ii) diffusion, and (iii) field emission. During derivation, thermionic emission assumes E_{Fn} within depletion region is straight, while diffusion theory assumes it to be inclined.

i) Thermionic emission theory

Thermionic emission (TE) theory derives the on-current density by calculating thermal injection of free electrons over the potential barrier. The free electron density at the Schottky interface is calculated by

$$n = N_C e^{(E_{Fn}-E_C)/kT} = N_C e^{-q(\phi_b - V)/kT},\qquad (4.2)$$

where E_{Fn} is the quasi Fermi-level, Φ_b is potential barrier, and V is the applied voltage. This equation assumes that the quasi Fermi-level within the depletion region is flat, which is valid only when the diffusion length (L_D) is longer than the depletion region width (W_d). TE theory assumes that on current is dominated by thermal injection of free carrier density, n, in Equation (4.2), the x-axis average thermal velocity of which would be $v_{thx} = -\sqrt{2kT/\pi m_n}$, where m_n is the effective mass of electron. Then overall on-current density,

$$J = J_{S \to M} - J_{M \to S} = -\frac{1}{2} q v_{thx} (n_{S \to M} - n_{M \to S}) = \frac{4\pi q m_n k^2}{h^3} T^2 \{ e^{-q(\phi_b - V)/kT} - e^{-q\phi_b/kT} \}$$

$$= \frac{4\pi q m_n k^2}{h^3} T^2 e^{-q\phi_b/kT} (e^{qV/kT} - 1) = A^* T^2 e^{-q\phi_b/kT} (e^{qV/kT} - 1), \qquad (4.3)$$

where $A^* = \frac{4\pi q m_n k^2}{h^3}$ is the Richardson constant. Therefore, in TE theory, the saturation current in Equation (4.1) should follow:

$$J_s = A^* T^2 \exp\left[\frac{q\phi_b}{kT}\right]. \qquad (4.4)$$

Therefore, if TE theory were valid, *ln (J_s/T^2)* vs. *1000/T* plot, so-called Richardson plot, should show a straight line, and such evaluation method is often used to confirm the validity of TE theory.

ii) Diffusion theory

However, the assumption that E_{Fn} is flat in depletion region might not be valid when the diffusion length (L_D) is comparable with the depletion region width (W_d). In that case, the excess majority carrier within the depletion region will reduce due to recombination and therefore, E_{Fn} will start from E_{F0} at the edge of depletion region (i.e., $x=W_d$) and drop to E_F of metal (E_{FM}) as it reaches the metal (i.e., $x=0$) (Figure 4.1). In this scenario, free electron density at the interface follows $n(0) = N_C \exp\left[\frac{-q\phi_b}{kT}\right]$, and that at the edge of depletion region follows $n(W_d) = N_C \exp\left[\frac{(E_{F0}-E_C)}{kT}\right]$. Also in this scenario, the energy level of the bottom of conduction band, E_C, referenced from the E_F of the metal, follows $E_C(0)=q\Phi_b$ and $E_C(W_d)=E_{F0}-E_C+qV$. Then the drift and diffusion current at point x, $J(x) = qD_n\left(\frac{n}{kT}\frac{dE_c}{dx} + \frac{dn}{dx}\right)$, when multiplied by $exp\left(\frac{E_c(x)}{kT}\right)$ to be integrated from $x=0$ to $x=W_d$, leads to $\int_0^{W_d} J(x)exp\left(\frac{E_c(x)}{kT}\right) dx = qD_n\, n(x)exp\left(\frac{E_c(x)}{kT}\right)\Big|_0^{W_d}$. For continuous current, $J(x)$ will be constant, J, and using the boundary condition at $x=0$ and $x=W_d$,

$$J = \frac{qD_n n(x)exp\left(\frac{E_c(x)}{kT}\right)\Big|_0^{W_d}}{\int_0^{W_d} exp\left(\frac{E_c(x)}{kT}\right)dx} \approx q\mu_n N_C E_S exp\left(\frac{-q\phi_b}{kT}\right)\left\{exp\left(\frac{qV}{kT}\right) - 1\right\}. \tag{4.5}$$

Therefore, in diffusion theory, the saturation current in Equation (4.1) should follow:

$$J_s = q\mu_n N_C E_S \exp\left[\frac{q\phi_b}{kT}\right]. \tag{4.6}$$

iii) Field emission theory

Other than thermal injection over the barrier and drift and diffusion current within the depletion region, there can be another possible transport process for electron: tunneling directly through the potential barrier. This is feasible when the potential barrier is so thin that the wave function of electron in semiconductor can penetrate through the barrier and exist in metal side.

This is usually the case for heavily-doped semiconductors which lead to thin depletion width. This happens when tunneling parameter, $E_{00} \gg kT$, where

$$E_{00} = \frac{qh}{4\pi} \sqrt{\frac{N_{depl}}{\varepsilon_s \varepsilon_o m^*}}. \tag{4.7}$$

The detailed derivation and resulting *J-V* equation can be found in ref. [135], [161], where tunneling current is calculated by $J = \frac{A^{**}T^2}{kT} \int_{E_{FM}}^{q\phi_b} F_s\, T(E)(1 - F_m)dE$. F_s and F_m are the Fermi-Dirac distribution functions of semiconductor and metal respectively, and *T(E)* is the tunneling probability at energy level, *E*.

4.2.2 Models to explain non-ideal behavior

Equation (4.3) and (4.6) indicates that based on either thermionic emission or diffusion theories, ideality factor *n* in Equation (4.1) should be unity. However, most of the experimental data measured from Schottky diodes, including our V-TFDs, show ideality factor much higher than one. Although *n* being slightly higher than one (<1.1) could be understood with the additional tunneling current (i.e. field emission), *n* much higher needs to be understood with other explanation. Various models to explain this non-ideal behavior have been introduced. They include (i) inhomogeneous barrier model, (ii) interfacial layer model, (iii) image force lowering, and (iv) generation-recombination in space-charge region. Here, we introduce (i) and (ii) for our future analysis.

i) Inhomogeneous barrier model
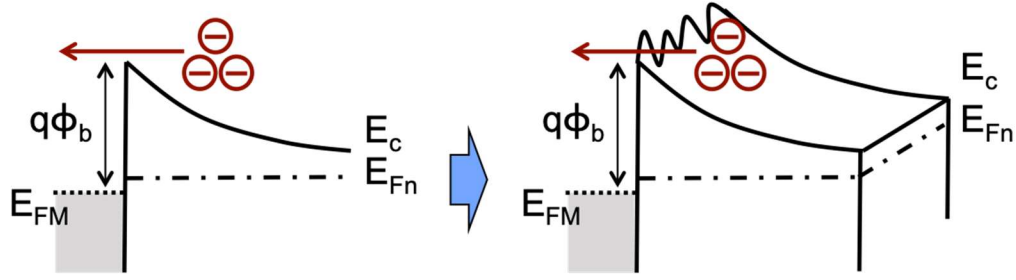
Figure 4.2 The illustration showing the model of spatially inhomogeneous barrier (on the right) compared to ideal Schottky theories which assume spatially homogeneous barrier (on the left).

Based on Equation (4.1) and (4.4), TE theory guides temperature-independent ϕ_b and n. However, *Werner et al.* [162] showed that even when the charge transport over the Schottky barrier is dominated by ideal TE theory, when the potential barrier is spatially non-uniform, the measured *J-V* characteristics can show temperature dependence of ϕ_b and n. The mathematical derivation of this temperature dependence was done with the assumption that the inhomogeneous barrier, ϕ_b, follows Gaussian distribution:

$$P(\phi_b) = \frac{1}{\sigma_s\sqrt{2\pi}} e^{-(\bar{\phi}_b - \phi_b)^2/2\sigma_s^2},\tag{4.8}$$

where $\bar{\phi}_b$ is the mean potential barrier and σ_s is standard deviation. $P(\phi_b)$ is the probability density function: $\int_{-\infty}^{\infty} P(\phi_b)\, d\phi_b = 1$. Under this assumption, the on-current density by TE theory in Equation (4.3) now becomes

$$J = J_{S\to M} - J_{M\to S} = \int_{-\infty}^{\infty} A^* T^2 \{e^{-q(\phi_b - V)/kT} - e^{-q\phi_b/kT}\} P(\phi_b) d\phi_b =$$

$$A^* T^2 \left\{\int_{-\infty}^{\infty} e^{-q\phi_b/kT} P(\phi_b) d\phi_b\right\}(e^{qV/kT} - 1).\tag{4.9}$$

Comparing Equation (4.9) with Equation (4.3) indicates, that potential barrier extracted from measured *J-V* characteristics based on ideal TE theory, ϕ_b^j, has the following relationship with the potential barrier distribution: $e^{-q\phi_b^j/kT} = \int_{-\infty}^{\infty} e^{-q\phi_b/kT} P(\phi_b) d\phi_b$. The right hand side

of this equation needs the following scalings to be simplified: $u = q\,(\phi_b - \bar{\phi}_b)/kT, \sigma_{s,T} =$

$q\,\sigma_s/kT, \phi_{b,T} = q\,\phi_b/kT, \bar{\phi}_{b,T} = q\,\bar{\phi}_b/kT$, which leads to $e^{-q\phi_b^j/kT} =$

$e^{-\bar{\phi}_{b,T}} \frac{1}{\sigma_{s,T}\sqrt{2\pi}} \int_{-\infty}^{\infty} e^{-u} e^{-u^2/2\sigma_{s,T}^2} du = e^{-\bar{\phi}_{b,T}+\sigma_{s,T}^2/2}$. This retrieves the relationship between

effective potential barrier extracted using Equation (4.4), ϕ_b^j, and actual inhomogeneous barrier,

ϕ_b, with its mean $\bar{\phi}_b$ and standard deviation σ_s.

$$\phi_b^j = \bar{\phi}_b - q\,\sigma_s^2/2kT \ . \tag{4.10}$$

Therefore, ϕ_b^j extracted from Equation (4.4) show a certain temperature dependence based on

inhomogeneous barrier model: ϕ_b^j should be linear with respect to *1/T*.

When this spatially non-uniform potential barrier is accompanied by a certain bias

dependence, it leads to *n* to be non-ideal values. To illustrate, if the distribution of ϕ_b with

Gaussian distribution change with respect to bias, $\bar{\phi}_b$ and σ_s^2 will become function of bias (i.e.,

$\bar{\phi}_b(V)$ and $\sigma_s(V)^2$) and Equation (4.10) can be rewritten as $\phi_b^j(V) = \bar{\phi}_b(V) - q\,\sigma_s(V)^2/2kT$.

Then, Equation (4.9) can be also rewritten

$$J = A^* T^2 e^{\bar{\phi}_b(V)-q\sigma_s(V)^2/2kT} (e^{qV/kT} - 1). \tag{4.11}$$

Then, the ideality factor, *n*, by equating Equation (4.11) with Equation (4.1) without R_S can be

expressed as

$$\frac{1}{n} - 1 = -\frac{\left(\bar{\phi}_b(V)-\bar{\phi}_b(0)\right)}{V} + \frac{q(\sigma_s(V)^2-\sigma_s(0)^2)}{2kT}. \tag{4.12}$$

Note that if $\bar{\phi}_b$ and σ_s^2 are not affected by bias and $\bar{\phi}_b(V) = \bar{\phi}_b(0)$ and $\sigma_s(V)^2 = \sigma_s(0)^2$, *n=1*

in Eq (4.12). However, if $\bar{\phi}_b$ and σ_s^2 were linearly dependent to the voltage,

$$\bar{\phi}_b(V) = \bar{\phi}_b(0) + \gamma V \text{ and } \sigma_s^2(V) = \sigma_s^2(0) - \xi V, \tag{4.13}$$

then Equation (4.12) becomes

$$\frac{1}{n} - 1 = -\gamma - \frac{q\xi}{2k}. \tag{4.14}$$

Therefore, if the non-uniform barrier ϕ_b, with $\bar{\phi}_b$ and σ_s, changes with respect to bias following Equation (4.13), then n^{-1}-1 would show linear relationship to $1/T$ based on Equation (4.14).

ii) Interfacial layer model

Although inhomogeneous ϕ_b in Figure 4.2 may lead to a certain distribution described by $\bar{\phi}_b$ and σ_s in (i), it does not explain the physical origin of their bias-dependence, described by Equation (4.13). An inhomogeneous ϕ_b only leads temperature dependence of ϕ_b^j by Equation (4.10) and therefore, unless diodes need to be used at wide range of operation temperature, its effect on device applications may be trivial. In contrary, bias-dependence of ϕ_b in Equation (4.13) is a critical matter for diode performance, especially its switching characteristics, quantified by n. The voltage-induced deformation of ϕ_b, quantified by the coefficients ξ and γ in Equation (4.13), leads n to be higher than one, since Equation (4.14) holds. If ξ>0 and γ>0 from Equation (4.13), forward bias (V) not only narrows the inhomogeneity distribution but also increases the mean Schottky barrier, $\bar{\phi}_b$. The origin of this increase can explained by interfacial layer theory [163]. In the presence of thin interfacial layer, the potential change across this layer and the occupation of interface states at forward bias can lead to linear bias dependence of ϕ_b:

$$\phi_b = \phi_{b0} + \left(1 - \frac{\varepsilon_i \varepsilon_o}{\varepsilon_i \varepsilon_o + q^2 N_{ss}\delta}\right)V, \tag{4.15}$$

where ε_i is relative permittivity of interfacial layer, δ is its thickness, and N_{ss} is the interfacial states distributed within this layer. The lower N_{ss} and δ are, the less bias-dependent ϕ_b becomes.

Therefore, making a Schottky contact with the thinnest interfacial layer with minimum amount of interfacial states can lead to ideal switching of V-TFD with *n* near one.

4.2.3 Charge transport mechanisms in the bulk of AOS

i) Ohmic conduction

All semiconductors possess donors or acceptors that can provide free mobile charge carriers internally within the bulk. When the semiconductor is in contact with metal, which is an effective source of carriers, these carriers can be injected into the semiconductor under the applied external field, forming "space-charge" within the bulk of semiconductor. If the impurity content is high such that semiconductors have sufficient mobile carriers internally, then externally injected space-charge is only significant in the vicinity of the contacts. In this scenario, the mobile carrier density in the bulk of the semiconductor (n_{free}) is determined predominantly by the impurity (i.e., donor for n-type) density. Therefore, for normally-doped semiconductors, a relatively small, applied fields are able to produce large current. The total current is then mainly due to the band-like transport of free electrons thermally generated in the bulk. This conduction, modeling the current flowing through the bulk of semiconductor by a drift of free electrons generated internally by the impurities within, is called ohmic conduction. The drift current can thus be expressed as:

$$J = q\mu_o n_{free}E, \tag{4.16}$$

where μ_o is the band mobility, and E the electric field that drives this current. Thus, the current through the bulk semiconductor is linearly proportional to the electric field.

When the bulk of semiconductor shows ohmic conduction, it implies that relaxation time of the semiconductor (τ_r) is shorter than the carrier transit time (τ_t) and thus injected carriers will redistribute themselves in maintaining electric charge neutrality. Thus, the excess energy electrons gain from the e-field between collisions is smaller than mean electron thermal energy (kT), and can be satisfactorily dissipated during collision.

ii) Trap-free space-charge limited current (SCLC)

The situation changes when we deal with dielectric materials or semiconductors with low n_{free}. Even for these materials, as long as injected carriers due to external field do not overcome thermally generated carriers, the condition for ohmic conduction still holds. Thus, at very low forward bias with limited injection, these materials follow ohmic conduction. If the applied voltage V is smaller than V_{tr} (referred as transition voltage), the injected carriers will redistribute themselves with a tendency to maintain electric charge neutrality internally in a time comparable to τ_t. Consequently, the injected carriers are dissipated before travelling across the material.

This ohmic conduction no longer predominates in the case of strong injection. When $V>V_{tr}$ for materials with low n_{free}, the injected excess carriers start to dominate the thermally generated carrier since the excess carrier transit time (τ_t) is too short for their charge to be relaxed by the thermally generated carriers (τ_r). In this situation, the excess energy gained from the field is now comparable with kT and ohmic conduction no longer holds. In this case, the material capped with two electrodes can be thought as capacitor, that stores charge Q in its interior space when given voltage is V. Thus,

$$Q=CV, \tag{4.17}$$

where C is the capacitance density of the dielectric, $C = \varepsilon_r\varepsilon_o/d$. For a given transit time T, the stored charge Q transits from injecting electrode to collecting electrode, leading to a current

$$I=Q/T. \tag{4.18}$$

For electrode spacing d, as the charge Q will travel the dielectric through drift, $T=d/E\mu=d^2/V\mu$. Combining Equation (4.17) and Equation (4.18), we get current equation for insulator under strong injection, which is called as Child's law: $J = 9\varepsilon_r\varepsilon_o\mu_oV^2/8d^3$, where ε_r is the dielectric constant and ε_o is the permittivity of free space. This current derived using Equation (4.17) and (4.18) is referred as space-charge limited current (SCLC), as it is limited by the space charge stored in insulator. Child's law indicates that when SCLC dominates in a trap-free medium, due to its $J \propto V^2$ relationship, $ln\ J$ vs. $ln\ V$ should show the straight line, with its slope being an exponent, $m=2$.

iii) SCLC limited by distribution of trap states

When the dielectric has traps distributed in its subgap, however, the Q in Equation (4.18) need to be distinguished from that in Equation (4.17). Thus, Child's law needs modification. When there are trap states in dielecric medium, electrons within can be trapped in these states during transport. These trapped charges will contribute to $Q=CV$, but not to $I=Q/T$. Therefore, the ratio between free mobile charge and trapped charge, θ, needs to be considered. Solving this for the dielectric that has traps was done by Rose [164], which we introduce here only for exponential distribution of traps. The DOS of exponential tail states, $g_{tail}(E)$, is illustrated in Figure 4.3 and can be expressed as

$$g_{tail}(E) = g_{tc}e^{(E-E_C)/kT_t}. \tag{4.19}$$
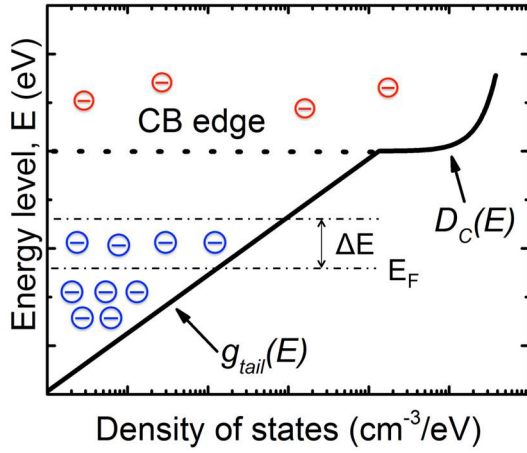
Figure 4.3 The schematic showing density of states when a material has exponential tail states underneath the conduction band edge. The blue electrons indicate trapped charge (n_{trap}) while red ones indicate mobile charge (n_{free}). The dotted line indicates the energy level of conduction band edge, which would be E_C. Reprinted with permission from [165].

The stored charge Q in Equation (4.17) is distributed in three major parts: free charge in CB, trapped charge in between E_C and E_F, charge filled below E_F. With the approximation that charges filled below E_F is dominant, the rise of E_F (ΔE) due to applied voltage can be related to the stored charge, Q, as

$$n_{trap}(E_F + \Delta E) = \int_{E_F}^{E_F+\Delta E} g_{tail}(E)\, dE = \frac{Q}{q} = \frac{VC}{q}. \tag{4.20}$$

Note that this approximation is same as what was made in TLC (Equation (2.8)). (Here, E_F and $E_F+\Delta E$ corresponds to E_{F0} and E_F in TLC.) The substitution of Equation (4.19) into Equation (4.20) gives $\Delta E = kT_t(K + lnV)$, where $K = (E_C - E_F)/kT_t + \ln(C/qN_{tc}kT_t)$. On the other hand, n_{free} for given $E_F + \Delta E$ can be calculated with Boltzmann approximation:

$$n_{free}(E_F + \Delta E) = \int_{E_C}^{\infty} D_C(E)f(E)\, dE = N_C \exp\left[\frac{E_F-E_C}{kT}\right] \exp[\frac{\Delta E}{kT}], \tag{4.21}$$

where N_c is the effective density of states. Substituting $\Delta E = kT_t(K + lnV)$ in above n_{free} equation and calculating n_{free}/n_{trap} leads to

$$\theta = q\, N_c e^{-E_F/kT} e^{\Delta E/kT}/VC = \frac{q\, N_c}{VC} \cdot \left(\frac{VC}{q\, g_{tc}kT_t}\right)^{T_t/T}. \tag{4.22}$$

The overall current from the mobile carriers that make it to the collecting electrode is expressed as:

$$J = \frac{\theta \cdot Q}{T \cdot A} = q N_c \mu_o \left(\frac{\varepsilon_r \varepsilon_o}{q g_{tc} k T_t}\right)^{T_t/T} \frac{V^{T_t/T+1}}{d^{2T_t/T+1}} \propto V^{T_t/T+1}. \tag{4.23}$$

Therefore, when SCLC dominates in dielectric medium with exponential tail states, the on-current follows Equation (4.23). This is referred as SCLC limited by exponential tail states (ET-SCLC), and has been derived by Rose [164]. When this mechanism dominates, *ln J* vs. *ln V* should show the straight line, with its slope being an exponent, *m=l+1*, following Equation (4.23). Also, as *l=kT_t/kT*, the exponent, *m*, should show linear relationship with respect to *1/T* with the slope being kT_t, and the y-axis intercept should be equivalent to one.

iv) Trap-filled SCLC

Even when the material has exponential tail states as was discussed so far, the traps becomes filled at higher bias as E_F rises, and eventually be entirely filled at critical voltage, V_C. After all traps are filled up, the subsequently injected carriers will be free to move in the dielectric films, so that at the critical voltage (V_C) to set on this transition, the current will shift from its low trap-limited value to a high trap-free SCL current. Thus, V_C is defined as the voltage required to fill the traps or, in other words, as the voltage at which Fermi level (E_F) passes through E_t (or E_C for exponential tail states). In this case of very strong injection, all traps are filled and the conduction becomes the fully space-charge-limited. Therefore, observed *J-V* characteristics at this very strong injection follow square law dependence ($J \sim V^2$, Child's law), just as trap-free SCLC case in (ii).

To summarize SCLC, there exist several conditions required for SCLC mechanism to dominate. First, the material should have wider band gap for low generation-recombination rate.

This follows from the fact that τ_t needs to be smaller than τ_r, so that the injected excess carriers dominate the thermally generated carrier. Second, the injecting electrode should be ohmic contact so as to efficiently inject carriers. Third, ohmic conductivity due to carriers generated thermally from impurity or valence band should be small, i.e., n_{free} has to be low enough. This can come from either low doping of material or excess acceptor trap states present to reduce n_{free}. These conditions can be easily met when a material has a wide band gap, low mobility or low mobile carrier density. Thus, SCLC was observed not only from the dielectrics, but was also for semiconductors that meet these requirements, such as organic material [166]–[168] and a-Si [169]–[171].

4.3 PdO$_x$:ZTO diode charge transport analysis

Based on the background knowledge established in Section 4.2, we implement charge transport analysis on both PdO$_x$:ZTO and Mo:ZTO diode. In this section, temperature-dependent current-voltage measurements were taken on PdO$_x$:ZTO diode using a Lakeshore Cryotronics TTPX cryogenic probe station and an HP4156A semiconductor parameter analyzer. All current-voltage measurements were taken in continuous sweep mode with a step voltage of 0.01 V, with medium integration time. A +1 V to -1 V sweep took approximately 30 sec, so that the measurements can be considered quasi-static.

4.3.1 Forward current analysis

i) Thermionic Emission over Inhomogeneous Barrier

The measured *J-V* data are shown in Figure 4.4 (a). At temperatures from 260 K to 340 K, near room temperature, the diodes obey Equation (4.1). Values of n and J_s are extracted from measured *J-V* data in forward bias from 0.1 to 0.2 V while R_S values are extracted from 0.8 to 1.0 V. Figure 4.4 (b) shows the measured forward bias *J-V* curves for temperatures at or above 260 K alongside Equation (4.1) fits. Based on thermionic emission theory, Equation (4.4) holds: $J_s = A^*T^2 \exp\left[-\frac{q\phi_{eff}}{kT}\right]$, where ϕ_{eff} is the effective Schottky barrier height and A^* is the Richardson's constant. If the barrier is homogeneous and thermionic emission theory is valid, ϕ_{eff} is temperature-invariant, $n=1$, and the y-axis intercept of the Richardson plot of *ln (J_s/T^2)* vs. *1000/T* should retrieve *A**. However for our devices, the ideality factor is greater than one and the *A** value retrieved is unreasonably small, 5.4×10^{-4} A·cm^{-2}·K^{-2} (Figure 4.4 (c)). To explain these observations not aligned with thermionic emission theory, we consider various charge transport mechanisms. One possible explanation for this behavior is the occurrence of electron tunneling via thermionic field emission (TFE) [135]. However, the measured temperature-dependent *I-V* data cannot be fit by TFE theory (Figure 4.4 (d) and (e)). Next, recombination current is unlikely to dominate in our a-ZTO diodes as holes in AOS exhibit poor transport qualities due to the existence of broad valence band tail states [172], [173]. Lastly, image force lowering was simulated with 2D Silvaco TCAD simulation [101] which showed that it plays only a marginal role to explain our diode deviation for thermionic emission theory.
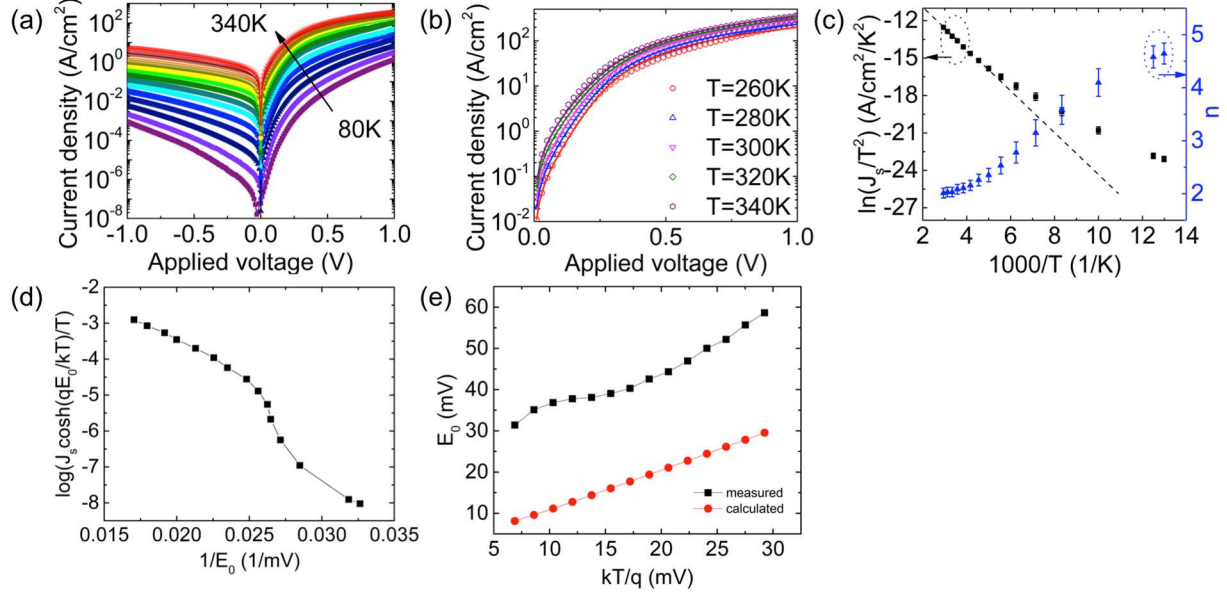
Figure 4.4 Charge transport analysis on PdO$_x$:ZTO diode based on general Schottky theories (a) Measured temperature-dependent *J-V* of PdO$_x$:ZTO Schottky diode. The top Schottky contact is a circle with diameter of 100 μm. (b) Measured data and fit lines for forward bias *J-V* curves for 260 to 340 K. Symbols are experimental data. Solid lines show plots of Equation (4.1), using *n* and ϕ_{eff} values extracted from 0.1 to 0.2 V and R_S values fit from 0.8 to 1.0 V. Richardson plot for measured *J-V* of PdO$_x$:ZTO Schottky diode. The dashed lines shows a fit to $J_s = A^*T^2 \exp\left[-\frac{q\phi_{eff}}{k_B T}\right]$. The extracted value of A^* for this fit line is 5.4×10^{-4} A·cm^{-2}·K^{-2}. This value is unreasonably small. In addition, the ideality factor, *n*, is greater than unity. Therefore, the measured data cannot be explained by thermionic emission over a homogeneous Schottky barrier. (d) Plot of log[J_s cosh(qE_0/kT)/T] vs. $1/E_0$ and (d) comparison of measured E_0 values with those calculated based on the thermionic field emission model (TFE) [135]. Using $J = J_s \exp[V/E_0]$, measured values of E_0 are extracted from the 0.1 V to 0.2 V region of forward bias. Calculated E_0 values are obtained from $E_0 = E_{00}coth(E_{00}/kT)$, where E_{00} is the tunneling parameter, defined as $(qh/4\pi)(N_{depl}/\epsilon_s m^*)^{1/2}$. For m^*=0.34 [131], ϵ_s=19, and N_{depl} =5×10^{17} cm^{-3} (the depletion charge density, which along with the relative permittivity was obtained from measured *C-V* data in [101]), the calculated value of E_{00} is 5.15 meV. If transport is via TFE, plot (d) should show linearity and the plot (e) should show good agreement between measured and calculated E_0 values. Neither of these conditions is true, indicating the invalidity of the TFE model. We also note that TFE or FE transport requires $kT/E_{00} \leq 1$. Here, the calculated value of E_{00} (5.15 meV) is small compared to kT in the given temperature range (80 K to 340 K), and so we are unlikely to observe TFE or FE transport. Reprinted with permission from [165].

Similar *J-V* behavior has been observed for *a*-IGZO [151], [154], nanocrystalline ZnO [153], [174], [175], and crystalline Ga$_2$O$_3$ [176] and has been explained by thermionic emission over an inhomogeneous barrier having a voltage-dependent barrier height. Barrier inhomogeneity theory was explained in Section 4.2.2. (i). In this theory, under the condition followed by Equation (4.13), $\bar{\phi}_b = \bar{\phi}_{b0} + \gamma V$ and $\sigma^2 = \sigma_0{}^2 - \xi V$, where $\bar{\phi}_{b0}$ and σ_0 are the values at zero bias, Equation (4.10) and (4.14) give: $\phi_{eff} = \bar{\phi}_{b0} - \sigma_0^2 q/2kT$ and $n^{-1} - 1 = -\gamma - q\xi/2kT$. Note that the equations for $n^{-1} - 1$ and ϕ_{eff} are both linear with respect to T^{-1}.

The coefficients γ and ξ represent the voltage-induced deformation of the Schottky barrier distribution. This bias-dependency can be physically interpreted as the voltage taken up by interfacial layer with interfacial states, as explained in Section 4.2.2. (ii).

To explain our data using inhomogeneous barrier model, ϕ_{eff} is calculated at each temperature from measured values of J_s, using Equation (4.4). Since no A^* values have yet been reported for zinc tin oxide, we use A^*=41 A·cm^{-2}·K^{-2}, obtained for amorphous IGZO [131]. Near room temperature, from 260 K to 340 K, both ϕ_{eff} and n^{-1}-1 are linear with T^{-1} as predicted by the barrier inhomogeneity model (Figure 4.5 (a)). A linear regression fitting of ϕ_{eff} vs. T^{-1} yields values for $\bar{\phi}_{b0}$ and σ_0. The extracted $\bar{\phi}_{b0}$ value of 0.72 eV is within the expected range based upon the Pd work function, Φ_{Pd}=5.22-5.6 eV [132], and ZTO electron affinity, χ_{ZTO}=4.35-4.6 eV [133], [134]. The value extracted for the potential barrier fluctuation, σ_0=0.12 eV, is close to the values previously reported for a-IGZO (0.13 eV) and ZnO (0.134 eV) Schottky diodes [151], [174]. Therefore, in this temperature and voltage regime (260-340 K, 0.1-0.2 V), charge transport in our Schottky diodes is dominated by thermionic emission over a voltage-dependent inhomogeneous barrier. We note that extracted ξ and γ using Equation (4.14) are positive. Following Equation (4.13), such positive ξ and γ indicate the larger voltages homogenizing the potential fluctuations and increase the mean Schottky barrier, $\bar{\phi}_b$. The increase of effective Schottky barrier at forward bias can be explained by interfacial layer, which indicates that Pd/ZTO junction in our PdO$_x$:ZTO diode may possess interfacial states. XPS depth profile of the Pd/ZTO junction, shown in Figure 3.3, indicated metal alloy formation between Zn, Sn, and Pd, which may have led to undesirable interfacial states. This in turn can lead to ideality factor higher than one. More discussion on interfacial layer will be made in Chapter 6.

Previous reports on Schottky junctions made using a variety of materials [151], [174], [177]–[179], have used the above method combined with a modified Richardson plot to extract values of A^*. By combining Equation (4.1), (4.4), and (4.10), it can be shown that

$$\ln(J_s/T^2) - q^2\sigma_0{}^2/2k^2T^2 = \ln(A^*) - q\bar{\phi}_{b0}/kT. \tag{4.24}$$

To create a modified Richardson plot, the extracted σ_0 value is used to calculate and plot $\ln(J_s/T^2) - q^2\sigma_0{}^2/2k^2T^2$ vs. T^{-1}. A linear regression on the data from 260 to 340 K is used to obtain values of $A^* = 44$ A·cm^{-2}·K^{-2} and $\bar{\phi}_{b0} = 0.72$ eV for our PdO$_x$:ZTO diodes (Figure 4.5 (b)). These values are close to the A^* value used to extract ϕ_{eff} (41 A·cm^{-2}·K^{-2}) and the $\bar{\phi}_{b0}$ value extracted from the ϕ_{eff} vs. T^{-1} plot (0.72 eV).

We note that this method requires an initial assumption for A^* in order to determine σ_0. In order to evaluate the impact of the initial A^* value on the extracted values of A^*, $\bar{\phi}_{b0}$ and σ_0, we repeated the fitting procedure for a range of initial A^* values. The results are shown Figure 4.5 (d). For initial A^* values ranging from 8 to 200 A·cm^{-2}·K^{-2}, σ_0 varies only slightly, from 0.11 eV to 0.13 eV. The extracted values of $\bar{\phi}_{b0}$ vary over a slightly broader range, from 0.64 to 0.80 eV. Inspection of Equation (4.24) indicates that, over a narrow temperature range, a larger value of A^* can be compensated by a slightly larger value of $\bar{\phi}_{b0}$. This leads to the weak positive dependence of extracted $\bar{\phi}_{b0}$ values on the chosen initial value of A^*. The extracted A^* values range from 8.4 to 215 A·cm^{-2}·K^{-2}: this method returns an A^* value close to the initially assumed value. Therefore, we conclude that, for our data, the fitting methodology is robust for obtaining σ_0 values within ±0.01 eV and $\bar{\phi}_{b0}$ values within ±0.08 eV, but it is not possible to uniquely determine a value for A^*.
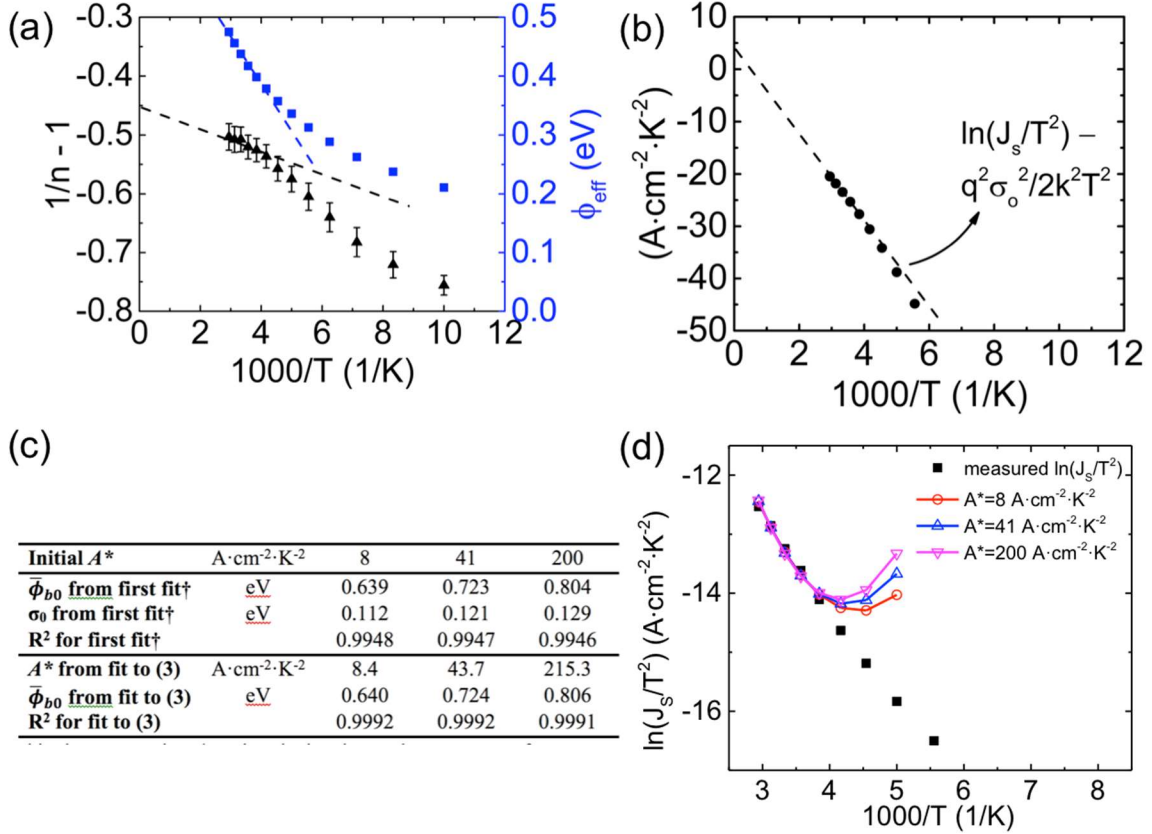
Figure 4.5 Charge transport analysis on PdO$_x$:ZTO diode based on inhomogeneous barrier (a) Plot of ϕ_{eff} and n^{-1}-1 vs. *1000/T* and (b) modified Richardson plot based on the inhomogeneous barrier model. In (a) and (b), symbols indicate values obtained from measured data, while dashed lines indicate linear fits over the temperature range of 260 to 340 K. (c) results of measured data fits for three different initial values of A^*. ϕ_{eff} is calculated at each temperature from measured values of J_s, assuming an initial value of A^*, using $J_s = A^* T^2 \exp\left[-\frac{q\phi_{eff}}{kT}\right]$. Values of $\bar{\phi}_{b0}$ and σ_0 are obtained by linear regression of ϕ_{eff} to T^{-1} using $\phi_{eff} = \bar{\phi}_{b0} - \sigma_0^2 q/2kT$. (d) The fits were performed over a temperature range of 260 to 340 K, and show good fit quality, indicated by $R^2 > 0.994$, where R^2 is the coefficient of determination in the regression analysis. The figure compares measured $\ln(J_s/T^2)$ vs. calculated $\ln(J_s/T^2)$, for thermionic emission over an inhomogeneous barrier. Calculations are done using Equation (4.24), using the extracted values of A^*, $\bar{\phi}_{b0}$, and σ_0 listed in the table. $\ln(J_s/T^2)$ lines are calculated and plotted for three different initial values of A^*. The three lines overlap in the temperature region of interest, 260-340 K. This indicates that, because our diodes obey inhomogeneous barrier theory over a narrow temperature range, the measured data cannot be used to uniquely obtain an A^* value. However the fitting procedure does a robust job of determining values for $\bar{\phi}_{b0}$ and σ_0. Reprinted with permission from [165].

ii) Space-Charge Limited Current

At temperatures below 260 K, the measured *J-V* curves cannot be fitted to Equation (4.1), as shown in Figure 4.6 (a). Instead, the forward bias *J-V* measurements at temperatures from 80 to 240 K follow straight lines when plotted as *ln J* vs. *ln V* Figure 4.6 (b). The $J \propto V^m$

relationship indicates space-charge-limited current (SCLC). SCLC is widely used to explain charge transport in materials with low free carrier density such as dielectrics or semiconductors with wide bandgaps or low doping levels. As explained in depth in Section 4.2.3 [166], [169], [180]–[183], the distribution of traps within the material changes the resulting *J-V* equations. Many previous studies of amorphous oxide semiconductors have observed localized states below the conduction band with an exponential distribution with energy [50], [54], [78], [85], [159], [160], [173]. The exponential density of states in the sub-bandgap region can be expressed using Equation (4.19), $g_{tail}(E) = g_{tc} \exp\left[\frac{E-E_C}{kT_t}\right]$, where E is the electron energy, E_C is conduction band energy level, g_{tc} is the tail state density when $E=E_C$, and kT_t is the characteristic energy of the exponential tail states. The presence of these trap states changes the *J-V* relationship of SCLC, as explained in Section 4.2.3, (iii). For SCLC occurring in the presence of exponential tail states (ET-SCLC), the *J-V* characteristic in Equation (4.23) can be written as [164], [184], [185]:

$$J = \frac{qN_c\mu_o}{2}\left(\frac{2\varepsilon_s\varepsilon_o}{qg_{tc}kT_t}\right)^l \frac{V^{l+1}}{d^{2l+1}} f(l), \qquad (4.25)$$

where $f(l) = \left(\frac{1}{2}\right)^{l-1}\left(\frac{l}{l+1}\right)^l\left(\frac{2l+1}{l+1}\right)^{l+1}$, $l=kT_t/kT$, q is the electronic charge, and N_c is the effective density of conduction band states. For values of l ranging from unity to four, i.e. $0.25T_t < T < T_t$, *f(l)* takes values of 1.125 to 0.9675 and can be approximated as unity. Under this condition, the temperature dependence of the current-voltage relationship for ET-SCLC transport in Equation (4.25) obeys $J \propto V^m$, where the exponent, *m*, is given by $m = l + 1 = \frac{kT_t}{kT} + 1$. For our forward biased *a*-ZTO Schottky diodes, the extracted values of *m* are linear with T^{-1} for temperatures below 260 K (Figure 4.6 (c)), showing that transport occurs via SCLC in the presence of exponential tail states. Fitting the data in Figure 4.6 (c), we extract $kT_t = 0.026$ eV.
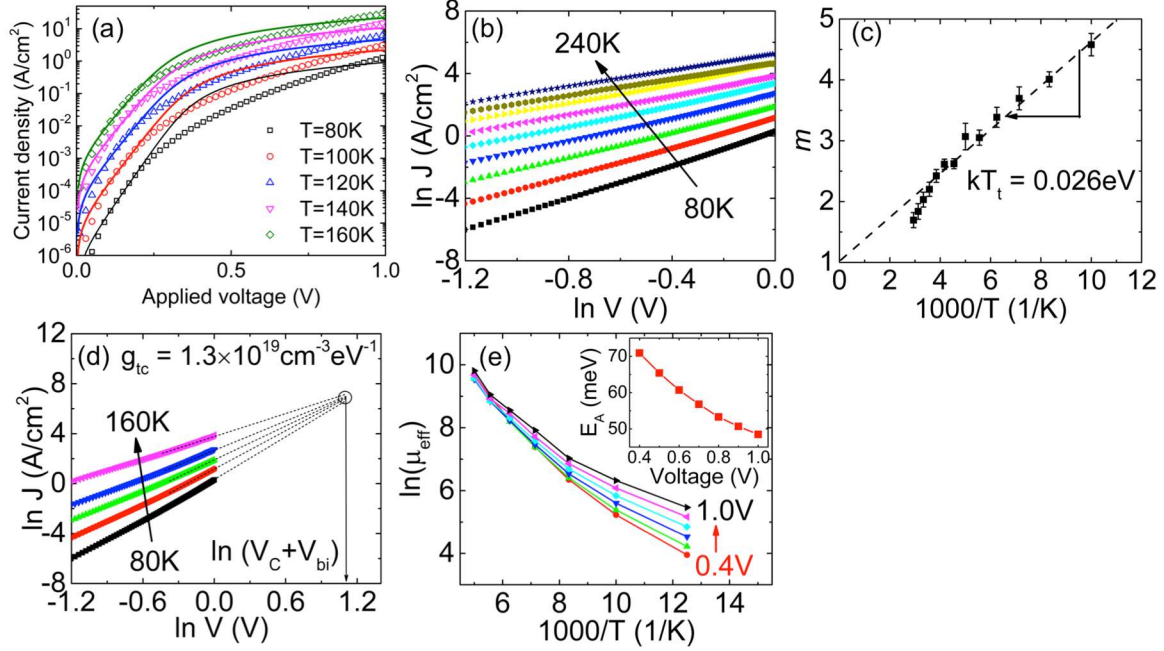
Figure 4.6 Charge transport analysis on PdOx:ZTO diode based on SCLC (a) Measured data and fit lines for forward bias *J-V* curves from 80 to 160 K. Symbols are experimental data. Solid lines show plots of Equation (4.1) and (4.4), using *n* and ϕ_{eff} values extracted from measured data in the 0.1 to 0.2 V region, and R_S values fit to measured data from 0.8 to 1.0 V. Equation (4.1)-(4.4) do not fit the measured data in this temperature regime excluding general Schottky theories such as thermionic emission, thermionic field emission, or thermionic emission/diffusion theory. (b) Forward *J-V* characteristics of the diode plotted as *ln J* vs. *ln V*. Different symbols and colors indicate different temperatures. (c) Exponent *m* of $\boldsymbol{J} \propto \boldsymbol{V^m}$ extracted from *ln J* vs. *ln V*. (d) Temperature-independent critical voltage, V_C, extrapolated from *ln J* vs. *ln V*. (e) shows the decrease of thermal activation at higher forward bias, due to the filling of traps. Reprinted with permission from [165].

In addition to kT_t, the remaining parameter extract $g_{tail}(E)$ is g_{tc}. As forward bias increases and energy bands bend, the localized states fill. They are completely filled at a critical voltage, defined as $V_C = \frac{qg_{tc}kT_t}{2\epsilon_s\epsilon_o}d^2$ [184], [186] as explained in Section 4.2.3, (iv). At this voltage, the diode current is largely independent of temperature:

$$J(V = V_C + V_{bi}) = \frac{q^2 N_C \mu_o g_{tc} kT_t}{4\varepsilon_s\varepsilon_o} \cdot d \cdot f(l) \approx \frac{q^2 N_C \mu_o g_{tc} kT_t}{4\varepsilon_s\varepsilon_o} \cdot d \qquad (4.26)$$

Because the value of V_C is independent of temperature, it can be obtained by extrapolating the *J-V* curves [180], [186] to find the common cross-over point of 3.0 V in Figure 4.6 (d). Using a built-in potential of 0.24 V and a relative permittivity of $\varepsilon_s = 19$ for *a*-ZTO which were

measured from *C-V* measurements in Figure 3.5, we calculate a critical voltage, $V_C = 2.76$ V and thus obtain a tail state density of $g_{tc} = 1.34 \times 10^{19}$ cm^{-3}/eV.

In conclusion, ET-SCLC theory fits our diode experimental data from 80 K to 240 K. This theory dominates at low temperature because when $kT \ll kT_t$, when thermal energy alone cannot excite all of the electrons trapped in the exponential tail states. Here, the density of electrons trapped within the tail states at the bulk (n_{trap}) increases while that of free electrons above conduction band minimum (n_{free}) decreases. When this occurs, $n_{free}/(n_{free}+n_{trap})$ can change dramatically with respect to the external bias, leading to bulk-limited transport via ET-SCLC. For our *a*-ZTO, bulk-limited charge transport (ET-SCLC) dominates diode transport below 240 K, for which $m > 2.5$ in Figure 4.6 (c).

On the other hand, when kT becomes comparable to kT_t, the thermal energy can excite a significant number of free carriers and n_{free} increases while n_{trap} decreases. The value of $n_{free}/(n_{free}+n_{trap})$ approaches unity and becomes weakly dependent on applied bias. The additional thermally-generated carriers ensure that the semiconductor bulk exhibits ohmic conduction by drift of free electrons moving within the conduction band. This ohmic loss contributes to R_S in Equation (4.1). For our *a*-ZTO, this occurs when kT is above 260 K and moderately high diode voltage is applied (> 0.5 V). At lower voltages and near room temperature, charge transport is predominantly via thermionic emission over an inhomogeneous, voltage-dependent Schottky barrier, as described above. Under these conditions, the low on-current ensures that the voltage drop across the bulk ohmic region (i.e. R_S due to n_{free}) is negligible.

Based on ET-SCLC analysis, DOS near CB is extracted (Figure 4.7 (a)). To illustrate the variation in free and trapped charge concentrations with temperature, we calculate n_{free}, n_{trap}, and the ratio $n_{free}/(n_{free}+n_{trap})$ with respect to quasi-Fermi level, E_F, for *a*-ZTO at 100 K and 340 K

(Figure 4.7 (b)). The calculation method, published previously [80], [187], was explained more in depth in Section 2.3.3. We follow Equation (2.9) and Equation (2.10) for n_{trap} calculation, re-written here as $n_{trap}(E_F) \approx \frac{1}{2} g_{tc} kT_t \left(\frac{2(E_c - E_F)}{kT_t} \right)^{T_t/T} \exp[\frac{E_F - E_C}{kT_t}]$ for high temperature

$n_{trap}(E_F) \approx g_{tc} kT_t \exp[\frac{E_F - E_C}{kT_t}]$ for low temperature. The value of n_{free} for a given value of E_F can be calculated using the Boltzmann approximation: $n_{free}(E_F) = N_C \exp\left[\frac{E_F - E_C}{kT}\right]$ [161], where

the effective density of states, $N_c = 2 \left[\frac{m_n^* kT}{2\pi\hbar^2} \right]^{3/2}$, is calculated from the reported m_n^* of amorphous IGZO [131], since no values for zinc tin oxide are available in the literature. Using these equations with the extracted values of $g_{tc} = 1.34 \times 10^{19}$ cm^{-3}/eV and $kT_t = 0.026$ eV, n_{free}, n_{trap}, and the ratio $n_{free}/(n_{free} + n_{trap})$ are calculated for a-ZTO at 100 K and 340 K and plotted in Figure 4.7 (b). As shown, at 340 K, n_{free} and n_{trap} are similar in value, and $n_{free}/(n_{free} + n_{trap})$ is relatively constant with respect to E_F. In this regime, electron transport is via thermionic emission over an inhomogeneous, voltage-dependent barrier with ohmic loss in the bulk semiconductor. In contrast, at 100 K, n_{free} is significantly reduced and $n_{free}/(n_{free} + n_{trap})$ changes dramatically with E_F. In this regime, transport is bulk limited, with space-charge-limited conduction with exponential tail states (ET-SCLC).
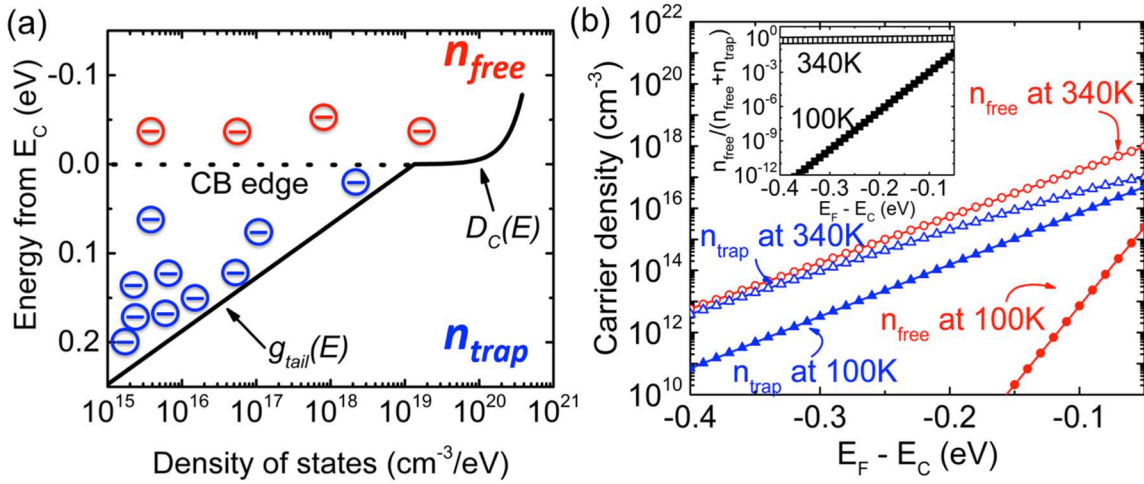
Figure 4.7 (a) Density of states (DOS) in *a*-ZTO near the conduction band (CB) edge. The blue electrons in the figure illustrate trapped electrons, which are localized, and the red electrons illustrate free electrons, which move with band-like transport. The tail state distribution is $g_{tail}(E) = g_{tc} \exp\left[\frac{E-E_C}{kT_t}\right]$, where the values of $g_{tc} = 1.34 \times 10^{19}$ cm⁻³/eV and $kT_t = 0.026$ eV are extracted from experimental data, as shown in Figure 4.6 (c) and (d). $D_C(E)$ is the DOS above the CB edge, $D_C(E) = (\sqrt{2}\, m^{*\,3/2}/\pi^2\hbar^3)\sqrt{E - E_C}$. Since no effective mass has been reported for ZTO, the relative effective electron mass for *a*-IGZO, $m_n^* = 0.34$ [131], is used. (b) n_{free} and n_{trap} calculated at 100 K and 340 K, using experimentally-extracted DOS in (a). The inset shows the ratio $n_{free}/(n_{free}+n_{trap})$. Reprinted with permission from [165].

Previous studies of amorphous semiconductor Schottky diodes have shown one dominant forward bias charge transport mechanism. For example, *a*-IGZO Schottky diodes showed an exponential relationship between current and voltage, and electron transport was explained by thermionic emission over inhomogeneous barrier down to about 160 K [118], [151], [154]. In contrary, *a*-Si Schottky diodes obeyed a power-law *J-V* relationship and thus were explained by SCLC even at temperatures above 300 K [169]–[171]. The observation of different charge transport mechanisms in these two materials is likely due to the very different tail-state distributions present [173]: *a*-IGZO has $g_{tc} = 2 \times 10^{19}$ cm⁻³eV⁻¹ and $kT_t = 20$ meV [78] while *a*-Si has $g_{tc} = 2 \times 10^{22}$ cm⁻³eV⁻¹ and $kT_t = 29$ meV [79]. Our wide-bandgap *a*-ZTO exhibits intermediate values of $g_{tc} = 1.34 \times 10^{19}$ cm⁻³eV⁻¹ and $kT_t = 26$ meV, uniquely allowing experimental observation of the transition between these two charge transport mechanisms as a function of temperature. The difference in tail states between *a*-ZTO and *a*-IGZO may be due to

different cation composition, differences in oxygen and hydrogen-related states, or changes induced in the *a*-ZTO film during the solution-process deposition and annealing. More work is needed to understand the physical origin of the tail states.

4.3.2 Reverse current analysis

Reverse leakage current charge transport was also analyzed using temperature-dependent *J-V* characteristics. The measured data showed linearity when plotted as *ln (J/E)* vs. $\mathcal{E}^{1/2}$ (Figure 4.8), indicating that leakage current is either due to Schottky emission or Poole-Frenkel (PF) emission. Fitting to the Schottky emission equation [188] resulted in a dynamic dielectric constant of ZTO close to that of free space. This is not a physically-sensible result and leads us to reject Schottky emission as the likely transport method in reverse bias.

The conventional PF emission equation [188] assumes a trap-free material with only donor-like states. Following Simmons [189], we modify the model to include neutral traps. The modified PF emission equation can be written as:

$$J = q\mu_o N_C \left(\frac{N_d}{N_t}\right)^{1/2} \mathcal{E} \exp\left[\frac{-(\Phi_t + \Phi_d - q\sqrt{q\mathcal{E}/\pi\varepsilon_r\varepsilon_o})}{2kT}\right], \tag{4.27}$$

where ε_r is dynamic dielectric constant of *a*-ZTO, N_d and N_t are donor and trap densities, respectively, and Φ_d and Φ_t are the discrete energy levels for these states relative to the conduction band. The measured data were fit to Equation (4.27) across a wide temperature region (Figure 4.8). The extracted value of $\Phi_t + \Phi_d$ is approximately 0.4 eV. Because Φ_t for exponential tail states is typically much shallower than Φ_d, this agrees well with the Φ_d values of 0.4 eV previously reported experimentally [159] and theoretically [92] for oxygen vacancy

defects in *a*-ZTO. Therefore, this tells us that the thermal excitation of electrons from V_O defects are the main source of leakage current in PdO_x:ZTO diode. We note that Equation (4.27) assumes a single discrete trap level (with N_t and Φ_t), which is different from continuous distribution of tail states used to describe forward bias transport in *a*-ZTO. Therefore N_t and Φ_t in Equation (4.27) cannot be directly compared with the g_{tc} and kT_t values obtained from the exponential tail state equations. Finally, while the *a*-ZTO ε_s value obtained from *C-V* characteristics is 19 [101], the value of ε_r obtained from Equation (4.27) is about 5. Since thermal excitation of trapped electrons takes place more rapidly than dielectric relaxation, the material does not have enough time to be polarized, causing ε_r to be smaller than ε_s [188], [190].
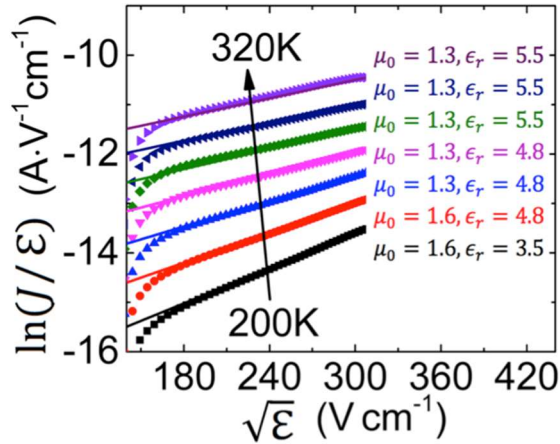
Figure 4.8 Charge transport analysis on reverse current of PdO_x:ZTO diode. Reverse *J-V* characteristics of the diode plotted as *ln (J/$\mathcal{E}$)* vs. $\mathcal{E}^{1/2}$. The different symbols indicate different temperatures and the solid lines show fittings using Equation (4.27). Fit values of μ_o have units of $cm^2 \cdot V^{-1} \cdot s^{-1}$. Reprinted with permission from [165].

4.4 Mo:ZTO diode charge transport analysis

4.4.1 Forward current analysis

Temperature-varying electrical measurements on forward current were performed on Mo:ZTO diode. Unlike Pd V-TFD case, the on-current of Mo V-TFD disobeys Equation (4.1) in

the entire temperature range. In the temperature range of 80 to 340 K, measured on-current always followed power relationship with the voltage ($J \propto V^m$). This is illustrated in Figure 4.9 that when the measured data is ploted in *ln(J)* vs. *ln(V)*, the linear curves are observed in all temperatures. All of the data measured in the temperature range of 100 to 340 K, could be explained with Equation (4.25): *J-V* relationship can be modeled using $J = \frac{qN_c\mu_o}{2}\left(\frac{2\varepsilon_s\varepsilon_o}{qg_{tc}kT_t}\right)^l \frac{V^{l+1}}{d^{2l+1}} f(l)$, where $f(l) = \left(\frac{1}{2}\right)^{l-1}\left(\frac{l}{l+1}\right)^l\left(\frac{2l+1}{l+1}\right)^{l+1}$ and $l=kT_t/kT$. Using this equation, measured on-current in temperature range of 100 K-340 K could be fitted using μ_o=0.5-1.5 cm^{2}V^{-1}s^{-1}, N_c=6×10^{16} cm^{-3}, ε_s=15, g_{tc}=6.6×10^{19} cm^{-3}eV^{-1}, kT_t=0.040 eV, d=80 nm, shown in Figure 4.9. Thus, the on-current of our V-TFD follows ET-SCLC.

In addition to forming a 50-nm MoO$_x$ layer with a smooth morphology, Mo also diffuses into ZTO, forming another 80-nm ZTMO layer as shown in Chapter 3. Previously, Mo doping into ZnO and SnO$_2$ layers have been reported [147]–[149]. Based on these studies, Mo was easily incorporated into ZnO and SnO$_2$ layers due to a smaller ionic radius of Mo^{6+} compared to those of Zn^{2+} and Sn^{4+}, but in all cases, an excess Mo doping (>2 at.%) led to conductivity loss of the ZnO and SnO$_2$ film. The origin of this conductivity loss can be passivation of donors, increase of acceptors, and exacerbation of charge transport in this layer due to crystallization or phase segregation. In this work, we focus on actual impact of Mo diffusion on a device operation of solution processed *a*-ZTO V-TFD, for the purpose of utilizing this *in situ* interaction in making a useful rectifier for commercial applications. Dominance of ET-SCLC mechanism as opposed to general Schottky theory indicates ZTMO layer with lower conductivity leads to bulk-dominance when V-TFD is in on-state, and that this prevents the on current to increase exponential with voltage when it is in on-state. That is to say, ZTMO has less mobile carriers than ZTO, and thus even at higher temperatures SCLC dominates. Despite such limitations on

forward current due to ZTMO layer, this layer enables high-voltage operation and long-time operation of Mo V-TFD, making it useful for energy harvesting application, as we will show in the following chapter.
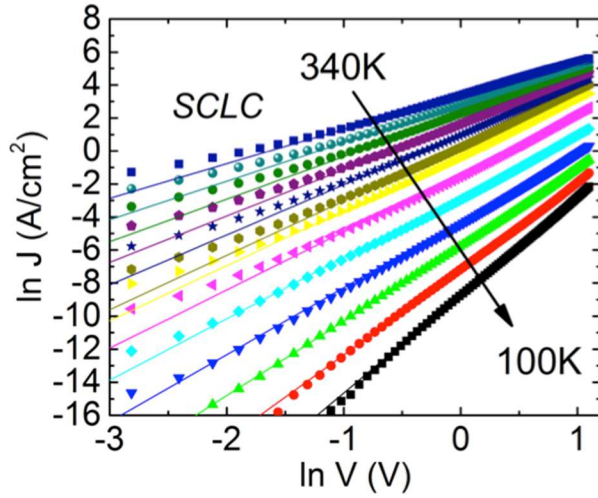
Figure 4.9 Charge transport analysis on Mo:ZTO diode based on SCLC. Forward bias *J-V* measurements at temperatures from 100 to 340 K follow straight lines when plotted as *ln J* vs. *ln V*, indicating SCLC. The shapes refer to measure data, and the solid lines refer to the calculated results based on SCLC model with exponential tail states (ET-SCLC). Reprinted with permission from [146].

4.4.2 Reverse current analysis

Reverse leakage current charge transport was also analyzed using temperature-dependent *J-V* characteristics. The measured data showed constant leakage current over bias, shown in Figure 4.10. Such constant leakage can be explained with Schottky emission without image force lowering. Based on this mechanism the leakage current follows:

$$J_r = A^* T^2 \exp\left(\frac{-\Phi_b}{kT}\right), \tag{4.28}$$

where A* is Richardson constant and Φ_b is potential barrier. The temperature variance as well as bias independence of the off-current could be explained with Equation (4.28), using the values of *A** as 0.74 Acm^{-2}K^{-2} and Φ_b as 0.34 eV. Thus, leakage current is guided by the thermionic emission over the potential barrier of 0.34 eV, formed by the work function of MoO$_x$ and

electron affinity of ZTMO layer. Therefore constant leakage current over reverse bias is obtained. We note that for Mo:ZTO diodes, the leakage current is much lower than PdO$_x$:ZTO diodes, and that thermal excitation of electrons from V$_O$ does not appear. Thus, the presence of ZTMO layer prevents this mechanism. This can be explained either by shallow donor of V$_O$ being passivated due to Mo diffusion, or the energy level of V$_O$ (Φ_d) within ZTMO layer being much deeper than ZTO (i.e., Φ_d is higher than 0.4 eV) to be thermally activated at room temperature. Both of these scenario accords with lower conductivity of ZTMO layer, as observed in the previous section by dominance of SCLC in forward bias.
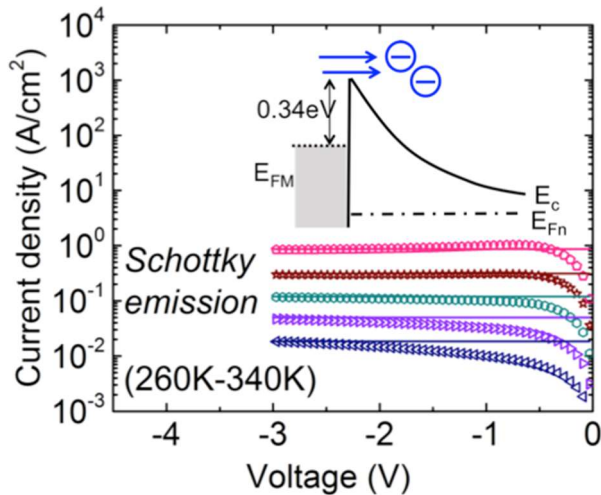
Figure 4.10 Temperature-varying reverse *J-V* measurements (symbols) of Mo:ZTO diode. The bias-independent reverse current obeys Schottky emission over a potential barrier of 0.34 eV without image force lowering (solid lines). Reprinted with permission from [146].

4.5 Conclusion

The main goal of this chapter is to investigate the V-TFDs made using bottom Schottky contacts, so that we can determine the origin of their non-ideal behaviors and obtain better diode performance in the future V-TFD design. Although the sample preparation and subsequent solution process were done in the same way, the change in the bottom electrode led to significant

difference in diode curves. In brief, Pd V-TFD has high on-current exponentially increasing with forward bias, but its leakage current also increases with reverse bias, which leads to undesirable off-state loss. On the other hand for Mo V-TFD its reverse current was lower and did not increase with reverse bias, but the on-current followed power-relationship with forward bias instead of exponential relationship. This led to lower on current of Mo V-TFD, which leads to undesirable on-state loss. In order to analyze the origin of these non-ideal switching characteristics, their charge transport mechanisms were analyzed and compared with their material compositions obtained in the previous chapter. The conclusions are made as follows.

First, we observe that due to the localized states in AOS, the on-current of its V-TFD can be limited by the bulk instead of the Schottky interface. In case of Pd V-TFD, we observe a temperature-dependent transition of the dominant charge transport mechanism in the *a*-ZTO bulk. At low temperature with less free carriers present in *a*-ZTO, its transport obeys space-charge-limited current theory with an exponential tail states below the conduction band (ET-SCLC). Thus, Pd V-TFD at low temperature does not follow Schottky diode theory. However, at around room temperature in which the device operates, the on-current does follow general Schottky diode theory, and thus it increase exponentially at low forward bias. In case of Mo V-TFD, however, both at high and low temperatures, the on-current follows ET-SCLC theory, and exhibits lower on-current. Such bulk dominance is attributed to 80 nm of ZTMO layer uniquely generated for Mo V-TFD, due to *in situ* diffusion of Mo. This layer thus has low conductivity, such that it limits the on-current and prevents the on-current to increase exponentially over bias. Although this low conductivity is undesirable in obtaining higher on-current, we will show that the ZTMO layer within Mo V-TFD diode provides a huge benefit towards other important

parameters for rectifier application. These parameters are namely breakdown voltage and bias-stress endurance, and they will be the main topic in the following chapter.

Second, even for PdO_x:ZTO diode with higher on-current, the obtained Schottky diode behavior is not ideal. For a sharp turn-on of Schottky diode, the ideality factor, n in Equation (4.1), should be as low as possible, and general Schottky theories predict n to be ideally one. Our charge transport analysis on Pd V-TFD shows that thermionic emission over spatially inhomogeneous barrier dominates in forward bias, but the obtained n is as high as 1.9. This large value of n reveals that better switching characteristics can be obtained for future AOS V-TFD. The temperature dependence of n further indicated that Schottky barrier in Pd/a-ZTO junction shows bias dependence such that the mean potential barrier increases linearly with respect to forward bias. This behavior can be indicates the existence of thin interfacial layer in Pd/a-ZTO junction, as explained in Section 4.2.2, (ii). Our XPS depth profile and cross-sectional SEM image in Figure 3.3 (b) show possible origin of interfacial layer: Pd/a-ZTO junction in PdO_x:ZTO diode has rough interface morphology due to rigorous redox reaction between PdO_x and ZTO. Such rigorous transfer of oxygen ions, inevitable for Schottky contact generation with bottom metal, can be the source of interfacial layer formation with high interface states. In addition, from XPS depth profile metallic Zn^0 and Sn^0 appear only in Pd/a-ZTO junction, which imply metal alloy formation due to solution annealing. As reported for Pd/ZnO junctions [113], metal alloy formation by annealing creates interface states and degrades its Schottky contact.

Based on these observations, we lead to the following conclusions. While our solution process offers truly in-air stable thin-film deposition method with environmental-friendliness, it requires annealing temperature of ~500°C due to the law of thermodynamics. While this may not be a problem when it is deposited on thermally stable oxides, such as glass or alumina, as shown

in Chapter 2, depositing it on metals can lead to various chemical reactions that influence overall device behavior. In order to obtain Schottky contact with bottom metals, we made use of Mo oxidation and PdO_x reduction, but these interface chemistries come along with non-ideal reactions which prevents us from getting sharp and clean Schottky interface. At Mo/a-ZTO junction, the *in situ* diffusion of Mo forms resistive ZTMO layer, which limits the on-current. At Pd/a-ZTO junction, the rough interface and alloy formation forms interfacial layer, which limits steep switching of V-TFD. Moreover, for Pd V-TFD, the deep-level donors present in a-ZTO, leads to high leakage current which increases further at high reverse bias.

In order to obtain ideal Schottky contact with AOS, a high work function metal should be in contact with AOS with less deep-donors, and form an abrupt junction with smooth interface morphology, and spatially uniform interface metallurgy. However, using an in-air deposition with high-temperature annealing, the interface chemistry that occurs on bottom metal during AOS deposition prevents from obtaining such clean interface. To build upon our achievements so far and fabricate AOS V-TFD with higher switching characteristics, we will design the new AOS V-TFD in Chapter 6. The strategy here is that we choose top-Schottky contact and bottom-ohmic contact structure for the new AOS V-TFD, in order to prevent interface reactions with bottom metal from degrading Schottky contact quality. Before the design of new V-TFD, more analysis should be made on Pd V-TFD and Mo V-TFD to fully evaluate their rectifier application. Their actual application in constant AC-DC conversion requires more than just quasi-static analysis conducted in this chapter. These additional analyses include frequency response, breakdown voltage, and stress endurance tests, which will be the main scope of the next chapter. The Mo:ZTO diode exhibit promising features toward these parameters, which allows its application for RFID harvesters.

Chapter 5 High voltage V-TFD for large-area wireless energy harvesters

5.1 Introduction

In addition to the diode *I-V* switching characteristics evaluated in Chapter 4, other important device parameters need to be examined for rectifier applications. When the diode rectifies a supplied AC voltage, most of the input voltage is applied as reverse bias across the diode, since the diode has higher impedance when it is in the off-state than in the on-state. However, when the reverse bias across the diode exceeds a certain value, the diode breaks down and fails to function as a rectifier. The voltage at which this occurs is called the breakdown voltage (BV) of the diode. BV is an important device parameter for energy harvesters, as it determines the maximum magnitude of the AC input voltage [191]. Therefore, a high BV is desired for a rectifier. To achieve a high BV, the breakdown mechanism(s) in AOS vertical Schottky diodes should first be analyzed. Equally important to BV is the diode stress endurance. In AC-DC rectification, the diode will be mainly in reverse bias. Thus, the diode should have strong endurance to reverse bias, in order to ensure a long lifetime as an AC rectifier. Both BV and stress endurance of V-TFD are very important parameters for rectifier applications, and determine the operation voltage range and the device stability.

However, most of the work reported on AOS V-TFDs for power rectifiers has focused merely on its functionality [16], [107] without evaluating device stability. Characterization of stress effects is especially critical for AOS due to its unique material properties. Unlike atoms in covalent semiconductors, ions in ionic semiconductors such as AOS can drift within the lattice

under high electric field. If the field is maintained for a long period, the accumulation of migrated ions can cause degradation and breakdown within AOS devices [192]–[194]. For this reason, these reverse bias effects are thoroughly characterized here for both PdO_X:ZTO and Mo:ZTO diodes. In this chapter, we experimentally demonstrate that the breakdown mechanism for our PdO_X:ZTO diodes is conductive filament formation guided by ion migration. Due to this mechanism, the PdO_X:ZTO diode breaks down at low voltage. Then, we show that the same mechanism in PdO_X:ZTO diode leads to a device degradation due to reverse bias stress, even prior to breakdown. However, unlike the PdO_X:ZTO diode, the Mo:ZTO diode has promise to achieve the desired characteristics, thanks to the formation of a ZTMO layer during ZTO growth. As a result, the Mo:ZTO diodes show high BV, and do not exhibit device degradation during constant reverse bias stress.

After characterizing the BV and bias stress effect, the frequency response of the diodes will be tested. This requires use of a half-wave rectifier configuration, where a single diode rectifies an AC input and supplies a DC output to the load. In this circuit, we sweep the input frequency using a signal generator in order to confirm the functionality of our diodes as a function of frequency. By performing this experiment with different AC voltage levels, we experimentally verify the importance of stress endurance and BV for a given diodes in practical rectifier applications. Thanks to the high stress endurance and high BV of the Mo:ZTO diode, it operates stably as a rectifier, while the PdO_X:ZTO diode has severe device degradation and breaks down at low AC voltages.

After observing the promising features of the Mo:ZTO V-TFD, we compare this V-TFD with its TFT counterpart for power rectifying applications. As explained in Chapter 1, the main motivation for fabricating V-TFDs comes from the understanding that V-TFDs can enable higher

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operation frequency and higher efficiency that TFTs due to the V-TFD's vertical current conduction across a thin film. The superior rectifier performance of V-TFDs [16], [107] compared to TFTs [109], [108] was previously reported for vacuum-deposited AOS, and was enabled by the larger on-current and shorter device length of the V-TFD. Here, we confirm these performance advantages for our Mo:ZTO diode.

Despite their good performance, the AOS V-TFDs reported to date face significant fabrication challenges in integrating them directly with TFTs. TFTs are inevitable components for thin film logic circuits [17], [195], but integration of AOS TFDs with TFTs normally requires deposition and patterning of a new, high work function metal, often followed by sophisticated oxidation steps in order to reduce oxygen vacancy-related defects near the Schottky interface [101], [118]. Such additional process steps increase fabrication cost and complexity, leading to a tradeoff when we choose between these two devices as a rectifier. However, this is not the case for our Mo:ZTO V-TFD. The Schottky contact in our Mo:ZTO diode is formed via *in situ* chemical reactions, without deposition, patterning, or oxidation of a new metal. Moreover, because Mo makes a good electrode for TFTs [59], our Mo:ZTO diodes can be fabricated alongside our bottom-gate TFTs without adding any fabrication steps. Such co-fabrication of TFTs and V-TFDs has not yet been reported, and this opens up new opportunities for future solution-processed thin-film ICs. Therefore, we fabricate Mo:ZTO diodes and bottom-gate TFTs on the same sample to demonstrate a facile solution process for fabricating novel devices. After co-fabrication, we compare the rectifying performance of diodes and TFTs of the same size and compare their operation frequencies. After confirming the superior rectifier performance of the Mo:ZTO V-TFDs, these devices are demonstrated as wireless energy harvesters using a commercial RFID reader and antenna.

5.2 PdO$_x$:ZTO rectifier for low voltage handling

5.2.1 Breakdown of PdO$_x$:ZTO diodes

Prior to breakdown, the PdO$_x$:ZTO devices function as normal diodes, with on-current scaling predictably with the top ohmic electrode area. This is plotted on a linear *I-V* scale in Figure 5.1 (a)). On working diodes, breakdown (BD) measurements were performed by applying DC voltage sweeps. As shown in Figure 5.1 (b), we observe breakdown at a very low voltage of approximately -3 V. The BV of AOS V-TFDs have been measured and reported by others, but the exact mechanism guiding this breakdown has not been studied. Here, we investigate possible breakdown mechanisms of the PdO$_x$:ZTO diode. Two common breakdown mechanisms in diodes are Zener breakdown (due to tunneling) and avalanche breakdown (due to impact ionization) [196]. However in our diodes, the amount of direct tunneling of electrons through a 100-nm thick film with moderate doping (N_{depl} ~10^{17} cm^{-3}) is expected to be low and thus Zener breakdown is seen as unlikely. Thus, impact ionization is analyzed here. In other amorphous covalent semiconductors, such as *a*-Se and *a*-Si:H, impact ionization does occur and is used for x-ray imaging purposes [197]. In these materials, the impact ionization rate is calculated using the revised *lucky drift model* suggested by *Kasap et al.*, which statistically calculates the energy that an electron gains (E_a) under the applied electric field (F) as it goes through a certain number of elastic and inelastic collisions (k_l, k_u, and m). An in-depth explanation of this model can be found in ref. [23].

To determine whether impact ionization can explain the measured BV of our diode, we applied this model to simulate the impact ionization rate of ZTO with respect to electric field.

Impact ionization in amorphous ZTO is illustrated in Figure 5.1 (c). This model requires the choice of several parameters including the ionization threshold energy, E_i, the optical phonon energy, E_r, and the mean free path of elastic and inelastic scattering, λ_{el} and λ_{ie}. Here we use similar parameters to those obtained for a-Se and a-Si:H [23], [198]. Based on our measurement of the optical bandgap of ZTO (~3.3 eV) and our understanding that ZTO has midgap states as well as tail states near the valence band, we choose E_i to range from $E_g/2$ to E_g (1.7-3.3 eV). For E_r, we use values of 30 to 100 meV, and we used the same values of λ_{el} and λ_{ie} as *Kasap et al.*, 6 Å and 72 Å, respectively [198]. The simulated impact ionization coefficient (IIC) in ZTO is shown in Figure 5.1 (d). Next, using this IIC, we use 2D TCAD simulations to predict the onset of avalanche breakdown in our PdO_x:ZTO diode. Our TCAD simulation shows that avalanche breakdown should not occur up to -22 V (Figure 5.1 (e), black symbols). This predicted value of BV is much larger than our observed value of -3 V. Therefore neither Zener BD nor avalanche BD can explain the BV observed for our PdO_x:ZTO diodes.
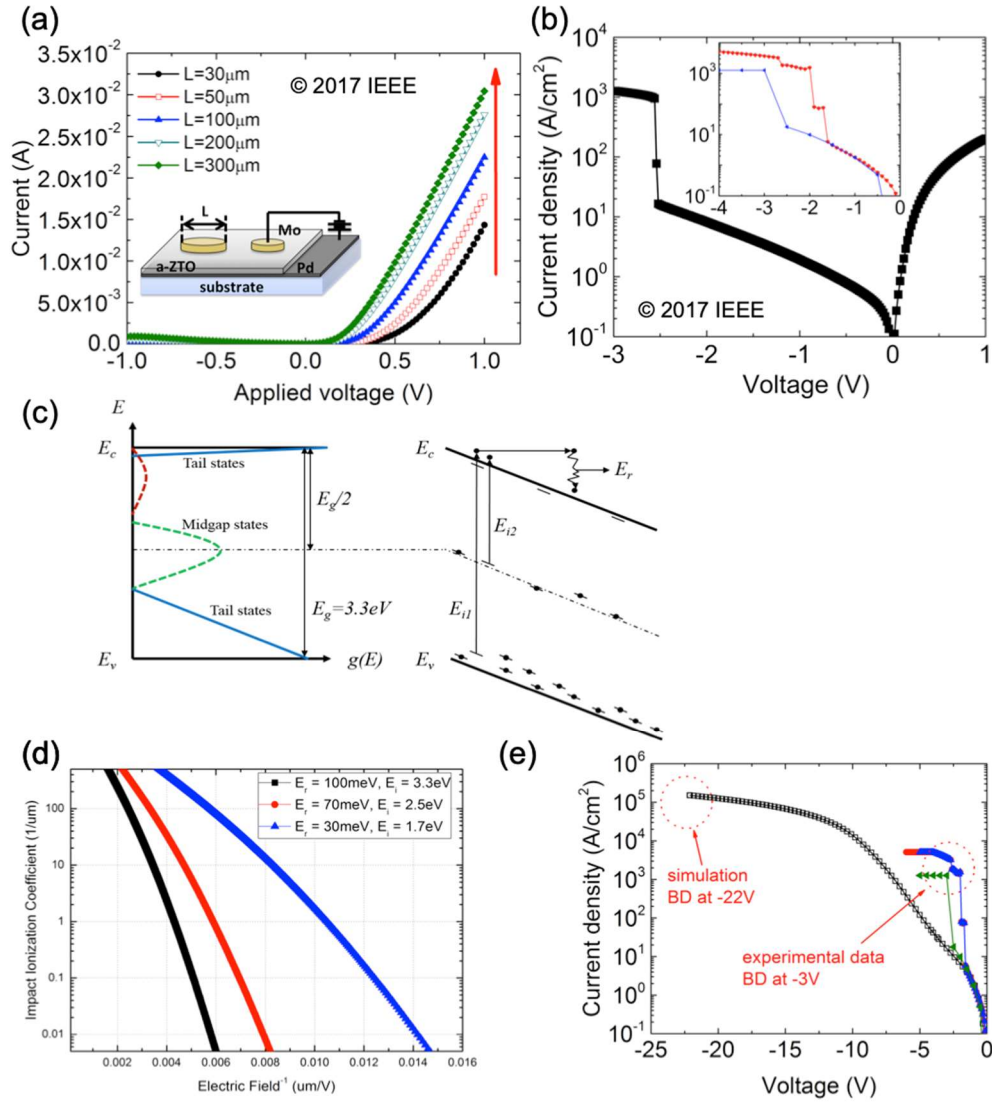
Figure 5.1 Evaluation of possible breakdown mechanisms of PdO$_x$:ZTO diodes. (a) Area-dependent *J-V* measurements of PdO$_x$:ZTO Schottky diodes. The device structure is shown in the inset where *L* refers to the diameter of the top electrode. (b) BD measurement with BV observed at -2.5 V. The inset of (b) shows similar BV of other devices. (c) Schematic of DOS in *a*-ZTO (left) suggested by [4] and energy band diagram of impact ionization of electron within this DOS (right) (d) Impact ionization coefficient with respect to 1/field. Reasonable values of E_r and E_i were used: E_r = 30 – 100 meV, and E_i = 1.7 - 3.3 eV (e) 2D TCAD simulation of BD and measurement of BD on several PdO$_x$:ZTO Schottky diodes. For simulation, we used the worst-case impact ionization rate calculated from (d).

After BD occurs, as shown in Figure 5.1 (b) the PdO$_x$:ZTO diodes no longer show rectifying behavior (Figure 5.2 (a)). This again leads us to believe that neither Zener BD nor avalanche BD are likely to be the cause of hard BD, as neither of those mechanisms should

induce permanent changes in the diode. Some amorphous oxides, including titanium oxide [199] and tantalum oxide [200] have shown that exposure to moderate electric fields can cause the oxygen vacancies (V_O) present in the oxides to drift within the film [201]. The field-driven movement of V_O creates a conductive filament (CF) that bridges the two electrodes. This is known as "CF forming." When such oxides are used in two-terminal devices with high work function metals, the rectifying behavior at the Schottky interface can be affected by the movement of V_O, and forming can permanently increase the device current [202]. Such field-induced structural change has been extensively developed and exploited for resistive memory (RRAM) applications [203], [204], but has not yet been reported as a failure mechanism in AOS Schottky diodes.

Thus, we performed additional electrical measurements to determine whether V_O migration acts as a breakdown mechanism in our PdO_x:ZTO devices. After inducing BD, the applied voltage was swept back and forth to various voltages. The results are shown in Figure 5.2 (b). The set-and-reset behavior that is characteristic of RRAM is clearly observed. This observation required the application of a sufficiently large bias (± 3 V sweep) to the post-breakdown diode in order to induce the set-and-reset process. Thus, after BD, the devices no longer act as rectifiers but instead exhibit bipolar resistive memory (RRAM) behavior with repeatable switching between low resistance state (LRS) and high resistance state (HRS) (Figure 5.2 (c)). This RRAM behavior is typically attributed to one of the two mechanisms: either conductive filament (CF) formation or interface modulation [202].

To confirm whether the observed behavior is due to CF formation or due to interface modulation, we examined the area dependence of diode current before and after forming. Before BD, the rectifying diode current is directly dependent on electrode area, indicating that current

flows uniformly through the semiconductor (Figure 5.1 (a)). In contrast, after BD, the diode current is independent of electrode area (Figure 5.2 (c)), indicating that current is flowing through spatially confined conductive filament(s). Based on this evidence, we conclude that the low-voltage BD observed in PdO_x:ZTO diodes is due to CF formation (Figure 5.2 (g)). As Pd and Mo are inert electrodes [205], the CF in ZTO most likely consists of oxygen vacancy defects (V_O). We note that the XPS depth profile of a PdO_x:ZTO sample, shown in Chapter 3, revealed atomic percent-range concentration of V_O (i.e. oxygen near oxygen vacancies) evenly distributed in solution-processed ZTO. These oxygen vacancies act as the source of the conductive filament in a-ZTO film, as illustrated in Figure 5.2 (e). They accumulate at Schottky interface as shown in Figure 5.2 (f) and then form a conductive filament when BD occurs, as shown in Figure 5.2 (g). We recall that in Chapter 4, the leakage current of PdO_x:ZTO diode was found out to be due to electrons that are thermally excited from deep donors. The deep donor energy level of 0.4 eV below the conduction band corresponds to the predicted energy level for V_O in ZTO. This was true when PdO_x:ZTO diode is operating at low bias regime (i.e., in the state described by Figure 5.2 (e)). However, if V_O in ZTO accumulates near Schottky interface prior to CF formation as illustrated in Figure 5.2 (f), it is expected that these V_O can degrade the Schottky contact via tunneling, increasing leakage current. In order to confirm this hypothesis, a bias stress test was performed on diodes that had not yet been broken down (i.e. "formed", in RRAM terminology). As shown in Figure 5.2 (d), diodes that were stressed with low, constant DC bias showed an increase in their leakage current, eventually leading to breakdown.
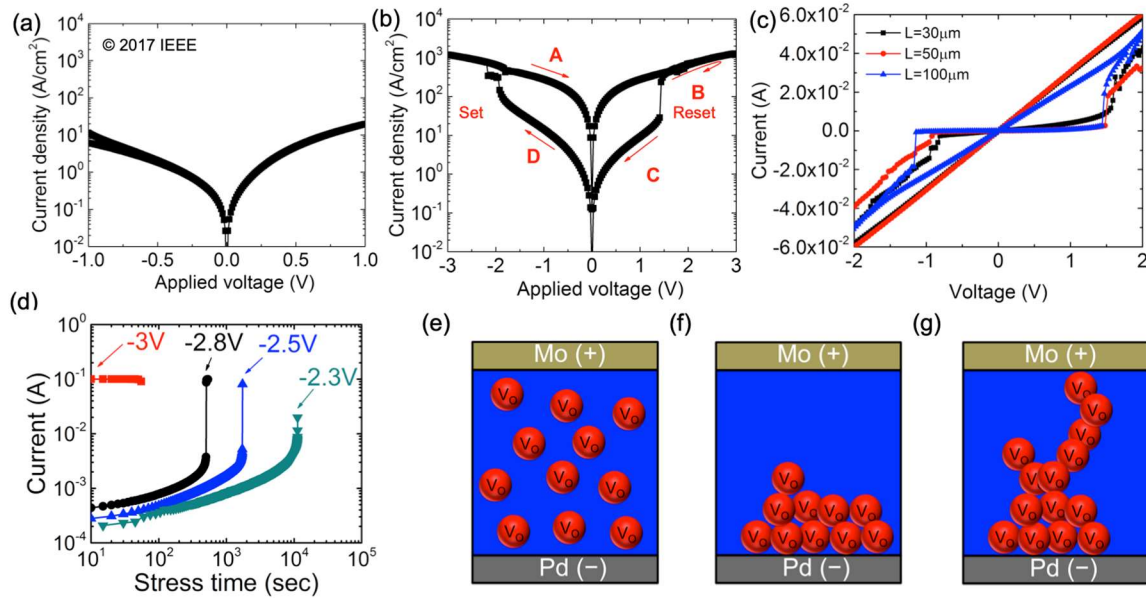
Figure 5.2 Conductive filament formation as the breakdown mechanism in PdO_x:ZTO diodes. (a) A ±1 V sweep after hard BD (shown in Figure 5.1 (b)). No rectifying behavior is observed. In (b), a ±3 V double sweep after hard BD shows the set/reset behavior characteristic of resistive memory devices. The sweep was done $A \rightarrow B \rightarrow C \rightarrow D$. In (c) we show the electrode area dependence of resistive memory devices after BD. The resistance is not dependent on electrode area, indicating that BD is due to CF formation. Image (e)-(g) shows a cartoon of CF formation caused by drift of V_O. (e) Illustrates ZTO prior to reverse bias stress, (f) Illustrates the situation at moderate reverse bias, where accumulation of V_O near Schottky interface can degrade the rectifying contact and increase leakage current as shown in (d). (g) Illustrates breakdown, at which a conductive filament is formed that shorts the bottom electrode and top electrode.

Based on these observation, the following conclusions can be made regarding PdO_x:ZTO diodes. V_O present in *a*-ZTO is detrimental to the diode's reverse characteristics. Its migration can lead to conductive filament formation and cause premature breakdown, with a BV as low as -3 V. This is much lower than what is expected by impact ionization or tunneling. Such premature breakdown needs to be prevented in order to increase the voltage handling capability of AOS V-TFDs. Even when the diode is operating at voltages lower than the BV (i.e. lower than the forming voltage), V_O can migrate and accumulate due to reverse bias, leading to degradation at the rectifying contact and an increase of leakage current, degrading the rectifier performance. As shown in Figure 5.2 (d), this phenomenon eventually breaks down the device over time. As a

rectifying diodes operates mostly in reverse bias, this phenomenon will lead to severe limits in rectifier operation, as will be shown in Section 5.2.3.

5.2.2 Cutoff frequency of PdO$_x$:ZTO diodes

So far, only the DC characteristics of the vertical Schottky diodes have been analyzed, from which we were able to understand charge transport and breakdown mechanisms. However, many applications of diodes require they be driven by AC signals, and therefore understanding the diode's AC characteristics is equally important. Furthermore, because high-speed operation is one of the advantages of Schottky diodes, estimating the cutoff frequency of our Schottky diodes has significant value. Here, we performed an impedance measurement of our PdO$_x$:ZTO diodes. The diode's zero DC bias impedance was measured with a 50 mV AC signal with a frequency range from 20 Hz to 1 MHz, using an HP 4284A Precision LCR meter. The measured data were fit to a standard diode small-signal equivalent circuit [106], [119] consisting of a parallel resistor and capacitor, R_b and C_b, in series with a resistance, r_s, as shown in the Figure 5.3 inset. One of the main advantages of a Schottky diode over a PN diode is its high cut-off frequency. As unipolar devices, Schottky diode switching is limited by the fast response time of the majority carriers. By extending this equivalent circuit model to higher frequencies, as was done in [106], [119], [130], the cut-off frequency of our diode [206] can be estimated to be

$$f_{cutoff} = 1/(2\pi r_s C_b). \qquad\qquad (5.1)$$

The extracted cut-off frequency value for our devices was 235 MHz. This value is the same order of magnitude as that found for a-IGZO Schottky diodes, 900 MHz [119]. This high $f_{cut-off}$ makes the PdO$_x$:ZTO diode promising for high frequency applications. However the bias stress and low BV can be limiting factors. Improving these features is the subject of the following section. We

also note here that, despite its common use [108], [112], Equation (5.1) can only evaluate operating frequency in a limited fashion, because it is based on small-signal analysis. In reality, the sinusoidal input voltage applied to a wireless harvester can range up to 10 V peak-to-peak. In such scenario, the values of r_s and C_b change dramatically with voltage, which makes modeling the rectifiers using constant values of r_s and C_b a very broad approximation. Later, in Section 5.3.3., when we analyze and compare the maximum operation frequency of our Mo:ZTO diode and TFT, we will apply another calculation method based on large-signal analysis.
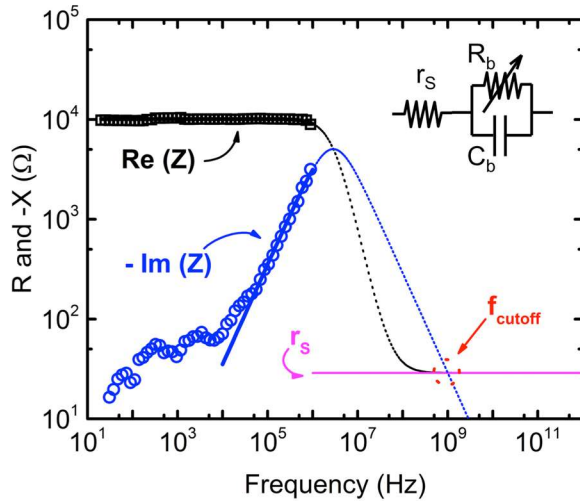
Figure 5.3 Impedance measurement of a 50 µm diameter PdO$_x$:ZTO diode (real and imaginary parts shown as squares and circles, respectively). During measurement, the DC voltage was 0 V, the AC voltage was 50 mV, and the frequency was swept from 20 Hz to 1 MHz. The small-signal diode model (lines) is based on the circuit diagram shown in the inset. Here, values of r_s=28.8 Ω, R_b=10100 Ω, and C_b=5.5 pF were fit to the measured data. Reprinted with permission from ref. [165]

5.2.3 The limits of PdO$_x$:ZTO diodes for rectifier applications

The electrical measurements in the previous section suggested that PdO$_x$:ZTO diodes have a high $f_{cut-off}$ up to 235 MHz, but its vulnerability to bias stress and low BV may limit its practical implementation in AC rectifiers. This projection, made from DC bias stress test results, was based on the understanding that when a diode rectifies AC signal, it will predominantly be exposed to reverse bias. Now, we seek to experimentally characterize the diode's response to a

sinusoidal input when being used as AC rectifier, to see whether the diode's operation in a rectifier is consistent with the aforementioned DC bias stress results.

In this section, we measured our diode in an AC rectifier circuits, and tested its frequency response up to 15 MHz. We attached a PdO_x:ZTO diode to a signal generator and connected discrete resistors and capacitor to form a half-wave rectifier, as shown in Figure 5.4 (b). For sinusoidal input voltages (V_{in}) of 2.0 V_{pp} and 3.0 V_{pp}, DC output voltages (V_{out}) of 0.7 V and 1.1 V are measured, respectively (Figure 5.4 (c)). The rectifiers work up to 15 MHz, which is the maximum frequency of our signal generator. No roll-off of V_{out} due to diode cutoff is observed (Figure 5.4 (d)).

During AC-DC rectification, the behavior of the PdO_x:ZTO diode is expected to be limited by the following mechanisms: (i) its low BV will limit its voltage handling capability, such that it can only rectify small AC signals at its input, and (ii) its leakage current will increase due to bias stress, leading to degradation of the rectifier's efficiency over long operation times. These expectations, based on previous quasi-static measurements, were confirmed using a half-wave rectifier. Namely, when V_{in} is only 5.0 V_{pp}, the diode breaks down and no longer rectifies the AC signal, as shown in Figure 5.4 (e) and (f). Even when the applied V_{in} is slightly lower than the diode's BD voltage (e.g., 4.3 V_{pp}), while this extends the operation time of the rectifier, the V_{out} indeed decreases from 1.5 V to 1.35 V in just 120 mins (Figure 5.4 (h)). This decrease is attributed to the stress-induced increase in leakage current, which was confirmed by Cadence simulation (not shown). We observed that a constant reverse bias stress leads to an increase in leakage current, with only marginal changes in forward current, as shown in Figure 5.4 (i).
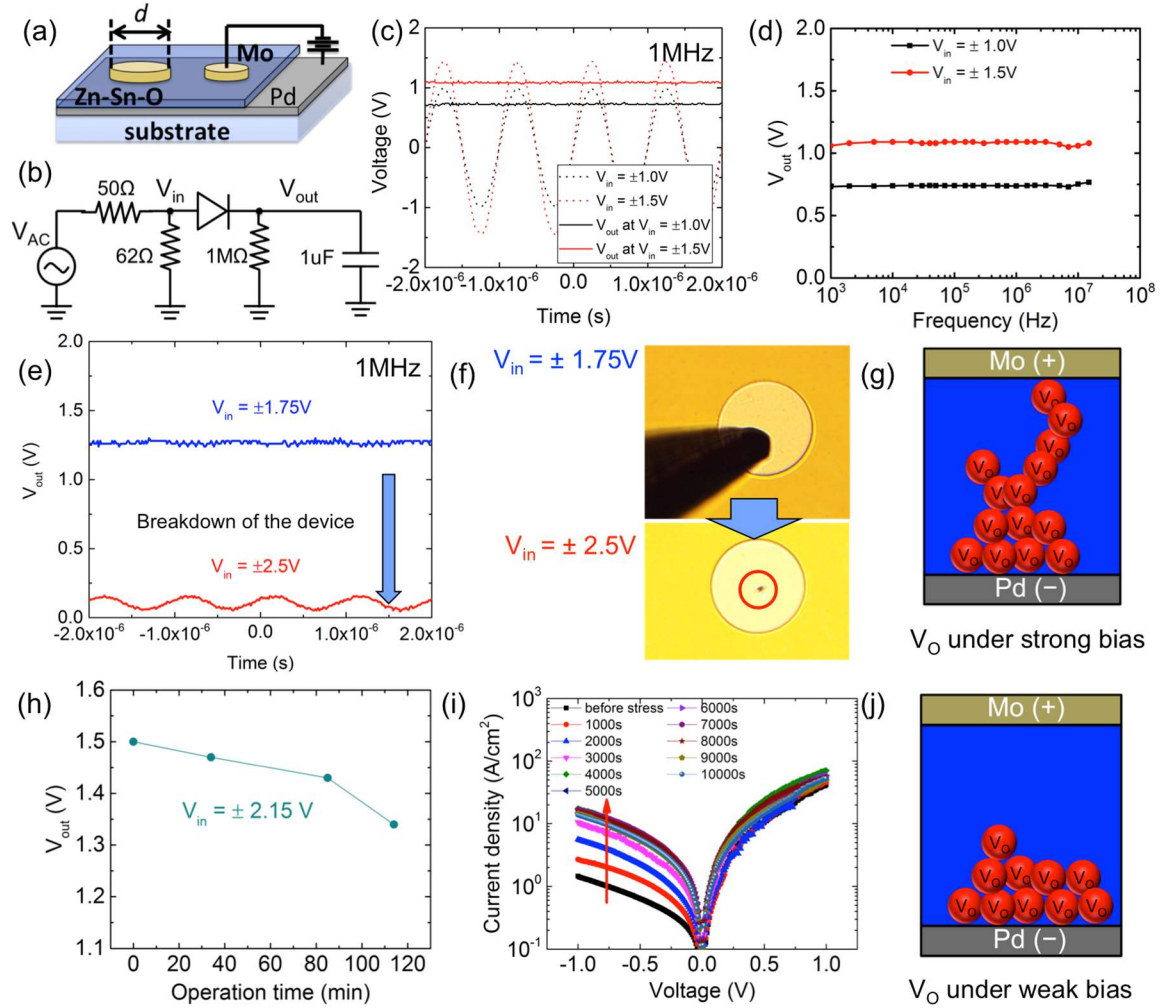
Figure 5.4 Severe drawbacks of the PdO$_x$:ZTO diode in AC power rectifiers. (a) Schematic of PdO$_x$:ZTO diode structure. The tested devices shown in this figure have d = 100 μm, the same size as Mo V-TFD. (b) Half-wave rectifier measurement setup. (c) 1 MHz AC input voltage (V_{in}) of 2.0 V$_{pp}$ and 3.0 V$_{pp}$ and corresponding DC output voltage (V_{out}). (d) Frequency response of V_{out} from 1 kHz to 15 MHz, showing no cut-off. (e) V_{out} measured for higher V_{in} of 3.5 V$_{pp}$ and 5.0 V$_{pp}$ and (f) microscope images of the diode showing pinhole defect when V_{in} = 5.0 V$_{pp}$, caused by breakdown. The breakdown mechanism is conductive filament formation [192], shown in (g). (h) The decrease of V_{out} over time. This is due to leakage current increase due to bias stress, shown in (i). In (i), the diode was repetitively tested after applying -2 V across the diode for 1000 sec. The increase in leakage current is attributed to tunneling by oxygen vacancy (V$_O$) accumulation near the Schottky interface, as illustrated in (j). Reprinted with permission from ref. [146].

5.3 Mo:ZTO rectifier for high voltage handling

5.3.1 Reverse characteristics of Mo:ZTO diode

For the PdO$_x$:ZTO diode, the BV (~3 V) was too low for it to be used in commercial energy harvesters, and constant reverse bias stress led to an increase of leakage current and

eventually to breakdown. These properties are detrimental for practical rectifier applications, in which the diode is mostly in reverse bias: The rectifier degrades within a short period of time (tens of minutes) and breaks down at low input AC voltage (5 V_{pp}). Thus, these challenges must be overcome to make useful rectifier.

Therefore, in this section we describe V-TFDs made via a Mo/ZTO junction that shows promising features to address these challenges. We first measured the BV of our Mo:ZTO diode. As shown in Figure 5.5 (a), the Mo V-TFD has high BV of over 10 V, and a constant leakage current prior to breakdown. Such bias-independent leakage current was previously attributed to Schottky emission without image force lowering, which obeys $J_r = A^* T^2 \exp\left(\frac{-\Phi_b}{kT}\right)$, with A^* as 0.74 Acm^{-2}K^{-2} and Φ_b of 0.34 eV, in Section 4.4.2. The BV of over 10 V is a significant improvement for the Mo:ZTO diodes compared to PdO$_x$:ZTO ones. 10 V is a suitable AC voltage magnitude for many practical applications [207], indicating that the Mo V-TFD can be widely used in power rectifiers.

Equally important to achieving high BV is to maintain stable operation of the diode under reverse bias lower than BV. In the case of PdO$_x$:ZTO diodes, its poor stress endurance led to device degradation during AC-to-DC conversion. Thus, we test the reverse bias stress effects of Mo:ZTO diodes, and compare them with the PdO$_x$:ZTO diodes. First, the effect of bias stress on leakage current was tested using the same condition used for PdO$_x$:ZTO diode in Figure 5.4 (i). A reverse bias of -2 V was applied and the *I-V* properties of the diode was tested every 1000 sec. As shown in Figure 5.5 (c), the *I-V* curves of Mo:ZTO diode do not change significantly due to the stress. Second, a constant bias stress was applied to Mo:ZTO diodes at a higher voltage, greater than that used for PdO$_x$:ZTO diode testing. As shown in Figure 5.5 (d), the Mo:ZTO diode shows much better endurance to the reverse bias stress than the PdO$_x$:ZTO diode. While

applying reverse bias as small as -2.3 V to a PdO$_x$:ZTO diode can lead to breakdown after 11,280 sec, while in contrast the Mo:ZTO diode does not show breakdown even when stressed at -8 V for 60,000 sec. Equally important is that the leakage current tends to stay nearly constant with stress time, indicating the marginal physical effects of bias stress. Therefore, the Mo:ZTO diode has better reverse characteristics than the Pd diode, enabling a rectifier that is useful for commercial energy harvesters.
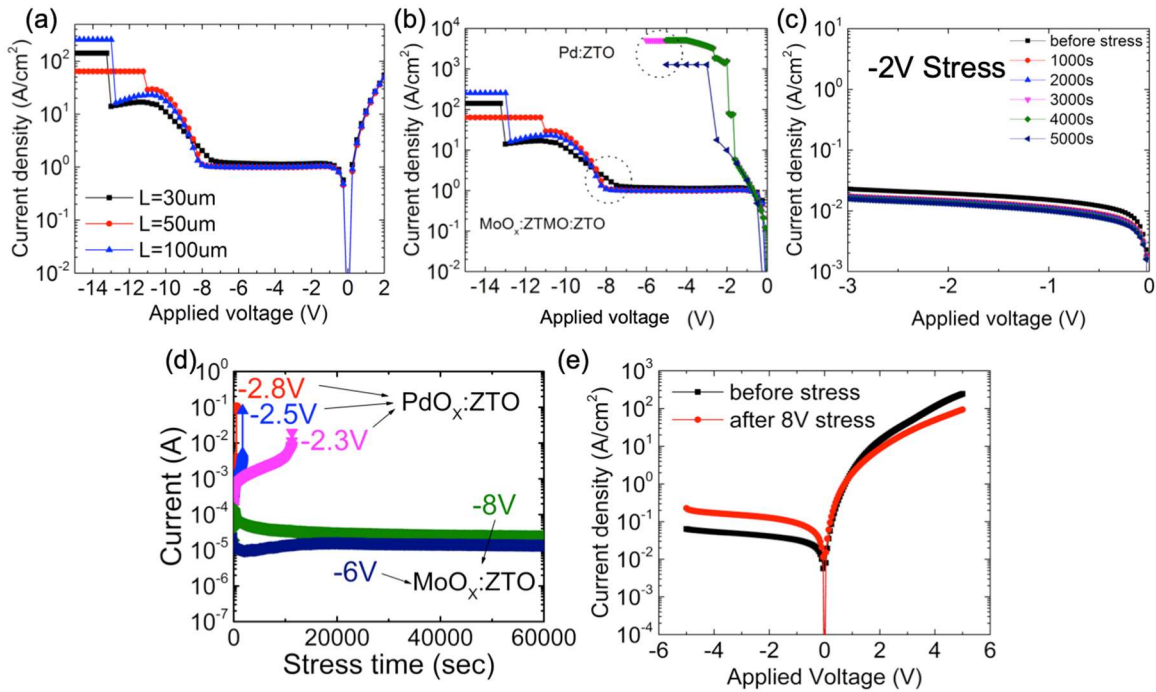
Figure 5.5 Superior voltage handling capability of Mo:ZTO diode over PdO$_x$:ZTO diode. (a) Breakdown voltage (BV) measured using voltage sweeps across Mo:ZTO V-TFDs with various electrode sizes. A BV over 10 V is achieved. (b) The measured BV of Mo V-TFDs vs. Pd V-TFDs compared under the same condition. The Mo:ZTO diode can withstand a much larger voltage prior to BD. (c) Effect of reverse bias on reverse current of the Mo:ZTO diode. Here, the diode was repetitively tested after applying -2 V across the diode for 1,000 sec. The change in leakage current is marginal, especially compared to PdO$_x$:ZTO diode shown in Figure 5.4 (i). (d) Reverse current over bias stress time measured for 100-μm diameter PdO$_x$:ZTO diodes and MoO$_x$:ZTO diodes. (e) *J-V* characteristics of a MoO$_x$:ZTO diode before and after -8 V stress for 60,000 sec. A slight change in the *I-V* curve is distinguishable. This compares favorably to the irreversible change in *I-V* behavior observed for PdO$_x$:ZTO diodes. Reprinted with permission from ref. [146].

Here we explain the origin of the Mo:ZTO diode's good voltage handling capability. The limited voltage handling capability of PdO$_x$:ZTO diodes was attributed to oxygen vacancy (V$_O$)

migration within ZTO, causing trap-assisted tunneling and conductive filament (CF) formation. For the tunneling and CF formation to occur via V_O migration, the V_O defects should first accumulate adjacent to the Schottky interface and then form a CF in order to short the bottom and top electrodes (Figure 5.4 (g)). While the same a-ZTO is deposited for the Mo:ZTO and Pd diodes, the devices have different structures: the Mo:ZTO V-TFD has a ZTMO layer formed by diffusion between the MoO_x rectifying contact and the a-ZTO layer. Therefore, the reverse bias behavior of Mo V-TFD is determined by the dynamics of V_O migration within the ZTMO layer. The existence of this ZTMO layer enables stronger stress endurance and higher BV. In order to explain this more fully, the ZTMO layer should be examined and compared with a-ZTO.

In order to further analyze the differences between the ZTMO and a-ZTO layers and explain the origin of their different V_O dynamics, transmission electron microscopy (TEM) was carried out on device cross sections. For measurements, an in-situ FIB lift-out cross-sectional specimen was studied using a JEOL JEM-3100R05 analytical electron microscope (AEM) attached with double Cs-correctors operated at 300 keV. First, a scanning transmission electron microscopy (STEM) image was taken on the entire Mo/MoO_x/ZTMO/a-ZTO stack, shown in Figure 5.6 (a). Morphological differences between layers are shown. The MoO_x layer exhibits a smooth morphology compared to the ZTMO layer, agreeing with cross-sectional SEM image in Figure 3.6 (b). Next, energy-dispersive X-ray spectroscopy (EDS) studies were carried out with the microscope in STEM mode. High-angle annular dark-field (HAADF) images were taken to define the mapping regions. Figure 5.6 (b) shows two distinctive regions between Mo and a-ZTO: a ~50 nm thick MoO_x layer and a ~80 nm thick Sn-rich, Mo-doped ZTMO layer. This agrees with our previous analysis using XPS depth profile, in Figure 3.6. In order to further characterize the ZTMO and a-ZTO layers, high resolution transmission electron microscopy

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(HRTEM) imaging was performed with the microscope operated in conventional TEM mode. The HRTEM images and fast Fourier transform (FFT) diffraction patterns obtained for the *a*-ZTO and ZTMO layers are shown in Figure 5.6 (c) and (d), respectively. While the *a*-ZTO layer possesses an amorphous structure, as expected, the ZTMO layer is polycrystalline.

Thus, our experimental data so far suggest the following physical origins for the different V_O behavior observed within ZTMO. First, compared to *a*-ZTO, the ZTMO layer has a Sn-rich composition with Mo incorporated by diffusion, as shown in Figure 3.6 (a) and 5.6 (b). The different metal cation stoichiometry of ZTMO compared to *a*-ZTO may lead to high activation energies for V_O formation and migration, caused by changes in oxygen ion hopping distance or in potential barriers within the ionically-bonded structure. This approach – modifying activation energies for V_O formation and its migration with the help of impurity doping – is often used to tune forming behavior in memristive devices [208]. Second, in addition to the effect of chemical composition, the different crystallinity of the film may affect V_O migration and CF forming behavior. It has been previously reported that annealing *a*-IGZO with diffused copper can generate crystalline clusters which results in prevention of CF forming behavior [193]. Thus, crystalline structures formed in ZTMO layer can further prevent V_O migration. Third, as indicated by analysis of the forward *J-V* curves in Section 4.4.1, the ZTMO layer functions as a low-doped region, which may reduce the maximum electric field at the Schottky interface under reverse bias. All of these mechanisms prevent or reduce field-induced accumulation of V_O defects at the Schottky interface, as illustrated in Figure 5.5 (e). As a result, in Mo V-TFDs we obtain a reduced leakage current, compared to the Pd V-TFDs, and avoid premature breakdown by CF formation. To further optimize Mo V-TFD diode performance, in the future work could be done to quantify the diffusion kinetics occurring *in situ* during solution-processed film deposition

and annealing, in order to more precisely control the thickness and stoichiometry of the MoO_x and ZTMO layers.
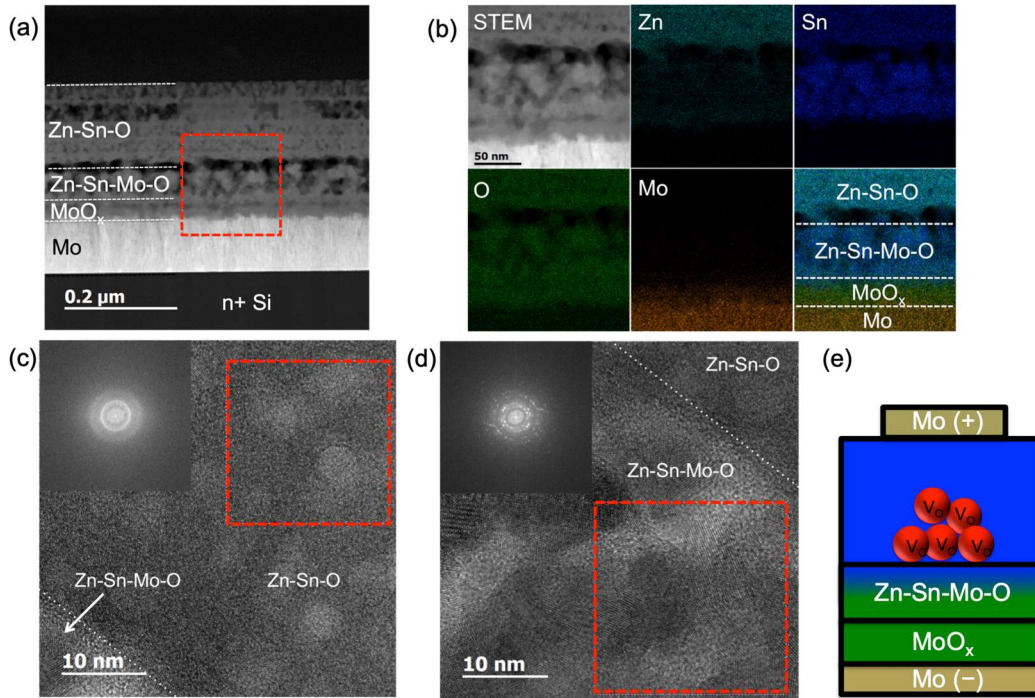
Figure 5.6 Further material characterization of the Mo:ZTO interface. (a) Cross-sectional dark-field STEM image of Mo/*a*-ZTO junction. The region where STEM image and EDS mapping were carried out is marked with a red dashed line in (b). (b) Cross-sectional STEM dark-field image and EDS elemental mapping of Zn (cyan), Sn (blue), O (green), and Mo (orange) obtained near the Mo/*a*-ZTO junction. Two additional interfacial layers (i.e., MoO_x and ZTMO) appear between metallic Mo and ZTO, which accords with the XPS depth profile shown in Figure 3.6(a). (c) and (d) HRTEM images near the *a*-ZTO/ZTMO interface. The interface is marked with a white dotted line. The regions for FFT analysis are marked with red dashed boxes and the corresponding FFT patterns are shown in the insets. ZTO shows an amorphous morphology in (c) while ZTMO is polycrystalline in (d). (e) Illustration showing that due to the presence of ZTMO layer, oxygen vacancies (V_O, red circles) cannot accumulate near Schottky interface (i.e., at the MoO_x/ZTMO interface). Reprinted with permission from ref. [146].

5.3.2 Frequency response of the Mo:ZTO diode

In the previous section, a strong endurance to the reverse-bias stress in addition to high BV were observed for Mo:ZTO diodes. These results indicate that Mo:ZTO diodes will be able to rectify larger AC input signals, and operate more stably than PdO_x:ZTO diodes. To validate this hypothesis, we conducted half-wave rectifier measurements on Mo:ZTO diodes.

The measurement configuration is identical to that used with PdO_x:ZTO diodes, shown in Figure 5.4 (b). The AC input voltage (V_{AC}) was generated by a HP 33120A function generator, operated in 50 Ω mode and used with a 62 Ω input resistor. For voltage measurements, a Tektronix MSO2024b oscilloscope was used. In order to obtain a stable DC voltage at the load, the discharge time of the load capacitance, C_L, through the load resistor, R_L, should be very small during one AC cycle (period $T = 1/f$), leading to $R_L C_L >> 1/f$. In addition, the ratio between C_L and the diode capacitance, C_D, defines the amplitude of the small-signal AC voltage, so C_L needs to be very large compared to C_D; $C_L >> C_D$ [168], [195]. Therefore, a 1 µF load capacitor and 1 MΩ load resistor were used, which gives $R_L C_L$=1 sec and $C_L >> C_D$, where C_D for the diode used here (d=100 µm) is around 25 pF when measured at 1 MHz at zero bias.

Using this circuit configuration, our Mo:ZTO diode rectified the supplied AC voltage (Figure. 5.7 (a)) into a DC voltage (Figure 5.7 (b)). V_{in} plotted in Figure 5.7 (a) shows the actual voltage measured across the input resistor, not the voltage supplied by the function generator (see the circuit diagram in Figure 5.4 (b)). As shown in Figure 5.7 (b), an AC voltage as high as 10 V_{pp} can be rectified to generate a DC output as high as 3 V. This high voltage handling capability was enabled by the diode's high BV of >10 V. In Figure 5.7 (c), we can observe that the diode did not show any cutoff behavior up to 15 MHz, indicating its usefulness for HF (13.56 MHz) RFID tag. In addition, a drop of V_{out} over time was not observed for the Mo:ZTO diode thanks to its strong endurance to bias stress. Thus, the high BV and high stress endurance of Mo:ZTO diode enables the long-term stability of AC rectifiers using this diode.
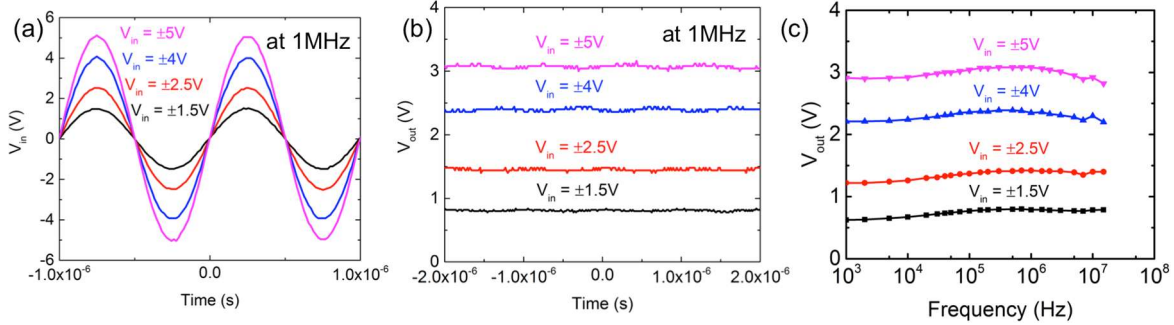
Figure 5.7 AC-DC rectification of Mo:ZTO rectifier. The measurement of single-stage rectifier using the test circuit setup shown in Figure 5.4 (b). The devices tested here have diameters of 100 μm. (a) 1 MHz sinusoidal input voltages (V_{in}) with various magnitudes and (b) the corresponding DC output voltages (V_{out}). (d) The frequency response of V_{out} from 1 kHz to 15 MHz.

5.3.3 Comparison of Mo:ZTO diodes with lateral TFTs

We have now demonstrate a V-TFD that can withstand voltages up to 10 V_{pp} and can operate stably up to 15 MHz. This diode was fabricated by depositing solution-processed a-ZTO film on top of Mo layer. The main purpose of establishing the V-TFD technology was to fabricate rectifiers that can operate at higher frequency and efficiency compared to those made using diode-connected TFTs [20]. Due to the advantageous material properties of AOS, both lateral thin-film transistors (TFTs) [108] and vertical thin-film diodes (V-TFDs) [16] have been demonstrated as a power rectifier. Although the exact cutoff frequency and efficiency of a rectifier can change depending on its operating conditions, V-TFDs are expected to far exceed TFTs performance as a rectifier for the same condition (e.g., device size, input voltage, attached load, etc.) [20], [108], [195]. Superior rectifier performance of V-TFDs [16], [107] compared to TFTs [109], [108] were previously reported for vacuum-deposited AOS, enabled by the larger on-current and shorter device length of V-TFDs.

In order to demonstrate the strength of our Mo:ZTO V-TFDs over TFTs when used as a rectifier, these two devices were made on the same sample. A heavily-doped n-type Si with 100-nm thermally grown SiO_2 was used as the substrate. On top of a cleaned substrate, 60-nm

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Mo was sputtered to form the gate electrode for TFTs and bottom electrode for V-TFDs. Then, the bottom Mo layer was patterned using a RIE etch. Next, a 55-nm Al_2O_3 gate dielectric was deposited using atomic layer deposition at 250°C. The Al_2O_3 thickness was confirmed using spectroscopic reflectometry. To make an opening for bottom gate metal contacts for TFTs and to form the V-TFD active region, Al_2O_3 layer was patterned by wet etch, using a base solution. After solvent cleaning, five layers of ZTO solution were deposited using the process mentioned earlier. Next, the solution-processed layer was patterned by wet etch using an acid solution. This process completely etched the layer for device isolation and for bottom gate exposure for TFT measurements. Top electrodes of 100-nm Mo were then sputtered to obtain ohmic contacts for both TFTs and TFDs, and were patterned via lift-off. The fabrication steps are identical to those required for bottom-gate top-contact TFTs, and are illustrated in Figure 5.8. Thus, making our Mo V-TFDs does not require any extra fabrication steps beyond those used for TFT fabrication, which makes it attractive compared to other V-TFDs reported so far. *J-V*, BV characteristics and SEM images obtained from five-layer V-TFDs are shown in Figure 5.9.
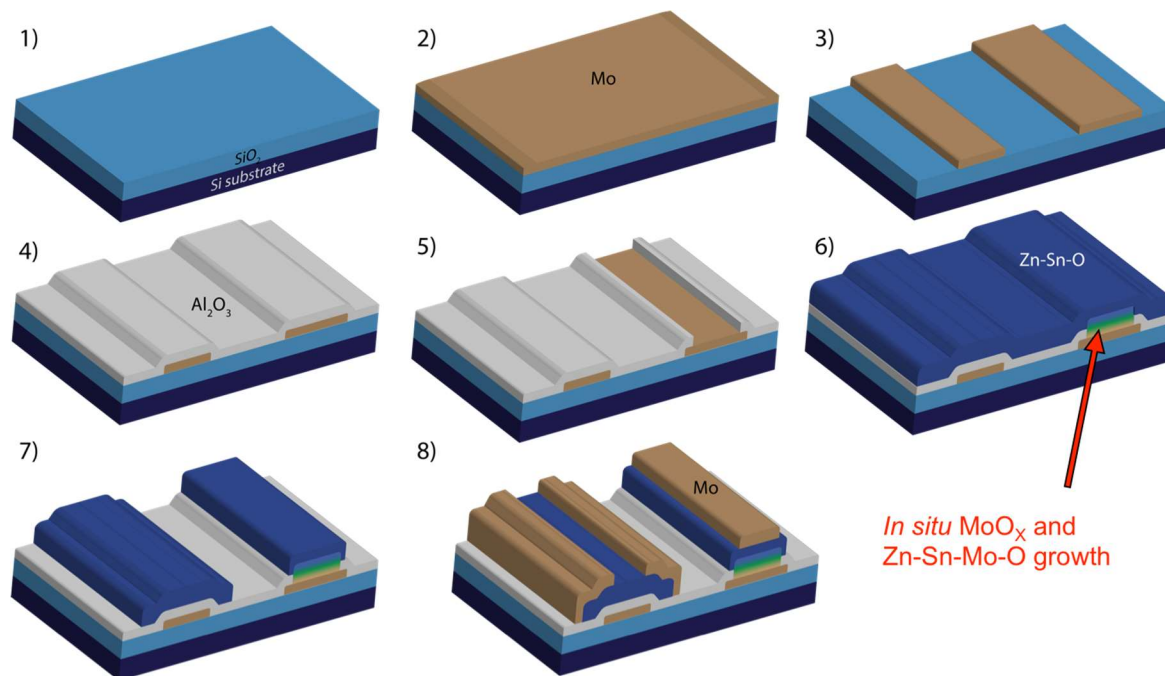
Figure 5.8 Fabrication steps of vertical thin-film diodes (V-TFDs) and lateral thin-film transistors (TFTs): 1) SiO_2 (100 nm)/Si substrate; 2) 60 nm Mo deposition via sputtering (Kurt J. Lesker Lab 18); 3) RIE etch of Mo (LAM 9400); 4) 55 nm of Al_2O_3 deposited by atomic layer deposition at 250°C (Oxford OpAL ALD); 5) Wet etch of Al_2O_3 using dilute NH_4OH; 6) Five-layer ZTO deposition, with each layer spin-coated and then pre-annealed at 520°C for 1 min. After final layer, post-annealing was performed at 520°C for 1 hr; 7) Wet etch of ZTO film using dilute HCl and HNO_3 solution; 8) 100 nm Mo deposition via sputtering (Kurt J. Lesker Lab 18), patterned by liftoff. Reprinted with permission from ref. [146].
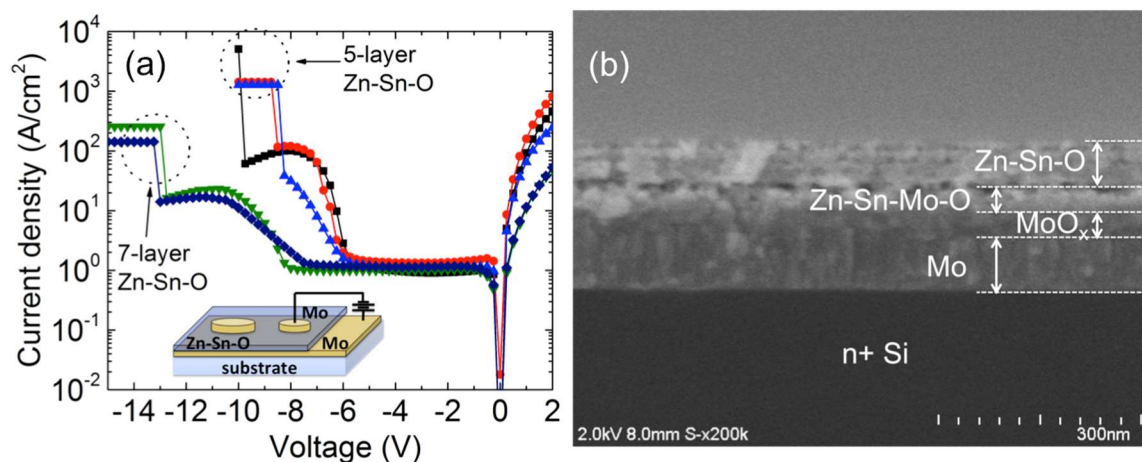
Figure 5.9 Mo:ZTO diode made with 5-layer ZTO. For comparison of V-TFD and TFT, we deposited five layers of ZTO instead of seven layers. Thus, *J-V* characteristics and BV were measured to confirm Mo:ZTO diode behavior for devices made with five-layers of ZTO. (a) BV of 5-layer V-TFD is slight lower (>8 V) than that of 7-layer V-TFDs (>10 V), but this BV range is still sufficient to harvest energy from commercial rectifiers with 200 mW of output power. (b) Cross-sectional SEM image obtained from the five layer ZTO on top of Mo. It shows similar features to the seven-layer case, with distinct MoO_x and ZTMO layers. The film thickness of ZTMO and ZTO together is ~150 nm. Reprinted with permission from ref. [146].

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The cross-sectional schematic of V-TFD and TFT integrated on the same substrate is shown in Figure 5.10 (a). Figure 5.10 (b) shows transfer curves and output curves of fabricated TFTs, with normal, enhancement-mode operation. For simple logic circuits, enhancement-mode is more desirable than depletion-mode, as it does not require level shifting [209]. For enhancement-mode TFTs to be used as rectifiers, however, the positive turn-on voltage limits the on-current of the diode-connected TFT (i.e., with gate and drain connected). TFT has additional weaknesses compared to the V-TFD, due to its long transit length (channel length) and narrow conduction area (cross-sectional area of thin film). In order to confirm the advantages of a V-TFD over a diode-connected TFT for rectifier applications, the two devices were measured and compared. Both devices were on the same sample, had the same size of 100 μm×100 μm. For the TFT, this area includes the top contact area. The microscope images of these devices are shown in Figure 5.10 (c) and (d). Due to the lower turn-on voltage, the larger conduction area (size of electrode), and shorter carrier transit length (film thickness) compared to a lateral TFT, the on-current of the V-TFD was more than five orders of magnitude greater than that of the diode-connected TFT, as shown in Figure 5.10 (e). Such high on-current of V-TFDs is important as it can not only reduce the voltage drop and increase the overall efficiency of rectifiers, but it can also enhance the operation frequency of the rectifier.
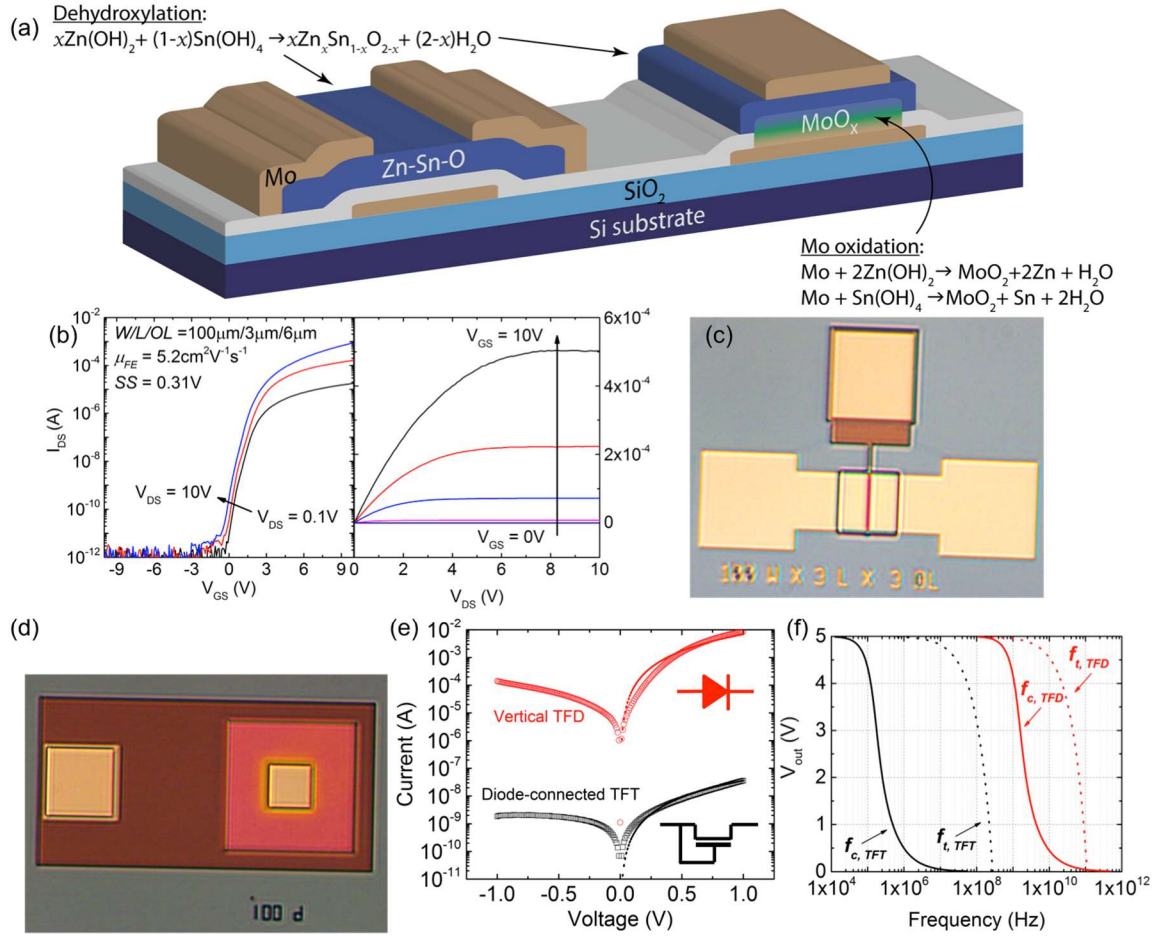
Figure 5.10 Comparison of Mo V-TFD and diode-connected TFT as rectifiers. (a) Schematic of fabricated V-TFD and TFT on the same substrate. Thin films with different chemical composition are grown via different chemical evolution during solution process. (b) Transfer curves (left) and output curves (right) obtained from a TFT with device dimensions of 100 μm in width, 3 μm in channel length, and 6 μm in overlap length, which leads to 100 μm×100 μm in overall size including source and drain contacts. (c) Microscope image of the TFT. (d) Microscope image of a vertical TFD fabricated on the same substrate. The size of top electrode is 100 μm×100 μm, the same effective device size as the TFT. (e) Comparison of I-V curves obtained from the TFT in (b) with its gate and drain connected, and from a V-TFD. Hollow circles and squares are measured data and dotted lines are the on-current model used to calculate $f_{c,TFT}$ and $f_{c,TFD}$ in (d). (d) Maximum operation frequencies calculated based on transit time (f_t) and measured on-current (f_c). Reprinted with permission from ref. [146].

The theoretical limits of operation frequencies for V-TFD and TFT were calculated for comparison. These were estimated using two approaches: the transit time of carriers (f_t) and measured on-current (f_c). f_t considers the time that it takes for the fastest electron (with velocity v) to transit from one electrode to the other (the carrier transit length, L). The equation of this frequency can be expressed as:

$$f_t = \frac{v}{2\pi L} = \mu \frac{V_{in} - V_{out}}{2\pi L^2}. \qquad\qquad (5.2)$$

L would thus be the channel length for a TFT (i.e., 3 μm) while it would be the film thickness for

V-TFD (i.e., 150 nm). V_{in} is the maximum input voltage applied to the rectifier, and V_{out} is the

DC output voltage, such that $V_{in} - V_{out}$ is the actual voltage across the rectifier that drives the

drift of an electron. For calculation, the Hall mobility extracted from the same five-layer a-ZTO

bulk film, reported earlier to be 5 cm^{2}V^{-1}s^{-1} [58], was used. With a fixed V_{in} of 5 V, f_t was

calculated versus V_{out} for both devices. These parameters are referred to as $f_{t,\ TFD}$, and $f_{t,\ TFT}$,

respectively. It is worth noting that the actual maximum frequency would be lower than these f_t

values as they overestimate the actual mobility of electrons. In the case of the TFT, a minimum

gate voltage is required to accumulate charges before they move with the given mobility 5 cm^{2}V^{-1}s^{-1}. This voltage is called the threshold voltage, V_T. V_T for our TFT was calculated to be ~3 V, as

shown in Figure 5.10 (b), but is not considered in Equation (5.2). In case of V-TFD, we showed

in Figure 3.6 that our V-TFD in fact consists of two different films, namely ZTMO and ZTO.

The carrier mobility across ZTMO layer is expected to be lower than the value of 5 cm^{2}V^{-1}s^{-1}

used for ZTO, because the on-current of Mo V-TFD was dominated by SCLC (Figure 4.9),

indicating low mobility Furthermore, the A^* value extracted by fitting leakage current with

Schottky emission (Figure 4.10) was very low, 0.74 Acm^{-2}K^{-2}, compared to that obtained from

PdO$_x$:ZTO [165], 44 Acm^{-2}K^{-2}. These values indicate a low mobility (or high m^*) of the ZTMO

layer compared to a-ZTO.

    A better way to calculate operation frequency of V-TFD and TFT would be the large-

signal analysis method used by *Steudel et al.* [210], which has also been used by others [20],

[167], [168]. In contrast to carrier transit time, f_c is determined by the speed at which the charges

consumed by the load (R_L) at V_{out} during one frequency cycle ($2\pi f_c$) becomes comparable to the

charge stored on the load capacitance (C_L) by the on-current going through the rectifier during the fraction of the cycle when the rectifier is in forward bias. Thus, it follows that $\frac{V_{out}}{R_L}\frac{1}{f_c} = \int_{t_1}^{t_2} I_{rectifier}\, dt$, where the rectifier is in on-state from t_1 to t_2. To calculate f_c, the measured on-current of the V-TFD and TFT in Figure 5.10 (e) were modeled using the equations, $I_{TFD} = A\frac{9\varepsilon_o\varepsilon_r\mu_{TFD}V_{forward}^2}{8L^3}$, and $I_{TFT} = \frac{\mu_{TFT}C_{ox}W}{2L}(V_{forward})^2$, which give μ_{TFD} of 0.15 cm^{2}V^{-1}s^{-1} and μ_{TFT} of 0.015 cm^{2}V^{-1}s^{-1}. Once again, these mobility values are quite low compared to the Hall mobility, and this difference is attributed to the presence of the ZTMO layer (for the V-TFD) and the threshold voltage (for the TFT). Based on these *I-V* equations, the maximum operation frequency for V-TFD ($f_{c,TFD}$) and diode-connected TFT ($f_{c,TFT}$) can be expressed as follows [195]:

$$f_{c,TFD} = \frac{9\mu_{TFD}}{16\pi L_{TFD}^2 V_{out}}\left\{\left(V_{in}^2 + 2V_{out}^2\right)\cos^{-1}\left(\frac{V_{out}}{V_{in}}\right) - 3V_{out}\sqrt{V_{in}^2 - V_{out}^2}\right\} \qquad (5.3)$$

$$f_{c,TFT} = \frac{\mu_{TFT}}{4\pi L_{TFT}^2 V_{out}}\left\{\left(V_{in}^2 + 2V_{out}^2\right)\cos^{-1}\left(\frac{V_{out}}{V_{in}}\right) - 3V_{out}\sqrt{V_{in}^2 - V_{out}^2}\right\} \qquad (5.4)$$

The calculated results of $f_{t,TFD}, f_{t,TFT}, f_{c,TFD}$, and $f_{c,TFT}$ are shown in Figure 5.10 (f). It is clear that V-TFDs have a higher operating frequency than TFTs connected in the diode configuration. The estimated maximum frequency of the V-TFD for V_{in} of 5 V and V_{out} of 3 V (i.e., the magenta line in Figure 5.7) may be as high as 1.6 GHz. This estimate agrees with the previous demonstration of gigahertz-range operation of AOS V-TFDs made with *a*-IGZO [16], [107]. The high operating frequency of the V-TFD is primarily due to the higher effective μ due to the lack of a turn-on voltage and the shorter L due to the vertical structure. For the TFT, L corresponds to the channel length (L_{TFT}=3 μm) while for V-TFD, it corresponds to the film thickness (L_{TFD}=150 nm).

5.4 Mo:ZTO rectifier for RFID energy harvester application

We have thus demonstrated a V-TFD technology that can be simply integrated with TFTs, in which the V-TFDs exhibit a much higher operation frequency and efficiency as a rectifier than diode-connected TFTs. This combined technology can significantly improve thin-film IC performance for future large-area electronics (LAE) [1]. An application of particular interest in LAE is the radio-frequency identification (RFID) tag, as its market size is projected to grow up to \$30.24 billion by 2024 [211]. A key enabler in expanding RFID tags to new applications is reducing tag cost [20]. The miniaturization of CMOS-based RFID chips has helped to reduce the cost of electronic components, but this approach requires pick-and-place of a small silicon chip onto the tag with high precision [1]. At present the attachment cost is a significant portion of overall tag cost [20]. Replacing the CMOS chip with thin-film electronics is thus expected to resolve the current bottleneck in lowering RFID tag cost, by reducing or eliminating the packaging/attachment cost. Our unique thin-film process that can simultaneously fabricate both TFTs and V-TFDs in air without the need of vacuum deposition tools can provide a straightforward way to further reduce RFID tag cost. In order to obtain thin-film based RFID tags, one of the key tasks is to build energy harvesters out of rectifiers to convert AC power inductively coupled from an antenna into DC power that can be used to operate logic circuitry within the RFID tag. As explained in Section 5.3.3, our Mo V-TFDs show superior rectifier performance compared to diode-connected TFTs.

With this understanding, in this section we investigate Mo:ZTO V-TFDs for their wireless energy harvesting application in future RFID tags. For this test, a full-wave rectifier (FWR) made out of four 100 μm × 100 μm Mo:ZTO V-TFDs was fabricated. The full-wave rectifiers were wire-bonded to a printed circuit board (PCB) on which the load components and

SubMiniature version A (SMA) connectors were soldered. Prior to attaching the RFID antenna, the FWR was first tested in a wired configuration. Its full-wave rectification, frequency response, and input voltage dependence tests are shown in Figure 5.11 (a), (b), and (c), respectively.

Next, to validate its applicability for wireless energy harvesting, a commercial 13.56 MHz RFID tag reader (DLP-RFID1, DLP Design) and antenna (DLP-RFID-ANT, DLP Design) were used. The reader has an output power of 200 mW and a read range of 10 cm (Protocol: ISO 15693 and ISO 18000-3). As shown in Figure 5.11 (d), the PCB was connected to the antenna to assess the energy harvested via inductive coupling from a commercial RFID reader. The circuit diagrams of the wireless test setup for both input and output voltages are shown in Figure 5.11 (e). The AC voltage (V_{in}) delivered to the antenna via inductive coupling was measured using 1 MΩ load resistor (Figure 5.11 (e), bottom). As shown in Figure 5.11 (f), the maximum peak-to-peak V_{in} coupled from the reader to the antenna at 0 mm of distance was ~8.7 V, which gives the output power of the reader to be $V_{rms}^2/50\,\Omega \approx 190$ mW. For DC output voltage (V_{out}) measurement, a 1 µF load capacitor and 1 MΩ load resistor attached to PCB via surface mount were connected to the full-wave rectifier as shown at the top of Figure 5.11 (e). The result, shown in the Figure 5.11 (f) inset, measured with an oscilloscope, is excellent AC-DC conversion using the V-TFD FWR for wireless energy harvesting. DC output voltages are measured across the load as a function of distance, with V_{out}/V_{in} exceeding 80% at < 40 mm of distance. At 0 mm, V_{out} as high as ~5 V is obtained, which demonstrates that V-TFDs rectifiers can be used to power thin-film logic circuitry. In order to obtain even higher V_{out} with a larger antenna-reader distance, a voltage multiplier configuration can be implemented.
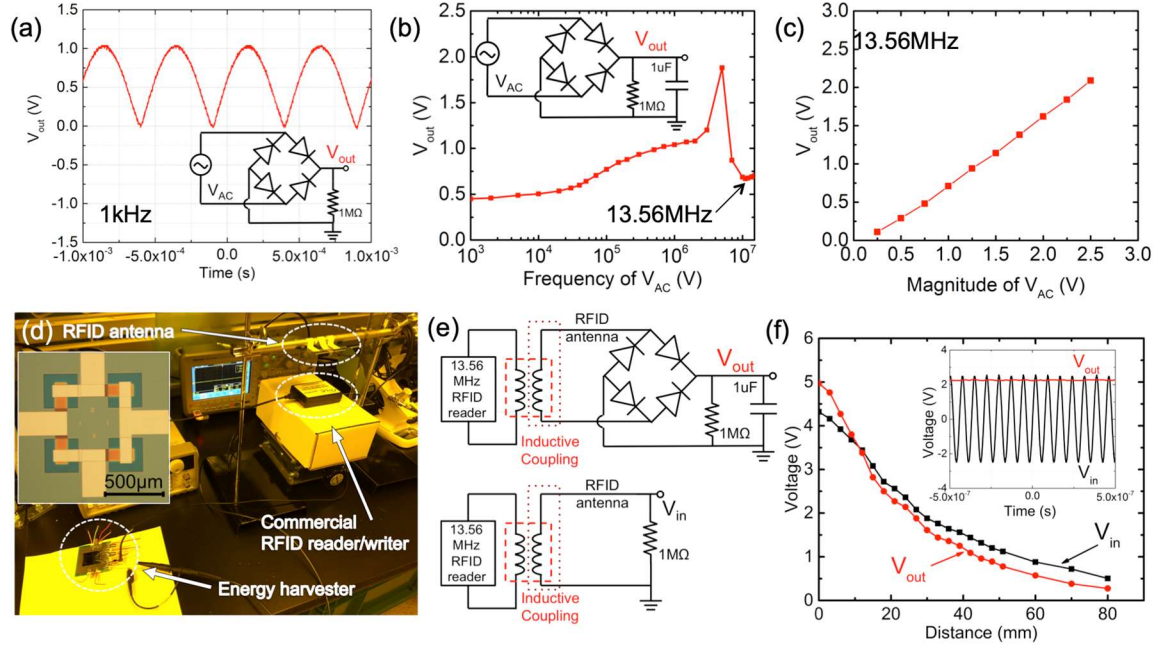
Figure 5.11 Full-wave rectifier (FWR) measurements in wired configurations (a)-(c) and wireless configurations (d)-(f). For (a)-(c), the input AC voltage was supplied by an HP 33120A function generator. Voltage measurement was done using a Tektronix MSO2024b oscilloscope. To ensure that V_{AC} floats from the ground of the load, an isolation transformer was used to power the function generator and isolate its ground from the ground of the oscilloscope. (a) In order to confirm operation of full-wave rectifier, a 1 MΩ load resistor was attached without a smoothing capacitor. For a peak-to-peak 3 V 1 kHz AC signal (V_{AC}), the voltage at the output node (V_{out}) has a period of 5×10^{-4} s, indicating rectification of a full cycle. (b) The frequency response of a FWR measured by sweeping the frequency of the function generator from 1 kHz to 15 MHz, while measuring DC V_{out} across the load. To obtain the DC output voltage, a smoothing capacitor of 1 μF was used, as shown in the inset. We notice that V_{out} peaks at 7 MHz, which is attributed to resonance effects from parasitic inductances within the printed circuit board (PCB). (c) For a 13.56 MHz AC signal, the magnitude of input voltage (V_{AC}) is compared with the measured DC V_{out}. (d) Wireless energy harvesting experimental setup. A commercial HF (13.56 MHz) RFID antenna and reader with 200 mW output power were placed in parallel. The power from the reader was wirelessly harvested using the antenna while the distance between them was varied. The antenna was attached via SMA connection to an FWR wire-bonded onto a PCB with surface-mount loads. The DC output voltage of the FWR was measured with an oscilloscope. The inset shows a microscope image of a FWR with four 100 μm × 100 μm V-TFDs. (e) Circuit diagrams showing the wireless energy harvesting measurement setup (top). To compare the measured V_{out} with V_{in}, V_{in} was measured as the voltage across a 1 MΩ resistor attached to the antenna, without the rectifier included (bottom). The maximum peak-to-peak V_{in} obtained at a distance of 0 mm was ~8.7 V, which gives $P_{out} = V_{rms}^2/50\ \Omega \approx 190$ mW, close to the maximum output power of the reader. (f) The magnitude of V_{in} and V_{out} as a function of separation distance. V_{out} exceeds over V_{in} when the distance is < 10 mm, which is attributed to resonance due to mutual inductance. The inset shows V_{in} and V_{out} measured over time with the antenna and reader separated by a distance of 21 mm. Reprinted with permission from ref. [146].

5.5 Conclusion

In Chapter 3 and 4, we successfully fabricated two different versions of V-TFDs by forming Schottky contacts with various bottom metals, namely Pd and Mo. The main goal of V-TFD fabrication is to achieve a rectifier that can surpass the performance of a diode-connected

TFT, so that diodes can be used to further enhance the application of thin-film ICs, e.g., by providing wireless energy harvesting capability as explained in Section 3.1. Our PdO_x:ZTO diode was the first solution-processed AOS V-TFD to be reported [101], and it allows higher on-current compared to Mo:ZTO diodes. However, the PdO_x:ZTO V-TFD faces two major challenges for practical applications. The first challenge is its poor voltage handling capability. As shown in Figure 5.2, the PdO_x:ZTO V-TFD suffers from low BV and severe degradation when in reverse bias, which limit its use as a rectifier: The rectifier degrades within short period of time (tens of minutes) and breaks down at low input AC voltage (5 V_{pp}), as shown in Figure 5.4. These limitations came from V_O migration within the *a*-ZTO film. This must be overcome to make a useful rectifier. The second challenge for PdO_x:ZTO V-TFDs is fabrication complexity. As with previously reported AOS thin film diodes [101], [118], [212], forming rectifying contacts with Pd require deposition and patterning of a new high work function Schottky metal, followed by sophisticated oxidation steps in order to reduce oxygen vacancy defects near Schottky interfaces. These additional process steps make V-TFDs incompatible with TFT fabrication. This has led to the frequent use of diode-connected TFTs in rectifiers (by shorting the TFT gate and drain to form a two-terminal device), as introduced in Section 3.1. However, diode-connected TFTs exhibit intrinsically poor rectifier performance due to the lateral flow of current through a thin film.

Our V-TFDs made via a Mo:ZTO junction show promising features to address these challenges. Mo V-TFD has a high BV of over 10 V, and constant leakage current prior to breakdown. In addition, Mo:ZTO diodes did not show any degradation during reverse bias, even when relatively high voltages of 6 V and 8 V were constantly applied for up to 60,000 sec. Thanks to these features, stable operation of Mo:ZTO diodes in half-wave rectifiers was

demonstrated, showing a great improvement over the PdO$_x$:ZTO diode rectifiers. The Mo:ZTO V-TFD rectifier could rectify AC inputs as high as 10 V$_{pp}$ and up to 15 MHz, the maximum frequency of our signal generator. The advantageous features of the Mo:ZTO diode reverse characteristics are attributed to the formation of ZTMO layer via *in situ* diffusion. In addition to its high-voltage and high-frequency handling capability, the Mo:ZTO diode provides a critical advantage in its fabrication process. As shown in Figure 5.8, Mo:ZTO diodes can be fabricated alongside ZTO TFTs without requiring any additional process. This is made possible by harnessing the chemical evolution of our ink that is controlled by the material underneath, and simultaneously growing both rectifying junctions and high-quality AOS channel layers. As a result, using a single fabrication process we are able to integrate high-voltage diode rectifiers - which can operate at a much higher frequency than TFT rectifiers - alongside TFTs, which can be used for future digital circuitry. To our knowledge, this is the first report of simultaneous formation of different materials via chemical evolution of ink in order to fabricate different active circuit elements with a single solution-process. The resulting high voltage and high frequency operation of V-TFDs enables wireless energy harvesting from a commercial high frequency (HF) RFID reader. We note that Mo is one of the most commonly used metal electrodes for AOS TFTs due to its high-quality ohmic contact properties with various AOS. Thus, our exploitation of Mo interaction with *a*-ZTO may be widely adapted to other AOS.

Chapter 6 Top-Schottky contacts for 3D monolithic integration of thin-film IC

6.1 Introduction

In addition to low-cost chip-less RFID circuitry, thin-film electronics can be applied to Si-based electronics for beyond-Moore. Two-dimensional device scaling guided by Moore's law has enabled an exponential increase of the performance-to-cost ratio in Si CMOS (Complementary Metal-Oxide-Semiconductor) integrated circuits (ICs) over the past fifty years [4]. The rapid development of new applications in artificial intelligence and internet-of-things demands further IC performance enhancement. Because device scaling cannot continue indefinitely, multiple routes to improve system performance, termed "More-than-Moore," are being explored, including novel computing methods, device structures, and integration schemes [5]. Three-dimensional (3D) integration, in which multiple layers of active components are vertically wired together, offers a way to increase the areal device density further [5]. In addition to a smaller form factor, vertical integration can greatly reduce interconnect delays, which play a dominant role in limiting overall performance of deep sub-100 nm Si process nodes [213]. 3D integration can be done at the package-level [214], die-level [215], wafer-level [216], or device-level [217]. Device-level integration, i.e. monolithic 3D integration, is the most attractive of these to achieve maximum performance enhancement and miniaturization. Monolithic 3D integration occurs when additional layers of devices are directly fabricated on top of Si CMOS wafers. Such monolithic integration also eliminates the need for additional processes, such as via/metal bump formation, wafer thinning, pick-and-place, and aligning/bonding processes that are necessary for wafer-, die- or package-level integration.

For device-level integration to be feasible, the top device layers must be deposited at process temperatures compatible with back-end-of-line (BEOL) Si CMOS (<525°C) [218], with uniformity across large wafers (>8" diameter), and at low cost. In this work, we demonstrate, for the first time, monolithic integration of solution-derived amorphous oxide semiconductor (AOS) thin film transistors (TFTs) on top of a Si IC containing fin-shaped Field Effect Transistors (finFETs), without degrading the Si transistor performance. Solution-processed AOS offers a low thermal budget, large-area uniformity, substrate agnosticism, and low integration cost, and can avoid tool contamination issues, making it an attractive choice for monolithic 3D integration among the materials under consideration (Table 6.1).

Table 6.1 A brief summary of additive device layers on Si CMOS IC						
3D layer	Deposition method	Large-area uniformity	Tool contamination issue	3D-IC demonstration	Integration yield	Ref.
Poly-Ge	Flash-lamp annealing after sputtering a-Ge	N	Y	N	**high**	[219]
Poly-Si	Laser annealing after a-Si deposition	N	Y	**Y**	**high**	[220]
CNT	CNT layer transferred from quartz substrate	**Y**	**N**	**Y**	low	[221]
MoS$_2$ WSe$_2$	Exfoliation of MoS$_2$ flakes & pick-and-place of WSe$_2$	N	**N**	N	low	[222]
c-IGZO	Direct sputtering	**Y**	Y	**Y**	**high**	[223]
a-IGZO	Direct sputtering	**Y**	Y	N	**high**	[6]
a-ZTO	Direct spin-coating	**Y**	**N**	**Y**	**high**	This work

Table 6.1. The desirable features are written in bold. A low thermal budget (≤500°C) have been demonstrated with all of the materials listed. Our method of in-air monolithic integration of indium-free AOS has high process advantages over other candidates, including large-area uniformity, tool contamination issue, and integration yield. The column "3D-IC demonstration" indicates whether the proposed methods were experimentally integrated on active Si CMOS devices.

In this chapter, we explore solution-processed AOS for in-air monolithic integration of AOS 3D-IC on Si CMOS. Thus, we first confirm the integration capability of our in-air deposition, by fabricating standard metal-insulator-semiconductor field-effect transistors (TFT MISFETs, characterized in Chapter 2) on top of a Si finFET IC (100 nm node), without degrading the Si CMOS performance. The additional device layers should provide new

capabilities to the underlying Si IC, to enhance chip performance and functionality for a given area. Previously, monolithic integration of ReRAM [224], [225], DRAM [223], digital logic [225], and power management [224] circuit onto Si ICs has been demonstrated using various materials and devices. Here, we focus on a different application: the integration of high-voltage (HV) ICs onto low-voltage (LV) microcontroller units (MCUs) [6], [226], [227]. Today's multi-functional products require LV MCUs to be assembled at the board-level with HV loads and supplies [228], which in turn requires HV interface ICs to bridge between the two. Here, by LV we mean typical supply voltages for Si CMOS of ~1 V, and by HV we mean voltages anywhere from 2 V to >100 V, which are too large to be used with standard low-voltage CMOS technologies. AOS TFTs made using a MISFET (metal-insulator-semiconductor field-effect transistor) structure have previously been exploited for several HV IC applications, including display drivers [229], power switch drivers [6], audio amplifiers [230], ESD protection [231], and wireless energy harvesting [108]. Using our process, AOS HV interface circuits can be directly deposited on top of LV Si MCUs, providing a bridging layer to external HV loads and supplies, without requiring separately-packaged interface ICs [6], [226] (Figure 6.1(a)).

For effective bridging, the HV interface circuits must not only be able to handle HV, but should also be able to be driven by the LV digital signals output by the MCU. The latter may be challenging if the HV AOS circuits are fabricated using only MISFETs, due to relatively large MISFET switching voltages of >1.5 V (Figure 6.1(a)). In order to solve this issue, we use the same solution-processed AOS layer to realize two different devices, and with these devices we fabricate an AOS thin film IC that can be switched at LV. The two devices are the solution-processed AOS metal-semiconductor field-effect transistor (MESFET) and vertical thin-film Schottky diode (V-TFD) with a top Schottky contact (Figure 6.1(b)). These devices supplement

the capabilities of AOS MISFETs, enabling HV logic inverters with narrow transition width (<1 V for a supply voltage of 5 V) and HV rectifiers with low turn-on voltage (<0.5 V). In addition, the devices here show the best switching performance when compared with other AOS MESFETs and V-TFDs reported so far. To explain the operation of these high-quality devices, we comprehensively analyze the interface and electrical properties of Ag_xO top-Schottky and Pd bottom-ohmic contacts to solution-processed AOS.
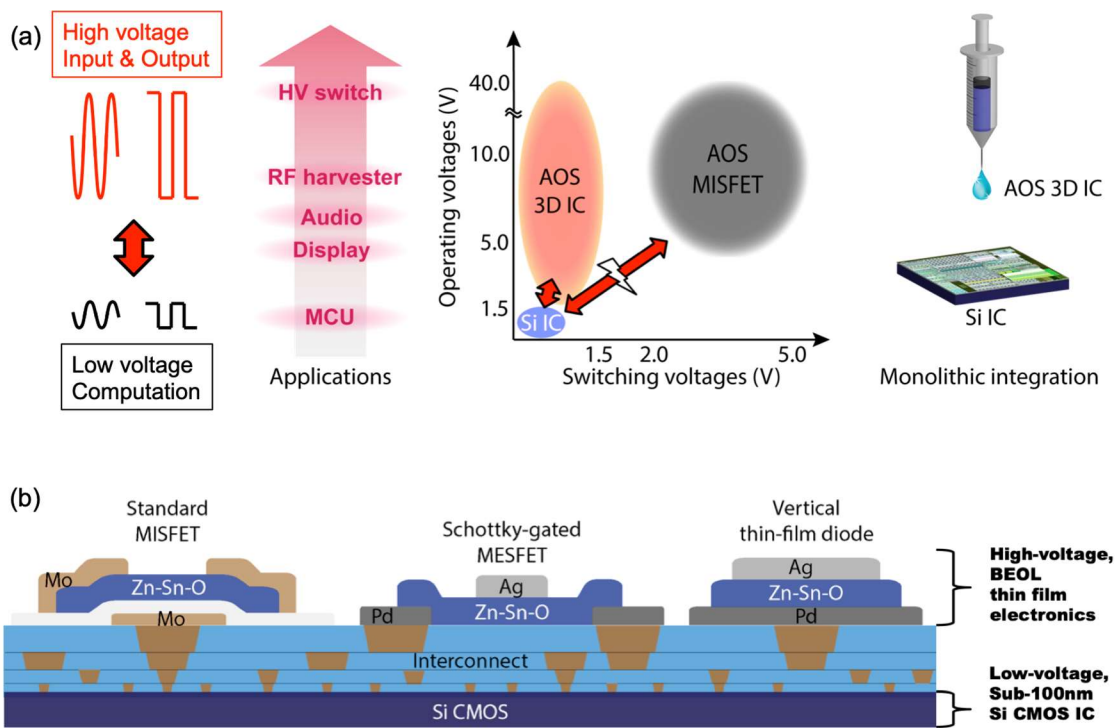
Figure 6.1 The opportunities and challenges of AOS 3D IC on Si MCU (a) Illustration of monolithic 3D integration of AOS circuits for HV-to-LV bridging of sub-100 nm Si MCUs with other HV applications. Possible uses for HV 3D AOS circuits are in HV power driver circuits, RF energy harvesting, audio amplifiers, and display drivers. The key contribution of this work is the realization of monolithically integrated AOS circuits deposited directly on 100 nm Si CMOS in air, with reduced switching voltage enabled by the introduction of MESFETs and V-TFDs. (b) Conceptual image of monolithic integration of various AOS thin-film devices on sub-100 nm node LV Si CMOS IC. The heights of thin-film devices are exaggerated to illustrate their structures.

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6.2 Monolithic integration of AOS MISFETs on Si CMOS

Monolithic 3D integration of additional transistor layers on Si CMOS ICs has so far been demonstrated with epi-like re-crystallized Si [220], c-axis-aligned crystalline (CAAC) IGZO [223], and carbon nanotubes [221]. There are many challenges in using these materials to obtain good electrical performance at process temperatures below 525°C, including grain-boundary-limited performance, film non-uniformity, and difficulty in using layer transfer processes or serial re-crystallization processes to obtain high-yield and high-density circuits for mass production (Table 6.1). Among the low-thermal-budget and substrate-agnostic thin film materials available, AOS provide unique advantages for monolithic 3D ICs: high carrier mobility, wide band-gap, and large-area device uniformity. These features have allowed AOS to dominate the active-matrix display TFT backplane industry. The commercial success of AOS display technology can now be extended to realize monolithic 3D IC [232]. Here, we use a solution process that allows deposition of high-quality semiconductor layers in air, without the need of a vacuum deposition process module [58]. This not only leads to low capital equipment cost, but also removes contamination issues caused by transferring BEOL wafers to the FEOL (front end of line) process flow for 3D integration [233]. Therefore, by choosing a solution-process route for AOS deposition, we can achieve monolithic 3D integration with the highest performance-to-cost ratio possible, which has been the critical driving force for Moore's law.

We have achieved monolithic integration AOS TFTs on BEOL Si CMOS using a solution process to deposit the semiconductor layer. As explained in Chapter 2, the highest temperature during our entire integration process is 520°C for 1 hr (thermocouple reading of 490-500 °C), which is below the BEOL thermal budget of standard Si CMOS [218]. In order to verify this thermal budget, prior to AOS integration we tested Si CMOS devices after annealing

at various temperatures up to 520°C. The Si CMOS used here are test die made using a 32 nm industry standard state-of-the-art process. The finFETs have 2 nm HfO$_2$ as a high-k gate dielectric and 15 nm TiN metal gate, with a minimum channel length (L) of 100 nm. FinFETs with L=100 nm have maximum operation voltage of ~1.5 V and thus are good target MCU component to be integrated with HV 3D-IC.

Dozens of finFETs with L=100 nm and 150 nm were measured after hot plate annealing at various temperatures for one hour in nitrogen. Due to the short-channel effect, at high V_{DS} the carrier velocity saturates and the resulting I_{DS} at high V_{GS} becomes [234] $I_{DS,sat} \approx W C_{ox} v_{sat}(V_{GS} - V_T)$. Here, $I_{DS,sat}$ is I_{DS} at saturation, v_{sat} is the carrier saturation velocity, and V_T is the threshold voltage. Using this equation, V_T and transconductance (g_m) were extracted from the transfer characteristics taken at V_{DS}=1.25 V and V_{GS} from -1 V to +1.25 V, where linearity of I_{DS} and V_{GS} is observed at high V_{GS}. The x-axis intercept and the slope of linear regression are used to extract V_T and g_m, respectively. V_T and g_m of the NMOS and PMOS finFETs are shown in Figure 6.2. The extracted device parameters show marginal change with annealing up to 500 °C.
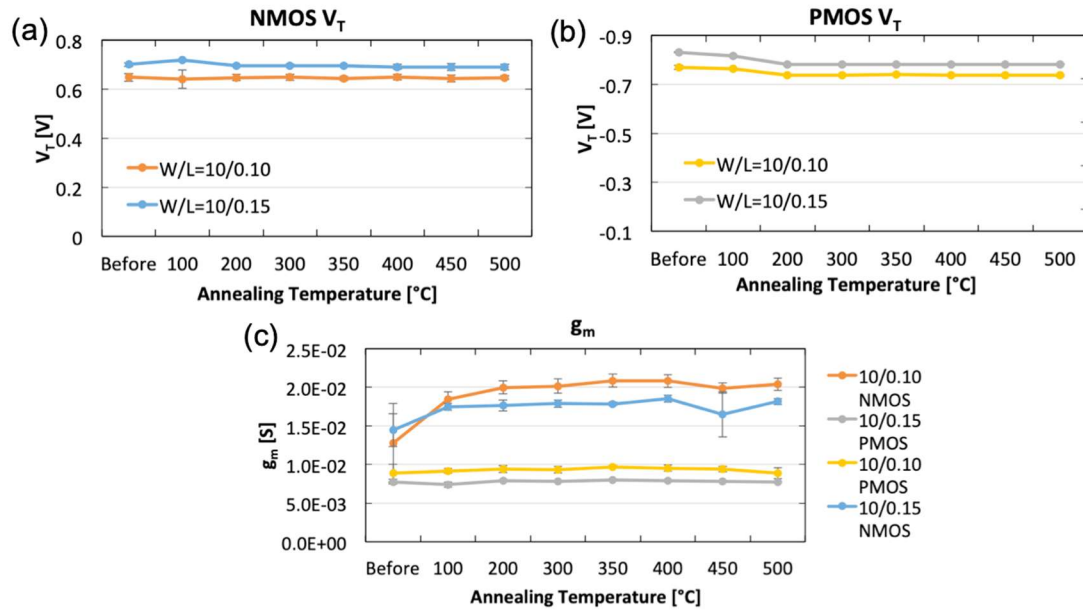
Figure 6.2 Verifying thermal budget of 100 nm-node Si finFET. Each data point is the average of five to six finFETs tested with the same dimensions. The error bars indicate the standard deviation of the measured parameter values. The temperatures listed are measurements from a thermocouple. The temperature setting of the hot plate was slightly higher (e.g., set at 540 °C to get 500 °C). The legends show device dimensions in μm. Threshold voltages (V_T) were extracted and compared in (a) for NMOS, and (b) for PMOS. In (c), transconductance (g_m) was extracted and compared. These plots confirm that the 100 nm-node Si finFETs can withstand sufficient thermal processing to enable monolithic 3D integration of our solution-derived AOS devices.

To accomplish monolithic 3D integration of AOS TFTs (Figure 6.3 (a)), the BEOL Si CMOS was first passivated with 1 μm PECVD (plasma enhanced chemical vapor deposition) oxide, then 40 nm Mo was sputtered and patterned by RIE (reactive ion etching) to form the MISFET bottom gate electrode. Al$_2$O$_3$ gate dielectric was deposited by ALD (atomic layer deposition) and patterned by wet etching. Next, the AOS solution was dispensed and spin-coated. Here, we use amorphous zinc tin oxide (*a*-ZTO) due to its earth-abundant and non-toxic composition as opposed to AOS containing indium [44]. Three layers were spin-coated. After each coating step, the film was annealed at 520°C for 1 min. After three coating steps, the film was annealed at 520°C for 1 hr and then patterned via wet etching. Lastly, 100 nm Mo was sputtered to form top ohmic contacts to *a*-ZTO [59], and patterned with lift-off. A microscope

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image of the completed Si finFET chip with AOS TFT monolithically integrated is shown in Figure 6.3 (b).

After TFT integration, both Si CMOS and AOS TFT devices were tested to confirm compatibility of our solution process for monolithic integration on Si CMOS. As expected, both AOS TFTs and Si finFETs show normal device behavior (Figure 6.3 (c) and (d)), and finFETs are not affected by the TFT process. Therefore, solution-derived AOS can realize monolithic 3D integration on Si, allowing direct deposition of additional device layers to enable greater functionality. A key advantage of the process demonstrated here is that the *a*-ZTO deposition and patterning steps are done in air [58], offering a large-area, low-cost deposition method, and eliminating contamination issues that arise when new process modules are added. The annealing conditions used here are typical for solution-derived AOS [235], [156]. While conventional sol-gel or decomposition-based process require temperatures ~500°C [236], in the future we can consider routes to lower the temperature to below 350 °C, including combustion [40], UV-assisted annealing [209], and redox methods [236]. Moreover, our demonstration of CMOS robustness to annealing paves the way for other solution processes to be explored for other desperately needed 3D-IC technologies, such as dense vertical interconnect [225].
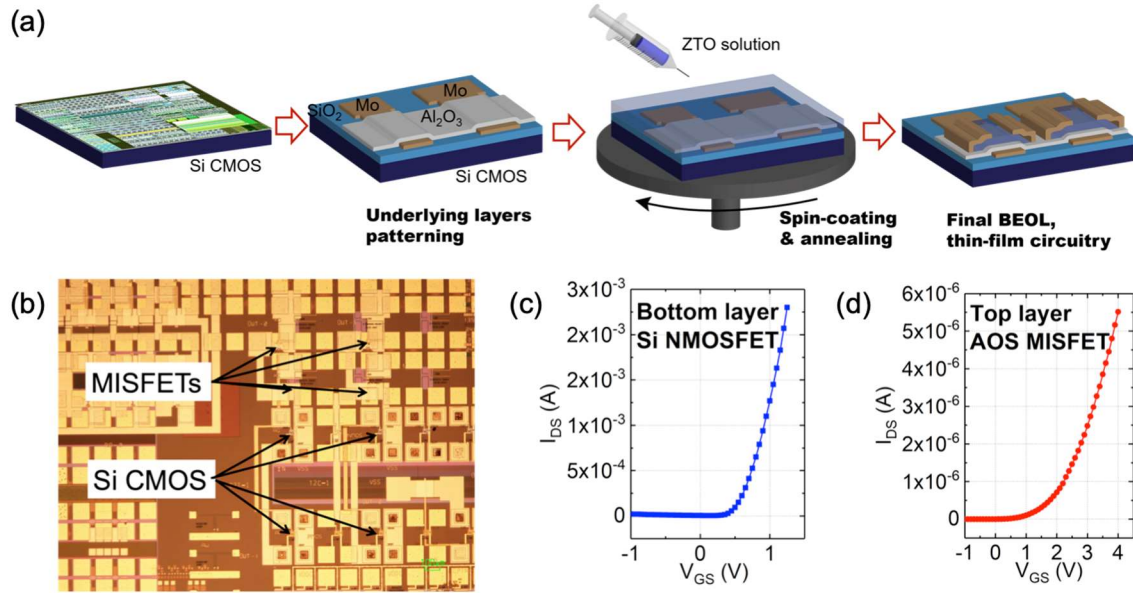
Figure 6.3 Monolithic integration of AOS thin-film devices on Si CMOS using our solution process (a) Simplified schematic of in-air additive fabrication of thin-film electronics on CMOS ICs using a solution process. (b) Microscope image of *a*-ZTO MISFETs fabricated on Si CMOS. Typical transfer curves in (c) of bottom layer Si NMOS with *W/L*=10 μm/150 nm, tested at V_{DS}=1.2 V, showing normal operation after additive fabrication of TFT and in (d) of top layer *a*-ZTO TFT with *W/L*=10 μm/7 μm, tested at V_{DS}=3.0 V.

Monolithically integrated AOS thin-film devices are uniquely beneficial for HV/LV interface circuits. Thanks to Si device scaling, the supply voltage (V_{DD}) of sub-100 nm node Si CMOS ICs is less than 1.2 V, allowing low power consumption [228], [237]. Although such a low voltage is desirable for efficient digital computation, LV digital ICs must interface with other components that use higher voltages. These HV components include power management systems accessed via input/output (I/O) bridging circuits [6], [226], on-chip power conversion such as AC-DC rectification [106], [107], and electrostatic discharge (ESD) protection [231], [238]. Versatile and compact autonomous devices require integration of diverse sub-blocks with HV/LV management and voltage conversion capabilities [228]. Therefore, monolithic 3D integration of HV power management circuits and LV Si MCU will be critical for future system-on-chip (SoC) designs. While HV Si CMOS processes are commercially available, these processes use larger feature sizes and thus cannot offer the same LV digital performance as

dedicated LV Si CMOS technologies. Alternatively, Si-based HV ICs could be fabricated separately and integrated on top of LV ICs, but this brings additional packaging, bonding, alignment issues, and does not meet the goal of monolithic 3D integration. Therefore, monolithic 3D integration of HV AOS thin film circuits on LV Si ICs is an attractive route to enhance functionality with minimal area and cost increase.

One challenge that must be overcome to realize this vision of monolithic 3D integration of HV AOS with LV Si ICs is reduction of the switching voltage of AOS circuits. The most common AOS transistor structure is the MISFET. AOS MISFETs typically have subthreshold slope (SS) of > 200 mV/dec [235], whereas the slope for c-Si finFETs is close to the Boltzmann limit of $\sim$70 mV/dec. Moreover, unlike Si, high-quality p-type AOS is yet to be reported [28], and therefore achieving bipolar AOS TFT inverters is challenging to date. As a result, while scaled Si CMOS ICs operate at < 1.5 V, AOS MISFET-based circuits typically require > 1.5 V for switching. For a single TFT, MISFET has $V_{switch} > 1.5$ V. Here, V_{switch} is defined as the gap between the turn-on voltage and the threshold voltage, V_T. For unipolar TFT inverter, using enhancement-mode MISFET for both drive-TFT and load-TFT leads to $V_{tran} > 1.5$ V. Here, V_{tran} is transition width where the digital logic value is undefined. This voltage mismatch means that LV Si CMOS cannot be used to switch AOS MISFET-based ICs, making integration of the two device layers difficult. Therefore, a different TFT that has low V_{switch} and can form an inverter with low V_{tran} should be developed. To achieve a full-swing unipolar inverter with low V_{tran}, it is desirable to use an enhancement-mode device for the drive-TFT [239], and a depletion-mode device for the load-TFT. This requires co-integration of enhancement and depletion-mode devices within the same monolithic 3D process. In summary, both HV handling and LV

switching capabilities are key factors to enable HV AOS 3D IC, but if only MISFET devices are available, the latter becomes a challenge.

6.3 Top-Schottky and bottom-ohmic contacts with AOS

6.3.1 Experimental section

The remaining part of this chapter will focus on achieving new types of thin-film devices made out of the same ZTO solution process used elsewhere in this thesis. By making devices other than MISFETs, the goals are: (i) to make a TFT switch with a V_{switch} lower than 1.5 V; (ii) to make a TFT with negative V_T such that an inverter with V_{tran} lower than 1.5 V can be obtained; and (iii) to make a rectifier with a V_{switch} lower than 1.5 V. As shown in Figure 6.1 (b), our approach is to develop high-performance MESFET and V-TFD devices that can be integrated with MISFETs. However, the fabrication of these devices requires a high quality Schottky contact. In order to obtain an ideal Schottky contact with AOS, a high work function metal should be in direct contact with AOS, forming an abrupt junction with minimum defects at the interface and within the bulk close to the interface. One of our conclusions in Chapter 4 was that it is difficult to obtain such a clean interface when using bottom Schottky electrodes combined with our solution-processed ZTO deposition, because of various interface chemistries (e.g., redox, diffusion, doping, crystallization, and alloy formation) happening simultaneously during solution annealing. To obtain high-performance MESFETs and V-TFDs, this process challenge should be resolved. Therefore, in this chapter, we focus on obtaining high quality Schottky contacts using a top-Schottky contact and bottom-ohmic contact structure. The key idea is that since the top metal electrode is not exposed to high temperature during AOS deposition, undesired interfacial reactions are minimized, allowing a sharp and clean Schottky interface.

Using this approach, the fabrication of MESFETs and V-TFDs are performed using the following procedures.

Heavily-doped *n*-type Si (n^{++}-Si (Sb), 0.01-0.02 Ω·cm, <100>) with 100nm thermally grown SiO$_2$ was used as the substrate, which was solvent-cleaned and dried. 100 nm/10 nm of Pd/Ti was evaporated to form the bottom electrode (Angstrom Engineering Evovac Evaporator), and patterned by lift-off resist. After solvent cleaning, five layers of ZTO were deposited and patterned via wet etching. Prior to top electrode deposition, O$_2$ plasma was performed at 60 °C and 100 W for descum. The top electrode of 10 nm/100 nm of Pd/Ag was then evaporated to form a Schottky contact to *a*-ZTO (Cooke Evaporator), and patterned with lift-off. Pd was deposited as capping layer to prevent further Ag oxidation in ambient and to ensure equipotential surface during measurement [175].

After fabrication, the contacts were analyzed via electrical and material characterization. For TEM measurements, an *in situ* FIB lift-out cross-sectional specimen was studied by using a JEOL JEM-3100R05 analytical electron microscope (AEM) attached with double Cs-correctors operated at 300 keV. Element mapping was conducted using X-ray signals with the microscope performed in scanning transmission electron microscopy (STEM) mode. High-angle annular dark-field (HAADF) images were taken for defining mapping regions. High-resolution transmission electron microscopy (HRTEM) imaging was performed with the microscope operated in conventional TEM mode. XPS was measured using Kratos Axis Ultra XPS. A monochromatic Al x-ray source (8 mA and 14 kV) was used pass energy of 20 eV, and step size of 0.1 eV. The Kratos charge neutralizer system was used. Argon ion sputtering was used with energy of 5 kV and ion source extractor current of approximately 90 µA, which resulted in a sputtering rate of 2-3 nm·min^{-1}. The depth profile was taken with 3-min sputtering cycles until

the Pd 3d peak is observed. Then, the Zn $2p_{3/2}$ and Sn $3d_{5/2}$ peaks measured at this point were analyzed by fitting the measured data using Gaussian–Lorentzian curves and a linear background. The XPS curves were analyzed using CasaXPS software version 2.3.17PR1.1. For TLM measurements, the *I-V* measurements were done using an HP4156A semiconductor parameter analyzer. For charge transport analysis, temperature-dependent *I-V* measurements were taken using an HP4156A semiconductor parameter analyzer with a Lakeshore Cryotronics TTPX cryogenic probe station.

6.3.2 Top Schottky contact using Ag

The excellent performance of the solution-processed AOS MESFET and V-TFD described above are due to high-quality top-Schottky and bottom-ohmic contacts. Here, we have used a low work function (Φ) metal, Ag, for the Schottky contact and a high-Φ metal, Pd, for the ohmic contact (Figure 6.4 (a)). Previous studies of AOS rectifiers used high-Φ metals (e.g., Pd) to obtain Schottky contacts, but their results showed that sophisticated surface treatments are often necessary to achieve the Schottky junction [101], [118]. Without these additional treatments, high-Φ metals tend to form alloys or create oxygen deficiency-related defects within AOS upon annealing, causing the contact to be ohmic rather than Schottky [101], [240] as we showed in Chapter 3. Therefore, for AOS, high quality Schottky contacts typically have required oxidized noble metals such as Ag_xO [117], PdO_x [118], and PtO_x [212]. In this work, we choose to form a bottom ohmic contact using Pd, by exploiting its *in situ* alloy formation during *a*-ZTO deposition to obtain an ohmic contact [101]. To get a high quality Schottky contact, we selected Ag as a top electrode. The evaporated layer of Ag oxidizes after deposition to form a Schottky

contact via Ag_xO [241]. In order to confirm the mechanisms of Ag oxidation and Pd alloy formation, we performed extensive materials characterization.

To study the top Schottky contact, scanning transmission electron microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDS) were carried out near the Ag/a-ZTO junction. Figure 6.4 (b) shows that the Ag layer close to the a-ZTO interface has become O-rich, indicating that Ag has been oxidized to Ag_xO. Since the Ag film was capped with 10 nm Pd during evaporation and the sample was moved into the TEM tool immediately after lift-out, we attribute the oxidation of Ag to oxygen out-diffusion from the a-ZTO layer, rather than to reactions with ambient air. Unlike Ag (Φ~4.3 eV), Ag_xO has a high Φ of >5.0 eV [242], [243], which explains the Schottky contact behavior. The high-resolution transmission electron microscopy (HRTEM) image in Figure 6.4 (c) shows the existence of a ~3 nm, non-uniform interfacial layer between Ag and a-ZTO, which may be due to inter-diffusion.
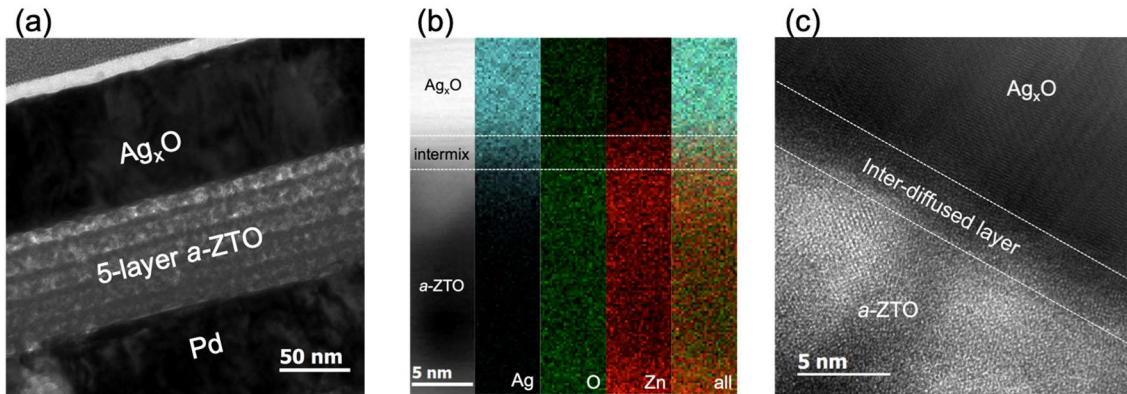
Figure 6.4 Material characterization of top Schottky contact. (a) Cross-sectional bright-field TEM image of a five-layer spin-coated V-TFD. The vertical structure, with a-ZTO in the middle showing a five-layered morphology, with a total a-ZTO thickness of ~110 nm, is observed. (b) Cross-sectional STEM dark-field image (left) and EDS elemental mapping of Ag (cyan), O (green), Zn (red), and all elements (right) obtained near the Ag/a-ZTO junction. The presence of bright green in the Ag region shows co-existence of O and Ag due to Ag oxidation. The location of a ~3 nm thick interfacial layer between Ag and a-ZTO is indicated by white dotted lines. (c) HRTEM images near Ag/a-ZTO junction. The brightness of the interfacial layer and the a-ZTO varies spatially, indicating the possibility of a non-uniform Schottky barrier (Φ_b).

After materials characterization, the charge transport mechanisms across the Schottky contact were analyzed following the same procedure established in Chapter 4. The J-V curves of V-TFD were obtained from 260 K to 340 K, as shown in Figure 6.5 (a). From J-V curves in all temperatures, the values of n and J_s were extracted from low forward bias region of 0.13-0.23 V, using $J = J_s \left\{ \exp\left[\frac{qV}{nkT}\right] - 1 \right\}$, where J_s is the saturation current density, k is Boltzmann's constant, and n is the ideality factor. Next, from extracted J_s, the effective Schottky barrier height (ϕ_{eff}) is calculated using Equation (4.4). If the barrier were homogeneous with no interfacial states, ϕ_{eff} should be temperature-invariant, $n=1$, and the y-axis intercept of the Richardson plot of ln (J_s/T^2) vs. $1000/T$ should retrieve A^*. However, both ϕ_{eff} and n show temperature dependence (Figure 6.5 (b)), and A^* value retrieved is unreasonably small, 9.0×10^{-3} A·cm^{-2}·K^{-2} (Figure 6.5 (c)). As established in Chapter 4, these observations can be explained by the Schottky barrier (ϕ_b): (i) being spatially inhomogeneous and (ii) having a voltage-dependence. Inhomogeneous ϕ_b corresponds to spatially-distributed fluctuations in the conduction band energy level or metal work function, due to non-uniform interface morphology or metallurgy. In addition to the spatial non-uniformity, ϕ_b distribution can be bias-dependent under the presence of interfacial layer [163]. When these two conditions are met, both $n^{-1} - 1$ and ϕ_{eff} become linear with respect to T^{-1} following Equation (4.10) and (4.14). The same tendencies are observed in Figure 6.5 (b). Therefore, charge transport in our Schottky diodes is dominated by thermionic emission over a inhomogeneous barrier with the presence of interfacial states. A linear regression fitting of ϕ_{eff} vs. T^{-1} yields values for $\bar{\phi}_{b0}$ and σ_0. The extracted $\bar{\phi}_{b0}$ and σ_0 show ϕ_b distributed 0.97±0.1 eV at zero forward bias. Previous reports on Schottky junctions made using a variety of materials [151], [174], [177]–[179], have used a modified Richardson plot to extract values of A^*. Based on Equation (4.24), the term $\ln(J_s/T^2) - q^2\sigma_0{}^2/2k^2T^2$ should be linear with respect

to T^{-1} and its linear regression of y-axis intercept should give the value of A^*. Thus, the extracted σ_0 value is used to calculate and plot $\ln(J_s/T^2) - q^2\sigma_0^2/2k^2T^2$ vs. T^{-1}, which is shown in red circles in Figure 6.5 (c). A linear regression on the data from 260 to 340 K extracts values of $A^* = 40.7\text{A·cm}^{-2}\text{·K}^{-2}$ and $\bar{\phi}_{b0} = 0.98$ eV for our V-TFD. These values are close to the A^* value used to extract ϕ_{eff} (40.8 A·cm^{-2}·K^{-2}) and the $\bar{\phi}_{b0}$ value extracted from the ϕ_{eff} vs. T^{-1} plot (0.97 eV). These results imply that ϕ_b in our Ag$_x$O/a-ZTO junction is inhomogeneous.

Inhomogeneous ϕ_b by itself, however, only leads temperature dependence of ϕ_{eff} by Equation (4.10) and therefore, unless diodes need to be used over a wide range of operating temperatures, its effect on device applications may be trivial. In contrast, the bias-dependence of ϕ_b is a critical matter for diode performance, as it affects switching characteristics, quantified by n. While n should be theoretically one, the voltage-induced deformation of ϕ_b, quantified by the coefficients ξ and γ in Equation (4.13), lead n to be higher than one, since $n^{-1} - 1 = -\gamma - q\xi/2kT$. ξ and γ extracted from temperature dependence of n^{-1}-1 are 0.05 and 0.01 respectively. Since $\xi > 0$ and $\gamma > 0$, from Equation (4.13), an applied forward bias (V) will narrow the inhomogeneity distribution and increase the mean Schottky barrier, $\bar{\phi}_b$. This variation is calculated for low forward bias up to +0.3 V, and is shown in Figure 6.5 (d). The origin of this variation can be explained by interfacial layer theory [163]. In the presence of a thin interfacial layer, the potential change across this layer and the occupation of interface states at forward bias can lead to a linear bias dependence of ϕ_b: $\phi_b = \phi_{b0} + \left(1 - \frac{\varepsilon_i\varepsilon_o}{\varepsilon_i\varepsilon_o + q^2 N_{ss}\delta}\right)V$, where ε_i is the relative permittivity of the interfacial layer, δ is its thickness, and N_{ss} is the density of interfacial states distributed within this layer. The lower N_{ss} and δ are, the less bias-dependent ϕ_b becomes. Equation (4.15) can be inserted to Equation (4.3) so that we can extract the energy-level distribution of interfacial states, $N_{ss}(E)$. Its detailed derivation is found in Türüt, *et al.* [163]. As

our cross-sectional EDS mapping and HRTEM images show the presence of 3 nm interfacial

layer as shown in Figure 6.4 (b) and (c), $\delta \approx 3$ nm was used and ε_i equal to ε_s of a-ZTO, extracted

as 13 from C-V measurement, was assumed to derive $N_{ss}(E)$. This is shown in Figure 6.5 (e). The

$N_{ss}(E)$ extracted for the Ag_xO/ZTO junction is compared with that of the Pd:ZTO diode,

characterized in previous chapters and shown in Figure 6.5 (f). As shown, the interface states at

the Ag_xO/ZTO junction are much less than those at the Pd/ZTO junction, indicating the higher

quality of the Ag_xO Schottky contact. Reducing these states can allow an efficient shift of the

quasi Fermi level within AOS and thus allow steep switching of V-TFDs as well as of

MESFETs.
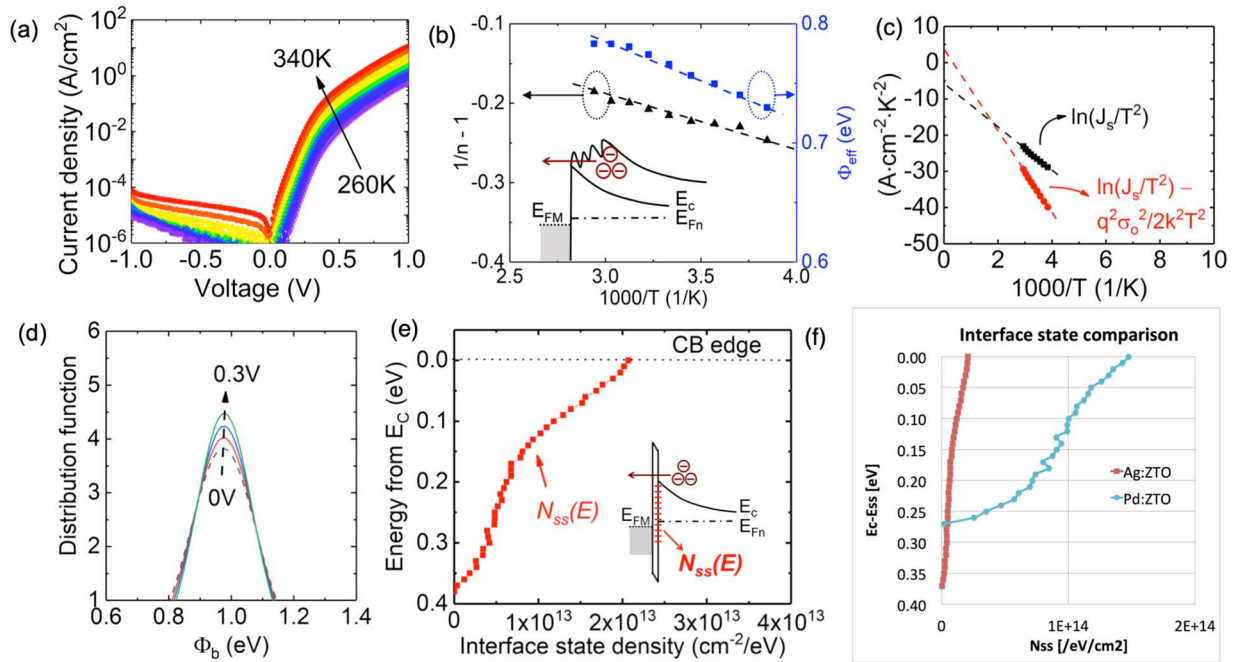
Figure 6.5 Electrical characterization of top Schottky contact (a) Temperature-varying *J-V* curves taken from 260 K to 340 K. The measurements were taken using a Lakeshore Cryotronics TTPX cryogenic probe station and an HP4156A semiconductor parameter analyzer. Temperatures were swept from 260 K to 340 K with a step temperature of 10 K. All measurements were taken at ±1 V in continuous sweep mode with a step voltage of 0.01 V. The measured device is in a crossbar structure and has 30 μm×30 μm size. (b) Ideality factors (*n*) and effective potential barrier (*Φ*ₑ𝒻𝒻) extracted from temperature-varying *I-V* measurements conducted at 260-340 K with 10 K steps. The dashed lines show the linearity of $1/n$-1 and *Φ*ₑ𝒻𝒻 over 1000/*T*, as predicated by the inhomogeneous *Φ_b* model, illustrated in the inset. (c) Standard Richardson plot (black squares) and modified Richardson plot (red circles). Black symbols are obtained from *J-V* curves using Equation (4.4). The dashed lines shows a fit to extracted *A**. The obtained value is unreasonably small. The red symbols are obtained using Equation (4.24), giving reasonable

value of A^*. (d) Distribution of Φ_b, which changes due to forward bias. Here we show the change in Φ_b for applied voltages from 0 V to +0.3 V. These changes indicate the existence of interface states, which causes $n > 1$. (e) Interfacial state density distribution ($N_{ss}(E)$) extracted using interfacial layer theory. In the future, minimizing the density of interface states can enable steeper switching of both the V-TFD and MESFET. (f) $N_{ss}(E)$ of a Ag$_x$O/ZTO junction compared with a Pd/ZTO junction.

6.3.3 Bottom ohmic contact using Pd

Next to characterize the bottom ohmic contact, HRTEM was taken at the Pd/a-ZTO interface. For a good ohmic contact to be formed, a low-Φ metal should be in contact with a-ZTO layer. Figure 6.6 (a) shows the existence of ~7 nm layer between the Pd and a-ZTO, with a crystalline morphology that indicates possible alloy formation at the interface. X-ray photoelectron spectroscopy (XPS) analysis after sputtering reveals that metallic Zn and Sn are observed only at the Pd interface (Figure 6.6 (b)). This suggests the formation of a Pd-Zn-Sn alloy. Metal alloy formation mixes the workfunctions of each metal [244], [245]. Therefore, high-Φ Pd (5.22 eV) mixed with low-Φ Zn (3.63 eV) and Sn (4.42 eV) [141] results in a low-Φ metal with a good ohmic contact with a-ZTO. The alloy formation observed here is attributed to *in situ* process occurring during the 520°C annealing step used for a-ZTO layer formation. To characterize the quality of resulting ohmic contact, we conducted transmission-line measurements (TLM). The measured *I-V* curves are linear and a low specific contact resistance (R_C) of 3.1×10^{-4} Ω·cm^2 is extracted for the Pd/a-ZTO junction, as shown in Figure 6.6 (c).
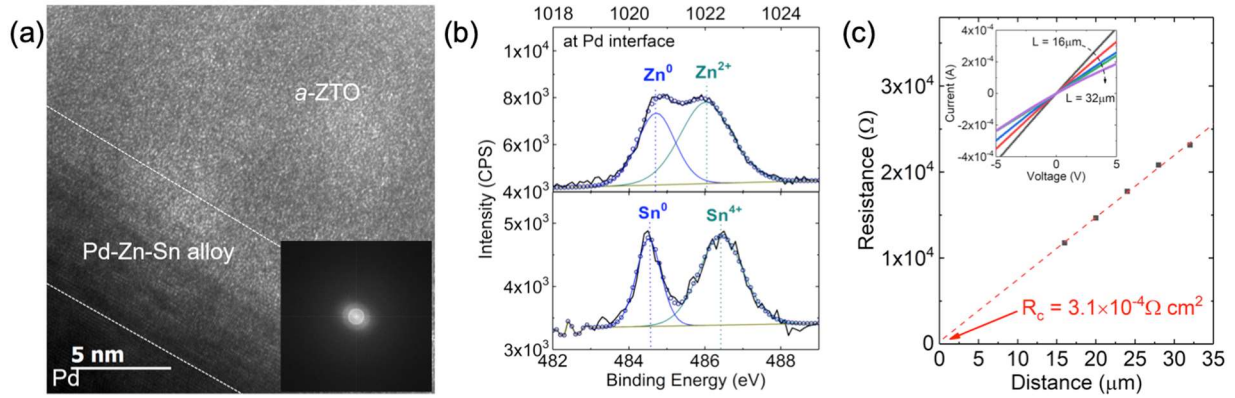
Figure 6.6 Characterization of bottom ohmic contact (a) HRTEM images near the Pd/*a*-ZTO junction. The interfacial layers are marked with white dotted lines. The inset shows fast-Fourier transform patterns taken from the *a*-ZTO region, indicating an amorphous morphology. At the interface there exists a ~7 nm interfacial layer with crystalline morphology, indicative of alloy formation. (b) XPS Zn 2p3/2 and Sn 3d5/2 core level analysis near the Pd/*a*-ZTO junction, obtained by sputtering *a*-ZTO until the Pd 3d peak is observed. In EDS, O peaks overlap with Pd peaks, and thus XPS depth profile was performed to confirm the oxidation states of the metals. Unlike in the bulk of *a*-ZTO, where Zn and Sn exist in their oxidized states (Zn^{2+} and Sn^{4+}, drawn in cyan), near Pd electrode metallic Zn and Sn are observed (Zn^0 and Sn^0, drawn in blue). This confirms that a Pd-Zn-Sn alloy forms at the ohmic contact interface. (c) TLM measurements to extract Pd/*a*-ZTO contact resistance.

6.4 New V-TFD and MESFET fabrication

6.4.1 Top-Schottky V-TFD

Using these top-Schottky and bottom-ohmic contacts, V-TFD and MESFETs were fabricated following the procedures described in Section 6.3.1. The *J-V* curves of the V-TFDs were measured at -1 V to +1 V with 0.01 V step as shown in Figure 6.7 (a). The curves show that on-current density can be as high as >10 A/cm^2, and off-current density as low as ~10^{-7} A/cm^2, resulting in a very high on/off ratio of >10^8 at ±1 V. In the low forward bias region of 0.1-0.3 V, we can extract from our diode *J-V* curves a nearly-ideal *n* that is less than 1.1, and high ϕ_{eff} of ~0.85 V. The same extraction methods were used in other AOS V-TFD literatures [101], [118], [151], [152], [165], [246], and thus these values are tabulated for comparison in Table 6.2. Using this extraction method, 27 V-TFD devices are analyzed, as shown in Figure 6.7 (d)-(f). The devices show good uniformity.

The *C-V* curves of V-TFDs were measured from -2 V to +0.6 V with 0.02 V step, using a 10 mV AC signal at 1 MHz. Complex impedance was fit using the C_p-R_p model. The resulting A^2/C^2 vs. *V* plot is shown in Figure 6.7 (b), where *A* stands for the device area. The diode capacitance changes with respect to applied bias: The minimum constant capacitance in reverse bias corresponds to full depletion, and the large increase in capacitance in the weak forward bias region indicates reduction of the depletion region width. Such bias-dependence of diode capacitance follows Equation (3.4), which allows us to experimentally extract V_{bi}. V_{bi} is also a effective turn-on voltage of the diode when it is used as a rectifier. Linear extrapolation from the 0.2-0.4 V region gives V_{bi} of 0.47-0.49 V. At this voltage, the depletion region width (*w*) should be near zero. On the other hand, a constant minimum capacitance in reverse bias implies full depletion of the film, where *w* is the film thickness, 110 nm, measured by TEM in Figure 6.4 (a). From the equation $C = \varepsilon_s \varepsilon_o \frac{A}{w}$, *w* at full depletion is indeed calculated to be 110 nm by using ε_s of 13, reported similarly for *a*-IGZO [151], [247], [248]. Using this ε_s, the depth profile of N_{depl} is obtained from Equation (3.4), and is shown in Figure 6.7(c).
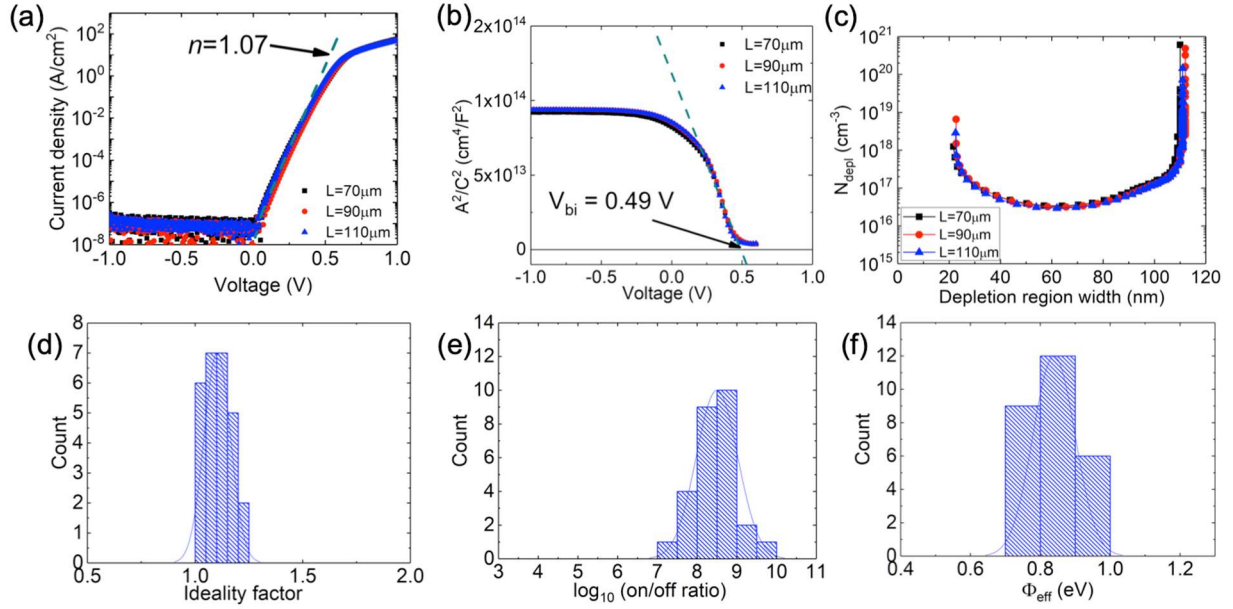
Figure 6.7 Electrical characterization of top-Schottky Ag_xO:ZTO diode. (a) *J-V* characteristics and (b) *C-V* characteristics of V-TFDs with square electrodes. *L* in the legends indicates the length of the square edge. The area-normalized measurements show good agreement between devices of different areas, indicating good uniformity and marginal edge/surface effects. The dashed line in (a) is to the 0.1-0.3 V region using Equation (4.1), used to extract *n*. The dashed line in (b) is linear regression from the 0.2-0.4 V region using Equation (3.4), used to extract V_{bi}. (c) Depletion concentration (N_{depl}) depth profile obtained from (b). Our *a*-ZTO film shows an N_{depl} of 3×10^{16} to 1×10^{18} cm^{-3}, similar to reports of other AOS V-TFDs. (d) *n*, (e) on/off ratio, and (f) Φ_{eff} extracted from *J-V* measurements from 27 V-TFDs. The tested devices have various structures (8 cross-bar structures, 14 circular devices, and 5 square devices) and sizes (squares of 30×30 μm^2 to 110×110 μm^2, or circles with 30 μm to 200 μm diameters). The extracted device parameters have narrow distributions in (d)-(f).

Table 6.2 A brief summary of the properties of AOS V-TFDs									
AOS	Schottky metal	Sol	Vertical	*n*	on/off	Φ_{eff}	*t* (nm)	year	Ref.
a-ZTO	Pt	N	N	1.05	2.7×10^7	1.25	600-700	2017	[246]
a-ZTO	PtO$_x$	N	N	1.6	5.5×10^5	0.9	300	2017	[212]
a-ZTO	PdO$_x$	Y	Y	1.9	5×10^2	0.72	130	2017	[101], [165]
a-ZTO	MoO$_x$	Y	Y	>3	1×10^3	0.34	190	2018	[146]
a-IGZO	Pt	N	Y	2.1	>10^3	0.51	100	2015	[107]
a-IGZO	Au	N	Y	1.29	>10^4	0.82	500	2017	[249]
a-IGZO	Pt	N	Y	1.04	>10^8	1.2	50	2011	[151]
a-IGZO	RuSiO	N	N	2.13	8.4×10^5	0.79	30	2018	[250]
a-IGZO	PdO$_x$	N	Y	1.51	>10^7	0.79	280	2012	[118]
a-IGZO	PdO$_x$	N	Y	1.22	7.3×10^6	0.79	100	2018	[251]
a-IGZO	PtO$_x$	N	Y	1.36	2.4×10^6	0.92	50	2016	[152]
a-ZTO	**Ag$_x$O**	**Y**	**Y**	**<1.1**	**>10^8**	**0.85**	**110**	**This work**	

Sol: Whether AOS material was deposited using solution process; Vertical: Whether fabricated thin-film diode has vertical sandwiched structure; *n*: Ideality factor; Φ_{eff}: Effective potential barrier extracted from *I-V* measurements; *t*: AOS film thickness.

6.4.2 Schottky-gated MESFET

Using the same contacts as the V-TFD, MESFETs were fabricated. In order to show the benefits of MESFETs over MISFETs, which we characterized in Chapter 2, MISFETs were also fabricated using an identical five-layer solution process. Then, MISFET and MESFET of the same device dimensions were compared. The microscope images, transfer curves, and output curves of both TFTs are shown in Figure 6.8 (a)-(f). The evaluation of MISFET performance was done as described in Chapter 2, using Equation (2.3). At $V_{DS} << V_{GS}$ (i.e., in linear region), Equation (2.3) reduces to

$$I_{DS} \approx \frac{W}{L}\mu_{lin}C_{ox}\left[(V_{GS} - V_{T,lin})V_{DS}\right].$$ (6.1)

Here, μ_{lin} refers to linear mobility and can be calculated according to $\mu_{lin}=(\partial I_{DS}/\partial V_{GS})(L/WC_{OX}V_{DS})$ [58], [76]. Thus, from the transfer curves of five-layer MISFET taken at V_{DS}=0.1 V in Figure 6.8 (b), μ_{lin} and $V_{T,lin}$ are extracted at high V_{GS} of 4-10 V using Equation (6.1). This leads to μ_{lin}=5.2 cm^{2}V^{-1}s^{-1} and $V_{T,lin}$=0.29 V extracted for the MISFET.

The field-effect mobility (μ_{FE}) and V_T for our MESFET should be extracted for comparison with our MISFET and with other published MESFETs. Due to the different device operation of the MESFET and MISFET, Equation (6.1) cannot be used for the MESFET. In the linear regime when V_{DS} is low and when $V_{GS} \approx V_{bi} - V_p$, I_{DS} of a MESFET obeys [252]:

$$I_{DS} \approx \frac{q\mu_{FE}tN_{free}W}{2V_pL}(V_{GS} - V_{bi} + V_p)V_{DS},$$ (6.2)

where V_{bi} is the built-in potential, V_P is the pinch-off voltage, N_{free} is the free carrier concentration, and t is the channel thickness. Under the Schottky gate, the channel becomes fully depleted at the drain edge at a certain V_{GS} value, which is referred to as the pinch-off voltage and

defined as $V_p = q\,N_{depl}t^2/2\varepsilon_s\varepsilon_o$, where ε_s is the relative permittivity of the active channel layer. From our V-TFD analysis, explained in Section 6.4.1, we know that N_{depl}=2×10^{17} cm^{-3}, V_{bi}=0.49 V, and ε_s=13. The value of V_p is thus calculated to be 1.68 V. The V_T of the MESFET is V_{bi}–V_p, or -1.19 V. To apply Equation (6.2) and extract μ_{FE}, we use the output characteristic taken at V_{GS}=-1.0 V, where the condition of Equation (6.2), $V_{GS}{\approx}V_{bi}$–V_p, holds. From the linear region where V_{DS} is low, Equation (6.2) holds and the mobility can be calculated using $\mu_{FE}{\approx}(\partial I_{DS}/\partial V_{DS})2V_P/\{(V_{GS}\text{-}V_{bi}+V_p)(qtN_{free}(W/L))\}$. $(\partial I_{DS}/\partial V_{DS})$ is the output conductance in linear region, g_{D0}, extracted as 4.29×10^{-6} S. Lastly to calculate μ_{FE}, N_{free} is taken from our Hall measurement [58], 4.6×10^{16} cm^{-3}. This leads to μ_{FE}=4.5 cm^{2}V^{-1}s^{-1}.

It is important to note here that mobilities extracted from both MISFET (μ_{lin}=5.2 cm^{2}V^{-1}s^{-1}) and MESFET (μ_{FE}=4.5 cm^{2}V^{-1}s^{-1}) here are similar to Hall mobility obtained (μ_{Hall}=5.5 cm^{2}V^{-1}s^{-1}) from our five-layer a-ZTO [58]. Such good agreement of a-ZTO mobility extracted from different structures indicates that non-ideal metal contacts and carrier scattering at the interfaces play a marginal role in our devices. In addition, both our MESFET and MISFET have low leakage current, thanks to a high-quality Schottky gate and gate-dielectric, respectively. These features make possible some general comparisons between the MISFET vs. MESFET in Section 6.5.1.
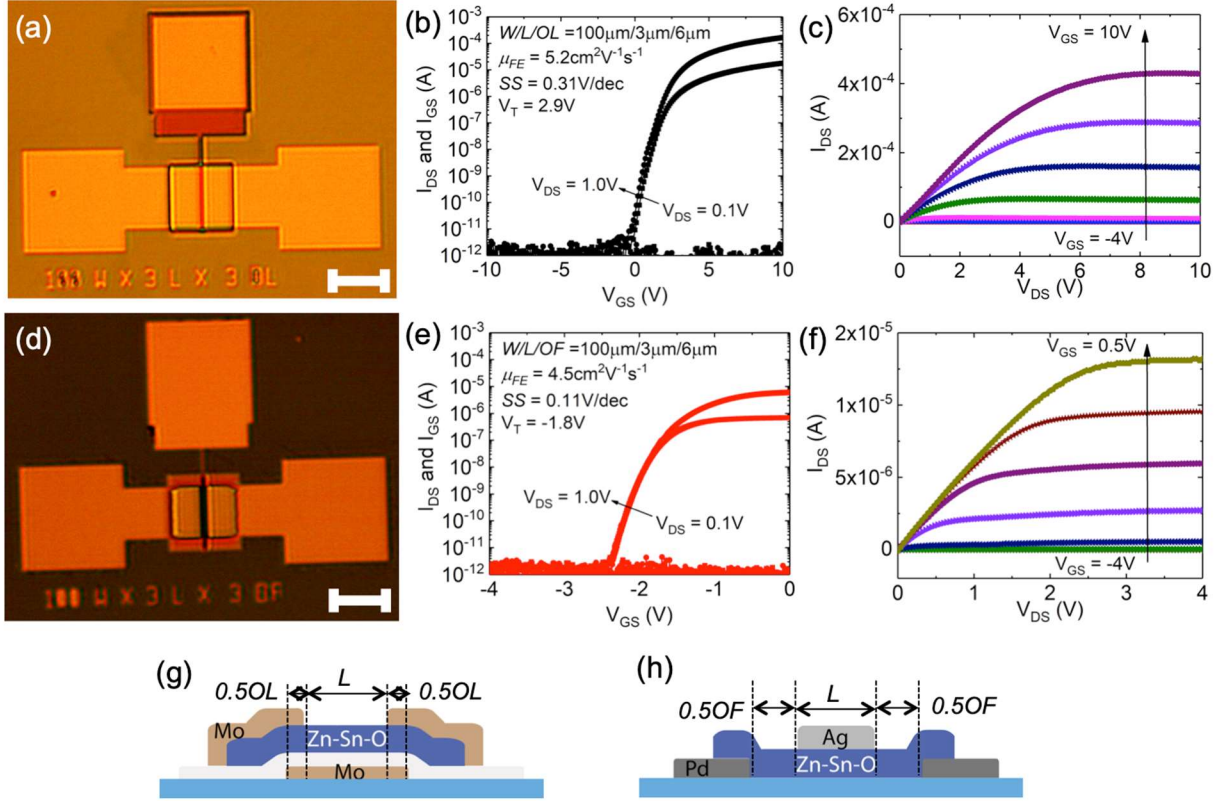
Figure 6.8 AOS MISFET and MESFET Measurements. Microscope images, transfer curves, and output curves of *a*-ZTO MISFET ((a)-(c)) and *a*-ZTO MESFET ((d)-(f)). The cross-sectional structures of each device are illustrated in (g) for MISFET and (h) for MESFET. The MISFET shown here have channel width (W) of 100 μm, length (L) of 3 μm and G-D, G-S overlap length (OL) of 6 μm. The MESFET here have channel width (W) of 100 μm, length (L) of 3 μm and G-D, G-S offset length (OF) of 6 μm. Therefore, the active device area is identical for both TFTs compared here. The electrical measurements shown in (b), (c), (e), and (f) were all taken with medium integration time for quasi-static *I-V* measurements. The scale bars in (a) and (d) represent 100 μm.

Using this approach, AOS MESFETs are obtained using high-quality top-Schottky contacts. While Schottky-gated MESFETs intrinsically have a negative V_T, they have several advantages over MISFETs due to the absence of a gate dielectric and its interfaces, a lower *SS*, lack of hysteresis and instability issues [117], faster switching speed, and a simpler fabrication process [175]. Thanks to these advantages, AOS MESFETs fabricated by vacuum deposition or atmospheric CVD process have been studied and reported [117], [253]. Here, we report the first spin-coated AOS MESFET that is suitable for monolithic 3D integration. The devices show

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excellent switching performance comparable to the best AOS MESFETs reported so far. The device parameters obtained here are compared with those from literature in Table 6.3.

Table 6.3 A brief summary of the properties of AOS MESFETs											
AOS	Metal	Sol	on/off	I_{on} (μA/μm)	SS (V/dec)	V_{on}	V_T	μ_{eff} (cm^{2}V^{-1}s^{-1})	t (nm)	year	Ref.
a-IGZO	Pt	N	>1×10^6	3.3×10^{-3} (V$_{DS}$=3V)	0.13	-7.1	-	0.5 (V$_{GS}$=0V)	230	2012	[254]
a-IGZO	Ag$_x$O	Y[a]	3.8×10^7	3.1×10^{-1} (V$_{DS}$=3V)	0.35	-6.0[b]	-	3.2 (V$_{DS}$=3V)	95	2015	[255]
a-IGZO	RuSiO	N	>1×10^3	>2.5×10^{-2} (V$_{DS}$=2V)	0.42	-	-0.52	8.8 (V$_{DS}$=2V)	30	2015	[256]
a-ZTO	PtO$_x$	N	1.8×10^6	5.7×10^{-2} (V$_{DS}$=2V)	0.12	0.0[b]	0.47	0.9 (V$_{DS}$=2V)	24	2018	[253]
a-ZTO	Ag$_x$O	Y[a]	8×10^6	>3.8×10^{-1} (V$_{DS}$=2V)	0.18	-2.5[b]	-1.73	12 (V$_{DS}$=3V)	22	2017	[117]
a-ZTO	**Ag$_x$O**	**Y**	**>1×10^6**	**6.0×10^{-2} (V$_{DS}$=1V)**	**0.11**	**-2.3**	**-1.6**	**4.5 (V$_{GS}$=0V)**	**110**	**This work**	

When more than one MESFET are reported in a literature, the one with the best on/off ratio is listed.
Metal: Metals used to obtain rectifying Schottky contact; I_{on}: On-current normalized by channel width; V_{on}: Turn-on voltage, a minimum V_{GS} when I_{DS} is larger than leakage current; μ_{eff}: Mobility extracted from TFT measurements. V_{GS} is listed when output characteristics were used, and V_{DS} is listed when transfer characteristics were used; t: AOS film thickness.
[a] Solution was dispensed by Mist-CVD, not spin-coating; [b] Values estimated from the figures.

6.5 3D monolithic integration of AOS PMIC for More-than-Moore

6.5.1 The application of MESFET for I/O bridging

The main motivation for MESFET fabrication is to realize a TFT with low V_{switch} and negative V_T in order to supplement the MISFET. For comparison of these two TFTs along with the Si finFET, their transfer characteristics taken at V_{DS}=0.1 V were used to extract the following parameters. To compare on-current (I_{on}), I_{DS} at V_T was determined and normalized by the channel width. The turn-on voltage (V_{on}) is defined as the minimum V_{GS} where I_{DS} is larger than leakage current [235], and the switching voltage (V_{switch}) is defined as the difference between V_T and V_{on}. From the same curves, the subthreshold swing (SS) is calculated as the minimum value of $\partial V_{GS}/\partial log_{10} I_{DS}$ in the subthreshold region [58], [76]. Figure 6.9 (a) shows that our MISFET has a

SS of 310 mV/dec and a positive V_T and V_{switch} of 2.9 V, which exceeds the operation voltage of Si finFETs. In comparison, thanks to a smaller *SS* of 110 mV/dec, the MESFET has a lower V_{switch} of 1.1 V, within the operating voltage range of LV Si CMOS. Therefore, AOS MESFET fabricated on top of a LV Si MCU can operate together with the LV Si CMOS IC. Due to the high carrier mobility of silicon and the high aspect ratio of the finFET structure, the Si NMOSFET has high current capability. However, due to scaling, it can only endure a low BV. This weakness can be compensated by monolithic integration of AOS TFTs. Therefore, the voltage handling capability of these three FETs were tested. Both MESFET and MISFET show blocking voltages (*BV)* greater than 40 V, much higher than the *BV* of the Si finFET (Figure 6.9 (b)). The low V_{switch} and high *BV* of our MESFET enable HV AOS TFTs to interface with LV Si CMOS ICs. The device parameters extracted from Figure 6.9 (a) and (b) are summarized in Figure 6.9 (e). The low V_{switch} and high *BV* of the MESFET enable HV AOS TFTs to bridge the LV signal from MCU with HV external components.
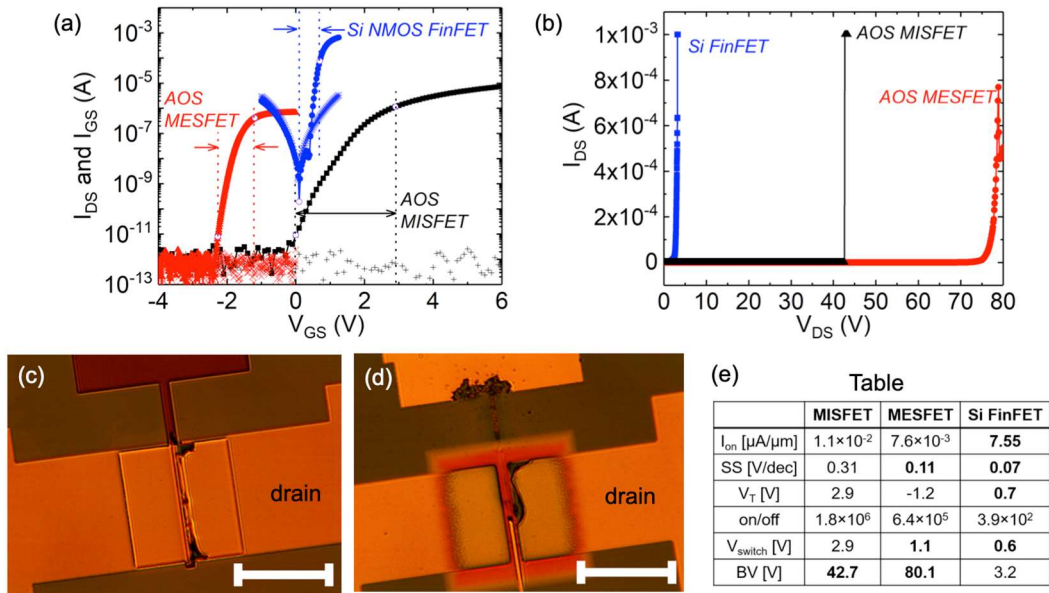
Figure 6.9 AOS MISFET and MESFET Measurements. (a) Typical measured transfer curves showing both I_{DS} and I_{GS} and (b) typical breakdown of solution-processed AOS MESFET, MISFET, and Si NMOS finFET. The

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MESFET and MISFET both have W/L=100 μm/3 μm, while the Si finFET has W/L=10 μm/ 150 nm. In (a) all transistors were tested at V_{DS}=0.1 V. The gaps between the dotted vertical lines show the V_{switch} of each device, which is defined as the gap between the turn-on voltage and V_T. In (b) the MESFET and MISFET were measured at V_{GS} = -4 V and the Si finFET at V_{GS} = 0 V, to turn off the devices. Then V_{DS} was increased until device breakdown occurred. Both MESFET and MISFET exhibit HV operation (>40 V) compared to Si finFET (~3 V). The microscope images of (c) MISFET and (d) MESFET were taken after the breakdown measurements in (b) The scale bars represent 100 μm. (e) Device parameters extracted from (a) and (b) for comparison.

Therefore, using a MESFET structure, we report a new AOS TFT with a low V_{switch} that can be formed via an identical ZTO spin-coating method as the MISFET. For AOS MISFETs, a high-quality gate dielectric with certain thickness should be deposited in order to obtain low gate leakage, which in turn causes high SS and stress instability issues [175]. These issues may be problematic for integration with 100nm-node Si CMOS. As observed by others [117], [175], [253], [256], the MESFET provides many advantages, especially low SS [253] and high stability [117], compared to the MISFET due to the absence of an insulator. As shown in Figure 6.9 (c), our MESFET also exhibits an SS value much lower than that of the MISFET. Furthermore, the SS value of the MESFET may be lowered even further, for example by reducing interfacial trap states at Schottky contact [257], extracted in Figure 6.5 (e). We note here that unlike the MESFET, the AOS MISFET has been studied much more extensively, particularly regarding the optimization of the gate dielectric to reduce SS (and thus V_{switch}). Nonetheless, the attempts made so far to reduce SS of MISFET often exhibit low on/off ratio, probably due to the higher leakage current through thin gate dielectric. Using solution-processed a-ZTO, the MISFETs reported so far are summarized in Table 6.4. In Table 6.4, the results that show SS comparable to our MESFET, 0.11 V/dec, are highlighted in bold text, which also show low on/off ratio. Our results indicate that the MESFET structure may provide a better opportunity to obtain low SS and low V_{switch}.

AOS	Gate Ins.	Sol	SS (V/dec)	μ_{eff} ($cm^2V^{-1}s^{-1}$)	On/off	V_T	year	Ref.
a-ZTO	SiO$_2$	Y	-	1.1	10^6	0.9	2008	[258]
a-ZTO	SiO$_2$	Y	0.77	17.02	1.88×10^6	5.01	2013	[259]
a-MgZTO	SiO$_2$	Y	1.5	0.27	3.3×10^6	5.4	2014	[260]
a-HfZTO	SiO$_2$	Y	0.44	0.115	7.9×10^5	-1.2	2012	[261]
a-ZTO (3nm)	SiO$_2$	Y	~0.4	8	~10^7	~0	2014	[262]
a-ZTO (7nm)	SiO$_2$	Y	0.54	1.99	2.36×10^8	5.4	2013	[263]
a-ZTO	SiO$_2$	Y	0.27	5.6	2×10^8	3.3	2013	[264]
a-ZTO	SiO$_2$	Y	0.25	7.8	10^8	0.11	2013	[265]
a-ZTO/ a-IGZO	SiO$_2$	Y	0.49	2.09	~10^6	2.72	2013	[266]
a-ZTO	Si$_3$N$_4$	Y	~0.25	7.7	~10^7	-	2013	[267]
a-IZTO	AlO$_x$	Y	0.16	114.8	>10^6	-0.16	2014	[33]
a-ZTO	SiO$_2$	Y	0.4	4.3	4.1×10^7	0.0	2014	[268]
a-GaN: ZTO	SiO$_2$	Y	0.35	4.84	~10^7	0.04	2014	[269]
a-ZTO	SiO$_2$	Y	0.9	17	>10^7	-1.5	2012	[270]
a-ZTO	AlO$_x$	Y	0.25	2.6	~10^4	0.36	2015	[271]
a-ZTO	AlO$_x$	Y	**0.096**	33	**~10^5**	1.2	2011	[272]
a-ZTO	HFO$_x$/ AlO$_x$	Y	**0.117**	3.84	**~10^5**	0.84	2012	[273]
a-IZTO	SiO$_2$	Y	0.2	90	10^5	<2	2010	[274]
a-ZTO	SiO$_2$	Y	1	>6	>10^6	-5	2014	[59]
a-ZTO	ZrO$_2$	Y	0.122	16.2	10^7	5	2010	[275]
a-ZTO	-	Y	0.22	0.42	10^7	1.1	2012	[276]
a-ZTO	ZrO$_2$	Y	**0.074**	4	**~10^6**	2	2012	[277]
a-ZTO	HfO$_x$	Y	**0.07**	13.2	**<10^6**	2	2017	[236]
a-ZTO	SiO$_2$	Y	0.31	13.6	~10^8	3	2013	[278]
a-YZTO	AlO$_x$ / Parylene	Y	35	0.8	10^3		2018	[279]
a-IZTO	ZrO$_2$	Y	0.133	2.6	10^8	-0.6	2016	[280]
a-ZTO	SiO$_2$	Y	0.2-0.5	2.3-4.2	10^{6-7}	-1.6-0.2	2017	[55]
a-IZTO	ZrO$_2$	Y	0.114	4.75	10^9	0	2016	[281]
a-ZTO	SiO$_2$	Y	0.35	7.76	10^8	7	2016	[282]
a-ZTO	SiO$_2$	Y	0.33	66.7	2×10^7	1.2	2016	[283]
a-ZTO	Al$_2$O$_3$	Y	0.31	5.2	1.8×10^6	2.9	Our work	

Table 6.4 A brief summary of solution-processed a-ZTO MISFETs reported so far

In order to build a HV IC with logic components for I/O bridging applications, HV TFT inverters with a narrow transition width (V_{tran}) would be required. Prior to demonstrating the advantages of logic inverter made by combining a negative-V_T MESFET and positive-V_T MISFET, we first show TFT inverters made with other configurations. Their voltage transfer characteristics (VTC) are shown here in Figure 6.10. In all configurations, V_{DD} has been modulated from 1 V to 5 V. To the authors' knowledge, the only inverters tested with solution-processed AOS TFTs have used external resistors for a load [236], [279]. Thus, we first

measured our MISFET, shown in Figure 6.10 (a), in a resistor-loaded inverter configuration. This configuration is illustrated in Figure 6.10 (b). Here, the high impedance of the load is helpful for obtaining a sharp VTC. Using a 1 MΩ external resistor, we obtained a sharp VTC as shown in Figure 6.10 (c). The gain of the VTC is calculated by $\partial V_{out}/\partial V_{in}$, and its absolute value is plotted in Figure 6.10 (d). Due to the external resistor load, a high gain of 10.0 V/V is achieved at 5 V V_{DD}. Despite the high gain compared with other resistor-loaded inverters [236], a ~MΩ-range resistor is not feasible for on-chip integration. For practical applications, a load-TFT should replace this resistor.

Next, we tested an inverter made out of MESFETs-only, shown in Figure 6.10 (e). Good VTC curves are observed as shown in Figure 6.10 (g). However, due to the negative V_T of drive-MESFET, this inverter operates at negative V_{in}, which would require additional level shifter for each inverter for use in circuit applications [175], [239]. This adds unaffordable circuit complexity and consumes layout area.
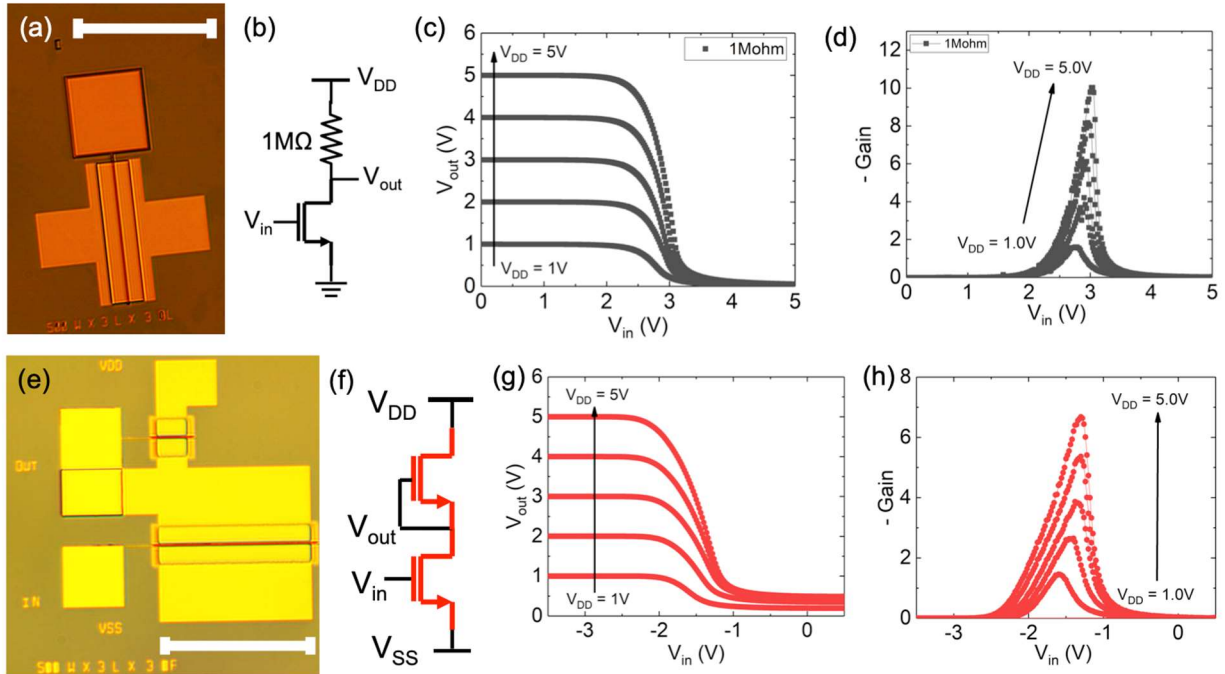
Figure 6.10 AOS inverters made with external resistor and MESFET-only (a) Microscope image (left) of the drive-TFT (*W/L/OL*=500 μm/3 μm/6 μm) tested here. The scale bar length is 500 μm. (b) Circuit diagram of the drive-TFT in the resistor-loaded inverter configuration. The obtained VTC curves and gain curves for this inverter are shown in (c) and (d), respectively. Despite the sharp VTC and high gain, a 1 MΩ load would be difficult to integrate on chip. (e) Microscope image and (f) circuit schematic (right) of an inverter made only with MESFETs. For comparison, both the drive-TFT (*W/L/OF*=500 μm/3 μm/6 μm) and load-TFT (*W/L/OF*=100 μm/3 μm/6 μm) have the device dimension ratio, i.e., *β*=5. (g) The obtained voltage-transfer characteristics and (h) voltage gain at various V_{DD} from 1 V to 5 V. Although a large output swing is obtained for these inverters, the voltage at which the inverter switches is negative, ~-1.5 V. Inverter operation at negative voltages requires integration of additional level shifter circuitry, which consumes additional chip area [175], [239]. In (a) and (e), the scale bar shows 500 μm.

Due to these reasons, the drive-TFT in an AOS inverter should be a positive-V_T MISFET, while its load should also be a TFT (load-TFT) for practical on-chip fabrication. For I/O bridging applications, a negative-V_T MESFET can be combined with a positive-V_T MISFET to form a high performance logic inverter. When a normally-on MESFET is used as a load-TFT with its gate and source shorted, it acts as a current source, allowing a rapid and large change in output voltage, V_{out}, as the input voltage, V_{in}, changes. To compare the performance of MESFET versus MISFET load transistors, two inverters were made, one with a MISFET and one with a MESFET used as the load-TFT (both devices having the same size), connected to a MISFET drive-TFT (Figure 6.11 (a)). As shown in Figure 6.11 (b) and (c), the MESFET-loaded inverter shows much

sharper V_{out} transition compared to MISFET-loaded case. For comparison of the different inverters, the noise margins were analyzed. The input high (V_{IH}) and low (V_{IL}) voltages and the output high (V_{OH}) and low voltages (V_{OL}) are extracted from the VTC curves at the points where $|\partial V_{out}/\partial V_{in}|$=1. The corresponding high noise margin (NM_H=V_{OH}–V_{IH}) and low noise margin (NM_L=V_{IL}−V_{OL}) are then calculated. From these values, a total noise margin is calculated as (NM_H+NM_L)/V_{DD}. The transition voltage (V_{tran}) is defined as V_{IH}−V_{IL}. The swing of an inverter is the difference of the maximum and minimum V_{out}. For optimal logic circuit performance, high noise margins, low V_{tran}, and large V_{out} swing are desirable. The parameter values extracted at 5 V of V_{DD} are listed in Table 6.5 for comparison. The MESFET-loaded inverter shows much sharper V_{out} transition, leading to higher voltage gain (-12.1 V/V at 5 V V_{DD}) and lower transition voltage (V_{tran} of 0.96 V) compared to MISFET-loaded case (V_{tran} of 1.90 V and gain of -1.8 V/V). The key result here is that our HV inverter not only can operate at V_{DD} of 5 V for HV applications, but also can be switched at low V_{tran} of 0.96 V, within Si MCU operation voltage (< 1.2 V). In order to demonstrate the utility of the MESFET-loaded inverter, it was tested with a square wave input. A ΔV_{out} of 4.5 V can be generated with low ΔV_{in} of 1.2 V (Figure 6.11 (d)). As a result, HV AOS 3D-IC on LV Si CMOS IC can effectively convert LV signals from Si ICs into HV signals for external HV loads, as illustrated in Figure 6.11 (e). This unique capability is due to the improved performance of AOS inverters that use a MESFET load-TFT, compared to MISFET-only circuits. The excellent performance of our inverter is compared with other results in Table 6.6.
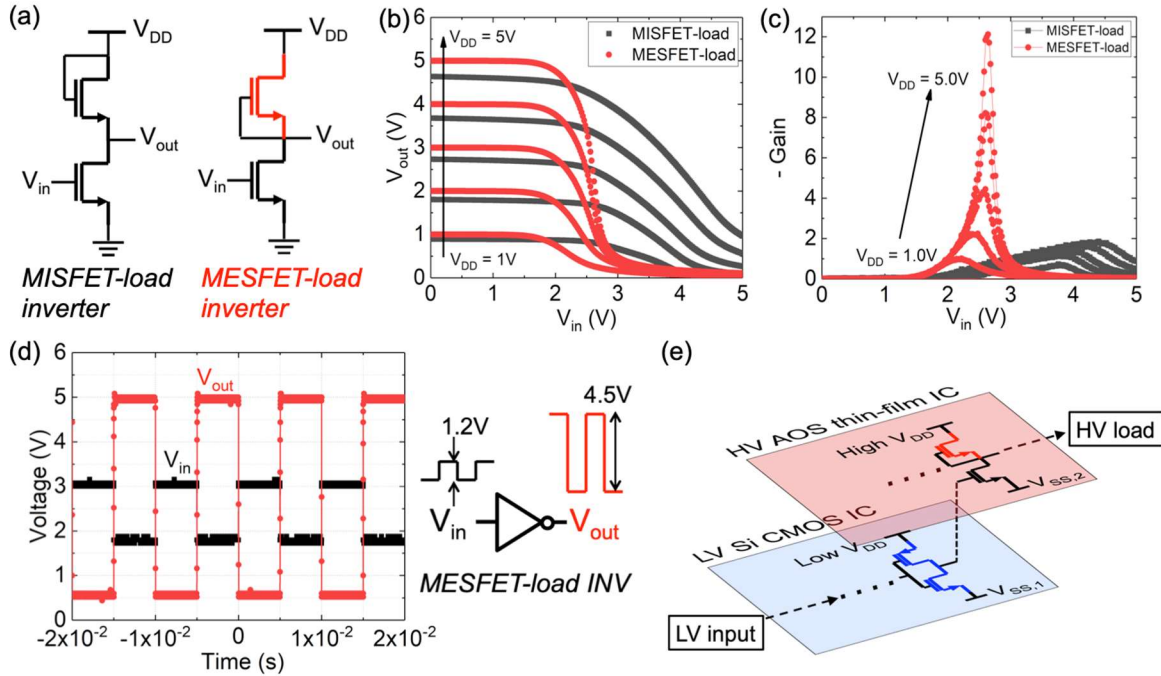
Figure 6.11 AOS inverters made with MISFET and MESFET. (a) Circuit diagrams of inverters tested. In both cases, the bottom transistor is a drive-TFT, using 500 μm/3 μm MISFET, and the top transistor is a load-TFT, where either 100 μm/3 μm MISFET (left) or MESFET (right) is used. Thus in both cases, the aspect ratio is β=5. (b) Their voltage transfer characteristics (VTC) and (c) gain curves, where both were tested at V_{DD} from 1 to 5 V. MESFET-loaded inverter result is marked with red circles and MISFET counterpart is marked with black squares. Sharper VTC with higher gain is observed for MESFET case. (d) The MESFET-loaded inverter test result with a 100 Hz square wave input with ΔV_{in}=1.2 V. A ΔV_{out} of 4.5 V is obtained when V_{DD} is 5 V. (e) A conceptual diagram of future HV AOS circuits using MESFET-loaded inverters, monolithically integrated on LV Si CMOS IC for I/O bridging to a HV load.

Table 6.5 A brief summary of various loads for AOS inverter tested here								
Load	NM$_H$	NM$_L$	NM$_{tot}$ (%)	V$_{out}$ swing (V)	Swing (%)	V$_{tran}$ (V)	|gain| (V/V)	P$_{max}$ (μW)
1MΩ, external resistor	1.58	2.84	68.4	4.93	99	0.96	10.0	25.5
MISFET, G-D shorted	-1.09	2.00	18.1	3.78	75	1.90	1.84	245.6
MESFET, G-S shorted	1.70	1.58	65.5	4.89	97	0.96	12.1	86.9

For all configurations, the same MISFET with $W/L/OL$=500 μm/3 μm/6 μm shown in Figure 6.10 (a) was used for drive-TFT. The results obtained at V_{DD}=5 V are compared. To analyze the noise margin characteristic of the inverter, the input high (V_{IH}) and low (V_{IL}) voltages and the output high (V_{OH}) and low voltages (V_{OL}) are extracted from VTC curve where $|\partial V_{out}/\partial V_{in}|$=1.
NM_H=V_{OH}−V_{IH}; NM_L=V_{IL}−V_{OL}; NM_{tot}=$(NM_H+NM_L)/V_{DD}$; V_{tran}=V_{IH}−V_{IL}; $|gain|$=$|\partial V_{out}/\partial V_{in}|_{max}$; P_{max}=$|V_{DD}\times I_{DD}|_{max}$.

Table 6.6 A brief summary of the properties of AOS NMOS inverters reported so far										
AOS	Sol	Drive	Load	D-mode	β	V$_{DD}$	V$_{tran}$	|gain|	year	Ref.
a-ZTO	Y	E-mode MISFET	2MΩ	-	-	2.5	0.28	11	2017	[236]
a-YZTO	Y	MISFET	100MΩ	-	-	500	~40[a)]	19	2018	[279]
a-IGZO	N	E-mode MISFET	10MΩ	-	-	10	3.5	3.2	2018	[284]
a-IGZO	N	E-mode MISFET	Un-gated channel	-	-	5	~1.2[a)]	5	2014	[285]

a-ZTO	N	E-mode MISFET	E-mode MISFET	-	10	20	~6[a]	2.5	2008	[286]
a-IGZO	N	E-mode MISFET	E-mode MISFET	-	5	18	~7[a]	1.7	2007	[287]
a-IGZO	N	E-mode MISFET	E-mode MISFET	-	20	20	2.2	18.4	2012	[288]
a-ZTO	N	E-mode MISFET	E-mode MISFET	-	3	5	~1.5[a]	~3[a]	2018	[289]
a-ZTO	N	E-mode MISFET	D-mode MISFET	Bi-layer ZTO	2	10	1.87	10.6	2009	[290]
a-SZTO	N	E-mode MISFET	D-mode MISFET	Si doping	-	15	2.7	14.2	2017	[291]
a-IGZO	N	E-mode MISFET	D-mode MISFET	Double-gate	30	10	~1.7[a]	4.18	2011	[292]
a-IGZO	N	E-mode MISFET	D-mode MISFET	Light induced	9	10	1.9	16.9	2012	[293]
a-IGZO	N	E-mode MISFET	D-mode MISFET	Light induced	1	2	<0.1[a]	220	2016	[294]
a-IGZO	N	E-mode MISFET	D-mode MISFET	SIZO MISFET	1	5	~1.2[a]	2.3	2012	[295]
a-IGZO	N	E-mode MISFET	D-mode MISFET	SnO$_x$ capping layer	1	5	~1.9[a]	5.9	2016	[296]
a-IGZO	N	E-mode MISFET	D-mode MISFET	Laser-annealing	5	20	~3.0[a]	20.5	2014	[297]
a-IGZO	N	E-mode MISFET	D-mode MISFET	Bi-layer IGZO	21	1	0.12	24	2016	[298]
a-ZTO	**Y**	**E-mode MISFET**	**D-mode MESFET**	**MESFET**	**5**	**5**	**0.96**	**12.1**	**This work**	

Sol: Whether AOS material was deposited using solution process; Drive/Load: Structures of drive-TFT and load(-TFT) used; D-mode: When a negative-V_T TFT (D-mode) is used for load, the method of obtaining negative V_T is listed; β: the ratio between the geometry of drive-TFT and load-TFT, $β=(W_{drive}/L_{drive})/(W_{load}/L_{load})$; V_{DD}: Operation voltage of an inverter. The values closest to 5 V were listed for comparison with our work.

[a] Values estimated from the figures.

6.5.2 The application of V-TFD for AC-DC conversion and ESD protection

In addition to TFTs for I/O bridging, a HV thin-film rectifier can provide new functionality to LV Si MCU, such as wireless energy harvesting [107], [146] and ESD protection [231], [238]. The same electrodes used for the AOS MESFET can be used to make a vertical thin-film diode (V-TFD), as shown in Figure 6.1 (b). Thus, rectifiers can be fabricated simultaneously with MESFETs. As a rectifier, V-TFDs offer superior performance over TFTs because their vertical current flow through a thin active layer allows a lower turn-on voltage and higher on-current [20], as explained for the Mo V-TFD in Section 5.3.3. For the Ag V-TFD characterized in this chapter, its fundamental strength in high on-current, compared to the G-D

shorted MISFET, stems from the following two reasons. First, based on Equation (4.1), the diode on-current shows exponential dependence on voltage. This sharp increase of on-current is in contrast with the G-D shorted MISFET rectifier, which follows $I_{DS,sat} = \frac{W}{2L}\mu_{FE}C_{ox}(V_{GS} - V_T)^2$, a square-law. Second, the turn-on voltage of the Ag V-TFD is smaller, V_{bi}=0.49 V (Figure 6.7 (b)), than that of MISFET, V_T=2.9 V (Figure 6.8 (b)). To demonstrate these strengths, we compare the switching performance of V-TFDs with MISFETs connected in a diode configuration, i.e. with the gate and drain (G-D) shorted. Typical *I-V* measurements are shown in Figure 6.12 (a). The V-TFD shows much lower leakage (~pA at -1 V) with much higher on-current (~mA at +1 V), compared to the MISFET. This comparison confirms the improved switching characteristics of V-TFDs for LV operation.

In AC-DC conversion, a low switching voltage in a rectifier allows for efficient power conversion, i.e. a high DC output voltage (V_{out}) can be obtained for a given AC input voltage (V_{in}). For monolithic 3D integration of power circuitry, in addition to handling LV switching, the rectifier should be suitable for HV applications such as wireless energy harvesting [107], [146]. This requires stable operation throughout wide range of V_{in}. To test V_{out} vs. V_{in}, both MISFET and V-TFD rectifiers were measured in a half-wave rectifier (HWR) configuration to compare their AC-DC rectification behavior (Figure 6.12 (b)). We note that both rectifiers show uniform frequency responses from 1 kHz to 1 MHz (Figure 6.12 (d) and (e)). As shown in Figure 6.12 (c), the V-TFD has higher V_{out} than MISFET, and a high V_{out} is obtained for a wide range of V_{in}. Specifically, the V-TFD can rectify AC V_{in} of ±5 V, greatly exceeding the LV Si CMOS voltage limit, and can supply a high DC V_{out}, ~2.3 V. Therefore, the V-TFD can provide LV switching and HV rectification for a wide variety of applications.
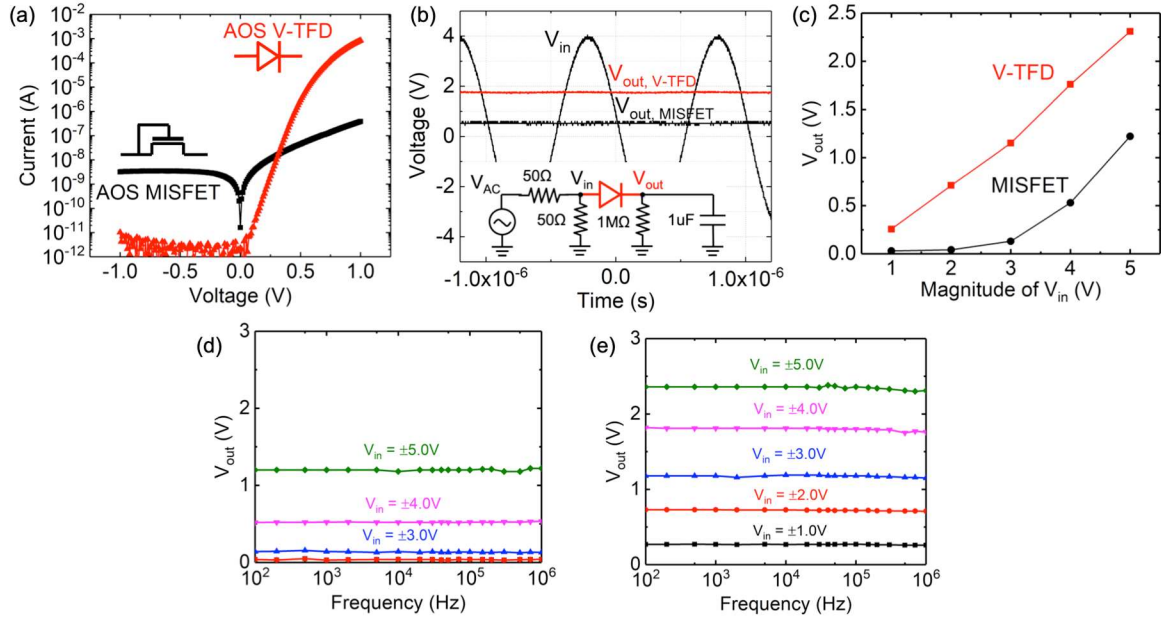
Figure 6.12 High voltage operation of AOS V-TFD with low-voltage switching. (a) Typical *I-V* measurements of AOS V-TFD and AOS MISFET in diode configuration, with its G-D shorted as shown in the inset. The V-TFD has a diameter of 100 μm, while the MISFET has total device area of 100 μm×100 μm. (b) and (c), AC-DC conversion of V-TFD (red) and MISFET (black) in the half-wave rectifier (HWR) configuration shown in the inset. An AC input voltage (V_{AC}) was generated by a signal generator operated in 50 Ω mode. The resulting V_{in} across a matching 50 Ω parallel input resistor is a 1 MHz ±4 V sinusoid. A load consisting of 1 MΩ and 1 μF in parallel is used to obtain a DC output voltage (V_{out}). (c) Measured $|V_{out}|$ versus $|V_{in}|$ at 1 MHz. Thanks to a lower V_{switch}, the V-TFD has a consistently higher V_{out}. (d) and (e), HWR measurement results using the configuration shown in the inset of (b). The input AC voltage was supplied by an HP 33120A function generator. Its frequency was swept from 100 Hz to 1 MHz for each magnitude of voltage, V_{in}. Measurements at frequencies above 1 MHz cannot be done due to parasitic inductance of the probe cable. V_{out} measurements were done using a Tektronix MSO2024b oscilloscope. To obtain the DC V_{out}, a 1 μF smoothing capacitor (C_L) and 1 MΩ load resistor (R_L) were used, which give a time constant, R_LC_L of 1 s. The resulting frequency response of V_{out} for various V_{in} is shown in (d) for a G-D shorted MISFET with $W/L/OL$=100 μm/3 μm/6 μm and (e) for a V-TFD with a 100 μm-diameter.

In order to demonstrate the utility of AOS V-TFDs for monolithically-integrated 3D power circuits, a V-TFD HWR was connected to a Si finFET using a wafer probe station (Figure 6.13 (a)). An AC V_{in} of ±2.5 V was connected to a V-TFD for rectification into a DC V_{out} of ~0.7 V (Figure 6.13 (b)), which was then applied to the gate of an NMOS finFET. We modulated the AC input signal, and observed that the measured finFET current, I_{DS}, turns on and off in synchrony with the AC modulation (Figure 6.13 (c)). Note that the magnitude of V_{in} is much too high for sub-100 nm Si finFETs to handle – this task could not be done solely by the Si CMOS – while simultaneously V_{in} is too low to be rectified by a diode-connected AOS MISFET (Figure

6.12 (c)). Thus, the AOS V-TFD uniquely enables us to rectify HV AC signals and convert them into LV signals that can be read by Si CMOS.
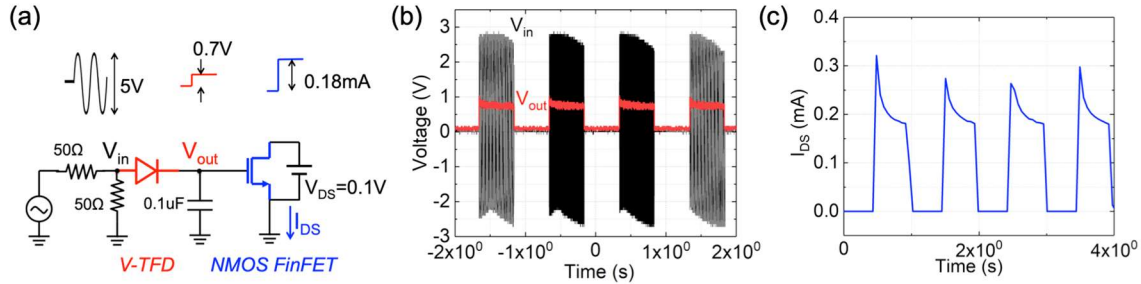
Figure 6.13 Experimental demonstration of AOS V-TFD rectifier (100 μm-diameter) driving a Si finFET (L=150 nm). (a) A square-shaped amplitude modulated (AM) wave with a carrier frequency of 100 kHz and interval of 1 s was applied to the V-TFD rectifier input (V_{in}). The NMOS finFET was operated at V_{DS}=0.1 V supplied by a source meter. (b) The V-TFD rectifies ±2.5 V AC wave and supplies ~0.7 V of DC V_{out} to switch the finFET. (c) The modulated on-current of finFET. The transfer curve of tested NMOS finFET is in Figure 6.9 (a), which shows that an on-current of ~0.18 mA at V_{DS}=0.1 V corresponds with the I_{DS} measured when V_{GS}=V_{out}=~0.7 V. (b) was measured with an oscilloscope and (c) with a source meter.

The AOS V-TFDs are further characterized with stress tests in order to determine their safe-operating area and future application window. For example, based on the AC-DC conversion demonstrated in Figure 6.12, the V-TFD may be used for energy harvesters [107], [146] to wirelessly power LV Si ICs for autonomous operation. In this case, most of the V_{in} is applied as reverse bias to the V-TFD, and thus its breakdown voltage (BV) and reverse-bias-stress endurance determine the maximum V_{in} that can be applied and the diode's lifetime [146] as established in Chapter 5. In addition to long-term rectification, the diodes may be used for short-term events, such as ESD protection. An ESD event can send undesirably high current spikes to CMOS circuits that cause permanent IC failure [299]. To bypass the ESD current and protect the IC, circuit designers typically integrate diodes that can endure a high current for a short period of time, i.e. 100 ns, in parallel with LV Si CMOS ICs pads. The diode on-state resistance (R_{on}) and on-current-stress endurance thus become critical parameters. Therefore, along with R_{on} and BV,

the stress endurance of AOS V-TFDs should be analyzed to explore the potential use of AOS V-TFDs in ESD circuits for monolithically integrated systems.

We first show that these V-TFD characteristics can be further modulated to suit other HV operation windows, by changing AOS thickness as shown in Figure 6.14 (a). Increasing the AOS thickness comes with higher voltage handling capability, with a trade-off in current handling capability. Our five-layer a-ZTO V-TFDs show low R_{on} of ~869 Ω and high BV of ~11 V. Characterization of stress effects is especially critical for AOS as shown in Chapter 5. Unlike atoms in covalent semiconductors, ions in ionic semiconductors such as AOS can drift within the lattice under high electric field. If a high field is maintained for a long time, the accumulation of migrated ions can cause degradation and breakdown within AOS devices [192]–[194]. Assessing this time-dependent behavior requires stress endurance tests of AOS V-TFD [146]. To perform current stress measurements, we flow a given on-current (I_{stress}) through a V-TFD for various stress times, until the devices show degradation. To test bias stress endurance, various reverse biases (V_{stress}) are applied until the measured off-current reaches the compliance current level. The test results are summarized in Figure 6.14 (b) and (c), respectively. For AOS V-TFDs, the shorter the stress duration, the larger the value of I_{stress} or V_{stress} that can be endured. For example, for a 1 min stress period, the V-TFD can supply 10 mA without degradation, and can block voltages as high as -8 V. For I_{stress}=10 mA, the voltage drop across V-TFD was ~3.68 V, leading to an R_{on} of ~368 Ω. Thus, in addition to the high BV and large V_{stress} exhibited by our V-TFDS, which make them useful for energy harvesters [107], [146], the large value of I_{stress} and low value of R_{on} measured here indicate that the V-TFDs potentially may be used for high current applications, such as ESD protection.
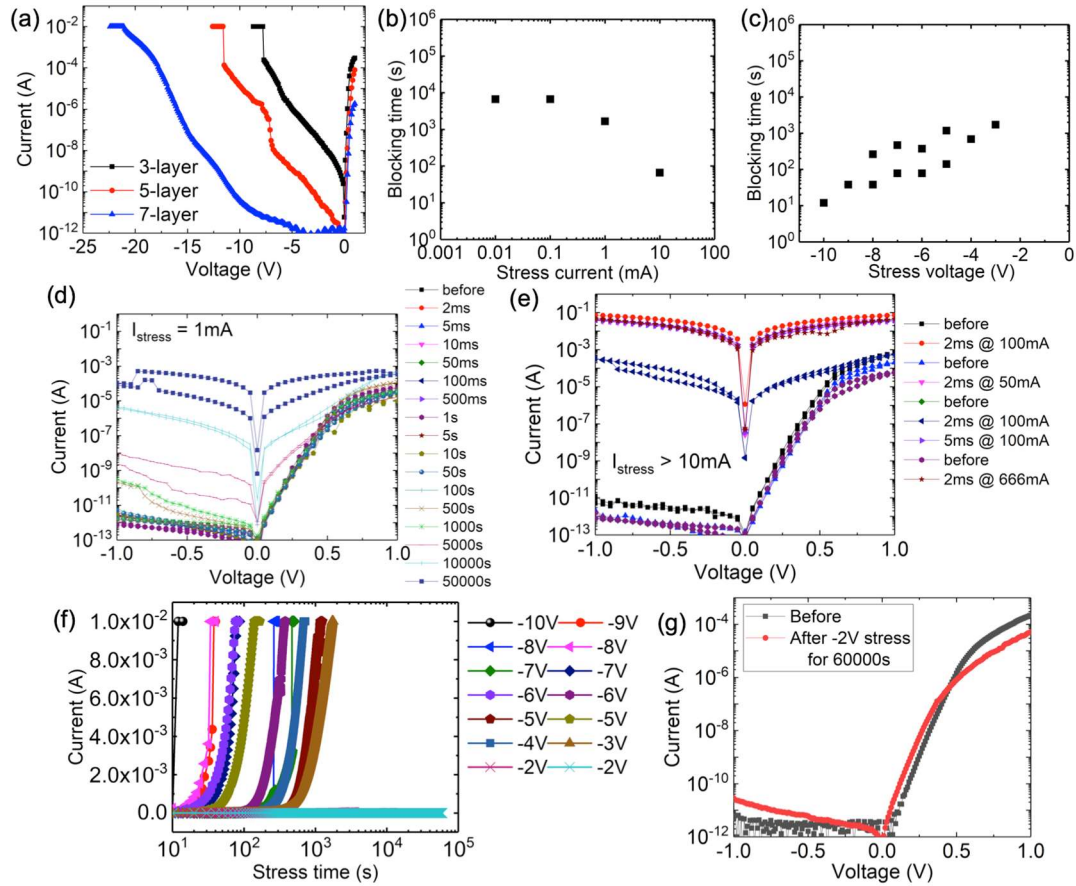
Figure 6.14 Determining safe operating area and design window of AOS V-TFD These measurements were done on 50 μm-diameter V-TFDs. (a) Typical breakdown voltage (*BV*) measurement of V-TFDs made with different *a*-ZTO thickness, from quasi-static voltage sweep. By spin-coating more AOS layers, higher *BV* can be obtained with corresponding trade-off in on-state resistance (*R*$_{on}$). (b) and (c) summarize the results of on-current and reverse-bias stress tests, respectively, performed on five-layer *a*-ZTO V-TFDs . In (b), various on-currents (*I*$_{stress}$) from 0.01 mA to 666 mA were applied for various times, increasing from 2 ms to 50,000 s, until the V-TFD started to degrade, as indicated by an increase in the off-current. To confirm device degradation, the *I-V* curves were measured in between stress events as shown in (d). The corresponding blocking time is the total stress time required to increase off-current at -1 V to above 1 nA. In (c), reverse bias stress tests were performed for various DC voltages (*V*$_{stress}$) from -2 V to -10 V. Here, the blocking time is defined as the stress time required for the off-current to increase up to the level of the compliance current. Both (b) and (c) show that the blocking time of the V-TFD decreases as the current or voltage level increases. (d) *I-V* curves measured between *I*$_{stress}$ = 1 mA stress tests of various durations. Here, diode failure occurs by loss of rectifying behavior in reverse bias. The stress tests and *I-V* measurements were automated using LabVIEW, so that there was minimal down-time between the stress and *I-V* measurements. The *I-V* measurements were performed with short integration time with a 0.05 V step. It is worth noting that several V-TFDs (e.g. navy squares) show an opening of the forward-reverse *I-V* sweep after failure, which indicates conductive filament formation. The filament formation may be occurring via Ag ion migration, which also causes the change in forward bias behavior. (e) *I-V* curves measured between short-duration current stress tests with *I*$_{stress}$ from 50 mA to 666 mA, measured in an identical manner to those described in (d). For these high currents, the diodes break down at 2 ms, the minimum stress time that can be applied with our tool. Since the effective blocking time cannot be extracted for these currents, these results are not included in (b). (f) Reverse currents of 14 V-TFDs tested at constant reverse bias (*V*$_{stress}$) from -2 V to -10 V. The stress times required to increase the leakage current to the compliance current level of 10 mA are obtained for *V*$_{stress}$ of -3 V to -10 V, and are plotted in (c). The measurements shown here were done with medium integration time. When *V*$_{stress}$ is as low as -2 V, the V-TFDs do not breakdown even after applying stress for 60,000 s. (g) *I-V* measurements obtained from a V-TFD before and after it was exposed to a -2 V bias stress for 60,000 s. The changes in *I-V* behavior due to the bias stress are minimal.

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In summary, by adding MESFET and V-TFD devices to an existing AOS MISFET technology, we have successfully fabricated TFTs, logic inverters, and rectifiers that can switch at LV for effective bridging with LV Si MCUs. Similar circuits made using only MISFETs typically have high driving voltages >1.5 V. Thus in previous AOS 3D-IC demonstrations, BEOL inverters could only be driven by an MCU at ≥5 V [6], and their ESD protection diodes exhibited a undesirably high R_{on} of >1 kΩ [238]. Previous attempts have been made to improve MISFET circuit behavior by lowering its V_{switch} or R_{on}, or by making both enhancement-mode and depletion-mode MISFETs, but these methods often compromised the device switching performance [236], [298], [300], [238]. Here, by developing a new AOS contact structure that enables high-performance MESFET and V-TFD devices, we have demonstrated a way to solve all of these limits at once. Here, by incorporating MESFET and V-TFD devices with MISFETs, the switching voltage is reduced from 2.9 V to 1.1 V for TFTs, from 1.9 V to 0.96 V for inverters, and from 2.9 V to 0.49 V for rectifiers. These low switching voltages are critical for monolithic integration with sub-100 nm node MCUs that operate at ~1.2 V. In addition to LV, AOS IC made with MISFET, MESFET, and V-TFD can handle HV applications, thanks to their large BVs (>40 V for MISFET, >80 V for MESFET, and >10 V for V-TFD). The enhanced inverter and rectifier performance combined with in-air monolithic integration of AOS demonstrated here allow future HV driver ICs [6], [226] or power harvesters [107], [146] to be fabricated directly on Si MCUs, allowing functionality diversification and miniaturization beyond Moore's law (Figure 6.1 (a)).

6.6 Individual bypass diodes for large-area power management on solar cell panels

The AOS V-TFD developed herein, with excellent switching characteristics, can be further exploited in other large-area electronics applications such as solar cells, for efficient power management. When solar cells are used to harvest energy, they are connected serially in a chain in order to produce the necessary voltage. If, however, just one solar cell in a serial chain becomes shaded, it acts as a load to the entire chain and severely limits the performance of the overall array. To solve this issue, bypass diodes may be connected in parallel with solar cells. When some solar cells are shaded and act as a load, the current generated from neighboring solar cells can bypass the shaded cells through bypass diodes that are now turned on. Ideally, in order to manage the partial shading issue, we would have one bypass diode for each solar cell [301]. However, attaching a separate bypass diode across each solar cell is not feasible due to package/integration cost. Monolithic integration of bypass diodes along with solar cells is ineffective in terms of fabrication cost and device structure since the diode can occupy non-negligible area of the entire solar cell. Due to these limitations, standard solar cell arrays typically have only one bypass diode for each 12-24 solar cells, to prevent irreversible breakdown of the panel under partial shading [8]. This configuration is shown in Figure 6.15 (a). However, one bypass diode for this many solar cells is not enough. In this scenario, the reverse biasing of a shaded solar cell by adjacent cells generates severe heat and hot spotting occurs [302]. Moreover, the corresponding loss leads to low efficiency in power harvested by adjacent cells. This partial shading issue may become even more severe in the future as solar cells adopt portable and mechanically flexible forms [303]. Thus, developing a way to manage this partial shading issue will be critical for future solar cell applications.
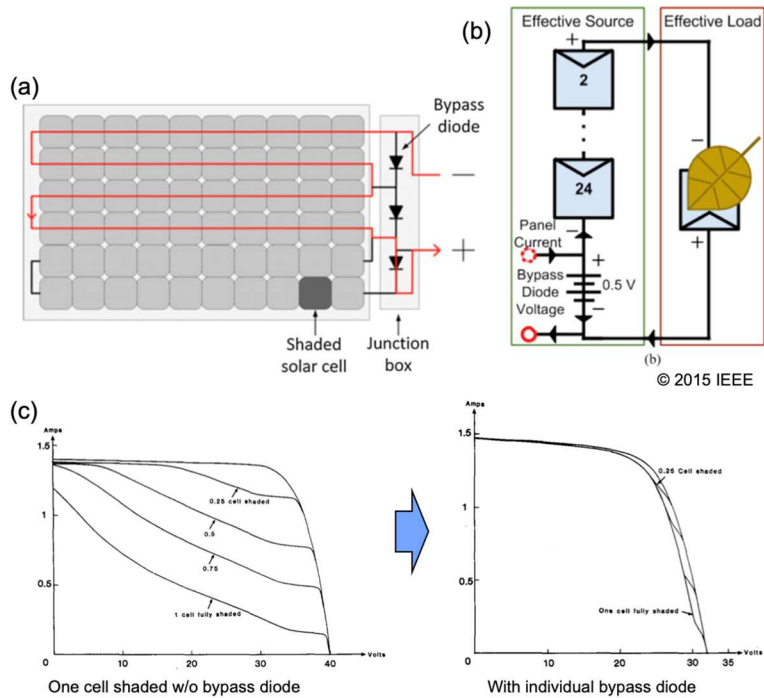
Figure 6.15 Illustration of the need for individual bypass diodes in solar cell arrays. (a) Common solar cell array configuration. Only one bypass diode is used for ~20 series solar cells due to integration challenges. (b) The impact when only one solar cell is shaded: the shaded cell acts as an effective load, causing a hot spot. (c) *I-V* curves measured for an entire array when a single solar cell is shaded without (left) and with (right) individual bypass diodes. The figures are taken from ref. [8], [302], reprinted with permission from ref. [304].

Our solution-processed AOS V-TFD can present a new solution to this challenge. The low-cost and large-area monolithic integration capability of our thin-film diodes can enable direct integration of individual bypass diodes with each solar cell, so that the partial shading issue can be effectively mitigated. As our devices can be integrated additively, one can directly stack the bypass diode layer on the side of solar panel where light is not absorbed, thereby preserving the structural fill factor of the solar panel. In order to demonstrate this application, we measured commercial solar cells under partial shading conditions and simulated the effect of future integration of our diode. First, a portable solar panel, Panasonic AM-1815 CA, was used (Figure 6.16 (a)). This is an indoor solar panel that requires illumination below 1,000 lux. The

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structure of AM-1815 consisted of *a*-Si that is sandwiched between a positive transparent electrode (TCO) and negative electrode (metal). As shown in Figure 6.16 (b), it consists of eight solar cells in series, with no bypass diodes integrated. The positive electrode of one solar cell connects to the negative electrode of the next cell. In order to measure the effect of partial shading, the *I-V* characteristics of the AM-1815 solar panel were tested under light, where one cell was shaded at various ratios (Figure 6.16 (c)). For illumination, two florescent light fixtures were used with a custom-built probe station, which showed peak power density of 389 μW/cm^2 at 290 nm (measured using a ThorLabs PM200 and S120VC sensor). When one solar cell was shaded, the *I-V* curves showed significantly decreased current and power output, as shown in Figure 6.16 (d). This was due to the shaded solar cell restricting the current through the entire panel in series. The serial connection is obtained by bottom TCO electrode of one solar cell connecting to the top metal electrode of the next cell. Therefore, an individual bypass diode can be monolithically integrated to each cell when properly deposited on the top metal electrodes, as shown in Figure 6.16 (e).
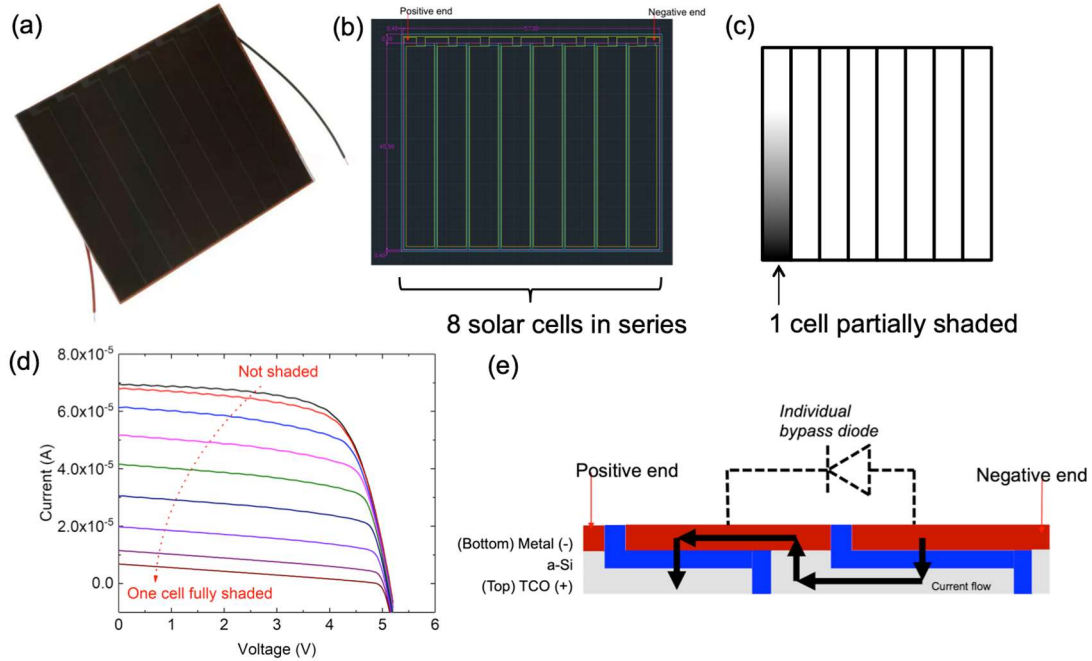
Figure 6.16 Testing of a commercial *a*-Si solar panel under partial shading condition. (a) A picture of the Panasonic AM-1815 CA solar panel. The size is approximately 4.7 cm × 5.6 cm. (b) The structure of the panel, showing eight columns. Each column is one solar cell serially connected to adjacent cells. (c) Test configuration for partial shading, done by shading just one cell out of eight cells. (d) The measured *I-V* characteristics under illumination with its peak power density of 389 µW/cm^2 at 290 nm. By shading just one solar cell out of eight, the current through the overall panel dramatically reduces. (e) A cross-sectional view of the tested solar cells, with the proposed individual bypass diode shown, which can be monolithically integrated with solar cells.

To confirm the benefit of future monolithic integration of our V-TFDs as individual bypass diodes, we performed Cadence simulations of the solar cells combined with AOS rectifiers, where the individual device performance was extracted from the aforementioned measurements (Figure 6.17 (a)). For the AOS rectifier, both the diode-connected MISFET (shown in Figure 6.17 (b)) and the Ag:ZTO V-TFD (shown in Figure 6.17 (c)) were simulated for comparison. The *I-V* curves of solar panel with these rectifiers were simulated and are shown in Figure 6.17 (d) and (e), respectively. Compared to the case without diodes, shown in Figure 6.16 (d), a higher panel output current is achieved in both rectifier cases. The impact of rectifier integration was further evaluated in terms of power efficiency. Shown in Figure 6.18 (a) is the power-voltage (*P-V*) curves measured from a solar panel under one cell shading (with no bypass

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diodes). Without shading, the AM-1815 solar panel under two florescent light fixtures generates a maximum power (P_{max}) of ~240 µW. However, as one cell becomes fully shaded, the cumulative area (the area under the power curve) decreases dramatically and P_{max} reduces to ~9 µW, leading to 4% peak efficiency. Using an AOS TFT as the individual bypass diode shows only marginal effect in resolving this shading issue. As shown in Figure 6.18 (b), with one cell shaded P_{max} reduces from ~240 µW to ~65 µW, leading to 27% peak efficiency. This inefficiency is attributed to the non-ideal switching of TFT-based rectifiers. Moreover, when the cell is not shaded fully, P_{max} are slightly lower when TFTs are used as bypass diodes.
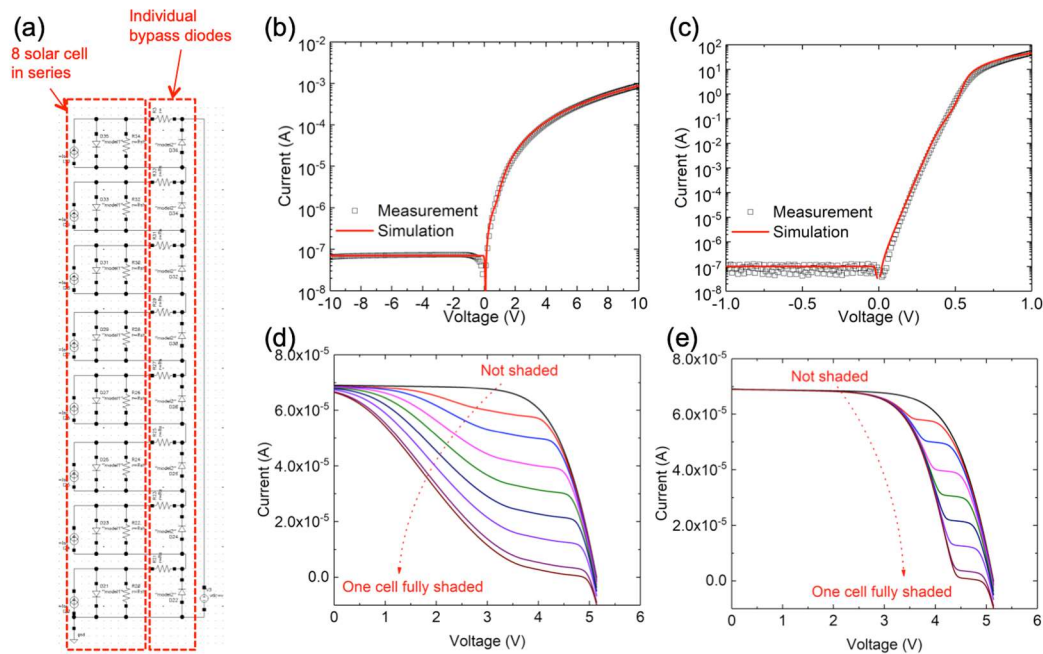
Figure 6.17 Cadence simulation of AOS TFT and AOS V-TFD as individual bypass diodes for a commercial *a*-Si solar panel (a) The schematic of solar panel and bypass diodes simulated in Cadence. As shown in the right dotted box, one rectifier was attached in parallel with each solar cell. (b) and (c) show the simulated rectifier *I-V* curves, which show good agreement with the measured behaviour. (b) *I-V* curves of the TFT diode, where the measured *I-V* curve was scaled for a channel width of 3 mm and length of 3 µm. (c) *I-V* curves of a Ag V-TFD, where the measured *I-V* curve was scaled for a device area of 1 cm^2. (d) and (e) Simulated *I-V* curves of the entire solar panel with the bypass diodes, when (d) the TFT shown in (b) is used, and (e) the V-TFD shown in (e) is used. The shading-induced reduction of solar panel output current is much less severe when V-TFDs are used.

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However, when V-TFD is used, these challenges can be effectively overcome. As shown in Figure 6.18 (c), the cumulative area does not decrease significantly under partial shading. P_{max} at one cell shading reduces only from ~240 μW to ~200 μW, leading to high peak efficiency of 83%. For comparison, the P_{max} for one cell shading with different bypass rectifiers are summarized in Figure 6.18 (d). This result confirms the opportunities of AOS V-TFD to enhance power efficiency of solar panels, opening the door for novel large-area power management via thin-film electronics.
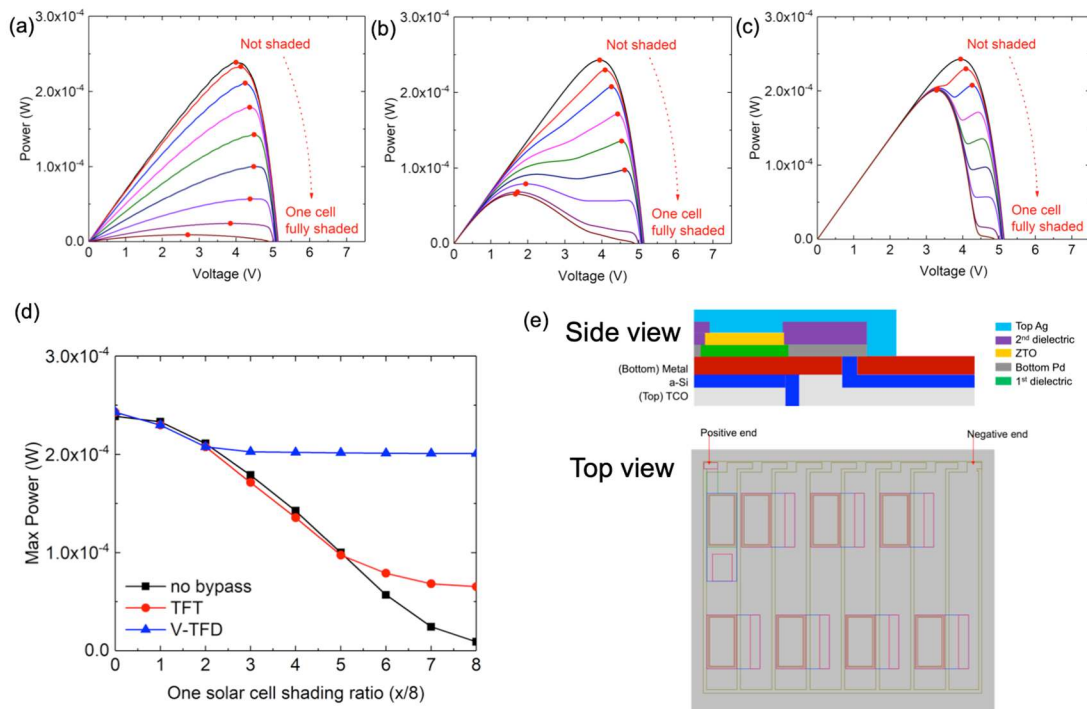
Figure 6.18 Efficient power management of the AOS V-TFD used as an individual bypass diode to mitigate partial shading. (a)-(c) are the *P-V* curves with one cell shaded. The maximum power points are marked with red dots. (a) Measured *P-V* curves of the solar panel without bypass diode. The maximum power as well as cumulative area decreases dramatically as the cell is shaded. (b) Simulated *P-V* curves of the solar cell array when connected with individual TFT diodes. The *P-V* curves are still dramatically affected by shading. (c) Simulated *P-V* curves of the solar cell array when connected with individual V-TFDs. This time, the shaded cell is effectively bypassed and the *P-V* curves are minimally changed by shading. (d) The value of P_{max} under shading for all three cases. (e) A possible design of AOS V-TFD (both device cross-sectional view and top layout view) to be integrated monolithically with the AM-1815 CA solar cell, which could be used to obtain the predicted result shown in (c).

6.7 Conclusion

In this chapter, we have shown how three-dimensional, monolithic integration of additional device layers using solution-processed AOS can further enhance the power-managing capability of current Si-based electronics. To enhance chip performance beyond the scaling limits of Moore's law, monolithic 3D integration of additional device layers can be done on top of sub-100 nm Si ICs. For device-level integration of the Si and 3D-integrated layers, the new device layers, here made using amorphous oxide semiconductors (AOS), must have a driving voltage of ~1 V. Here, we demonstrate monolithic integration of standard AOS MISFETs on top of state-of-the-art Si CMOS finFETs using an air-stable process [58]. We then show that MISFET-only AOS circuits pose challenges for obtaining a low driving voltage: the high SS of TFTs causes a high V_{switch} of >1.5 V, and its positive V_T leads to a high V_{tran} of >1.5 V for MISFET-only inverters. Due to the HV handling capability of AOS, the concept of BEOL CMOS integration for I/O bridging [6], [226] and ESD protection [238] has been presented by others. However, those works centered on the MISFET, and thus, their BEOL inverters were driven by MCU at ≥5 V [6], their wireless energy harvesters were operated at ≤13.56 MHz [20], [108], and their ESD protection diode exhibited high R_{on} of >1 kΩ [231], [238]. Likewise, our transistor, inverter, and rectifier based on an AOS MISFET exhibit undesirably high V_{switch} of 2.9 V, V_{tran} of 1.9 V, and V_T of 2.9 V, making it inapplicable for 3D-IC on LV MCU.

In addition to realizing HV 3D-IC on Si MCU, our AOS thin-film ICs can be used to implement novel power managing schemes for future large-area electronics. One example is the individual bypass diode for solar cells. Attaching one rectifier with good switching characteristics in parallel with each solar cell is ideal for efficient solar power harvesting under partial shading conditions. Monolithic integration of our devices on solar panel can achieve this

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without separate packaging/attaching of rectifiers, which is the current industry standard. Based on measurements of a commercial *a*-Si solar panel, we simulated the impact of integrating our MISFET as individual bypass diodes. However, once again due to the high V_{switch} of MISFET, it cannot efficiently bypass the solar cell current, and thus cannot manage the partial shading issue well. These demonstrations show that the high V_{switch} of the AOS MISFET poses fundamental barriers to the use of AOS thin-film ICs to further improve Si-based electronics.

In this chapter, we resolved this challenge by developing two different device structures. In order to obtain new transistors, inverters, and rectifiers that switch at low voltage, we develop high-quality top-Schottky and bottom-ohmic contacts for *a*-ZTO to fabricate MESFETs and V-TFDs. The choice of a top-Schottky structure comes from our experience with bottom-Schottky structures, which show non-ideal switching due to various interface chemistries. Thanks to the top-Schottky structure, superior switching performances are obtained. The contacts were thoroughly analyzed with material and electrical characterization. By introducing these devices alongside the MISFET, the AOS IC can perform LV switching, which is challenging with MISFET-only circuits. Namely, the MESFET shows low V_{switch} of 1.1 V, and depletion-load inverters made by integrating load MESFET with a drive MISFET has low V_{tran} of 0.96 V, while a rectifier made with a V-TFD has low V_{bi} of 0.49 V. In addition to LV switching, HV handling capability are also obtained using these devices, which show high BVs of >40 V for MISFETs, >80 V for MESFETs, and >10 V for V-TFDs. Therefore, the technologies demonstrated here can be used for HV-to-LV bridging using monolithically integrated AOS ICs on Si MCU. Moreover, using Cadence simulations, we successfully predicted better power efficiency of a solar panel under partial shading conditions if n AOS V-TFD is integrated with each solar cell. When one cell out of eight in the series is fully shaded, we predict that the corresponding peak power

efficiency can be increased from 4% to 83% by using a AOS V-TFD as the individual bypass diode. Thus, HV operation and LV switching capabilities of AOS thin-film IC together pave the way for a novel monolithic integration of 3D PMIC for future functionality diversification of Si-based electronics [232].

Chapter 7 Conclusion and Future Work

7.1 Conclusions

This thesis pushes the boundaries of AOS applications by developing an air-stable deposition process and applying it to fabricate new devices in addition to standard TFTs. In doing so, this thesis opens up new opportunities in power electronics application, enabled by monolithic integration of large-area, thin-film electronics. The main contributions of this thesis can be summarized as follows:

1. Air-stable deposition of high quality amorphous oxide semiconductors (AOS) using a solution process, which can be done across a wide humidity range (relative humidity (RH) of 10% - 83%), was achieved. As shown in Chapter 2, our amorphous zinc tin oxide (*a*-ZTO) films have μ_H of 5.53 cm^{2}V^{-1}s^{-1} and n_{free} of 4.6×10^{16} cm^{-3}, and thin film transistors (TFTs) with uniform μ_{lin} of 3.76-5.62 cm^{2}V^{-1}s^{-1} and *SS* of 0.23-0.39 V/decade were fabricated in air on both glass and silicon substrates. These were achieved by understanding the effect of chemical composition of ZTO on its electrical properties and by optimizing the chemical evolution of our film deposition process to eliminate hydroxyl defects at the channel layer region.

2. Using this air-stable deposition, AOS vertical thin-film diodes (V-TFD) were achieved with Pd or Mo electrodes as the bottom Schottky contact. We showed that the Schottky interface can be engineered by controlling chemical evolution during the solution process, namely by exploiting thermally-driven redox mechanisms at the metal-semiconductor interface. As

shown in Chapter 3, a bottom Pd layer, which would otherwise form an ohmic contact with *a*-ZTO, can form a rectifying contact (on/off ratios $>10^2$ at ± 1 V) when oxidized prior to ZTO deposition state. Oxidized Pd reduces to metallic Pd *in situ* during ZTO deposition and annealing, reducing oxygen vacancy defects at the interface. In contrast, a *bottom* Mo layer underneath forms a rectifying contact (on/off ratios $>10^2$ at ± 3 V) by being oxidized *in situ* during ZTO deposition and annealing. This is quite different than the case of *top* Mo, which forms a good ohmic contact to ZTO without oxidation [54]. This interfacial engineering approach can be applied to future vertical rectifiers and switches with other oxide semiconductors.

3. We addressed oxygen vacancy migration within AOS as a main source of instability and lifetime issues in AOS V-TFDs. By changing the bottom Schottky electrode from Pd to Mo and inducing *in situ* diffusion at the metal-semiconductor interface, the voltage handling capability and operation lifetime of V-TFD was increased: the reverse blocking voltage increased from <3 V to >10 V and we observe negligible bias stress effect when applying -8 V for 60,000 sec at room temperature. AC-to-DC conversion in half-wave rectifier configuration of Mo V-TFD showed AC input voltage as high as 10 V_{pp} can be rectified without degradation, with AC frequency up to 15 MHz.

4. Using high-voltage and high-frequency Mo V-TFDs, we demonstrated their use in wireless energy harvesters using a commercial 13.56 MHz RFID reader and antenna. Moreover, with Mo V-TFDs, we developed facile process method that can fabricate V-TFDs and TFTs simultaneously, without adding any fabrication steps. This was achieved by utilizing area-selective chemical evolution of our solution processed ZTO. We showed that, as a power rectifier, V-TFDs offer superior performance compared to diode-connected TFTs. Moreover

our V-TFDs have a theoretical cut-off frequency in the gigahertz range. On the other hand, TFTs are necessary for logic circuits. Thus, our co-fabrication process to integrate two devices and the successful demonstration of RFID AC-DC rectification paves the way for a future low-cost thin-film-based RFID tags.

5. After explaining the origin of non-idealities of *bottom* Schottky contacts, we developed high-quality Schottky contacts by using *top* Ag. Here, the bottom ohmic contact was made with Pd without pre-oxidation. We confirmed that the top Ag layer oxidizes after deposition to form a Ag_xO Schottky contact. Using this structure, we achieved a high-performance V-TFD with on/off ratio $>10^8$ at ±1 V, and ideality factor, $n <1.1$. Our charge transport analysis showed a high Schottky barrier at 0.97±0.1 eV, leading to a low leakage current density near $5×10^{-7}$ A/cm^2. Thanks to the low leakage current, we also fabricated the first spin-coated AOS MESFET (Schottky-gated TFT with MEtal-Semiconductor structure) with on/off ratios $>10^6$ and *SS* of 0.11 V/dec. The low n and *SS* obtained for V-TFDs and MESFETs can effectively reduce the switching voltage of AOS thin-film ICs.

6. We experimentally demonstrated monolithic integration capability of our solution process on top of active Si CMOS ICs, by additively fabricating standard TFTs on 100 nm-node Si finFET. Then, we incorporated top-Schottky V-TFDs and MESFETs to enhance the performance of thin-film circuitry, which is currently based on MISFETs. As a result, we obtain a switch, an inverter, and a rectifier all with low switching voltages of 1.1 V, 0.96 V, and 0.49 V, respectively. Such low switching voltages with high operation voltages allows the monolithic integration of interface ICs on 100 nm-node Si MCUs to bridge low-voltage MCU with external high-voltage supply or loads. This result paves the way for functionality diversification and miniaturization beyond Moore's law.

7. We demonstrated via simulation another potential application of our top-Schottky V-TFD, i.e., individual bypass diodes for large-area solar cell arrays. Simulating our measured AOS V-TFD and commercial *a*-Si solar cell array under partial shading conditions, we showed that direct integration of V-TFDs on the solar cell array can significantly resolve the partial shading issue. When eight solar cells are in series, shading on one solar cell reduces the maximum power generated down to 4% of its non-shaded value, but this can be increased up to 83% by integration of our V-TFDs as bypass diodes. This result illustrates the new opportunities of power management in large-area electronics via thin-film electronics.
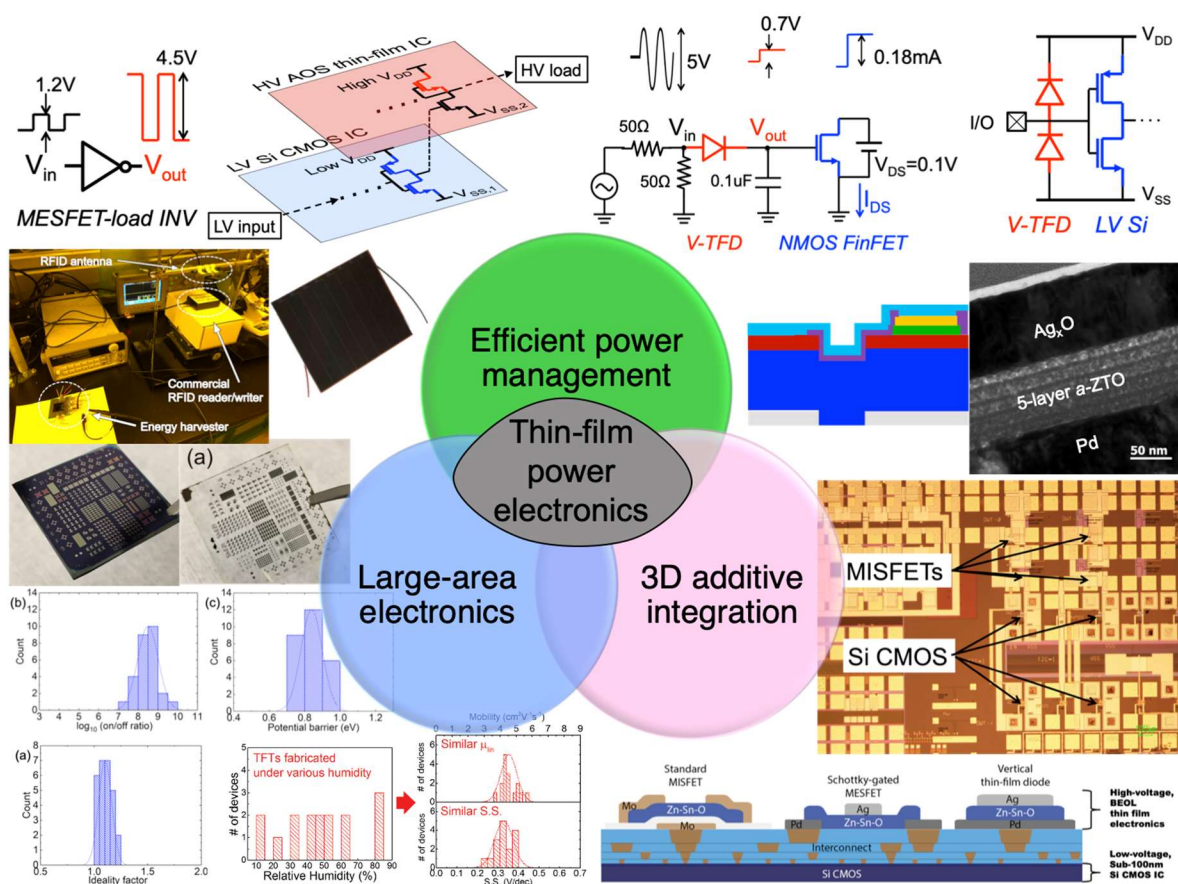
Figure 7.1 The scope of this thesis. The main motivation of this thesis is to make use of thin-film electronics that can be deposited on a large area and be integrated on various substrates or device layers, in order to open up novel thin-film power electronic application.

7.2 Future work

Throughout the thesis, solution-processed AOS thin film devices were developed and were widely exploited in novel thin-film power electronics. Further studies can extend the limits and widen the application window of thin-film power electronics. We propose the following future works that may expand the scope of this thesis further.

- **Tuning the electrical property of bulk AOS**: In this thesis, the deposition of a-ZTO layer was prevalently done with 520 °C annealing of ZTO solution with Zn:Sn=7:3. As a result, μ_H of 5.53 cm^{2}V^{-1}s^{-1} and free carrier density (n_{free}) of 4.6×10^{16} cm^{-3} were obtained. However, these parameters can be further modulated by changing stoichiometry of a-ZTO. For power-efficient devices, low on-state resistance (R_{on}) is desired, and this in turn requires high μ and n_{free}. Other literatures have shown that a-ZTO can have high μ of 28 cm^{2}V^{-1}s^{-1} and its doping can be controlled via Sn and O incorporation [90], [253], [305]. Therefore, the material design window for solution-processed a-ZTO should be further examined. While there are several studies reported on μ and n_{free} modulation for AOS in general, the variance of depletion carrier concentration (n_{depl}) has not been discussed thoroughly. We experimentally showed that unlike conventional crystalline semiconductors, the n_{free} within AOS is lower than n_{depl}. As the former contributes to lower R_{on} while the latter contributes to lower BV, it is important that the ratio of the two, n_{free}/n_{depl} is as high as possible for high power efficiency. In addition, we have established in Chapter 5 that the main breakdown mechanism within AOS is ion migration due to the electric field. We showed that this mechanism can be effectively suppressed by changing stoichiometry and/or crystallinity, but its controllability requires further study. Thus, the

controllability of AOS in regards to n_{depl} and ion migration dynamic, as well as μ and n_{free}, should be further addressed. Although solution-derived AOS was the main interest of material in this thesis, AOS can alternatively be deposited using atomic layer deposition (ALD) [46], [306] or sputtering [253], [290], which offer improved control over film stoichiometry.

- **Field-plated V-TFD with gradual doping**: Although this thesis achieved high-performance AOS V-TFD by obtaining high-quality metal contacts (Figure 7.2 (a)), the device performance can be further enhanced via device design. The intrinsic trade-off between R_{on} and BV in V-TFD can be resolved by proper doping and device structures that better distribute the electric field within the device. One method is to create a highly-doped region near the ohmic contact, while maintaining low-doping near the Schottky contact (Figure 7.2 (b)). This enables efficient electric field distribution *vertically* within AOS when the diode is in reverse bias. This highly-doped region, called a non-punchthrough layer, prevents the entire film from being depleted at moderate voltage. The electric field within AOS can further be distributed *laterally* to enhance R_{on} vs. BV. When the diode is in reverse bias, the maximum electric field is localized at the edge of Schottky contact. Thus, as shown in Figure 7.2 (c), a field-plate can be used to reduce the electric field near the edge, thereby effectively increasing the BV of AOS V-TFDs.
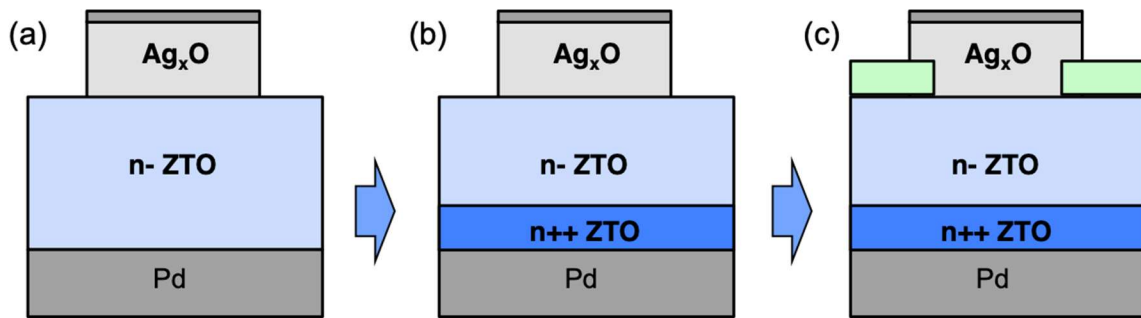
Figure 7.2 Further development of AOS V-TFD with lower R_{on} and higher BV. (a) A schematic of the V-TFD we

obtained experimentally in Chapter 6. As shown in (b), a highly-doped (n++) ZTO layer can be inserted near ohmic contact so that the V-TFD has lower R_{on} by doping, and a higher BV by preventing punch-through breakdown. This device can be further improved by incorporation of a field-plate structure, as shown in (c). As the maximum electrical field is located at the edge of top electrode, a thin dielectric layer (the green region) can be inserted to efficiently disperse the e-field at the edge. This in turn can lead to higher BV.

- **Novel vertical MESFET structures for high current**: As explained in Chapter 1, one motivation of this thesis is to enhance power performance of current AOS lateral TFTs by implementing vertical structures. This led us to obtain a high-performance power rectifier with V-TFD, but this same approach can be used for power switches, by making vertical TFT structures (V-TFT). Historically, Si power MOSFETs have achieved significant performance improvements via device innovation to vertical structures (e.g., planar to trench structures in MOSFETs). The same approach can be made for our AOS TFT, as shown in Figure 7.3. As shown in Figure 7.3 (b), our steep switching AOS MESFET obtained in Chapter 6 can be implemented in a vertical structure using sputtered Mo as the top ohmic contact. By making an inter-digitated structure for the top-ohmic and top-Schottky contacts, a high current conduction area and shorter channel length can be obtained using a vertical structure. This can allow lower R_{on} and higher cut-off frequency for AOS TFTs.
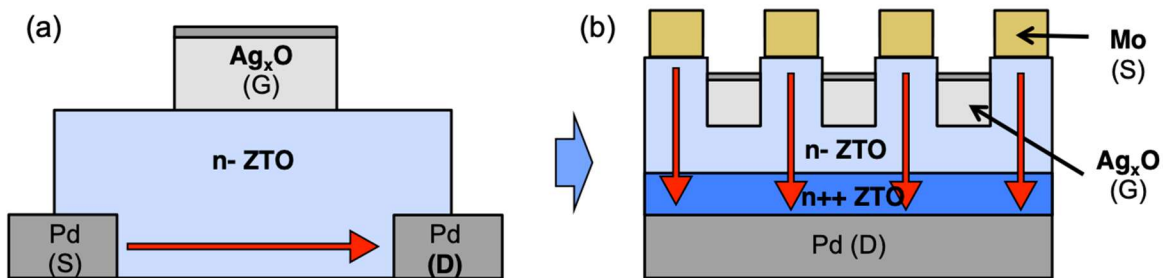
Figure 7.3 The future of AOS TFT for higher power efficiency. (a) A schematic of the MESFET that we obtained experimentally in Chapter 6. (b) A conceptual image of a vertical MESFET, obtained by high quality top-Schottky contact (Ag$_x$O), top-ohmic contact (Mo), and bottom-ohmic contact (Pd). The red arrows in both (a) and (b) indicates the electron flow when the MESFETs are turned-on. A larger current conduction area and shorter channel length are obtained for (b), allowing lower R_{on}, and higher cut-off frequency.

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