Energy-Efficient Integrated Circuits and Systems to Bridge the Gap between Power and Performance in Wireless Sensor Networks

by

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To my family

for always believing in me

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ABSTRACT

The vision of the Internet of Things (IoT) is to create an intelligent and invisible worldwide network of interconnected objects that can be sensed, controlled, and programmed. As we move towards ubiquitous deployment of IoT devices and in order to enable 50 billion connected nodes as predicted by technology leaders, ultra-low power consumption of wireless sensor nodes becomes critical. This is while existing low power approaches in wireless integrated circuits design often sacrifice performance metrics, such as noise, receiver sensitivity, transmitter efficiency, etc. which is not desirable for many IoT applications. Motivated by the ultra-low power requirements of IoT applications, this research presents low power circuit and system design methodologies to bridge the gap between performance and ultra-low power consumption in wireless sensor nodes for future IoT applications.

This work introduces an array of innovative design approaches at the RF and analog circuit level, as well as system architectures for wireless networks that enable ultra-low power consumption at the IoT sensor node, while providing high sensitivity and power efficiency values. This includes circuit designs for a long-range RF transmitter and receiver, along with front-end amplifiers for sensor read-out circuits. The proposed receiver and transmitter are designed to allow data rate agile, narrowband, and long-range IoT communications for Low Power Wide Area Networks (LPWAN) applications. More specifically, the receiver that operates at the Multi-Use Radio Service (MURS) frequency band, consumes only 152μW to achieve a sensitivity of -99dBm

at 5kbps, making it capable of communication ranges on the order of tens of kilometers. Another contribution of this work is a novel transmitter architecture. The transmitter utilizes an efficient system architecture with low power design methods, both in baseband data generation and RF circuits. It delivers a peak efficiency of 41% at a peak output power of 0dBm at 5kbps BPSK modulated data transmission, and also enables 16QAM OFDM transmission with a data rate of 384kbps, making it a suitable solution for remote IoT connectivity in multipath rich environments. In addition to the circuit level implementation of the presented ultra-low power MURS band transceiver, a narrowband transmission scheme along with a system level design and link budget analysis in the MURS band is also presented. The system analysis and transmission scheme in the MURS band shows that it can serve as an ultra-low power and long-range alternative for LPWAN applications.

Finally, an ultra-low power low-noise health monitoring analog front-end (AFE) is developed and presented in this work, that demonstrates the feasibility of <100 nW AFE for continuous ECG monitoring applications. The low-noise 68nW AFE was also integrated on a self-powered physiological monitoring System on Chip (SoC) that was used to capture ECG bio-signals from human subjects.

Chapter 1
Introduction

1.1. Internet of Things Era of Computing and Communication

The Internet of Things (IoT) is generally defined as a worldwide network of uniquely addressable interconnected objects (the "things"). It creates an intelligent, invisible network that can be sensed, controlled, and programmed [1.1]. The IoT is an evolution of the internet rather than a completely new concept. The internet allows for interconnecting hosts. Originally these hosts were super computers then became personal computers, laptops, and mobile phones. Today even machines or embedded devices are hosts.

The origin of internet dates back more than 4 decades to the ARPA network. In America the network grew from only a few hosts to a few dozen during its first decade in 1972 [1.2]. Today about 2.7 billion people have access to the internet in some form. That's roughly one third of the world population. In 2008 the number of things connected to the internet exceeded the number of people on earth. Projections estimate there will be 50 billion internet connected devices in the year 2020 [1.3]. This will include not just computers, smart phones, and tablets, but sensors, consumer electronics, and increasingly more connected objects from our daily lives. Connected things will be crucial enabling parts in many applications such as home automation, industrial control networks, health and sports, biomedical, transportations, agriculture, etc. Technology has come a

long way towards achieving today's remarkable visions for IoT. New disciplines such as wireless sensor networks (WSN) emerged and today can be considered a robust technology. 50 billion things connected to the internet will allow for a large range of applications. Sensors can be combined with data analytics in the cloud to build much more interactive applications which we can access on the internet using personal computers or mobile phones as interfaces. Estimations say that every person might be surrounded by 3,000 connected everyday things. Many IoT devices will be sensors and actuators. Providing this basic functionality does not often require extensive computational resources. However, for some IoT applications the processing of the sensing data should occur in the sensor node. From a performance point of view, it might make sense to do this processing in the cloud. However, the transfer of the raw sensor data to the cloud might present a bottleneck in both available communication bandwidth, and energy resources available on the possible battery driven or energy harvested device to send the data.

Fortunately, the computational power in integrated circuits has so far increased according to Moore's law, and makes more and more complex applications on the device's itself possible.

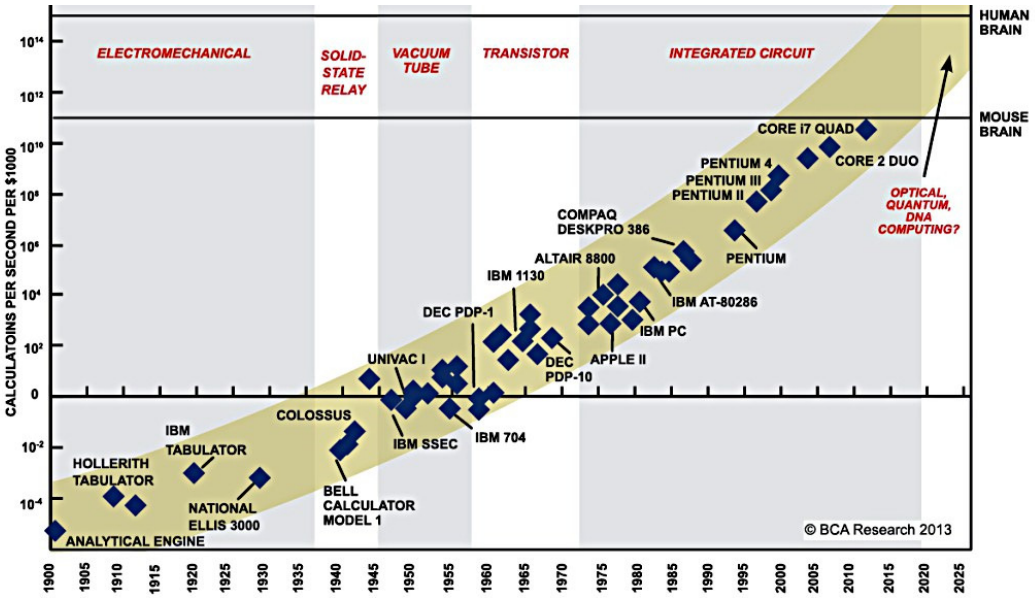
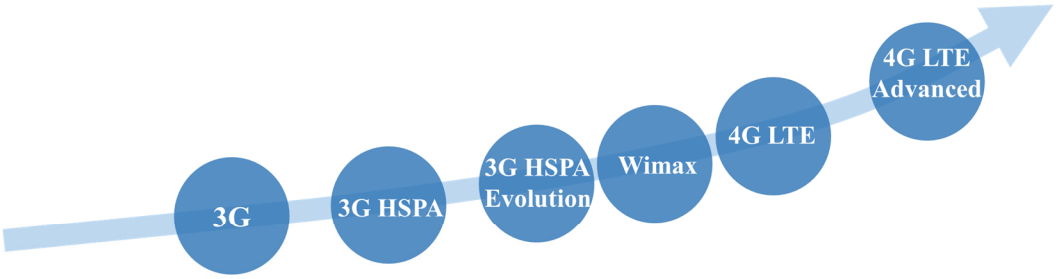


Figure 1.1. Moore's law and integrated circuits scaling [1.4]



Market Impact	2003	2006	2009	2010	2016
Peak rate	384 kbps	7 Mbps	42 Mbps	~150 Mbps	~1 Gbps
Typical user rate downlink	~200 kbps	1-2 Mbps	2-10 Mbps	10-20 Mbps	~30-100 Mbps
Typical user rate uplink	64 kbps	64-884 Mbps	0.5-4.5 Mbps	5-10 Mbps	~10-60 Mbps

Figure 1.2. Development of wireless cellular networks over the years

According to Moor's law, as shown in Figure 1.1, the number of transistors in a dense integrated circuit doubles approximately every two years. In addition, the development of wireless communication resulted in higher data rate and lower latency. Figure 1.2 shows how cellular networks are approaching data rates comparable with wired residential internet access just a few years ago. This makes denser and more advanced IoT wireless communications possible. Therefore, the continued improvements in efficient communication and moving towards denser computation units (Moore's Law), is enabling the true potential of the IoT revolution.

1.2. Wireless Sensor Networks

WSNs can be described as a network of sensor nodes and/or actuator nodes that cooperatively sense and control the environment and convey the information to gateways and clients. Recent advances in computing, communication and sensing technologies have resulted in significant changes in WSN research and brought it closer to the original vision. Research on WSNs dates back to 1980s when distributed sensor networks (DSNs) were developed [1.5]. DSNs

were considered to have many spatially distributed autonomous low-cost sensor nodes, communicating with each other. However the technology was not ready and the large size of these sensor nodes significantly limited the potential applications with wireless connectivity. The new wave of research on WSNs started around 2000 [1.5]. This research focuses on networking technology and information processing suitable for dynamic and resource-constrained sensor nodes.

The state-of-the-art sensor nodes are much smaller in size (i.e. from that of a pack of cards to dust particles), and much cheaper in price. Therefore, suitable for many new applications such as vehicular sensor network, body sensor networks, and environmental monitoring.

1.3. IoT Applications Enabled by WSNs

The IoT covers a broad range of applications and devices that can be divided into short range, medium range, and long range applications. These applications range from health care, vehicles and transportation, urban infrastructure, agriculture, to smart metering, and manufacturing. Figure 1.3 highlights major applications envisioned for IoT. There are a number

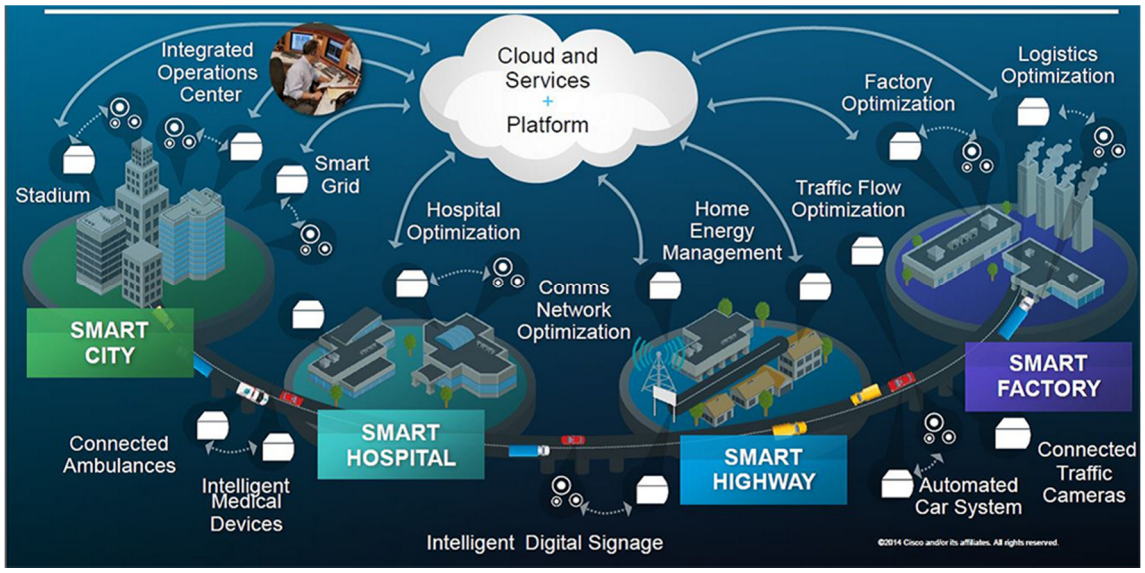


Figure 1.3. Internet of Things vision and major applications [1.6]

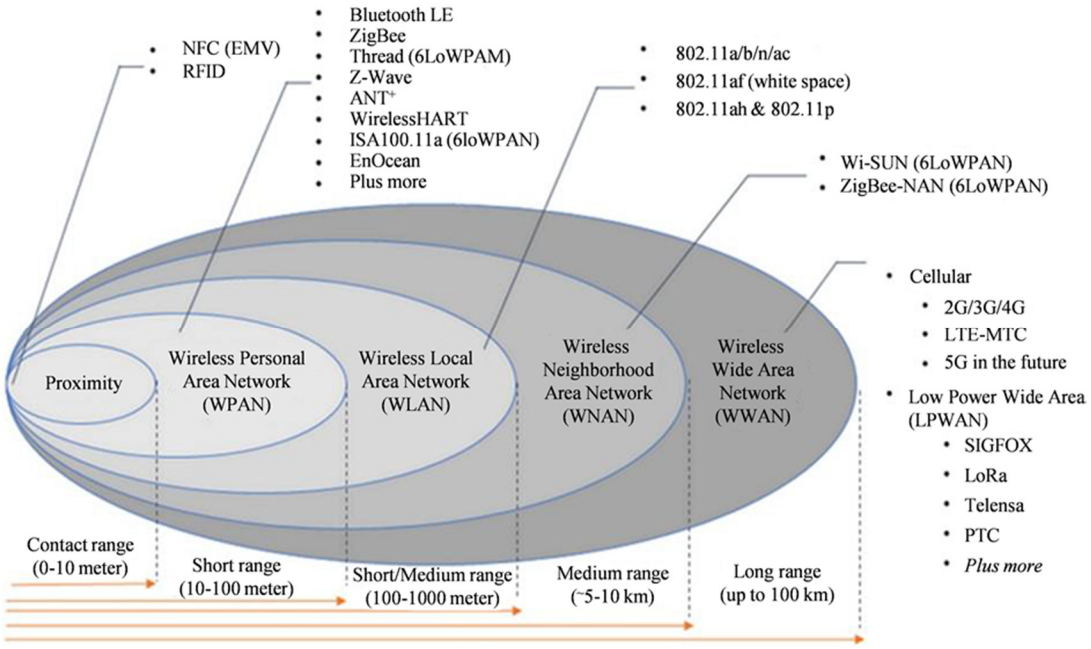


Figure 1.4. Wireless communication technologies and standards for IoT [1.7]

of wireless low-power technologies (e.g. Bluetooth low energy, Zigbee, LoRa, SIGFOX, etc.) that have been developed to address the requirements of IoT applications. These technologies are categorized based on their communication range and listed as in Figure 1.4. In the next two sections short-range and long-range applications of IoT are discussed in more details.

1.3.1. Short-Range IoT Applications

Advances in wireless technologies such as Bluetooth low energy (BLE) and IEEE 802.15.4 wireless personal area network (WPAN), have made many short-range IoT applications possible. One of the most common applications enabled by these technologies is healthcare monitoring systems. In the last decade, healthcare wearable devices have attracted much attention from the academic and industry community. Wearable devices in health monitoring are being used for motion tracking, and vital signs measurements such as ECG and EEG monitoring. With the

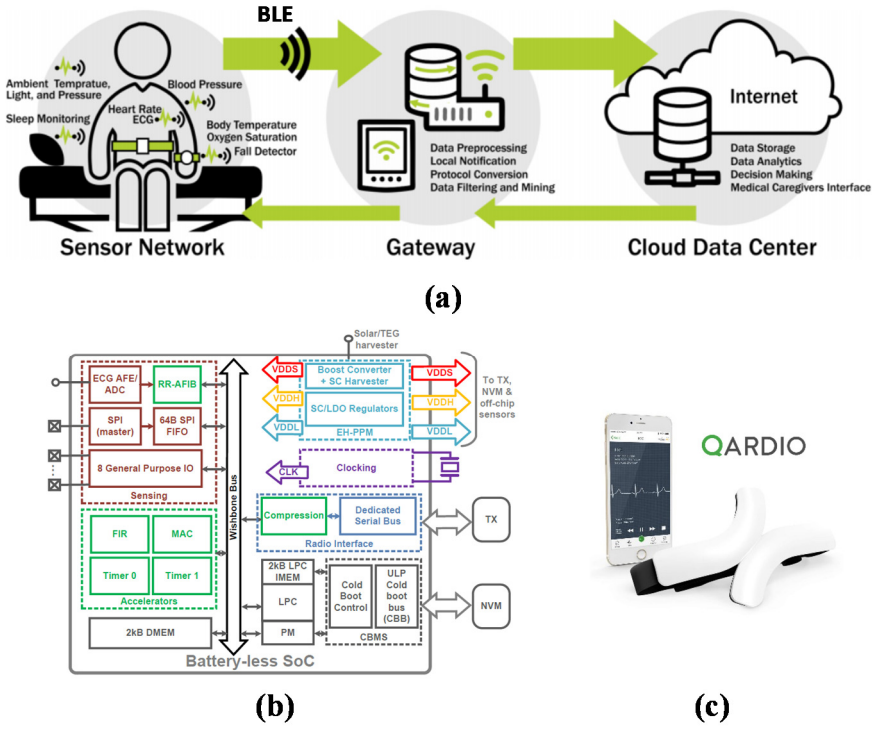


Figure 1.5. (a) General IoT-based health monitoring system [1.10], (b) Block diagram of the UMich/UVA sensor node [1.8], QardioCore ECG monitoring device [1.9]

development of WSNs, such devices can be autonomous and provide constant monitoring of patients without them being hospitalized. This helps improve quality of life and minimizes healthcare costs. As an example, in an IoT based ECG monitoring design, the ECG signal is detected by wearable sensors, sent through a short range communication technology such as BLE to the IoT wearable device where it is processed and analyzed. The analyzed data is finally sent to a remote gateway device for further analysis and storage via wide area connections such as Wi-Fi. A generalized IoT-based health monitoring system is shown in figure 1.5 (a).

An example of an academic sensor node, capable of autonomous ECG monitoring is presented in [1.8]. This work that has been done as a joint collaboration between the University of Michigan and the University of Virginia, measures ECG signals, but does so from harvested

thermos-electric energy instead of external batteries. Figure 1.5 (b) shows a block diagram of the sensor node. The battery-less system-on-chip (SoC) is designed as part of a system-in-package (SiP) with a 1 Mbps FSK transmitter (TX) at 2.4 GHz and a non-volatile memory, capable of sensing, processing, and transmission of the data. One commercial example of a smart wearable ECG monitor is QardioCore [1.9], shown in Figure 1.5 (b). This wearable device adopts wireless Bluetooth for data transmission and uses a lithium-ion polymer battery which enables a continual working time up to a day.

1.3.2. Long-Range IoT Applications

While short-range technologies are appropriate for many IoT applications, they are not well suited for all applications. Some applications such as water/gas metering in the utilities industry, lighting and waste management in smart cities, etc. require low power consumption levels and cost, but long IoT communication ranges. Therefore, Low Power Wide Area Networks (LPWAN) are considered as the evolution of WSNs for long range IoT applications. LPWAN technologies

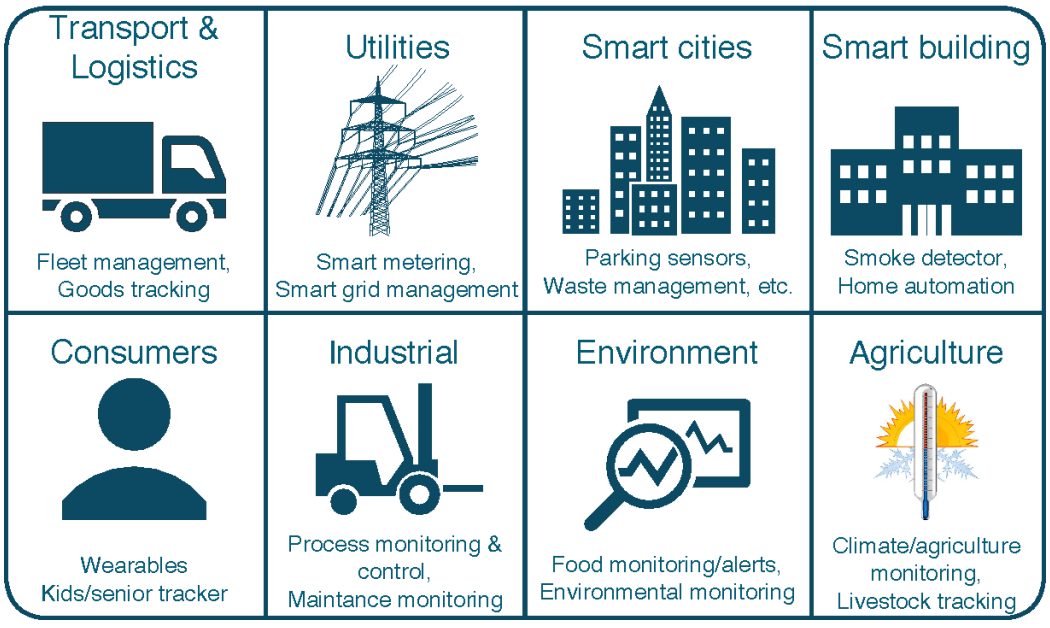


Figure 1.6. IoT applications enabled by LPWANs [1.11].

operate in both licensed and unlicensed spectrum, and has emerged to fill the gap to enable much wider range of IoT applications. LPWAN technologies have been used in different scenarios in manufacturing, power utilities, agriculture, and transportation. Examples of these applications scenarios are shown in Figure 1.6, and discussed below.

As one of the early adopters of LPWAN, power utilities use smart meters to read household energy usage as well as to send and retrieve billing information remotely in real-time using smartphones. Similarly, LPWAN technologies are making it possible for farmers to track the condition and health of soil and livestock by using LPWAN sensors. These sensors can send data on soil conditions, temperature, and humidity for fertilizer, or detect out-of-ordinary animal movement. Farming requires periodic transmission of data, a few times per hour, and due to remote and rural locations of farms, unlicensed LPWAN technologies are a good candidate for these applications. Additionally, LPWAN technologies can be used in transportation. Cellular networks can now monitor locations of vehicles, trains and boats. However, lower value assets such as parcels, luggage, and packages remain unconnected. This provides a great opportunity for LPWAN technologies, for periodic transmission of location data for these applications.

1.4. IoT Technologies for Long-Range Applications

As mentioned earlier, LPWAN technologies are attracting a lot of attention for long-range connectivity of IoT devices. This Section gives an overview of recent advances in these technologies. LPWANs are considered as the evolution of WSNs for IoT long-range low-data applications. These networks focus on low cost, scalability, extended range, and energy efficiency for end user devices as opposed to traditional broadband networks, which focus on high data rates and low latency. Some of the major applications foreseen for LPWAN are smart metering,

precision agriculture, smart homes, and intelligent transportation systems. Enabling these applications requires the following four key performance metrics for LPWAN technologies [1.12]:

- Long range: LPWAN sensor nodes are expected to communicate with base stations at distances ranging from a few to tens of kilometres.
- Ultra-low-power performance: the device should allow a battery life of greater than 10 years, or the ability to be powered by energy harvesting sensors.
- Low cost: the use of license-free bands and fully integrated transceivers with minimal off-chip components significantly reduces cost in LPWAN.
- Scalability: a single LPWAN base station is expected to connect tens of thousands of sensor nodes over several kilometers.

Several solutions have been proposed for long range connectivity to IoT devices for low data rate and low power applications. Amongst those, two of the common LPWAN technologies being deployed in higher frequency ranges of unlicensed sub-GHz ISM bands are Sigfox and Long range (LoRa) alliance. Sigfox is an ultra-narrowband technology that uses 100 Hz channels with differential binary phase-shift keying modulation [1.13]. LoRa is based on spread spectrum

Technology	SIGFOX	LoRa	RPMA	NB-IoT	Weightless-P
Freq. (MHz)	868/ 902	Sub-GHz ISM	2400	850/900	Sub-GHz ISM
Licensed	No	No	No	Yes	Yes/No
Modulation	DBPSK/GFSK	CSS	RPMA	GMSK/ QPSK (OFDMA)	GMSK/PSK
Data rate(kb/s)	0.1	0.3-37.5	0.01-8	20-250	0.2-100
Coverage range (km)	Rural: 50 Urban: 10	Rural: 15 Urban: 5	15	40	Urban: 2

Table 1.1. LPWAN technologies performance summary and comparison.

techniques and Gaussian frequency shift keying [1.14]. Another solution for IoT connectivity is NB-IoT cellular IoT technology that utilizes licensed LTE bands with 200 kHz bandwidths [1.15]. Table 1.1 summarizes the key performance metrics for the most common LPWAN technologies [1.13-1.17]. The existing LPWAN technologies often use a high uplink transmit power (>13dBm) and high receiver sensitivity values of around -140 dBm in downlink. These performance metrics result in a high power consumption in the RF front-end of sensor nodes. In addition, most of the existing LPWAN solutions utilize the sub-GHz band to target reliable long range communications with low power budgets. However, these solutions still have excessive power consumption that limits their on-time and adoption for ultra-low-power radios for massive IoT connectivity. More detailed discussions about power constraints in wireless sensor nodes are presented in the following sections.

1.5. Power in IoT Wireless Sensor Nodes

Ultra-low power operation is a key requirement to tap into the huge business opportunity by battery-powered IoT devices. In some applications such as those of LPWAN, a battery lifetime of 10 years or more with AA or coin cell batteries is desirable to achieve lower maintenance costs. Additionally, in some energy-constrained applications a self-powered and battery-less operation of sensor nodes is of crucial importance, and significantly reduces the costs associated with replacing batteries.

As mentioned earlier, the basic functionality of a typical IoT sensor node is: sensing the environment, processing some of the data on node, and wirelessly communicating with the outside world. In these devices often receivers and transmitters that are responsible for the wireless communication of the data, dominate the power budget. There are many reasons why transceivers consume higher power compared to other components in a sensor node. This is often tied into the

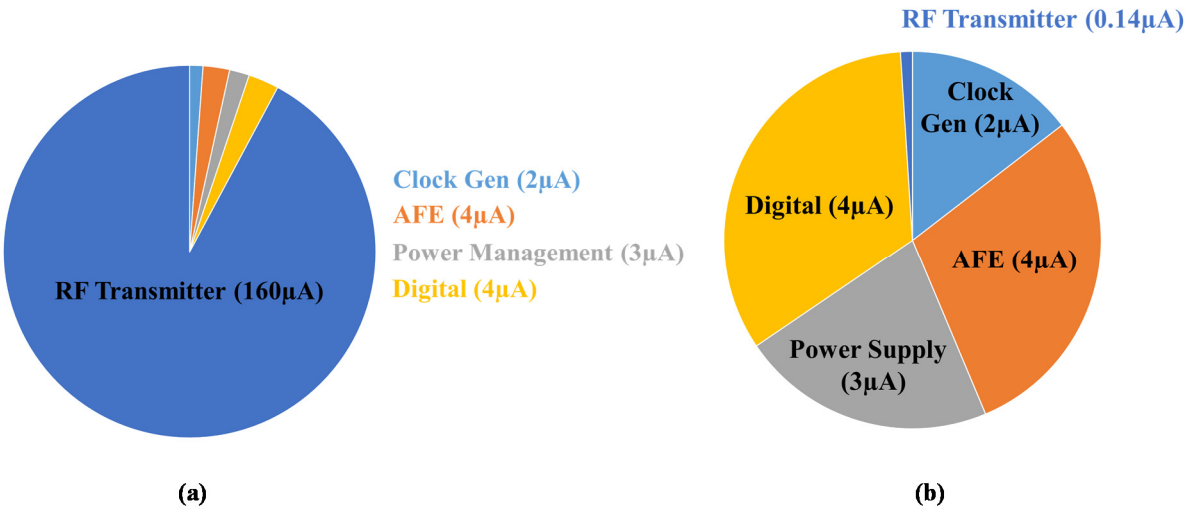


Figure 1.7. Current consumption breakdown of state-of-the-art wireless sensor node with (a) continuous transmission, (b) selective, duty cycled transmission

deliverables and specifications of radios. The main performance requirements of transceivers which leads to their high power consumption are: the high operating frequency, low noise performance and sensitivity requirements of receivers, high output power and efficiency of transmitters, and high interference tolerance which creates the need for high precision and power hungry clock generation. As a reference point, the power breakdown of the academic wireless sensor node presented in [1.18] is shown in Figure 1.7 (a). The current consumption breakdown confirms that in a state-of-the-art wireless sensor node the receiver and transmitter are the energy bottleneck.

In some IoT applications where there is no need for a continuous data transmission in the wireless sensor node, duty cycling is employed in the radios to save power. Therefore, the captured data is only transmitted if required or at specific time intervals. Although this method significantly reduces the power overhead of radios, in many scenarios analog front-ends (AFEs), which are the primary input blocks in a sensor node and responsible for amplification of the sensed data, need to stay on at all times to perform a continuous monitoring of the data. Therefore, the power

consumption for AFEs becomes comparable to the overall power consumption of sensor nodes. This is specifically important in scenarios where multiple sensing channels exists or the sensor node has to operate from a harvested energy. Figure 1.7 (b) shows this comparison and confirms the importance of ultra-low power AFEs in wireless sensor nodes.

1.6. Power-Performance Tradeoff

1.6.1. Radio Design Tradeoffs

IoT applications demand different wireless technologies and radio specifications. Some applications such as connected cars require high data rates for short-range communications, while others like LPWAN call for very long-range low data rate communications. Pushing for any of the performance metrics in a receiver or a transmitter often results in a higher power consumption. From a system-level perspective, long-range communication translates into a high link budget for a transceiver, which accounts for all the gains and losses in the transmitter to receiver path. In

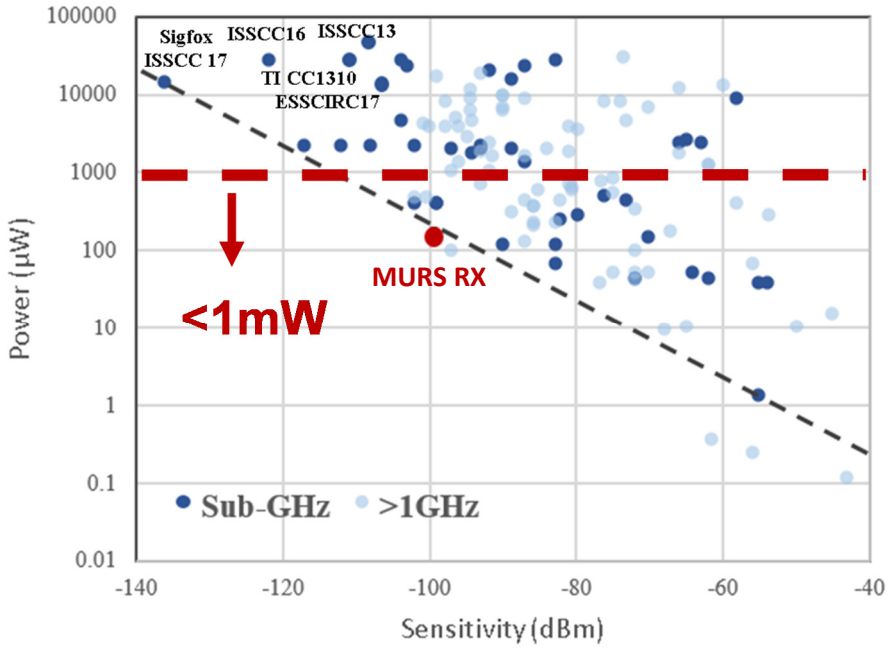


Figure 1.8. Low power radio survey: Power vs. Sensitivity, from 2005 to present. The data of the radio survey is from top conferences and commercial transceiver chips, [1.19]

order for a transmitter to enable a long-range transmission with a low power consumption, it needs to provide high output powers with high efficiency values. In addition, for receivers to enable long-range communications, they require high sensitivity values. A highly sensitive receiver would require a very good noise performance which results in a high power consumption in the receiver.

The radio survey presented in Figure 1.8 spans major conferences and journals from 2005 to 2018, and includes commercial transceiver chips, demonstrating this power-sensitivity tradeoff for low power receivers. With sensitivity, in dBm, on the x-axis and power, in μW, on the y-axis, a linear trend-line is shown on the figure that suggests a correlation between sensitivity and power. As highlighted on the top left corner of the plot, long-range LPWAN radios often target high sensitivities and interference tolerance, but have a high power consumption. In addition, some of these LPWAN technologies such as SigFox, highly sacrifice wireless communication data rate in order to achieve long range communications. It should be noted that while the survey separates radios of different frequencies, it includes receivers of different data rates, architectures, and interference characteristics; none of which is separated in the plot.

With the rapid growth in the number of IoT devices, there is a need for long-range ultra-low power, with less than a milliwatt power consumption, radios that can bridge this gap, and enable wide area ubiquities communication. In the radios presented in this work, we have performed highly efficient circuit and system design techniques to realize a balanced power-sensitivity design and to bridge the gap between long-range LPWAN and ultra-low power radios. As it is highlighted in Figure 1.8, a receiver with a power-sensitivity of around 150μW at -100dBm is presented, that can achieve similar coverage ranges to other LPWAN technologies at a much lower power consumption.

1.6.2. AFE Design Tradeoffs

As mentioned earlier in the discussion about power in wireless sensor nodes, to ensure a long lifetime for IoT devices without battery replacement, having an ultra-low power analog front-end amplifier in a sensor read-out circuit is of crucial importance. The accuracy of decisions based on the sensed data, directly depends on the performance of the front-end amplifier. One of these main performance metrics for a sensor read-out circuit is the overall noise performance which is typically dominated by the AFE. For a given amplifier topology, there exists a fundamental tradeoff between power and noise. Therefore, to achieve a better noise performance, amplifiers often consume a sufficiently large amount of power. In addition, the amplifier power does not decrease with technology scaling, as it is noise limited rather than technology limited.

Recent advancements in state-of-the-art self-powered systems, such as [1.9], have demonstrated sub-µW operation for these systems. This highlights the requirement for <100 nW AFEs. However, targeting low absolute power often results in poor noise performance. Figure 1.9

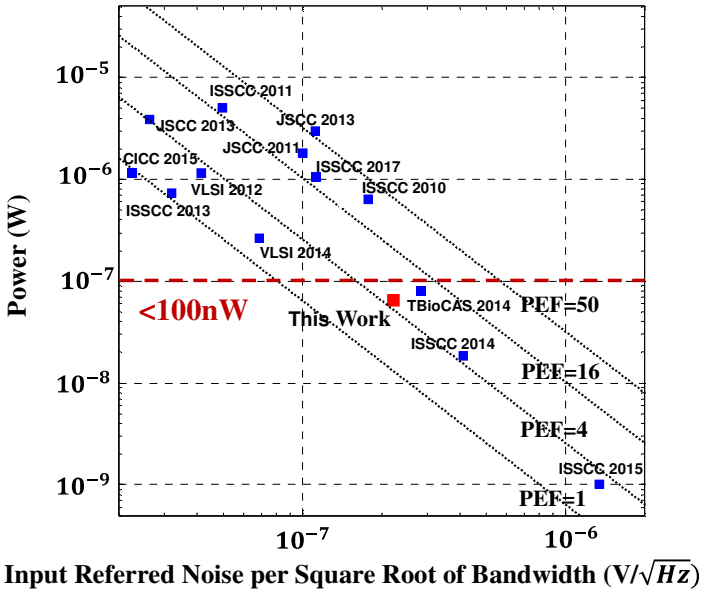


Figure 1.9. Power efficiency comparison between this work and other state-of-the-art works in PEF contours. [1.20].

presents a comparison of power consumption versus root mean square (RMS) input-referred noise per square root of bandwidth for the recent state-of-the-art signal acquisition systems, and shows the power-noise tradeoff for these front-ends. As shown in the plot, the majority of signal-acquisition systems, sacrifice power to achieve a better noise performance or vice versa. Note that constant power efficiency factor [1.21] (PEF) contours are shown on the plot.

In order to enable large utilization of IoT sensors, there is a need for ultra-low power AFEs with less than 100 nW power consumption with low noise performance. As shown in Figure 1.9, an AFE is developed in this work which sits between ultra-low power and high performance AFEs in order to bridge this gap.

1.7. Contributions

As we move towards ubiquitous deployment of IoT devices and in order to enable 50 billion connected nodes as predicted by technology leaders, ultra-low power consumption of wireless sensor nodes becomes critical. However, low power approaches in wireless integrated circuit design often result in sacrificing the performance, such as noise, receiver sensitivity, transmitter efficiency, etc. which is not desirable for many IoT applications. To mitigate these challenges, this thesis presents innovative low power system and circuit design techniques that bridges the gap in performance in wireless sensor nodes to ultra-low power consumptions for future IoT applications.

1.7.1. Multi-Use Radio Service Band for Long-Range Communications

As discussed earlier, with the rapid growth of IoT applications requiring long-range data transmission, LPWAN technologies are attracting a lot of attention. However, enabling communication ranges on the order of tens of kilometers by using ultra-low power wireless nodes

is very challenging. In order to address the ultra-low-power requirement and conflicting challenges of LPWAN, we introduce a narrowband transmission scheme along with a system level design and link budget analysis in the MURS band as a long range and low-power alternative system wireless link demonstration for the LPWAN IoT applications. Experimental channel and link characterization for the proposed MURS band system architecture for LPWAN long-range scenarios has also been performed.

1.7.2. Ultra-Low Power Long-Range Receiver

As seen from the low power radio survey in Figure 1.8, most receiver's that are intended for long-range applications are high power with power consumption values greater than 1mW. Therefore, for energy-constrained applications there is a need for ultra-low power radios that enable long distant communications. To this end, we have developed a receiver system architecture and low power RF circuit design techniques to allow ultra-low power consumption for kilometer range applications. In Chapter 2, a 152 μW Multi-Use Radio Service (MURS) band receiver is presented that addresses the low active power, high sensitivity, and interference rejection challenges and requirements of LPWAN radios. The RX achieves a sensitivity of -99 dBm at 5kbps, capable of over 10 km communication.

1.7.3. Ultra-Low Power Long-Range Transmitter

Similar to receivers, power is often scarified in transmitters to achieve a better efficiency or a higher data rate. As a solution for IoT long-range connectivity, an efficient design for an ultra-low power digital transmitter is introduced and implemented. As mentioned earlier, long-range IoT technologies use low data rate transmission schemes to mitigate the power constraints. We have developed systematic low power design methods both in baseband data generation and RF circuits to enable a lower power consumption while achieving a high efficiency value for the

transmitter. In Chapter 4 we present an ultra-low power digital transmitter that uses our method of class-B I/Q cell sharing in order to deliver a peak efficiency of 41% at a peak output power of 0 dBm at 5 kbps in the MURS frequency channels. It also enables 16QAM OFDM transmission with a data rate of 384 kbps, making it a very suitable solution for remote IoT connectivity in multipath rich environments.

1.7.4. Ultra-Low Power ECG Monitoring Analog Front-End

As it was shown in the power breakdown of Figure 1.7, the ultra-low power consumption of AFEs is essential for organic growth of WSNs. However, low absolute power often results in poor noise performance in AFEs, as shown in the plot in Figure 1.9. In Chapter 5 we present an ultralow power low-noise AFE that meets the requirements of ultra-low power energy-harvesting physiological sensors. The AFE uses low-noise and low-power circuit design methodologies and aggressive voltage scaling to satisfy both the low power consumption and low input-referred noise requirements of ECG signal acquisition systems. We show the feasibility of <100 nW AFE for continuous ECG monitoring applications. The low-noise 68nW AFE was also integrated on a self-powered physiological monitoring System on Chip (SoC) that was used to capture ECG bio-signals from human subjects from wet and dry wearable electrodes.

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Chapter 2
Murs Band For Long-Range IoT Communications

As stated in Chapter 1, the four key performance metrics for IoT LPWAN applications are extended range, scalability, low cost, and ultra-low power. This chapter discusses the advantages of MURS frequency band for LPWAN applications and introduces a transmission scheme along with a system level and link budget analysis for the operation on this band as the first demonstration of MURS band potential for LPWAN applications in the literature. Many LPWAN applications such as smart parking, smart agriculture, and smart metering are expected to exchange limited data with low data-rates, and can therefore benefit from operation in the VHF band. VHF band possesses a much better propagation characteristic compared to the higher frequency bands allocated to LPWAN technologies. As an example, according to Hata model [2.1], the path loss (PL) value decreases by about 21 dB when the frequency is lowered from 915 MHz to 151 MHz.

In this chapter the FCC regulations and requirements for operation in the MURS band are discussed. An experimental measurement campaign is carried out in order to analyse the channel characteristics and measure the PL and path loss exponent (PLE) values for different transmission scenarios. We introduce a narrowband transmission scheme in the MURS band as an alternative solution for LPWAN technologies. Finally, a system level and link budget analysis is performed and the proposed long-range transmission scenario in the MURS band is compared with the other LPWAN technologies.

By leveraging ultra-low-power circuit design techniques and low-loss propagation characteristics at the low VHF frequencies, along with the system architecture presented in this chapter, it is shown in the following chapters that we can achieve a significant (90-fold) reduction in the power consumption in our MURS transceiver compared to the existing state-of-the-art commercial solutions, while maintaining similar coverage ranges.

2.1. MURS Frequency Band

Unlike other IoT standards that operate in the already crowded ISM bands, MURS operates in five narrowband channels in the VHF band. The FCC authorizes a maximum bandwidth of

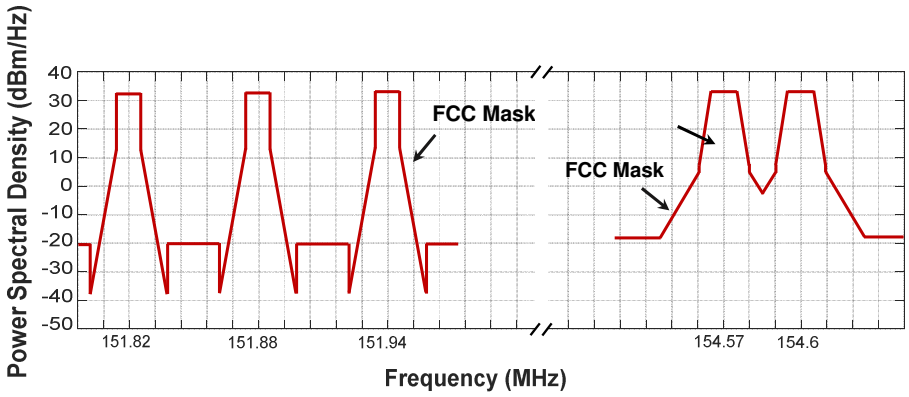


Figure 2.1. FCC spectral mask for 151.82-151.94 MHz, and 154.57-154.6 MHz MURS band channels.

11.25 kHz at 151.820, 151.880 and 151.940 MHz channels, and a maximum bandwidth of 20 kHz at 154.570 and 154.500 MHz MURS channels [2.2]. The FCC allows both data and voice communication in MURS band with a maximum transmit power of 2 watts. The high allowable output power and the ability to use high gain antennas, is an advantage over other long-range IoT technologies. Additionally, there is no legislative requirements for duty cycling the data in this band. The FCC authorized transmission mask for the MURS band is depicted in Figure 2.1.

2.2. Modulation Scheme

For the MURS band long range communication, we propose an adjustable modulation scheme, enabling adaptive modulations [2.3]. It uses single carrier as well as multi-carrier modulations to compensate for multipath events. The single-carrier communication is based on binary phase-shift keying (BPSK) modulation that uses narrowband 10 kHz sub-carriers at any of the MURS channels. By choosing 10 kHz channel bandwidths, we are able to use a total of five channels to transmit a maximum allowable power of 33 dBm at a data rate of 5 kbps per channel. Figure 2.2 shows the channel allocation of the proposed single carrier modulation scheme for long-range low data rate applications.

In order to support bandwidth hungry use cases in dense IoT applications, we have also implemented an orthogonal frequency division multiplexing (OFDM) multi-carrier modulation in the MURS band. The multi-carrier modulation approach is based on compromising the maximum transmitted power with the goal of achieving higher continuous bandwidths for higher data rate applications and be FCC compliant. By utilizing different numbers of contiguous subcarriers in the MURS band, the multi-carrier modulation allows adaptive modulations based on QPSK, 8-

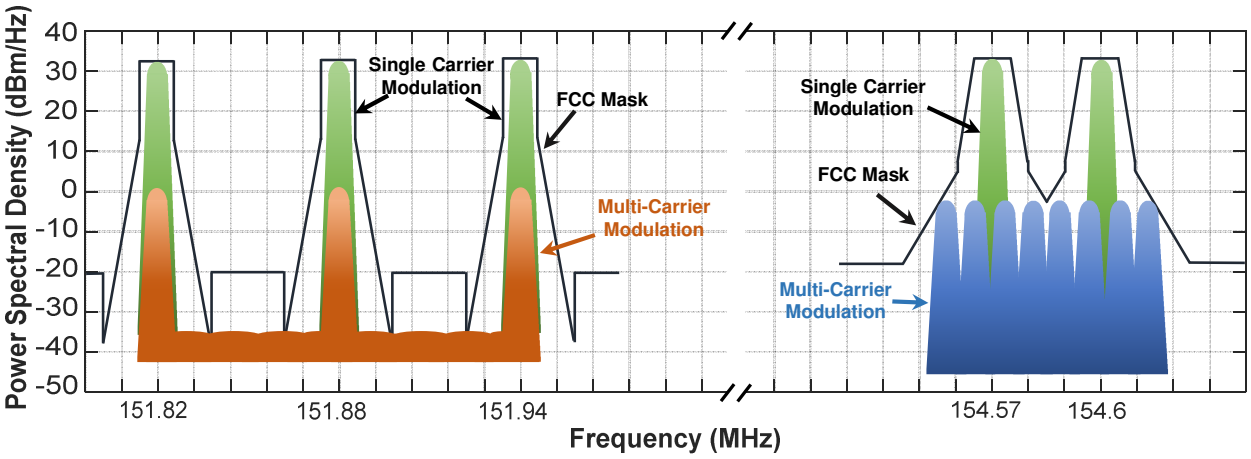


Figure 2.2. Proposed single-carrier and multi-carrier modulation schemes.

PSK, or 16QAM constellations. An example of such multi-carrier modulation over the higher frequency 154.570 – 154.600 MHz MURS band is shown in Figure 2.2, where by lowering the maximum transmit power to -5 dBm, an 8-PSK constellation points can be mapped to 8 subcarriers with a 10 kHz subcarrier spacing. Additionally, the multi-carrier transmission can be realized at higher transmit power values, by using null subcarriers for the intermediate spaces. This is shown as an example multi-carrier transmission over the three over MURS frequencies in Figure 2.2.

By using this selective modulation technique in MURS band, we are able to achieve long-distance communications at agile data rates of 5-384 kbps (assuming a guard time ratio of ¼). The feasible coverage range using the mentioned modulation techniques is described in the section 2.3.

2.3. MURS band Signal Propagation and Path Loss Measurements

In order to study the feasibility of MURS band communication for LPWAN applications, PL characterization of MURS band propagation at various common scenarios, such as smart parking, agriculture, and smart metering, is performed. PL represents the signal attenuation between the transmitted signal power and the received signal power. The well-known Friis free-space equation describes this relation as presented in (2.1):

$$P_r = P_t + G_r + G_t - 20\,log_{10}\left(\frac{4\pi}{\lambda}\right) - 10PLE\,log_{10}(d) \quad (2.1)$$

Where G_r and G_t are the antenna gains at the receiver and the transmitter respectively, λ is the wavelength (1.98 m at 151 MHz), d is the distance between the transmitter and the receiver, and PLE is the path loss exponent. The value of PLE is equal to 2 in free-space and for urban scenarios it typically ranges from 2.5 to 4, due to various phenomena like reflection, diffraction, multi-path induced fading, shadowing, etc.

To measure the PLE for the aforementioned applications, the power level of the narrowband continuous wave (CW) received signal at 151MHz is measured and the PLE value is extracted from (2-1). Due to multi-path fading, the narrowband received power fluctuates over a small area. In order to mitigate the effect of multi-path fading, the received signal power needs to be averaged along several wavelengths on a linear track for a reliable estimate of the local average power [2.5-2.6]. In the measurement campaign in this work, PL from outdoor base stations to external receivers placed at various locations around the campus is measured for two different indoor and outdoor scenarios. The following sections describe the methodology for measuring PL and PLE as well as descriptions of measurement procedures, sites, and hardware.

2.3.1. Measurement Equipment and Setup

The measurement setup consists of a receiver and a transmitter implemented using universal software radio peripherals (USRP) N210, with WBX USRP daughterboards to generate and receive MURS band signals in the 151 MHz frequency band, as shown in Figure 2.3. The USRPs are connected to omnidirectional, loaded, quarter wavelength antennas (EXR150) with a gain of about -2 dBi and the antennas are tuned to achieve better than 15 dB of measured return loss at the 151 MHz MURS channel. The transmitter power has been adjusted to deliver 21 dBm to the antenna and a laptop computer was used to record the power samples received at the receiver.

Before initiating measurements at each of the measurement sites, calibrations were performed, where the transmitter and the receiver were connected back to back using a calibrated cable bypassing the antennas in order to calculate the overall system gain and installation losses.

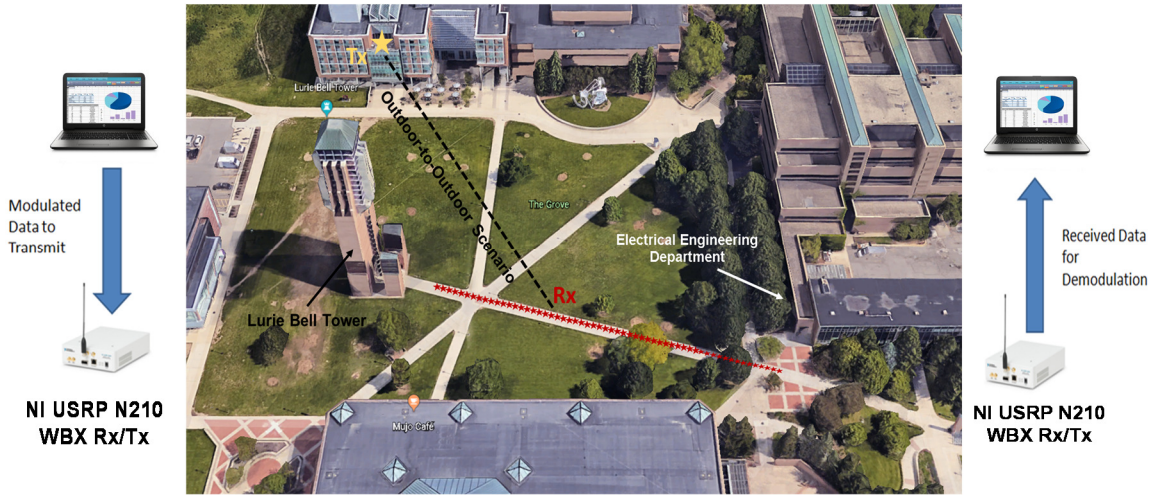


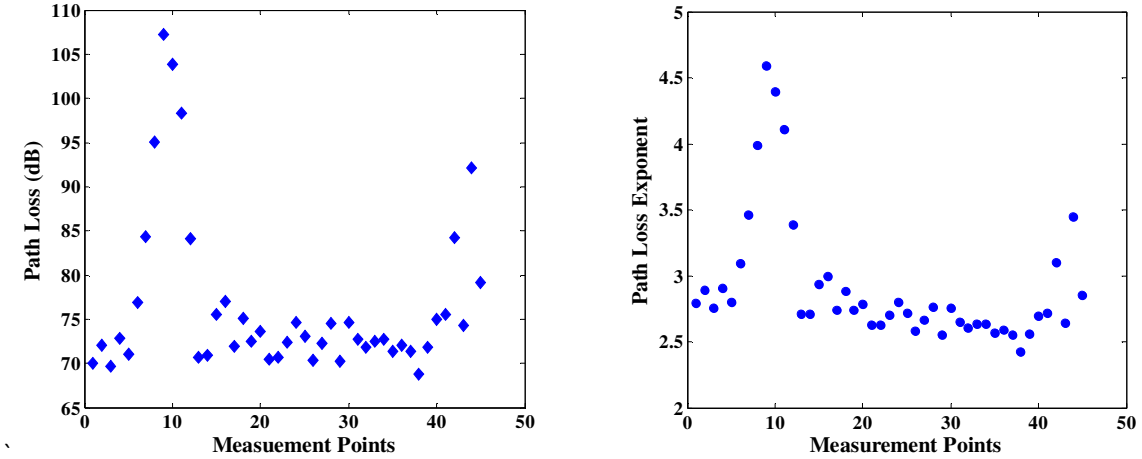
Figure 2.3. Outdoor-to-Outdoor measurement scenario and measurement equipment.

2.3.2. Measurement Procedure

In order to characterize the PL properties for the stated applications in the MURS band, the measurements are performed in two different scenarios, namely, (a) outdoor-to-outdoor propagation, and (b) outdoor-to-indoor propagation scenario.

The outdoor-to-outdoor scenario represents typical smart parking or smart agriculture applications where the base station is positioned on a tower and the ground-level sensors are placed within the coverage area of the tower. In this measurement the transmitter is placed at a fixed location 11 m above ground, illuminating the north campus area at the University of Michigan. The CW received power was collected as the receiver (at 1 m above ground) was moved along the 50λ long track for 45 measurement points (Figure 2.3), and at every location the received power is averaged over 500 cycle of the signal. Figure 2.4 shows the measured PL and PLE associated with the CW received power at the 45 measurement points. As shown, for the measurement points nearby large obstacles, such as those near the Lurie Bell Tower and the Electrical Engineering Department, there are higher fluctuations in the measured received power and therefore PL. These

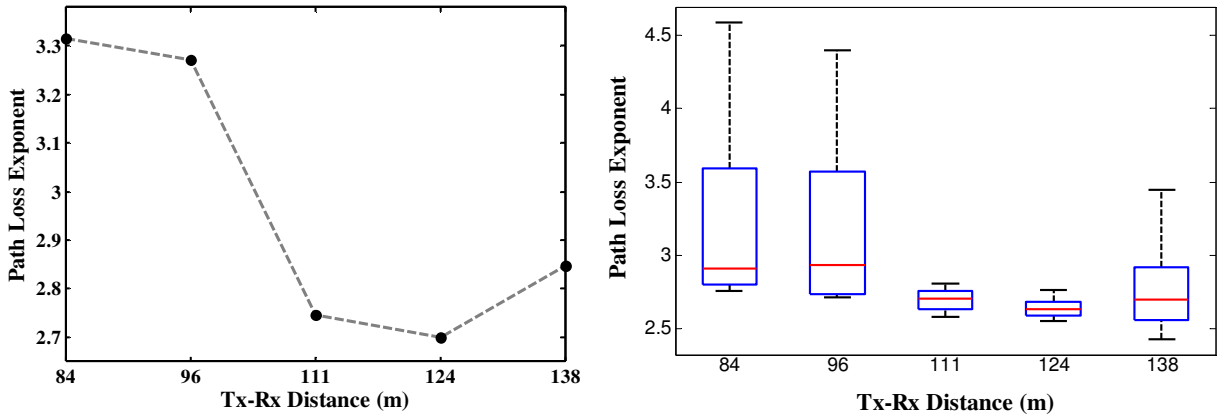
points correspond to the two ends of the measurement track, and are caused mainly due to the fading from these obstacles.



(a) (b)

Figure 2.4. (a) PL (b) PLE measurements for outdoor-to-outdoor measurement scenario

As mentioned before, in order to eliminate the effect of multi-path fading, the received power collected along the linear path has been averaged over every 10λ distanced measurements. Figure 2.5 presents the average path loss exponents measured over the aforementioned test scenario. Based on these measurements, the MURS band propagation exhibits an average PLE of



(a) (b)

Figure 2.5. (a) Averaged PLE for selected distances for outdoor-to-outdoor scenario, (b) PLE distribution representation using box and whisker plots

2.9 with a standard deviation of 0.3 for outdoor-to-outdoor communication scenarios in environments similar to university campuses.

The second measurement scenario is the outdoor-to-indoor scenario representing typical smart metering applications. In these applications the meters are often placed underground or inside buildings and the base stations are usually located outdoors on street-level mountings such as building rooftops or street lamps. Since the wireless sensors are placed indoors or underground for these applications, the system experiences more attenuation due to building penetration and installation losses.

In our measurements we have positioned the transmitter outside of the Electrical Engineering Department (1 m above ground), as shown in Figure 2.6, and the receiver is placed in the basement of the Automotive Engineering Lab. Similar to the outdoor-to-outdoor scenario, the

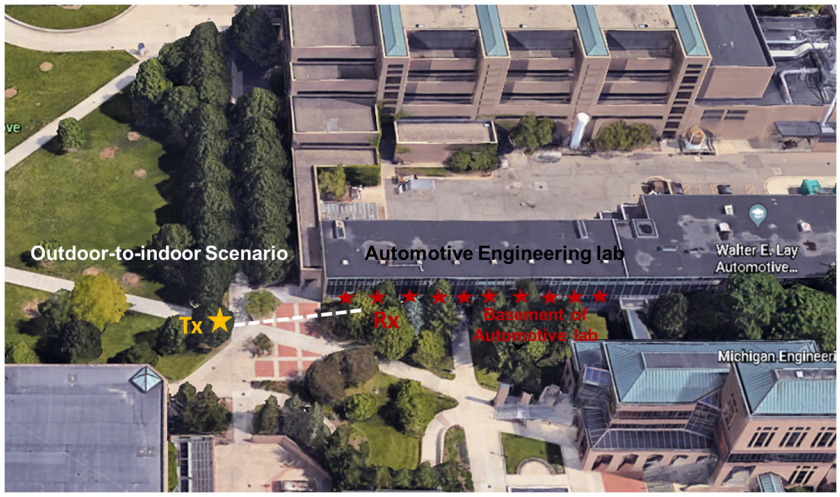


Figure 2.6. Outdoor-to-Indoor measurement scenario

	Mean	Standard Deviation
PL (dB)	77.8	1.7
PLE	4.7	0.12

Table 2.1. Measured mean value and the standard deviation value for PL and PLE for outdoor-to-indoor scenario.

received power is measured at several adjacent locations in the basement with 1λ displacement, and the received power values have been averaged accordingly in order to mitigate the fast-fading effects. Table 2.1 summarizes the measured PL and PLE for this scenario, where a PLE of 4.7 is reported.

2.4 Link Budget and System Level Analysis

In this section we discuss the link budget and system level analysis and considerations for the proposed MURS band communication method. Many of LPWAN applications such as smart agriculture, smart cities, and smart metering, require long km-range communications. To this end, existing LPWAN technologies often use a high uplink transmit power (>13dBm) and high receiver sensitivity values of around -140 dBm in downlink to achieve such communication ranges. These performance metrics result in a high power consumption in the RF front-end of sensor nodes and are not suitable for ultra-low-power (ULP) or battery-less wireless sensors in ULP IoT applications [2.4]. In this work, our goal is to achieve a similar coverage range to other LPWAN solutions at a much lower active power consumption of <1 mW for the sensor nodes. In order to achieve this goal, a link budget analysis is performed and by utilizing the experimental propagation loss parameters discussed in the previous chapter as well as Hata empirical PL model [2.1], the required specifications for the TX and RX power and sensitivity values are derived and proposed.

In this work we assume that the sensor nodes only communicate with the base stations, and hence forming a star network. In a star topology, the sensor nodes do not need to listen to other devices that want to relay their traffic through them which results in significant energy savings. For long-range IoT applications in the MURS band using single carrier BPSK and multi-carrier OFDM modulations, we aimed at achieving >1 km communication ranges. By using the average PLE value (~2.9) extracted from our outdoor-to-outdoor measurement scenario, a maximum

coupling loss (MCL) of over 100 dB is required to achieve this coverage range. MCL is a metric chosen by 3GPP [2.7] to evaluate coverage of a radio access technology. Coupling loss is defined as the total channel loss over the transmission link between the TX and RX antenna ports, and it includes antenna gains, path loss, shadowing, etc. MCL is the limit value of the coupling loss at which the system can tolerate and still be operational (defined by a minimum acceptable received power level). The calculation for the MCL value is described in more details in Table 2.2.

The uplink (UL) and downlink (DL) chains for the MURS communication are designed in order to satisfy the FCC requirements and enable a low power and multi data rate long-range communication. As shown in Table 2.2, in the DL chain, the base station only transmits using the single-carrier modulation over 10 kHz channels, and in the UP chain the sensor nodes can transmit using either single carrier or multi-carrier modulation with 10-160 kHz bandwidths and lower transmit powers to satisfy the FCC allowable transmit power.

The link budget analysis for the aforementioned transmission modulations and the target coverage range is presented in Table 2.1. MURS sensor node transceivers in the uplink chain can transmit output power levels of less than 0 dBm and in the DL chain a RX sensitivity of -100 dBm is required for the single-carrier mode. The MURS base stations, on the other hand, have a transmit power of 33 dBm in the DL channel, and a required sensitivity value of -120 dBm in the UL. Based on the link budget analysis summarized in Table 2.2, we achieve a MCL of 133dB and 120 dB in the DL and UL, for the single carrier mode respectively. Similar calculations are performed for the multi-carrier mode and are presented in detail in Table 2.2.

The maximum achievable coverage ranges for the proposed transmission link in the MURS band is calculated using the measured average PLE of 2.9 and are listed in the table. As discussed in section 2.3 the TX antenna height was at 11 m above ground and the measurements were

Technology	**MURS LPWAN**	
UL/DL	UL	DL
Data rate (kbps)	5-384	5
Modulation	BPSK→OFDM 16QAM	BPSK
Transmitter		
(1) TX Power (dBm)	**0 → -20**	**33**
Receiver		
(2) Thermal noise (dBm/Hz)	-174	-174
(3) RX noise figure (dB)	3	20
(4) Channel bandwidth (kHz)	10 → 160	10
(5) Effective noise power (dBm)		
= (2) +(3) + 10log((4))	-131 →-119	-114
(6) Required SINR (dB)	9→17	9
(7) Implementation loss & margin (dB)	2	5
(8) RX sensitivity		
= (5) + (6) + (7) (dBm)	**-120 → -100**	**-100**
MCL= (1)- (8) (dB)	**120 → 80**	**133**
Coverage Range (km)		
Hata Model	**Rural: 11 → 1** Urban: 2 → 0.2	**Rural: 25** Urban: 5
Experimental, PLE= 2.9	**4 → 0.2**	**11**

Table 2.2. Link budget for MURS LPWAN.

performed at the UMich north campus area which can be viewed as a suburban environment. The coverage range is also calculated using the Hata model PL formulation, for comparison where an antenna height of 30 m is considered for these calculations. As shown in Table 2.2 we have calculated the coverage radius to be 11 km and 4 km at 5 kbps for the UL and DL chains, respectively and by considering a PLE of 2.9.

Table 2.3 summarizes the MURS band performance and presents a comparison with the state-of-the-art LPWAN sensor nodes. As described in Table 2.3 by utilizing the MURS transmission scheme, and the system level design in this chapter we present an alternative solution for large scale IoT connectivity that can achieve km-range communications with lower required

LPWAN Technology	SIGFOX [2.8]	LoRa [2.9]	NB-IoT [2.10]	Weightless-P [2.11]	MURS
Freq. (MHz)	868/ 902	433/868/915	850/900	Sub-GHz ISM	151/154
Licensed	No	No	Yes	Yes/No	No
Modulation	UNB (DBPSK)	CSS/FSK	OFDMA/ SC-FDMA	GMSK/PSK	OFDM/ BPSK
Data rate(kb/s)	0.1	0.3-37.5	20-250	0.2-100	5 -384
Coverage (km) **Rural** **Urban**	30-50 3-10	10-15 3-5	10-40	- 2	1-25 0.2-11
TX P_{out} (dBm)	14	13	23	17	0
RX Sensitivity (dBm)	-134	-138	-141	-128	-100

Table 2.3. MURS long-range connectivity comparison with other LPWAN technologies.

receiver sensitivity and transmitter output power which significantly reduces the power consumption in the sensor node. In accordance to the presented link budget analysis and in order to show the feasibility of ULP transceivers for long range communications, we have implemented a MURS band transmitter and a receiver that are discussed in Chapter 3 and Chapter 4 respectively.

2.5. Summary

A MURS band transmission scheme in support of the low power and long-range communication for LPWAN applications is presented. An agile modulation approach at the low VHF frequency of MURS band is introduced, where adjustable data rates of 5-384kb/s with a coverage range of tens of kilometers is achieved. An experimental work aiming at PL and channel characterization in the MURS band was performed which was used for the system level and link

budget analysis in the MURS band. The link analysis presented in this chapter is the first demonstration of MURS band communication for LPWAN as an alternative solution for battery-less long range IoT applications.

Chapter 2: References

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Chapter 3
Ultra-Low Power Long-Range Injection Locked Receiver

The rapid growth of IoT applications requiring long-range data transmission is leading to the prosperous development in long distance wireless communication systems. Different standards are being proposed in sub-GHz bands which target narrowband, low data-rates, and long-range connectivity for low-power IoT applications [3.1-3.3]. As stated in the Introduction Chapter, RF transceivers are considered to be energy bottlenecks in a wireless sensor node, and there are several challenges to overcome before sensor nodes can be deployed ubiquitously as ultra-low power solutions for massive IoT applications.

The tradeoff between power and sensitivity was discussed in Chapter 1, highlighting the high power consumption of long-range receivers. In this chapter, we present a 152μW MURS band receiver addressing the low active power, high sensitivity, and interference rejection challenges and requirements of LPWAN radios. By utilizing an optimized system architecture and low power circuit techniques, we were able to demonstrate the capability for long-range communications at a much lower power consumption. The receiver operates at the FCC compliant MURS band at 151-154MHz, which exhibits lower path-loss and building penetration loss compared to other higher frequency bands used for LPWAN applications, as discussed in Chapter 2. The BPSK/16QAM OFDM receiver (RX) is data rate agile and suitable for remote IoT connectivity in multipath rich environments. The RX achieves a sensitivity of -99dBm at 5kb/s, capable of over 10 km

communication. This is enabled by a power efficient RX architecture, shown in Figure 3.1, and several low power design techniques, including a dual intermediate frequency (IF) RX architecture using passive multipliers, an edge combiner sub-harmonic mixer first architecture which enables the operation of the frequency synthesizer at a much lower frequency, injection locked local oscillators (LOs) which enable more energy efficient frequency generation compared to PLLs, and efficiently distributing the gain and noise performance requirements in the RF and IF blocks. The RX achieves a -128dBc/Hz phase noise (PN) at 1MHz offset for the LO and realizes a blocking rejection of 48dB and 63dB at 2MHz and 10MHz offsets, respectively.

3.1. System Architecture

The RX operates in two modes of single-carrier and multi-carrier transmission and is designed with the goal of achieving a similar coverage range to LPWAN technologies at a much lower power consumption. As discussed in Chapter 2, the MURS band single-carrier transmission scheme is based on 5kb/s BPSK modulation with 10 kHz channel bandwidth (BW), and 60 kHz channel spacing. Based on our link budget analysis and Hata model, for the RX sensitivity of -100 dBm (sensor node) and an uplink power of 33 dBm (base station), we can achieve a communication range of over 20 km. For higher data-rate applications in denser environments, an OFDM modulated multi-carrier transmission scheme is utilized, which uses 16-QAM on 16 subcarriers with 10 kHz subcarrier spacing. The multicarrier modulation symbols have a symbol duration of 125μs with a data rate of 384kb/s.

To achieve the low power consumption requirements of IoT transceivers along with the specifications for the proposed transmission scheme, a mixer-first injection locked dual IF RX architecture is employed [3.4], as shown in Figure 3.1. Achieving maximum sensitivity at low

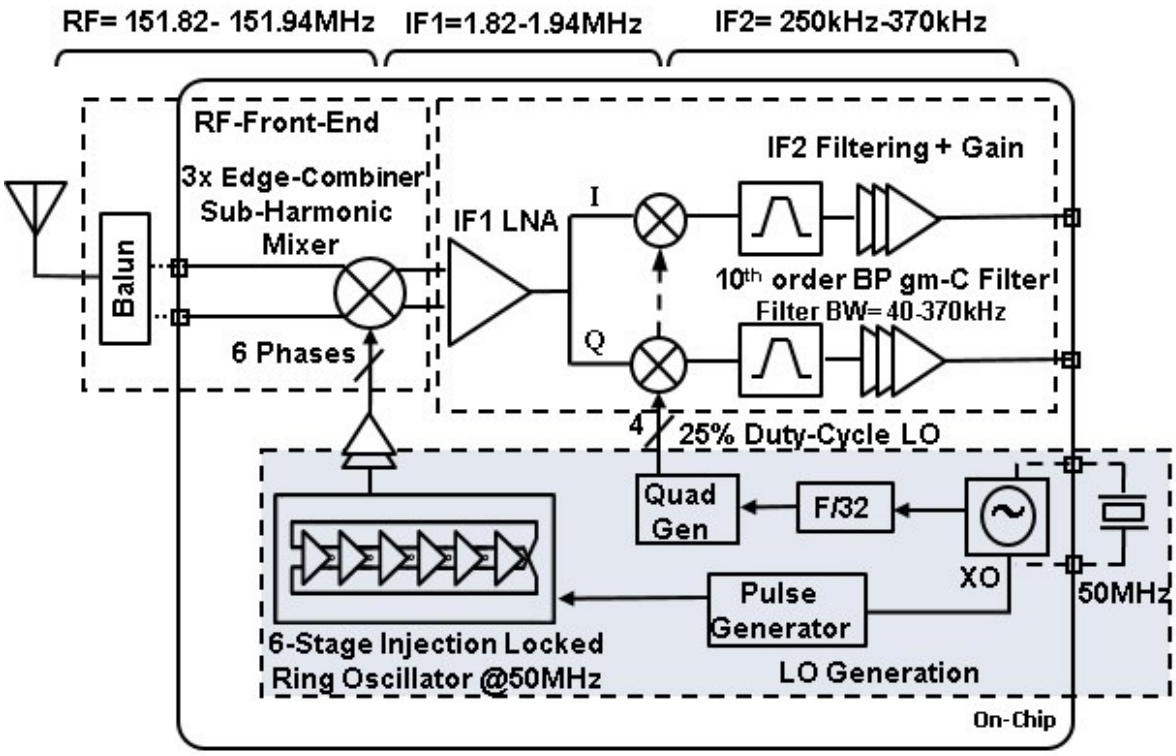


Figure 3.1. Block diagram of the receiver.

current levels is a major challenge. This is enabled by two major considerations in the system-level design of the RX architecture. 1) The dual IF, sub-harmonic mixer-first architecture is chosen in order to transfer the high dynamic range and hence gain requirements of the RX to the baseband blocks as well as shifting the dual I/Q paths to the lower IF frequency where the power consumption is minimized. In addition, due to the very low IF in the second IF stage (250–370 kHz), the dynamic range and complexity of the required analog to digital converter (ADC) is highly relaxed. 2) The LO frequency generation, which is often the most power hungry block in a RX, is implemented by an injection locked frequency synthesizer at 50MHz, and therefore down-conversion is performed by a 3x sub-harmonic edge-combiner passive mixer. This also enables us to achieve the required PN at a much reduced power.

As shown in Figure 3.1, the edge combiner at the input of the receiver is driven by three-phase differential LOs from the injection-locked ring oscillator (ILRO) and is followed by a low-noise amplifier (LNA) at the first IF frequency (IF1), 1.82–1.94MHz, providing 25dB of gain in the first down-conversion step. This is loaded by a quadrature passive mixer driven by 25% duty cycled LOs that are directly driven from the divide-by-32 divider from the on-chip crystal oscillator operating at 50MHz. The second mixers are then followed by very low IF (IF2) 10th order bandpass filters providing 20–54 dB of gain and a tunable bandwidth (BW) of 40–370 kHz. All the blocks are AC coupled to reject DC off-sets.

3.2. Design Implementation

3.2.1. RF Front-End

Figure 3.2 represents the RF front-end of the receiver. We have used an on-chip differential double balanced edge-combining sub-harmonic mixer at the input of the RX to save power and reject LO feedthrough due to the presence of random mismatches in the LO phases in the IF signal. An off-chip balun is used for impedance matching to the 50Ω source and single to differential

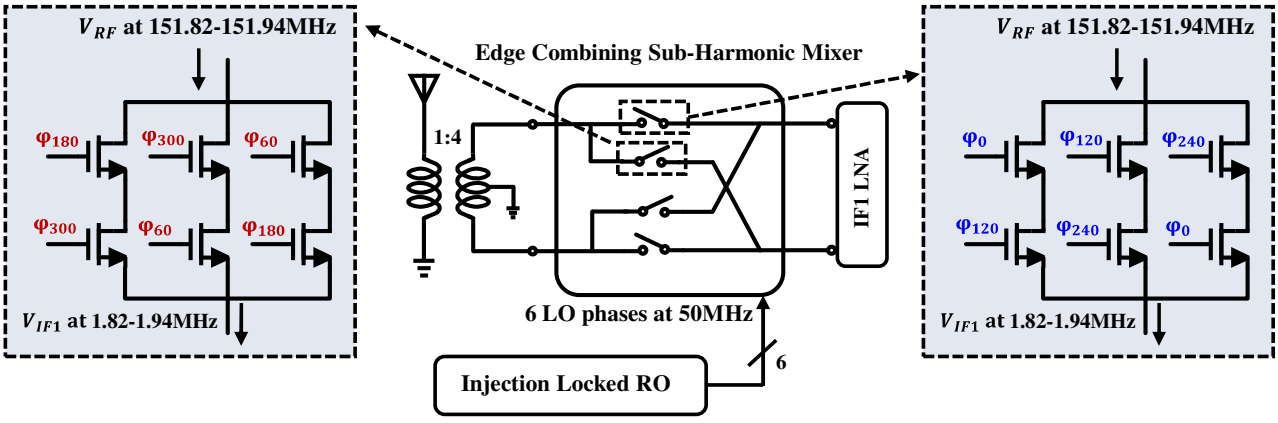


Figure 3.2. RX RF front-end.

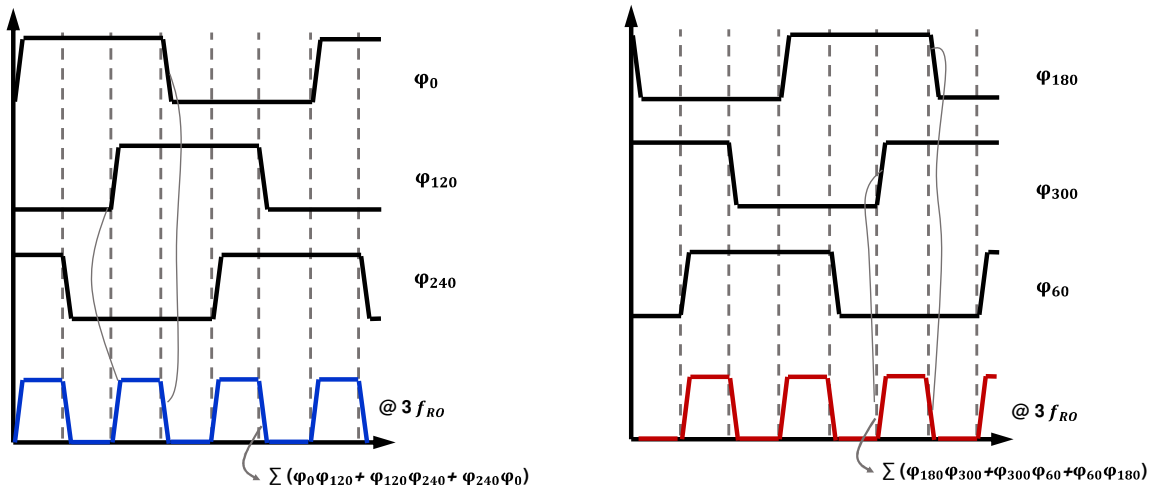


Figure 3.3. Double balanced edge-combining mixer's waveforms.

conversion. The six differential three-phase LO signals driving the edge-combiner are fed by the ILRO operating at 50MHz and are phase shifted by 120°.

The performance principle of the edge combining passive mixer is shown in more details in Figure 3.3. Signals φ_0, φ_{120}, φ_{240} and φ_{180}, φ_{300}, φ_{60} represent the waveforms from the differential ILRO running at frequency f_{RO} (50 MHz) and the waveforms $\sum(\varphi_0\varphi_{120}+\varphi_{120}\varphi_{240}+\varphi_{240}\varphi_0)$ and $\sum(\varphi_{180}\varphi_{300}+\varphi_{300}\varphi_{60}+\varphi_{60}\varphi_{180})$ are square waveforms of frequency $3f_{RO}$ (150 MHz) that show the multiplication factor of 3 for the edge-combining mixer. As shown in Figure 3.2, the voltage mode edge-combiner is realized by NMOS transistor switches to perform an AND operation on the LO waveforms in each branch and an OR operation to select one of the non-overlapping down-converted signals in each of the three main branches. Overall, the network of 24 NMOS switches, resembles a passive double balanced mixer comprising 4 combined switches operating at 3×LO frequency or 150MHz. The effect of the systematic phase error of injection locking on the output of the sub-harmonic mixer is carefully simulated and discussed in the next section.

3.2.2. Injection-Locked Frequency Synthesizer

As shown in Figure 3.4, the injection locked ring oscillator (ILRO) at 50MHz is implemented by a six stage differential ring oscillator directly locked to an on-chip reference crystal oscillator (Figure 3.4), providing the six output phases from three differential outputs. Injection locked systems behave like a first order PLL, and by eliminating the loop filter components it provides a much better energy efficiency as well as a good phase noise performance. In addition a lower power reduced phase noise ring oscillator can be tolerated, as the ILRO phase noise follows its injected reference in the locking condition.

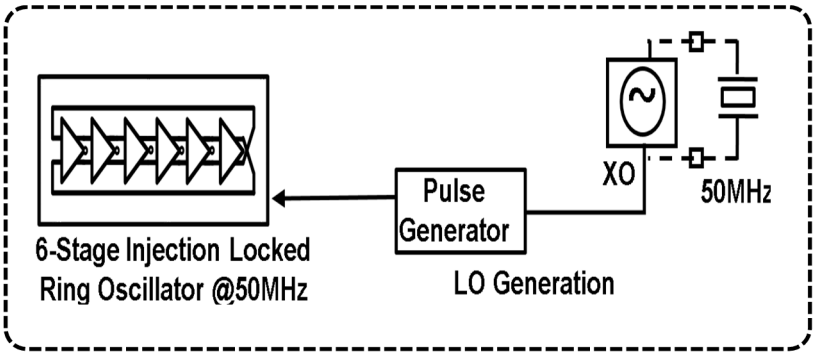


Figure 3.4. Injection locked LO generation blocks including the 6-stage RO and RO delay Pulse generator and 50 MHz crystal oscillator.

The schematic of the crystal oscillator (XO) is shown in Figure 3.5(a). An off-chip crystal is used and an inverter with a resistive feedback is utilized as the primary amplifier. Additionally, similar to the XO architecture in [3.5] a feedback path is employed to starve the primary amplifier until it settles to a measured power consumption of 29μW. Initially the transconductance of the primary amplifier is greater than the critical transconductance of the crystal, however, as the oscillation starts and the amplitude increases, the DC level of the oscillation drops which is used

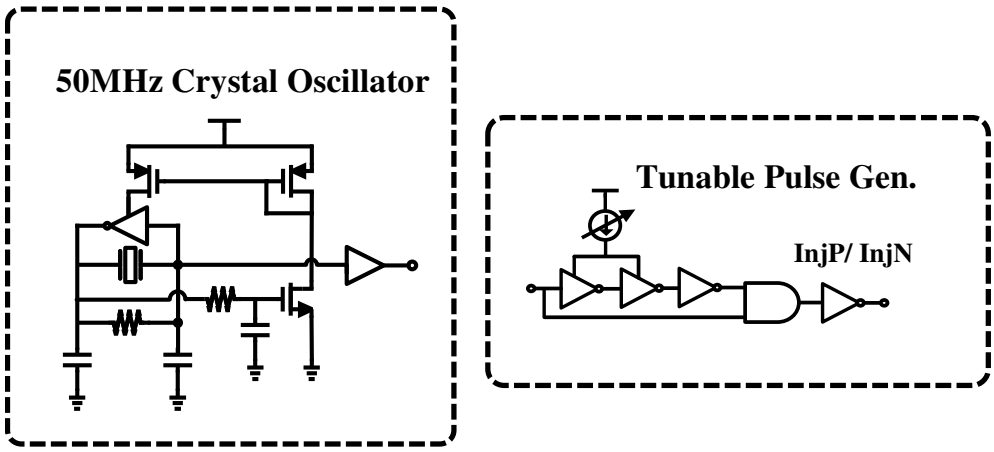


Figure 3.5. (a) Schematic of the crystal oscillator, (b) Block diagram of the tunable pulse generator.

in feedback to starve the amplifier until it settles to 32μA and sustaining oscillation. The oscillation is then buffered to a tunable pulse generator to provide the injection signals to the RO.

The tunable pulse generator shown in Figure 3.5(b) is implemented by an AND operation on the reference signal and tunable delayed versions of the reference. It outputs programmable pulse width signals, Inj_P and Inj_N, to tune the locking range and ensure that the pulse width of the injected signals is smaller than half of the crystal oscillator period. The injection differential pulses drive M_1 and M_2 transistors and short the differential output of the RO, as shown in Figure 3.6.

Since the injection often only happens in the first stage of the RO, ILRO systems have a systematic phase mismatch between the stages which leads to spurs occurring at LO frequency in the frequency multiplied signals in the IF stage of the receiver [3.6]. One method to reduce the phase error is to use a multiphase injection locking [3.7]. However, the additional RO that is required in multiphase injection locking systems increases the power consumption.

In order to minimize the effect of this systematic phase error on the receiver's overall performance, we first derive the relations for the output phases of the RO. The free running RO in

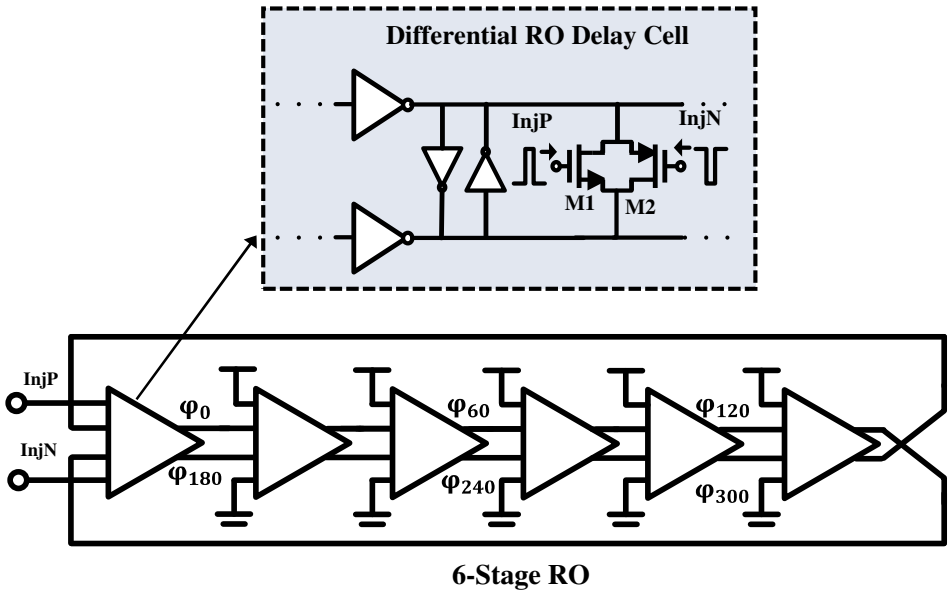


Figure 3.6. Differential RO and the RO delay cell.

Figure 3.6 oscillates at the frequency $f_{RO} = \frac{1}{T_{RO}} = \frac{1}{2t_d \times 6}$ where t_d is the propagation delay time of each stage. Therefore every two stages of the 6-stage RO provides a phase delay of:

$$\theta_{RO} = \frac{2\pi(2t_d)}{T_{RO}} = \frac{\pi}{3} \tag{3.1}$$

When the injection happens the RO locks to the frequency of the injection signal (f_{inj}). However, since the injection only happens in the first stage of the RO, it results in a phase error in the generated output phases of the following stages. As an example, the delay between φ_{60} and φ_{120}, in Figure 3.6, is:

$$\theta_{ILRO} = \frac{2\pi(2t_d)}{T_{inj}} = 2\pi f_{inj} \times \frac{1}{6f_{RO}} = \frac{\pi}{3} + \frac{\pi}{3}\frac{(f_{inj} - f_{RO})}{f_{RO}} \tag{3.2}$$

Therefore, based on (3-1) and (3-2), the systematic phase error in the ILRO is proportional to the frequency difference between the free running RO (f_{RO}) and the injected signal (f_{inj}), and the phase error between every two stages in the 6-stage ILRO in this work and can be written as:

$$\theta_{error} = \frac{\pi}{3}(f_{RO} - f_{inj})/f_{RO} \tag{3.3}$$

This systematic phase error was simulated with the edge combiner mixer to ensure the LO feedthrough is small enough and can be filtered by the baseband filters. For this reason an 8-bit current DAC is used to tune the RO frequency and minimize the effect of the phase mismatches on the receiver performance. This eliminates the use of multiphase injection locking techniques and therefore, saves power.

3.2.3. First Intermediate Frequency (IF1) Stage

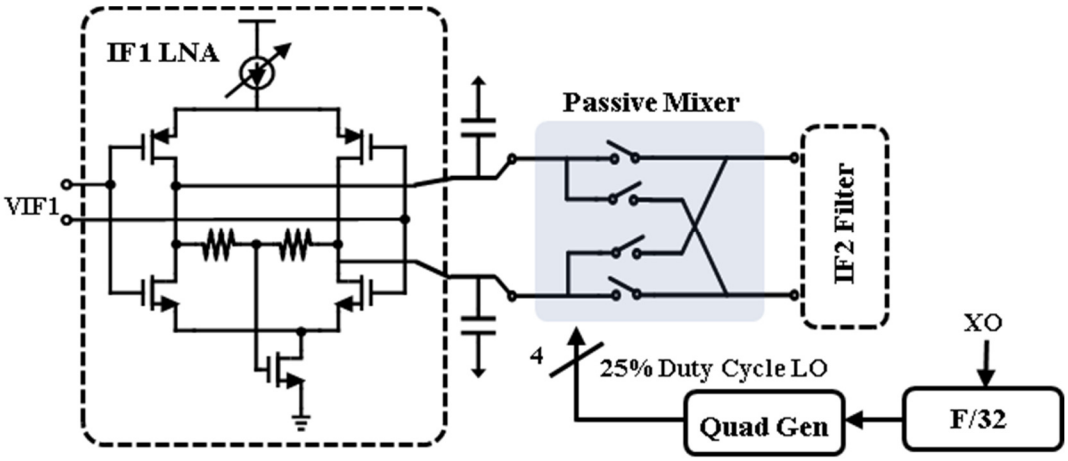
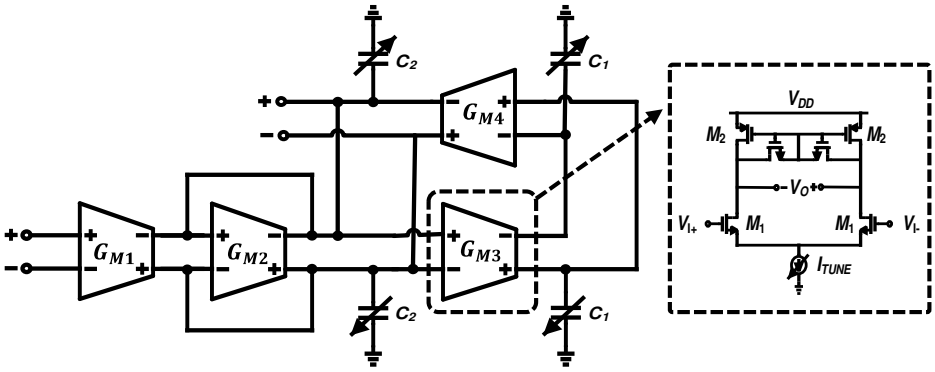


Figure 3.7. IF1 stage and schematic of IF1 LNA.

As shown in Figure 3.7, an inverter based topology is used for the IF1 LNA for gain and noise efficiency. Common mode feedback is provided by both the pseudo resistors and the bottom NMOS transistor, guaranteeing the output common mode stay at half V_{DD}. Since the input impedance of the LNA directly affects the receiver's input impedance and therefore noise performance through the passive mixers, the LNA's input devices as well as the tail currents are adjusted to match the desired noise level. The outputs of the LNA are directly loaded by a quadrature passive mixer driven by 25% duty cycled LO signals. The LO signals, are generated by a divide-by-32 divider driven by the XO. This further down-converts the signal for an optimum power consumption as well as a good blocker rejection performance.

3.2.4. Second Intermediate Frequency (IF2) Stage



(b)

Figure 3.8. Block diagram of a single stage of IF2 10th order filter.

In order to enable the targeted specifications for MURS communication, a 10th-Order Chebyshev-I bandpass g_m-C filter is designed. The filter is implemented using five cascaded biquad stages. Each of the biquad stages provide a 1st-order high-pass and low-pass response with programmable pole frequency, quality factor, and gain, as shown in Figure 3.8. In order to achieve a broad tuning range, both g_m and capacitors of each stage are designed to be tunable. The g_m variation of the G_m-cells, often causes a significant change in DC operating points. Therefore, in order to prevent DC operating point variations, and maximize the tuning range simultaneously, self-biased differential G_m-cells are used in the biquad stages. The programmability feature enables the filter to create a Chebyshev response or Bessel with different band widths, making the receiver reconfigurable for different modes of operation. The filter has two modes of operation, one providing higher measured gain of 20–54dB and a BW of 40kHz for BPSK operation mode. The other mode provides a lower gain of 20–32 dB, but higher BW from 170–370 kHz for OFDM mode of operation with higher data rates. The devices in the IF2 stages are optimally dimensioned to reduce the flicker noise. The differential filtered IF2 signals are fed to an off-chip 5MS/s ADC for digitization and baseband processing.

3.3. Measurements

The RX was fabricated in a 40nm CMOS process and packaged in a 6×6mm QFN40 package. The RX core blocks, not including the I/O pads, occupy an area of 0.17mm^2. Figure 3.9 shows the die photo of the receiver. The power spectral density of the locked and unlocked RO and the phase noise of the free-running RO, XO and ILRO are shown in Figure 3.10 and 3.11,

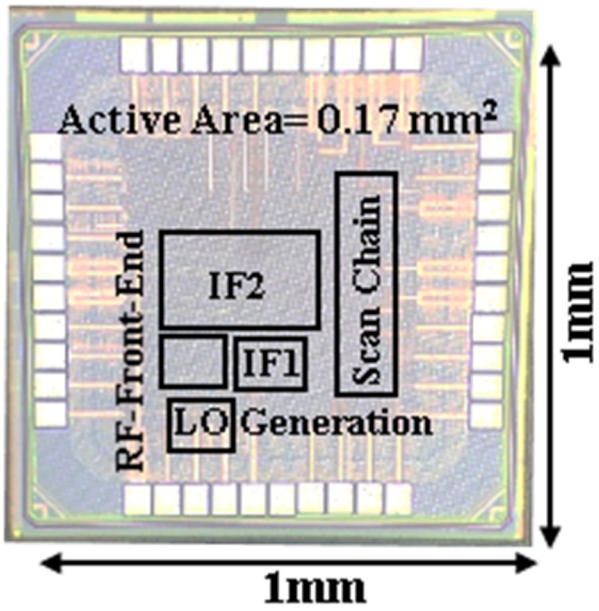


Figure 3.9. Die micrograph of the RX.

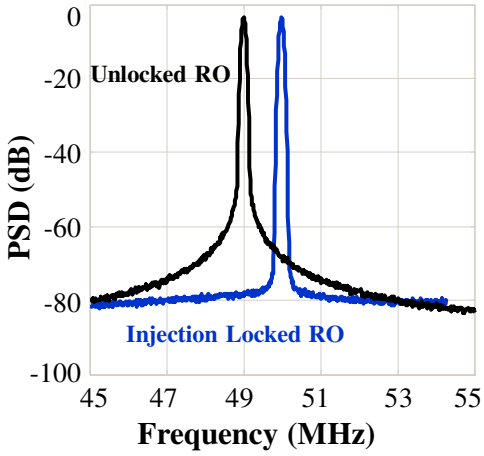


Figure 3.10. Unlocked and locked RO PSD.

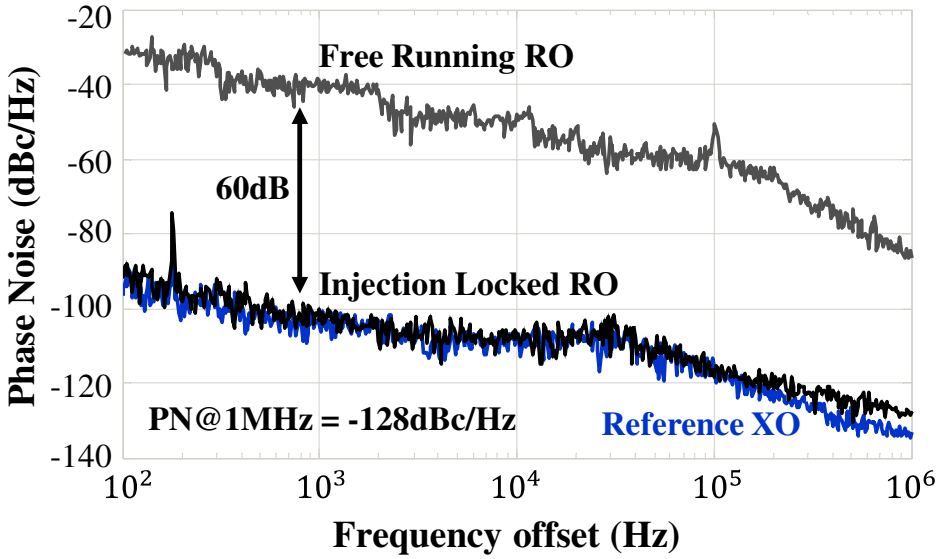


Figure 3.11. ILRO, XO and unlocked RO PN.

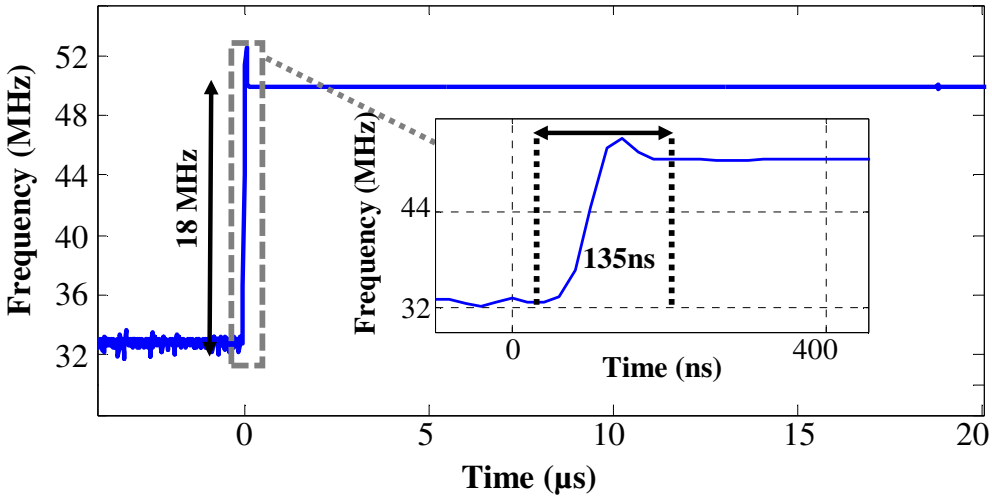


Figure 3.12. Frequency transient showing the settling time for ILRO.

respectively. The measured PN at 1MHz offset is -128dBc/Hz that minimizes reciprocal mixing of LO PN. An off-chip SMD crystal (AMB8) is used with the on-chip XO. The power dissipation of the XO and RO (and RO buffers) is 29µW and 21µW, respectively, and the pulse generator and LO dividers consume 17µW total. The maximum locking range for the ILRO is 18MHz and Figure

3.12 shows the ILRO lock time of shorter than 135ns, which is measured by enabling the injection signal when the free running RO is operating at 17.6 MHz offset from f_{inj}.

The measured sensitivity at BER of 10^{-3} is -99dBm for the BPSK mode at 5kb/s and is -77dBm for the 16-QAM OFDM mode at 384kb/s. Figure 3.13 presents the BER performance vs. the input RF power for the two modes of operation. The blocker rejection ratio for out of band blockers is shown in Figure 3.14.The blocker rejection ratio for 2MHz and 10MHz offsets are 48dB and 63dB, respectively, for 3dB sensitivity loss. The receiver consumes 152µW from a 0.9V

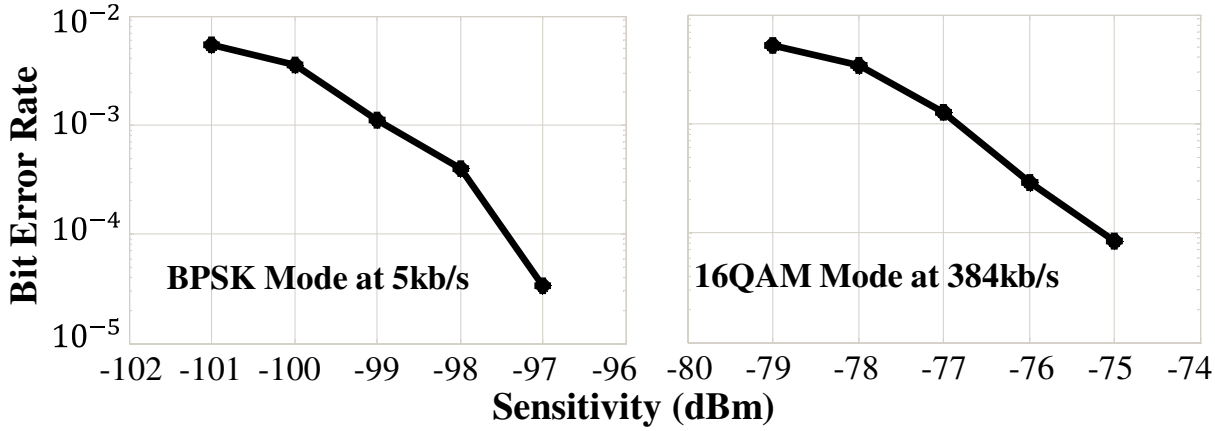


Figure 3.13. BER vs. sensitivity for BPSK and 16QAM OFDM modes.

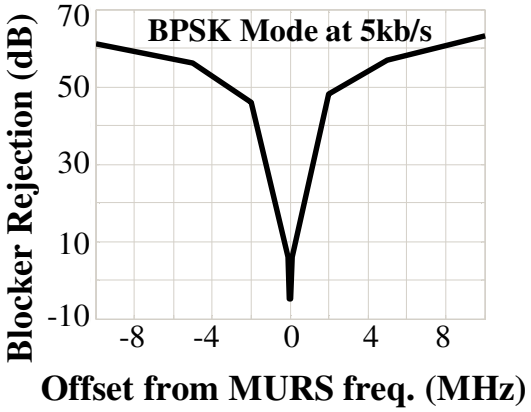


Figure 3.14. Blocker rejection for the BPSK mode.

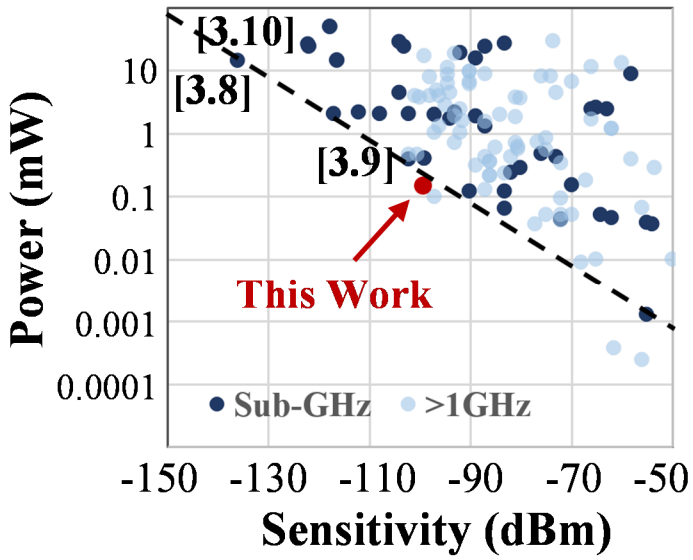


Figure 3.15. Low-power radio survey from 2005 to present. The data of the radio survey is from top conferences and commercial RX chips [3.11].

Reference	**This Work**		**[3.8] ISSCC17**	**[3.9] RFIC15**	**[3.10] ISSCC16**
Technology (nm)	40		65	130	180
Architecture	Dual-IF w/ Sub-Harmonic Mixer and ILRO		Low-IF	Low-IF	Low-IF
Carrier Freq. (MHz)	151.82-151.94		850-920	433	160/960
Supply Voltage (V)	0.9		3.3	1.2/0.5	2.2/3.6
Modulation	BPSK	16QAM OFDM	UNB DBPSK	2-FSK	2-GFSK
Data-rate (kb/s)	5	384	0.100	1	2.4/37.5
Active Power (µW)	152		14500	378	57000
Sensitivity (dBm)	-99*	-77*	-136	-102.5	-122
Blocking, 3 dB sens. loss (dB)	48 @2MHz/ 63 @10MHz		90 @10MHz	14 @ 0.2MHz	93 @ 2MHz
Oscillator PN (dBc/Hz)	-128 @ 1MHz		-106 @ 1MHz	N/A	-138 @ 2MHz

* Sensitivity is reported at BER of 10^{-3}

Table 3.1. Performance summary and comparison with the state-of-the-art narrowband receivers.

power supply, and the IF1 LNA and IF2 filters consume 59µW and 26µW, respectively. The overall gain of the receiver is 79dB at the maximum gain mode, with 25dB in the RF front-end and IF1 stages and 54dB in the IF2 stage.

Table 3.1 summarizes the measured performance of the receiver and presents a comparison between this work and other state-of-the-art narrow-band receivers. According to the low power radio survey shown in Figure 3.15 [3.11], this receiver sits below the power vs. sensitivity trend-line, demonstrating the best reported power amongst sub-GHz receivers with sensitivities < -90dBm.

3.4. Summary

In this chapter, a low power MURS band receiver with an efficient system-level design and several low power design techniques is proposed for LPWAN applications. The receiver utilizes an edge-combiner mixer first with two step down-conversion architecture, and uses an injection locked ring oscillator for LO. It achieves -99dBm sensitivity with 152μW of power at 5kb/s and a 63dB blocker rejection at 10MHz offset. The ILRO, which is locked to a stable 50MHz crystal reference, achieves a PN of -128dBc/Hz at 1MHz offset. In terms of sensitivity versus power consumption tradeoff, this radio shows the lowest power consumption compared to the state-of-the-art receivers with better than -90dBm sensitivity values.

Chapter 3: References

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Chapter 4
Energy-Efficient Long-Range Digital Transmitter

As discussed in Chapter 1, minimizing RF transceivers power consumption is of crucial importance for IoT wireless sensor nodes massive deployment. In addition, the high power consumption of current LPWAN technologies, and the need for ultra-low power radios were highlighted. To this end, an ultra-low power RX for low power long-range applications of IoT was presented in Chapter 3. Chapter 4 presents an ultra-low power long-range digital transmitter for the MURS band that is frequency and data rate agile, as a low-power solution for remote IoT communications. Digital transmitters (DTX) heavily rely on signal processing in the digital domain for calibration and programmability. Therefore due to their flexibility to support complex communication standards as well as compact size and high efficiency, a DTX is a suitable candidate for this application. As a low power and efficient solution for the IoT long-range connectivity problem, we present a current-mode quadrature digital transmitter architecture that uses the MURS band frequency planning developed in Chapter 2. The DTX utilizes 25% duty cycled non-overlapping LO signals combined with a digital class-B code profile for the input I/Q baseband signals, which both improve efficiency.

The chapter is organized as follows. Section 4.1 presents the MURS band transmission scheme used in this work. Section 4.2 discusses the existing solutions for digital transmitters and introduces our proposed efficiency enhancement method and quadrature digital transmitter

architecture. This section also discusses the efficiency enhancement techniques we have introduced and used in this design. The design implementation of the digital baseband processing blocks and the digital power amplifier will be presented in section 4.3 and the experimental results are discussed in Section 4.4.

4.1. Transmission Scheme

Recently the IoT wireless connectivity problem has been challenged by new types of low-data rate, long-range, technologies mainly operating in sub-GHz frequency bands referred to as LPWANs. Our goal was to achieve a similar coverage range, while lowering the power consumption in the uplink chain and relaxing the requirements for the downlink, and therefore reducing power on the IoT device. As discussed in Chapter 2, the MURS band is an unlicensed band at 151-154MHz that includes 5 narrowband channels [4.1]. MURS is similar in regulations to the Family Radio Service (FRS) band used for two-way radios. However, unlike FRS, the FCC allows data communications in the MURS band, for any use, with a limit of 2W transmit power. Based on a link budget analysis, for a transmission range of ~60km and a path loss exponent of 2, we only need to transmit 0dBm of power over a narrow bandwidth (5kHz) and require a receiver sensitivity of -110dBm. Therefore relaxing the requirements for the uplink/downlink chains compared to other solutions shown in Table 2.2 of Chapter 2.

As discussed in Chapter 2, in the uplink, we use both multi-tone and single-tone transmissions. The single-tone transmission is based on either a 10kHz or 5kHz bandwidth, operating at any of the five MURS frequency bands ranging from 151.82MHz to 154.6MHz. To reduce the peak to average power ratio (PAPR), single-tone transmission uses BPSK modulation with data-rates of 5kb/s and 10kb/s. For higher data-rate applications, we use a multi-tone

transmission based on 16QAM OFDM with a 10kHz subcarrier spacing and a symbol duration of 125µs (assuming a guard time ratio of ¼). The OFDM symbols occupy 160kHz of bandwidth over the three lower frequency MURS channels (151.820-151.940MHz) and the 16QAM constellation points are mapped to 16 subcarriers including 12 data, 2 pilot tones and 2 null subcarriers. The data-rate for the multi-tone transmission is 384kb/s. This frequency planning allows realization of a low power multi-mode transmitter enabling long range transmissions for ultra-low-power IoT applications.

4.2. Digital Transmitter Architecture

Typical digital transmitters consist of many direct digital-to-RF conversion unit cells, where the digital information is directly up-converted to the continuous-time real-valued RF output signal. As shown in Figure 4.1, the digital baseband signals are applied to a set of digital-to-RF conversion cells comprising digital mixer cells and digital power amplifier (DPA) unit cells.

4.2.1. Existing Digital Transmitter Architectures

A number of approaches for digital transmitters have been reported in the literature, including polar, quadrature and out-phasing [4.2- 4.5]. For DTX architectures, recently, polar

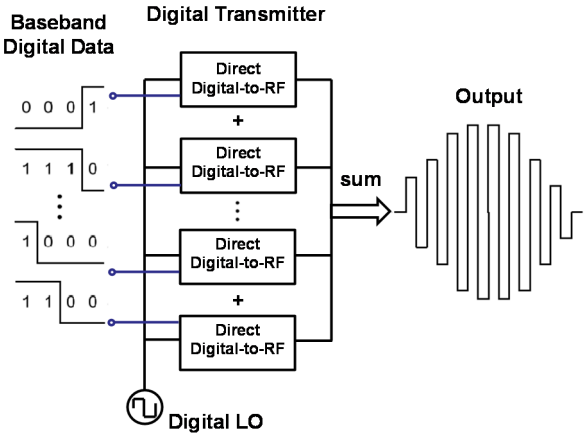
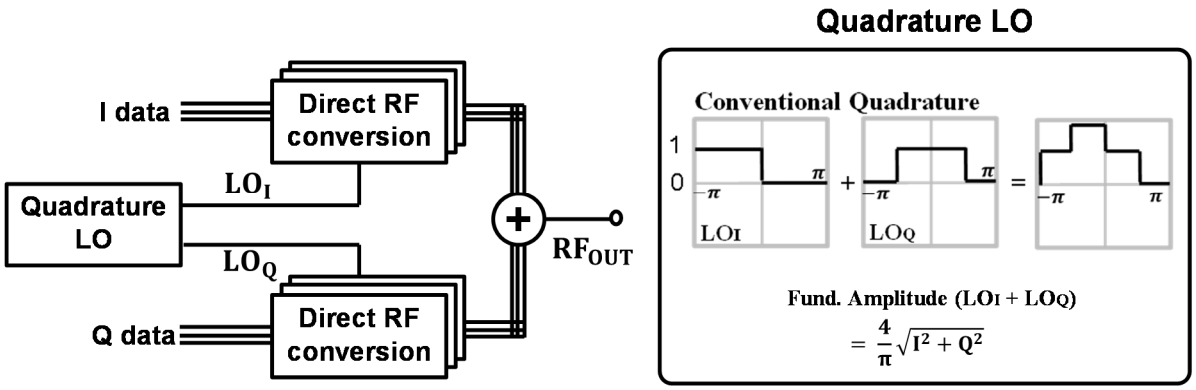


Figure 4.1. Block diagram of a typical digital transmitter.

architectures have become more popular due to their higher efficiency compared to quadrature architectures. However, polar transmitters require high power consumption and high computation cost due to the use of a CORDIC block for in-phase (I) and quadrature (Q) data to polar conversion, as well as the requirement for accurate timing alignment between phase and amplitude. Therefore in this work, quadrature architectures have been studied.

Quadrature transmitters are based on Cartesian coordinate signals with I and Q information. As illustrated in Figure 4.2(a), the RF output signal in a quadrature DTX is obtained from the summation of the I and Q signals. The conventional quadrature digital transmitters, as the voltage-mode quadrature architecture proposed in [4.2], suffer from a lower output power compared to polar transmitters with the same input I/Q magnitude, due to the use of 90° phase shifted digital I/Q LO signals. The I and Q LO waveforms of the quadrature transmitter are shown in Figure 4.2(b). Since the transmitter uses square wave I and Q LO signals with 50% duty cycle and a phase difference of 90°, the fundamental amplitude of the combined I and Q voltages can be written as:

$$\text{Fund. Amplitude } (LO_I + LO_Q) = \frac{4}{\pi}\sqrt{I^2 + Q^2} \tag{4-1}$$



(a) (b)

Figure 4.2. (a)Block diagram of quadrature digital transmitters (b) I and Q LO waveforms of quadrature transmitters

In [4.4] three level LO signals have been used to overcome the low efficiency problem for voltage-mode quadrature architectures, and in current-mode quadrature DTX as the one in [4.5], the problem is addressed by using extra I/Q sign bits and two separate DACs for I and Q paths while using the non-overlapping LO signals.

In this work, a digital quadrature architecture is presented that employs switched-current DPAs and uses a digital class-B input code profile in combination with non-overlapping LO signals to overcome the low efficiency problem of conventional quadrature architectures. By employing digital class-B input signals we reduce the number of I/Q DACs to half and eliminate the need for extra processing of the sign bits in current-mode digital quadrature transmitters, therefore improving the efficiency. Section 4.4.4 discusses the proposed DTX design procedure.

4.2.2. Proposed Digital Class-B I/Q Cell Sharing TX Architecture

The block diagram of the proposed DTX architecture is shown in Figure 4.3. As shown, all signal processing is performed in the digital domain, preceding digital to analog conversion. By employing non-overlapping 25% duty cycled quadrature LO signals, we are able to time share and use the same digital-to-RF cell for both I and Q baseband data. Time division multiplexing of the data in this way reduces the number of cells to half and significantly saves power. As shown in Figure 4.3, the mixing as well as I/Q data combination are all implemented in the digital domain, and every digital-to-RF cell includes I/Q data combination block, multiplier, and digital power amplifier block which is responsible for digital to analog (D/A) conversion and amplification.

There are two types of DPAs, which are responslible for amplification and digital to analog conversion, typically used in DTXs. One uses current-mode switched-current sources and the other type uses voltage-mode switched-capacitors for the PA cell. In switched-current DPAs (SC-DPA)

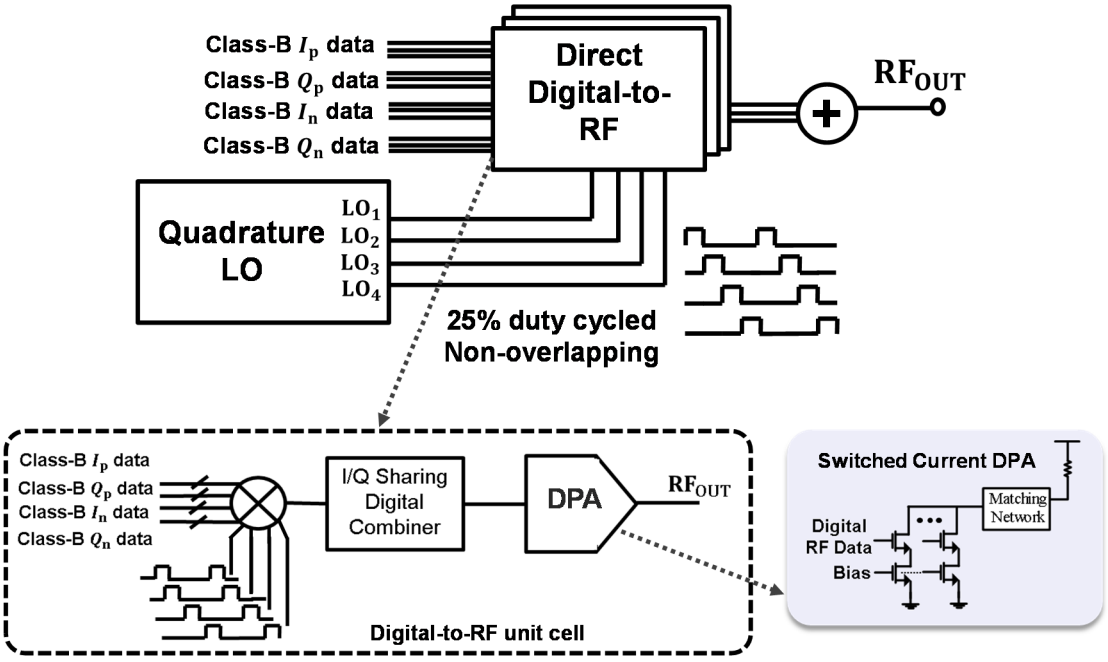
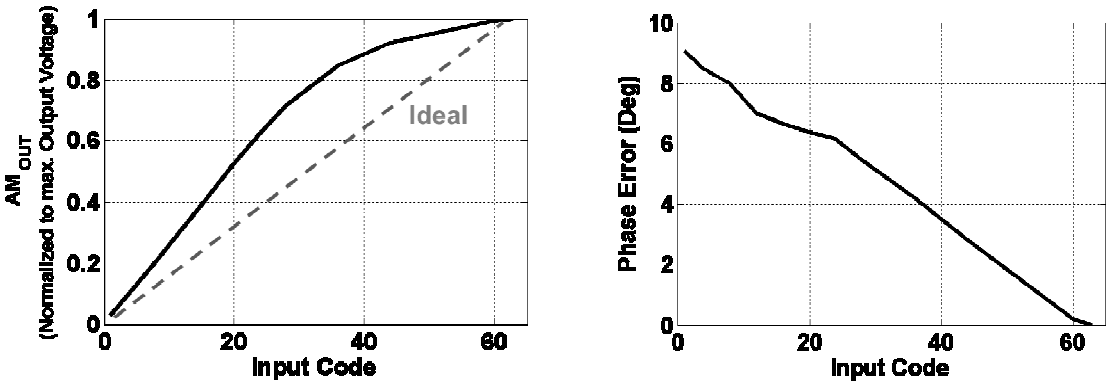


Figure 4.3. Block diagram proposed digital class-B I/Q cell sharing TX.

the code-dependent output impedance would introduce AM-AM and AM-PM distortion, however, an ideal peak-to-peak amplitude of 2×VDD can be achieved to maximize their output power [4.5]. The switched-capacitor DPAs, on the other hand, have less distortion due to their code-independent impedance but they only have a maximum swing of VDD at the output. In order to achieve the maximum swing in the output of the DTX we have utilized a 6-bit segmented SC-DPA for the amplification and D/A conversion. The schematic of the SC-DPA is shown in Figure 4.3. The transistors at the bottom are used to adjust the bias current in the DPA while the cascode transistors are controlled by the up-converted I/Q code words at the RF frequency.

To minimize the AM-AM distortion in this architecture which is mainly due to the finite output resistance of the DPA [4.6], we appropriately sized the NMOS transistors used in the DPA to achieve a higher output resistance and to partially improve the linearity. However, pre distortion linearization techniques are required to completely remove the distortion. The simulated AM-AM and AM-PM characteristics of the digital transmitter are shown in Figure 4.4. By sacrificing the



(a) (b)

Figure 4.4. (a) Simulated Input Code- AM characteristic, (b) Simulated Input Code- PM characteristic.

available output power and digitally tuning the input code for a lower output power we are able to operate the DPA in the less AM distorted region.

Motivated by the idea of class-B PAs and with the goal of enhancing the efficiency of the switched-current DPA based quadrature DTX discussed above, the digital baseband I/Q signals in this design are generated in two pairs of I/Q inputs, namely, I_p/Q_p and I_n/Q_n. The baseband signal coding or what we call the class-B baseband signals of the quadrature architecture presented in this work is shown in Figure 4.5. The digital I_p and Q_p data, represent the information for the positive values of baseband I and Q signals, respectively, with the negative values of those signals

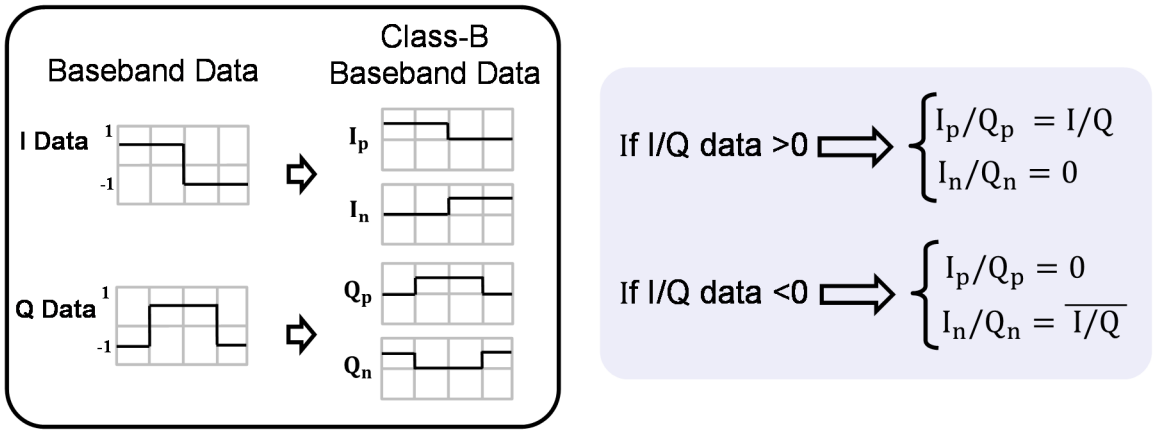


Figure 4.5. Baseband class-B coding of I/Q data.

set to zero and similarly, I_n and Q_n codes contain the information for the positive values of the inverted I and Q signals with their negative values set to zero. By coding the digital input data using the proposed class-B method, for each I_p/Q_p and I_n/Q_n data, the digital power amplifier only conducts for the positive half cycle similar to class-B analog power amplifiers [4.7].

The quadrature mixing in this design is performed in the digital domain by mixing the input I and Q data by non-overlapping 25% duty cycled LOs using combinational logic. This topology also creates a band pass filter for the up-converted data and also performs image rejection [4.8].

The operation of the class-B I/Q cell sharing DTX is illustrated in Figure 4.6. As shown in Figure 4.6 (c), at every quarter of the carrier period each of the I_p, Q_p, I_n, Q_n signals are multiplied

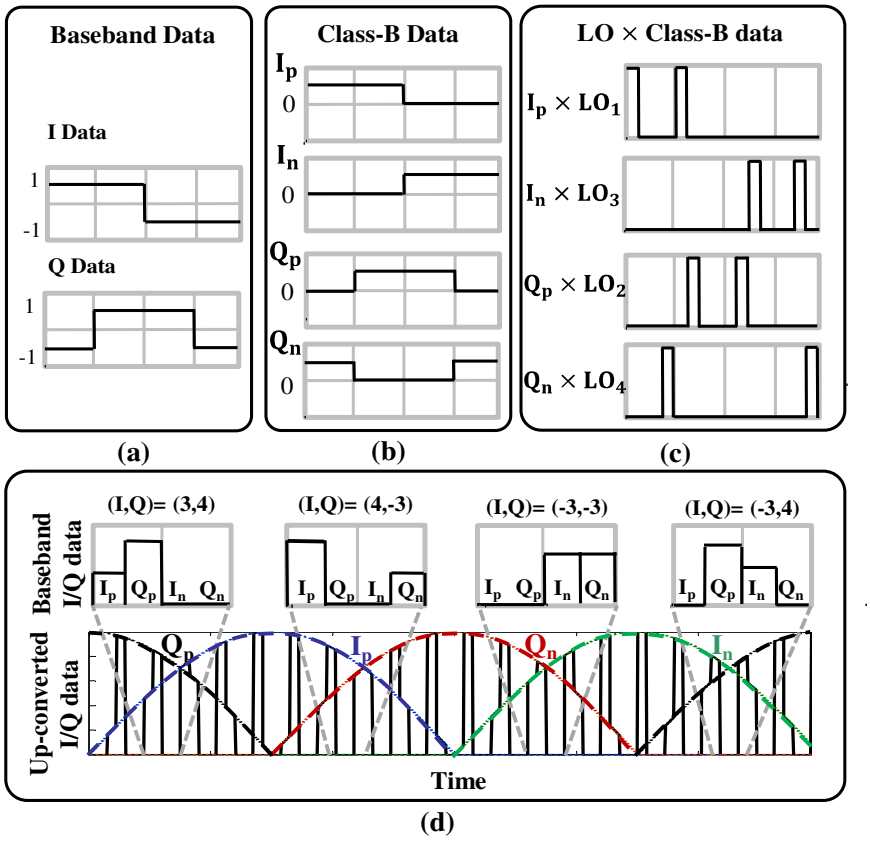


Figure 4.6. Baseband signal processing of DTX (a) Baseband I/Q data, (b) Baseband class-B modified I/Q data (c)Up-converted I/Q data, (d) Single tone example of the I/Q combining method.

by the corresponding $LO_{1\text{-}4}$ to produce the non-overlapping up- converted I/Q signals and therefore for every LO period only one of the I_p, I_n, pair or Q_n, Q_p, pair contains I/Q baseband information with the other one set to zero. The up-converted signals are then combined in the time domain to produce the digital form of the modulated signal, therefore the up-converted signal cyclically interchanges between the I_p, Q_p, I_n, Q_n values. A simple example of a single tone sinusoidal I/Q input data is presented in Figure 4.6 (d). Combining the digital I/Q data in the digital domain instead of summing them at the output of the DPA is possible in this design since the quadrature signals are never enabled at the same time.

By utilizing the digital class-B coding technique and non-overlapping LOs with a switched-current DPA, we are able to 1) overcome the low output power of conventional quadrature DTX

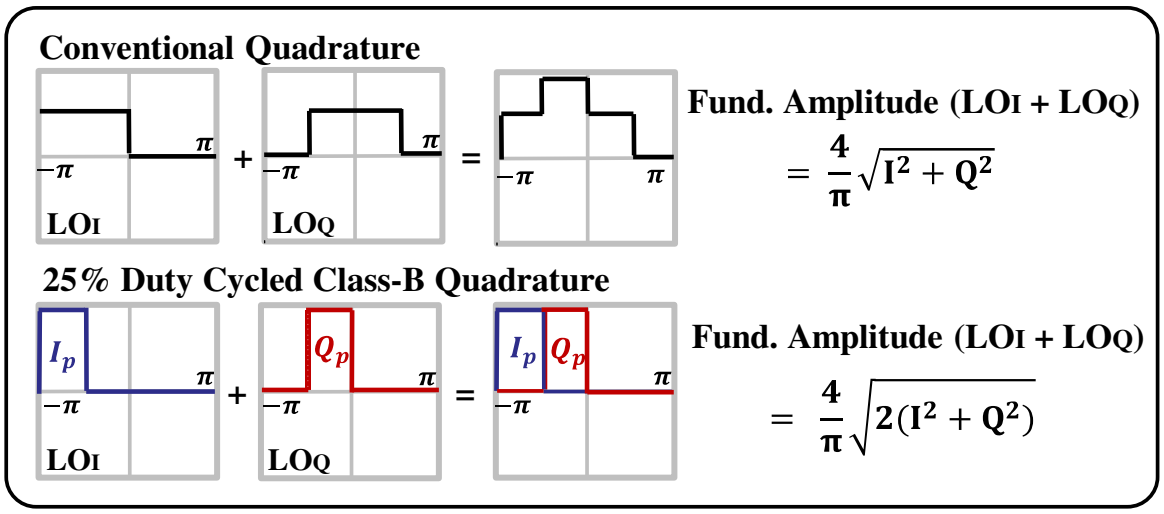


Figure 4.7. LO_I/LO_Q waveforms and the IQ combined fundamental components in conventional and class-B quadrature TX.

and improve the power of the fundamental RF frequency by 3dB when the power of I and Q inputs are equal, as shown in Figure 4.7; 2) achieve an ideal peak-to-peak amplitude of $2\times V_{DD}$ at the output of the current-mode DPA with lower power consumption compared to un-coded I/Q inputs; 3) eliminate the need for using I/Q sign bits and two separate digital-to-RF blocks for I and

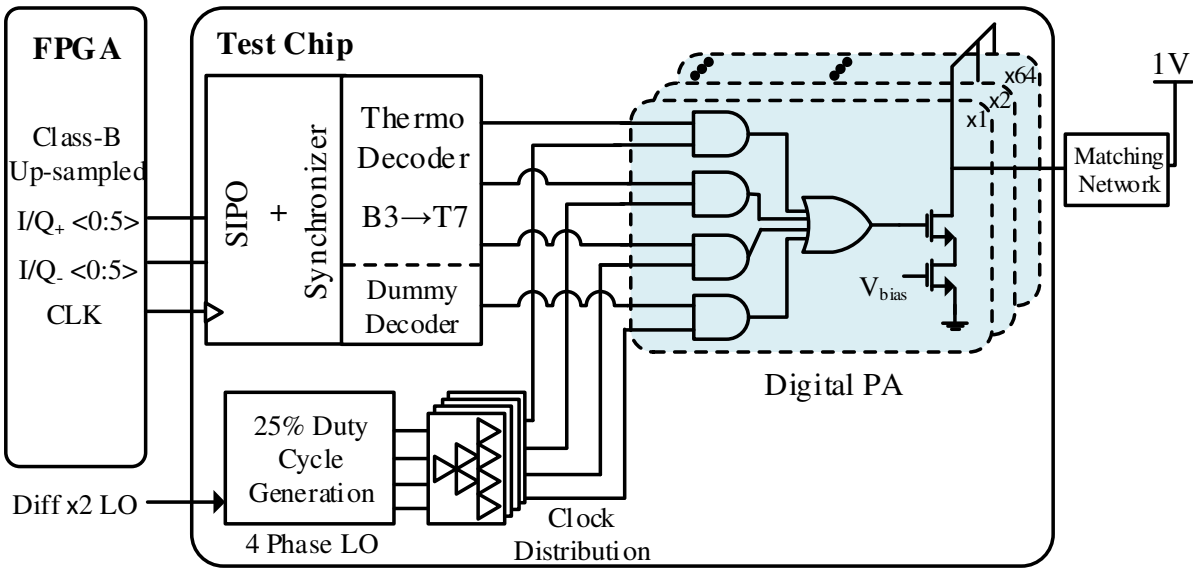


Figure 4.8. Block diagram of the proposed digital transmitter.

Q paths and reducing the number of switch cells to half. Hence an improved efficiency is achieved compared to a conventional quadrature DTX.

4.3. Design Implementation

4.3.1. Digital Data Path

As shown in the block diagram of Figure 4.8, the digital class-B I/Q baseband signals, which are generated and quantized by 6 bits on an FPGA, are loaded to the chip in a serial mode. The serial-to-parallel converter and the synchronizer align the data to compensate for the delay caused by the code processing. The digital baseband signals are therefore fed to the 16x oversampling DAC at 3.2MHz. In direct RF modulators, such as this work, the quantization noise and aliases reach the output load unfiltered and they can be reduced by increasing the DAC resolution or the sampling rate. By benefiting from the relaxed spectral mask constraints in the MURS band, the selection of this sampling frequency balances the timing constraints and enables a low IF implementation of the transmitter, reducing power consumption in the digital data path.

This data is then segmented by a binary to thermometer decoder. The higher three bits are configured in thermometer code and the lower three bits are implemented in binary. Therefore a total of 10 bits of IF data for each of the four I/Q channels reach the mixing DAC, among which there are 7 thermometer-coded and 3 binary bits.

4.3.2. Digital Power Amplifier

The DPA is implemented with 6-bits resolution. As shown in Figure 4.9, each unit cell consists of an analog and a digital part. The mixing of the IF digital data and LO signals is done in the digital part using AND gates and the time division multiplexing of the up-converted signals is done using OR gates. The analog part of the unit cell consists of an LSB size NMOS current source, which is biased by an internal standard beta multiplier bias generator, and a cascode NMOS switch that is controlled by the input digital data. The current source transistors are sized appropriately to maximize the output dynamic range and minimize noise. The 64 unit cells are drain-combined and connected to the output load. Figure 4.10 shows the floorplan of the segmented DPA and the special switching scheme proposed in this work. The DAC is implemented with a common centroid layout architecture and dummy cells are added to avoid the edge effects. For linearity purposes and in order to mix the input digital signal with the LO signal with the right phase, the

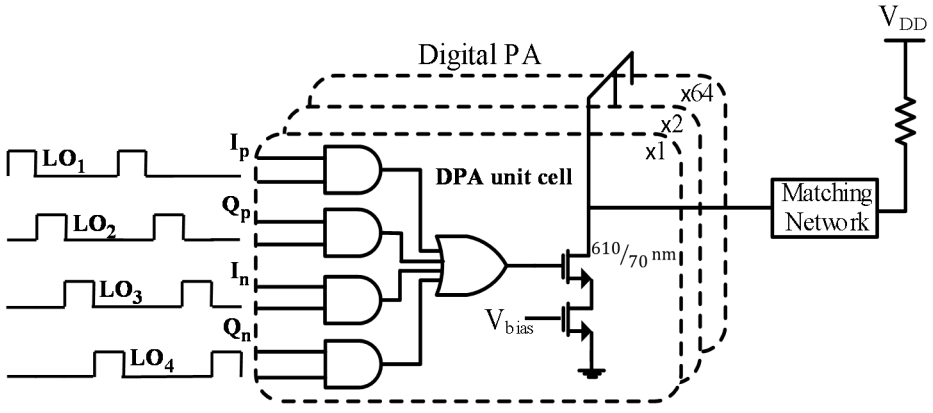


Figure 4.9. Class-B IQ cell sharing DPA.

digital I/Q mixing and combining, the switches and the current sources are all placed in the same array. Since 64 unit current sources have to be placed in the DAC array and only 32 digital I/Q combining blocks are needed for all the unit cells, two separate types of unit cells are designed. The 32 shaded unit cells include both the analog and digital parts of the DAC, and the other 32 non-shaded unit cells only include the analog part of the DAC together with dummy I/Q combining digital blocks that are placed for the symmetry of the layout. The wiring of the 7 bit thermometer and 3 bit binary segments of all four I/Q channels is done accordingly.

The differential 2×LO signals at twice the carrier frequency are fed from an external source to an LO generator block shown in Figure 4.11, which creates the 25% duty cycled LOs using a divide-by-2 circuit and combinational logic. In this design, it is important that the four 25% duty cycled LO signals are synchronized, therefore a careful 32 point custom clock routing

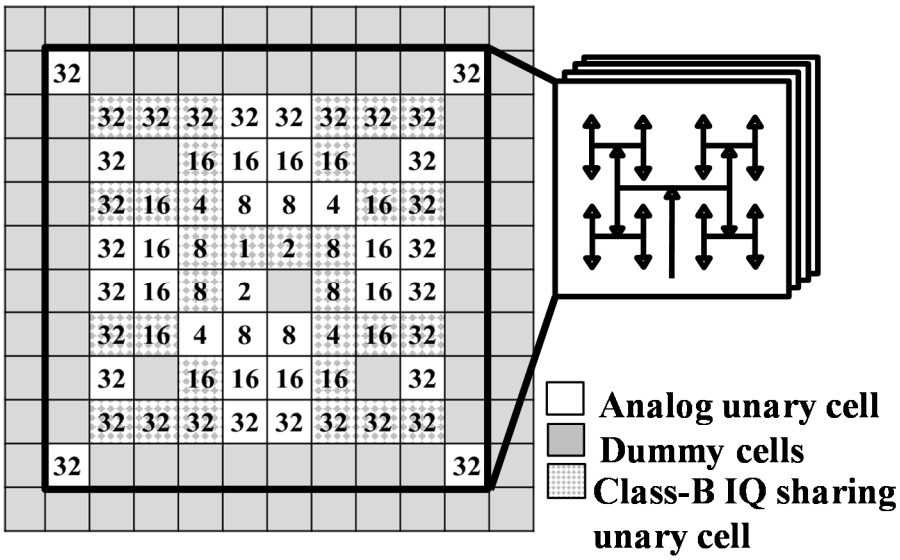


Figure 4.10. Floor plan of the segmented DPA.

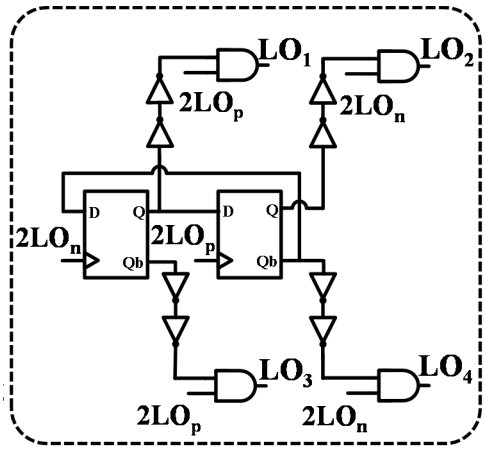


Figure 4.11. 25% duty cycle LO generator block.

implementation is done in the DAC layout using a separate HTree clock distribution for each of the four LO signal phases to ensure a very low skew.

4.4. Measurements

The transmitter was fabricated in a LP-65nm CMOS process and packaged in a 5x5mm QFN32 package. The transmitter core blocks, not including the I/O pads, occupy an area of

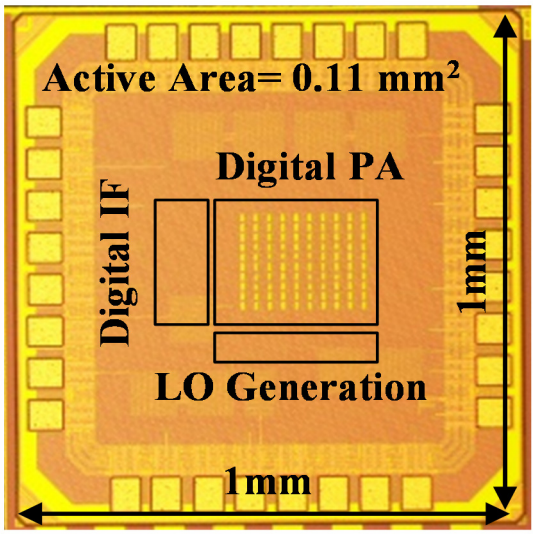


Figure 4.12. Die micrograph of the transmitter.

450x225um^2. Figure 4.12 shows the die photo of the transmitter. An off-chip bandpass filter suppresses the harmonics of the up-converted signal and provides the fundamental MURS band signal. The output matching network of the transmitter is designed by a parallel LC tank using a normal size inductor (22nH) which is matched to a high load impedance at the desired MURS frequency band This, maximizes the peak output power of the DPA, however in order to lower the code dependent compression of the output impedance, a digital pre-distortion technique is required to improve the linearity in this architecture [4.9]. The standalone measurement results of the DPA efficiency vs. power is shown in Figure 4.13. The DPA delivers 41% of efficiency at a peak output power of 0dBm after the matching network. The DPA and all the digital blocks in the design are operating from a 1.2V supply voltage. The transmitter is measured with MURS single-tone and multi-tone transmission schemes. The FCC mask together with the power spectral density (PSD) for the BPSK modulated single-tone transmission of the MURS three lower frequencies of 151.820, 151.880 and 151.940MHz with a data-rate of 5kb/s is presented in Figure 4.14. It is shown that the signals are below the FCC mask.

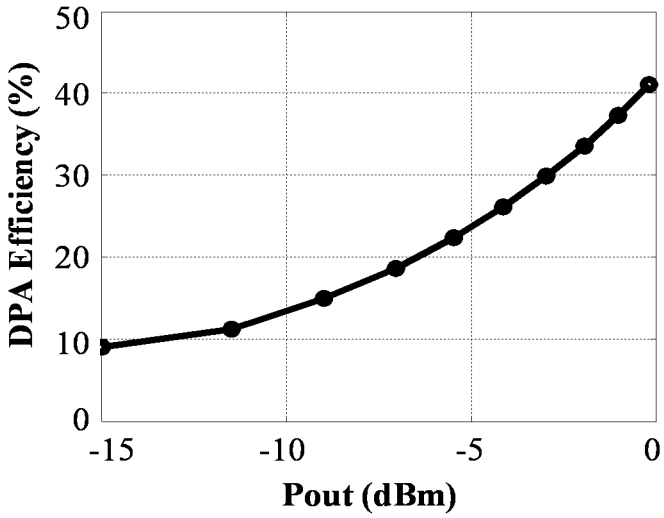


Figure 4.13. DPA efficiency.

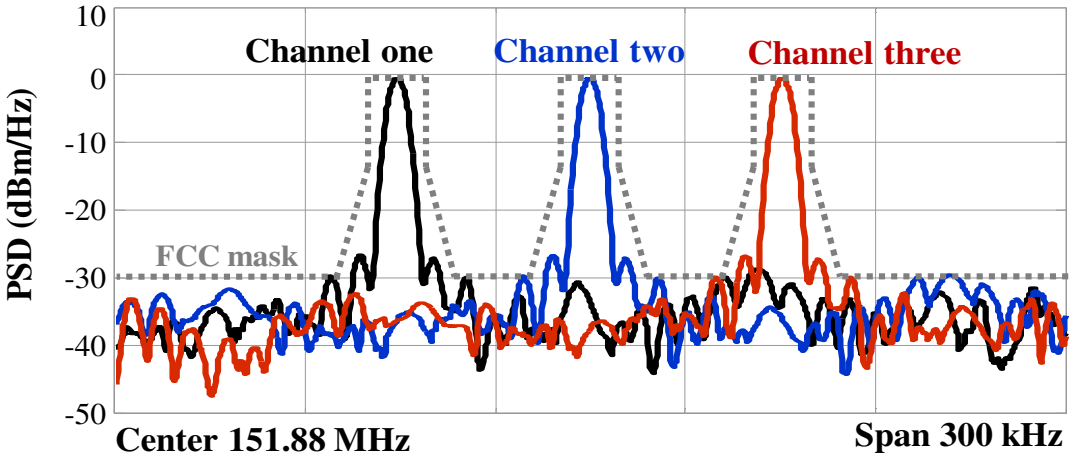


Figure 4.14. Measured output spectrum of single-tone BPSK at 5kb/s.

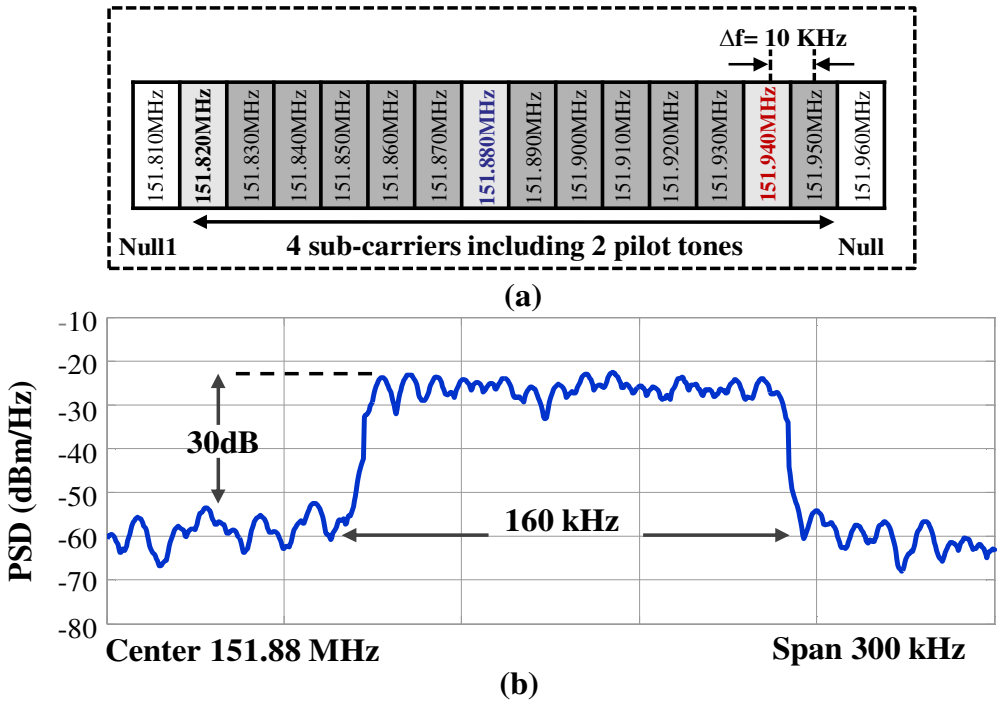


Figure 4.15. (a) OFDM modulation frequency planning. (b) Measured close-in PSD of multi-tone MURS transmission at 384kb/s.

For the spectrally efficient long range communication mode, the multi-tone transmission in MURS band is measured with a 16QAM OFDM signal discussed in section 4.1. The proposed OFDM frequency planning used for the multi-tone MURS transmission is presented in Figure 4.15

(a). It achieves 384kbps of raw data-rate over 160kHz of bandwidth. The multi-tone transmission is not FCC compliant because it utilizes the white spaces between the MURS band channels for signal, however it is used as a proof of concept for a spectral efficient performance of the DTX over a narrowband OFDM modulation for long-range IoT applications requiring higher data-rates. The measured close-in PSD of the 16QAM, MURS band OFDM modulation with 6.9dB PAPR is shown in Figure 4.15 (b), which shows an ACLR value of -30dB at 160kHz frequency offset for a transmit power of -7dBm. The average efficiency of the DPA at 7dB back-off power is 19.2%. Based on our link budget analysis for an average transmit power of -7dBm over 160kHz of bandwidth, a line-of-sight coverage range of 4km is achievable assuming a path loss component of 2. The measured far-out spectrum of 160kHz 16QAM signal is shown in Figure 4.16 (a) and the spurs are repeated every sampling rate of 3.2MHz. As shown in Figure 4.16 (b) the RMS EVM at -7dBm output power is 4.2%. At higher output powers the DPA goes to the cut-off region out of the 6.9 dB PAPR range, and the EVM starts to degrade as shown in the table in Figure 4.16 (b). Figure 4.17 shows a comparison between the efficiency for the transmitter in this work and the

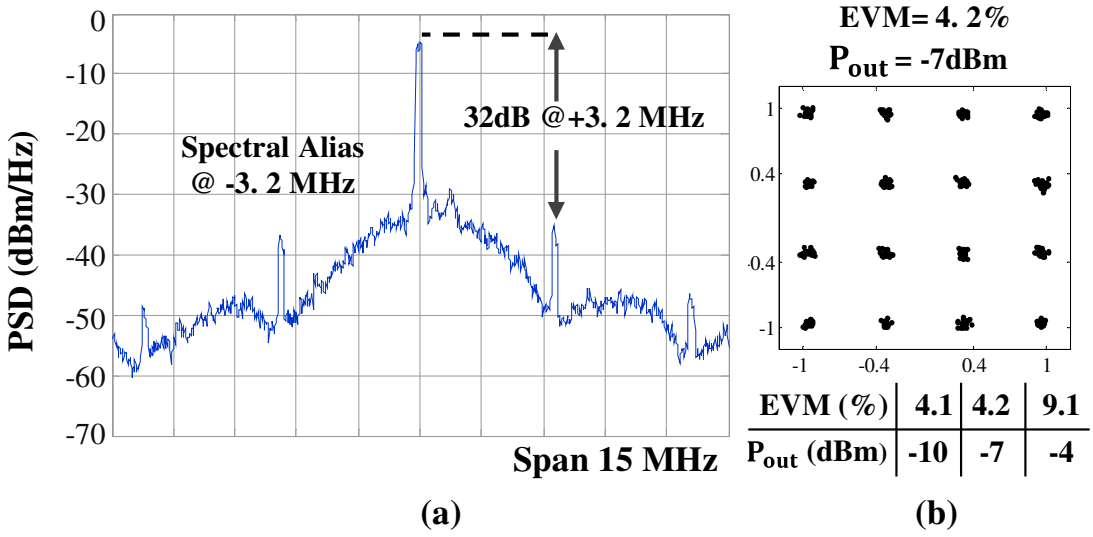


Figure 4.16. Far-out PSD of multi-tone transmission (b) EVM and constellation diagram of 160kHz 16QAM symbols.

state-of-the-art narrowband transmitters used for LPWAN applications. Table 4.1 summarizes the measured performance of the transmitter in this work [4.18-4.19] and compares this work to the state-of-the-art narrowband transmitters.

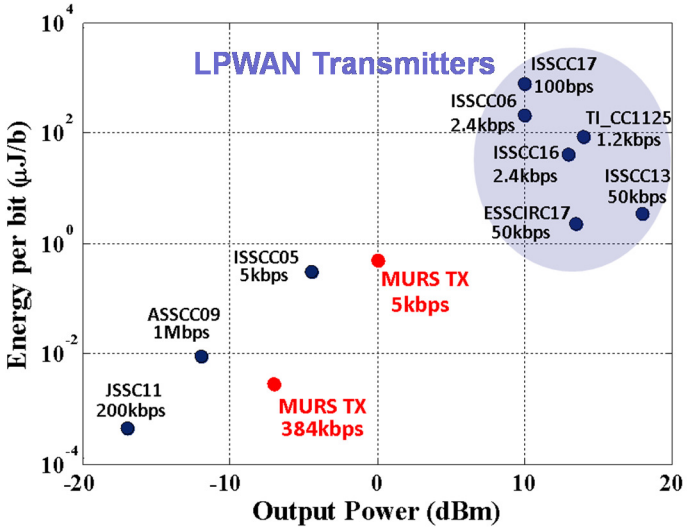


Figure 4.17. Energy efficiency vs output power comparison between this work and state-of-the art narrowband transmitters [4.10-4.17]

Reference	**This Work**		**[4.3] JSCC16**	**[4.10] ISSCC17**	**[4.11] JSSC11**	**[4.12] RFIC14**
Technology	65nm		40nm	65nm	130nm	130nm
Architecture	Digital Class-B I/Q cell sharing		Digital Polar	Digital Polar	Digital	Analog MUX/ILO
Carrier Freq.	151.82-151.94MHz		750-930MHz	850-920MHz	433MHz	2360-2480MHz
Supply Voltage	1.2V		1V	3.3V	1V	1.5/1V
Modulation	BPSK	16QAM OFDM	64QAM OFDM	UNB DBPSK	BFSK	π/4-DQPSK
Data-rate	5kb/s	384kb/s	-	100b/s	200kb/s	971 kb/s
Peak Power	0dBm		8dBm	14.7dBm	-11dBm	-
Peak Efficiency	41%		45%	-	30%	-
Avg. Power	-7dBm		0dBm	10dBm	-17dBm	-10dBm
ACLR	-30dB at 160KHz offset		-	-	-	-33dB
EVM	4.2%		4.4%	<5%	-	3.2%

Table 4.1. Performance summary and comparison with state-of-the-art narrowband transmitters.

4.5. Summary

This chapter presents an ultra- low power digital quadrature transmitter. By utilizing the MURS frequency planning a low power solution is proposed for wide area coverage for the IoT. Existing digital transmitters are discussed. We introduce a quadrature DTX architecture where we use energy efficiency enhancement techniques to improve the efficiency performance over conventional quadrature DTX architectures. The transmitter efficiency is enhanced by employing the digital class-B input codeword profile in combination with the time division multiplexing of the quadrature data. The class-B I/Q cell sharing technique allows the transmitter deliver a peak efficiency of 41% at a peak output power of 0dBm. This work provides a competitive solution for emerging long-range IoT applications at a much lower power consumption.

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Chapter 5
Nano-Watt Analog Front-End For ECG Monitoring

One of the most common applications of short-range IoT is in the medical healthcare space, as was discussed in Chapter 1. In recent years, there has been a growing demand for ultralow power (ULP) energy-harvesting body sensor nodes for continuous and low-cost monitoring of patient bio -signal data for diagnosis and prevention of various illnesses, such as heart arrhythmia [5.1–5.4]. One of the most important challenges for many of these sensors is the operating lifetime. These sensors often operate in energy-constrained environments where there is a need to harvest energy by different methods, such as photovoltaic cells or thermoelectric generators (TEGs). Additionally, these systems need to operate from very low supply voltages. For example, a 1 cm^3 TEG energy harvester attached to a running person delivers only 2.2 µW of power, and the voltage available at the output of TEG energy harvesters is often only tens of millivolts [5.5]. Therefore, low-voltage operation of battery-less signal acquisition sensors highly relaxes the voltage boost conversion requirement for generating a usable supply voltage.

As stated in Chapter 1, due to the continuous bio-signal monitoring of these sensor nodes, the power consumption of signal acquisition AFEs plays an important role in the overall power consumption of the sensors. Recent advancements in state-of-the-art self-powered systems, such as the UMich/UVA SoC discussed in the Introduction chapter [5.2], have demonstrated sub-µW operation for these systems. This highlights the requirement for <100 nW AFE. One of the

important requirements of ECG signal acquisition systems is the capability to detect very small input signals on the order of 100 μV to 4 mV at near-DC frequencies, where flicker noise is dominant. Therefore, low noise operation of the AFE is one of the primary specifications of an ECG front-end, and signal acquisition systems often compromise the power consumption of the system to achieve lower input-referred noise specifications or vice versa.

This chapter presents an ultralow power low-noise AFE that meets the requirements of ULP energy-harvesting physiological sensors. By utilizing a weak inversion biasing technique, and with a power consumption of only 68 nW, the AFE realizes a very low flicker noise corner frequency and achieves an input-referred noise of 2.8 μV_{rms}. The AFE operates from a low power supply of 0.5 V, which relaxes the voltage boost requirements of energy-harvesting systems. Fully differential topology is utilized to ensure a high common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR). The AFE in this work attains a noise efficiency factor of 2.78, corresponding to a power efficiency factor [5.6] (PEF, also known as NEF^2xV_{DD}) of 3.9. The AFE achieves an input-referred noise of <10 μV_{rms} with a <100 nW power consumption, which demonstrates a very good balance for the noise–power trade-off, compared to state-of-the-art amplifiers. Figure 5.1 presents a comparison of power consumption versus root mean square (RMS) input-referred noise per square root of bandwidth for the recent state-of-the-art signal acquisition systems [5.6–5.18]. The proposed AFE has the lowest input-referred noise per square root of bandwidth compared to the state-of-the-art AFEs with power consumptions below 100 nW. Constant PEF contours are shown on the figure, highlighting the low-power and low-noise trade-off for designs of amplifiers with similar PEF. PEF is used here to account for noise, current, and required voltage headroom of amplifiers. The presented AFE was also integrated in a self-powered physiological monitoring SoC [5.2]. The performance of the AFE was validated in a real-world

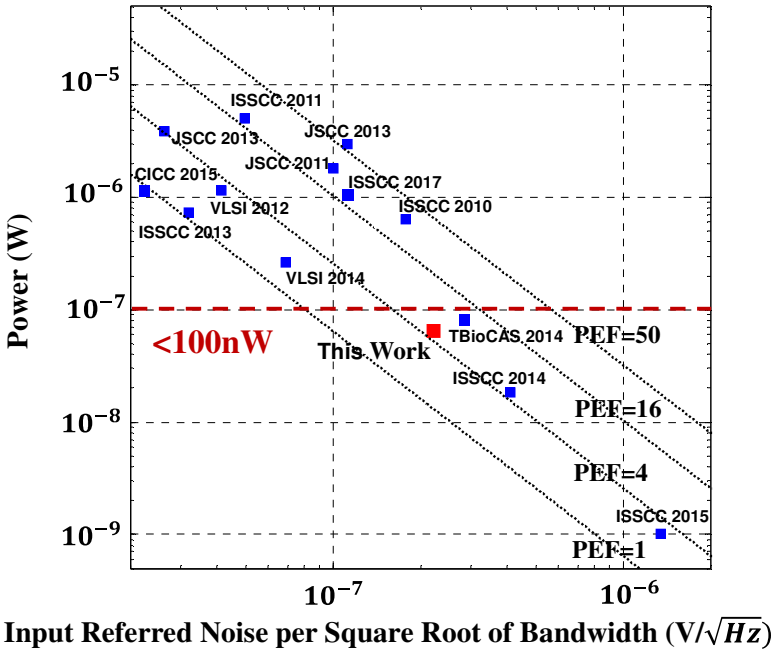


Figure 5.1. Power efficiency comparison between this work and other state-of-the-art works in power efficiency factor (PEF) (NEF^2xV_{DD}) contours. [5.6–5.18].

test scenario, by capturing and processing ECG bio-signals from human subjects. The AFE output signals were digitized on the SoC using an integrated successive approximation (SAR) analog-to-digital (ADC), and they were used to successfully perform ECG heart rate (R-R) extraction.

The outline of this chapter is as follows. We introduce the AFE architecture in Section 5.2, focusing on the three-stage AFE integration and features of circuit building blocks. In Section 5.3, we discuss the state-of-the art low-noise biopotential amplifiers and present the low-noise amplifier design in this work. The design considerations for a low-noise low-power design of the AFE are discussed here. Section 5.4 presents the designs of the low-pass filter and variable gain amplifier. Finally, the measurement results for the AFE chip are discussed in Section 5.5 and the AFE integration on the SoC and real-world test scenarios for arrhythmia detection are presented.

5.1. AFE Architecture

To meet the low-power and low-noise performance requirements of battery-less signal acquisition sensors, and the specifications for the ECG signal detection, the AC-coupled ultralow-power analog front-end was employed as shown in Figure 5.2. Achieving minimum input-referred noise performance and high power efficiency at low current levels is a major challenge. This is enabled by several considerations in the architecture and component level design of the AFE. The fully differential non-chopping capacitive feedback architecture was chosen in order to transfer the high dynamic range and hence gain requirements of the AFE to the lower ECG band frequencies, as opposed to chopper amplifiers where the amplification is done at higher chopping frequencies. The low supply voltage and efficient weak inversion biasing approach in the design of the AFE's building blocks enables low-power and high-gain realization of the AFE. Transistor-level low-noise design considerations were implemented in the design of the AFE to enable a low-noise performance. In this work, we present a fully integrated AFE, which realizes a low-noise performance, as well as an ultralow-power consumption, and ensures enough circuit reliability, bandwidth, and precision to enable practical ECG monitoring applications. The AFE consists of three stages and includes a low-noise instrumentation amplifier (LNA), a tunable bandwidth low-pass filter (LPF), and a variable gain amplifier (VGA). A self-biased current reference generator provides bias currents to the building blocks of the AFE, and a digital control scan chain block sets the gain and bandwidth of the AFE by programming the integrated voltage digital-to-analog converters (DACs).

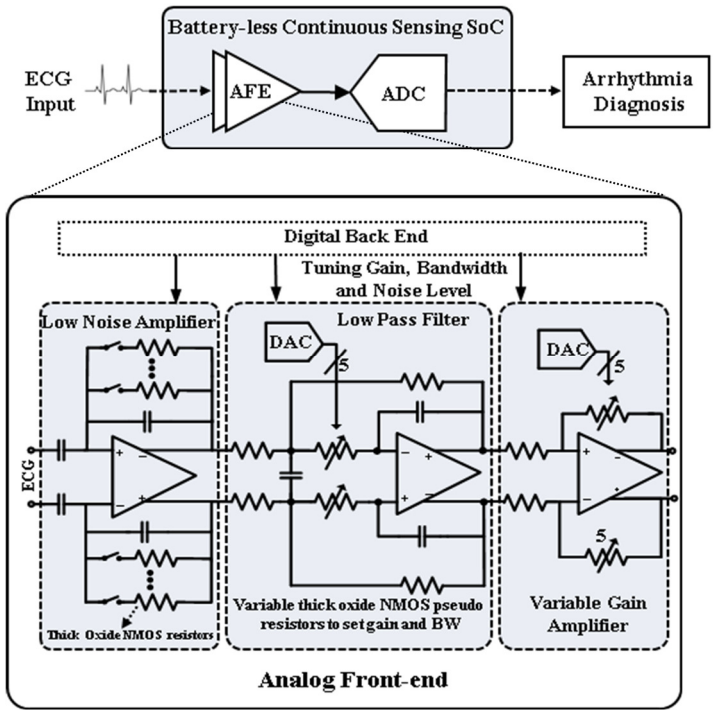


Figure 5.2. Block diagram of the AFE.

The differential input bio-signals are capacitively coupled to the input LNA to reject DC offsets introduced at the electrode tissue interface. The LNA provides a mid-band gain of 30 dB, and therefore alleviates the following stages input-referred noise requirements. The high-pass corner frequency of the AFE is set by the feedback resistors and capacitors in the LNA. The LNA is followed by a tunable low-pass filter, which controls the low-pass corner frequency of the AFE and provides a tunable bandwidth of 40–250 Hz. This corner frequency was chosen in order to capture the usable spectral content in a typical ECG signal. The LPF is loaded by the VGA, which has a programmable gain with a 21 dB range. As a result, the total gain of the front-end can be adjusted from 31 to 52 dB based on the input data. Extensive digital tuning, controlled with the digital back-end on the chip, is implemented to account for the sensitivity of pseudo-resistors to process variations.

As for the power distribution among the three stages of the AFE, the LNA consumes 27 nW, which is the most power consumption among all the blocks to enable a low-noise performance. The following stages have much less contribution to the overall noise performance, therefore, the filter has a much lower power consumption at 5 nW. Finally, the third stage, VGA, has a negligible noise contribution but drives larger capacitive loads due to the integration with the ADC; therefore, its power consumption lies between those of the LNA and LPF and is 20 nW

5.2. Low-Noise Amplifier Design

5.2.1. State-of-The-Art Biopotential Low-Noise Amplifiers

Reducing the amplifier power consumption while keeping the noise level the same is crucial for a wide range of energy constraint applications. The input-referred noise of the overall AFE is dominated by the noise performance of the first stage of the amplifier. Therefore, the current consumption in LNAs is often set for an optimized noise–power trade-off. Many outstanding research works have been carried out to address the power–noise tradeoff of AFEs [5.6–5.18]. One main idea in these designs is to increase the transconductance (g_m) of amplifiers by keeping the bias current constant. The AFE designs in prior work include inverter-based LNAs, where the amplifier g_m is increased by using stacked PMOS and NMOS pairs [5.18]. Another design approach is current-reuse through stacking amplifiers to further boost g_m of the overall amplifier [5.19]. The AFE in [5.18] achieves a very good noise efficiency factor (NEF) by using a single-stage current-reused differential amplifier topology. However, it requires a high supply voltage due to the cascode configuration and is not suitable for low-voltage ULP energy-harvesting sensors. Additionally, the orthogonal current-reuse amplifier in [5.19] achieves a high level of current-reuse by using N-time current-reuse between N-channel inputs. The 2N number of outputs

are then combined, which results in an increased power consumption due to the additional peripheral circuits, which is not desirable.

In addition to the above techniques, the chopping method has been widely employed to enhance the noise performance of amplifiers [5.7, 5.8]. Although chopping significantly reduces the flicker noise contribution of amplifiers, it requires amplifiers with larger bandwidths and chopping clock generation circuits that can increase the overall power consumption of the amplifier. In chopper amplifiers, the bio-signals are up-converted to a higher frequency and the amplification is done at high frequencies, therefore, the power consumption performance of the amplifier is not optimized. Additionally, this technique reduces the DC input impedance of the sensing front-ends [5.9], and the low input impedance can generate harmful offset currents.

In this work, we were able to lower the flicker noise corner frequency of the AFE below 100 Hz by keeping the power consumption less than 100 nW. This is enabled by using weak inversion biasing and low-noise design techniques, without the necessity of using chopping modulators. This allows the amplifier to operate at lower frequencies compared to chopper amplifiers. The frequency domain behavior of the voltages in chopper amplifiers and in the non-chopper approach is presented in Figure 5.3.

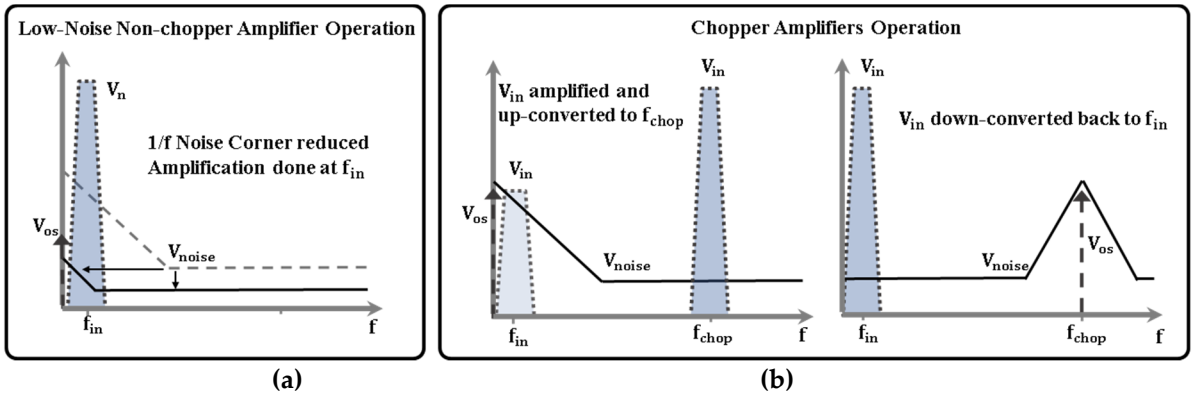
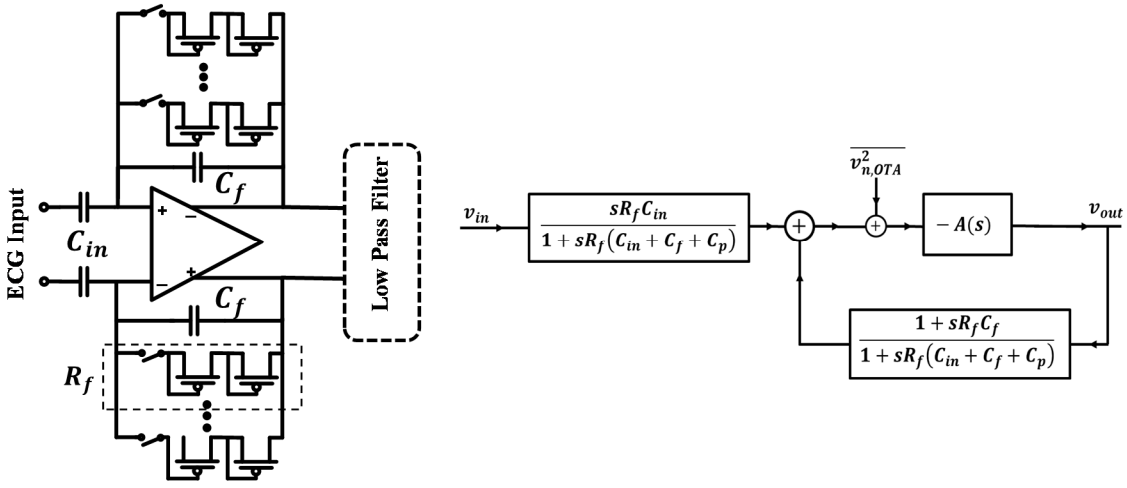


Figure 5.3. Frequency domain representation of voltages (input signal V_{in}, noise voltage V_{noise} and offset voltage V_{os}) in (a) the proposed low-noise amplifier; (b) chopper amplifiers

5.2.2. Low-Power Low-Noise Amplifier

5.2.2.1. Capacitively Feedback Amplifier

The LNA block diagram is shown in Figure 5.4 (a). It uses capacitive feedback topology, a popular topology in biomedical recording amplifiers [5.20], and uses capacitors to set the mid-band gain and to reject DC offset from the input signals. A fully differential architecture is used to achieve a high PSRR and CMRR. The ratio of the capacitors C_f and C_{in} sets the gain of the LNA amplifier. The lower cutoff frequency of the amplifier is set by$1/(2\pi R_f C_f)$, where R_f resistors are



(a) (b)

Figure 5.4. (a) Circuit diagram of the low-noise instrumentation amplifier (LNA); (b) block diagram representing the operation of the feedback amplifier.

implemented by pseudo-resistors. Pseudo-resistors can realize resistances larger than 10^{12} Ω by occupying a small area. We have used thick oxide PMOS devices to implement the pseudo-resistors due their better noise performance. The tunable lower cutoff frequency of the amplifier is adjusted by selecting the pseudo-resistors in the feedback path of the LNA with 4-bit resolution. The input-referred noise of the overall amplifier can be estimated using the capacitive feedback circuit diagram of the LNA shown in Figure 5.4 (a). From the nodal analysis, the operation of the feedback amplifier can be described by the feedback block diagram of Figure 5.4 (b), where

$v_{n,OTA}^2$ represents the input-referred noise per unit bandwidth of the operational transconductance amplifier (OTA), and C_p represents the parasitic capacitance at the input of the amplifier. According to the block diagram of Figure 5.4 (b), the overall input-referred noise of the LNA can be expressed as

$$\overline{v_{n,LNA}^2} = \left(\frac{1 + sr_f\left(C_{in} + C_f + C_p\right)}{sr_f C_{in}}\right)^2 . \overline{v_{n,OTA}^2} \tag{5.1}$$

5.2.2.2. Design of the OTA

Due to the low supply voltage, cascode and current-reuse topologies for the amplifiers are impractical. Therefore, all three main blocks in the design are implemented by two stage differential common source amplifiers with PMOS input devices for the best noise and power efficiencies. The circuit implementation is illustrated in Figure 5.5 (a). Currents and dimensions in the amplifiers are optimized for the input-referred noise, gain, power, and loading conditions in each stage of the AFE. The device dimensions for the main transistors in the OTA for the LNA are shown in Figure 5.5 (a).

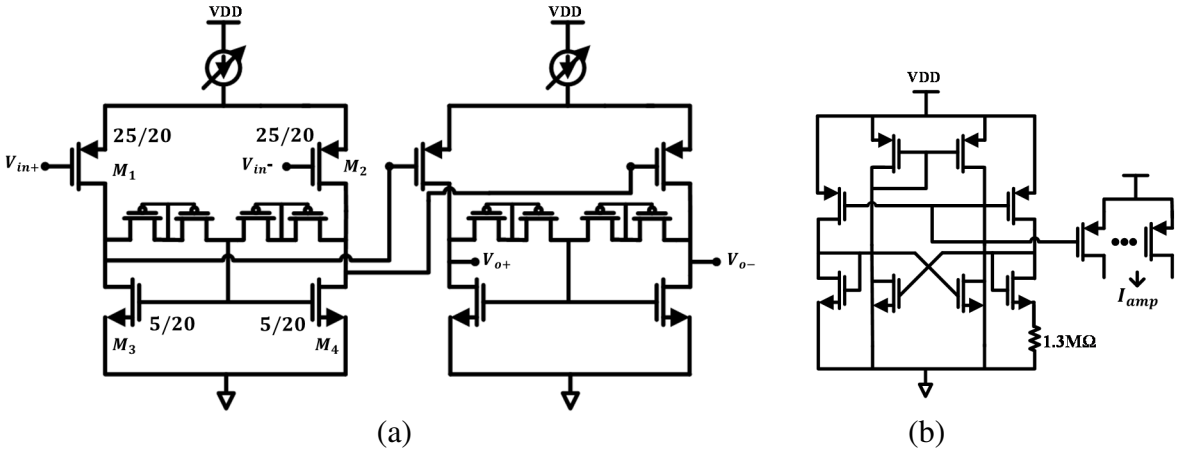


Figure 5.5. (a) Circuit implementation of the operational transconductance amplifier (OTA); (b) circuit implementation of the constant g_m current biasing circuit.

According to Equation (5.1), in order to achieve a low-noise performance, the input-referred noise of the OTA, $\overline{v_{n,OTA}^2}$, needs to be minimized. It is well known that to ensure a low input-referred noise, as well as a low power consumption, the G_m of the first stage amplifier in the LNA has to be maximized. Therefore, the currents in the first stage differential pair are set at a higher value than the second stage to meet the noise requirements. The input-referred noise of the OTA can be approximated by the input-referred noise of the first transconductance stage, which is dominated by the noise contributions from the differential PMOS (M_1 and M_2) input pair and the NMOS (M_3 and M_4) load devices. Using the transistor's small signal parameters, the input-referred thermal noise of the OTA can be approximated as

$$\overline{V_{n,OTA,th}^2} = \frac{1}{{g_{m1}}^2}\left(\frac{4kTg_{m1}}{\kappa} + 8kT\gamma g_{m3}\right) \tag{5.2}$$

where k is the Boltzmann's constant, T is the absolute temperature in kelvin, γ is the noise excess factor of transistors in strong inversion, and κ is the reciprocal of the sub-threshold slope factor n_p. The input-referred flicker noise can be calculated as:

$$\overline{V_{n,OTA,1/f}^2} = \frac{1}{C_{ox}}\left(\frac{K_n}{(WL)_1} + \frac{K_p\ {g_{m3}}^2}{(WL)_3{g_{m1}}^2}\right) \tag{5.3}$$

where C_{ox} is the gate dielectric capacitance, and K_n and K_p are process-dependent values that represent the PMOS and NMOS flicker noise constants.

In order to minimize the input-referred thermal noise and to achieve maximum g_m, transistors M_1 and M_2 are biased in the sub-threshold region with low bias currents. A constant g_m current reference with voltage regulation is used as the current reference generator, providing the bias current for the amplifiers [Figure 5.5 (b)]. In the sub-threshold region, g_m of the transistors is

independent of the device width and is proportional to the driving current. Therefore, for a given current level, it is advantageous to operate the input transistors M_1 and M_2 in the sub-threshold region to achieve a high g_m efficiency.

According to [5.21], PMOS and NMOS devices have a lower noise contribution in the weak inversion region for low frequencies (1 mHz to 100 Hz) compared to strong inversion. However, Equation (5.2) suggests strong inversion biasing for a low thermal noise contribution for NMOS load devices in the OTA. For an optimized noise performance, in order to minimize the flicker noise contribution of the NMOS devices in low frequencies, as well as to satisfy the low thermal noise requirement suggested by Equation (5.2), these transistors are biased in the near-threshold region.

In order to further reduce the flicker noise and to lower the noise corner frequency, the input devices are implemented with large gate area PMOS transistors ($M_{1,2}$). In addition, long NMOS devices M_3 and M_4 ($L = 20\ \mu m$) are employed as the load in the differential pair to achieve a lower $g_{m3,4}$ (transconductance of M_3 and M_4) value and hence further improve the flicker noise and thermal noise performance. Equation (5.1) highlights the importance of the parasitic capacitance at the differential input of the OTA. While using large transistors at the differential input of the OTA reduces the flicker noise corner frequency, it can degrade the overall input-referred noise of the amplifier. Therefore, in this design, a proper sizing for the transistors was implemented to address this trade-off. The design considerations mentioned above and the biasing technique approach allow us to considerably lower the noise corner frequency, as well as reduce the thermal noise level, and to implement a low-power low input-referred noise instrumentation amplifier at the ECG signal frequency level.

5.3. Low-Pass Filter and VGA Design

The tunable bandwidth low-pass filter controls the upper corner frequency of the AFE and adjusts the input voltage swing at the input of the VGA to prevent any distortion or clipping of the AFE's output signal. A multiple feedback topology is employed for the differential second-order LPF, which offers an increased dynamic range in the output, as shown in Figure 5.6. The gain of the filter is set by the ratio of the pseudo-resistors R_1 and R_3, and the upper cutoff frequency is tuned by the variable pseudo-resistors R_2 with fixed capacitors C_1 and C_2. The employed architecture has the advantage of having separate controls over bandwidth and gain. A 5-bit voltage mode resistive DAC is used to program the cutoff frequency of the LPF. The use of variable pseudo-resistors for gain and bandwidth tuning, instead of capacitor arrays, has the advantage of minimizing the area, which is one of the key factors in energy-harvesting signal acquisition devices.

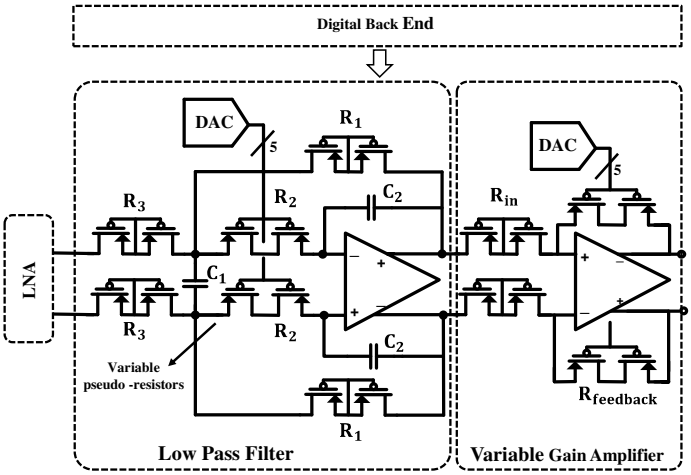


Figure 5.6. Circuit implementation of the low-pass filter (LPF) and variable gain amplifier (VGA).

As the last stage of the amplifier, the VGA provides sufficient gain for the maximum voltage swing. Similar to the LPF, the gain of the VGA is defined by the ratio of resistors $R_{feedback}$ and R_{in} and is tuned by varying the value of the pseudo-resistors in the feedback path by adjusting

the control voltage values applied to the gate of the transistors. The variable pseudo-resistors are controlled by a 5b voltage DAC that is programmed by the digital back-end. The circuit implementation of the VGA is shown in Figure 5.6.

5.4. Experimental Results

5.4.1. AFE Performance Measurements

The prototype was fabricated in a 130 nm CMOS process, and the AFE core blocks, not including the I/O pads, occupy an area of 0.24 mm^2. Figure 5.7 shows the die micrograph of the AFE chip.

The LNA–VGA chain consumes 53 nW of power and delivers a variable gain of 31–52 dB. The measured gain and bandwidth of the AFE are presented in Figure 5.8. All the measurements were done at room temperature with a measured ±2 dB gain variation in the 0–40 °C range. The AFE offers a digitally tunable bandwidth control, where the lower corner frequency is set by the LNA and varies from 0.5 to 5 Hz. The upper corner frequency is adjusted to meet the

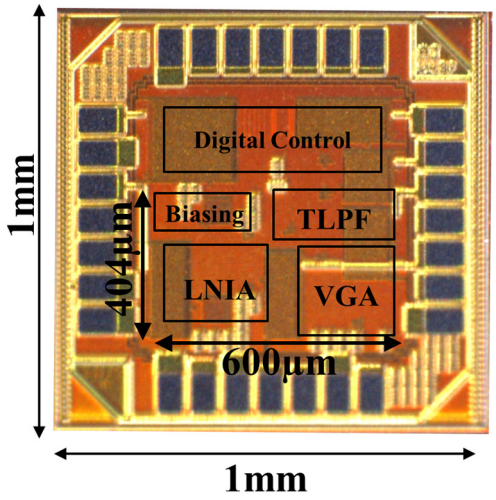
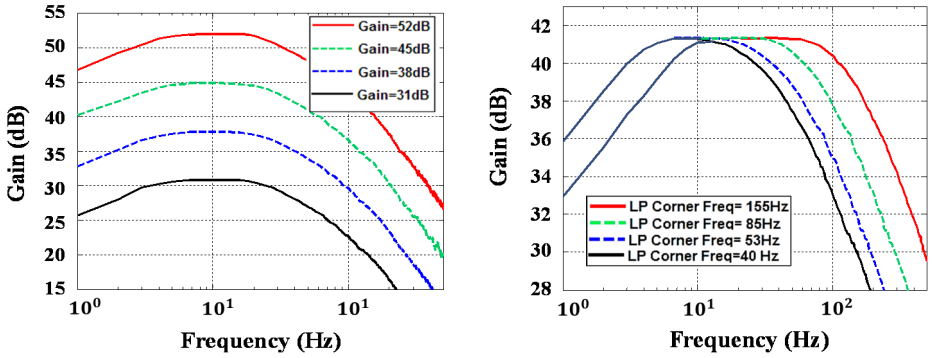


Figure 5.7. Chip die micrograph

ECG signal monitoring requirements. Most of the diagnostic information in ECG signals is contained below 100 Hz [5.22], and the AFE is designed to satisfy this requirement with a tunable bandwidth up to 155 Hz at the maximum gain. For applications with higher frequency contents, such as ECG signals for infants, the bandwidth can further be increased by sacrificing the gain of the VGA stage with a constant gain–bandwidth product. For example, for a tunable bandwidth of



(a) (b)

Figure 5.8. Measured frequency response of the AFE. (a) gain tuning, (b) bandwidth tuning.

up to 250 Hz, the AFE can provide a gain of 39 dB.

Figure 5.9 shows the measured input-referred noise density of the amplifier. The measurements show a good matching to the expected performance, confirming the power-efficient low-noise design techniques of the AFE. The AFE has a measured RMS input-referred noise of 2.8 μV over a 155 Hz bandwidth and has an input-referred noise density of 200nV/√Hz at 155 Hz. The circuit exhibits a noise efficiency factor (NEF) of 2.78, which is well in range with other state-of-the-art AFEs. This work realized a PEF ($NEF^2 x V_{DD}$) of 3.9, while maintaining a balanced power consumption–input-referred noise trade-off. As shown in Figure 5.1, the proposed AFE has the lowest input-referred noise per square root of bandwidth compared to the sub-100nW state-of-the-art AFEs. The measured CMRR and PSRR exceed 60 dB and 70 dB over the bandwidth of the

AFE. Total harmonic distortion (THD) is measured in the low-gain setting of the AFE. The THD stays below 1% for inputs less than 2.5 mV peak–peak. Table 5.1 summarizes the measured performance of the AFE and presents a comparison between this work and the state-of-the-art AFEs [5.6–5.8,5.10,5.18].

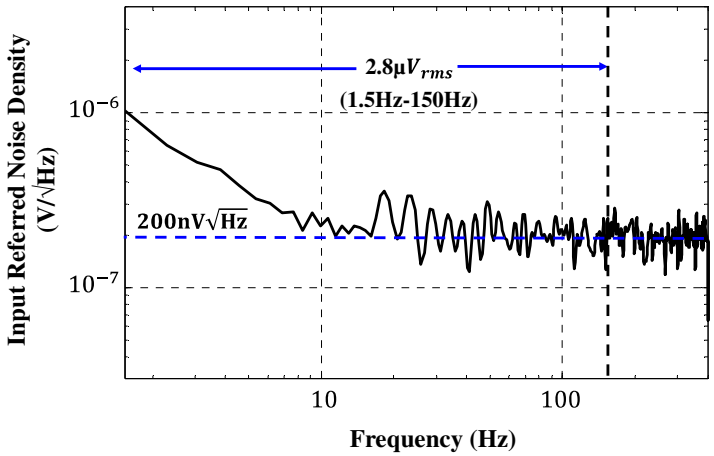


Figure 5.9**.** Measurement input-referred noise density of the analog front-end.

	This Work	**[6]**	**[7]**	**[8]**	**[10]**	**[18]**
Technology (nm)	130	65	180	180	130	350
V_{DD} (V)	0.5	0.5	1	1.8	1.2	2.5
Area (mm^2)	0.24	0.013	0.25	-	0.4	0.17
Blocks in comparison	AFE	AFE, ADC	AFE	AFE	AFE	AFE
Power (nW)	68	5040	266	8250 *	5300	82.5
Gain (dB)	31–52	32	42–51	52–80	45–71	40.7
HP corner Freq. (Hz)	0.5	1	1	0.07	1	0.05
LP corner Freq. (Hz)	40–250	300–10,000	500	30-100	100	100
Input Referred Noise (μV_{rm})	2.8 [1.5–155 Hz]	4.9 [300 Hz–10 kHz]	1.54 [1–500 Hz]	0.91 [0.5–100 Hz]	0.45 [1–100 Hz]	2.8 [0.05–100 Hz]
Input Impedance (MΩ)	115	N/A	N/A	>500	>100	N/A
NEF	2.78	5.99	1.38	5.12	3.7	1.96
PEF	3.9	17.96	1.9	47*	16.4	9.6
CMRR (dB)	62	75	89	>90	>95	>70

* This value is calculated based on the reported performance.

Table 5.1. Performance summary and comparison with the state-of-the-art biopotential AFEs.

5.4.2. Arrhythmia Diagnosis

The AFE is also integrated on an energy-harvesting continuous monitoring SoC [5.2, 5.23], and the SoC is used to perform human ECG signal acquisition in a real-world scenario. In the SoC, the AFE is directly coupled to an integrated single-ended 12-bit SAR ADC. When enabled, the ADC uses the clock generated on the SoC to provide 12-bit parallel output every 16 clock cycles. The combined power consumption of the integrated AFE and ADC is 301 nW at 0.5 V. The input impedance of the AFE is measured at 115 MΩ, which is sufficient for our measurements of ECG signal acquisition. In this measurement setup, we have used the commercial, 3M 2560 Red Dot, electrodes to successfully capture ECG data from a human subject.

The digitized ECG signals were processed and analyzed off-chip using heart rate extraction algorithms. The R-R extraction algorithm is based on the popular Pan–Tomkins algorithm [5.24]. The algorithm uses an initial 4 s time frame to estimate the DC baseline value for the ECG waveform, and through thresholding and time windowing, extracts the ECG R-peaks. Desired accuracy can be achieved by adjusting the sampling rate in the algorithm. Figure 5.10 shows the measured R-R interval for the ECG signal calculated by the R-R extraction algorithm, with a

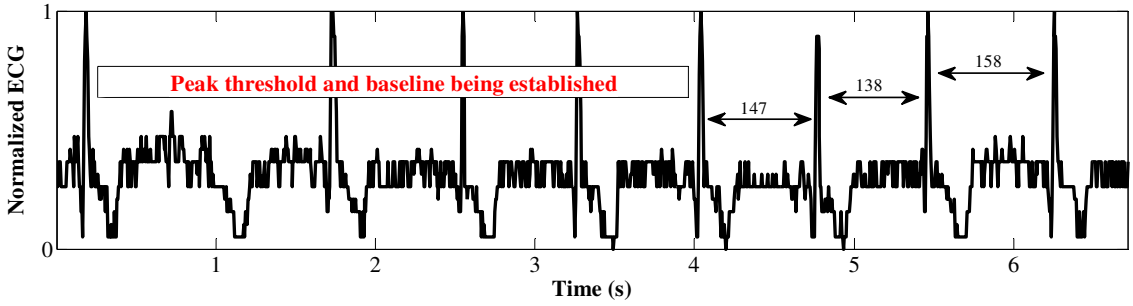


Figure 5.10. Measured electrocardiogram (ECG) results for an R-R extraction algorithm. The measured results are for the acquired ECG data through the AFE integrated on the SoC.

sampling rate of 200 Hz. The annotated numbers represent the number of samples between consecutive peaks.

The performance of the AFE was also demoed using wearable ECG electrodes in [5.25]. The AFE which is integrated in a battery-less physiological SoC, was succesfully used to capture ECG signals using wet electrodes and dry wearable electrodes. The measured ECG signals from a human subject with wearable dry ECG eclectrodes (ECG wearable shirt) is shown in Figure 5.11.

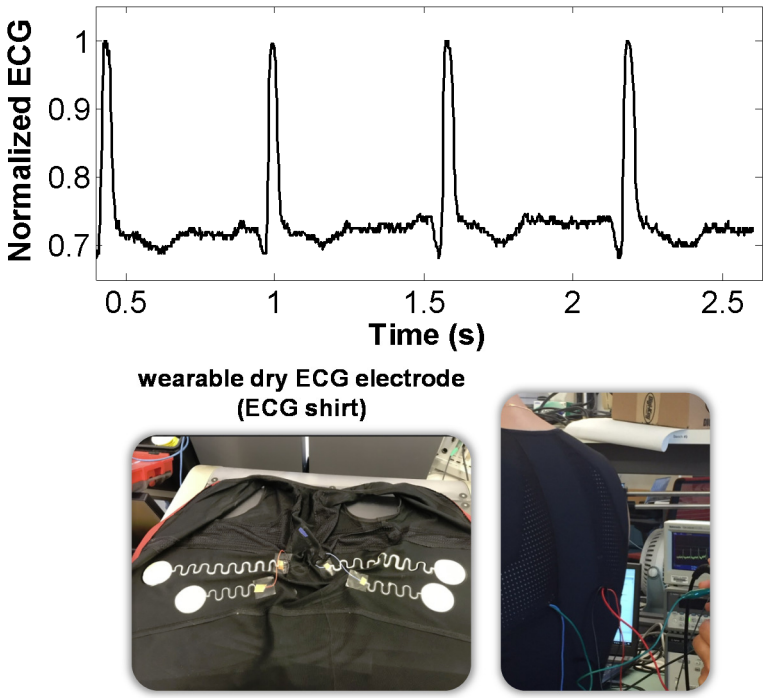


Figure 5.11. Measured ECG results using dry wearable electrodes. The measured results are for the acquired ECG data through the AFE integrated on the SoC.

5.5. Summary

An ultralow power ECG AFE with a balanced noise and power performance is presented in this chapter. The AFE provides bio-signal monitoring with programmable gain and bandwidth, amplifying ECG signals as low as a few microvolts while consuming <100 nW. To realize a high-noise and -power efficiency, a weak inversion biasing technique was used together with other low-

noise design techniques. The proposed AFE has a power consumption of only 68 nW operating at 0.5 V supply voltage. The AFE provides a variable gain of 31–52 dB with NEF and PEF of 2.78 and 3.9, respectively. It was fabricated in a 130 nm CMOS technology and occupies an area of 0.24 mm^2. Arrhythmia diagnosis algorithms were implemented and the feasibility of the AFE performance for energy-harvesting applications was validated by integrating it on a battery-less SoC and successfully performing human ECG signal acquisition with an R-R extraction algorithm.

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Chapter 6
Concluding Remarks

6.1 Summary of Contributions

The focus of this thesis has been to develop circuit and system techniques in order to bridge the gap between power consumption and performance in WSNs. In support of long-range communication WSNs, such as LPWANs, we developed a low power transmission link architecture in the MURS frequency band that can be used as an alternative solution for LPWAN applications. We showed the feasibility of such transmission link by an integrated receiver and a transmitter chip as well as experimental channel characterizations in the MURS band.

This thesis presents an agile modulation approach at the low VHF frequency of MURS band, where data rate values of 5-384 kb/s can be achieved over km-range distances. A link budget analysis showing km-range coverage area in the MURS band was performed while proposing ultra-low power consumptions for the RF blocks such as the wireless sensor node receiver and transmitter.

One of the major contributions of this dissertation is the development of an ultra-low power receiver capable of long-ranges of communications. The receiver uses efficient system-level and low power design techniques, such as injection locking, edge combining passive mixer first topology, two step down conversion, etc. It achieves -99dBm sensitivity with 152μW of power at 5kb/s and a 63dB blocker rejection at 10MHz offset. The ILRO, which is locked to a stable 50MHz

crystal reference, achieves a PN of -128dBc/Hz at 1MHz offset. In terms of sensitivity versus power consumption tradeoff, this radio shows the lowest power consumption compared to the state-of-the-art receivers with better than -90dBm sensitivity values.

Another major contribution of this dissertation is the development of a low power digital transmitter capable of km-range communications. By using the method of class-B I/Q cell sharing introduced in this work, we were able to improve the theoretical efficiency of our digital TX architecture compared to conventional quadrature DTX architectures. The transmitter efficiency is enhanced by employing the digital class-B input codeword profile in combination with the time division multiplexing of the quadrature data and it delivers a peak efficiency of 41% at a peak output power of 0dBm.

Finally an ultralow power ECG AFE with a balanced noise and power performance is presented in this dissertation. Since AFEs are amongst the power hungry blocks in WSNs readout circuits, designing a power efficient AFE while achieving sufficient performance is of crucial importance. The AFE in this work provides bio-signal monitoring with programmable gain and bandwidth, amplifying ECG signals as low as a few microvolts while consuming <100 nW. Arrhythmia diagnosis algorithms were implemented and the feasibility of the AFE performance for energy-harvesting applications was validated by integrating it on a battery-less SoC and successfully performing human ECG signal acquisition from human subjects with an R-R extraction algorithm.

6.2 Future Directions

In the design of the low power MURS band digital transmitter, we have used numerous techniques in order to improve the efficiency and reduce the power consumption. In order to improve the efficiency of large PAPR signals, such as the 16QAM OFDM modulated signals

considered for the MURS band, external linearization circuitry can be used to reduce the DC power consumption of the DTX at lower output powers. One solution and a future work for the DTX in this work is to include a linearization technique such as the technique used in class-G power amplifiers. In this method multiple power supply voltages are used in a way that lower V_{DD} values are used to generate lower output transmit power. This leads to lower DC power consumption and therefore higher efficiency. For the class-B I/Q cell sharing discussed in this thesis, the method of class-G linearization can be used and optimal supply voltages can be selected based on the digital code word in the digital domain.

In this work separate RX and TX chips were fabricated in order to show the low power long-range performance in the MURS frequency band. One future work on the overall system is to develop and fabricate a single transceiver chip in the MURS band using a single reference clock frequency for LO generation to further reduce the power consumption and demonstration of the long-range performance in this band.